Energy Harvesting Circuit with Input Matching in Boundary Conduction Mode for Electromagnetic Generators

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ABSTRACT

The proposed circuit intends to harvest kinetic energy from ElectroMagnetic Generators (EMGs). In order to extract maximum power from an EMG, an AC-DC boost rectifier is designed to match the impedance of the EMG. Rather than operate a buck-boost converter in Discontinuous Conduction Mode (DCM) in other impedance matching cases, the proposed method is running the boost topology in Boundary Conduction Mode (BCM). So it would perform resistive input matching, while reducing the converter power loss. The boost rectifier also merges a rectifier and a boost converter to reduce power loss for rectification. It also utilizes the internal inductance of the EMG to eliminate the impedance matching error and reduce the off-chip inductor size. An optional buck converter regulates the output voltage to 5 V to power devices through USB ports.

The proposed circuit is designed and fabricated in BiCMOS 0.18 μm technology. Its functionality is shown through simulation results. The measurement of the IC is also performed. However, since the IC only work partially, test result is gathered using some discrete components as substitutes. It indicates the circuit can realize the proposed control method.

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GENERAL AUDIENCE ABSTRACT

The development of energy-efficient semiconductor devices has reduced the power requirements of electronic circuits. As the electronics' scale decreases, so does the energy consumption. In this sense, batteries were also produced in smaller size providing more energy storage availability. However, due to technical and technological issues, the batteries have not been followed by the same evolutionary trend limiting the operational time and performance of portable devices as it need to be recharged or replaced periodically. On the other hand, portable electronic devices such as cell phones, GPS, cameras, etc. are powered only by batteries. For circumstances that power supplies are not accessible, energy harvesting (EH) from human or environmental sources has proven to be an effective alternative or complement.

Light, thermal, mechanical and RF are major sources in EH. Among them, mechanical energy from wind, waves, vibrations, etc. is commonly existed in our daily life. The energy is harvested by using micro generators and the various types include electromagnetic, piezoelectric and electrostatic. In particular, the ElectroMagnetic Generator (EMG) is of great interest for its potentially high energy density and efficiency.

Since EMG is an AC voltage generator while portable devices usually require a stable DC supply, an EH circuit as a rectifier ought to be designed. At the same time, for EH application, we would like to harvest as much power as possible from EMGs. This research project addresses the development of a unique EH circuit capable of fulfilling the distinct needs illustrated above.

To my parents and grandparents

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Chapter 1

Introduction

1.1 Motivation

The development of energy-efficient semiconductor devices has reduced the power requirements of electronic circuits. As the electronics' scale decreases, so does the energy consumption. In this sense, batteries were also produced in smaller size providing more energy storage availability. However, due to technical and technological issues, the batteries have not been followed by the same evolutionary trend limiting the operational time and performance of portable devices as it need to be recharged or replaced periodically. On the other hand, portable electronic devices such as cell phones, GPS, cameras, etc. are powered only by batteries. For circumstances that power supplies are not accessible, energy harvesting from human or environmental sources has proven to be an effective alternative or complement.

From a broader perspective, the systems for energy harvesting may be based on several sources, like the light energy, thermal energy, mechanical energy and RF energy. The energy is harvested from the ambient environment and transferred to power by using energy harvesters, then converted to usable power by Energy Harvesting (EH) circuits, and then regulated to stable outputs by power management circuits. The diagram of an energy harvesting system is shown in Figure 1.1. The energy harvesters convert different kinds of energies into power. The EH circuit adopts maximum power transfer theory to ensure the maximum power is harvested. This power can be stored into devices such as batteries and super capacitors in some applications. For cases like charging portable devices, the power management circuit is designed to provide stable voltage to the load.

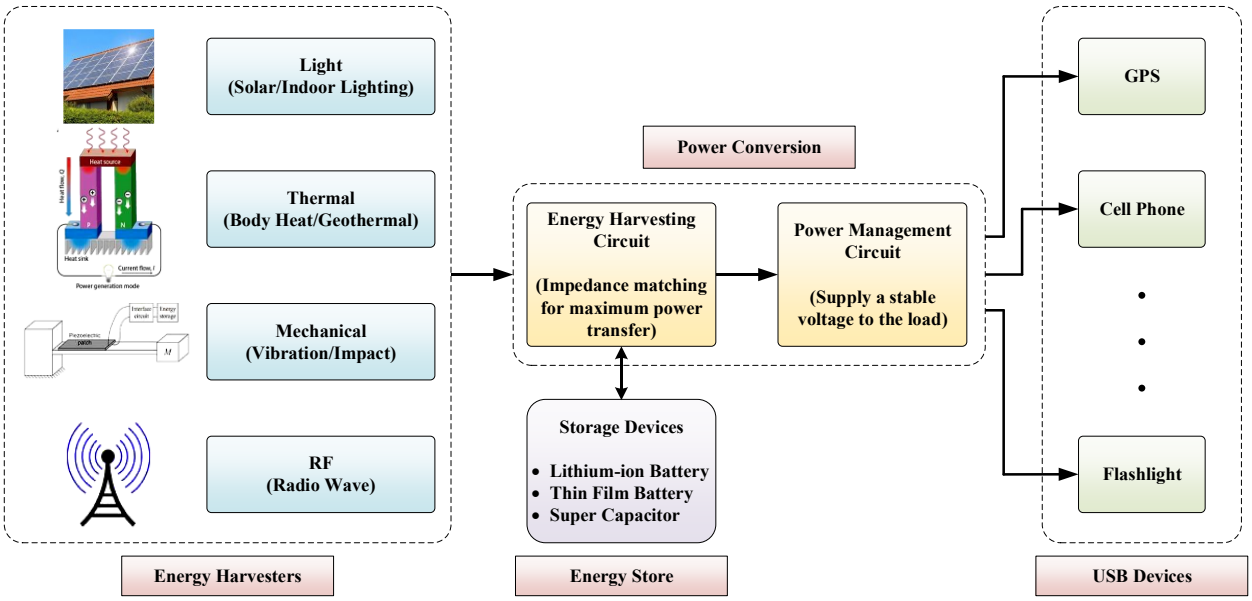


Figure 1.1 Energy harvesting system

Light, thermal, mechanical and RF are major sources in EH. Among them, mechanical energy from wind, waves, vibrations, etc. is commonly existed in our daily life. The energy is harvested by using micro generators and the various types include electromagnetic, piezoelectric and electrostatic. In particular, the ElectroMagnetic Generator (EMG) is of great interest for its potentially high energy density and efficiency.

Since EMG is an AC voltage generator while portable devices usually require a stable DC supply, an EH circuit as a rectifier ought to be designed. At the same time, for EH application, we would like to harvest as much power as possible from EMGs. This research project addresses the development of a unique EH circuit capable of fulfilling the distinct needs illustrated above.

1.2 Scope of the Proposed Research

The EMG generates low amplitude AC voltage for typical energy harvesting applications. Thus this voltage need to be rectified and boosted to be stored or used. Traditional passive rectifier would cause high power loss because of its forward voltage drop. Moreover, with a boost converter following after the full-bridge rectifier, the lower voltage and thus higher current on the input side of the boost converter would cause the combined circuit less efficiency. [1] uses an active rectifier to reduce the voltage drop on the rectifier and thus lower power loss. [2]-[4] propose several single

stage boost rectifiers which merge the rectifier and boost converter in one stage operating in Discontinuous Conduction Mode (DCM) to depress the dissipation.

Another issue of EH circuit design for EMG is that we would like to extract maximum power from the EMG. The maximum power transfer theorem indicates that we can achieve maximum power by impedance matching. A buck-boost converter operating in DCM is commonly used for impedance matching, but the RMS current is larger than its counterpart boost converter which would cause higher conduction loss. However, the input impedance of a boost converter in DCM depends on the input and output voltages, which results in less accurate matching and/or a more complex circuit.

This study aims to implement a simple control scheme which would allow the single stage boost rectifier to match the impedance of the EMG and thus fulfill not only rectification and voltage boost, but also impedance matching.

1.3 Proposed Approach and Technical Contributions

An EH circuit targeted for energy harvesting from an EMG to supply an USB host is designed and taped out. The major design objectives of the circuit is to extract maximum power from the EMG, maintain efficient power conversion, and provide a stable output voltage. Technical contributions of the proposed research are as follows.

The power stage is selected to not only can rectify the AC voltage harvested from the EMG, but also be able to boost the rectified voltage to a higher level. In order to extract maximum power from the EMG, a method of operating the boost rectifier in Boundary Conduction Mode (BCM) is proposed to maintain a constant input impedance. To realize BCM, the point when the current returns to zero ought to be detected. And then the next switching cycle is initiated. Thus the Constant On-Time (COT) control triggered by zero current is adopted.

For the Zero Current Detection (ZCD), normally, there’re four ways to sense the inductor current in the form of voltage, i.e. small resistor sensing, current sensor, transformer sensing, and DCR sensing. But sensing resistor and current sensor are more suitable for power level that is not very low. Transformer need to be carefully designed to fulfill the requirements. DCR sensing can convert the inductor current information to capacitor voltage, but the small DCR makes the

capacitor voltage level low as well. With a low level voltage contains current information, it is difficult to be used to determine the zero current point accurately. For EH circuits, a simpler and more accurate way is desired. Thus a method of using the inductor voltage for ZCD is proposed. And the zero current detector is designed to be able to detect zero current despite of the input polarity.

Some protection circuits are included in the propose design. First, a minimum off timer is designed as part of the COT generator. Second, in order to prevent ZCD failure, a maximum off timer is added in addition to the normal COT generator. Third, the output voltage of the boost rectifier is limited to protect the integrated transistors in the circuit. Last, a stage coordinator is applied to control the operation between the boost rectifier and the buck converter.

The proposed EH circuit except some passive components was designed in Cadence and fabricated in BiCMOS 0.18μm technology with a total area less than $10\mu m^2$. The measurement is done along with passive components on a breadboard. However, since some part of the IC doesn't work, test results are acquired by using some discrete components as the substitutes. The test results indicate that the circuit can realize the proposed control method with external supplies.

1.4 Organization of this Thesis

The organization of the thesis is as follows. Chapter 2 provides background and preliminaries for the proposed research work. This chapter discusses important characteristics about the EMGs which lead to the challenges and possible solutions in the EH circuit design. Some existing topologies are listed, of which the adopted one is explained along with its inadequacies. Then, the BCM is introduced based on Continuous Conduction Mode (CCM) and DCM. Finally, for the design of second-stage DC-DC buck converter, the COT V^2 control is analyzed, and its possible issues are noted. Chapter 3 presents the proposed EH circuit. In this chapter, the method of operating boost rectifier in BCM is proposed for direct impedance matching, followed by the detailed implementation of this method block by block. Then, to complete the EH circuit design, a stage coordinator, which is used to determine enable conditions, and a buck converter with COT control are illustrated. Transistor-level circuit diagrams of references and major components are included. Practical issues such as cold start and internal supply strategies are addressed. Chapter 4 shows the layout and simulated functionality in Cadence. Then the proposed EH circuit, with

nonfunctioning parts replaced by commercial chips and external supplies, is experimented and analyzed. Possible causes of the failed blocks are included as well. Finally, Chapter 5 draws conclusions on the proposed EH circuit design as well as suggesting future improvements.

Chapter 2

Preliminaries

This chapter presents preliminary information about the EMG, previous research activities, BCM, and COT V^2 Control. This introductory knowledge is necessary to understand the design approach taken with the proposed circuit. Section 2.1 illustrates requirements of the EH circuit based on characteristics of EMGs. Section 2.2 introduces the previous approaches of EH circuit design for EMGs. Section 2.3 explains the BCM. Section 2.4 describes the COT V^2 control scheme. Finally, section 2.5 summarizes this chapter.

2.1 Design Requirements

2.1.1 Electromagnetic Generator Characteristics

Energy harvesting with EMGs was investigated rather extensively [2]-[9], and an EMG model shown in Figure 2.1 is commonly used. The EMG model has the series connection of an AC voltage source, an inductor L_S, and a resistor R_S. L_S and R_S account for the inductance and the resistance of the EMG, respectively. The reactance of the inductor $|\omega L_S|$ is typically much smaller than R_S [9]. Thus, L_S is ignored at the beginning of the proposed impedance matching circuit design.

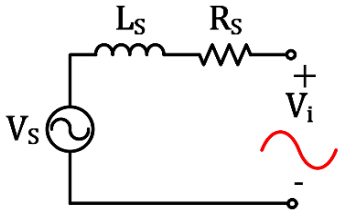


Figure 2.1 EMG Model

2.1.2 Design Challenges & Solution

One challenge of designing EH circuit for EMGs is that EMGs generate low amplitude AC voltage. This voltage needs to be rectified and boosted. The conventional AC-DC boost conversion consists of a full-bridge rectifier and a DC-DC boost converter as shown in Figure 2.2. It is not suitable for EMGs for two main reasons. Firstly, since the AC voltage generated by an EMG has low amplitude, the forward voltage drop in the diode bridge would be difficult to overcome. And secondly, for boost conversion, the current on the input side is higher than that on the output side, which causes more power dissipation on the diode bridge. Based on these reasons, the single stage AC-DC boost conversion which combines the rectifier and a boost converter would be more promising to EMG energy harvesting.

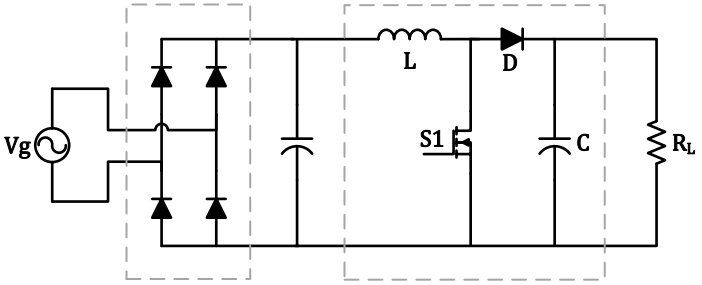


Figure 2.2 Conventional AC-DC boost conversion

Typical single stage AC-DC boost conversion topologies for EMGs are summarized in [10]. Some of them are shown in Figure 2.3. Figure 2.3 (a) shows the topology of a dual-boost rectifier. If the two diodes are replaced with MOSFETs, the topology would change to H-bridge rectifier. Figure 2.3 (b) shows the topology of a totem-pole rectifier. Figure 2.3 (c) shows a parallel boost & buck-boost topology which relies on the boost converter for the positive half cycle and the buck-boost converter for the negative one. Figure 2.3 (d) shows a dual-polarity boost rectifier which is basically two boost converters in parallel to deal with different input polarities. Figure 2.3 (e) shows a secondary side diode topology with two n-type MOSFETs as a bidirectional switch. Figure 2.3 (f) shows a split capacitor topology with a bidirectional switch formed by one NMOS and one PMOS. Among these topologies, dual-boost, H-bridge, totem-pole and secondary side diode topologies are commonly used as boost type Power Factor Correction (PFC) circuits. Their disadvantage is that there are always two switches, including MOSFETs and diodes, in the current conduction path, which generally would cause more power dissipation. Besides, to realize the

control scheme, topologies in Figure 2.3 (a) to (d) would need to detect the input polarity, which increases the complexity of the EH circuit design. Thus the split-capacitor topology shown in Figure 2.3 (f) is adopted as the single stage boost rectifier in this design.

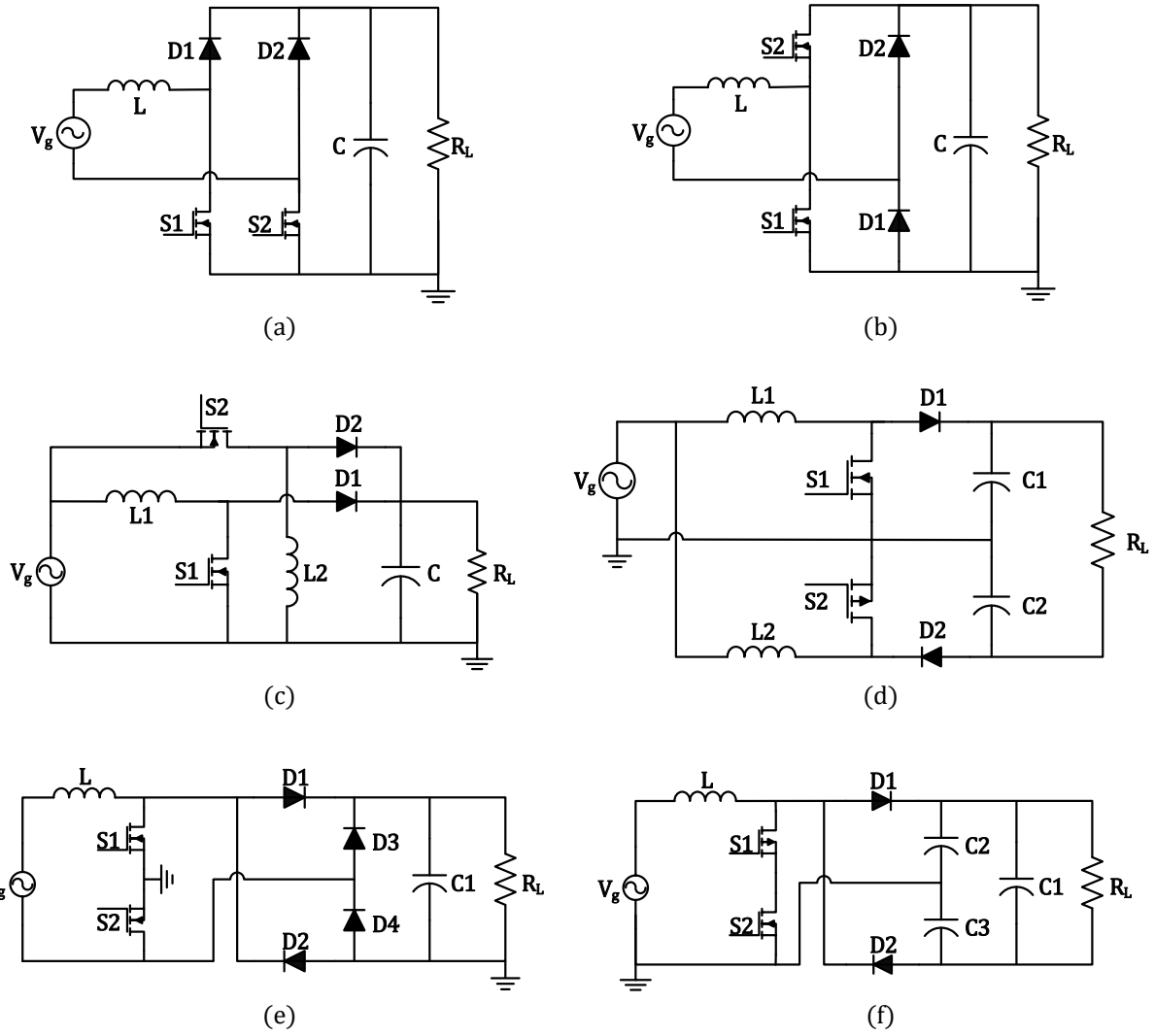


Figure 2.3 Single stage AC-DC boost conversion topologies: (a) dual-boost, (b) totem-pole, (c) parallel boost & buck-boost, (d) dual-polarity, (e) secondary side diode, (f) split-capacitor.

Another challenge of designing EH circuit for EMGs is that we want to extract maximum power from EMG. Maximum Power Transfer Theorem states that a source provides maximum power when load and source impedance are equal. Thus the load resistance of EMG should match the EMG resistance R_S shown in Figure 2.1. In another word, it is desired to have a converter whose input impedance matches the impedance of the EMG directly.

One common method of direct impedance matching is running a buck-boost converter in DCM. If the duty ratio of the buck-boost converter is D, the switching period is T_S and the inductor value is L, then the input impedance of this converter is

$$R_i = \frac{2L}{D^2 T_s} \tag{2.1}$$

which is constant when the circuit is designed and D is fixed. Thus by designing L, D, and T_S, the buck-boost converter can be tuned to emulate a matching resistive load to the source. Then maximum power can be extracted. However, generally, the efficiency of a buck-boost converter is lower than its counterpart boost converter. To deliver the same power to the output, the RMS current on the inductor would be lower for the boost converter and thus less power dissipation on the converter. So if a boost converter can provide the same feature, the boost topology would be preferred.

All in all, the objective of this design for EMG is to develop an AC-DC boost rectifier that emulates a resistive load to match the impedance of EMG while boosting and rectifying the voltage.

2.2 Previous Converter Design Approaches for EMG

2.2.1 Dayal's Direct AC–DC Boost Converter

Dayal etc. proposed a boost rectifier based on a split-capacitor topology shown in Figure 2.4 [11], and the circuit topology is adopted for the proposed circuit. The boost rectifier is composed of an inductor L, a pair of PMOS and NMOS switch, two diodes D1, D2, and capacitors C1 ~ C3.

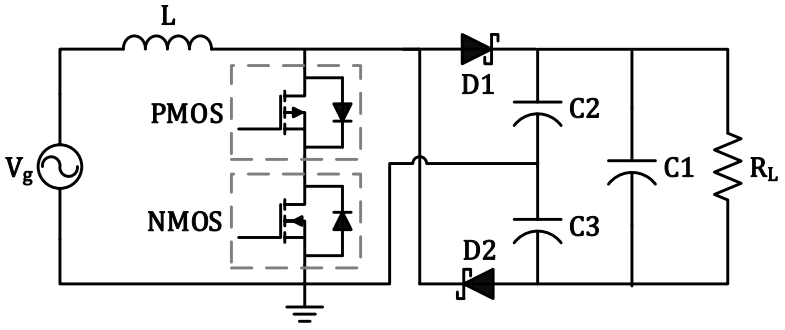


Figure 2.4 Circuit schematic proposed by Dayal

The PMOS and NMOS pair forms a bidirectional switch. They are turned on and off at the same time. They're both off when the gate voltages are 0. When the gate of NMOS is charged to 3V (above threshold), the NMOS is turned on, then the source terminal of PMOS is connected to ground through the conducting NMOS. Meanwhile, the PMOS gate drops to -3V, thus the gate-to-source voltage exceeds the PMOS threshold, PMOS is also turned on. Because of the existence of body diodes in power MOSFETs, the circuit relies on the NMOS to block during the positive half cycle and relies on the PMOS to block during the negative half cycle. The operation of this circuit is shown in Figure 2.5. During the positive half cycle, when MOSFETs are on, the inductor L is charged. When MOSFETs are off, the capacitor C2 is charged. The current paths are shown in Figure 2.5 (a) and (b) respectively. During the negative half cycle, when MOSFETs are on, the inductor L is charged reversely. When MOSFETs are off, the capacitor C3 is charged. The current paths are shown in Figure 2.5 (c) and (d) respectively. C1 has a voltage equals to the sum up of the voltages on C2 and C3. C1, C2, and C3 share energy through charge recycling. Although the voltage ripple of C2 and C3 are relatively high because of the charging process, the output voltage on C1 can remain relatively stable with a small ripple[11].

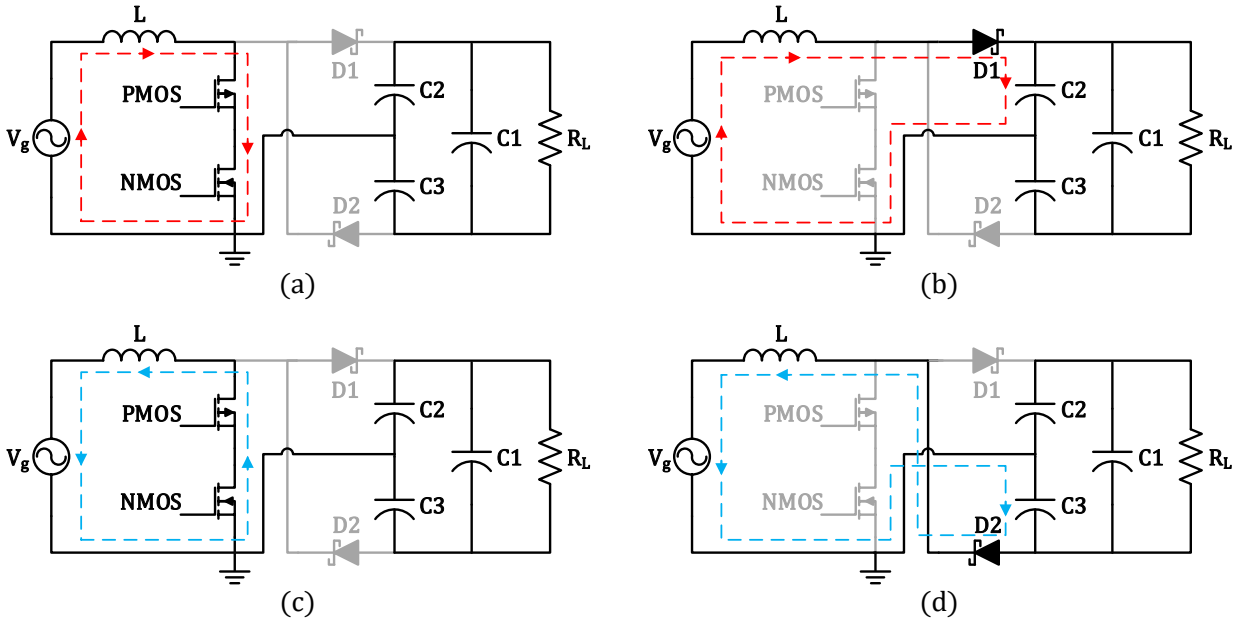


Figure 2.5 Circuit operation: (a) MOSFETs on during positive half cycle, (b) MOSFETs off during positive half cycle, (c) MOSFETs on during negative half cycle, (d) MOSFETs off during negative half cycle

In Dayal's design, the circuit was proposed to run in DCM. Since the switching frequency is much higher than the source frequency, the input voltage can be seen as a constant value within one switching cycle. Then the circuit can be analyzed as a DC/DC boost converter. Operating in DCM, the average input impedance of the boost converter and thus the boost rectifier can be derived to be

$$R_{in} = \frac{2L}{D^2 T_s}\left[1 - \frac{V_g(t)}{V_o(t)}\right] \tag{2.2}$$

The output voltage is regulated to be 3.3V by changing the duty ratio D. Meanwhile, V_g and V_o changes in different switching cycles. All these ends up with a changing input impedance of the boost rectifier in DCM. Even the duty ratio D can be fixed, we still need high conversion ratio $M = \frac{V_o}{V_g}$ to make R_{in} more constant.

2.3 Boundary Conduction Mode

For power converters, there are two common operation modes, CCM and DCM. CCM operation refers to a power converter which does not let the inductor current reach zero during a single switching cycle. Conversely, DCM operation refers to a power converter where the inductor current always returns to zero and stays at zero for a while during a switching cycle. The inductor current waveforms of CCM and DCM are shown in Figure 2.6 (a) and (b) respectively. The crossover point between these modes is referred to as the critical boundary, and operating under this condition is referred to as BCM or Critical conduction Mode (CrM). In BCM, the new switching period is initiated when the inductor current returns to zero. The inductor current waveform of the BCM is shown in Figure 2.6 (c).

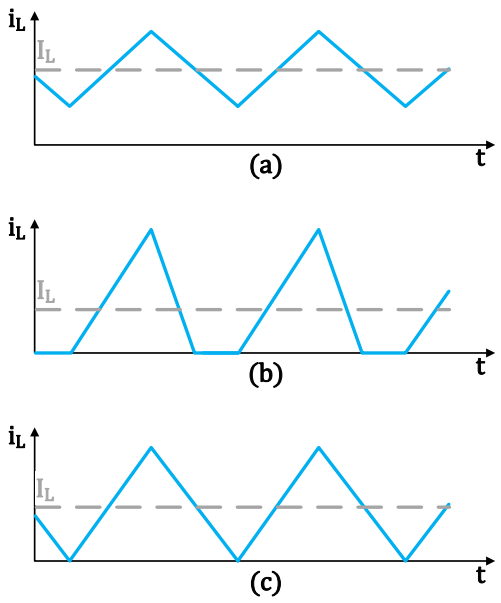


Figure 2.6 Power converter inductor current waveforms (a) during CCM operation, (b) during DCM operation, and (c) during BCM operation.

In general, DCM and BCM would have zero current when turning on the MOSFET, thus the turn-on loss of operating the power converter in DCM or BCM would be lower.

2.4 Constant On-time V^2 Control

For COT control, the switch is on for a designated period, the off-time is modulated. For voltage regulation, COT control tracks the valley voltage value. Once the detected value is below the threshold, a COT pulse is generated to turn on the switch for the designated period.

The concept of COT V^2 control is illustrated in Figure 2.7. There are two parallel voltage feedback loops; hence, the name V^2 control.

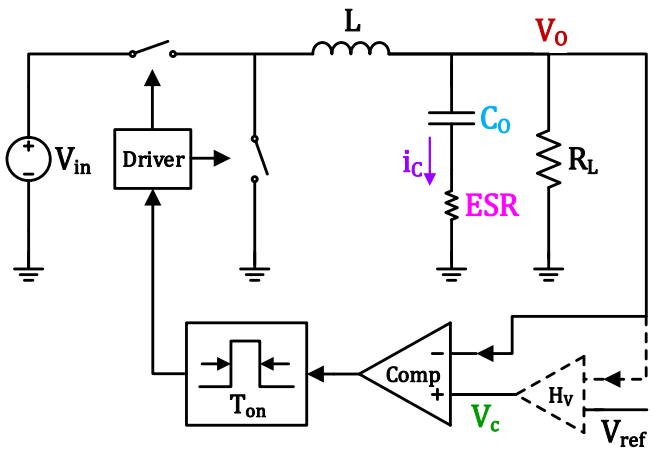


Figure 2.7 Schematic of COT V^2 control

The inner loop is the current loop. It captures the inductor current information through sensing the output voltage. This loop is fast and ensures rapid correction of transient perturbations. In the current loop, the output voltage is the sum of voltages across the output capacitor C_O and its Equivalent Series Resistance (ESR). As indicated in Figure 2.8, the C_O voltage stays nearly constant which represents the DC output voltage. The capacitor ESR voltage ripple is generated by the inductor current ripple. Thus the current loop relies on the ESR voltage ripple to acquire inductor current information. Considering the output voltage ripple, it is critical to design the output capacitor to ensure the ESR ripple dominates the capacitor ripple. So output capacitor with relatively big ESR should be used in the design.

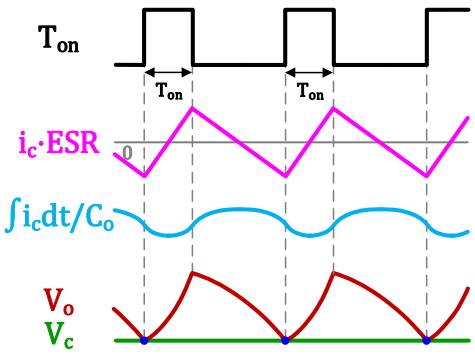


Figure 2.8 Key waveforms of COT V^2 control

The outer loop is the voltage loop. It sends the output voltage through a compensation network to generate the error information. The voltage loop is slow and ensures that the dc

component of the output voltage accurately follows the reference voltage. The primary purpose of the outer loop is to eliminate the steady state error which equals to half of the output voltage ripple. For applications where the steady state error is not critical, the outer loop can be omitted as described in [12].

Since the output voltage is directly connected to the controller through the inner current loop, when the output voltage changes due to the disturbance either from the input voltage or the load variations, the controller would respond immediately. Thus COT V^2 control has fast load transient response.

Another advantage of COT V^2 control is that it requires only a comparator for feedback loop rather than an oscillator, a comparator and a compensator required for conventional PWM control. Thus, COT V^2 control is easy to implement and can save many building blocks.

Although V^2 control has several advantages, V^2 control may suffer from sub-harmonic instability. One possible reason is small ESR of output capacitor[13]. When the ESR is small, its voltage ripple won't be able to dominate the output ripple anymore and thus can't be used to sense the inductor current. The other reason is big duty ratio when operating in CCM. V^2 controlled buck converter is stable in CCM when the duty ratio is less than 0.5 and in DCM for the whole range of duty ratio. When the duty ratio is larger than 0.5, sub-harmonic oscillation of V^2 controlled buck converter operating in CCM would need slope compensation to be eliminated [14].

2.5 Chapter Summary

Previous research activities related to the proposed work are reviewed in this chapter. The challenges and possible solutions are analyzed based on the design objectives of the EH circuit for EMGs. Dayal's direct AC–DC boost converter for EMG is investigated. Its operation is shown and its shortcoming is illustrated. Then, BCM, which is adopted in the proposed design, is explained along with CCM and DCM. At last, COT control is explored. The COT V^2 control is discussed including its advantages and possible issues. The primary goal of this research work is to develop an AC-DC boost rectifier can not only boost and rectify the voltage but also emulate a resistive load to match the impedance of the EMG.

Chapter 3

Proposed Energy Harvesting Circuit

The proposed energy harvesting circuit for EMG should satisfy several requirements. The first requirement is that the circuit should convert the low AC voltage generated by an EMG to a higher DC voltage. Thus an AC-DC boost rectifier is adopted in the circuit. The second requirement is that the circuit should emulate a constant resistance for maximum power transfer. It is achieved by adopting the BCM to operate the rectifier in the proposed circuit. The third requirement is that the output should be able to provide a regulated voltage, thus a voltage regulator is designed after the rectifier.

This chapter describes the proposed impedance matching method and the design of the energy harvesting system to fulfill the requirements. Section 3.1 specifies the design requirements. Section 3.2 introduces the method proposed to emulate the circuit as a resistor so as to perform direct impedance matching. Section 3.3 explains the detailed implementation of the proposed method. Section 3.4 illustrates the energy harvesting system designed for the EMG. Practical questions such as start-up and internal supply strategies are discussed. Section 3.5 summarizes the chapter.

3.1 Specification of the Proposed Converter

The target specifications of the proposed circuit are shown in Table 1. The EMG can generate an AC voltage with amplitude varies between 0.3V to 3V and frequency up to 700Hz. The proposed converter is designed to harvest energy generated by this EMG and then supply an USB port. Thus the output of the circuit is supposed to be a regulated 5V DC voltage.

Table 1: Target Specifications for the Proposed EH Circuit

Input (AC)	Min.	Typ.	Max.

Amplitude (V)	0.3	-	3
Frequency (Hz)	-	-	600 ~ 700
Power (W)	-	-	1
Output (DC)	Min.	Typ.	Max.
Voltage (V)	-	5	-

3.2 Proposed Direct Impedance Matching Method

To achieve impedance matching while rectifying and boosting the AC voltage from EMG, the method of operating the boost rectifier in BCM with COT control is proposed. The ideal operation waveforms are shown in Figure 3.1.

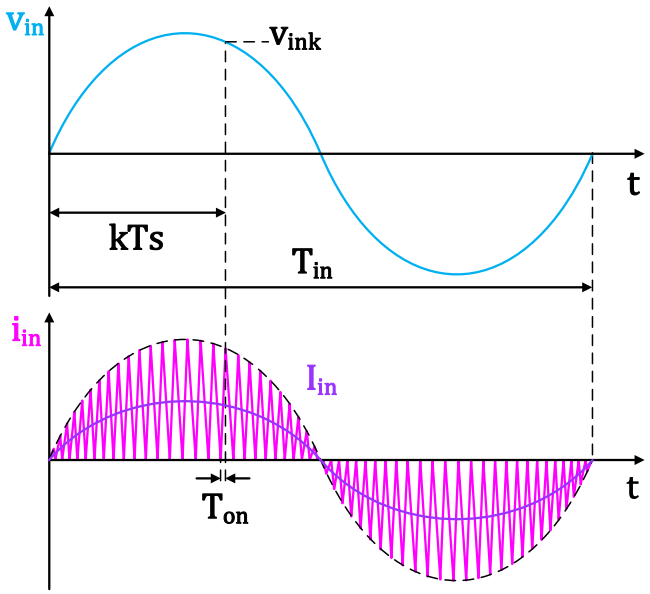


Figure 3.1 Ideal operation waveforms of the proposed circuit

Since the switching frequency f_s is much higher than the source frequency f, and the operation of for positive and negative input are identical, in the k_{th} switching cycle, the rectifier in Figure 2.4 can be seen as a DC-DC boost converter as shown in Figure 3.2. The ideal waveforms of its k_{th} cycle are shown in Figure 3.3.

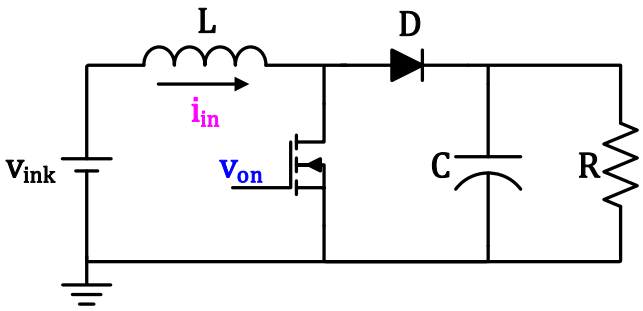


Figure 3.2 Equivalent circuit for k_{th} cycle of the boost rectifier

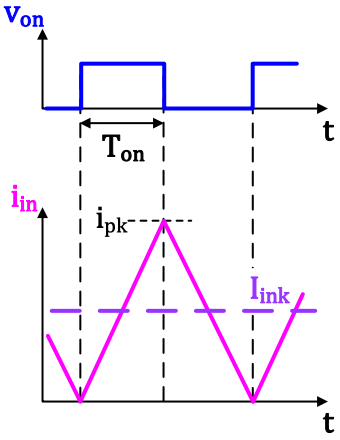


Figure 3.3 Ideal waveforms of the k_{th} cycle

With COT control, the peak current in the k_{th} switching cycle is

$$i_{pk} = \frac{V_{ink}}{L} \cdot T_{on} \tag{3.1}$$

As in BCM, the input current has a triangular waveform, so the average current of this cycle is

$$I_{ink} = \frac{i_{pk}}{2} = \frac{V_{ink} T_{on}}{2L} \tag{3.2}$$

Thus the emulated input impedance of the rectifier is

$$R_{in} = \frac{V_{ink}}{I_{ink}} = \frac{2L}{T_{on}} \tag{3.3}$$

which is constant as long as L and T_{on} are designed.

Comparing with R_{in} of boost converter working in DCM as in equation (2.2), BCM makes R_{in} independent of conversion ratio

3.3 Implementation of the Proposed Method

To implement the method, a block diagram is shown in Figure 3.4. Besides the boost rectifier power stage， it's consists of a zero current detector, a constant on-time generator, level shifter, and driver. For COT control in BCM, the next turn-on is initiated when the inductor current returns to zero. Thus zero current detector is necessary in order to detect the point when the inductor current becomes zero and generates a trigger signal. The trigger signal then initiates the COT generator to generate a pulse with a fixed on-time T_{on}. Level shifter and driver are connected to the COT generator to drive the power MOSFETs in the power stage with the correct voltage level. The implementation of each block is explained in this section.

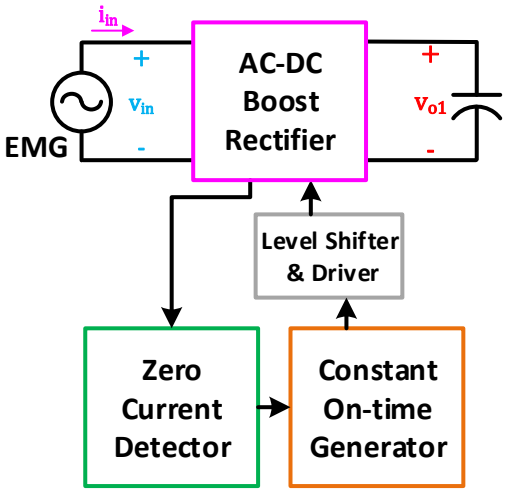


Figure 3.4 Block diagram of the proposed circuit

3.3.1 Zero Current Detector

The proposed implementation of ZCD is shown in Figure 3.5 along with the boost rectifier.

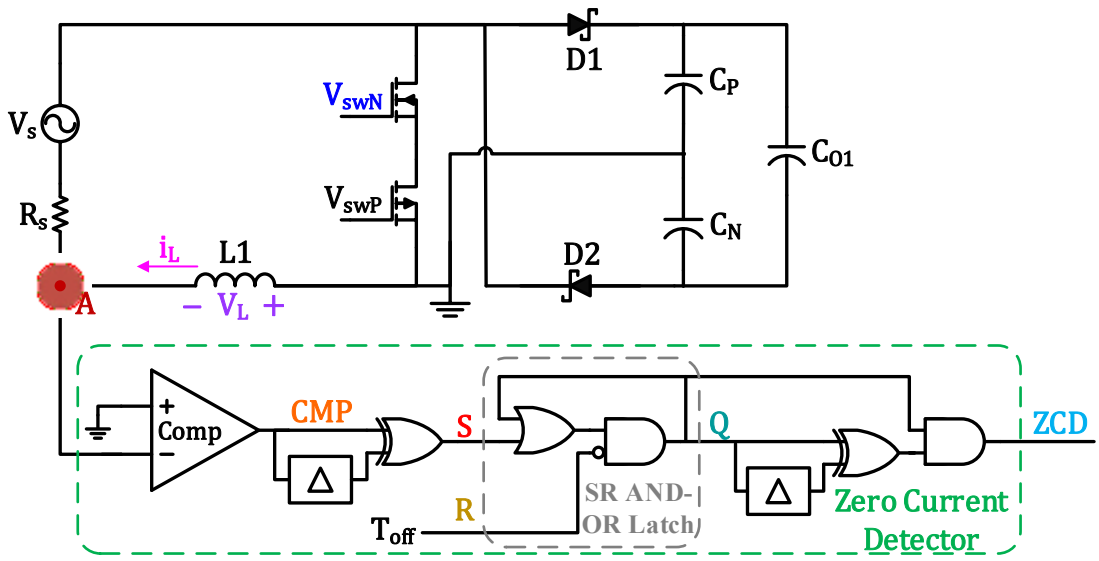


Figure 3.5 Proposed implementation of ZCD

Comparing with the original circuit shown in in Figure 2.4, the boost rectifier power stage in Figure 3.5 moves the inductor L1 from the upper side to the bottom side. In this way, one terminal of the inductor L1 is grounded, which allows the ZCD to sense the ground referenced voltage at node A as v_A. Since $v_A = -v_L$, inductor voltage information can be sensed only at one terminal rather than two terminals for the original circuit in Figure 2.4. Figure 3.6 shows waveforms and timing of relevant signals for an ideal ZCD circuit.

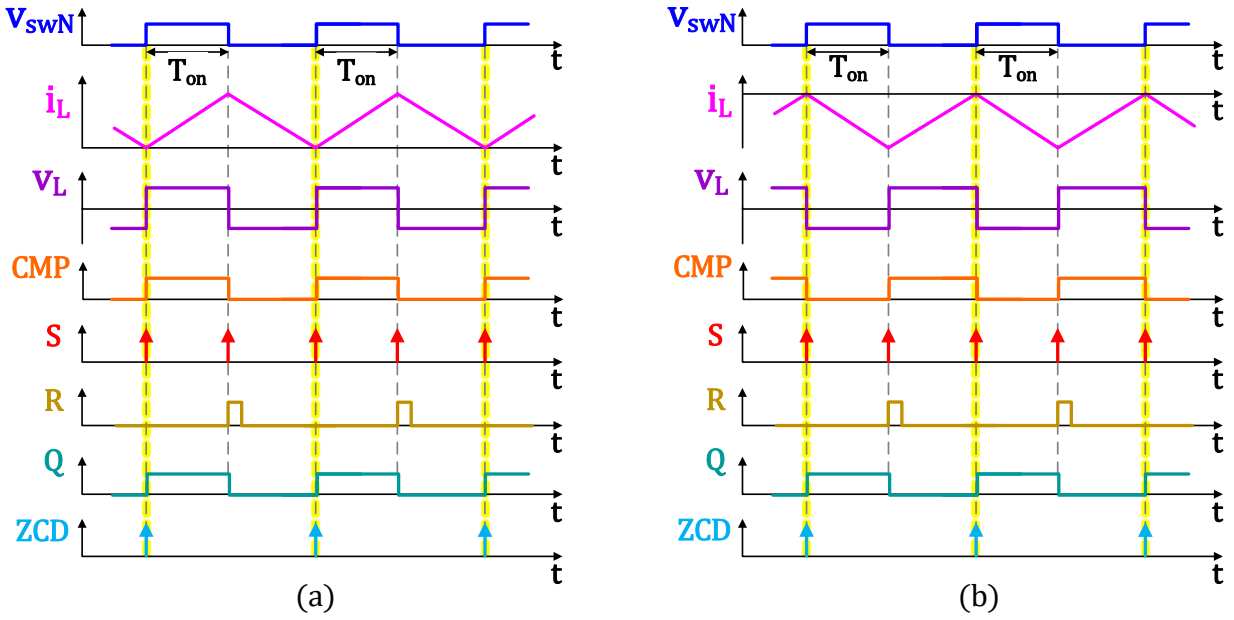


Figure 3.6 Waveforms of relevant ZCD signals in (a) positive half cycle (b) negative half cycle.

Ideally, during the positive half cycle, as shown in Figure 3.6 (a), while the inductor current i_L decreases to zero, for BCM, it is supposed to stop at 0 and start to increase. In this ideal case, at the meantime, v_L changes polarity since $v_L = L\frac{di_L}{dt}$, the slope of the inductor current indicates the polarity of the inductor voltage. So the v_L waveform jumps between a positive value and a negative value during each switching cycle. Comparing this v_L to the ground, a square waveform CMP would be obtained. With the help of a short delay and an XOR gate, rising edges and falling edges of CMP could be extracted as pulses shown as S. There would be two pulses in each cycle, corresponding to the timing that inductor current i_L reaches the cycle peak and returns to zero respectively. The pulse that we're interested in corresponds to $i_L = 0$. So this S signal is sent to the set terminal of an SR and-or latch, whose truth table can be found in Table 2. The reset terminal is connected to T_{off}, which is shown as R in Figure 3.6 and explained in the next section. Basically, signal R is set high when T_{on} ends and stays high for a fixed period T_{off}. By doing this, at the output terminal of the latch, Q is set to high by the pulse generated when $i_L = 0$, and reset to low by R. Connecting Q to a delay, an XOR gate and an AND gate as shown in Figure 3.5, the rising edge timing of Q could be generated as a pulse, shown in ZCD, which corresponding to the timing when i_L returns to zero. The other pulse, which corresponding to the peak of i_L, is blocked by T_{off}. So

far, the zero current point is sensed as ZCD pulse signal and could be used to trigger the COT generator.

Table 2: SR AND-OR Latch Truth Table

S	R	Q
0	0	Hold
1	0	1
X	1	0

From Figure 3.6, it can be found that the zero current corresponds to the rising edge of CMP during the positive half cycle but corresponds to the falling edge during the negative half cycle. This is the reason why the latch and the following gates are used instead of simply extracting the rising or falling edge alone from the CMP.

The ZCD of the proposed circuit senses the inductor voltage rather than the inductor current, so that the source inductance L_S can be taken into consideration in the design. Considering the circuit shown in Figure 3.7, the impedance of the rectifier combining with the source inductance L_S would be

$$R_{in} = \frac{2L_{tot}}{T_{on}} \tag{3.4}$$

Then the designed inductor L1 should be

$$L1 = L_{tot} - L_s = \frac{R_{in}T_{on}}{2} - L_S \tag{3.5}$$

In this way, v_A can still be used in ZCD. It is more adaptable when L_S is not much smaller than L1, or even when $|\omega L_S|$ is not much smaller than R_S. Moreover, by using the source inductance as part of the rectifier, the size of the designed inductor L1 can be reduced.

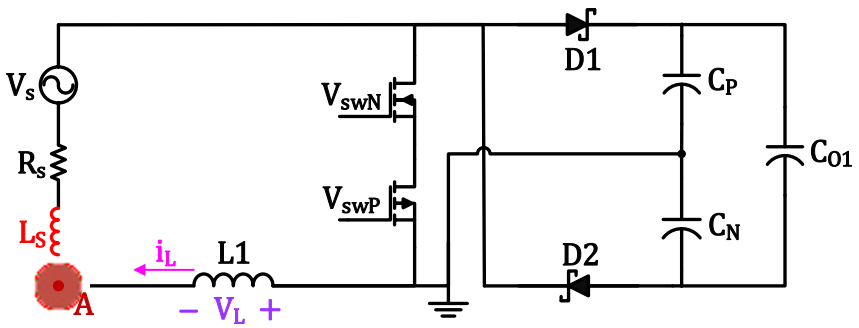


Figure 3.7 Source inductance L_S in the design of L1

On the other hand, this also brings a limitation for the proposed method. With a EMG with higher L_S, the T_{on} ought to be increased accordingly to reach $R_{in} = R_s$. In this way, if the switching cycle is so long that can't be considered much smaller than an input cycle, the proposed method won't be applicable.

The waveform analysis above are based on ideal BCM case. In the real circuit operation, using inductor voltage for ZCD actually relies on the oscillation between L1 and parasitic capacitors of the MOSFETs at the end of each cycle after L1 is discharged. Take the positive half cycle to illustrate, when the inductor current i_L decreases to zero, with the MOSFETs are off and diodes are not forward biased, the inductor L1 starts to oscillate with parasitic capacitors of the MOSFESTs. The equivalent circuit at different states are shown in Figure 3.8 and the corresponding ideal waveforms are shown in Figure 3.9.

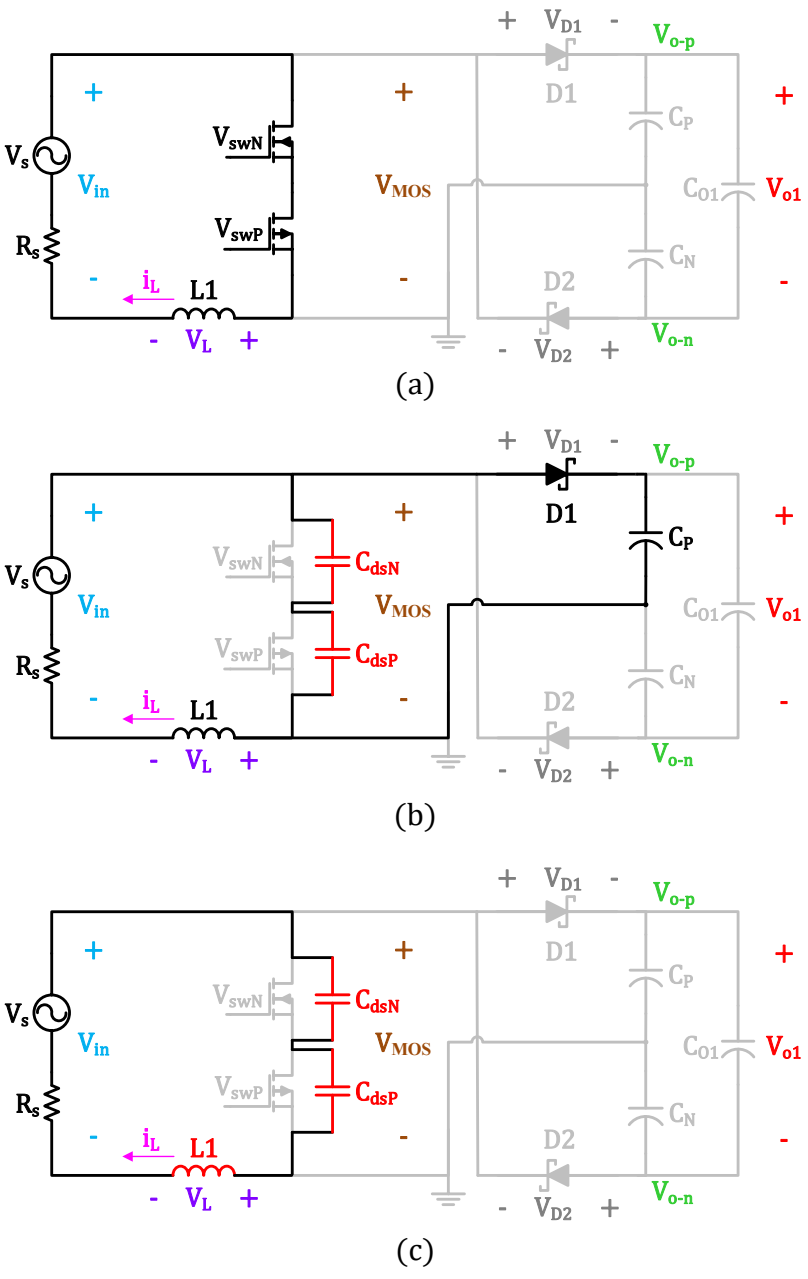


Figure 3.8 Equivalent circuit when (a) MOSFETs are on; (b) diode D1 is on: (c) switches are all off

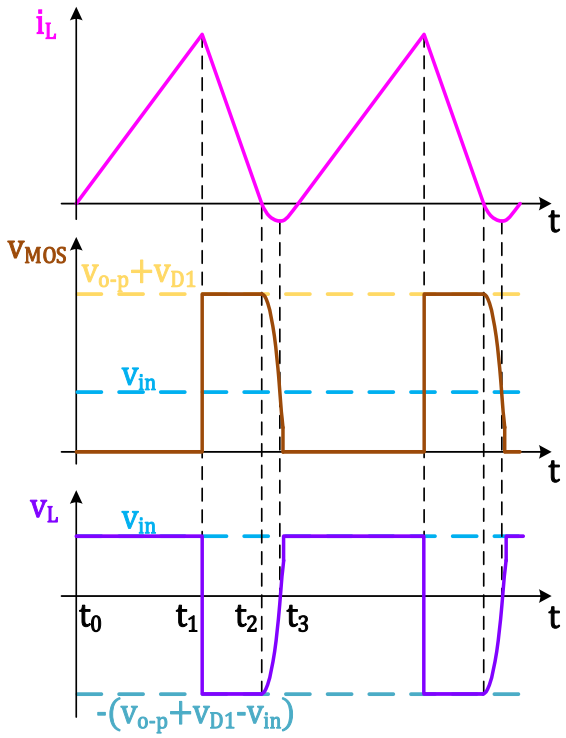


Figure 3.9 Ideal switching waveforms

At the beginning of each cycle, the MOSFET pair is turned on, the equivalent circuit is shown in Figure 3.8 (a), so $v_{MOS} \approx 0$ and thus $v_L \approx v_{in}$. L1 is charged till the on-time ends. This period is presented as $t_0 \sim t_1$ in Figure 3.9. When the MOSFETs are off and D1 is on as shown in Figure 3.8 (b), $v_{MOS} = (v_{o-p} + v_{D1})$ and $v_L = -(v_{o-p} + v_{D1} - v_{in})$, which corresponds to $t_1 \sim t_2$ in Figure 3.9. At t_2, the inductor is fully discharged and $i_L = 0$. After t_2, all the switches are off and L1 starts to oscillate with C_{dsP} and C_{dsN}. The equivalent circuit is shown in Figure 3.8 (c). The oscillation causes the blocking voltage of the MOSFETs v_{MOS} to decrease from $(v_{o-p} + v_{D1})$ to v_{in} during $t_2 \sim t_3$. Meanwhile, i_L goes on decreasing while v_L increases from $-(v_{o-p} + v_{D1} - v_{in})$ to 0. At t_3, the current decreases to most negative. After t_3, i_L starts to increase and v_L crosses 0 and become positive. So, theoretically, t_3 is the time when the ZCD signal is generated and used to initiate the next T_{on}. After the next T_{on} is initiated, v_{MOS} decreases to 0 and v_L increases to v_{in} again.

When the next T_{on} is initiated, the negative current helps to discharge parasitic capacitors of the MOSFETs and thus helps to turn on the MOSFETs. According to the turn-on loss equation

$$P_{loss(turn-on)} = \frac{1}{2} V_{MOS(off)} \cdot I_{MOS(on)} \cdot t_{on} \cdot f_s \tag{3.6}$$

as $V_{MOS(off)}$ is reduced, turn-on loss is reduced. The same phenomenon happens during the negative half cycle. Thus sensing v_A for ZCD would also help to suppress the switching loss.

The circuit diagram of the comparator used in this ZCD block is shown in Figure 3.10.

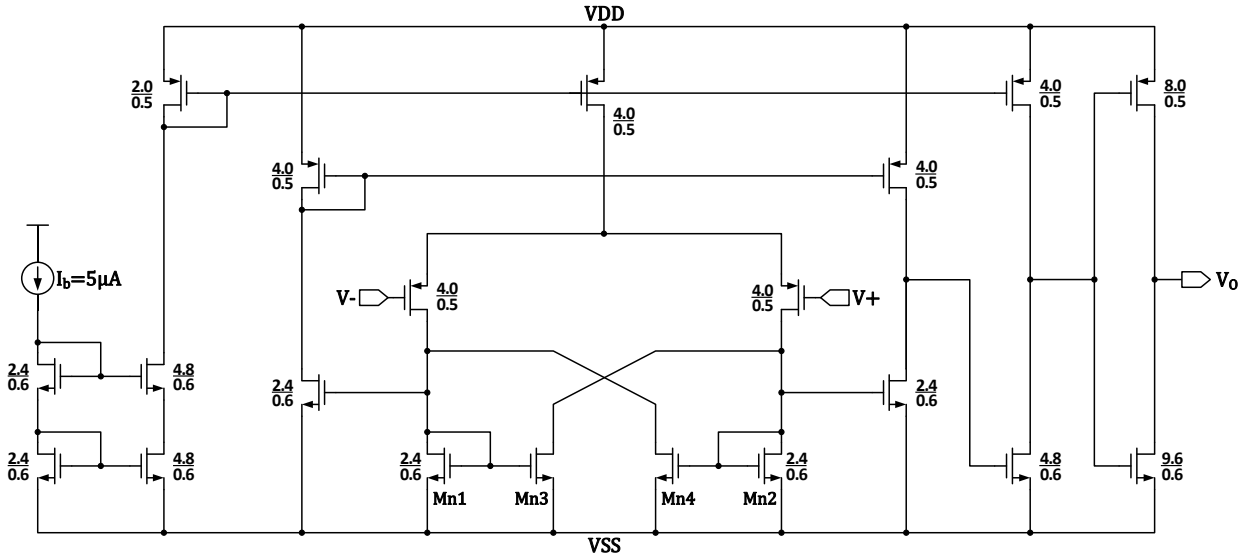


Figure 3.10 Comparator circuit diagram

This comparator is op-amp based, hysteresis is added by adding the cross-coupling formed by Mn1-4. This circuit uses positive feedback from the cross-gate connection of Mn3 and Mn4 to increase the gain of the decision element. Small hysteresis is added by setting the Mn3 and Mn4 to have a smaller width than Mn1 and Mn2, i.e. $\left(\frac{W}{L}\right)_{3,4} < \left(\frac{W}{L}\right)_{1,2}$. This configuration is also used in some of the blocks in the following sections. The width of Mn3 and Mn4 are adjusted according to the hysteresis requirements in each block.

3.3.2 Constant On-time Generator

The COT block shown in Figure 3.11 is composed of three timers, an on-timer, a minimum off-timer, and a maximum off-timer. Each timer consists of a bias current, an SR latch, an NMOS, a capacitor, and a comparator with small hysteresis.

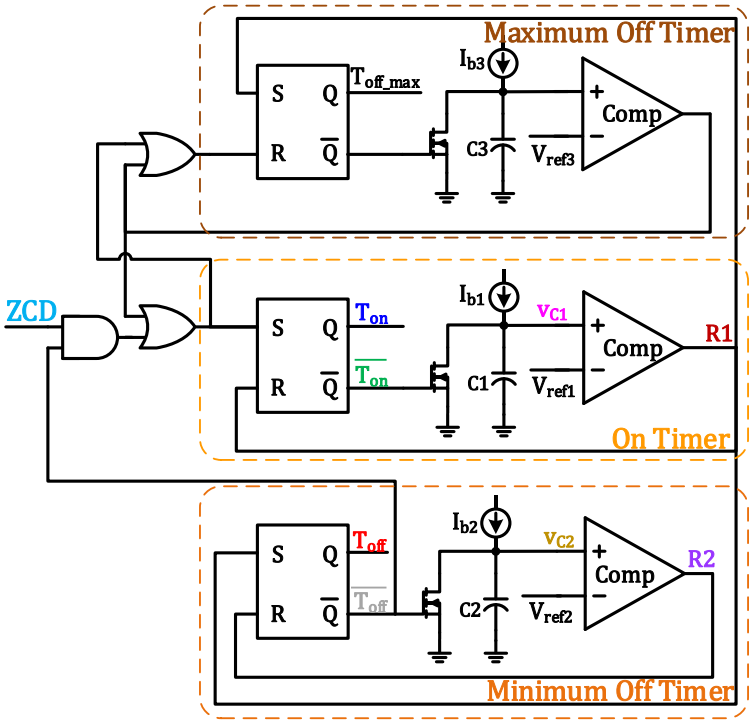


Figure 3.11 Constant On-time Generator

For each timer, suppose the initial voltage on the capacitor is 0, then the comparator would send a low signal to the reset terminal of the SR latch. When a high signal is sent to the set terminal of the SR latch, Q terminal would be high and $\overline{Q}$ terminal would be low. So the NMOS is off, and the bias current charges the capacitor till v_C reaches the reference voltage. Then the comparator would send a high signal to the reset the SR latch. Thus $\overline{Q}$ terminal goes to high and turns on the NMOS. The bias current then flows through the NMOS, the capacitor also discharges via the NMOS. When the capacitor voltage is discharged, the reset terminal becomes low again and the timer will be waiting for the next high signal to the set terminal. The timer is reset when the capacitor is discharged completely.

The ideal operation waveforms of the COT block timers are shown in Figure 3.12.

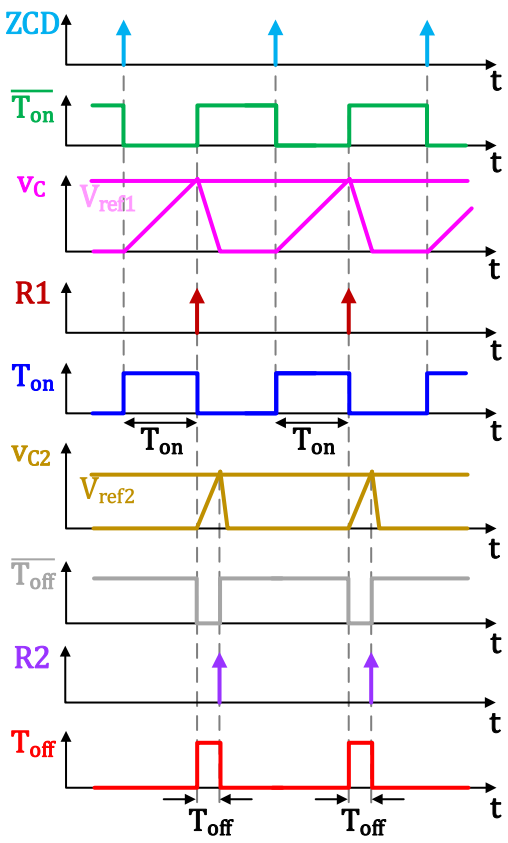


Figure 3.12 Ideal COT generator operation waveforms

The time that terminal Q stays high in a timer is determined by the capacitor charging current and the reference voltage. T_{on} of the on-timer is obtained as follows.

$$v_{C1}(T_{on}) = \frac{1}{C1}\int_0^{T_{on}} I_{b1}dt + V_{C1}(0) = V_{ref1} \tag{3.7}$$

$$T_{on} = \frac{C1\cdot(V_{ref1} - V_{C1}(0))}{I_{b1}} \tag{3.8}$$

As long as the initial capacitor voltage of C1 is zero,

$$T_{on} = \frac{C1\cdot V_{ref1}}{I_{b1}} \tag{3.9}$$

which is constant after C1, V_{ref1} and I_{b1} are fixed.

The minimum off-timer is necessary when $|v_{in}|$ is low, while the ZCD signal could be generated before C1 is fully discharged. This case corresponding to the shadow area on the left in Figure 3.13. The T_{off} period from the minimum off-timer ensures fully discharge of C1 at the

beginning of each cycle and thus ensures the constancy of T_{on}. The T_{off} signal is also used to reset the latch in the ZCD as mentioned in section 3.3.1.

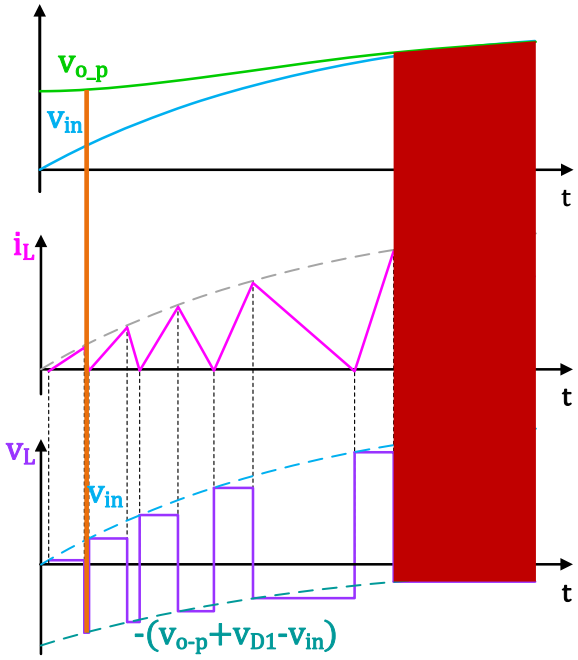


Figure 3.13 Ideal ZCD waveforms

A maximum off-timer is added to prevent ZCD failure when the rectifier output voltage is lower than the voltage generated by the EMG when the boost rectifier is just enabled and the MOSFET pair starts to switch. Take the positive half cycle as an example. The positive envelope of v_L waveform follows v_{in} and its negative envelope follows $-(v_{o-p} + v_{D1} - v_{in})$ as shown in Figure 3.13. Since v_{in} increases faster than v_{o-p}, $(v_{o-p} + v_{D1} - v_{in})$ would then decreases to very low as the shadow area on the right in Figure 3.13. Thus the inductor voltage v_L gets closer to 0 and won't change its polarity, which fails to be used for ZCD and in turn fails to trigger the COT generator. The maximum off-timer ensures to initiate the next T_{on} after elapse of the preset maximum off-time.

3.3.3 Level Shifter and Driver

The control signal generated by the COT generator needs to be converted to the right voltage level to control the MOSFETs in the boost rectifier. Or in other words, the control signal is a -3 ~ 3V signal, while the PMOS in the boost rectifier needs a -3 ~ 0V voltage to control and NMOS needs a 0 ~ 3V voltage. Level shifters are connected between the COT generator and the

drivers to shift the control signal to the appropriate voltage levels. Level shifters with a basic topology as in Figure 3.14 is used in this design. For positive level shifter as shown in Figure 3.14(a), the inverter powered by VSS and VDD1 would have an output high enough to turn on one of the NMOS at the bottom of the squared part. When a NMOS is on, its drain voltage will be pulled down and turn on the PMOS on the other side. Thus the output of the squared part is shifted to VSS to VDD2. The inverter on the output side is used to keep Y has the same logic as A. Similar for the negative level shifter in Figure 3.14(b).

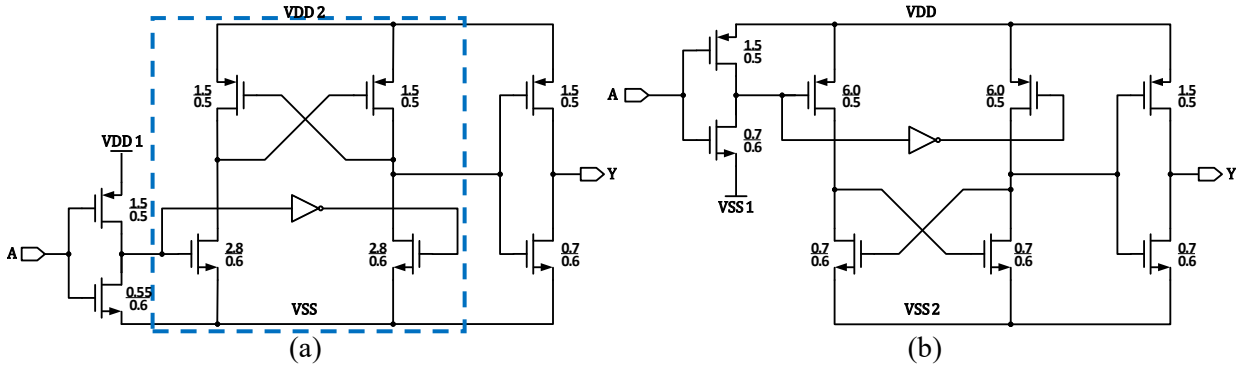


Figure 3.14 Level shifter circuit diagram: (a) for positive level; (b) for negative level

The driver is connected before a MOSFET gate to boost the driving ability and roughly control the turn-on and turn-off time. It usually consists of a series of inverters with increasing W/L to be able to provide higher driving current as the last stage. The circuit diagram is shown in Figure 3.15. The transmission gate is added with gate connected to VDD and VSS to keep the driver output at high impedance when the internal supply (VDD-VSS) is very low. So the leaking current would be minimized and thus the power dissipation on the driver during the start-up.

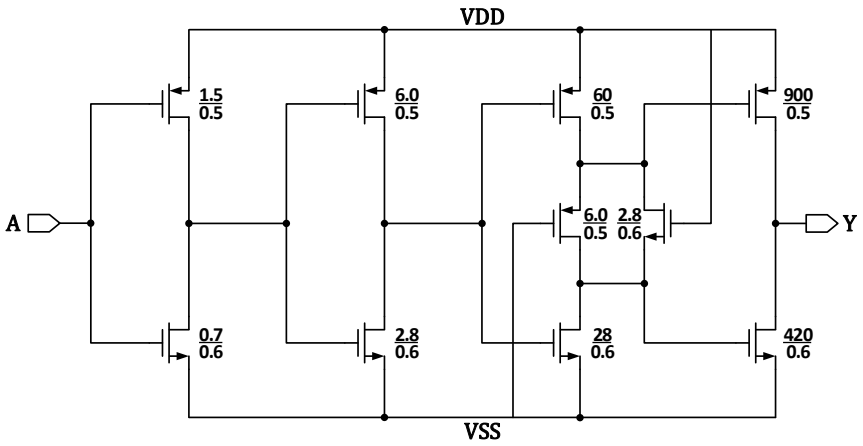
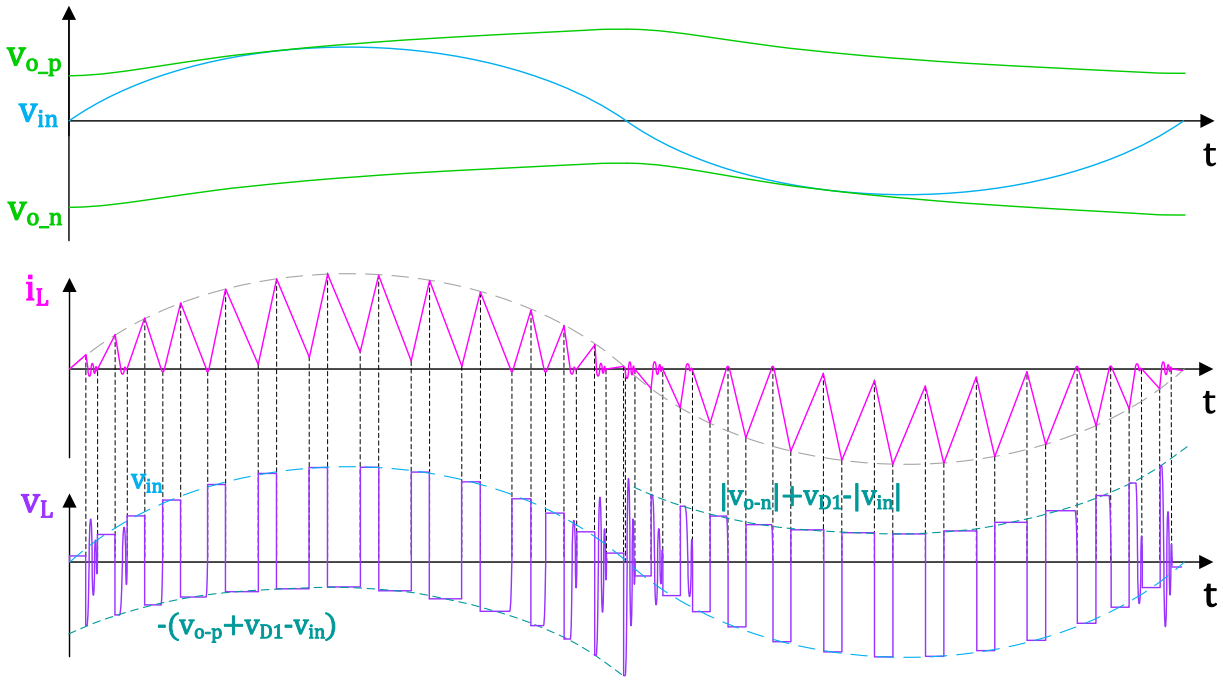


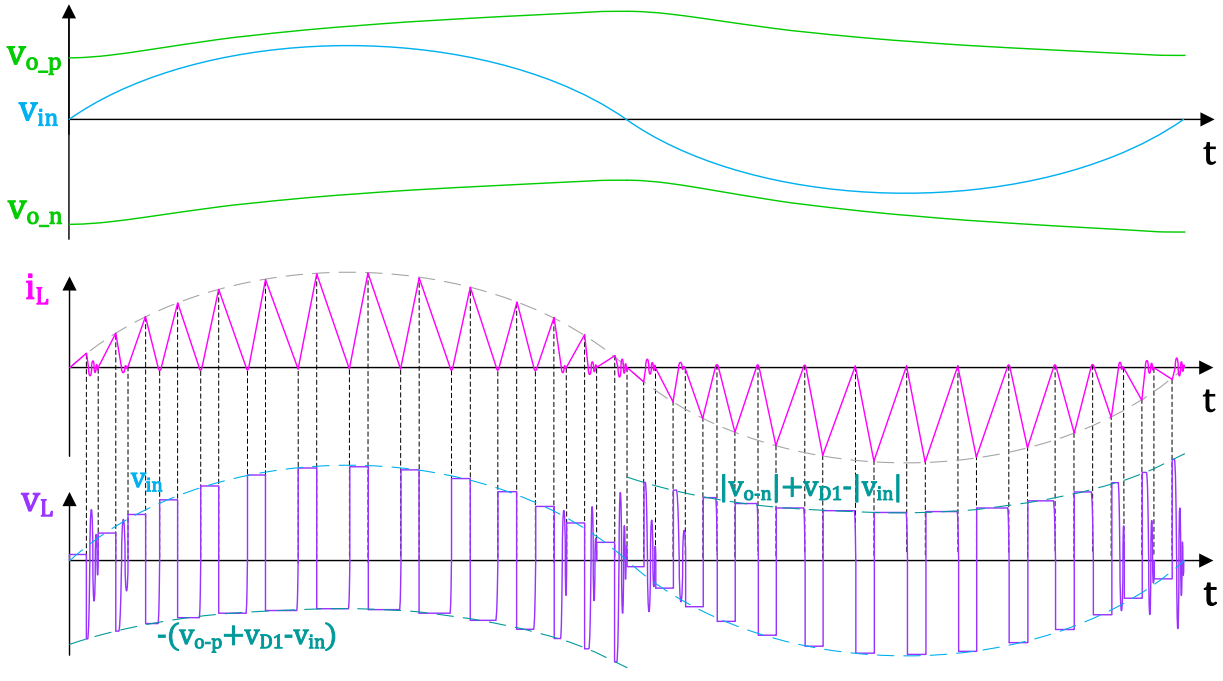
Figure 3.15 Driver circuit diagram

3.3.4 Ideal Waveforms of the Proposed Method

With the design from the previous sections, the ideal waveforms indicating the relationship between v_{in}, $v_{o\text{-}p}$, $v_{o\text{-}n}$, i_L and v_L are shown in Figure 3.16.



(a)



(b)

Figure 3.16 Ideal waveforms: (a) when $v_{O1} < V_{in,p\text{-}p}$, (b) when $v_{O1} > V_{in,p\text{-}p}$.

Figure 3.16 (a) shows the ideal waveforms when the boost rectifier output voltage is lower than the peak-to-peak voltage of the input voltage, i.e. $v_{O1} < V_{in,p\text{-}p}$, where $v_{O1} = v_{o\_p} - v_{o\_n}$. As

shown in Figure 1.1Figure 3.13 and explained at the end of section 3.3.2, when v_{in} is very low, the MOSFETs off-time is decided by the minimum off-time; when v_{in} increases, the MOSFETs off-time is decided by the zero current detector as it is supposed to be; when v_{in} increases to close to the input voltage amplitude V_p, the MOSFETs off-time is decided by the maximum off-time. Figure 3.16 (b) shows the ideal waveforms when $v_{O1} > V_{in,p-p}$, the MOSFETs off-time is decided by the minimum off-time only when v_{in} is very low, and decided by the zero current detector in other times.

3.4 Proposed Energy Harvesting System

The proposed EH system for EMG is shown in Figure 3.17. Besides the boost rectifier and its controller, the system has a buck converter with COT V^2 controller and a stage coordinator. The boost rectifier is used to match the impedance of EH circuit to that of EMG. Meanwhile, it rectifies and boosts the voltage generated by EMG. Since the boost rectifier cannot provide a regulated output by itself when running in BCM continuously, the buck converter is added to perform voltage regulation and deliver a stabilized DC voltage to the USB port. The stage coordinator senses the rectified voltage and uses it to decide when to enable the rectification stage and when to enable the regulation stage.

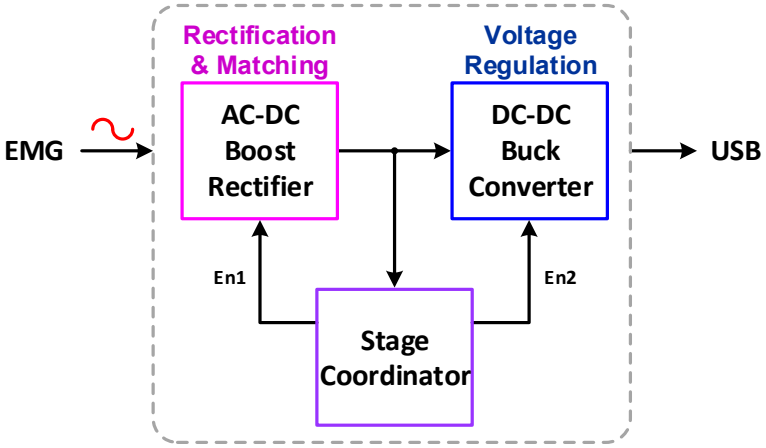


Figure 3.17 Proposed energy harvesting system

3.4.1 Stage Coordinator

The stage coordinator checks the rectified voltage and generates En1 and En2 signals to enable the rectification stage and regulation stage respectively. If the voltage is 4 ~ 7.5V, En1

would be high to enable the rectification stage. The minimum value is set to 4V to provide a roughly ±2V internal supply and thus ensure the turn-on of power MOSFETs in the boost rectifier. When the voltage is higher than 6V, the regulation stage would be enabled by the En2 high signal. The block diagram of the stage coordinator can be found in Figure 3.18. A table indicating its operation is shown in Table 3.

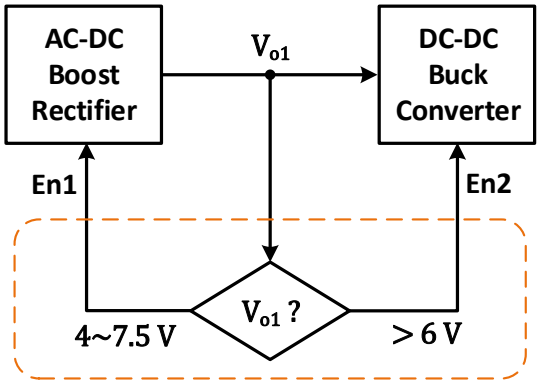


Figure 3.18 Stage coordinator block diagram

Table 3: Stage Coordinator Operation

V_{o1} (V)	En1	En2
< 4	0	0
4 ~ 6	1	0
6 ~ 7.5	1	1
> 7.5	0	1

To implement the stage coordinator, differential amplifier and comparators with hysteresis are used in this design as shown in Figure 3.19.

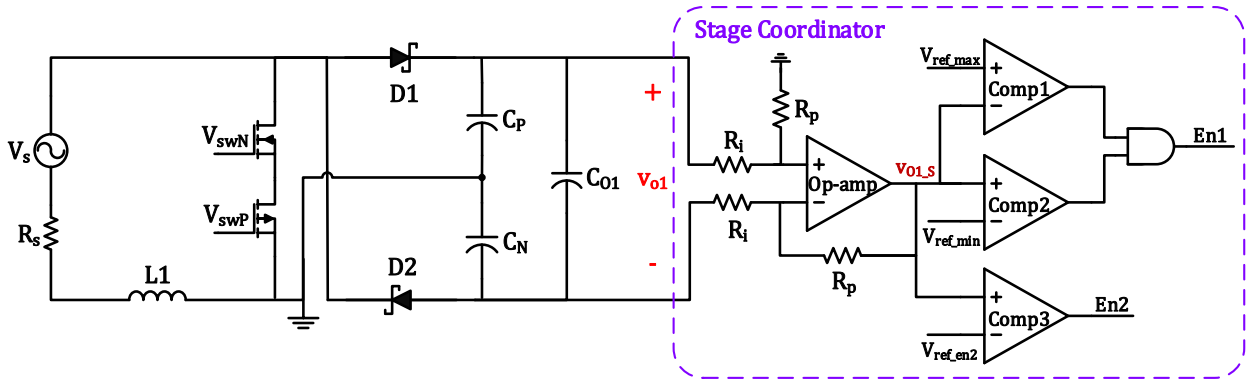


Figure 3.19 Implementation of stage coordinator

The differential amplifier senses the floating output of the rectification stage and converts it to a ground referenced voltage v_{O1_S}.

$$v_{O1\_S} = \frac{R_p}{R_i} \cdot v_{O1} \tag{3.10}$$

v_{O1_S} is then used to compare with different references and generate enable signals. Note that the closed loop gain of the sensing amplifier should be taken into consideration when setting the reference voltages.

Hysteresis is added in the comparators design so that there would be some margin for the voltage drop when turning on the switches.

The CMOS circuit diagram of the op-amp in Figure 3.19 is shown in Figure 3.20. This is a basic two-stage differential amplifier. A differential input stage drives an active load followed by a second gain stage. This circuit configuration provides good common-mode range, output swing, voltage gain, and common mode rejection ratio (CMRR) in a simple circuit.[15]

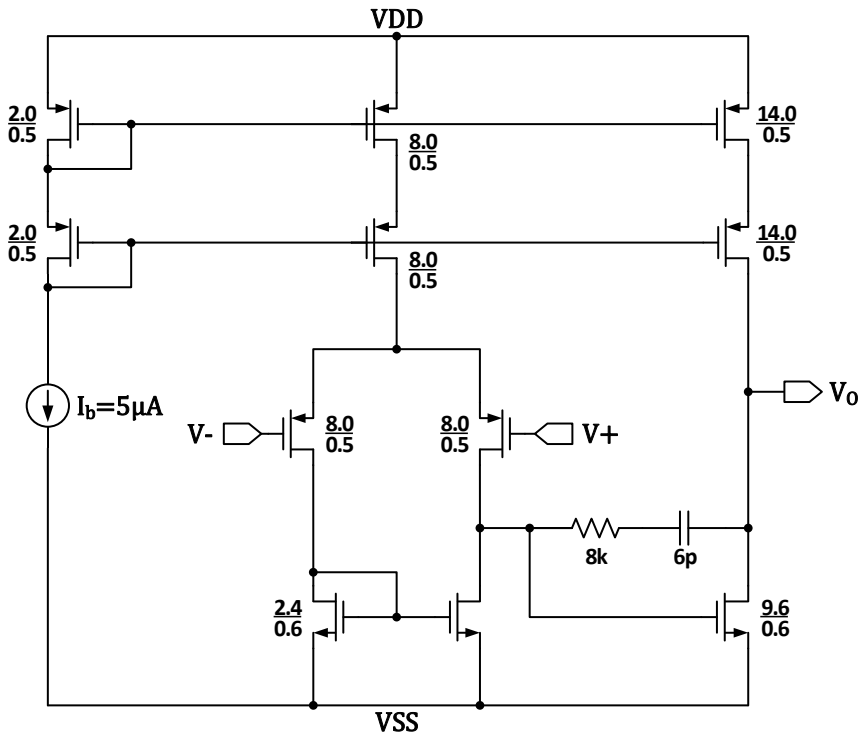


Figure 3.20 Op-amp circuit diagram

3.4.2 Voltage Regulation Stage

The boost rectifier is set to act as a resistor and match the impedance of the EMG. The on-time is fixed and the off-time changes with input voltage to achieve BCM so we loss the control of off-time in order to have impedance matching. Thus, the output of the boost rectifier is DC but not regulated. The boost rectifier alone may be used to charge a battery or super capacitor, but not for applications such as stable power supply through USB ports.

A buck converter shown in Figure 3.21 is added to regulate the output voltage for the proposed circuit. The buck converter adopts COT V^2 control to regulate the output voltage. The V^2 control inner loop, current loop, is used to limit the minimum value of v_{O2}. As shown in Figure 3.21, v_{O2} is sensed as v_{O2_S} by a differential amplifier. v_{O2_S} is then compared with the reference voltage to generate a pulse when v_{O2} is lower than 5V. The pulse is then used to trigger a COT pulse and thus the control signal. This signal also goes through a level shifter and a driver to shift to the appropriate voltage level and increase the driving ability.

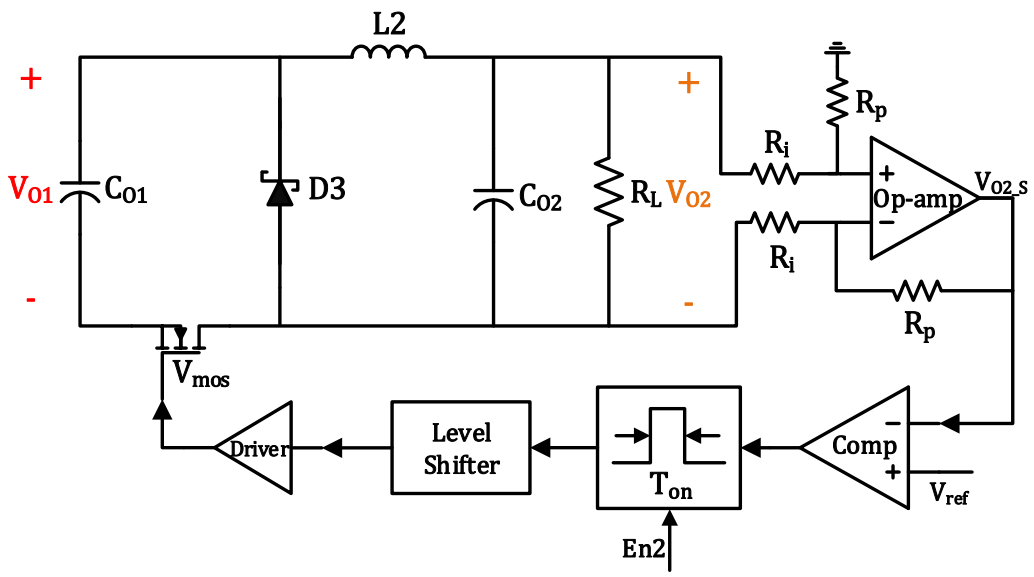


Figure 3.21 Circuit diagram of the regulation stage

This method leads to low circuit complexity and fast transient response. Since v_{O1} has a range of 6~ 7.5V and v_{O2} is 5V, if run the buck converter in CCM, then the duty ratio would be 0.67 ~ 0.83, which is above 0.5. According to [14], operating the buck converter in CCM with D > 0.5 would cause instability in the control loop, which would require an additional ramp to stabilize. To simplify the design, the buck converter in the proposed system is designed to operate in DCM.

3.4.3 Start-up and Supply Strategy

If the gate voltage of both MOSFETs of the boost rectifier is zero or too low during startup, the MOSFETs could remain off to fail the boost rectifier. The power stage of boost rectifier is then can be simplified as shown in Figure 3.22. Under this circumstance, the circuit is working as a voltage doubler and capable of charging C_P and C_N during the positive and negative half cycle respectively. So C_P and C_N, along with C_{O1} together, could be used to supply the control circuits. Node $v_{o\text{-}p}$ would be the positive supply while node $v_{o\text{-}n}$ would be the negative supply. Low-dropout (LDO) regulators can be connected to provide more stable supplies at AVDD and AVSS as shown in Figure 3.22.

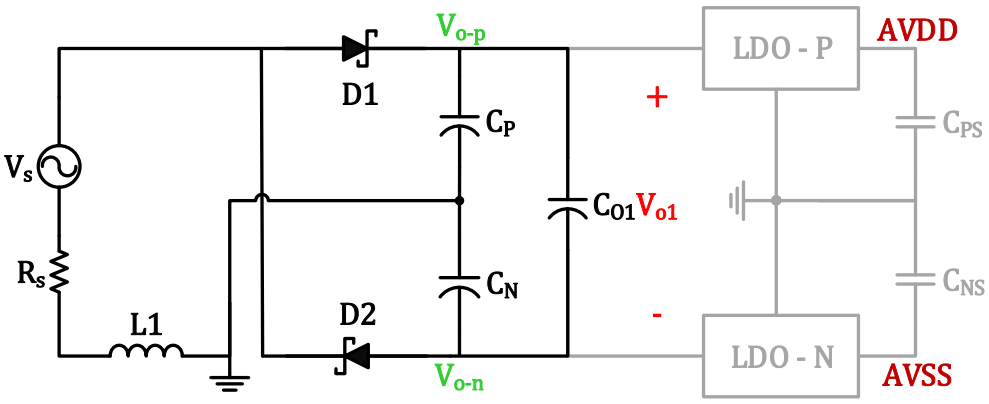


Figure 3.22 Startup and supply strategy

The circuit diagram of a LDO is shown in Figure 3.23. The output voltage of LDO is sensed and compared to a reference to determine whether to turn on or turn off the PMOS to charge the output.

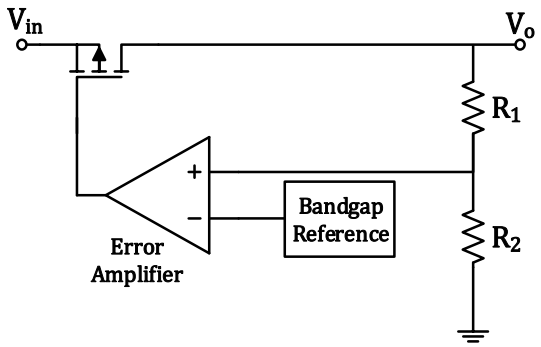


Figure 3.23 LDO circuit diagram.

3.4.4 Current Bias and Voltage Reference

The current bias circuit is supplied independent to provide a relatively stable current to bias components such as op-amp and comparator, and also be used as current sources in the COT generator block. The circuit diagram to generate a 5μA bias current is shown in Figure 3.24. The PMOS current mirror forces the current on both branch to be equal. The gate-to source voltage difference is added on the resistor. Since the gate-to-source difference is independent of supply voltage VDD and VSS, the current on the resistor would also be supply independent[15]. The circuit on the left acts as a start-up circuit for the main current biasing circuit.

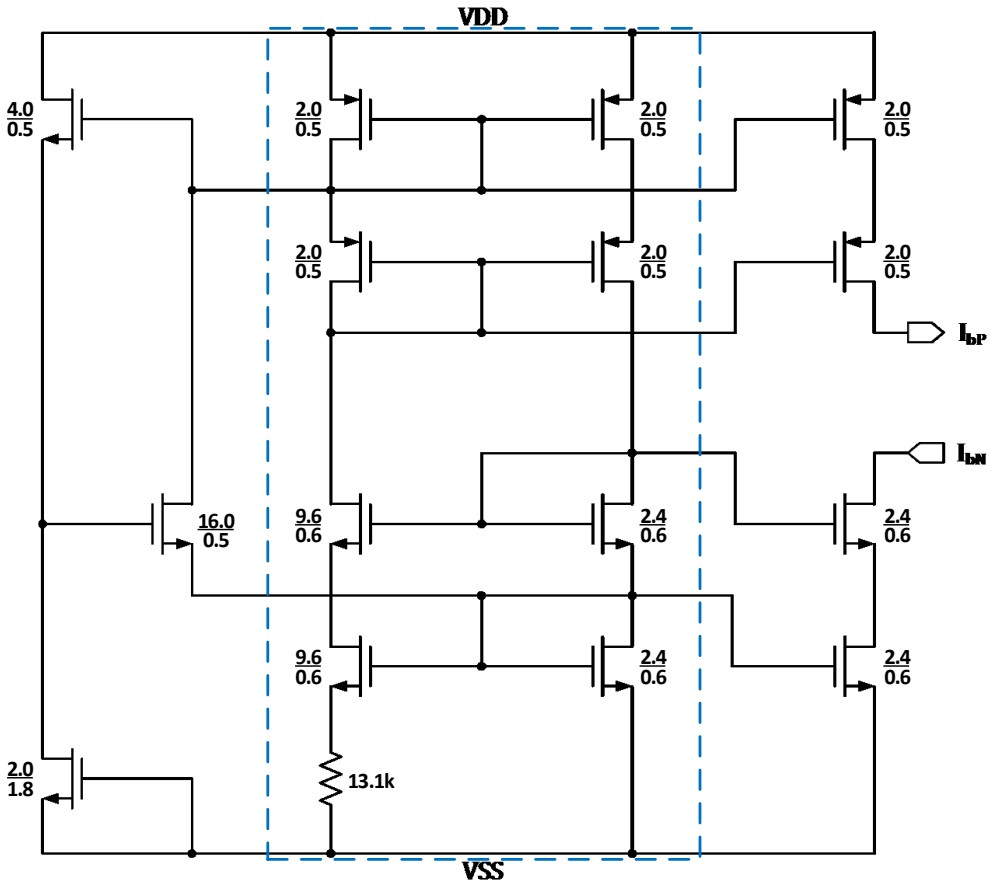


Figure 3.24 Current bias circuit diagram

Band-gap references are designed to offer supply independent and temperature independent references to minimize the error and increase the accuracy of the controller. The circuit diagram is shown in Figure 3.25. The V_{BE} of a Bipolar device is Complementary to Absolute Temperature (CTAT), while the voltage difference between two Bipolar devices is Proportional to Absolute Temperature (PTAT). [16] In this design, the voltage drop on R1 equals to $\Delta V_{BE} = V_{BE1} - V_{BE2} = Vt \cdot \ln(8)$, which is PTAT. So the current on R1 is also PTAT. This current is then mirrored to the output branch and generate a PTAT voltage across R2. Adding the CTAT voltage on the Bipolar device, a supply independent and temperature independent reference can be obtained.

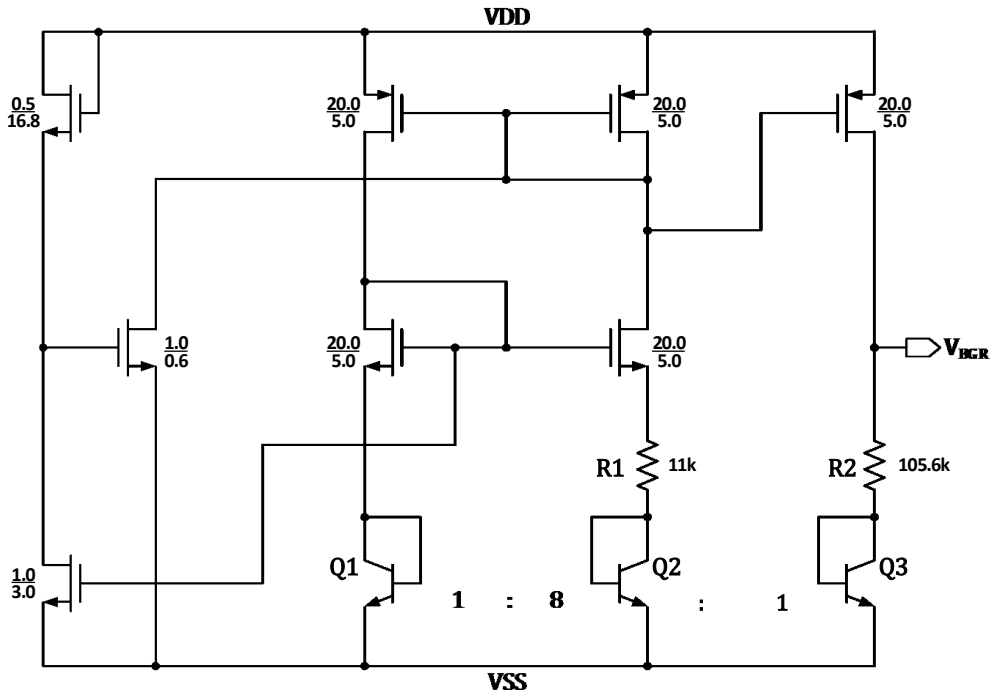


Figure 3.25 Band-gap reference circuit diagram

3.5 Chapter Summary

This chapter describes the proposed EH circuit design and highlights the implementation of the proposed direct impedance matching method. The boost rectifier is designed to run in BCM to emulate a resistor load to EMG and to reduce the switching loss, so maximum power can be harvested. Since the boost rectifier with COT control operating in BCM cannot provide a regulated output voltage, a buck converter as voltage regulator is designed to stabilize the output voltage of the system at 5V. All the detailed designs are explained block by block. Transistor level circuits are included for key components or blocks. Start-up and internal supply issues are addressed to fulfill the independent of the whole EH circuit.

Chapter 4

Simulation and Measurement Results

This chapter describes the functionality of the proposed converter through simulation and chip measurement. Section 4.1 shows the layout and its area. Section 4.2 details simulations of the functionality include ZCD, overall simulation of the EH circuit and cold start. The chip is tested and the result is presented in section 4.3. Lastly, section 4.4 summarizes the chapter.

4.1 Layout

The proposed EH circuit except for a few passive components and Schottky diodes was designed in 0.18 μm BiCMOS technology and taped out. The layout of the circuit is shown in Figure 4.1. Major blocks are marked in the figure. The total die area is less than 10 mm^2.

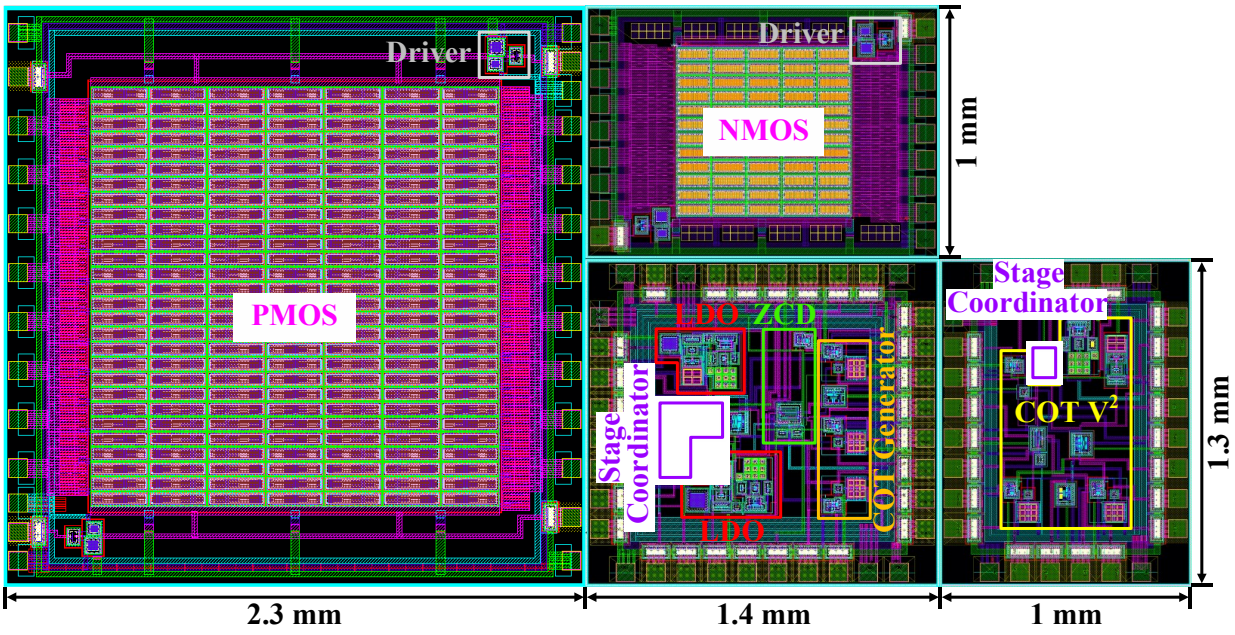


Figure 4.1 Circuit layout.

4.2 Simulation Results

The circuit simulation was performed in the Cadence environment. The source voltage V_S of the EMG is set to have 3V amplitude and 700 Hz frequency, the source resistance R_S is set to be 1Ω. The DCRs of inductors and ESRs of capacitors are included in the simulation. Major passive components for the boost rectifier in Figure 3.5 are L1=2.1μH, C_P=C_N=150μF, C_{O1}=300μF, and those for the buck converter in Figure 3.21 are L2=4μH and C_{O2}=33μF with ESR=35mΩ.

Figure 4.2 shows simulation results of the ZCD in Figure 3.5. From Figure 4.2 (a), it can be seen that during the positive half cycle, when the inductor current i_L decreases to the minimum value around 0, v_L jumps from negative to positive, which results in a rising edge in the CMP signal. This rising edge is picked up by the zero current detector which delivers a ZCD pulse and then the next on-time is triggered. Similar thing happens to the negative half cycle as shown in Figure 4.2 (b). The simulation results verify that the zero current detector can successfully perform ZCD, which leads to the intended operation of the boost rectifier in BCM.

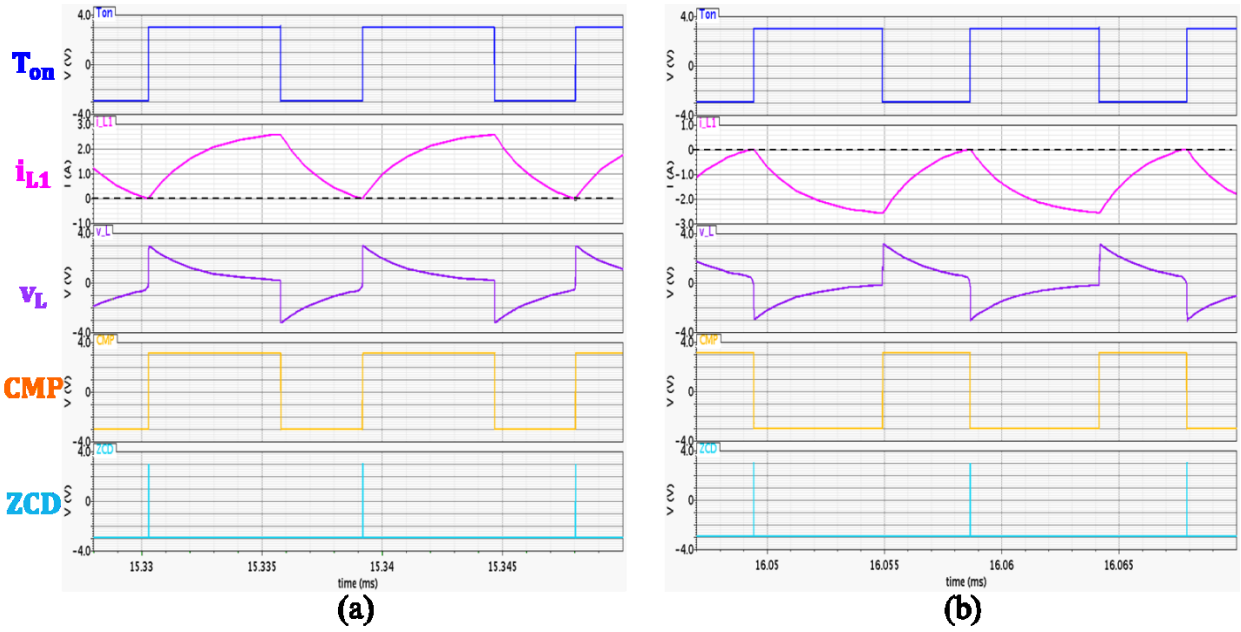


Figure 4.2 ZCD simulation results during (a) the positive half cycle, (b) the negative half cycle.

The next simulation intends to verify the coordination of the two stages as well as the operation of buck converter for output voltage regulation. The load resistor R_L of the buck converter in Figure 3.21 is set to 250Ω. Figure 4.3 shows the simulation result of the entire EH circuit with two stages coordinating. When v_{O1} is charged to 4.5V at t1, En1 changes from low to high. Then the boost rectifier starts to operate and charges C_P, C_N and C_{O1} more rapidly. Thus v_{O1}

increases faster. When v_{O1} increases to about 6.5V at t2, En2 jumps from low to high enables the buck converter. It starts to work and regulate the output voltage to 5V. Meanwhile, v_{O1} increases steadily. When v_{O1} reaches 7.6V at t3, En1 returns from high to low. Thus the boost rectifier stops charging the capacitors. However, the capacitors can still supply power to the buck converter and hence v_{O1} decreases. When v_{O1} drops to lower than 7.4V at t4, En1 goes to high again. So the AC/DC rectifier start to charge v_{O1} again.

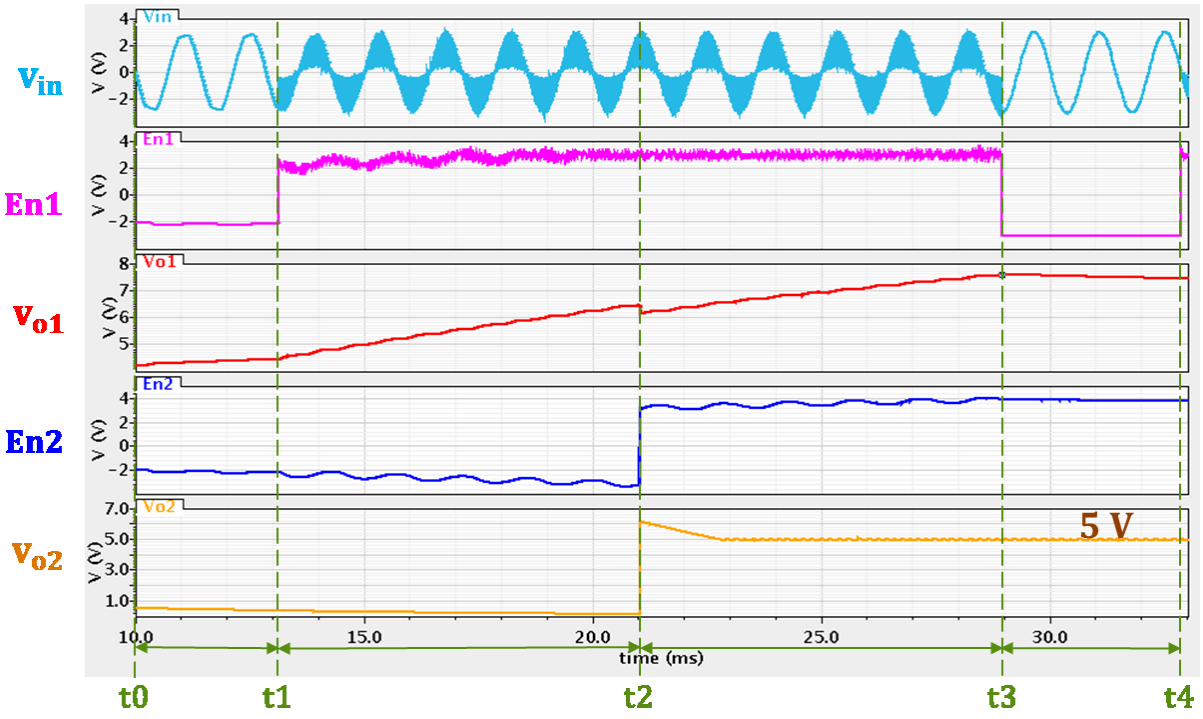


Figure 4.3 Simulation result of the entire EH circuit when R_L=250Ω.

The next simulation is done to prove the cold start capability. Capacitors C_P, C_N and C_{O1} of the boost rectifier in Figure 3.5 are set to have zero voltage as the initial condition. The simulation results can be found in Figure 4.4. At the very beginning, there's no power in the circuit, so the gate voltages of the PMOS and NMOS, VswP and VswN, in the boost rectifier stays at zero. Thus the circuit works as a voltage doubler, capacitors C_P, C_N and hence C_{O1} of the boost rectifier are charged up, so v_{O1} starts to increase. With v_{O1} charged up a little bit, the circuit and thus VswP and VswN are disturbed. But with v_{O1} continue being charged, VswP and VswN return back to zero and stay at zero. Meanwhile, En1 stays low until the v_{O1} rises to around 4.5V. Then En1 jumps to the high voltage level, which enables the switching mode boost rectifier. This is also indicated

as VswP and VswN start to switch and v_{O1} increases faster at t1 in Figure 4.4. So, the proposed EH is able to start-up when the capacitors C_P, C_N and C_{O1} are completely drained.

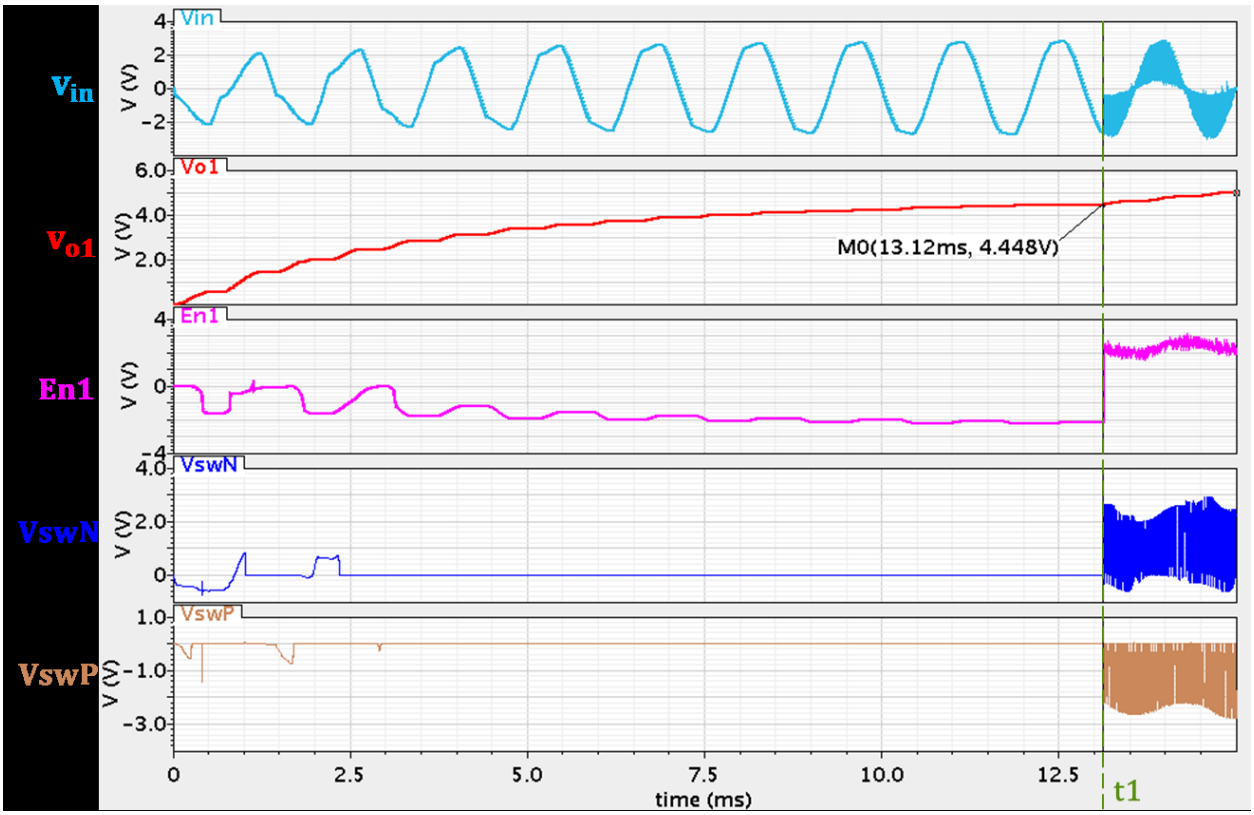


Figure 4.4 Cold start simulation results.

Figure 4.5 is the transient response of the buck converter load R_L changes from 47.4Ω, which is around the balance point, to 100Ω, which is a lighter load, at 20ms, and then to 30Ω, which is a heavier load, at 30ms. Before 20ms, v_{O1} reaches a relatively steady voltage since R_L is around the balance point of the system. From 20ms, load is lighter, v_{O1} starts to increase while v_{O2} remains 5V. From 30ms, load is heavier, v_{O2} maintains 5V until v_{O1} decreases to below 5.5V which makes En2 low and disables the buck converter. Then v_{O2} decreases and v_{O1} charges up till it reaches 6.5V, En2 jumps to high and enables the buck converter again.

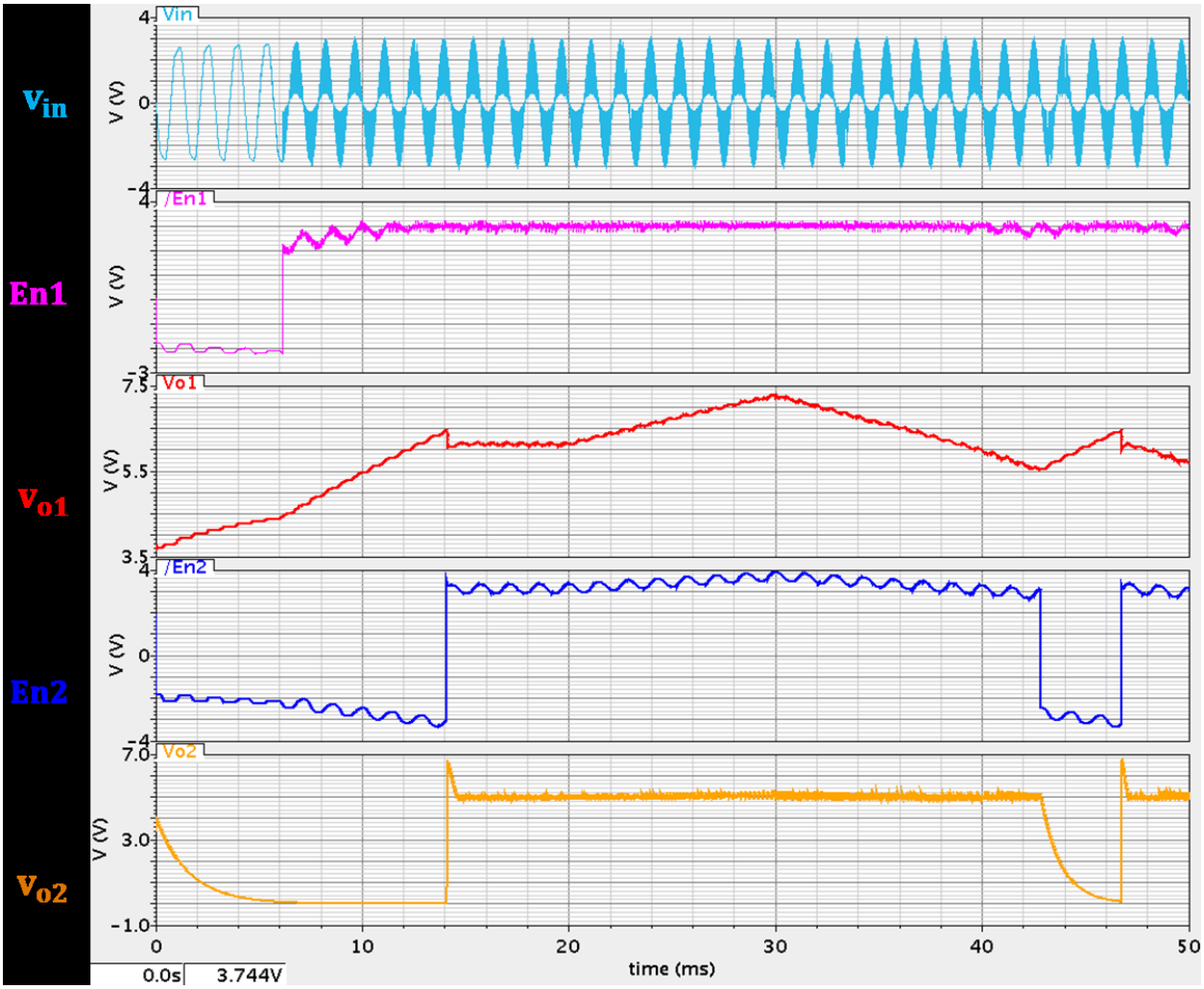


Figure 4.5 Transient response

The simulated efficiency of the boost rectifier is about 71%, and that of the buck converter is around 95%. The overall efficiency of the whole EH circuit proposed above is 67%.

The simulations above are done with a 3V amplitude, 700Hz AC source and a 1Ω R_S as EMG. If the EMG has a lower frequency, the output caps C_P and C_N should be increased roughly inversely proportional to the EMG frequency. If the EMG has a lower amplitude, the reference voltages in the stage coordinator should be lowered accordingly. However, the system requires a minimum supply voltage to run. Thus, it is recommended to have an EMG with amplitude higher than 2.5V. At this point, the proposed circuit doesn't meet the specification is listed in Table 1. Further improvement and design are required to deal with the lower voltage range.

4.3 Measurement Results

Every block or component in the control network are designed to be able to test individually. The first step of testing the chips is to verify the operation and functionality of the current biasing, voltage reference, each sub-block and each control blocks individually. After all the blocks are proved to be working, they are connected to realize the designed EH circuit system. Parts that couldn't work would be replaced by commercial chips.

For testing purpose, all the supplies for control circuit in block testing are from external DC power supply of $\mathrm{VDD} = 3\mathrm{V}$ and $\mathrm{VSS} = -3\mathrm{V}$ unless specified otherwise.

4.3.1 Current Biasing and Band-gap Reference

The current biasing circuit is designed to supply a current source to the timers, and bias the comparators and op-amps. The measurement result of a 5μA current biasing circuit is shown in Figure 4.6.

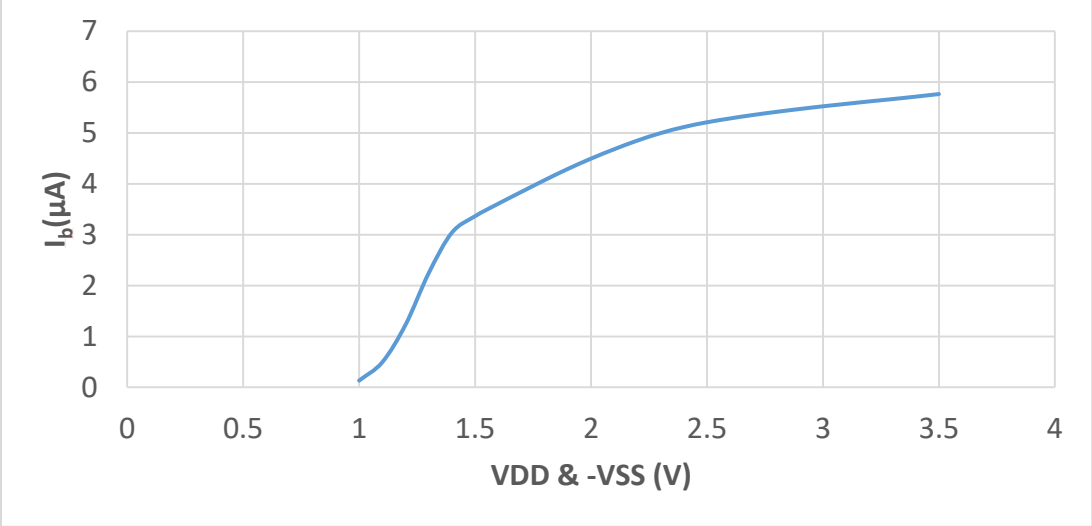
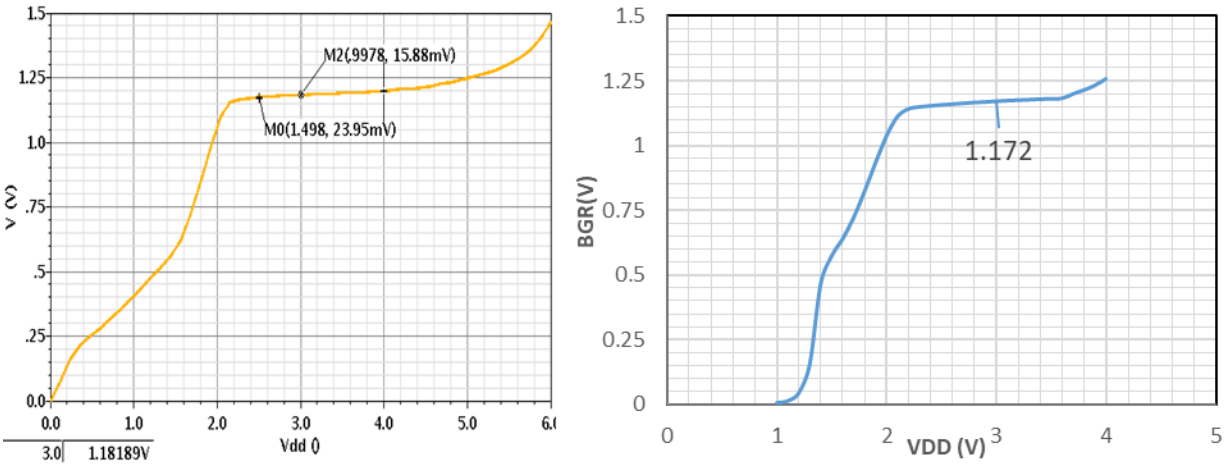


Figure 4.6 Current biasing circuit measurement result

It can be seen that the biasing circuit can provide a current varies within 6% when the supply voltage ranging from ± 2.5V to ± 3V.

Band-gap reference is designed to have a stable output independent of supply voltage and temperature within a range. The simulation result and measurement result are compared in Figure 4.7.



(a) (b)

Figure 4.7 Band-gap reference circuit: (a) simulation result; (b) measurement result

It can be found that although the measured value is slightly (0.8%) lower than that in the simulation, it varies within 3% when the supply voltage is 2.5 ~ 3.5V.

4.3.2 Sub-blocks

The first sub-block tested is a hysteretic comparator. This comparator is designed to have a hysteresis of 200mV. With the positive input V+ is connected to function generator while the V- is grounded, the comparator input v.s. output characteristic is tested and shown in Figure 4.8.

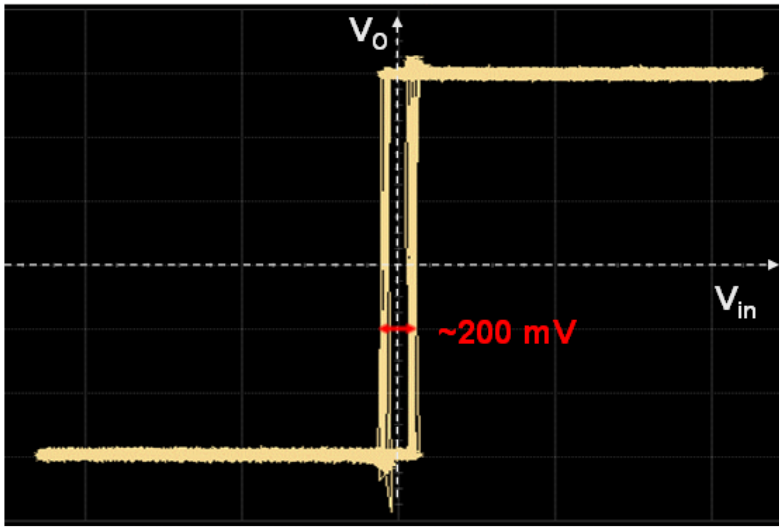


Figure 4.8 Comparator input v.s. output voltage characteristic

It can be found that the comparator has a hysteresis around 200mV which is close to the design.

The next sub-block tested is the differential amplifier used for v_{O1} and v_{O2} sensing. The differential amplifier consists of the op-amp shown in Figure 3.20 and four external resistors as shown in Figure 4.9.

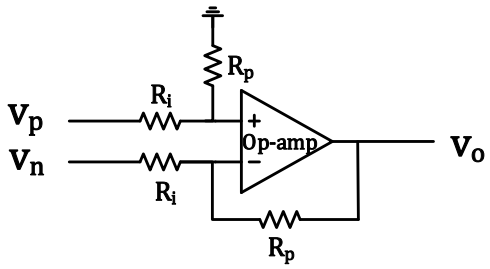


Figure 4.9 Differential amplifier for voltage sensing

In the test, the resistors are set to $R_i = 1k\Omega$ and $R_i = 5.1k\Omega$. From the test, it is found that v_o can only reaches a maximum value of around v_n + 0.3 V.

In order to run the amplifier to have a higher v_o range, the positive and negative inputs are exchanged as shown in Figure 4.10, so the higher input is connected to the negative terminal of the op-amp through R_i. This results in an inverted output. An op-amp based inverter is connected follows the differential amplifier to correct the polarity. The revised voltage sensing circuit is shown in Figure 4.10.

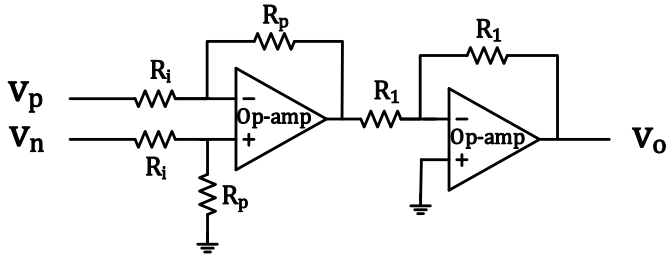


Figure 4.10 Revised voltage sensing circuit

The next one is a level shifter. It's designed to shift an input voltage of -3 ~ 3V to an output of 0 ~ 3V. The test result is shown in Figure 4.11 Level shifter input (A) and output (Y), which verifies the design. The rising and falling edge are not sharp enough since the last stage in the level shifter doesn't has enough driving ability. So the parasitic capacitance and resistance of the wire and probe would add a RC delay shown in the output Y. This can be improved by increasing the CMOS W/L ratios in the level shifter last stage.

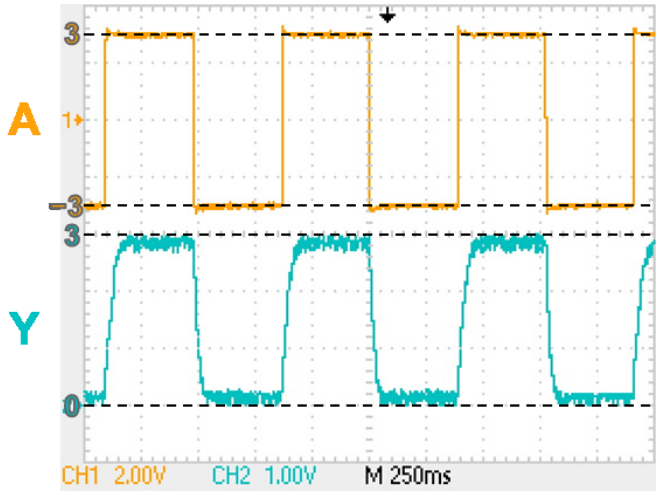


Figure 4.11 Level shifter input (A) and output (Y)

The last sub-block tested is the timer without the logic latch as shown in Figure 4.12. In the original design, I_b is set to 1μA. However, in the measurement, v_c increases from a negative value instead of 0 as shown in Figure 4.13, which results in a longer time for C to charge to V_{ref}. The reason of C charging from negative is probably because of a large miller capacitor formed between the gate and drain of the NMOS. When $\overline{Q}$ is high at 3V, NMOS $V_{gd} \approx 3V$. As soon as $\overline{Q}$ jumps to low at -3V, since the voltage on the miller capacitor won't be discharged immediately, the voltage at the NMOS drain, i.e. v_c is forced to a negative value. The large miller capacitor is probably formed by the layers on top of this NMOS in the layout, which worth further investigation in the future.

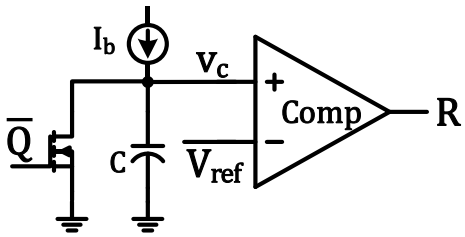


Figure 4.12 Timer circuit

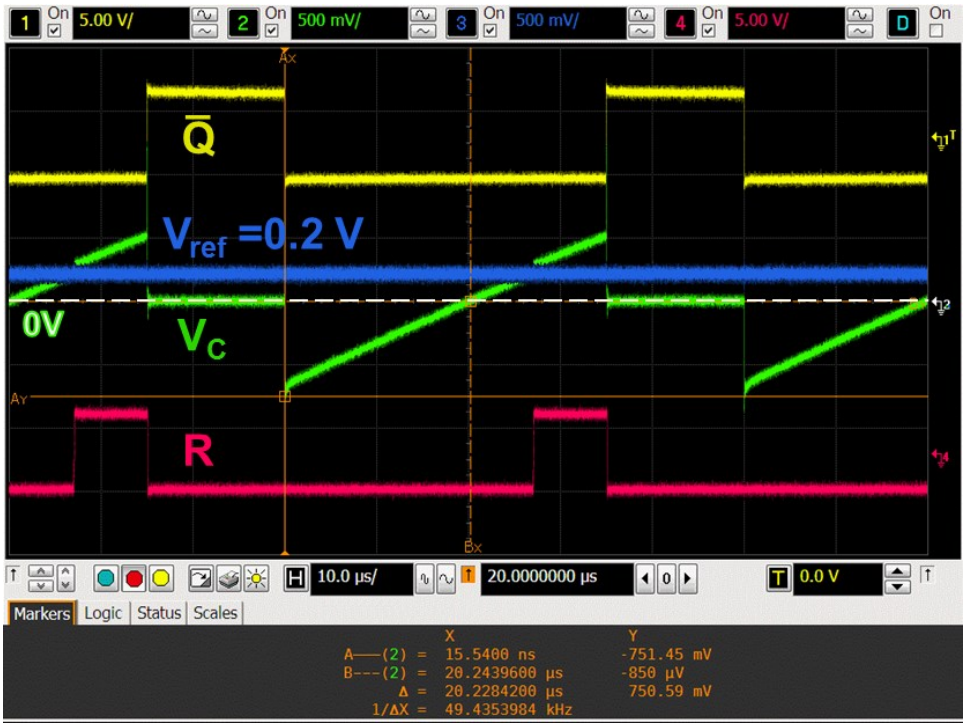


Figure 4.13 Issue of timer

In order to shorten the time it takes for the v_c to charge to 0, a 5µA bias current is added to I_b. By adjusting the V_{ref}, the time for C to charge to V_{ref} can be set to 5µs as shown in Figure 4.14.

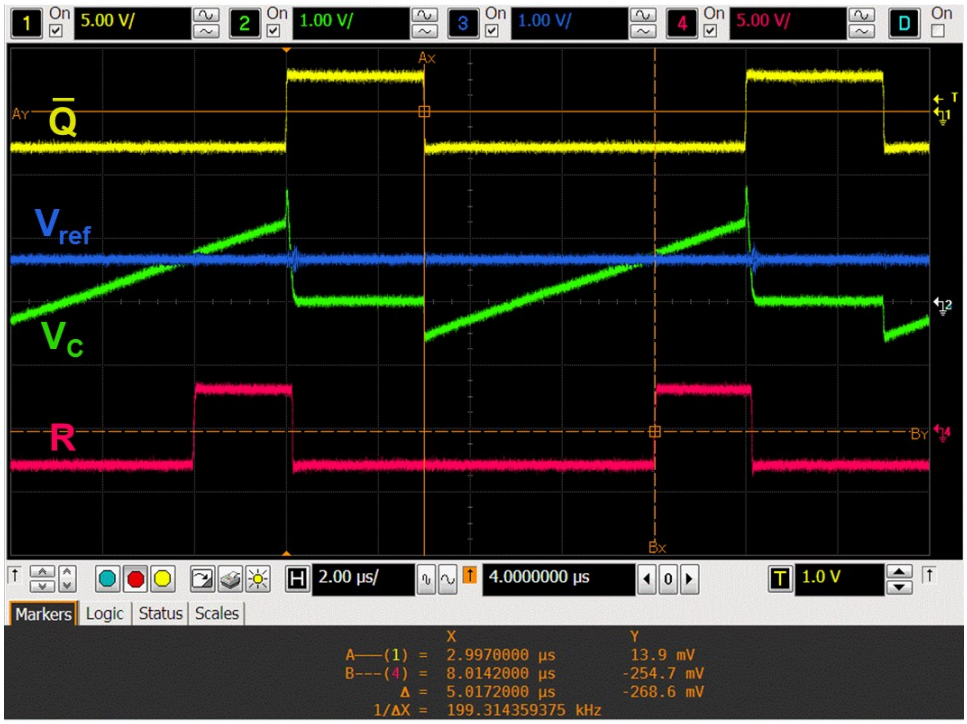


Figure 4.14 Test result of timer

After tuning V_{ref} to 1.3V, the period from $\overline{Q}$ falling edge to R rising edge is adjusted to 5µs.

Due to the possible cause illustrated before, the timer has a minimum value of 2µs. Thus the minimum off-time is around 2µs, which causes a bigger range of v_{in} where the MOSFETs off-time is decided by the minimum off-time.

4.3.3 Power Stage

The power stage circuit as shown in Figure 3.5 consists of an inductor, a MOSFET pair, two Shottky diodes and three output capacitors. The MOSFET pair was designed to be integrated. However, the test results show they're not functional. Thus IPP45P03P4L11 and STP27N3LH5 are used to replace the PMOS and NMOS respectively.

4.3.4 ZCD

The logic part in the ZCD block doesn't work in the test. However, the level shifter is tested functional while designed with same devices but higher W/L ratios. So the failure of the ZCD block is highly possibly caused by the low driving ability of the logic gates as the W/L ratios are low. To continue the test, all the logic gates are replaced by commercial chips.

The ZCD block is supposed to detect the inductor zero current point by sensing the inductor voltage at A node and generate a trigger signal as shown in Figure 3.5. To verify the function of ZCD block, PWM signals from function generator are used controlled MOSFET pair, the circuit in Figure 3.5 is tested with positive and negative DC inputs respectively. Since the PWM signals used to control the MOSFET pair has a fix duty cycle, v_L would oscillate freely after the targeted zero crossing point. The ZCD block would considered functional if a pulse can be generated shortly after v_L changes polarity. The results are shown in Figure 4.15 (a) and (b) when the input voltage is positive and negative respectively.

Figure 4.15 (a) and (b) indicate that the ZCD block can successfully catch the zero-current information and generate the ZCD signal after v_L changes polarity.

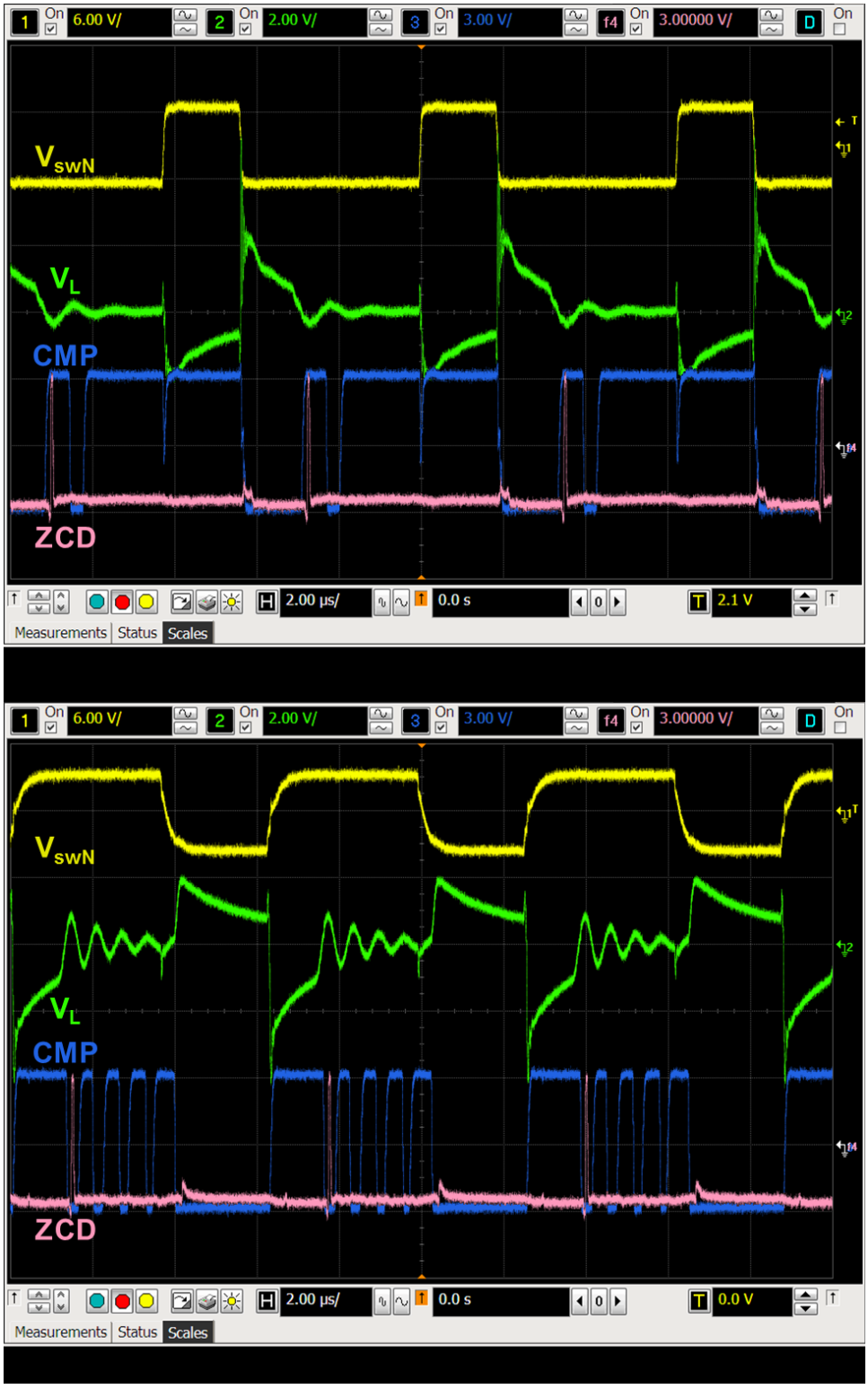


Figure 4.15 Inductor voltage based ZCD

4.3.5 COT Generator

The logic part of the COT generator in Figure 3.11 is also replaced by commercial chips while the other parts in the timers as shown in Figure 4.12 remain integrated. The COT generator is tested individually here. The voltage references in the timers are tuned so that their on-time can meet the design. As illustrated in section 3.3.2, when a ZCD pulse comes, the previous maximum off-time would be reset, and the new constant on-time period would be initiated. When the on-time ends, the minimum off-time and maximum off-time ought to be initiated. Without a new ZCD pulse coming in, the next on-time would be triggered when the maximum off-time ends. The test result of the COT generator is shown in Figure 4.16.

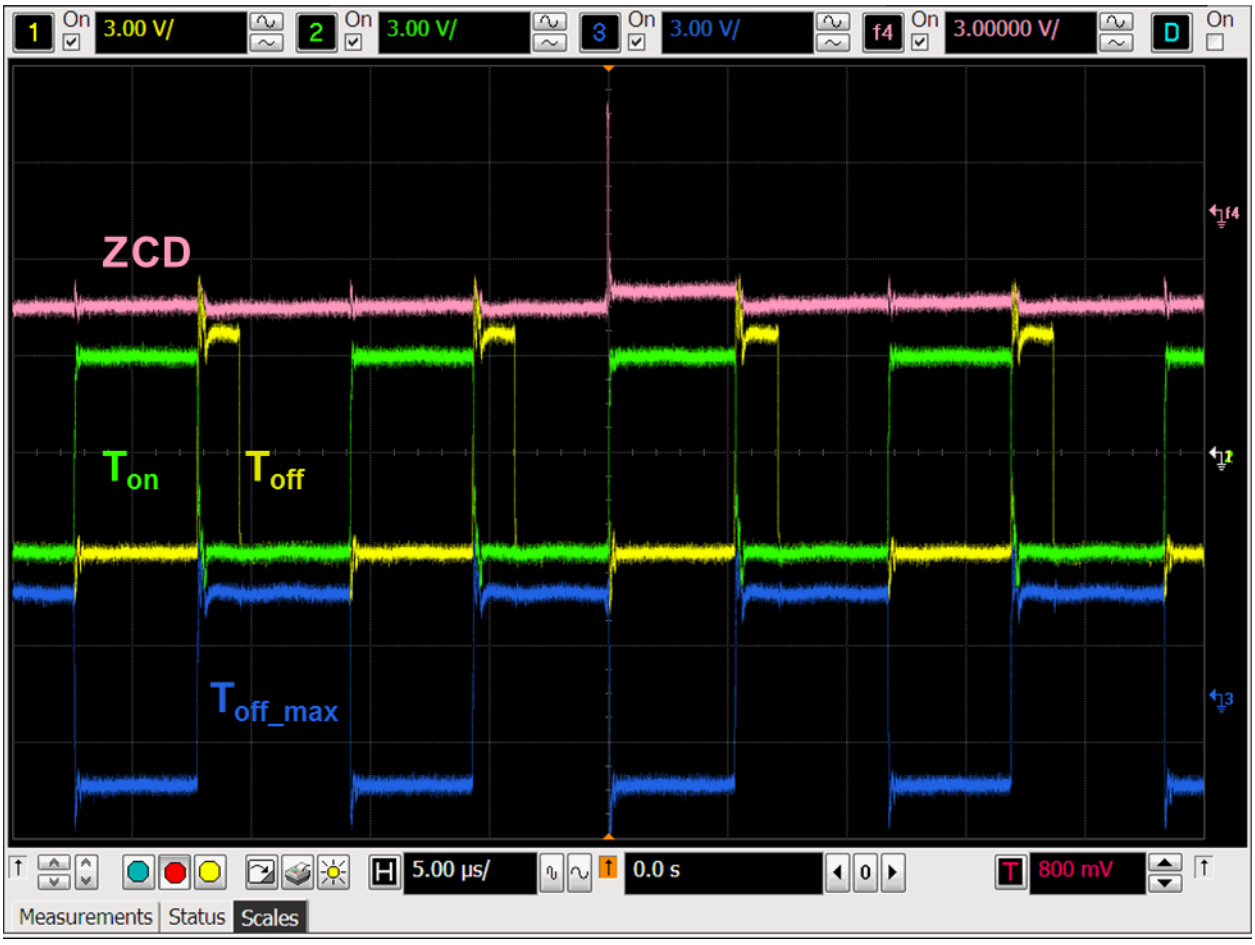


Figure 4.16 COT generator: ZCD triggered T_{on}, T_{off} and T_{off_max}

It can be seen that when a ZCD trigger signal comes, previous maximum off-time T_{off_max} ends immediately. At the same time, a constant on-time T_{on} is triggered. When T_{on} ends, a short

minimum off-time T_{off} and a long maximum off-time T_{off_max} are initiated. Since there's no ZCD pulse coming, the next on-time starts when the maximum off-time ends. These fits the design features of the COT generator.

As the COT generator is functional, it is connected to the ZCD block. The ZCD and COT generator built with discrete logic gates result in a time delay between the targeted ZCD point and T_{on} starting point. This delay is shown in Figure 4.17, which is around 300ns.

Figure 4.17 Inductor voltage V_L triggered COT T_{on}

4.3.6 Modified Test Circuit

The block level test results are summarized in Table 4.

Table 4: Test Results Summary

	Test Result
Current Bias	Works
Band-gap Reference	Works
Power MOSFETs	Doesn't work

Gate Driver	Doesn’t work
Op-amp	Limited input range
Comparators	Work
Logic Gates	Doesn’t work
Timer	Can be improved
Level Shifter	Works
LDO	Doesn’t work

The modified circuit for testing is shown in Figure 4.18 where the voltage sensing circuit is replaced by the revised one in Figure 4.10 and a 5μA current is added to each timer. Section 4.3.7 to 4.3.9 show the test results of this modified circuit.

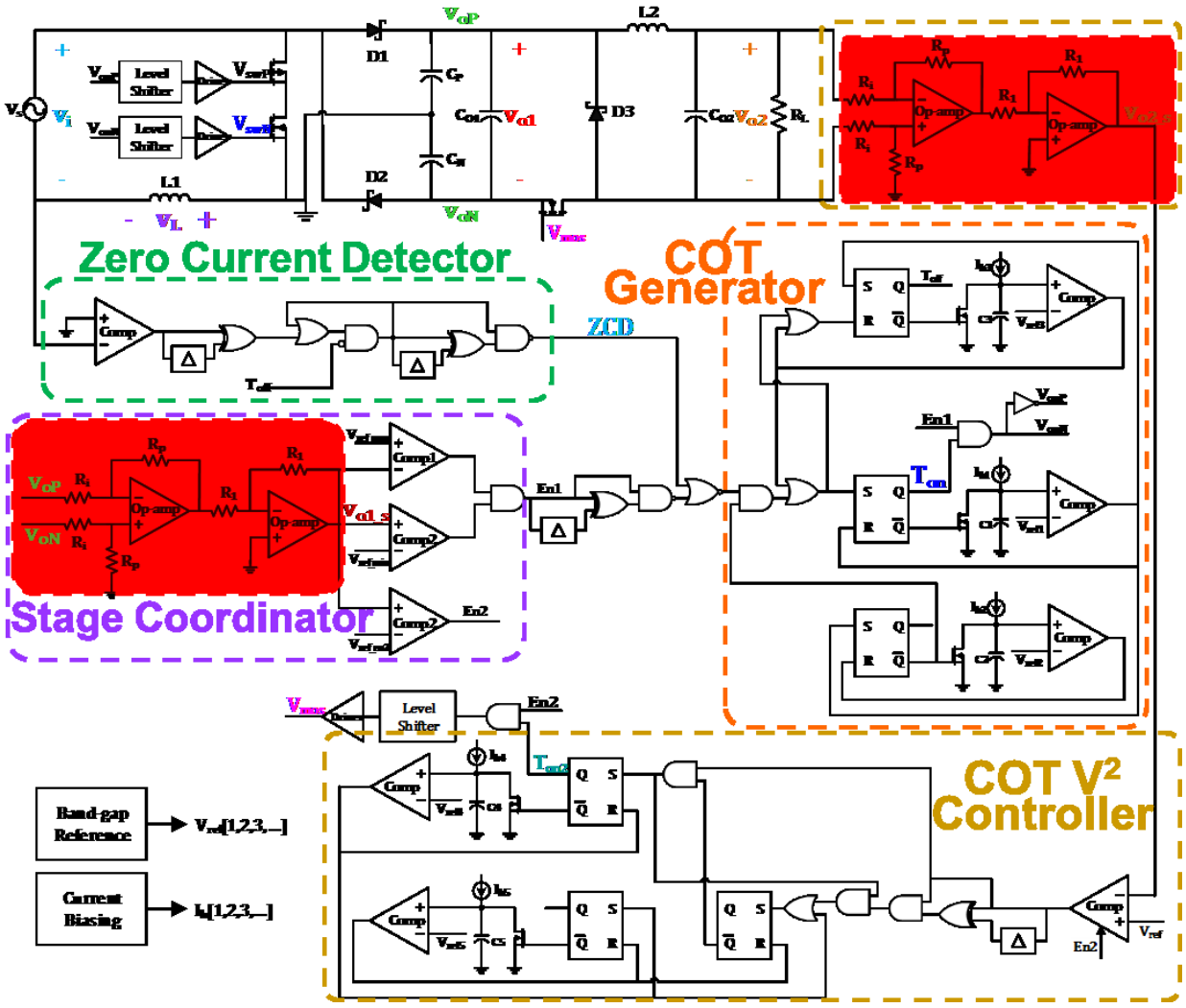
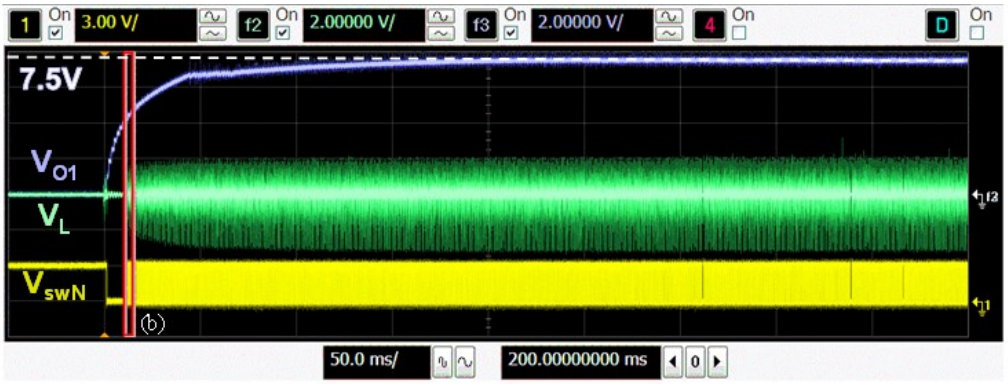


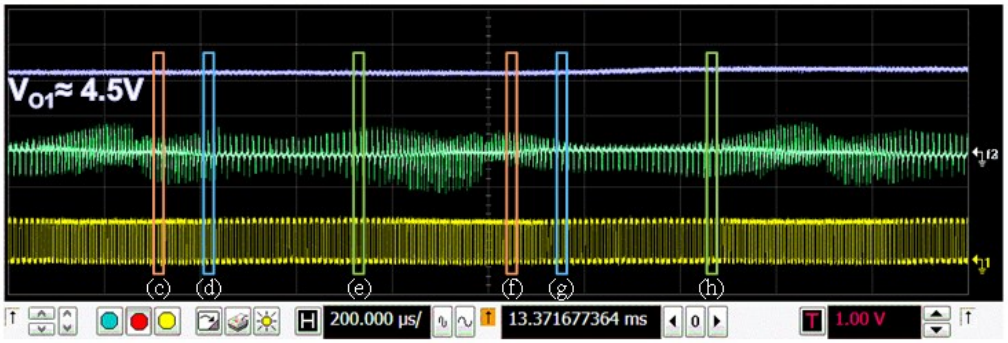
Figure 4.18 Modified test circuit

4.3.7 Boost Rectifier

To test the boost rectifier part, related blocks including boost rectifier power stage, Zero Current Detector, COT Generator and Stage Coordinator are connected as shown in Figure 4.18 and tested. The results are shown in Figure 4.19 (a). To verify the operation as illustrated in section 3.3.4, the figure is enlarged when v_{O1} is lower and higher than $v_{in,p-p}$ as shown in Figure 4.19 and Figure 4.20 respectively.

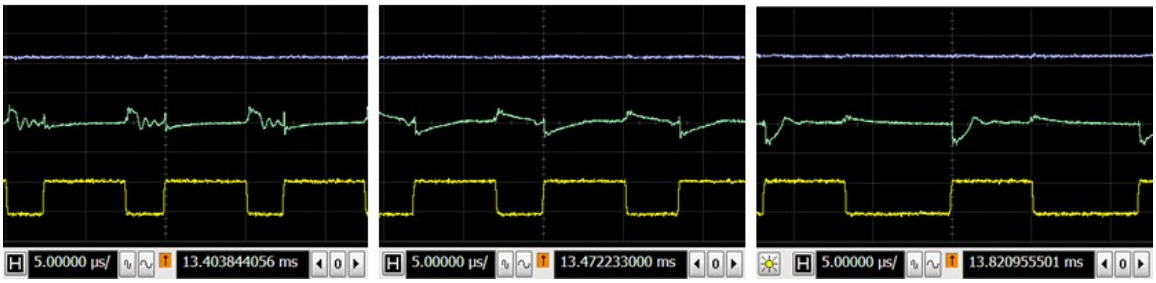


(a)



(b)

(c) (d) (e)

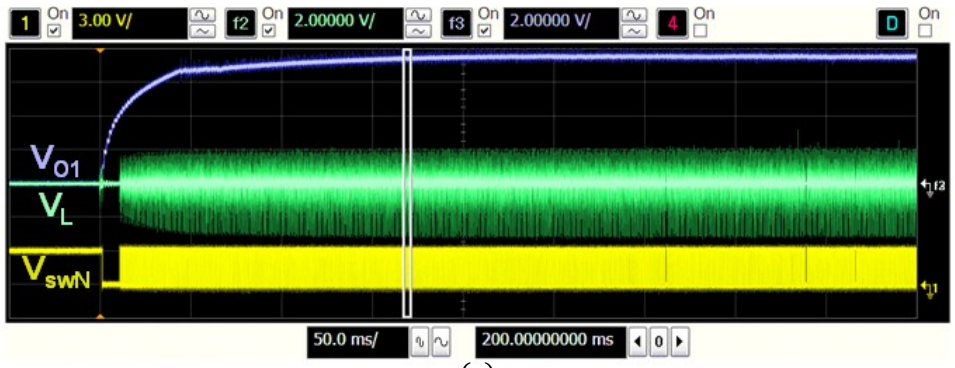


(f) (g) (h)

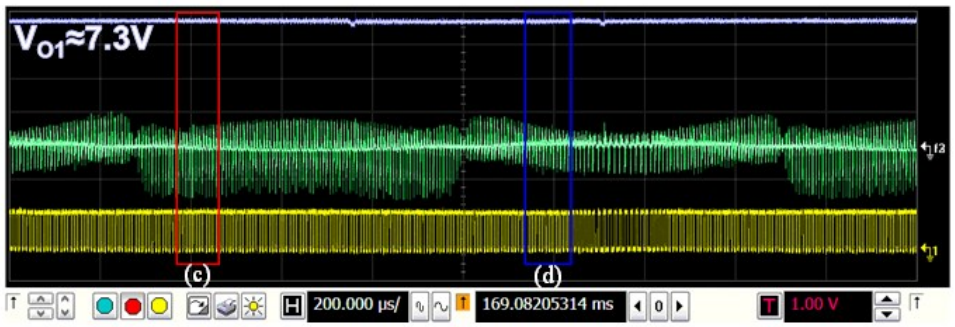
Figure 4.19 Boost rectifier (a) test results, (b) enlarged to one input cycle when $v_{O1}<V_{in,p-p}$, (c) when v_{in} is very low during positive half cycle, (d) when v_{in} is not very low and MOSFETs off-time is decided by ZCD during positive half cycle, (e) when v_{in} is close to V_p, (f) when v_{in} is very low during negative half cycle, (g) when v_{in} is not very low and MOSFETs off-time is decided by ZCD during negative half cycle, (h) when v_{in} is close to $-V_p$

Figure 4.19 (b) enlarges the squared part in Figure 4.19 (a), which is about one input cycle when $v_{O1} < V_{in,p-p}$. This period is targeted to match the waveforms shown in Figure 3.16 (a). Figure 4.19 (c)-(h) enlarge different periods in Figure 4.19 (b). Figure 4.19 (c) (d) (e) are in the v_{in} positive half cycle. Figure 4.19 (c) shows when the $|v_{in}|$ is very low, the MOSFETs on-time equals to T_{on}, and off-time equals to the minimum off-time T_{off}. With $|v_{in}|$ increases, as shown in Figure 4.19 (d), the MOSFETs off-time ends when the inductor voltage triggers the next on-time through ZCD. In Figure 4.19 (e), when the $|v_{in}|$ is close to V_p, the off-time is decided by the maximum off-time. Similar for Figure 4.19 (f) (g) (h) during the v_{in} negative half cycle. These verify the targeted control designed for the boost rectifier when $v_{O1} < V_{in,p-p}$ as illustrated in section 3.3.4.

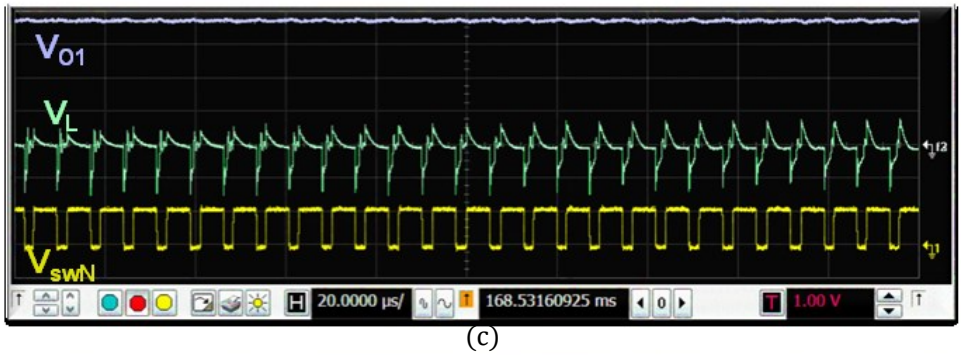
Figure 4.20 (a) is the same figure as Figure 4.19 (a). In Figure 4.20 (b), it enlarges the squared period in Figure 4.20 (a), which is about one input cycle when $v_{O1} > V_{in,p-p}$. This period is targeted to match the waveforms shown in Figure 3.16 (b). Figure 4.20 (c) (d) enlarge different periods in Figure 4.20 (b). From Figure 4.20 (c), it can be seen that, during the positive half cycle, when $|v_{in}|$ is very low, the MOSFETs off-time is decided by the minimum off-time; while $|v_{in}|$ increases, the MOSFETs off-time ends by the ZCD signal instead. Similar for the negative half cycle as shown in Figure 4.20 (d). These verify the targeted control designed for the boost rectifier when $v_{O1} > V_{in,p-p}$ as illustrated in section 3.3.4.



(a)



(b)



(c)

(d)

Figure 4.20 Boost rectifier operation (a) test results, (b) enlarged to one input cycle at $v_{O1}>V_{in,p-p}$, (c) during the positive half cycle off-time changes when v_{in} increases from low voltage value, (d) during the negative half cycle off-time changes when v_{in} increases from low voltage value.

4.3.8 Buck Converter with COT V^2 Control

The COT V^2 controlled buck converter part of the circuit shown in Figure 4.18 is designed to regulate the output voltage to have a valley voltage of 5V. The test results are shown in Figure 4.21. The actual on-time of the buck converter is tuned to 7µs.

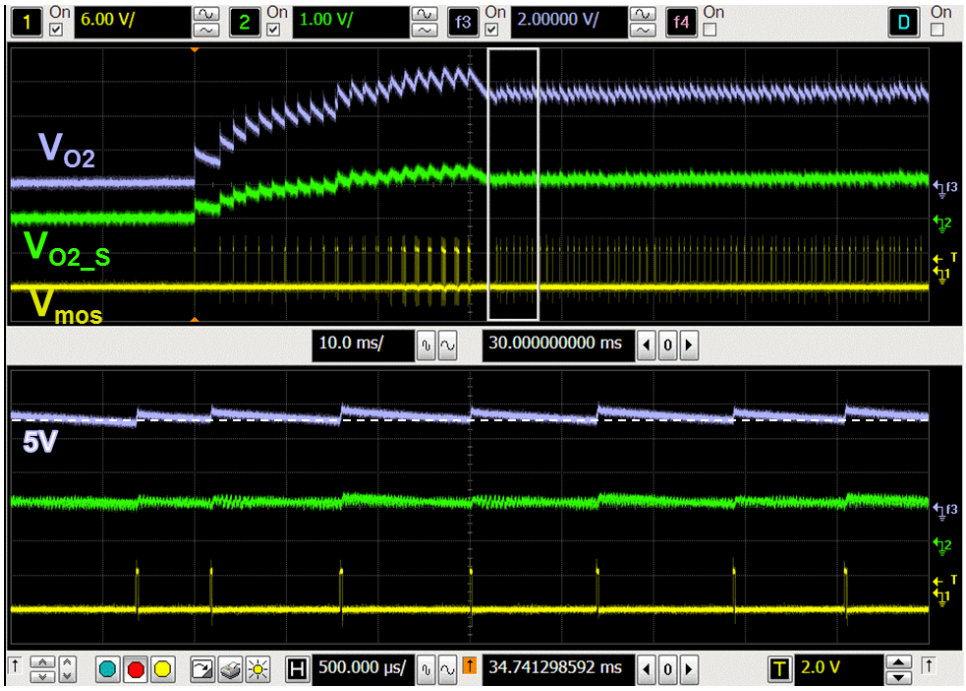


Figure 4.21 Buck converter operation

From Figure 4.21, it can be found that v_{O2_S} follows v_{O2} and is roughly 1/5 of v_{O2}, which indicates the right results from the revised voltage sensing circuit shown in Figure 4.10. Also, the v_{O2} has a valley voltage of 5V, which is the same as the design stated in section 3.4.2.

4.3.9 Stage Coordinator

The stage coordinator senses the rectifier output v_{O1} through a differential amplifier. Then the sensed voltage v_{O1_S} is compared with different references and decide when to enable the boost rectifier and when to enable the following buck converter.

The output voltages of the boost rectifier and buck converter are shown in Figure 4.22.

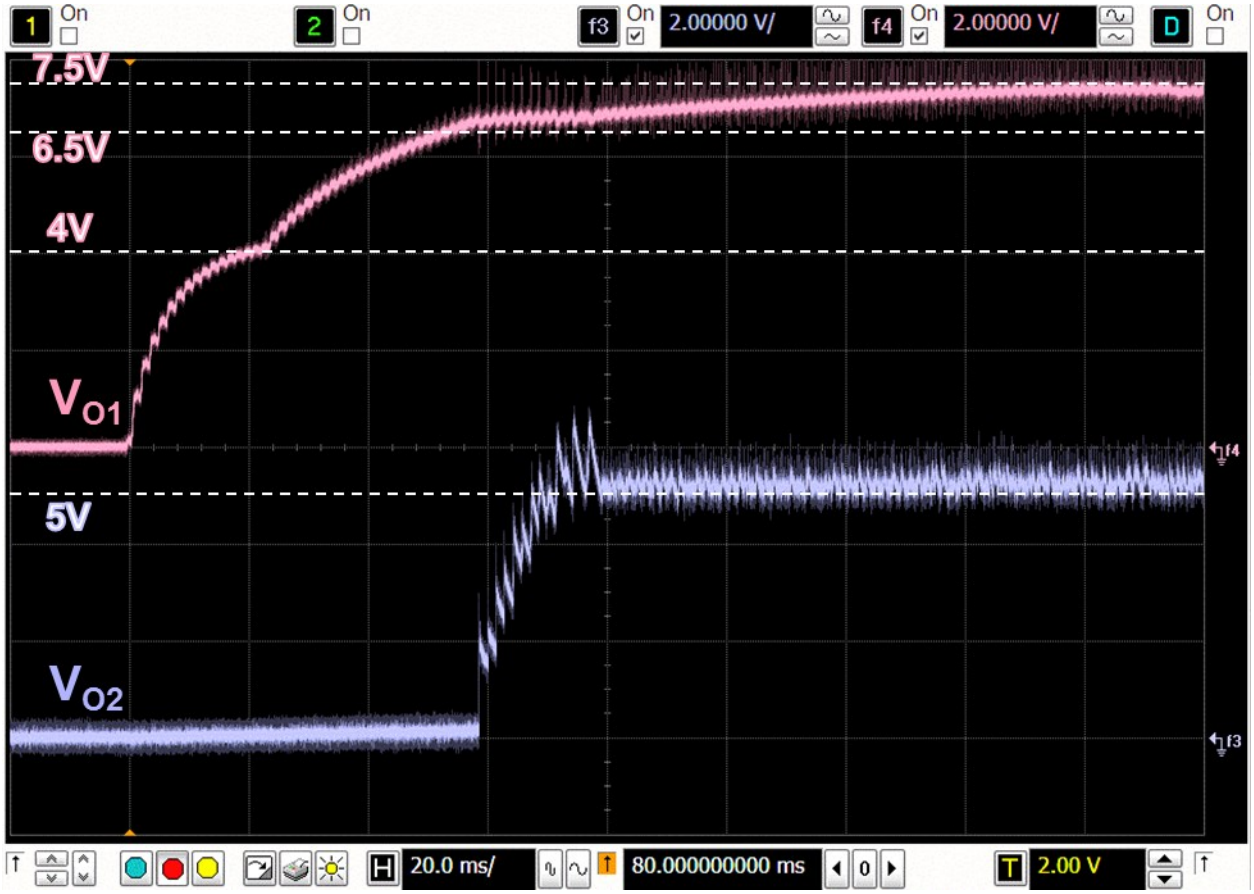


Figure 4.22 Boost rectifier and buck converter output voltages

From Figure 4.22, it can be found that v_{O1} increases faster after 4V since the boost rectifier controller is enabled. And when v_{O1} is charged to 6.5V, v_{O2} starts to be charged up and regulated to 5V. When v_{O1} reaches 7.5V, boost rectifier controller is disabled so v_{O1} won't increase further. These match the designed functions for the stage coordinator as listed in Table 3.

4.4 Chapter Summary

In this chapter, the proposed EH circuit is simulated in Cadence and tested along with discrete components on a breadboard. Its layout drawn in Cadence is shown with dimensions. Blocks with different functions are highlighted. The simulation results verify the ZCD design, BCM operation, and the cold start capability. The overall simulation of the EH circuit shows the boost rectifier can cooperate with the buck converter to provide a stable 5V output. The measurement results are also included in this chapter. Since part of the IC couldn't work, with some replaced by commercial parts, the test results verify the proposed control method for boost

rectifier. The system is functional with external supplies, logic part and MOSFET pair replaced by commercial components. But due to the delay comes along with building the logic part with commercial chips and noise from connecting the parts on breadboards, the circuit performance is not good.

Chapter 5

Conclusion

In this paper, an energy harvesting circuit designed for EMGs is presented. It adopts a single stage rectifier topology, which realize the rectification and boosting of the AC input from EMG at the same time. The boost rectifier is proposed to operate in BCM in order to match the EMG impedance and achieve maximum power extraction. To implement BCM, a ZCD method of sensing inductor voltage to detect current zero crossing point regardless of input voltage polarity is proposed. The rectifier is followed by a buck converter to regulate the output voltage to 5 V to power devices through USB ports.

The circuit is designed and taped out in 0.18 μm BiCMOS technology. Cadence simulation results validate the correct operation of the proposed circuit. The test is only done with external supplies and nonfunctional parts replaced by discrete components. It verifies the proposed control method for the boost rectifier. But the performance need to be improved.

A few future research areas to improve the proposed EH circuit are suggested below.

The proposed circuit can't deal with EMG amplitude as low as 0.3V in the specification. Thus another circuit targeting low input range such as charge pump and/or voltage doubler ought to be designed in addition.

The power dissipation on diodes could be reduced by replacing with or bypassing with active diodes. The active diode is form by an op-amp controlled MOSFET. In low power application, MOSFETs with low on resistance could dissipate less power than diodes. A common-gate amplifier can be designed to deal with the high common mode input voltage to the op-amp.

The boost rectifier adopted in this design has an output that is not grounded. The positive terminal is higher than 0 while the negative terminal is lower than 0. They are taken advantaged being used in internal supply to control the MOSFET pair in the proposed EH circuit. However,

the dual supply adds the complexity of the IC design and layout as two sets of voltage references, LDOs are required for positive and negative supply respectively. Besides, isolated devices with more layers are chosen to suppress the influences between different voltage levels. In this aspect, topologies with positive grounded output like dual boost or totem-pole are worth considering.

The control method of the buck converter can also be optimized to reduce the power loss of the controller. Simple control methods such as band-band control is worth investigated.

Other than EH circuit, the IC design could also be improved in the following areas.

The logic parts of the IC couldn't work highly possibly because of the W/L ratio of CMOS devices are designed not high enough. Increasing the W/L ratio would increase the driving ability and thus address this issue. Then control response can be faster, so the designed BCM can be achieved.

Other parts with issues including power MOSFETs, op-amp, NMOS in the timer could be caused by layout problems. Devices with isolation are used in this design to suppress the influences between different voltage levels. However, it adds extra layers and extra area to the layout, which introduce more parasitic. The layout issues should be further investigated so that they could be avoided in the future work. Extra attentions should be paid when laying out differential pairs and current mirrors. Adding dummy devices to achieve better matching.

Corner simulation of devices under different temperatures should be done in Cadence to assure the performance under different scenarios. Trimming circuits can be added to adjust the resistor value in key blocks such as bandgap reference to minimize the error.

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