# Design and Validation of a High-Density 10 kV Silicon Carbide MOSFET Power Module with Reduced Electric Field Strength and Integrated Common-Mode Screen

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## ABSTRACT

Advanced power electronics with improved efficiency, power density, reliability, and functionality will be critical in the future of motor drive, transportation, renewable energy, data center, and grid industries. In particular, silicon carbide (SiC) power semiconductors are enabling power electronics to meet growing demands, and have begun appearing in commercial products, such as traction and solar inverters, and uninterruptable power supplies. Even greater strides can be made in high-power systems due to the high breakdown electric field of SiC, which enables the fabrication of unipolar power devices with voltage ratings exceeding 10 kV. The ability of these devices to efficiently switch higher voltages at greater frequencies will revolutionize existing application areas and fuel emerging ones.

However, the current power module packages are limiting the performance of these unique switches. The objective of this research is to push the boundaries of high-density, high-speed, 10 kV power module packaging. The proposed package addresses the well-known electromagnetic and thermal challenges, as well as the more recent and prominent electrostatic and electromagnetic interference issues associated with high-speed, 10 kV devices. This dissertation will discuss the design, prototyping, and testing of an optimized package for 10 kV SiC MOSFETs.

The proposed power module achieves low and balanced parasitic inductances due to the embedded decoupling capacitors and symmetric layout, resulting in record switching

speeds of tens of nanoseconds with negligible ringing and voltage overshoot. An integrated screen contains the common-mode current that is generated by these fast voltage transients within the power module, rather than flowing to the system ground. This screen connection simultaneously increases the partial discharge inception voltage by reducing the electric field strength at the critical triple points of the insulating ceramic substrate. Further, a compact termination and system interface design is proposed that avoids exposed conductors, and includes field-grading plates in the bus bar to reduce the electric field strength in the air. The heat flux is addressed by employing direct-substrate, jet-impingement cooling. The cooler is integrated into the module housing for increased power density. With the integrated cooler included, the power module prototype achieves a power density of 4 $W/mm^3$.

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## GENERAL AUDIENCE ABSTRACT

Electricity is the fastest-growing type of end-use energy consumption in the world, and its generation and usage trends are changing. Hence, the power electronics that control the flow and conversion of electrical energy are an important research area. Advanced power electronics with improved efficiency, power density, reliability, and functionality are critical in data center, transportation, motor drive, renewable energy, and grid applications, among others.

Wide-bandgap power semiconductors are enabling power electronics to meet these growing demands, and have thus begun appearing in commercial products, such as traction and solar inverters. Looking ahead, even greater strides can be made in medium-voltage systems due to the development of silicon carbide power devices with voltage ratings exceeding 10 kV. The ability of these devices to switch higher voltages faster and with lower losses than existing semiconductor technologies will drastically reduce the size, weight, and complexity of medium-voltage systems. However, these devices also bring new challenges for designers.

This dissertation will present a package for 10 kV silicon carbide power MOSFETs that addresses the enhanced electric fields, greater electromagnetic interference, worsened dynamic imbalance, and higher heat flux issues associated with the packaging of these unique devices. Specifically, due to the low and balanced parasitic inductances, the power module prototype is able to switch at record speeds of tens of nanoseconds with negligible

ringing and voltage overshoot. An integrated common-mode current screen contains the current that is generated by these fast voltage transients within the power module, rather than flowing to the system ground. This screen connection simultaneously increases the partial discharge inception voltage by reducing the electric field strength at the triple point of the insulating ceramic substrate. Further, field-grading plates are used in the bus bar to reduce the electric field strength at the module terminations. The heat flux is addressed by employing direct-substrate, jet-impingement cooling. The cooler is integrated into the module housing for increased power density.

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# Chapter 1 Introduction

## *1.1 Motivation and Application Background*

The applications of power electronics are continuously expanding. Power electronics enable transportation electrification [1],[2],[3], renewable energy integration [1],[3],[4], power grid modernization [1],[5],[6], more-efficient data centers [1],[7], and variable-speed motor drives [1],[3], among others. Power semiconductor devices have been critical in this ongoing evolution of power electronics [8]. For several decades, silicon has been the primary semiconductor choice for power electronics applications [8]. Due to its long history, over which tremendous efforts and resources were dedicated to the development and fabrication optimization of silicon devices, as well as the large abundance of material, the manufacturing capability is high, and the costs are low. However, silicon is quickly approaching its limits in power conversion [3],[9]. Wide-bandgap (WBG) semiconductors have demonstrated improved efficiency, reduced size and weight, and lower system cost [2],[6],[3],[9],[10].

Of the various WBG semiconductors, silicon carbide (SiC) is one of the most promising, especially for high-temperature [11], and medium- and high-voltage applications [3],[9],[12]. Currently, medium- and high-voltage systems use silicon insulated gate bipolar junction transistors (IGBT), integrated gate-commutated thyristors (IGCT), or gate turn-off thyristors (GTO). While these devices have proven reliability and

ruggedness, they have several key disadvantages. In particular, they have limited voltage ratings (typically 6.5 kV or less), thus requiring the series connection of devices or multilevel converter topologies [13]. The series connection of devices raises the issue of voltage imbalance, and multilevel converters require additional components and complex control [13]. Moreover, these bipolar silicon devices are limited in terms of switching speeds and losses, which constrains the efficiency and switching frequency of the power converter [14],[15].

SiC power semiconductors are advantageous in these respects. Thus far, medium-voltage SiC MOSFETs [16],[17],[18], junction field effect transistors (JFET) [19],[20], bipolar junction transistors (BJT) [21], IGBTs [22],[23], GTOs [49], and emitter turn-off thyristors (ETO) [50],[51] have been demonstrated. Of these devices, the 10 kV SiC MOSFETs are of great interest due to their high blocking voltage, fast switching speed, simple drivability, reverse conduction capability, and moderate on-state losses. These features can increase the efficiency, reliability, and switching frequency, and reduce the complexity, size, and weight of medium- and high-voltage power conversion systems [23],[24].

In particular, applications in which space and weight savings are valuable could greatly benefit from the use of 10 kV SiC devices. One such application is all-electric ships. In order to improve reliability, survivability, and power quality, future shipboard power systems will upgrade from low-voltage ac to medium-voltage dc [25]. By using 10 kV SiC devices, the large, heavy, low-frequency transformer can be replaced by a smaller, lighter, SiC-based, high-frequency solid state transformer (SST) [26]. Other applications for 10 kV SiC devices include traction [15],[27], data center distribution, direct renewables

integration to a medium-voltage (13.8 kV) grid [22], fast charging stations [28], HVDC [29] and FACTS [30],[31], and transformer-less intelligent power substations (TIPS/SSPS) [22],[24],[26],[32],[33].

Due to the vast possibilities for ≥10 kV SiC devices, many resources have been devoted to their development. Though, to date, the majority of the reports on these devices have been focused on the characterization [12],[18],[24],[26],[34],[35], gate driver design [36],[37],[38],[39], and converter evaluation [24],[35],[40]. However, the packaging of the semiconductor dies has a significant impact on the performance, and is currently limiting their full potential (i.e., their switching speed, voltage rating, current rating, and operating temperature). In fact, it is widely accepted that much of the future progress of power electronics will come from the use of innovative packaging and integration technologies [41],[42],[43],[44]. Consequently, the packaging of these unique devices is critical for their adoption. This work will present the design, fabrication, and testing of an optimized power module package for 10 kV SiC MOSFETs that enables them to switch thousands of voltages in tens of nanoseconds, while having a small footprint, high partial discharge inception voltage (PDIV), and low electromagnetic interference (EMI).

## *1.2 Silicon Carbide Power Devices*

The benefits of SiC arise from its material properties (Figure 1-1). Specifically, SiC has a greater thermal conductivity, lower intrinsic carrier concentration, higher saturation electron drift velocity and critical electric field for breakdown compared to silicon [45],[46],[47]. The higher thermal conductivity of SiC makes it superior to silicon in terms of heat transfer to the environment, which allows for increased power densities

[9],[45],[46]. Additionally, due to the wider bandgap of SiC, it has a lower intrinsic carrier concentration, which allows these devices to operate at higher temperatures without suffering from excessive leakage, hence also allowing for higher power densities [45],[46]. The higher saturation drift velocity also makes SiC suitable for high-frequency applications [46].

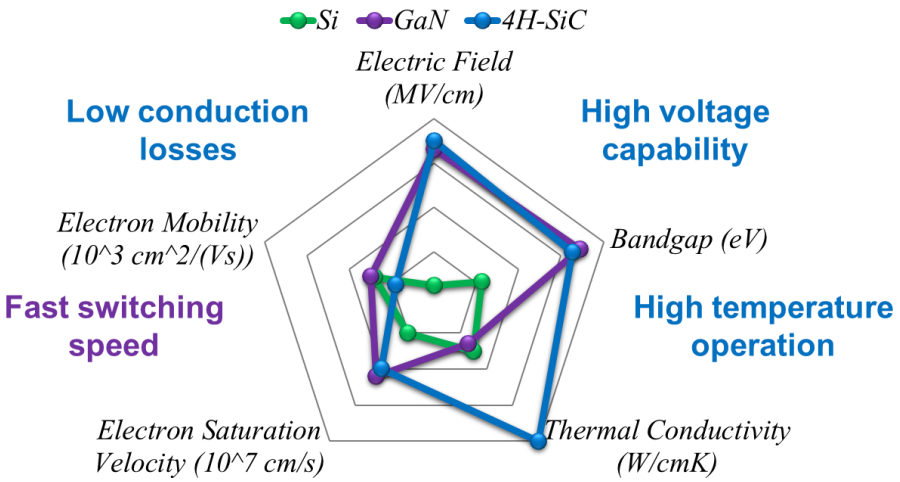



**Figure 1-1: Material properties for silicon (Si), GaN, and 4H-SiC.**

Moreover, SiC has a breakdown electric field that is more than eight times higher than that of silicon [45]. This means, for a given blocking voltage, SiC can be more heavily doped than silicon, thereby reducing the on-state resistance of higher-voltage devices by 200 times [17],[45]. This is significant because the low doping capability of silicon is the reason that the silicon MOSFET is not typically used beyond 600 V. Instead, at 1200 V and above, silicon bipolar devices, such as the IGBT, are more practical due to their lower on-state losses. However, the silicon bipolar devices are typically limited to 6.5 kV, again due to the high on-state losses [48]. Consequently, as mentioned earlier, in order to block higher voltages, devices are connected in series, or multilevel converter topologies are used.

Conversely, the higher doping capability of SiC, allows for the realization of medium-voltage unipolar devices, such as 10 kV and 15 kV SiC MOSFETs [18], with lower on-state losses. Beyond approximately 15 kV, the on-state losses for SiC MOSFETs becomes significant. Accordingly, bipolar devices, such as 15 kV SiC IGBTs [36], 20 kV SiC GTOs [49], and 22 kV SiC emitter turn-off thyristors (ETO) [50],[51] have been explored for higher voltages due to their lower on-state losses. These unipolar and bipolar devices can switch higher voltages, faster, and with lower losses than silicon devices (e.g., 6.5 kV silicon IGBTs) [15],[14]. While the majority of these ≥10 kV SiC transistors are still in the research stage, Wolfspeed, a Cree, Inc. company that has been at the forefront of the development of SiC devices, has recently begun selling their third-generation 10 kV, 350 mΩ SiC MOSFET, which are currently undergoing qualification, to select customers.

## *1.3 Power Module Packaging*

While SiC devices have shown exemplary static and dynamic performance at the discrete level, their performance at higher power levels is currently limited by the module packaging. A traditional power module package is shown in Figure 1-2. Starting from the bottom, a standard power module consists of a thermal management system, such as a heatsink or coldplate, followed by a thermal interface material (TIM) that is used to provide good contact to the baseplate. The baseplate is used in high power modules to spread the heat. An insulating substrate is typically soldered to the baseplate. The insulating substrate provides the electrical isolation between the semiconductor die and the thermal management system (e.g., heatsink). Direct bonded copper (DBC), which consists of a

copper-ceramic-copper structure, is a common type of insulating substrate in power electronics modules.

The semiconductor dies are attached to the topside metallization of the insulating substrate. Solder is a common die attach material, though silver (Ag) sintering is also being adopted for its improved reliability, thermal performance, and high-temperature capability [52]. The connections to the topside of the semiconductor dies are typically made using wire bonds. Terminals are used to connect the potentials within the module to the external circuitry, such as the gate driver and bus bar. Copper (Cu) bus bars are a common choice for the module terminations due to their affordability, ease of manufacturing, and high current capacity. These are typically soldered onto the topside metal of the insulating substrate and protrude through openings in the module housing (not shown). The module is encapsulated with a dielectric material to improve the electrical insulation, as well as to protect the semiconductors from environmental damages (e.g., moisture, corrosion, and radiation). Common encapsulants include potting compounds, such as silicone gels, and molding compounds, which are harder materials.

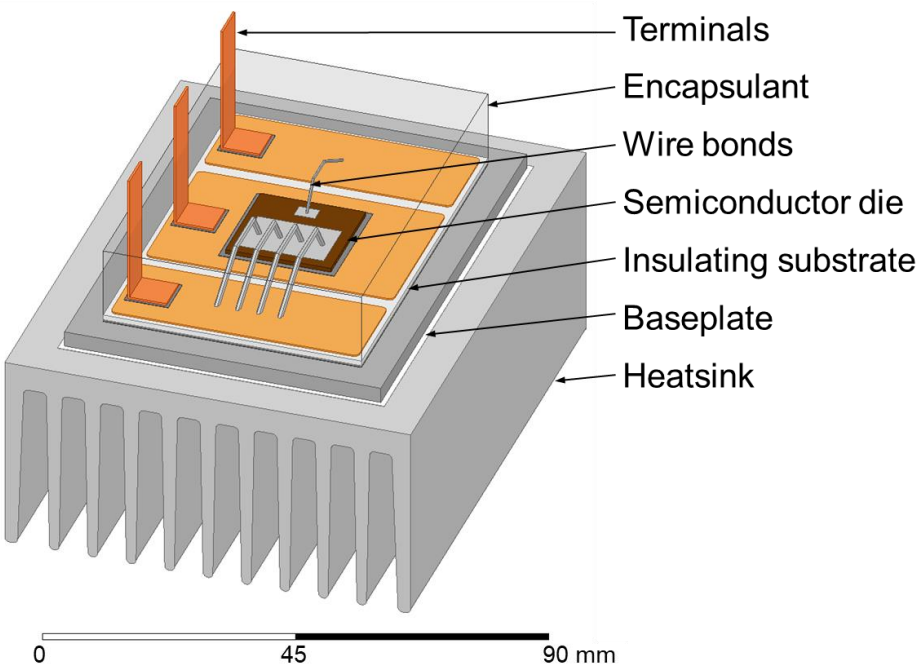



**Figure 1-2: Traditional power electronics structure.**

## *1.4 Research Objective and Challenges*

The objective of this research is to push the boundaries of high-density, high-speed, 10 kV power module packaging. The proposed package addresses the well-known electromagnetic and thermal challenges, as well as the more recent and prominent electrostatic and electromagnetic interference issues associated with high-speed, 10 kV devices. In the remainder of this chapter, these major challenges associated with packaging high-speed, high-voltage devices will be identified. A brief overview of the solutions proposed in the literature for each of these challenges will be presented, followed by the approaches taken in this work.

Due to their faster switching capability, SiC devices are more sensitive to parasitic elements in the module package, as well as in the bus bar and gate driver circuitry, than silicon. In particular, parasitic inductances can resonate with the device parasitic

capacitances, causing undesirable ringing that increases EMI [53]. Also, during high speed current transients (*di/dt*), these parasitic inductances can cause disastrous overvoltage across the drain-source of the device. This is particularly a concern in the event of a short-circuit fault since the *di/dt* values can far exceed those seen during normal operating conditions. In order to mitigate these issues, it has become common practice to increase the gate resistance of the device in order to slow down the switching speed. This is not an ideal solution since it increases the switching losses, and thus reduces the efficiency of the module, thereby diminishing the incentive to use the more-expensive SiC devices.

Instead, it is preferable to develop a module package with lower parasitic inductances. In an effort to reduce the parasitic inductances in the module package, several research groups and manufacturers have opted to replace the traditional wire bond interconnections with ribbon [54],[55]; flexible PCB [56],[57],[58],[59],[60], solid posts, shims, or bumps [61],[62],[63]; solder balls or ball grid arrays [64]; direct-bonded solder [65]; or vias in PCB or ceramic substrates [66],[67],[69],[68]. Several packages also include integrated decoupling capacitors to help mitigate the impact of stray inductances [67],[70],[71],[72],[73]. However, to date, these low-inductance packages have primarily been tested with silicon and SiC devices with voltage ratings of 1.2 kV or less.

One of the exceptions is a flip-chip sandwich structure used to package 3.3 kV silicon IGBTs [62]. However, no electric field analysis or partial discharge (PD) tests were performed to ensure the package could reliably operate at the rated voltage. In [65], a sandwich structure with ceramic substrates on the top and bottom was used for a 6.5 kV silicon super GTO (SGTO). The SGTO was connected to the substrates with solder preform [65]. An electric field simulation was presented to show that the peak electric field

strength exists in the gap between the top surface of the SGTO die and the bottom surface of the top substrate [65]. Since the SGTO die is only 0.5 mm thick, the thickness of the solder preform between the die and the top substrate was increased to reduce the electric field in this region [65]. However, it was shown that increasing the solder preform thickness increases the device junction temperature [65]. Additionally, benzocyclobutene (BCB) was used as a passivation layer on the substrates due to its high electric field strength [65]. Since the BCB coating is thin, an additional underfill was also used [65]. It should be noted that the only experimental test was of the leakage current at the rated device voltage of 6.5 kV [65], which does not test the ability of the module to operate at the rated voltage for longer periods of time.

It is not trivial to adapt most of the packages proposed in the literature for SiC devices with blocking voltages of 10 kV or greater. In this work, the sandwich structure concepts presented in [61] and [62] are modified to create a low-inductance power module that is suitable for 10 kV SiC MOSFETs. The resulting module has gate- and power-loop inductances of 3.8 nH and 4.4 nH, respectively, per MOSFET die. Electric field simulations and PD tests were also performed to design and verify the module's ability to operate at the rated voltage.

Furthermore, in order to increase the current rating of a power module, several dies are connected in parallel. If there exists a wide variation in the parasitic inductances for each of the paralleled dies, then current imbalance can occur during the switching transients. It has been shown for a commercial silicon IGBT module that the current overshoots for each of the paralleled dies can vary by more than two times [74],[75]. The dies that experience the higher current overshoots will have larger switching losses

[74],[75], and thus higher junction temperatures [75], which can reduce the overall lifetime of the module. Since SiC transistors are faster than silicon IGBTs, this problem is intensified. Consequently, to prevent severe current imbalance and circulating currents within the module, many commercial SiC power modules include embedded gate resistors. These resistors slow down the device switching, which reduces the sensitivity to parasitic inductances, but, as mentioned previously, also increases the switching losses, thereby diminishing the high-speed, high-efficiency advantages of SiC devices. By lessening these benefits of SiC, the higher cost may no longer be justifiable.

Alternative solutions include embedding capacitors and creating a symmetric layout for the dies [70],[72]. However, since the modules in [70],[72] use wire bonds for the interconnection, the capacitors must be placed beside the dies, thereby increasing the footprint of the module. Instead, in [67], the capacitors are placed above the semiconductor devices, creating a vertical high-frequency power loop that does not increase the module footprint, as it takes advantage of the third dimension. In this work, this vertical-capacitor-loop concept was adopted with some modifications. Each MOSFET switch pair has its own set of embedded decoupling capacitors located above it, resulting in a symmetric power loop inductance of just 4.4 nH for each. Additionally, each MOSFET has its own gate and Kelvin source connection to the external gate driver, yielding symmetrical gate-loop inductances of 3.8 nH for each, thereby further improving the dynamic current sharing.

In addition to having high stray inductance and increasing the module footprint, wire bonds can also reduce the reliability of the power module; cracking, lift-off, and aluminum (Al) metallization reconstruction are all common failure mechanisms, and are primarily due to thermomechanical stresses experienced during normal operation [77].

Additionally, wire bonds cannot absorb the large amounts of energy that occur during faults (e.g., short circuit) [76]. When the amount of energy exceeds the limit of the wire bonds, they fail as an open circuit [76]. In many high-voltage, high-power applications, such as HVDC, an open-circuit failure mode is undesirable. In [76], it was shown that the sandwich structure could maintain a short-circuit failure mode under 12 times more energy than wire-bonded samples, and 2.4 times more energy than samples with flexible PCB interconnection.

Press-pack modules, which use pressure contacts instead of wire bonds, are the current state-of-the-art for many high-voltage, high-power systems due to their short-circuit failure mode, improved reliability, double-sided cooling, and more uniform impedances for the paralleled dies [118]. However, there are several notable disadvantages, including a complex and bulky clamping system, which is needed to ensure the applied pressure is homogeneous [118]. If the pressure is not uniformly distributed to all the dies, then the thermal and electrical contact resistances could vary drastically. Accordingly, to achieve a high-density design that is capable of withstanding high-energy faults, a pressure-less sandwich structure is adopted in this work.

Additionally, there exists a parasitic capacitance across the insulating ceramic substrate (e.g., DBC). Since the cooling system (e.g., heatsink or coldplate) is generally grounded for safety, under high speed voltage transients (*dv/dt*), this parasitic capacitance becomes a path for common-mode (CM) current to flow through the system ground [72]. This problem is especially critical for the fast-switching SiC devices, which have higher *dv/dt* transients than silicon IGBTs. Typically, filters and/or chokes are added to help reduce the EMI; however, these add cost, size, and complexity to the power conversion

system. A simpler solution that requires fewer additional components is the implementation of a screen layer that returns the CM current back to the dc bus [78]. An improved CM current screen that is fully integrated into the power module is proposed in this work. The proposed screen is capable of reducing the ground current by 10 times.

Furthermore, the desire to create a high-density package for medium-voltage devices means the electric field strength within the module will be increased. If the electric field strength exceeds the electrical breakdown strength of the dielectric materials, then PD can occur, potentially causing permanent damage to the insulating materials, such as the insulating ceramic substrate [79]. Accordingly, the electric fields, both within the power module and at the external terminations to the rest of the power conversion system, must be carefully controlled. Recently, there has been focus on reducing the electric field strength near the insulating substrate, as this is typically where the PD occurs inside the power module [80],[81],[82].

Proposed solutions to reduce the electric field strength at this critical location include: increasing the ceramic thickness [79] and the permittivity of the encapsulation material [83]; adding a dielectric coating with high permittivity [84] or high breakdown field strength [85]; applying a high resistivity coating along the ceramic surface [85],[86]; using high permittivity non-linear dielectrics [87] or nonlinear resistive gel [88]; stacking multiple substrates [89]; and varying the metal-ceramic interface geometry [85],[90]. Of these methods, those that are simple to implement have limited improvement on the PD inception voltage (PDIV), and those that have the highest improvement are complicated to fabricate or have questionable reliability. Furthermore, none of these methods have been implemented and tested in an actual power module. In this work, a modified stacked

substrate approach is adopted, resulting in a 53 % increase in the PDIV without significantly impacting the thermal or electrical performances of the power module. This approach also acts as the CM screen mentioned earlier.

The electric field outside of the power module is also critical due to the low dielectric strength of air. To date, little work has been published on the analysis of the electric field at the module–system interface. In [91], the electric fields in the module bus bar were analyzed, though there was little discussion about the module–bus bar interface. In this work, the module housing and bus bar interface are carefully designed to comply with creepage and clearance standards, and to minimize the electric field strength in the air in order to increase the PDIV. Field grading methods were also applied to the gate driver board that interfaces with the power module. With these methods, the PDIV of the board increased by five times. This is the first work reported in the literature to implement and test advanced electric field reduction methods both internal and external to the package of a high-density 10 kV SiC MOSFET power module. Moreover, this work also presents a module–system interface scheme that avoids exposed conductors, thereby circumventing creepage and clearance standards that would otherwise limit the minimum size of the power module.

In the next chapter, Wolfspeed's first- and third-generation 10 kV SiC power modules are evaluated, and areas for improvement are identified. Other state-of-the-art and research-level medium-voltage power modules for silicon and SiC devices are reviewed. In Chapter 3, the design of the proposed 10 kV SiC MOSFET power module is explained and justified in detail. The materials, components, and methods used to prototype the designed module are discussed and evaluated in Chapter 4. The experimental

characterization and testing of the fabricated prototypes are then presented to validate the design. In Chapter 5, the analysis, implementation, and testing of the integrated CM screen are presented. Finally, Chapter 6 will discuss the key conclusions and opportunities for future work.

# Chapter 2 Medium-Voltage Power Module Evaluation

## *2.1 Introduction*

Cree, Inc. has been at the forefront of the development of SiC wafers and power semiconductor devices for over a decade, releasing the first 1.2-kV SiC Schottky diode in 2006, followed by the first SiC power MOSFET in 2011. However, while Cree, Inc. is a world leader in SiC wafers and power devices, the traditional discrete and module packages were hindering the semiconductor performance. To overcome this bottleneck, in 2015, Cree, Inc. acquired APEI (Arkansas Power Electronics International, Inc.), a frontrunner in high-end power module packaging. Together, APEI and the Power and RF group at Cree, Inc. formed Wolfspeed. Wolfspeed is currently the world's largest SiC and GaN power and RF fabrication facility in the world, and now offers greatly improved packages that result in better electrical performance of the SiC power modules.

In 2010, Cree, Inc. published on the world's first 10 kV, 120 A SiC power module. However, at the time, much of the effort was focused on the design and fabrication of the 10 kV SiC devices themselves, and little work had been done on the packaging. As such, a modified version of a standard package typically used for 6.5 kV silicon IGBTs was used. These modules were characterized and integrated into a power electronics building block (PEBB) for a more-electric ship application [92],[93],[94]. Unfortunately, it was

discovered that this package was hindering the full capability of the 10 kV SiC devices, and even limited the operating conditions for the developed converter. Accordingly, in 2016, after the APEI acquisition, Wolfspeed developed an improved package for their latest-generation 10 kV SiC MOSFETs. In this chapter, the characterization and testing of these power modules will be presented, followed by a discussion on both commercial and research-level packages for medium-voltage silicon and SiC power devices.

## *2.2 First-Generation 10 kV, 120 A SiC MOSFET and JBS Diode Module*

The development of 10 kV SiC MOSFETs [95], and 10 kV SiC junction barrier Schottky (JBS) diodes [96] gave rise to the first 10 kV SiC MOSFET power module in 2012 [97]. The modules are in a phase-leg configuration, with each switch (high side and low side) comprising twelve parallel 10 kV, 10 A SiC DMOSFETs, and six parallel 10 kV, 10 A SiC junction barrier Schottky (JBS) diodes, yielding a current rating of 120 A [97]. These first-generation modules were critical components in the development of a high-density 1 MVA solid-state power substation, which employed soft switching techniques and was capable of switching up to 20 kHz [98]. When compared with 6.5 kV silicon IGBT modules, these 10 kV SiC modules demonstrated higher efficiency and switching frequency potential [14].

## *2.3 10 kV SiC-Based Power Electronics Building Block (PEBB)*

The concept of a PEBB is the integration of fundamental components, such as power devices, gate drivers, and control schemes, which can be used in a variety of

applications [99],[100]. This concept offers high-scalability and enables various power conversion topologies to be implemented. Through series and parallel connections of the PEBB units, virtually any desired voltage, current, and power rating can be achieved. The versatility of the PEBB allows for high return on investment, and also has the potential to reduce the cost, size, weight, loss, design complexity, installation, and maintenance of power electronics systems [99],[100]. In the design of a PEBB, stress on the power devices, parasitic inductances, switching speed, losses, thermal management, and protection must all be taken into consideration [99],[100]. Accordingly, WBG semiconductors are of great interest due to their superior electrical and thermal properties. In particular, the high critical electric field and thermal conductivity of SiC allow for the conception of high power, efficient, and compact PEBBs.

The schematic for the PEBB developed in this work is shown in Figure 2-1a, and the specifications are listed in Table 2-1. Each PEBB includes an H-bridge, which is comprised of two first-generation 10 kV, 120 A SiC half-bridge modules [98], gate drivers, decoupling capacitors, and liquid coldplates (Figure 2-1c). The H-bridges were designed and assembled by General Electric. The PEBB also includes dc-link capacitors, arm inductors, and a 6.5 kV IGBT that protects the H-bridge from the energy stored in the bulk capacitors in the event of a fault (Figure 2-1a). Each PEBB also features a high-speed digital controller, and an uninterruptable power supply. The developed PEBB has a volume of 0.69 $m^3$, and a power density of 1 $MW/m^3$. This high power density is greatly due to the fast switching of the 10 kV SiC module, and makes these PEBBs ideal for the power systems of next-generation electric ships. Further details of the PEBB can be found in [92].

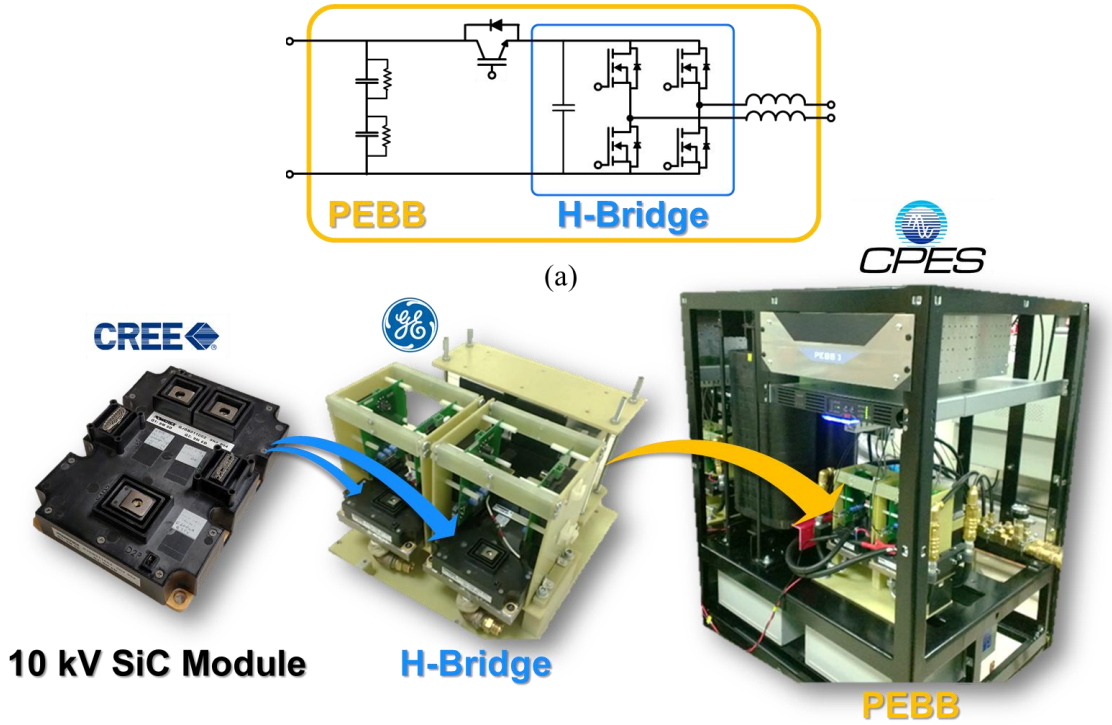



**Figure 2-1: (a) PEBB schematic, (b) first-generation 10 kV, 120 A SiC module, (c) H-bridge, and (d) PEBB.**

**Table 2-1: PEBB Specifications**

| | |
|---|---|
| DC voltage | 5 kV |
| AC voltage | 4.16 kV |
| Current | 100 A |
| Switching frequency | 10 kHz |

### *2.3.1 First-Generation 10 kV, 120 A SiC Module Switching Tests*

Double-pulse tests (DPTs) were performed in order to evaluate the hard switching characteristics of the 10 kV, 120 A SiC modules. Simulations were also carried out and compared to the experimental results. This model could be used to simulate the full PEBB

integration such that the control and power stage designs could be verified. The PEBB model will further allow designers to evaluate the PEBB performance in other applications.

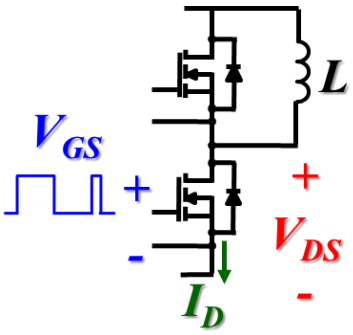
Each module and gate driver underwent DPTs up to 4.7 kV and 100 A in order to evaluate their hard switching performance. The voltage was limited to 4.7 kV due to the voltage rating of the bulk film capacitors (5 kV). The module DPT schematic and hardware setup is shown in Figure 2-2. A 1-mH inductor with high voltage wire for the winding was connected across the high-side (top) switch of the module. The high-side switch was kept off with a gate-source voltage of -8 V supplied by its gate driver such that the antiparallel JBS diode would freewheel the current in the inductor when the low-side switch is off.

The low-side switch received the double-pulse signal through a fiber optic cable. The gate-source voltage of the low-side switch was monitored using a 300-V, 1-GHz passive probe (Tektronix TPP1000), the drain-source voltage of the low-side switch was measured with a 20 kV, 20-MHz passive probe from Tektronix (P6105A), and the drain current was sensed with a Rogowski coil (PEM CWT Ultra Mini). DPTs were initially conducted using a low-inductance current shunt (T&M Research SSDN). The Rogowski coil and current shunt waveforms proved to be in good agreement, and thus the remaining tests were conducted with the Rogowski coil since the connections necessary for inserting the shunt into the testing setup add additional parasitic inductance into the power loop.

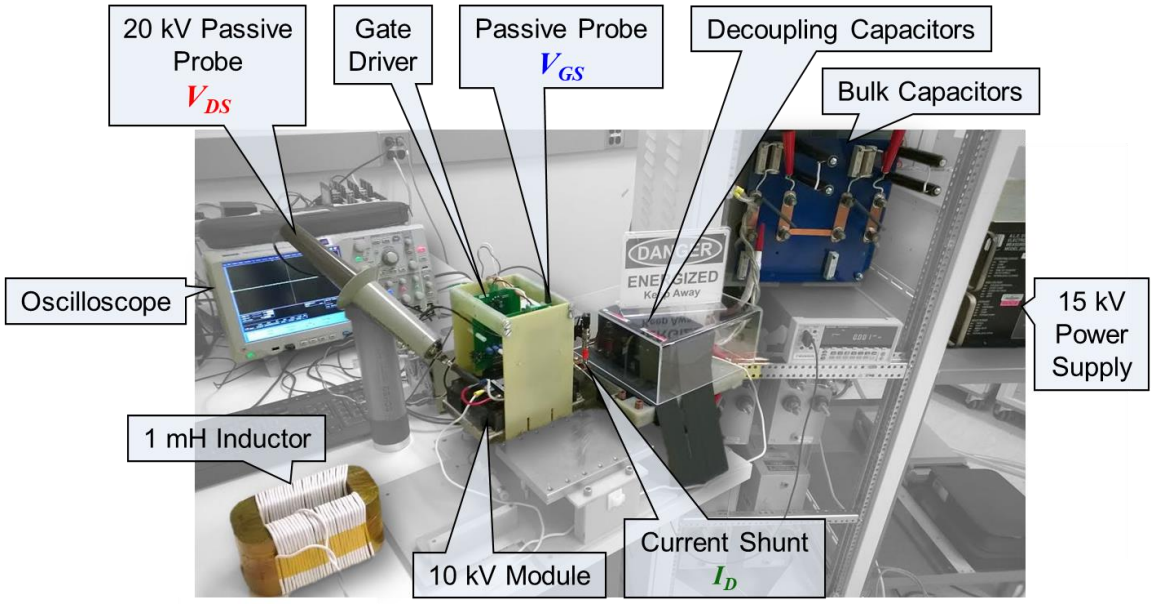
A 15 kV power supply from TDK-Lambda (203/303L) was used to charge two series 850 μF, 2.5 kV bulk capacitors. Once the capacitors are charged, the power supply is disconnected. A double-pulse signal is then sent from the function generator, to the gate driver of the low-side switch using a fiber optic cable. From the dc bus voltage, inductance, and drain current values, the width of the first pulse needed to achieve the desired current

level can be determined. At the end of this first pulse, the turn-off switching waveforms for the device under test can be captured. In order to obtain the turn-on switching waveforms under the same conditions, a short second pulse is applied. The rising edge of this second pulse gives the turn-on switching waveforms for the device under test.

The module DPTs revealed fast switching with limited ringing and overshoots. Waveforms from one of the DPTs conducted on the low-side switch at 4.7 kV and 100 A with an external gate resistance of 5 Ω is shown in Figure 2-3. Table 2-2 lists the overshoot, undershoot, rise and fall times, and switching rates from the DPT waveforms. Compared to medium-voltage silicon IGBTs, these SiC modules demonstrate faster switching, which corresponds to lower switching losses.

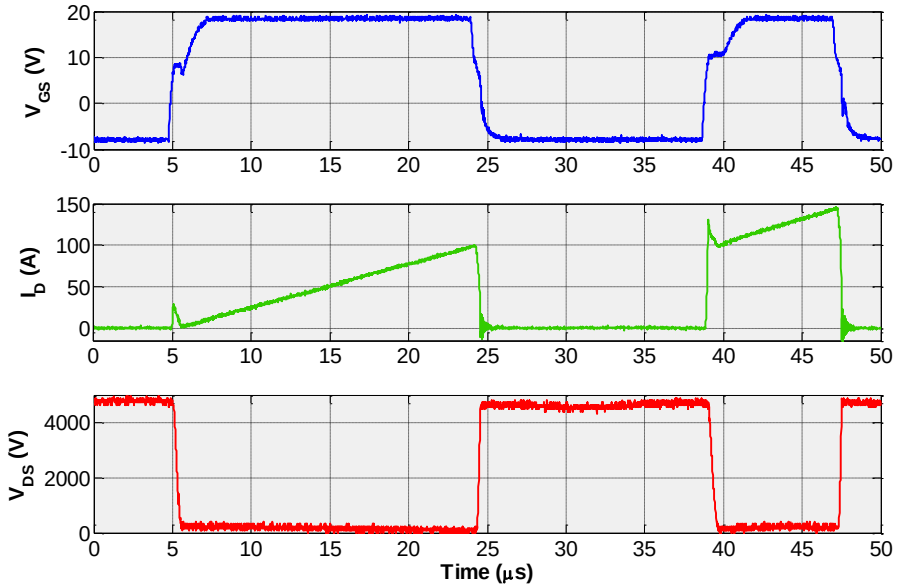



(a)

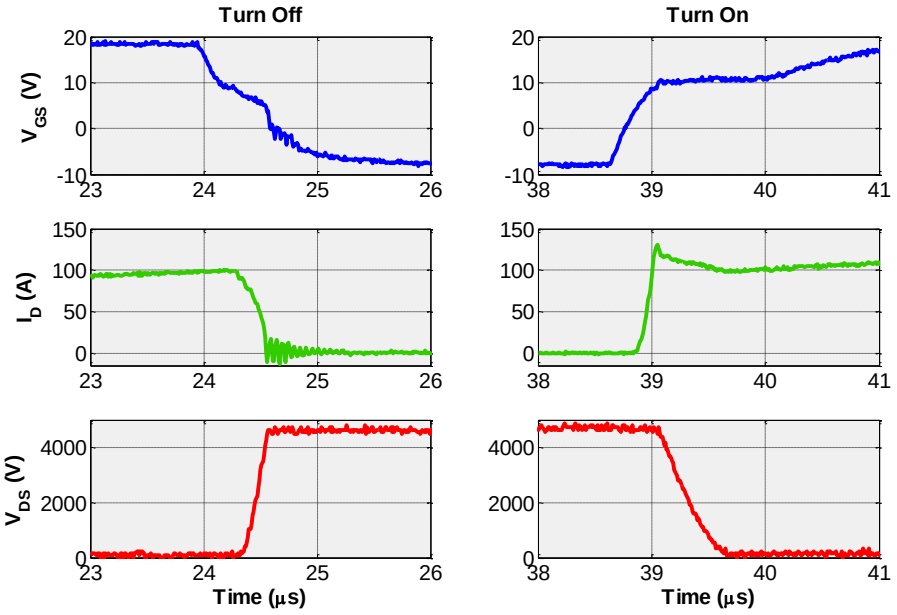



(b)

**Figure 2-2: 10 kV SiC module DPT (a) schematic and (b) hardware setup.**




(a)




(b)

**Figure 2-3: 10 kV SiC module DPT waveforms showing the (a) full double-pulse, and (b) turn off (left) and turn on (right) transients.**

**Table 2-2: First Generation 10 kV, 120 A SiC Module DPT Results**

| Parameter | Value | | |
|---|---|---|---|
| | ***Gate-Source Voltage*** | ***Drain Current*** | ***Drain-Source Voltage*** |
| Overshoot | None | 30 A | None |
| Undershoot | None | 10 A | None |
| Rise time* | 2020 ns | 110 ns | 170 ns |
| Rise *dv/dt* | 0.01 V/ns | 0.73 A/ns | 22.1 V/ns |
| Fall time* | 980 ns | 240 ns | 460 ns |
| Fall *dv/dt* | 0.02 V/ns | 0.33 A/ns | 8.2 V/ns |

*Parameter measured from 10 % to 90 % of the steady-state value.

### *2.3.2 PEBB Switching Tests*

After the hard switching capability of the modules was evaluated, DPTs were carried out on the PEBBs. It is crucial to perform DPTs on the PEBB in order to determine the impact of added parasitic elements on its hard switching behavior. The parasitics introduced during the PEBB integration include inductance from the bus bar and series IGBT short-circuit protection, and the winding capacitance of the PEBB inductor. For this testing, the PEBB inductor was connected across the switch not under test. For instance, if the low-side switch of one of the two modules in the H-bridge were to be evaluated in the DPT, then the inductor would be connected across the high-side switch. The high-side switch would then be gated off such that the antiparallel JBS diode would freewheel the current (Figure 2-4). The high- and low-side switches of the second module in the H-bridge would be kept off at a gate-source voltage of -8 V. For the PEBB DPTs, the switching of

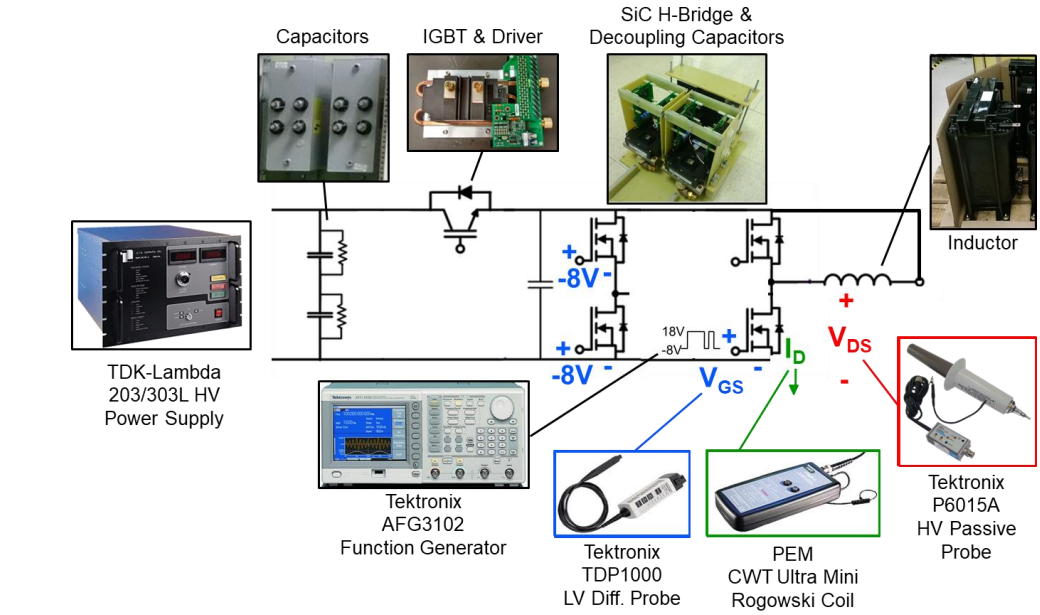
both the high- and low-side switches of each module in the H-bridge was assessed. This results in a total of four DPTs conducted per PEBB.

Figure 2-5 shows the turn-off and turn-on waveforms from one of the PEBB DPTs conducted on the low-side switch at 4.7 kV and 80 A. A lower peak drain current was used for the PEBB DPTs in order to prevent the drain current from surpassing the IGBT overcurrent protection limit at the end of the second pulse, since, as shown by Figure 2-5, the drain current can reach up to 150 A. The PEBB DPT waveforms were compared to the results of the module DPTs for the same switch (shown as the black curves). From the turn-off waveforms shown in Figure 2-5a, it can be observed that less ringing was experienced in the drain current turn off waveform for the PEBB DPT compared to that of the module DPTs. The greater ringing in the module DPTs could be due to the added source inductance from the current shunt connection. This figure also shows a lower drain-source voltage *dv/dt* for the PEBB DPT. This could be partially due to the lower peak drain current; the peak drain current of the module DPTs was 100 A, whereas the peak drain current of the PEBB DPTs was 80 A. The turn-

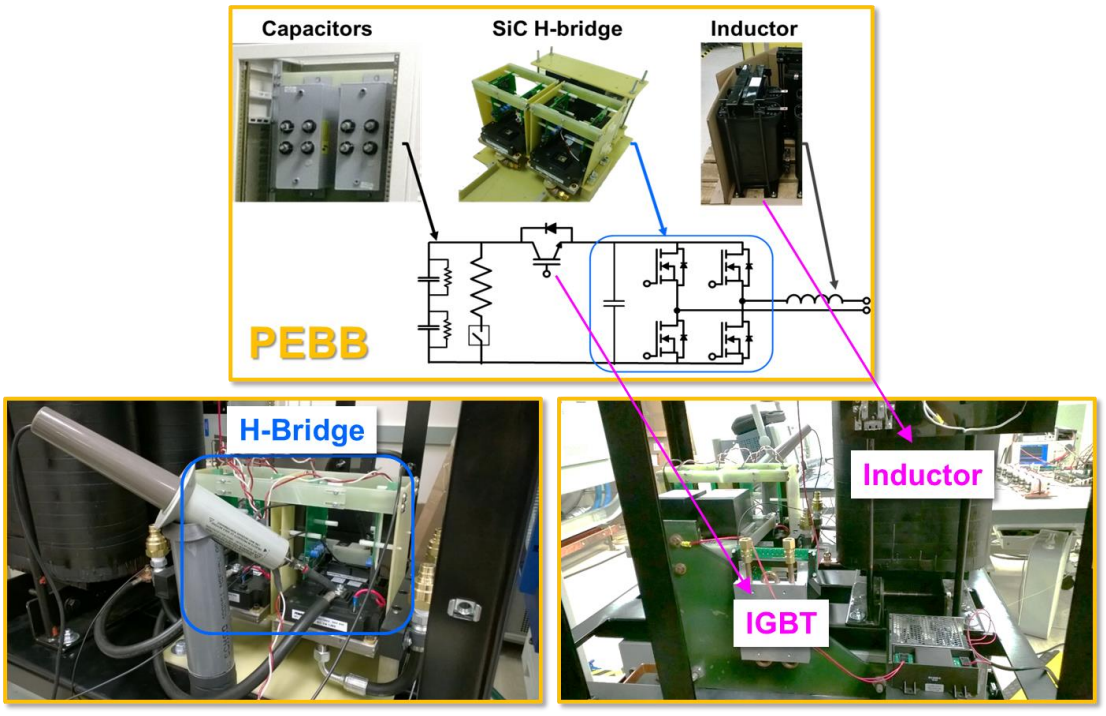
off waveforms, shown in Figure 2-5b, reveal that the drain current overshoot increased by approximately 30 A for the PEBB DPT. This larger overshoot could be attributed to the larger winding capacitance of the PEBB inductor compared to that of the inductor used for the module DPTs.

The high-side switches of each module in the PEBB were also tested. Due to the high voltage across the high-side switch, the drain-source voltage could not be measured, and a high-voltage differential probe was used for the gate-source voltage measurement. The Rogowski coil was connected around the drain terminal of the high-side switch to

sense the drain current. The waveforms matched well with those from the low-side switch DPTs.




(a)




(b)

**Figure 2-4: PEBB DPT (a) schematic and (b) hardware setup.**

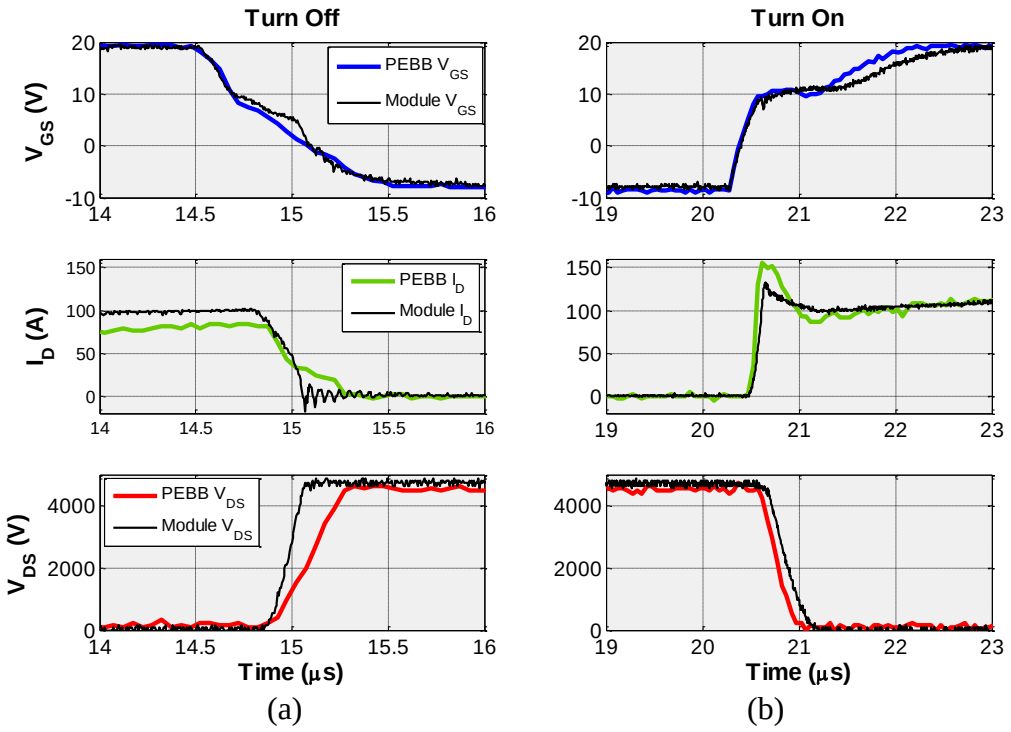



**Figure 2-5: PEBB DPT waveforms (a) turn off, and (b) turn on.**

Another objective of this work was to develop a detailed switching model of the PEBB. This model allows for verification of the control and power stage designs. Additionally, the model can be used to examine the versatility of the PEBB by simulating different applications. A Saber model of the 10 kV, 120 A SiC half-bridge was developed by the National Institute of Standards and Technology (NIST). In [101], the model proved to have excellent agreement with the measured results. In this work, a circuit that resembles the module DPT setup was generated in Saber using these half-bridge models (Figure 2-6), and the results were compared to the experimental waveforms (Figure 2-7). As shown by Figure 2-7, the simulation and experimental waveforms are in good agreement. However, there is some discrepancy during the turn-on process; the experimental results revealed faster gate-source voltage and drain current rise, and lower drain-source voltage *dv/dt* than the simulation waveforms. Though, for this application, these differences are minor.

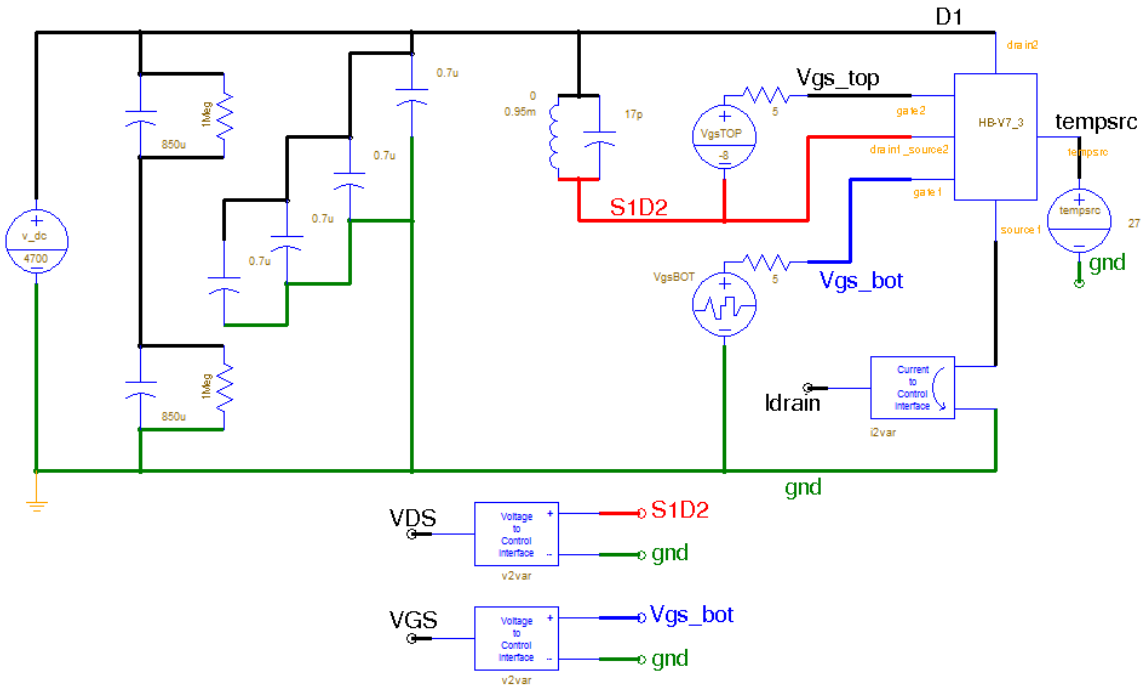
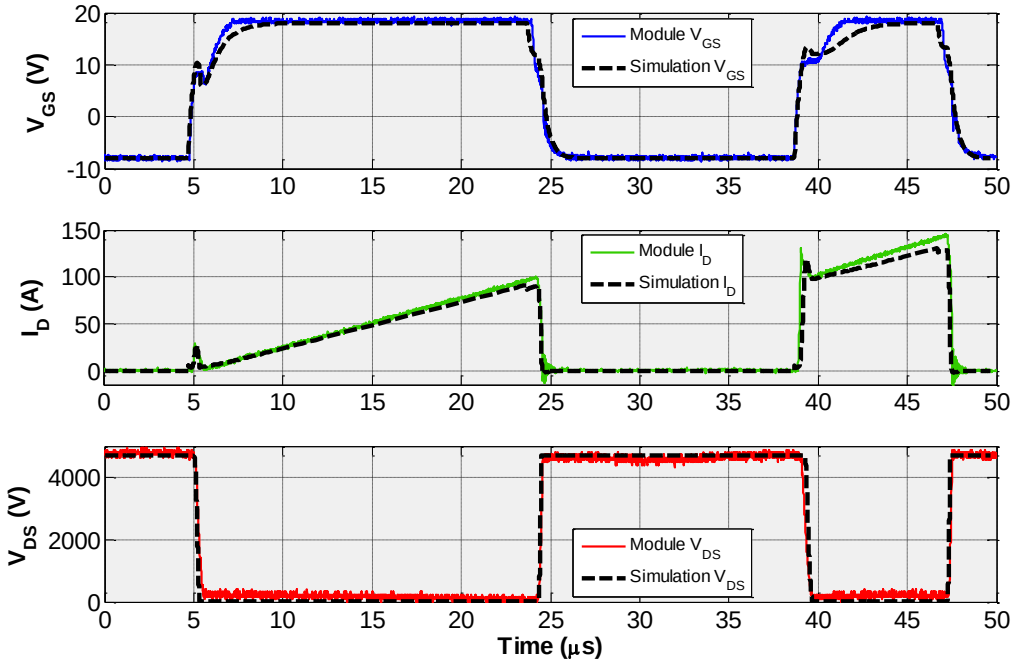
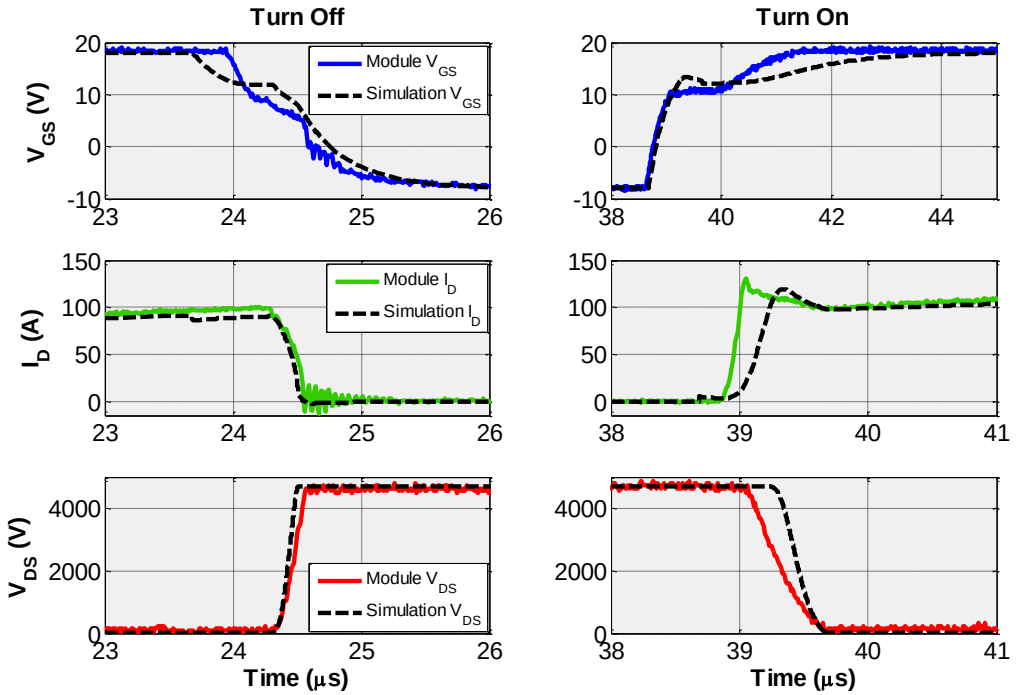



**Figure 2-6: Saber schematic for the 10 kV SiC module DPT simulations.**




(a)




(b)

**Figure 2-7: Comparison of experimental and simulation (dashed black curves) 10 kV module DPT waveforms (a) full double-pulse, and (b) turn off (left) and turn on (right).**

### 2.3.3 *PEBB Converter Tests*

After successful discrete tests were performed, continuous tests were carried out to further evaluate the performance of the PEBBs. Due to power limitations in the CPES laboratory at Virginia Tech, two separate buck tests were performed on the modules: one at high voltage and low current and the other at low voltage and high current. The high voltage test was done to evaluate the continuous high-voltage, high *dv/dt* capability of the unit, while the high current test was done to test the thermal performance. The schematic for the buck tests is shown in Figure 2-8. As can be seen from the schematic, only one of the two 10 kV half-bridge modules was used for the tests. The specifications for the two tests are listed in Table 2-3.

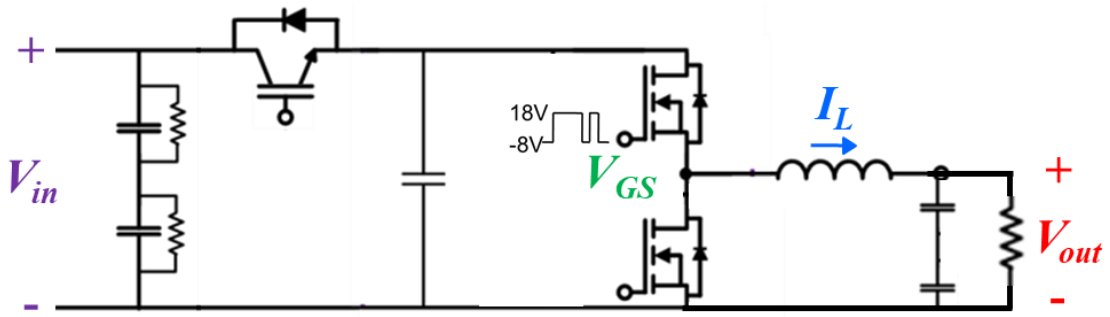



**Figure 2-8: PEBB buck test schematic.**

**Table 2-3: PEBB buck test specifications**

| Parameter | High-Voltage, Low-Current Rest | Low-Voltage, High-Current Test |
|---|---|---|
| Input voltage | 4.7 kV | 0.67 kV |
| Output voltage | 0.47 kV | 0.32 kV |
| Output current | 4 A | 100 A |
| Duty cycle | 10 % | 50 % |
| Switching frequency | 10 kHz | 10 kHz |

Figure 2-9 shows the gate-source voltage for the high-side switch of the half-bridge module and the inductor current waveform for the PEBB buck test at an input voltage of 4.7 kV and output current of 4 A. The gate-source voltage waveform appears distorted due to the varying potential of the source, which impacted the differential probe measurement. This distortion is a measurement error, and is not reflective of the actual device gate-source voltage. This waveform is being shown to demonstrate that the device was switching at the correct duty cycle (10 %). This 4.7 kV continuous test revealed some potential EMI issues. During the switching, "snow" began to appear across the oscilloscope screen, and the lights in the testing bay began to flicker.

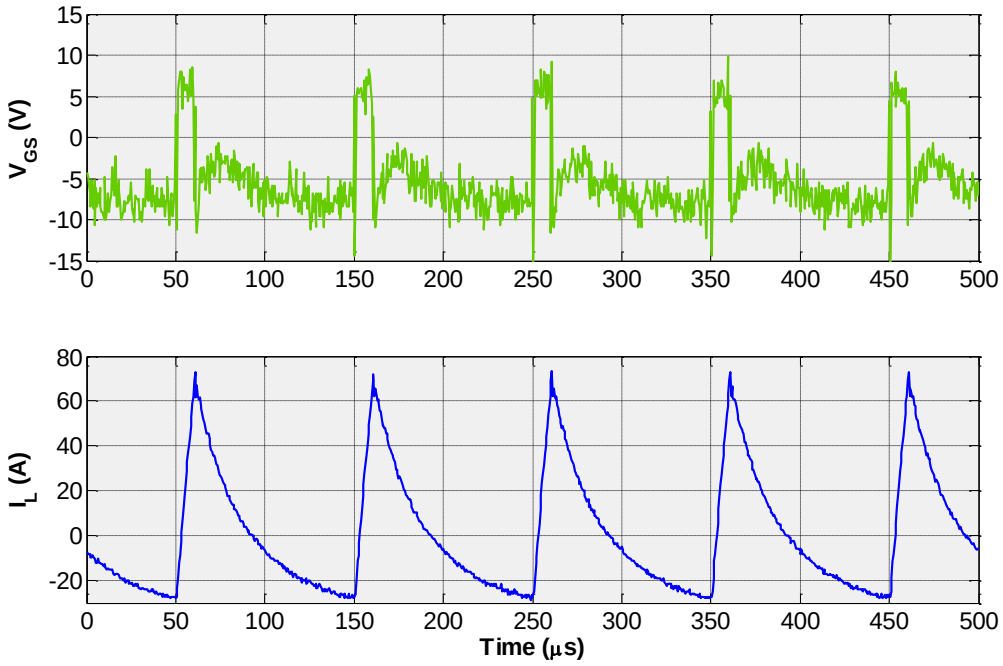



**Figure 2-9: Gate-source voltage (top) and inductor current (bottom) waveforms for buck tests of the PEBB at an input voltage of 4.7 kV and and output current of 4 A.**

Figure 2-10 shows the high-side switch gate-source voltage and inductor current waveforms for a buck test at an input voltage of 0.67 kV and output current of 100 A. The PEBB was tested in this mode for one hour to ensure good thermal performance. During

the tests, the 10 kV SiC module was cooled with a liquid coldplate. The module baseplate temperature was measured with a thermocouple. The temperature measurements showed that the module temperature remained in the desired range during the 100-A buck test.

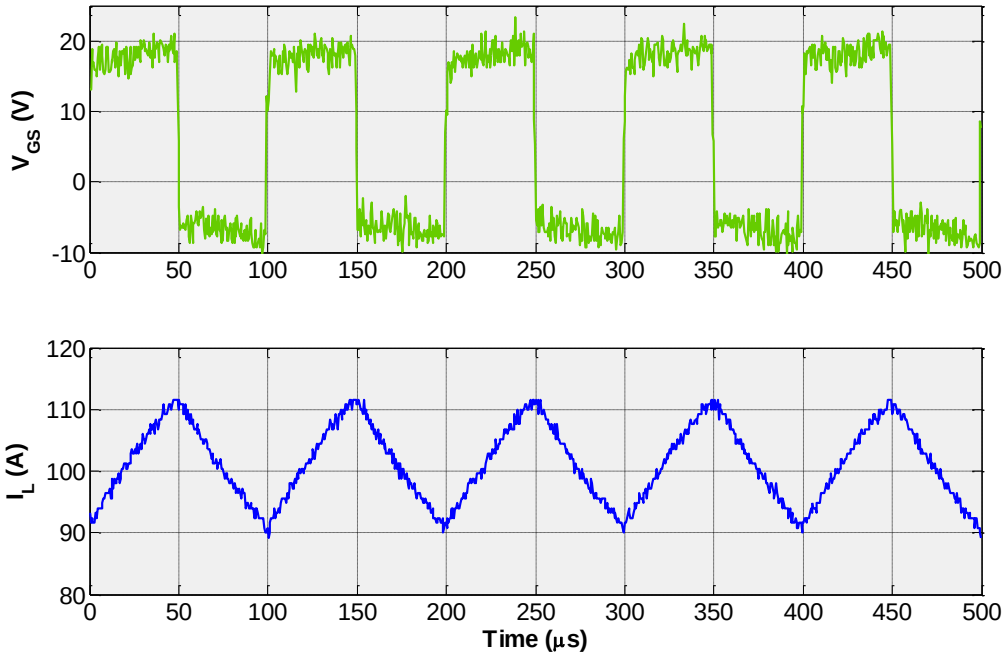



**Figure 2-10: Gate-source voltage (top) and inductor current (bottom) waveforms for buck tests of the PEBB at an input voltage of 0.67 kV and an output current of 100 A.**

After successful validation of the transient and thermal performances of the PEBBs, they were shipped to the Center for Advanced Power Systems (CAPS) at Florida State University for full-power tests [93]. Once the setup was completed in the CAPS facility, a full-power buck test was performed on the PEBBs. Next, the PEBBs were operated in inverter mode at 4 kV input, 480 V output, and 15 % duty cycle (Figure 2-11). These tests revealed good operation of the individual PEBB units in buck and inverter modes.

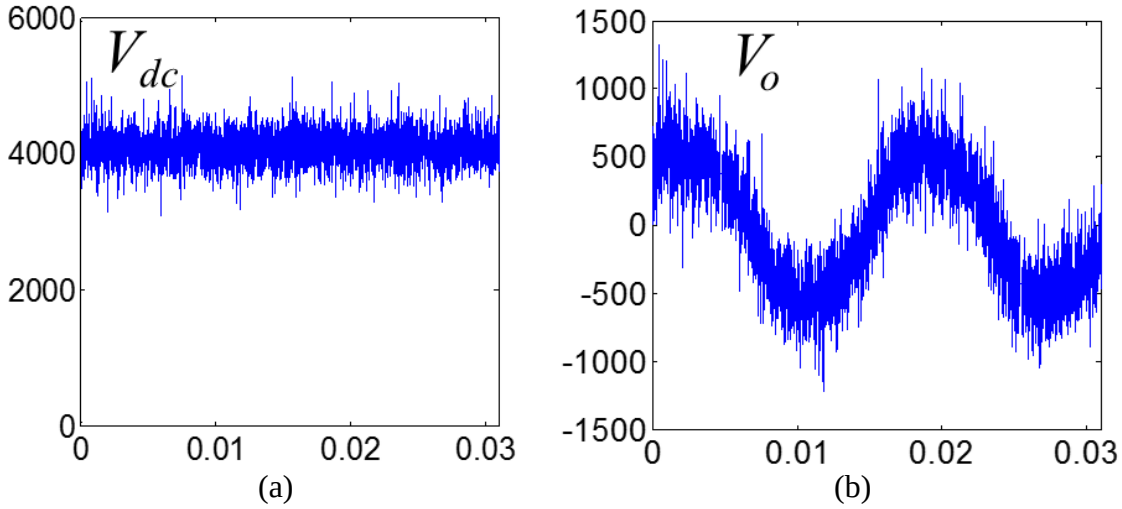



**Figure 2-11: (a) Input voltage and (b) output voltage waveforms for inverter tests of the PEBB at an input voltage of 4 kV and output voltage of 480 V. Images used with permission of Igor Cvetkovic.**

### *2.3.4 Impedance Measurement Unit Operation Tests*

The developed PEBB units could be readily used in all major power processing roles; namely generation, propulsion, energy storage, SSPS, high-power high-energy loads, and distribution apparatus, operating from 4.16 kV to 13.8 kV ac busses, and generating up to 20 kV MVDC for distribution purposes. Thus, the development of these SiC PEBB units provides the means to develop advanced MVDC systems, featuring modularity, scalability, and the flexibility to support different load configurations, while emphasizing simplicity, high-power-density, efficiency, and low-cost and low-engineered solutions.

For instance, the designed PEBB allowed for the realization of the first medium-voltage impedance measurement unit (IMU), which injects current and voltage perturbations into an electrical system in order to identify the impedance of the source and load, and then predicts the small-signal stability of the system [102]. The 10 kV SiC modules are uniquely qualified for this application because they can inject the magnitudes

and frequencies needed to perturb medium-voltage systems. The IMU mode of operation was also tested at the CAPS facility. For this mode, three PEBB units were operated together. Impedance measurements at 2.8 kV were achieved [94]. This is the first medium-voltage online measurement of system impedances. Unfortunately, the full voltage and power levels could not be achieved due to significant, unresolvable EMI. After intense analysis, it was found that substantial current was flowing through the system ground (Figure 2-12). The contaminated ground was causing the controller to mailfunction, thereby limiting the operating conditions.

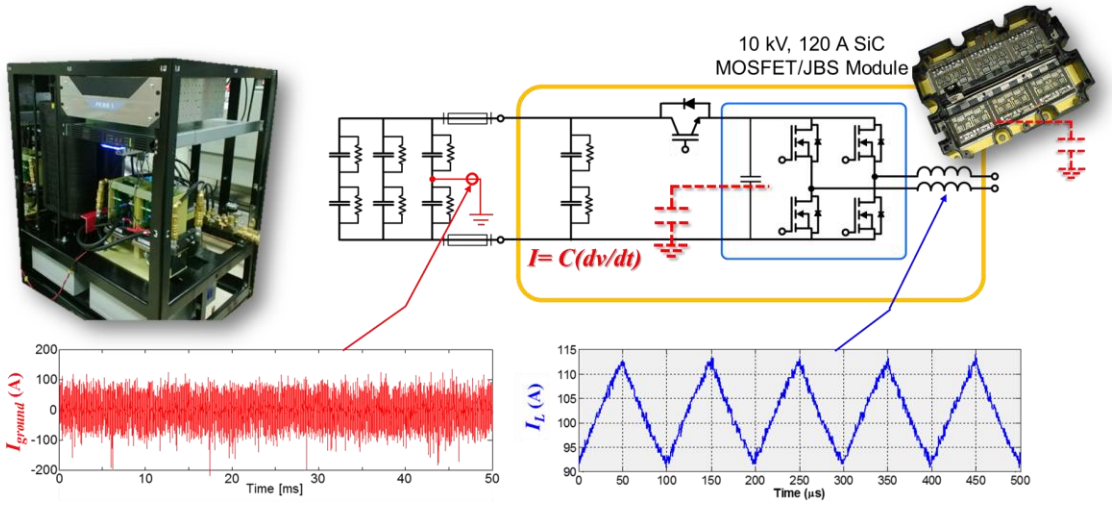



**Figure 2-12: PEBB schematic and hardware images (top), and ground current (bottom left) and inductor current (bottom right) waveforms.**

As mentioned previously, there exists a parasitic capacitance across the DBC substrate in the power module. When there is a voltage transient (i.e., *dv/dt*), this capacitance can become a path for CM current to flow. Therefore, this capacitance should be minimized, especially for fast-switching devices. However, since at the time no suitable packages were available for 10 kV SiC devices, a standard module package that is commonly used for 6.5 kV silicon IGBTs was utilized [97],[103]. Evidently, putting these

high-speed, 10 kV SiC devices in a package intended for slower, 6.5 kV silicon IGBTs was not ideal. While the module was sufficient to demonstrate the basic functionality of these first-generation 10 kV SiC MOSFETs, the continuous operation was limited.

From ANSYS Q3D simulations, the parasitic capacitance between the output node of the half-bridge (i.e., the source of the high-side switch and drain of the low-side switch, or S1D2) and the module baseplate is approximately 300 pF. For a *dv/dt* of 22 V/ns, this gives a calculated peak current of nearly 7 A. It should be noted that the 22 V/ns switching speed was achieved with internal and external gate resistances slowing down the devices. If it were not for these resistances, the switching speed would be even higher, which would increase the efficiency, but further worsen the CM current. So, while this capacitance may not have been critical for 6.5 kV silicon IGBTs, it is a major limitation for the operation of the 10 kV SiC MOSFETs. Clearly this capacitance, as well as other possible CM current paths at the converter and system levels, need to be minimized in order to realize the full potential of 10 kV SiC modules. Accordingly, there was a major effort to reduce the EMI in this work. This was done by minimizing this capacitance as well as implementing a screen that would contain the generated CM current within the power module package. The proposed method will be discussed in detail in Chapter 5.

Further issues with the module package were identified in [104]. The parasitic impedances of the package used for the 10 kV SiC devices were extracted and put into a circuit simulator with 2 kV SiC MOSFET die models. The results showed notable ringing in the switching waveforms due to the module parasitic impedances [104]. Even more troublesome was the current imbalance during the switching transients [104]. Due to the asymmetrical parasitic inductances among each of the paralleled dies, the maximum

difference in the current overshoot was 150 % [104]. This severe imbalance will cause the die with the greater overshoot to have larger switching loss [74],[75], and thus a higher junction temperature [75], ultimately reducing the lifetime of the module. To reduce the imbalance and circulating currents, gate resistances are often put inside the power module. As mentioned previously, this solution slows down the switching speed, thus increasing the losses and diminishing the advantages of using SiC devices over silicon. It is also common for the module current to be de-rated to account for the imbalance. This is clearly not desirable in terms of cost.

## *2.4 Third-Generation 10 kV, 240 A SiC MOSFET Module*

The first-generation 10 kV SiC MOSFETs could not conduct through the body diode, as it led to the propagation of stacking faults, which ultimately degraded the performance of the device [105],[106]. Consequently, antiparallel 10 kV SiC JBS diodes were needed to conduct reverse current [97]. Further, in order to ensure that the body diode did not conduct before the JBS diode, low-voltage silicon Schottky diodes were placed in series with the SiC MOSFETs [97]. More recently, Wolfspeed has developed a third-generation 10 kV SiC MOSFET, which has twice the current density of the first-generation device, and can reliably conduct through the body diode without degradation [18],[103],[107]. Given the enhanced performance of the third-generation device, the need for a new packaging that will enable its full potential is even more essential.

Accordingly, Wolfspeed has developed an improved package with lower stray inductance for these third-generation 10 kV SiC MOSFETs [108]. This new module does not include antiparallel diodes, and instead uses synchronous rectification with eighteen 10

kV SiC MOSFET dies in parallel per switch position to achieve a total module current rating of 240 A [108]. Thus far, few details of the module design have been reported, and characterization has only been shown for the module populated with a single 10 kV SiC MOSFET die [108].

CPES measured the parasitic capacitance between the module output terminal of the half bridge (i.e., S1D2) and the baseplate with an impedance analyzer. The measured capacitance is approximately 255 pF. The simulated parasitic capacitance for the first-generation 10 kV power module is around 300 pF. So, the third-generation module only has a 15 % lower parasitic capacitance. This is a concern considering this module has two times the current rating of the first-generation module, meaning the turn-off switching speed (i.e., *dv/dt*) will be faster. The specifications for Wolfspeed's first- and third-generation 10 kV SiC MOSFET power modules are listed in Table 2-4.

As can be seen from the table, the third-generation 10 kV SiC module has nearly the same footprint as the first-generation module, but has a 45 % lower profile. This lower volume, combined with the higher current rating, results in a nearly four times greater power density, in regards to volume. In terms of weight, the third-generation module only has a 7.5 % higher power density than the first-generation module. This is because the third-generation module is 85 % heavier than the first-generation. Moreover, due to the larger number of MOSFET dies, the third-generation module has nearly half the junction-to-case thermal resistance as the first-generation module.

A key improvement of the third-generation module is the lower power-loop inductance (57 % lower). Furthermore, the power terminals of the third-generation module are distributed along the package, thereby reducing the power-loop inductance asymmetry

among the paralleled dies. Recall that the severe asymmetry in the power-loop inductances for the parallel dies in the first-generation module resulted in significant dynamic current imbalance [104]. The asymmetry was a result of the power terminal location, which was at the far end of the module. Hence, the die that was closest to that end had the lowest power-loop inductance, whereas the die that was on the other side of the module, had the largest.

**Table 2-4: Specifications for Wolfspeed's First- and Third-Generation 10 kV SiC Power Modules**

| **Parameter** | **First-Generation 10 kV, 120 A** | **Third-Generation 10 kV, 240 A** |
|---|---|---|
| Number of dies per switch | 12 MOSFETs, 6 JBS | 18 MOSFETs (no JBS) |
| On-resistance (at 25 °C) | 42 mΩ | 19.4 mΩ |
| Maximum junction temperature | 150 °C | 175 °C |
| Dimensions | 187 × 137 × 44 mm (7.4 × 5.4 × 1.7 in) | 195 × 125 × 24 mm [108] (7.7 × 4.9 × 0.9 in) |
| Weight | 1.3 kg (2.9 lbs) | 2.4 kg (5.3 lbs) |
| S1D2-baseplate capacitance | 300 pF (simulated) | 255 pF (measured) |
| Power-loop inductance | 37 nH [104] | 16 nH [108] |
| Gate-loop inductance | 21 nH [104] | Unknown |
| Partial discharge inception voltage | Unknown | Unknown |
| Power density (volume) | 1.1 W/mm$^3$ (17.7 kW/in$^3$) | 4.1 W/mm$^3$ (70.7 kW/in$^3$) |
| Power density (weight) | 930 kW/kg (421 kW/lb) | 1000 kW/kg (453 kW/lb) |

While the third-generation module is clearly an improvement compared to the first-generation, there are still several aspects that could be enhanced. First, it should be noted that the primary reason for the four-times increase in the power density is due to significant

improvements in the 10 kV SiC MOSFETs. Due to design and fabrication refinement, the third-generation 10 kV SiC MOSFET has nearly double the current density as the first-generation. Additionally, as mentioned previously, the first-generation module needed two diodes per MOSFET die—one to conduct the reverse current (the 10 kV JBS diode) and another to prevent the MOSFET body diode from conducting before the JBS diode (the low-voltage silicon diode). Due to the enhanced reliability of the third-generation SiC MOSFET body diode, the external diodes could be eliminated, allowing for more SiC MOSFET dies to be included in the power module.

As shown in Table 2-4, the footprint of the third-generation module is only 5 % smaller than the first generation. Accordingly, the parasitic capacitances to the baseplate are similarly large. This large capacitance must be addressed in future designs in order to operate the module at its fastest switching speed, and thus its full potential, while achieving low EMI.

Moreover, the electrostatic performance of the modules has not been reported in the literature. While the third-generation module features creepage extender rings around the terminals to satisfy the creepage distance standards [109], no PD tests have been reported. Sufficient PDIV is essential to ensuring safe operation of the 10 kV power module.

Furthermore, while the distributed power terminals in the third-generation module help to reduce the power-loop inductance asymmetry, they make it difficult for system designers to integrate these modules into the power conversion system. A custom bus bar with careful electric field analysis at the connection points, such as the one presented in [91], must be designed, which can be a challenge for system designers.

Finally, both modules employ wire bonds for the internal interconnections. As mentioned previously, wire bonds can reduce the reliability of the power module [77], and fail as an open circuit under moderate energy levels [76]. In the following sections, other packages that have been reported for medium-voltage SiC and silicon devices will be presented.

## *2.5 Other Wire-Bonded Power Modules for Medium-Voltage SiC Devices*

The standard packaging technologies shown in Figure 1-2 are commonly used for the packaging of commercial 6.5 kV silicon IGBT modules, and have also been used for other medium-voltage SiC devices, such as 6 kV, 10 kV, and 15 kV SiC thyristors [110]; 6.5 kV SiC JFET [111]; 6.5 kV SiC MOSFET [112]; 15 kV SiC n-IGBT [113],[114],[115]; and 24 kV SiC IGBT [115]. Currently, few details on the actual design, fabrication, and testing of the majority of these medium-voltage SiC modules exist. This is likely because the devices themselves are still in the research or early development stages.

In 2015, APEI designed and built a half-bridge power module capable of 15 kV that could house up to eight devices in parallel per switch position [115]. The module, which was intended to be used for a wide range of medium-voltage device types, featured an integrated temperature sensor to monitor the junction temperature of the devices during operation [115]. The module uses high-temperature solder to attach the baseplate and insulating substrates [115]. Using solder for these large bonding areas has been shown to be unreliable [116]. The dies are then bonded to the substrates and wire bonded. The housing was molded from high-temperature plastic, and was designed to provide pollution

degree 2 creepage and clearance in air, in agreement with standards [115]. APEI claims to also offer sealed connections, which would meet creepage requirements for pollution degree 3 and higher [115]. The internal clearances are maintained by potting the power module with silicone gel [117].

Double-pulse tests were performed on the module at 8 kV and 47 A, and showed switching speeds up to 16 V/ns [115], which is comparable to APEI's commercial 1.2 kV SiC modules. The simulated stray inductances from the drain and source to the S1D2 are 30 nH and 48 nH, respectively, which are similar to those for commercially-available, lower-voltage, wire-bonded power modules [117]. However, as was shown in [72], this significant mismatch can result in greater high-frequency noise. APEI also claimed that they internally developed a wire-bond-less version of the 15 kV power module, which employed flip-chip mounting technology [117]; though, no further details could be found.

APEI also designed and built a high-temperature evaluation module for ≥20 kV SiC IGBTs from Cree, Inc. [115]. A housing design that meets the appropriate clearance and creepage to pollution degree 2 for this voltage level would require a module footprint of over 300 mm × 300 mm, which was too large for APEI's requirements; the final size of the demonstrator module was 81.3 mm × 95.3 mm × 25.4 mm [115]. Since the terminal spacings did not meet the clearance requirements in air, this module could only be safely operated while immersed in dielectric fluid [115]. This clearly puts a significant constraint on the usage of the power module and reduces its practicality.

The module housing, potting/encapsulation, and baseplate for this ≥20 kV SiC module were the same as those used for the 15 kV package [115]. Due to the higher voltage rating, a thicker ceramic substrate was required. However, as shown in [79], increasing the

ceramic thickness gives limited improvement in the PDIV. Furthermore, by increasing the ceramic substrate thickness, the thermal resistance of the power module also increases. APEI utilized finite element modeling and CAD design tools to model the mechanical stresses, thermal gradients, current density, electric field strengths, and module inductance; though, no details were provided in the paper [115]. For the gate connection, small RF coaxial connectors were used [115]. APEI claims that the coaxial cables were designed with insulation up to 30 kV [115].

## *2.6 Press-Pack Power Modules*

As mentioned previously, there are several limitations of traditional wire-bonded packages. Namely, they have low reliability [77], high parasitic inductance [61], high on-state losses/limited current conduction capacity, and low energy-absorption capability during faults [76], typically resulting in an open circuit failure mode and having a risk of explosion [124]. These drawbacks are of particular concern in some high power, high-voltage applications, such as HVDC and FACTS, where a large number of devices and/or submodules are placed in series. The requirements for these applications include: high current ratings (1000 A or more), high reliability (lifetime of tens of years), ease of series connection (at the module and/or submodule level for multi-level and modular multi-level converter schemes, respectively), short-circuit failure mode (external bypass circuits [118] add cost, size, weight, and complexity), high explosion resistance during faults, low thermal resistance for effective cooling, low parasitic inductance to minimize the voltage overshoot across the device (especially during high *di/dt* short circuit events/faults), and symmetrical gate connections for good dynamic current sharing among the paralleled dies.

To address these stringent requirements, manufacturers, such as Toshiba and Westcode, applied pressure contact technology that was traditionally used for thyristors for industrial applications to high-power silicon IGBTs in the 1990s [119]. In press-pack modules, the electrical connection to the semiconductor dies are made through rigid electrodes and strain buffers, which are in physical pressure contact to the devices by an external clamping system. The electrode pillars are typically made of Cu, which has a higher coefficient of thermal expansion (CTE) than silicon. Accordingly, to reduce the stress on the dies, strain buffers are inserted between the electrodes and the dies. These buffers are typically made of molybdenum (Mo), which has a CTE closer to that of silicon [120], thereby reducing the stress on the dies.

The advantages provided by press-pack packaging are the higher reliability due to the absence of wire bonds and solder joints; short-circuit failure mode due to the pressure contacts; more uniform distribution of stray inductance among paralleled dies, double-sided cooling, and easy configuration in parallel and series due to the parallel top and bottom electrodes; and improved explosion resistance due to the hermetically-sealed housing [124].

A major drawback to the press-pack module is the complex and bulky mechanical assembly [118]. The rigid, dry-contact structure of the press pack has strict requirements on the uniformity of the applied pressure; if the pressure is not homogeneously distributed, then some of the dies may not be in good physical contact with the electrodes, resulting in unequal physical, electrical, and thermal stresses on the devices. This stress non-uniformity can occur due to variations in the die thicknesses, strain buffer and electrode pillar heights, and flatness and parallelism of the electrodes [124]. Moreover, this non-uniformity issue

is amplified when the die area is increased and/or when multiple modules are stacked in series [124]. Consequently, this type of rigid, dry-contact, press-pack structure has extremely tight tolerances on all of the components.

To address these issues, ABB developed the StakPak$^{TM}$, which is a compliant press-pack structure that uses springs instead of rigid electrode pillars to individually contact each die within the module [121]. This mechanism limits the maximum pressure on each die and reduces the requirements for the component tolerances and the uniformity of the applied pressure. As a result, the die area can be increased, resulting in higher current modules (up to 3000 A [122]). The gates of the IGBTs also have spring contacts. Silicone gel is potted into the housing to provide passivation and protection. After curing of the silicone gel, a fully functioning submodule is ready for testing [123]. However, using springs in place of the rigid electrode pillars reduces the cooling performance from the topside of the dies, effectively returning to a single-sided cooling structure (as in the wire-bonded modules).

Moreover, press-pack modules typically have a single connection to the gate and auxiliary emitter (i.e., gate signal return path) terminals, resulting in poor gate distribution to the paralleled dies, and thus in significant variations in the gate loop inductances, which can result in unsynchronized switching [124]. As a result, some dies will have greater current stress than others, requiring the entire module to be derated [124]. Furthermore, these modules typically do not employ a Kelvin connection for the gate return path. Accordingly, during high *di/dt* transients, the voltages generated across the parasitic inductances of the electrodes can change the gate reference level for the dies, further desynchronizing the switching of the devices [124].

Furthermore, the dry contacts used in traditional press packs, can have high thermal resistances due to gaps at the interfaces caused by surface roughness [124]. Additionally, dry contacts put restrictions on the type of encapsulation material that can be used in the module. For instance, a dielectric gel could enter the dry contact interfaces, thereby increasing the electrical and thermal resistances of the joints [125]. A common solution is the use of sulphur hexafluoride ($SF_6$); however, this requires a hermetically-sealed package and specialized equipment to implement, and the dies/module cannot be tested at their full voltage rating until the module is completely sealed [124]. Additionally, $SF_6$ is harmful to the atmosphere [126].

Dynex recently proposed a modified press-pack structure to overcome these disadvantages. First, Dynex uses Ag sintering to bond the strain buffers to the IGBT die surface [124]. This Ag sintered joint increases the contact area, thereby reducing the thermal resistance of the interface [124]. However, a reliability concern may still exist due to the sliding between the Mo stress buffer and the Cu pillar dry contact [127]. Second, Dynex uses silicone edge passivation to enhance the voltage breakdown capability of the module [124]. This method allows the dies to be fully tested to their rated voltage in air using standard testing equipment [124]. Finally, to resolve the switching desynchronization issue, Dynex developed a low-inductance circuit board for the gate and Kelvin emitter paths to each die in the module [124]. By separating the gate return path from the emitter electrode (i.e., implementing a Kelvin emitter connection, which is common in power modules) the gate loop inductance can be further reduced and the effects of high *di/dt* transients are mitigated [124]. To the author's knowledge, no further details on the design or test results supporting these claims have been published.

Despite the advantages and improvements of press-pack modules listed above, the stray inductances are still preventing their application to SiC MOSFETs. A major contributor to the stray inductance is the heatsink; since the press pack structure does not include an insulating substrate, the heatsink is included in the power loop, which increases the inductance. Furthermore, these packages are typically only made for a single switch, so, to create a phase-leg connection, multiple packages would have to be connected externally, thus further increasing the commutation-loop inductance. The stray inductance for traditional press-pack modules is in the range of hundreds of nanohenry [118]. While this may be acceptable for silicon IGBTs and thyristors, it is not suitable for fast-switching WBG devices.

There have been several attempts to reduce the inductance of the press-pack structure for lower-voltage silicon IGBTs [128]. In [128], a low inductance of 2.3 nH was claimed, though the voltage and current ratings for the module were not reported, and it is unclear if an actual power module was fabricated and tested. Moreover, the structure was complex and required a large number of components and layers, which could have a negative impact on the cost, manufacturability, and reliability. The external clamping system was also several times larger than the module itself [128], resulting in low power density.

In [129], a new press-pack structure was proposed for 1.2 kV, 25 mΩ SiC MOSFETs. The dies are mounted onto a baseplate, which is attached to a cooler. On the top of the dies, there is an interposer with conductors that connect to an upper low-temperature co-fired ceramic (LTCC) substrate, which is attached to another cooler. The proposed module has power and gate loop inductances of 4.3 nH and 6 nH, respectively

[129]. With the bus bars, the power loop inductance increases to 12 nH [129]. The switching waveforms show a 33 % (200 V for a 600 V bus voltage) drain-source voltage overshoot during the turn-off transient [129], which is higher than expected for a claimed power loop inductance of 12 nH . While there is also some ringing present, it is dampened after roughly 200 ns [129].

To achieve low parasitic inductance, an LTCC micro-channel cooler with a thickness of 2.7 mm was developed [129]. The junction-to-heatsink thermal resistance was about 0.2 K/W, and the heatsink to coolant thermal resistance was 0.8 K/W [129]. These thermal resistances are much higher than the junction-to-case values listed in Table 2-4, especially considering this modified press-pack module employs double-sided cooling, whereas those in Table 2-4 use single-sided cooling.

The module uses fuzz buttons, which contact the dies through holes in the interposer, in place of the usual rigid pillar or spring contacts. These fuzz buttons are only capable of conducting 5 A each [130]. Since only twelve fuzz buttons could fit on a MOSFET die, the continuous current is limited to 60 A even though the chips are rated at 71 A at 100 °C case temperature (98 A at 25 °C case temperature) [131]. The proposed module also requires many custom components and processing steps, and employs soldering, which is known to be a reliability concern.

Furthermore, high voltage stress occurs between the baseplate and the upper LTCC substrate [129]. The interposer (the material of which is not reported), which is in between the baseplate and upper substrate, is providing the insulation [129]. The report claims the voltage blocking capability of the package could be increased by covering the exposed areas of the baseplate with insulation film or coating, or by hermetically sealing inert gas

into the package [129]. The actual dielectric performance of the module was not evaluated in [129], and it is not trivial to alter this design for higher-voltage SiC devices.

Another major challenge for applying press-pack technology to SiC devices is the much smaller die and contact pad areas. Silicon Power Corporation's ThinPak technology attempts to overcome this obstacle [132]. According to Silicon Power Corporation, ThinPak technology results in high power module yields, reduces parasitics, and simplifies module manufacturing so it can be automated as a simple pick and place operation [132]. It is a metallized ceramic lid that sits on top of the semiconductor die and allows for an easy, solderable connection to the device [132].

This technology was used in the fabrication of a wire-bond-less package for 9 kV SiC super gate turn off thyristors (SGTO) [133]. The module is comprised of a baseplate for the cathode contact, dielectric sidewalls, silicone-based potting compound, plated Cu internal and external high-current anode contacts, and a PCB for the gate connections [133]. Silicon Power Corporation's module contains sixteen 1.0 $cm^2$ SiC SGTOs in parallel, and has package dimensions of 8.3 cm × 8.3 cm × 1.2 cm [133]. However, the focus of this module is primarily on the high pulse current capability, and it is unclear if the module was tested at the rated voltage.

There are few publications that discuss the electric field distribution within the press-pack modules, and those that do exist are very recent [134],[135],[136]. This is concerning because, in [134], it was determined from detailed modelling and simulation that the electric field strength within the module is greater than the critical electric field strength of the insulating gas (nitrogen, in this case). Accordingly, there is a strong chance that PD will occur. Similarly, in [135], the simulated electric field strengths in the dielectric

materials within the press-pack module exceeded the critical electric field strength of those materials. As a result, according to the simulation, breakdown could occur at 2.5 kV in air at atmospheric pressure and 4 kV in nitrogen at 0.15 MPa (1.5 bar) [135]. Experimental measurements confirmed that breakdown occurs at these voltages [135]. This is concerning since the module is claimed to be a 4.5 kV, 2400 A press-pack module for silicon IGBTs [135].

## *2.7 Conclusion*

In this chapter, Wolfspeed's first- and third-generation 10 kV SiC power modules were evaluated, and areas for improvement were identified. A discussion of other state-of-the-art and research-level medium-voltage power modules for silicon and SiC devices were also presented. In particular, the limitations of traditional wire-bonded packages were identified. Namely, they have low reliability [77], high parasitic inductance [61], high on-state losses/limited current conduction capacity, and low energy-absorption capability during faults [76], typically resulting in an open circuit failure mode and having a risk of explosion [124].

These drawbacks are of particular concern in high-voltage, high-power applications, such as HVDC and FACTS, where a large number of devices and/or submodules are placed in series. Accordingly, press-pack modules are commonly used in these applications due to their improved short-circuit failure mode, enhanced reliability, and ease of stacking. However, press-pack modules also have several disadvantages, including a complex and bulky mechanical assembly that is needed to ensure uniform contact to each die cell, and large parasitic inductances [118]. Moreover, recent analysis of

press-pack modules has shown the simulated electric field strength in the package exceeds the critical breakdown field strength of the insulating gas [134],[135].

It is clear these state-of-the-art power modules are not suitable for obtaining the full benefit of 10 kV SiC MOSFETs. In the following chapter, an optimized design for these unique devices is proposed. The module has fast switching speed due to the low and balanced parasitic inductances, high PDIV as a result of the reduced electric field strength, and lower EMI because of an integrated screening layer. At the same time, the module has greater power density than any other reported 10 kV SiC MOSFET power module.

# Chapter 3 Design of a Wire-bond-less, Planar, 10 kV SiC MOSFET Power Module

## *3.1 Introduction*

This chapter will present the detailed design of a high-power-density, high-speed, half-bridge power module package for Wolfspeed's 10 kV, 350 mΩ SiC MOSFET [18]. There are several challenges associated with creating a high-density package for high-speed, 10 kV power semiconductors. First, it is well known that high-power-density packages have greater power dissipation densities and hence require a more thoughtful thermal design. Additionally, since no external diodes are used in this module, the MOSFETs have higher average power dissipation, thus further emphasizing the need for a package with low thermal resistance and a good thermal management system. The challenges associated with high-speed switching include sensitivity to parasitic inductances, which can result in significant voltage overshoot, ringing, and current imbalance among paralleled die [104],[74],[75]. Furthermore, the high *dv/dt* can result in CM current flowing through the parasitic capacitance that exists between the devices and the cooling system. If the cooling system is grounded, then this current can flow through the system ground, potentially coupling into the control and logic circuitry, which could result in false signals.

In addition to these common challenges associated with packaging high-speed, WBG devices, the desire to create a high-density package for 10 kV devices means the electric field strength within the module will be increased. If the electric field strength exceeds the electrical breakdown strength of the dielectric materials, then PD can occur, potentially causing permanent damage to the insulating materials, such as the insulating ceramic substrate [79]. Therefore, the internal and external/surrounding electric field strengths of the power module must be carefully controlled. In collaboration with the University of Nottingham, colleagues at CPES, and visiting scholars from Tianjin University, an optimized power module for 10 kV SiC MOSFETs that addresses all of these challenges was designed, prototyped, and tested. The design will be presented in this chapter, followed by the prototyping and testing in Chapter 4.

## *3.2 Sandwich Power Modules with Metal Post Interposers*

Of the various power module structures that have been proposed in the literature, the sandwich structure has several key advantages for 10 kV SiC module packaging, including low parasitic inductance, small footprint, high integration, and good electrical isolation, energy absorption, reliability, and manufacturability. Two sandwich structures with metal post interposers reported in the literature will be reviewed in this section.

The metal post interconnect parallel plate structure (MPIPPS) module structure proposed by Virginia Tech in 1999 [61], achieves both low parasitic inductance and high power density. The proposed module structure is shown in Figure 3-1. Instead of traditional wire bonds, the MPIPPS module uses Cu posts and a top insulating substrate to achieve the interconnections. According to [61], while a typical wire bond has an inductance between

6 nH and 16 nH, a Cu post that is 5 mm × 4 mm × 1.69 mm has an inductance of just 1.7 nH. Additionally, gate driver components can be mounted on the top substrate in order to achieve a higher level of integration, as pictured in Figure 3-1 [61].

Although the MPIPPS module was demonstrated using a 600 V, 50 A silicon IGBT and diode [61], the structure is scalable to higher voltages. This is due to the Cu posts, which provide electrical isolation between the top and bottom substrates, as well as relax the electric field at the edge of the semiconductor die [141]. Therefore, by increasing the post height, higher voltage ratings can be achieved.

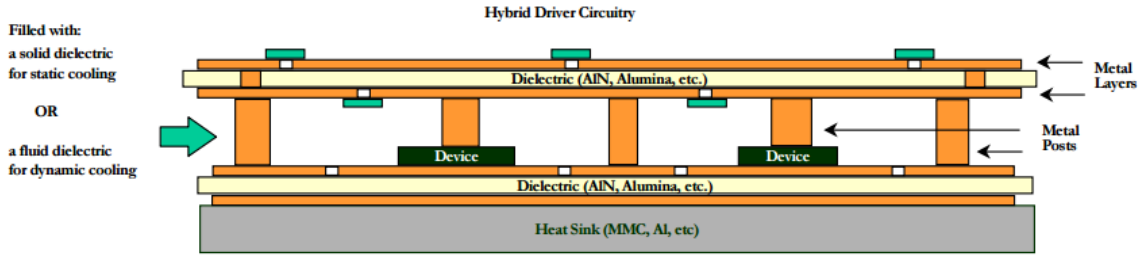



**Figure 3-1: Cross-section of MPIPPS structure [61].**

More recently, the University of Nottingham fabricated a hybrid half-bridge module (Figure 3-2), which has several key distinctions from the MPIPPS [62]. The proposed module is a flip-chip design, unlike the single-sided MPIPPS module, and employs double-sided cooling for improved thermal performance (Figure 3-2). The module also uses flexible PCB for low-inductance terminations. Additionally, copper/molybdenum/copper (Cu-Mo-Cu) laminate is used for the posts instead of pure Cu. This was done to increase the thermal cycling capability of the module [62]. The improved reliability is attributed to the reduced CTE mismatch between the posts and the die. Mo has a CTE of 4.9, which is closer to that of silicon (2.6) and SiC (3.7) than Cu (17), and thus will result in lower thermomechanical stresses at the post–die interface compared to pure

Cu [142]. However, since solder and sintering metals do not adhere well to Mo, a laminate that sandwiches the Mo between two Cu sheets was used to achieve good bonding. In [142], it was found that a thinner Cu layer increases the module reliability. This is due to the lower equivalent CTE of the CMC post.

While it is more complicated to fabricate, a significant advantage of this flip-chip structure is the lack of a parasitic capacitance between the switching node (i.e., the emitter of the high-side switch and collector of the low-side switch, labeled "Load" in Figure 3-2) and the cooling system, which can reduce the amount of CM current. Of course, this will depend on how the switching node terminal is connected to the rest of the system.

This module was demonstrated using a 3.3 kV silicon IGBT and diode [62]. However, no electric field analysis or PD tests were performed on the module to ensure it can safely and reliably operate at the rated voltage. In particular, the close proximity of the terminals, caused by the flip-chip and double-side cooling structure, could pose an issue in terms of PD, creepage, and clearance.

The module is 104 mm × 103 mm × 23 mm with the double-sided, turbulent cooler [62]. The current rating for the IGBT dies used in [62] is 50 A. This results in a module power density of 0.5 W/mm$^3$. The parasitic inductance of the power module is approximately 20 nH. As a result, the voltage overshoot is 80 V (4 %) at 2000 V bus [62]. Although this may appear low, the *di/dt* is relatively slow. While this may be sufficient for silicon IGBT modules, it is not suitable for high-speed SiC devices. Moreover, the gate-loop inductance is also a concern, as it appears the terminals are rather far from the IGBTs. Consequently, this type of layout may be difficult to adapt for a module with multiple dies

in parallel since the parasitic inductances may not be symmetrical, resulting in dynamic imbalance.

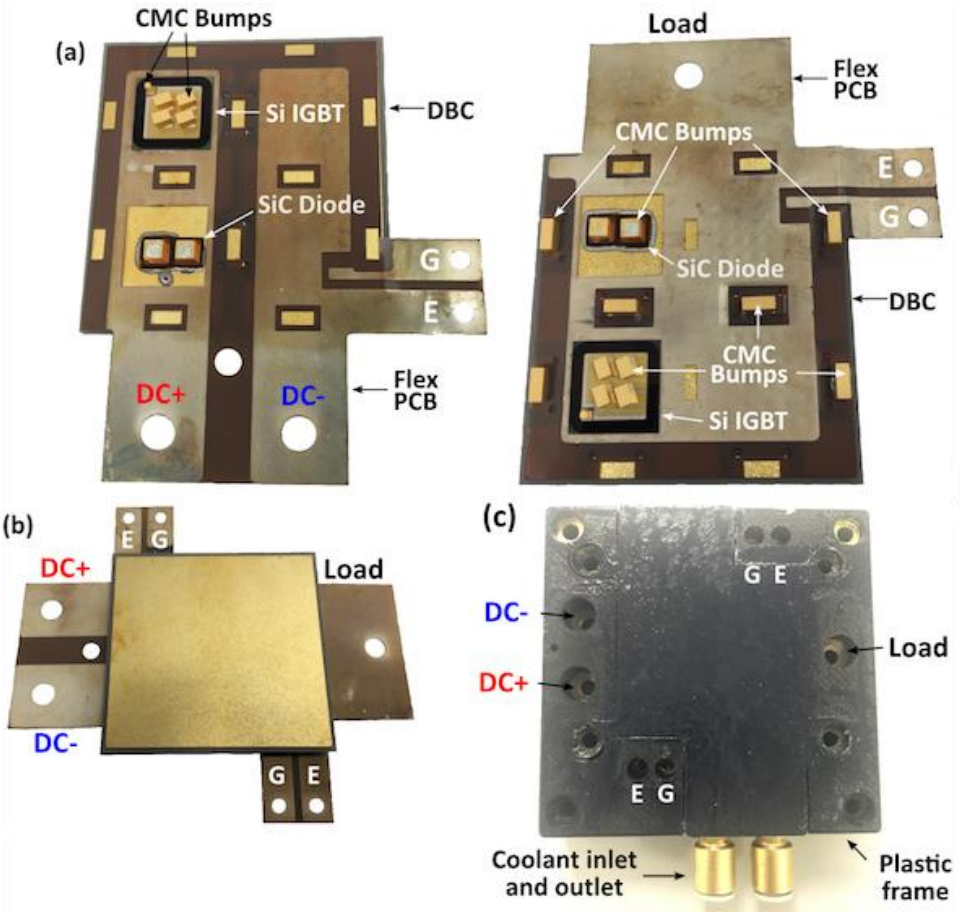



**Figure 3-2: University of Nottingham module (a) before flip-chip assembly, (b) after flip-chip assembly, and (c) after mounting in cooling system [62]. Images used with permission of Bassem Mouawad.**

In the following sections, the first detailed account of the design of a compact, multi-chip 10 kV SiC MOSFET half-bridge module will be presented. The module has low parasitic inductance and a symmetric, scalable layout for high-power capability with good dynamic performance. Care was also taken to minimize and contain the EMI generated by the high-speed switching. The electric field strengths internal and external to the power

module were also carefully controlled. This is the first time these issues have been addressed in detail for a 10 kV SiC MOSFET power module.

## *3.3 Module Design Overview*

Figure 3-3 shows the schematic and 3D model of the designed half-bridge power module. The colors of the metal pads in the 3D model (Figure 3-3b–Figure 3-3f) correspond to the node in the schematic (Figure 3-3a) with the same color. In the schematic, the node notations are as follows:

D1= drain of the high-side switch,

S1D2= the source of the high-side switch and the drain of the low-side switch,

S2= the source of the low-side switch,

G1= the gate of the high-side switch,

G2= the gate of the low-side switch,

$C_{D1}$, $C_{D2}$= embedded decoupling capacitors (Figure 3-3c),

Mid= the midpoint of the two series decoupling capacitors, and the middle metal of the bottom substrate stack,

$C_{P1}$= parasitic capacitance across the top substrate in the bottom stack (Figure 3-3d),

$C_{P2}$= parasitic capacitance across the bottom substrate in the bottom stack (Figure 3-3d).

The half-bridge module has three 10 kV, 350 mΩ, 8.1 mm × 8.1 mm dies in parallel per switch position for a total module current of 54 A. This value is based on the preliminary datasheet for the 10 kV SiC MOSFET die, which rates the continuous drain

current at 18 A for a case temperature of 90 °C, junction temperature of 175 °C, and gate-source voltage of 20 V. To increase the power density and reduce the cost, no external antiparallel diodes will be used in the module; instead, the reverse current will flow through the MOSFET channel, and the body diode will only conduct during the dead time. This synchronous operation is made possible due to the symmetrical reverse conduction and superior internal body diode of SiC MOSFETs, which have lower reverse recovery and thus lower losses than silicon MOSFET body diodes [137],[138]. In the past, conduction of the SiC MOSFET body diode was avoided because it led to the propagation of stacking faults, which ultimately degraded the performance of the device [105],[106]. However, recently, it was shown that the body diode of SiC MOSFETs is stable [18],[103],[107]. While some work has evaluated the performance of SiC MOSFETs operating in synchronous mode without external antiparallel diodes [139],[140], few diode-less power modules have been reported. However, recently, some diode-less SiC modules are becoming available. Wolfspeed's third-generation 10 kV, 240 A module, for instance, does not include external antiparallel diodes [108].

The module has a planar, sandwich structure, using posts and direct-bonded-aluminum (DBA) substrates as the die interconnection instead of wire bonds. This type of structure allows for increased power density, and reduces the parasitic inductances and capacitances in the module, thereby improving the transient performance. Furthermore, by eliminating the wire bonds, the energy absorption capability (e.g., during faults) of the module may be increased, as was shown in [76]. This structure also allows decoupling capacitors to be embedded within the module to further improve the dynamic performance

without increasing the module footprint. In total, four substrates are used in the power module: two beneath the dies (DBA1 and DBA2) and two on the top (DBA3 and DBA4).

The total module footprint is 74.3 mm × 49.2 mm × 11.4 mm, including the decouping capacitors, but not the housing. This gives a power density of 13.0 W/mm$^3$. With the housing and integrated cooler, the dimensions become 83.3 mm × 68.2 mm × 24.7 mm, which results in a power density of 3.8 W/mm$^3$. For reference, the power density of Wolfspeed's 10 kV, 240 A SiC MOSFET module is 4.1 W/mm$^3$ without the cooling system [108]. The footprint of the proposed power module includes pads for wire bonds in case the posts could not be successfully connected to the small MOSFET gate pads. Since successful connection was achieved, future revisions could eliminate these extra pads. This would further reduce the module size to 83.3 mm × 54.2 mm × 24.7 mm, thereby increasing the power density to 4.8 W/mm$^3$ with the housing and cooler. The various aspects of the module design evolution will be discussed in more detail in the following sections.

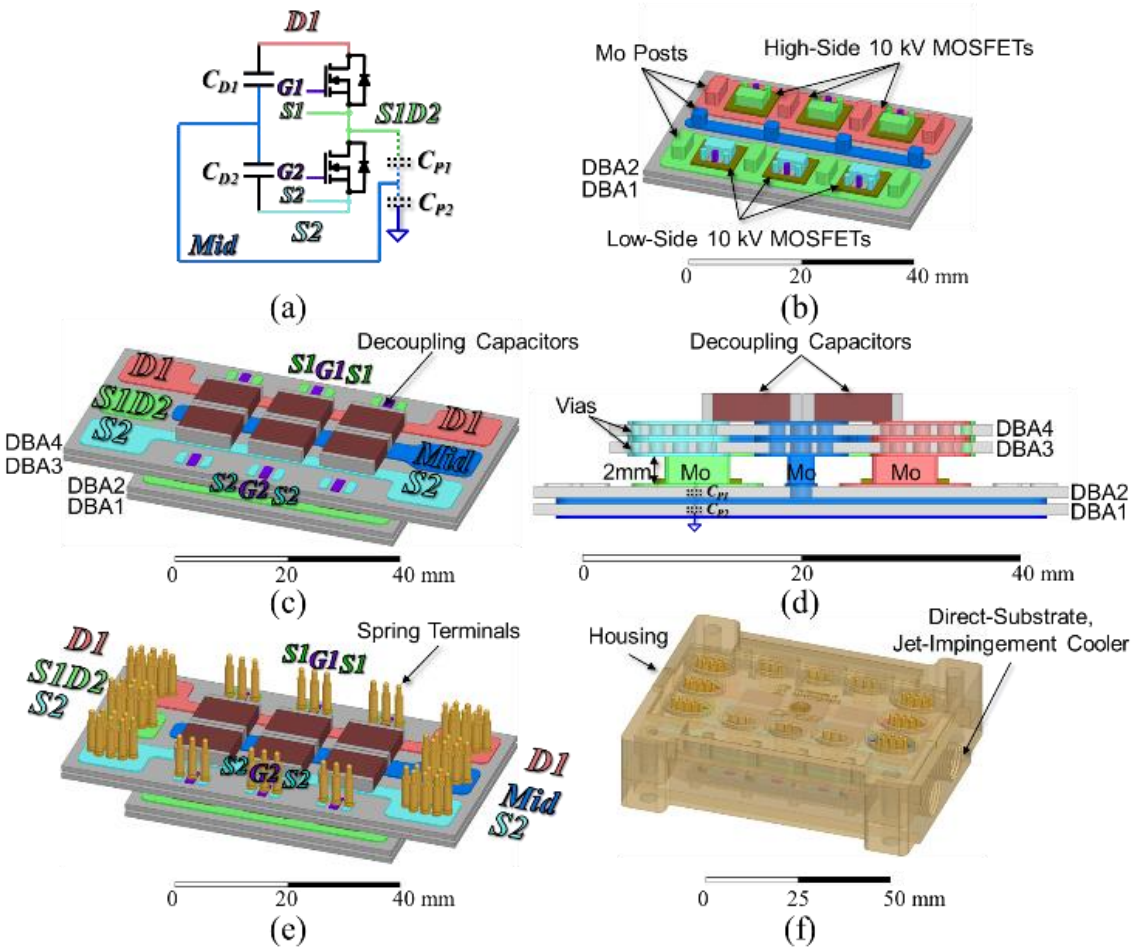



**Figure 3-3: (a) Schematic, (b) bottom stacked substrates with six 10 kV SiC MOSFET die and posts, (c) top substrates stack and embedded decoupling capacitors, (d) side view with the vias shown, (e) module with spring terminals, and (f) housing with integrated direct-substrate cooler.**

## *3.4 Insulating Substrate Design*

As mentioned earlier, the desire to create a high density package for medium-voltage devices means the electric field strength within the module will be increased. If the electric field magnitude exceeds the electrical breakdown strength of the dielectric materials, then PD can occur, potentially causing permanent damage to the insulating materials, such as the insulating ceramic substrate [79]. Accordingly, the electric fields

both within the power module and at the external terminations to the rest of the power conversion system must be carefully controlled. Recently, there has been focus on mitigating the electric fields around the insulating substrate, as this is typically where the highest fields occur inside the power module [80],[81],[82],[143].

In order to address the enhanced electric field and thermal effects associated with a high-voltage, high-density design, the DBA substrate must be thoughtfully designed and evaluated. The ceramic of the DBA typically has a dielectric strength around 20 kV/mm. At 10 kV, one would think that 1-mm-thick AlN would provide sufficient margin for the module to operate reliably at this voltage. However, the peak electric field strength will actually be much greater than the expected 10 kV/mm. This is because the electric field will be highly concentrated at the triple point, which is where the ceramic (i.e., AlN), metal (i.e., Al), and encapsulation meet [80],[81],[82],[143]. If this electric field exceeds the breakdown field strength of the insulation materials (i.e., the AlN or encapsulation), then PD can occur. Repetitive PD events can ultimately result in insulation failure, such as cracking of the ceramic substrate as shown in [79], thus destroying the power module.

In [89], it was found that the PDIV for a standard 1-mm-thick aluminum nitride (AlN) DBC substrate immersed in isolation fluid was 7.7 kV, on average, and could be as low as 5 kV. While it was not stated in the paper, it is assumed that these are rms values, as traditional PD tests use a 50 Hz or 60 Hz ac voltage excitation. In this case, the results would be in good agreement with those in [79], which also found the PDIV of a 1-mm-thick AlN substrate immersed in inert fluid to be around 13.5 kV (assumed to have been converted from rms to peak voltage). Clearly, this is unacceptable for 10 kV SiC MOSFETs. Accordingly, methods for reducing the peak electric field in the power module

need to be explored. A review of proposed methods will be discussed in the following section.

### *3.4.1 Literature Review of Proposed Solutions to Improve the Partial Discharge Performance of the Insulating Substrate*

As stated previously, there have been several proposed solutions to reduce the electric field strength at this critical triple point. The solutions related to the insulating substrate will be discussed in this section. The proposed solutions include: increasing the ceramic thickness [79]; varying the pad size [79], pad corner curvature [79], the offset between the top and bottom pads [79], and the metal-ceramic interface geometry [85],[90], [144]; and stacking multiple substrates [89]. The advantages and disadvantages of these methods will be discussed in detail in this section.

In [79], the geometry of DBC substrates was varied to analyze the impact on the electric field and PDIV. Two types of ceramics were evaluated: AlN and alumina/aluminum oxide ($Al_2O_3$). The AlN samples had thicknesses of 0.63 mm and 1.0 mm, while the $Al_2O_3$ samples had thicknesses of 0.38 mm and 0.63 mm. For the same thickness (i.e., 0.63 mm), no differences in the simulated electric fields or experimental PDIVs were found for the two types of ceramic [79]. Next, the impact of the ceramic thickness was assessed. As expected, it was found the simulated electric field reduces and the experimental PDIV increases as the ceramic thickness is increased [79]. However, the benefit is limited; doubling the ceramic thickness does not halve the electric field or double the PDIV [79]. In other words, the high electric field at the triple points do not follow the linear E=V/d relationship [79]. In [79], PD tests showed a 69 % increase in PDIV for a 163

% increase in the ceramic thickness (from 0.38 mm to 1.0 mm). Since increasing the ceramic thickness increases the thermal resistance of the power module, continuing to increase the ceramic thickness is not preferred. Instead, other methods should be explored to further reduce the electric field/increase the PDIV. The researchers also investigated the influence of the size and corner curvature of the metal pads; no significant influence on the experimental PDIV measurements were observed [79].

This is contrary to [145], which found that the number and magnitude of PD events noticeably increase as the size of the DBC increases and the corner radius of curvature decreases. Specifically, in [145], at 10.0 kV, the number of PD events and the summarized apparent charge increased by 500 times and 40 times, respectively, as the lateral length increased just three times (from 5 mm to 15 mm). It was also reported in [145] that the PDIV of samples with a metal pad size of 47 mm × 47 mm was half that of those with a pad size of 5 mm × 5 mm. Regarding the corner radius, in [145], at a peak voltage of 7.0 kV, the number of PD events and the summarized apparent charge decreased by 96 % and 93 %, respectively, by changing the metal shape from a 40-mm-wide square (i.e., approximately 90 degree angles) to a 40-mm-diameter circle. In [145], it was also found that the etching rate used to pattern the metal in the DBC manufacturing process also has an impact on the maximum apparent charge, with low etch rates having higher apparent charge than longer etch rates [145]. This is because low etch rates can result in a thin layer of metal remaining on the ceramic surface [145]. The electric field at the end of this layer is very high and is likely to result in PD [145]. However, the number of PD of low apparent charge was not affected by the etch rate (i.e., the thin metal layer) [145]. In [82], influence of the etching process on the PDIV is also discussed. It should be noted that in [79], the

PDIV was used as the metric to compare the different DBC geometries, whereas in [145] the same voltage was applied to each sample, and the number and magnitude of PD events were compared.

In [79], the impact of the offset between the top and bottom metal pads on the PD performance was also investigated. The offset was varied from -1.0 mm to +2.0 mm in 0.5 mm increments; a negative value indicates the top pad is larger than the bottom, while a positive value indicates the reverse [79]. The experiments showed that the maximum PDIV is achieved when the offset is zero (i.e., the top and bottom metal pads are the same size) [79]. This was true for AlN and $Al_2O_3$ substrates of 1.0 mm, 0.63 mm, and 0.38 mm thicknesses [79]. Moreover, it was found that the reduction in PDIV as a result of an increase in offset was more significant for thinner ceramic [79]. For the 0.38-mm $Al_2O_3$, the PDIV increased by 51 % when the offset was decreased from 2 mm to zero [79]. For the 0.63-mm $Al_2O_3$ and AlN, the PDIV increased by 25 % for the same change in offset [79]. Finally, the 1.0-mm AlN only experienced a 17 % increase in its PDIV when the offset was reduced [79].

In [85], it was proposed to embed the top metal pad into the ceramic and round the sharp corners. With this structure, the highest electric field occurs inside the ceramic instead of the encapsulation [85]. Due to the increased radius of curvature of the corner, the peak electric field is noticeably reduced. This was verified by 2D electric field simulations [85]. Of course, this structure is not trivial to fabricate and will incur additional costs. No prototypes or experimental results were reported in [85]. Furthermore, no solutions for the bottom metal pad (and thus the bottom triple points) were proposed in

[85]. The overall ceramic thickness may need to be increased as a result of the metal embedding, which would increase the thermal resistance of the power module.

In [90], the researchers proposed a protruding structure, where the ceramic underneath the edges of the metal pad are removed and filled with encapsulant. The edges of the Cu that overhang are rounded. In this way, the electric field is distributed along the rounded edge of the metal instead of at a single point (i.e., the triple point) [90]. Hence, the peak electric field is reduced compared to a traditional DBC substrate structure [90]. When the samples are immersed in dielectric fluid, the PDIV of the protruding substrates increased by 38 % compared to a traditional substrate [90]. However, when the samples are encapsulated with silicone gel, the PDIV of the protruding substrates decreased by 58 % compared to the samples that were immersed in the fluid [90]. On the other hand, the PDIV of the encapsulated traditional substrates only decreased by 21 % [90]. Additionally, the dispersion of PDIV values for the encapsulated protruding samples was very wide, ranging from 1.7 kV to 6.5 kV. The majority of these values were less than the PDIV values for the encapsulated traditional substrates [90]. This could be due to poor encapsulation quality, such as the presence of voids and/or contamination [90]. This result shows the difficulty to implement such a structure, in addition to the manufacturing challenges. Furthermore, there were again no solutions for the bottom metal pad (and thus the bottom triple points).

In [144], a trench structure was proposed. When the trench height is 0.6 mm, the simulated electric field strength reduces by 57 % [144]. However, this requires a significant increase in the ceramic thickness, which will increase the thermal resistance.

In [89], it is proposed to stack DBC substrates one on top of the other, thereby reducing the electric field strength both within the bulk ceramic and at the critical triple points. The paper analyzed the electric field distribution for a simple substrate structure, and found the peak electric field at the triple points could be reduced when stacking two substrates, even when they result in the same overall thickness [89]. The PD tests revealed that the PDIV could be increased by 94 % by stacking two 0.32-mm $Al_2O_3$ substrates compared to having a single 0.63-mm substrate [89]. The impact of stacking a third ceramic substrate was also simulated, and found to have a small additional benefit of just 15 % lower electric field [89]. This could in part be due to the large baseplate used in the simulation model, which reduced the homogeneity of the electric field [89]. Furthermore, the simulation results showed that as the total ceramic thickness increases, the reduction in electric field strength achieved when using two stacked substrates compared to a single substrate diminishes (42 % at 0.63-mm total thickness to 33 % at 1.3-mm thickness) [89].

However, the practical implementation of this method was not discussed in [89]. For instance, in a power module, the top and bottom metal layers are not symmetrical; the top metal is patterned to create the circuit (e.g., half bridge). Further, the various traces in the top metal pattern are at different potentials during the module operation. Due to the asymmetry and different potentials of the top metal traces, the isolation capacitances across the ceramic layers could have a large disparity. As a result, if the middle metal layer of the substrate stack is left floating, then it may not be at a potential that will yield a meaningful reduction in the electric field strength.

This phenomenon is demonstrated by ANSYS Maxwell 2D electrostatic simulations (Figure 3-4). Figure 3-4a and Figure 3-4b show the electric field distribution

for the case when the top and bottom metal layers, and thus the isolation capacitances, are symmetrical. For this case, the peak electric field strength, both within the bulk ceramic (AlN in this case) and at the triple points, are reduced by 40 % when two substrates are stacked together (Figure 3-4b) compared to when there is only a single substrate (Figure 3-4a). This reduction is due to the potential of the middle metal layer, which, due to the vertical symmetry of the stacked substrate structure, floats to half of the voltage applied across the top and bottom metal layers. For example, when 10 kV is applied across the top and bottom metal layers, then, due to the vertical symmetry, the middle metal layer will float to 5 kV.

Figure 3-4c and Figure 3-4d show the electric field distribution for the case when the top metal substrate is patterned and has different potentials (as would be the case in an actual power module). It can be seen that, when the middle metal layer is left floating, the peak electric field strength is not as notably reduced (Figure 3-4c) compared to the case with the vertical symmetry (Figure 3-4b). This is because the asymmetry and different potentials cause the middle metal layer to float to a potential that is less than half of the applied voltage (2.4 kV for this example). Accordingly, the reduction in the peak electric field is not as prominent (27 % compared to 40 %). However, if the middle metal layer is electrically connected to half of the applied voltage (Figure 3-4d), then the electric field is again reduced by 40 % compared to the single-substrate case (Figure 3-4a). This method of stacking two substrates and connecting the middle metal layer to half of the applied voltage is the proposed solution in this work. Further details of the design and implementation will be discussed in the following sections.

It should also be noted that none of the previously proposed solutions were implemented and tested in an actual power module, and, as mentioned, several of those methods are not practical for module fabrication and manufacturing. The method proposed in this work, on the other hand, is effective at reducing the peak electric field, and thus increasing the PDIV, while also being practical and simple to fabricate and implement.

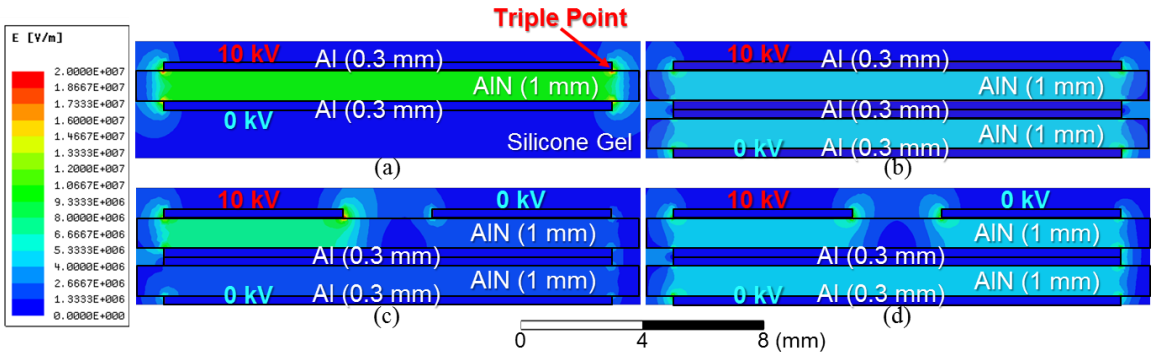



**Figure 3-4: Simulated 2D electric field plots for single and stacked substrates.**

### *3.4.2 Bottom Substrate Design (DBA1 and DBA2)*

Finite element electrostatic simulations were performed using ANSYS Maxwell 16.0 (later updated to ANSYS Electronics Desktop 2017.2.0) in order to develop an insulating substrate design suitable for a 10 kV application. However, while the finite element method (FEM) has many benefits, it is unable to accurately model the triple points, which is essential for developing an optimized module design. Typically, the metal-ceramic-encapsulant interface is embodied as a sharp edge (Figure 3-4). As a result, a singularity exists at the edge, creating an infinite electric field strength. Accordingly, the simulated electric field strength at this point will depend on the resolution of the mesh; as the mesh size is reduced, the electric field magnitude at the triple point will increase.

In [143], it was shown that FEM software could accurately predict the electric field when the measurement point is at least 20 μm from the triple point. It is claimed this method is independent of the mesh; though, only mesh sizes of 25 μm and below were evaluated in [143]. If the mesh size is much greater than 25 μm, then the measurement points may need to be farther away from the triple point edge. Nevertheless, this is a good solution for using FEM to simulate the electric field distribution near a triple point. In this work, however, the plots of the electric field distributions were used to evaluate the effect of design variations, rather than extracting an exact value at select points.

First, 2D electrostatic simulations were carried out using ANSYS Maxwell. The maximum length of the mesh element was set to 0.2 mm for all objects, and the maximum number of elements was restricted to 60,000 to avoid long simulation times and/or freezing of the computer/simulation (e.g., due to running out of memory). Figure 3-5 shows an example of the resulting mesh for a single substrate and two stacked substrates. Each substrate has 1-mm-thick AlN and 0.3-mm-thick Cu. This example is only showing the mesh in the ceramic. For the stacked substrate sample, the middle metal is two times the thickness of the top or bottom metal (i.e., 0.6 mm). This would be the case when two identical substrates are bonded together, as is done in this work, due to the lack of suitable (i.e., medium voltage) multilayer ceramic substrates at the time of this work. Note that these simulations are roughly to scale; the simulated substrates are 49 mm long (similar to that of the final design) with 2 mm distance between the end of the metal and the end of the ceramic. Leaving space between the edge of the metal and the edge of the ceramic is common practice. This spacing provides creepage distance between the top and bottom

metal pads and can be used to mitigate the impact of poor etching of the metal on the ceramic surface.

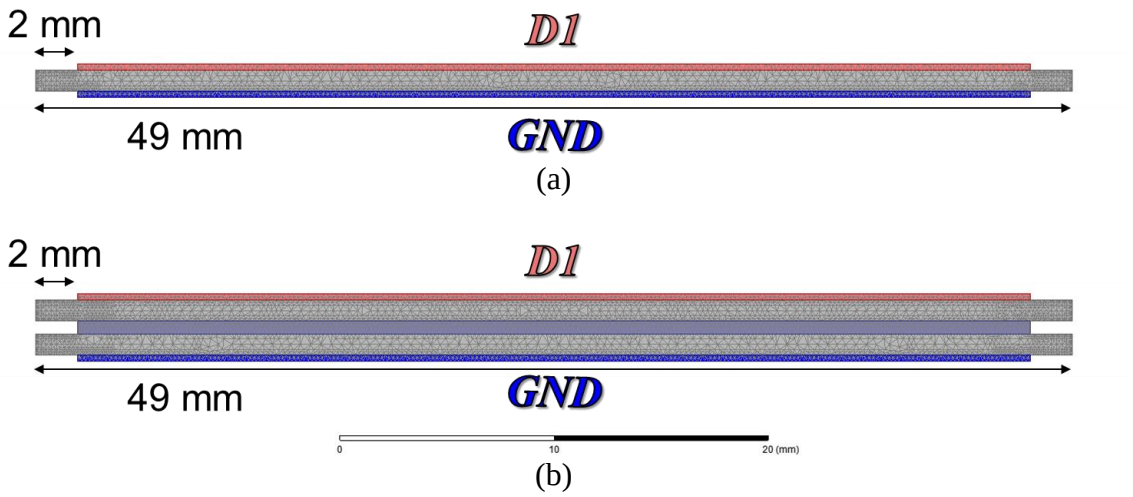



**Figure 3-5: Generated meshes for the 2D electrostatic simulations of the (a) single and (b) stacked substrate cases.**

As stated previously, in [89], it was shown the PDIV could be increased by 94 % by stacking two 0.32-mm $Al_2O_3$ substrates compared to having a single 0.63-mm substrate. To better understand the reason for this significant reduction, 2D electrostatic simulations were performed. In Figure 3-6, the electric field distributions for a single 0.63-mm $Al_2O_3$ substrate, two 0.32-mm $Al_2O_3$ substrates with 0.6-mm middle metal, and two 0.32-mm $Al_2O_3$ substrates with 0.3-mm middle metal, are shown for the case when 6 kV is applied to the top metal while the bottom metal is grounded. As can be seen from the figure, since the overall thicknesses are nearly the same, the electric field strengths within the bulk ceramics are similar. However, the electric field strengths at the triple points are reduced when two thinner substrates are stacked compared to the thicker single substrate.

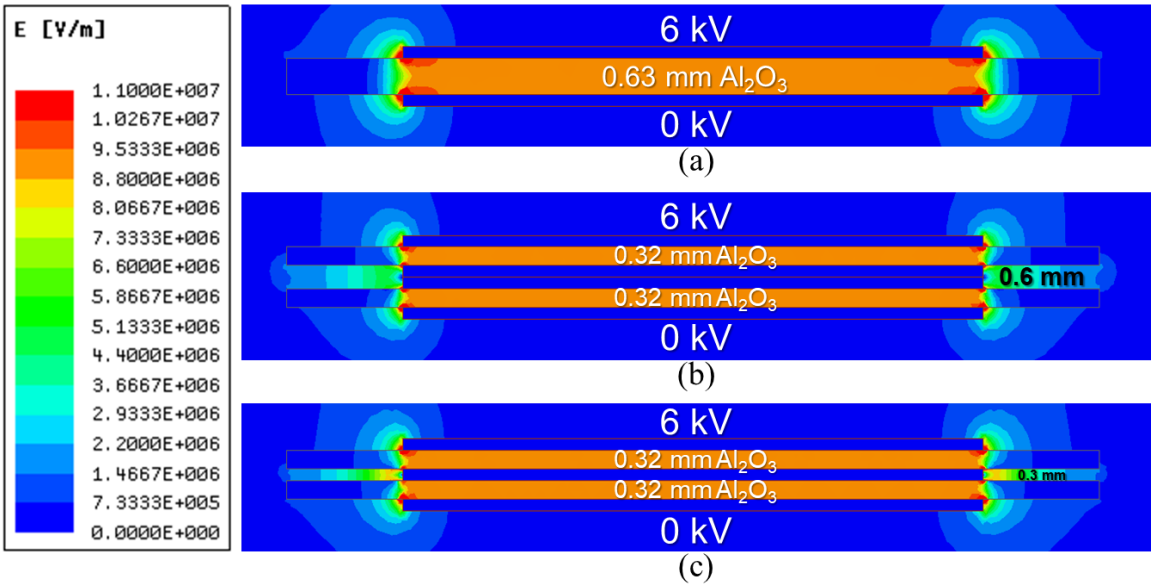



**Figure 3-6: Simulated 2D electric field strength of (a) single 0.63-mm $Al_2O_3$, (b) two 0.32-mm $Al_2O_3$ with 0.6-mm middle metal, and (c) two 0.32-mm $Al_2O_3$ with 0.3-mm middle metal.**

In [89], the distance of each metal layer to the edge of the ceramic was varied. Three types of structures were evaluated: 1) a uniform structure where all metal layers are equal distances from the ceramic edge, 2) a pyramid structure where the top metal is the farthest from the ceramic edge and the bottom metal is the closest to the ceramic edge, and 3) a recessive structure where the top and bottom metal pads are the same distance to the edge and the middle metal is recessed [89]. The distances of the metal pads from the ceramic edge were varied from 0.25 mm to 1.0 mm [89]. While the details of the simulation results for each of these structures were not presented in [89], it was shown that the 1.0-mm recession of the middle metal layer had the lowest simulated electric field strength compared to the case with lower recessions. When two substrates were stacked together, the model with a 1.0-mm recess had approximately 10–14 % (depending on the total ceramic thickness) lower simulated peak electric field strength compared to the model with

a 0.25-mm recess [89]. However, it is not clear which structure(s) was (were) tested in the experiments shown in [89].

Due to the lack of details provided in [89] regarding the simulations for the different structure types, and since no baseplate will be used in the proposed power module, further analysis on the impact of the distances of the metal layers to the ceramic edges on the electric field distribution is provided in this work through 2D electrostatic simulations. Figure 3-7 shows the simulated 2D electric field distributions for two stacked 1-mm AlN substrates with 0.3-mm Cu metallization on the top and bottom, and 0.6-mm in the middle. In the simulation, 10 kV is applied to the top metal and 0 V is applied to the bottom metal. The four cases shown are as follows: 1) no recess (all distances from the metal layers to the ceramic edges are equal), 2) 1-mm extension of the middle metal layer, 3) 1-mm recession of the middle metal layer, and 4) 0.5-mm recession of the middle metal layer. As can be seen from Figure 3-7a and Figure 3-7b, the 1-mm extension causes the electric field strength at the top and bottom triple points to increase, while those in the middle decrease. In Figure 3-7c, the opposite occurs; the electric field strength at the triple points on the top and bottom are reduced while those in the middle are increased. It can also be observed that the electric field strength in the encapsulant in the gap between the two ceramics is increased directly underneath and above the top and bottom triple points, respectively. The case with a 0.5-mm recession, shown in Figure 3-7d, appears to have the best balance between the electric field strength at the various triple point locations, indicating that this structure may result in the highest PDIV. However, the electric field between the ceramics is higher compared to the uniform case in Figure 3-7a. Consequently, if there are any defects, such as voids, in the encapsulant in this region, then the PDIV may be reduced.

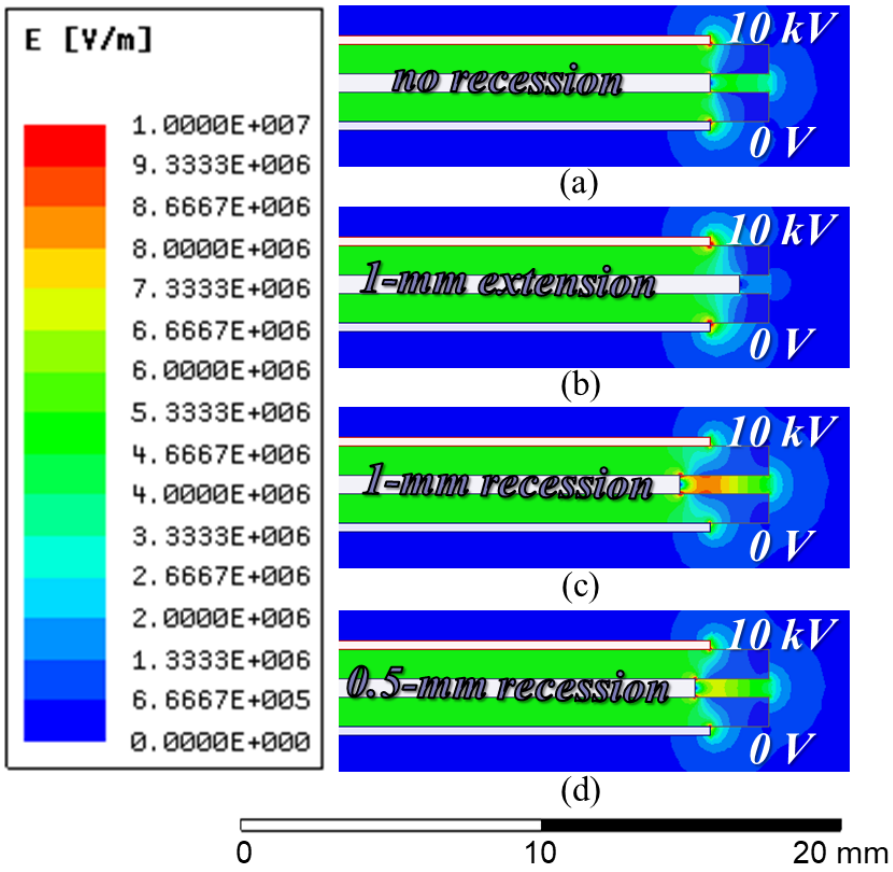



**Figure 3-7: Simulated 2D electric field distribution for two stacked 1-mm AlN substrates with the middle metal at recessions of (a) 0 mm, (b) -1.0 mm, (c) 1.0 mm, and (d) 0.5 mm relative to the top and bottom metal pads.**

While this simulation provides a good depiction of the influence of the recession on the electric field distribution, this was a simplified case. As stated previously, the actual power module substrates will have more complex patterns and different potentials on the upper layer. Figure 3-8 shows a 2D model of the final design for the proposed power module. This final design will be discussed in more detail later in this section. Figure 3-9 shows the simulated 2D electric field distribution for the model shown in Figure 3-8. The simulated cases are: 1) floating middle metal with 0.5-mm recession, and middle metal at half the applied voltage (i.e., 5 kV) with 2) 0.5-mm recession, 3) 0-mm recession, and 4)

0.5-mm extension. For all of these cases, the drain of the high-side switch (D1) is at 10 kV, and the low-side switch drain (S1D2) and source (S2) are both at 0 V. This models the case when the high-side switch is blocking and the low-side switch is conducting. As will be shown later, this switch state results in the worst-case electric field strength. Figure 3-9a illustrates if the middle metal is left floating, then the electric field strength is heavily concentrated around the D1 pad. As can be seen by the electric field strength in the two ceramic substrates, the middle metal is floating to a potential that is close to the potentials of S1D2 and S2 (i.e., 0 V). This was verified by plotting the voltage distribution (Figure 3-11a).

Figure 3-9b–Figure 3-9d have the middle metal fixed at 5 kV. Figure 3-9b has a recession of 0.5 mm. As can be seen from the figure, the electric field strength is greater at the middle triple points than at those at the far ends on the top and bottom. In Figure 3-9d, the 0.5-mm extension causes the opposite effect; the electric field strength at the top and bottom triple points on the far ends are greater than at those in the middle. Figure 3-9c, which simulates the case with no recession, shows the electric field is well distributed between the top and bottom far-end triple points and those in the middle. This is contrary to the result shown in Figure 3-7 and demonstrates the significance of simulating the more detailed model. Accordingly, no recession is used in the final design.

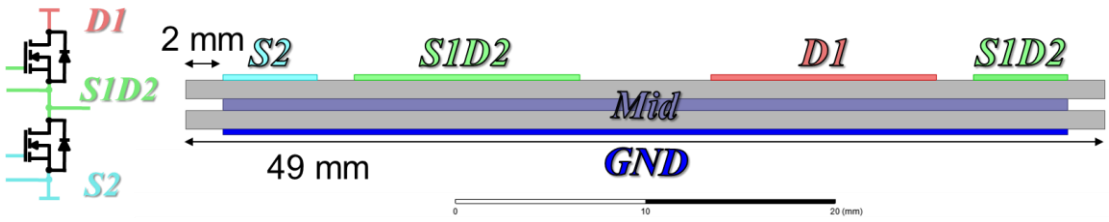



**Figure 3-8: 2D model of the side view of the bottom substrates with a top metal pattern.**

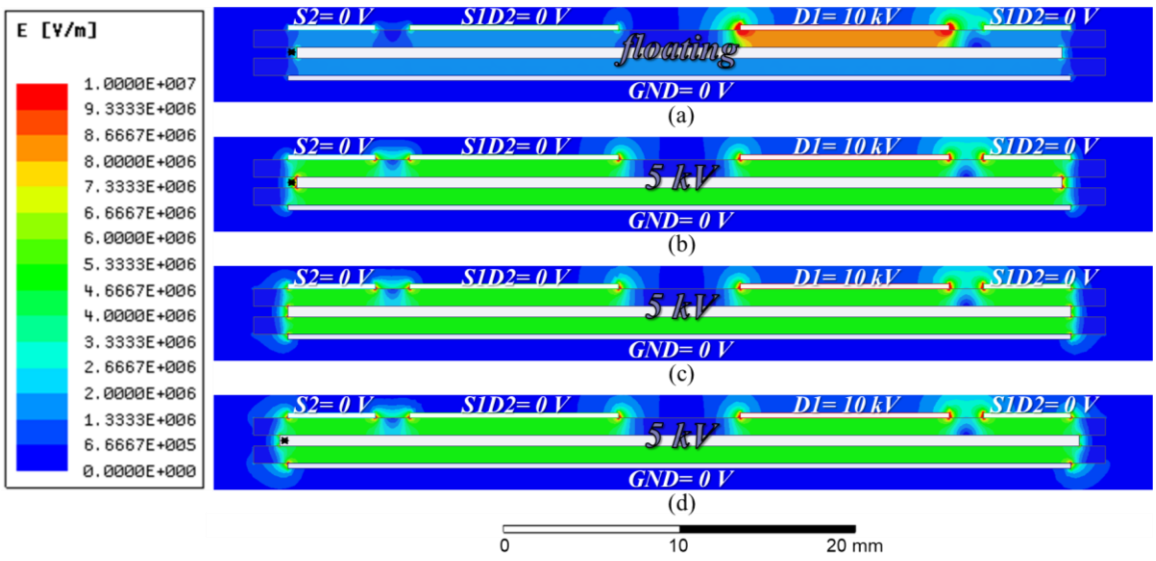



**Figure 3-9: Simulated 2D electric field distribution for two stacked substrates with S1D2= S2= 0 V and the middle metal (a) floating and a recession of 0.5 mm, and at 5 kV and recessions of (b) 0.5 mm, (c) 0 mm, and (d) -0.5 mm.**

Figure 3-10 displays the case when the high-side switch is conducting and the low-side switch is blocking. In other words, S1D2= D1= 10 kV and S2= 0 V. As was the case when S1D2= S2= 0 V (Figure 3-9), the model with no recession (Figure 3-10c) has the lowest electric field at the triple point locations near the substrate edges. However, unlike the previous case, it can be seen from Figure 3-10a when the middle metal is left floating, the electric field distribution is not noticeably worse as when the middle metal is at half the applied voltage (Figure 3-10b). This is because now the majority of the top metal pads are at 10 kV, thereby distributing the electric field more uniformly over the substrate.

This is shown by Figure 3-11. Figure 3-11a plots the voltage distribution for the case when S1D2= S2= 0 V and the middle metal is floating. The simulation shows the potential of the middle metal is around 1 kV. As a result, the field lines are heavily concentrated around the D1 (10 kV) pad. In Figure 3-11b, the middle metal is at 5 kV. As

a result, the field lines are more uniformly distributed. Figure 3-11c shows the case when S1D2= D1= 10 kV and the middle metal is left floating. In this case, the middle metal floats to nearly 4 kV. This results in a more uniform distribution in the field compared to Figure 3-11a, though further homogeneity can be achieved by connecting the middle metal to 5 kV (Figure 3-11d).

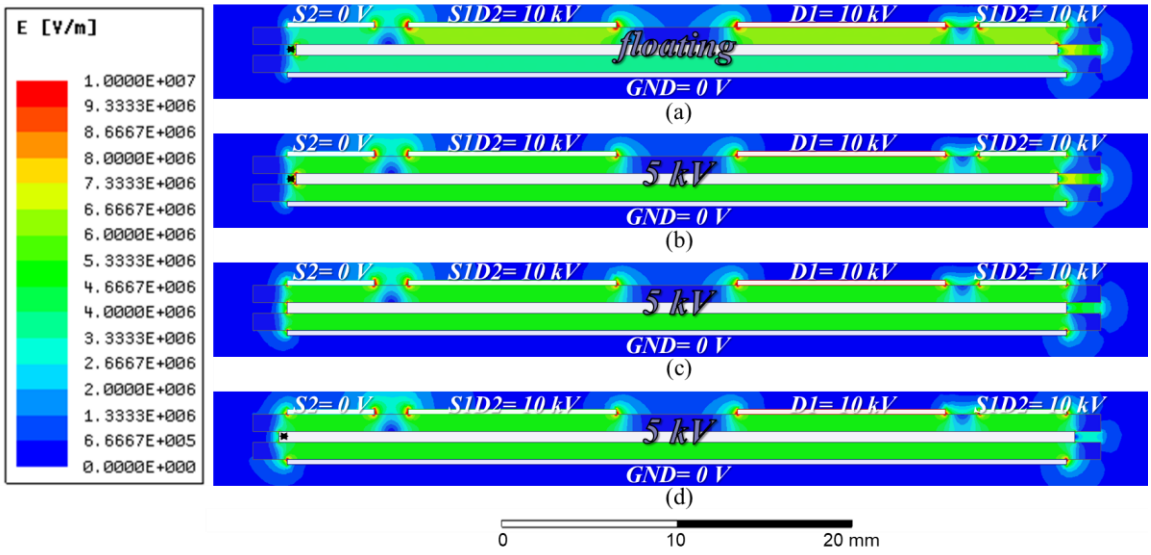



**Figure 3-10: Simulated 2D electric field distribution for two stacked DBCs substrates with S1D2= D1= 10 kV and the middle metal (a) floating and a recession of 0.5 mm, and at 5 kV and recessions of (b) 0.5 mm, (c) 0 mm, and (d) -0.5 mm.**

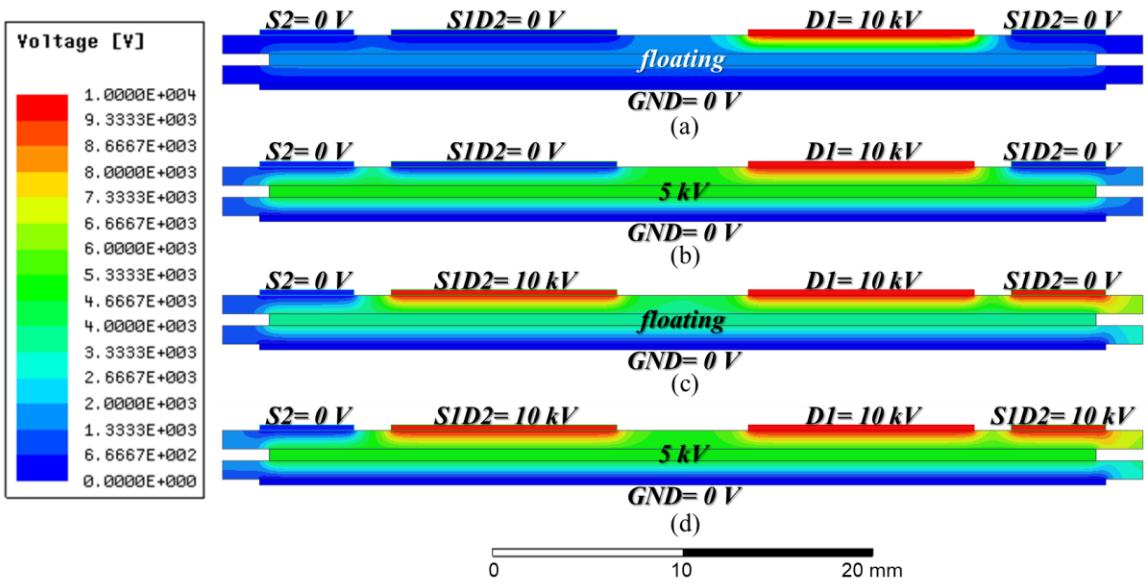



**Figure 3-11: Simulated 2D voltage distribution for two stacked substrates with S1D2= S2= 0 V and the middle metal (a) floating, and (b) at 5 kV, and S1D2= D1= 10 kV and the middle metal (c) floating, and (d) at 5 kV.**

The influence of field grading rings on the electric field distribution was also explored in this work. Rings were placed around the D1 and S1D2 pads. The width and potential of the rings, and the distance between the rings and the pads, were varied. The simulation results did not show any significant impact on the electric fields near the triple points. Accordingly, no field-grading rings were included in the substrate design. Other cases that were simulated were: stepped metal edges, sloped metal edges, patterned middle metal layer, and embedded material in the ceramic. The simulations showed little influence on the electric field distribution. The simulation results for these cases are included in the appendix.

The size and arrangement of the top metal pads were determined by several factors: the parasitic capacitance to the heatsink, thermal resistance, current density, and parasitic inductance. For instance, a larger pad size will improve the lateral heat spreading, as well

as increase the current capacity, and reduce the parasitic inductance. The metal thickness also has a large impact on these factors. At the same time, a large pad size results in a higher capacitance to the heatsink, which can cause detrimental EMI. Larger pad sizes also increase the module footprint. Accordingly, an optimal pad size is one that is large enough to provide sufficient spacing between the dies to minimize thermal coupling, yet small enough to reduce the parasitic capacitance and module footprint.

Figure 3-12 shows the final bottom DBA substrate pattern. A spacing of 5.5 mm between the 8.1 mm × 8.1 mm dies was chosen. This spacing allows for low thermal coupling between the dies while maintaining a compact design with low parasitic inductances, variation of the inductances among the paralleled dies, and parasitic capacitances to the bottom metal (i.e., the heatsink ground).

Due to the small size of the MOSFET gate pads and their close proximity to the source pads, it was not certain if the post attachment to the gates would be successful. As a backup, additional pads were added to the substrate to accommodate wire bonds for the gate and Kelvin source. With these pads, the dimensions of the bottom substrates are 50.3 mm × 49.2 mm (1.98 inches × 1.94 inches).

The distances between the metal pads, and from the end of the outer metal pads to the edge of the ceramic, are also important parameters, especially for high-voltage modules. The distance should be large enough to reduce the electric field strength and minimize the chance of a short-circuit, yet small enough to enable low parasitic inductance and small footprint. A distance of 2 mm was chosen to satisfy these requirements. A distance of 2 mm for a 10 kV module gives an electric field strength of 10 kV/mm,

providing sufficient margin to the dielectric strengths of the encapsulant and ceramic. Of course, this distance also has an impact on the electric field strength at the triple point.

For the stacked substrate structure, no recession was used in this design. The top metal pattern is symmetric for improved current sharing among the paralleled dies. Details of the current distribution will be shown in the next section. Metal pads were also included in the corners for thermistors. These thermistors allow the substrate temperature to be monitored in real time. 3D electrostatic simulations were performed on the final model for the bottom DBA substrate structure. The electric field distribution for the case when the low-side switch in the half bridge is blocking 10 kV (i.e., S1D2= D1= 10 kV) is shown in Figure 3-13, along with the defined mesh for the simulation. As can be seen from the figure, the electric field strength under this condition is roughly 5 kV/mm in the bulk of the ceramic (underneath the metal pads). This is expected since the middle metal layer is at 5 kV. As anticipated, the electric field strength at the triple points around the metal pads is significantly higher—exceeding 10 kV/mm.

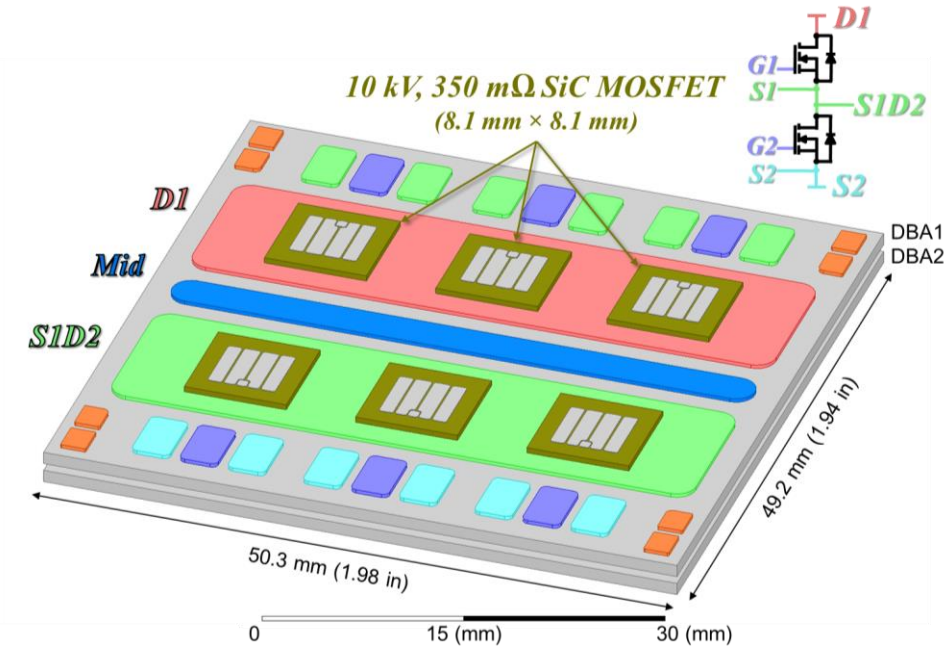
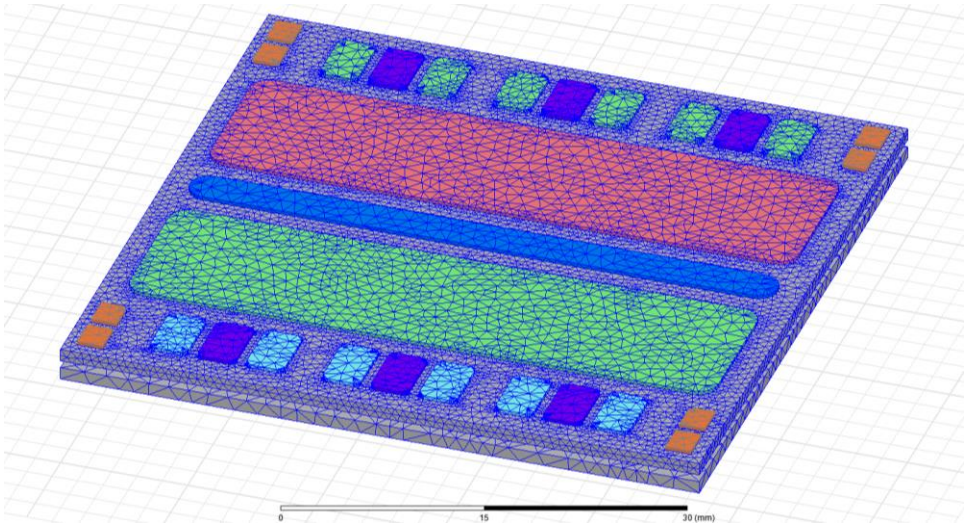
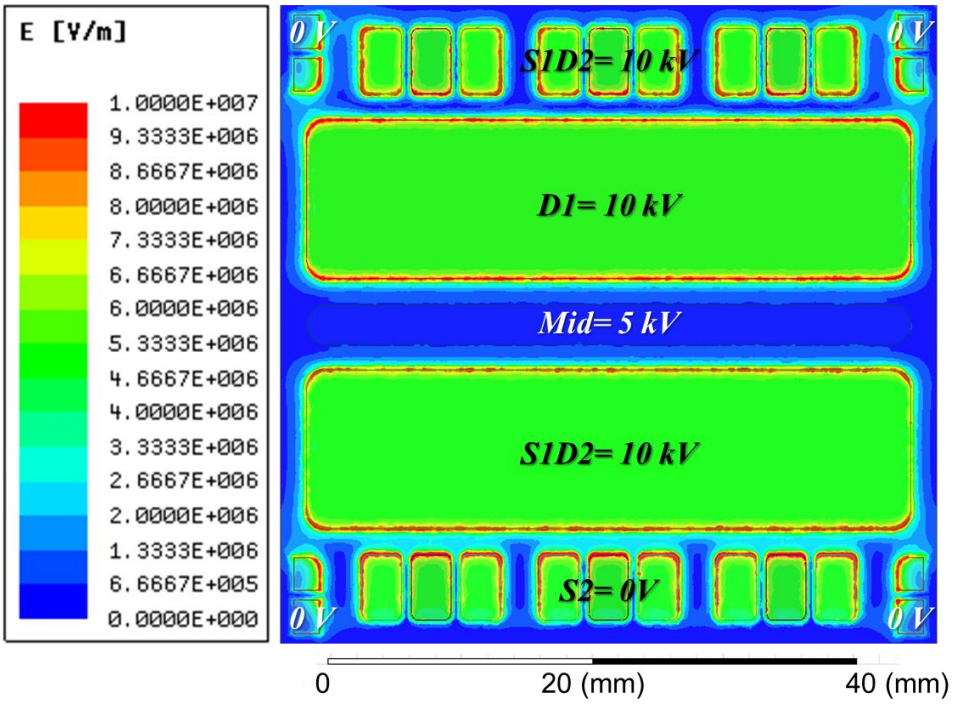



**Figure 3-12: Final design for the bottom substrate stack and 10 kV SiC MOSFET die locations.**




(a)




(b)

**Figure 3-13: (a) Mesh for the 3D electrostatic simulations of the bottom substrate stack, and (b) the electric field distribution on the top surface of the bottom substrate stack for S1D2= D1= 10 kV.**

### *3.4.3 Top Substrate Design (DBA3 and DBA4)*

Thus far, only the bottom substrates have been discussed. However, the top substrate design also requires careful analysis. Figure 3-14 shows how the source of the high-side switch (S1) will be connected to the drain of the low-side switch (D2) using the bottom metal of the top substrate (DBA3). The shape of this metal pad was adjusted based on current density and electric field simulations. Figure 3-15 shows how increasing the radius of curvature improved the uniformity of the current density and electric field distributions.

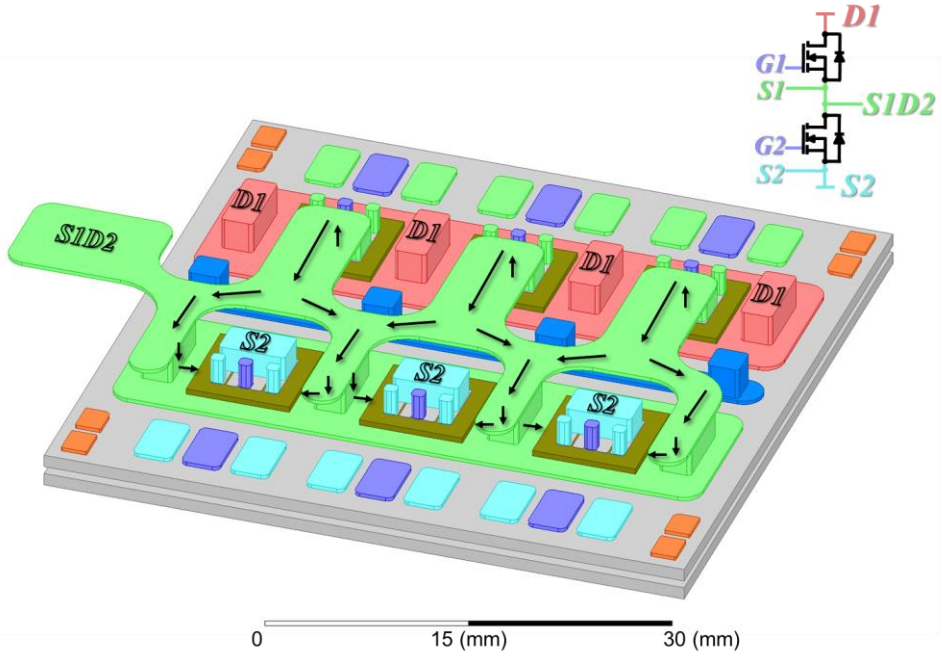
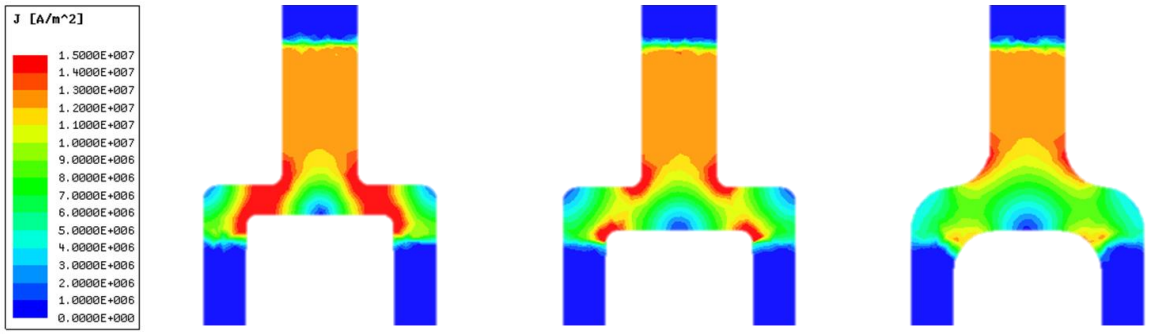
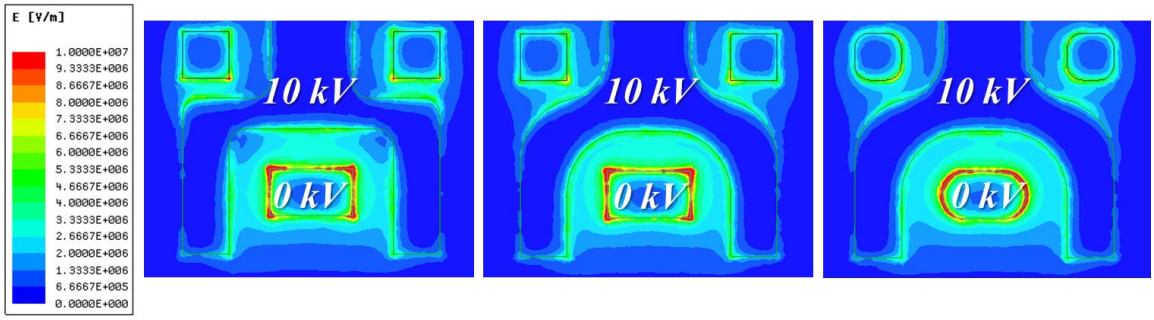



**Figure 3-14: Connection from the source of the high-side switch (S1) to the drain of the low-side switch (D2).**




(a)




(b)

**Figure 3-15: Simulated (a) current density and (b) electric field distributions for different designs of the S1D2 pad on the bottom of DBA3.**

Figure 3-16 shows the design for a single top substrate; the ceramic was made transparent so the pads on the bottom could be clearly seen. There were several factors constraining the pad sizes, locations, and spacing, including the MOSFET die pads, size of the embedded decoupling capacitors (to be discussed in the following section), and terminal connections (to be discussed later in this chapter). Additionally, it is desirable to cover both sides of the ceramic with metal pads in order to maintain good thermomechanical performance. The symmetry of the metal on the top and bottom of the ceramic will also impact the bending under temperature variations.

The module termination is done from the topside of the topmost substrate (DBA4). These termination pad sizes were determined by the size of the terminal connectors, which

will be discussed in a later section. The pad arrangement is very important for the system integration; a poor layout can make interfacing to the bus bar, gate driver, etc. difficult for the system designer. At the same time, as mentioned previously, symmetry is essential in balancing the parasitics among the paralleled dies. For these reasons, the pattern shown in Figure 3-16 was selected; the D1 and S2 connections are on both sides of the power module, S1D2 is in between them on one side, and the middle metal layer is between them on the opposite side. Having D1 and S2 on both sides balances the power-loop parasitics for the paralleled dies. Of course, having the decoupling capacitors significantly improves the balancing. Moreover, having double the terminals reduces the inductance and resistance, allowing for faster switching and higher current.

The S1D2 terminal is only on one side of the module because, typically, it is beneficial to have distinct sides for the input and the output. The S1D2 is connected to the load, so the left side is considered to be the output side. The “Mid” terminal is placed on the right side. This could be used to connect the midpoint of external capacitors to further stabilize the potential of the middle metal layer. It could also be beneficial for filtering. The right side could thus be considered the input side. The gate and source connections for the high-side and low-side switches are on the far and near sides, respectively. This perpendicular orientation to the power loop improves the decoupling between the signal and power loops.

If D1 and S1D2 or S2 and S1D2 overlap, then the high potential difference across the ceramic will cause a high electric field strength not only within the ceramic, but also at the triple points in this area. To reduce the peak electric field, this overlap should be avoided. Unfortunately, the overlap between D1 and S1D2 is unavoidable; these overlap

areas are identified in Figure 3-16. Figure 3-17 shows the electric field distributions from 3D electrostatic simulations for the single and stacked substrate cases when S1D2 is equal to S2 (i.e., 0 V) and D1 is equal to 10 kV. As can be seen from the figure, when a single substrate is used, the electric field in the areas with the overlapping D1 and S1D2 traces has the highest electric field. By stacking two substrates, this electric field strength is reduced by more than 50 % at the triple points and by half in the bulk of the ceramic. Accordingly, a stacked substrate structure was also employed for the top substrate. Figure 3-18 shows the final designs for the top substrates with via, capacitor, and post locations shown.

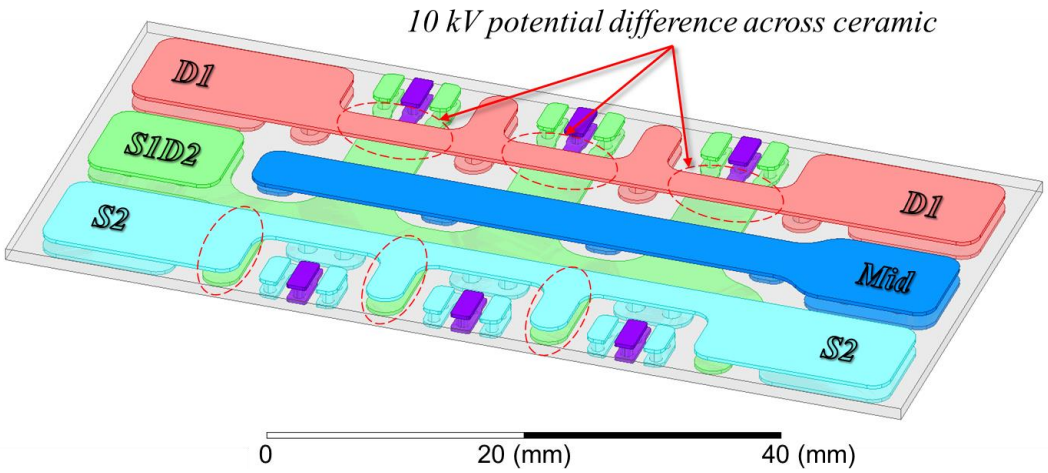



**Figure 3-16: Example single-substrate design for the top substrate. The areas with the highest electric field are highlighted.**

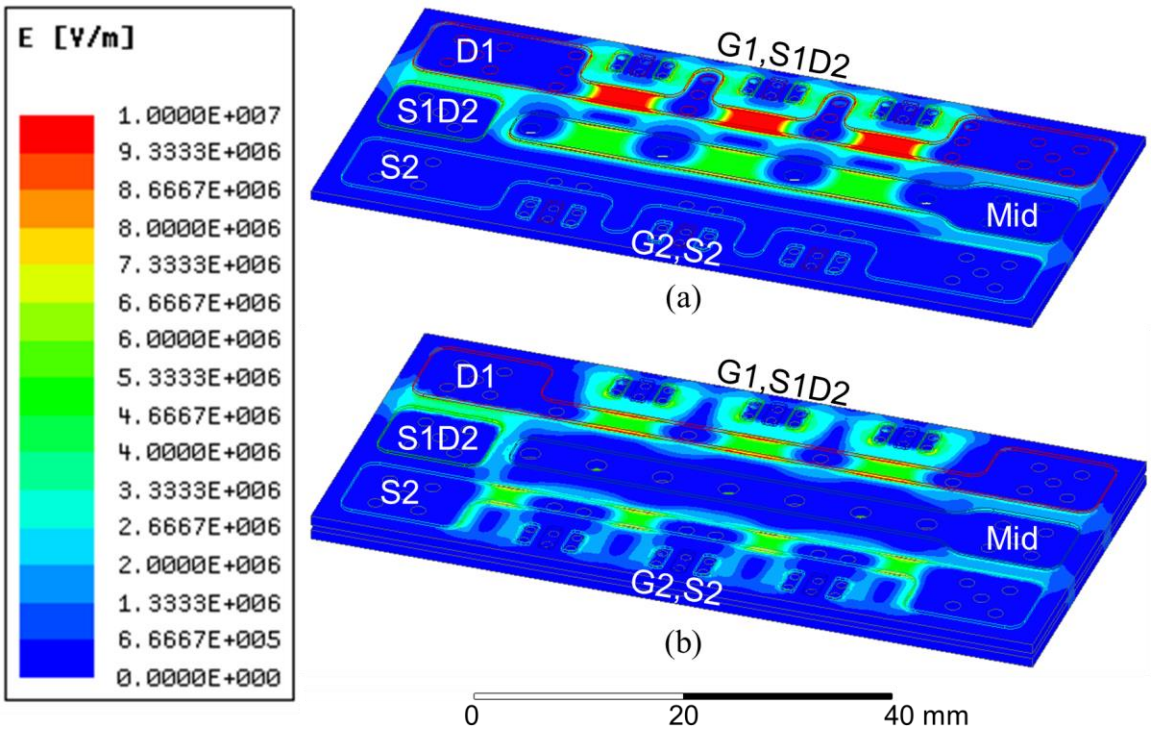



**Figure 3-17: Simulated 3D electric field distributions for (a) single and (b) two stacked substrates.**

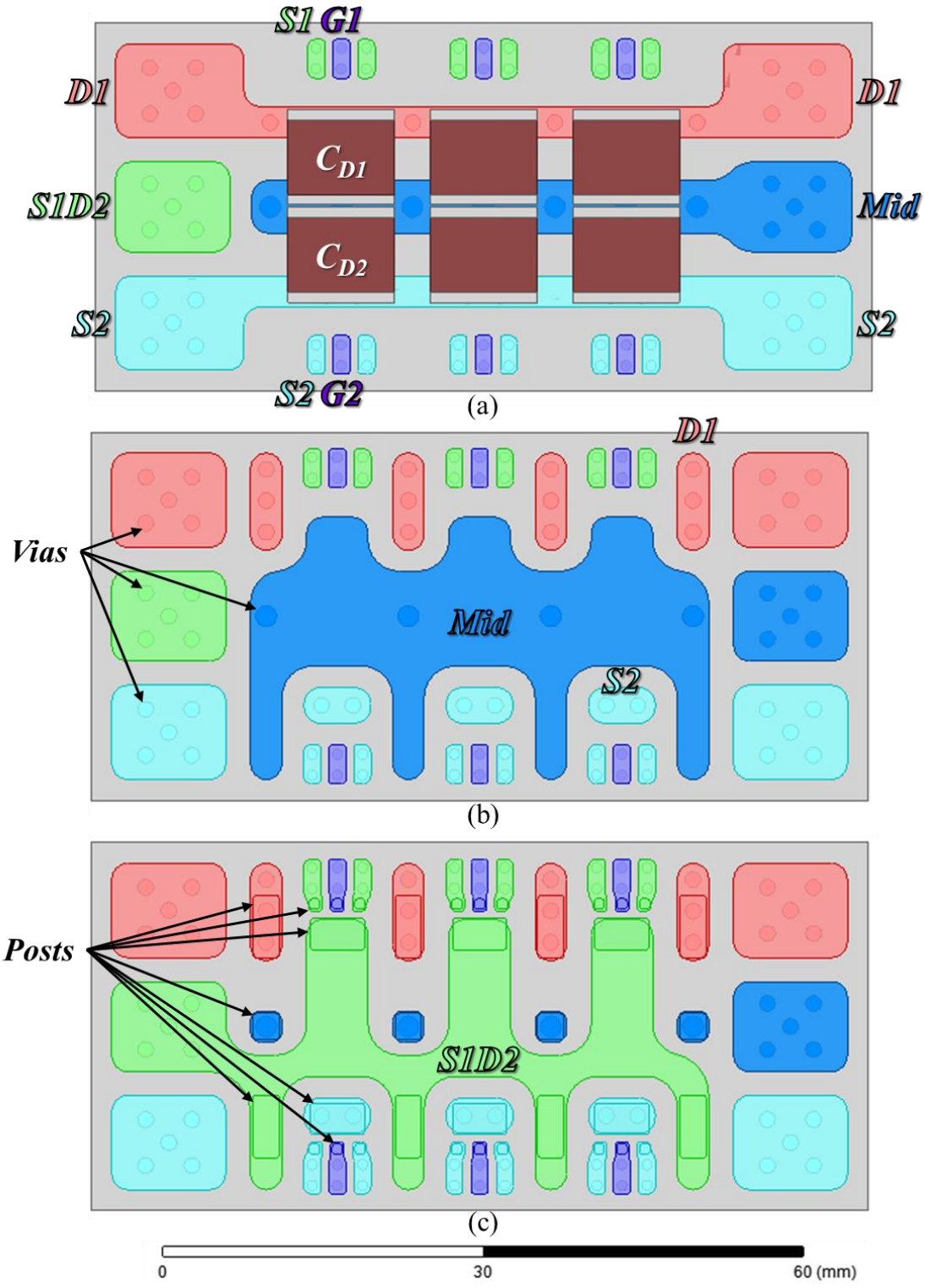



**Figure 3-18: Final design of the top substrate stack (a) top view with capacitor locations, (b) view of middle metal pattern, and (c) bottom view with post locations.**

### *3.4.4 Substrate Material Selection and Final Design Discussion*

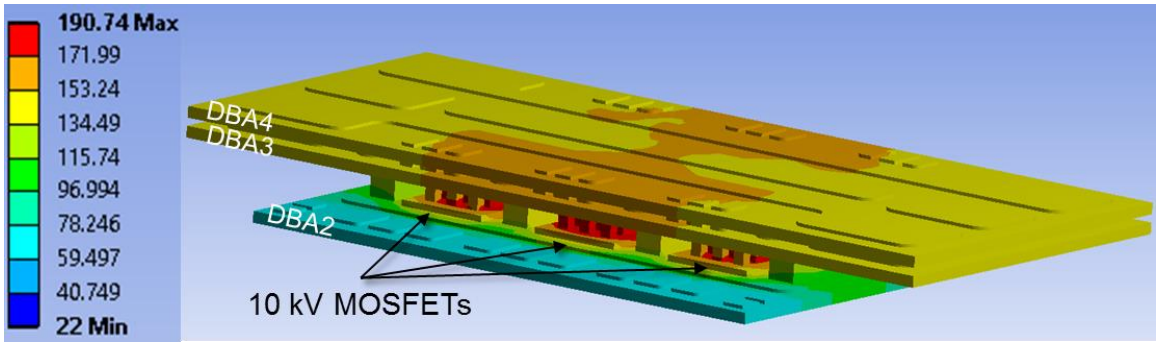
There are several factors to consider when selecting the substrate material. The ceramic should have good thermal conductivity to allow the heat from the semiconductor to be dissipated. Since the ceramic is meant to provide electrical isolation, a high dielectric strength is also important. A high flexure strength and fracture toughness are preferable such that the substrate can be thin (and thus have lower thermal resistance $R_{th}$), but not break from the mechanical stress. Finally, the CTE of the substrate should be close to that of the bonded components in order to minimize the mechanical stress on the SiC devices and thus improve the reliability. Cost is also an important factor when selecting a substrate material; however, due to the high cost of the 10 kV SiC MOSFETs, the price of the substrate is a small fraction of the overall cost for this power module. Commercial availability was also considered during the selection process.

In this work, both DBA and DBC substrates with 1-mm-thick AlN and 0.3-mm-thick metal were evaluated. Although less common, DBA has higher thermal-cycling capability than DBC [146]. AlN was chosen due to its high thermal conductivity, good mechanical stability, low CTE (lower than that of $Al_2O_3$) [147], and because it is commonly available in 1-mm thickness, which provides the needed high-voltage isolation. As mentioned previously, the module terminations are made from the top side of the topmost substrate. To achieve this connection with low inductance and high density, vias are used.

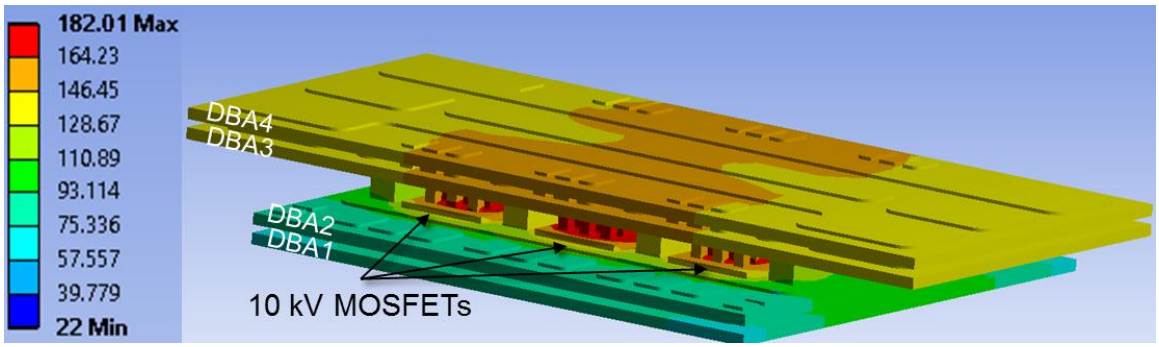
Creating the vias requires special processing; hence, this feature is only offered by a few substrate manufacturers, the capabilities of which placed some constraints on the final design. The DBA substrates with vias that were used in this work were supplied by DOWA. The via constraints from DOWA included a minimum via diameter of 1 mm, and

minimum spacing to the edge of the metal pattern of 0.3 mm. These limitations were due to the via fabrication process. The vias are filled with pure Al, resulting in good electrical conductivity, and had low concavity in the metal pad above and below the vias. The DBCs with vias were supplied by Remtec. Remtec's via limitations were quite different; the maximum via size was 1 mm, and the vias had to be at least 1.5-times the diameter apart. The same design was used for both the DOWA and Remtec substrates.

A major concern in stacking two substrates below the MOSFET dies is the impact on the thermal performance. ANSYS Workbench steady-state thermal simulations were used to evaluate this impact. Figure 3-19 shows the temperature distribution for the designed power module when there is a single, 1-mm AlN-DBA substrate on the bottom, and when there are two, 1-mm AlN-DBAs stacked together. Stacking the DBAs reduces the peak junction temperature by 9 °C for a heat transfer coefficient of 7000 $W/m^2K$ (applied to the bottom-most surface only), a power loss of 200 W per MOSFET, and a conservative thermal conductivity of 100 W/m·K for the sintered Ag joints, which are 100 µm thick between the stacked DBAs, and 50 µm thick for the die and Mo attach layers. The reduction in the peak junction temperature can be attributed to the lateral heat spreading. Although the vertical thermal resistance is increased due to the addition of the second ceramic, the thicker substrate also increases the heat spreading. Other embodiments of the design presented in Figure 3-3 can be developed to incorporate topside cooling. However, this may complicate the termination and system interfacing designs, as well as the decoupling capacitor placement, and thus was not evaluated in this work.




(a)




(b)

**Figure 3-19: Simulated temperatures (in degrees Celsius) for modules with (a) a single substrate and (b) two stacked substrates with a heat transfer coefficient of 7000 W/m$^2$K, and a power loss of 200 W per MOSFET.**

As mentioned earlier, the parasitic capacitance between the SiC dies and the cooling system is a path for CM current under high-*dv/dt* switching. Specifically, the parasitic capacitance between the S1D2 and the bottom metal layer (connected to the cooling system) are of interest since the S1D2 node experiences high *dv/dt*, as the high-side and low-side switches in the half-bridge alternately conduct. By stacking two substrates, this capacitance is reduced by 22 % since there are now effectively two parasitic capacitors in series (Figure 3-3a and Figure 3-3d). For a single substrate, the parasitic capacitance between the S1D2 trace and the bottom metal layer is 46 pF ($C_{P1}$). When two DBAs are stacked together, the effective capacitance becomes 36 pF due to the series connection of

a 160-pF parasitic capacitor across the second DBA substrate ($C_{P2}$). These values, which were simulated using ANSYS Q3D Extractor, are in good agreement with the calculated capacitances. With this proposed design, the parasitic capacitance to the cooling system is more than sixteen times lower than that for the module evaluated in [104], and nearly six times lower than Wolfspeed's first- and third-generation 10 kV SiC power modules. However, these modules have a greater number of dies in parallel. Wolfspeed's third-generation module has 18 dies per switch position, which is six times greater than the power module proposed in this work. Accordingly, if the measured parasitic capacitance for the third-generation module is divided by six, then the difference reduces to 17.6 %.

It can be seen from Figure 3-3d that there are vias in the top and bottom substrate stacks that connect the middle metal layer to the midpoint of the embedded decoupling capacitors. This is also shown schematically in Figure 3-3a. This connection allows the middle metal layer to be at half of the dc bus voltage. As shown in the previous section, this will reduce the electric field strength at the triple points by 40 %. Additionally, when the middle metal layer in the DBA stack is connected to the dc bus midpoint, then part of the CM current that flows through $C_{P1}$ will be diverted back to the dc bus (i.e., the midpoint of the two series decoupling capacitors) rather than going through $C_{P2}$ to the cooling system. This will reduce the amount of CM current that flows through the system ground. The amount of CM current that is diverted will depend on the high-frequency impedance of the connection path between the middle metal layer and the dc bus. This screen will be further analyzed and evaluated in Chapter 5.

## *3.5 Semiconductor Die Arrangement*

Asymmetrical parasitic elements among paralleled die can result in significant current imbalance [36],[74]. Specifically, during the switching transients, more current will flow to the dies with the lower-impedance paths. Those dies will have higher losses, leading to greater junction temperatures than the others [74]. As a result, these die are likely to fail before their predicted lifetime, which reduces the overall module reliability. To address this issue, care was taken to ensure that the gate- and power-loop inductances are symmetrical for each of the paralleled dies.

For the gate loop, this is achieved by having individual gate and source connections for each die. This requires that the gate driver connects to each MOSFET. The gate driver component placement and PCB traces can be adjusted to achieve symmetrical impedances for optimal balancing. It should be noted that this module design employs a Kelvin connection, which separates the power source from the gate source. This decoupling prevents the negative feedback between the two loops, thereby increasing the switching speed [148]. According to ANSYS Q3D Extractor, the gate-loop inductance for each MOSFET die is 1.6 nH without the terminals.

For the power loop, embedded decoupling capacitors are used to help balance the parasitic elements within the proposed module, as well as to minimize the impact of the bus bar stray inductances on the device switching (i.e., the voltage overshoot and ringing). Each high-side and low-side MOSFET pair (i.e., phase leg) has its own set of decoupling capacitors placed directly above it (Figure 3-3c). This gives symmetrical, low-impedance paths for each of the paralleled MOSFET pairs. Further, the vertical power loop (awarded by the planar, sandwich structure) is perpendicular to the gate loop, thus minimizing the

coupling between them. With the decoupling capacitors, the parasitic power-loop inductance decreases from 10.3 nH (including the terminals) to 4.4 nH. This is more than eight times lower than the module reported in [104] and more than three times lower than Wolfspeed's third-generation module [108].

## *3.6 Interconnections*

The most common form of die interconnection in commercial power modules is wire bonding. Wire bonds are available in Al, Cu, aluminum clad copper, and gold (Au), among others, and come in a variety of gauges. In fact, wire bonding is so prevalent that most power semiconductor devices have an Al topside metal layer so they can be compatible with wire bonding. The popularity of wire bonds can be attributed to its low cost and relatively good manufacturability/ease of implementation since it is fast and does not require any additional heating steps. However, the reliability of wire bonds is notoriously low due to thermomechanical stresses that can lead to heal cracking or lift off [77]. When this occurs, the current capacity of the module reduces since now there are fewer wire bonds to conduct the current.

As mentioned previously, wire bonds are not suitable for high-speed switching devices, such as WBG semiconductors, because of their high parasitic inductance. Wire bonds also increase the footprint of the power module, thereby reducing the power density and increasing the parasitic capacitances to the cooling system ground. Furthermore, wire bonds have a fuse current, which, once exceeded, will melt the wire and lead to an open circuit failure mode. This is undesirable for many high power applications. Accordingly, sandwich structures with dry, pressure-contact interconnections that remain intact (i.e.,

conduct current) under greater current and energy levels in the event of a fault, such as the press-pack and StakPak$^{TM}$ modules, are desirable. However, as mentioned previously, press-pack and StakPak$^{TM}$ modules require complex and bulky clamping systems, and have high stray inductances, which are not suitable for high-density, high-speed modules.

Other wire-bond-less, sandwich structures with alternative interconnect technologies have also been proposed in literature. In [61], solid Cu posts were used as the interconnect between the dies and the top insulating ceramic substrate. In [62], Mo posts laminated with Cu were used. The benefit of using the Cu-Mo-Cu laminate is the lower CTE, which reduces the thermomechanical induced stresses on the semiconductor compared to solid Cu posts, resulting in a three-times increase in the number of thermal cycles [142]. In [149], aluminum graphite contacts were used, resulting in lower junction temperatures for the devices; though, finite element simulations revealed higher stresses on the diodes compared to Mo.

Further works have evaluated flip-chip technology with solder bumps [150],[151], Cu microposts [152], beryllium-copper (BeCu) pressure contacts [153], Cu cylinders [154], and compressed Ag tubes [155]. While these technologies offer several advantages, such as reduced inductance, increased power density, and improved reliability, they may be difficult to fabricate with the aspect ratio needed for the 10 kV SiC MOSFETs. To package these devices, the interconnect must have a small footprint to be able to fit on the tiny pads of the SiC MOSFET dies, while being tall enough to provide the 10 kV isolation between the dies and the substrate. Accordingly, in this work, solid Mo posts were selected due to their high aspect ratio, as well as their simple manufacturability, attachment, and low inductance, resistance, and CTE.

The optimal post height is a tradeoff between the electromagnetic and electrostatic performances; a shorter post height will reduce the parasitic inductances and resistances, but will increase the electric field strength between the edge termination of the 10 kV MOSFET dies and the source potential on the top substrate (i.e., the bottom metal of DBA3). This latter feature was explored in [141]. To determine the optimal height of the posts in this work, 2D electrostatic simulations were performed using ANSYS Maxwell. Figure 3-20 shows the electric field distribution in the module cross-section with post heights of 1 mm and 2 mm. In this simulation, the voltage distribution was graded along the top surface of the 10 kV SiC MOSFET in order to mimic the guard rings of the MOSFET die, as was done in [141]. It can be seen from Figure 3-20 that the electric field strength between the top of the die and the bottom metal of the top DBA reduces when the post height is increased. If the electric field between the die and the top DBA exceeds the breakdown field strength of the encapsulation material, then PD and even arcing could occur, resulting in a short circuit between the drain and source terminals of the SiC MOSFET. A post height of 2 mm was selected for this 10 kV SiC MOSFET module because of the lower electric field strength.

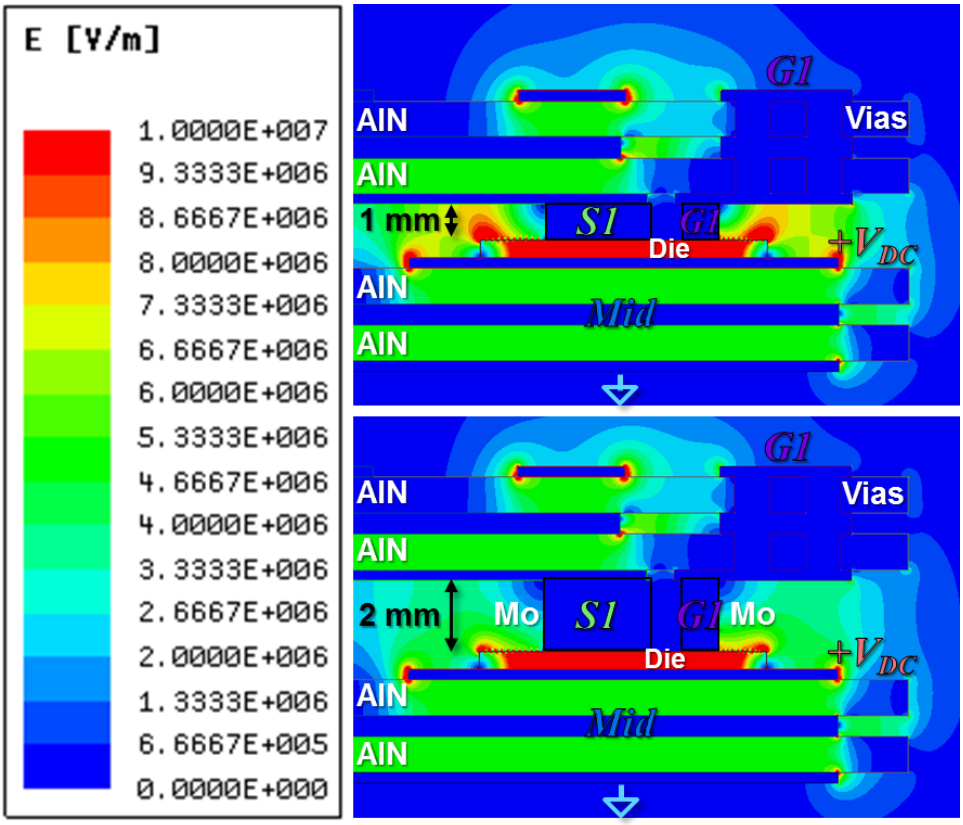



**Figure 3-20: Simulated electric field distributions for 1-mm post height (top) and 2-mm post height (bottom).**

The areas of the posts that are to be attached to the MOSFET die surface were determined by the metallization pattern on the die (Figure 3-21). 1.0 mm × 1.0 mm posts were used for the Kelvin source connections. A post was placed on either side of the gate for symmetry. The power source post is made as large as possible, while still staying within the bounds of the existing die metallization and providing sufficient spacing from the gate to minimize the likelihood of a gate-source short during post attachment. The original gate pad of the die is 0.8 mm × 0.8 mm and is only 0.16 mm from the neighboring source pads. Two options were pursued for the gate post attachment. In one, a special die metallization process was used to enlarge the gate pad and isolate it from the neighboring source pads.

With this metallization process, a 1.0 mm × 1.0 mm gate post could be used. In the other approach, the original gate metallization pattern is kept, and a post size of 0.7 mm × 0.7 mm is used. This option requires high accuracy during the post attachment process, due to the small margin.

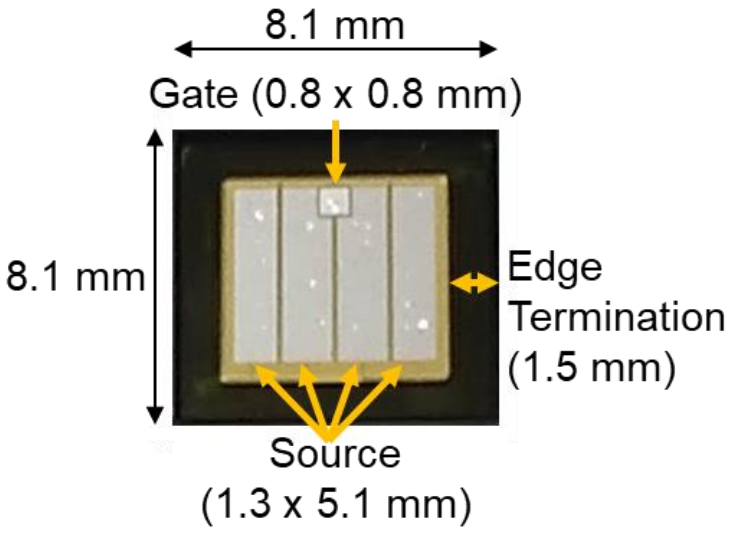
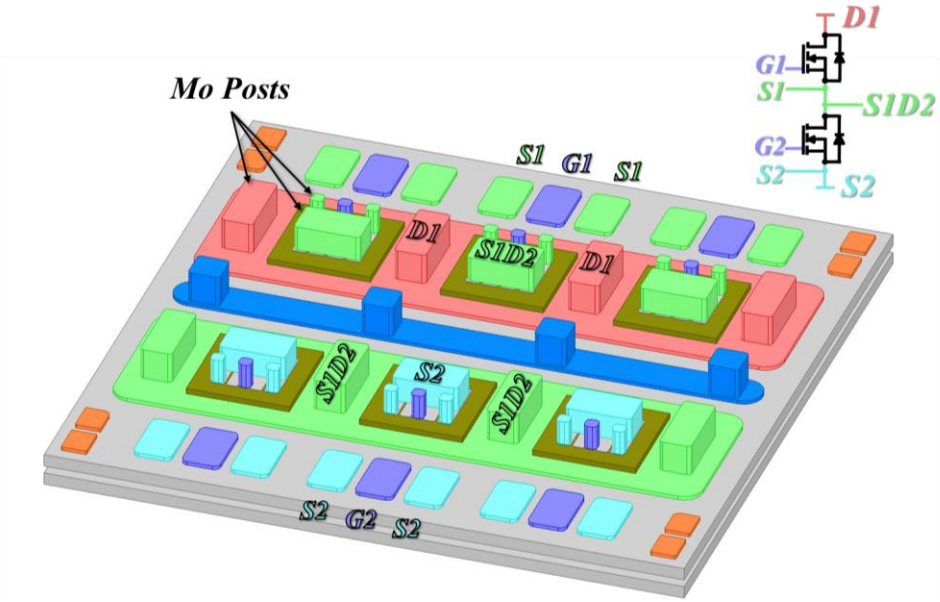



**Figure 3-21: Top view of 10 kV SiC MOSFET die (note that the drain contact is the bottom surface).**

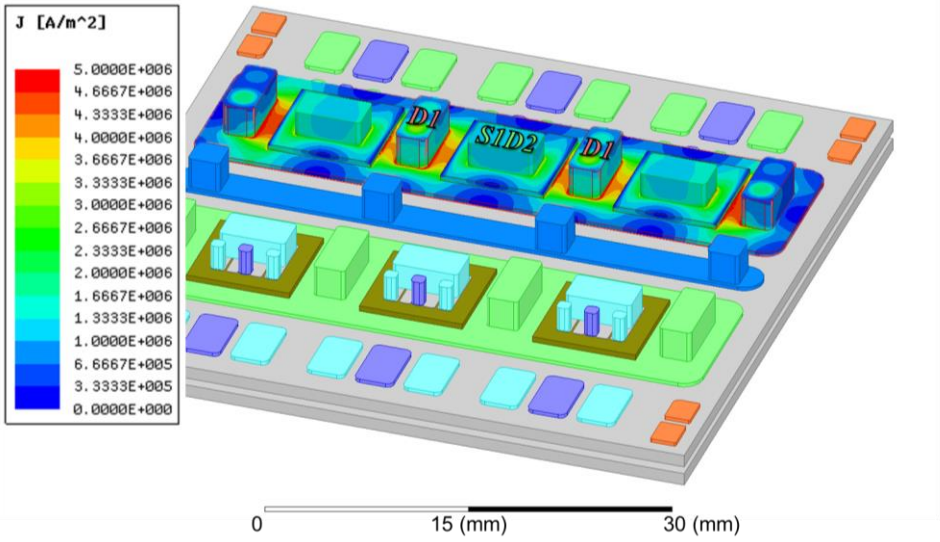
For the posts directly connecting the upper and lower substrate stacks, the sizes, quantities, and locations were determined based on several factors. The areas and quantities should be large enough to have good mechanical stability, bonding strength, low parasitic inductance and resistance, and high current handling capability, yet small enough to still allow for high power density. The locations of these posts are also critical. It was determined to have several posts distributed around the dies for symmetrical parasitics, uniform current distribution, and uniform pressure distribution to the thermal management system. As can be seen from Figure 3-22a, the arrangement is symmetrical.

The current density distribution was simulated using ANSYS Maxwell, and is shown in Figure 3-22b. As can be seen from the figure, the current is uniformly distributed

to all of the parallel dies. The distributed posts also provide more options for the housing-to-cooling-system connection. For instance, the housing could be designed such that the mounting force is distributed to the posts. In this way, all of the dies will be in better contact with the cooling system compared to a traditional power module, where the force is typically applied to the outer corners of the module. As a result, in a traditional module, the dies in the center may have higher thermal resistance than those at the corners. Further discussion on the housing and thermal management designs will be provided in a later section.




(a)




(b)

**Figure 3-22: 3D model of the (a) post arrangement, and (b) simulated current density distribution.**

The final post dimensions and the quantity of each needed per module are listed in Table 3-1. Since the SiC MOSFET dies are approximately 0.5-mm thick, the posts that are bonded to the dies are 0.5 mm shorter than those that are attached directly onto the substrates.

**Table 3-1: Post Dimensions**

| Node(s) (locations) | Dimension (mm) | Pieces per Module | Image (to scale) | Corner Radius (mm) |
|---|---|---|---|---|
| D1 and S1D2 (substrate–substrate) | 6.0 × 2.5 × 2.5 | 8 |  | 0.3 |
| Mid (substrate–substrate) | 2.5 × 2.5 × 2.5 | 4 |  | |
| S1D2 and S2 (MOSFET–substrate) | 5.2 × 3.0 × 2.0 | 6 |  | |
| S1D2 and S2 (MOSFET–substrate) | 1.0 × 1.0 × 2.0 | 12 |  | |
| G1 and G2 (MOSFET–substrate) | 0.7 × 0.7 × 2.0 | 6 |  | |
| | Total | 36 | | |

## *3.7 Embedded Decoupling Capacitors*

In [104], the parasitic impedances for a package intended for 10 kV SiC MOSFETs were extracted and put into a circuit simulator with a 2 kV SiC MOSFET die model. The results showed notable ringing in the switching waveforms due to the module parasitic impedances [104]. Even more troublesome was the current imbalance during the switching transients [104]. Due to the asymmetrical parasitic inductances among each of the paralleled dies, the maximum difference in the current overshoot was 150 % [104]. This severe imbalance will cause the die with the greater overshoot to have larger switching losses [74],[75], and thus a higher junction temperature [75], ultimately reducing the lifetime of the module. As a result, users often slow down or de-rate the devices, thereby diminishing the advantages of using SiC over silicon.

A major cause for the imbalance simulated in [104] could be due to the asymmetrical terminal and die arrangement. The D1 and S2 power terminals were on one

end of the power module and the dies were distributed side-by-side from one end of the module to the other. As a result, the dies on the opposite end of the power module (i.e., the farthest from the power terminals) have larger power loop inductance than the dies that are located closest to the power terminals. A rough model of Wolfspeed's first-generation 10 kV SiC module was created to estimate this imbalance. With this model, the power loop inductance was estimated to be around 37 nH for the dies located closest to the power terminals and 70 nH for the dies located the farthest from the terminals. This is nearly a two times difference. As it is not always practical for the system designers to use a power module with multiple distributed power terminals, such as Wolfspeed's third-generation module [108], it is proposed to use embedded decoupling capacitors to improve the dynamic balance among the paralleled dies.

As can be seen from Figure 3-3c, the proposed power module design allows room to accommodate embedded decoupling capacitors. Each MOSFET switch pair has its own set of decoupling capacitors placed above it, providing a low-impedance, high-frequency loop, which compensates for the different distances to the module terminals. This type of vertical capacitor loop was reported in [67], which allowed for a very low parasitic loop inductance of less than 1 nH, for the packaging of 1.2 kV SiC JFETs. However, [67] did not report on the utilization of these capacitors for improving the current balance among paralleled dies. This is a key advantage of this structure, especially for high-current modules with multiple dies in parallel.

This concept of embedding a decoupling capacitor for each die switch pair was reported in [70],[72],[156]. However, since the modules in [70],[72],[156] use wire bonds for the interconnection, the capacitors must be placed beside the dies, thereby increasing

the footprint of the module. The vertical capacitor loop, on the other hand, does not increase the module footprint.

There are few commercially-available medium-voltage capacitors that are suitable for embedding inside a high-density power module. A capacitor with 5 kV rating was selected, and thus two are connected in series. This means, unlike in [67],[70],[72],[156], the dc bus midpoint is accessible within the module. This provides a low-impedance connection for the middle metal layer in the bottom substrate stack to the dc bus midpoint (i.e., half of the dc bus voltage). As was shown previously, connecting the middle metal layer reduces the electric field strength at the triple points by 40 %. Additionally, this connection acts as a screen, diverting some of the generated CM current back to the dc bus and, in this case, also containing it within the power module. The details of this screen will be discussed in Chapter 5.

With this in mind, a surface-mount, 680 pF, C0G, 5 kV multilayer ceramic capacitor (MLCC) from AVX Corporation was selected. This is the highest capacitance value that could be found for the C0G material with 5 kV voltage rating in a small, surface-mount package that is commercially-available and in-stock. C0G was selected because its capacitance is stable with temperature and voltage [157],[158]. While X7R capacitors appear to have higher capacitance, the capacitance can decrease by 50 % or more when operated close to the rated voltage and temperature [157],[158] to the point where it becomes comparable to the capacitance of the C0G capacitors. The capacitor package is 3640 (9110 metric), with dimensions of 9.14 mm × 10.20 mms × 2.54 mm. These dimensions are important as they determine the topside pattern of the topmost DBA substrate (DBA4). The placement of the capacitors can be seen in Figure 3-3c. The

capacitance tolerance was ±5 %. This tolerance is significant because it will determine the voltage balance between the two capacitors in series. Additionally, balancing resistors can be added into the power module to further improve the voltage sharing. 10 MΩ resistors with ±5 % tolerance and 1.5 W rating in a 4020 package were selected (HVC4020V1005JETCT).

## *3.8 Module Termination Design*

To date, little work has been done to analyze the electric field at the module-system interface. Preliminary analysis of the electric fields for the module bus bar was reported in [91]. The work presented in this dissertation will be the first to implement and test advanced electric field reduction methods both internal and external to the package of a 10 kV SiC MOSFET power module.

A major challenge associated with the high-density design is the module termination. Specifically, the interfacing of the module with the rest of the medium-voltage system is not trivial since standards stipulate minimum creepage and clearance distances. Creepage is the shortest distance between two conductors along the surface of a solid insulating material, while clearance is the shortest distance between two conductors in air. According to UL-840, the minimum clearance distance for electrical equipment rated at an impulse withstand voltage peak of 12 kV is 14 mm [109]. At 10 kV operating voltage, the minimum creepage distance is 100 mm for material group IIIa,b (e.g., FR4) and pollution degree 2 (normally non-conductive pollution with some temporary conductivity caused by condensation) [109]. Clearly, these standards make it difficult to achieve a high-density package for medium-voltage semiconductors due to the large distances needed for the

connection to the system. In this work, a custom design that avoids exposed conductors was developed. In this way, the minimum creepage and clearance distance requirements do not apply.

First, several terminal types were considered: 1) bus bar, 2) pins, and 3) springs. These designs were evaluated based on the tradeoffs between electric field concentration, current capacity, parasitic inductance, ease of assembly, interface method, and reliability. Bus bars are common in high-power modules due to their high current capacity and lamination option, which offers lower inductance. However, the sharp edges result in high electric field concentration, and, to improve the mechanical stability, they are typically large in size. Moreover, they must be custom-designed for each power module layout.

Pin and spring connectors, on the other hand, have a rounded geometry, resulting in lower electric field concentration. However, pins, like bus bars, are through-hole connections and are typically secured using screws, solder, or press-fit sockets. This is undesirable for this work because, in order to avoid the minimum creepage and clearance distance requirements, the conductors must be insulated. This could be done by potting or encapsulating the exposed conductors after connecting the module to the system. However, this could make the disassembly difficult and impractical.

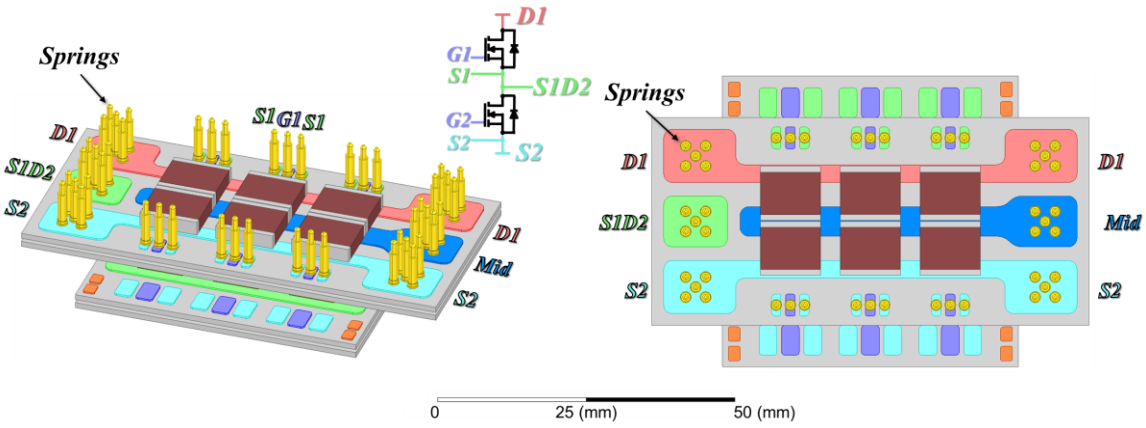
In terms of mechanical reliability and ease of connecting and disconnecting the module, spring connectors are preferred compared to rigid bus bars and pins. Multiple springs can also be placed in parallel to reduce the parasitic inductance and increase the current capacity. Commercially-available springs can be used and arranged as needed throughout the module to maintain impedance symmetry for the paralleled dies and create

a more even pressure distribution throughout the module, providing uniform contact to the cooling system. For these reasons, springs were chosen for the module terminals.

The springs selected for this module each have a continuous current rating of 10 A, and have a small, surface-mount footprint diameter of 1.88 mm (CG-2.5-6-SM) [159]. The arrangement of the spring terminals is shown in Figure 3-3e and Figure 3-23. According to ANSYS Q3D Extractor simulations, the gate-loop inductance for each MOSFET die is 3.8 nH with the spring terminals. This is more than five times lower than the gate-loop inductance reported in [104], which models a package intended for 10 kV SiC MOSFETs. For the power loop, the total parasitic inductance is still 4.4 nH with the spring terminals due to the embedded decoupling capacitors. This is more than ten times lower than the power-loop inductance reported in [104], and more than three times lower than that reported in [108]. For the power loop, the total parasitic inductance is 10.3 nH with the spring terminals (without capacitors). This improved layout provides more symmetrical impedances for each of the paralleled dies compared to those in traditional modules, which, as shown in [104], can have more than 100 % difference in the peak current among the paralleled die during the switching transients. Table 3-2 lists the module parasitic inductances and capacitances, as well as the power density.

**Table 3-2: Module Parameters Simulated with ANSYS Q3D Extractor**

| Parameter | Value | Condition |
|---|---|---|
| Gate-loop inductance | 1.6 nH | Without spring terminals |
| | 3.8 nH | With spring terminals |
| Power-loop inductance | 10.3 nH | With terminals, without decoupling capacitors |
| | 4.4 nH | With terminals, with decoupling capacitors |
| S1D2-baseplate capacitance | 46 pF | Single substrate |
| S1D2-baseplate capacitance | 36 pF | Two stacked substrates |
| Power density | 13.0 W/mm$^3$ | With decoupling capacitors, without housing |
| | 3.8 W/mm$^3$ | With housing and integrated cooler |




(a) (b)

**Figure 3-23: (a) Angled view and (b) top view of the 10 kV module with the spring terminals.**

## *3.9 Encapsulation*

Once the dies and terminals are attached and interconnected, and the housing (to be discussed in the next section) is sealed, the module is ready to be encapsulated. Encapsulation is done to improve the dielectric strength, physically protect the components (e.g., SiC MOSFETs) from environmental conditions (e.g., humidity, contaminants, and mechanical damages), and increase the reliability. To do this, the encapsulant must have

high dielectric strength (typically greater than 10 kV/mm), low moisture and ion content (usually less than a few ppm), as well as low hardness and a CTE close to that of the other module components (e.g., semiconductor, wire bonds, and substrate). The low hardness will enable thermally-induced movements of the module components. If the encapsulant is hard and/or has a significantly different CTE compared to the module components, then thermal gradients that result from usual module operation can cause damage to the components and reduce the reliability. Ideally, encapsulants would also have high thermal conductivity to remove the heat from the semiconductor devices. However, the thermal conductivity of the common encapsulants that meet the previous requirements is typically low (less than 5 W/m·K) compared to that of the ceramic substrates, and thus often does not make a significant contribution to the heat removal.

It has been shown in [160] that encapsulants, such as silicone gel, drastically reduce electrochemical migration of the sintered Ag and solder joints. Without an encapsulant, dendrite growth was shown to rapidly form from sintered Ag and solder joints [160]. The growth was directly related to the applied voltage and time to failure [160]. Accordingly, encapsulation is critical to extending the lifetime of the power module, especially for medium-voltage applications.

There are generally two categories of encapsulants: 1) those with glass transition temperatures greater than the highest working temperature, and 2) those with glass transition temperature lower than the highest working temperature [161]. The former are harder materials, such as polyimide and benzocyclobutene, while the latter are softer materials, such as silicone gel [161]. The processability (flowability and curability), temperature dependence of the dielectric properties (dielectric strength and permittivity),

and the thermal aging of commercially-available encapsulants was explored in [161]. Since the application was for a high-temperature power module, polymers with glass transition temperatures greater than 250 °C and silicone-based soft materials with glass transition temperatures of -100 °C or lower were evaluated [161]. It was found in [161] that the materials belonging to the first category had poor processability compared to those in the second category. This poor processability significantly reduced the dielectric strength of the test samples in [161].

The materials belonging to the first category, on the other hand, had good processability. Although, it was also found that the relative permittivity and dielectric strength of the silicone elastomers decreased with temperature (40–53 % and 30–42 %, respectively, from 25 °C to 250 °C) [161]. The thermal aging at 250 °C was shown to have little impact on the relative permittivity of the silicone elastomers [161]. However, the thermal aging caused a drastic (61–78 %) decrease in the dielectric strength [161]. Specifically, after thermal aging, the dielectric strength of the best-performing silicone elastomer was 13 kV/mm [161]. This degradation needs to be taken into consideration when designing a medium-voltage power module.

Other works have also investigated the usage of dielectric fluids [83] and gases [162],[163],[164] as encapsulants. For these materials, the power module package must be hermetically sealed, which could increase the fabrication and design complexity. In [164], it was found that using $C_4F_8$ instead of air can double the PDIV. Using nitrogen, on the other hand, reduced the PDIV by 12 % compared to air [164]. The PDIV of a module in the nitrogen- and $C_4F_8$-filled chambers decreased with temperature by 25 % and 19 %,

respectively [164]. It was found in [164] that increasing the pressure of the $C_4F_8$ in the chamber further increased the PDIV of the module; increasing the pressure from 0.1 MPa to 0.15 MPa increased the PDIV by 20 % at all tested temperatures. Further increasing the pressure to 0.2 MPa further increased the PDIV by approximately 34 % at room temperature [164]. No comparison to a gel-filled sample was provided in [162],[163],[164].

When it comes to higher voltage applications, a disadvantage of gels is their limited self-healing capability; repetitive PD events could eventually result in serious degradation of the gel [165],[166]. Although, the self-healing of gels is better than for solids, it is still not suitable for repetitive PD [165],[166]. Liquids, on the other hand, are able to recover from PD events [165],[166]. This could be due to "PD regimes" that form in the gel [165],[166]. These regimes could be due to the 1000-times longer lifetime of the cavities that are formed by PD events (streamers) in gels compared to those formed in non-viscous liquids [165],[166]. The longer lifetime can result in a self-sustained gaseous cavity (i.e., "PD regime"), thereby reducing the PD performance [165],[166].

The material properties of encapsulants and coating materials can be used to reduce the electric field strength at the critical triple points. Several solutions have been proposed in the literature. These solutions include increasing the permittivity of the encapsulant [83],[167], applying a dielectric with high permittivity [84] or high breakdown field strength [85] on top of the metal-ceramic intersection before encapsulation, applying a resistive coating along the ceramic surface [86],[85], and adding fillers to create an encapsulant with nonlinear resistivity [88] or nonlinear permittivity [87]. The advantages and disadvantages of these methods will be discussed in detail in this section.

In [83], the influence of adjusting the permittivity of the encapsulation on the PD performance was explored. The relative permittivities of AlN and $Al_2O_3$ are 9.0 and 9.8, respectively, while those of transformer oil and typical silicone gels are around 2.1 to 2.2 [83]. Accordingly, the electric field will be higher in the encapsulation since it has a lower permittivity than the ceramic [83]. When the electric field strength in the encapsulant exceeds its dielectric strength, PD will occur. Simulations and PD tests in [83] confirmed that the higher electric field shifts more and more into the ceramic as the permittivity of the encapsulant is increased. Samples encapsulated with Novec 649 and Novec 7100, which have a permittivity of 1.8 and 7.4, respectively, were tested [83]. It was found the samples encapsulated with Novec 7100, which has a four times greater permittivity than the Novec 649, only had a 22 % higher PDIV [83]. Moreover, the Novec 7100 is a fluid, which means the package must be hermetically sealed, and it will not provide mechanical support to components within the power module.

Figure 3-24 shows 2D electrostatic simulations of the bottom substrate stack for the designed power module when the permittivity of the encapsulant is varied from 1 to 30. As can be seen from the figure, there is negligible reduction in the electric field strength at the triple points when the module is encapsulated in silicone gel, which typically has a permittivity around 2.7, compared to air, which has a permittivity of 1. Silicon dioxide, which has a permittivity around 3.5, also does not noticeably reduce the electric field strength. The electric field reduction at the triple points finally becomes obvious when the permittivity reaches 15. At a permittivity of 30, the effect became more significant.

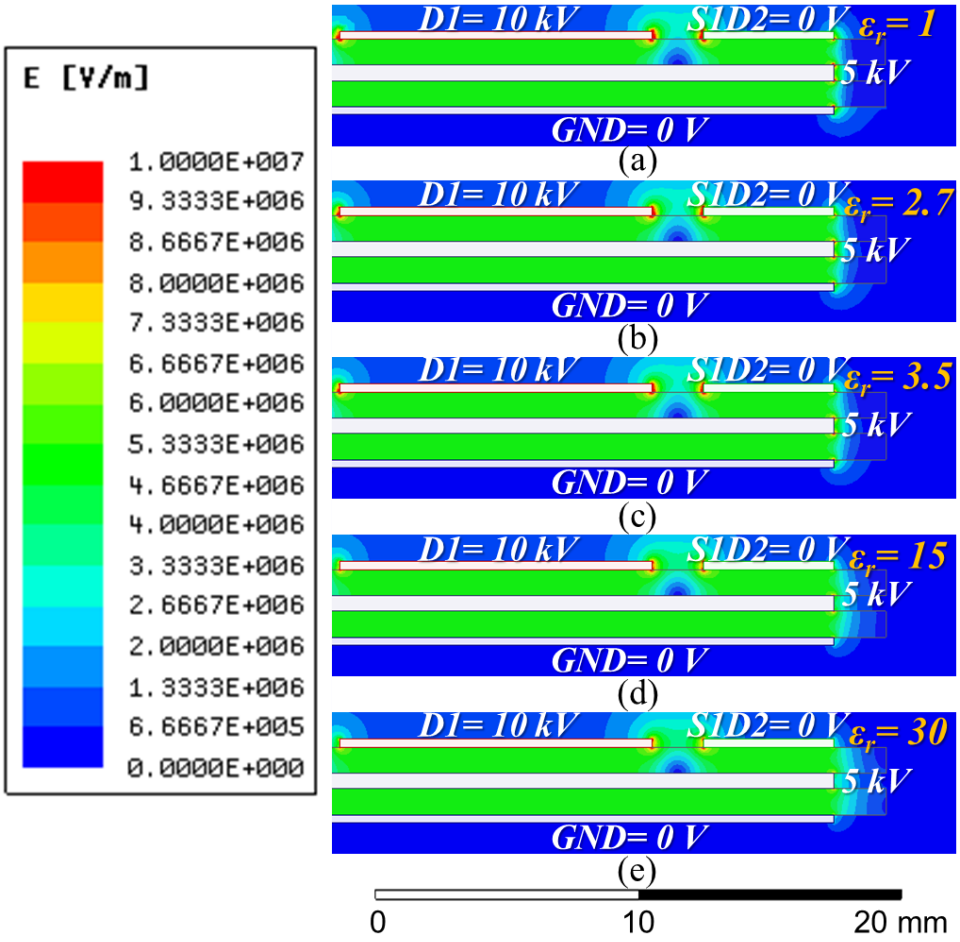



**Figure 3-24: Electric field distribution for encapsulant permittivies of (a) 1, (b) 2.7 (silicone gel), (c) 3.5 ($SiO_2$), (d) 15, and (e) 30.**

Although there are currently no suitable, commercially-available encapsulants with a permittivity of 15 or greater, there has been research on developing such materials. In [167], for instance, the addition of barium titanate ($BaTiO_3$) and strontium titanate ($SrTiO_3$) micro-fillers to epoxy resin was found to increase the permittivity as much as 8.7 times; 45 % $BaTiO_3$ by volume increased the relative permittivity from 4 (for unfilled epoxy resin) to 34.9. However, the addition of the $BiTiO_3$ reduced the breakdown strength by 66 % (from 44.1 kV/mm for the unfilled epoxy to 15.2 kV/mm for the 45 % $BaTiO_3$ by volume epoxy) [167]. Accordingly, there is a tradeoff between the increase in the permittivity,

which reduces the peak electric field, and the breakdown strength, which is the maximum electric field that the material can withstand without breaking down. In [167], electric field simulations found that the peak electric field is roughly 150 kV/mm near the triple point for an encapsulant with a permittivity of 30, and 110 kV/mm for a permittivity of 100. Accordingly, the 45 % $BaTiO_3$ by volume encapsulant, which has a permittivity of 34.9, alone would not be suitable as it cannot reduce the peak electric field at the triple point to below its breakdown strength of 15.2 kV/mm. However, this material could potentially be combined with other solutions to improve the PD and breakdown performance.

In [87], 15 % by volume $BaTiO_3$ was added to silicone gel, which increased the permittivity 1.6 times and reduced the simulated electric field strength by 10 %. However, $BaTiO_3$, which is ferroelectric, experiences enhanced polarization mechanisms at high electric field strengths [87]. This results in the permittivity of the filled gel being field-dependent; the permittivity increases as the electric field strength increases [87]. When this effect is taken into account in the simulation, the peak electric field reduces by 29 % [87]. PD tests showed an increase in the PDIV by 60 % [87]. Additionally, the fillers increase the thermal conductivity of the gel by 37 % (from 0.161 W/m·K to 0.22 W/m·K), which could help to reduce hot spots within the power module [87]. However, the density of the filled gel is 77 % higher than the unfilled, which could result in a total weight increase of the power module by 11 % [87]. Additionally, the fillers increased the viscosity of the gel by five times [87], which could result in trapped air bubbles and/or unfilled small gaps. The inclusion of the $BaTiO_3$ also increases the power loss by 18 times (279 W at 3 kV for the filled gel compared to 15 W for the unfilled) [87]. Moreover, the field-dependent permittivity only occurs under an alternating field; under a dc field, the only benefit of the

filled gel is the increased permittivity [87]. Also, it was not mentioned in [87] if the 15 % $BaTiO_3$ fillers will impact the breakdown strength.

In [84], it was proposed to apply a high-permittivity dielectric directly over the triple points (i.e., at the edges of the metal pads) prior to encapsulation. In [84], epoxide resin, which has a dielectric strength greater than 30 kV/mm and a permittivity of 4.4, was selected. The weight ratio of the epoxide resin determined the bevel and filling height. PD tests showed, compared to a reference sample, which was encapsulated in SilGel 612 (23 kV/mm dielectric strength and 2.7 permittivity), the sample with 40 % weight epoxide resin coating had a 42 % higher PDIV [84]. Of the three weight percentages tested (10 %, 40 %, and 80 %), the 40 % had the highest average PDIV of 13.5 kV [84]. However, it was also reported in [84] that the 40 % epoxide sample broke down at 13.5 kV as a result of high PD. This brings the PDIV determination criteria into question. Unfortunately, no further details on the PDIV criteria are provided in [84], so it is unclear how the average PDIV and breakdown voltage are both 13.5 kV. The 80 % weight epoxide resin coated sample had an average PDIV of 12 kV, and a large standard deviation [84]. This could be due to the high viscosity of the 80 % epoxide resin coating, which could cause wettening defects or uncoated areas [84].

Instead of using materials with high permittivity, those with low conductivity and moderate resistivity could be used. In [86], a 300-nm layer of doped hydrogenated amorphous silicon (a-Si:H), whose resistivity decreases with increasing voltage, was applied to the edge of the ceramic, creating a small current between the top and bottom metal pads. This current should be large enough to homogenize the electric field, yet small enough to satisfy insulation requirements. Of 27 test modules with the a-Si:H coating, 18

had PDIV exceeding 10 kV, 6 had PDIV up to 8 kV, and 3 failed [86]. So, 90 % of the test modules had a 100 % increase in PDIV compared to a sample without the coating [86]. However, when full modules were tested, only 8 of 13 modules had a PDIV greater than 5 kV; two modules had PDIV at 5 kV or less, and three experienced insulation failure [86]. It was reported in [86] that the resistivity of the coating significantly reduced during the module manufacturing process, though exact numbers were not provided. The risk of the resistivity decreasing to the point where it results in insulation failure is a serious issue that must be resolved before this method can be implemented in practice.

Similarly, in [88], zinc oxide (ZnO) microvaristors were added to polyimide to create a coating with field-dependent resistivity. The coating was applied to the triple points (i.e., at the metal edges) [88]. The simulations showed a reduction in the electric field by 97 % when a coating with a resistivity that decreases with increasing electric field is applied [88]. No PD tests were reported in [88]. A ratio of 0.3:1 of ZnO microvaristors to polyimide was selected [88]. The nonlinear resistivity of the material was determined by the sintering process [88]. The resulting material had a leakage current of 1 mA at 6.5 kV [88]. At 8.5 kV, the current increased to 20 mA, which is a power loss of 170 W [88]. Furthermore, when soldering the sample to a baseplate, it was mentioned that the resistivity and nonlinearity coefficient strongly reduced, though exact values were not provided in [88]. The authors claimed this degradation could be resolved by sealing the coating with a layer of polyimide, though this was not tested [88].

In [115], a silicone gel from Nusil was tested. The researchers looked at the leakage current at different temperatures (up to 250 °C) and gap widths (as small as 0.36 mm) [115]. The results showed the breakdown voltage at 200 °C notably reduced from more than 30

kV to about 21 kV when the gap width was reduced from 0.87 mm to 0.44 mm [115]. When the temperature was increased to 250 °C, the breakdown voltage at a gap width of 0.44 mm further reduced from 21 kV to 20 kV [115]. These results suggest the insulating characteristics of the gel are determined by the gap width and temperature. The PD performance of the gel was not evaluated in [115]. In this work, silicone gel is selected as the encapsulant because of its good processability, which as demonstrated in [161], is important for maintaining good dielectric strength. Several commercially-available gels were evaluated, and will be discussed in more detail in the following chapter.

## *3.10 Housing and Thermal Management System Design*

The housing is another important feature of the power module, especially for high-density, medium-voltage applications. The housing has a significant impact on the overall size, thermal resistance (and thus current capacity), and voltage rating. To safely and reliably utilize the module at the rated voltage, creepage and clearance requirements [109], and PD/breakdown standards, should be considered. At 10 kV operating voltage, the minimum creepage distance is 100 mm for material group IIIa,b (e.g. FR4) and pollution degree 2 (normally non-conductive pollution with some temporary conductivity caused by condensation) [109]. Clearly, it is not practical to have exposed connectors for a high-density module. No previous literature was found on the development or comprehensive investigation of high-density power module connectors for medium-voltage applications. Accordingly, a new connection scheme is proposed in this work.

First, to avoid the creepage and clearance distance requirements, a sealed connection is designed. The housing design and system interface scheme that was

developed for this 10 kV power module is shown in Figure 3-25. As can be seen from the figure, the external PCB bus bar is mounted on top of the power module. Pressure is applied to the top of the PCB through four mounting screws. This pressure compresses the springs until the bus bar contacts the protrusions in the housing lid. In this way, the springs are not exposed, and thus creepage and clearance distance requirements do not apply.

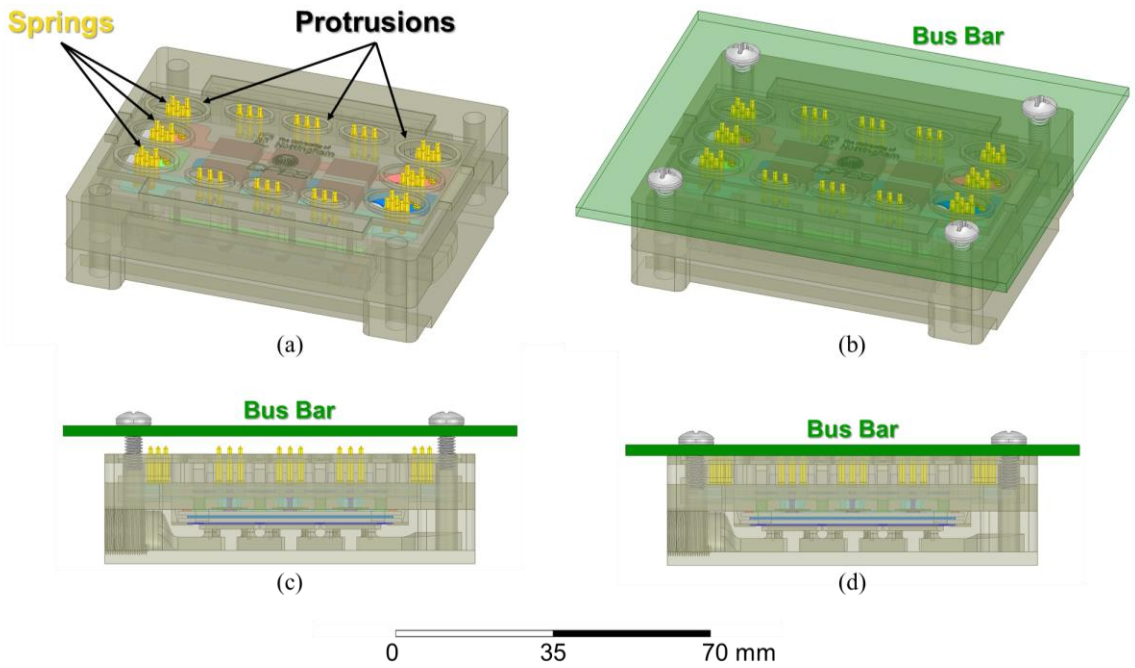



**Figure 3-25: 3D model of the (a) module with the housing and lid, (b) module with the bus bar, (c) side view of the module, and (d) side view of the module with the bus bar compressing the spring terminals.**

In addition to creepage and clearance requirements, attention must also be paid to the electric field strength in order to have sufficient PDIV and breakdown voltage. In particular, the electric field concentration in the air is critical due to the low breakdown field strength of air, which is just 3 kV/mm. For this reason, protrusions were added to the housing lid (Figure 3-25). Without these protrusions, small air gaps could exist between the PCB and the module lid; the smaller the air gap, the larger the electric field strength,

and thus the lower the PDIV. Accordingly, increasing the height of the protrusions will increase the PDIV. However, increasing the height of the protrusions will also increase the inductance and resistance. Given these considerations, a protrusion height of 1 mm was selected, though this air gap alone is not sufficient.

In order to further reduce the electric field strength in the air, particularly near the top of the springs, field control plates are included in the PCB bus bar. These field plates shift the peak electric field from the air to the PCB (e.g., FR4), which has a higher breakdown field strength. Electrostatic simulations were performed using ANSYS Maxwell to develop a PCB layout that would have low electric field strength in the air. Figure 3-26 shows the 2D electric field distribution for a cross-section of the module–bus bar interface. As shown by Figure 3-26a, when no field-grading plates are used in the PCB, the electric field strength in the air exceeds 3 kV/mm. Figure 3-26b shows how the field-grading plates can be used to shift the peak electric field strength from in the air to inside the PCB. A series of 2D and 3D electrostatic simulations were performed to determine the track and field-grading plate locations, shapes, and dimensions.

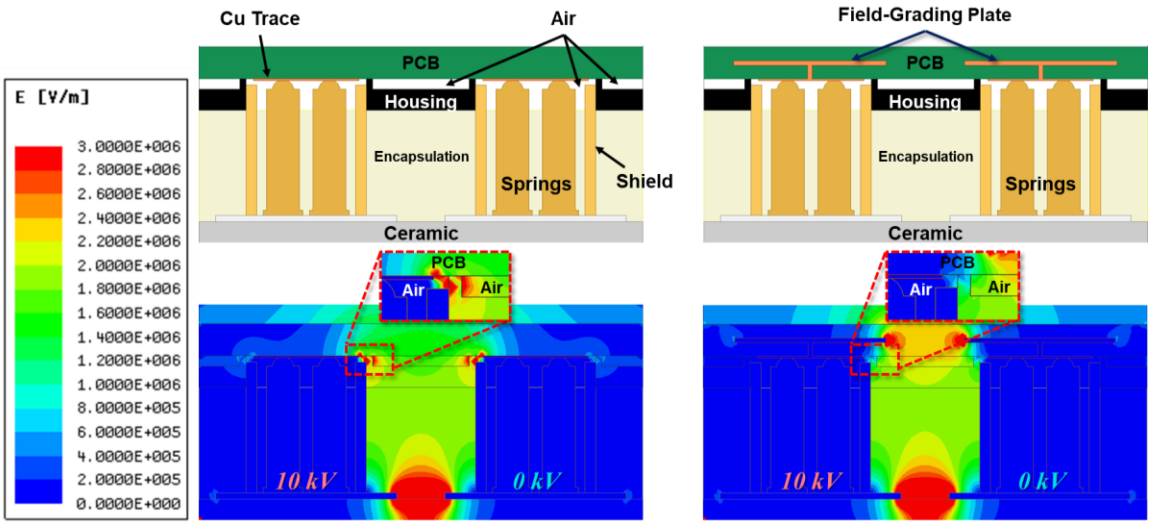



**Figure 3-26: 2D simulated electric field distribution (a) without and (b) with field-grading plates in the PCB.**

There also exists an air gap in the openings in the lid where the spring terminals protrude from the module. If the electric field strength in this area surpasses the breakdown field strength of air, then PD may occur. Electrostatic simulations were performed to develop a design that would result in sufficiently low electric field strength. Figure 3-27 shows the electric field plots for several design iterations. The worst-case simulation results are shown, which is when the S1D2 terminal is equal to S2 (i.e., the low-side switch is conducting and the high-side switch is blocking). In Figure 3-27a, the 3D model being simulated is shown. In Figure 3-27b, a top view of the electric field plot is presented. For this case, the air gap between the springs and the housing is approximately 0.5 mm. As can be seen from the figure, the electric field strength is exceeding 3 kV/mm, the dielectric field strength of air. In particular, the electric field is concentrating around the springs that are closest to the housing and opposing potential, namely, the D1, S1D2, and S1,G1 springs.

To help reduce the peak electric field strength, it is proposed in this work to add metal cylinders around the springs. The cylinders are at the same potential as the springs, resulting in no electric field within them. The cylinders are essentially shielding the springs. The peak electric field strength is now in the air gap between the metal cylinder/shield and the housing. As can be seen from Figure 3-27d, the electric field strength is more uniformly distributed along the cylinder/shield compared to the case without it. However, due to the small air gap (0.5 mm), the electric field strength exceeds 3 kV/mm. When the air gap is increased, the electric field strength is reduced to around 2.2 kV/mm (Figure 3-27e). The radius of curvature of the shield was also adjusted to yield the best electric field distribution (Figure 3-27e).

Unfortunately, it is difficult to implement this shield around the gate and source springs; due to the close proximity of the gate and source terminals, the shield could cause an unintentional short between the two if not carefully implemented. Since the electric field strength is the highest around the S1,G1 springs, adding the shields around the power terminals may not improve the PDIV of the entire module. Accordingly, it was decided to proceed without the shields for the initial module prototype. This shield should be explored in future prototypes to further evaluate its impact on the PD performance. The final design is shown in Figure 3-27f. The air gap has been further increased, and the radius of curvature of the openings in the lid was also adjusted to minimize the electric field strength.

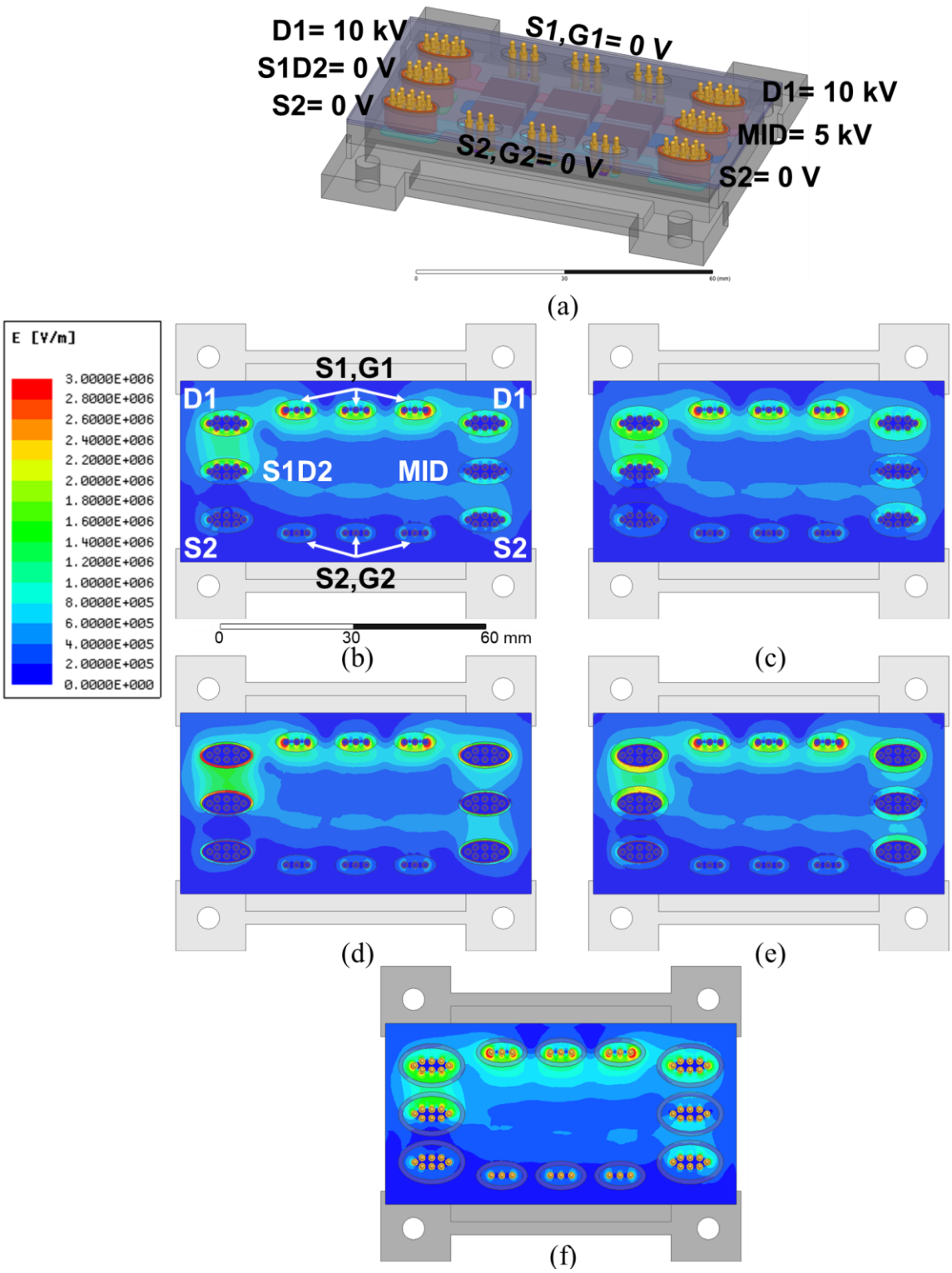



**Figure 3-27: Simulated electric field plots for the housing lid design.**

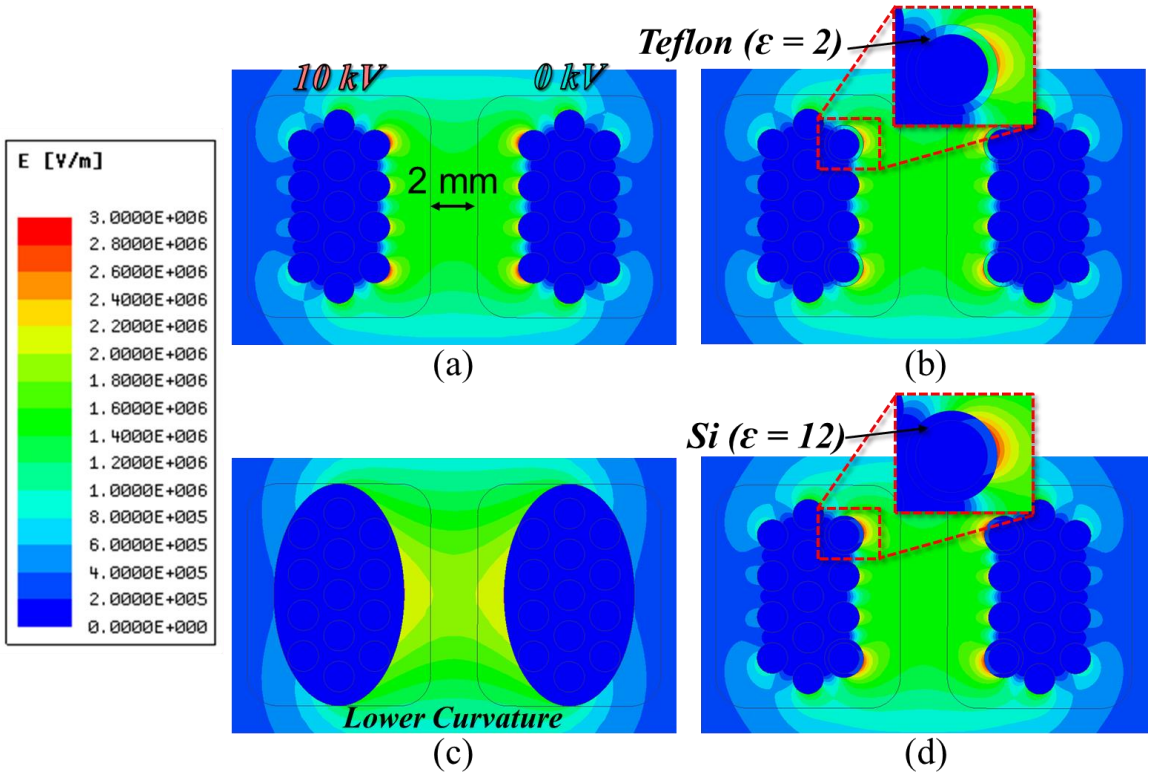
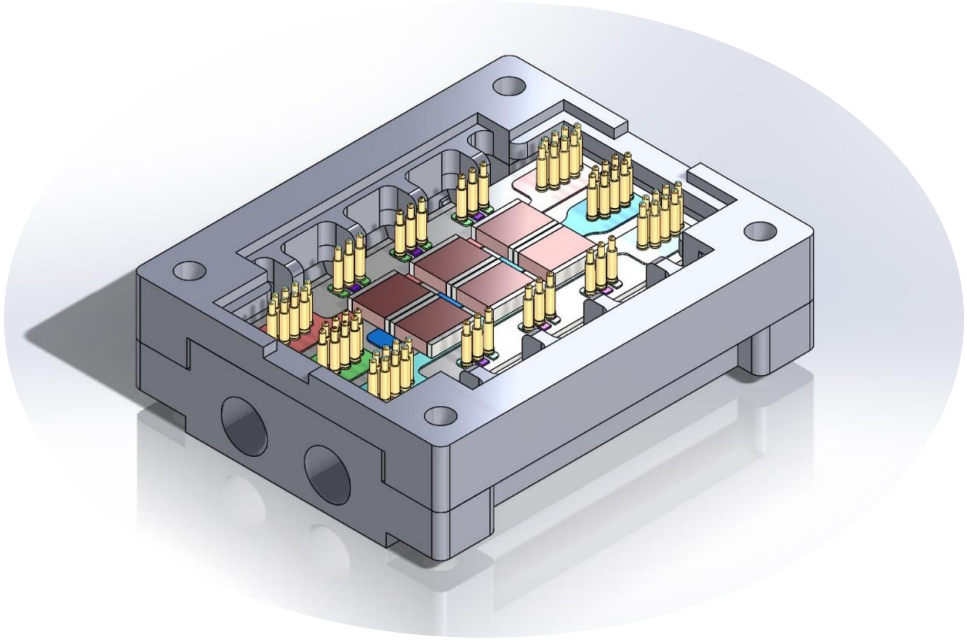



**Figure 3-28: Simulated 2D electric field distribution for (a) spring terminals, (b) springs with a Teflon coating, (c) springs surrounded by a conductive shield with low curvature, and (d) springs with a silicon coating.**

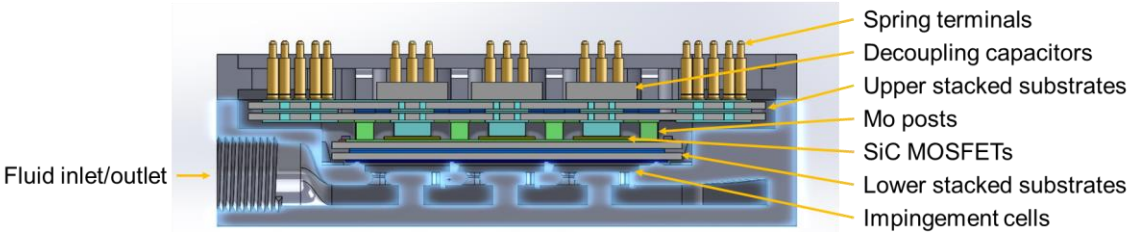
The housing also determines how the thermal management system will be connected/interfaced. Traditional power modules have the substrates and housing mounted to a baseplate. The substrates are typically attached to the baseplate with solder. Due to the large area, significant voiding occurs, which increases the thermal resistance. Moreover, this solder layer is known to be unreliable. A thermal interface material is used between the baseplate and the cooling system (e.g., heatsink or coldplate), which further increases the thermal resistance. Overall, this traditional method often results in high thermal resistance, poor reliability (i.e., it degrades over time), and increased weight.

The thermal management system for the proposed module was designed by the University of Nottingham. To further improve the module power density, the cooling system is integrated into the module housing structure. Direct-substrate, jet-impingement cooling was selected for this module. By eliminating the baseplate, there is one less layer in the heat removal path. Instead, the substrate is sealed directly to the housing/cooler. The housing has open cells that are located underneath each SiC MOSFET die. This allows the incoming cooling fluid to impinge a jet onto the bottom of the lower substrate underneath each die for targeted, efficient cooling. Jet-impingement cooling was studied in detail in [168],[169].

The final design of the housing and cooler is shown in Figure 3-29. As can be seen from the figure, the cooler is integrated into the housing. The final power density of the designed module with the housing and jet-impingement cooler is 3.8 W/mm$^3$, which is similar to that of Wolfspeed's third-generation 10 kV, 240 A SiC MOSFET module [108] without the cooling system.



(a)




(b)

**Figure 3-29: (a) 3D model of the final housing and cooler design for the 10 kV SiC MOSFET module and (b) the cross-section view. Image used with permission of Robert Skuriat.**

## *3.11 Conclusion*

In order to achieve high power density, no external antiparallel diodes are used in the power module. Instead, the reverse current will be conducted through the MOSFET channel, and the internal body diode will be used during the dead time. To further improve the power density, as well as reduce parasitic inductances, and increase the reliability and energy absorption capability, no wire bonds are used in the power module. Instead, a

sandwich structure is used. The power density of the resulting design is 13.0 W/mm$^3$ without the housing.

Having a high power density design for 10 kV SiC MOSFETs results in increased electric field strength within the power module. If not properly addressed, the high electric field strength could exceed the dielectric strength of the dielectric materials, resulting in PD and/or breakdown. Accordingly, several methods are used to reduce the electric field strength both internal and external to the power module. First, due to the thinness of the 10 kV MOSFET dies, posts are used to provide sufficient spacing between the top and bottom substrates in the sandwich structure in order to reduce the electric field strength in this region.

Next, a method for reducing the electric field at the critical triple points at the metal-ceramic-encapsulant interface was selected. Of the many methods proposed in the literature for reducing the electric field and PD at the triple point, the stacked substrate approach was chosen due to its ease of implementation, limited negative consequences, and multi-functionality. Specifically, it is proposed in this work to stack two 1-mm AlN substrates and connect the middle metal layer to the dc bus midpoint. This was found to reduce the simulated electric field by more than 50 % at the critical triple points compared to a design with a single substrate. It was also determined through static thermal simulations that the second substrate does not negatively impact the thermal performance of the power module. Additionally, stacking the substrates and connecting the middle metal to the dc bus midpoint reduces the CM current by creating a low-impedance path at high frequency for the current to circulate instead of going to the system ground.

With the housing and integrated direct-substrate, jet-impingement cooler, the module dimensions are 83.3 mm × 68.2 mm × 24.7 mm, resulting in a power density of 3.8 W/mm$^3$. To avoid the stringent creepage and clearance requirements, a module–system interface was designed such that no conductors are exposed. Additionally, to reduce the electric field strength in the air, field-grading plates are used in the bus bar. These plates shift the peak electric field into the solid dielectric of the bus bar, thereby reducing the electric field strength in the air to less than 3 kV/mm.

Using the top substrate stack to integrate decoupling capacitors above each MOSFET switch pair results in a low and symmetrical power loop inductance of just 4.4 nH for each. This symmetry will improve the dynamic current sharing among the paralleled dies, and the low inductance will result in minimal voltage overshoot and ringing. These features will enable the 10 kV SiC MOSFETs to operate at their fastest switching speeds and at higher voltages and currents.

Another challenge with having a high density, high power module is the high heat flux. To address this issue, direct-substrate jet-impingement cooling is employed for its high heat transfer capability. The cooler, which was designed by the University of Nottingham, is integrated into the module housing. Additionally, materials and processes with high thermal conductivity were selected for the designed power module in order to further enhance the heat removal. In the next chapter, the detailed prototyping, testing procedures, and results of the designed power module will be presented.

# Chapter 4 Prototyping and Experimental Validation of a Wire-bond-less, Planar, 10 kV SiC MOSFET Power Module

## *4.1 Introduction*

In this chapter, the prototyping of the designed power module will be discussed in detail. Specifically, the attachment method for bonding the insulating substrates, dies, and posts will be discussed, followed by the module encapsulation. The testing procedures and results for the module prototypes will then be presented. Static, dynamic, and thermal characterization tests were performed on the prototypes, as well as PD tests on the various module constituents, to evaluate the electrical, thermal, and electrostatic performances. Since this is the first time these advanced packaging technologies and processes have been applied to 10 kV SiC MOSFETs, CPES at Virginia Tech and the University of Nottingham pooled their resources and expertise to prototype and test the jointly-designed power module.

## *4.2 Module Prototyping*

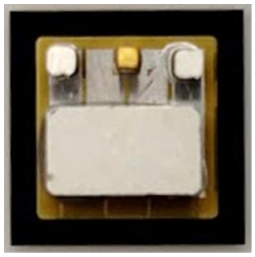
Table 4-1 summarizes the materials evaluated for the prototyping of the designed 10 kV power module. As can be seen from the table, several substrates and attachment methods/materials were evaluated. In particular, Ag sintering was chosen for the substrate-

substrate, die, and post attach because it creates a bond with lower voiding content, higher thermal conductivity, and improved reliability than solder [52]. Although the materials and processes used in this power module are more expensive than traditional packaging technologies (e.g., Al wire bonds, single $Al_2O_3$ DBC without vias, and solder), they allow for improved electrical and thermal performance and reliability. Hence, costs could be saved at the system level, and in the long-term operation of the module, due to extended lifetime and lower maintenance.

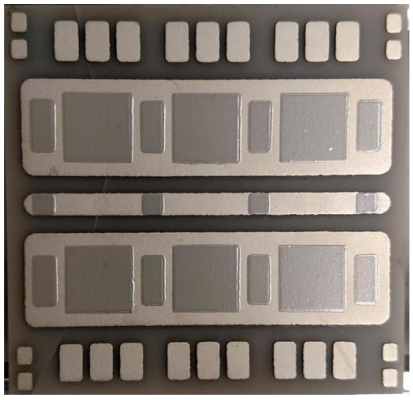
Figure 4-1 and Figure 4-2 summarize two of the tested module prototyping procedures. Figure 4-1 shows the procedure when pressure-less Ag sintering is used for the post and die attachments, while Figure 4-2 shows the procedure when pressure-assisted Ag sintering is used. The former was refined and used by CPES, while the latter was refined and used by the University of Nottingham. The substrate-substrate attachment (not pictured) is the first step in both procedures. A pressure-less sintering process was not explored for the substrate-substrate attach due to the large bonding area. The spring, capacitor, and housing attachment and encapsulation steps are not shown in Figure 4-2, as they are the same as those shown in Figure 4-1. The details of the fabrication steps will be discussed in more detail in the following subsections.

**Table 4-1: Packaging Processes and Materials Selected for the 10 kV SiC MOSFET Module**

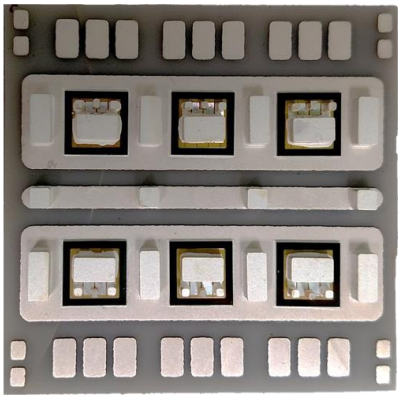
| Component | Process | Material | Advantages |
|---|---|---|---|
| Substrate | Direct-bonded aluminum (DBA) | Ag-plated 1-mm AlN with vias | High thermal conductivity, voltage isolation, and reliability |
| | Direct-bonded copper (DBC) | Au-plated 1-mm AlN with vias | High thermal conductivity, voltage isolation |
| Substrate attach | Pressure-assisted sintering | Nano-Ag paste | Low voiding and high thermal conductivity |
| Die attach | Pressure-less sintering | Nano-Ag paste | Low voiding, and high temperature, thermal conductivity, and reliability |
| | Pressure-assisted sintering | Dried nano-Ag paste | Low voiding, and high temperature, thermal conductivity, and reliability |
| Interconnect | e-beam deposition of Ti, Ni, and Ag | Mo posts | Low inductance, low effective CTE |
| | N/A | Au-plated Cu-Mo-Cu posts | Compatable with soldering, no extra processing |
| Interconnect attach | Pressure-less sintering | Nano-Ag paste | Low voiding and high thermal conductivity |
| | Pressure-assisted sintering | Dried nano-Ag paste | Low voiding and high thermal conductivity |
| | Soldering | Sn96.3/Ag3.7 paste | Thick bondline, compliant |
| Terminals | Pressure contact | Au-plated springs | Round geometry, easy connection, good reliability, and distributes pressure |
| Terminal and capacitor attach | Soldering | Sn63/Pb37 paste | Thick bondline, compliant, low melting temperature |
| Encapsulation | Deareation in vacuum and cure in furnace | Silicone gel (SilGel612) | Good dielectric strength, medium hardness |



1. Sinter posts to dies

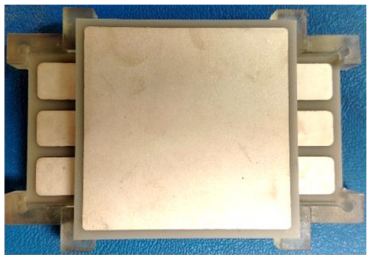


2. Print Ag paste onto bottom substrate stack

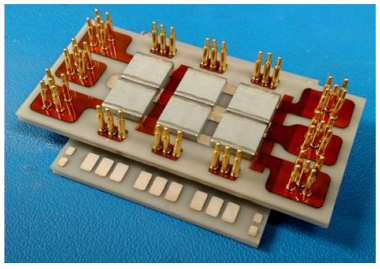


3. Place dies and posts on printed paste

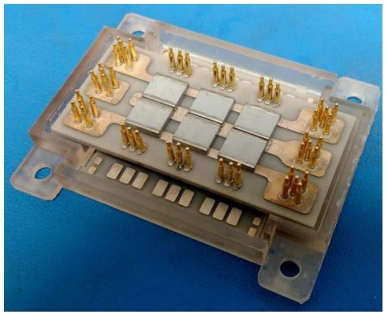
4. Print solder paste



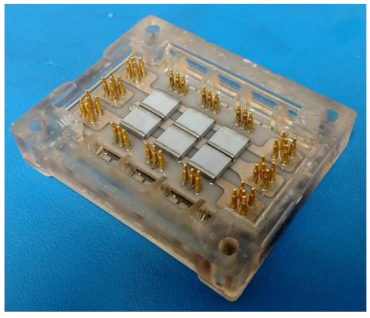
5. Align substrates with jig



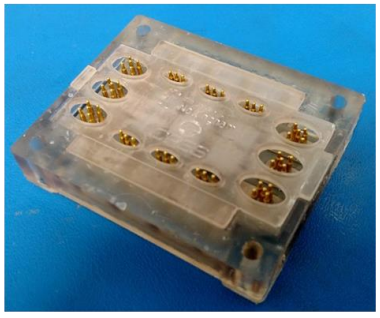
6. Dispense solder paste, place springs and capacitors, and solder



7. Seal module to housing



8. Pour silicone gel, degas in vacuum, and cure



9. Final module with lid

**Figure 4-1: Module prototyping procedure with pressure-less sintering and Ag-plated DBA substrates.**

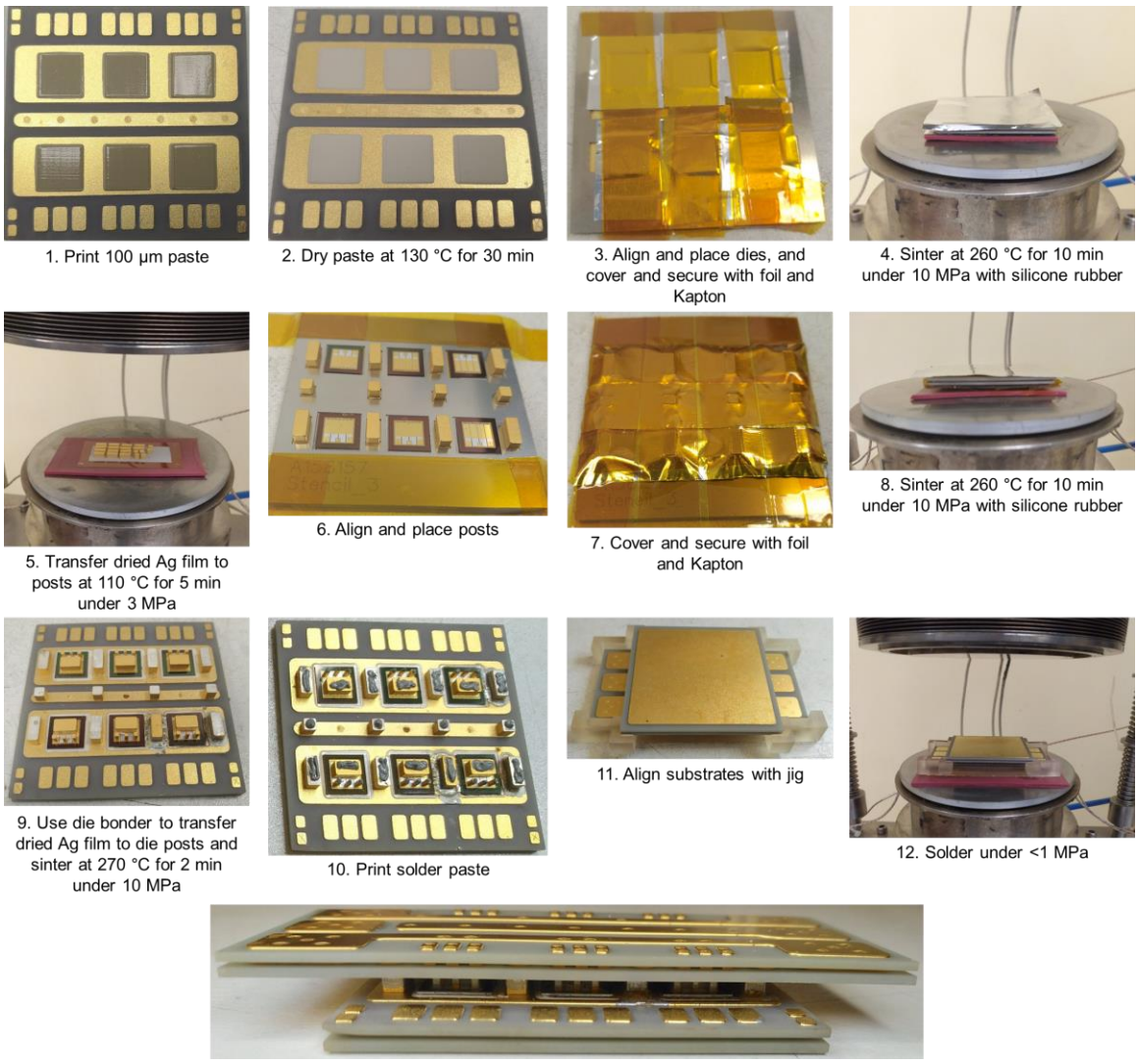



**Figure 4-2: Module prototyping procedure with pressure-assisted sintering and Au-plated DBC substrates.**

### *4.2.1 Substrate-Substrate Attachment*

As shown in the previous chapter, stacking two ceramic substrates can reduce the electric field strength and the EMI of the power module. While multilayer ceramic substrates, such as LTCC [170],[171] and ceramic PCBs [172], are commercially available, they often have limitations that are not suitable for high power applications due to low

maximum via sizes and Cu thicknesses. The performance of these multilayer ceramics under medium-voltages has also not been evaluated. As a result, in this work, a bonding process for attaching two separate substrates to create each stack was developed [173],[174].

A pressure-assisted Ag-sintering process was developed for bonding the 50.3 mm × 49.2 mm bottom and the 35.2 mm × 74.3 mm top stacked substrates. Sintering was chosen instead of soldering because of the lower voiding content and higher thermal conductivity and reliability [52]. Furthermore, since the melting temperature after sintering (960 °C) is lower than the sintering temperature (≤ 260 °C), the sample can undergo multiple sintering processes without affecting the previously-sintered joints. This is essential for this type of planar structure that requires the substrates, dies, and posts to be attached in stages. Solder, on the other hand, will reflow when its melting point is reached. Accordingly, it is common practice to use multiple types of solder with varying melting points. The solder with the highest melting point would be used first, followed by ones with sequentially decreasing melting points to avoid reflowing the previous solder layers. As the number of bonding steps increases, so too does the needed number of solders. The maximum operating temperature of the final prototype will be limited by the last solder paste, which has the lowest melting point.

For the developed large-area sintering process, a 200-µm-thick stainless steel stencil is used to print nano-Ag paste onto one of the two substrates to be bonded. The printed paste is then dried in an oven at 130 °C for 30 minutes. The substrate without the paste is then placed on top of the one with the dried paste. An L bracket is used to help with the alignment. Kapton tape is used to secure the two substrates together and prevent

them from shifting during sintering. Aluminum foil is placed on the top and bottom of the substrate stack to keep the surfaces clean. Silicone rubber is used to improve the pressure uniformity; however, it is not a good thermal conductor. Since only the top plate in the hydraulic press is heated, it is not desirable to put the silicone rubber in between the top plate and the substrate. Instead, the rubber is placed on the bottom of the substrate stack since the bottom plate of the hydraulic plate is not heated and is therefore not contributing to the sintering process. The silicone rubber is cut to roughly the same size as the substrates; if the silicone rubber is too large, then it could surround the substrates and reduce the amount of air around the Ag paste.

The sample is then centered in the hydraulic press. Prior to sintering, the pressure distribution of the press was tested to ensure uniformity. This is important because if the press is not uniform, then the force will not be homogeneously distributed to the substrate and could result in cracking of the ceramic or poor bonding quality. Since only the top plate of the hydraulic press is heated, the side of the substrate stack with the largest metal area is facing upward to allow the heat to better flow to the sintering area. A pressure of 1 MPa (approximately 550 lbs.) was slowly applied to the substrates with the hotplate between 70 °C and 130 °C; the temperature should be more than 70 °C to soften the silicone rubber yet not more than 130 °C to ensure the Ag paste does not begin sintering before the full 1 MPa is applied. Applying the pressure slowly also allows the silicone rubber time to deform. Once the pressure is applied, the hotplate temperature is increased to 260 °C. Once the hotplate reaches 260 °C, the temperature and pressure are held for 30 minutes. After 30 minutes, the hotplate is turned off and the sample cools under pressure. This helps to reduce

the bending/warpage of the substrates that is caused by the CTE mismatch between the Al and AlN and the differences in the metal patterns between the two substrates. The pressure slowly releases naturally with time and change in temperature. Once the temperature reaches below 70 °C, the pressure can be removed entirely. This substrate-substrate sintering process is pictured in Figure 4-3.

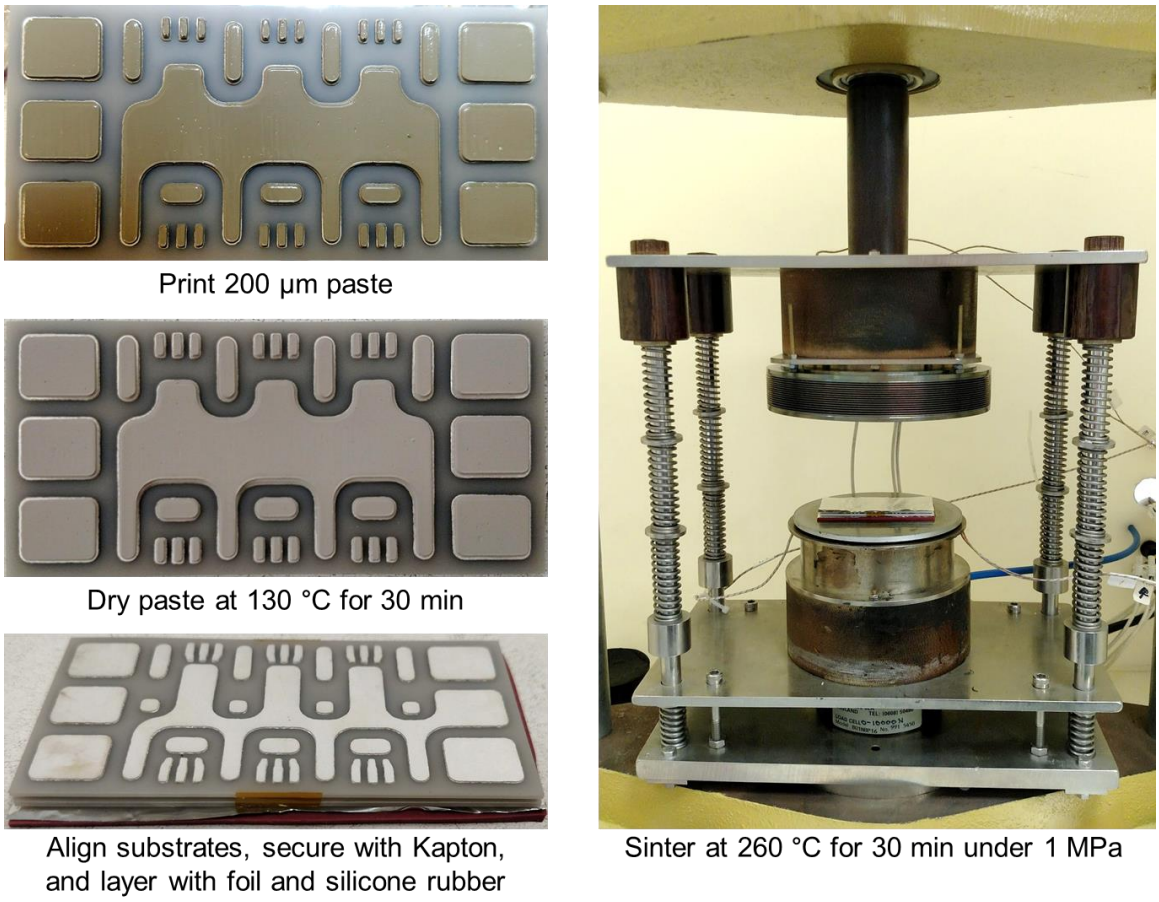



**Figure 4-3: Substrate-substrate sintering procedure.**

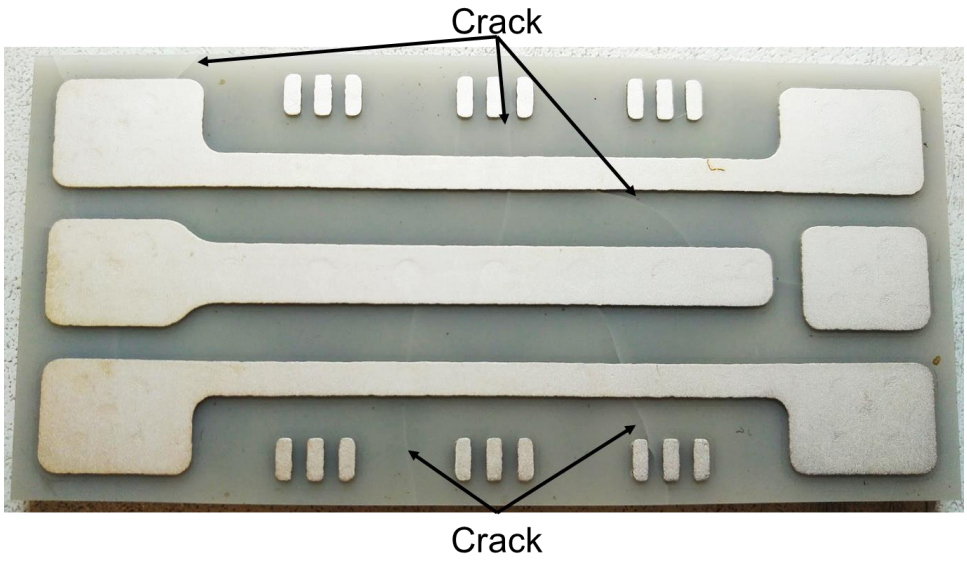
This process results in: no cracks in the ceramic; a high-quality bond layer with low voiding content, defects, and thermal resistance; and low warpage of the substrates. To check the quality of the bonding layer and condition of the ceramic (e.g., cracks), X-ray computed tomography (XCT) scans were performed. XCT was used because it can produce

cross-section images of specific areas of the substrates without cutting the sample. This is achieved by taking many X-ray measurements from different angles and then processing the images in a program that compiles them. Figure 4-5 shows the XCT images of the bottom and top substrate stacks after sintering. These images were taken at the University of Nottingham. The images do not show any significant cracks in the ceramic, voids or defects in the bond line, or misalignment between the two substrates.

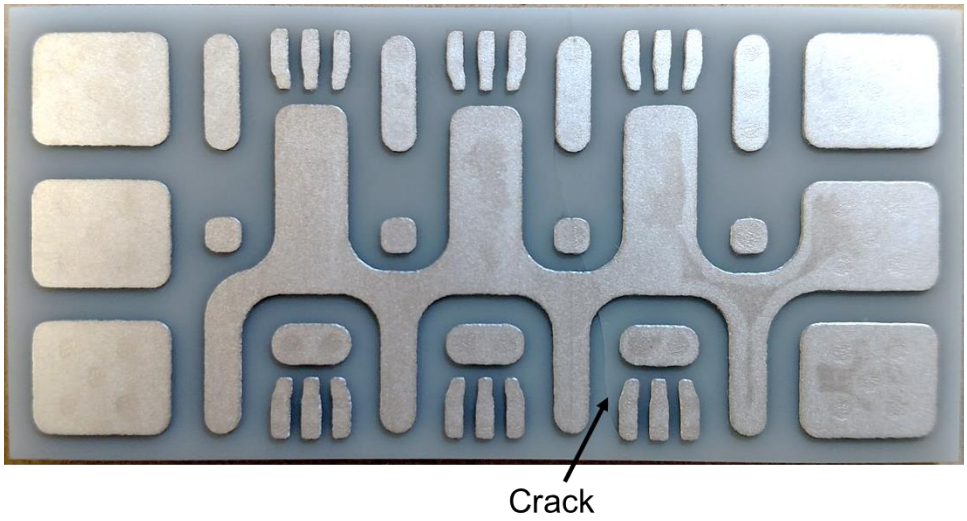
To obtain a process with these desirable results, several revisions were made. In an earlier process, the substrates were sintered at 250 °C for 10 minutes with 10 kN (approximately 4.0 MPa and 3.8 MPa for the top and bottom substrate stacks, respectively), and Teflon was used to improve the pressure uniformity during sintering. However, this process resulted in cracking of the ceramic. A cause for the cracking could be due to pressure nonuniformity, which was causing some parts of the sample to be under higher pressure than others, resulting in cracking in the places with the higher pressure. To address this issue, first, the flatness of the press was checked using pressure measurement film. Next, the film was used to determine the pressure distribution on the substrate when it is under pressure in the press. From this test, it was found that the Teflon was not sufficient for distributing the pressure uniformly. When the Teflon was replaced by silicone rubber, the pressure uniformity was improved.

In an attempt to further improve the pressure uniformity and thus reduce the likelihood of cracking the ceramic, negative stencils were created to fill the spaces in between the metal traces. The idea behind these stencils is that they would essentially act as though the substrate has a single solid trace on the top and bottom. The pressure measurement tests showed some improvement in the uniformity when these negative

stencils were used; however, several samples still cracked during sintering, even with the stencils and silicone rubber. It was found that lowering the pressure to 1 MPa was effective in ensuring no cracking of the ceramic while still achieving high bonding quality. Figure 4-4 shows images of two different top DBA stacks that cracked when sintering under 5 MPa and 2 MPa. Comparing the two samples, it is clear that decreasing the pressure from 5 MPa to 2 MPa reduced the number of cracks.




(a)




(b)

**Figure 4-4: Cracked DBAs after sintering under (a) 5 MPa and (b) 2 MPa.**

In particular, it is essential to have low voiding content in the areas below the SiC MOSFET dies so the heat generated by these devices can be effectively removed from the module. The approximate die locations are outlined in Figure 4-5. No significant voiding is observed in these critical areas. To further check the thermal characteristics of the sintered bottom substrates, thermal impedance tests were performed at six locations along

the surface of the sample where the SiC dies would be located [52]. Cumulative structure-function analysis was then used to find the thermal resistance of the bond-line at each location [173]. The measured thermal resistances ranged from 0.11–0.14 K/W, resulting in a specific thermal resistance of approximately 6.9–8.8 $mm^2K/W$ [175], which is close to the low-end of the 4–100 $mm^2K/W$ range found in most thermal interface materials [176]. The low variation of the measured thermal resistances indicates good uniformity of the bond, and confirms that no large voids or cracks exist in these locations. This conclusion is in good agreement with the XCT scan images (Figure 4-5)a.

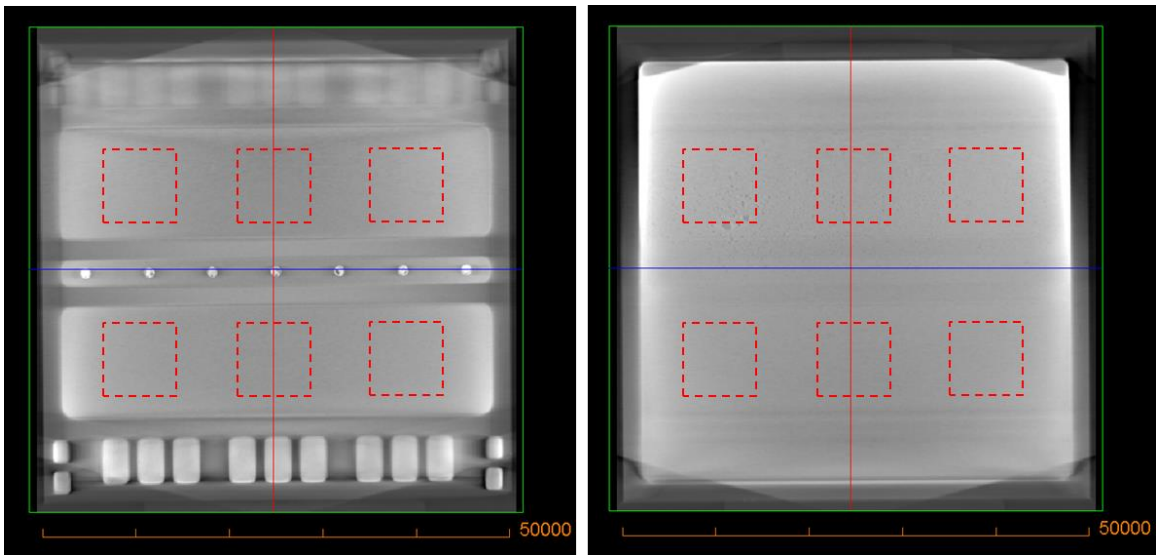



**Figure 4-5: XCT images of the bottom substrate stack after sintering. The dashed red boxes indicate the approximate location of the 10 kV SiC MOSFET dies.**

To check the warpage of the substrate stack after sintering, surface profile scans were performed. Figure 4-6 shows the scan results for the bottom and top substrate stacks before and after sintering. As can be seen from the figure, while the bottom substrate stack maintained good flatness after sintering, the top substrate stack has approximately 50 µm of residual bending. This could be due to the more complex pattern of the top substrates

(DBA3-4), which may have resulted in non-uniform thermomechanical stresses on the top and bottom substrates during sintering. The University of Nottingham had performed thermomechanical simulations of the DBA sintering process using Abaqus 6.14 [177]. Although the simulation results for the top substrate (DBA3-4) sintering only showed a residual bending of 3 µm, the direction of the bending was the same as that observed in the experiment [177].

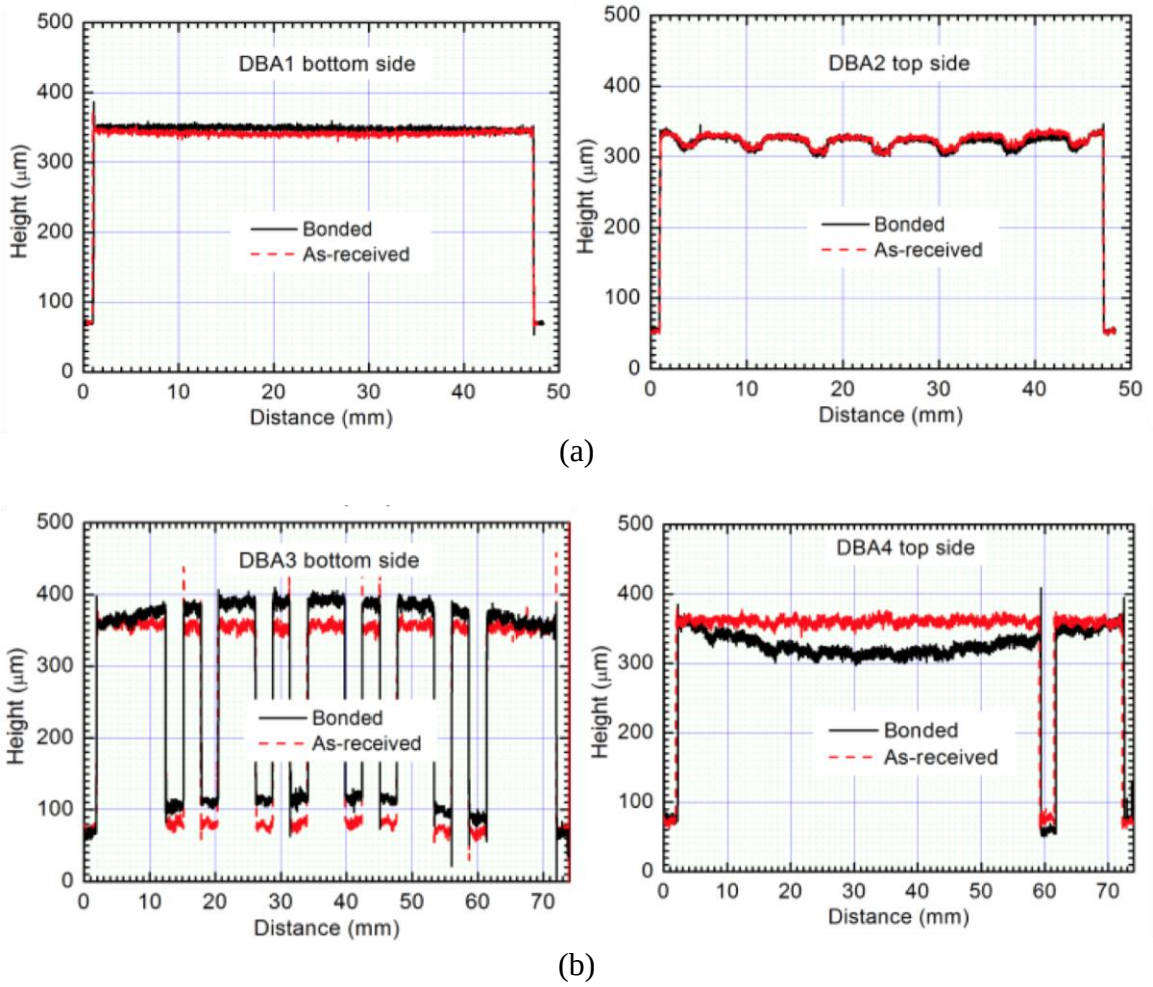



**Figure 4-6: Surface profile scans of (a) bottom (DBA1-2) and (b) top (DBA3-4) substrate stacks before (red line) and after (black line) sintering [177].**

### *4.2.2 Semiconductor Die Topside Metallization*

The 10 kV SiC MOSFET dies, like most power semiconductor devices, have Al metallization on the top pads (i.e., the gate and source). This is common practice as it is compatible with customary Al wire bonding. However, this Al metallization is not compatible with soldering or sintering, which is needed to attach the posts. Therefore, Ti and Ag were deposited on top of the original Al pads such that the posts could be sintered to the topside of the dies.

As mentioned in the previous chapter, two methods were evaluated for the post attach to the dies. In the first method, a two-step photolithography process was used to re-pattern the top surface of the MOSFET. The new pattern enlarged the gate pad and increased the distance between the gate and source pads, thereby reducing the likelihood of an unintentional short between the two during the post attachment process. By enlarging the gate, the same 1.0 mm × 1.0 mm posts that were used for the Kelvin source could also be used for the gate.

Prior to the metallization procedure, the dies are characterized using a Keysight B1505A curve tracer. Since the tests are done in air, the voltage is limited to 2.5 kV. Beyond this value, the high electric fields could breakdown the air, resulting in PD and potentially arcing. Next, the die surfaces are cleaned with an oxygen plasma. BCB is then spin-coated onto the dies. The first photolithography step is then performed using a photoplot to create the openings in BCB such that the existing Al pads can be contacted. After the BCB is exposed and developed, it goes through a curing process. After curing, the film is descummed with an $O_2$-$CF_4$ plasma in order to remove a thin polymer film leftover from the develop process. A photoresist layer is then spin-coated onto the die. A

second photolithography step is then done using another photoplot to create the new gate and source pad patterns. After the photoresist is exposed and developed, it is again descummed with another $O_2$-$CF_4$ plasma. Sputtering or e-beam is then used to deposit approximately 100–200 nm of Ti and 100–200 nm of Ag. Finally, the photoresist is lifted off using acetone.

Figure 4-7 shows one of the newly-metallized dies. This method, though complex, gives high accuracy and precision of the new pattern. The static characteristics were repeated after the die metallization process, and no changes in the reverse drain leakage current (Figure 4-8a) or on-state resistance (Figure 4-8b) were observed. While developing this re-metallization procedure, only semi-functional 10 kV SiC MOSFET dies were used. Hence, the characteristics shown in Figure 4-8a and Figure 4-8b are for semi-functional dies. The fully-functional 10 kV die have lower leakage current.

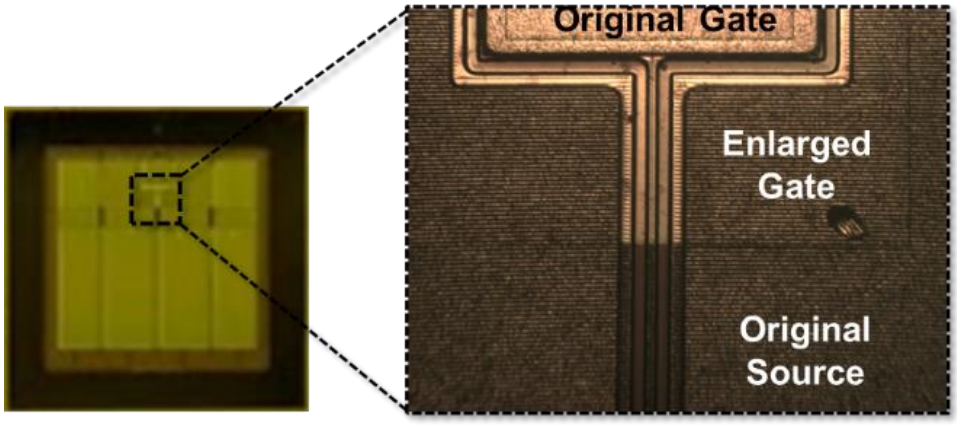
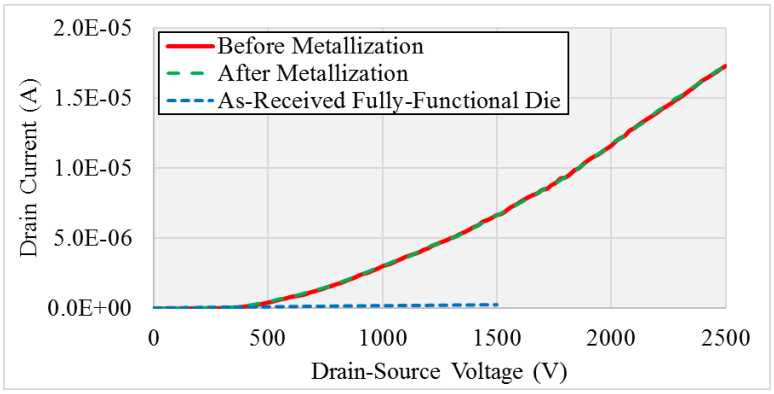
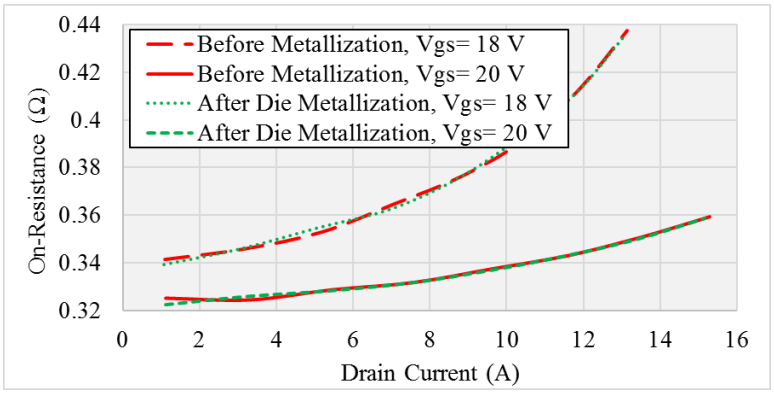



**Figure 4-7: 10 kV SiC MOSFET die after metallization process with enlarged gate pad (right).**




(a)

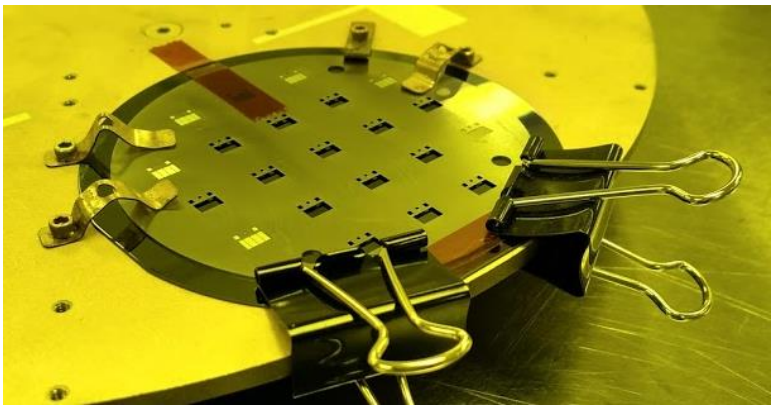



(b)

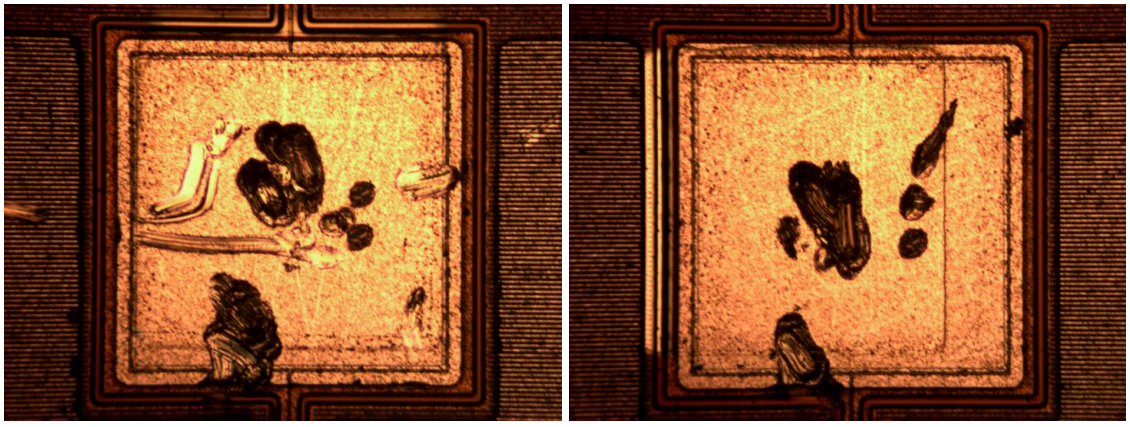
**Figure 4-8: (a) Reverse drain leakage currents at VGS= 0 V and 25 °C, and (b) on-resistances at $V_{GS}$= 18 V (dashed curve) and $V_{GS}$= 20 V (solid curve) and 25 °C before (red curves) and after (green curves) the die re-metallization. The die used for testing the metal**

While this procedure is effective, it is time consuming; it requires multiple photolithography steps, and only one die can be processed at a time to achieve uniform coating of the BCB and photoresist layers. A faster solution is to use a shadow mask to deposit metal onto the existing Al pads. This process allows multiple devices to be metallized at once, though the accuracy of the deposited metal is significantly reduced. Two metal combinations were evaluated: 1) niobium (Nb) and Au, and 2) Ti and Ag. Both combinations resulted in high bonding strength. Figure 4-9 shows the designed shadow mask and images of the gate pad of two dies. While one of the images shows good

alignment of the deposited metal, the other shows the deposited metal is shifted to the left and is nearly overlapping (and thus shorting) the neighboring source pad. Moreover, since the gate pad is not enlarged in this process, a smaller gate post must be used. The gate posts used for the dies metallized with this method are 0.7 mm × 0.7 mm. Since no dielectric was deposited in this metallization process, the distance between the gate and source remains small (0.16 mm). As a result, the post attachment must be done with high accuracy in order to avoid a gate-source short. The post attachment processes will be discussed in the following section.



(a)



(b) (c)

**Figure 4-9: (a) Shadow mask die metallization process, and images of MOSFET gate pad after deposition with (b) good and (c) bad alignment.**

### *4.2.3 Post Attachment*

Mo was selected as the post material because it has a lower CTE compared to Cu; however, solder and Ag (for sintering) do not adhere well to Mo. Accordingly, additional metal layers are needed. Two types of posts were evaluated: 1) Au-plated Cu-Mo-Cu laminate posts, and 2) Ag-plated Mo posts. The first was similar to those used in [62]. For the 2-mm-tall posts, 1.48 mm of Mo was sandwiched between two 0.26-mm Cu layers. The posts were then either plated with Ni and Au (2–5 µm Ni and 0.1 µm Au) or Ni and Ag (2–5 µm Ni and 0.1 µm Ag). The Cu and Ni layers act as solder diffusion barriers for compatibility with soldering, while the Au and Ag layers are used to improve the bonding strength when sintering.

It was shown in [62] that thinner Cu layers can improve the thermal cycling capability. As such, pure Mo posts with no Cu laminate were also evaluated. To make the Mo posts compatible with soldering and sintering, thin layers of Ti, nickel (Ni), and Ag were deposited. Prior to deposition of the metal layers, the oxide on the Mo must be removed to improve the bonding. To remove the oxide, the Mo posts were placed in a bath of aqua region (1:3 nitric acid to hydrochloric acid) for approximately 10 minutes. After rinsing and drying the Mo posts, they were immediately transferred to the deposition chamber to minimize oxide regrowth. Both sputtering and e-beam evaporation were explored for depositing the metal layers onto the Mo. While sputtering can provide high-quality deposition layers, the deposition rates are longer. Accordingly, if only 100–200 nm of Ti and Ag need to be deposited (i.e., no solder diffusion barrier is needed), then sputtering would be a good choice. However, if a thick solder diffusion barrier is needed, as is the case in this work, then e-beam is preferred due to its faster deposition rates.

Specifically, an e-beam evaporator was used to deposit 100–200 nm of Ti, 1000 nm of Ni, and 100–200 nm of Ag. The thickness of these layers is more than an order of magnitude lower than that of thinnest Cu laminate evaluated in [142], which was approximately 60 μm. As such, it is expected that the effective CTE of these posts will be closer to that of Mo, thereby further improving the reliability compared to the Cu-Mo-Cu laminated posts. It should be noted that the thick Ni layer was added as a solder diffusion barrier. If only Ag sintering were to be used, then the Ni layer could be omitted. High bonding strength was achieved for Ti/Ag-coated Mo posts that were sintered without pressure to Ag-plated substrates. However, since soldering will be used to attach the tops of the posts to the top substrate, as will be discussed later, the posts also needed to be compatible with soldering. Hence, the thick Ni layer was added between the Ti and Ag layers.

Two sintering methods were evaluated: 1) pressure-less sintering with nano-Ag paste, and 2) pressure-assisted sintering with dried Ag film. For the pressure-less sintering, Ag paste was stenciled onto the substrate with a thickness of 50 μm. The posts were then placed on top of the stenciled paste, and the sample was transferred to a hotplate and sintered. The sintering profile varied depending on the type of Ag paste used. For nanoTach-LT paste from NBE Tech, the sintering was performed at a ramp rate of 5 ˚C/min to 280 ˚C and held for 30 minutes. Die shear tests were performed on several of the Ag-coated Mo posts using a Dage Series 4000 bond tester. Bonding strengths between 31.3 MPa and 67.0 MPa (depending on the area of the post) were achieved when the posts were sintered to the Ag-plated substrate. The Ag-coated Mo posts were also sintered to the MOSFET die with the Ag topside metallization using the same sintering process. Shear

tests revealed bonding strengths were 47.3 MPa, on average, for the Kelvin source posts (1.0 mm × 1.0 mm) and 33.1 MPa for the power source posts (5.2 mm × 3 mm). Figure 4-10 shows the die after shear testing. From the image, it can be seen the Ag adhered well to both the posts and the die metallization, as desired.

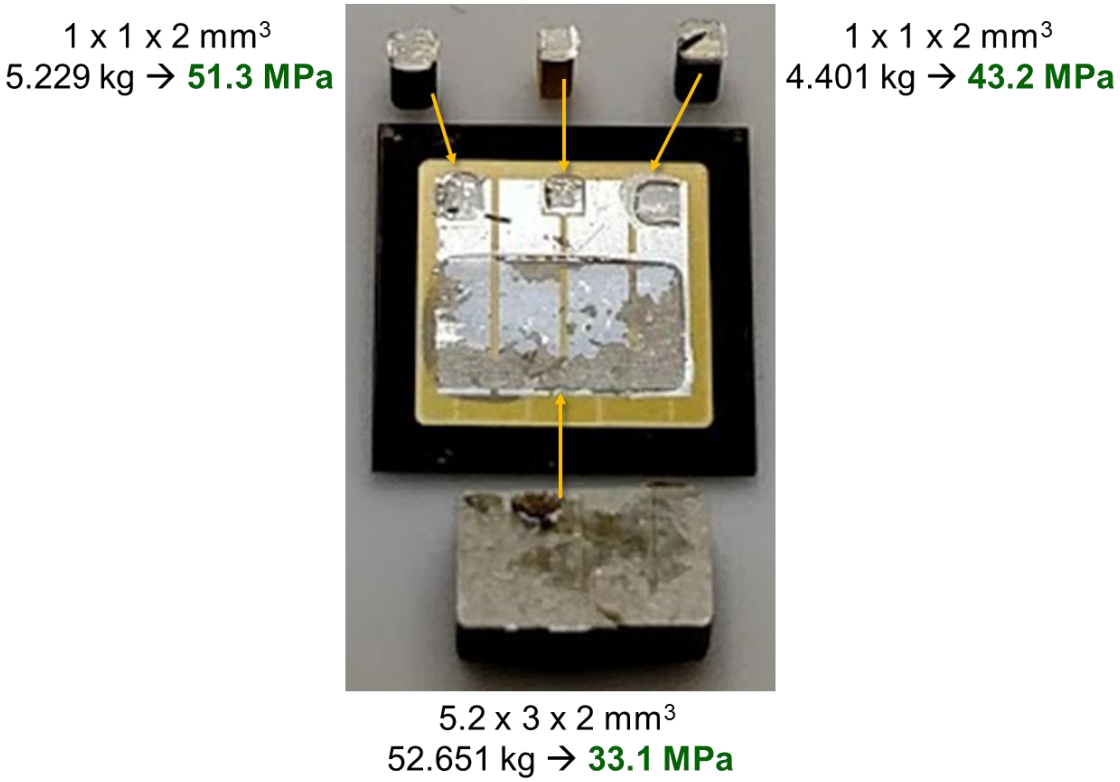



**Figure 4-10: Die after post shear test.**

For the pressure-assisted process, Ag paste was dried and then the posts were stamped onto the dry film either with a die bonder or a hydraulic press (depending on the size of the post). This stamping transferred the Ag film to the post. The sintering was then performed with either the die bonder or hydraulic press. The die bonder was used for sintering the small Kelvin source and gate posts as it could provide sufficient pressure (10 MPa) and accurate placement. This accurate placement is essential when the 0.7 mm × 0.7 mm gate posts are used with the non-dielectric die metallization process. If the placement

is not accurate, then the gate and source could be shorted. For the larger posts, the die bonder could not provide sufficient pressure, so they were placed by hand and then sintered using the hydraulic press.

### *4.2.4 Semiconductor Die Attachment*

As mentioned above, Ag sintering was chosen for the die attach because it has been shown to have lower thermal impedance and thermal cycling capability compared to solder [52]. Both pressure-less and pressure-assisted Ag sintering processes using different types of nano-Ag paste were evaluated. The 10 kV SiC MOSFET dies are 8.1 mm × 8.1 mm × 0.5 mm and have Au metallization on the bottom surface (i.e., the drain contact). Since Ag diffuses faster than Au, a sintering profile that limits the Ag diffusion is essential [178],[179]. If too much Ag diffuses into the Au, then Kirkendall voids will form at the Ag-Au interface, resulting in a bond with low shear strength [178]. After several iterations, the final sintering profile shown in Figure 4-11 was determined to yield the best bonding quality for pressure-less sintering. Using Kyocera's CT2700R7S Ag paste and this sintering profile, the resulting die shear strength was 14.6 MPa, on average, with a peak of 18.4 MPa, for the 8.1 mm × 8.1 mm dies [175]. Figure 4-12 shows the substrate after the die shear test. It can be seen that the sample with lower bonding strength (right) has a circular pattern on both the substrate and die. This pattern was present in most of the poorly-bonded samples. It is unclear what causes this pattern. It could be due to some sort of contamination on the die. Plasma cleaning was performed on the dies to eliminate the possible contamination, though no improvement in the bonding strength was found.

Changing the Ag paste and sintering profile yielded the greatest improvement in the bonding strength.

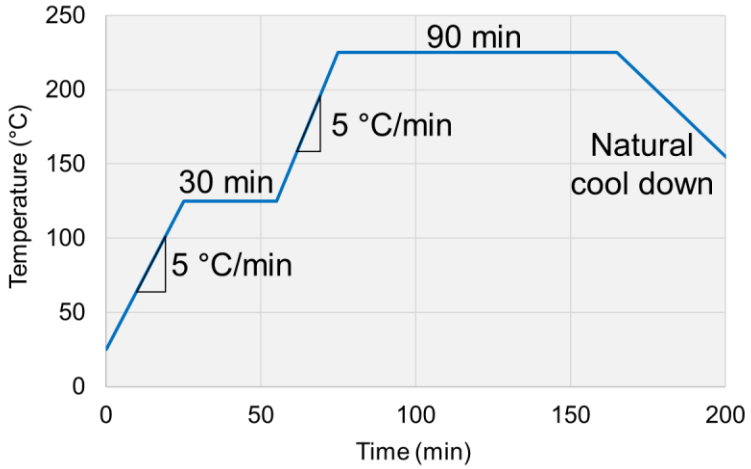



**Figure 4-11: Pressure-less sintering profile for the Kyocera nano-Ag paste with the Au-plated dies.**

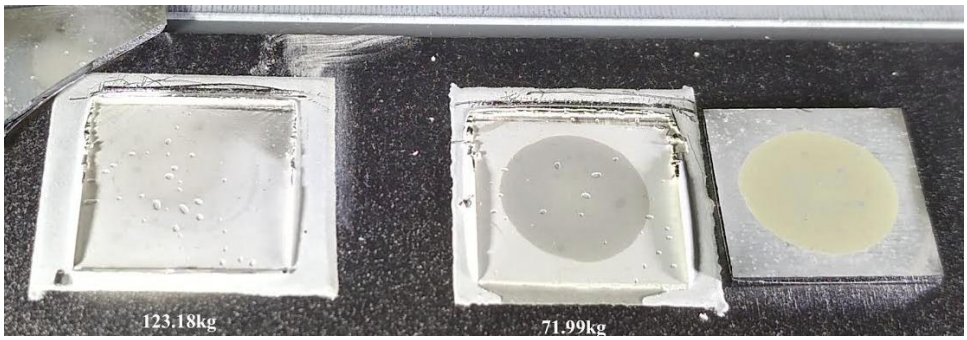
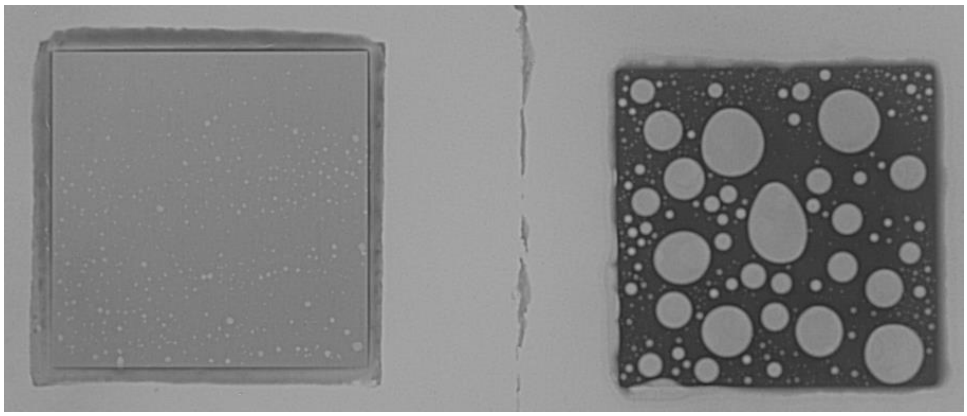



**Figure 4-12: Substrate after die shear test. Image and die shear tests courtesy of Tianjin University.**

Applying pressure during sintering can further improve the shear strength by creating a denser Ag layer [178]. However, pressure-assisted sintering is more complex, especially when sintering multiple dies simultaneously, since the pressure must be uniformly applied to all of the dies. Nonetheless, pressure-assisted sintering was also evaluated for the die attach. Ag paste was screen printed onto the Ag-plated DBA with a thickness of 100 µm, and then dried in an oven at 130 °C for 10 minutes. Once the paste was dried, a 10 kV die was placed on top, and the sample was sintered at 250 °C for 5

minutes with 10 MPa using a hydraulic press. The die shear strength of the pressure-assisted Ag-sintered sample was 25.0 MPa. X-ray images of the bonding layer show low voiding content (Figure 4-13).

Soldering was also evaluated for the die attach. For the soldering, 50-µm-thick 96.5Sn/3.5Ag preform with 1 % NC-10HF flux coating from Indium Corporation was used. This preform was selected because it is compatible with the Ag-plating of the DBAs, and it has a high melting temperature of 221 °C. To test this method, a 10 kV SiC MOSFET die was soldered to a Ag-plated DBA. The soldering was done in air at 260 °C. The die shear tests revealed a bonding strength of 36 MPa; however, the x-ray images (Figure 4-13) showed significant voiding (approximately 40–50 %). Hence, a high thermal resistance can be expected. Vacuum reflow soldering could be used to reduce the voiding content, though it was decided to proceed with the sintering methods for the module prototypes.



(a) (b)

**Figure 4-13: X-ray images of die attach layers for a 10 kV 8.1 mm × 8.1 mm die using (a) pressure-less Ag sintering, and (b) 96.5Sn/3.5Ag solder preform. Image and X-rays courtesy of Tianjin University.**

### *4.2.5 Substrate-Post Attachment*

The top substrate stack is attached to the posts using solder paste. Solder is chosen for this bonding instead of sintering for several reasons. First, solder can create a thicker bondline than sintering. In this case, a thicker bondline is preferred to accommodate height tolerances for the posts, and curvature of the substrates. Second, solder is more compliant than Ag. Compliance is important in this layer as it will enable some thermomechanical movement. If the entire structure is rigid, then the stresses will be high and could affect the reliability. Finally, since the top surface is not used for cooling in this version, the thermal resistance of this bond layer is not critical.

The solderability of the posts was also evaluated. Initially, posts with approximately 100–200 nm each of Al, Ti, and Ag were soldered to Ag-plated DBA substrates with Sn10/Pb88/Ag2 solder paste. This solder paste was selected initially because it contains Ag, which should improve the bonding strength to the Ag-plated Mo, and it has a high melting temperature of 268–290 °C [180]. The resulting bonding strengths of the solder joints were less than 10 MPa, with values reaching as low as 3.4 MPa. As a result, a Ni diffusion barrier was added between the Ti and Ag layers. For a Ni thickness of approximately 500 nm, the bonding strength was still very low, indicating the barrier was not thick enough. After increasing the Ni thickness to 1000 nm, the bonding strength with Sn10/Pb88/Ag2 solder paste was increased to 33.3 MPa, on average, indicating high bonding quality.

For the final power module, Sn96.3/Ag3.7 solder paste, which has a lower melting temperature of 221 °C and a tensile strength of 8.36 ksi [180], was selected. A 200-µm-

thick layer of paste is printed onto the bottom surface of the top substrate (i.e., DBA3). A 3D-printed jig made of high-temperature resin [181] is used to align the two module halves. The sample is then placed in a furnace to reflow the solder. The furnace is first set to 180 °C for 10 min to heat up the sample, and then increased to 320 °C to melt the solder. This high temperature is needed due to the large thermal mass of the multi-ceramic module structure. A multimeter is used to verify that all the posts are successfully attached to the appropriate pad on DBA3. Figure 4-14 shows an XCT image of the soldered modules, which shows the good alignment of the posts to the DBA.

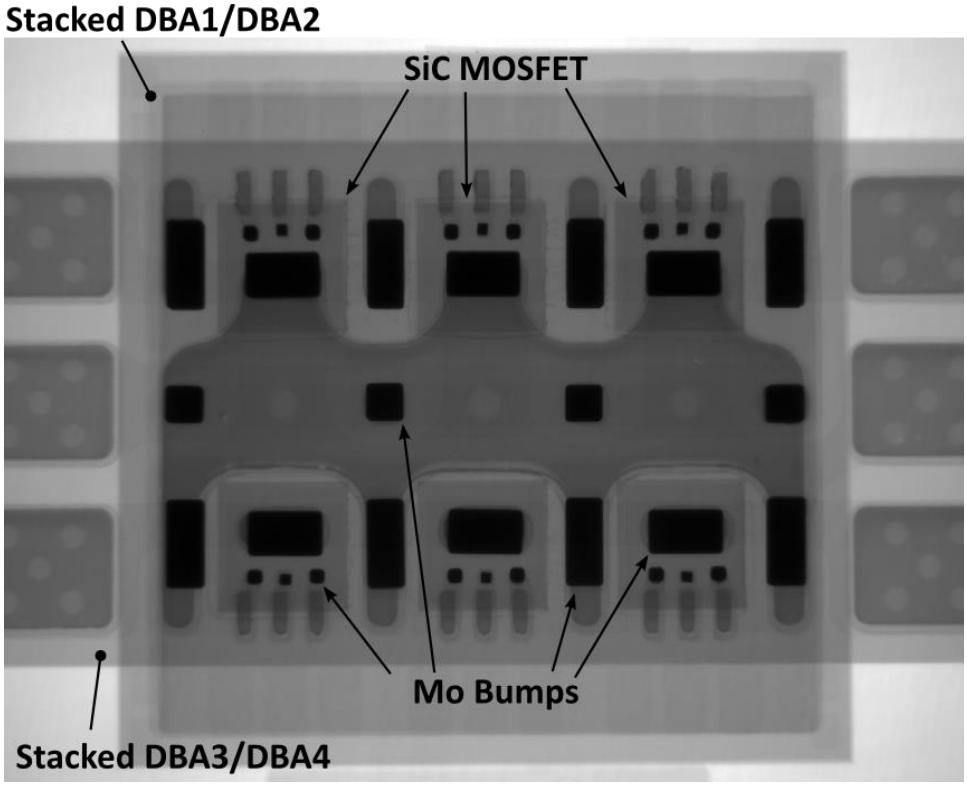



**Figure 4-14: XCT image of the module after the top DBA was soldered to the posts.**

### *4.2.6 Spring and Capacitor Attachment*

Next, the spring terminals and decoupling capacitors are attached. The springs used in this power module are CG-2.5-6-SM from Smiths Interconnect/Interconnect Devices [159]. They have a continuous current rating of 10 A, resistance of less than 10 mΩ, and are plated with Au for compatibility with soldering [159]. A laser is used to cut a stencil for the springs out of 5-mil Kapton tape. The tape is then transferred to the top surface of DBA4. Tacky flux (TSF6502 30 from TSF) and Sn63/Pb37 solder paste are then dispensed, and the springs are placed. Sn63/Pb37 has a melting temperature of 183 °C [180], which is lower than that of the Sn96.3/Ag3.7 solder used to attach the posts to DBA3. The sample is first heated to 150 °C for 5 minutes and then increased to 250 °C for another 5 minutes. Once the solder reflows, the springs self-align. The shear strength for the soldered springs, which have a diameter of 1.88 mm, is 64.2 MPa on average, with a maximum of 69.5 MPa. After soldering, the samples are soaked in acetone and alcohol on a hotplate at 50 °C for 15 minutes each to remove excess flux.

### *4.2.7 Encapsulation*

The housing with the integrated jet-impingement cooler for the power module was 3D printed out of high-temperature resin, which has a heat deformation temperature of 289 °C at 0.45 MPa [181] (Figure 4-15). Silicone sealant was used to seal the bottom substrate stack to the housing. After curing, the module can be encapsulated. For the reasons mentioned earlier and explored in [161], silicone gel was selected for the encapsulation. Two silicone gels were tested: 1) Nusil R-2188 from Nusil, and 2) SilGel 612 from Wacker. The SilGel 612 was also evaluated in [84], and was found to have stable PDIV after aging

1000 hours at 85 ℃ and 85 % relative humidity. Nusil R-2188 was evaluated in [161] and was found to have good stability at high temperatures. The material properties for these two gels are shown in Table 4-2. The SilGel 612 has 18 % higher dielectric strength, and has nearly 13 times lower viscosity. This lower viscosity is preferred as it will more easily fill small gaps in the power module (e.g., in between the stacked substrates).

**Table 4-2: Silicone Gel Material Properties**

| Material | Operation Temperature (°C) | Dielectric Strength (kV/mm) | Dielectric Constant | CTE (ppm/°C) | Viscosity (mPa·s) |
|---|---|---|---|---|---|
| SilGel 612 | < 200 [84] | 23 [183] | 2.7 [183] | Unknown | 1000 [183] |
| Nusil R-2188 | -65–300 [161] | 19.5 [182] | 2.6 [182] | 320 [182] | 12500 [161] |

The encapsulation procedure is as important as the material itself. These silicone gels come with two parts (A and B) that must be mixed together. For the Nusil R-2188, the recommended 1:1 ratio of part A to part B is used [182]. For the SilGel 612, ratios of 1:1 and 1.5:1 were tested. The 1.5:1 ratio (i.e., reducing the amount of part B) results in a harder formulation that was less tacky than the 1:1 formulation [183]. If these two parts are mixed in air, then air becomes entrapped in the mixture. This trapped air is significant because it could impact the PD [87]. This trapped air could be avoided by airless mixing.

Due to equipment limitations, the parts were mixed by hand in air and then the mixture was placed in a vacuum to remove the entrapped air. The mixture is degassed for 30 minutes. The degassed mixture is then removed from the vacuum chamber and poured into the module housing. Since this pouring process introduces more air, the filled module is put into the vacuum chamber for another 30 minutes to remove the air bubbles. Since

the gel is also slowly curing, the degassing step should not be too long as it will be harder for the trapped air to escape. Therefore, the degassing steps are limited to 1 hour total.

The module is then placed in a box furnace for curing. The module is cured at 100 °C for 20 minutes for the SilGel 612, and 100 °C for 30 minutes for the Nusil R-2188. A box furnace is used because it helps the gel to cure more uniformly. If a hotplate was used, the heat must travel from the bottom of the module to the top. Due to the thickness/height of the module, the silicone gel at the bottom of the module will cure faster than the gel at the top.

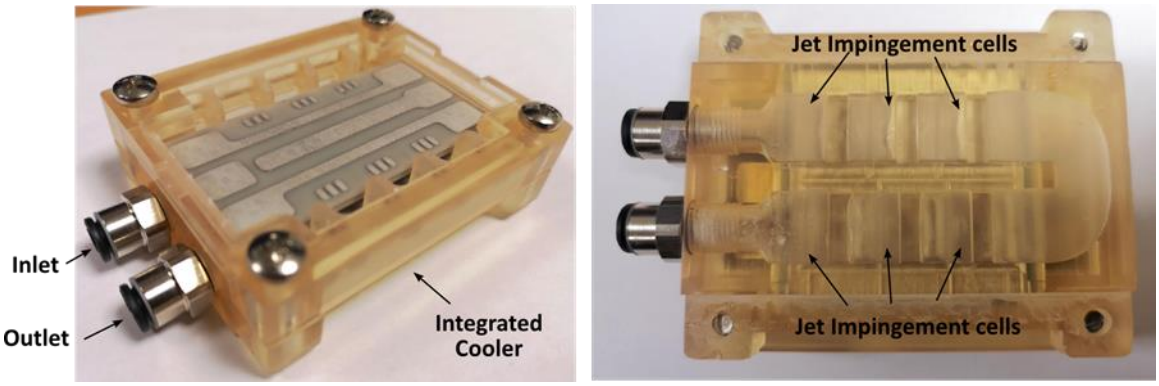
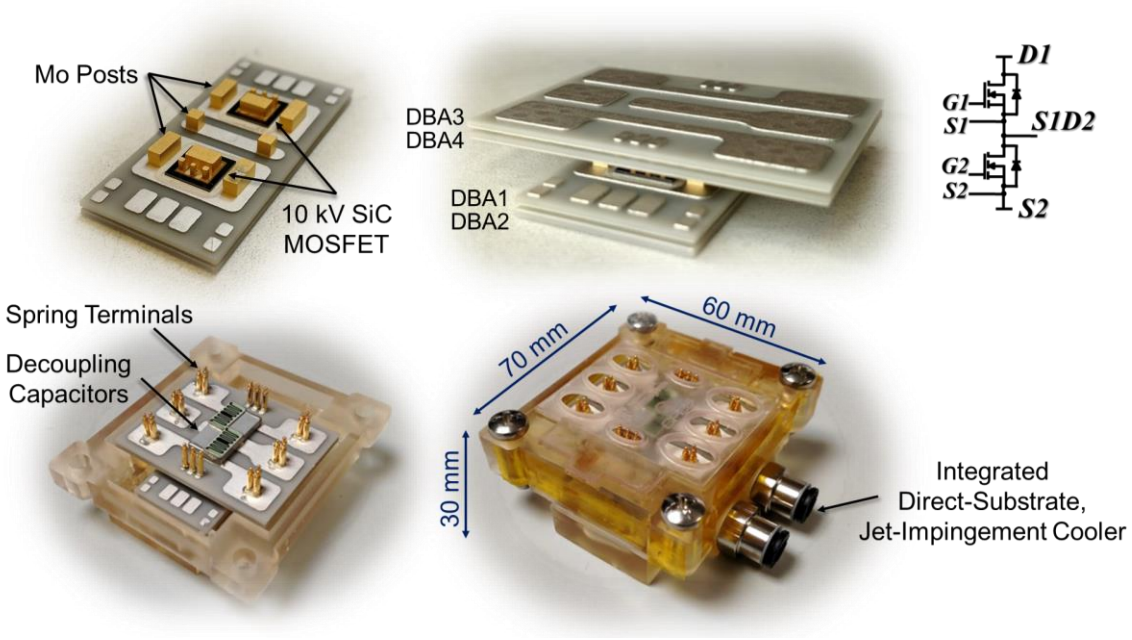
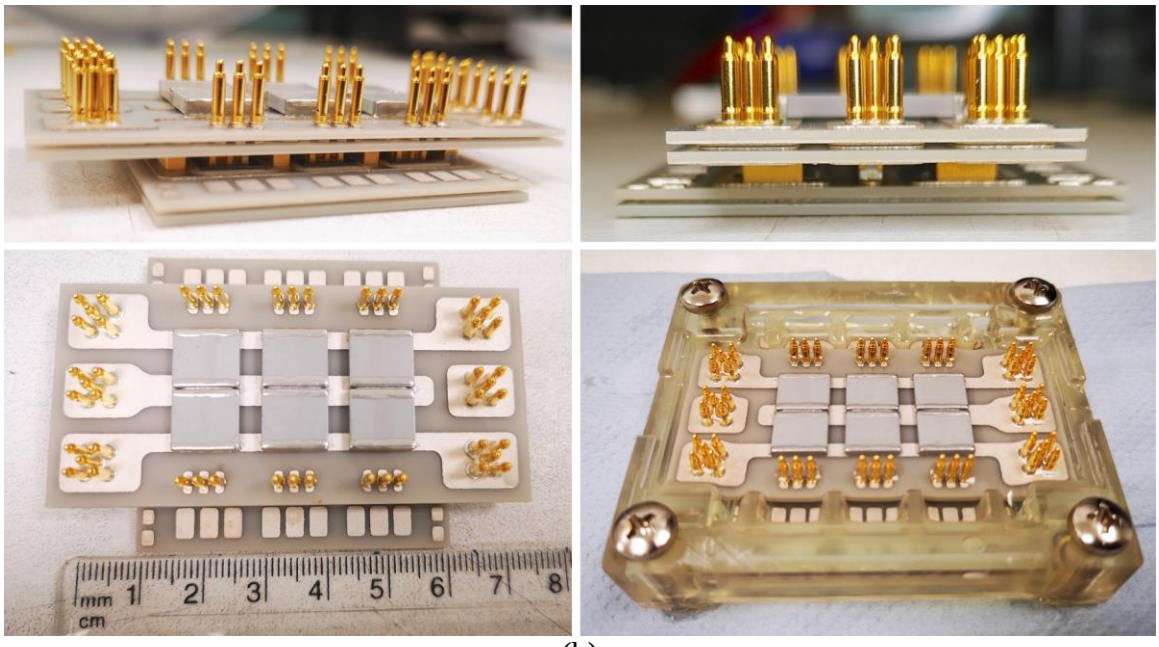



**Figure 4-15: The assembled 10kV module placed in its housing with the integrated cooler and jet-impingement cells [177].**

Figure 4-16 shows two module prototypes. To test the fabrication steps, semi-functional 10 kV SiC MOSFET dies were used. These dies, though functional (i.e., they could conduct current and block voltage), have characteristics outside of the manufacturer tolerances. Further, scaled-down modules with two dies (i.e., none in parallel) were also assembled and used for initial testing (Figure 4-16a). The testing of these module prototypes will be presented in the following sections.




(a)




(b)

**Figure 4-16: 10 kV SiC MOSFET module prototypes with (a) two dies (none in parallel), and (b) six dies (three in parallel per switch position). Images used with permission of Bassem Mouawad.**

## *4.3 Module Testing*

Once the modules are fabricated, they undergo a series of static and dynamic characterization tests to evaluate the electrical performance. PD tests were also performed on the module subcomponents (e.g., the DBA substrates, encapsulation, and gate driver PCB) in order to assess the high field strength performance. Finally, thermal characterization tests were performed on the full power module with the housing and integrated cooler to test the thermal performance. The detailed setups and results for each of the tests will be presented in the following subsections.

### *4.3.1 Static Characterization*

Prior to module fabrication, the 10 kV SiC MOSFET bare dies were tested with the Keysight B1505A curve tracer. To test the bare dies using the curve tracer's standard three-receptacle fixture (intended for use with 3-pin through-hole packages, such as TO-247), a special adapter was designed and built. The adapter and testing procedure are shown in Figure 4-17. This adapter allowed for accurate, high-current (20 A) tests that would be difficult to achieve with a traditional probing station. The adapter was 3D printed and the Cu leads were machined. Springs with 10 A current capacity were used to contact the die pads. The springs were soldered onto the Cu leads, which were inserted into the 3D printed housing. The die is placed in a cut-out in one of the housing pieces, and then a second housing piece is flipped on top of the die. The two pieces are then clamped together on either side, compressing the springs, and resulting in low contact resistance for accurate static characterization measurements. At the time of this work, the dies were still going through the qualification process and therefore did not have a final datasheet. However, the

static characterization results were in good agreement with the preliminary datasheet provided by the die manufacturer. As can be seen from Figure 4-17, as expected for a SiC MOSFET, the 10 kV dies have symmetrical channel conduction in the first and third quadrants. Therefore, using synchronous rectification (instead of external SiC Schottky diodes) will result in low on-state losses.

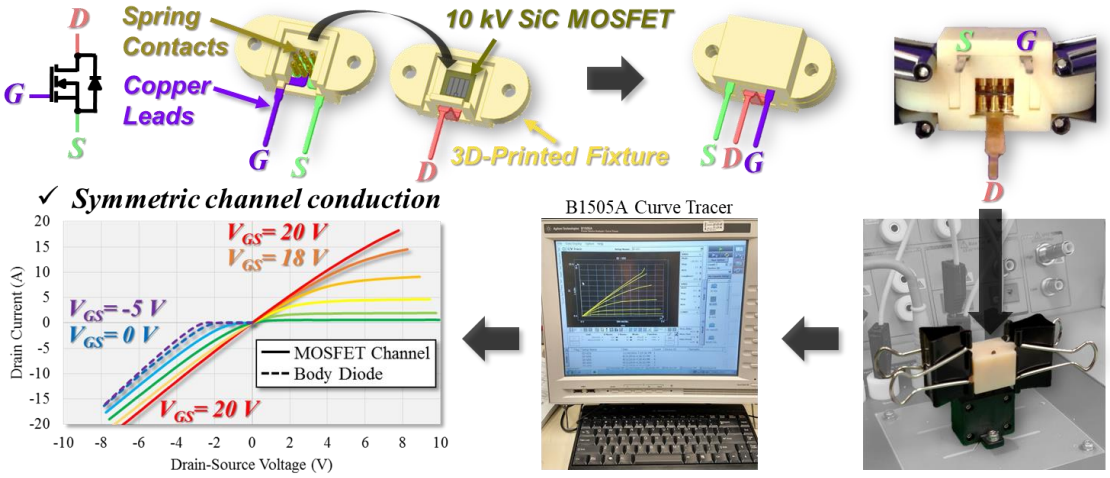



**Figure 4-17: Static characterization testing procedure for the 10 kV SiC MOSFET bare die using a 3D-printed adapter to interface to the curve tracer.**

Figure 4-18–Figure 4-22 show the static characterization for a 10 kV SiC MOSFET bare die at room temperature. Figure 4-18 shows the forward and reverse output characteristics for positive (10 V to 20 V) and negative (-5 V to -20 V) gate-source voltages. The dashed curves indicate that the current is being conducted through the SiC MOSFET internal body diode rather than the channel. As mentioned above, the MOSFET is turned on to conduct current in the reverse direction since the resistance of the MOSFET channel is lower than that of the internal body diode.

Figure 4-19 shows the on-resistance versus drain current for gate-source voltages of 18 V and 20 V. These gate-source voltages were selected because they are recommended for driving these 10 kV SiC MOSFETs. As expected, a gate-source voltage of 20 V results in a lower on-resistance. Specifically, a gate-source voltage of 20 V reduces the on-resistance by 4–6 %. This reduction increases as the drain current increases. Accordingly, 20 V will be used for the on-state driving voltage to reduce conduction losses. At 14 A and a gate-source voltage of 20 V, the on-resistance is 434 mΩ, which is below the maximum value of 450 mΩ that is specified in the preliminary datasheet. According to the preliminary datasheet, the typical on-resistance at 15 A drain current, 20 V gate-source voltage, and room temperature is 350 mΩ.

Figure 4-20 shows the transfer characteristics at drain-source voltages of 10 V, 15 V, and 20 V. The curves show that increasing the drain-source voltage increases the transconductance (i.e., the slope) for drain currents above 10 A. The transconductance at approximately 15 A is about 2.0, 3.6, and 4.0 for drain-source voltages of 10 V, 15 V, and 20 V, respectively. These values are similar to those of 1.2 kV SiC MOSFETs. According to the preliminary datasheet, the typical transconductance at 15 A and a drain-source voltage of 40 V is 4.8 at room temperature.

Figure 4-21 shows the drain current vs. gate-source voltage at a drain source voltage of 10 V at a lower drain current scale. This curve is used to determine the threshold voltage. If the threshold voltage is defined to be the gate-source voltage at which the drain current reaches 1 mA, then the threshold voltage would be 4.6 V. This threshold voltage is about double that of 1.2 kV SiC MOSFETs. This greater threshold voltage reduces the susceptibility to a false turn-on event, such as those caused by the Miller effect. In the

preliminary datasheet, the threshold voltage at a drain-source voltage of 10 V and drain current of 1 mA is 4.3 V.

Finally, Figure 4-22 shows the drain leakage current at a gate-source voltage of 0 V. The bare die cannot be tested beyond 2 kV in air because PD and arcing will occur due to the small chip size. Consequently, the breakdown voltage tests of the bare die prior to encapsulation were stopped at 1.5 kV for safety. The drain leakage current at 1.5 kV is 272 nA. While this leakage current is higher than that of 1.2 kV SiC MOSFETs, which typically have leakage currents in the low nanoamperes, it is reasonable for these 10 kV SiC MOSFETs. In the preliminary datasheet for the 10 kV SiC MOSFET dies, the specified maximum leakage current at 10 kV is 1000 µA. It can also be observed from Figure 4-22 that, unlike 1.2 kV SiC MOSFETs which have flat leakage current curves, the leakage current for the 10 kV SiC MOSFETs is quite linear. If this linear behavior continues, the leakage current at 10 kV would be approximately 56 µA, which is well below the maximum specified in the preliminary datasheet.

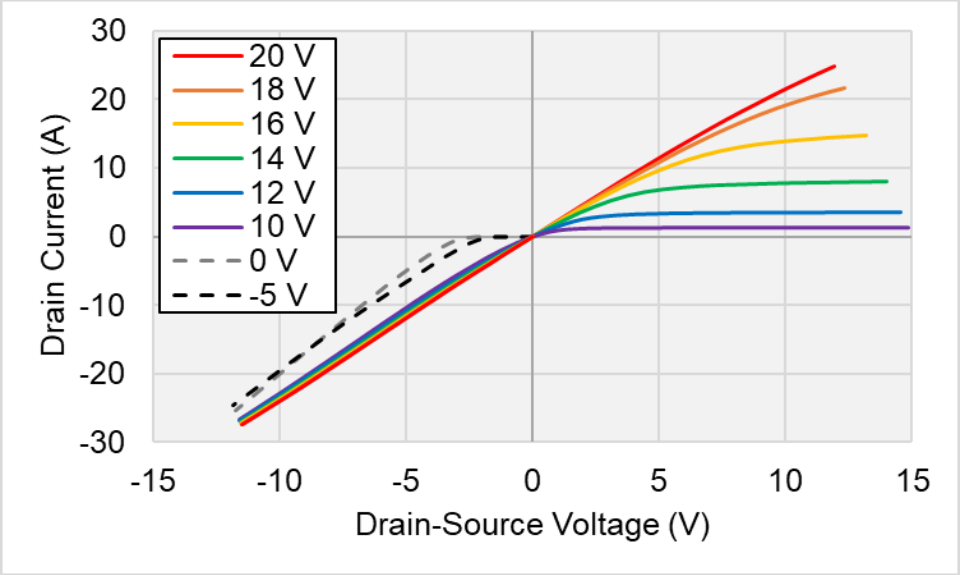



**Figure 4-18: Output characteristic curves for a 10 kV SiC MOSFET bare die at different gate-source voltages.**

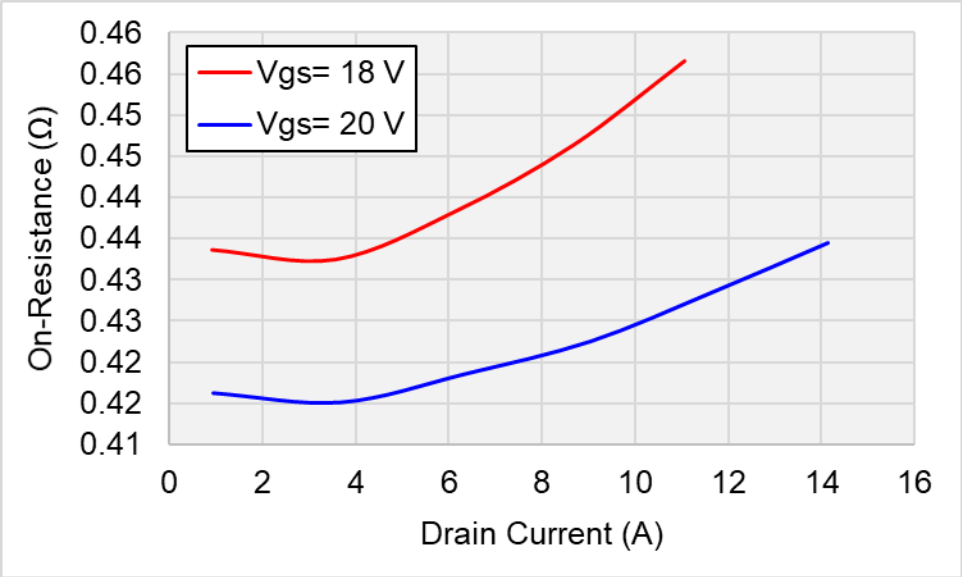



**Figure 4-19: On-resistance vs. drain current for a 10 kV SiC MOSFET bare die at gate-source voltages of 18 V (red) and 20 V (blue).**

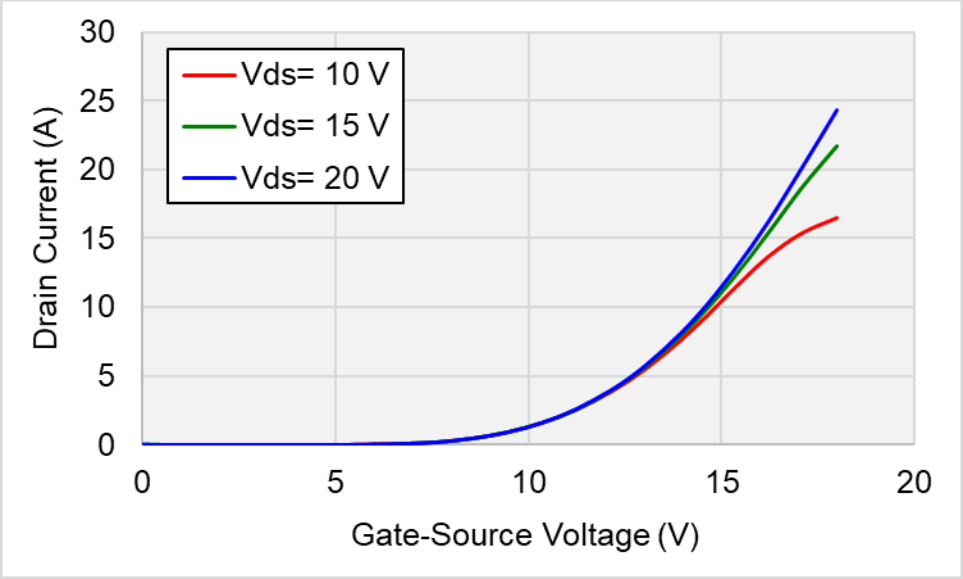



**Figure 4-20: Transfer characteristic curves for a 10 kV SiC MOSFET bare die at different drain-source voltages.**

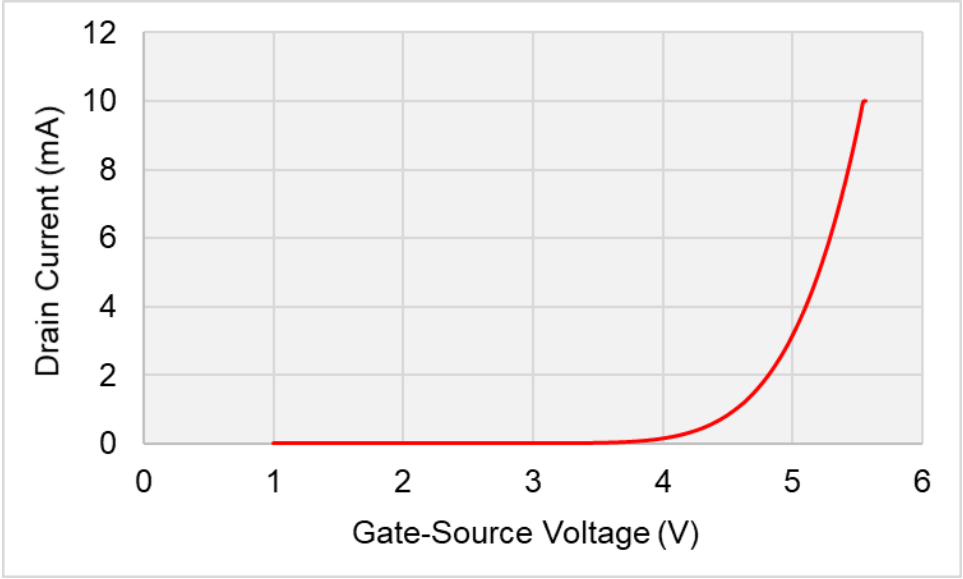



**Figure 4-21: Threshold voltage curve for a 10 kV SiC MOSFET when the drain-source voltage is equal to the gate-source voltage.**

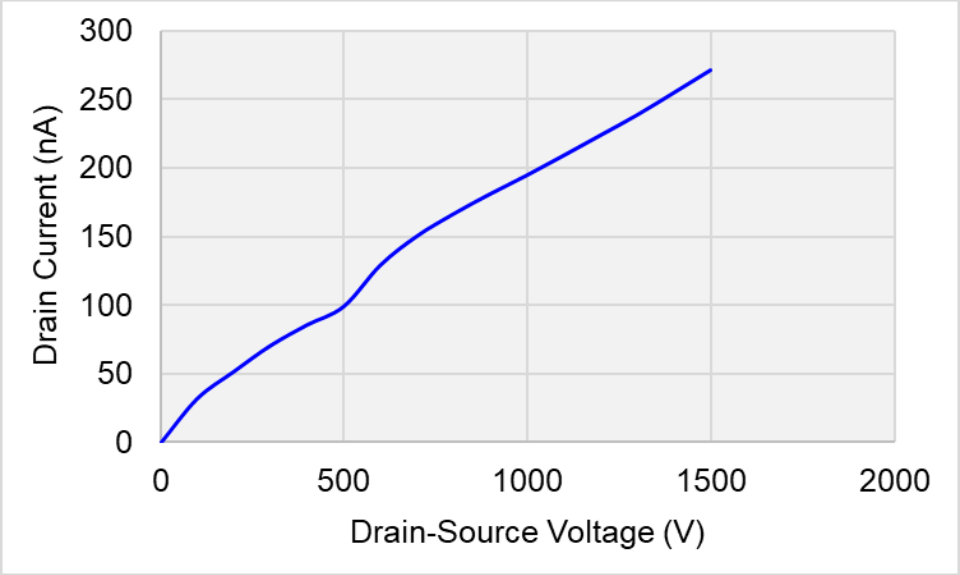



**Figure 4-22: Drain current leakage for a 10 kV SiC MOSFET bare die.**

After module fabrication, the static characterization was repeated and compared to those of the bare die. In the module shown in Figure 4-16a, two semi-functional SiC MOSFET dies were used. Figure 4-23 compares the breakdown voltages of these semi-functional SiC MOSFET dies before and after module fabrication. As can be seen from the figure, the leakage characteristics up to 1.5 kV did not increase after packaging. This indicates the processes and technologies used to assemble the module do not negatively impact the performance of the devices (up to 1.5 kV). The breakdown voltage of the module is greater than 10 kV, though the leakage current of the high-side MOSFET is 580 µA at 10 kV. This is higher than the fully-functional 10 kV SiC MOSFETs (Figure 4-22), but still below the maximum value of 1000 µA specified in the preliminary datasheet.

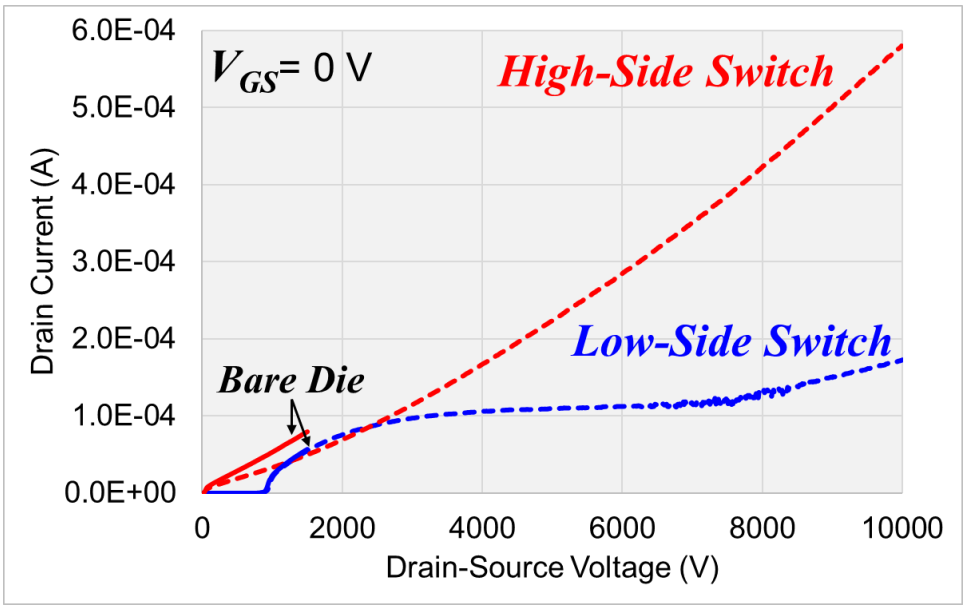



**Figure 4-23: Breakdown voltages for the semi-functinoal high-side (red) and low-side (blue) SiC MOSFETs before (solid curves) and after (dashed curves) module fabrication.**

### *4.3.2 Gate Driver Design*

In order to perform the dynamic characterization, a gate driver is needed for the 10 kV SiC MOSFETs. While there has been meaningful work published on the development of gate drivers for medium-voltage SiC transistors [36],[37],[38],[39], the drivers have only been designed for and demonstrated on low-current modules, typically consisting of just a single transistor. These gate drivers are also large in size, often several times larger than the module itself [36],[37],[38],[39]. In this work, a high-power-density, high-speed gate driver was developed and tested on Wolfspeed's first-generation 10 kV, 120 A SiC MOSFET module [34]. In this section, this gate driver, which was later adapted to be compatible with the planar 10 kV module proposed in this work, will be discussed. The target specifications for the gate driver will first be discussed, followed by the component

selection, design, and testing results. This work was previously published in [184], and is based on a similar design as that reported in [185].

In order to realize fast switching of the 10 kV MOSFETs, a high-speed gate driver with good *dv/dt* immunity and voltage isolation must be utilized. With this in mind, target specifications of the gate driver for the 10 kV, 120 A SiC module were developed. These specifications, which are in part based on the module datasheet parameters, are listed in Table 4-3.

**Table 4-3: Target Gate Driver Specifications**

| Specification | Influential MOSFET Parameters | Target | Purpose |
|---|---|---|---|
| Driving voltage range | Minimum and maximum gate-source voltage | -10 V / +20 V | Cross-talk immunity and low losses |
| Peak driving current | Maximum driving voltage range, total gate resistance, input capacitance | > 20 A | Small $R_{g,ext}$ for low switching loss and Miller effect |
| *dv/dt* immunity | Rise and fall times | > 80 V/ns | Low switching loss and EMI |
| Switching frequency | Parasitic capacitances | > 20 kHz | Reduce size of converter passive components |
| Isolation voltage | Leakage current and breakdown voltage | > 10 kV | Safety |

Isolation between the medium-voltage gate driver components and the lower-voltage control board is critical, especially when high *dv/dt* is expected. Fiber optic transmitters and receivers provide ample signal isolation for medium-voltage and high *dv/dt* applications. Thus, although they are more expensive and have a larger footprint than digital isolators, they have been selected for this application. The power supplied to the gate driver should also be isolated. This can be realized with on-board isolated dc–dc

converters. The target specifications for this isolated power supply are listed in Table 4-4. The supply should have wide input and output voltage ranges to suit the gate driving voltages for the 10 kV SiC MOSFETs (Table 4-3), isolation voltage greater than that of the module, low isolation capacitance to minimize the CM current due to the high *dv/dt* transients, and sufficient power rating for high switching frequency operation.

At the time of this work, only one company, RECOM Power, sold power supplies with 10 kV isolation. The REC6/R series of dc–dc converters from RECOM Power offer 10 kV dc reinforced isolation with sufficient power rating (6 W) and wide input voltage ranges [186]. The selected power supply has an output voltage of +24 V. Consequently, the sum of the on-state and off-state driving voltages of the MOSFETs will be limited to 24 V. While these specifications meet the targets, the isolation capacitance does not. The isolation capacitance for this power supply is 20 pF [186]. Since it is expected the 10 kV SiC MOSFETs will switch with high *dv/dt*, this capacitance could be a path for undesirable CM current.

Alternatively, an isolation transformer could be custom-designed and built, as was done [36],[39]. This approach would provide more flexibility in terms of the isolation voltage, isolation capacitance, and driving voltages. However, the need for ancillary components, such as drivers and rectifiers, results in added complexity, and potentially a larger footprint, compared to using an off-the-shelf isolated dc–dc converter. Accordingly, the RECOM power supply was selected for the gate driver, and CM chokes were added to help suppress the CM current.

**Table 4-4: Target Power Supply Specifications**

| Specification | Influential Parameters | Target |
|---|---|---|
| Maximum output voltage range | Minimum and maximum MOSFET gate-source voltage | -10 V / +20 V |
| Isolation voltage | Module voltage rating | > 10 kV |
| Isolation capacitance | Module *dv/dt* | < 2 pF |
| Power rating | Switching frequency, module gate charge, and MOSFET gate-source voltage range | > 4 W |

Additionally, it is desirable for the gate driver to have under-voltage lockout (UVLO), overcurrent protection, soft turn-off, and active Miller clamping. The UVLO prevents insufficient voltage from driving the SiC MOSFET module. The overcurrent protection limits the current through the devices. In order to ensure the MOSFET drain current remains within the safe operating range of the module, the overcurrent protection must have a quick response time. When the overcurrent protection is triggered, the driver should turn off the device slowly such that the overvoltage (caused by parasitic inductance in the module and surrounding circuitry) is kept within a safe range. Finally, active Miller clamping should be employed in order to prevent false turn-on of the MOSFET due to the Miller effect.

To implement the protection features listed previously, it is preferable to use a gate driver IC as it has higher power density and lower cost than a discrete solution. These ICs are typically isolated, thereby further enhancing the noise immunity of the gate driver. A survey of commercial gate driver ICs was performed. The main characteristics of interest include: peak output current $I_{peak}$, propagation delay time to high $t_{PLH}$ and low $t_{PHL}$ output levels, rise $t_r$ and fall $t_f$ times, desaturation sense to low propagation delay time $t_{desat(low)}$, and desaturation threshold $V_{desat(th)}$. Table 4-5 lists these parameters for commercial gate

driver ICs. All of these ICs are isolated, feature a wide supply voltage range, and offer the desired functions listed above.

For the overcurrent protection, all of the listed ICs use desaturation detection. During a short-circuit event, the high current flowing through the device will cause it to go into desaturation mode. If the drain-source voltage exceeds the desaturation threshold of the IC while the switch is turned on, then the fault detection will be triggered. The IC will then softly turn off the device, and send a fault output to the control.

According to the specifications determined in Table 4-3, none of the gate driver ICs listed in Table 4-5 satisfy the peak output current requirement (> 20 A). However, a current booster can be connected to the output of the gate driver IC in order to increase the output current and thus the driving speed. With this in mind, the STMicroelectronics STGAP1AS was selected because of its short and symmetrical propagation delays and rise and fall times, and its fast desaturation response.

**Table 4-5: Survey of Commercial Gate Driver ICs**

| **Manufacturer** | **Part No.** | $I_{peak}$ | $t_{PLH}$, $t_{PHL}$ | $t_r$, $t_f$ | $t_{desat(ow)}$ | $V_{desat(th)}$ |
|---|---|---|---|---|---|---|
| Avago | ACPL-331J | 1 A | 180 ns | 50 ns | 250 ns | 6.5 V |
| Fairchild | FOD8318 | 3 A | 300 ns, 250 ns | 34 ns | 850 ns | 7 V |
| ROHM | BM6102FV-C | 5 A | 150 ns | 50 ns | 3000 ns | Config. |
| STMicro-electronics | STGAP1AS | 5 A | 100 ns | 25 ns | 150 ns | 3~10 V |
| Toshiba | TLP5214 | 5 A | 85 ns, 90 ns | 32 ns, 18 ns | 200 ns | 6.5 V |

Although the desaturation threshold for the STGAP1AS is the highest of the surveyed ICs, a higher threshold is preferred. For instance, at 125 ºC, a desaturation threshold of 10 V could cause the protection to trigger at 100 A (after the blanking time

has elapsed). Considering that a high-voltage desaturation diode is also needed (or several low-voltage diodes in series), the on-state voltage at which the protection will trigger could be 6 V or lower. After a survey of high-voltage diodes, it was determined that putting three 3.3 kV SiC Schottky diodes, each with a forward voltage of 2.2 V, in series would give the highest on-state voltage (10 V - 3 × (2.2 V) = 4.9 V). This means, at 125 ºC, the protection could trigger at approximately 60 A. On the other hand, at 25 ºC, the protection could trigger at approximately 130 A. This is due to the temperature dependence of the SiC MOSFET I-V curve. Thus, in future revisions a discrete desaturation detection circuit, or a different overcurrent protection method, should be used. However, both of these options may increase the size of the gate driver.

A block diagram of the 10 kV gate driver circuit design is shown in Figure 4-24. The different background colors indicate the isolated planes of the PCB. The board is powered by 48 V. There is an isolated dc–dc converter that converts this 48 V into an isolated 24 V rail. The 24 V is then split into the desired on-state (+18 V) and off-state (-6 V) driving voltages using a Zener diode; alternatively, two linear dropout regulators (LDO) could be used. Another isolated dc–dc converter (with a smaller power rating and lower isolation voltage) is then used to convert the isolated 24 V to the 3.3 V needed to supply the gate driver IC, microcontroller (MCU), and fiber optic transmitter and receiver.

The output of the gate driver IC feeds into the current boosters (not shown), which connects to the gate and source terminals of the high-side and low-side switches. Three 10 A current boosters are connected in parallel to give a peak output current capability of 30 A for faster switching of the MOSFETs. The gate driver IC senses faults on the module.

When a fault is detected, the gate driver IC sends a signal to the fiber optic transmitter to communicate with the controller.

When designing the PCB, care was taken to minimize common- and differential-mode noise. CM chokes are placed before the dc–dc converters in order to reduce the CM noise, and decoupling capacitors are used throughout to attenuate high-frequency noise. Planes were used for the ground signals of the MOSFETs in order to ensure constant potential. To minimize noise coupling, no traces were routed underneath the dc–dc converter or gate driver IC isolation barriers, and overlap between the isolated and non-isolated (i.e., input signals from the controller) traces were avoided, when possible.

Additional consideration was needed in the PCB design to ensure the required creepage and clearance distances were met. According to the IPC-2221B Generic Standard on Printed Board Design [187], external, internal, and coated traces with a potential difference of 10 kV should be spaced a minimum of 50 mm, 24 mm, and 29.78 mm apart, respectively. According to the UL-840 Insulation Coordination Including Clearances and Creepage Distances for Electrical Equipment, the minimum clearance distance for electrical equipment rated at an impulse withstand voltage peak of 12 kV is 14 mm [109]. The minimum creepage distance is 100 mm for material group IIIa,b (e.g., FR4) and pollution degree 2 (normally non-conductive pollution with some temporary conductivity caused by condensation) [109]. Consequently, it becomes difficult to achieve a high-density design. To avoid these restrictions, the exposed conductors (e.g., the through-hole leads of the RECOM power supply that provides the high-voltage isolation) can be coated with an insulating material such as Super Corona Dope. Slots can also be cut in the PCB to increase the creepage distance.

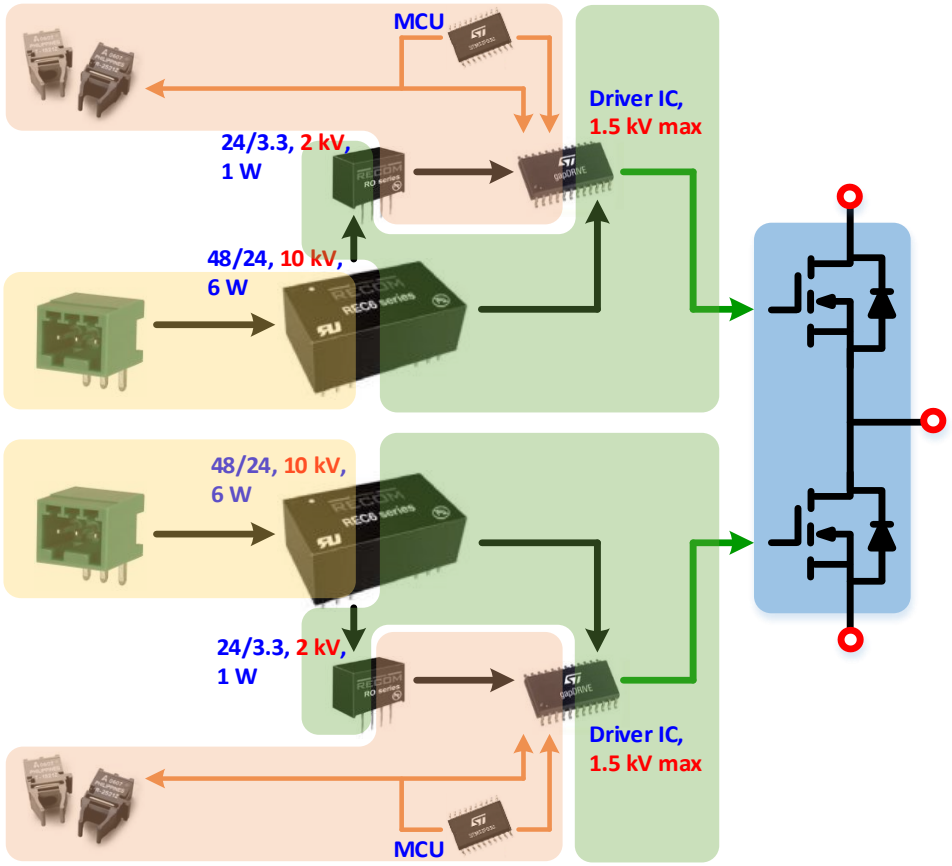



**Figure 4-24: Block diagram of the 10 kV gate driver. The background colors indicate the isolation planes.**

The constructed gate driver is shown in Figure 4-25 with the key components labeled. Unlike in previous reports [36],[37],[38], which use long wires to connect the gate driver to the SiC module, in this work, care has been taken to minimize the stray inductance in the gate-loop in order to improve the switching performance. This means, in addition to having an optimized loop on the gate driver board itself, the gate driver must also be in close proximity to the module, and suitable connectors should be used. In this work, the gate driver is placed directly on top of the module in order to achieve a small gate loop. As shown in Figure 4-25, a press-fit connector is used, which provides good mechanical support for the gate driver PCB, as well as easy connection. The gate driver dimensions

are 122 mm × 62 mm. For reference, Wolfspeed's first-generation 10 kV SiC module dimensions are 187 mm × 137 mm.

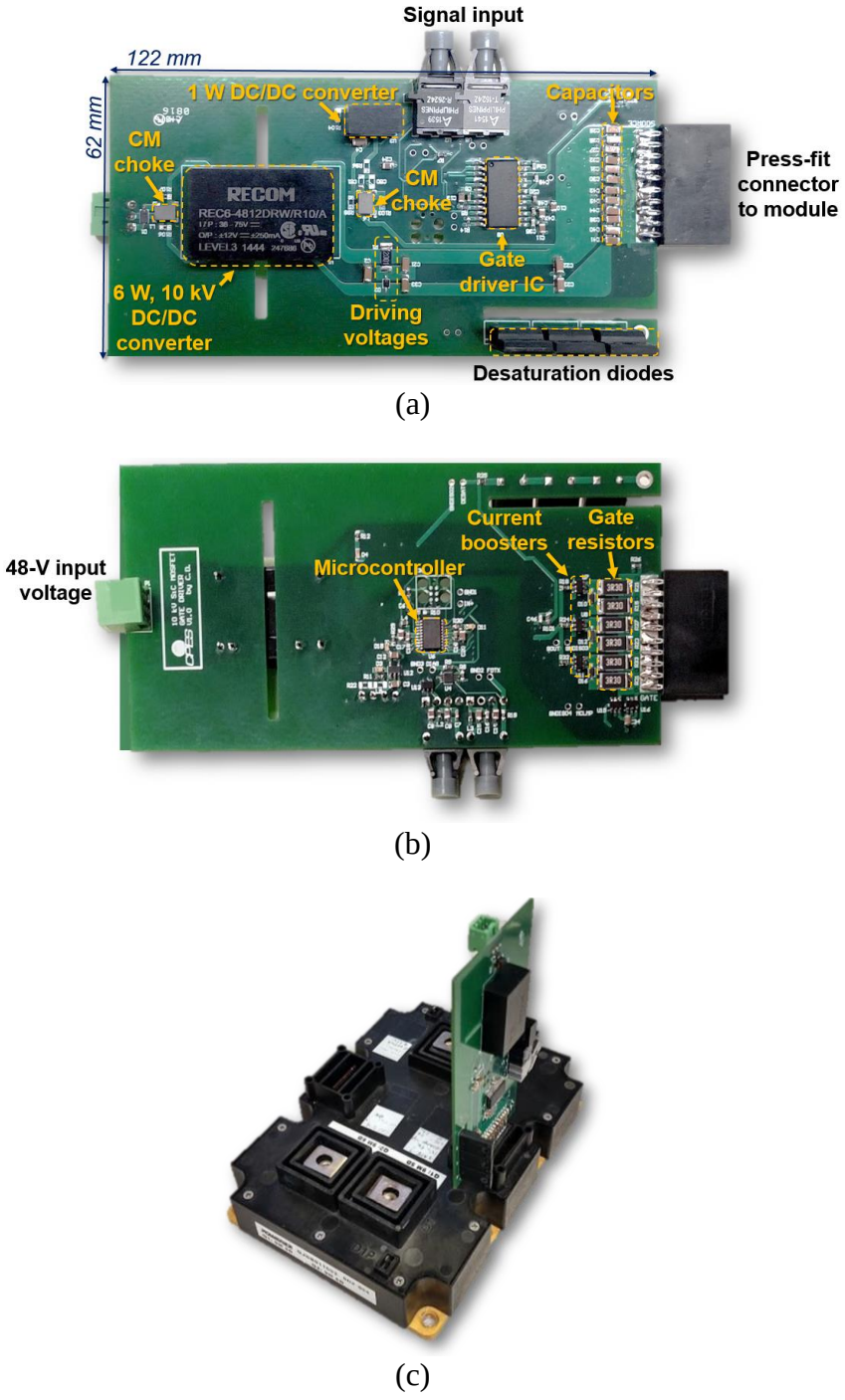
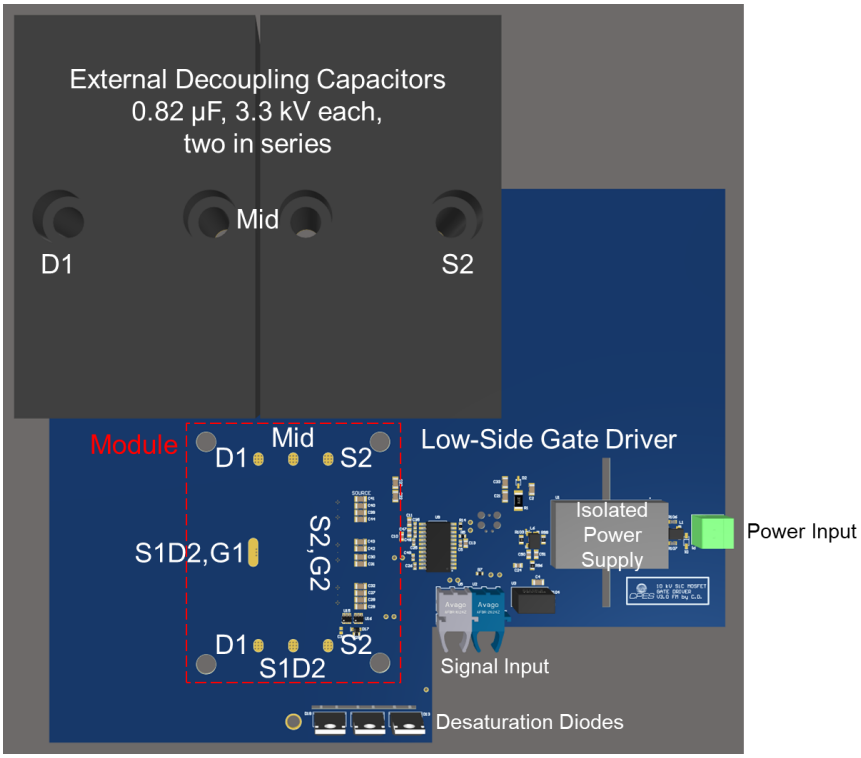


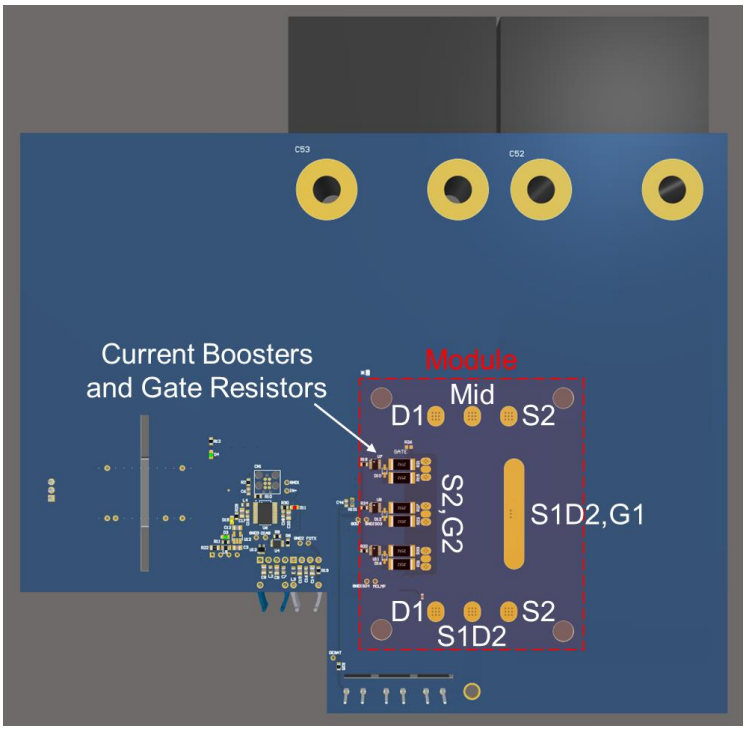

**Figure 4-25: (a) Top and (b) bottom view of the designed gate driver for (c) the first-generation 10 kV, 120 A SiC MOSFET module.**

### *4.3.3 Interface PCB with Gate Driver*

The footprint of the gate driver described in the previous section was adapted to fit the proposed planar 10 kV SiC MOSFET module. To test the fabricated module, the PCB must have a PDIV and breakdown voltage greater than 6 kV. Electrostatic simulations were performed using ANSYS Maxwell to develop a PCB layout that would have low electric field strength in the air. This was a major focus since, as mentioned previously, air has a low breakdown field strength of just 3 kV/mm. As described in the previous chapter, to reduce the electric field strength in the air, it is proposed to use field-grading plates in the PCB that compresses the springs. A series of 2D and 3D electrostatic simulations were performed to determine the track and field-grading plate locations, shapes, and dimensions. The final PCB with the gate driver and bus bar for external decoupling capacitors is shown in Figure 4-26 and Figure 4-27. It is a 4-layer PCB with a thickness of 2.36 mm (0.093 in). The PD testing of the designed PCB will be discussed in a later section.




(a)




(b)

**Figure 4-26: 3D model of DPT PCB (a) top view, and (b) bottom view.**

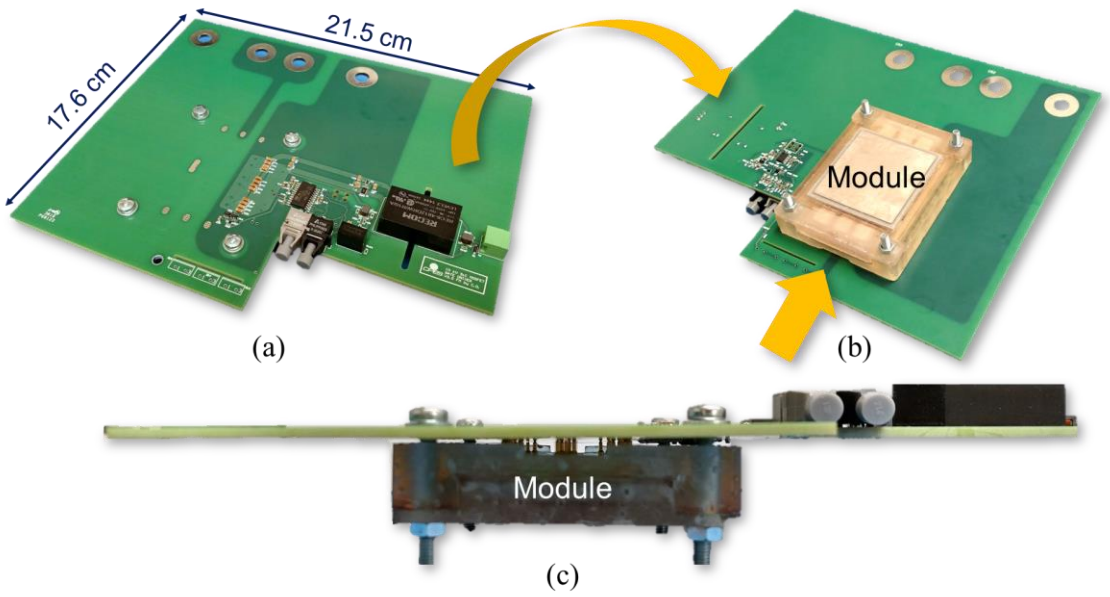
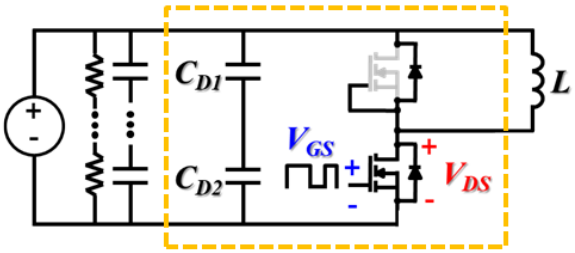



**Figure 4-27: (a) Top view, (b) bottom view, and (c) side view of the DPT PCB with module attached.**

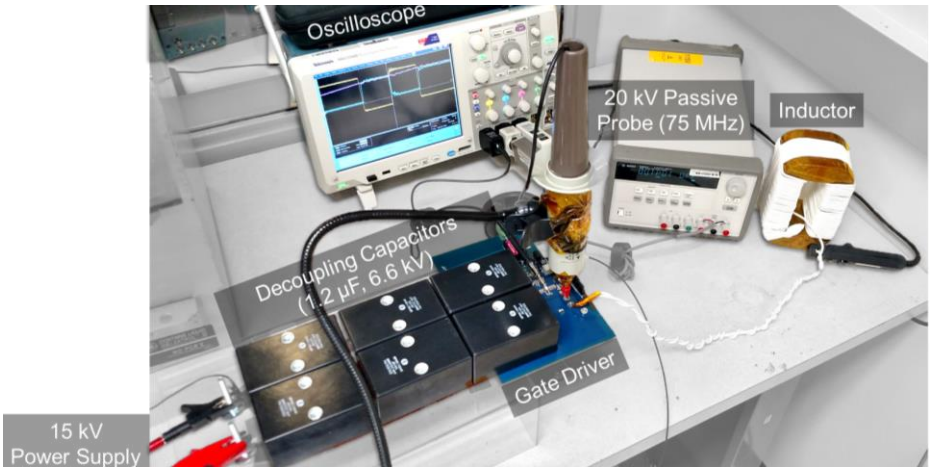
### *4.3.4 Double-Pulse Test Setup*

Double-pulse tests (DPT) were performed on the fabricated module shown in Figure 4-16a to evaluate its switching performance. The DPT schematic and setup are shown in Figure 4-28. The gate-source and drain-source voltages of the low-side SiC MOSFET were monitored using a 300 V passive probe with a bandwidth of 1 GHz, and a 20 kV passive probe with a bandwidth of 75 MHz, respectively. As shown in Figure 4-28b, these probes are placed directly above the MOSFET terminals in order to minimize the parasitic inductance in the measurement loop. Due to the embedded decoupling capacitors, the drain current of the SiC MOSFETs could not be measured. A 15 kV power supply was used to charge the external decoupling capacitors. The external decoupling capacitors are film capacitors that were donated in-kind from Electronic Concepts. Each capacitor is 0.82 µF and rated at 3.3 kV (MP80CV824K [188]). Six total capacitors were used—two in

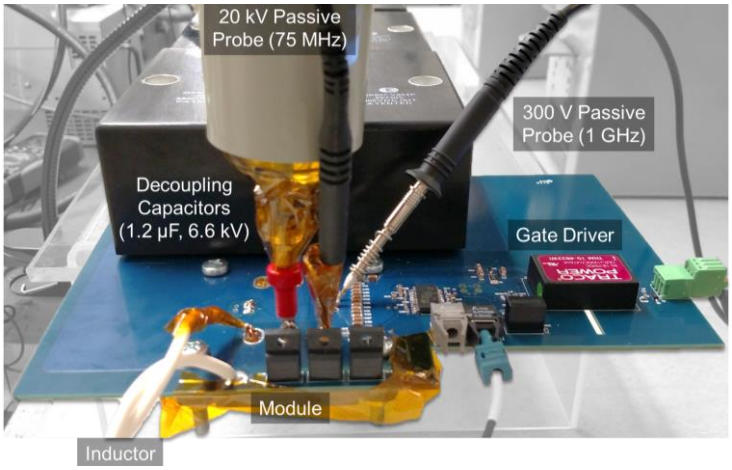
series and three in parallel for a total capacitance of 1.2 µF and voltage rating of 6.6 kV. Three capacitors were put in parallel to increase the capacitance and to reduce the inductance; each capacitor has an equivalent series inductance of 30 nH [188].




(a)




(b)




(c)

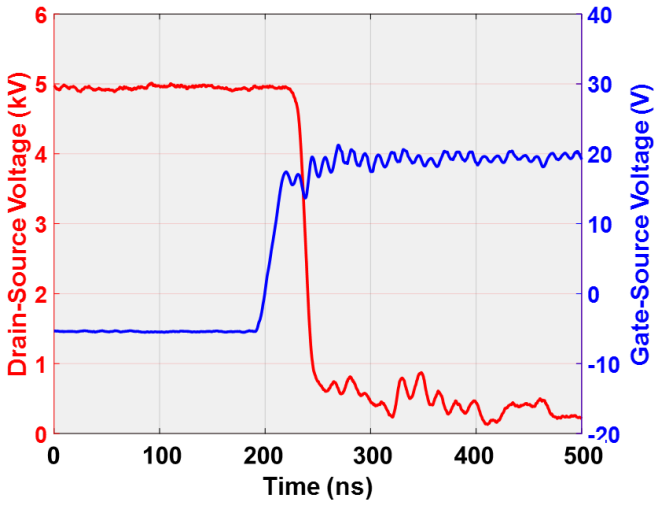
**Figure 4-28: Double-pulse test (a) schematic, (b) hardware setup, and (c) module connection.**

### *4.3.5 Dynamic Characterization*

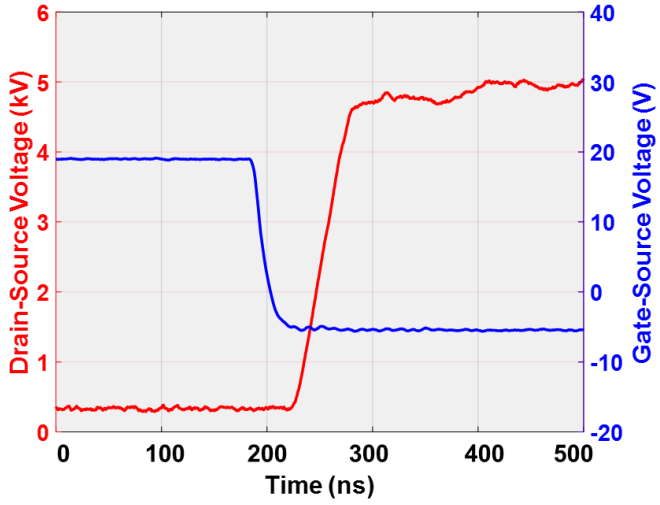
Figure 4-29 shows the gate-source and drain-source voltage waveforms for the turn-on and turn-off transients for the DPTs performed on the module shown in Figure 4-16a, which has two semi-functional SiC MOSFETs. The switching tests were performed up to 5 kV and 20 A with turn-on and turn-off gate resistances of 0.33 Ω and 0.17 Ω, respectively. As can be seen from the figure, the low inductances from careful power module and PCB layout designs resulted in minimal oscillations and voltage overshoot. Table 4-6 lists the overshoot, undershoot, rise and fall times, and switching rates from the DPT waveforms. During the turn-on transient, the fall time from 90 % to 10 % of the drain-source voltage is 13 ns, giving a *dv/dt* of 260 V/ns. At turn-off, the voltage rise time is 45 ns, which is a *dv/dt* of 83 V/ns. The voltage rise time is longer because it is controlled by the output capacitance and load current. Negligible voltage overshoot and ringing were measured, indicating low power- and gate-loop inductances. This is due to the low-inductance module design, as well as good layout and connection of the gate driver, bus bar, external decoupling capacitors, and measurement probes.

To the best of the author's knowledge, these are the fastest switching speeds reported for similarly-rated SiC MOSFETs and IGBTs. In fact, this is more than two times faster than those reported in [35],[108],[114],[189]. Specifically, Wolfspeed's switching results for a module populated with a single die had turn-on and turn-off transition times of approximately 80 ns and 120 ns, respectively, giving switching speeds of 88 V/ns and 58 V/ns at a bus voltage of 7 kV, drain current of 15 A, and gate resistance of 21 Ω [108]. The switching waveforms also showed a moderate voltage overshoot of approximately 300 V (4.3 %) [108].

For a discrete 4 kV silicon IGBT, the datasheet reports voltage rise and fall times of 146 ns and 514 ns at 1.25 kV, 30 A, and 2 Ω external gate resistance [190]. These switching times result in *dv/dt* values of 8.6 V/ns and 2.4 V/ns for the rise and fall, respectively, which are 10 and 100 times slower than the switching speeds achieved in this work. Accordingly, the proposed power module can enable faster-switching, higher-voltage power converters while maintaining high efficiency.




(a)




(b)

**Figure 4-29: (a) Turn-on and (b) turn-off gate-source (blue, right axis) and drain-source (red, left axis) voltages.**

**Table 4-6: 10 kV, 350 mΩ SiC MOSFET Module Prototype DPT Results**

| Parameter | Value | |
|---|---|---|
| | ***Gate-Source Voltage*** | ***Drain-Source Voltage*** |
| Overshoot | None | None |
| Undershoot | None | None |
| Rise time* | 20 ns | 45 ns |
| Rise *dv/dt* | 0.96 V/ns | 83 V/ns |
| Fall time* | 21 ns | 13 ns |
| Fall *dv/dt* | 0.93 V/ns | 260 V/ns |

*Parameter measured from 10 % to 90 % of the steady-state value.

### *4.3.6 Thermal Characterization*

To evaluate the performance of the integrated direct-substrate, jet-impingement cooler, thermal impedance measurements were carried out on a Mentor Graphics Power Tester [191]. The measured specific thermal resistance at different flow rates is shown in Figure 4-30 for the module prototype shown in Figure 4-16a. The lowest junction-to-ambient specific thermal resistance of the module was measured to be 26 $mm^2 \cdot K/W$ (0.38 K/W) for a flowrate of 0.47 l/min. This value is lower than the results using a stacked substrate structure reported in the literature [192].

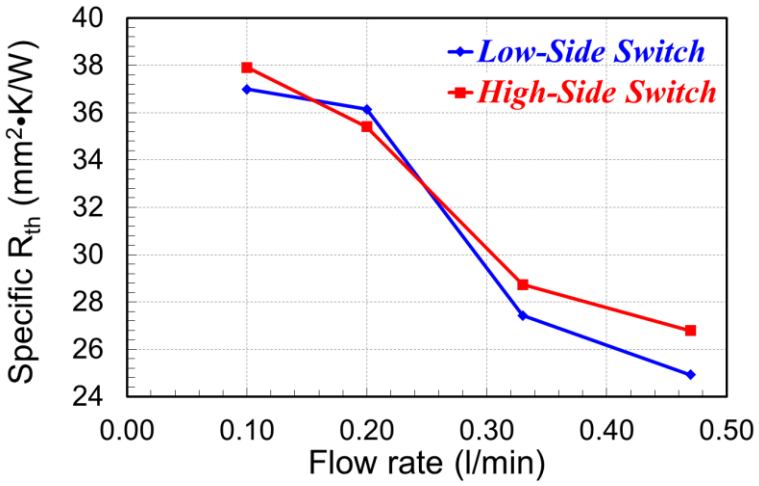



**Figure 4-30: Specific thermal resistance versus flow rate for the high-side (red) and low-side (blue) SiC MOSFETs.**

### *4.3.7 Partial Discharge Characterization*

PD tests were conducted to validate the electrostatic ANSYS Maxwell simulation results. The PD tests were performed using a 50 kV, 100-mA, 60-Hz ac power supply as the excitation source. To detect the PD events, a Doble PD Smart with the HFCT-300 sensor was used [193]. The Doble PD Smart complies with IEC 60270, VDE 0434, and various other standards [193]. It measures both the PD and the applied voltage under test [193]. The frequency range for the test voltage is 20 Hz–1.2 kHz [193]. For the PD, signals from 35 kHz to 20 MHz can be measured [193]. The lowest detectable apparent charge is 0.2 pC [193].

PD tests of a patterned, 1-mm-thick AlN-DBA substrate were performed. From the PD testing, it was revealed that, as was shown in the electrostatic simulations, the PD for the DBA substrates will occur at the triple points. Specifically, the PD will take place along the edge of the metal pad(s) where the high potential is applied. Three cases were tested:

1) a single substrate, 2) two stacked substrates with the middle metal left floating, and 3) two stacked substrates with the middle metal connected to half of the applied excitation voltage.

First, the PD tests were performed with the samples in air in order to have a high signal-to-noise ratio. The resulting PDIV for the three cases when the samples are tested in air are shown in Table 4-7. Each case was tested under two conditions: 1) S1D2= D1 (i.e., the high-side switch is conducting and the low-side switch is blocking), and 2) S1D2= S2 (i.e., the high-side switch is blocking and the low-side switch is conducting). The sample under test is shown in Figure 4-31. When S1D2 is equal to D1 (i.e., the applied voltage), the PDIV increases by 23.5 % when the two substrates are stacked together and the middle metal is left floating compared to the single substrate case. When the middle metal is connected to half of the applied voltage, the PDIV increases by 53 % compared to the single-substrate case [194].

When S1D2 is equal to S2 (i.e., the ground), the PDIV remained unchanged when the two substrates are stacked together and the middle metal is left floating compared to the single substrate case. This result suggests that the middle metal floated to a potential close to 0 V. This is due to the different potentials on the topside metal; the D1 and S1D2 pads, which are the same size, are equal to the applied voltage and ground (bottom metal potential), respectively. As a result, the middle metal will float to a potential that is closer to that of the S1D2 and S2 pads. The capacitances across the top and bottom substrates in the stack form a capacitive voltage divider. From this voltage divider, the potential of the middle metal layer will float to approximately 0.31 kV rms, which is one-seventh of the applied excitation voltage (2.2 kV rms). This case was also simulated in ANSYS Maxwell.

The simulated potential of the middle metal layer for an applied voltage of 2.2 kV was 0.32 kV, which is 3 % higher than the calculated value.

On the other hand, when the middle metal was connected to half of the applied voltage, the PDIV increased by 53 %, which is in good agreement with the simulation result. Therefore, it is not advised to leave the middle metal floating, as its potential will depend heavily on the switching state. Instead, it is recommended to connect the middle metal to half of the bus voltage, as this increases the PDIV and gives predictable, consistent results for both switching states.

Since the power module will be encapsulated, tests were also performed on a stacked substrate sample that was encapsulated with SilGel 612 from Wacker. The PDIV results for the three cases when this sample is encapsulated are shown in Table 4-7. By connecting the middle metal to 0 V, the electric field distribution is nearly the same as that for a single substrate. As can be seen from the table, there is only a 2.7 % increase in the PDIV when the middle metal is left floating and S1D2 is equal to S2 (the worst-case). However, when the middle metal is connected to half of the applied voltage, no PD could be measured up to 10.5 kV rms (14.8 kV peak). The testing setup was limited to 10.5 kV rms due to the voltage rating of the capacitors used to connect the middle metal to half of the applied voltage. Moreover, when the middle metal was connected to 0 V, breakdown occurred at 8.5 kV rms (12.0 kV peak). This means when a single substrate is used, there is little margin between the breakdown voltage and the voltage rating of the 10 kV SiC MOSFETs. Therefore, it is advantageous to use the stacked substrate structure with the middle metal connected to half the applied voltage in order to increase the safety margin.

This connection also decreases the CM current that flows through the system ground. This screen will be discussed in detail in the following chapter.

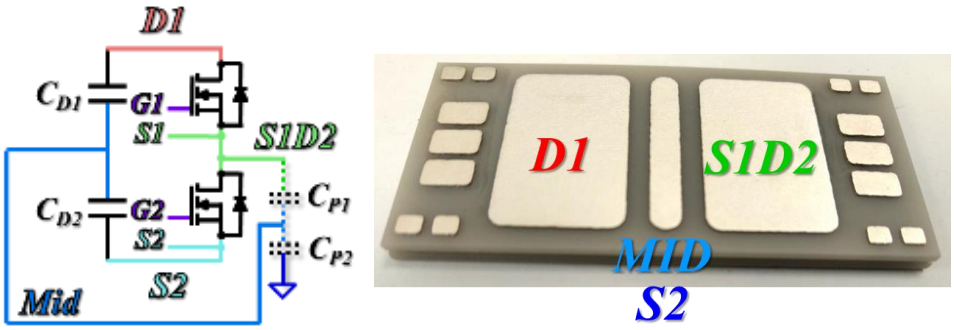



**Figure 4-31: PD testing sample.**

**Table 4-7: Partial Discharge Testing Summary**

| Sample | Voltage of Middle Metal | Environment | S1D2 Potential | PDIV (rms) |
|---|---|---|---|---|
| Single substrate (DBA1 only) | N/A | Air | D1 | 1.7 kV |
| | N/A | Air | S2 | 1.7 kV |
| Stacked substrates (DBA1 + DBA2) | Floating | Air | D1 | 2.1 kV |
| | Floating | Air | S2 | 1.7 kV |
| | 1/2 × $V_{AC}$ | Air | D1 | 2.6 kV |
| | 1/2 × $V_{AC}$ | Air | S2 | 2.6 kV |
| Encapsulated stacked substrates | 0 V | SilGel 612 | S2 | 7.4 kV |
| | Floating | SilGel 612 | S2 | 7.6 kV |
| | 1/2 × $V_{AC}$ | SilGel 612 | S2 | >10.5 kV |

PD tests were also performed on the PCB developed for the DPTs. Since the PCB will be in the air during the DPTs, the PD tests were too conducted in air. As mentioned earlier, field-grading plates were included inside the PCB to reduce the electric field strength in the air. The final PCB design has a PDIV of 6 kV rms (8.5 kV peak) when S1D2 is connected to S2, and 6.9 kV rms (9.8 kV peak) when S1D2 is connected to D1. The PDIV is lower for the case when S1D2 is equal to S2 because the high-side gate-source is

in close proximity to the D1 terminal. Accordingly, there is high electric field strength between the high-side gate-source and the D1 traces.

Without the field-grading plates, and with overlapping D1 and S2 traces (to reduce the power-loop inductance), the PDIV was only 1.2 kV rms (1.7 kV peak) for both switching state cases. When tested in oil, the PDIV for this PCB increased, indicating that the PD was occurring at the surface (known as a surface discharge). A silicone coating was applied to the PCB surfaces, and was shown to slightly improve the PDIV to approximately 1.4 kV rms (2.0 kV peak). However, including field-grading plates and avoiding overlapping D1 and S2 traces gave the greatest improvement, with five times higher PDIV.

Though, by not overlapping the D1 and S2 traces, the parasitic inductance of the power loop in the PCB increases from approximately 13 nH to 35 nH, according to ANSYS Q3D simulations. This increased inductance could impact the switching performance of the module (e.g., ringing and voltage overshoot). Thus far, the DPTs have been performed using the PCB with overlapping D1 and S2 traces, so it is unclear if and to what extent the larger power loop inductance of the PCB without the overlapping traces will impact the device switching waveforms.

Furthermore, it is expected the PDIV will increase when the module is connected, as this was how the PCB electrostatic performance was evaluated in the simulation. Unfortunately, this case cannot be tested with a real module and an ac excitation, as the body diodes of the MOSFETs will conduct. In the future, a module without MOSFETs could be fabricated to test the PDIV of the module and of the PCB with the module attached. The external decoupling capacitor board (underneath the capacitors shown in Figure 4-28b) was also tested in air, and was found to have a PDIV of approximately 6 kV

rms (8.5 kV peak). Therefore, using the gate driver PCB with the field-grading plates and non-overlapping D1 and S2 traces, and the external decoupling capacitor board, the power module can be safely switched with a dc bus of 7–8 kV without partial discharge.

## *4.4 Conclusion*

In this chapter, the procedures used to fabricate prototypes of the proposed module were presented. Specifically, the materials and processes for the substrate-substrate bonding, die attachment, post attachment, terminal attachment, and encapsulation were detailed. For the substrate-substrate bonding, reducing the sintering pressure to 1 MPa resulted in no cracks in the ceramic substrates while still maintaining a high quality bond with low voiding content and no notable defects. For the die and post attachments, both pressure-less and pressure-assisted Ag sintering procedures were evaluated. For the die attachment, using pressure-assisted Ag sintering resulted in higher shear strength compared to pressure-less sintering (25 MPa compared to 15 MPa, average). This could be due to the presence of Kirkendall voids as a result of the different diffusion rates of Ag and Au (the backside die metallization) [178]. By applying pressure, the voids are reduced.

The tops of the posts are attached to the top substrate stack with solder. Solder layers can be made thicker than sintered Ag, thus better compensating for differences in the post heights and/or bending of the substrates. Since Mo is not compatible with solder, coatings must be applied. Two types of posts were evaluated: 1) Cu-Mo-Cu laminate with Au plating, and 2) pure Mo with Ti/Ni/Ag plating. The Cu and Au in the former are well-suited for soldering. For the latter, the inclusion of a 1-μm-thick Ni diffusion barrier

improved the bonding strength of the soldered posts from less than 10 MPa to more than 30 MPa.

For the initial prototyping, scaled-down modules with two semi-functional 10 kV SiC MOSFETs each were fabricated. Upon successful fabrication of these smaller modules, the full-scale modules with six dies were prototyped. To test the switching performance of the module prototypes, a custom gate driver needed to be designed since there are currently no commercial gate drivers for 10 kV, high-speed power modules. The gate driver needs to have sufficient isolation voltage, low isolation capacitance to minimize CM current generated by the high *dv/dt* switching, and high output current to quickly charge the MOSFET input capacitances. The gate driver prototype uses a commercial dc-dc converter with 10 kV isolation, and an isolation capacitance of 20 pF. In future gate driver iterations, options with lower isolation capacitances should be explored. The gate driver also includes current boosters capable of providing a peak output current of 30 A.

The gate driver is mounted directly on top of the power module to maintain low gate- and power-loop inductances. Additional decoupling capacitors were also connected to the gate driver PCB to further improve the switching performance. DPTs at 5 kV and 20 A showed clean switching waveforms with little ringing and no measurable voltage overshoot, indicating low gate- and power-loop inductances in the module, gate driver, bus bar, and probe connections. The turn-on and turn-off switching times are 13 ns and 45 ns, respectively. The resulting switching rates are 260 V/ns and 83 V/ns, respectively. This turn-on *dv/dt* is more than two times faster than those reported for medium-voltage SiC MOSFETs or IGBTs [35],[108],[114],[189].

Finally, PD tests were presented for the module substrates and gate driver PCB. For the substrates, it was found that stacking two substrates and connecting the middle metal to half of the applied voltage increased the PDIV by 53 % compared to a single substrate case. When testing a single substrate encapsulated in silicone gel, breakdown occurred at just 8.5 kV rms (12.0 kV peak). This means when a single substrate is used, there is little margin between the breakdown voltage and the voltage rating of the 10 kV SiC MOSFETs. On the other hand, when stacking two substrates and connecting the middle metal to half of the applied voltage, the PDIV exceeded 10.5 kV rms. The PD tests were limited to 10.5 kV rms due to the testing setup. It was also evident that if the middle metal layer of the substrate stack was left floating, then the PDIV was close, and in some cases the same, as that for the single substrate case. Therefore, when using multiple substrates, it is highly recommended to connect the middle metal to half of the applied voltage in order to maximize the benefit.

For the gate driver PCB, it was found that when no field-grading plates were used and when the D1 and S2 traces were overlapped, the PDIV in air was just 1.2 kV rms. Clearly, this is not acceptable for a 10 kV SiC MOSFET module, as while the module may have sufficient PDIV, if the external circuitry does not, then the converter will not be able to operate safely and reliably at the rated voltage. Accordingly, the solution proposed in this work is to include field-grading plates and avoid overlapping of the D1 and S2 traces. This increases the PDIV by five times, to 6 kV rms (8.5 kV peak). However, by eliminating the overlap of the D1 and S2 traces, the parasitic inductance of the PCB is increased from approximately 13 nH to 35 nH, which could impact the switching performance of the module.

# Chapter 5 Analysis, Implementation, and Testing of an Integrated Common-Mode Screen

## *5.1 Introduction*

EMI arises from the voltage and current transitions occurring during operation of the switching cell, and can be conducted through the electrical connections, or radiated into the surrounding space. The usage of WBG semiconductors, which can have *dv/dt* orders of magnitudes higher than silicon devices, exacerbates the EMI. In Chapter 2, it was shown that the operation of a converter using Wolfspeed's first-generation 10 kV, 120 A SiC modules was limited due to significant CM current (Figure 2-12). As a reminder, spikes up to 100 A were measured flowing through the system ground. For perspective, the average inductor arm current was 100 A. This is clearly unacceptable, and needs to be addressed in order to utilize these exceptional devices at their full capability (i.e., without slowing them down).

The cause of the CM current is the high *dv/dt* that occurs when switching the 10 kV SiC devices. Possible paths for the CM current include the gate driver and the parasitic capacitance across the ceramic substrate. The former has been addressed in other work by reducing the isolation capacitance of the gate driver power supply [36],[37],[38],[39]. Little work has been done to mitigate the latter; therefore, the focus of this chapter will be on

reducing the CM current flowing through the parasitics associated with the module package.

It is especially important that this CM current is addressed in this work because the proposed planar 10 kV SiC MOSFET power module has a *dv/dt* that is more than an order of magnitude greater than that of the Wolfspeed first-generation module, which had a peak *dv/dt* of 22 V/ns. This higher *dv/dt* will result in substantially greater CM current. Moreover, since a major objective of this work is to create a high-density module, adding large external filters and screens at the converter and/or system level, which is common practice to reduce the EMI/meet the standards, would defeat the purpose. Instead, in this chapter, a method for containing CM current within the switching cell by integrating a screen inside the power module is proposed. Thus, the filtering requirements at the converter and/or system levels are reduced, which in turn decreases the overall size and weight.

## *5.2 Literature Review*

To address the issue of current flowing through the parasitic capacitance, Infineon patented a method for diverting the current back to the dc bus [78]. In the patent, the semiconductor dies are mounted to two insulating substrates, such as DBCs, which are stacked on top of each other. In this way, there are now effectively two parasitic capacitances in series, which results in a lower equivalent capacitance, thereby increasing the high-frequency impedance. Infineon proposed to connect the middle metal layer to either the positive or negative dc bus. In this way, the current that flows through the first

parasitic capacitance, $C_{P1}$, has an additional path; it can now flow to the bus instead of through the system ground.

The amount of current that is diverted (i.e., takes this new path) will strongly depend on the high-frequency impedance of the connection back to the dc bus. In particular, if the parasitic inductance of this path is too high, then the effectiveness of the screen will be significantly reduced. Accordingly, the implementation of this screen is critical. This will be discussed in more detail later on.

The module also consists of one or more half bridge cells, and bond wires are directly bonded to the intermediate metallization layer to provide the electrical connection. In another claim, it is stated that the module comprises a connection lug that is electrically connected to the intermediate metallization layer. This connection lug can be connected to either the positive or negative dc bus. As mentioned, the inductance of these connection lugs and wire bonds may impact the effectiveness of the screen.

Further claims in the Infineon patent explicitly exclude the usage of vias within the insulating layer. However, in the Background of the patent, it was stated that the usage of vias would allow for short electrical connections with reduced impedance. Though, due to the higher costs, this implementation method was not pursued in this patent. This is followed by a single statement that a lower inductance connection without vias is needed. However, there is no mention as to how this low inductance will be achieved, or if the connection lugs and wire bonds used in the proposed implementation are capable of achieving low-enough inductance.

In [156], a similar screen is proposed, though with a lower-inductance implementation method. The 1.2 kV SiC MOSFET power module in [156] uses two $Si_3N_4$

ceramic layers with 2-mm- and 1.5-mm-thick middle and bottom Cu layers, respectively, and has 1.6 µF ceramic and 30 µF film dc-link capacitors located close to the MOSFETs on the top layer of the substrate. The top ceramic in the multilayer substrate has vias that connect the middle metal layer to the negative dc bus potential on the top metal layer [156]. The vias, capacitors, and thick Cu layers result in a low power loop inductance of 1.15 nH [156]. As a result of the low-inductance layout, the module switching waveforms have less ringing and lower overshoot than the reference SiC MOSFET module, which has an inductance of 30 nH [156]. However, the proposed module still has a voltage overshoot of 17 % (100 V at 600 V dc bus), which is high for a module that is claimed to have a parasitic inductance of 1.15 nH [156]. In terms of EMI performance, the module has a 14 dB noise reduction compared to the reference module [156]. Further analysis and evaluation of the EMI for other versions of the power module were provided in [195].

Regarding the thermal performance, the thick Cu layers enhance the heat spreading of the power module, thereby reducing the impact of the added thermal resistance of the second $Si_3N_4$ substrate [156]. The bottom metal layer is also patterned with a pin-fin structure for enhanced cooling performance [156]. The liquid coolant is in direct contact with this bottom layer (i.e., no baseplate is used) [156]. It should be noted that, since the bottom metal layer of the multilayer substrate is floating, if a conductive casing for the cooler is not used (e.g., if plastic is used instead), then the noise level increases by up to 20 dB [156].

While this module has several advantageous features, there are also some areas for improvement. First, as mentioned previously, by connecting the middle metal to the negative dc bus, the top ceramic is providing all of the voltage isolation, and thus the second

ceramic is not being fully utilized. Second, by placing the capacitors on the same plane as the MOSFETs, the footprint of the module is significantly increased. Third, the module parasitics are not well balanced, which could have a negative impact on the EMI performance. The capacitors in this module are located on the far end of the top layer of the substrate, which is close to the high-side MOSFETs, but far from the low-side ones. As a result, there is a significant imbalance between the positive (i.e., from the high-side switch to the positive dc bus) and negative (i.e., from the low-side switch to the negative dc bus) dc-link inductances. Imbalance of these inductances has been shown to cause greater high-frequency noise compared to balanced designs [72].

In [72], CM and differential mode (DM) noise reductions of 32 dB and 30 dB, respectively, were achieved by balancing the positive and negative dc bus parasitic inductances and capacitanes. This balance was achieved by using a flip-chip layout, and evenly distributing capacitors within the power module [72]. No screening is implemented in the power module in [72]. The power module in [72], like that in [156], has the capacitors on the same plane as the MOSFETs. As a result, the footprint of the power module is increased, thereby reducing the power density. In this work, the capacitors are distributed above the MOSFETs to give balanced parasitic inductance while maintaining a small footprint. The middle metal layer is also connected to the dc midpoint, which is accessible inside the power module due to the series decoupling capacitors, which evenly distributes the electric field in both of the ceramic layers and reduces the electric field strength at the triple points. Thus, the proposed implementation will mitigate the CM current, while also improving the voltage isolation, increasing the PDIV of the power module, and maintaining a small footprint for high power density.

## *5.3 Impedance Analysis*

The condition required for the screen to effectively divert the CM current from the ground path to the dc bus may be summarized as follows:

$$Z_{screen} \ll Z_{GND} \text{ (1)}$$

where $Z_{screen}$ and $Z_{GND}$ are the impedances of the screen and ground paths, respectively. The impedance of the screen path must be much lower than that of the ground path (Eq. 1), especially at high frequency, in order for the current to be diverted from the ground to the screen. These impedances can be defined as follows:

$$Z_{screen} - \omega L_{screen} + \frac{1}{j\omega C_D} + R_s \text{ (2)}$$

$$Z_{GND} - \omega L_{GND} + \frac{1}{j\omega C_{P2}} + R_{GND} \text{ (3)}$$

where $L_{screen}$ and $L_{GND}$ are the parasitic inductances in the screen and ground paths, $R_s$ and $R_{GND}$ are the parasitic resistances in the screen and ground paths, $C_D$ is the decoupling capacitance (if any is connected to the dc bus), and $C_{P2}$ is the parasitic capacitance to ground (i.e., across the second/lower substrate). Therefore, Eq. 1 becomes:

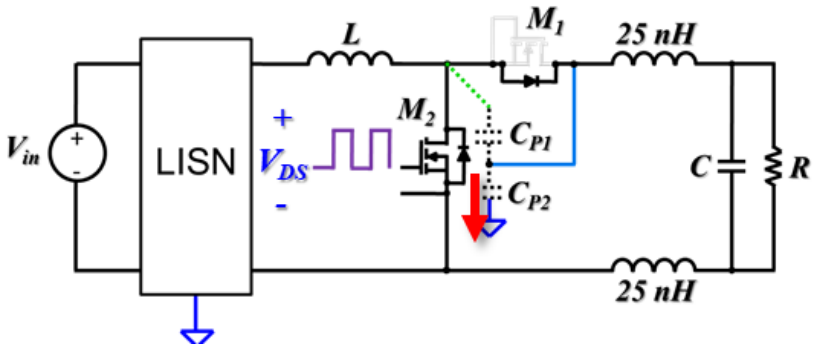
$$\omega L_{screen} + \frac{1}{j\omega C_D} + R_s \ll \omega L_{GND} + \frac{1}{j\omega C_{P2}} + R_{GND} \text{ (4)}$$

From Eq. 4, it is clear that $C_{P2}$ should be small in order to increase $Z_{GND}$. In order to minimize $Z_{screen}$, $L_{screen}$ should be as small as possible, while $C_D$ should be large. A more detailed analysis is presented in [196].

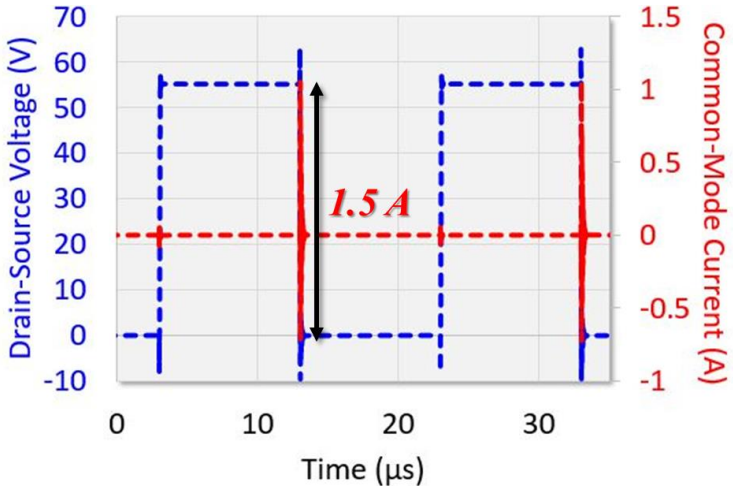
In order to demonstrate the impact of the parasitic inductance on the effectiveness of the screen, several circuit simulations were performed using LTspiceIV. The simulations in this case were performed for a dc–dc boost converter using a 1.2 kV SiC MOSFET model. The first simulation is for the case when the middle metal layer is connected to the

positive dc bus, which has 25-nH stray inductance (Figure 5-1a). This inductance value is typical for standard power modules and converters. Figure 5-1b shows the simulated drain-source voltage across $M_2$ and the current through $C_{P2}$ (i.e., the CM current). As can be seen from the waveforms, there is more than 1.5 A peak-to-peak of common-mode current flowing to the ground as a result of the high *dv/dt* when the MOSFET is turning on.

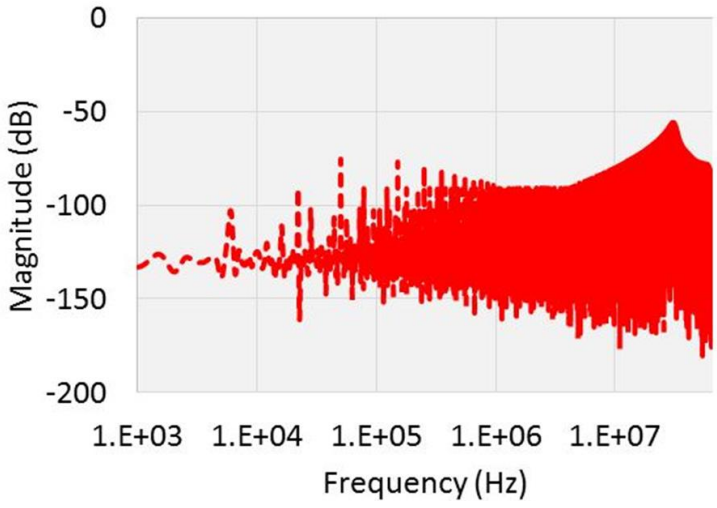
If instead there are decoupling capacitors integrated into the power module, such as shown in Figure 5-2a, and if the middle metal is now connected to these capacitors within the package, then the impact of the 25-nH dc-bus stray inductance is significantly reduced. As can be seen from Figure 5-2b, the CM current to the ground is now reduced by 86 % (7.5 times) and the high-frequency noise is decreased by 15 dB. This is because there is now a low-impedance, high-frequency path for the generated CM current to flow within the power module.




(a)

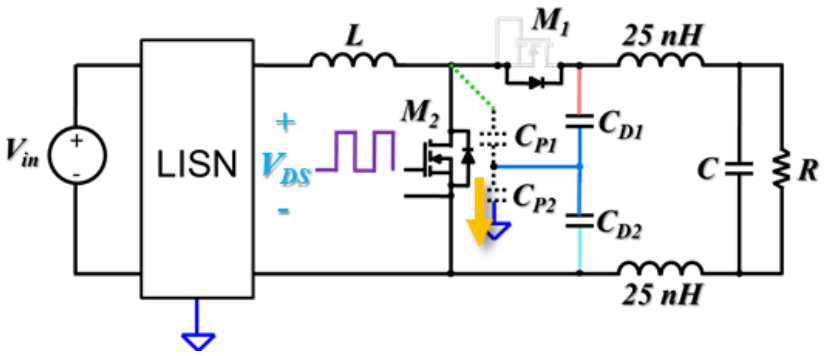



(b)

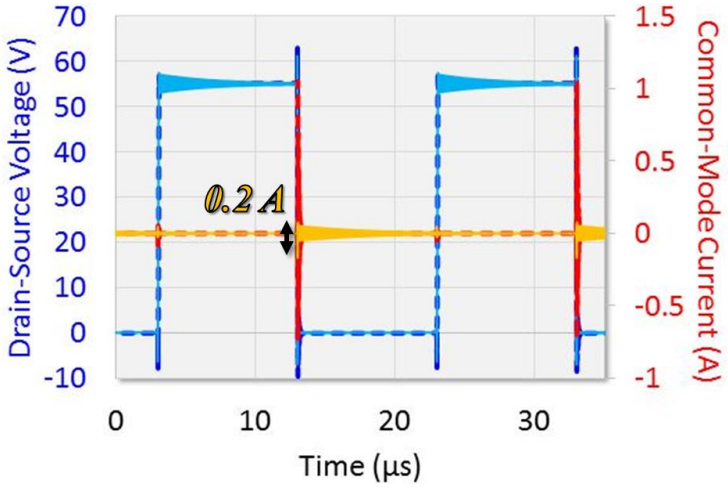



(c)

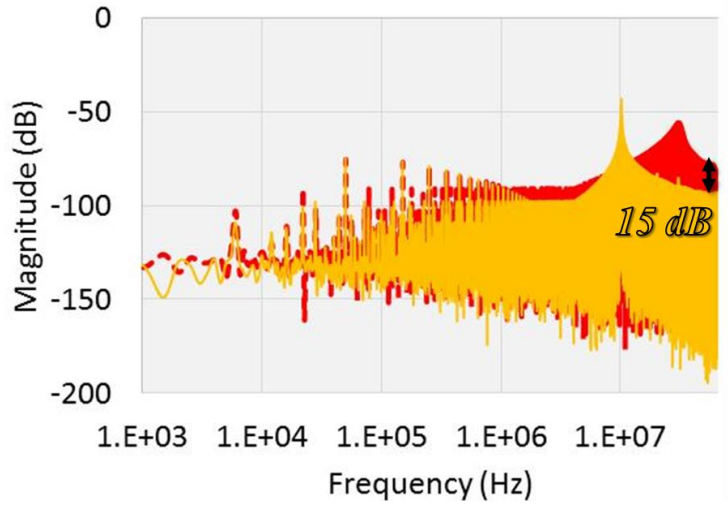
**Figure 5-1: (a) Schematic, and simulated drain-source voltage and $C_{P2}$ current in the (b) time and (c) frequency domains when the middle metal layer is connected to the external dc bus.**




(a)




(b)




(c)

**Figure 5-2: (a) Schematic, and simulated drain-source voltage and $C_{P2}$ current in the (b) time and (c) frequency domains when the middle metal layer is connected to the embedded capacitor midpoint.**

## *5.4 Common-Mode Current Screen Implementation*

Figure 5-3 shows the schematic and 3D model of the proposed 10 kV SiC MOSFET power module. In order to achieve a low-impedance implementation for the CM screen, it is proposed to embed capacitors within the power module, and to use vias within the insulating ceramic substrates to make the connection between the middle metal layer and the capacitor potentials. In this embodiment, two capacitors are placed in series, and the middle metal is connected to the shared node, which is at half of the dc bus voltage. By connecting the screen to the decoupling capacitors within the power module, the influence of the parasitic impedances external to the package are diminished.

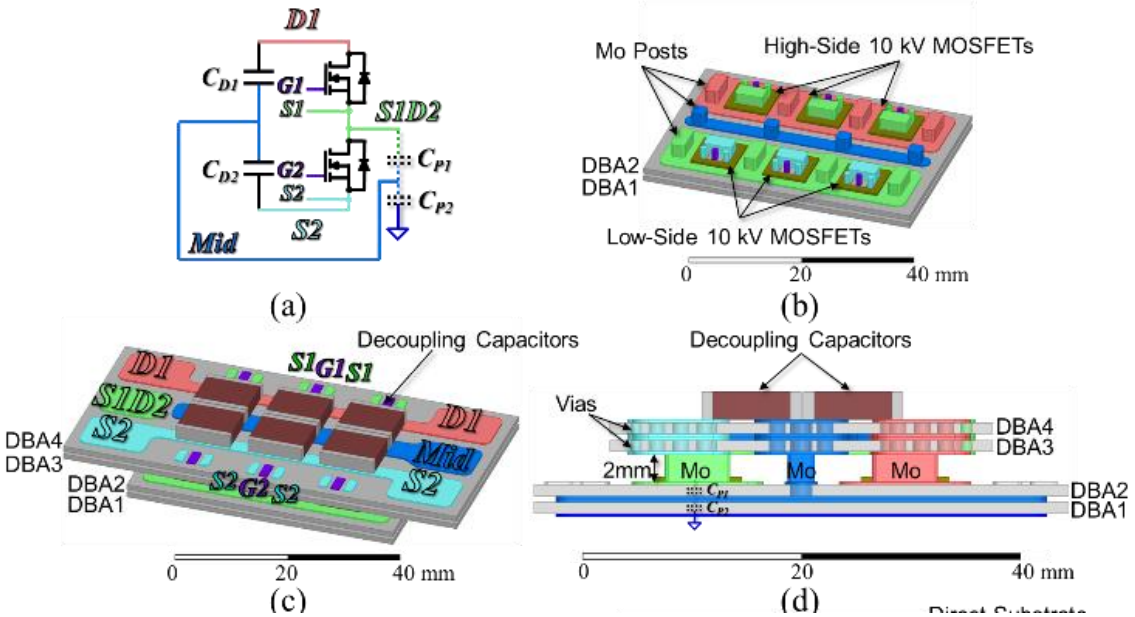



**Figure 5-3: (a) Schematic, (b) bottom stacked substrates with six 10 kV SiC MOSFET die and posts, (c) top substrate stack and embedded decoupling capacitors, and (d) side view showing the vias and CM screen connection.**

Moreover, having access to the dc-bus midpoint within the power module can help to reduce the peak electric field. As discussed in Chapter 3 and Chapter 4, by connecting

the middle metal of the bottom substrate stack to half of the dc bus voltage, the electric field strength can be reduced at the triple point, thus increasing the PDIV. If the middle metal is instead connected to the positive or negative dc bus, as was proposed in [78], then the electric field strength will be similar to the case when only a single substrate is used. This is shown in Figure 5-4, which shows the 2D electrostatic simulations for the different connection cases. From this simulation, it is clear that connecting the middle metal to either the positive or negative dc bus does not give any noticeable improvement in the electric field distribution. In this case, it may be difficult to justify the added cost and possible increase in thermal resistance of using a second substrate if it is not being fully utilized (i.e., to improve the voltage isolation).

Accordingly, it is proposed in this work to connect the middle metal to the midpoint of the embedded decoupling capacitors using posts and vias inside the ceramic substrates (Figure 5-3d) in order to both increase the PDIV and more-effectively reduce the CM current. According to ANSYS Q3D simulations, this connection method gives a parasitic inductance of less than 2 nH, allowing for a high proportion of the CM current to be diverted back to the dc bus and contained within the power module. Additionally, it was attempted to make the S1D2 pad as small as possible to minimize $C_{P1}$. For the proposed power module shown in Figure 5-3, $C_{P1}$ is 46 pF, and $C_{P2}$ is 160 pF, according to ANSYS Q3D simulations. Moreover, as described earlier, 680-pF capacitors were selected for the decoupling capacitors ($C_{D1}$ and $C_{D2}$). As shown in Figure 5-3c, there are three capacitors in parallel—one above each MOSFET switch pair—giving an equivalent capacitance of 2.04 nF. In the next section, experimental validation of this screen will be presented.

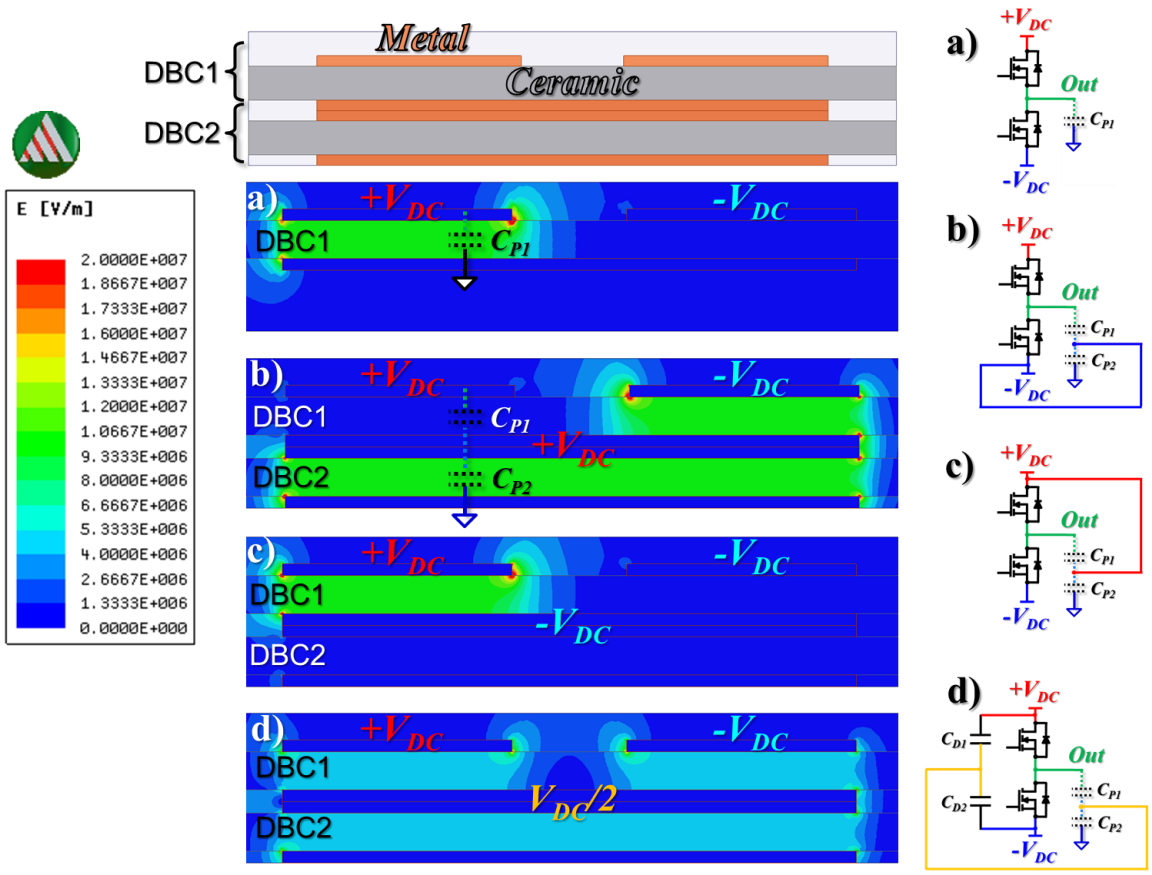



**Figure 5-4: Simulated 2D electric field distribution for (a) a single substrate, and two stacked substrates with the middle metal at the (b) positive dc bus, (c) negative dc bus, and (d) dc bus midpoint.**

## *5.5 Testing*

Switching tests were performed on a prototype of the full 10 kV SiC MOSFET power module to evaluate the effectiveness of the integrated CM current screen [194]. The tests were conducted up to 2 kV and 20 A with no external gate resistance. The voltage was limited due to the voltage rating of the test-rig bulk capacitors (2.7 kV). No external gate resistance was used in order to achieve the highest *dv/dt*, thereby testing the screen under a worst-case scenario. The hardware setup is shown in Figure 5-5.

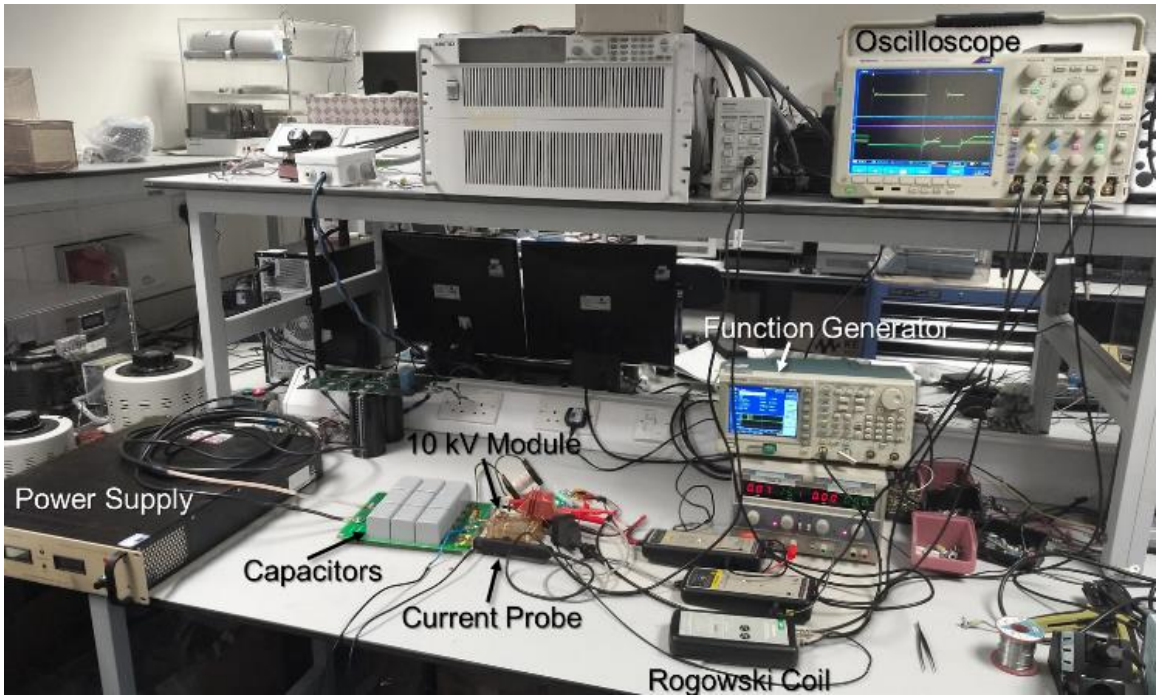
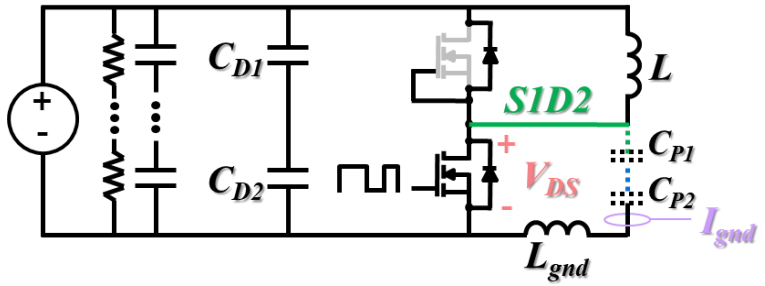


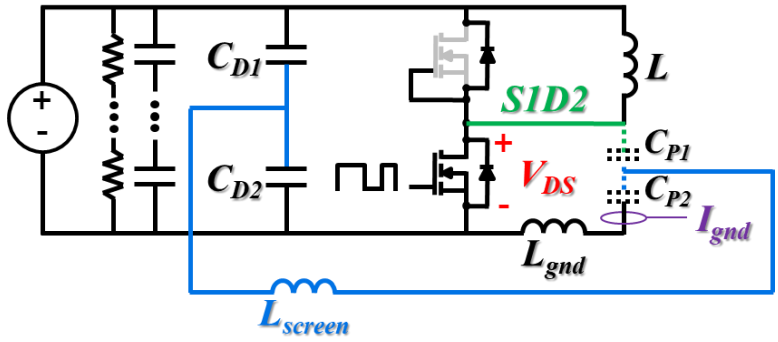

**Figure 5-5: Hardware setup for the switching tests of the 10 kV SiC MOSFET module [194].**

For these tests, a commercial gate driver from Wolfspeed was used to drive the low-side SiC MOSFET from -5 V in the off-state to +20 V in the on-state. The gate driver received the signal from a function generator. The gate-source and drain-source voltages of the low-side SiC MOSFET were measured using a 140 V active voltage probe with a bandwidth of 100 MHz (pico TA042), and a 7 kV active voltage probe with a bandwidth of 50 MHz, respectively. In order to measure the drain current, the decoupling capacitors were connected outside of the module encapsulation. This increased the parasitic inductance of the screen layer to approximately 25 nH. A Rogowski coil with a bandwidth of 30 MHz (CWT06) was connected between the capacitors and the power module to measure the drain current. A 10 kV, 600 W power supply was used to charge the bulk capacitors.

Figure 5-6a shows the schematic of the tests when the CM screen is not connected (i.e., the middle metal layer of the bottom substrate stack is left floating). In the testing setup, a wire was used to connect the bottom-most metal of the module substrate to the dc bus. This connection is estimated to have increased the parasitic inductance of the ground loop to more than 1 µH. Figure 5-6b shows the schematic of the tests when the CM screen is connected to the capacitor midpoint. A 420 µH inductor with high-voltage wire for the winding was connected across the high-side switch of the half-bridge module. The gate and source terminals of the high-side SiC MOSFET were shorted together such that its body diode would freewheel the current in the inductor when the low-side switch was off.




(a)




(b)

**Figure 5-6: Schematic of the testing setup (a) without and (b) with the CM screen connected [194].**

In order to validate the performance of the CM screen, the current through the ground path, $I_{gnd}$, was measured, as shown in Figure 5-6, using an RF current transformer with a bandwidth of 200 MHz (Fisher F-33-3). For these tests, the middle metal layer was

connected to the midpoint of the two series 680-pF decoupling capacitors. Three capacitors were placed in parallel.

Figure 5-7 shows the drain-source voltage and ground current waveforms with and without the screen at 2 kV and 20 A with no external gate resistance during the turn-off transient. The voltage rise time is 66 ns, which gives a *dv/dt* of 24 V/ns. The measured peak current through the ground path without the proposed screen is approximately 2.0 A. It should be noted that the *dv/dt* will increase as the dc bus voltage increases. Accordingly, the peak current will also increase. Furthermore, since two substrates are stacked together, the equivalent capacitance is just 36 pF. If only a single substrate were used, then the parasitic capacitance would be 46 pF (28 % higher), resulting in a larger peak current. With the CM screen connected, the measured peak current through the ground path is reduced to 0.2 A. This is a reduction of an order of magnitude. For this testing setup, the resonant frequency of the ground path is calculated to be approximately 10 MHz, which is in agreement with the ringing in the measured waveforms (Figure 5-7), indicating good analysis and estimation of the parasitics.

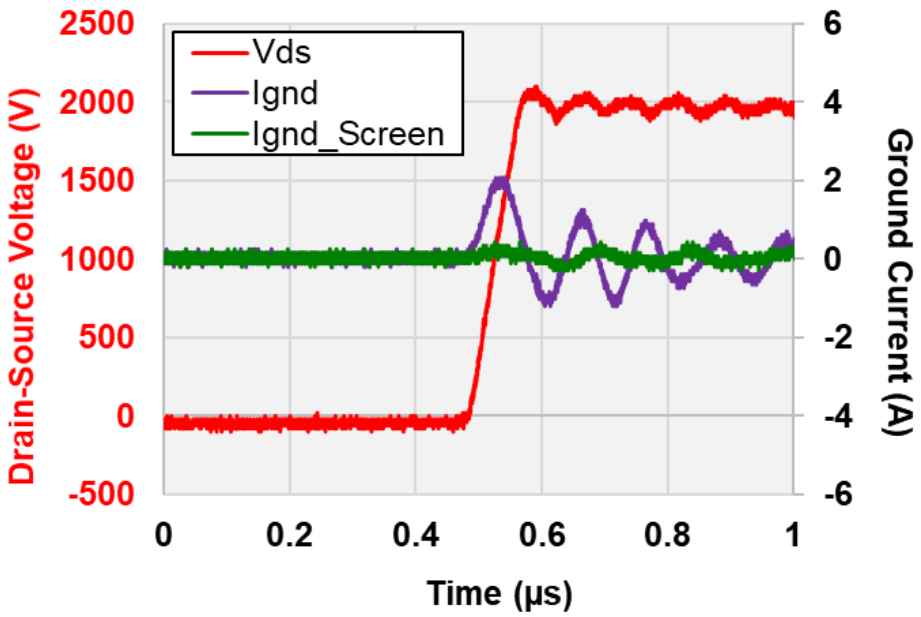



**Figure 5-7: Drain-source (red, left axis) and ground current (purple, right axis) waveforms with and without the CM screen.**

## *5.6 Conclusion*

With the correct implementation, the proposed integrated screen will reduce the need for filtering at the converter and/or system levels, thereby increasing the power density, lowering the cost, and simplifying the design of power electronic systems. Moreover, it will allow the 10 kV module to switch at its fastest speed without having to be slowed down. This screen connection also results in an increase in the PDIV by 53 % compared to when a singled substrate is used. A patent on this screen has recently been awarded [197]. In future tests, the decoupling capacitors will be placed inside the power module to reduce $L_{screen}$ and thus demonstrate further improvements for the screen. The connection from the bottom layer of the power module to the dc bus will also be improved.

# Chapter 6 Conclusion and Future Work

## *6.1 Conclusion*

This work proposed a high-density power module for 10 kV SiC MOSFETs with reduced electric field concentration and CM current. The stacked substrate structure with the middle metal layer connected to the capacitor midpoint increases the PDIV by 53 % compared to the case for a single substrate. This connection also forms a low-impedance path at high-frequency, diverting the current that would normally flow to the system ground to the bus through the embedded decoupling capacitors. Switching tests revealed a ten-times reduction in the ground current. The optimal layout and system interface also enable the module to switch 5 kV in tens of nanoseconds with negligible ringing and voltage overshoot. This is the fastest switching speed reported to date for 10 kV SiC MOSFETs.

The power density of the 10 kV module is 3.8 W/mm$^3$ with the integrated cooler. By eliminating the extra gate pads, the power density could be further increased to 4.8 W/mm$^3$, which would be 14 % higher than that of Wolfspeed's third-generation 10 kV, 240 A SiC MOSFET module without the cooler. This high power density was achieved by eliminating the external anti-parallel diodes and instead taking advantage of the superior reverse conduction characteristics of SiC MOSFETs, as well as by employing a sandwich structure and eliminating wire bonds. This high density module will significantly reduce the size and weight of medium- and high-voltage systems. Applications that could benefit from these reductions include more-electric ships, wind turbines, and HVDC systems.

The record 260-V/ns switching was accomplished due to the balanced, low-inductance design, which was achieved by the wire-bond-less, sandwich structure, and by embedding decoupling capacitors inside the power module. Each MOSFET switch pair has its own set of capacitors, resulting in a power-loop inductance of 4.4 nH for each. Without the embedded capacitors, the power-loop inductance would be more than two times higher. The fast switching significantly reduces switching losses, which enables medium-voltage converters to hard switch at frequencies in the tens of kilohertz while maintaining high efficiency. This is significant because hard switching is less complex than soft switching. Also, increasing the switching frequency of the power converter will allow the size of the passive components to shrink significantly, thereby further increasing the power density of the system.

By using two capacitors in series, the dc bus midpoint is accessible within the power module. This provides a simple way to connect the middle metal layer of the bottom substrate stack to half of the dc bus potential, which acts both as a screen to divert the CM current from flowing to the system ground, and reduces the peak electric field. The implementation of the CM screen is essential to its effectiveness. By integrating the capacitors inside the power module and using vias in the ceramic substrates, a low-inductance path for the CM current was created. This CM current screen is key to being able to operate the module at its fastest switching speed without compromising the rest of the system. If the CM current is not contained, then it can couple into the control circuitry, causing false triggering that could have disastrous consequences on the system. Moreover, the integrated screen reduces the need for external filters, thereby reducing the size and complexity of the system.

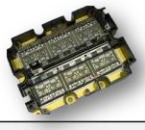
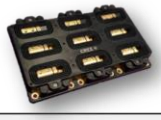
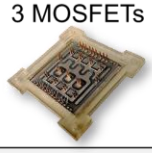
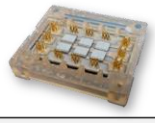
Stacking substrates was shown to be a simple and effective method for reducing the electric field strength at the critical triple points, provided the middle metal layer can be connected to a known potential, preferably half of the dc bus. By using the developed large-area Ag sintering process, two substrates can be attached with low voiding, defect density, and thermal resistance. The electric field strength in the air outside of the power module was also reduced by using field-grading plates inside the bus bar and gate driver PCB. This method does not add any cost and is simple to implement. Moreover, in order to increase the power density of the module, the creepage and clearance standards were circumvented by developing a module–system interface scheme that avoids exposed conductors.

A direct-substrate, jet-impingement cooler is integrated in the module housing. The cooler results in a compact and effective thermal management system, which will enable the module to operate at higher switching frequencies and conduct more current. This type of liquid cooler is also compatible with many medium-voltage, high-power applications.

Table 6-1 lists the key parameters for multi-chip 10 kV SiC MOSFET power modules reported in the literature. The key parameters are the power- and gate-loop inductances, parasitic capacitance from the S1D2 terminal to the heatsink, and power density. The modules listed in the table include the first-generation 10 kV, 120 A SiC MOSFET and JBS diode module from Cree and Powerex, the third-generation 10 kV, 240 A SiC MOSFET module from Wolfspeed, and the high-density module proposed in this work. It should be noted that the Powerex and Wolfspeed power modules have a larger number of SiC dies in parallel per switch position, as specified in the table.

Additionally, a wire-bonded 10 kV SiC MOSFET module was also designed and prototyped [198]. As shown by the table, the wire-bonded module is able to achieve low parasitic inductance and reasonable power density. This module also uses stacked substrates for improved electrostatic performance. However, no embedded decoupling capacitors are included in the wire-bonded module; due to the conventional 2D structure, the capacitors would need to be located on the bottom substrate, which would significantly increase the footprint of the power module. Accordingly, it was decided to have the decoupling capacitors outside of the power module. Therefore, the connection of the middle metal layer of the bottom substrate stack must be connected to the dc bus midpoint externally, which will increase the parasitic inductance and resistance of the CM screen path. This could reduce the effectiveness of the CM screen. Additionally, greater imbalance among the paralleled dies may occur. In comparison, the proposed wire-bond-less module is able to achieve half the parasitic inductance and capacitance, good balance among paralleled dies, and nearly two times the power density.

**Table 6-1: Comparison of Multi-Chip 10 kV SiC MOSFET Power Modules**

| | *10 kV, 120 A*<br>POWEREX<br>*2011*<br>12 MOSFETs, 6 JBS<br>  | *10 kV, 240 A*<br>Wolfspeed<br>*2016*<br>18 MOSFETs<br>  | *10 kV, 50 A*<br>CPES The University of Nottingham<br>*2017/2018*<br>3 MOSFETs<br>  | *10 kV, 50 A*<br>CPES The University of Nottingham<br>*2017/2018*<br>3 MOSFETs<br>  |
|---|---|---|---|---|
| $L_{power}$ | 37 nH [104] | 16 nH [108] | 9 nH [198] | 4 nH (per switch pair) |
| $L_{gate}$ | 21 nH [104] | -- | 9 nH (per die) [198] | 3 nH (per die) |
| $C_{PI}$ | 300 pF | 255 pF | 65 pF [198] | 36 pF + CM Screen |
| *Power Density* | 1 W/mm$^3$ | 4 W/mm$^3$ | 7 W/mm$^3$ [198] | 13 W/mm$^3$<br>4 W/mm$^3$ w/ cooler |

## *6.2 Future Work*

Many of the selected processing methods and materials were selected in order to improve the reliability of the power module. To test the reliability and find the weakest parts of the module, thermal (passive) and power (active) cycling tests will be performed. To save material and reduce costs, three scaled-down modules with only two semi-functional 10 kV SiC MOSFET dies per module were fabricated by the University of Nottingham. These modules will undergo thermal cycling tests. In the future, more of these modules can be fabricated and actively cycled.

Further analyses should be performed. In particular, the current density distribution in the posts under high frequency should be evaluated. In this work, only dc current density simulations were performed. However, especially with high-speed devices, the high-frequency current distribution should be analyzed since the skin effect could be significant, causing the majority of the current to stay at the outer surface of the posts.

In regards to the PD performance, a future prototype should be made without the SiC MOSFETs so PD testing can be performed on the fully-assembled package. This cannot be performed with the MOSFETs, as the body diodes will conduct if an ac excitation voltage is used. Additionally, the maximum applied excitation voltage would be limited by the breakdown voltage of the MOSFETs.

Moreover, it has been shown that pulse width modulation (PWM) voltage excitation results in a lower PDIV compared to an ac excitation [199]. Since the module will operate under PWM, it is important to evaluate the PD behavior of the module under this type of excitation. It has also been shown that PDIV decreases with increased switching frequency and *dv/dt* [199]. Since this module has high *dv/dt*, which allows the module to

switch at frequencies in the tens and hundreds of kHz range, it is important to evaluate the PD performance of this module under these conditions. Unfortunately, PD equipment with PWM excitation is not commonly available and is still being studied, so the PD tests conducted in this work were done under the standard line-frequency ac excitation. PDIV also decreases at low pressure, high temperature [166], and high humidity. Accordingly, depending on the application, the PD performance of the module under these conditions should be explored. An example of an application with these requirements is aerospace.

Further methods for increasing the PDIV, such as encapsulation and coating materials, should also be explored. As discussed previously, encapsulants and coatings with high permittivity and dielectric strength can be used to reduce the electric field strength at the triple point and increase the PDIV. Additional solutions for the module–system interface, such as the proposed metal shields around the spring terminals, should also be studied in greater detail to further enhance the system's PD performance.

Ultimately, these prototype 10 kV SiC MOSFET power modules should be used to create a high-density, medium-voltage power converter with low EMI and high efficiency while switching at tens of kHz. With this converter, the full noise spectrum can be measured, which will show the impact of the screen over a wide frequency range. The EMI testing setup itself will also be improved to reduce the parasitic impedances and improve the measurement quality. A systematic study could also be done to better understand the influence of various impedances on the effectiveness of the screen. This could allow an accurate model to be created.

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# Appendix

Additional methods for reducing the electric field at the triple point of the insulating substrate were investigated. In this appendix, 2D electrostatic simulations for these other explored methods will be presented. First, Figure A-1 shows the simulated electric field distributions when two stacked 1-mm substrates and 0.63-mm substrates are used. As can be seen from the figure, using two stacked 1-mm substrates results in lower electric field both within the bulk of the ceramic and at the triple points for the cases when S1D2 is equal to 0 V and 10 kV. Accordingly, it was decided to use two stacked 1-mm substrates in the proposed 10 kV SiC power module.

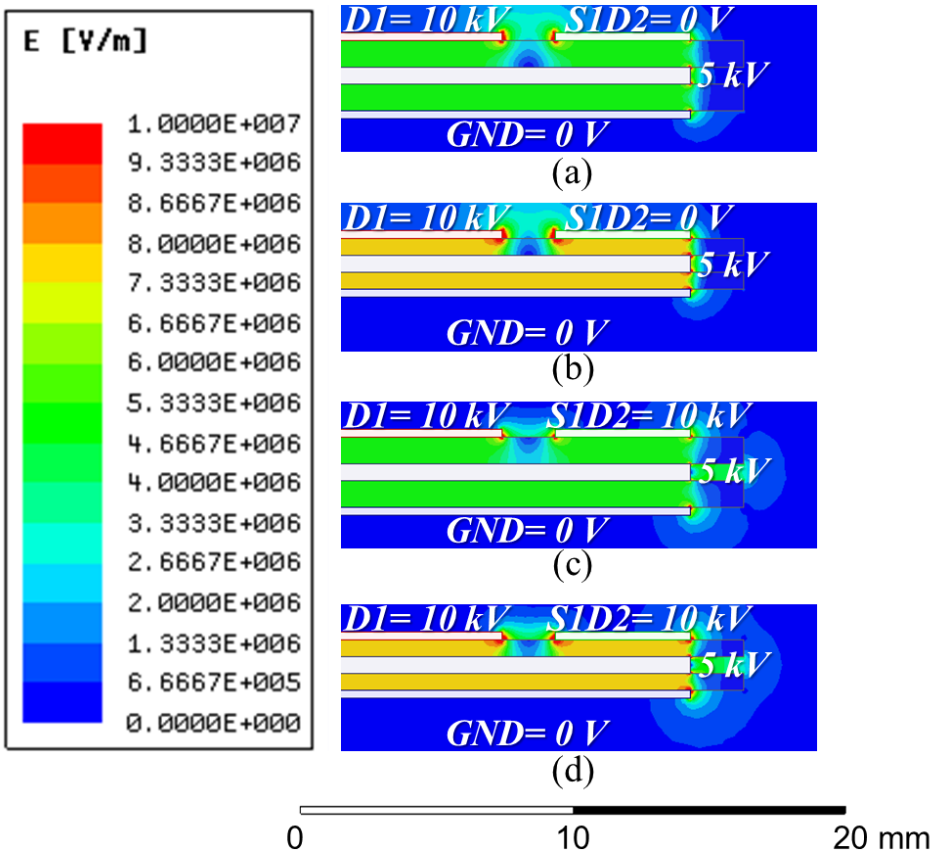


**Figure A-1: Simulated electric field for two stacked (a) 1-mm substrates when S1D2= 0 V, (b) 0.63-mm substrates when S1D2= 0 V, (c) 1-mm substrates when S1D2= 10 kV, and (d) 0.63-mm substrates when S1D2= 10 kV.**

Figure A-2 shows the simulated electric field distributions when a guard ring is placed between the D1 and S1D2 pads. The widths and potentials of the guard ring were varied to determine the influence on the electric field distribution. As shown by the figure, increasing the width of the guard ring, and thus its proximity to the D1 and S1D2 pads increases the electric field strength. Consequently, no guard rings were used in the proposed power module.

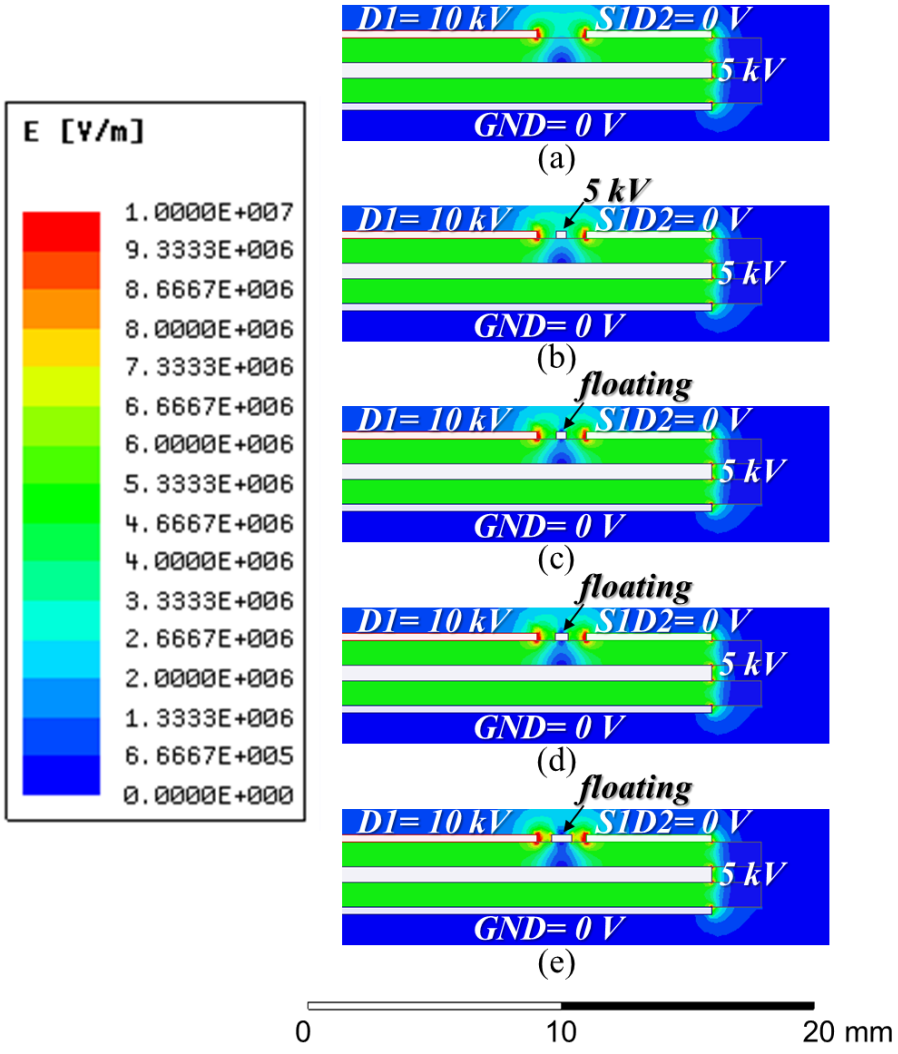


**Figure A-2: Simulated electric field for two stacked 1-mm substrates (a) without guard rings, (b) with a 0.3-mm-wide guard ring at 5 kV, (c) with a 0.3-mm-wide floating guard ring, (d) with a 0.5-mm-wide floating guard ring, and (e) with a 0.8-mm-wide floating guard ring when S1D2= 10 kV.**

Figure A-3 shows the simulated electric field distributions when the edges of the D1 and S1D2 pads are stepped. The heights of the steps were varied to determine the influence on the electric field distribution. As shown by the figure, the stepped edges and sloped edges have negligible impact on the electric field strength; therefore, no stepped or sloped edges were used in the proposed power module.

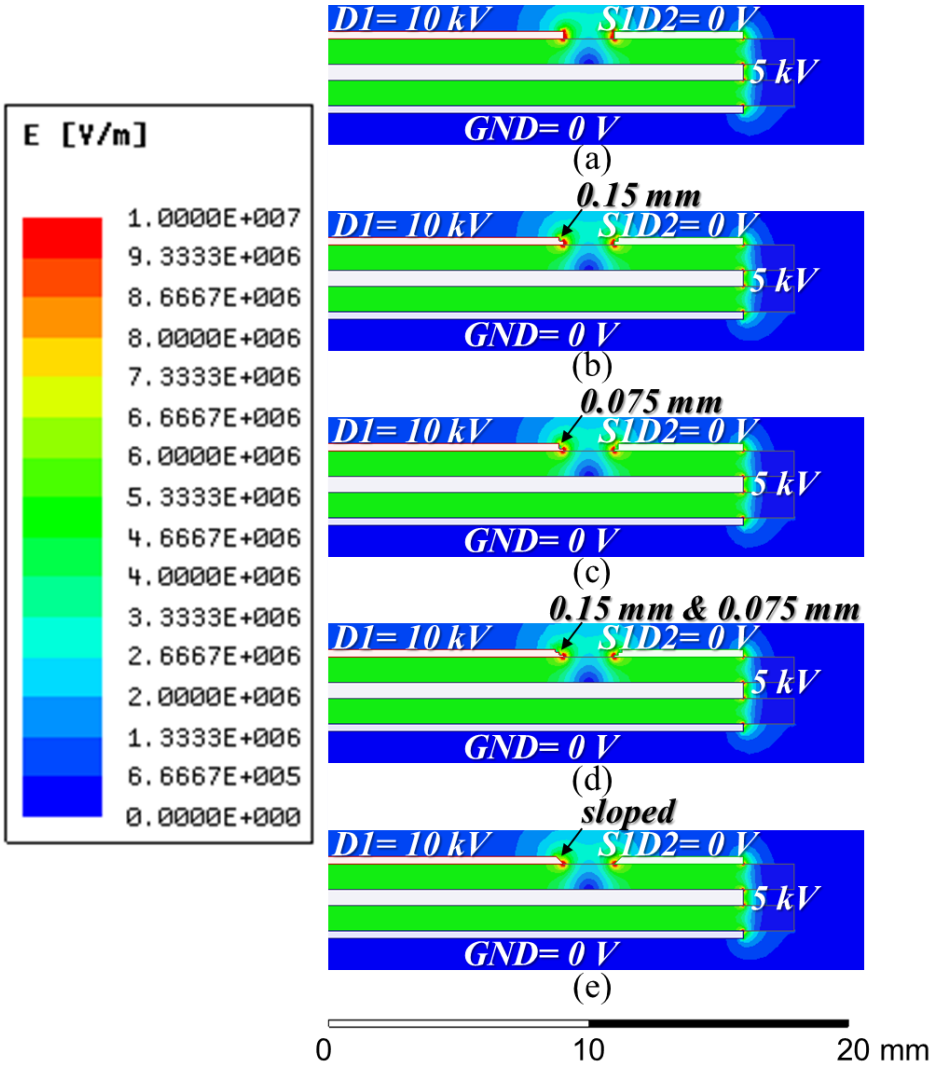


**Figure A-3: Simulated electric field for two stacked 1-mm substrates (a) without stepped edges, (b) with a 0.15-mm-tall stepped edge, (c) with a 0.075-mm-tall stepped edge, (d) with a 0.15-mm-tall and a 0.075-mm-tall stepped edge, and (e) with a sloped edge when S1D2= 0 V.**

Figure A-4 shows the simulated electric field distributions when the middle metal is patterned. As shown by Figure A-4b, when the patterned middle metal is at 5 kV and S1D2= 0 V, the influence on the electric field strength at the triple points is minimal. However, when S1D2= 10 kV, the patterned middle metal has a lower electric field strength at the triple points (Figure A-4e) than the solid middle metal case (Figure A-4d). However, the electric field strength in the open space between the middle metal patterns is increased. Accordingly, these spaces must be filled with a material that has sufficient dielectric strength and low defect density. Additionally, the metal patterns must be connected to a known potential; if the patterns are left floating, then the electric field strength will be increased (Figure A-4c). Because of the possible challenges associated with aligning these substrates, filling these spaces, and connecting these patterns to a known potential, this approach was not used in this version of the proposed 10 kV module. However, this method could be explored more in the future.

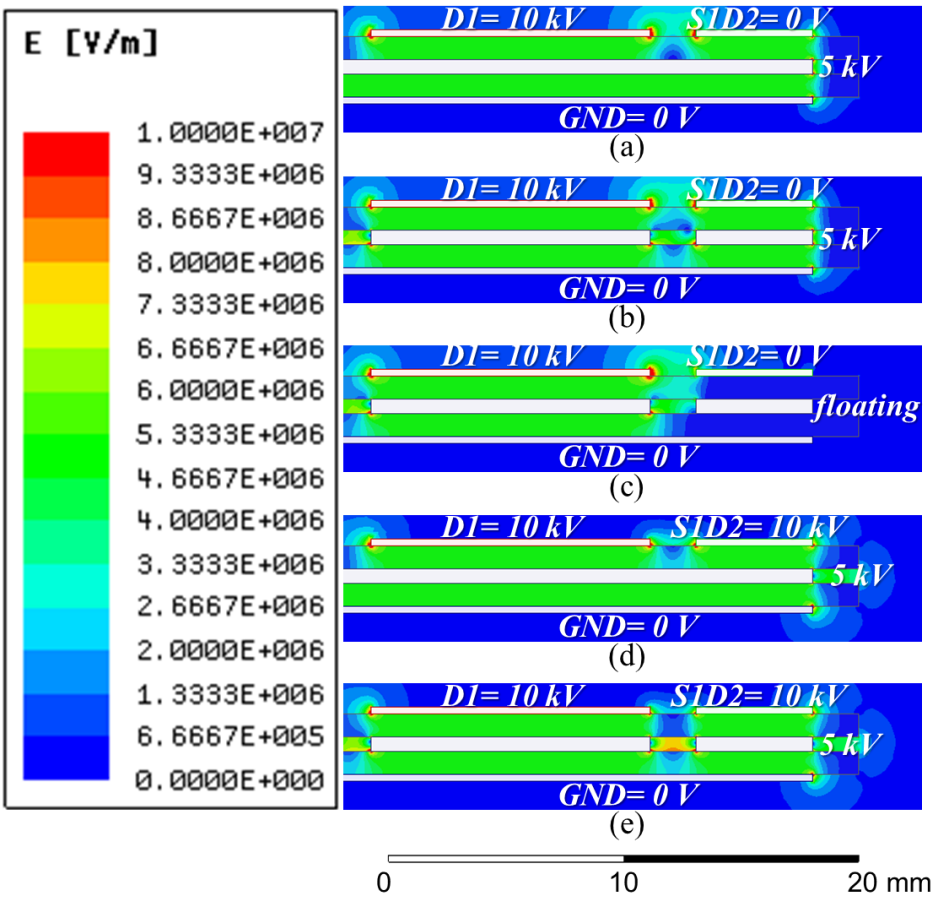


**Figure A-4: Simulated electric field for two stacked 1-mm substrates with (a) solid middle metal when S1D2= 0 V, (b) patterned middle metal at 5 kV when S1D2= 0 V, (c) patterned middle metal floating when S1D2= 0 V, (d) solid middle metal when S1D2= 10 kV, and (e) patterned middle metal at 5 kV when S1D2= 10 kV.**

Figure A-5 shows the simulated electric field distributions when different materials are embedded into the ceramic at the triple points. In Figure A-5b, a material with a relative permittivity of 16.5 (such as diamond) is used. Using a material with a high permittivity results in a reduction of the electric field strength at the triple points. If instead a material with a lower permittivity of 2.7 (such as silicone gel) is used, then, as shown in Figure A-5c, the electric field strength within the embedded material is increased. In Figure A-5d, the metal is embedded into the ceramic. It can be seen that the peak electric field is

concentrated at the bottom corner of the metal. If the bottom corner is rounded, as is shown in Figure A-5e, then the electric field strength is reduced. While these methods can reduce the electric field strength at the triple points, the reduction is small and the complexity for implementing these structures is high. Accordingly, these methods were not implemented in this version of the power module.

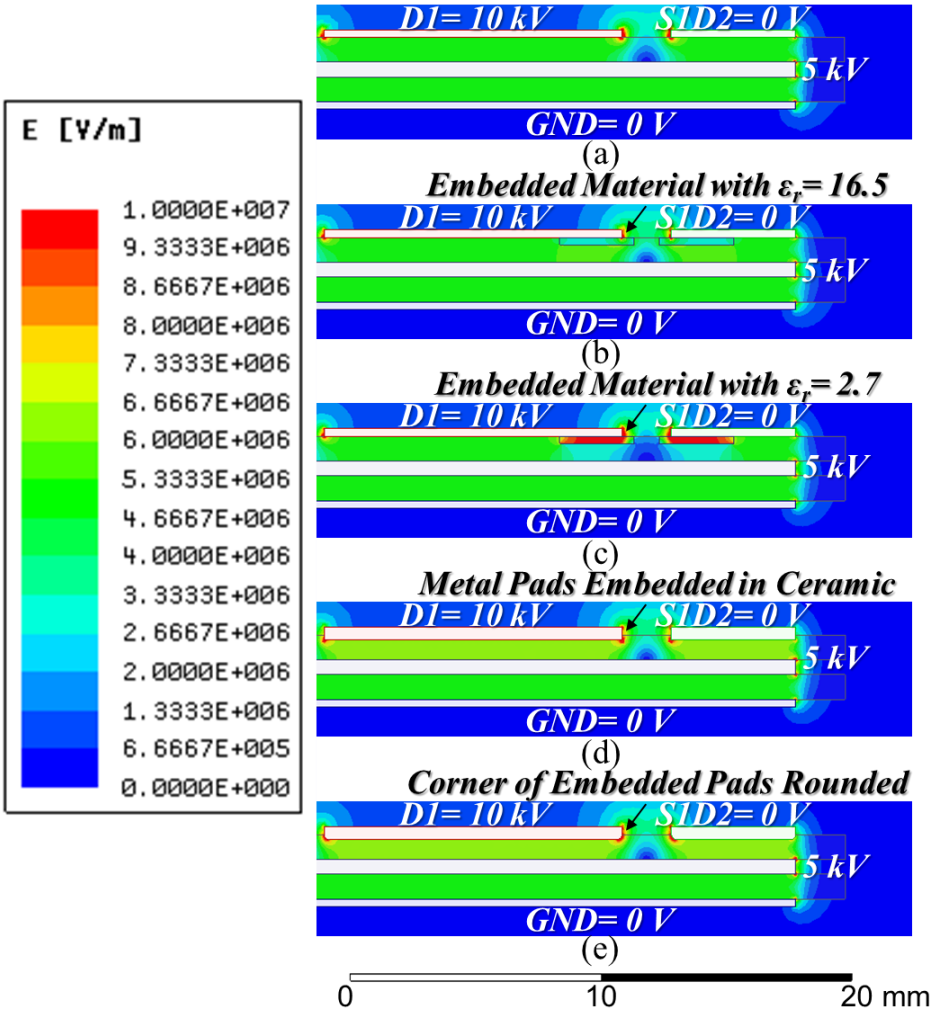


**Figure A-5: Simulated electric field for two stacked 1-mm substrates (a) without embedded material, (b) with embedded material with a permittivity of 16.5, (c) with embedded material with a permittivity of 2.7, (d) with metal pads embedded in the ceramic, and (e) with the metal pads embedded in the ceramic and the corners rounded when S1D2= 0 V.**