Power Efficient Transmit/Receive (T/R) Elements for Integrated Millimeter-wave Phased Arrays

Sadia Afroz

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Kwang-Jin Koh, Chair
Sanjay Raman
Dong S. Ha
Jeffrey H. Reed
Vinh Nguyen

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ABSTRACT

Thanks to a small wavelength (large bandwidth) combined with a low loss transmission window around 94 GHz and 120 GHz, the 75-120 GHz frequency band in millimeter wave (mm-wave) provides a promising opportunity for high data rate long range wireless communications and high-resolution imaging systems. Large-scale phased arrays have been exploited in such application for their beam forming and null steering capabilities, resulting in high directivity and improved SNR. But growing DC power consumption (P_{diss}) in such large scale arrays has become an on-going concern along with noise, linearity and phase resolution trade-offs in current phased array architectures. To address these issues, we propose a power efficient phase shifter (PS) architecture based on quadrature hybrid coupler, which leverages the benefits of conventional active and passive PSs at mm-wave. The phase shifter has low loss, resulting in low power dissipation and the power domain phase interpolation by the quadrature hybrid gives low phase error and high linearity. We design W-band (90-100 GHz) phased array transmit and receive (T/R) modules in 130 nm SiGe BiCMOS technology based on the proposed PS and our measurements show high power efficiency with the lowest power consumption at W-band to our knowledge (18mW and 26mW power dissipations at receiver (Rx) and transmitter (Tx) front-ends respectively). Rx shows 23 to 25 dB peak gain, 6 to 9.3 dB NF and Tx can deliver upto 7 dBm output power with 18% power efficiency. Moreover, our PS can achieve 5-bit phase resolution with $< 2^{\circ}$ RMS phase error and provides 0 dBm saturated output power at 94 GHz. The phase shifter (PS) is also scalable beyond W-band without significant loss. We demonstrate this with a 120 GHz two channel phased array receiver (Rx), where a single channel shows 15.6 dB peak gain with $P_{diss} = 53$ mW which

shows one of the highest gain efficiency (gain/P_{diss}) among D-band phased arrays. We can further reduce the power consumption by leveraging the bidirectional signal processing at the phased array front-end. To achieve this, we designed a W-band bidirectional variable gain amplifier with gain variation ranging from 6 to -1 dB at 94 GHz which can be used along with bidirectional PS. The amplifier will replace the lossy SPDT switch in the conventional bidirectional approach, reducing the overall power consumption.

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GENERAL ABSTRACT

The wireless technology is pushing towards the high operating frequencies to achieve high data rate and 75-120 GHz frequency band in millimeter wave (mm-wave) are of great current interest for the backhaul communications, radar and imaging systems. However, high frequency yields high propagation loss which has been overcome with large scale phased arrays in such applications for their high directivity, narrow beam forming capabilities and implementation with silicon technologies. The high dissipation due to large number of elements is a major concern which often requires heat sinks around the sensors leading to increase in cost, size and weight. For the large silicon array to be of practical use in commercial systems, it is paramount to maintain a high power efficiency and low power dissipation in the array element. In this research, a power efficient phased array architecture has been proposed which is implemented to design transmit/receive (T/R) modules in advanced silicon technologies. Experimental results show that the proposed architecture achieves the lowest power consumption and improved power efficiency per T/R element among state-of-the-art mm-wave phased arrays. The research also proposes an alternative way to improve power efficiency of phased arrays by reusing the amplifiers in both transmit and receive path where the amplifier replaces lossy switch as well, resulting in a low loss bidirectional system which can reduce the power consumption further. Finally, we believe that this research contribution has an significant impact in the effort of building low power large-scale phased arrays at mm-wave frequencies.

Dedicated

to

My Mother and Late Father

Author's Acknowledgments

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Chapter 1

Introduction

1.1 Background

The exponential increase in demand for high speed (i.e. high data rate) wireless communication can be achieved by large bandwidth and less interference which is possible at millimeter wave (mm-wave) data carrier frequencies (30-300 GHz) [1]-[3]. Several bands in the upper mm-wave region have been opened based on the transmission window shown in Fig 1.1 for commercial wireless system [4]. For an example, V-band (60 GHz) has the potential for indoor short range communication because of higher atmospheric attenuation [5][6]. Transmission windows (attenuation $<$ 0.6 dB/km) at 73 GHz, 83 GHz and 94 GHz (W-band) make it attractive for long range wireless communication: multi-Gb/s backhaul links in the cellular system, fixed and mobile satellite radar and radio astronomy, imaging system [7]-[9]. 70 GHz band has also been considered for future 5G application [10]. The 120 GHz frequency band is allocated for a moderate range of high data rate wireless communication [11]. Among these frequency bands, the use of 94 GHz and 120 GHz can improve the resolution of imaging systems and the communication system benefits from large available bandwidth around the high frequency carrier, enabling high data rate long range communication due to the presence of low atmospheric window.

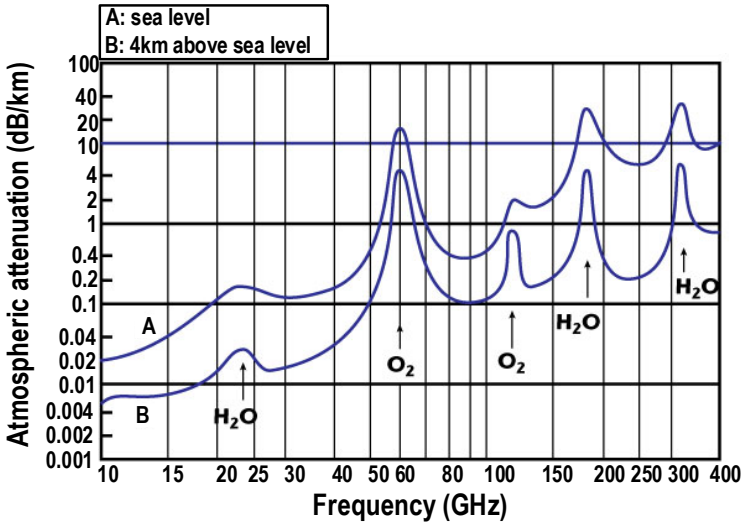


Figure 1.1: Average atmospheric attenuation (A: sea level, B: 4km altitude) [4]

Previously mm-wave circuits and systems were considered to be mainly implemented using compound semiconductor technologies such as GaAs or InP, but in the past few years, silicon technologies have gained much attention owing to their recent advancement in device speed and high level of IC integration. Advanced silicon technologies such as SiGe HBTs (silicon-germanium heterojunction bipolar transistor) and CMOS FETs have a high cutoff frequency for designing high performance, low-cost systems with more functionality, making them competitive at mm-wave [12]-[14]. While CMOS provides a higher density of digital integration, the effective cut-off frequency and power delivering capabilities of CMOS devices are lower than SiGe devices. Although the high-frequency performance of CMOS technology is further enhanced by introducing SOI (silicon-on-insulator) devices which are expensive, but still they have low breakdown voltage due to the downscaling of the transistors. In general, SiGe HBTs have superior RF performance than bulk CMOS because of high breakdown voltage and low noise. SiGe BiCMOS technologies have the advantage of having high performance SiGe devices while still providing CMOS integration for digital functions [15].

Although SiGe and advanced CMOS process have reached to the desired performance in order to be used efficiently in mm-wave integrated circuits, a number of imaging and wireless link

applications require highly directional transceivers, two-dimensional scanning and support for polarization operation in order to overcome the high propagation loss at mm-Wave frequencies. For such applications, phased array based solutions are well known for their beam forming and beam steering capabilities, which provide high range and high signal to noise ratio (SNR) than a single antenna-based system. Phased array system also allows spatial selectivity which reduces the interference and increases the overall capacity in a dense system, helping in multiple-input-multiple-output (MIMO) wireless technology [16].

1.2 Motivation

Large-scale active electrically scanned arrays (AESAs) are particularly needed to realize narrow beam forming for high-resolution radar sensors or long range multi-Gb/s backhaul links at mm-wave frequencies [17]. In recent research, it has been shown that atleast 960 number of elements are needed to achieve 10 km distance of backhaul link for 1 Gbps data rate communication at 94 GHz [18]. However, a high DC power consumption in such large scale arrays, especially in silicon-based phased arrays, raises a significant concern on the thermal management issues. Large number of ICs are needed to be thermally controlled simultaneously, potentially requiring a large size thermal cooling system and increasing the size and weight of the AESAs [18]. For low volume and compact array systems, it is critically important to design individual phased array transmit/receive (T/R) elements with a high power efficiency. The phase shifter (PS) is an indispensable element of phased arrays and significant efforts have been made to improve the performance of the integrated PSs in silicon technology from microwave to millimeter wave frequency. Different kind of phase shifting scheme in both base-band domain [19]-[22] and RF domain [23]-[39] have been reported at mm-wave frequencies. Fig 1.2 summarizes the DC power consumption per channel for transmitter and receiver of recent state-of-the-art works at mm-wave phased array system. Even though a significant reduction in DC power consumption/channel has been achieved at around 60 GHz utilizing baseband phase shifting approach with advanced silicon technologies [21][22], power consumption is still high at W-band frequency and beyond. Generally, base-band and LO

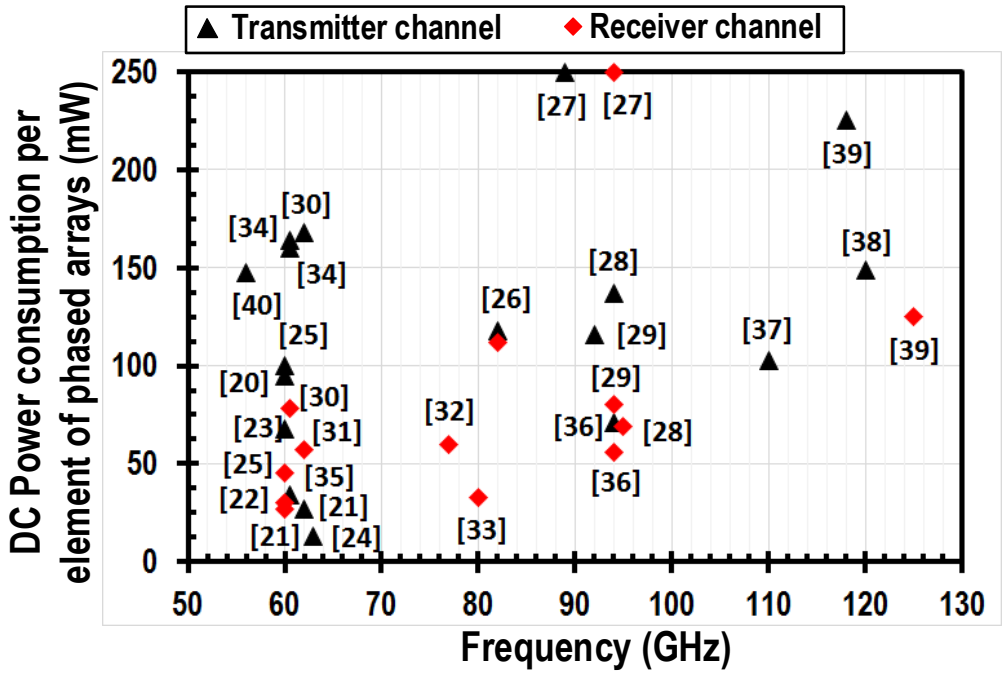


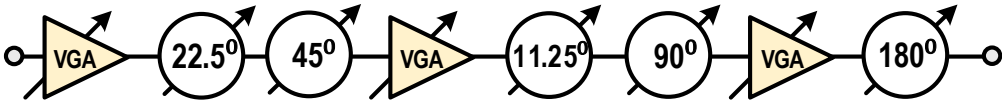
Figure 1.2: DC power consumption per element of phased array front-end at mm-wave frequencies.

phase shifting approach require substantial LO distribution network, mixers and quadrature generations for each element [40]-[42]. While RF phase shifting is still promising at high-end mm-wave frequencies for using minimum number of hardware and simplicity in signal combining and distribution, resulting in low power and compact area at front-end. It also rejects a larger portion of strong in-band interferer before the mixer, relaxes the linearity requirement of the mixer. But the drawback of RF phase shifters, which can be either passive or active type, is low power efficiency (η) due to poor gain and linearity with large DC power consumption. In the target of large arrays, the required element output power (P_{out}) is typically 3-5 mW. In such a modest P_{out}, the signal loss (P_{loss}) of passive phase shifters (PSs) becomes a major culprit for degrading η.

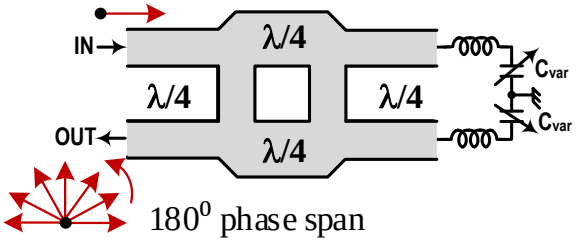
For integrated phased arrays at the microwave to low-end mm-Wave bands, the passive PSs based on switchable LC networks have been popular [25][43]-[45]. However, when implemented in the silicon process, P_{loss} of the passive PSs is directly dependent on the NMOS switch loss that could be substantial at W-band frequency and beyond where the speed of the NMOS (e.g. f_T or f_{max}) may not be sufficient. For an example, in $0.13\mu m$ SiGe BiCMOS process, which is still

Loss @ 0.13 µm SiGe BiCMOS Tech.

ON	1.6	2.7		1.4	4.0		8.3
OFF	2.9	3.8		2.5	4.8		8.7



(a)



(b)

Figure 1.3: Passive phase shifting approaches: (a) discrete NMOS switch based LC phase shifter, and (b) reflection type phase shifter (RTPS).

preferable to nano-scale CMOS process in defense applications due to its high breakdown voltage, the 4-bit passive PS with switchable LC network shows overall 20 dB loss at W-band [33] (see Fig 1.3(a)). The compensation of such large loss claims substantial DC power dissipation. Albeit the passive PSs can achieve a high linearity, the loss compensation amplifier can inflict nonlinearity, nullifying the benefit of linearity performance. Furthermore, the switched LC based PSs suffer from the tradeoff between phase resolution and loss: namely, increasing phase resolution requires cascading more switched LC sections and incurring more loss from the LC networks.

The reflection type phase shifters (RTPS), comprised of the 90-degree hybrid coupler with varactor loads, are often used for bidirectional signal flow in transmitters (Tx) and receivers (Rx) [46] (see Fig 1.3(b)). Inherently, the RTPS has a tradeoff between phase shift range and insertion loss because of limited capacitance range and a poor quality factor of varactors. A relatively low loss

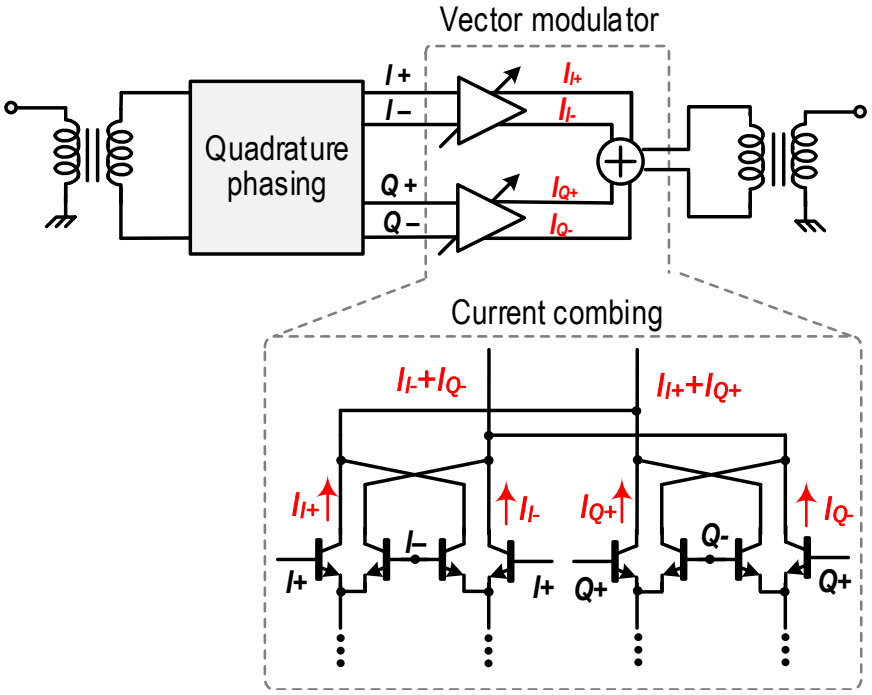


Figure 1.4: Active phase shifting approach: gilbert cell based vector modulator.

(-8 dB) with nearly zero DC power consumption can be achieved by the RTPS with 180-degree phase span at W-band [29] [47]. However, in order to generate the discrete phase shift in full 360-degree phase domain, cascaded structure of RTPSs is needed which increases the overall loss of the PS. A Balun with $0^0/180^0$ phase inversion active circuitry can also be used to get full 360-degree phase, by which RTPS is no longer remain bidirectional and the power consumption increases. Moreover, variable gain amplifiers are often needed in order to reduce the large gain variation over different phase states in RTPS, which degrades the overall linearity and power efficiency of the PS as well.

The vector modulator (VM) based active PSs can achieve virtually unlimited phase resolution by interpolating quadrature phases in a continuous way as shown in Fig 1.4 [21][27][30][35]. In general, the Gilbert-cell based VMs leveraging the quadrature current combining to synthesize a new phase, exhibit poor gain performance at the expense of a large DC power consumption. Another limitation of vector modulators is the crosstalk between the I and Q signal vectors during

current combining, where the variable gain of one component (I or Q) can depend on the value of the other component (Q or I). This results in phase and amplitude variation across different phase settings, complicating the control scheme to minimize the phase error. This issue becomes more severe at high end mm-wave frequencies due to the reduced output impedance of the common gate (CG) stage of the vector modulators. The current combining efficiency is also poor due to the parasitics at mm-wave. The linearity of the current mode VM is not often sufficient to drive the next stage power amplifier (PA) and the phase distortion is large at high input power level due to nonlinear capacitances at the output of the VM [28].

This research proposes a power mode vector modulator composed of weighting amplifiers and a 90-deg hybrid coupler, for a low loss and power efficient T/R elements, which is implemented at 94 GHz and 120 GHz frequency band. The fundamental difference of the proposed VM compared with the conventional current mode VM is that input differential signals are weighted first; then, their phases are split by 90 degrees and added in the power domain by a quadrature hybrid to synthesize a new phase. Unlike the switched LC PSs or RTPSs, the phase resolution or variable phase range in the proposed PS is not traded with the loss, resulting in a high phase resolution in the full 2π radian space with a high power efficiency. The loss of the PS is determined by the hybrid couplers which are wide band structures. The I/Q combining error by the quadrature hybrid is less vulnerable against input impedance variation by the weighting amplifiers at different phase states because of the high isolation between the inputs of quadrature hybrid, resulting in low phase error PS architecture. The size of hybrids gets smaller at high frequencies, thus a low loss and compact phase shifter can be achieved at high-end mm-Wave frequencies. Furthermore, by interpolating phases in power domain using a pure passive hybrid coupler, the potential nonlinear phase distortion at high input power is minimized compared to current mode vector modulators. The proposed phase shifter is implemented to design power-efficient T/R modules in 0.13 μm SiGe BiCMOS process. With the optimum design configuration of the PS in terms of loss, the phased array T/R elements show one of the lowest power consumption with highest power efficiencies at both 94 GHz and 115 GHz.

In order to reduce power consumption further and also the chip area in RF shifting scheme, a

bidirectional T/R system has been proposed where the phase shifter and amplifiers block should be reused by T/R element and bidirectional signal flows in PS and amplifier. With this purpose, a bidirectional amplifier has been designed at 94 GHz which also eliminates the use of lossy SPDT switch at the T/R front-end and improves noise figure.

1.3 Thesis Overview

The thesis is organized as follows:

Chapter 2 introduces the proposed 90^0 hybrid coupler based power domain phase interpolator type phase shifting sub system at W-band for power-efficient phased arrays. The chapter discusses the overall phase and gain error analysis due to the finite gain and phase error of passive hybrid networks. It also discusses the effect on I/Q generation and phase interpolation by quadrature hybrid due to the variation of impedance at different gain states. The proposed phase shifter is used to design a 90-100 GHz Tx phase shifter and a Rx channel in $0.13\mu m$ BiCMOS SiGe process. A details design procedure and measurement results are also presented in chapter 2.

In chapter 3, quadrature hybrid based phase interpolator is modified to achieve an optimum power efficient phase shifting system at 92-98 GHz in $0.13\mu m$ BiCMOS SiGe technology. A whole transceiver system design has been discussed in details with measurement results, which shows state-of-the-art figure of merit (FOM) in terms of Tx power efficiency and Rx power normalized dynamic range compared to previous phased array works.

A low power two element 120 GHz phased array receiver front-end has been designed by utilizing quadrature hybrid based phase interpolator in $0.13\mu m$ BiCMOS SiGe process and a details design procedure including measurements upto 115 GHz are discussed in chapter 4.

Chapter 5 presents the proposed bidirectional T/R system and the design details of 94 GHz bidirectional variable gain amplifier. An extensive analysis of matching networks that enables bidirectional signal processing and measurement results are discussed in this chapter.

Chapter 6 concludes the thesis by giving a summary of the contributions in this research and the future work for implementing the designs in power efficient large-scale phased arrays.

Chapter 2

A Quadrature Hybrid Coupler Based Vector Modulator for W-band (90-100 GHz) Phased Array Applications

2.1 Introduction

As described in chapter 1, passive phase shifters (PSs) suffer with a tradeoff of loss and phase resolution while active phase interpolator type phase shifters consume large DC power. In order to leverage the benefits of both active and passive phase shifters with a minimum tradeoff, a phase shifter architecture has been proposed which interpolates phase in a passive way by utilizing quadrature phasing and power combining capability inherited in 90^0 hybrid-coupler. The PS is favorable for single-ended signal processing and all building blocks can be designed with 50 Ω matched impedance, suitable for a large-scale array (# of elements 100$\sim$1000's) at W-band and beyond.

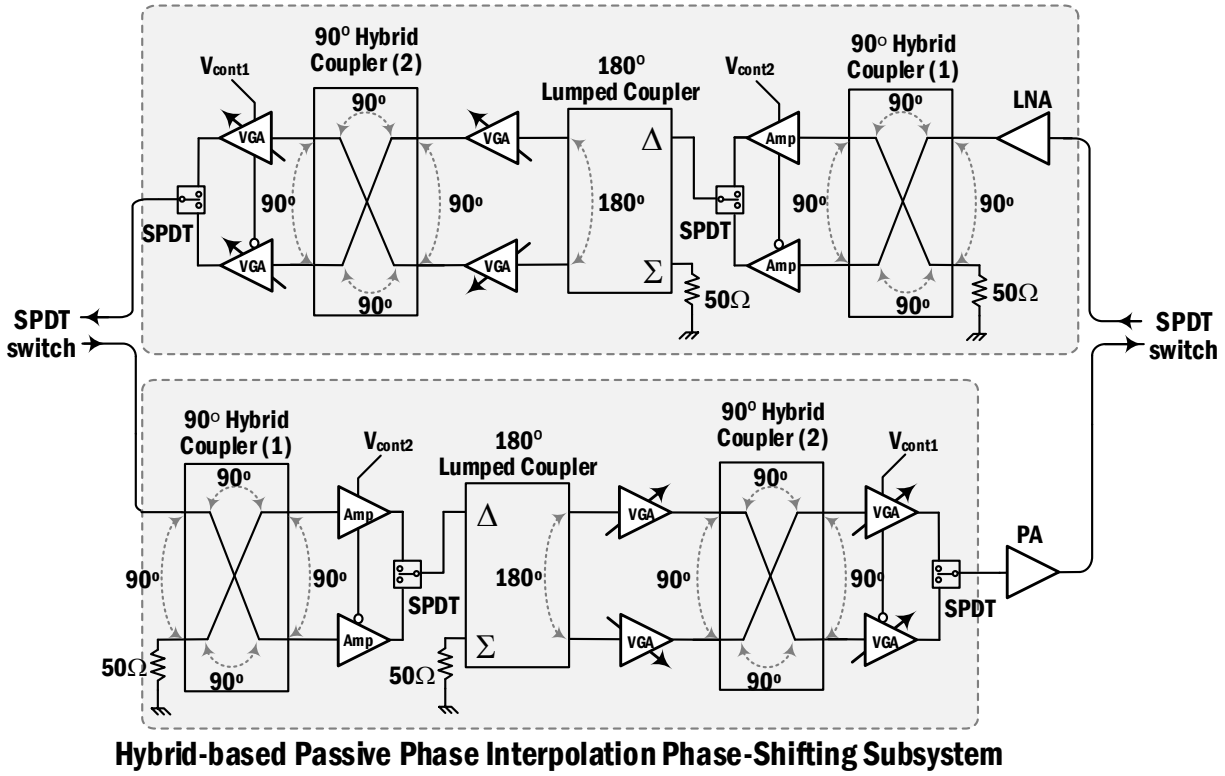


Figure 2.1: Block diagram of the T/R channel utilizing 90-degree hybrid based phase interpolator.

2.2 Power Mode Vector Modulator

The block diagram of the T/R element adopting the quadrature hybrid coupler based vector modulator is shown in Fig 2.1. In the proposed phase shifting architecture, the quadrature hybrid plays as a phase interpolator by combining quadrature signals in the power domain. Fig 2.2 shows conceptual diagram of synthesizing four quadrant phases by interpolating differential input phases in a 90^0 hybrid-coupler. Suppose the input is a narrow band signal having λ-wavelength and all ports are terminated with a matched impedance. When the differential signals I and $\bar{I}$ are injected through two isolation ports, I and $\bar{I}$ are delayed by 90^0 and 180^0, respectively, because of $\lambda/4$ and $\lambda/2$ path delays, and added together in power domain at the output port ①, synthesizing a 45^0 phase. The inverted phase is obtained while taking the output at ②, creating a 225^0 phase. This is essentially vector summing in a purely passive way and by changing the magnitude of the input vectors indi-

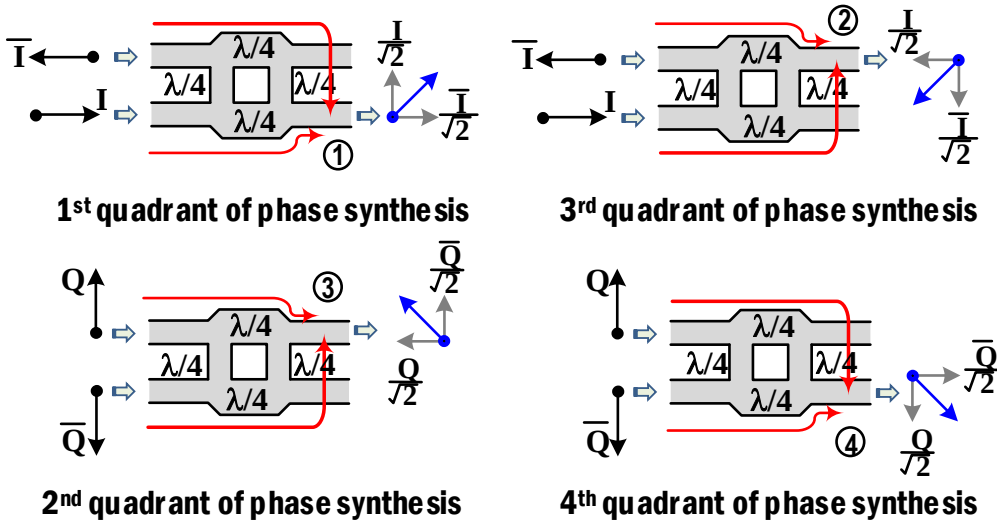


Figure 2.2: Power domain phase synthesis by 90^0 hybrid coupler at all four quadrant.

vidually, it can synthesize different phase states in the first and third quadrant phase domains. In a similar way, the differential vectors, while selecting quadrature input signal, Q and $\bar{Q}$ generate phases in the second and fourth quadrant phase domains at outputs ③ and ④, respectively. Fundamentally, the hybrid splits input differential phases into quadrature phases and interpolates the quadrature phases simultaneously, synthesizing all four quadrant phases with $1/\sqrt{2}$ gain factor at the output.

2.3 Operation of the Phase Shifter

The block diagram of the proposed phase shifter adopting the quadrature hybrid coupler based vector modulator is shown in (see Fig 2.3), where the functionality of each block is also illustrated using signal vector representation. Here, the passive 90^0- and 180^0-hybrids are interposed in between the cascaded amplifiers stages to create basis I/Q signals. The input signal will be split into I/Q vector signals by the first 90^0-hybrid coupler (① or ②). The in-phase (V_I) and quadrature phase (V_Q) component signal can be expressed in terms of RF input signal (V_{in}) as $V_I = V_{in}/\sqrt{2}$ and $V_Q = jV_{in}/\sqrt{2}$, respectively. One of the I/Q phases will be selected in the pre-selection

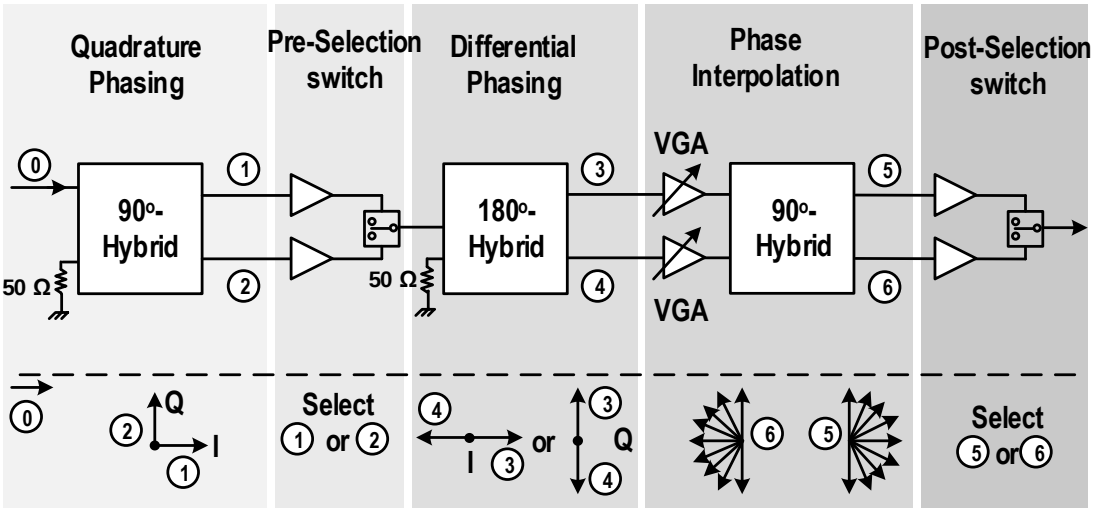


Figure 2.3: Block diagram of the phase shifter employing the 90^0 hybrid-coupler based phase interpolation with representing vector signal phasing at each function block.

stage and the 180^0-hybrid generates differential phases based on each set of the I/Q vectors at ③ and ④, which are fed to the variable gain amplifiers (VGAs) for further fine phase processing. The second 90^0-hybrid plays as a phase interpolator as discussed before: i.e., it takes independently weighed differential inputs, changes the differential phases into quadrature phases, and finally adds the quadrature-phased signals at the outputs. A continuous gain control in the VGAs will result in two-quadrant continuous phases at each output of ⑤ and ⑥, respectively. The cascading of the post phase selection stage completes 360^0 of phase rotation at the final output. If the weighting factors of the two VGAs are w_u, w_l and assuming losses from hybrids and SPDTs are properly compensated by the amplifiers, then the output signal of the phase shifter can be expressed as,

$$V_{out} \propto \begin{cases} (w_u + jw_l) \cdot V_{in} \text{ or } (-jw_u - w_l) \cdot V_{in}; & \text{if } V_I \text{ is selected} \\ (-jw_u + w_l) \cdot V_{in} \text{ or } (-w_u + jw_l) \cdot V_{in}; & \text{if } V_Q \text{ is selected} \end{cases} \tag{2.1}$$

The overall loss is contributed by passive hybrids: 3.5×2= 7 dB from the two 90^0 hybrids and 0.5-dB loss from the 180^0 hybrid. The SPDT switch adds extra loss ($\sim$2 dB) which is compensated by amplifiers. Thus the passive hybrids are responsible for quadrant switching where the phase interpolation at each quadrant is done by power combining of weighted signals by the 90^0 hybrid.

A wide-band hybrid network can be designed at mm-wave frequency with a low phase error. The phase distortion of the PS at high input power level is determined by the nonlinearity of the VGA only, contrast to the conventional nonlinear gilbert cell based vector modulators. Thus PS can handle relatively high input power without significant phase distortion compared to gilbert-cell based vector modulators in Tx application.

2.4 Gain and Phase Error Analysis of the Phase Shifter

There are mainly three non-desirable effects in a phased array system for amplitude and gain error: i) increased sidelobes, ii) erroneous beam pointing angle, and iii) reduction in directivity of arrays. The quantization error also occurs due to the finite resolution of the phase shifters. Generally, sidelobes are increased due to the quantization error. But still 5-bit phase resolution provides a reasonable approximation with the ideal case [48]. In the application of high precision radars that require high directivity and high suppression of sidelobes such as military radars, imaging systems, a low amplitude and phase errors are required.

The gain and phase errors of the proposed phase shifter are highly dependent on the amplitude and phase imbalances of the quadrature and differential signal generators. In the proposed system, both are based on 50Ω matched passive hybrids and are much tolerant to the loading effect as long as the load impedance is close enough to 50Ω. However, some degree of signal errors- amplitude and phase errors exist because of the layout parasitic effects in the lumped 180^0-hybrid and layout mismatches between through and coupled paths in the distributed 90^0-hybrid. In this section, the gain and phase errors by the hybrid networks and their impact on overall phase shift performance are analyzed.

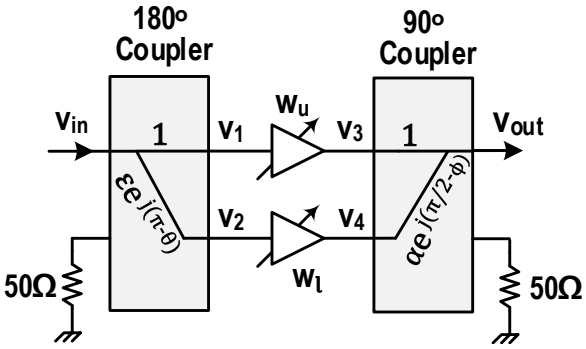


Figure 2.4: Analysis of gain and phase mismatches by passive 90^0 and 180^0 hybrid coupler in the power-mode vector modulator.

2.4.1 Gain and Phase Mismatches in the Hybrid Couplers

In Fig 2.4, ε and θ represent the gain and phase errors in the 180^0-hybrid. α and ϕ are the gain and phase errors between through and coupled paths in the 90^0-hybrid coupler. For simplicity, the power division factor of $1/\sqrt{2}$ has been normalized to unity for both couplers. Assuming that v_{in} is the input to the 180^0-hybrid coupler, the input and output of the weighting VGAs can be expressed as $v_1 = v_{in}, v_2 = v_{in}\varepsilon e^{j(\pi-\theta)}, v_3 = w_u v_{in}$, and $v_4 = w_l v_{in}\varepsilon e^{j(\pi-\theta))}$, where w_u and w_l express the weighting factors of the VGAs. Then, the output voltage, v_{out} is

$$\begin{aligned} v_{out} &= v_{in}\left\{w_u + \alpha\varepsilon w_l e^{j\left(\frac{3\pi}{2}-\theta-\phi\right)}\right\} \\ &= v_{in}\left(w_u - w_l\Delta n\sin\Delta\theta - jw_l\Delta n\cos\Delta\theta\right) \end{aligned} \tag{2.2}$$

where $\Delta n = \varepsilon\alpha$ is the total gain error and $\Delta\theta = \theta + \varphi$ is the overall phase deviation at the output from the desired phase shift of $3\pi/2$. The magnitude and phase of v_{out} is given by

$$|v_{out}| = w_l v_{in}\sqrt{\left(\frac{w_u}{w_l} - \Delta n\sin\Delta\theta\right)^2 + (\Delta n\cos\Delta\theta)^2} \tag{2.3}$$

and

$$\angle v_{out} = -\tan^{-1}\left(\frac{\Delta n\cos\Delta\theta}{\frac{w_u}{w_l} - \Delta n\sin\Delta\theta}\right) \tag{2.4}$$

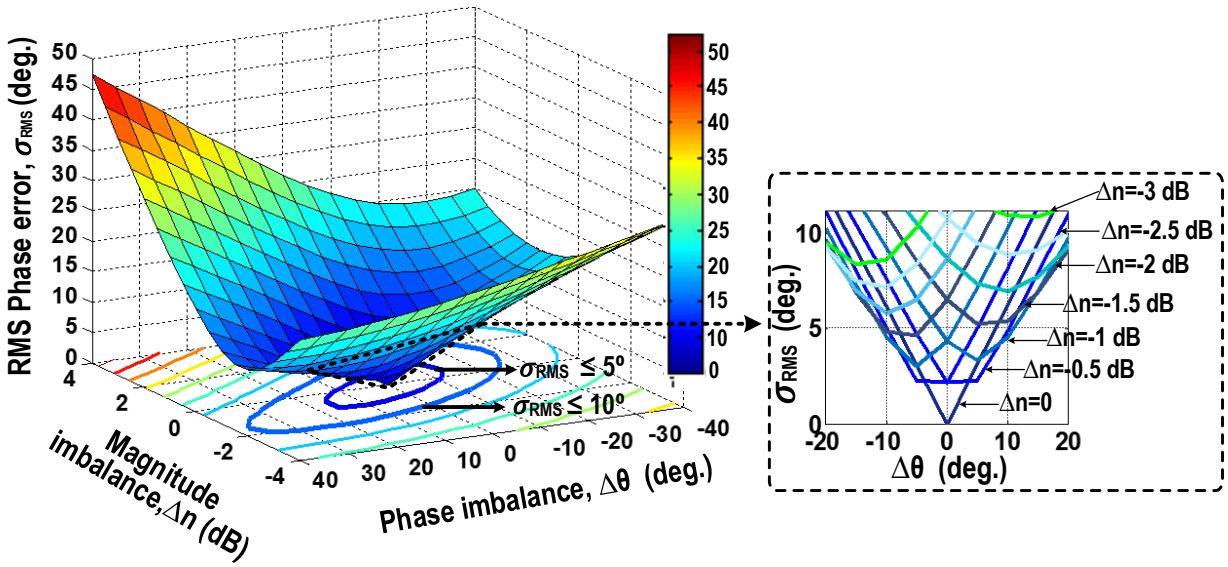
The phase error at the output can be expressed as:

$$\begin{aligned}\sigma_{error} &= \tan^{-1}\left(\frac{\Delta n\cos\Delta\theta}{\frac{w_u}{w_l}-\Delta n\sin\Delta\theta}\right)-\tan^{-1}\left(\frac{w_l}{w_u}\right)\\ &= \tan^{-1}\left(\frac{\Delta n\cos\Delta\theta\ -\ 1+\ \frac{w_l}{w_u}\ \Delta n\sin\Delta\theta}{\frac{w_u}{w_l}\ -\ \Delta n\ \sin\Delta\theta\ +\ \frac{w_l}{w_u}\ \Delta n\ \cos\Delta\theta}\right)\end{aligned} \tag{2.5}$$

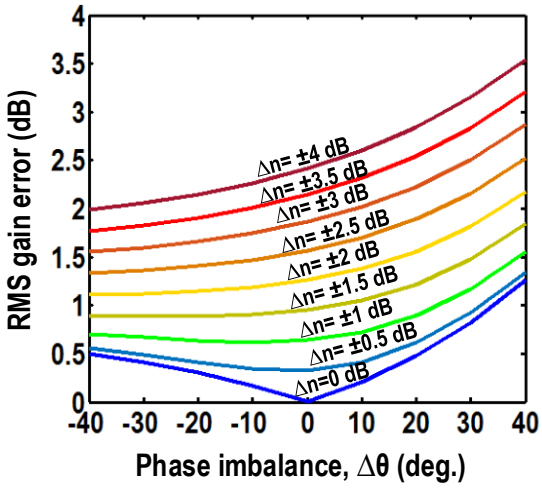
where $-tan^{-1}(w_l/w_u)$ is the desired phase shift at the output without any error. Fig 2.5 shows the contour plot of the calculated RMS phase error (σ_{RMS}) over the phase imbalance ($\Delta\theta$) and gain imbalance (Δn) with proper settings of $\frac{w_l}{w_u}$ ratios for 5-bit phase resolution in the 1^{st} quadrant phase domain (0^0 to 90^0 with 11.25^0 phase step). For N bit phase resolution, the maximum phase error (σ_{RMS}) should be $< 2\pi/2^{N+1}$ [49]. So, for 5-bit phase resolution, σ_{RMS} should be $< 5.625^0$ and for 4-bit phase resolution, σ_{RMS} should be $< 11.25^0$. It is seen from Fig 2.5(a) that, in order to maintain $\sigma_{RMS} < 5.625^0$, Δn should be $< \pm 2$ dB and $\Delta\theta$ should be $< \pm 14^0$. For 4-bit phase resolution, the RMS phase error remains less than 11.25^0 for $\Delta n < \pm 3^0$ dB and $\Delta\theta < \pm 20^0$.

The maximum and minimum gain can be obtained from (2.3) by setting the same w_l/w_u ratios as before for the 1^{st} quadrant phases. The maximum gain occurs when $w_l/w_u = 1$ while the minimum gain condition is at 0^0 or 90^0 phase state where $w_l/w_u \Longrightarrow 0$ or $w_l/w_u \Longrightarrow \infty$. Fig 2.5(b) shows the RMS gain error (G_{RMS}) of the phase shifter for 5-bit phase resolution versus $\Delta\theta$ at different Δn. Ideally, G_{RMS} is 0 dB without any gain and phase imbalances assuming a fine resolution DAC has been used in order to maintain same gain for all phase states. In order to keep $G_{RMS} < 2$ dB, the overall gain imbalance, Δn should be $< \pm 3$ dB and the phase imbalance, $\Delta\theta$ should be $< \pm 20^0$.

In this work, the hybrids are designed to have $\Delta\theta < 10^0$ over the frequency range of 90-100 GHz in targeting 5-bit phase resolution. The lumped 180^0-hybrid and distributed 90^0-hybrid coupler provide < 0.5 dB and < 1.2 dB of gain mismatches, respectively, resulting in $\Delta n < 1.7$ dB at 94 GHz after electromagnetic (EM)-wave simulations of hybrids using EM software (SONNET) [50].



(a)



(b)

Figure 2.5: (a) 3-D plot of RMS phase error (σ_{rms}) with respect to magnitude imbalance and phase imbalance of hybrid couplers, 2D plots shows σ_{rms} versus phase imbalance at different magnitude error (Δn) for $\sigma_{rms} < 11^0$, (b) RMS gain error versus phase imbalance $\Delta\theta$ for different levels of gain mismatches (Δn).

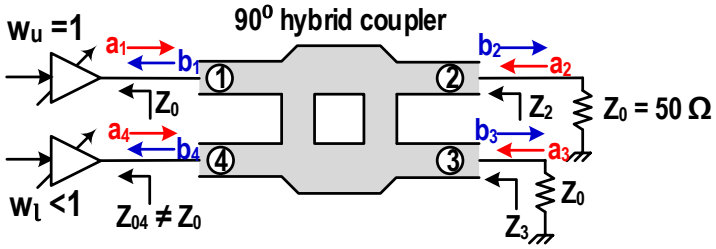


Figure 2.6: Variation of load at port 4 (Z_{04}) in 90^0 hybrid coupler when VGA gain changes while other ports are matched with load Z_0=50Ω.

2.4.2 Effect of Impedance Variations at the Input of the 90^0 Hybrid Coupler

In general, the output impedance of the weighting VGA, Z_{out} is matched with the input of the 90^0-hybrid when the VGA exhibits reasonable gain performance, i.e. Z_{out} = 50Ω. However, when the VGA gain setting is low, Z_{out} deviates from the matched condition, causing the different driving impedance to the quadrature hybrid. The worst case driving impedance disturbance at the input of the 90^0-hybrid happens when one VGA is nearly turned OFF (during 0^0 or 90^0 phase state).

In Fig 2.6, the S-parameter matrix of 90^0 -hybrid is given by [51]

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = -\frac{1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} \rightarrow \left\{ \begin{array}{l} b_1 = -\frac{1}{\sqrt{2}}(ja_2 + a_3) \\ b_2 = -\frac{1}{\sqrt{2}}(ja_1 + a_4) \\ b_3 = -\frac{1}{\sqrt{2}}(a_1 + ja_4) \\ b_4 = -\frac{1}{\sqrt{2}}(a_2 + ja_3) \end{array} \right\} \tag{2.6}$$

where, a_1 and b_1 are the incident and reflected waves at port ① which is connected to the VGA at nominal gain state. a_{2-4} and b_{2-4} are reflected and transmitted waves at ports ②, ③ and ④. The reflection coefficient at port ④ ($\Gamma_4 = a_4/b_4$) will not be zero if it experiences a load variation from 50Ω while other ports are matched to $Z_0 = 50\Omega$. Assuming the two input ports of 90^0-hybrid (port ① and ④) are isolated enough to have negligible b_4/a_1, the following can be derived from (2.6),

$$\Gamma_{21} = \frac{b_2}{a_1} = \frac{-1}{\sqrt{2}} \left(j + \frac{b_4}{a_1}\Gamma_4 \right) \approx \frac{-j}{\sqrt{2}} \tag{2.7}$$

$$\Gamma_{31} = \frac{b_3}{a_1} = \frac{-1}{\sqrt{2}}\left(1 + j\frac{b_4}{a_1}\Gamma_4\right) \approx \frac{-1}{\sqrt{2}} \tag{2.8}$$

which show that the transmission coefficients, Γ_{21} and Γ_{31} are still 90^0 out of phase, even though the port ④ is not matched. From (2.6), we can further write,

$$\begin{aligned} &\frac{b_4}{a_1} = \frac{-1}{\sqrt{2}}\left(\frac{b_2}{a_1}\Gamma_2 + j\frac{b_3}{a_1}\Gamma_3\right) = 0 \\ &\Rightarrow \Gamma_2 + \Gamma_3 = 0 \\ &\Rightarrow \frac{Z_0 - Z_2}{Z_0 + Z_2} + \frac{Z_0 - Z_3}{Z_0 + Z_3} = 0 \end{aligned} \tag{2.9}$$

$$\Rightarrow {Z_0}^2 = Z_2 Z_3 \tag{2.10}$$

where $\Gamma_2 = a_2/b_2$ and $\Gamma_3 = a_3/b_3$ are the reflection coefficients at ports ② and ③. Z_2 and Z_3 are the equivalent impedances looking into the ports ② and ③. Note that Z_2 and Z_3 can vary depending on the unmatched load at port ④ but their impedance variation relationship follows (2.10), inversely proportional to each other. Under a reasonable driving impedance variation at port ④, both impedance loci of Z_2 and Z_3 can stay inside same reflection coefficient circle, for instance, S_{22} & $S_{33} < -10$ dB circle, in the Smith chart, causing negligible reflection power loss to the following amplifier stages.

These analyses are verified by simulations using W-band 90^0-hybrid coupler where the isolation (S_{41}) is finite (-25 dB) and the load at port ④ (Z_{04}) is changed in resistive, inductive or capacitive ways. The phase differences between port ② and ③ are plotted over different Z_{04} in Fig 2.7(a). It is seen that the variation of the load has little effect on the overall phase difference and remains close to 90^0 for a wide variation of Z_{04}. Thus, the I/Q imbalance of the proposed phase shifter is robust against impedance variation of different phase states. Fig 2.7(b) shows when Z_{04} varies over 30-150 Ω, the Z_2 and Z_3 changes from 30 to 60 Ω, resulting in < -10 dB of reflection coefficients (Γ_2 and Γ_3).

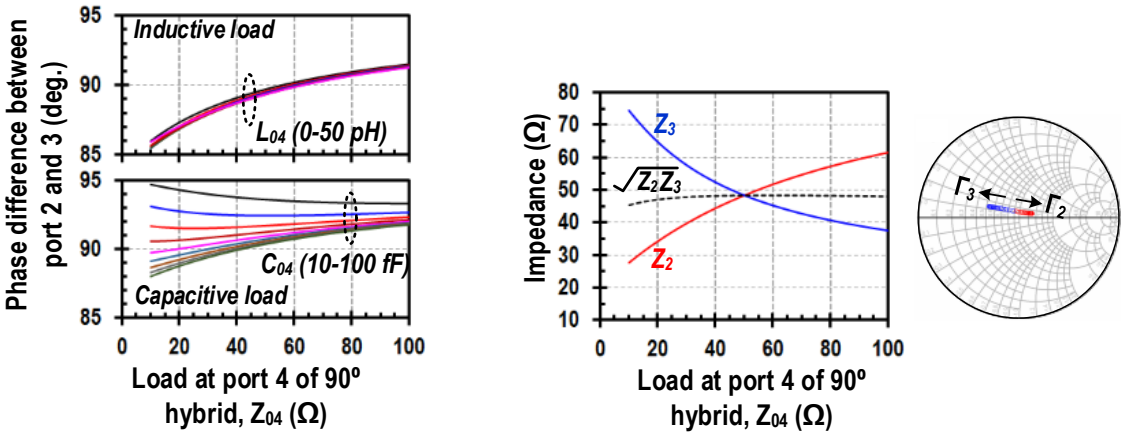


Figure 2.7: (a) Phase difference between two output ports (port 2 and 3) when load Z_{04} varies in inductive and capacitive way with respect to real value of Z_{04}, and (b) impedance variation at port 2 and 3 looking towards hybrid coupler shows inverse relationship between Z_2 and Z_3 when Z_{04} changes resistively.

2.5 Building Block Design of T/R Module

The phasing system is implemented in IBM 0.13μm BiCMOS technology of f_T = 200 GHz [52]. The transistor peak f_T degrades upto 180 GHz when considering transistor interconnections, done in SONNET (see Fig 2.8). The process (IBM8HP) has seven metal stacks with the top two being thick aluminium metal layers (AM and LY layer). All the interconnections are realized using coplanar waveguide with 10μm signal width and 12μm spacing ground (MQ metal layer as the bottom ground plane). All the inductors are in AM layer with M1 ground plane. The custom-made 50Ω matched GSG pads are designed at the input and output for testing purpose. In order to minimize the associated parasitic inductance, wide metal planes with multiple metal layers connected with vias are used for supply (VCC) and ground (GND). To prevent potential low-frequency oscillation, multiple low Q-capacitor banks with the different range of capacitances are inserted between the VCC and GND planes.

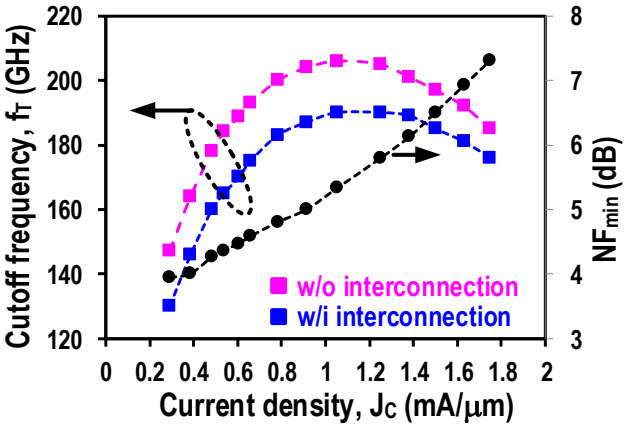


Figure 2.8: Transistor cutoff frequency and NFmin (at 94 GHz) verses current density.

2.5.1 Design of Low Noise Amplifier (LNA)

The LNA is designed based on the cascode topology because of its high reverse isolation and improved stability (see Fig 2.9(a)). The design of VGA is the same as LNA except the variable gain function is realized by steering bias current from the main signal path by controlling $I_{control}$ using DAC (see Fig 2.9(b)). The emitter length of Q_1 and Q_2 is 6 μm and the maximum bias current is 4 mA from 2.2 V supply. All the transistor interconnects and inductors are modeled using SONNET EM simulator. After including all layout interconnects, the transistor cutoff frequency is 170 GHz at operating bias point (see Fig 2.8). Fig 2.9(c) shows full SONNET layout of the LNA. High Q metal-oxide-metal (MOM) capacitor is used instead of MIM capacitor for output matching. The bypass capacitor ($C_B \approx 660fF$) is added immediately after the load inductor to avoid any parasitic inductance at the VCC interconnection and to make a solid AC ground at 94 GHz. The simulated gain of LNA is 11 dB and NF is 7.2 dB. The VGA gain ranges $-20 \sim 10$ dB (see Fig 2.10(a)). The output reflection coefficient (S_{22}) remains below -10 dB for all the gain states of VGA.

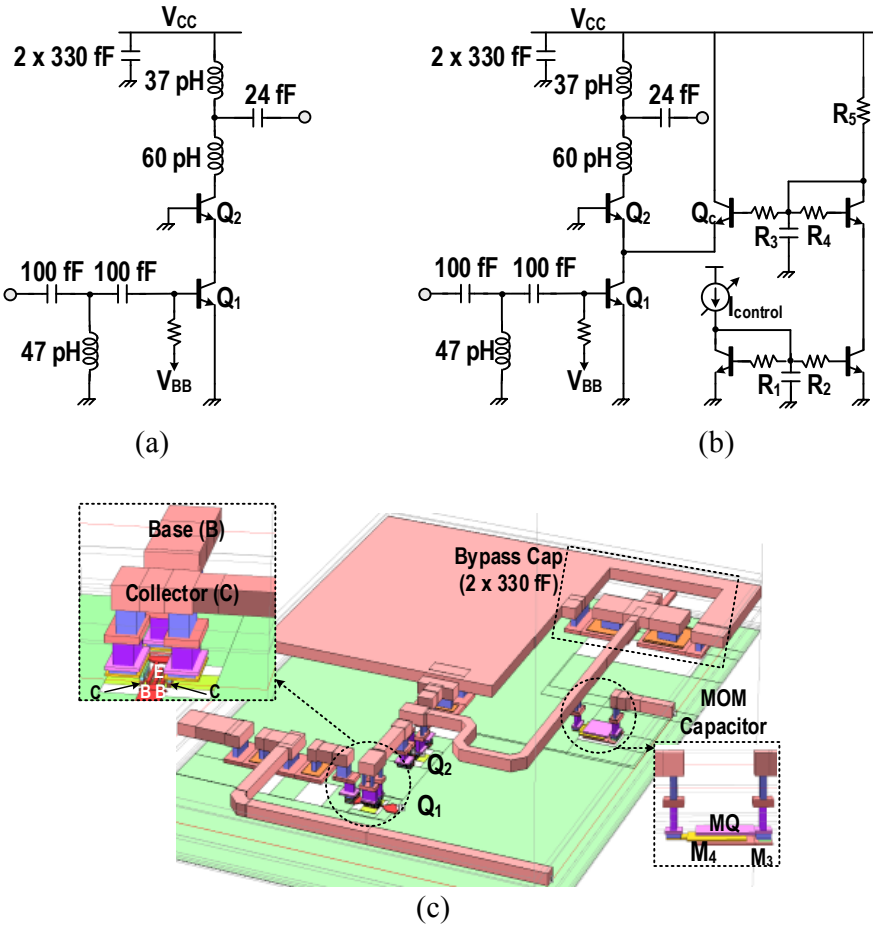


Figure 2.9: Schematic of (a) LNA, (b) VGA and (c) SONNET layout of LNA showing the transistor interconnection and MOM capacitor at output.

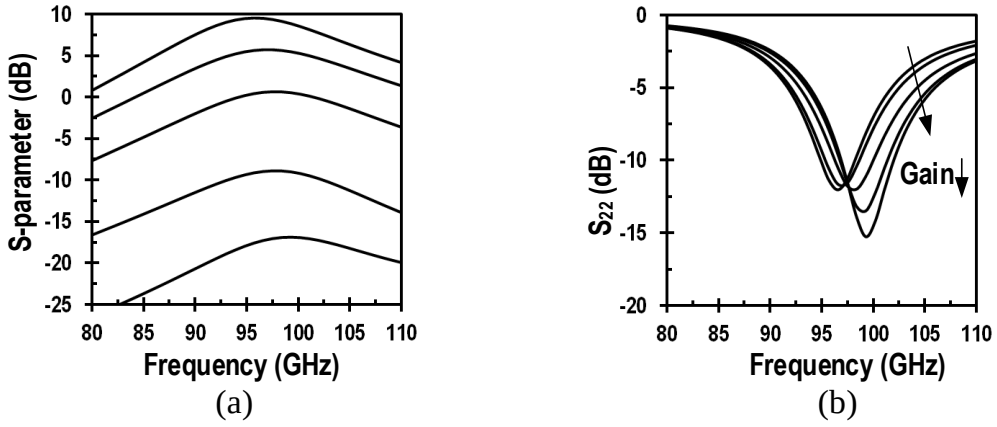


Figure 2.10: (a) Gain and (b) S_{22} of VGA at different gain states.

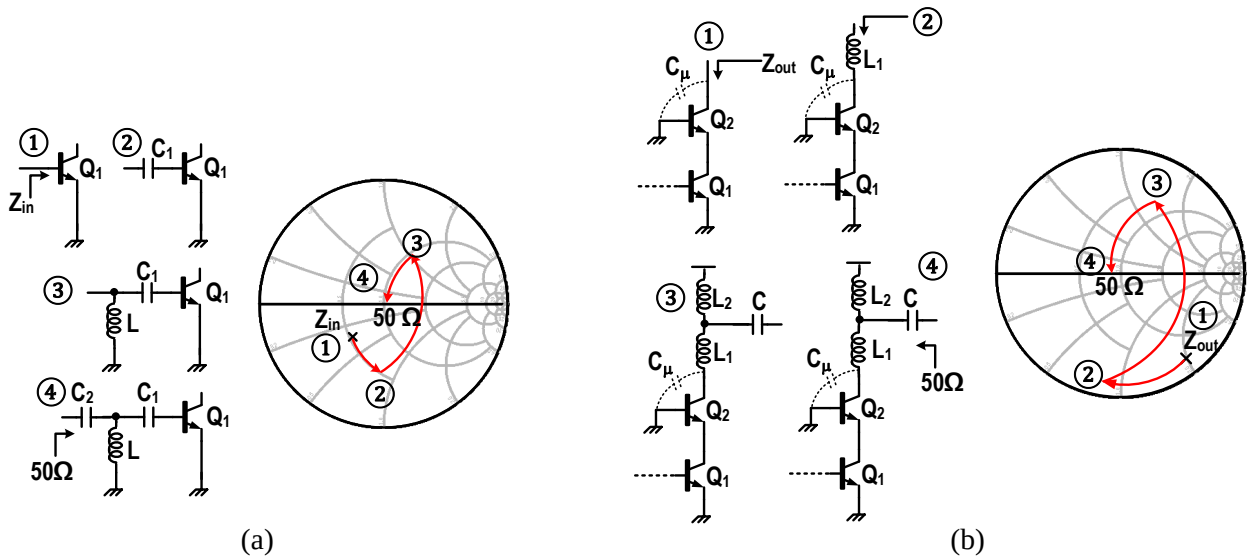


Figure 2.11: Step-by-step design procedure of (a) input and (b) output matching networks.

Design of Matching Network:

Fig. 2.11 describes the design of input and output matching network in smith chart. Input impedance can be expressed as, $Z_{in} = R_i - \frac{j}{\omega C_i}$. Here, $Z_{②,in} = R_i - \frac{j}{\omega C_{eq}}$.

$$\begin{aligned} Z_{③,in} &= \frac{\left(R_i - \frac{j}{\omega C_{eq}}\right) \times j\omega L}{R_i - \frac{j}{\omega C_{eq}} + j\omega L} \\ &= \frac{j\omega L R_i + \frac{L}{C_{eq}}}{R_i + j\left(\omega L - \frac{1}{\omega C_{eq}}\right)} \\ &= \frac{\frac{L}{C_{eq}}}{R_i + j\left(\omega L - \frac{1}{\omega C_{eq}}\right)} + \frac{j\omega L R_i}{R_i + j\left(\omega L - \frac{1}{\omega C_{eq}}\right)} \end{aligned} \tag{2.11}$$

At resonance, $\omega = \frac{1}{\sqrt{LC_{eq}}}$. Then $Z_{④,in} = \frac{L/C_{eq}}{R_i} + j\omega L - \frac{j}{\omega C_2}$,

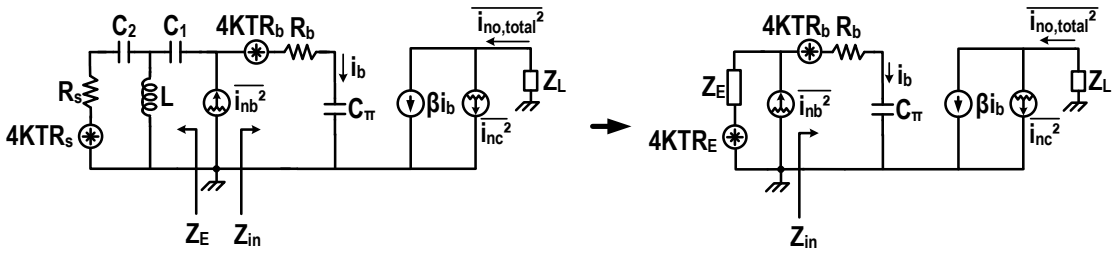


Figure 2.12: Noise equivalent circuit of the transistor with input matching network.

which results $\omega = \frac{1}{\sqrt{LC_2}} = \frac{1}{\sqrt{LC_{eq}}}$. So at matching condition, $Z_{④,in} = \frac{L/C_{eq}}{R_i} = 50\Omega$.

For the output impedance matching network, Z_{out} is mainly capacitive because of small $C\mu$, so large inductor L_2 is needed (>150 pH) for output matching. In order to improve Q of the matching network, a series inductor L_1 is used to decrease the effect of capacitance looking from ②, thus the required L_2 becomes lower to resonate out the output capacitance. If $Z_{out} = R_0 - \frac{j}{\omega C_{\mu s}}$, similar expression can be obtained for output impedance matching network,

$Z_{④,out} = \frac{L_2/C'}{R_0} + j\omega L_2 - \frac{j}{\omega C}$,

where $Z_{②,out} = R_0 - \frac{j}{\omega C_{\mu s}} + j\omega L_1 \approx R_0 - \frac{1}{\omega C'}$.

The resonance condition for output matching network is, $\omega = \frac{1}{\sqrt{CL_2}} = \frac{1}{\sqrt{LC'}}$

and at matched condition $Z_{④,out} = \frac{L_2/C'}{R_0} = 50\Omega$.

Noise Analysis of LNA:

Generally, the optimum noise matching impedance of the transistor is different than 50Ω. For BJT, base shot noise and collector shot noise are the dominant noise source. They can be expressed as, $\overline{i_{nb}^2} = 2qI_b\triangle f$ and $\overline{i_{nc}^2} = 2qI_C\triangle f$, respectively. The equivalent circuit for noise analysis is shown in Fig. 2.12. The analysis is done to have optimum C_1-L-C_2 network to have simultaneous noise and impedance matching. For simplification, noise voltage, $4kTR_E$ is used as an input noise source where Z_E is the equivalent impedance looking towards the source after adding matching network.

The noise contribution at the output due to base resistance (R_b), $\overline{i^2_{onRb}} = \dfrac{4KTR_b}{(Z_E + Z_{in})^2} \times \beta^2$, where $\beta = g_m/sC_\pi$ and $Z_{in} = R_b - 1/sC_\pi$. R_b is assumed to be very small compared to Z_E and Z_{in}.

The output noise contribution due to the source noise, $\overline{i^2_{onRE}} = \dfrac{4KTR_E}{(Z_E + Z_{in})^2} \times \beta^2$.

The output noise contribution due to the base shot noise, $\overline{i^2_{onb}} = (\dfrac{Z_E}{Z_E + Z_{in}})^2 \times \overline{i^2_{nb}} \times \beta^2$.

So the total output noise current, $\overline{i^2_{no,total}} = \overline{i^2_{nc}} + \overline{i^2_{onRb}} + \overline{i^2_{onRE}} + \overline{i^2_{onb}}$.

The Noise figure can be expressed as,

$$
\begin{aligned}
F &= \frac{\overline{i_{no,total}}^2}{\overline{i_{onRE}}^2} \\
&= \frac{\overline{i_{nc}}^2 + \dfrac{4kTR_b}{(Z_{in} + Z_E)^2} \times \beta^2 + \dfrac{4kTR_E}{(Z_{in} + Z_E)^2} \times \beta^2 + (\dfrac{Z_E}{Z_{in} + Z_E})^2 \times \overline{i_{nb}}^2 \times \beta^2}{\dfrac{4kTR_E}{(Z_{in} + Z_E)^2} \times \beta^2} \\
&= 1 + \frac{R_b}{R_E} + \frac{Z_E{}^2}{4kTR_E} \times \overline{i_{nb}}^2 + \frac{(Z_{in} + Z_E)^2}{4kTR_E \times \beta^2} \times \overline{i_{nc}}^2 \\
&= 1 + \frac{R_b}{R_E} + \frac{Z_E{}^2}{4kTR_E} \times \left\{ \overline{i_{nb}}^2 + (1 + \frac{Z_{in}}{Z_E})^2 \times \frac{\overline{i_{nc}}^2}{\beta^2} \right\} \\
&= 1 + \frac{R_b}{R_E} + \frac{Z_E{}^2}{4kTR_E} \times \left\{ 2qI_b + (1 + \frac{Z_{in}}{Z_E})^2 \times \frac{2qI_c}{\beta^2} \right\}
\end{aligned}
\tag{2.12}
$$

The optimum noise source impedance can be obtained by differentiating equation (2.12) with respect to Z_E. The matching network C_1, L and C_2 is designed to have optimum input noise source impedance (Z_{Eopt}).

2.5.2 90^0- and 180^0-Hybrid Couplers with Measurement Results

The 90^0-hybrid coupler is based on distributed structure (see Fig 2.13). The 35Ω quarter-wavelength T-lines in the AM layer are meandered to reduce the overall footprint of the hybrid (size: $180\mu m \times 430\mu m$). The LY layer is used as ground plane, which results in the minimum width of signal lines ($4\mu m$ of AM layer for 50Ω and $9.5\mu m$ for 35Ω T-lines), decreasing the size of the hybrid further.

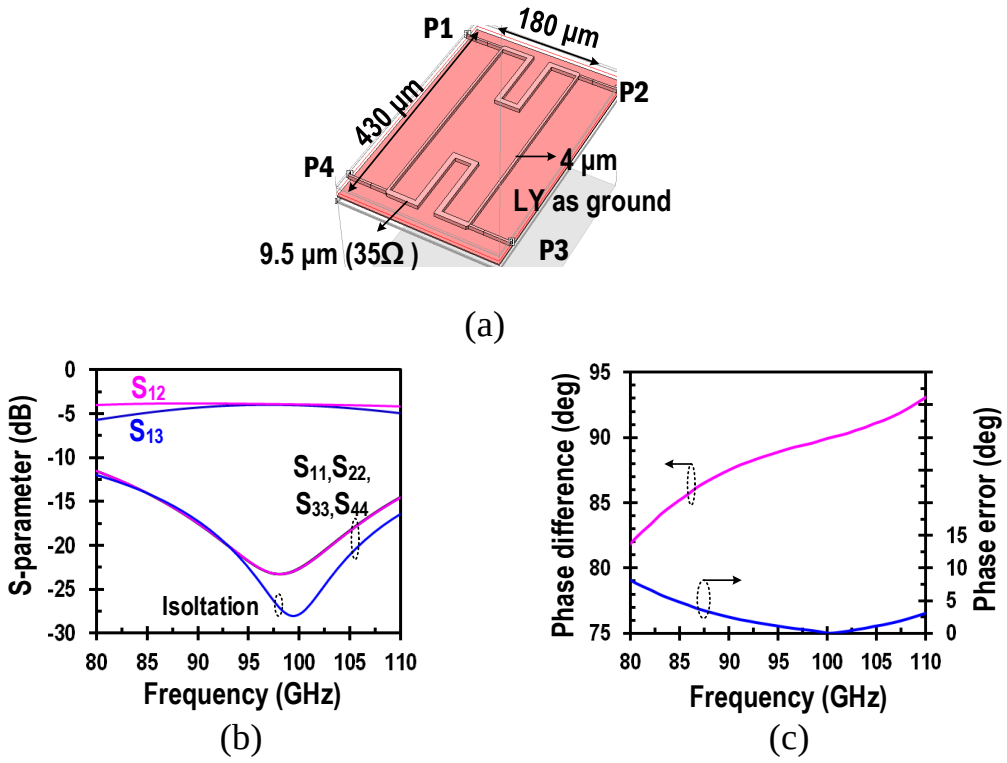


Figure 2.13: (a) S-parameter simulation and (b) phase response and phase error of 90^0-hybrid coupler with SONNET layout (size: 185×430 μm^2).

The loss of the 90^0-hybrid coupler is 1∼1.5 dB and phase error is $< 5^0$ over 84-118 GHz in the simulation (see Fig 2.13(b) and (c)). Input and output reflection coefficients, S_{11} and S_{22} remain < -10 dB for wide frequency range, 80-110 GHz. In order to reduce the area of the 180^0-hybrid coupler, it is designed with lumped components [53]. The schematic and layout of lumped hybrid is shown in Fig 2.14. The overall size of the 180^0-hybrid is $245\mu m \times 345\mu m$, which is much smaller than the distributed structure in the IBM PDK model ($320\mu m \times 500\mu m$). The hybrid layout has been done carefully to have the same loss at ports 2 and 3 at 94 GHz. The M1 layer is used as ground and the cell is shielded by AM ground layer. The inductance (L) and capacitance (C_2) are determined by the equation: $\omega L = 1/\omega C_2 = \sqrt{2}Z_0$. For Z_0 = 50Ω at 94 GHz, L=120pH and C_2 = 24fF. Fig 2.14(b) and (c) show the measured S-parameter results of 180^0-hybrid. The loss is 0.7 dB at 94 GHz and less than 1.5 dB over 90-100 GHz. The phase error is $< 8^0$ at 90-110 GHz.

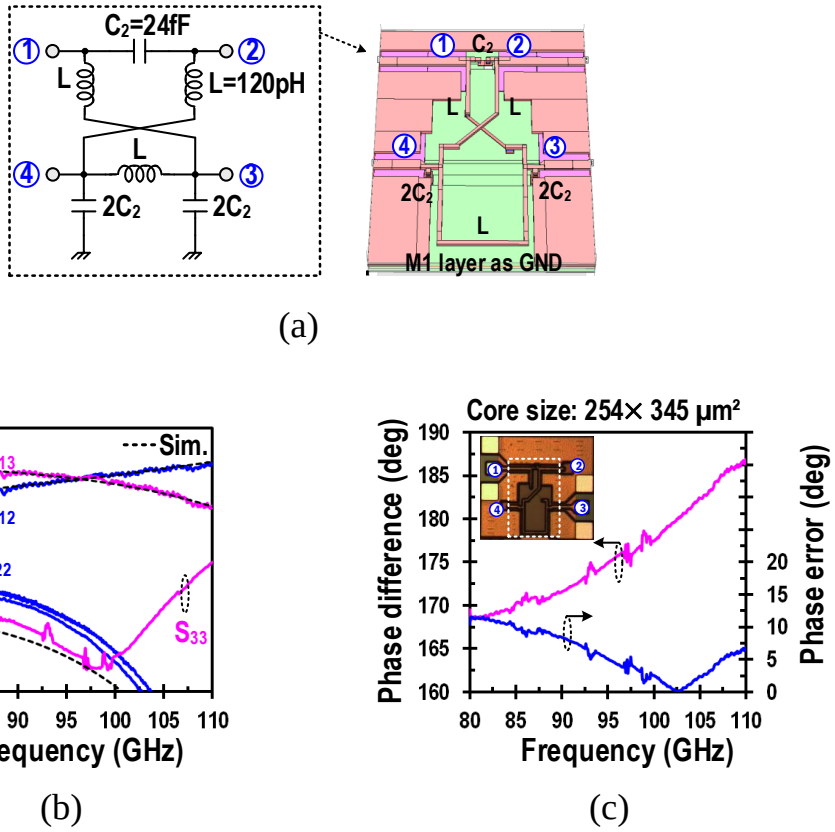


Figure 2.14: (a) Schematic and SONNET layout, Measured: (b) S-parameter results and (c) phase difference and RMS phase error between port 2 and 3 of 180-deg lumped hybrid coupler (core size: 245×345 μm^2).

The measured S_{11} and S_{22} are < -10dB for a wide frequency range of 85-105 GHz.

2.5.3 Phase Selection Stages: Loss Compensation Amplifier and SPDT Switch

Loss Compensation Amplifier: The amplifier topology in phase selection stages are the same as LNA with optimization of input/output matching networks based on different layout parasitics. The amplifier has two bias setting conditions: the PMOS M1 and R1 (see Fig 2.15(a)) set a nominal bias current when it needs the maximum gain. For minimizing DC power consumption, amplifiers should be turned OFF when non-selected condition. In order to keep input reflection coefficient

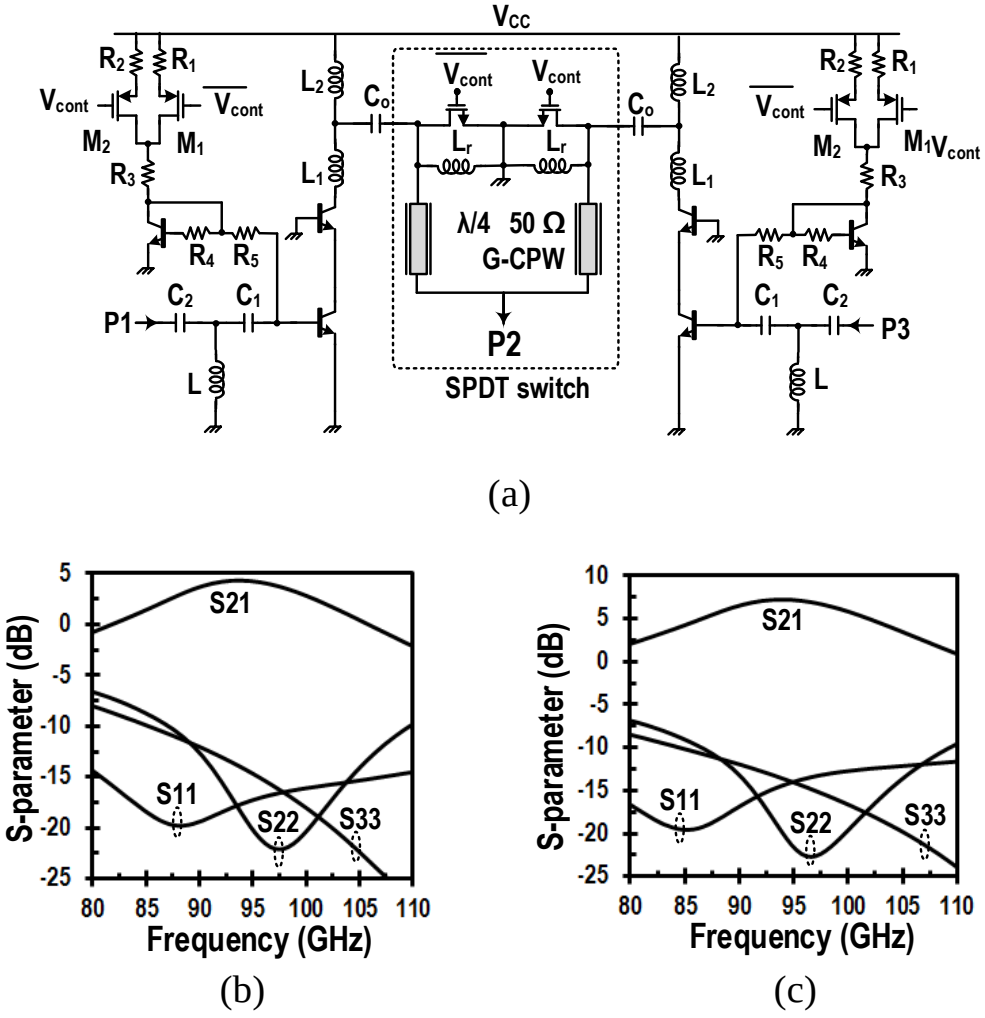


Figure 2.15: Loss compensation amplifier with SPDT: (a)schematic and (b) S-parameter simulation results.

< -10 dB at OFF state amplifier, a small bias current ($\sim 90\mu A$) has been applied, which is set by M2 and R2. Thus it ensures minimal power consumption and low quadrature phase error from the 90^0-hybrid couplers. The Tx and Rx loss compensation amplifier topologies are the same. For Rx, the pre- and post- selection amplifiers are biased with maximum 4 mA current resulting in 8 dB gain including the SPDT switch (see Fig 2.15(b)). The total DC power consumption by the loss compensation amplifiers for Rx is 18 mW. The amplifier gain in the post-selection stage can also be controlled to reduce the gain variation across the different phase states. For Tx phase shifting system, the gain of the pre-selection amplifier is reduced to 5 dB to improve the linearity, consuming 3.5 mW DC power. The reflection coefficients of all the ports remain below -10 dB at both ON and OFF condition of the amplifier.

SPDT switch: The I/Q signals from amplifiers are selected by SPDT switch as shown in Fig 2.15(a). The SPDT switch is designed using $\lambda/4$, 50Ω grounded co-planar waveguide which provides a high impedance at the output when low impedance occurs at the input side, i.e. when the NMOS switch is ON [54]. The NMOS size ($40\mu m/0.12\mu m$) is optimized for low loss (<2.7 dB). The OFF state parasitic capacitance of the NMOS is resonated out by an inductor L_r (∼95pH). The isolation between two input ports remain < -18 dB at 90-100 GHz.

2.5.4 Simulation Performance of the Phase Shifter

The simulated gain of Tx phase shifter is 7-11 dB with $< 5^0$ RMS phase error at 90-100 GHz. The output P_{-1dB} (OP_{-1dB}) is -3.7 dBm and saturated output power (P_{sat}) is 0 dBm at the highest gain state (see Fig 2.16). The phase response from 0^0 to 90^0 with 11.25^0 phase step at various input power levels is shown in Fig 2.16(b). The RMS phase error remains $< 10^0$ up to the input power level -5 dBm, which corresponds to saturated output power. Thus, the phase shifter maintains 4-bit operation close to the saturation condition. The Rx channel (LNA+phase shifter) gain is 21-25 dB at 94 GHz. The RMS gain error is <1.5 dB and RMS phase error is $< 6^0$ over 32 phase states at 92-100 GHz. The simulated NF varies 9.5-10.5 dB for all over the phase states. The input P_{-1dB} is -26 dBm at the highest gain state of the receiver.

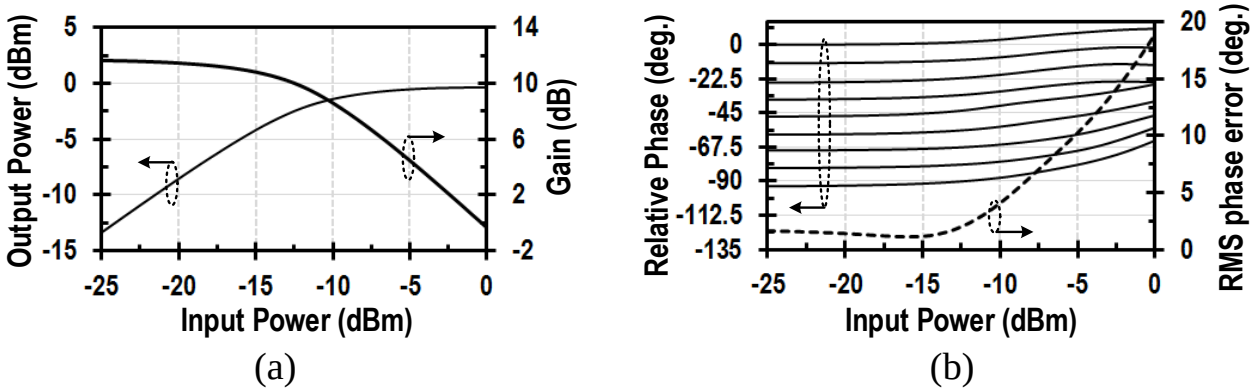


Figure 2.16: Simulated (a) output power and power gain, (b) relative phase from 0^0 to 90^0 (at 1^{st} quadrant) and RMS phase error verses input power of transmitter phase shifter.

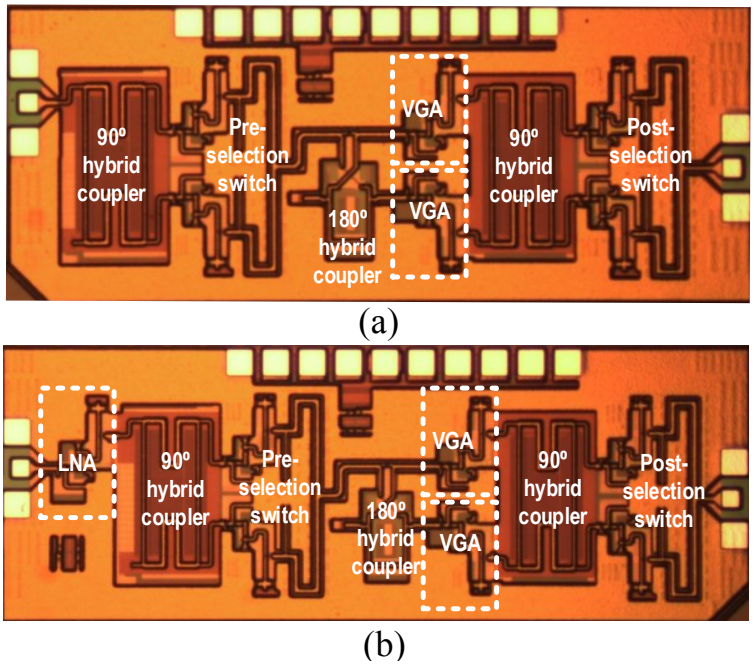


Figure 2.17: Chip photos: (a) transmitter phase shifter (chip size: $1.55\times0.55\ mm^2$) and (b) receiver single channel (chip size: $1.65\times0.55\ mm^2$).

2.6 Measurement Results

Fig 2.17 shows the chip photographs of the Tx phase shifter and receiver channel. The Tx phase shifter chip size is 1.55×0.55 mm^2 and Rx channel size is 1.65×0.55 mm^2 excluding pads. The S-parameters are measured on the wafer after standard GSG SOLT calibration using a 4-port network analyzer (R&S ZVA24) with W-band frequency extender (R&S ZVA-Z110). The input and output GSG pad losses (about 1 dB) are de-embedded from the measurement data.

2.6.1 Transmitter Phase Shifter

Fig. 2.18 shows the measured S-parameter results for 5-bit phase states of the phase shifter. The peak gain is 7.7-11 dB depending on the phase states and shifted to 97 GHz. The average gain is 9 dB at 97 GHz. The frequency shifting may be because of the variation in custom made MOM capacitor at the output of amplifiers. The measured gain is 4.8-9.7 dB with RMS gain error 1.5 dB at 94 GHz. The gain error remains $<$ 1.6 dB over 93-108 GHz. The measured RMS phase error for 5 bit phase response is $< 4^0$ over 92-98 GHz and $< 9^0$ over 88-100 GHz. S_{11} and S_{22} are below -10 dB over 85-110 GHz. A careful measurement has been conducted for linearity testing: Fig 2.19 shows the measurement set-up for measuring compression point at W-band. Here, all the losses at input and output including waveguide sections, attenuator and probe loss have been characterized and de-embedded from measurement data. The power measurement has been done by using two W-band power sensors for input and output side of DUT (Agilent W8486A) and a dual channel power meter (Keysight N1912A). The measurement result (see Fig. 2.20(a)) shows, OP_{-1dB} is -4 dBm at the highest gain state at 94 GHz which is close to the simulation. The OP_{-1dB} varies from -5.6 to -3.5 dBm over 16 phase states which are enough to drive PA (Fig. 2.20(b)). The DC power consumption of the phase shifter is 31 mW from 2.2 V supply voltage. Table 2.1 summarizes the performance and comparison of the Tx phase shifter with different kind of RF phase shifting scheme. The comparison shows the proposed phase shifter can have low power consumption with high gain and comparable linearity performance compared to other PS

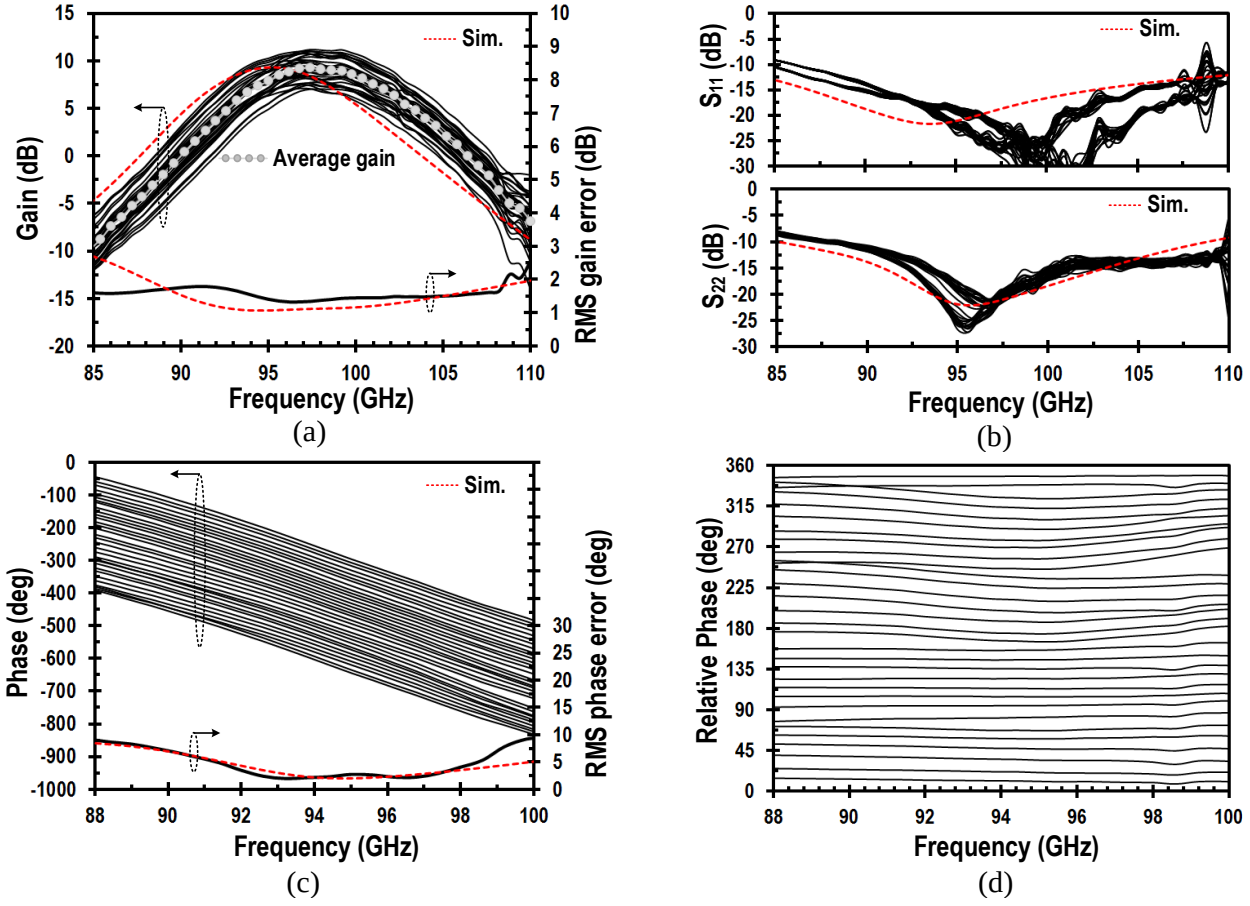


Figure 2.18: Measured: (a) Gain (S_{21}), (b) input (S_{11}), output (S_{22}) reflection coefficients, (c) absolute phase response and RMS phase error, and (d) relative phase versus frequency for 32 phase states of the transmitter phase shifter.

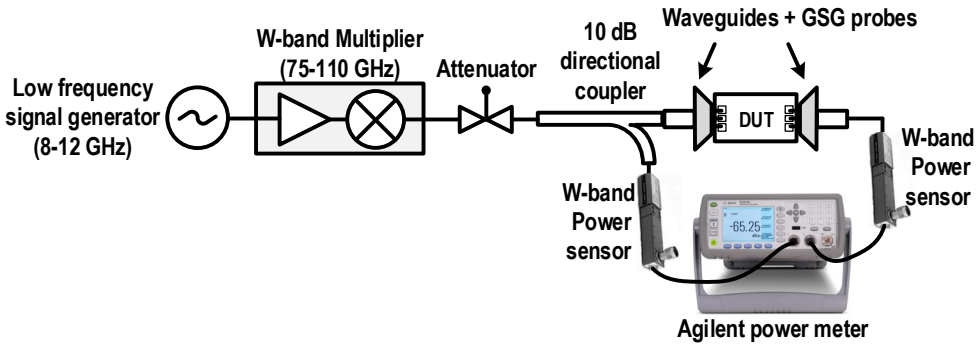


Figure 2.19: Measurement set-up for linearity measurement at W-band.

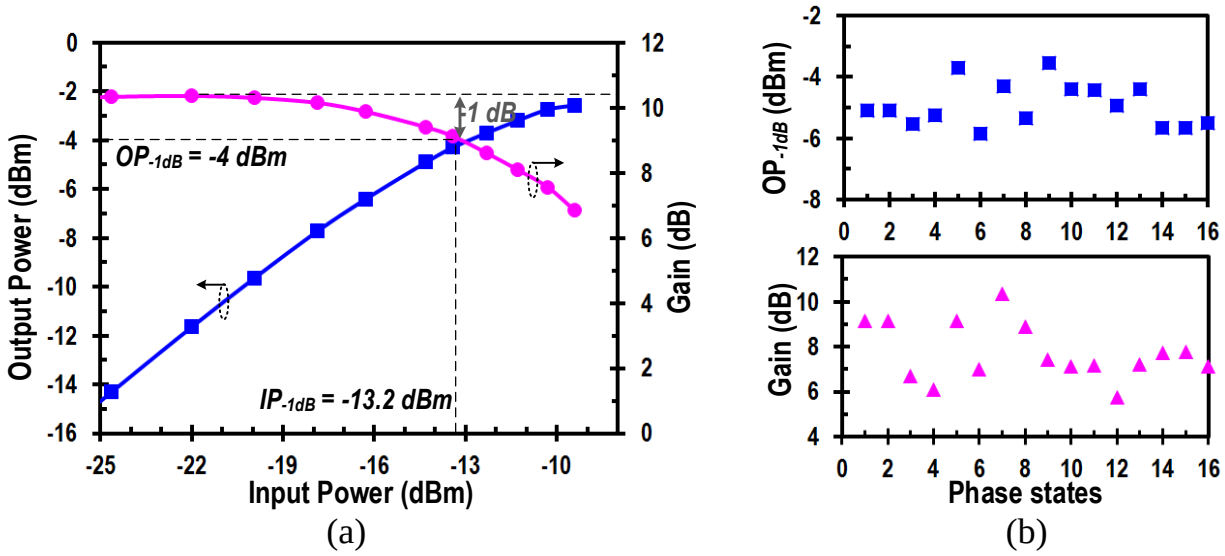


Figure 2.20: Measured: (a) Output P-1dB (OP_{-1dB}) and gain versus input power at 94 GHz at highest gain state and (b) OP_{-1dB} and gain over 16 phase states of the transmitter phase shifter.

architectures.

2.6.2 Receiver Front-end

The LNA test chip size is 280×140 μm^2 excluding I/O pads. Fig 2.21 shows the S-parameter measurement results of LNA test chip. The peak gain is 11.6 dB at 90 GHz. At 94 GHz, the measured gain is 10 dB. S_{11} is < -10 dB over 80-110 GHz. The high-Q MOM capacitor at the output matching network results in a narrow band S_{22}, but still, keeps < -5 dB for 90-100 GHz. The NF is measured by using a W-band noise source and the output signal from DUT is down-converted to IF frequency (780 MHz) using a W-band mixer as shown in Fig 2.22. The IF signal is then amplified by an LNA followed by a band-pass filter (BPF) before being measured by a spectrum analyzer (R&S FSW67). The noise calibration is performed including waveguides + mixer + IF LNA + IF BPF and W-band amplifier is required to suppress the noise contribution by the mixer which has loss >15 dB at 94 GHz. LNA NF is 7 dB at peak gain frequency (90 GHz) and 7.5 dB at 94 GHz. The measured IP_{-1dB} of the LNA is -14 dBm with 9 mW power consumption.

Table 2.1. Performance summary and comparison of the Tx PS

Reference	This work	TMTT 2014 B.H.Ku *et al.* [26]	TMTT 2013 Golcuk *et al.* [28]	TMTT 2015 Natarajan *et al.* [29]
Frequency (GHz)	90-100	76-84	90-100	88-96
PS Type	Passive VM (Power Combining)	Active VM (Current Combining)		RTPS
Process	0.13 µm SiGe BiCMOS	0.13 µm SiGe BiCMOS	0.13 µm SiGe BiCMOS	0.13 µm SiGe BiCMOS
Gain (dB)	7.7 ~ 11	-7	3.5	5 ~ 8
Phase resolution	5	5	4	5
RMS gain error (dB)	< 1.8	< 1.5	< 1.2	< 2.5
RMS phase error	< 4°	< 11°	< 5°	< 12°
OP_{-1dB} (dBm)	-3.5	1 (Sim.)	-7	N/A
Power consumption (mW)	31	30	40	> 45

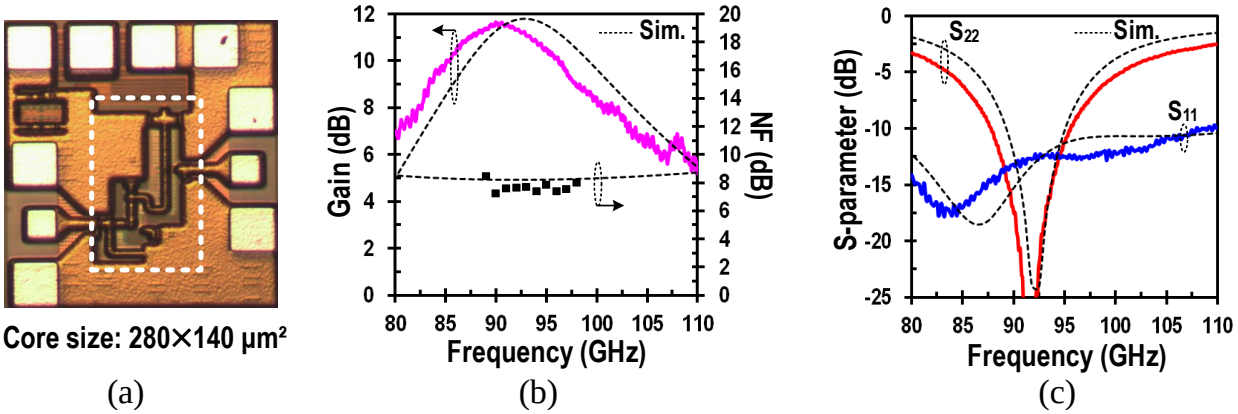


Figure 2.21: (a) Chip photo of LNA (the core size: $280\times140\ \mu m^2$), measurement results of LNA: (b) Gain and NF and (c) Input (S_{11}) and output (S_{22}) reflection coefficients versus frequency .

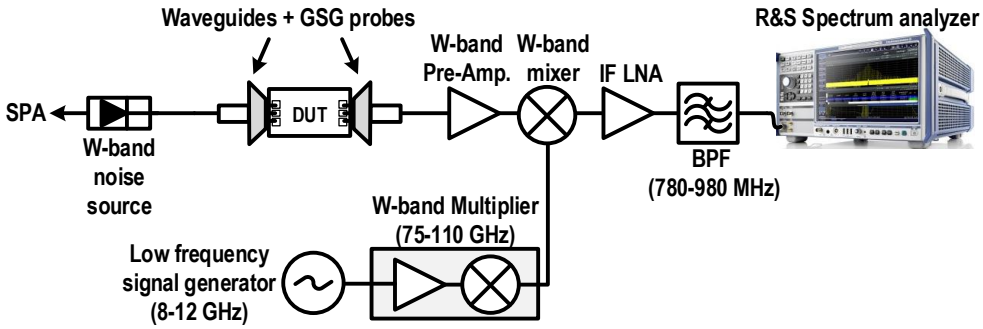


Figure 2.22: Measurement set-up for Noise Figure measurement at W-band.

Fig 2.23(a)-(c) shows the measured S-parameter results of the single channel receiver for 32 phase states. The peak gain is 23-26 dB at 96 GHz and 3-dB bandwidth is 92-100 GHz. At 94 GHz, the gain is 21-25 dB and the average gain is 22 dB. The RMS gain error is 1.4 dB at 94 GHz and remains below 1.8 dB for 92-100 GHz. S_{11} and S_{22} are better than -10 dB over 85-105 GHz. Fig 2.23(c) shows 5-bit phase response of Rx. The RMS phase error is 2.5^0 at 94 GHz and lower than 8^0 for 88-98 GHz. The measured NF is 9.3-11 dB over 16 phase states at 94 GHz as shown in Fig 2.23(d). It is observed that as the frequency deviates from the design center frequency (94 GHz), the error between the measured and simulated NF becomes higher. This is mainly because no W-band amplifier was used before the mixer which causes less suppression of the mixer noise at the outside of the center frequency in measurement. Also, LO power level of the mixer is lower than nominal value as frequency goes higher, results in more noise from the mixer. The linearity measurement shows IP_{-1dB} vary between -27.5 dBm to -25 dBm over the 4-bit phase states at 94 GHz (Fig 2.24). The comparison table 2.2 shows that the proposed Rx channel has low power consumption without degrading the performance metric relative to the prior proposed state-of-the-art Rx architectures.

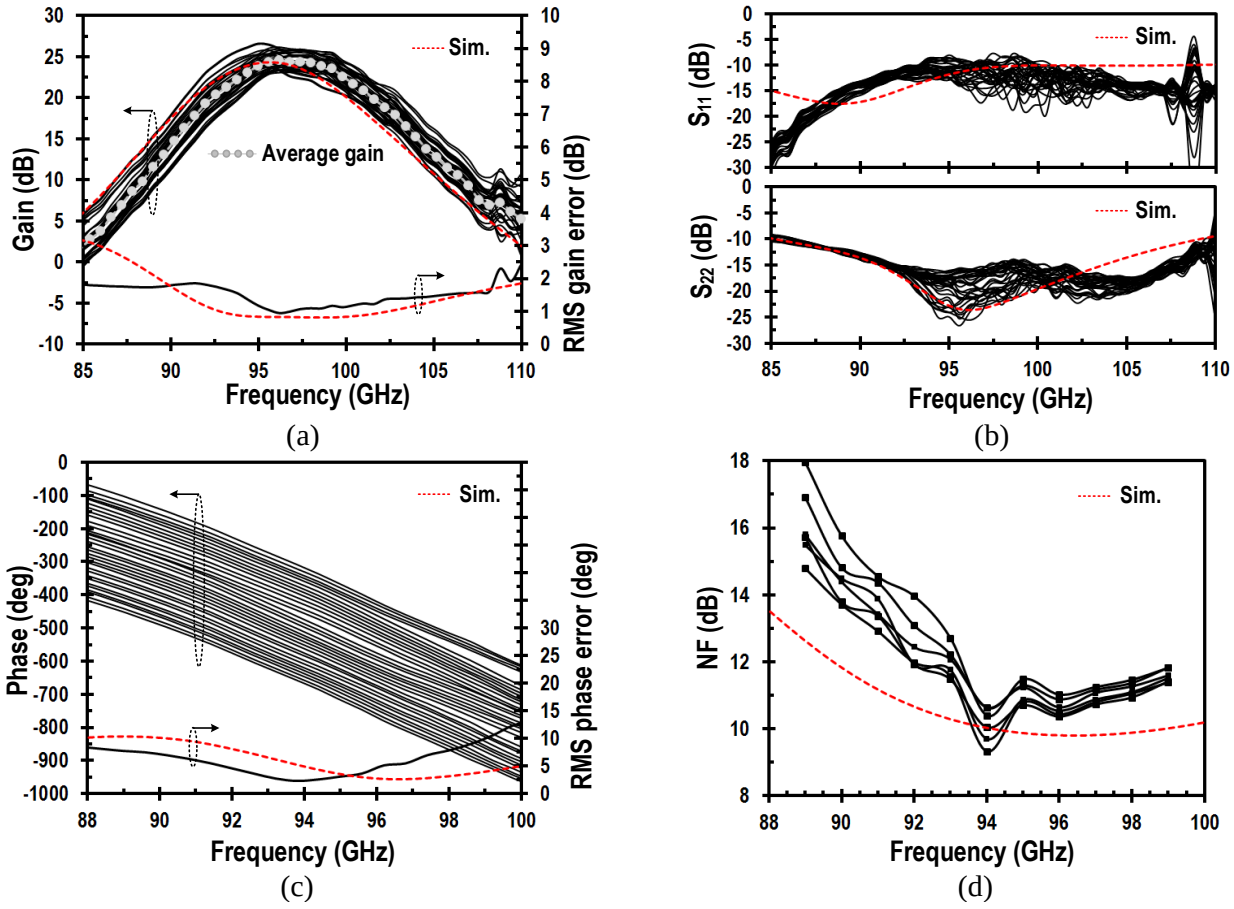


Figure 2.23: Measured: (a) gain (S_{21}), (b) input (S_{11}), output (S_{22}) reflection coefficients, (c) absolute phase response and RMS phase error for 32 phase states, and (d) NF versus frequency of the single channel receiver.

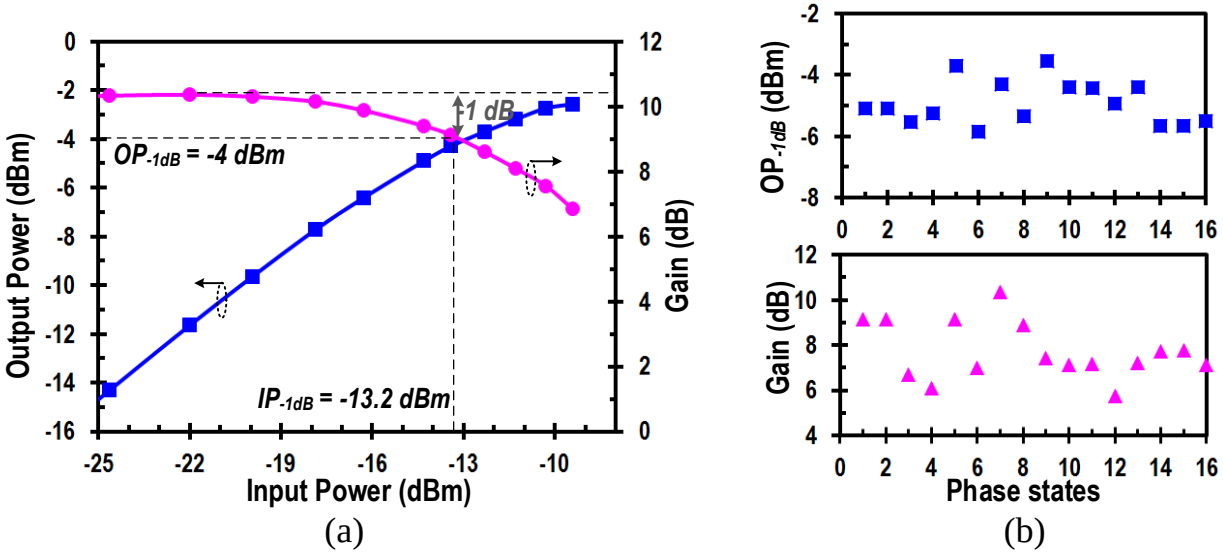


Figure 2.24: Input P_{-1dB} and gain over 16 phase states of power at 94 GHz of Rx.

Table 2.2. Performance summary and comparison of the Rx channel

Reference	This work	TMTT 2014 B.H.Ku *et al.* [26]	TMTT 2013 Golcuk *et al.* [28]	JSSC 2013 Sharamian *et al.*[27]	TMTT 2015 Natarajan *et al.*[29]	TMTT 2013 S.Y. Kim *et al.* [32]	JSSC 2012 S.Y. Kim *et al.* [33]
Frequency (GHz)	90-100	76-84	90-100	80-100	88-96	76-84	76-84
PS Type	Passive VM (Power Combining)	Active VM (Current Combining)			RTPS	Passive PS	
Process	0.13 µm SiGe BiCMOS	0.13 µm SiGe BiCMOS	0.13 µm SiGe BiCMOS	0.18 µm SiGe BiCMOS	0.13 µm SiGe BiCMOS	0.13 µm SiGe BiCMOS	0.13 µm SiGe BiCMOS
Gain (dB)	23-26	8	26-29	19	30	11-16	10-19
NF (dB)	9.3-11	16	9-11	7	8	11.4-13	11
Phase resolution	5	5	4	4	5	4	4
RMS gain error (dB)	< 1.8	< 1.5	< 1.2	1.5	< 1.8	<1	< 1.1
RMS phase error	< 5°	< 9.5°	< 5°	5°	< 10°	< 11°	< 10°
IP_{-1dB} (dBm)	-26	-10	-31	-35	-37	-26	-26
Power consumption (mW)	50	118	69	250*	80	60	33

*Includes Mixer

2.7 Summary

This chapter presents a power domain vector modulator for W-band phased arrays in $0.13\mu m$ SiGe BiCMOS process. In the proposed approach, the phase interpolation is accomplished in a passive way by the 90^0-hybrid after weighting amplifiers, which is essentially a linear process. Thus, it can achieve a high phase resolution with a fine gain control as in conventional current-mode vector modulators while being less subjected to nonlinearity issue involved in the phase synthesis. The phase distortion at high input power level is dependent on nonlinearity of weighting amplifiers only. The quadrature hybrid based phase interpolation is also robust to the output impedance variation of the weighting amplifiers. The loss of the phase shifter is determined by passive hybrid networks. The size of the hybrids gets smaller as frequency increases, achieving a low loss and compact phase shifter with a high power efficiency, promising at W-band and higher frequencies.

Chapter 3

Power-Efficient W-band (92-98 GHz) Phased-Array Transmit and Receive Elements with Quadrature-Hybrid Based Passive Phase Interpolator

3.1 Introduction

High resolution mm-Wave radar sensors with beamwidth less than several degrees need large antenna array. For the large array to be of practical use, it is paramount to maintain a high power efficiency (η) in the array element. This chapter presents a power efficient architecture of phase shifter to improve power efficiency at the W-band (92-98GHz) phased array transmit and receive (T/R) channels in 0.13μm SiGe BiCMOS process by modifying the prior proposed vector modulator as described in chapter 2. A RF domain phase shifting approach utilizing quadrature hybrid based power domain phase interpolator has been proposed by eliminating the use of SPDT switches, resulting in low passive loss with minimum number of hardware and compact in size. This leads to

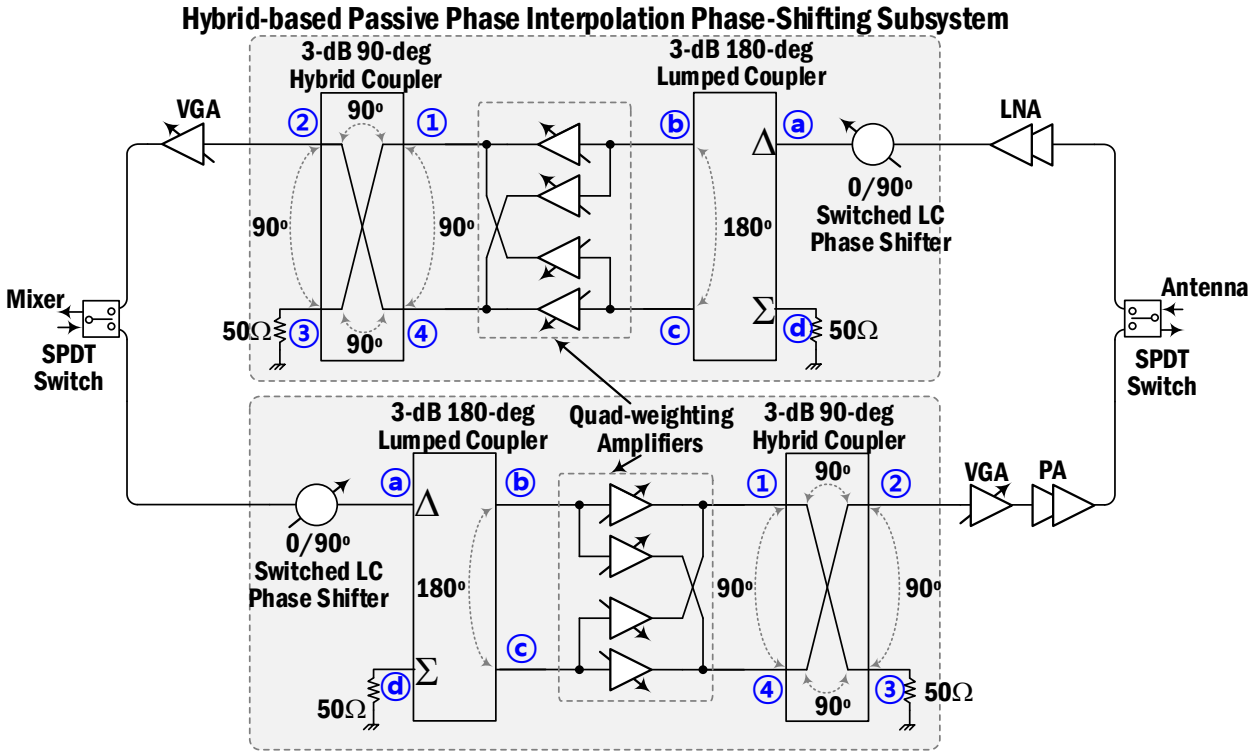


Figure 3.1: Block diagram of the TRX system utilizing 90-degree hybrid based phase interpolator.

the lowest DC power consumption in phased array T/R element among the recent state of the art works. The linearity of the phase shifter is mostly dependent on the phase interpolating VGAs, which can be much higher than gilbert cell based vector modulators in the active phase shifter, results in a low phase distortion up to high input power level in Tx. The high linearity and low loss i.e. low DC power consumption lead to the proposed phase shifter architecture to have one of the best power efficiencies among recent state-of-the-art works at W-band phased array T/R element. In addition to the transceiver performance, the LNA achieves one of the best figure of merit (FOM) considering gain/P_{diss} and NF compared to prior works at W-band in advanced silicon technologies.

3.2 Phase Shifter Architecture

The block diagram of the transceiver system utilizing 90-deg hybrid coupler based phase interpolator is shown in Fig. 3.1. The 90^0 hybrid coupler is acting as a phase interpolator by combining the weighted signal power from quad weighting amplifiers (QVGAs). In this work, the loss and the overall area of the PS are reduced by eliminating the I/Q generator, i.e. the 90^0 hybrid coupler and SPDT switches as the pre-selection stage in previous work. The I/Q generation and the selection can be done by using switchable LC network based 0^0/90^0 passive phase shifter [33]. The loss of the 90^0 PS is the same as the 90^0 hybrid coupler when considering $1/\sqrt{2}$ gain factor at the outputs of 90^0 hybrid. The QVGAs control the amount of signal power flow from 180^0 hybrid coupler to the 90^0-hybrid for fine phase processing in all the four quadrants by adding wighting factors.

Fig. 3.2 summarizes the operation of the phase shifter. The 0^0/90^0 switched LC PS generates either I or Q phase at ⓐ and the 180^0-coupler creates differential I/Q signals at ⓑ and ⓒ. Assuming the gains of the two VGAs, W_U and W_L, are equal, the weighted differential signals I and $\bar{I}$ at 0^0 state of LC PS are injected to two isolated ports of the 90^0-coupler (① and ④). They will be delayed by 90^0 and 180^0, respectively, because of $\lambda/4$ and $\lambda/2$ delays in the coupler, and then added at the output node ②, creating a 45^0 phase. The redirecting signal flow using inner VGAs as shown in Fig. 3.2(b) synthesizes a 135^0 phase. Similarly, while selecting quadrature component of the input signal generated from 90^0 phase shift of the signal by LC PS, the 2^{nd} and 4^{th} quadrant phase synthesis can be achieved (see Fig. 3.2(c) and (d)), completing 360^0 phase rotation. Thus the inherent functions of orthogonal phase splitting and power combining in the 90^0-coupler essentially create a complex weight, $jW_U + W_L$ or $-W_U - jW_L$, for a given differential input, enabling 90^0- hybrid coupler as a phase interpolator.

To account for the loss factors, 0^0/90^0 passive LC PS causes maximum ∼3.5dB loss at 90^0-delay state due to the finite NMOS switch on/off resistances [33]; the loss from the lumped 180^0-coupler is 0.5-1 dB; and a half power is split to the 50Ω terminations in the 90^0-hybrid coupler, in addition, leads to 0.5-1dB ohmic loss. These result in total 7.5-8.5 dB phase shifter loss which can be compensated by the weighting VGAs with relatively small DC penalty compared to pure passive

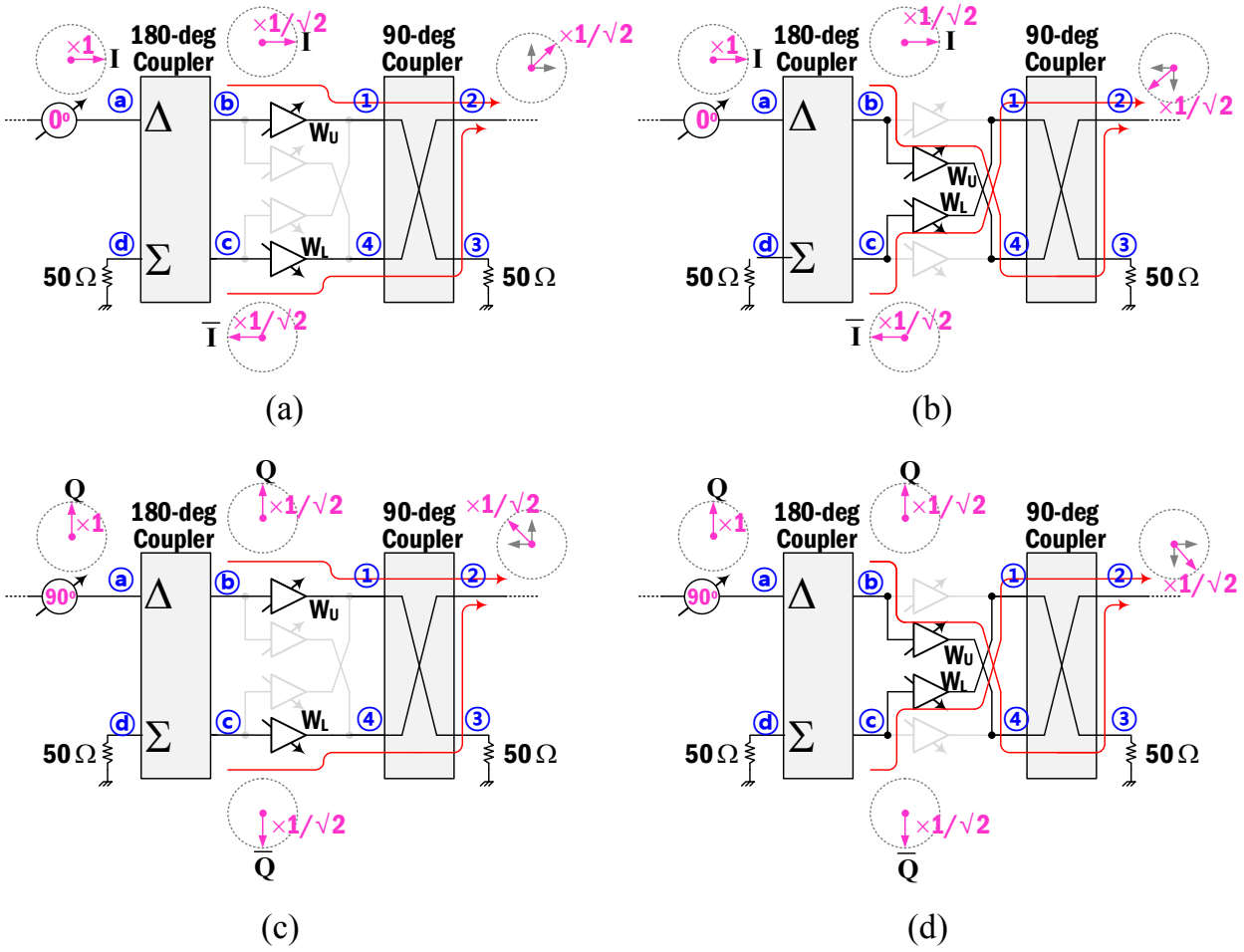


Figure 3.2: The operation of 90-deg hybrid based phase interpolator to synthesize phases in (a) 1^{st} and (b) 3^{rd} quadrants at bypass state, (c) 2^{nd} and (d) 4^{th} quadrants at delay state of 90^0 switched LC PS.

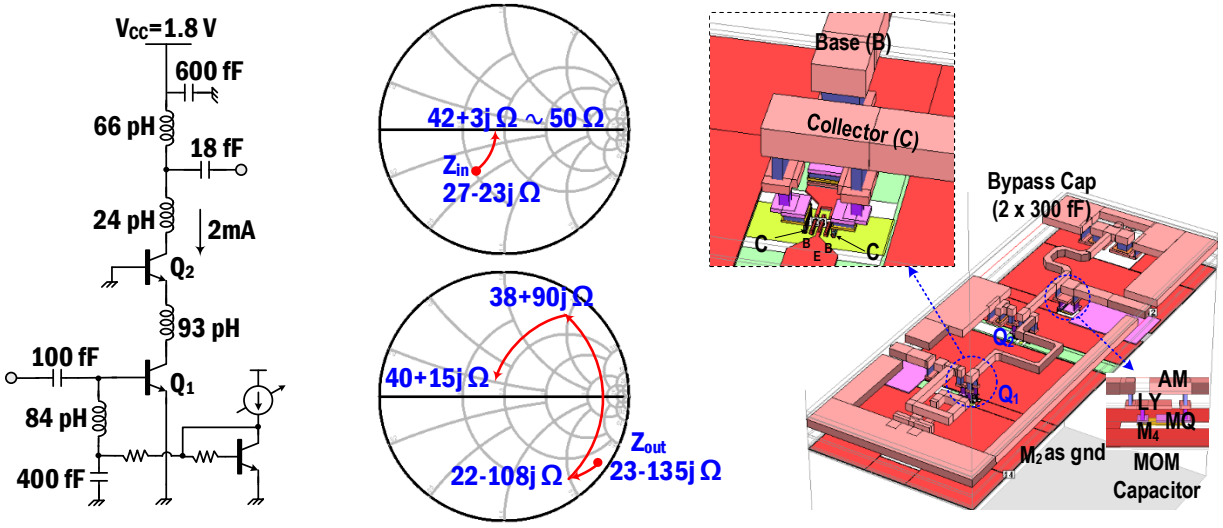
or active PSs. Compared to conventional current-mode vector summing PSs, the power-mode vector summing in the hybrid is a linear passive process and can result in low phase distortion at high input power level. Further, the power domain approach requires relatively low matched impedance (50Ω), leading to better circuit immunity to parasitic effects. The phase performance of the passive hybrids are also less vulnerable to impedance variation at its ports for wide range of frequencies at different phase states, resulting in low phase error.

3.3 Building Block Design

The design is done in IBM 0.13μm SiGe BiCMOS technology of f_T/f_{max} = 260/330 GHz. The process has seven metal stacks with the top two being thick aluminum metal layers (AM and LY layer). All the inductors for each design blocks are in AM layer with interdigitated ground plane of M2-M1 layers. The patterned ground plane improves the loss due to the substrate and enhances the Q of the inductors. In order to minimize the associated parasitic inductance in supply (VCC) and ground (GND) plane, wide metal planes are used alternatively as VCC and GND, which are stacked together by connecting with vias. In order to prevent potential low frequency oscillation, multiple low Q-capacitor banks with different range of capacitances are inserted between the VCC and GND planes.

3.3.1 Design of LNA/VGA and Measurement Results

The LNA (see Fig. 3.3) is based on cascode topology because of its high reverse isolation and high gain, suitable for mm-wave frequencies. Two stage LNA is used to have enough gain in order to suppress noise from the front-end. The peak f_T of the transistor degrades upto 240 GHz after including electromagnetic-wave (EM) model of the transistor's layout interconnection from SONNET (see Fig. 3.4(a)). The bias current density of the transistor is chosen to be 0.67 mA/μm which is close to NFmin considering low DC power consumption. At this bias current density, f_T is 200 GHz with considering transistor interconnection. The emitter length of all transistors is 3μm



(a) (b) (c)

Figure 3.3: (a) Schematic of LNA, (b) input and output matching technique, and (c) SONNET layout of the LNA showing transistor interconnection and output MOM capacitor.

and biased at 2mA current from 1.8V supply, resulting in 3.6 mW DC power consumption/stage. The noise and gain circles in smith chart (see Fig. 3.4(b)) shows a clear tradeoff between NFmin and maximum gain matching at design frequency. The input matching network (see Fig. 3.3(b)) is chosen accordingly to achieve low NF (~4.5 dB) with relatively high gain. The L-type LC network is used as input and output impedance matching. The inter-stage inductor of L_p = 93pH is used between two cascode transistors to resonate out the parasitic capacitance between the cascode transistors which improves the gain and noise figure. The bypass capacitor (C_B ≈600 fF) is added immediately after the load inductor to make a solid AC ground at 94 GHz. All the inductors and transistor interconnections are modeled using SONNET. Fig. 3.3(c) shows full SONNET layout of the LNA. High Q metal-oxide-metal (MOM) capacitor, made by top four metal layers, has been used for output matching. The VGA, used after phase interpolator, has the same topology as LNA. The variable gain is achieved by controlling the bias current of the amplifier and the gain variation is 5-10 dB with 1 dB gain step in simulation. The gain control is sufficient to reduce the gain error of the PS.

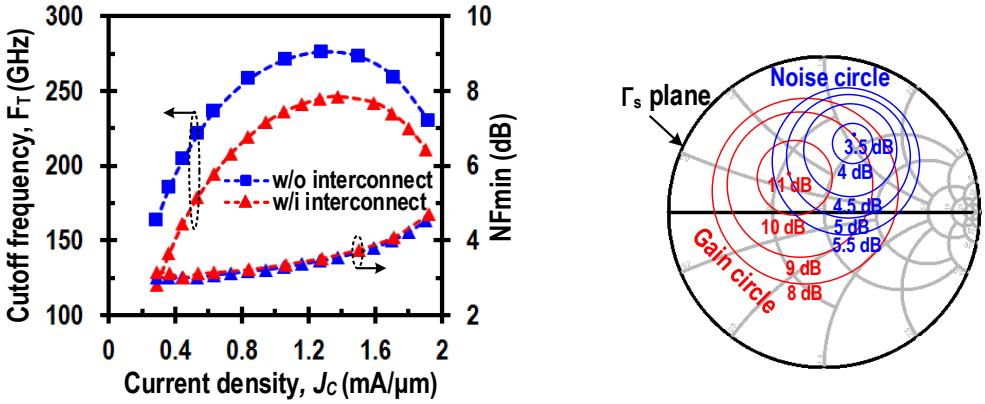


Figure 3.4: (a) Cutoff frequency and NFmin verses current density with and without EM model of interconnects, and (b) noise and gain circles in Γ_s plane in Smith chart.

Measurement Results of LNA

The measurement results of LNA are shown in Fig. 3.5. The LNA test chip has core size 130×430 μm^2 (see Fig 3.5(c)). The peak gain is 9.7 dB, shifted to 97 GHz and 3-dB BW is 90-107 GHz. The gain is 9 dB at 94 GHz. S_{11} and S_{22} are < -5 dB at 92-105 GHz (S_{22} is narrow band because of high-Q MOM capacitor at the output). The measured NF remains 4.86-5.2 dB at 92-100 GHz where 4.9 dB at 93 GHz which is lower than simulation. The NF can be lower as current density increases because gain increases at peak gain frequency (97 GHz). The measured input 1-dB compression point (IP_{-1dB}) is -15 dBm.

Table 3.1 shows the comparison of LNA with previous W-band LNAs in advanced silicon technologies [58]-[63]. The figure of merit (FOM) of the amplifier can be defined as $Gain[dB]/(F-1)\cdot P_{diss}[mW]$ which is plotted in Fig 3.6 [55]-[57]. The comparison shows the LNA achieves one of the best FOM compared to other LNAs even with lower cutoff frequency (f_T) of the transistors.

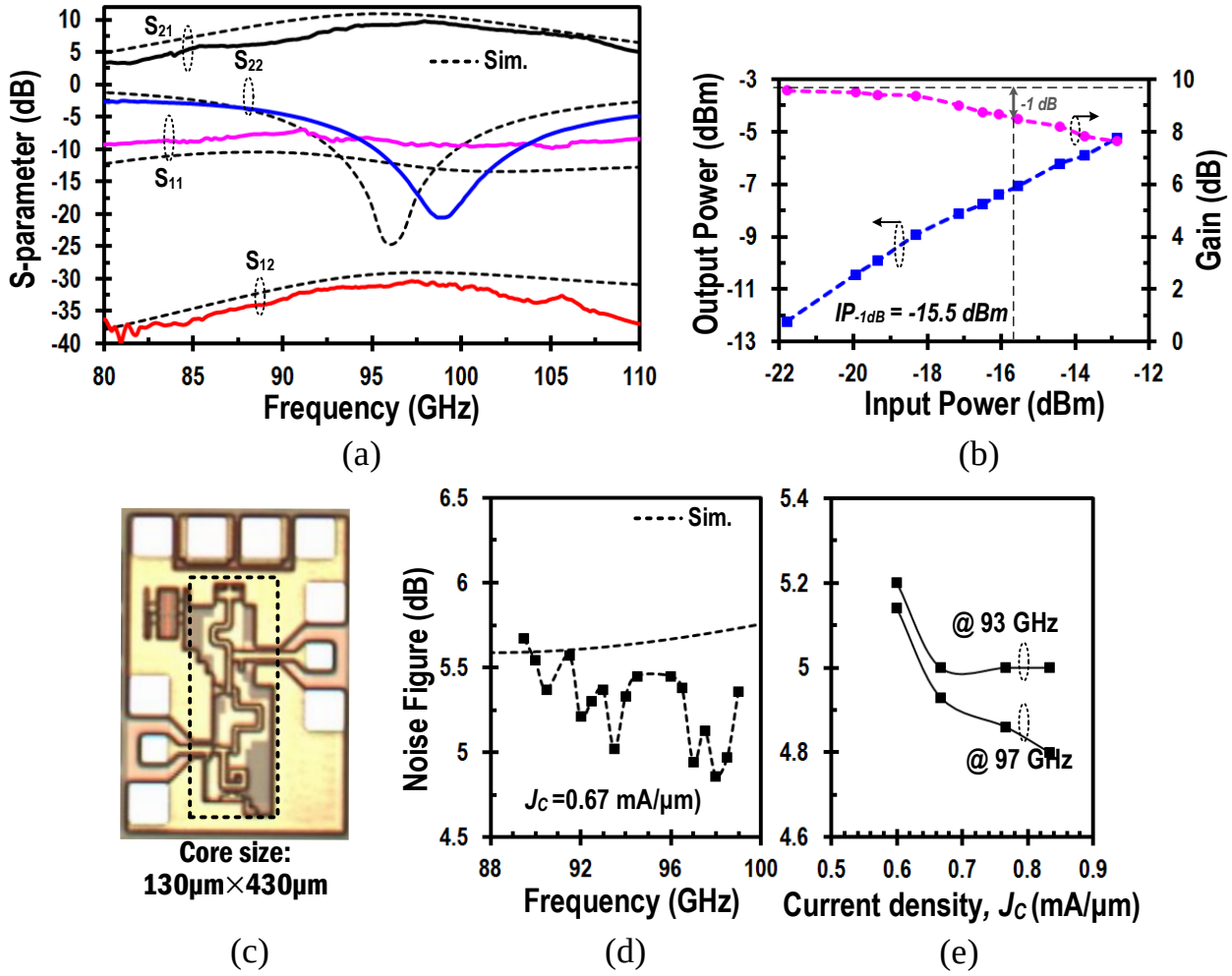


Figure 3.5: Measurement results of 1-stage LNA : (a) S-parameters: Gain (S_{21}), input and output reflection coefficients (S_{11}, S_{22}) and isolation (S_{12}) over frequency, (b) output power and gain verses input power at 94 GHz, (c) chip photo (chip size: 130×430 μm^2), and noise figure measurements: (d) noise figure verses frequency and (e) noise figure vs current density at 93 GHz and 97 GHz of LNA.

Table 3.1. Comparison of LNAs at W-band in advanced silicon technologies

Reference	Frequency (GHz)	Peak Gain (dB)	NF (dB)	IP_{-1dB} (dBm)	No. of stages	Pdiss (mW)	Process
This work	97	9.7/stage	4.86	-15	1	3.6/stage	0.13 µm SiGe BiCMOS (F_T=260 GHz)
X. Bi, MWCL,2013 [58]	94	45 (11/stage)	7	-43.8	4	19.2 (4.8/stage)	0.13 µm SiGe BiCMOS (F_T=240 GHz)
S.Y. Kim, JSSC, 2012 [33]	80	12 (6/stage)	8.8	-21	2	11 (5.5/stage)	0.13 µm SiGe BiCMOS (F_T=200 GHz)
B. H. Ku, TMTT, 2014 [26]	80	13.8 (6.9/stage)	7.7	-10.5	2	50 (25/stage)	0.13 µm SiGe BiCMOS (F_T=200 GHz)
F. Golcuk, TMTT, 2013 [28]	94	18.5 (9/stage)	8.7	-21	2	20 (10/stage)	0.13 µm SiGe BiCMOS (F_T=200 GHz)
P. Song, TMTT 2014 [61]	94	25 (5/stage)	4	-23	5	15.6 (3.2/stage)	90 nm SiGe BiCMOS (F_T=300 GHz)
Y. Yang, CSCIS, 2013 [60]	90	19 (4.7/stage)	5.1	-20	4	43 (10.7/stage)	90 nm SiGe BiCMOS (F_T=300 GHz)
A. C. Ulusoy, IMS,2013 [59]	110	20 (10/stage)	4	-24	2	17 (8.5/stage)	0.13 µm SiGe BiCMOS (F_T=300 GHz)
B. Cetinoneri, TMTT, 2012 [62]	94	11 (3.7/stage)	6	-8	3	52 (26/stage)	45 nm CMOS SOI (F_T=340 GHz)
D. Pepe, MWCL, 2012 [63]	91	32 (5.3/stage)	5.3	-41	6	36 (6/stage)	28 nm bulkCMOS (F_T=300 GHz)

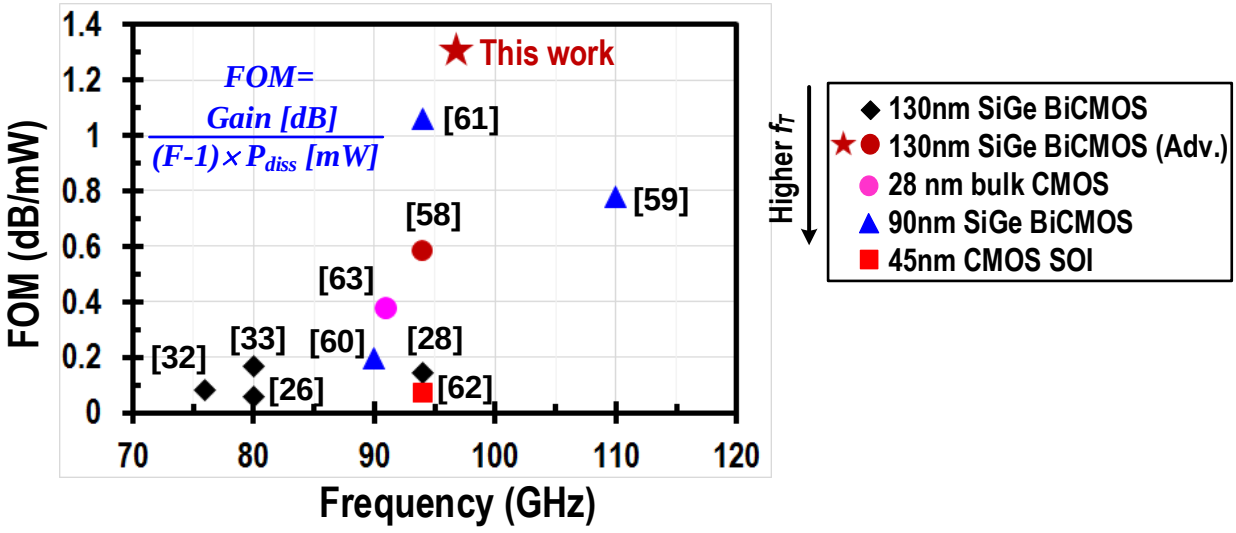


Figure 3.6: Comparison of LNA FOM (= $Gain[dB]/(F-1)\cdot P_{diss}[mW]$) with state-of-the-art LNAs in advanced silicon technologies ($f_T \geq 200$ GHz).

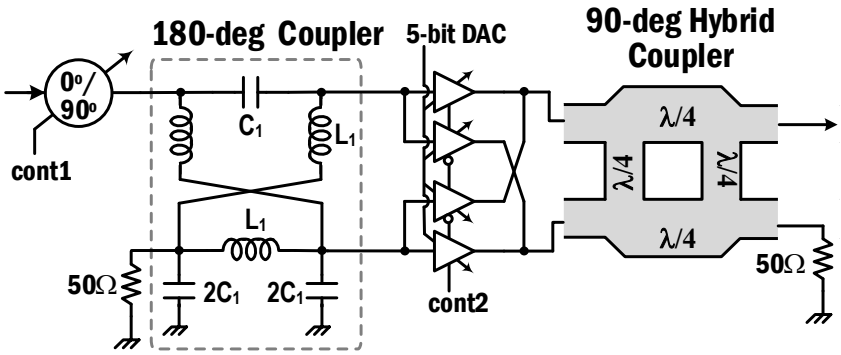


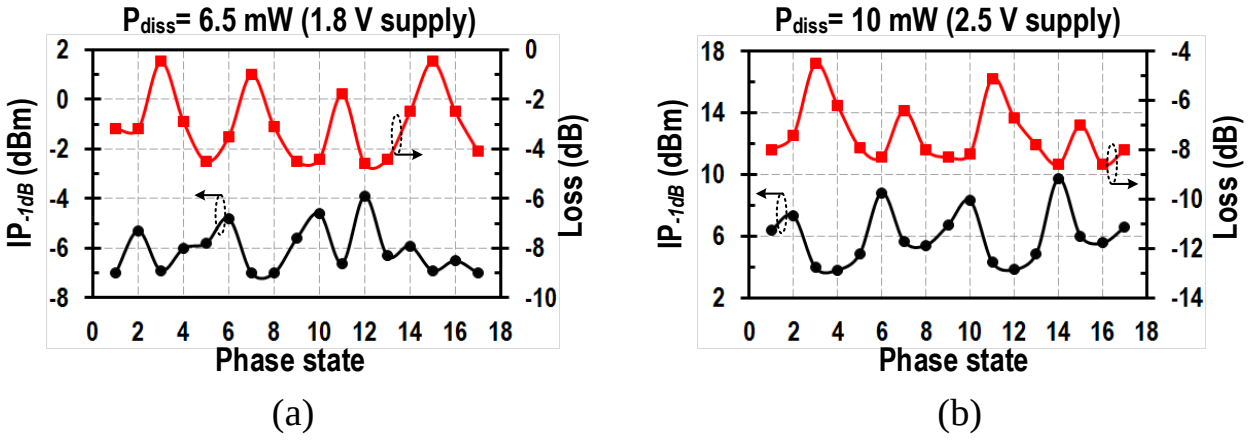
Figure 3.7: Architecture of the Phase shifter.

3.4 Design of the Phase Shifter

The phase shifter (see Fig. 3.7) is comprised of 90-deg switched LC type phase shifter, 180-deg lumped hybrid coupler, QVGAs and 90-deg hybrid coupler. The design of 90-deg and 180-deg hybrid couplers are the same as described in chapter 2. The 90^0 phase shifting and the selection of QVGAs are done by two separate control voltages, and the gain of QVGAs is controlled by 3-bit DAC. The architectures of Rx and Tx phase shifter are same, except Tx PS operates at higher supply voltage than Rx (Rx: 1.8 V and Tx: 2.5 V) to have better linearity in Tx, resulting in 6.5 mW and 10 mW P_{diss} respectively for Rx and Tx PS. The linearity is mostly constraint by QVGAs and the switched LC PS has negligible impact on this. The simulated loss of Rx PS varies 0-4.5 dB with maximum -3.9 dBm of input 1-dB compression point up to lowest -7 dBm (see Fig. 3.8(a)). For Tx PS, loss is higher (-4.5 to -8.6 dB) and IP_{-1dB} is 4-10 dBm (see Fig. 3.8(b)). The loss is compensated by the output amplifier.

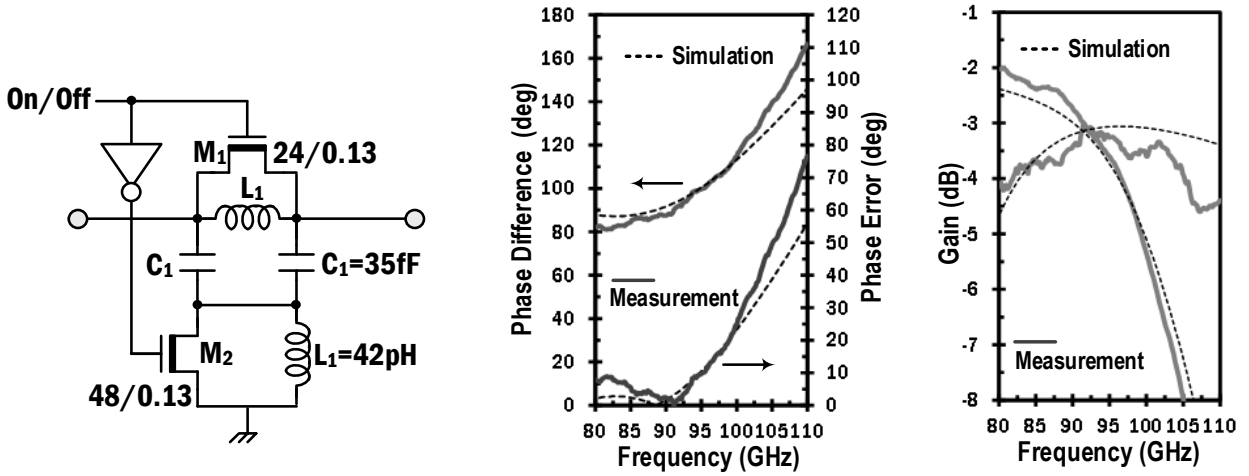
3.4.1 90^0 Switchable LC Phase Shifter and Measurements

The 90^0 NMOS switch based LC phase shifter is based on switched 50Ω low-pass networks [33] (see Fig 3.9). In the bypass-state, M1 is ON and M2 is OFF. The OFF state parasitic capacitance is resonated out by inductor L_r=42 pH. At 90^0 delay state, M1 is OFF while M2 is ON. The size of the transistors is optimized to have a low loss (M1/M2=24μm/48μm). The measured phase



(a) (b)

Figure 3.8: Simulated Rx and Tx PS loss and input 1-dB compression point (IP_{-1dB}).



(a) (b)

Figure 3.9: (a) Schematic and (b) S-parameter measurement results of 90^0 switchable LC phase shifter.

response is well-matched with simulation. The simulated loss of the phase shifter is maximum 4 dB at delay state and phase error is $< 10^0$ over the 75-100 GHz. Although a full EM simulation including post layout extraction of the transistors were done for the whole phase shifter during the design process, still an extra 1 dB loss was observed at bypass in measurement (see Fig 3.9(b)). This discrepancy appears may be because of the signal leakage through the substrate via OFF state parasitic capacitance of the transistor, which could not be captured in the simulation. The simulated IP_{-1dB} is 10 dBm.

3.4.2 Quad Weighting VGAs and Measurement Results

Fig 3.10 shows the schematic of quad weighting amplifiers (QVGAs) compatible with layout floor plan. Each amplifier has the same topology as LNA. The variable gain operation is achieved by steering DC current (I_w) controlled by the DAC and the VGA can be turned ON and OFF by cutting off the bias current (I_{sw}) using a switch network. The maximum current of each amplifier is 2mA from 1.8V supply for Rx, and 2.5V for Tx, resulting in a DC power consumption of 3.6 mW and 5 mW for Rx and Tx, respectively (two amplifiers are ON at a time). Fig 3.11 shows the input and output matching networks in details. The OFF state parasitics of the transistor are in parallel with the input impedance (Z_{in}), resulting in an impedance of $Z_{inP} = 12 - 17j$ in smith chart. In order to match input close to 50Ω, an inductor (L_{IM} = 50pH) is well enough to keep input reflection coefficients < -10 dB. Asymmetric layout in the input matching does not impact significantly on the performance of the PS as long as reflection coefficients are below -10 dB. In designing output matching network, practically 15$\pm$5fF (C_p) and 20$\pm$5pH ($L_{p,1-2}$) of parasitics are typical due to the layout interconnection. In addition with OFF state parasitics of the transistor, this results in a low capacitive impedance locus, $Z_{out} \Rightarrow$ ⓧ $\Rightarrow$ ⓨ $\Rightarrow$ ⓩ in the Smith chart, in the vicinity of the VGAs output junction node (see Fig 3.11(b)). This low-Z parasitic network absorbs any transistor impedance disturbances caused by the VGA gain control, resulting in fairly constant 50Ω matching resistance over the VGA gain variations.

The chip photo and measurement results of QVGA for Rx channel are shown in Fig 3.12. The

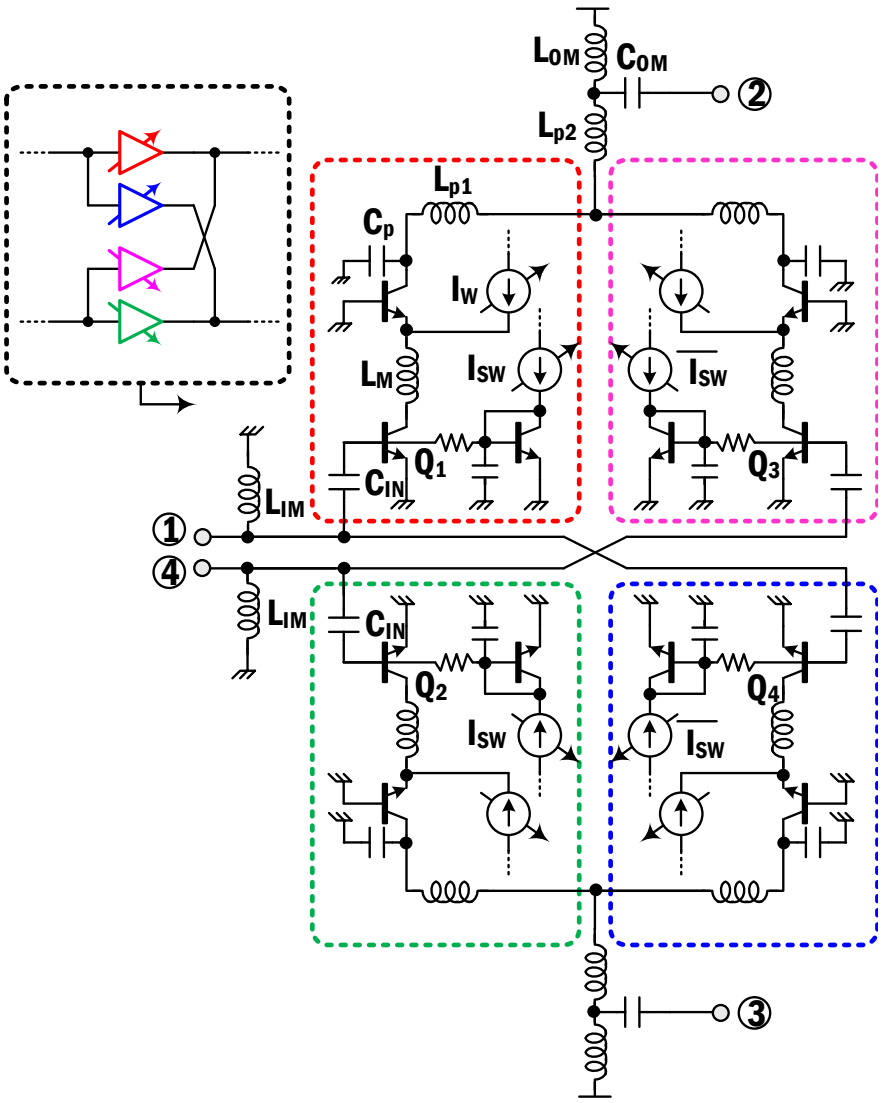


Figure 3.10: Schematic of Quad-weighting VGAs.

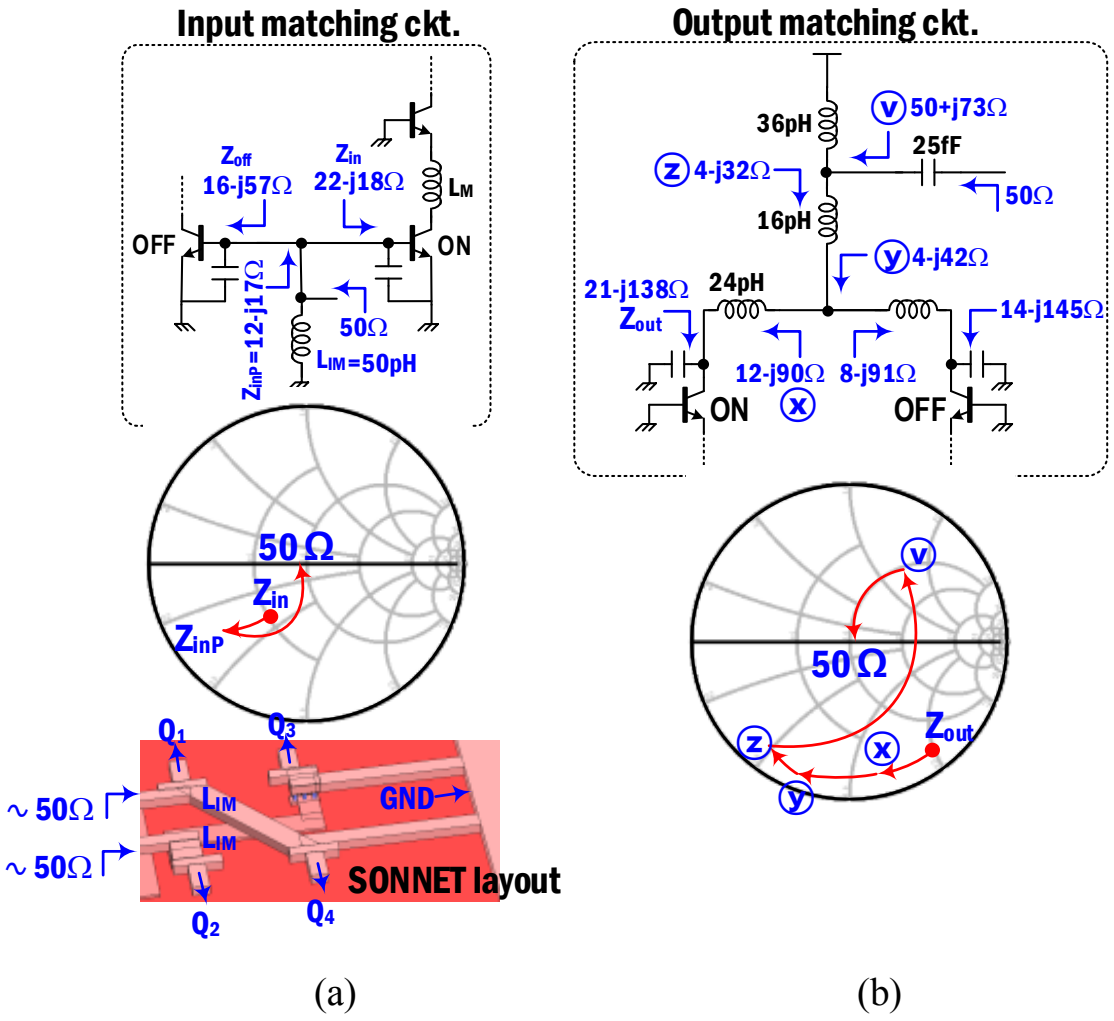
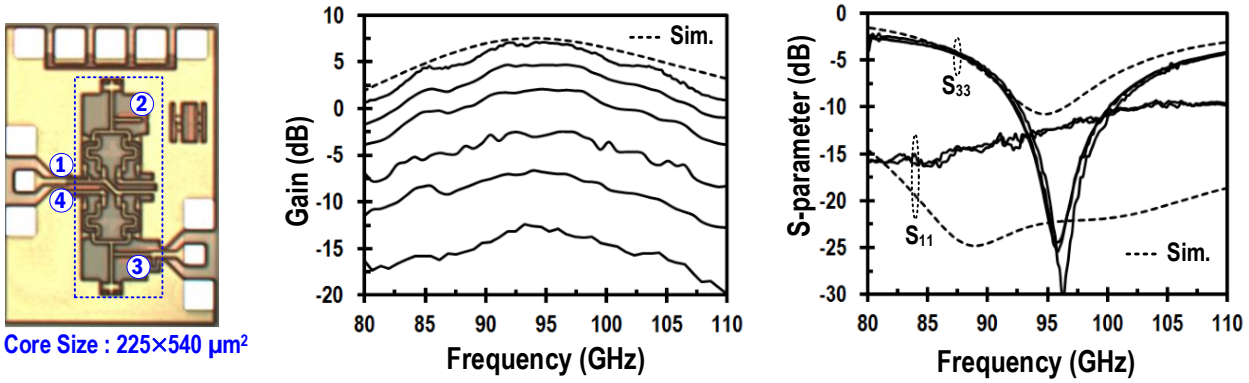


Figure 3.11: (a) Input matching network with SONNET layout of interconnection and (b) Output matching network in details with smith chart for Quad weighting amplifiers.



(a) (b) (c)

Figure 3.12: (a) Chip photo (core size: 225×540 μm^2) and Measured (b) gain response (c) input and output reflection coefficients of Rx Quad-weighting VGA.

measured gain variation ranges -15∼7 dB, where the peak gain response is well-matched with simulation (Fig 3.12(b)). S_{11} and S_{22} are < -10 dB at 92-100 GHz for all over the gain states. S_{22} remains almost same over all the gain states of VGA, maintaining low impedance variation at the input of 90-deg hybrid.

3.4.3 SPDT Switches at Back-end and Front-end

SPDT switches at front-end and back-end are shown in Fig 3.13 which is based on $\lambda/4$, 50Ω transmission lines. The NFET sizes are optimized to have low insertion loss and high isolation between Tx and Rx side ($86\mu m/0.12\mu m$ with number of fingers 24). A small inductor of 20 pH is enough to resonate out the OFF state parasitic capacitance of the MOSFET. Gaurd rings were used around the NFET in order to shield it from noise. A whole EM simulation is done with NFET interconnection up to M2 layer (see Fig 3.13(b)). The simulation result shows the insertion loss is 2 dB with isolation between Tx and Rx is better than 20 dB. Input and output reflection coefficients are -10 dB at 82-100 GHz and the leakage from the OFF state Tx/Rx upto the output is < -18 dB. The digital control signal has supply of 1.2V.

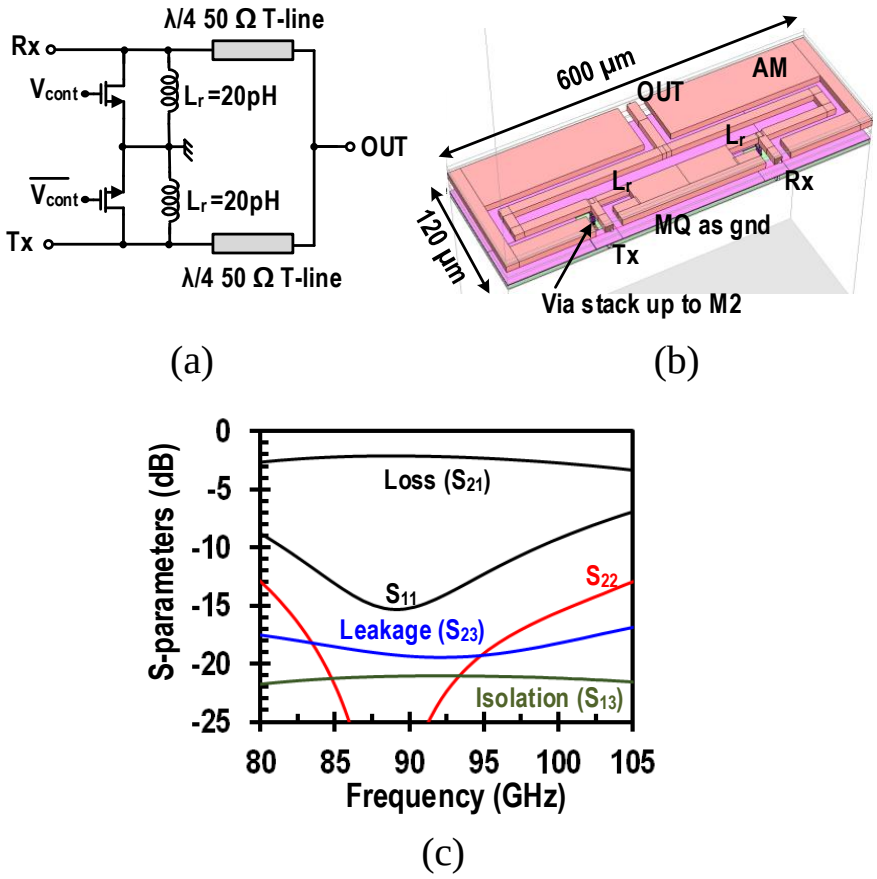
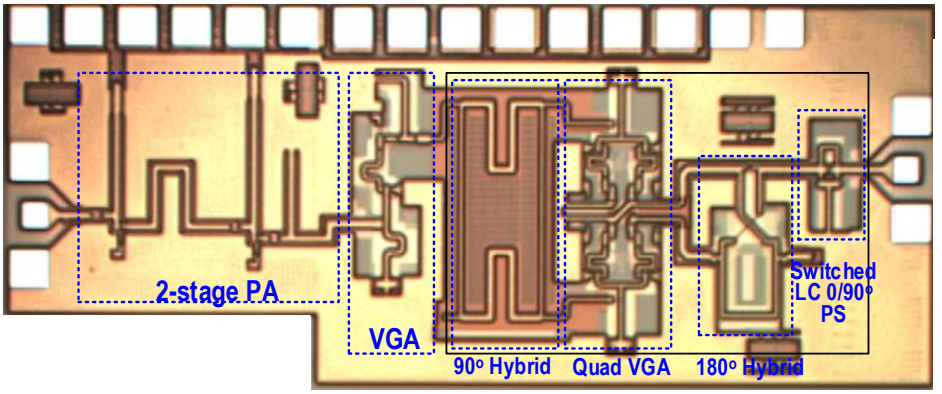
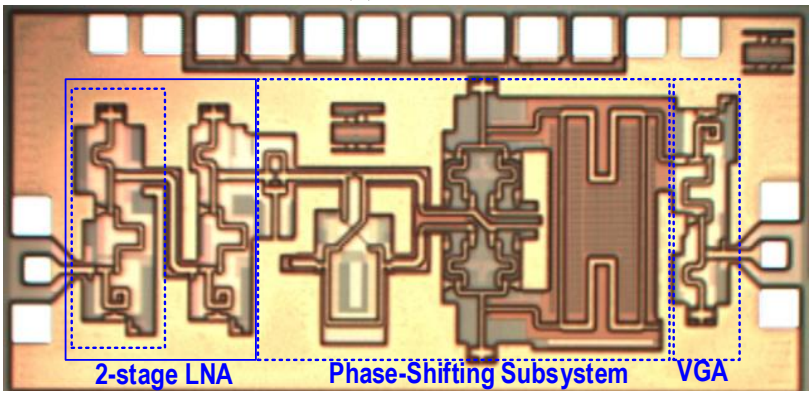


Figure 3.13: (a) Schematic, (b) SONNET layout, and (c) S-parameter simulation results of the SPDT switch.



(a)



(b)

Figure 3.14: Chip photos: (a) transmitter (chip size: 1.4×0.55 mm^2) and (b) receiver (chip size: 1.2×0.55 mm^2) excluding I/O pads.

3.5 Measurement Results

Fig 3.14 shows chip photograph of T/R element. The core area of Tx and Rx are 1.4×0.55 mm^2 and 1.2×0.55 mm^2, respectively. The size is small enough to be integrated into the $\lambda/2 - \lambda/2$ (1.6×1.6 mm^2) array lattice with a room for SPDT switches and other array interfaces at 94 GHz. The S-parameters of the T/R channels are measured after standard SOLT calibration with W-band frequency extension modules. About 1 dB of the input and output GSG pad losses are de-embedded from the measurement data.

3.5.1 Transmitter Phase Shifter

Fig 3.15 shows the measurement results and chip photo of stand-alone transmitter phase shifter with output VGA. The core size of the phase shifter is 0.95×0.55 mm^2. The peak gain is 1-5 at 97 GHz with RMS gain error $<$ 1.8 dB for 4-bit operation at a fixed gain state of the output VGA. The RMS phase error is $< 6^0$ at 88-98 GHz for 16 phase states. S_{11} and S_{22} remain less than -5 dB at 90-100 GHz. The fluctuation in S_{11} is because of the input impedance variation of 90^0 LC PS at bypass and delay state. The output matching is narrow band due to the high Q MOM capacitor at output of the VGA. A 5-bit phase resolution can be got with some phase gapes (total number phase states are 30), but still maintaining $< 7^0$ RMS phase error at 90-100 GHz (see Fig 3.16). The phase gap occurs may be because of the phase error in 90-degree switched LC phase shifter. The overshoot in phase response at 92 GHz is because of the calibration. We have not observed this kind of overshoot during measurement of whole Tx. The gain variation for 5-bit is the same as 4-bit gain response. A careful measurement is done for linearity testing which is described in chapter 2. The linearity measurement is done by using Agilent W-band power sensor and dual channel power meter. All the losses at input and output including waveguide sections, attenuator, and probe loss have been calibrated. Fig 3.17 shows the linearity measurement results of stand-alone transmitter phase shifter with output VGA for 16 phase states. The saturated power, P_{sat} varies from -1.5 to $+1.5$ dBm with peak power gain 0-5 dB at 96 GHz which is close to simulation. OP_{-1dB} varies $-6 \sim -4$ dBm. The DC power consumption of the Tx PS with output VGA is maximum 17 mW. Table 3.2 compares the phase shifter with state-of-the-art PS at W-band for Tx application, including both RF and base-band phase shifting approach which are promising nowadays for low power arrays around 60 GHz applications. The proposed PS delivers high power with low DC power consumption and high linearity compared to prior works.

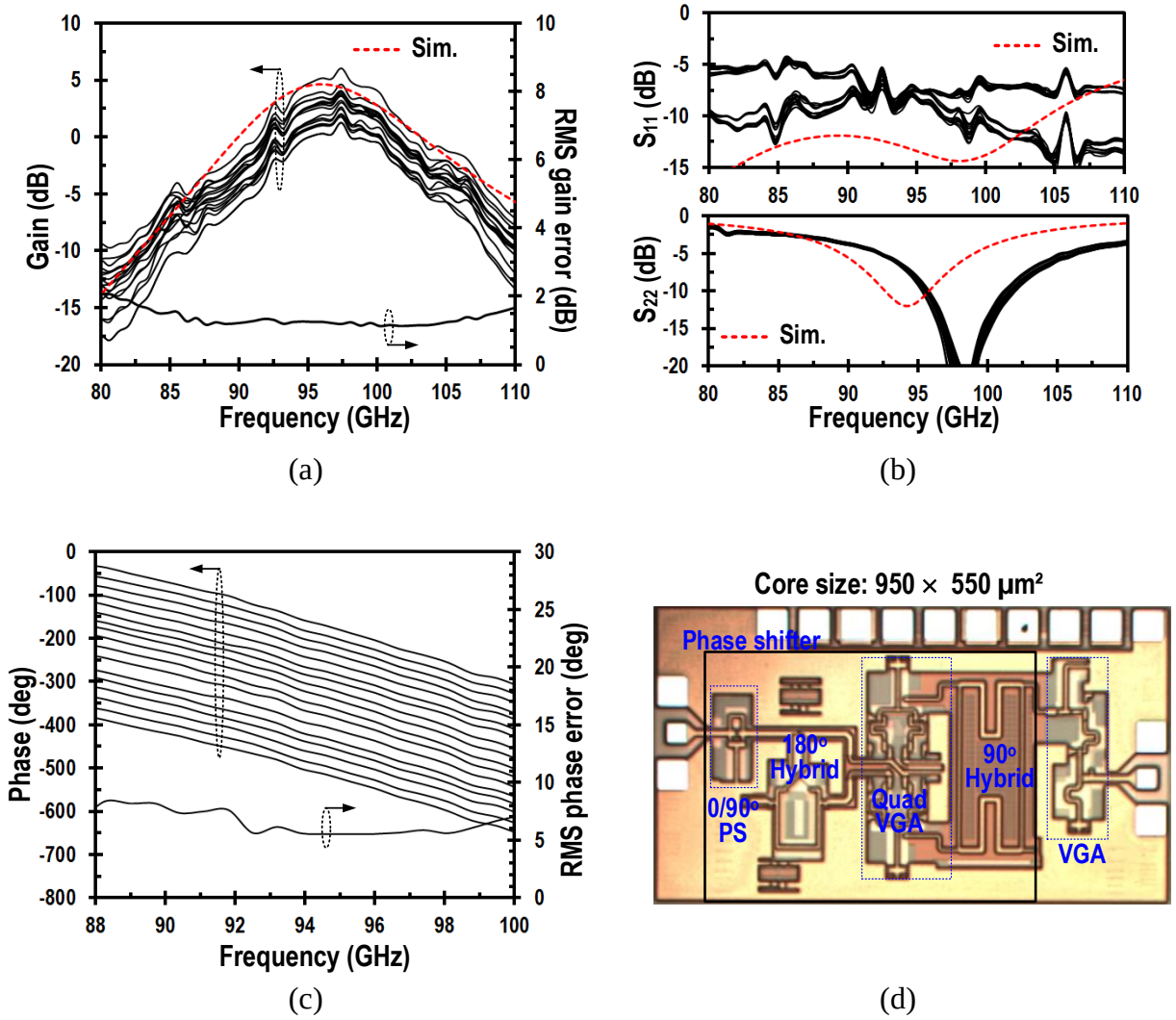


Figure 3.15: Measured: (a) gain, (b) input and output matching, (c) phase response for 16 phase states of the transmitter phase shifter with output VGA, (d) chip photo of the phase shifter (chip size: $0.95 \times 0.55\ mm^2$) .

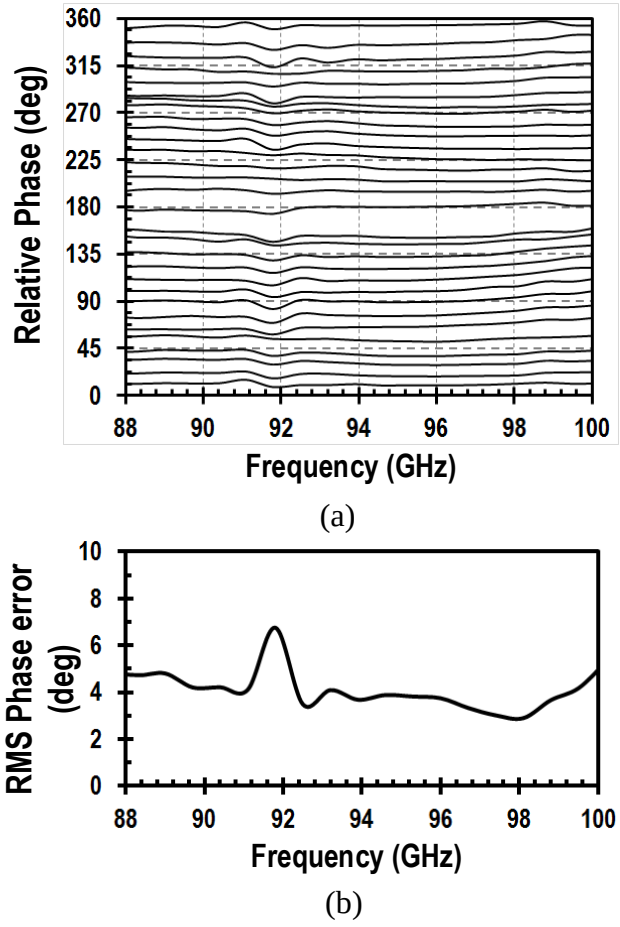


Figure 3.16: Measured: (a) 5-bit phase response and (b) RMS phase error for 5-bit phase resolution of the phase shifter.

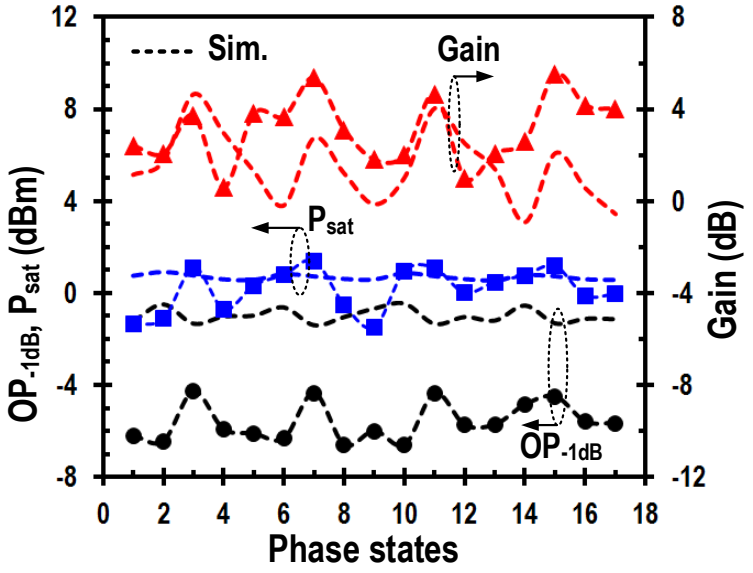


Figure 3.17: Measured power gain, P_{sat} and OP_{-1dB} at 16 phase states of the Tx phase shifter with output VGA.

Table 3.2. Tx phase shifter Performance Summary and Comparison

Ref.	Freq. (GHz)	PS Topology	Gain (dB)	P_{sat} / OP_{-1dB} (dBm)	Pdiss (mW)	Phase resolution	RMS gain/ phase error	Process
This Work	96	RF Passive VM (Power Combining)	1-5.5	1.4/−4	17	5	< 1.4 dB/ < 5.5°	0.13µm SiGe BiCMOS
Fatih, TMTT 2013 [28]	94	RF Active VM (Current Combining)	−5	−5/-	~40++	4	< 1.2 dB/5°	0.13µm SiGe BiCMOS
B. H. Ku, TMTT, 2014 [26]	80	RF Active VM (Current Combining)	−5	-/−2*	30*	5	< 1.5 dB/ < 11°	0.13µm SiGe BiCMOS
Natarajan, TMTT 2015 [29]	94	RTPS	−4*	-	18*	5	< 2.5 dB/ < 12°	0.13µm SiGe BiCMOS
S. Kundu, JSSC, 2015 [22]	57	BB Cartesian PS (Current Combining)	0.2	-/−7.8	25	5	< 2 dB/ < 5°	45nm SOI CMOS

++Calculated from the whole Tx data *Simulation

3.5.2 Transmitter

The transmitter phase shifter has been integrated with a class AB power amplifier (PA). The PA is comprised of two stage common-emitter amplifier where the first stage is a driver followed by the output stage. The small signal power gain of PA is 6.8 dB at 94 GHz with 8.4 mW power consumption. PA provides maximum 7.4 dBm output power (P_{sat}) and OP_{-1dB} is 3.9 dBm. The maximum power added efficiency (PAE) is 18.2% at P_{sat} condition. The Tx S-parameter measurement result (see Fig 3.18(a)-(c)) shows the peak gain is 7-11 dB at 96 GHz with the average gain of 9 dB, 3-dB BW is 92-100 GHz. At 94 GHz, the peak gain is 10 dB. The RMS gain error $<$1.28 dB at 85-105 GHz. The 4-bit phase response shows the RMS phase error is 1.5^0 at 94 GHz and is less than 6^0 at 88-98 GHz. 5-bit phase resolution can be achieved which spans 0^0 to 330^0 phase (phase gap occurs like the phase shifter response) and the RMS phase error remains below 6^0 at 90-100 GHz as shown in Fig 3.19. The measured S_{11} and S_{22} are below -8 dB over 90-110 GHz. The variation of S_{11} reflects the impedance variation at the input of the switched LC PS at the bypass and delay states. Fig 3.18(d) shows 7.3 dBm P_{sat} held in the Tx channel while OP_{-1dB} decreases to 2.6 dBm (IP_{-1dB}=$-$8.4 dBm) because of the nonlinearity of the proceeding VGA and phasing circuits (Note, the power gain is higher than S-parameter gain in measurement). The overall Tx channels collector efficiency (η_C) and PAE are 11% and 8%, respectively. P_{sat} ranges from 6.2-7.3 dBm and OP_{-1dB} ranges 1.57-2.6 dBm over 16 phase states at 96 GHz (see Fig 3.20). The maximum PAE of the Tx varies 6.32-8.63% at 96 GHz. Fig 3.21 shows the results for 94 GHz. OP_{-1dB} ranges $-$0.5 to 0.62 dBm, P_{sat} varies by 5.2 to 6.5 dBm and PAE ranges from 3.44% to 6.85%. Fig 3.22 presents OP_{-1dB} and P_{sat} over the frequency band, which shows $>$ 4 dBm output power is held for all over the frequency band (90-98 GHz). While the phase errors get worse after gain becomes compressed because of AM-PM phase distortion in the Tx channel, the measured RMS phase error is $< 8^0$, guaranteeing 4-bit accuracy up to well above the gain compression point (upto P_{in}=$-$2 dBm) in Fig 3.23 at both 94 GHz and 96 GHz. The DC power consumption of the Tx channel is 26 mW at the nominal bias condition of PA.

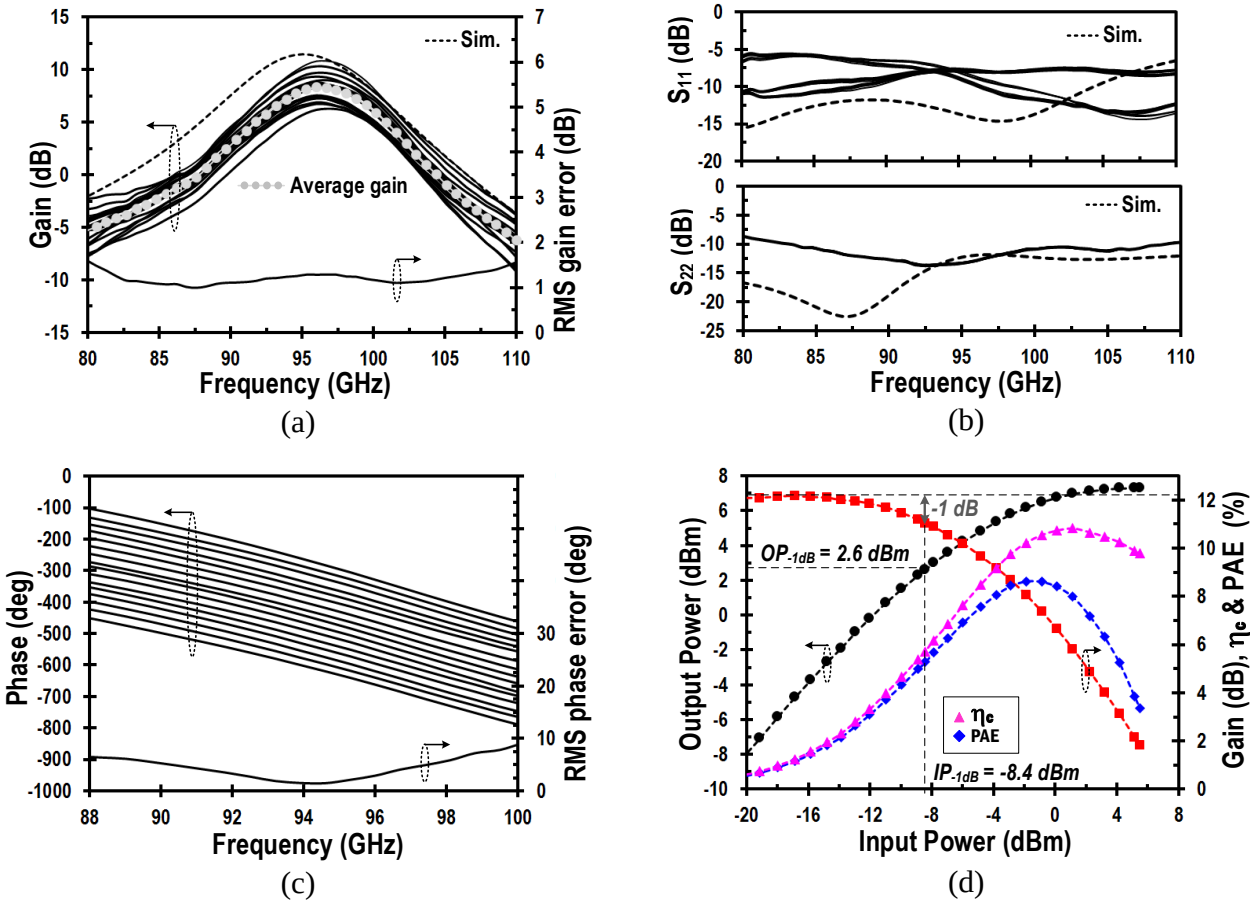


Figure 3.18: Measured: (a) gain (S_{21}), (b) input (S_{11}), output (S_{22}) reflection coefficients, (c) absolute phase response and RMS phase error versus frequency for 16 phase states, and (d) Output power, gain, collector efficiency and PAE versus input power at 96 GHz at highest gain state of the transmitter.

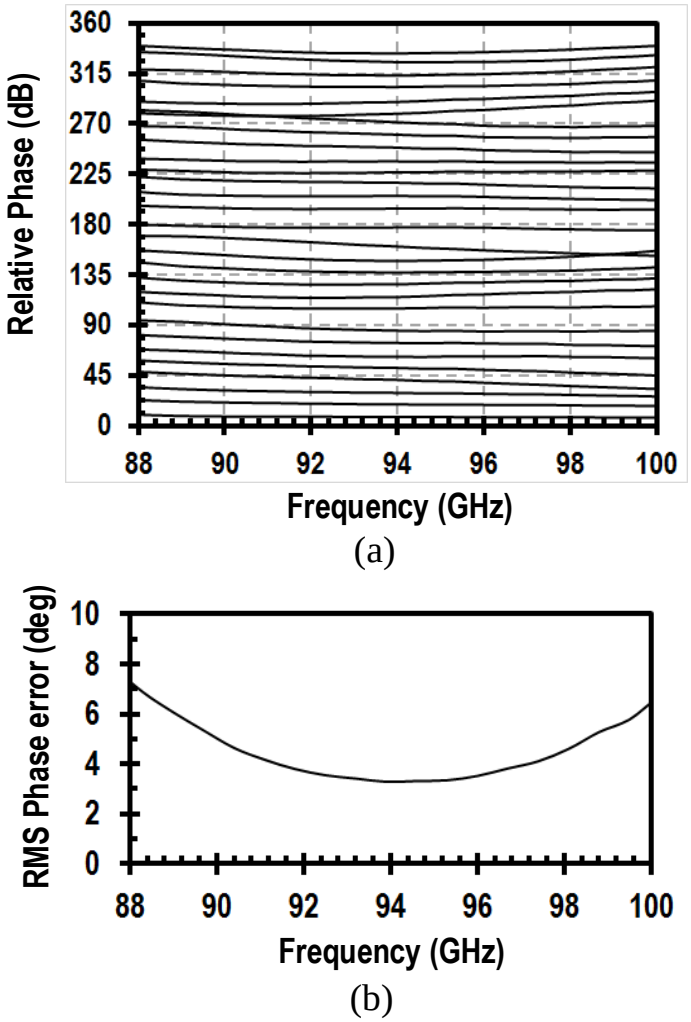


Figure 3.19: Measured (a) 5-bit phase response and (b) RMS phase error for 5-bit phase resolution of the transmitter.

3.5.3 Receiver

The Rx channel measurement results show (see Fig 3.24) the peak gain is 17-23 dB over 16 phase states with the average gain of 21 dB and 3-dB BW of 92-100 GHz. About 5 dB of gain drop is observed in measurement likely because of some extra losses in cascading the Rx channel building blocks. The RMS gain error is $<$ 1.4 dB at 90-100 GHz. The 4-bit phase response shows the RMS phase error is 2.4^0 at 94 GHz and remains below 6^0 at 91-98 GHz. The measured IP_{-1dB} is

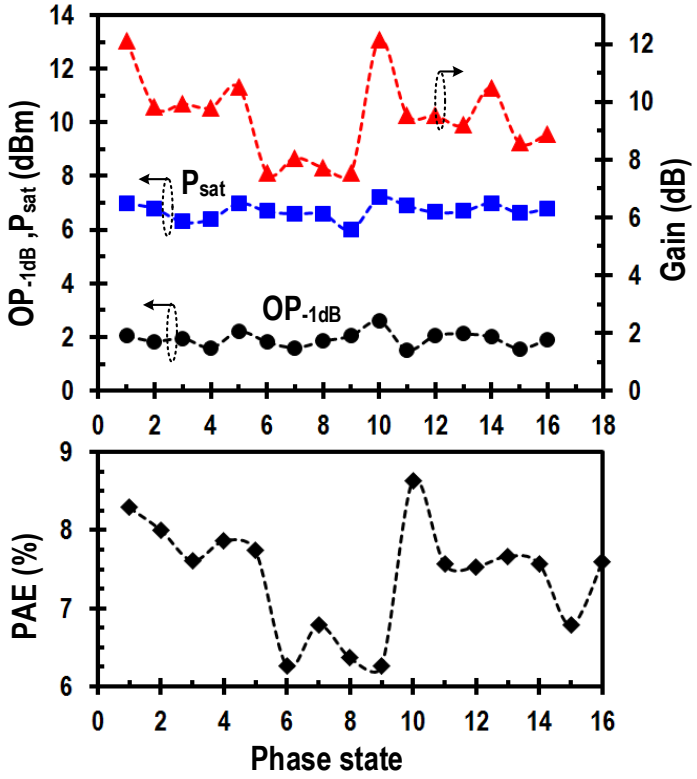


Figure 3.20: Measured power gain, OP_{-1dB}, P_{sat} and PAE over 16 phase states at 96 GHz of Tx.

-31 dBm. The NF is measured by using a W-band noise source and the output signal is amplified by a W-band amplifier and down-converted to IF frequency using a W-band mixer as described in chapter 2 which is finally measured by noise figure meter instead of spectrum analyzer. The measured NF ranges 5.7-to-6.7 dB at 92-98 GHz and NF variation over the 4-bit phase states is $\sim$0.5dB (see Fig 3.25). The gain drop did not affect the NF because the two-stage LNA gain was enough to suppress the noise from front-end. The total DC power consumption of the Rx is 18 mW.

3.5.4 Transceiver

Fig 3.26 shows the chip photo of the transceiver. The size of the chip is 1.93×1.25 mm^2 excluding pads. The SPDT switches are integrated at front- and back-end of the T/R module. The size of

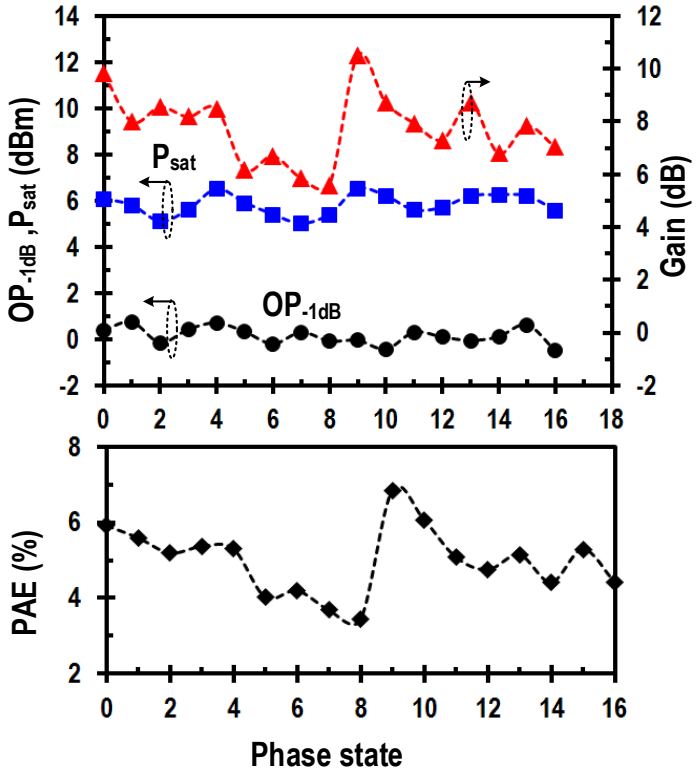


Figure 3.21: Measured power gain, OP_{-1dB}, P_{sat} and PAE over 16 phase states at 94 GHz of Tx.

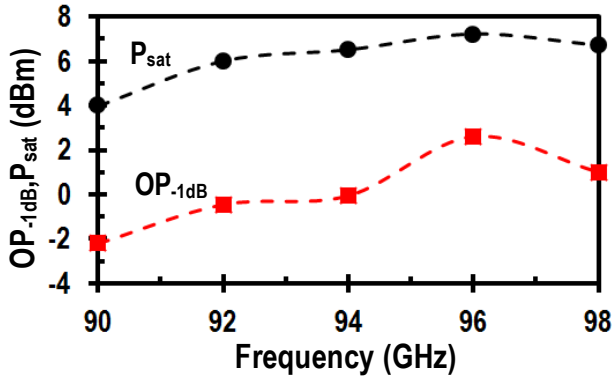


Figure 3.22: Measured output P_{-1dB} (OP_{-1dB}) and saturated output power (P_{sat}) verses frequency at highest gain state of Tx.

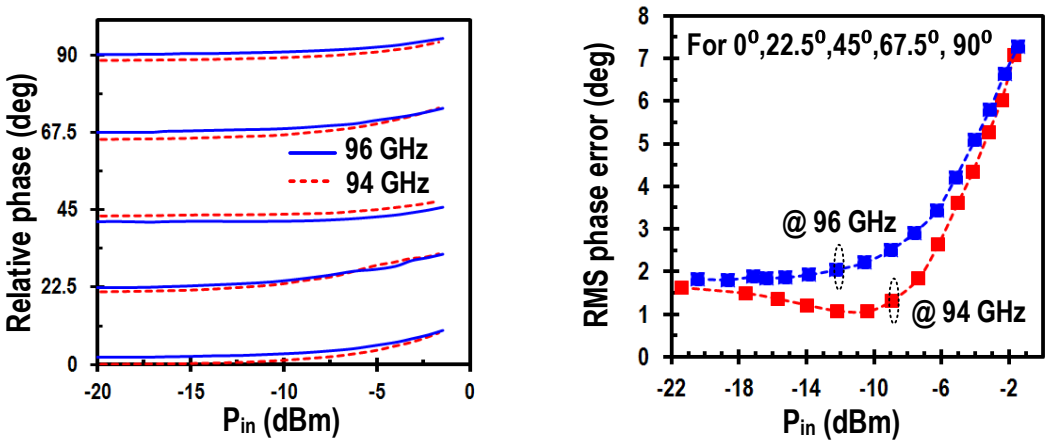


Figure 3.23: Measured: (a) Relative phase, and (b) RMS phase error verses input power at 94 GHz and 96 GHz for $0^0, 22.5^0, 45^0, 67.5^0$ and 90^0.

the Rx channel is smaller than Tx channel, so an extra 200 μm T-line is used to connect the Rx output with the back-end SPDT switch. The loss of the T-line is close to 0.7 dB in simulation. Fig 3.27 shows the S-parameter measurement results of the receiver only including SPDT switches. The measured gain of Rx channel with front-end and back-end switches is 14-18 dB which agrees well with simulation considering 4 dB loss in total from SPDT switches. The phase response is close to single channel Rx (see Fig 3.27(b)). S_{11} and S_{22} still remain < -5 dB. A different Tx architecture than previous section has been used for this integration which could not be measured due to stability issue.

3.6 Comparison

Table 3.3 and 3.4 shows the comparison of proposed Tx/Rx channel with the previous state of the art works for phased array system which utilizes different kind of phase shifting approach like RF active and passive PSs, LO phase shifting and base-band Cartesian type phase shifting. To compare, a Tx efficiency (η) FOM is defined by $P_{sat} \cdot (1 - 1/G_p)/P_{diss,Q} \times 100\%$ where a linear power gain G_P and DC power consumption, $P_{diss,Q}$ at quiescent bias point, are used because of the

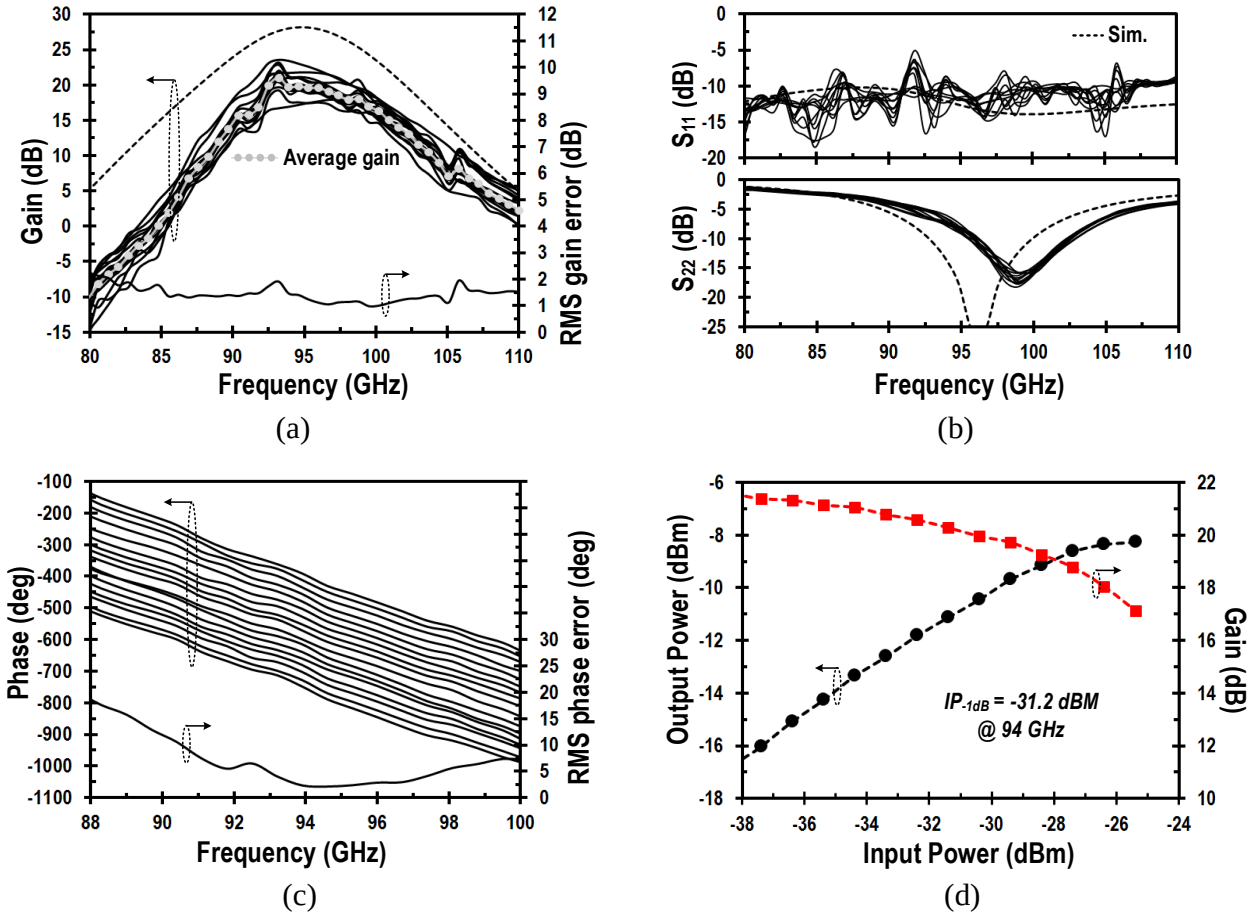


Figure 3.24: Measured (a) gain (S_{21}), (b) input (S_{11}), output (S_{22}) reflection coefficients, (c) absolute phase response and RMS phase error versus frequency for 16 phase states, and (d) Output power and gain versus input power at 94 GHz of the receiver.

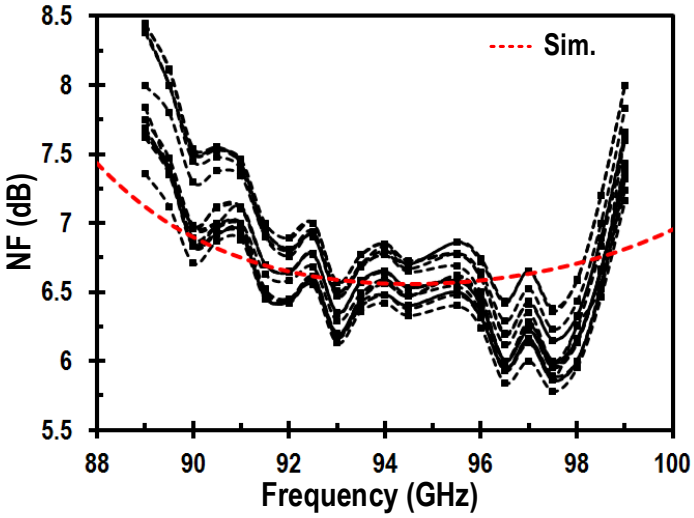


Figure 3.25: Measured noise figure of the receiver over 16 phase states.

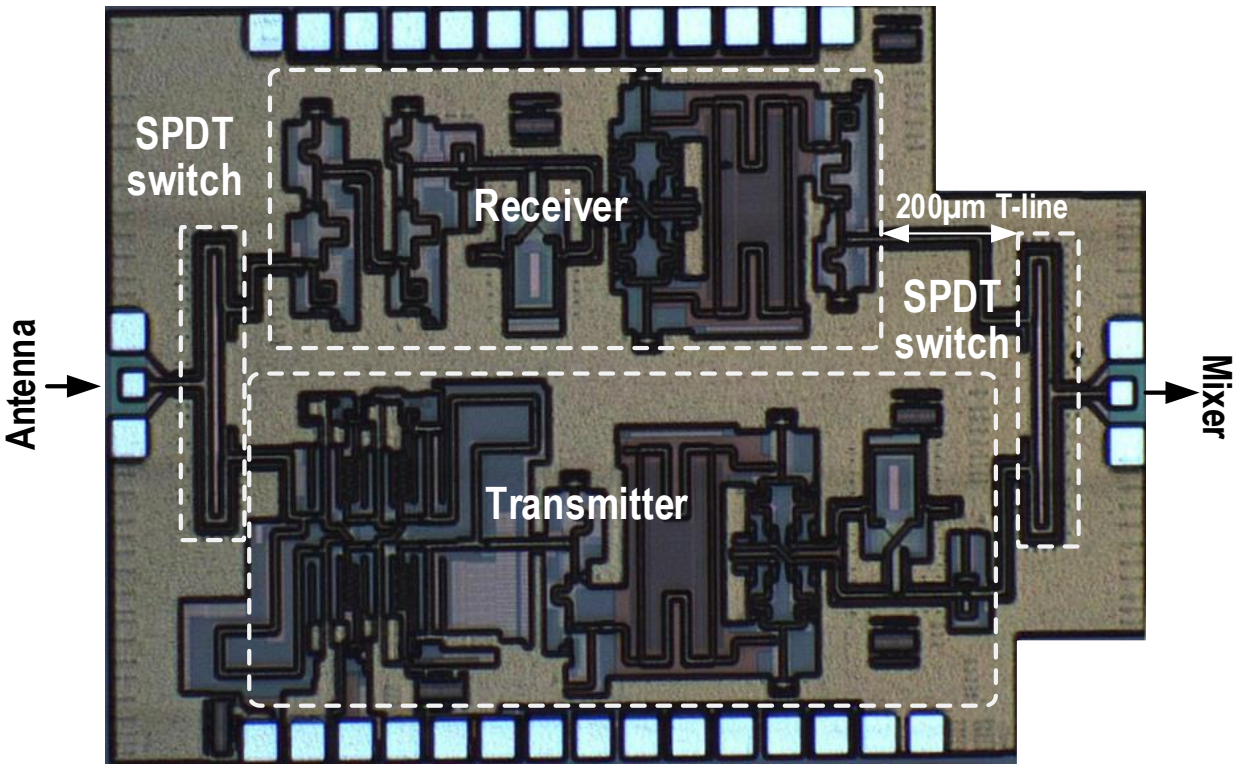


Figure 3.26: Chip photo of the transceiver (The chip is 1.93×1.25 mm^2 excluding I/O pads).

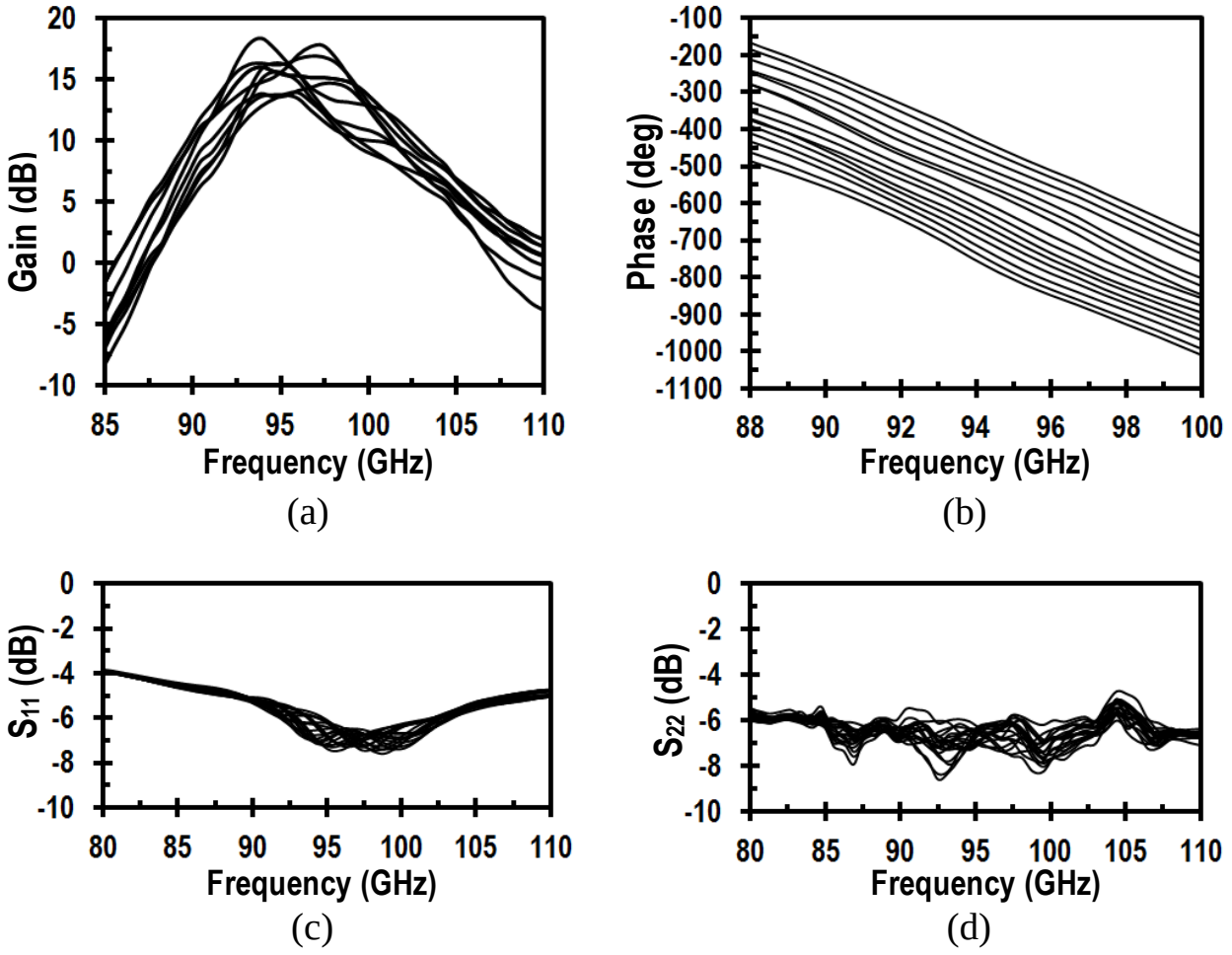


Figure 3.27: Measured S-parameter results of Transceiver: (a) gain, (b) 4-bit phase response, (c) input (S_{11}) and (d) output (S_{22}) reflection coefficients.

Table 3.3. Tx Channel Performance Summary and Comparison with State-of-the-art works

Reference	Freq. (GHz)	PS Topology	Gain (dB)	P_{sat} (dBm)	P_{diss} (mW) / Channel	++Tx η FoM (%)	Process
This Work	92-98	Passive VM (Power Combining)	7.5-12	6-7.2	26	18	0.13μm SiGe BiCMOS
JSSC 2010 Yu *et al.* [30]	60	Active VM (Current Combining)	7.7	8.3	168	3.4	65nm CMOS
JSSC 2013 Sharamian *et al.* [27]	78-97	Active VM (Current Combining)	19	8.5	250*	2.8	0.18μm SiGe BiCMOS
TMTT 2013 Golcuk *et al.* [28]	90-100	Active VM (Current Combining)	17	-4.4	137	< 1	0.13μm SiGe BiCMOS
JSSC 2011 M.Tabesh *et al.* [21]	58.75-65	Active VM @Baseband (Current Combining)	NA	-1.5	27	< 2.6	65nm CMOS
TMTT 2012 J.L.Kuo *et al.* [25]	57-66	Passive Switched LC	< 0.5	7	100	< 1	65nm CMOS
JSSC 2010 A.V.Garcia *et al.* [34]	57-65	RTPS	30	12	164	9.7	0.13μm SiGe BiCMOS
TMTT 2015 Natarajan *et al.* [29]	88-96	RTPS	> 25	6.3	116	3.7	0.13μm SiGe BiCMOS
JSSC, 2017 A. Townley [36]	94	LO phase shifting	-	6.5	71	6.3**	0.13μm SiGe BiCMOS

++: Tx η FOM is calculated from $P_{sat}(1-1/G_p)/P_{diss}$@quiescent x 100%, *Including Mixer. **Simulated efficiency (P_{sat}/P_{diss})

Table 3.4. Rx Channel Performance Summary and Comparison with State-of-the-art works

Reference	Freq. (GHz)	PS Topology	Gain (dB)	NF (dB)	IP_{-1dB} (dBm)	P_{diss} (mW) / Channel	++PNDR (dB·Hz/mW)	Process
This Work	92-98	Passive VM (Power Combining)	23	5.8-6.6	-31.4	18	7.6	0.13μm SiGe BiCMOS
JSSC 2010 Yu *et al.* [30]	58.25-63.75	Active VM (Current Combining)	12	6.7-7.2	-16	78	1.9	65nm CMOS
JSSC 2013 Sharamian *et al.* [27]	78-97	Active VM (Current Combining)	19	7	-33	250*	0.5	0.18μm SiGe BiCMOS
TMTT 2013 Golcuk *et al.* [28]	90-100	Active VM (Current Combining)	26-29	9-11	-28	69	2	0.13μm SiGe BiCMOS
JSSC 2015 Kundu *et al.* [22]	44-66	Active VM @ Baseband	26	5.5	-27	30	4.7	45nm SOI CMOS
JSSC 2017 A. Townley *et al.* [36]	94	LO phase shifting	-	< 9.5	-19	56	-	0.13μm SiGe BiCMOS
JSSC 2012 S.Y Kim *et al.* [33]	76-84	Passive Switched LC	10-19	10.5	-26	33	4.2	0.13μm SiGe BiCMOS
JSSC 2011 Natarajan *et al.* [31]	58-65	RTPS	18	6.8-7.3	-28**	57	2.4	0.13μm SiGe BiCMOS
TMTT 2015 Natarajan *et al.* [29]	88-96	RTPS	30	8	-37	80	1.6	0.13μm SiGe BiCMOS

++: PNDR is calculated from $[(174 + IP_{-1dB}(dB) - NF(dB)]/P_{diss}$, *Including Mixer, **$IP_{-1dB}$ of LNA only.

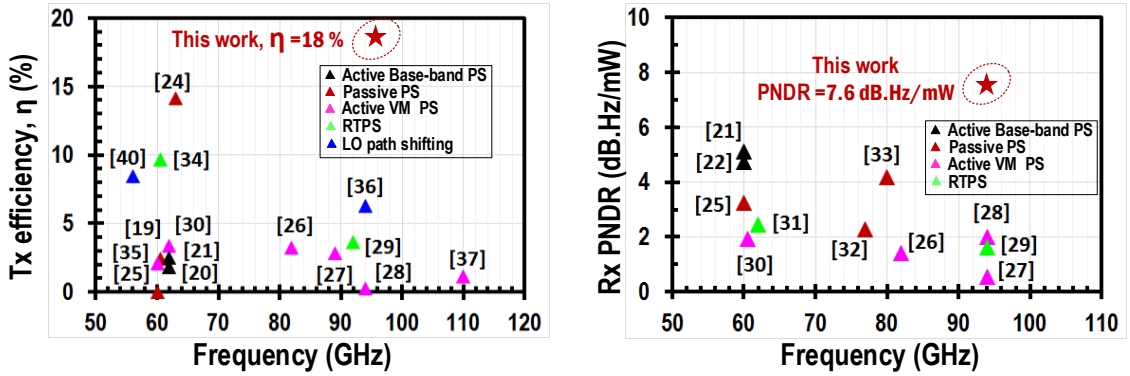


Figure 3.28: Graphical representation of comparison of Tx efficiency (η) and Rx power normalized dynamic range ($PNDR$) FOM with prior phased array works.

lack of information on the G_P and P_{diss} at P_{sat} point in the prior Tx channels. For fair comparison of Rx channel, a power normalized dynamic range, $PNDR = (174 - NF + IP_{-1dB})/P_{diss}[mW]$ is introduced to evaluate Rx efficiency collectively by taking dynamic range (DR) and P_{diss} into account in table 3.4. With significantly low P_{diss} (Tx: 26 mW and Rx: 18 mW) because of a low loss in the power-domain phasing system, the proposed Tx channel η FOM is 18% and Rx achieves 7.6 dB·Hz/mW $PNDR$, are far superior to the other works. Fig 3.28 shows a graphical representation of the comparison of T/R channel FOM of different types of phase shifting approach for a wide range of mm-wave frequencies (60-120 GHz). It shows, the FOM of the proposed T/R channel is not only superior at W-band, but also higher than any previous works for phased arrays at 60-120 GHz frequency band.

3.7 Summary

A W-band phased array transmit/receive channel employing 90^0-hybird phase-interpolator based phase shifting subsystem is implemented in 0.13μm SiGe BiCMOS process. The proposed phase shifter architecture exhibits a high power efficiency performance because of having low loss PS which can be compensated with relatively small DC power penalty, compared to prior pure passive or active PSs. Utilizing this phase shifter, the W-band T/R channel achieves a record high Tx

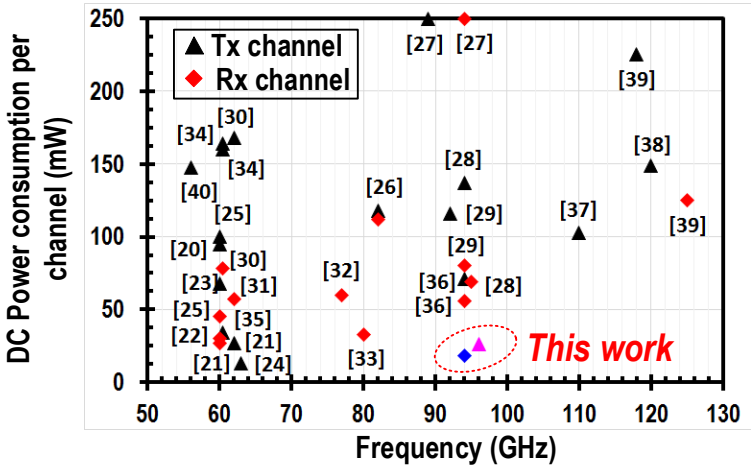


Figure 3.29: Comparison of DC power consumption per element of phased array front-end with previous works at mm-wave frequencies.

efficiency and Rx power DR FOM at the expense of the lowest DC power compared to prior state-of-the-art integrated T/R channels at W-band in silicon technology (see Fig 3.29). The high power efficiency is particularly promising for practical large-scale phased arrays at high-end mm-Wave frequencies.

Chapter 4

A Low power 120 GHz Two-Element Phased Array Receiver using Quadrature Hybrid Based Phase Interpolator

Thanks to a low loss transmission window around 120 GHz, D-band is utilized for multi-Gb/s wireless communications and high resolution imaging and radar sensors. The outdoor wireless links at 120 GHz require high gain antennas to overcome propagation loss, requiring large scale phased arrays. It is challenging, however, to design phase shifters (PSs) to be low loss and power efficient, making the large arrays impractical at D-band, especially in silicon (Si) process. In general, passive LC switch based PSs or reflection type PSs tend to cause a high loss as discussed before [33, 29], suboptimal for power-efficient D-band application. Vector modulators (VMs) have been popular at W-band [28, 27] and D-band [39] [64]. LO phase shifting approach has been also used at high-end D-band with the expense of large dissipation [65]. But the power efficiency is still limited, claiming a large DC power dissipation (P_{diss}), and raises significant thermal management issues for large-scale arrays.

This chapter describes a two-element phased array receiver in $0.13\mu m$ SiGe BiCMOS process at 120 GHz by utilizing power domain phase shifting approach as described in chapter 2. The

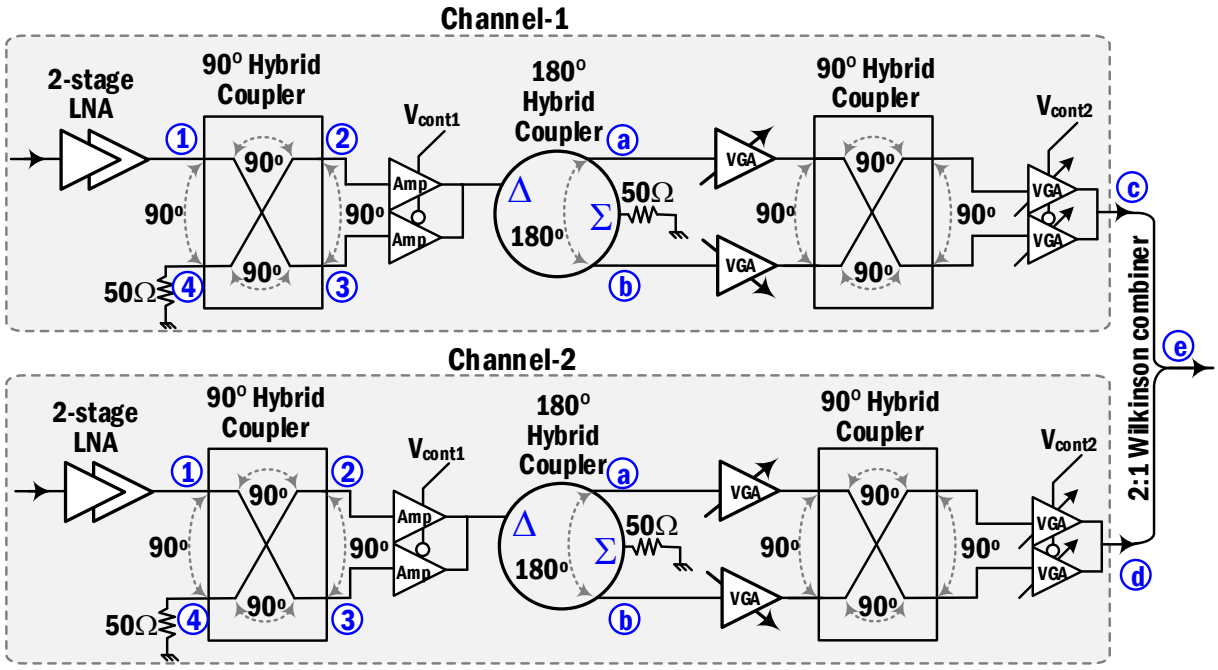


Figure 4.1: Block diagram of two-element 120 GHz phased array system.

phase shifter is based on pure passive hybrid couplers and the overall loss of the phase shifter is contributed by the ohmic loss of the transmission lines and the 3-dB loss for power splitting. The loss can be compensated with a small DC power penalty, compared with prior VMs. This results the proposed receiver achieves one of the highest gain efficiencies at D-band.

4.1 Phased Array Architecture

Fig 4.1 shows the block diagram of 120 GHz two channel receiver utilizing quadrature hybrid based phase interpolator phase shifter which is composed of two VGAs and a 90^0 hybrid coupler. Each receiver channel consists of two-stage LNAs followed by the phase shifter. The input signal at ① splits into ② and ③ with a factor of $1/\sqrt{2}$ by the 90^0 hybrid. An active switch is used to select between ② and ③, and differential signals are generated at ⓐ and ⓑ using 180^0 hybrid coupler before processing by the phase interpolator. The differential signals are weighted by VGAs and combined in a quadratic way at the output of the 90-hybrid coupler. Another active switch is used

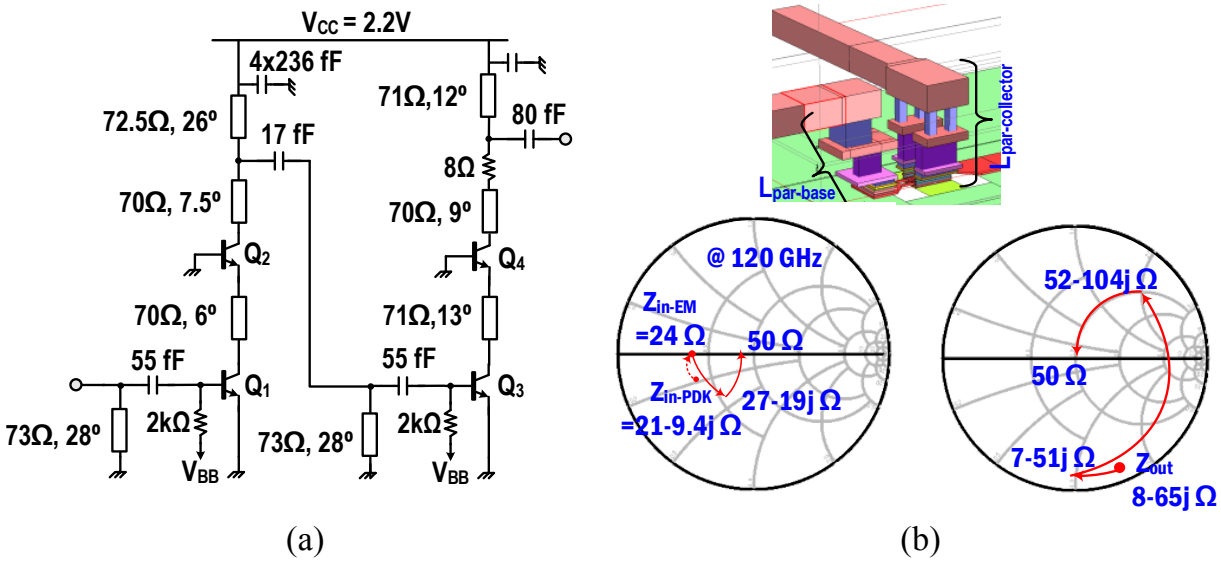
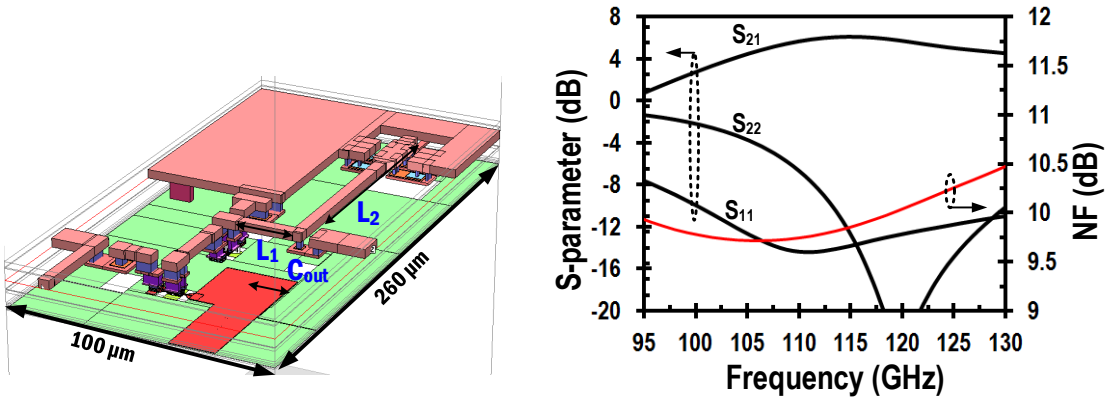


Figure 4.2: (a) Schematic of Two-stage LNA, and (b) input and output matching of first-stage of LNA with transistor interconnection in SONNET.

to select the final output between the outputs from 90^0, resulting in a fully 360^0 phase rotation. Both hybrid couplers are wide-band transmission line (T-line) based structures. The overall loss of the phase shifter is contributed by the passive hybrids only. In order to account the loss factors: 4×2 (90^0 hybrid) + 1.5 (180^0 hybrid) = 9.5 dB considering $1/\sqrt{2}$ power split and 1-1.5 dB ohmic loss at 120 GHz. The loss can be compensated by active switch amplifier with relatively low DC power penalty, resulting in a low power phased array architecture at D-band frequencies

4.2 Building Block Design

The design is done in $0.13\mu m$ SiGe BiCMOS process (f_T/f_{max}=200/220 GHz, IBM8HP) [52]. At 120 GHz (λ= $1200\mu m$), each μm length of T-line gives $\sim 0.3^0$ of phase shift, resulting in a large inductance even with small interconnection lines. So careful electromagnetic (EM) simulation of all interconnections are done using 2D simulator SONNET.

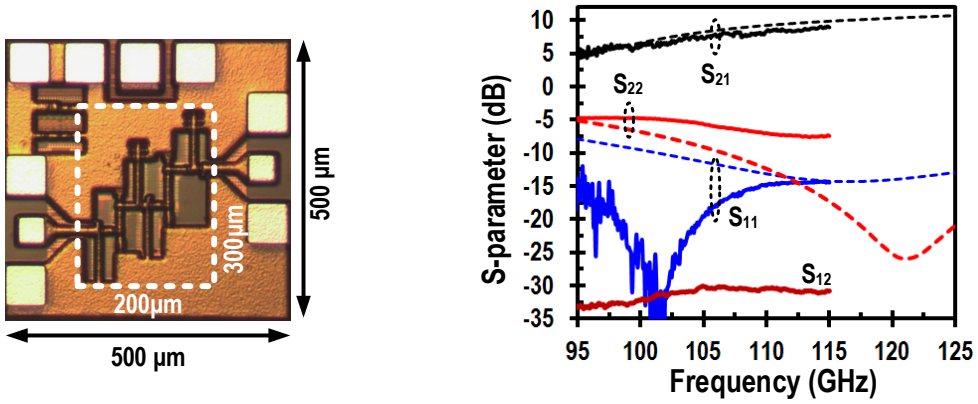


(a) (b)

Figure 4.3: (a) SONNET layout, and (b) simulation results of first stage of LNA.

4.2.1 Design of 120 GHz LNA and Measurement Results

Fig 4.2 shows the design of two-stage LNA which is based on standard cascode topology. The emitter length of each transistor is $6\mu m$ and is biased with 4 mA current from 2.2V supply. The transistor is operating close to peak cut-off frequency (180 GHz). A large input capacitance of Q_1, C_{be} ($\sim$140-160 fF) gives an input impedance of $21-9.4j\Omega$, shown in smith chart (see Fig 4.2(b)). The via stack up to the top metal layer (AM) adds 11$\sim$13 pH parasitic inductance ($L_{par-base}$) at the base, resulting in a real impedance of $\sim 24\Omega$ at the base of Q_1. A T-type LC section is used for input matching. The interconnection lines between cascade transistors including via inductance at the collector side ($L_{par-collector}$) are carefully characterized in EM simulation which can result up to 8^0 of phase shift at 120 GHz. The T-type LC section is also used for output matching where Z_{out} of the transistor is 8-65j Ω, resulting in a high Q-matching at the output. In order to improve the BW, a small n-type diffusion resistor (8Ω) is used at the output of the second-stage amplifier. Multiple dual-MIM capacitors are used at the end of the drain inductor in order to have solid AC ground at 120 GHz. Fig 4.3(a) shows the SONNET layout of first stage LNA. The simulated gain is 5 dB and NF is 9.6 dB at 120 GHz (see Fig 4.3(b)). So 10 dB of simulation gain is achieved from two stage LNAs. Fig 4.4 shows the chip photo and the measurement results of two-stage LNA. The two-stage LNA core size is 200×300 μm^2. The measurement is done upto 115 GHz.



(a) (b)

Figure 4.4: (a) Chip photo (core size: 200×300 μm^2), and (b) measured S-parameter results of Two-stage LNA.

The measured gain is 9 dB at 115 GHz which is well-matched with simulation. $S_{11} < -10$ dB at 95-115 GHz. The deviation of the output matching from the simulation is due to the model mismatches in diffusion resistance but still keeps $S_{22} < -5$ dB above 100 GHz.

4.2.2 Active Switch Amplifiers

The active switch amplifier is used to select the output from 90^0-hybrid coupler. Fig 4.5(a) shows the schematic of active switch amplifier. Cascode based amplifier has been used to have improved isolation between input and output. When the non-selected condition (V_{cont}=1), Q_3 and Q_4 are turned OFF by cutting off the bias of Q_3. The signal leakage at OFF state of the amplifier is below -30 dB. The OFF state parasitic, $C_{\mu OFF}$ and $C_{\pi OFF}$, which can be as high as 30fF, are considered in designing input and output matching networks. All the transistors are biased at 3.5-4mA current from the 2.2V supply. The simulated S-parameter results are shown in Fig 4.5(b). The gain is 5 dB and input reflection coefficients are below -10 dB at both ON and OFF state of the transistor, which is required for low phase error in preceding 90^0 hybrid coupler.

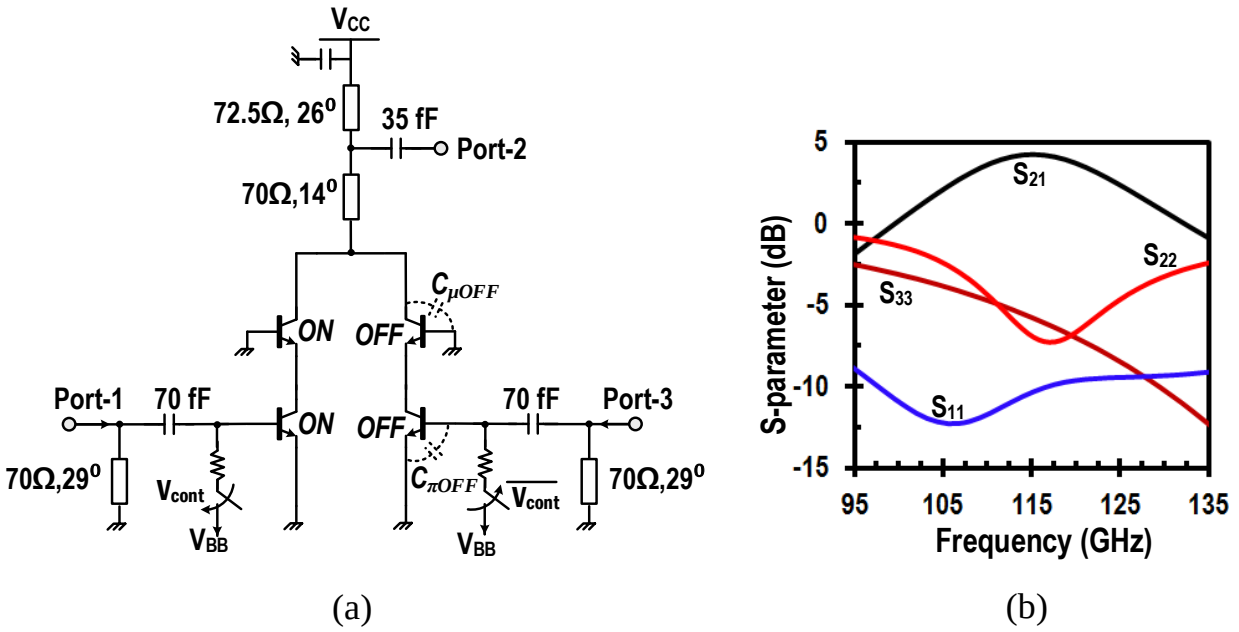
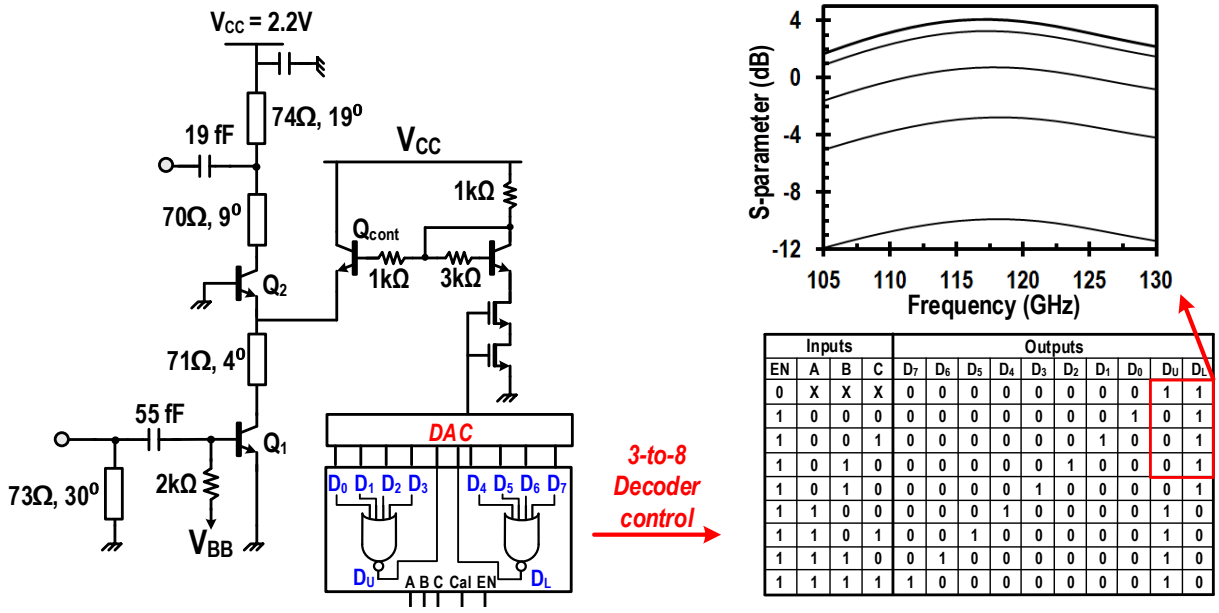


Figure 4.5: (a) Schematic of switched amplifier, and (b) S-parameter simulation results of switched amplifier when port-1 is selected as input.



Inputs				Outputs									
EN	A	B	C	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_U	D_L
0	X	X	X	0	0	0	0	0	0	0	0	1	1
1	0	0	0	0	0	0	0	0	0	0	1	0	1
1	0	0	1	0	0	0	0	0	0	1	0	0	1
1	0	1	0	0	0	0	0	0	1	0	0	0	1
1	0	1	0	0	0	0	0	1	0	0	0	0	1
1	1	0	0	0	0	0	1	0	0	0	0	1	0
1	1	0	1	0	0	1	0	0	0	0	0	1	0
1	1	1	0	0	1	0	0	0	0	0	0	1	0
1	1	1	1	1	0	0	0	0	0	0	0	1	0

Figure 4.6: Schematic of VGA with DAC control and simulated S-parameters of the upper VGA of the phase interpolator at 5-different gain states.

4.2.3 VGAs and DAC

Variable gain amplifier (VGA) (see Fig 4.6) in phase interpolator has the same topology as LNA, except the gain control is done by steering the current of Q_2 by changing the bias of Q_{cont} using a 4-bit control of DAC. The digital inputs are decoded by a 3-to-8 decoder as shown in the table in Fig 4.6. The truth table shows the contol bits of the upper and lower VGAs in phase interpolator. When the gain of a VGA varies, the other one remains at maximum gain state. The simulation result shows the upper VGA gain varies $-10\sim4$ dB for five different digital control states without any calibration. With calibration, the gain can be as low as -18 dB which results nearly cutoff region of the amplifier. The lower VGA gain control is done in a similar way while keeping upper VGA at maximum gain state. Fig 4.7 shows the control circuits of upper and lower VGAs, thus a total 9 phase states at each quadrant are achieved. So the phase shifter was originally designed for 5-bit phase states. A $100\mu A$ reference current has been used for DAC and the successive PMOS sizes are set to 4x, 5x, 5.6x, 6.4x and 8x where x(=$5\mu m$) is the width of the driving MOSFET. All transistors have channel length of 500nm. The sizing of transistors are set based on the required phase, so the gain step is not uniformed.

4.2.4 Passive Devices: Hybrids and Wilkinson Combiner

The 90^0 and 180^0 hybrid couplers are based on $\lambda/4$-based distributed structures. Meandering lines are used in order to reduce the area of the hybrids. Fig 4.8 and 4.9 show the SONNET layout of the hybrid networks and the simulation results. For the 90^0 hybrid, the minimum width of $4\mu m$ AM layer over LY as the ground is used for 50Ω T-line, resulting in a loss of maximum 2.5 dB and phase error is 2^0 at 120 GHz. The phase error $< 5^0$ for wide frequency range, 100-130 GHz. All the port matching and isolation between port 1 and 4 remain below -10 dB at 90-130 GHz. The 180^0 hybrid coupler has relatively larger size (core size: 230$\times$ 480 μm^2) and $4.7\mu m$ of AM layer over MQ layer as ground is used for 70Ω line impedance. The loss of 180^0 hybrid is maximum 1.1 dB and the phase error is $< 10^0$ over 115-130 GHz. Reflection coefficients at input and outputs

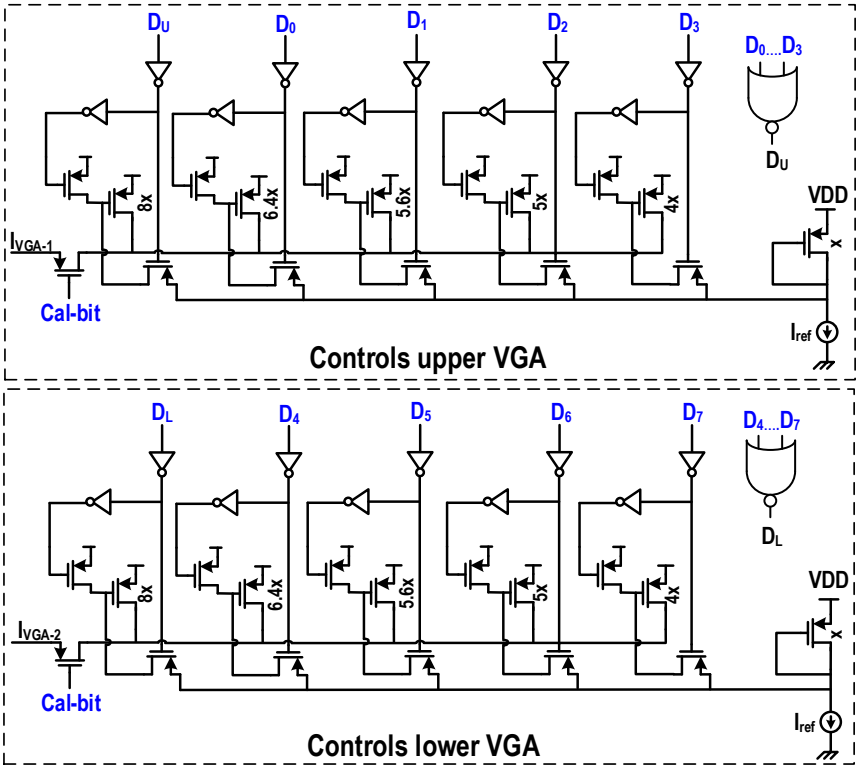


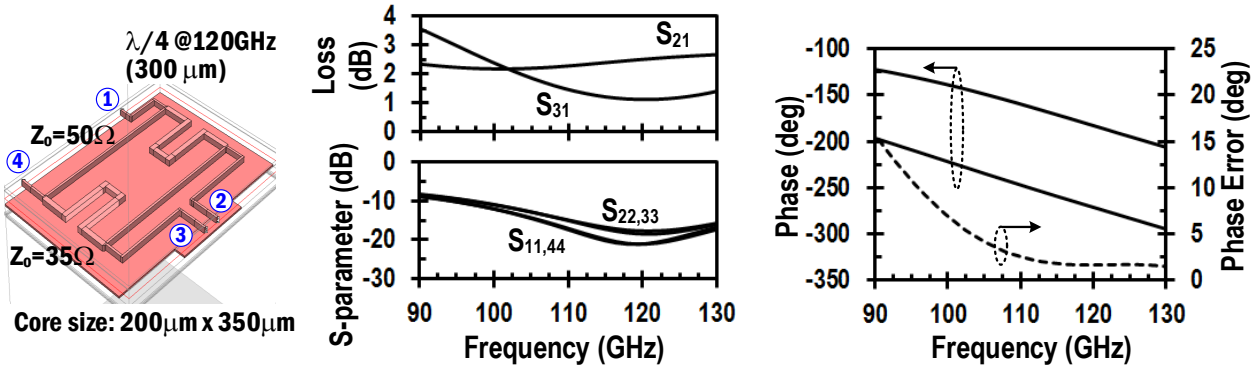
Figure 4.7: Schematics of the DAC control for both upper and lower VGAs.

are < -10 dB at 90-135 GHz. A 2:1 Wilkinson power combiner (see Fig 4.10), realized with $\lambda/4$ T-line of 70Ω impedance to combine the outputs from each receiver channel. The maximum loss of the combiner is 0.75 dB and the isolation between two inputs remains < -25 dB at 110-130 GHz. S_{11} and S_{11} is -20 dB at 90-130 GHz.

The simulated single channel receiver gain is maximum 17 dB with 5-dB gain variation. The simulated NF of Rx channel is 10-12 dB and input 1-dB compression point is -21.5 dBm. The two channel power gain is 19.5 dB when both channels are at maximum gain state.

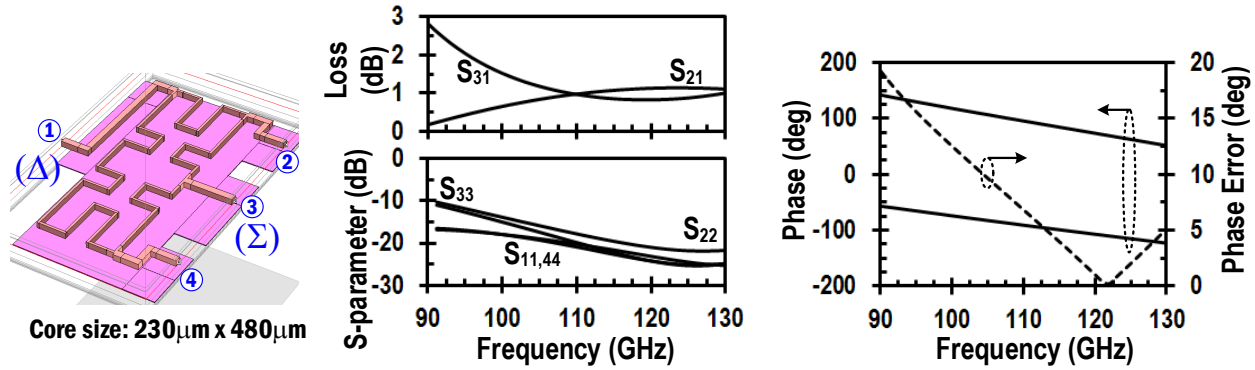
4.3 Measurement Results

Fig 4.11 shows the chip photo of two-element phased array receiver. The core size is 1.7$\times$1.24 mm^2 excluding I/O pads. The size of a single channel is 1.5$\times$0.55 mm^2. The S-parameter mea-



(a) (b) (c)

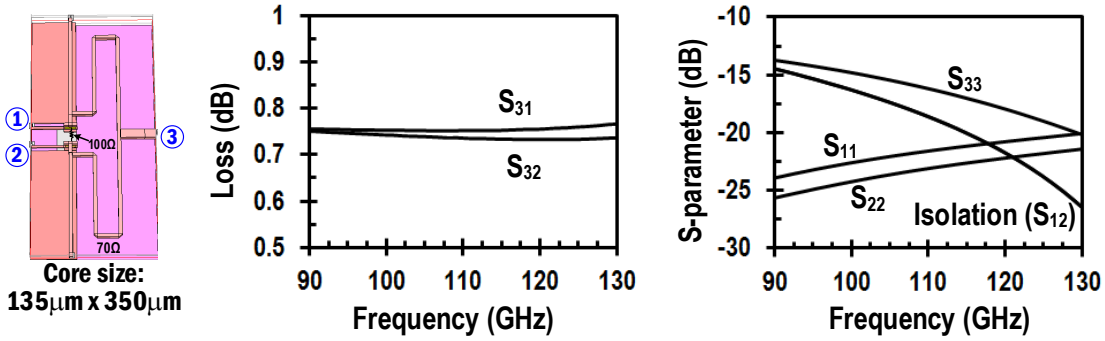
Figure 4.8: (a) SONNET layout, (b) loss and I/O matching, and (c) phase response of 90^0-hybrid coupler.



(a) (b) (c)

Figure 4.9: (a) SONNET layout, (b) loss and I/O matching, and (c) phase response of 180^0-hybrid coupler.

surement of the single channel Rx has been done up to 115 GHz using W-band set-up: W-band GSG probe and frequency extension module (70-115 GHz) after SOLT calibration. Input and output pad transition loss ($\sim$1-1.5dB at $>$ 100 GHz) are de-embedded from the measurements. Fig 4.12 shows the S-parameter measurement results. The measured gain is 11-15.6 dB with 1.53 dB RMS gain error at 115 GHz for 4-bit phase resolution. The gain error is $<$ 2 dB at 108-115 GHz. The RMS phase error is 5^0 at 115 GHz and remains $< 9^0$ at 107-115 GHz GHz. S_{11} is < -10 dB at 95-115 GHz. The measured S_{22} is close to simulation. The DC power consumption per channel



(a) (b) (c)

Figure 4.10: (a) SONNET layout, (b) loss, and (c) I/O matching and isolation of wilkinson combiner.

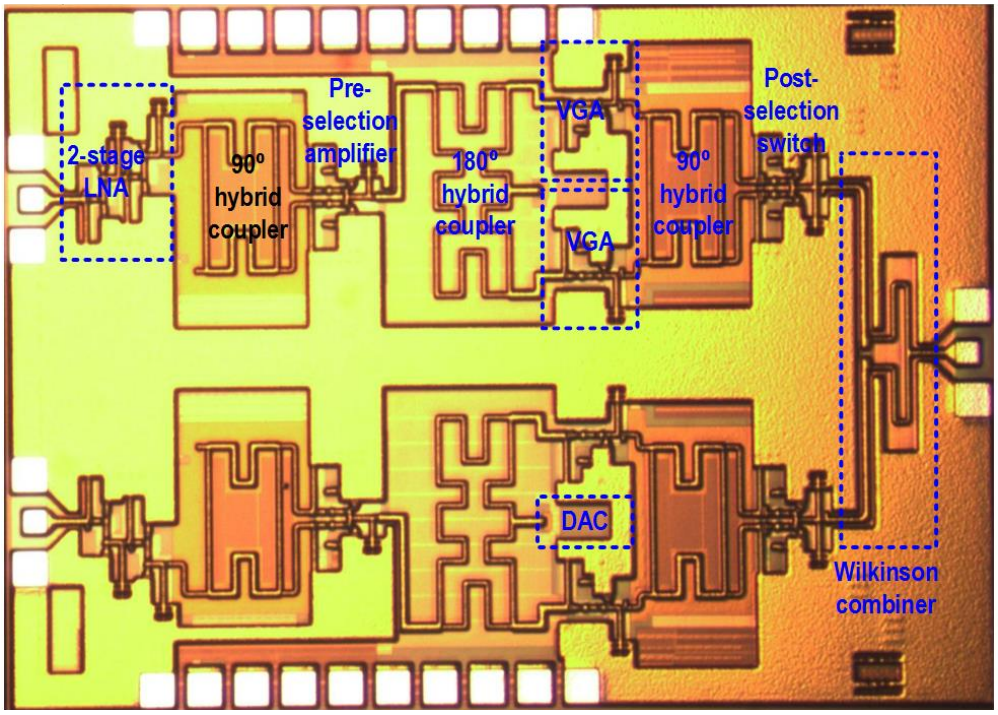


Figure 4.11: Chip photo of two-element phased array receiver (chip size: 1.7×1.24 mm^2), each element size: 1.5×0.55 mm^2.

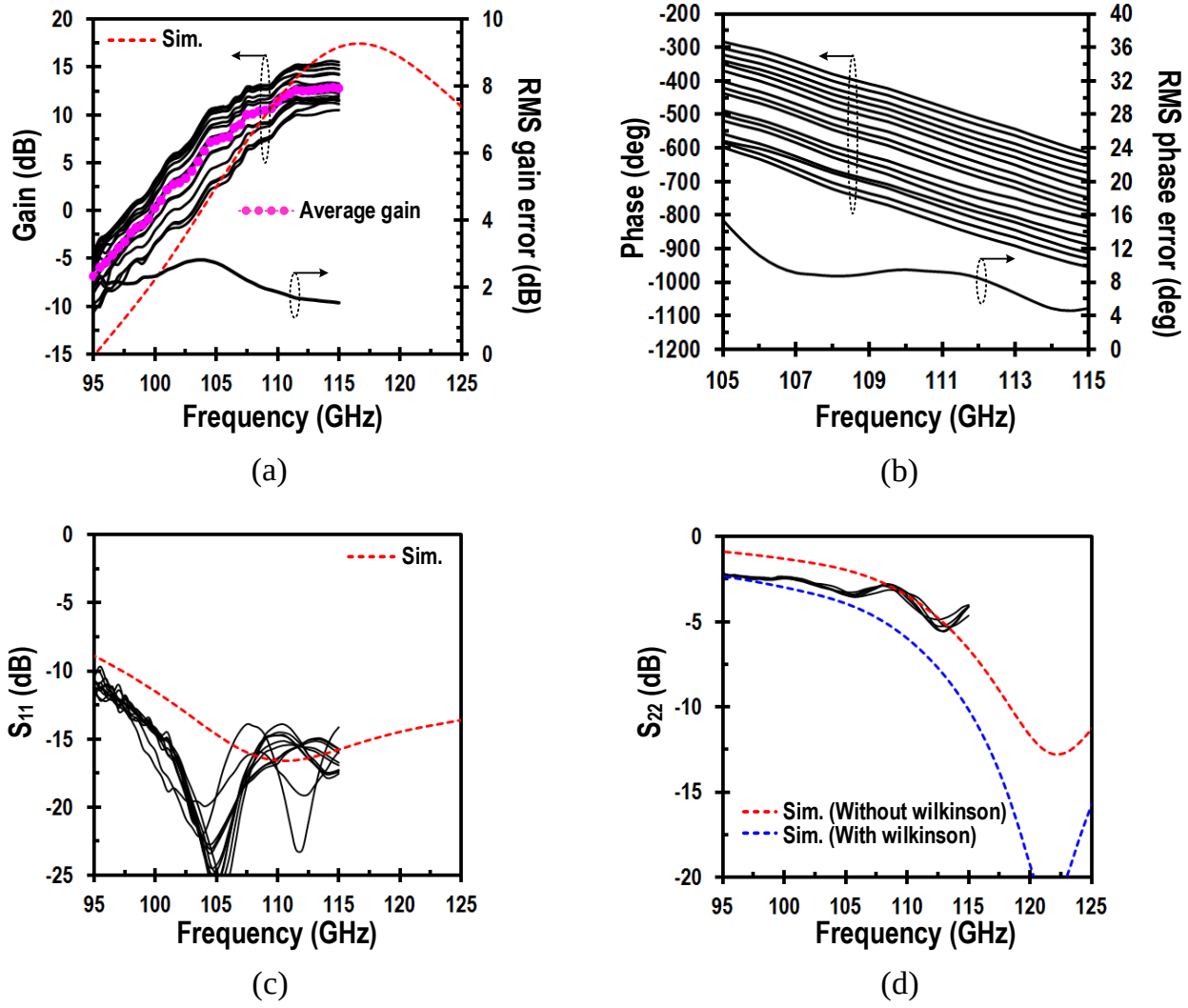


Figure 4.12: Measured Rx channel performances: (a) small signal Gain and RMS gain error, (b) 4-bit phase responses and RMS phase error, (c) input reflection coefficient (S_{11}) and (d) output reflection coefficient (S_{22}) of single channel phased array receiver.

Table 4.1.
Comparison of phased array T/R elements in advanced Si technologies

Metric	This work	Ozturk, SiRF, 2016 [22]	W. Shin JSSC,2012 [37]	Elkhouly, GMC, 2012 [38]	A. Vahdati, EuMA,2015 [64]	B. P. Ginsburg, JSSC 2014 [65]
Frequency (GHz)	115	125	110	120	105	160
Topology	RF Passive VM	RF Active VM	RF Active	RF Active	RF Active VM	LO PS using T-lines
# of element	2 Rx	1 Rx	4×4 Tx	2 Tx	Only PS	4×4 Rx
Gain/element (dB)	15.6	15	12.5	-10	2.5	29**
NF (dB)	10-11*	-	-	-	-	22.5**
IP-1dB (dBm)	-21.5*	-17.3	-	-19	-	-
Phase resolution	4	> 4	2	4	2	5
RMS gain/ phase error	< 1.3 dB/ 5.5°	-	-	-	1.5 / <13°	-
Pdiss (mW)	53	125	> 103	148	123	313**
Process	0.13μm SiGe BiCMOS (f_T =200 GHz)	0.13μm SiGe BiCMOS (f_T =250 GHz)	0.18μm SiGe BiCMOS (f_T =240 GHz)	0.25μm SiGe BiCMOS (f_T =180 GHz)	28 nm CMOS FDSOI (f_T =260 GHz)	65 nm CMOS (f_T =160 GHz)

*Simulation **Whole Rx including mixer

is 53 mW from 2.2V supply. The NF and linearity could not be measured because of the lack of instrument facilities. Table 4.1 summarizes the performance of the receiver and comparison with previous F- and D-band phased array works in advanced silicon technologies. Our proposed Rx consumes lowest power consumption with high gain compared to prior works.

4.4 Summary

A 120 GHz two-element phased array receiver employing a 90^0-hybird phase interpolator based phase shifter is realized in $0.13\mu m$ SiGe BiCMOS process. The proposed Rx channel exhibits one of the highest gain efficiency performance (0.3 dB/mW) as shown in Fig 4.13. This is because of a low loss PS architecture, where the loss can be compensated with a small DC power penalty, compared to pure passive or active PSs, making the proposed Rx suitable for power efficient D-band phased arrays.

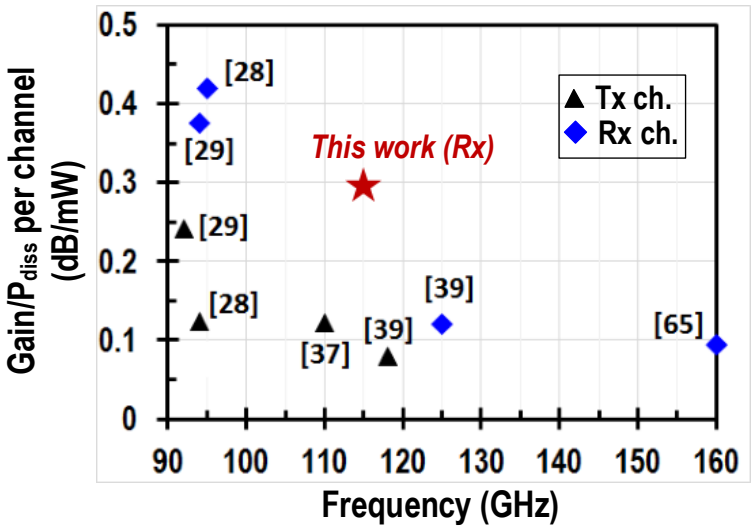


Figure 4.13: Comparison of gain efficiency (=Gain/P_{diss}) for phased array Tx/Rx single element at F- and D-band.

Chapter 5

94 GHz Bidirectional Variable Gain Amplifier for Phased Array Transmit and Receive (T/R) Applications

There has been growing research effort to realize bidirectional signal processing in T/R modules in order to minimize the power and complexity in large scale phased arrays [24, 66]. Fig 5.1 shows conventional T/R module architecture adopting a common leg comprised of variable gain amplifier (VGA), phase shifter (PS), and two single-pole-double-through (SPDT) switches. The SPDT switches establish bidirectional signal flow in order to process both transmit and receive signals in the common leg. Indeed, for millimeter wave applications the cumulative insertion loss from a series of passive switches could be significant in silicon technology. This is because of higher switch transistor turn-on resistance at the high frequency. While it has been popular in discrete T/R implementation at RF to microwave ranges, the traditional architecture is vulnerable to substantial signal loss in integrated circuit (IC) technologies especially at mm-wave frequencies. For an example, typical SPDT switch insertion loss would range 2.5-3 dB in SiGe BiCMOS technologies at W-band [54]. This could cause around 8-10 dB or more signal loss in the back-end three switch chain when considering extra interconnection loss between the switches in Fig 5.1(a). To

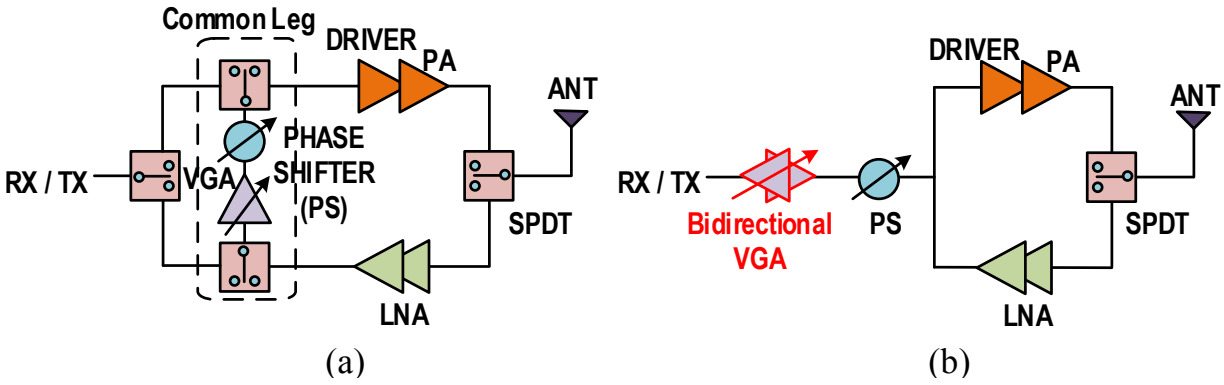


Figure 5.1: Transmit and receive (T/R) module architectures: (a) conventional T/R employing a common leg composed of phase shifter, VGA, and input/output switches for bidirectional signal processing, and (b) power-efficient T/R by employing bidirectional VGA and phase shifter to eliminate back-end SPDT switches and losses thereof for integrated phase arrays.

compensate the loss, multiple stage amplifiers are needed, potentially sacrificing power efficiency of the T/R channel substantially.

The signal loss and power efficiency penalty thereof can be improved significantly by eliminating the back-end switches and by using a bidirectional variable gain amplifier in series with a bidirectional phase shifter as shown in Fig 5.1(b). Passive phase shifters can be leveraged to achieve the bi-directionality in phase generation [33]. This work presents a bidirectional VGA at W-band in $0.13\mu m$ SiGe BiCMOS technology for more power-efficient integrated T/R channel applications.

5.1 Design Technique of W-band Bidirectional VGA

The W-band bidirectional VGA is designed using IBM8HP technology [52]. The schematic of the VGA is shown in Fig 5.2. The cascode amplifier topology is used due to its high gain and reverse isolation. All the transistors have emitter length (L_e) of 4 μm and are biased with 4.5 mA DC current ($J_C = 1.125mA/\mu A$). The transistor length and bias are chosen to have close to

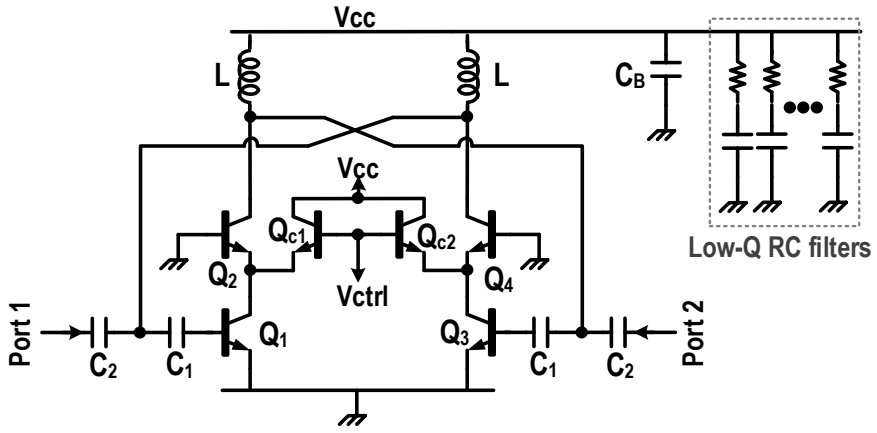


Figure 5.2: Schematic of Bidirectional variable gain amplifier.

peak f_T of 190 GHz when including parasitics of layout interconnection. In the forward operation from Port-1 to Port-2, transistors Q_1 and Q_2 are ON, and Q_3 and Q_4 are OFF, which is done by cutting off the bias current of Q_3. The reverse operation is vice versa. The gain of the VGA can be controllable by bypassing signal current from the main signal path through Q_{C1} (Q_{C2} for reverse operation).

Fig 5.3 shows impedance matching networks and step-by-step input and output impedance locus in the Smith Chart. The symmetric passive matching networks need to serve as both input and output matching when forward operation by turning off the half circuit, e.g. turning off $Q_{3,4}$ and Q_{C2} in Fig 5.2. Complete matching networks including major transistor parasitcs for input and output are shown in Fig 5.4. In the forward operation, input impedance of the transistor Q_1 is mainly determined by base ohmic resistance (r_b) and capacitances including base-emitter diffusion capacitance (C_π), resulting in a low impedance of 25-j20 (see Fig 5.3(b)). L-type LC section can be used for the input to be matched to 50Ω. However in the output node, the cascode transistor produces a high impedance (50-j250) at the output in Fig 5.3(c). To match the large impedance to 50Ω, we need another L-type LC network. Since the L is same for both cases the optimal topology of the matching network results in T-type as shown in Fig 5.4.

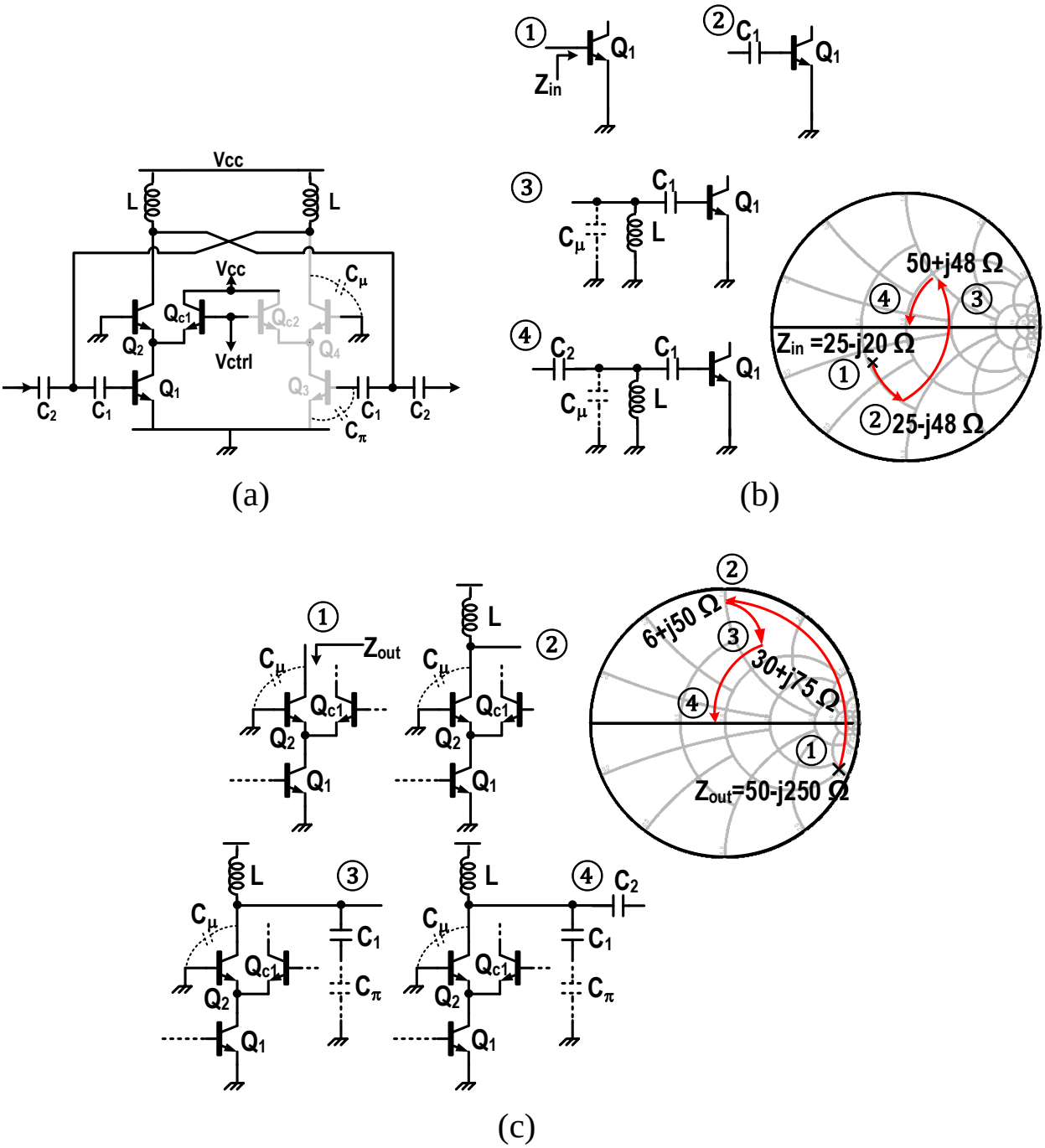


Figure 5.3: Forward operation: transistors in gray are turned off in (a), equivalent schematic of the bidirectional VGA and step-by-step descriptions of input and output impedance locus in (b) and (c), respectively.

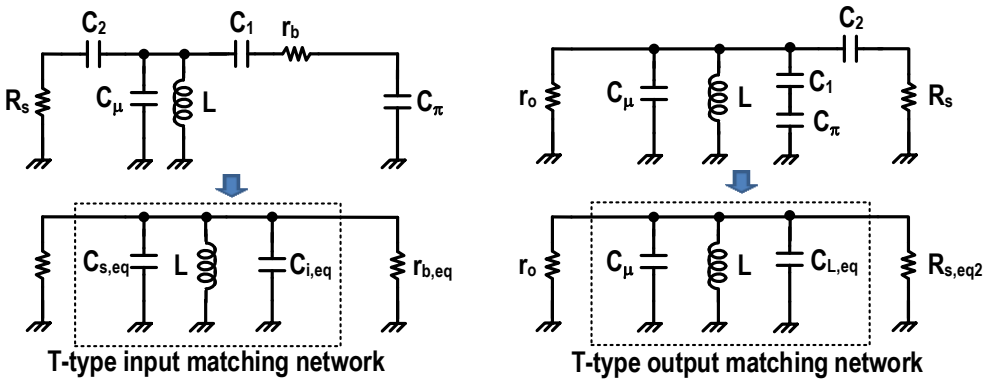


Figure 5.4: Equivalent T-type input (a) and output (b) matching networks, including the transistor parasitic resistances and capacitances.

In Fig 5.4(a), for input matching network,

$$\begin{aligned} \mathrm{R_{s,eq1}} &= \mathrm{R_s}\left(1+\mathrm{Q_1}^2\right) \\ \mathrm{C_{s,eq}} &= \frac{\mathrm{C_1 Q_1}^2}{1+\mathrm{Q_1}^2} \\ \mathrm{C_{i,eq}} &= \frac{(\mathrm{C_\pi}||\mathrm{C_1})\mathrm{Q_x}^2}{1+\mathrm{Q_x}^2} + \mathrm{C_\mu} \end{aligned} \tag{5.1}$$

Where,

$$\begin{aligned} \mathrm{Q_1} &= \frac{1}{\omega_0 \mathrm{R_s C_2}} \\ \mathrm{Q_x} &= \frac{1}{\omega_0 \mathrm{r_b}(\mathrm{C_\pi}||\mathrm{C_1})} \end{aligned} \tag{5.2}$$

In Fig 5.4(b), at output matching,

$$\begin{aligned} \mathrm{C_{L,eq}} &= \mathrm{C_1}||\mathrm{C_\pi} + \frac{\mathrm{C_2 Q_1}^2}{1+\mathrm{Q_1}^2} \\ \mathrm{R_{s,eq2}} &= \mathrm{R_s}\left(1+\mathrm{Q_1}^2\right) \end{aligned} \tag{5.3}$$

Both input and output matching occurs when the resonance condition,

$$\omega_0 = \frac{1}{\sqrt{\mathrm{L}(\mathrm{C_{s,eq}}+\mathrm{C_{i,eq}})}} = \frac{1}{\sqrt{\mathrm{L}(\mathrm{C_{1eq}}+\mathrm{C_\mu})}} \tag{5.4}$$

The matching networks act as an amplifier load as well, which causes a tradeoff between impedance matching or gain and noise performance. Any parasitic inductance in the supply line

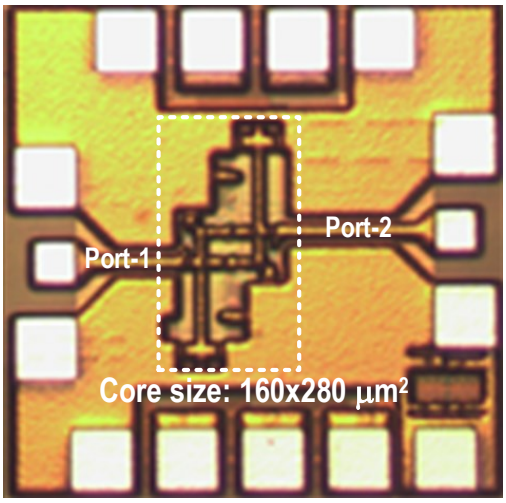


Figure 5.5: chip photograph ($0.56mm \times 0.56mm$ including pads)

would cause substantial degradation in the matching and gain. Therefore, a bypass capacitor C_B (600 fF) is added immediately after the load inductors in layout to make a solid AC ground at 94 GHz. Finally, in order to prevent low-frequency instability, low-Q on-chip filter networks composed of 20Ω resistors in series with 300-750 fF dual MIM capacitor banks are integrated in the supply line. All the transistor interconnects and passive components are characterized with electromagnetic wave simulations (SONNET). The simulated S_{11} and S_{22} are better than -10 dB. The input P_{-1dB} is -7 dBm with 6 dB gain and 0 dBm with -1 dB gain, respectively. The reverse isolation is below -30 dB in simulation. NF is 9 dB for the highest gain state. The performance of reverse operation is the same as forward case.

5.2 Measurement Results

Fig 5.5 shows implemented the chip photograph. The chip size is $0.56mm \times 0.56mm$ including input and output pads (core size: $0.16mm \times 0.28mm$). In layout, the output interconnection line to the RF pad is slightly longer than the input side. This mismatch, however, does not cause any significant performance mismatch between the reverse and forward operations as confirmed in Fig 5.6(a) and (b). The chip is measured on wafer after SOLT calibration. The gain varies from -1

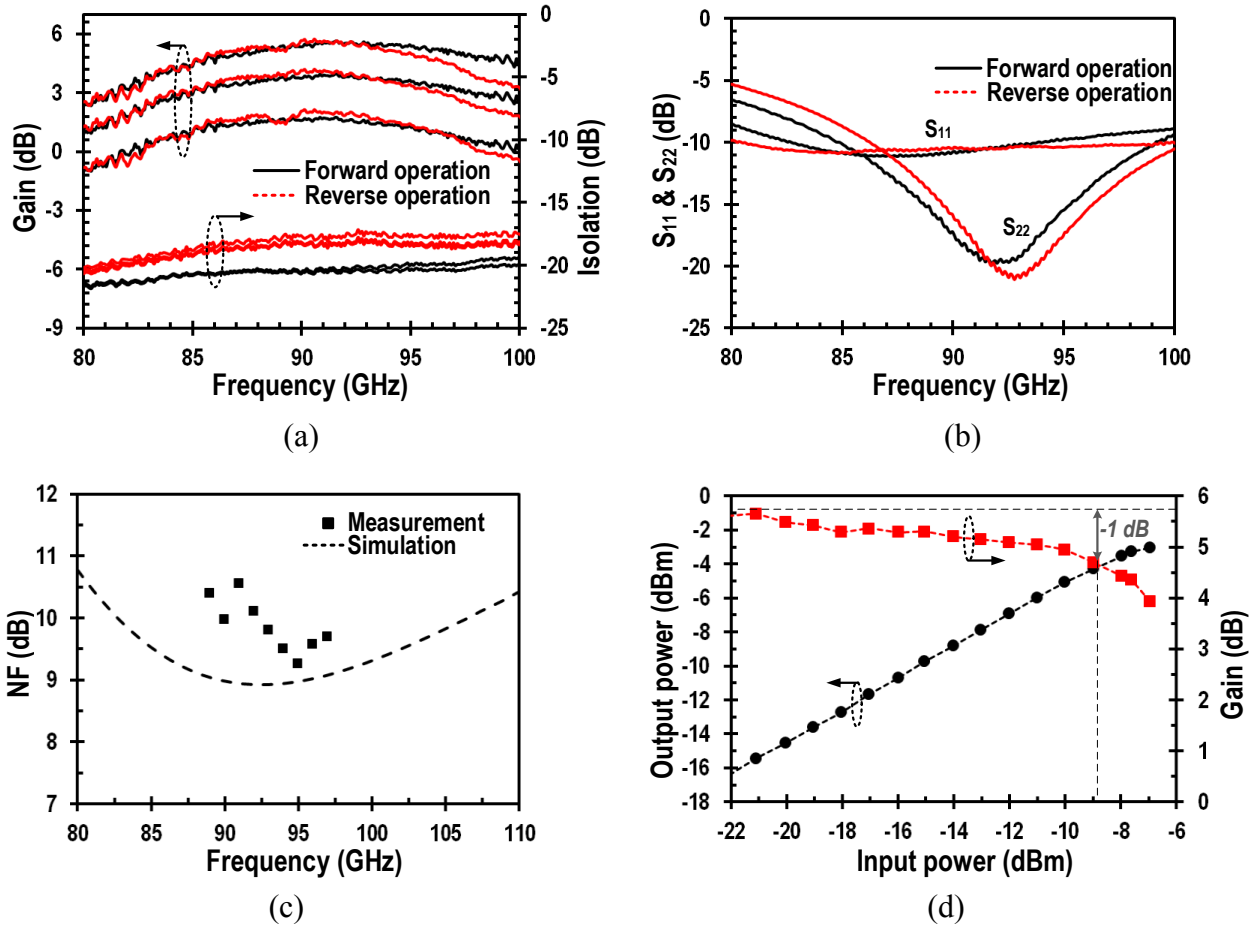


Figure 5.6: Measured (a) gain and reverse isolation for forward and reverse operations, (b) input and output impedance matching, (c) NF in the forward operation, and (d) input 1-dB compression point (IP_{-1dB}) at maximum gain state in the forward operation.

Table 5.1. Comparison of Bi-directional amplifier with previous works at mm-wave frequency

Reference	Freq. (GHz)	Gain (dB)	NF (dB)	OP_{-1dB} (dBm)	P_{diss} (mW)	# of stages	Process
This Work	82-100	5.7	9.2	-3.5	10	1	0.13μm SiGe BiCMOS
CICC, 2010 J. Kim [68]	82-97	16	11	N/A	66	10	0.13μm SiGe BiCMOS
TMTT, 2010 E. Cohen [24]	60	12	N/A	N/A	14.3	1	90nm CMOS
TMTT, 2013 S. Sim [66]	8.5-10.5	6.2	6.1	7.4	43	1	0.13μm CMOS
MWCL, 2013 M. K. Cho [67]	3-18	11	3.2-6.5	8	68	5	0.13μm CMOS

to 5.7 dB range, which is close to simulation. Fig 5.6(a) reports three different gain settings for both bidirectional operations. The gain mismatch between the forward and reverse operations is negligible, less than 1 dB. Measured reverse isolation is below -18 dB which is about 12 dB worse than simulation. This difference may arise from OFF state leakage due to parasitics which could not be captured in the design step. S_{11} and S_{22} for both forward and reverse operations are better than -10 dB over 86-98 GHz (see Fig 5.6(b)). The measurement procedure is the same as described in chapter 2 and no W-band pre-amplifier was used. The measured NF at maximum gain setting is 9.5 dB at 94 GHz which is close to simulation (see Fig 5.6(c)). The measured input P_{-1dB} is -8.5 dBm at 94 GHz (see Fig 5.6(d)). The bidirectional VGA consumes 4.5 mA current from 2.2 V power supply.

5.3 Comparison and Summary

Table 5-I shows the measurement results summary and comparison with previous bidirectional TRx works at mm-wave frequency band [24], [66]-[68]. To define figure of merit (FOM), gain efficiency which is $Gain/P_{diss}$ is defined in chapter 4. The gain efficient is plotted in Fig 5.7. It is seen that, the designed Bidirectional amplifier has superior FOM (gain efficiency=0.57 dB/mW) over prior bidirectional amplifiers for wide range of frequencies. The bidirectional amplifier can

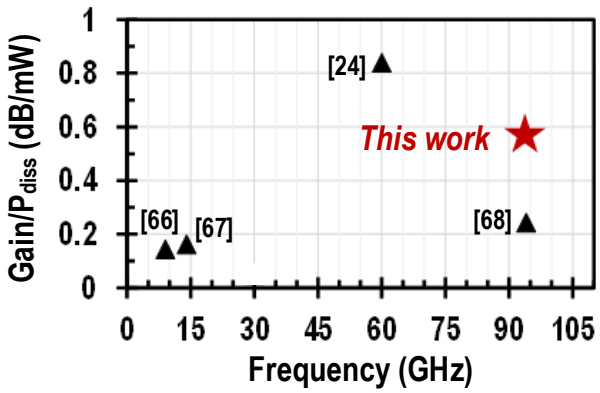


Figure 5.7: Comparison of Gain efficiency ($Gain/P_{diss}$) of Bidirectional Amplifiers from microwave upto W-band frequencies.

also be optimized to design PA/LNA by removing SPDT switch at the front-end. Thus with the bidirectional signal processing in amplifier, one can eliminate back-end SPDT switch in T/R channel and potentially front-end switch as well. This enables a minimum number of hardware use at front-end, thus reducing the overall loss and power consumption of phased array system.

Chapter 6

Conclusions

6.1 Thesis Summary

In this research, we have proposed a power domain vector modulator for W-band and D-band phased arrays in 0.13 μm SiGe BiCMOS process. In the proposed approach, the phase interpolation is accomplished in a passive way by the quadrature hybrid after weighting amplifiers, which is a linear process causing less phase distortion at high input power level. The quadrature hybrid based phase interpolation is also robust to the output impedance variation of the weighting amplifiers, resulting in low phase error. Thus, the system level innovation not only provides a phase shifting architecture with low loss and minimal phase interpolation error but also gives high linearity by interpolating phase in a passive way.

The proposed phase shifter has been implemented in designing 90-100 GHz and 120 GHz phased array transmit/receive modules and we achieve the lowest power consumption with high power efficiencies compared to the prior state of the arts at high-end mm-wave infrequences. In measurements, the receiver achieves 23-25 dB gain and 6-9.3 dB NF at 94 GHz. The transmitter can deliver up to 7 dBm saturated output power with 0 dBm maximum power from the phase shifter. A 5-bit phase resolution can be achieved with $< 5^0$ phase error at 92-100 GHz. The two element

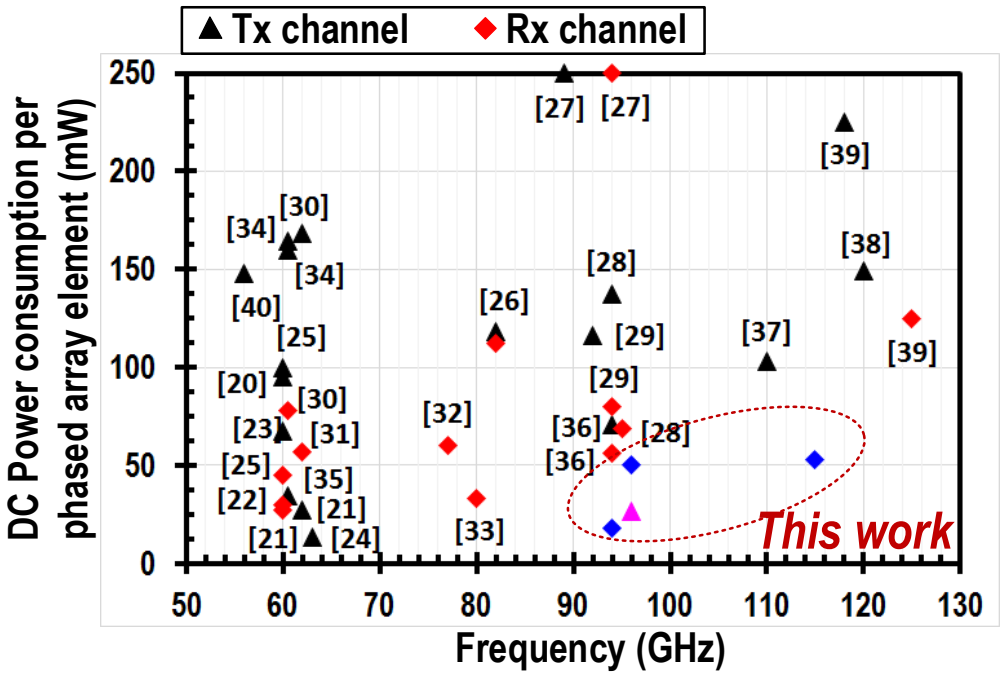


Figure 6.1: Comparison of DC Power consumption per element of phased array front-end with priors works at mm-wave frequencies.

120 GHz phased array shows 15.6 dB peak gain with 53 mW power dissipation at 115 GHz. Fig 6.1 summarizes the contribution of this research in terms of DC power consumption per channel which shows the proposed designs achieve significantly low power consumption compared to prior works. The size of hybrid gets smaller as frequency increases, achieving a low loss and compact phase shifter with a high power efficiency, promising at W-band and beyond.

Finally, the research also proposes a bidirectional phased array transceiver system with replacing back-end lossy switch by a bidirectional variable gain amplifier for further improvement in power efficiencies.

6.2 Future Work

The research has been focused on improving the power efficiencies of phased array single elements. The future of this work is to build a 4×4 array integrated with on-chip antennas. Generally, at mm-wave frequencies, the integration of antenna is done by stacking a glass or quartz substrate with a metal patch on top of the RFIC [18] [37]. The interconnection between antenna and T/R front-end can be done by electromagnetic coupling or by using a glass/quartz through vias (TQV/TSVs). Wilkinson power combiners are used to combine the output power from each array element. The 16-elements of phased array front-ends can be used as a prototype to build larger arrays in the applications for power efficient long-range backhaul links.

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Appendix A

W-band Phased Array Transceiver in 32nm CMOS SOI Process

In chapter 2 and 3, W-band T/R modules have been designed in advanced SiGe process. SiGe BiCMOS technologies are the platform for mixed signal systems and they have shown great potentials for front-end applications while CMOS will remain the backbone of digital logic. In order to enhance the RF performance of CMOS, SOI technology has been emerged where substrate of SOI provides DC and AC isolation, as well as opportunities for further device and circuit innovations. High performance CMOS SOIs can have low noise and low DC power because of low breakdown voltages, while performing high speed digital functions as well. In this chapter, a 94 GHz phased array transceiver system has been designed in 32nm CMOS SOI process. Here, Rx and Tx are integrated with SPDT switches both at back-end and front-end. The phase shifting scheme utilizes 90-degree hybrid coupler based phase interpolator as described in chapter 2, but the architecture has been modified to reduce the loss of the PS.

The 32nm CMOS SOI process has 12 metal stacks with top three thick metal layers and the stacking hight is $\sim 10 \mu m$ (see Fig A.1). The intrinsic device performance without any layout interconnects shows that the floating body RF transistor has f_T and f_{max} of 350 and 500 GHz, respectively. But the distributed R and C effects due to the interconnections of the transistor dom-

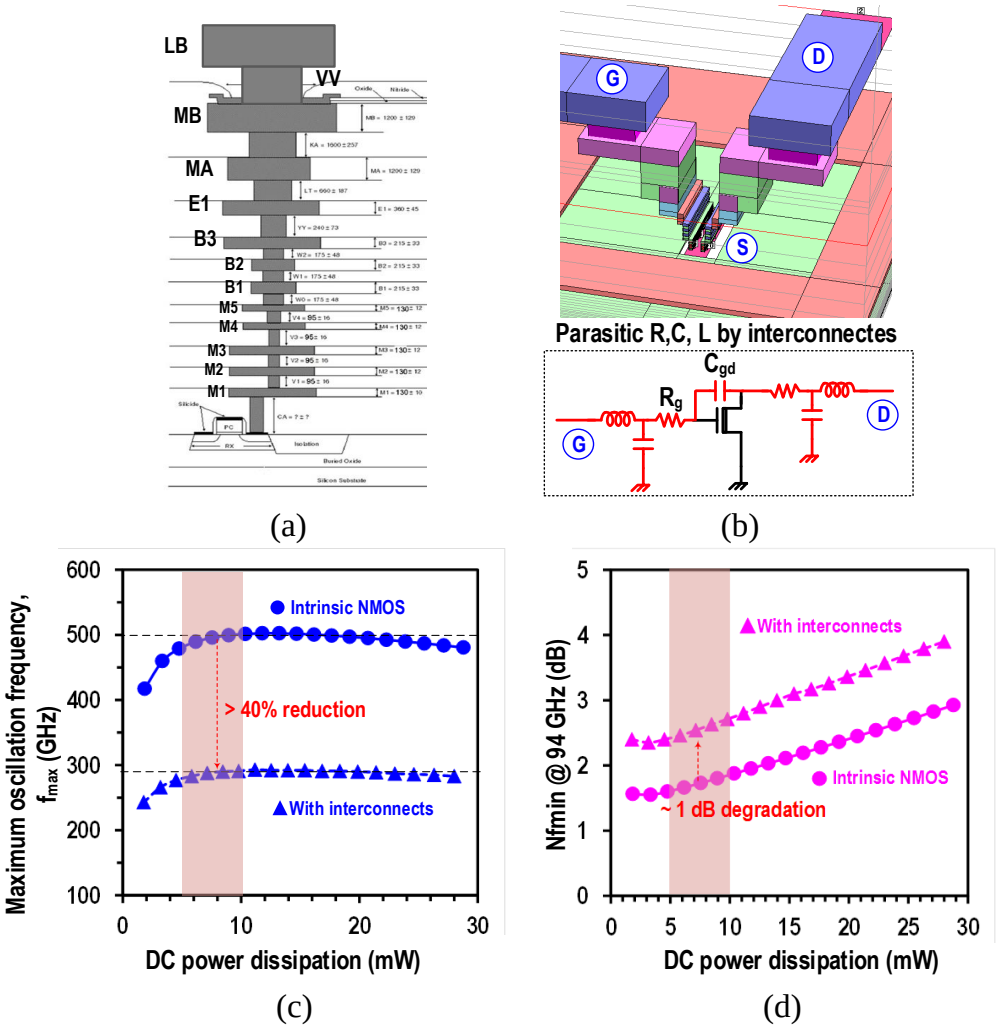


Figure A.1: (a) Metal stack-up of 32nm CMOS SOI process, (b) NMOS transistor interconnections in SONNET with associated parasitics at different node, (c) maximum oscillation frequency f_{max}, and (d) Nfmin at 94 GHz verses DC power dissipation of N-FET in 32nm CMOS SOI process.

inate at W-band frequency. This limits the device speed, f_T and f_{max} significantly. Fig A.1(b) shows the layout interconnects in SONNET upto metal layer M2 and associated parasitics at gate and drain of a NMOS transistor. As f_T and f_{max} are related by the equation: $f_{max} \propto \sqrt{\frac{f_T}{R_g C_{gd}}}$, so degradation of f_{max} causes a proportional decrease in f_T. Fig A.1(c) shows that with interconnections, f_{max} of a NMOS transistor decreases upto 260 GHz which is more than 40% reduction in speed. Similarly minimum noise figure (NFmin) also decreases by 1 dB at 94 GHz when in-

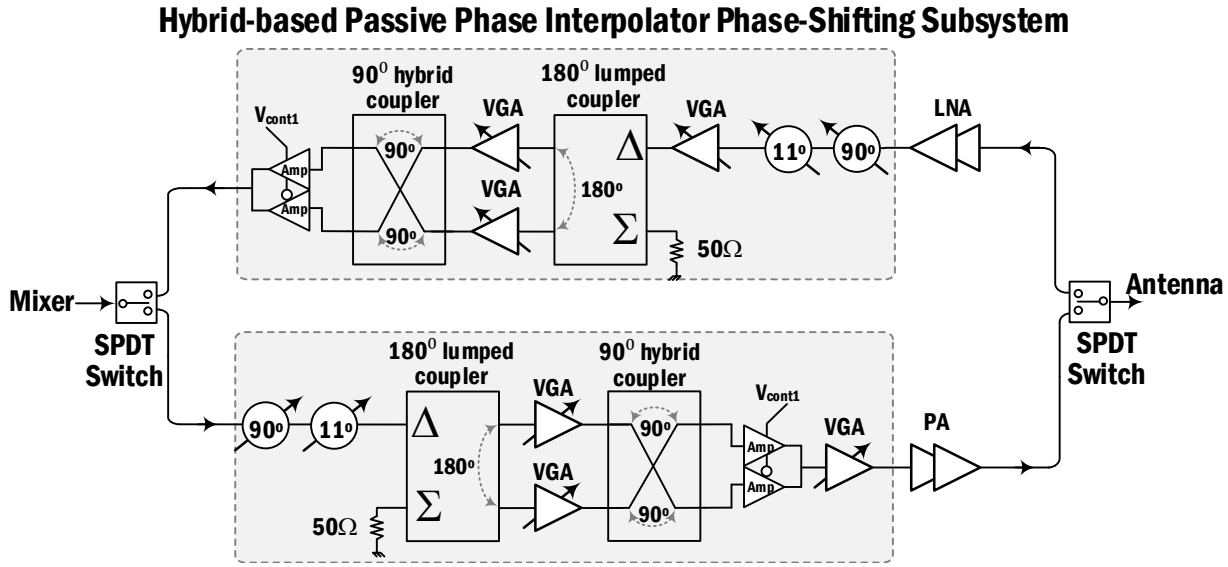


Figure A.2: Block diagram of phased array transceiver utilizing quadrature hybrid based power domain phase interpolator type phase shifter.

cluding the interconnections (see Fig A.1(d)), because NFmin is related with f_T by the equation: $NFmin \propto \frac{f}{f_T}\sqrt{\gamma(\gamma + g_m R_g)}$. The shaded region is of practical interest for low power applications.

A.1 Transceiver Architecture

Fig A.2 shows the transceiver architecture. The phase shifter topology is based on 90-deg hybrid coupler based power domain phase interpolator as described in chapter 3. The 90^0 switched LC type phase shifter is followed by a calibration bit of 11^0 which is also a switched type LC phase shifter. The size of the 11^0-PS is small enough not affect the overall size of the PS significantly. The output of phase interpolating 90-deg hybrid coupler is selected by an active switch. VGAs are needed to control the gain variation and improving the gain of PS. In Rx PS, VGA is used after the discrete switched LC phase shifter in order to suppress noise from them. For Tx PS, VGA is used before PA as a driving amplifier. Standard quarter-wavelength 50Ω T-line based SPDT switches

are used at both front-end and back-end to integrate with antenna and mixer respectively [54].

A.1.1 Design of LNA

Two stage LNAs are used at Rx front-end. The LNA is designed based on cascode topology. Each transistor size is 12μm/40nm and the number of fingers used is 24. Parasitic extraction of transistors are done upto the metal M_1 and EM simulation is done from layer M_2 up to the top metal layer LB. The transistor is biased with 2.8 mA from 1V supply voltage. The noise circle in Fig A.3(b) shows the optimum noise impedance is far from 50Ω impedance at input. The matching is done by a T-matching LC network. A large inductor, L_r of 190pH is used to resonate out the parasitic capacitance at the junction of the cascode transistors which improves the noise and gain by reducing the leakage of signals towards ground through the capacitances. L_r has effect on input impedance of the transistor M_1 as NMOS has poor isolation between gate and drain. The input impedance of M_1, including parasitic extraction and EM effect of interconnections, is 15-j70 Ω as shown in the smith chart in Fig A.3(b). The series inductor at the gate of M_1 including L_r results an impedance of 14-j12Ω which can be matched with 50Ω by a shunt inductor of 50pH. With the T-matching network, a good noise matching can be achieved with NFmin of 3.5 dB. The CG stage is designed for maximum gain and it adds additional 0.5 dB noise in the system. Fig A.3(c) shows the SONNET layout of the LNA. All the matching and bypass capacitors are custom made MOM (metal-oxide-metal) capacitors to have high quality factor. Inductors are designed in top metal layer LB with B1 as ground plane. The simulation result shows the peak gain is 8 dB and NF is 4.3 dB with 2.8mW power dissipation (see Fig A.4).

A.1.2 Switched LC Phase Shifters and Measurement Results

The 90^0 and 11^0 phase shifters are designed in standard topology of NMOS switch based LC low pass network [33]. Fig A.5 shows the schematic of 11^0 phase shifter. For 11^0 phase shifter, the 11^0 delay can be achieved by using a series inductor of 54pH (Fig A.5(a)). The simulation result

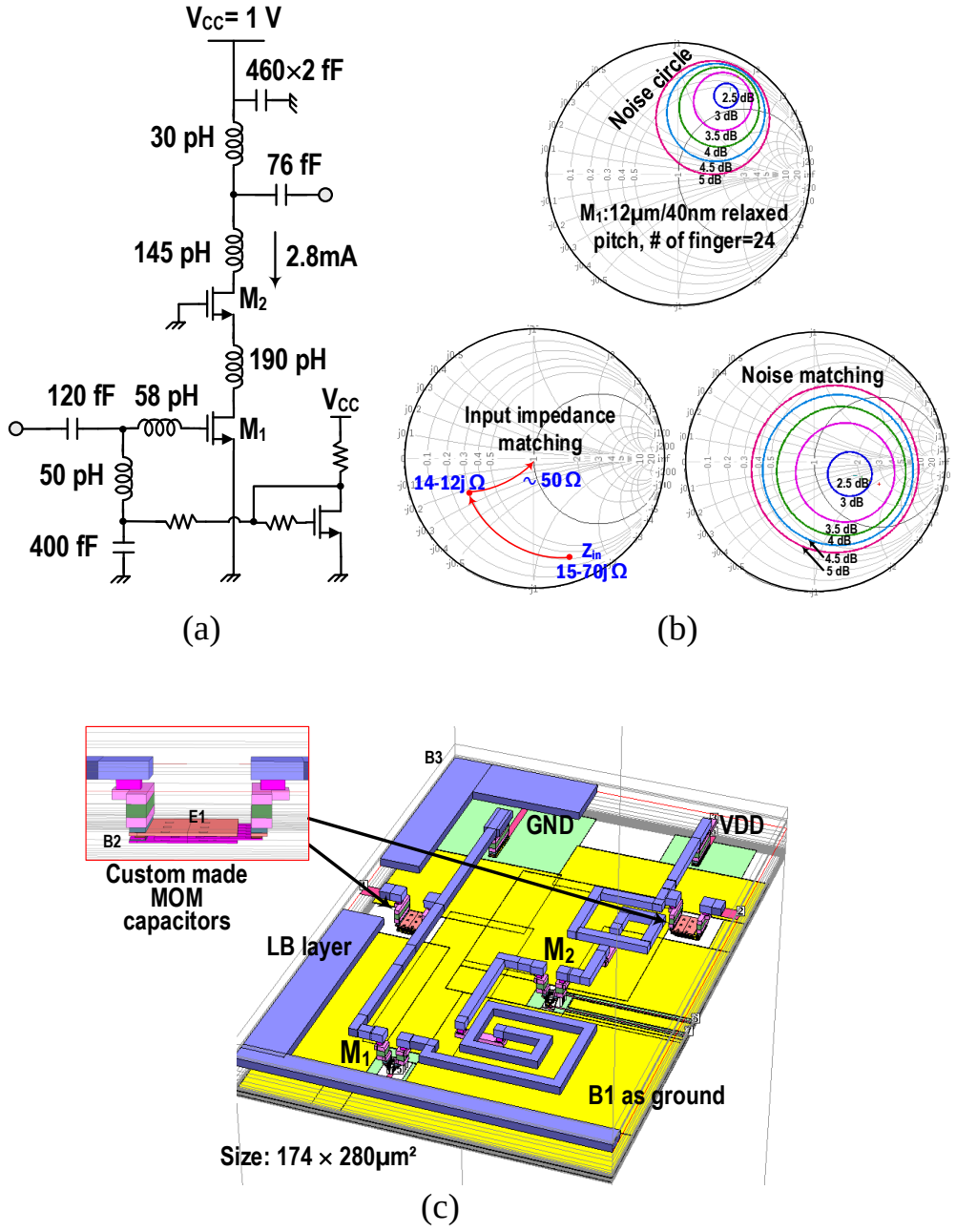


Figure A.3: (a) Schematic of LNA, (b) noise circles and input impedance matching including parasitic extraction + EM interconnection for CS stage of the LNA.

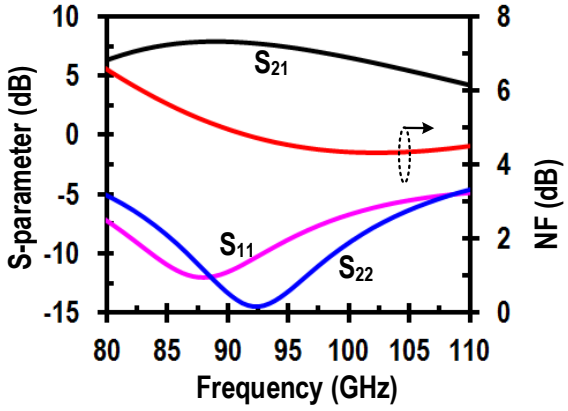


Figure A.4: S-parameter simulation of single stage LNA.

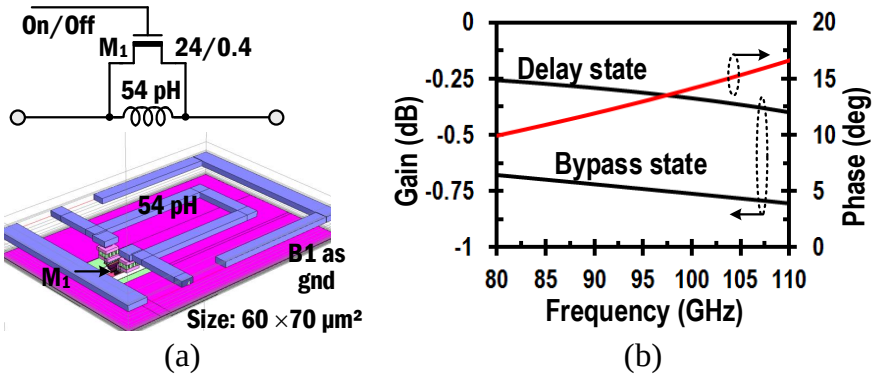


Figure A.5: (a) Schematic and SONNET layout, and (b) S-parameter simulation of 11-deg switched LC phase shifter.

shows maximum loss of the PS is 0.7 dB at bypass state due to the NMOS loss. Fig A.6(a) shows the schematic of 90^0 switched LC phase shifter. A post layout extraction and full EM simulation are done for the whole phase shifter. The width size of M_1/M_2 is optimized as $20\mu m/50\mu m$. The measurement results of 90-deg LC PS are shown in Fig A.7. The phase error remains $< 5^0$ at 85-105 GHz. The loss at bypass and delay states are 3 dB and 5 dB respectively at 94 GHz. The extra loss in delay state is because of the signal leakage through the off-state transistor M_1 when M_2 is ON. The modeling of NMOS parasitic is not accurate enough to predict the behavior at W-band frequency. S_{11} and $S_{22} < -7$ dB at 90-110 GHz.

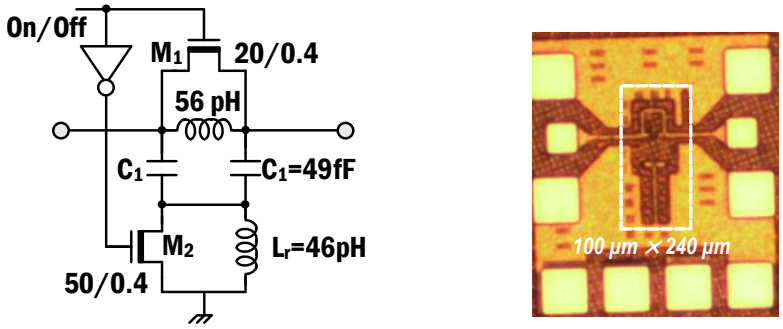


Figure A.6: (a) Schematic and, and (b) chip photo of 90-deg switched LC PS.

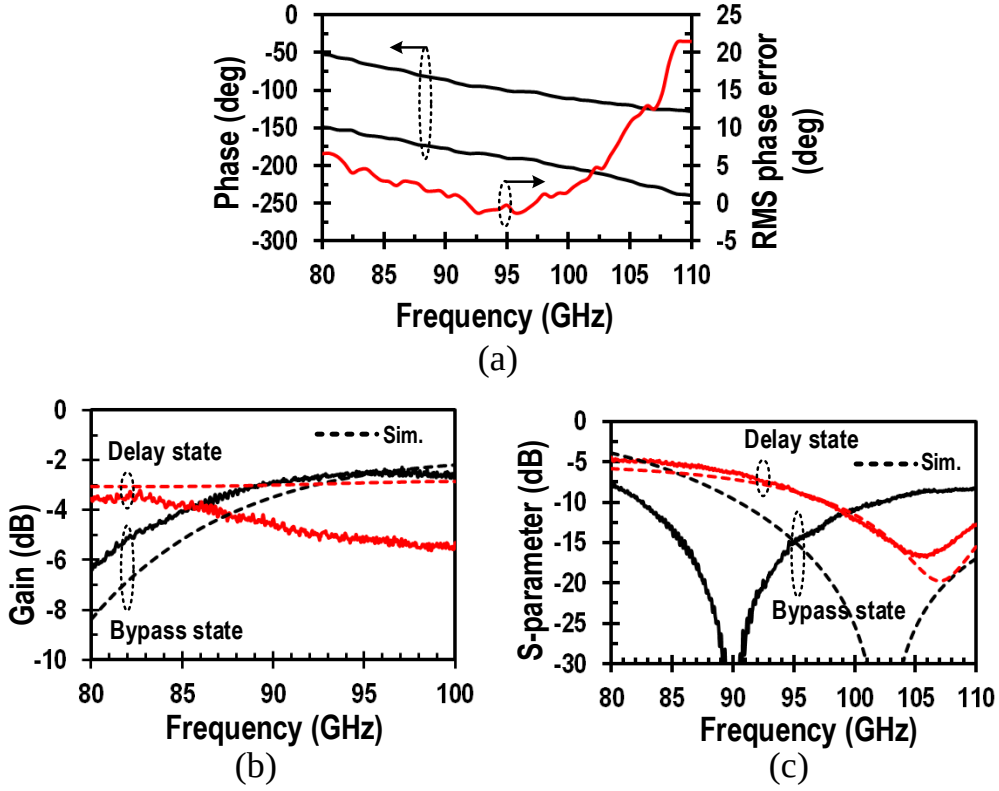


Figure A.7: Measured (a) phase performance, (b) gain and (c) input and output reflection coefficients of 90-deg switched LC PS.

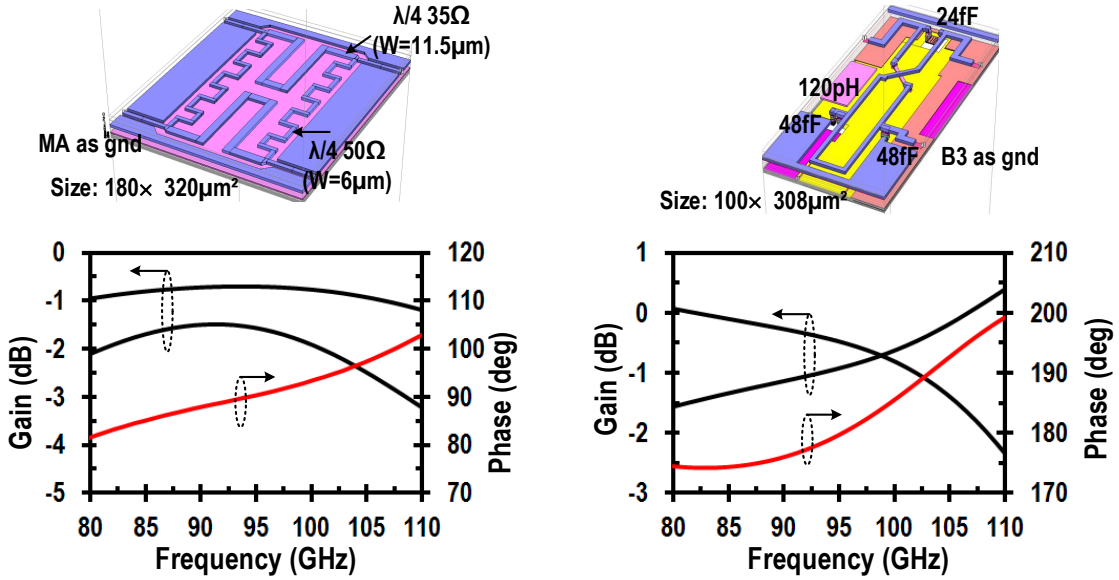


Figure A.8: SONNET layout and S-parameter simulation results of (a) 90-deg hybrid and (b) 180-deg lumped hybrid coupler.

A.1.3 Passive Hybrids

The 90-deg hybrid coupler is based on distributed structure (see Fig A.8(a)). Meandering lines are used in both 50Ω and 35Ω quarter-wavelength lines in order to shrink the area. The top metal layer LB is used on MA as ground plane which gives minimum width for desired characteristics impedances. The overall size of the hybrid is reduced to 180×320 μm^2, which is much smaller than chapter 2 and 3. The simulation shows the loss of the hybrid is maximum 1.5 dB at 94GHz and phase error $< 10^0$ at 80-110 GHz. The lumped 180-deg hybrid structure is shown in Fig A.8(b) which is based on lumped structure where inductors are on LB layer with B3 as ground plane. The simulated loss is $<$ 1 dB at 95 GHz and phase error is $< 5^0$ at 80-100 GHz. The input and output reflection coefficients of both hybrid couplers are below $-$10 dB at 85-100 GHz.

A.1.4 Design of VGA and Measurement Results

The gain error minimizing VGAs have the same topology as LNA. The size of the transistor is $20\mu m$/40nm and is biased with 3.2mA from 1V. The input and output matching components are modified based on different parasitics. The gain of the amplifier is controlled by changing the bias current of M_1. Fig A.9(c) shows the chip size of the VGA. The measurement result shows the gain varies 0-5.6 dB with 5 gain steps. The gain of the phase interpolating VGA goes below -15 dB at minimum gain state where the transistor is operating near cut-off region (multiple of 0^0 or 90^0 phase states). S_{11} and S_{22} are < -5 dB at 85-105 GHz in measurement.

A.1.5 Active Switch

Fig A.10 shows the schematic and simulation results of active switch. The design technique of the switch is the same as discussed in chapter 4. Input and output matching networks are T-type LC networks. The amplifier is deselected by cutting off the bias of M_1 or M_3, by setting V_b equals to 1 or 0 respectively. At off-state of the transistor, the input impedance is very high and it is no longer matched with 50Ω where 50Ω matching is required for minimizing phase error by preceding 90-deg hybrid coupler stage. So NMOS switches (M_{1p} and M_{3p}) are used at inputs of switched amplifiers which are controlled by the bit V_b. At OFF state of M_1 (or M_3), M_{1p} (or M_{3p}) is ON. The ON resistance of M_{1p} combined with 40Ω results nearly 50Ω impedance at input port. At ON state, M_{1p} is OFF so it can be ignored due to its high drain impedance, and the matching network operates in normal operation. The layout parasitics of M_{1p} (or M_{3p}) must be included in designing matching networks. The simulated S-parameters of the active switch shows the peak gain is 4.5 dB and input and output reflection coefficients are < -5 dB at 85-100 GHz when V_b = 1. The similar performance is achieved when V_b = 0.

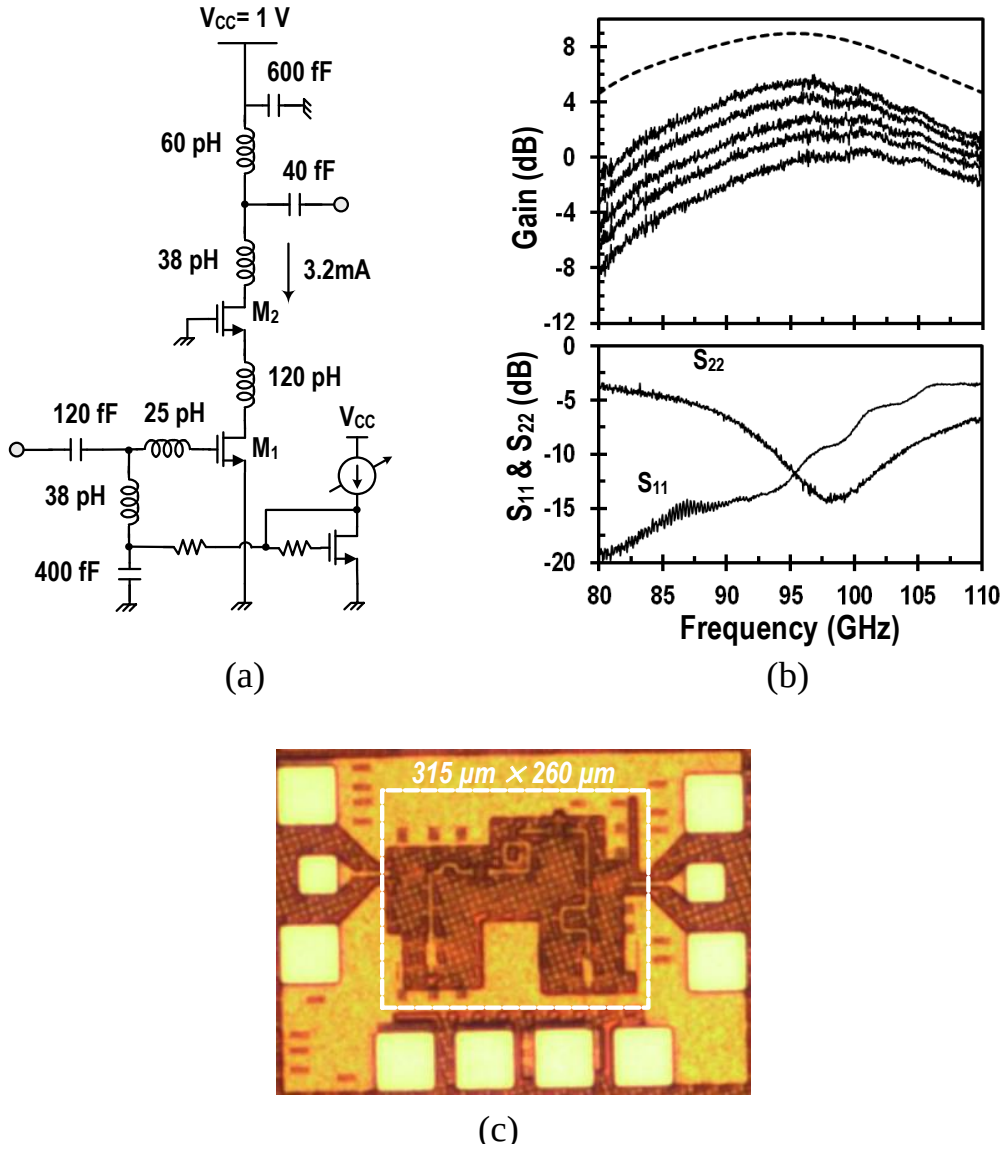


Figure A.9: (a) Schematic , (b) measured S-parameter results and (c) chip photo of VGA.

A.2 Simulation Results of T/R Modules

Fig A.11 and A.12 shows the simulation results of Rx channel and Tx phase shifter. The peak gain of the Rx channel is 24-27 dB and NF is 5 dB. The phase resolution can be >6bit. The input 1-dB compression point is −33 dBm. The total power consumption is 17 mW. The Rx chip size is 1450×380 μm^2 without I/O pads. The Tx phase shifter simulation shows the peak gain ranges 7-

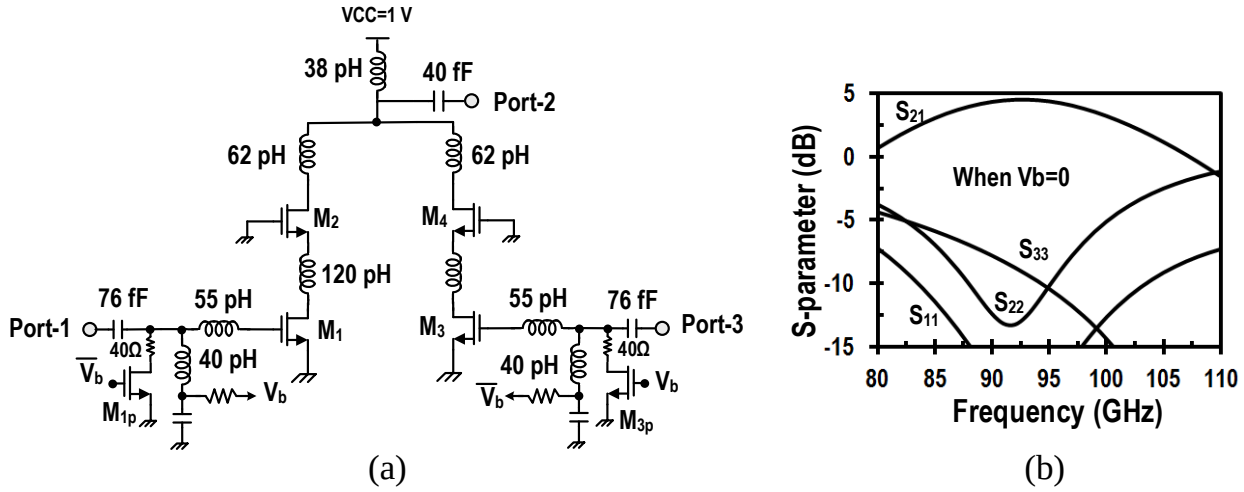


Figure A.10: (a) Schematic , (b) simulated S-parameter results of the active switch when M1 and M2 are ON, M3 and M4 are OFF (V_b=1 state).

12 dB and the phase resolution can be also >6-bit. The variation in S_{11} is because of the variation of impedance in 90^0 PS at bypass and delay states. The input and output 1-dB compression point of Tx PS is -16.5 dBm and -5.6 dBm, respectively at maximum gain state. The power consumption is 11.4 mW from 1V supply. The Tx PS chip size is 1140×360 μm^2 without I/O pads. The chip is under measurement. Fig A.13 shows the layout of Rx channel and Tx Ps.

A.3 Conclusion

This work demonstrates a 94 GHz T/R module for phased array application in 32nm CMOS SOI process. The phase shifting architecture utilizes our prior proposed phase interpolator with more flexibility in phase calibration, resulting in high phase resolution ($>$ 6 bit). The loss of the phase shifter can be much lower than $0.13\mu m$ SiGe process as the NMOS switch loss in CMOS SOIs is much smaller, thus a low power and highly efficient transceiver system can be obtained at W-band which can be easily integrated with fast digital base-band system designed in 32nm CMOS process.

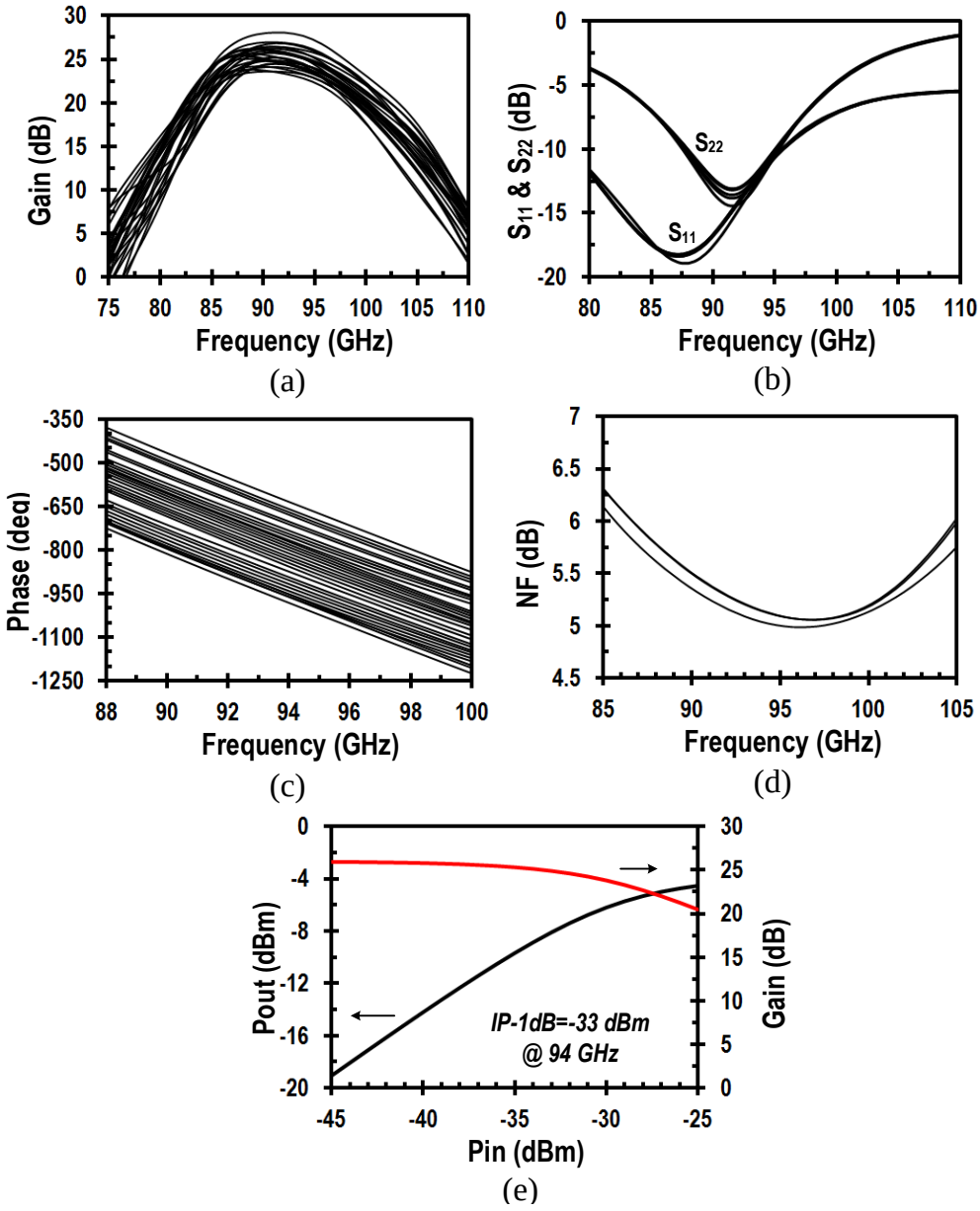


Figure A.11: Simulated (a) gain, (b) input S_{11} and output S_{22} reflection coefficients, (c) phase response of >5-bit phase resolution, (d) NF and (e) linearity response at average gain state of the single channel receiver.

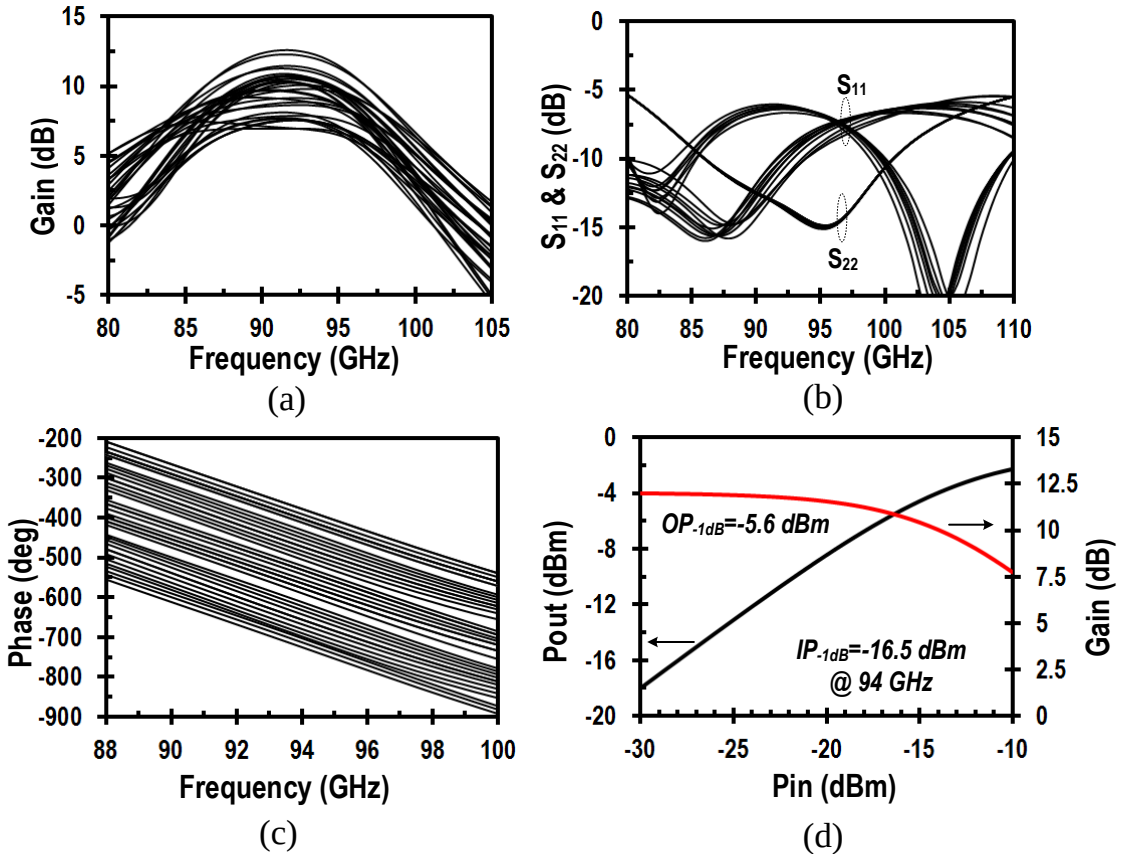
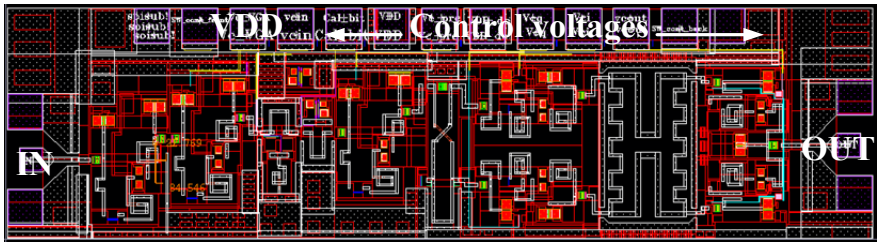
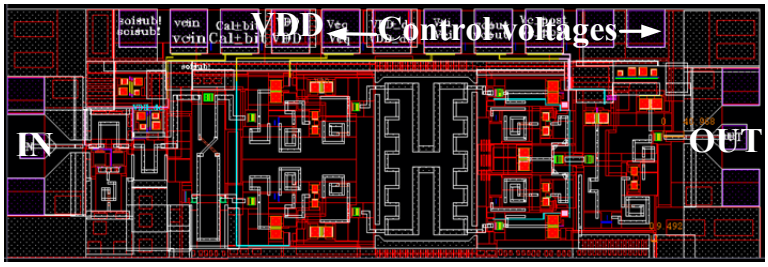


Figure A.12: Simulated (a) gain, (b) input S_{11} and output S_{22} reflection coefficients, (c) phase response of >5-bit phase resolution and (d) linearity response at highest gain state of the transmitter phase shifter.



(a)



(b)

Figure A.13: Layouts of (a) receiver channel, and (b) transmitter phase shifter.