THE DEVELOPMENT OF A SPICE2 MODEL FOR
TRANSIENT SIMULATION OF THE SCHOTTKY TRANSISTOR

by

Darryl W. Royster

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APPROVED:

Dr. A. A. R. Riad, Chairman

Dr. S. M. Riad  Dr. W. A. Davis

Dr. C. W. Bostian

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(ABSTRACT)

In order to simulate the Schottky Transistor and its effect on circuit applications, a computer model has been developed for the device. The focus of this research is the development of such a model for SPICE2 (a circuit simulation computer program) using a new method for model construction.

This new method develops a model by approximating the mathematics of the simulation via perturbations and iterations. The model developed by the new method yields a minimum simulation accuracy of 65% in a variety of circuit applications. In comparison, a model developed by the conventional method, which uses measured data to complete the physical constructs of the SPICE2 model, offers the same margin of accuracy for the same circuits. So the new method is just as effective as the old method for the circuits that were tested.

Yet with further development, the new method for model construction can be automated eliminating the time consuming and possibly inaccurate measurements of the old method that
would discourage the use of SPICE2. So this research, in addition to developing two successful SPICE2 models for the Schottky Transistor, also introduces a new method for model construction that can make SPICE2 easier to use.
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Chapter I

INTRODUCTION

The Schottky Transistor has many applications where high-speed digital switching is desired. The effects the Schottky Transistor has on a circuit's performance can be illustrated by computer simulation in the time domain. But computer simulation requires an accurate model of the device. Thus the focus of this research is the development of a computer model for the Schottky Transistor.

Because of its general capabilities and speed, SPICE2 is chosen to be the computer package for simulating the Schottky Transistor. The device is modeled in two parts, the Bipolar Junction Transistor (BJT) component and the Schottky Barrier Diode (SBD) component. Chapter II examines the ability for SPICE2 to model these two components. The focus of the research then emphasizes the determination of values for the user selected parameters used in both models.

The first component, the BJT, is modeled as described in Chapter III. By first examining the physical mechanisms of the digital switch, the response times are defined. The response times are used to compare the simulation results to the experimental measurements on a sample of BJT's. The user selected parameters for the model are then determined using a new experimental method. This new method, called
the Transfer Function Method, which iteratively determines parameter values necessary to obtain a desired set of response times. To verify the effectiveness of this new method, the conventional Physical Measurements Method is used to also develop a BJT model. This method determined parameter values from laboratory measurements of BJT characteristics such as I-V and C-V curves as described by Getreu [1]. The simulation results from the two models are then compared to assess the two methods.

The second component of the Schottky Transistor, the SBD, is modeled in Chapter IV. By understanding the distinctions between the SBD and the normal p-n junction diodes, the SBD is easily represented by the SPICE2 Diode model. So the determination of the parameter values for this model does not require either of the two modeling methods used for the BJT model.

In Chapter V, all three models (which comprise two Schottky Transistor models) are used to simulate various switching circuits. The simulation results are compared to the actual measured response times obtaining a minimum of 65% accuracy for both Schottky Transistor models. Accuracy greater than 75% cannot be expected due to various limitations. But since both Schottky Transistor models behave similarly, the new Transfer Function Method shows positive signs for modeling effectiveness and accuracy.
Chapter VI summarizes the research work by further comparing the Transfer Function Method to the Physical Measurements Method. Also, ideas for further research with the Transfer Function Method are suggested. With automation, the Transfer Function Method can replace the conventional Physical Measurements Method and thus simplify the use of SPICE2.
Chapter II

*SPICE2: THE TOOL FOR SIMULATION*

2.1 Introduction

The ability to anticipate a circuit's performance greatly assists the design engineer. But when many linear and nonlinear components add to the complexity of the network, an exact solution is usually impractical and hard to find. For such cases, iterative solutions are used. But because of the large number of calculations necessary (particularly for a transient solution), computers are used to simulate the circuits.

Computer simulation offers several advantages [1]. Computer simulation of prototype circuits can replace experimental "breadboard" versions. Simulated prototypes are not plagued by stray capacitance offered by the circuit board. Simulated prototypes can be monitored without requiring loading effects. Worstcase and sensitivity analyses can easily be performed on simulated prototypes. So circuit simulation simplifies design engineering.

Because of the generality of electronic components, various circuit simulation algorithms have been developed. These algorithms require the type of component, its location in the network, and certain parameter values as input.
Depending on what the user determines for output, various types of analyses are performed. These algorithms greatly speed up the simulation process because the user needs simply to enter the three types of input for each circuit and does not determine manually the iterative procedures for analyzing the networks with computers.

Several circuit simulation algorithms have been developed. Some of these algorithms are CANCER, TCAP, SEPTER, SUPER SEPTER, and SPICE. SPICE is one of the most popular algorithms because of its trade off between general capabilities for high computational speed for transient analysis [2]. Linear components such as resistors, capacitors, and inductors are readily incorporated by property values. For example, to include a source resistance, $R_s$ of 50Ω between circuit nodes labeled 1 and 2, the SPICE entry would be:

```
RS 1 2 50
```

Nonlinear components such as diodes and transistors are modeled by various parameters. If a diode labeled D1 were between nodes 1 and 2 (2 being the cathode), the SPICE entry would be:

```
D1 1 2 DIODE_MODEL_01
.MODELL DIODE_MODEL_01 D (Parameter List)
```
For more examples, look in any of the appendixes for a SPICE source file.

The accuracy of the nonlinear models depends on the method of selecting values for these parameters. The equations governing the nonlinear models vary slightly with different editions of SPICE. SPICE2, a particular edition of SPICE, is chosen to simulate the Schottky Transistor because of its popularity and availability on many computer facilities.

This chapter examines SPICE2 for its ability to simulate the Schottky Transistor in the time domain. This task is achieved by considering the Schottky Transistor's two main components which are the Bipolar Junction Transistor (BJT) and the Schottky Barrier Diode (SBD). Section 2.2 examines the SPICE2 BJT model, and Section 2.3 examines the SPICE2 Diode model. Section 2.4 concludes the chapter. The section examines what is required from the user to model the Schottky Transistor with SPICE2.

2.2 SPICE2 BJT Model

BJT switching for digital applications has been studied using the Ebers-Moll model [3]. By including the emitter-base and the collector-base junction capacitances, the four
response times due to transient switching can be calculated [4]. Thus the SPICE2 BJT model must stem from the Ebers-Moll model with junction capacitances included in order to achieve an accurate model. As shown in Figure 2.1, the SPICE2 BJT model is derived from the Ebers-Moll model [1]. Figure 2.1a shows the Ebers-Moll model [5]. This model consists of two p-n junction diodes back-to-back (labeled $D_{1a}$ and $D_{2a}$) and two current sources (labeled $CS_{1a}$ and $CS_{2a}$). The equations for these four components are of the form

\begin{align}
I_{D_{1a}} &= I_{CS}\left[\exp\left(\frac{V_{bc}}{V_t}\right) - 1\right] \\
I_{D_{2a}} &= I_{ES}\left[\exp\left(\frac{V_{be}}{V_t}\right) - 1\right] \\
I_{CS_{1a}} &= \alpha_f \cdot I_{ES}\left[\exp\left(\frac{V_{be}}{V_t}\right) - 1\right] \\
I_{CS_{2a}} &= \alpha_r \cdot I_{CS}\left[\exp\left(\frac{V_{bc}}{V_t}\right) - 1\right]
\end{align}

where $V_t = K \cdot T/q$, $I_{CS}$ and $I_{ES}$ are the saturation current values for the two diodes, and $\alpha_f$ and $\alpha_r$ represent the forward and reverse current gain ratios, respectively. $V_{bc}$ and $V_{be}$ are the voltages between the base-collector and the base-emitter junctions, respectively. Equations 2.1 formulate the collector current, $I_c$, and the emitter
Figure 2.1 The Development of the SPICE2 BJT Model. (a) The Ebers-Moll Model, (b) An Intermediate Step, and (c) The SPICE2 Representation.
current, $I_e$, as

$$I_c = \alpha_f \cdot I_{ES} \left[ \exp \left( \frac{V_{be}}{V_t} \right) - 1 \right] - \alpha_r \cdot I_{CS} \left[ \exp \left( \frac{V_{bc}}{V_t} \right) - 1 \right]$$

(2.2a)

$$I_e = -I_{ES} \exp \left( \frac{V_{be}}{V_t} \right) + \alpha_r \cdot I_{CS} \left[ \exp \left( \frac{V_{bc}}{V_t} \right) - 1 \right].$$

(2.2b)

By the reciprocity relations, $\alpha_f \cdot I_{ES} = \alpha_r \cdot I_{CS}$ [5]. If $\alpha_f \cdot I_{ES}$ is renamed as $IS$, Equation 2.1 is rewritten as

$$I_{D_{1a}} = \frac{IS}{\alpha_r} \exp \left( \frac{V_{bc}}{V_t} \right) - 1$$

(2.3a)

$$I_{D_{2a}} = \frac{IS}{\alpha_f} \exp \left( \frac{V_{be}}{V_t} \right) - 1$$

(2.3b)

$$I_{CS_{1a}} = IS \exp \left( \frac{V_{be}}{V_t} \right) - 1$$

(2.3c)

$$I_{CS_{2a}} = IS \exp \left( \frac{V_{bc}}{V_t} \right) - 1$$

(2.3d)

Figure 2.1b shows the two previous current sources, $CS_{1a}$ and $CS_{2a}$, combined to form the source $CS_{3b}$. This current represents the flow from the collector, through $CS_{1a}$, $D_{2a}$, and to the emitter with the reverse current feeding back through $CS_{2a}$. Therefore,
\[ I_{CS3b} = I_{CS1a} - I_{CS2a} = IS[\exp\left(\frac{V_{bc}}{V_t}\right) - \exp\left(\frac{V_{bc}}{V_t}\right)]. \]  

\[ (2.4) \]

For \( I_c \) and \( I_e \) to remain correct, \( D_{1a} \) and \( D_{2a} \) must be modified to compensate for the new \( CS_{3b} \). \( D_{1a} \) and \( D_{2a} \) are replaced by \( CS_{1b} \) and \( CS_{2b} \) and are expressed as

\[ I_{CS1b} = \frac{IS}{\alpha_r}\exp\left(\frac{V_{bc}}{V_t}\right) - 1 \quad \text{and} \quad I_{CS2b} = \frac{IS}{\alpha_f}\exp\left(\frac{V_{be}}{V_t}\right) - 1 \]  

\[ (2.5a) \]

\[ (2.5b) \]

Since \( \frac{1}{\beta} = \frac{1}{\alpha} - 1 \), Equation 2.5 can be rewritten as

\[ I_{CS1b} = \frac{IS}{\beta_r}\exp\left(\frac{V_{bc}}{V_t}\right) - 1 \]  

\[ (2.6a) \]

\[ I_{CS2b} = \frac{IS}{\beta_f}\exp\left(\frac{V_{be}}{V_t}\right) - 1 \]  

\[ (2.6b) \]

The last step of the derivation sums \( CS_{1b} \) and \( CS_{2b} \) to form \( CS_{1c} \) as shown in Figure 2.1c. This term is also the base current, \( I_b \). To compensate for this modification, \( CS_{3b} \) is changed to \( CS_{2c} \) which is also \( I_c \). The new expressions are of the form
The expressions of Equation 2.7 are used in the SPICE2 BJT model.

The basic configuration of Figure 2.1c is further developed to include more components as shown in Figure 2.2 [6]. The ohmic resistances due to the terminal contacts are represented by RB, RC, and RE. The DC characteristics of the intrinsic BJT are represented by the current sources Ib and Ic. Collector-substrate capacitance for the integrated BJT is represented by CCS. Stored base charge in the depletion region and charge-storage from minority carrier diffusion are represented by the junction capacitances Cbe and Cbc, respectively.

The nonlinear equations which govern the current sources and the junction capacitances in the SPICE2 BJT model are

\[
I_{CS_{1c}} = I_b = \frac{I_S}{\beta_f} \left( \exp \left( \frac{V_{be}}{V_T} \right) - 1 \right) + \frac{I_S}{\beta_r} \left( \exp \left( \frac{V_{bc}}{V_T} \right) - 1 \right)
\]

\[
I_{CS_{2c}} = I_c = I_S \left( \exp \left( \frac{V_{be}}{V_T} \right) - \exp \left( \frac{V_{bc}}{V_T} \right) \right) - \frac{I_S}{\beta_r} \left( \exp \left( \frac{V_{bc}}{V_T} \right) - 1 \right)
\]
Figure 2.2 The SPICE2 BJT Model.
\[ I_c = IS\exp\left(\frac{V_{b'e'}}{V_t}\right) - \exp\left(\frac{V_{b'c'}}{V_t}\right) - \frac{IS}{BR}\exp\left(\frac{V_{b'c'}}{V_t}\right) - 1 \]  
\[ (2.8a) \]

\[ I_b = \frac{IS}{BF}\exp\left(\frac{V_{b'e'}}{V_t}\right) - 1 + \frac{IS}{BR}\exp\left(\frac{V_{b'c'}}{V_t}\right) - 1 \]  
\[ (2.8b) \]

\[ C_{be} = \frac{TF\cdot IS}{V_t}\exp\left(\frac{V_{b'e'}}{V_t}\right) + CJE\left[1 - \frac{V_{b'e'}}{PE}\right]^{-ME} \]  
\[ (2.8c) \]

\[ C_{bc} = \frac{TR\cdot IS}{V_t}\exp\left(\frac{V_{b'c'}}{V_t}\right) + CJC\left[1 - \frac{V_{b'c'}}{PC}\right]^{-MC}. \]  
\[ (2.8d) \]

The user must determine numerical values for the 16 parameters included in Equations 2.8. The physical significance of these parameters as determined by Getreu [1] is as follows: BF is the forward current gain; BR is the reverse current gain. RB, RC, and RE represent the ohmic resistances due to the terminal contacts. CCS is the collector-substrate capacitance present in BJT's in integrated circuits. TF is the total forward transit time, and TR is the total reverse transit time. CJE is the emitter-base junction capacitance when the voltage across this junction is zero. Similarly, CJC is the collector-base junction capacitance at zero junction voltage. IS is the saturation current. PE is the emitter-base barrier potential, and PC is the collector-base barrier potential. EG is the energy gap of the semiconductor material used to
adjust IS for temperature variations using the relation,

\[
    IS(T) = IS(T_{nom}) \cdot \left[\frac{T}{T_{nom}}\right]^3 \cdot \exp\left\{\frac{-EG}{K} \left(\frac{1}{T} - \frac{1}{T_{nom}}\right)\right\}
\]  

(2.9)

where \( T \) is the simulation temperature in degree Kelvin, \( T_{nom} \) is the measurement temperature in degree Kelvin, and EG is in eV. Finally, ME and MC are the capacitance gradient factors for the emitter-base and the collector-base junctions, respectively.

The expressions for \( I_c \) and \( I_b \) in Equations 2.8 are derived from the basic Ebers-Moll relationships for two current sources and two diodes [1]. Both junction capacitance expressions, \( C_{be} \) and \( C_{bc} \), contain two components. The first component represents the diffusion capacitance which is proportional to the current through the particular junction. This component stems from the minority carriers and dominates when the junction is forward biased. The second component represents the depletion capacitance significant only when the junction is reversed biased.

Thus the SPICE2 BJT model represents the two current sources of the Ebers-Moll model and the emitter-base and the collector-base junction capacitances with nonlinear equations. These equations contain 16 user selected parameters which are BF, BR, RB, RC, RE, CCS, TF, TR, CJE,
CJC, IS, PE, PC, EG, ME, and MC. As will be shown in Chapter III, these 16 parameters of Equations 2.8 will enable SPICE2 to simulate the BJT used in a particular Schottky Transistor application. Yet since the Schottky Transistor also contains a SBD, the SPICE2 Diode model must also be examined. This is done next in Section 2.3.

2.3 *SPICE2 Diode Model*

The SPICE2 Diode model is capable also of modeling the SBD. Like the BJT model, the SPICE2 Diode model uses nonlinear equations to represent the diode current and the diode junction capacitance. These equations contain user selected parameters allowing a wide variety of diodes to be modeled.

The I-V characteristics of the SBD follow the basic diode equation [7]. Also, as explained in Chapter IV, the depletion capacitance considered at an applied reverse bias is similar to that of ordinary diodes. The major difference between the SBD and the p-n junction diode is the lack of the diffusion capacitance in a forward biased SBD.

SPICE2 incorporates a general p-n junction diode (Figure 2.3) [6]. The nonlinear current source, $I_d'$, models the DC characteristics of the diode as a function of the junction voltage. Charge-storage in the depletion region
Figure 2.3 The SPICE2 Diode Model.
due to the minority carrier diffusion is represented by $C_d$. Ohmic resistance due to the terminal contacts is represented by $R_S$. The nonlinear equations for the current source, $I_d$, and the capacitance, $C_d$, are

$$I_d = IS\{\exp\left(\frac{V_d}{N\cdot V_t}\right) - 1\}$$

(2.10a)

$$C_d = \frac{TT\cdot IS}{N\cdot V_t}\exp\left(\frac{V_d}{N\cdot V_t}\right) + CJ0[1 - \frac{V_d}{PB}]^{-M}.$$  

(2.10b)

Equations 2.10 offer 8 parameters for user selection. $R_S$ models the ohmic resistance of the terminal contacts. TT is the total transit time. $C_{JO}$ is the junction capacitance at zero junction voltage. $I_S$ is the saturation current. $P_B$ is the barrier potential of the junction. $E_G$ is the energy gap of the semiconductor material affecting $I_S$ as described previously in Equation 2.9. $M$ is the capacitance gradient factor for the junction. $N$ is called the "ideality factor" which allows for deviations in behavior from the ideal diode equation [8]. As will be shown in Chapter IV, Equations 2.10 can be used to model the SBD if TT is set to zero and M to 0.5 [8].

So the SPICE2 Diode model can be used to represent the SBD. This task can be achieved by offering 8 user selected
parameters, RS, TT, CJO, IS, PB, EG, M, and N. Because a SBD is being modeled, the values for two of the parameters are already known leaving only six parameter values to be determined. This task is the purpose of Chapter IV.

2.4 Summary

The models offered by SPICE2 can be used to represent the Schottky Transistor if proper parameter values are selected. The 16 parameters for the SPICE2 BJT model are BF, BR, RB, RC, RE, CCS, TF, TR, CJE, CJC, IS, PE, PC, EG, ME, and MC. For the SPICE2 Diode model the 8 parameters are RS, TT, CJO, IS, PB, EG, M, and N. Note that the saturation current, IS, and the energy gap, EG, may have different numerical values for the two SPICE2 models.

The accuracy of the models depends on the accuracy of the values selected for those parameters. Since the BJT model is the most significant component of the Schottky Transistor, greater care is spent determining the 16 parameters for that model. Procedures for that process are described next in Chapter III. The 8 parameters for the Schottky Barrier Diode model are selected in Chapter IV. But even though SPICE2 does not offer a direct model for the Schottky Transistor, determination of the necessary 24 parameter values allows SPICE2 to be used as the tool for
computer simulation.
Chapter III

DEVELOPMENT OF A BIPOLAR JUNCTION TRANSISTOR MODEL

3.1 Introduction

In this chapter, the Bipolar Junction Transistor (BJT), the first nonlinear component of the Schottky Transistor, is modeled for SPICE2 simulation. The development of this model starts with the examination of the physics of the BJT used as a digital switch (Section 3.2). This general understanding is used to measure the physical data (Section 3.3) in order to determine the SPICE2 parameters for its BJT model (Section 3.4). The parameters are determined using two methods. The chapter concludes with Section 3.5 by comparing the accuracy of the two methods in providing models to simulate the switching response times.

3.2 Review of the Physics of the BJT Switch

A successful model for transient simulations is defined as one whose simulated response times \( (t_d, t_r, t_s, \text{ and } t_f) \) agree with those measured in an actual constructed circuit. Therefore, these response times must be clearly defined and understood in order to assess any model's credibility. This section reviews the definitions of the response times and
examines their governing physics for the BJT.

The response times are shown in Figure 3.1 for a Single-Stage Inverter circuit [4]. By applying a voltage pulse varying between the levels $V_2$ and $V_1$, the response times can be measured from the output current, $I_c$, or the output voltage, $V_{out}$.

With the input at $V_2$, the output current, $I_c$, is zero, and the output voltage, $V_{out}$, is at $V_{cc}$. Once the input rises to $V_1$, the output begins to change with $I_c$ and eventually reaches the saturation current value, $I_{cs}$ (approximately $V_{cc}$ divided by $R_c$), and $V_{out}$ reaches $V_{sat}$ (about 0.2 v). The Delay Time, $t_d$, is measured when an output variable reaches 10% of its final value. This time, $t_d$, is determined by measuring the time at which $I_c = 0.1 \cdot I_{cs}$ or when $V_{out} = 0.9(V_{cc} - V_{sat})$. The Rise Time, $t_r$, measures the transition time from the 10% mark to the 90% mark. Thus the time, $t_r$, is determined by measuring the interval between the time when either $I_c = 0.9 \cdot I_{cs}$ or $V_{out} = 0.1(V_{cc} - V_{sat})$ and the time of the previous 10% mark.

Similarly, when the input voltage falls back to $V_2$, the output current, $I_c$, eventually returns to zero and the output voltage, $V_{out}$, to $V_{cc}$. The Storage Time, $t_s$, is the delay time between the instant the input switches back and either $I_c = 0.9 \cdot I_{cs}$ or when $V_{out} = 0.1(V_{cc} - V_{sat})$. Finally, the Fall Time, $t_f$, is measured from the time of the
Figure 3.1 Input and Output Waveforms of the Single-Stage Inverter Circuit Showing (a) The Circuit, (b) The Input Voltage, (c) The Output Current, and (d) The Output Voltage.
90% mark to the time when \( I_c = 0.1 \cdot I_{cs} \) or when \( V_{out} = 0.9(V_{cc} - V_{sat}) \). So by monitoring the input voltage and either the output current or the output voltage, the four response times can be measured for any circuit. Next, the factors effecting these four response times are examined.

The Delay Time, \( t_d \), allows the BJT to move from the cutoff region to the active region. This transition requires three distinct processes [4]. First, the junction and the diffusion capacitances are charged to the cut-in voltage. Second, the minority carriers cross the base region. Third, the collector current rises from 0 to 10% of the saturation current value. These three effects are more carefully examined below as they apply to the test circuit shown in Figure 3.1.

The first component of the Delay Time, \( t_{d_1} \), is the time necessary for charge build-up to bring \( V_{b'e} \) to the cut-in value which is 0.5 V for silicon. Since the BJT is in cutoff during this time, the cutoff model shown in Figure 3.2 is used to analyze the response. This model is a hybrid-pi model with the normal current source short-circuited. Because \( r_{\pi} \) is inversely proportional to emitter current, it is assumed to be very large. The base-spreading resistance is represented by \( r_{X} \). A typical value of \( r_{X} \) is of the order of 200Ω. Because the emitter diffusion capacitance is neglected due to zero emitter current, \( C_{\pi} \)
Figure 3.2 The Cutoff Model for the BJT Used to Calculate $t_{dl}$.
simply represents the common base input transition capacitance which is about 8 pF. Similarly, $C_\mu$ represents the collector transition capacitance which is about 4 pF.

As the input voltage, $V_{in}$, rises from $V_2$ to $V_1$, $C_\pi$ and $C_\mu$ are charged exponentially. Solving the exponential relationships for voltage $V_{b'e}$ shown in Figure 3.2, one can get

$$V_{b'e} = [V_2 - V_1] \exp\left\{\frac{-t}{R' \cdot C'}\right\} + V_1$$

(3.1)

where $R' = r_x + R_s$, the source resistance of the circuit, and $C' = C_\pi + C_\mu$. Once $V_{b'e}$ rises to the value of the cut-in voltage, $V_t$, the model of Figure 3.2 is no longer valid as the transistor begins to turn on. Solving Equation 3.1 for $V_{b'e} = V_t$, $t_{d_1}$ takes the form

$$t_{d_1} = R' \cdot C' \ln\left\{\frac{V_1 - V_2}{V_1 - V_t}\right\}.$$  

(3.2)

Once $V_{b'e} = V_t$, the BJT enters the active region. Minority carriers begin to cross the base. The time it takes the electrons to cross the base constitutes the second component of the Delay Time, $t_{d_2}$. This time can be approximated by
where \( \omega_T \) is the transition frequency of the BJT [4].

When the minority carriers reach the collector junction, the collector current, \( I_C \), begins to increase from zero value. \( I_C \) also increases exponentially until the BJT saturates. The third component of the Delay Time, \( t_{d3} \), ends when \( I_C \) reaches 10% of the saturation current value, \( I_{cs} \). Using the model shown in Figure 3.3, \( I_C \) is given by

\[
I_c(t) = h_{FE} \cdot I_{b1} \left[ 1 - \exp\left(\frac{-t}{T_r}\right)\right]
\]

(3.4)

where \( I_{b1} = (V_1 - V_t)/(R_s + r_x) \), \( T_r = h_{FE}(1/\omega_T + C \mu \cdot R_c) \), \( h_{FE} \) is the static forward current gain, and \( R_c \) is the collector resistor of the circuit. Solving this equation for \( I_C = 0.1 \cdot I_{cs} \) at time \( t_{d3} \) yields

\[
t_{d3} = -T_r \ln\left[1 - \frac{0.1 \cdot I_{cs}}{h_{FE} \cdot I_{b1}}\right]
\]

(3.5)

where \( I_{cs} = V_{cc}/R_c \).

The Delay Time, \( t_d \), is the algebraic sum of the three components, \( t_{d1} \), \( t_{d2} \), and \( t_{d3} \). In the Single-Stage Inverter
Figure 3.3 The Active Model for the BJT Used to Calculate $t_{d3}$. 
circuit shown in Figure 3.4, \( t_d \) is found to be equal to 5.9 ns (\( t_{d_1} = 4.55 \text{ ns}, t_{d_2} = 177 \text{ ps}, \) and \( t_{d_3} = 2.17 \text{ ns} \)). Using a fast pulse generator (the rise time and fall time were less than 10 ns), the Delay Time was measured in the laboratory to be equal to 5 ns. The 38% error may stem from incorrect estimates of the BJT characteristics and the measurement errors in the laboratory. Details on the measurement procedures are described in Section 3.3.

The Rise Time, \( t_r \), is the time required for \( I_c \) to rise from 10% to 90% of the saturation current value, \( I_{cs} \). This transition is strictly within the active region of operation; therefore, the exponential equation described for \( t_{d_3} \) applies for \( t_r \) also, and it is of the form

\[
I_c(t) = h_{FE} \cdot I_{b_1} \left[ 1 - \exp\left( -\frac{t}{T_r} \right) \right]
\]  

(3.4)

where \( I_{b_1} = (V_1 - V_t)/(R_s + r_X) \) and \( T_r = h_{FE}(1/\omega_T + C_\mu \cdot R_c) \).

Allowing \( I_c(t_1) = 0.1 \cdot I_{cs} \) and \( I_c(t_2) = 0.9 \cdot I_{cs} \), \( t_r = t_2 - t_1 \). Thus solving for \( t_1 \) and \( t_2 \) yields

\[
t_1 = -T_r \ln\left(1 - \frac{0.1 \cdot I_{cs}}{h_{FE} \cdot I_{b_1}} \right)
\]

(3.6a)

\[
t_2 = -T_r \ln\left(1 - \frac{0.9 \cdot I_{cs}}{h_{FE} \cdot I_{b_1}} \right)
\]

(3.6b)
Figure 3.4 The Single-Stage Inverter Circuit Used to Calculate the Response Times.
Solving for $t_r$ gives

$$t_r = T_r \ln \left\{ \frac{0.1 \cdot I_{cs}}{h_{FE} \cdot I_{b1}} \right\} \div \left\{ \frac{0.9 \cdot I_{cs}}{h_{FE} \cdot I_{b1}} \right\}. \quad (3.7)$$

For the Single-Stage Inverter circuit of Figure 3.4, $t_r$ was calculated to be 18 ns and measured as 10 ns.

As long as the input signal remains in the high state, $I_c$ continues to rise according to Equation 3.4 until the limiting value of the saturation current, $I_{cs'}$, is reached. The BJT is now in the saturation region of operation with excess minority carriers building up charge in the base. Once the input voltage falls back to the level $V_2$, this charge has to be removed before $I_c$ changes. The time required for the charge removal and for $I_c$ to drop to 90% of $I_{cs}$ is the Storage Time.

The Storage Time, $t_s'$, is generally the longest of all the response times; thus, it is the limiting factor for switching speed. As described above, $t_s$ is composed of two components. The first, $t_{s1}'$, is the time required to remove the excess charges from the minority carriers in the base region. This transition takes the BJT from saturation to the border of the active region of operation. Thus $t_{s1}'$ is calculated from the model of the BJT in saturation with both forward and reverse current components. The emitter current, $I_{e'}$, is of the form
Rearranging terms and substituting expressions allows the reverse current component, $I_{e_r}$, to be expressed as

$$I_{e_r} = -\alpha_r \left[ \frac{I_{cs} + \alpha_f I_e}{1 - \alpha_f \alpha_r} \right].$$  \hspace{1cm} (3.9)

Previous work by Moll has shown that Equation 3.9 can be expressed in the frequency domain by taking transforms [9]. Particularly, $\alpha_f$ and $\alpha_r$ can be expressed as

$$\alpha_f = \frac{\alpha_f}{1 + j(\omega/\omega_f)}$$  \hspace{1cm} (3.10a)

$$\alpha_r = \frac{\alpha_r}{1 + j(\omega/\omega_r)}.$$  \hspace{1cm} (3.10b)

Thus, the difference $\Delta I_{e_r}$ can be expressed as

$$\Delta I_{e_r} = \frac{\alpha_f \alpha_r [I_{e_1} - I_{e_2}]}{1 - \alpha_f \alpha_r [1 - \text{EXP}\{s_0 t\}]}$$  \hspace{1cm} (3.11)
where \( s_0 = \omega_f \cdot \omega_r (1 - \alpha_f \cdot \alpha_r) / (\omega_f + \omega_r) \), and \( I_{e1} \) and \( I_{e2} \) represent the total emitter current just before and just after the input signal transition, respectively. By definition, \( t_{s1} \) occurs when \( I_{e1} \) is zero and all of the emitter current comes from the forward component, \( I_{e1} \). For this to happen, \( \Delta I_{e1} \) must compensate for the value of \( I_{e1} \) just when \( V_{in} \) falls to \( V_2 \). If this value is defined as \( I_{e1} \), then \( t_{s1} \) ends when \( \Delta I_{e1} = -I_{e1} \). Using this to solve Equation 3.11 for \( t_{s1} \) yields

\[
 t_{s1} = T_s \ln \left[ \frac{I_{b1} - I_{b2}}{I_{cs}/h_{FE} - I_{b2}} \right]
\]

(3.12)

where \( T_s = \frac{\omega_f + \omega_r}{\omega_f \cdot \omega_r (1 - \alpha_f \cdot \alpha_r)} \) and \( I_{b2} = (V_2 - V_t)/(R_s + r_x) \).

The second component of the Storage Time, \( t_{s2} \), is the time required for \( I_c \) to drop to 90\% of \( I_{cs} \). The BJT is in the active region during this period. Therefore, \( I_c \) follows a similar differential equation to that which led to the derivation of \( t_{d3} \) and \( t_r \). Here, the equation is solved as

\[
 I_c(t) = h_{FE} \cdot I_{b2} + \{h_{FE} \cdot I_{b2} + I_{cs} \exp \left[ -\frac{t}{T_r} \right] \}
\]

(3.13)

where \( I_{b2} = (V_2 - V_t)/(R_s + r_x) \) and \( T_r = h_{FE}(1/\omega_T + C_w \cdot R_c) \).
By solving Equation 3.13 when \( I_C = 0.9 \cdot I_{CS} \), \( t_{S2} \) is determined to be equal to

\[
t_{S2} = T_r \ln \left\{ \frac{1 - \frac{I_{CS}}{h_{FE} \cdot I_{b2}}} {\frac{0.9 \cdot I_{CS}}{h_{FE} \cdot I_{b2}}} \right\}.
\]

Thus the Storage Time, \( t_s \), is given by the sum of \( t_{S1} \) and \( t_{S2} \). For the specific test circuit shown in Figure 3.4, \( t_s \) is calculated to be 303 ns (\( t_{S1} = 290 \) ns and \( t_{S2} = 13 \) ns). Taking the average value for \( t_s \) of nine 2N3904 BJT's, a measured value of 314 ns is obtained yielding 96% accuracy with the results.

The Fall Time, \( t_f \), is the time required for \( I_C \) to continue dropping exponentially to 10% of \( I_{CS} \). The BJT is strictly within the active region of operation, so Equation 3.13 applies for \( t_f \) also. Taking the time interval between \( I_C = 0.9 \cdot I_{CS} \) and \( I_C = 0.1 \cdot I_{CS} \) gives \( t_f \) as

\[
t_f = T_r \ln \left\{ \frac{1 - \frac{0.9 \cdot I_{CS}}{h_{FE} \cdot I_{b2}}} {\frac{0.1 \cdot I_{CS}}{h_{FE} \cdot I_{b2}}} \right\}.
\]

In the Single-Stage Inverter circuit of Figure 3.4, \( t_f \) was calculated to be 127 ns and measured to be equal to 66 ns. The above results are tabulated in Table 3.1 (response times are indicated in ns).
Table 3.1 Response Time Comparison for the Single-Stage Inverter Circuit.

<table>
<thead>
<tr>
<th>Response Time</th>
<th>Measured Value</th>
<th>Calculated Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_d$</td>
<td>5</td>
<td>6.9</td>
</tr>
<tr>
<td>$t_r$</td>
<td>10</td>
<td>18</td>
</tr>
<tr>
<td>$t_s$</td>
<td>314</td>
<td>303</td>
</tr>
<tr>
<td>$t_f$</td>
<td>66</td>
<td>127</td>
</tr>
</tbody>
</table>

These results indicate to the reader the expected accuracy of the computer models yet to be developed. Yet note that the accuracy is dependent on the BJT data and the measurements made. Since most of these data are generalizations obtained from a manufacturer's specification sheet, some variations between the measured and the calculated values are expected. Similarly, experimental errors made during measurements would reduce accuracy. More discussion of these measurements is the subject of the next section.

3.3 Physical Measurements of Sample Transistors

The measured response times of the preceding section were necessary not only as verification for the calculated response times but also as a goal for the SPICE2 BJT model to achieve for the Single-Stage Inverter circuit. This
section describes the techniques used in measuring the response times.

A sample of 9 BJT's were analyzed using the Single-Stage Inverter circuit of Figure 3.4. The values of $R_s$ and $R_c$ were selected as a compromise between the test circuit used in the manufacturer's specification sheet and another circuit used later in the research. $R_s$ is taken to be equal to 3.4 kΩ and $R_c$ to 380Ω. A 5 v DC supply voltage limited $I_{c_s}$ to 13 mA. The input signal was a 5 v pulse applied to $R_s$. The inverter output was measured at the collector of the BJT.

The load for the output was a high impedance oscilloscope probe. By measuring the impedance of the probe on a vector impedance bridge, an L R C equivalent circuit accounted for this loading effect. The measured results were $L = 188$ nH, $R = 76$ Ω, and $C = 14$ pF. The input pulse had a 5 ns Rise Time and a 9 ns Fall Time. The 90% and 10% values of this pulse were used to initiate the BJT response times. The values of $t_d$, $t_r$, $t_s$, and $t_f$ were taken from the output waveform as shown in Figure 3.5.

For the sample of 9 BJT's, the response times were measured in ns and listed in Table 3.2.
Figure 3.5 Input and Output Waveforms Showing the Response Times.
Table 3.2 Measured Response Times for the Single-Stage Inverter Circuit.

<table>
<thead>
<tr>
<th>BJT #</th>
<th>t_d</th>
<th>t_r</th>
<th>t_s</th>
<th>t_f</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5</td>
<td>10</td>
<td>270</td>
<td>62</td>
</tr>
<tr>
<td>2</td>
<td>4.5</td>
<td>10</td>
<td>400</td>
<td>75</td>
</tr>
<tr>
<td>3</td>
<td>5</td>
<td>10</td>
<td>300</td>
<td>66</td>
</tr>
<tr>
<td>4</td>
<td>4.5</td>
<td>10</td>
<td>360</td>
<td>64</td>
</tr>
<tr>
<td>5</td>
<td>4.5</td>
<td>10</td>
<td>235</td>
<td>65</td>
</tr>
<tr>
<td>6</td>
<td>5</td>
<td>9.5</td>
<td>340</td>
<td>65</td>
</tr>
<tr>
<td>7</td>
<td>5</td>
<td>10</td>
<td>325</td>
<td>67</td>
</tr>
<tr>
<td>8</td>
<td>5</td>
<td>10</td>
<td>270</td>
<td>62</td>
</tr>
<tr>
<td>9</td>
<td>4</td>
<td>9</td>
<td>325</td>
<td>65</td>
</tr>
</tbody>
</table>

The average of these values are compared to the maximum values listed by the manufacturer using a different test circuit. These data in ns are tabulated in Table 3.3.

Table 3.3 Response Time Comparison between the Average Measured Value and the Manufacturer's Data.

<table>
<thead>
<tr>
<th>Response Time</th>
<th>Average Value</th>
<th>Specification Maximum Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_d</td>
<td>4.7</td>
<td>35</td>
</tr>
<tr>
<td>t_r</td>
<td>9.8</td>
<td>35</td>
</tr>
<tr>
<td>t_s</td>
<td>314</td>
<td>200</td>
</tr>
<tr>
<td>t_f</td>
<td>66</td>
<td>50</td>
</tr>
</tbody>
</table>

The differences arise because different voltages and resistances were used in the manufacturer's test circuit.

Thus by taking response time measurements of a sample of 2N3904 BJT's, an average set of values were determined
which would be used as a goal for the SPICE2 model. This goal is listed as follows:

\[ t_d = 5.0 \text{ ns} \]
\[ t_r = 10.0 \text{ ns} \]
\[ t_s = 314.0 \text{ ns} \]
\[ t_f = 66.0 \text{ ns} \]

3.4 Determination of the SPICE2 Parameters

In order to simulate the response times with the computer, the SPICE2 BJT model parameters have to be selected. This section examines two schemes which determine these values. The first scheme considers the SPICE2 BJT model as a transfer function; and, the second scheme examines the device parameters obtaining numerical values from actual physical measurements. These two methods are then compared for the Single-Stage Inverter circuit application.

For the Transfer Function Method, the Single-Stage Inverter circuit (Figure 3.6) was modeled by SPICE2. The linear components such as resistors, capacitors, inductors, and voltage sources were readily incorporated into the SPICE2 model for the entire circuit. The main focus of the Transfer Function Method was on the nonlinear BJT model
Figure 3.6 The Single-Stage Inverter Circuit Used to Determine the SPICE2 BJT Model Parameters.

- $V_{cc}$: 5 V
- $R_s$: 3.4 kΩ
- $R_C$: 380 Ω
- $Q$: 2N3904
- $V_{in}$: 5V pulse
- $L_1$: 188 nH
- $R_1$: 77 Ω
- $C_1$: 14 pF

Figure 3.6 The Single-Stage Inverter Circuit Used to Determine the SPICE2 BJT Model Parameters.
As was explained in Chapter II, SPICE2 uses the model shown in Figure 2.2 for the BJT. The governing equations for this model were presented in Chapter II (Equations 2.8). Thus, as stated earlier, the SPICE2 model offers 16 variables to be incorporated into the transfer function.

Consider the system representation illustrated in Figure 3.7. Let the actual simulation of the Single-Stage Inverter circuit be considered a system with the input being the 16 parameters and with the output being the four response times. Let the effect that any input parameter, \( P_j \), has on a particular response time, \( t_i \), be described as a function, \( f_{ij} \). Then any response time can be considered the sum of 16 functions which can be expressed as

\[
t_i = f_{i1}(P_1) + f_{i2}(P_2) + \cdots + f_{i16}(P_{16}).
\]  

(3.16)

By varying the values of the 16 SPICE2 parameters, one determines that four did not significantly affect the simulated response time results. Therefore, these parameters were eliminated from consideration. This reduced the number of parameters to 12 which are BF, BR, CCS, TF, TR, CJE, CJC, IS, PE, PC, ME, and MC. So Equation 3.16 can also be reduced from 16 to 12 functions for the four response times.
Figure 3.7 The Transfer Function Method's Representation for the SPICE2 BJT Model.
In order to determine values for the 12 parameters, a first order Taylor's approximation was applied to Equation 3.16 resulting in Equation 3.17 as

\[ t_i = a_{i0} + (a_{i1})(\Delta P_1) + (a_{i2})(\Delta P_2) + \cdots + (a_{i12})(\Delta P_{12}). \]  

(3.17)

Arranging the information in a matrix form, one can write,

\[
\begin{bmatrix}
    t_d \\
    t_r \\
    t_s \\
    t_f
\end{bmatrix}
= 
\begin{bmatrix}
    t_{d_0} \\
    t_{r_0} \\
    t_{s_0} \\
    t_{f_0}
\end{bmatrix}
+ 
\begin{bmatrix}
    a_{1,1} & a_{1,2} & \cdots & a_{1,12} \\
    a_{2,1} \\
    a_{3,1} \\
    a_{4,1}
\end{bmatrix}
\begin{bmatrix}
    \Delta P_1 \\
    \Delta P_2 \\
    \cdots \\
    \Delta P_{12}
\end{bmatrix}
\]

(3.18)

Thus a set of linear equations could be used to approximate the response times as long as the \( \Delta P \)'s were small.

The coefficients of Equation 3.18 were determined from results found by SPICE2 simulations. An initial estimate for the 12 SPICE2 parameters would yield the response time values for \( t_{d_0}, t_{r_0}, t_{s_0}, \) and \( t_{f_0} \). By perturbing each of the parameters separately, the coefficients for \( a_{ij} \) could be calculated.

This process presents one difficulty; 12 parameter
variables must be found from only four response time equations. So only four parameters could be determined at a time. The approach taken was to rank the effect each parameter had on the response times. The four parameters which had the greatest effect were solved first using the goal values for the four response times. This process was then repeated twice until the last set of four parameters was also solved. So even with just four equations, all 12 parameters could be determined iteratively, as shown below:

1. Determine an initial "guess" as to the values of all 12 parameters.

2. Rank the parameters by the magnitude of the effect they have on the response times.

3. Choose the four most significant parameters and introduce perturbations running a total of five simulations.

4. Analyze the data using a matrix algorithm to achieve four new values for the parameters.

5. Shift the process to the next four most significant parameters and analyze.

6. Shift the process to the last four parameters and analyze.

7. Using all new parameters, iterate steps 2 through 6 until the system output matches the goal response times.

This procedure led to the following values:
BF = 100
BR = 30
CCS = 27 pF
TF = 0.4 ns
TR = 10 ns
CJE = 5 pF
CJC = 2 pF
IS = 1 pA
PE = 0.9 V
PC = 0.5 V
ME = 0.33
MC = 0.66

So the Transfer Function Method could be used for evaluating the SPICE2 BJT model parameters. The response times in ns resulting from simulation using parameters evaluated by this method are compared to the goal values in Table 3.4.

Table 3.4 Response Time Comparison for the Transfer Function Method.

<table>
<thead>
<tr>
<th>Response Time</th>
<th>Goal</th>
<th>Simulation Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_d$</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>$t_r$</td>
<td>10</td>
<td>11</td>
</tr>
<tr>
<td>$t_s$</td>
<td>314</td>
<td>318</td>
</tr>
<tr>
<td>$t_f$</td>
<td>66</td>
<td>61</td>
</tr>
</tbody>
</table>

Thus close results can be achieved at the expense of many iterations.

For the second scheme of determining the SPICE2 BJT model parameters, physical properties of the BJT were
measured. The same Single-Stage Inverter circuit of Figure 3.6 was again modeled by SPICE2. The Physical Measurements Method determined the 16 parameters to be used in the simulation. These measurements were taken as described by Getreu [1].

BF, the forward current gain, was found by taking the ratio of $I_c$ to $I_b$ from a curve tracer. The average BF measured at $I_c = 13$ mA and $I_c = 1$ mA was found to be equal to 170. Similarly, BR, the reverse current gain, was measured at $I_c = -200$ mA with an average value of 0.6. The energy gap, $E_G$, was taken to be equal to 1.11 eV. For $I_S$, the saturation current, $I_c$ and $V_{be}$ data were taken with $V_{bc} = 0$. Thus the SPICE2 equation would reduce to

$$I_c = I_S\exp(\frac{V_{be}}{V_t}) - 1$$

(3.19)

Plotting $\ln(I_c)$ as a function of $V_{be}$ results with a line since the $-1$ term of Equation 3.19 is negligible. This line is extrapolated back to $V_{be} = 0$ yielding $\ln(I_S)$. This gave a value for $I_S$ of 0.4 pA. This value was then temperature compensated from 21 °C to 27 °C using the relation,

$$I_S(T_2) = I_S(T_1)\cdot\left(\frac{T_2}{T_1}\right)^{3}\cdot\exp\left(-\frac{E_G}{K}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right)$$

(3.20)
The compensated value for IS was 1 pA.

For CJE, PE, and ME (the emitter-base junction capacitance at $V_{be} = 0$, the emitter-base barrier potential, and the emitter-base capacitance gradient factor respectively) data was taken for the reverse bias junction capacitance as given by the manufacturer [10]. Under the reverse bias conditions, the capacitance, $C$, from the data can be expressed as

$$C = CJE[1 - \frac{V_{be}}{PE}]^{ME} + C_k$$

(3.21)

where $C_k$ is a constant value stemming from capacitance of the measuring device. Plots of the difference of $C$ and $C_k$ as a function of $V_{be}$ on a log-log scale for various values of $C_k$ and PE would generally be nonlinear. An iterative procedure led to the correct values for $C_k$ and PE as indicated by a linear representation of the data on the log-log scale. CJC, PC, and ME (the collector-base junction capacitance at $V_{bc} = 0$, the collector-base barrier potential, and the collector-base capacitance gradient factor respectively) were determined in the same manner. The resulting parameter values are
CJE = 2.21 pF  
PE = 2.0 V  
ME = 1.81  
CJC = 2.57 pF  
PC = 2.0 V  
MC = 0.802

The substrate capacitance, CCS, was set equal to zero. Since the particular device is a discrete component and not an IC transistor, there is no substrate capacitance.

The ohmic contact resistance, RB, was measured using pulse techniques. When a step pulse switches from high to low current into the base of the BJT, a very small change can be measured in V\(_{\text{be}}\) before an exponential decay brings V\(_{\text{be}}\) to 0. This small change in V\(_{\text{be}}\) divided by the original high base current yields RB. RB was found to be equal to 13.2Ω.

RE was measured from the slope of the line obtained by plotting I\(_b\) as a function of V\(_{\text{ce}}\). The slope was measured giving the reciprocal of RE as shown in Figure 3.8. RE was determined to be equal to 2.5Ω.

RC was measured as the reciprocal of the slope of a line drawn through the current "knees" as shown in Figure 3.9. Note that while the actual value of RC varies with I\(_c\), the value is bounded by RC\(_{\text{sat}}\) and RC\(_{\text{active}}\). For the purpose of digital switching, RC\(_{\text{sat}}\) was used for RC and was measured at 1Ω.

To determine TF, the total forward transit time, the
Figure 3.8 $I_b$ Versus $V_{ce}$ Characteristics Showing the Value of $RE$. 

High Current Effects

Slope = $\frac{1}{RE}$
Figure 3.9  $I_c$ Versus $V_{ce}$ Characteristics Showing the Limiting Values for $RC$. 

\[ \text{Slope} = \frac{1}{RC_{\text{sat}}} \quad \text{Slope} = \frac{1}{RC_{\text{active}}} \]
maximum transition frequency, $f_{T_{\text{max}}}$, had to be measured. Since $f_T$ is a function of $I_C$, values of $f_T$ were measured for various levels of $I_C$. By extrapolating $f_T$ for larger values of $I_C$ from the data taken, TF could be calculated according to

$$TF = \frac{1}{(2\pi f_{T_{\text{max}}})} - C_{bc} \cdot RC$$

(3.22)

where $C_{bc}$ is determined from $V_{bc}$ and $RC$ is the RC active value at the appropriate value of $I_C$. With $f_{T_{\text{max}}} = 2.05$ GHz, $C_{bc} = 3.24$ pF, and $RC = 6\Omega$, TF was calculated as 58.2 ps.

TR, the total reverse transit time, is calculated from previous results and from $T_s$ according to the expression,

$$TR = T_s \left[ \frac{1 - \frac{\alpha_f}{\alpha_r}}{\alpha_r} \right] - \left[ \frac{\alpha_f}{\alpha_r} \right] TF$$

(3.23)

where $T_s$ is indicated in Equation 3.12. $T_s$ was found to be equal to 169 ns, yielding a value equal to 282 ns for TR.

So by the Physical Measurements Method, the 16 parameters for the SPICE2 BJT model were evaluated as follows:
BF = 170
BR = 0.6
RB = 13.2 Ω
RC = 1 Ω
RE = 2.5 Ω
CCS = 0 pF
TF = 58.2 ps
TR = 282 ns
CJE = 2.21 pF
CJC = 2.57 pF
IS = 1 pA
PE = 2.0 V
PC = 2.0 V
EG = 1.11 eV
ME = 1.81
MC = 0.802

The response times resulting from these parameters are discussed next.

SPICE2 simulation of the Single-Stage Inverter circuit of Figure 3.6 was also conducted for the parameters found using the Physical Measurements Method (PMM). The response times in ns which resulted are compared to those from the Transfer Function Method (TFM) in Table 3.5.
Table 3.5 Result Comparison between the Transfer Function and the Physical Measurements Methods.

<table>
<thead>
<tr>
<th>Response Time</th>
<th>Goal</th>
<th>TFM Results</th>
<th>PMM Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_d$</td>
<td>5</td>
<td>4.5</td>
<td>0</td>
</tr>
<tr>
<td>$t_r$</td>
<td>10</td>
<td>11.5</td>
<td>5.5</td>
</tr>
<tr>
<td>$t_s$</td>
<td>314</td>
<td>329.0</td>
<td>291.5</td>
</tr>
<tr>
<td>$t_f$</td>
<td>66</td>
<td>46.5</td>
<td>36.5</td>
</tr>
</tbody>
</table>

Examining the above results, the Transfer Function Method provides greater accuracy than the Physical Measurement Method. Nonetheless, both methods provide reasonable estimates for the response times which validates the effectiveness of the models.

3.5 Summary

A SPICE2 model for the BJT can be derived to give useful response times. The parameters for this model can be derived using two different methods; each method yields results as accurate as the calculated values which result directly from the physics of the BJT for the Single-Stage Inverter circuit. Compare the percentage errors listed in Table 3.6.
Table 3.6 Result Error Analysis.

<table>
<thead>
<tr>
<th>Response Time</th>
<th>Calculated Error</th>
<th>TFM Error</th>
<th>PMM Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_d$</td>
<td>38%</td>
<td>10%</td>
<td>100%</td>
</tr>
<tr>
<td>$t_r$</td>
<td>80%</td>
<td>15%</td>
<td>45%</td>
</tr>
<tr>
<td>$t_s$</td>
<td>4%</td>
<td>5%</td>
<td>7%</td>
</tr>
<tr>
<td>$t_f$</td>
<td>92%</td>
<td>30%</td>
<td>45%</td>
</tr>
</tbody>
</table>

It is to be noticed that accurate values for $t_s$ are provided, $t_s$ being the most critical response time because of its length. Thus a satisfactory model for the BJT as it applies to the Single-Stage Inverter circuit can be developed.
Chapter IV

DEVELOPMENT OF A SCHOTTKY BARRIER DIODE MODEL

4.1 Introduction

The SPICE2 development for the BJT model presents the first part in modeling the Schottky Transistor. The second part concerns the development of a SPICE2 model for the Schottky Barrier Diode (SBD). This chapter is dedicated to that purpose.

Unlike the development of the SPICE2 BJT model, only one set of model parameters is derived for the SBD model. Since the SPICE2 Diode model has fewer parameters than the BJT model, a more direct development is used to obtain the diode instead of using the Transfer Function Method.

The developmental process for the SBD model consists of first examining the nature of the SBD and then comparing its basic characteristics to those of the normal p-n junction diode. This task is described in Section 4.2. In Section 4.3, the physical results are then applied to the SPICE2 Diode model. Although SPICE2 is designed to model p-n junction diodes, the model is to be modified to accommodate the SBD. The accuracy of this new SPICE2 SBD model is examined in the Single-Stage Inverter circuit using the Schottky Transistor. Section 4.4 ends the chapter by
reviewing the modeling approach, the model derived, and its accuracy.

4.2 Physics of the Schottky Barrier Diode

Before modeling the SBD, the physics of the device are reviewed. More specifically, relationships for the diode current and the diode capacitance as a function of the applied voltage are presented. These relationships are also compared to the regular p-n junction diode to understand the special considerations to be incorporated into the SBD model.

The SBD is a metal-semiconductor junction diode which results in a separation of energy levels between the two materials known as the Schottky barrier [11]. Such a diode can be formed by depositing aluminum, with the n+ diffusion omitted, onto n-type silicon. The resulting junction between the metal and the semiconductor is a rectifying contact as opposed to the usual ohmic contact formed when a lead is applied to the semiconductor [7]. As Rhoderick has explained, the SBD is a majority carrier device with four current transport mechanisms for these carriers under forward bias condition [8].

The dominant transport mechanism is that of electron emission over the barrier. Although two processes are
involved (diffusion of electrons from the semiconductor side to the interface and thermionic-emission of electrons from the interface to the metal), the diode current is estimated from the process which is most limiting. However, if the barrier height is much larger than one KT, electron collisions within the depletion region are negligible, and the effect of image force may also be neglected, then the thermionic-emission is the dominant process [8]. Using these assumptions for modeling the SBD, the resulting current density expression, \( J \), is of the form

\[
J = J_0 \left[ \exp \left( \frac{qV}{nKT} \right) - 1 \right]
\]

(4.1)

where \( J_0 \), the thermionic-emission current density at thermal equilibrium, is assumed to be constant possessing a typical numerical value, \( n \) is a constant depending on the material called the "ideality factor", \( q \) is the electronic charge, \( K \) is Boltzmann's constant, \( T \) is the absolute temperature, and \( V \) represents the voltage applied across the junction. This expression dominates the current-voltage relationship as all other current transport mechanisms describe slight variations between physical observations and Equation 4.1.

The second transport mechanism is the electron tunneling through the Schottky barrier. Because electrons
can enter excited energy states due to temperature extremes, high energy electrons can penetrate the barrier. The third mechanism is the electron-hole recombination within the depletion region. This is similar to the phenomenon observed in the p-n junction but is more pronounced in a SBD made from gallium arsenide and operating at low temperature. The fourth mechanism is the hole injection. If the barrier height is too large, a high density of holes can accumulate adjacent to the metal. These holes can then diffuse into the neutral region. But this effect as with the previous two current transport mechanisms is only significant under extreme environmental conditions such as low temperature, high diode current, or extremely low diode current including reverse bias operation.

The SBD is being modeled for application in the Schottky Transistor. As described in Chapter 1, the diode's purpose is to prevent the transistor from entering saturation and to cause a fast switch-off in order to minimize the Storage Time. These effects do not involve the extremes described previously since a silicon SBD is modeled at room temperature, the thermionic-emission theory is used to describe the current-voltage relationship. Equation 4.1 can be rewritten as
where $I_d$ is the diode current, $V_d$ is the applied voltage, and $V_t$ is the thermal voltage ($V_t = K \cdot T/q$). Equation 4.2 describes the I-V characteristics of the Schottky barrier not including the ohmic contact resistance. This is examined for a particular SBD in Section 4.3.

With the I-V relationship presented for the Schottky barrier, the junction capacitance is left to be examined. Since the SBD has only majority carriers, there are no minority carrier storage to offer diffusion capacitance [8]. The result is that the capacitance of the depletion region is the most significant capacitance with the diode forward biased, as long as the effect of "traps" are ignored. Traps act as localized groups of electrons within the bulk of the semiconductor which can accumulate charge thus affecting the capacitance value. Assuming this effect is negligible, Rhoderick's expression [8] for the capacitance of the depletion region, $C_d$, represents the total capacitance of the junction and is expressed in a slightly modified form as

$$C_d = C_{d0} \left[1 - \frac{V_d}{\phi_b}\right]^{-0.5}$$

(4.3)
where $C_d$ is the junction or depletion capacitance, $V_d$ is the junction voltage, $C_{d0}$ is the capacitance across the junction at zero bias, and $\phi_b$ is the barrier potential. Thus Equation 4.3 describes the junction capacitance as a function of the junction voltage.

The SBD current expression for Equation 4.2 has the same form for p-n junction diodes. Thus under the assumptions made, the I-V characteristics of the SBD and the p-n junction diode are the same. Note that the transport mechanisms governing these characteristics are different as the p-n junction diode depends on the diffusion of minority carriers, while the SBD conducts due to thermionic-emission of majority carriers. While this major difference has little effect on the I-V characteristic, the capacitance under forward bias is greatly altered. Under reverse bias, both diodes experience similar capacitance effects of the depletion region. Thus the major difference between the SBD and the p-n junction diode is the forward biased diffusion capacitance offered by the p-n junction diode which accounts for the faster switching speed of the SBD.

4.3 Determination of a SPICE2 Model

In this section, the current and the capacitance expressions presented in Section 4.2, are to be incorporated
into a SPICE2 model for a particular SBD. To relate the present SPICE2 Diode model to the physical expressions, values for the SPICE2 parameters need to be determined. These values are found from data listed on the manufacturer's specification sheet. The values are then incorporated into the SPICE2 model for the SBD. Simulation results of the Single-Stage Inverter circuit yield response times which are compared to those obtained from physical measurements of the circuit.

The existing SPICE2 Diode model was examined to see if it can accommodate the SBD. The SPICE2 Diode model combines a nonlinear voltage dependent current source, $I_d'$, and a capacitor, $C_d'$, with a series resistance, $R_s$, as described in Chapter II, Figure 2.3. As described before, the nonlinear expression for the current source, $I_d'$, and the nonlinear junction capacitance, $C_d'$, are functions of the junction voltage, $V_d'$, as represented in Equations 2.10. So the SPICE2 Diode model possess 8 parameters, $R_s$, $TT$, $CJO$, $IS$, $PB$, $EG$, $M$, and $N$. In this section the mathematical expressions of the model are compared to the physical expressions to see if the SPICE2 model can accommodate the SBD.

The I-V and C-V expressions presented for the SBD in Section 4.2 can be incorporated into the SPICE2 Diode model. By comparing Equation 4.2 to Equation 2.10a, the SPICE2 I-V
expression matches the SBD physical expression if IS represents I₀. Comparison of Equation 4.3 to Equation 2.10b shows that the SPICE2 C-V expression can match the SBD physical expression if TT is set to 0 which removes the diffusion capacitance term, CJO is exchanged with \(C_{d_s}'\), PB with \(\phi_b'\), and M with 0.5. So in order for the SPICE2 Diode model to incorporate the physical expression of the SBD, two of the parameters, TT and M, have to be set to fixed values and the remaining six parameters must have values determined from data obtained from the manufacturer's specification sheet as discussed next.

The particular SBD used in this research is an HP 5082-2800. In order to find values for this diode for the 6 remaining parameters (RS, CJO, IS, PB, EG, M, AND N), various data points were taken from an I-V characteristic curve provided by the manufacturer [12]. Assuming the data fit the form of Equation 2.10a, these data were plotted on a semi-log scale (Figure 4.1). Because of the exponential nature of the data, the resulting plot placed the data points on a straight line with the exception of diode current values greater than 1 mA. Therefore, the data for current values less than 1 mA fit the form of Equation 2.10a. Extrapolating the line for the y intercept yielded the ln(IS). The slope of the line determined \([N\cdot V_t]^{-1}\). From the actual line IS was calculated to be 39 nA and N to
Figure 4.1 Semi-Log Plot of the Typical I-V Characteristics for the SBD.
Next, the data for diode current greater than 1 mA were considered. Solving Equation 2.10a for $V_d$ in terms of $I_d$ and using the above values for $I_S$ and $N$, values for $V_d$ were calculated for the corresponding values of $I_d$ from the data points. The difference between the data points and the calculated values is divided by the particular value of $I_d$. This allows for the discrepancies in data to be accounted for by a series resistance, $R_S$. By taking the average value determined by this method, $R_S$ was determined to be 21Ω. Thus $R_S$ was used to compensate for the deviation of the data from Equation 2.10a.

Using the values of $I_S$, $N$, $R_S$, and the model shown in Figure 2.3, the I-V characteristics for the HP 5082-2800 SBD were compared to that offered by the model. The results are shown below in Table 4.1.
Table 4.1 I-V Comparison between the SPICE2 Model and the Data.

<table>
<thead>
<tr>
<th></th>
<th>( I_d ) (in mA)</th>
<th>( V_d ) from Data (in V)</th>
<th>( V_d ) Calculated (in V)</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.01</td>
<td>0.22</td>
<td>0.21</td>
<td>4.5%</td>
<td></td>
</tr>
<tr>
<td>0.05</td>
<td>0.26</td>
<td>0.27</td>
<td>3.8%</td>
<td></td>
</tr>
<tr>
<td>0.10</td>
<td>0.29</td>
<td>0.30</td>
<td>3.4%</td>
<td></td>
</tr>
<tr>
<td>0.50</td>
<td>0.35</td>
<td>0.37</td>
<td>5.7%</td>
<td></td>
</tr>
<tr>
<td>1.00</td>
<td>0.38</td>
<td>0.40</td>
<td>5.3%</td>
<td></td>
</tr>
<tr>
<td>1.32</td>
<td>0.40</td>
<td>0.42</td>
<td>5.0%</td>
<td></td>
</tr>
<tr>
<td>8.00</td>
<td>0.60</td>
<td>0.63</td>
<td>5.0%</td>
<td></td>
</tr>
<tr>
<td>13.0</td>
<td>0.80</td>
<td>0.75</td>
<td>6.3%</td>
<td></td>
</tr>
</tbody>
</table>

Setting \( IS = 39 \, \text{nA}, \, N = 1.462, \) and \( RS = 21\Omega \) allows SPICE2 to simulate the I-V characteristics of the HP 5082-2800 SBD to within 93% accuracy.

A similar approach was used to find values for \( C_{JO}, PB, \) and \( M. \) Examining the C-V characteristic curve for the HP 5082-2800 SBD as provided by the manufacturer [12] data points were obtained. Because these data were assumed to fit Equation 4.3 having a \(-1/2\) exponent, the reciprocal of the square of the capacitance was plotted as a function of reverse bias voltage. Actually, because of the stray capacitance due to the measuring techniques, a variation of Equation 4.3 was used which is of the form

\[
[C_d - C_k]^{-2} = K[\phi - V_d]
\]  

(4.6)
where $C_k$ is the stray capacitance value and $K = C_d^e - \phi_b^v$. Various values for $C_k$ were used until the resulting data plots were linear. Note that this process is very similar to the one used to determine the depletion capacitance terms for the SPICE2 BJT model as described in Chapter III. The process yielded $C_k = 0.18 \text{ pF}$.

Since the y intercept of the line described previously was $C_d^e - \phi_b^v$, this value was readily determined to be $0.3715 \text{ pF}^{-2}$. Although this corresponds to a value for $C_d^e$ of $1.641 \text{ pF}$, the value of $1.470 \text{ pF}$ was used as it improved the accuracy. $K$, the slope of the line, was measured as $0.9263$. Since $K = C_d^e - \phi_b^v$, $\phi_b$ was calculated to be $0.4010 \text{ v}$.

Using the values for $C_d^e$, $\phi_b$, $C_k$, and Equation 4.3 where $C_k$ is added to $C_d^e$, the calculated values of capacitance were compared to the manufacturer's data and is listed below in Table 4.2.

Table 4.2 C-V Comparison between the SPICE2 Model and the Data.

<table>
<thead>
<tr>
<th>$V_d$ (in V)</th>
<th>$C_d$ from Data (in pF)</th>
<th>$C_d$ Calculated (in pF)</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0</td>
<td>1.50</td>
<td>1.65</td>
<td>10.0%</td>
</tr>
<tr>
<td>-1.3</td>
<td>1.00</td>
<td>0.89</td>
<td>11.0%</td>
</tr>
<tr>
<td>-5.2</td>
<td>0.63</td>
<td>0.57</td>
<td>9.5%</td>
</tr>
<tr>
<td>-10.0</td>
<td>0.50</td>
<td>0.47</td>
<td>6.0%</td>
</tr>
<tr>
<td>-20.0</td>
<td>0.41</td>
<td>0.39</td>
<td>4.9%</td>
</tr>
</tbody>
</table>
Thus the depletion capacitance can be calculated to within 89%.

From the capacitance results, the SPICE2 parameters of Equation 2.10b were easily obtained. From previous results, $TT = 0$ and $M = 0.5$. Similarly, $C_{JO} = C_d = 1.47 \ pF$ and $PB = \psi_B = 0.401 \ V$. The last remaining SPICE2 parameter, $EG$, took the value of 0.69 eV which is the appropriate value for the energy gap of the Schottky barrier [13]. Thus values for all 8 parameters of the SPICE2 SBD model were obtained as follows:

\[
\begin{align*}
RS & = 21 \ \Omega \\
TT & = 0 \\
C_{JO} & = 1.47 \ pF \\
IS & = 39 \ nA \\
PB & = 0.401 \ V \\
EG & = 0.69 \ eV \\
M & = 0.5 \\
N & = 1.462
\end{align*}
\]

Other effects also modeled were the package capacitance of 0.25 pF and the package lead inductance of 3.0 nH as given by the manufacturer. So this completed the development of the SPICE2 SBD model. The next step was to evaluate the performance of the model.

The SPICE2 SBD model was used to simulate the same Single-Stage Inverter circuit described in Chapter III. This circuit now contains the SBD between the base and the collector terminals of the BJT. The SPICE2 model for the
configuration is shown in Figure 4.2. Note that this includes all of the modeling effects for the SBD. Conducting simulation at room temperature yielded transient response curves of digital switching from which the response times were measured. Since the results of Chapter III gave two SPICE2 BJT models [one modeled by the Transfer Function Method (TFM), the other by the Physical Measurement Method (PMM)], both BJT models were simulated. The results in ns are compared to physical measurements made from the actual circuit as shown in Table 4.3.

<table>
<thead>
<tr>
<th>Case</th>
<th>$t_d$</th>
<th>$t_r$</th>
<th>$t_s$</th>
<th>$t_f$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measured Results:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Real Circuit - without SBD</td>
<td>4.0</td>
<td>12.0</td>
<td>350.0</td>
<td>75.0</td>
</tr>
<tr>
<td>Real Circuit - with SBD</td>
<td>4.0</td>
<td>14.0</td>
<td>32.5</td>
<td>75.0</td>
</tr>
<tr>
<td>Simulated Results:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TFM BJT - without SBD</td>
<td>6.0</td>
<td>13.5</td>
<td>330.0</td>
<td>55.5</td>
</tr>
<tr>
<td>TFM BJT - with SBD</td>
<td>6.0</td>
<td>14.5</td>
<td>8.55</td>
<td>60.5</td>
</tr>
<tr>
<td>PMM BJT - without SBD</td>
<td>0.5</td>
<td>9.0</td>
<td>293.5</td>
<td>54.5</td>
</tr>
<tr>
<td>PMM BJT - with SBD</td>
<td>1.0</td>
<td>11.5</td>
<td>11.5</td>
<td>70.0</td>
</tr>
</tbody>
</table>

If the total response time, the sum of the four response times, are calculated and compared for the four simulations, the overall effectiveness of the models can be examined. These results in ns along with the percentage
Figure 4.2 The SPICE2 Model for the Single-Stage Inverter Circuit Including the SBD.
errors are listed in Table 4.4.

Table 4.4 Total Response Time Error Analysis for the Single-Stage Inverter Circuit.

<table>
<thead>
<tr>
<th>Case</th>
<th>Total Response Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>TFM BJT - without SBD</td>
<td>405.0 (8.2%)</td>
</tr>
<tr>
<td>TFM BJT - with SBD</td>
<td>89.5 (29.%)</td>
</tr>
<tr>
<td>PMM BJT - without SBD</td>
<td>357.5 (19.%)</td>
</tr>
<tr>
<td>PMM BJT - with SBD</td>
<td>94.0 (25.%)</td>
</tr>
</tbody>
</table>

Thus, the SPICE2 SBD model offers enough accuracy for the Schottky Transistor to be simulated to within 71% of the total response time in the Single-Stage Inverter circuit by using either model for the BJT. This accuracy is further examined in Chapter V.

4.4 Summary

Investigating the I-V characteristics of the SBD under reasonable assumptions, the behavior of the SBD was compared to that of a p-n junction diode which can already be modeled by SPICE2. Although different transport mechanisms account for the current flow through the diodes, the SBD follows the regular diode equation, Equation 4.2. Since Equation 4.2 readily adapted to the equation governing the SPICE2 Diode model, Equation 2.10a, only values for the parameters had to
be determined. Using data provided by the manufacturer for the particular SBD that was used, values for the SPICE2 parameters IS, N, and RS were determined. By using these parameters and the SPICE2 model, the I-V characteristics of the SBD could be simulated to within 93% of the manufacturer's data.

The C-V characteristics of the SBD differed from that of the p-n junction diode. While both diodes exhibited depletion region capacitance, the regular p-n junction diode also offered diffusion capacitance resulting from the minority carrier charge-storage under forward bias conditions. The SPICE2 Diode model could also incorporate the SBD capacitance relationship of Equation 4.3. The SPICE2 expression, Equation 2.10b, aligns with Equation 4.3 if TT is set to 0 and M is set to 0.5. Values for the rest of the parameters (CJO, PB, and M) were obtained by plotting data provided by the manufacturer on various scales. These values enabled the SPICE2 model to simulate the SBD's capacitance to within 89%. So from the developed SPICE2 models, the Single-Stage Inverter circuit with the Schottky Transistor was simulated yielding a total response time accurate to within 71%.
Chapter V

ANALYSIS USING THE MODELS

5.1 Introduction

The goal of this chapter is to evaluate the accuracy of the SPICE2 Schottky Transistor model and to further compare the results of the two BJT models developed in Chapter III. The first model used the Transfer Function Method (TFM) where the SPICE2 parameter values were determined by perturbations and iterations. The second model was developed by Physical Measurements Method (PMM) where laboratory measurements of various characteristics of a test BJT were used to determine values for the SPICE2 parameters.

Section 5.2 evaluates the expected performance of SPICE2. Certain limitations restrict the accuracy of the simulations even before model errors can be noticed. By accounting for these limitations, a tolerance margin is established to allow for successful simulation results.

In Section 5.3 the SPICE2 models are used to simulate many variations of the Single-Stage Inverter circuit. In Section 5.4 two other circuit configurations which use multiple transistors are simulated. Calculating the total response time, the algebraic sum of the four response times, the simulation results are compared to measured results.
Section 5.5 concludes the chapter by reviewing and condensing the results. The worst case accuracy for the overall ability to model the Schottky Transistor is also determined.

5.2 *Expected Accuracy*

Before the SPICE2 simulation results can be adequately compared to the results of the circuit response measurements, the limitations of accuracy need to be examined. The SPICE2 results have a maximum accuracy to which they can possibly match to a circuit. To understand this limit, two factors are examined – the variations made during physical measurements and the variations among versions of SPICE2. Although the accuracy of the SPICE2 models as developed in Chapters 3 and 4 also affect the simulation results, these models are assumed to be as accurate as possible. From the maximum possible accuracy, a tolerance is established to use as a margin of accuracy between the SPICE2 simulation results and those of circuit response measurements.

The main data used in this thesis were taken from the Single-Stage Inverter circuit of Figure 3.4. The four response times were measured in ns during three separate experiments. The data are shown in Table 5.1.
Table 5.1 Measured Response Time Data for the Single-Stage Inverter Circuit.

<table>
<thead>
<tr>
<th>Experiment #</th>
<th>$t_d$</th>
<th>$t_r$</th>
<th>$t_s$</th>
<th>$t_f$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5</td>
<td>10</td>
<td>325</td>
<td>67</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td>12</td>
<td>350</td>
<td>75</td>
</tr>
<tr>
<td>3</td>
<td>1.5</td>
<td>12</td>
<td>295</td>
<td>80</td>
</tr>
</tbody>
</table>

As shown, less accuracy is available in measuring the shorter response times. Calculating the largest percent variation for the data of each response time, the tolerance is given and is recorded as shown in Table 5.2.

Table 5.2 Error Analysis of the Measured Data.

<table>
<thead>
<tr>
<th>$t_d$</th>
<th>$t_r$</th>
<th>$t_s$</th>
<th>$t_f$</th>
</tr>
</thead>
<tbody>
<tr>
<td>233%</td>
<td>20%</td>
<td>19%</td>
<td>19%</td>
</tr>
</tbody>
</table>

So with the exception of the extremely short Delay Time, $t_d$, the circuit response measurements can be measured to within 80% accuracy.

During the course of research work, a newer version of SPICE2 was also tried. The new version, SPICE2.G, offered slight modifications to the SPICE2.E version [14]. Because revisions generally offer only slight modifications, the
exact differences between SPICE2.E and SPICE2.G were not explored. A comparison of simulation results performed by both versions offer interesting results as shown in Table 5.3. It is important to notice in this respect that all response time results are in ns.

<table>
<thead>
<tr>
<th>Version</th>
<th>$t_d$</th>
<th>$t_r$</th>
<th>$t_s$</th>
<th>$t_f$</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPICE2.E</td>
<td>5.0</td>
<td>11.0</td>
<td>328.5</td>
<td>46.5</td>
</tr>
<tr>
<td>SPICE2.G</td>
<td>5.5</td>
<td>12.0</td>
<td>322.0</td>
<td>59.0</td>
</tr>
<tr>
<td>Variation</td>
<td>10%</td>
<td>9%</td>
<td>2%</td>
<td>27%</td>
</tr>
</tbody>
</table>

Thus results may vary as much as 27% depending on which particular version of SPICE2 is used.

With circuit response measurements accurate only to 80% and SPICE2 versions varying up to 27%, an estimated margin of accuracy is set at 75%. Consider a SPICE2 model which is 100% accurate. Simulation could yield results which are only 90% (a conservative figure) accurate due to different versions of SPICE2 which would all use the same SPICE2 model. But at the worst case, circuit response measurements may yield values which are 120% of the actual response times. Thus an error of 30% could result from a SPICE2 model of 100% accuracy. So the maximum expected accuracy
for the SPICE2 simulation results is 75% which allows for percentage error of only 25%.

Various circuits can now be simulated by SPICE2 with the results compared to actual measurements. Percentage errors less than 25% indicate a totally successful simulation. Errors greater than 25% begin to reflect flaws in the SPICE2 models. Note that SPICE2.E is used throughout all of the simulations in the research. Also note that variations of 2 or 3 ns for τd are allowable to compensate for possible measurement errors. Using these results, the credibility of the SPICE2 models could be examined on a particular circuit as is described in the next section.

5.3 Variations of the Single-Stage Inverter Circuit

Using an anticipated accuracy of 75% and remembering to allow a 2 or 3 ns tolerance to τd', the SPICE2 results for the Single-Stage Inverter circuit were checked for accuracy. Also, five other variations of this circuit were simulated to improve the credibility of the SPICE2 models. The overall accuracy from these analyses rates the performance of the SPICE2 models.

The Single-Stage Inverter circuit shown in Figure 3.4 was simulated with SPICE2. R_c', with a nominal value of 380Ω, was measured as 364Ω. R_s was measured as 3.31 kΩ. Q_1
was modeled with the Schottky Transistor model. Both BJT models developed in Chapter III were used. These simulation results are compared to the circuit response measurements in ns by listing the percentage error as shown in Table 5.4.

Table 5.4 Modeling Method Comparison for the Single-Stage Inverter Circuit.

<table>
<thead>
<tr>
<th>Case</th>
<th>t\textsubscript{d}</th>
<th>t\textsubscript{r}</th>
<th>t\textsubscript{s}</th>
<th>t\textsubscript{f}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real Circuit</td>
<td>2.0</td>
<td>13.0</td>
<td>11.0</td>
<td>75.0</td>
</tr>
<tr>
<td>SPICE2-TFM</td>
<td>6.0 -</td>
<td>14.5(12%)</td>
<td>8.5(23%)</td>
<td>60.5(19%)</td>
</tr>
<tr>
<td>SPICE2-PMM</td>
<td>0.5 -</td>
<td>11.5(12%)</td>
<td>12.5(14%)</td>
<td>70.0(7%)</td>
</tr>
</tbody>
</table>

Note that the accuracy of t\textsubscript{d} was ignored since the 2 or 3 ns deviation would severely change the results. Thus both parameter determining methods yielded models which can be used to simulate the Single-Stage Inverter circuit with the Schottky Transistor within the allowable 75% margin.

As was described in Chapter III, the four response times are affected by various constraints. These constraints are the high level input voltage, \( V_1 \), the low level input voltage, \( V_2 \), the supply voltage, \( V_\text{CC} \), the source resistor, \( R_s \), and the collector resistor, \( R_c \). Thus by varying any one of these five constraints, any of the four response times will correspondingly vary. So SPICE2 simulations should also reflect these variations if the models are truly accurate. Therefore, to assess the
accuracy of the SPICE2 models, five variations of the Single-Stage Inverter circuit were considered. The results are listed in ns in Table 5.5.
Table 5.5 Response Time Comparison for the Five Variations of the Single-Stage Inverter Circuit.

Variation 1:  $V_1 = 7 \text{ v}$

<table>
<thead>
<tr>
<th>Case</th>
<th>$t_d$</th>
<th>$t_r$</th>
<th>$t_s$</th>
<th>$t_f$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real Circuit</td>
<td>0.5</td>
<td>8.0</td>
<td>10.0</td>
<td>75.0</td>
</tr>
<tr>
<td>SPICE2-TFM</td>
<td>2.5 -</td>
<td>10.5(31%)</td>
<td>9.0(10%)</td>
<td>60.5(19%)</td>
</tr>
<tr>
<td>SPICE2-PMM</td>
<td>0.0$^1$</td>
<td>6.5(19%)</td>
<td>17.0(70%)</td>
<td>70.0(7%)</td>
</tr>
</tbody>
</table>

Variation 2:  $V_2 = -1 \text{ v}$

<table>
<thead>
<tr>
<th>Case</th>
<th>$t_d$</th>
<th>$t_r$</th>
<th>$t_s$</th>
<th>$t_f$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real Circuit</td>
<td>5.5</td>
<td>13.0</td>
<td>5.0</td>
<td>35.0</td>
</tr>
<tr>
<td>SPICE2-TFM</td>
<td>9.5</td>
<td>14.5(12%)</td>
<td>5.0(0%)</td>
<td>42.5(21%)</td>
</tr>
<tr>
<td>SPICE2-PMM</td>
<td>3.0</td>
<td>11.5(12%)</td>
<td>5.5(10%)</td>
<td>31.5(10%)</td>
</tr>
</tbody>
</table>

Variation 3:  $V_{cc} = -1 \text{ v}$

<table>
<thead>
<tr>
<th>Case</th>
<th>$t_d$</th>
<th>$t_r$</th>
<th>$t_s$</th>
<th>$t_f$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real Circuit</td>
<td>2.0</td>
<td>20.0</td>
<td>40.0</td>
<td>95.0</td>
</tr>
<tr>
<td>SPICE2-TFM</td>
<td>7.0</td>
<td>19.0(5%)</td>
<td>10.5(74%)</td>
<td>69.5(27%)</td>
</tr>
<tr>
<td>SPICE2-PMM</td>
<td>1.0</td>
<td>15.0(25%)</td>
<td>15.0(63%)</td>
<td>82.0(14%)</td>
</tr>
</tbody>
</table>
Variation 4: $R_s = 600\Omega$

<table>
<thead>
<tr>
<th>Case</th>
<th>$t_d$</th>
<th>$t_r$</th>
<th>$t_s$</th>
<th>$t_f$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real Circuit</td>
<td>0.0(^1)</td>
<td>5.0</td>
<td>10.0</td>
<td>20.0</td>
</tr>
<tr>
<td>SPICE2-TFM</td>
<td>0.0(^1)</td>
<td>4.0(20%)</td>
<td>2.5(75%)</td>
<td>37.5(88%)</td>
</tr>
<tr>
<td>SPICE2-PMM</td>
<td>0.0(^1)</td>
<td>0.5(^2)</td>
<td>86.5(77%)</td>
<td>21.0(5%)</td>
</tr>
</tbody>
</table>

Variation 5: $R_c = 62\Omega$

<table>
<thead>
<tr>
<th>Case</th>
<th>$t_d$</th>
<th>$t_r$</th>
<th>$t_s$</th>
<th>$t_f$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real Circuit</td>
<td>2.0</td>
<td>200.0</td>
<td>50.0</td>
<td>200.0</td>
</tr>
<tr>
<td>SPICE2-TFM</td>
<td>7.5(^{-})</td>
<td>40.0(80%)</td>
<td>5.0(90%)</td>
<td>60.0(70%)</td>
</tr>
<tr>
<td>SPICE2-PMM</td>
<td>0.0(^1)</td>
<td>1.0(100%)</td>
<td>58.0(16%)</td>
<td>10.5(95%)</td>
</tr>
</tbody>
</table>

\(^1\) Note that 0.0\(^1\) indicates that the output voltage was at 10% of the saturation value before the input voltage had risen to 90% of $V_1$. Thus no delay was experienced from the circuit.

\(^2\) Note that this Rise Time is inaccurate because the 0.0 Delay Time affected the starting point for $t_r$.

Although the previous results showed where the SPICE2 models were yielding moderate accuracy, the results of variation 5 indicated that the models failed to represent this circuit. With $R_c$ at 62\(\Omega\), the minimum value of $V_{ce}$ was measured at 0.57 v (0.52 v for the circuit without the SBD). This large value indicates that the transistor may not have fully saturated. Since both SPICE2 models yielded
significant errors for the particular circuit, a link between model accuracy and the degree of saturation may exist.

The data presented so far can be clarified if the total response times are compared. The total response time has been defined as the algebraic sum of the four response times. These values have been computed with the percentage error comparison in Table 5.6.

Table 5.6 Total Response Time Error Analysis for the Single-Stage Inverter Circuit.

<table>
<thead>
<tr>
<th>Variation #</th>
<th>SPICE2-TFM</th>
<th>SPICE2-PMM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Original Circuit</td>
<td>11%</td>
<td>6%</td>
</tr>
<tr>
<td>Variation 1</td>
<td>12%</td>
<td>0%</td>
</tr>
<tr>
<td>Variation 2</td>
<td>22%</td>
<td>12%</td>
</tr>
<tr>
<td>Variation 3</td>
<td>32%</td>
<td>28%</td>
</tr>
<tr>
<td>Variation 4</td>
<td>26%</td>
<td>210%</td>
</tr>
<tr>
<td>Variation 5</td>
<td>75%</td>
<td>85%</td>
</tr>
</tbody>
</table>

This comparison shows that when both models are within the margin of 25% error, the Physical Measurement model is more accurate than the Transfer Function model for simulating total response time. This is shown in the original circuit and in variations 1 and 2. However, both models failed to adequately simulate the total response times for variations 4 and 5.

Although variations 4 and 5 brought erroneous results,
these cases are very exceptional. $R_s = 600\Omega$ yields a base current, $I_b$, of 7.2 mA; $R_c = 62\Omega$ yields a collector current at saturation, $I_{CS}$, of 81 mA. Yet both SPICE2 BJT models were developed for values of 1.3 mA and 13 mA, respectively. Thus the simulation had to extrapolate from the SPICE2 models to determine the I-V characteristics of the BJT's. So the accuracy of the results may have been altered. Hence, the SPICE2 models may lose accuracy when they are used outside of the designed operation conditions as were the cases when $R_s = 600\Omega$ and $R_c = 62\Omega$.

So the SPICE2 Schottky Transistor model was used to simulate six different Single-Stage Inverter circuits to inspect the accuracy of the models. The results indicated that the SPICE2 results were adequate in three of the circuits; for these the BJT model derived from the Physical Measurements Method yielded the best results. Data from two of the other three circuits were invalid because the range of the models was exceeded. So in order to further explore the accuracy of the models, circuit configurations other than the Single-Stage Inverter are examined.

5.4 Other Circuits

While variations of the Single-Stage Inverter circuit offered proof that the SPICE2 model for the Schottky
Transistor was valid, the models were applied to other circuit configurations to further verify the performance of the simulation capability. These other circuits were the Two-Stage Buffer circuit and the Inverter Buffer circuit which uses five transistors. These circuits were simulated with SPICE2, and the response time results were compared to measured values by allowing the 75% tolerance margin described in Section 5.2. From this comparison the SPICE2 models are further assessed.

The Two-Stage Buffer circuit shown in Figure 5.1 is really two Single-Stage Inverter circuits staged together. SBD's were used to form Schottky Transistors out of both $Q_1$ and $Q_2$. Both of these transistors saturate to the same degree as the transistor of the original Single-Stage Inverter circuit.

The response times were measured from this circuit and obtained using SPICE2 simulation results. As before, BJT models developed by both the Transfer Function Method and the Physical Measurements Method were used. The results in ns are listed in Table 5.7.
Figure 5.1 The Two-Stage Buffer Circuit.
Table 5.7 Modeling Method Comparison for the Two-Stage Buffer Circuit.

<table>
<thead>
<tr>
<th>Case</th>
<th>$t_d$</th>
<th>$t_r$</th>
<th>$t_s$</th>
<th>$t_f$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real Circuit</td>
<td>20.0</td>
<td>120.0</td>
<td>45.0</td>
<td>27.0</td>
</tr>
<tr>
<td>SPICE2-TFM</td>
<td>25.5(28%)</td>
<td>76.0(37%)</td>
<td>26.0(42%)</td>
<td>14.5(46%)</td>
</tr>
<tr>
<td>SPICE2-PMM</td>
<td>19.5(3%)</td>
<td>75.0(38%)</td>
<td>22.0(51%)</td>
<td>22.0(19%)</td>
</tr>
</tbody>
</table>

The total response times were also computed in ns with the percentage error comparisons listed in Table 5.8.

Table 5.8 Total Response Time Error Analysis for the Two-Stage Buffer Circuit.

<table>
<thead>
<tr>
<th>Case</th>
<th>Total Response Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real Circuit</td>
<td>212.0</td>
</tr>
<tr>
<td>SPICE2-TFM</td>
<td>142.0 (33%)</td>
</tr>
<tr>
<td>SPICE2-PMM</td>
<td>138.5 (35%)</td>
</tr>
</tbody>
</table>

The data shows that SPICE2 simulation of the Two-Stage Buffer circuit also offered only moderate accuracy with either BJT model. By examining the total response time data, the SPICE2 BJT model developed using the Transfer Function Method proves just as accurate as the Physical Measurements Method model. However, neither model could offer the 75% accuracy that was desired for this circuit. But the total response time results could be simulated to within 65%.
The last circuit configuration to be simulated with SPICE2 was the Inverter Buffer circuit shown in Figure 5.2. This five-transistor circuit contains four Schottky Transistors. $Q_4$, the regular BJT, is used as an emitter follower. The response times for the circuit were measured and compared to those offered by SPICE2 simulation results. Again, both models were used by SPICE2. The results of this comparison in ns along with the error analysis are listed in Table 5.9.

<table>
<thead>
<tr>
<th>Case</th>
<th>$t_d$</th>
<th>$t_r$</th>
<th>$t_s$</th>
<th>$t_f$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real Circuit</td>
<td>13.0</td>
<td>17.0</td>
<td>12.0</td>
<td>35.0</td>
</tr>
<tr>
<td>SPICE2-TFM</td>
<td>10.5(19%)</td>
<td>12.5(26%)</td>
<td>11.5(4%)</td>
<td>37.0(6%)</td>
</tr>
<tr>
<td>SPICE2-PMM</td>
<td>2.5 -</td>
<td>12.0(29%)</td>
<td>12.0(0%)</td>
<td>42.0(20%)</td>
</tr>
</tbody>
</table>

The total response times in ns were calculated with the percentage errors as shown in Table 5.10.
Figure 5.2 The Inverter Buffer Circuit.
So from the data, the total response times for the Inverter Buffer circuit could be simulated within the 75% margin of accuracy by SPICE2 using either model.

To further indicate the accuracy of the SPICE2 models, the Two-Stage Buffer circuit and the Inverter Buffer circuit were simulated. Obtaining the total response times from both the Transfer Function Method model and the Physical Measurement Method model, the results were compared to circuit measurements. This comparison is summarized in Table 5.11 by listing the percentage error for each case.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>SPICE2-TFM</th>
<th>SPICE2-PMM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Two-Stage Buffer</td>
<td>33%</td>
<td>35%</td>
</tr>
<tr>
<td>Inverter Buffer</td>
<td>7%</td>
<td>11%</td>
</tr>
</tbody>
</table>

From this analysis the Transfer Function Method for determining the parameter values for the SPICE2 BJT model is
as accurate as the Physical Measurement Method. But neither model could guarantee the 75% accuracy tolerance as desired. 65% was the best that could be offered. While these results seem to conflict somewhat with the results of Section 5.3 which showed less accuracy particularly with the Transfer Function Method, an overall explanation is offered next in Section 5.5.

5.5 Summary

In this chapter, the BJT models and the SBD model presented in Chapters III and IV, respectively, were used by SPICE2 to analyze various circuits. From this the accuracy of the models were determined. While a certain tolerance of error was allowed, discrepancies beyond this margin were examined to investigate the errors. From the remaining data, the two modeling methods of Chapter III were compared to determine their performances. The results of the comparison were then summarized.

The SPICE2 SBD model, BJT model developed by the Transfer Function Method, and BJT model developed by the Physical Measurements Method were all used to simulate the Schottky Transistor in various applications. Comparing the total response times of the simulation results to those of measurements made on the circuits, the accuracy of the
models was assessed. The results showed that the models could achieve 65% accuracy. However, the error could increase if the models were used to simulate circuits where the base current or collector current were much greater than 1.3 mA and 13 mA, respectively. But the results did indicate that the Transfer Function Method was as successful as the Physical Measurements Method. The significance of these results is reviewed in the next Chapter.
Since transient simulation of the Schottky Transistor was desired, SPICE2 models were developed for its two device components. One component, the Schottky Barrier Diode (SBD), can readily be modeled by SPICE2. The second component, the Bipolar Junction Transistor (BJT), offers greater difficulty because of the complexity of the device (a large number of parameters which must be incorporated in the appropriate SPICE2 model). Although the conventional method for evaluating these parameter values was used, another method was presented to reduce this complexity. The two methods were compared. Each method yielded SPICE2 models for the Schottky Transistor of equivalent accuracy.

When a BJT is used as a digital switch, four delay times limit the switching speed. The most critical of these times is the Storage Time which occurs as the BJT begins to move from the saturation region to the cutoff region. This time may be an order of magnitude greater than the other delay times. The largest component of the Storage Time is the time required for the BJT to leave saturation and enter the active region (a necessary interval before cutoff can be reached). This requires that excess charges stored in the base region be removed. In order to prevent the BJT from
entering the saturation region, thus to minimize the Storage Time and to increase the switching speed, a SBD is connected between the base and the collector of the BJT. This connection results in the Schottky Transistor.

Obviously, applications with the Schottky Transistor are speed oriented. While the exact values for the four response times (the delays) can be calculated from circuit component values and device characteristics, the complexity of the mathematics and size of the circuit may make the calculations difficult and impractical. Thus an iterative approach is required which usually requires a computer for speed and accuracy for the large number of calculations. Several computer programs have been developed for circuit modeling. One of these programs is SPICE2 which is well suited for transient analysis offering general capabilities at moderate computational speeds.

SPICE2 can readily incorporate linear components such as resistors, capacitors, and inductors into simulation models. Nonlinear components require more complex modeling. For the SPICE2 BJT model and the SPICE2 Diode model, nonlinear equations parallel the I-V and the C-V characteristics of the devices. The constants of the equations which would vary among individual components are left as adjustable parameters for the user. So the nonlinear models are used by determining values for these
SPICE2 parameters; the selection of these values affect the accuracy of the simulation results. Thus the main difficulty of using SPICE2 and the focus of this research was the determination of parameter values to give the Schottky Transistor model acceptable accuracy.

The SPICE2 BJT model was derived from the Ebers-Moll model. 16 parameters allowed a wide range of BJT's to be modeled. The major problem was finding a dependable and accurate method for determining corresponding parameter values for the 2N3904 BJT. The conventional method used to evaluate the 16 SPICE2 parameters used data obtained from experimental results. This method was referred to as the Physical Measurements Method. From measurements of such physical properties as current gains, contact resistances, and junction capacitances, values were calculated for the parameters. Using these values, simulations were conducted on the Single-Stage Inverter circuit yielding the estimated response times. Summing the four response times in order to determine the total response time, the simulation results were compared to measured response times and found to agree to 84%. This accuracy even exceeded the desired accuracy of 75% for SPICE2 which was estimated from anticipated measurement errors and version discrepancies.

In addition, an alternative method was presented and compared to the results from the previous simulations. This
method was referred to as the Transfer Function Method. In this method, the Single-Stage Inverter circuit was simulated as a system. The input to the system was the 16 parameter values of the SPICE2 BJT model. The system output was the four response times. A set of linear equations could be developed describing the response times as linear functions of the parameters. The coefficients of these linear functions were determined by perturbations. Adopting matrix algebra to represent the equations and then inverting the coefficient matrix, the Transfer Function Method derived a new set of parameter values from a particular set of goal response times. The goal response times had been previously determined as the average of response time measurements taken from a sample of BJT's in a Single-Stage Inverter circuit. An iterative process was required for all 16 parameter values to be assessed. The Transfer Function Method for the BJT model allowed the SPICE2 simulation results to achieve 99% accuracy.

The development of the SPICE2 Schottky Transistor model was completed by modeling the SBD. The SPICE2 diode model was used for this purpose with slight modifications. As was the case for the SPICE2 BJT model, the Diode model offered the user parameters to characterize particular diodes. The I-V and C-V data obtained from the manufacturer's specification sheet for the HP 5082-2800 diode were curve
fitted into appropriate mathematical expressions in order to find the 8 parameters needed. Simulation results were obtained and compared to the measured response times, and they were found to yield 29% accuracy.

Two SPICE2 models for the Schottky Transistor were actually presented. One model used the Physical Measurements Method for the BJT model; the second model used the Transfer Function Method. Both models shared the same SBD model. The two models were then compared in various applications to determine which was superior in performance and the degree of accuracy SPICE2 simulation would offer.

Three different circuit applications were tested where digital switching was applicable. The first application was a set of six Single-Stage Inverter circuits with each being slightly different from the rest. SPICE2 simulation results were erroneous with two of these circuits because current values through the BJT greatly exceeded those to which both models were designed for. Neglecting these two Single-Stage Inverter cases, all of the simulated total response times matched actual values by a margin of 65% accuracy. Although an accuracy margin of 75% was desired, results proved that both BJT models simulated to the same degree of accuracy in all cases (even the two erroneous cases). Thus the Physical Measurements Method and the Transfer Function Method were equally successful for contributing to the SPICE2 Schottky
Transistor model. This model provided results accurate to within 65%.

While data indicated that either the Physical Measurements Method or the Transfer Function Method could be used to evaluate the 16 parameters of the SPICE2 BJT model, the two methods differed greatly. The Physical Measurements Method correlated the physical significance of the SPICE2 BJT model to characteristics measured for particular BJT's. Although no computer time was required, these measurements were tedious requiring several days to manually perform and were with questionable accuracy. The data then had to be averaged to provide a generalized model for the BJT. This method was recommended by people experienced with SPICE2 [4].

The Transfer Function Method was developed to avoid the extensive data measurement process. The desired response characteristics were measured from a test circuit. These measurements required only a few hours, but then several days of computer simulation were required for the iteration process which evaluated the 16 parameters. The values of the 16 parameters differed greatly between the two methods; the simulation results were of equal accuracy. The Transfer Function Method replaces the physical consideration of the BJT model with numerical analysis to achieve an accurate net result of desired response characteristics for a particular
test circuit. The method could be totally automated with the desired response characteristics as input. This preliminary research has so far shown that this method can be used as an equivalent replacement for the Physical Measurements Method.

But more research needs to be conducted to further evaluate the Transfer Function Method. The method itself could be improved by including more response characteristics. This would create more accurate response curves for the simulation results. Also, the more constraints that are given corresponds to more parameter values that can be solved simultaneously. This reduces the number of iterations required. The linear algebra could also be improved to incorporate inequality constraints such as parameter values being positive. A detailed algorithm could be developed which offers explicit, programmable steps for the process.

The SPICE2 simulation results offered by the Transfer Function Method need to be further examined. Many more digital circuits need to be simulated. A temperature analysis should be conducted. Circuits offering various current levels to the BJT should also be attempted. The method could also be applied to frequency response analyses to further determine domain limitations.

In summary, a SPICE2 model was desired for the Schottky
Transistor to allow for accurate simulation of circuit applications using this device. Such a model was presented using conventional methods. The model yielded a 65% accuracy margin. But due to the complexity of developing a portion of the model, a new method was presented and used to complete the SPICE2 model. This alternative model also offered a 65% accuracy margin for the simulation results. The method needs to be further improved and tested. But it offers a distinct advantage over the conventional method; it is simpler to use making SPICE2 a more powerful tool to the design engineer.
REFERENCES


APPENDIX A

SPICE2 SIMULATION DATA FOR THE SINGLE-STAGE INVERTER CIRCUIT
Figure A.1 The Single-Stage Inverter Circuit.
Source File for the Single-Stage Inverter Circuit

SSI  SINGLE-STAGE INVERTER CIRCUIT WITH SBD  (PM MODEL)
*  
* FOR THE CIRCUIT COMPONENTS
RS  1 2  3.31K
RC  4 5  364
V_SUPPLY  5 0  DC  5
C_SUPPLY  5 0  3500U
VIN  1 0  PULSE ( 0 5  500N 7N 11.5N 1.U )  
*  
Q1  4 2 0  QMOD
  .MODEL QMOD NPN (BF=170 BR=0.6 RB=13.2 RC=1. RE=2.5 CCS=0.
+ TF=58.2P TR=282N CJE=2.21P CJC=2.57P IS=1.E-12 PE=2. PC=2.
+ EG=1.11 ME=1.81 MC=0.802)
*  
* FOR THE COMPONENT SOCKETS
C_BC  2 4  1.0P
C_BE  2 0  0.5P
C_CE  4 0  0.5P
*  
* FOR THE OSCILLOSCOPE PROBE
R_PROBE  4 6  76.3
L_PROBE  6 7  188N
C_PROBE  7 0  14.0P
*  
* FOR THE SBD
C_PACKAGE  2 4  0.25P
L_PACKAGE  3 4  3.0N
D1_SBD  2 3  DMOD
  .MODEL DMOD D (RS=21. TT=0. CJO=1.47P IS=39.N PB=0.4010
+ EG=0.69 M=0.5 N=1.462)
*  
* FOR THE ANALYSIS
  .OPTIONS (LIMPTS=5000 ITL5=50000 TNOM=25 NUMDGT=7)
  .DC VIN  0 5  5
  * V(1) IS V_IN  V(4) IS V_OUT
  .PRINT DC V(1)  V(4)  V(2,4)  V(2)
  *  
  .TRAN  0.5N  2.0U
  .PRINT TRAN V(1) V(4)
  .CALPLT TR  2
  .END
Figure A.2 SPICE2 Simulation Results for the Single-Stage Inverter Circuit.
APPENDIX B

SPICE2 SIMULATION DATA FOR THE
TWO-STAGE BUFFER CIRCUIT
Figure B.1 The Two-Stage Buffer Circuit.
TSBC  2-STAGE BUFFER CIRCUIT WITH SBD  (PM MODEL)  
*  
*  FOR THE CIRCUIT COMPONENTS  
RS1  1  2  3.3K  
RS2  3  5  3.3K  
RC1  3  4  360  
RC2  4  6  360  
V_SUPPLY  4  0  DC  5  
C_SUPPLY  4  0  320U  
VIN  1  0  PULSE ( 0  5  500N  7.5N  7.5N  1.U )  
*  
XQ1  3  2  0  ST  
XQ2  6  5  0  ST  
*  
*  FOR THE SCHOTTKY TRANSISTOR  
.SUBCKT ST  3  2  1  
Q  3  2  1  QMOD  
.MODEL  QMOD  NPN  (BF=170  BR=0.6  RB=13.2  RC=1.  RE=2.5  CCS=0.  
+  TF=58.2P  TR=282N  CJE=2.21P  CJC=2.57P  IS=1.E-12  PE=2.  PC=2.  
+  EG=1.11  ME=1.81  MC=0.802)  
*  
*  FOR THE SBD  
C_PACKAGE  2  3  0.25P  
L_PACKAGE  3  4  3.0N  
D1_SBD  2  4  DMOD  
.MODEL  DMOD  D  (RS=21.  TT=0.  CJO=1.47P  IS=39.N  PB=0.4010  
+  EG=0.69  M=0.5  N=1.462)  
.ENDS  
*  
*  FOR THE OSCILLOSCOPE PROBE  
R_PROBE  6  7  76.3  
L_PROBE  7  8  188N  
C_PROBE  8  0  14.0P  
*  
*  FOR THE ANALYSIS  
.OPTIONS  (LIMPTS=5000  ITL5=50000  TNOM=25  NUMDGT=7)  
.DC  VIN  0  5  5  
*  
V(1)  IS  V_IN  V(6)  IS  V_OUT  
.PRINT  DC  V(1)  V(6)  
.TRAN  0.5N  2.0U  
.PRINT  TRAN  V(1)  V(6)  
.CALPLT  TR  2  
.END
Figure B.2 SPICE2 Simulation Results for the Two-Stage Buffer Circuit.
APPENDIX C

SPICE2 SIMULATION DATA FOR THE INVERTER BUFFER CIRCUIT
Figure C.1 The Inverter Buffer Circuit.
Source File for the Inverter Buffer Circuit

IBC  INVERTER BUFFER CIRCUIT WITH SBD  (PM MODEL)
*
* FOR THE CIRCUIT COMPONENTS
R1    1 2  4.7K
R2    4 5  240
R3    4 6  120
R4    3 7  390
R5    9 0  3.3K
R6    7 8  25
V_SUPPLY 7 0 DC 5
C_SUPPLY 7 0 320U
VIN  1 0 PULSE ( 0 5 500N 7.5N 7.5N 1.U )
*
XQ1   3 2 4 ST
XQ2   6 5 0 ST
XQ3   8 3 9 ST
Q4    8 9 10 QMOD
.MODEL QMOD NPN (BF=170 BR=0.6 RB=13.2 RC=1. RE=2.5 CCS=0.
+ TF=58.2P TR=282N CJE=2.21P CJC=2.57P IS=1.E-12 PE=2. PC=2.
+ EG=1.11 ME=1.81 MC=0.802)
XQ5   10 4 0 ST
*
* FOR THE SCHOTTKY TRANSISTOR
.SUBCKT ST 3 2 1
Q  3 2 1 QMOD
.MODEL QMOD NPN (BF=170 BR=0.6 RB=13.2 RC=1. RE=2.5 CCS=0.
+ TF=58.2P TR=282N CJE=2.21P CJC=2.57P IS=1.E-12 PE=2. PC=2.
+ EG=1.11 ME=1.81 MC=0.802)
*
* FOR THE SBD
C_PACKAGE 2 3  0.25P
L_PACKAGE 3 4  3.0N
D1_SBD  2 4 DMOD
.MODEL DMOD D (RS=21. TT=0. CJO=1.47P IS=39.N PB=0.4010
+ EG=0.69 M=0.5 N=1.462)
.ENDS
*
* FOR THE OSCILLOSCOPE PROBE
R_PROBE 10 11  76.3
L_PROBE 11 12  188N
C_PROBE 12 0  14.0P
*
* FOR THE ANALYSIS
.OPTIONS (LIMPTS=5000 ITL5=50000 TNOM=25 NUMDGT=7)
.DC VIN 0 5  5
* V(1) IS V_IN    V(10) IS V_OUT
.PRINT DC V(1)  V(10)
.TRAN  0.5N  2.0U
.PRINT TRAN V(1)  V(10)
.CALPLT TR 2
.END
Figure C.2 SPICE2 Simulation Results for the Inverter Buffer Circuit.
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