# A TWO-PHASE BUCK CONVERTER OPTIMIZE BY
# ECHO STATE NETWORK

SHUANG CHENG

Thesis submitted to the faculty of the Virginia Polytechnic Institute and State University

in partial fulfillment of the requirements for the degree of

Master of Science

In

Electrical Engineering

Yang Yi, Chair

Dong S. Ha

Xiaoting Jia

December, 11 2018

Blacksburg, VA

Key Word: Two-phase buck converter,  Neural Network, Echo State Network, optimize efficiency

A Two-Phase Buck Converter Optimize by Echo State Network

Shuang Cheng

# Abstract

Buck converter is a power converter which drops high input voltage into a low output voltage in high efficiency. With this characteristic, it has been used in a great number of applications. Optimized the maximum load to increase the buck converter's efficiency at the cost of light load efficiency is a general way used in a traditional buck converter because it has a higher impact on power consumption. We propose a novel way of designing the two-phase buck converter with light load efficiency improvement in this thesis.

The purposed two-phase buck converter uses RC delay to control switch frequency. Different frequency will affect the buck converter in output value and efficiency. RC delay includes two parts; part one connect with phase one, part two connect with phase two. After the test, when resister's value of part one is 100kΩ, and the capacitor’s value is 50 pF, the resister’s value of path two is 40kΩ, and the capacitors' value is 50 pF, the buck converter can reach maximum efficiency.

The inspiration of the neural network is derived from the biological brain, neural is similar with the human neural, and the s “ynaptic weights can treat as the connection between two nodes. Reservoir computing can be seen as an extension of the neural network since it is a framework for computation. Echo State Network(ESN) is one of the major types of reservoir computing, and it is a recurrent neural network. Compared with a neural network, it only trains output weights, which can save a lot of time but keep the accuracy of the training at the same time.

The efficiency of the two-phase buck converter and power loss for each phase in the control scheme were measured. The input voltage set to be 30V, with the switch frequency change from

40 μs to 100 μs, the output voltages change from 9.2V to 6V, the output current range is 18 mA to 30 mA. The efficiency ranges are 94% to 98%. The teaching target set for the ESN is the output voltage of the two-phase buck converter. The ESN will read data from two-phase buck converter's simulation, including input voltage, the frequency of the switches and based on that to compute the output voltage.

A Two-Phase Buck Converter Optimize by Echo State Network

Shuang Cheng

# General Audience Abstract

Buck converter is a power converter which drops high input voltage into a low output voltage in high efficiency. With this characteristic, it has been used in a great number of applications. Most of the buck converter optimized the maximum load to increase the efficiency, however, it will also increase the power consumption of the buck converter. For this reason, we propose a novel way of designing the two-phase buck converter optimize with Echo State Network(ESN).

The inspiration of neural network is derived from the biological brain, similar with a human brain, the neural network also have self-learning ability. Reservoir computing is one kind of neural network, it can save more time on computing data and increase the efficiency at the same time. Compare with normal two-phase buck converter, the purposed two-phase buck converter optimize with ESN can increase the efficiency and also decrease the running time.

# Dedication

I would like to thank my advisor, Dr. Yang Yi, who has guided me and give me suggestions with her knowledge and professionalism. I would like to thank my colleagues, Chenyuan Zhao, Kangjun Bai, Qiyuan An, and Hongyu An. They helped me a lot during the thesis.

I would like to thank my parents and my boyfriend. They always support me during the graduate life. I would also like to thank all of my friends, they are my families at Blacksburg.

# Table of Contents

# List of Figure

# List of Tables

# List of Abbreviations

| | |
|---|---|
| P.I.D | Proportional Integral Derivative |
| PWM | Pulse-Width Modulation |
| NN | Neural Network |
| ESN | Echo State Network |
| COT | Continuous Conduction Mode |

# Chapter 1

# Introduction

## 1.1 Overview

Buck converter is a ubiquitous DC-DC converter that can convert a high voltage to a low voltage in high efficiency. With its high efficiency, less cost, buck converter has been used in many applications, such as laptops, keyboards, mice, and other connections of the smartphone. Besides these applications, buck converter also used in chargers, for example, battery charger and solar charges. The reason is efficient power conversion can extend battery life, reduces heat, and allows for smaller gadgets to be built. [1] Nevertheless, buck converter also has some inconvenience, such as high voltage ripples at the output, high peak current in semiconductors, also, when the buck converter is in a very small or a very large duty cycle, the converter's efficiency will become very small. To solve these problems, multi-phase buck convert had been designed.

The neural network can learn originally, which means that a neural network is not limited by the given inputs and outputs, it has the ability to generalize the inputs. Neural networks also have the ability to model non-linear and complex relationships, because, in real life, most relationships between inputs and outputs are non-linear and are very complex [2].

## 1.2 Specific Topics of the Thesis

Even though the buck converter has so many benefits, it still has some disadvantage, for example, when the input current is high, the power consumption will increase and the efficiency will decrease. Since the design limitation, when a high voltage needs to drop to a low voltage, more than one buck converter will be needed, which will increase power consumptions. For example, if an input voltage of 50V wants to drop to 1V, two buck converter will be needed, it first needs to drop 50V to 10V, then drops 10V to 1V. However, compared use only one buck converter, add more converters will have more components, which will occur more power dissipated. Two-phase buck converter can help solve these problems. Besides these benefits, two-phase buck converter can reduce ripple current and ripple voltage, and it also reduces the RMS current power dissipation in the transistors.

Traditional buck converter usually uses pulse-width modulation(PWM) controller or proportional-integral-derivative(PID) controller to control the switch. The benefits of PWM are it has high efficiency and lower initial cost, it also fits many applications. The advantage of a PID controller is that it is a straightforward method to find and control the parameters. Another advantage for PID controller is its feasibility and easy to be implemented, which make them the most frequently used control tools in the industry.

Though PWM and PID have many benefits and widely used in many applications, there still exits have some disadvantages. For example, the PWM controller is a non-regenerative operation, and if the switch in high frequency, it may cause motor heating and insulation breakdown. Otherwise, a PWM controller requires a large bandwidth as compared to an analog system.

PID controller usually needs to balance all three parameters impact on the entire system and may compromise the transient response. The designed PID gains may not resist the uncertainty and interference if the system parameters cannot be exactly estimated or achieved. [3] Also, a PID controller may amplificated of noise, abrupt changes in output upset operators. Moreover,

To avoid these, an RC delay with inverter has been designed to control switches of the two-phase buck converter. To optimized the output voltage and the efficiency, an ESN has also been applied on the two-phase buck converter.

Since ESN has self-learning ability, it will generate the output based on the input data. The steps of the process are, first, a dataset will be collected from the two-phase buck converter's simulation, and then, the ESN will read the dataset as input, and based on the input data to compute the output. After getting the output, ESN will check if the output is in the teaching target. A teaching target is a range of desired output. If the output is out of the teaching target, ESN will repeat the steps to calculate the output, until it is in the teaching. If the output is in the teaching target, then the process will be done.

The teaching target is set by the output voltage, by changing the frequency of the switches, the output voltage would be the difference. So the ESN will only check the output voltage to see if they are in the teaching target. By connecting an ESN with a two-phase buck converter, the efficiency will be increased, and the time will be decreased.

## 1.3 Organization of the Thesis

The thesis is organized as follows. Chapter 2 give the background of the buck converter, including introduction, principle, advantages, and disadvantages of the buck converter. Next section was introduction two-phase buck converter, what is the benefits of two-phase buck converter than single-phase buck converter. Analysis power dissipated of a two-phase buck converter in continuous conduction mode(COT). Introduce delay circuit of the two-phase buck converter, the principle of the delay circuit and how it works, analysis general loss in converter and efficiency improvement in the two-phase buck converter. Finally, components selection will be provided. Chapter 3, first, the background of neural will be provided, including working principle, advantages, and applications. Next is the introduction of reservoir computing, what is the difference with a neural network, and why it was used in this thesis. After that, ESN will be introduced, such as what is the special part for ESN and how to apply ESN to buck converter. Chapter 4 is a simulation and measurement result. In this section, the result of buck converter from the steady state will be provided, the comparison of two results from two-phase buck converter and ESN will also be provided and analyzed. The last part will draw a summary of the proposed system and how to improve it in future work.

# Chapter 2

## Buck Converter

### 2.1 Introduction of Buck Converter

Buck converter is a power converter which is mainly used to stepping down the voltage from its input to the output load. Figure 1 shows a general block diagram for a buck converter. The diode parallels with the MOSFET to ensure the current goes in the right direction. When the MOSFET is turned ON, a reverse input voltage will be applied across the power diode. Therefore, the ON state of MOSFET means the diode should be in OFF state. In other words, as long as the MOSFET is ON state, the diode must remain OFF. When the MOSFET turned on, inductor current $I_L$will accumulate exponentially due to the inductance L. MOSFET will keep on during Ton and keep off when it turned off. In this case, inductor current will have a peak value of the output current at the instant of MOSFET turns OFF.

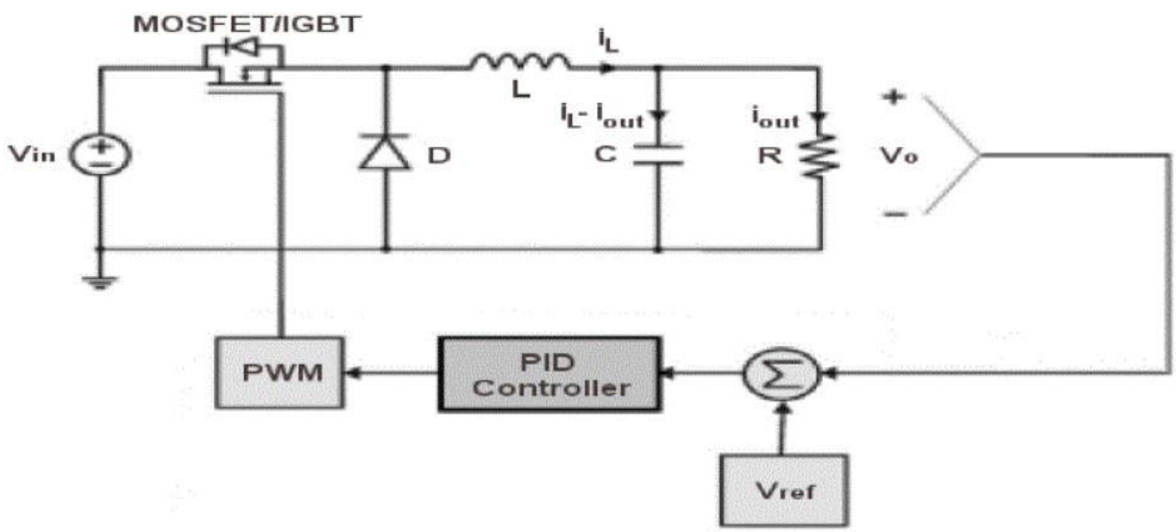


Fig. 2. 1: Voltage step down chopper with feedback controller. Source: Modelling of Buck DC-DC Converter Using Simulink, Mahesh Gowda N M, Yadu Kiran, Dr. S.S Parthasarthy

Inductance L is used to ensure the inductor current will not suddenly drop to zero. An induced voltage L $\frac{dil}{dt}$ across the inductance will appear because of the decay of $I_L$. The power diode becomes forward-biased because of the voltage and the current flow will also be continued and decayed exponentially. The term “Free-Wheeling” is commonly used to describe the flow of current in this manner without the aid of a voltage source, but solely due to the stored energy in the inductance. [4] When the MOSFET is turned off, the diode will provide a free-wheeling path for it. Due to the presence of an inductance with stored energy, the diode will automatically turn on at the instant when the MOSFET turns off. The decay of $I_L$ will continue as the MOSFET stay off, the duration of the decay is Toff. Figure 2 labeled the lowest value of the current falls at the end of the first cycle is $I_{V1}$. After the first cycle of MOSFET turns on and off, it will repeat the same process at the second cycle. The second period begins when the MOSFET has turned ON again at the end of the first period, and the current will again start to build up. However, during the second cycle, because of the initial current $I_{V1}$ was greater than the one at the first period, the second peak current will also be larger than the peak current of the first period. The waveform for initial current and peak current also shown in figure 2. The initial current and peak current will be continues increased with the switching progresses. After several cycles of the MOSFET on and off, the difference of voltage and peak current will be too small to count so that it can be ignored. And at that time, the system reaches a steady state, which means the peak current is the same in successive cycles. The relationship between the input voltage, output voltage, and the duty cycle is [3]:

$$v_{\text{out}} = v_{in} * D \tag{1}$$

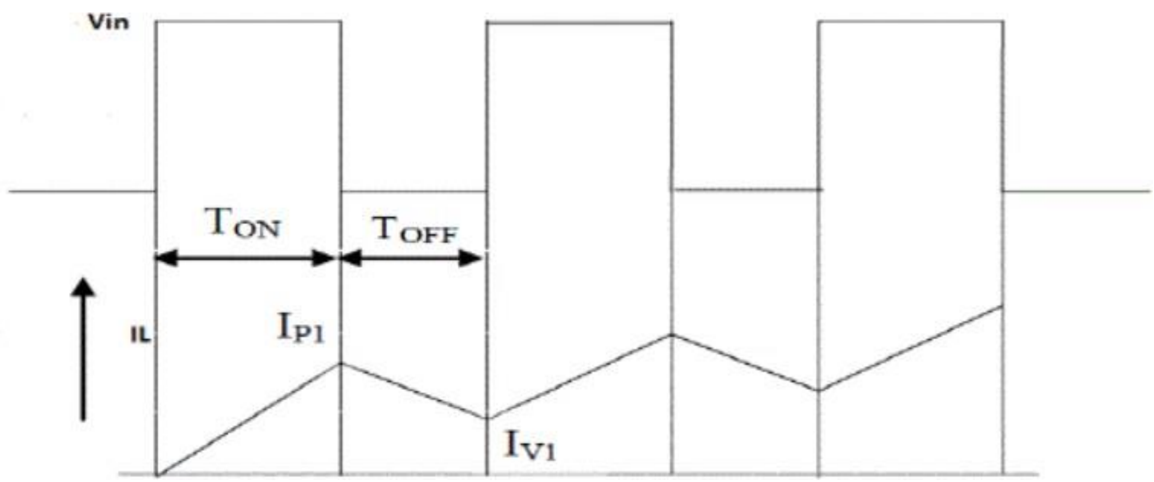


Fig. 2. 2: Output voltage and the current waveform. Source: Modelling of Buck DC-DC Converter Using Simulink, Mahesh Gowda N M, Yadu Kiran, Dr. S.S Parthasarthy

The PID controller is to generate the required duty cycle based on the error signal. P, I, and D parameters can be entered manually or tuned by using some tools such as Matlab. However, the forward path of the control loop is caused by the linearization of zero at same point dut to the PWM logic, which will further lead to linearization errors when attempting to run the tuning tool. [4]

Though single-phase buck converter work well for low-voltage in high efficiency, when either the voltage or current is high, the power dissipation and efficiency will become a problem. Compared with multi-phase buck converter, single-phase buck converter also has larger ripple current and current. To avoid these problems, a two-phase buck converter has been designed.

### 2.1.1Two-phase Buck Converter

The two-phase buck converter is parallel of a set of two buck power stage. Each power stage contains their own set of MOSFETs and inductors. This stage is called phase. These two phase share one input voltage, one output capacitor and loads. During the steady-steady operation, each phase is active at spaced intervals equal to 180° throughout the switching period. A basic diagram for two-phase buck converter as shown below. From the figure, $M_1$, $M_2$, $L_1$ are phase one, $M_3$, $M_4$, and $L_2$ are phase two, C is output capacitor, R is the output load.

In the purposed two-phase buck converter, only lower MOSFETs parallel with a power diode. Path C and Path D connected with the delay circuit. When the input current goes through the MOSFETs, because of the delay circuit, they will have a phase difference of 180º.

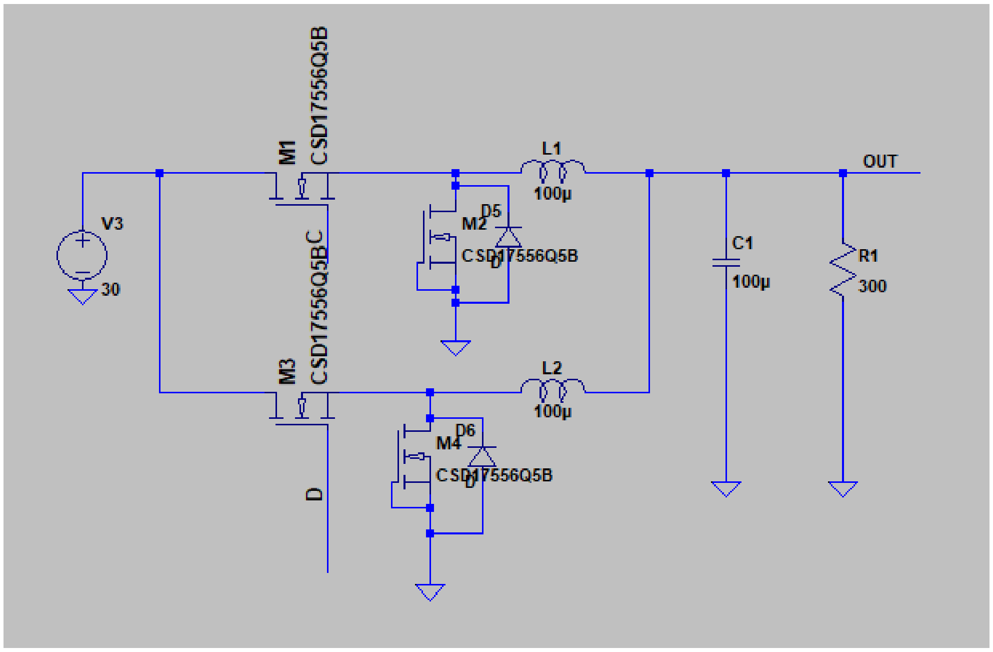


Fig. 2. 3: a Two-phase buck converter

Compared with single-phase buck converter, two-phase buck converter have several performance advantages for high – power and high-performance applications [5]:

a. reduced ripple voltage

Additional phases can decrease the RMS input current flowing through the decoupling capacitors, therefore, the ripple input voltage will be reduced. Since that, to keep the input ripple voltage within specifications, fewer capacitors are needed. Due to equivalent series resistance, ESR and self-heating effects within the capacitors themselves are also reduced.

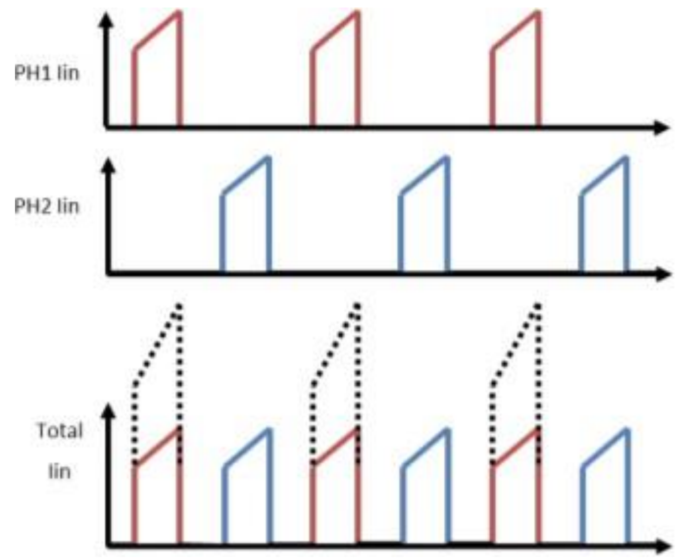


Fig. 2. 4: Input Current waveforms. Source: Carmen Parisi, “Multiphase Buck Design from Start to Finish (part 1),” Texas Instruments Application Report, April 2017.

Figure 4 shows the input current waveforms for a two-phase buck converter compared to a single-phase one. The dashed line is single-phase buck converter's input current. The input ripple current is higher than the two-phase buck converter's. RMS current is also lower than single-phase buck converter. Besides reduce RMS, the second phase also let the upper MOSFET of each phase have less stress.

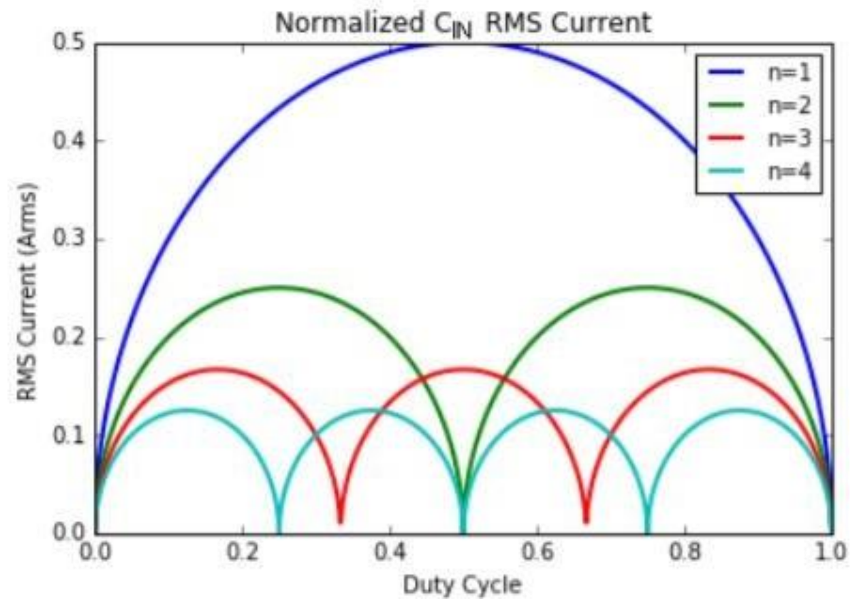


Fig. 2. 5: Normalized Input Capacitance RMS Current. Source: Carmen Parisi, "Multiphase Buck Design from Start to Finish (part 1)," Texas Instruments Application Report, April 2017.

Figure 5 shows the normalized input capacitance RMS current in a different phase, it is easy to see that with more phases added, the RMS current become less, this is because of the cancellation of each individual ripple current of each phase. Ideally, for more phase, the RMS current will drop to zero because of the cancellation, but it is impossible to achieve. There are many reasons, such as noise, line transients, load transients, and natural variations, all of these in the duty cycle make it no possible to realizable in real life, especially when the phase number is higher 4. So that in this thesis, a two-phase buck converter is used.

b. Reduced ripple current

The current for two-phase buck converter is interleaved, figure 6 below shows how it works. Two-phase buck converter has the intrinsic time-interleaved operation, with this operation, the ripple current was cancelled. Smaller ripple current through the output capacitor will decrease the output ripple voltage. To keep output voltage within tolerance, the amount of capacitance will also reduce.

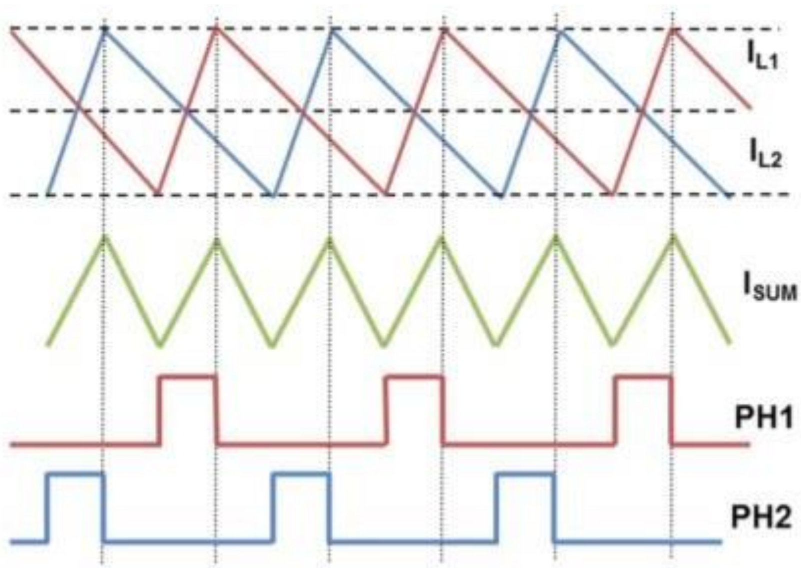


Fig. 2. 6: Inductor Ripple Current Waveforms. Source: Carmen Parisi, “Multiphase Buck Design from Start to Finish (part 1),” Texas Instruments Application Report, April 2017.

Since each phase has the same components, and they share the same input source, the input current will split equally into two phases. For example, if the input current is 10A, in a two-phase buck converter, the current through each phase is only 5A. So the current delivered to each inductor is only 5A. Both inductance and inductor are reduced because of the lower current.

c. Improvement thermal performance and efficiency

In a single-phase buck converter, all components are in one phase, which means all of the input currents will go through these components and the power loss is focus on these components. When the input current reaches a really high value, it will be very hard for MOSFETs and inductors to reach such a large current, otherwise, the components satisfied the requirement is very expensive. Since all the components are in the same phase, the efficiency of the buck converter will also be increased.

Since two-phase buck converter is parallel two same phases, the input current split equally into two phases, similar with the input current, power loss is also spread evenly through each phase. In this way, current flow to each component will be reduced, which the thermal strain placed on each component is also reduced. As mentioned before, reduced input and output capacitor have also reduced the self-heating and power loss for the capacitors, so that the efficiency and performance of the buck converter will also increase.

The relationship between ripple current, output ripple voltage, and the external LC components are shown below.

$$\Delta I_0 \approx \frac{V_0}{f_{sw} \cdot L_0}\left(1 - \frac{V_0}{V_i}\right) \tag{2}$$

$$\Delta V_0 \approx \Delta I_0\left(\frac{v_0}{8f_{sw} \cdot C_0} + R_{esr}\right) \tag{3}$$

Where $\Delta V_0$ is the output ripple voltage, $V_0$ is the output voltage, $\Delta I_0$ is the ripple current, $V_i$ is the input voltage, $L_0$ is the output inductance, $f_{sw}$ is the switching frequency, $C_0$ is the output capacitor, and $R_{esr}$ is the ESR of the output capacitor. [6]

Different current needs a different number of phases, at low current, fewer phases are used. With the current increase, conduction loss will be higher than switching loss, so that more phases needed to keep the converter in high efficiency. In this thesis, the current is about 18 mA, so two-phase is enough for the converter.

d. Improve transient response

the required capacitance requirement for load transients are much greater than the capacitance requirement required to successfully achieve DC ripple targets, and this occurs in many high-performance applications. In order to achieve a given design that maintains output voltage with the specification, a multiphase buck converter is required. The reason for multiphase bucker is it has the characteristics of it required less output capacitance in the load conversion device.

In transient, in order to effectively parallel the inductors together, during the load step, the multiphase controller will overlap phase, or it will turn of fall phase during load release. And it will reduce equivalent inductance, called LEQ, have a relationship of the total number of phase. Since the smaller LEQ, when the phase is completely turned off, the excess charge stored in the appliance is transferred to the output capacitor, thus reducing the overshot. Similarly, reducing the undershoot is due to the quick charge of smaller LEQ from the supply to the output capacitors.

### 2.1.2 Challenges for Multiphase Converter

Even multiphase converter has such more benefits, it still has some challenges to make it works. By adding more phases, buck converter will need more components, that will increase the cost. Moreover, if the buck converter is designed in a PCB board, more phases also need more areas, how to design it in a minimize area will be a problem. The third challenge for the multiphase converter is how to manage each phase. To reach the highest efficiency and performance, the current goes through each phase should be equal to each other, so that the thermally stressing for each phase will reach an optimal ripple cancellation.

## 2.2 Delay Circuit Design in Buck Converter

Compared traditional buck converter using a PID controller or PWM controller, to avoid the disadvantage of these two controllers, the purposed two-phase buck converter uses an RC delay circuit instead. A diagram of RC delay shows below, it contains two parts, part one is the upper part shows in the figure who connect with phase one, part two is the lower part of the diagram connect with phase two. Part two is connected with part one after the voltage goes through path C, it will keep going through part two.

For the delay circuit, each part has even number of inverters, the reason is each inverter will invert the current phase in 180 degrees, even number of the inverter will ensure the circuit stay in the same direction.

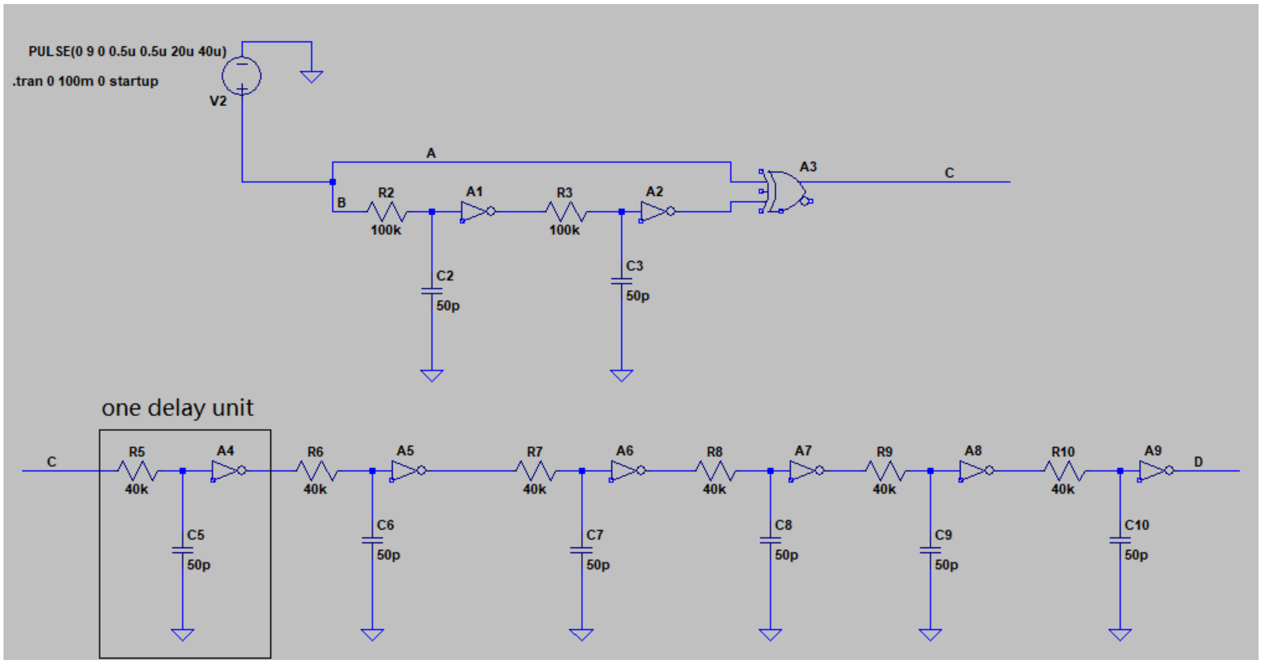


Fig. 2. 7: Diagram of RC delay.

Set a resistor, a capacitor and an inverter as one delay unit, shows in the black squire in figure 7. There are two units for part one and six units for part two. Voltage through path A is the input voltage, the voltage through path B will delay, delay time determined based on the resister and capacitor's value, which called $\tau$. The equation for $\tau$ is:

$$\tau = RC \qquad (4)$$

Where R is the resistor in Ω and C is a capacitor in Farads. Delay time can be adjusted by changing the value of resistor and capacitor.

In part one, an XOR gate is connected with path A and path B to generate a new duty cycle. For an XOR gate, if one of the input is exactly true, the output will be true, if both inputs are true or both inputs are false, the outputs will be false. Table 1 is the truth table for XOR gate, figure 8 is the waveform of the XOR gate. The XOR gate is used to generate a new duty cycle for the delay circuit.

| Inputs | | Outputs |
|---|---|---|
| X | Y | Z |
| False | False | False |
| False | True | True |
| True | False | True |
| True | True | False |

Table 2. 1: Truth table for the XOR gate.

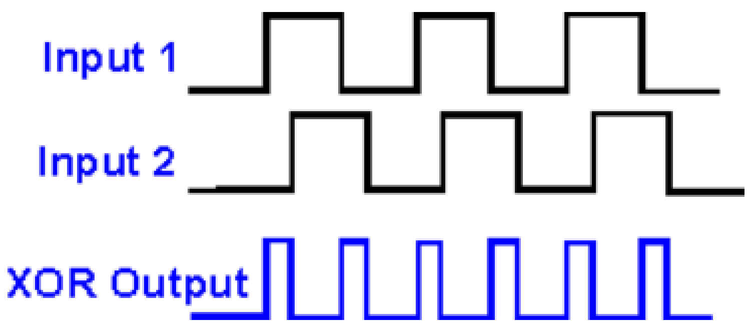


Fig. 2. 8: XOR phase detector waveforms. Source: I. Poole, "PLL Phase Detector / Comparator," Op Amp Gain | Operational Amplifier Calculation Equations | Radio-Electronics.com.

The two-phase buck converter is interleaved, which means two-phase turns on in a different time, that will make current also have a time difference. Therefore, only one delay circuit is not enough, another delay circuit is needed to let phase two's current interleaved with phase one. Path D was designed for this reason, there are six delay units in path D.

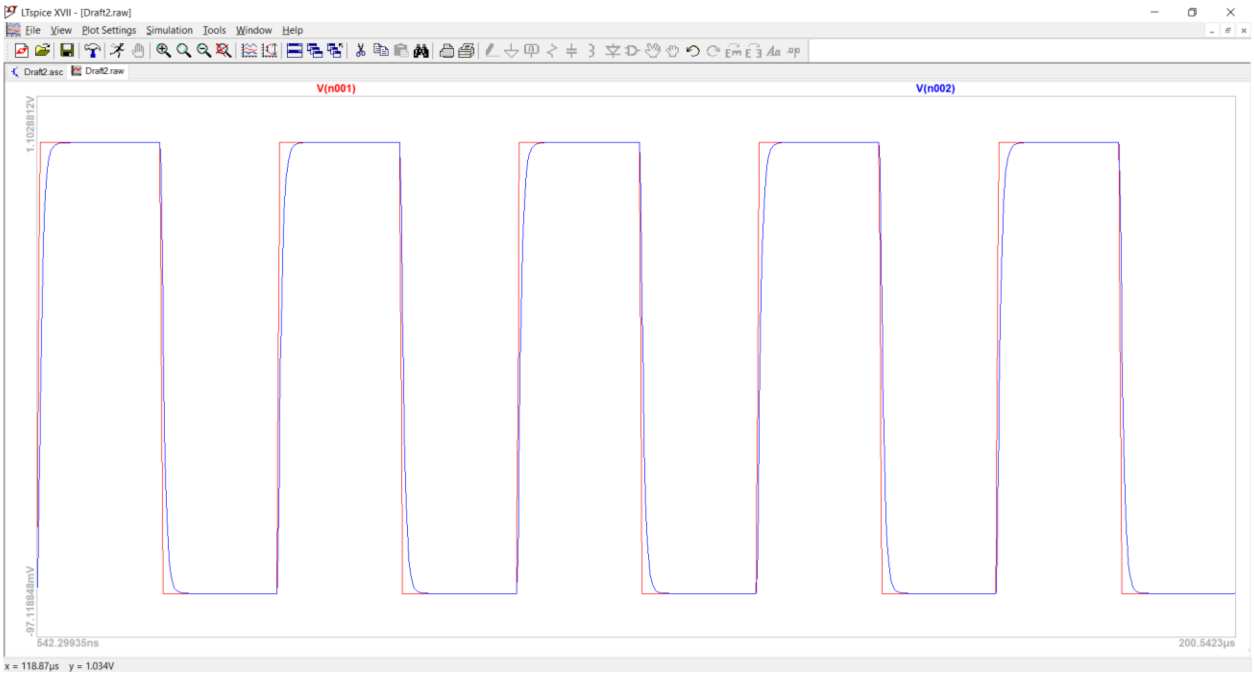


Fig. 2. 9: RC circuit waveform

Figure 9 shows the RC circuit waveform when the capacitor is fully charging. The blue square waveform is input voltage, the red on is the capacitor's output voltage. Since fully charge of a capacitor cannot finish instantaneously, it will need time to fully charge, the relationship between current and time is

$$I = \frac{\Delta Q}{\Delta t} \tag{5}$$

So the period after the delay circuit will actually decrease. To avoid this problem, more delay unit will be needed. Therefore, path D has six delay units.

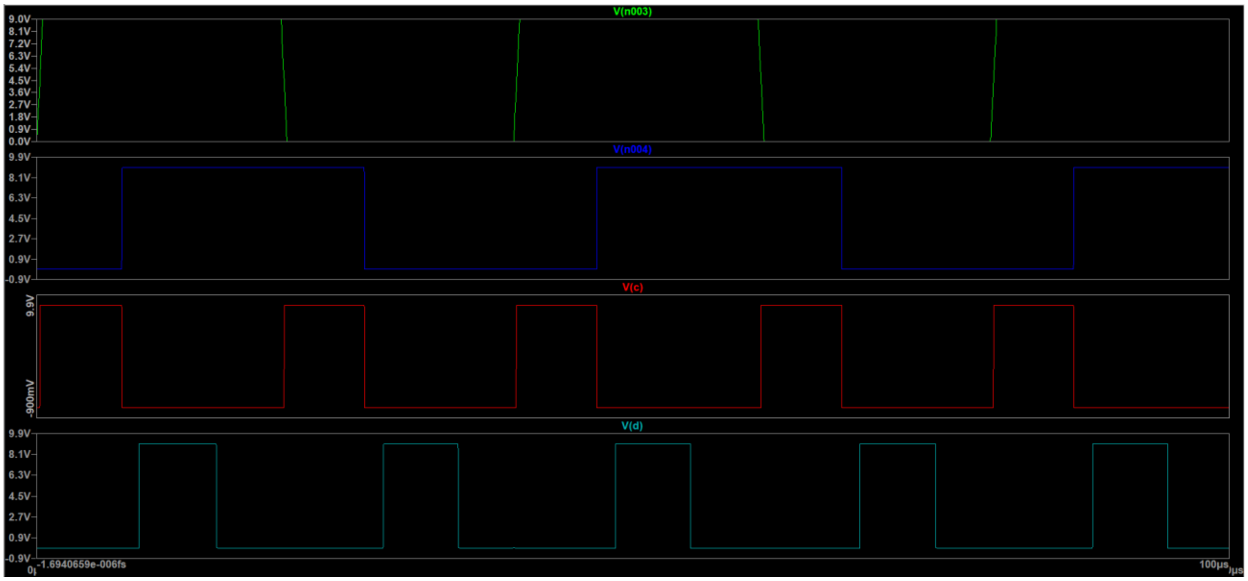


Fig. 2. 10: RC delay waveforms for path C and path D.

When input voltage goes through path B, it will pass two delay units, so that the input voltage will have a delay at the end of the path B. When voltage arrive XOR gate, they actually have a time difference.

The green one is path A's voltage, it is input x for XOR gate, the blue one is path B's voltage, it is input y for XOR gate. Delay for voltage B is 7.16µs, based on characteristics of XOR gate, treat voltage A as true, voltage B as false, a new period is generated. The red one is path C's voltage, and the new period of path C is 7.14 µs. Last voltage is path D's voltage, it has the same period with path C, but turn on time is different. The voltage source set as pulse wave, Vin = 9V, $T_{rise}$= 0.5 µs, $T_{fall}$= 0.5 µs, $T_{on}$ = 20 µs, $T_{period}$ =40 µs. A 100 KΩ resistor and a 50 pF capacitor have been choosing for the phase one, for phase two, the resistors value is 40 KΩ and capacitors value are 50 pF.

$\tau$ for phase one is:

$$\tau = 100K * 50 * 10^{-12} = 5 * 10^{-6}s \tag{6}$$

$\tau$ for phase two is:

$$\tau = 40K * 50 * 10^{-12} = 2 * 10^{-6}s \tag{7}$$

From waveform, path B has a 7.16 μs delay. A new duty cycle has generated in V(c), the new period of V(c) is 20.72 μs, Ton is7.16 μs, the duty cycle is 0.35. Ideally, the period of V(c) and V(d) should be the same, however, there is still a tinny time difference, the reason is the voltage need time to rise and fall. That will make the time not exactly the same, therefore, but V(d)'s period is 20.42μs, Ton is 6.37μs, the duty cycle is 0.32.

## 2.3 General Loss in Converter

Converter's efficiency is not always the same, with different input and output voltage required, the power dissipation may be different. The efficiency of buck converter depends on its components characteristics. The formula for efficiency is [7]

$$\eta = \frac{P_{out}}{P_{in}} \tag{8}$$

Usually, power is calculated by $P = V * I$, since a buck converter is a step-down voltage converter, the output voltage will have a large difference with the input voltage, this equation cannot be used. Based on this situation, equation xxx are selected to calculate converter’s efficiency.

$$\eta = \frac{P_{out}}{P_{out}+P_{Dissipated}} \tag{9}$$

Where $P_{out}$ is output power and $P_{Dissipated}$ is the sum of all other components’ power loss. The general loss for the buck converter is the load loss, inductor loss, MOSFET loss, and switching loss. Each component of power loss is shown below:

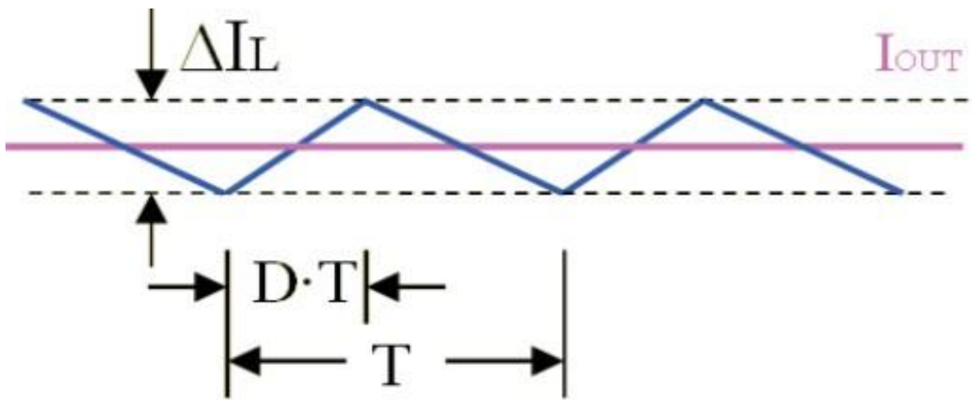


Fig. 2. 11: Inductor current. Source: Arvind Raj, "Calculating efficiency", Texas Instruments Application Report Feb 2010

Figure 11 shows how current through an inductor in a DC-DC converter. The red line is output current, the blue line is ripple current of the inductor. The inductor power dissipated is:

$$P_L = I^2_{RMS\_L} * R_{DCR} \tag{10}$$

Where $R_{DCR}$ is the DC-Resistance of the inductor, in the purposed two-phase buck converter, the DC-Resistance is set as 0.5 Ω. The rms inductor current is given by:

$$I^2_{RMS\_L} = I^2_0 + \frac{\Delta I^2}{12} \tag{11}$$

$$\Delta I = \frac{(V_{IN} - V_{OUT}) * V_{OUT}}{L * f * V_{IN}} \tag{12}$$

Compared with output current, ripple current is small, and after it squired, it will become much smaller than the output current, so that the ripple current could be ignored. Therefore, the power dissipated for inductor can be rewritten as

$$P_L = I^2_o * R_{DCR} \tag{13}$$

MOSFETs are the most significant components of a buck converter, in a converter, MOSFETs have high-side and low-side, with a different side, the ripple current will be different. High- side MOSFET is the MOSFET connect with a power source, in the purposed converter, are M1 and M3. Low-side MOSFET is the MOSFET connects to ground, in the purposed converter, are M2 and M4. The power dissipated in the high-side MOSFET is given by [8]:

$$P_{M1} = I^2_{RMS\_M1} * R_{DSON1} \quad (14)$$

Where $R_{DSON1}$ is the on-time drain-to-source resistance of the high-side MOSFET.

Plug $I^2_{RMS\_M}$ into equation xxx, a new equation of $P_{M1}$ is:

$$P_{M1} = \frac{V_{OUT}}{V_{IN}} * (I^2_0 + \frac{\Delta I^2}{12}) * R_{DSON1} \quad (15)$$

Power dissipated for M3 is the same concept as M1.

The power dissipated in the low- side MOSFET is:

$$P_{M2} = I^2_{RMS\_M2} * R_{DSON2} \quad (16)$$

$R_{DSON1}$ is the on-time drain-to-source resistance of the low-side MOSFET.

Plug $I^2_{RMS\_M}$ into equation xxx, a new equation of $P_{M2}$ is:

$$P_{M2} = (1 - \frac{V_{OUT}}{V_{IN}}) * (I^2_0 + \frac{\Delta I^2}{12}) * R_{DSON2} \quad (17)$$

The power dissipated of M4 is the same concept as M2.

The total power dissipated in phase one's MOSFET is:

$$P_{FET} = P_{M1} + P_{M2} = (I^2_0 + \frac{\Delta I^2}{12}) * [\frac{V_{OUT}}{V_{IN}} * (R_{DSON1} - R_{DSON2}) + R_{DSON2}] \quad (18)$$

Since in the purposed converter, $R_{DSON1} = R_{DSON2}$

Therefore,

$$P_{FET} = (I^2_0 + \frac{\Delta I^2}{12}) * R_{DSON2} \quad (19)$$

The total power dissipated in the converter is

$$P_{Dissipated} = P_L + P_{FET} + P_{other} + P_{other\_loss} \quad (20)$$

Other power dissipated including switching loss, conduction loss.

$$\eta = \frac{P_{out}}{P_{out}+P_{Dissipated}} \tag{21}$$

In these equations, L in Henry, f in hertz, both $V_{IN}$ and $V_{OUT}$ in voltage. The result of buck converter's efficiency will show in later part.

## 2.4 Efficiency Improvement in Converter

Based on the previous equations, there are several ways to improve the buck converter's efficiency, they are improved by reducing conduction loss of MOSFETs, use Schottky diode instead of normal diodes, choosing capacitors with ESR, [9]

a. Reduce conduction loss of MOSFETs.

From equation $P = I^2 * R$, use a smaller $R_{DSON}$ will reduce the conduct less. There are switching loss in MOSFET too, to reduce switching loss, use a faster high-side MOSFETs can let the MOSFETs operate quickly so that the power dissipated of switching will be reduced. [6]

b. Use Schottky diode instead of normal diodes.

Compared with normal diodes, a Schottky diode with voltage drop can reduce power loss. It can also reduce switching losses as well. As mention before, the use of diodes is to let current goes in a correct way, and it will provide a free-wheeling path for MOSFET with it is turned off. In this case, the free-wheeling diode becomes a significant source of efficiency. It is important for those applications which have low voltage and high current, change winding of inductors.

c. Choosing capacitors with ESR

As described earlier, with more phases, the ESR will be decreased, on the other hand, choosing a capacitor with ESR will also reduce the output ripple voltage and extend the usage time of the capacitors, which will increase the efficiency of the buck converter.

d. Changing winding of inductors.

Inductor has copper and core losses. Switch magnetic domains back and forth in the core requires energy which will cause core losses. Based on the equation $P = I^2 * R$, copper loss is related to its own resistance and high-frequency losses in the wiring of the inductor. With the difference windings of the inductor, the resistance would be a difference, with bigger windings, the DC resistance would be smaller. Because multiple coils could be wind in parallel ways, that will reduce the AC resistance.

## 2.5 Design Approach and Component Selection

### 2.5.1Design Approach

The design of each draft is discussed in detail in this section. The design contains four drafts, each draft improve the design by circuit design, components selection and adjust values.

In draft one, Cadence virtuoso was chosen as the circuit design application. But the MOSFET library didn't have a model can reach a high drain to source voltage, the maximum voltage the models in Cadence virtuosos can reach is 3V, which is too small to a buck converter. In order to use a model with a higher drain to source voltage, there are several more steps need to be done. The first is find a model in other spice software, such as LTspice or Pspice, the next step is converter the model from spice into Cadence virtuoso, and create a new library for the symbol at the same time, which is too complete to do.

For draft two, the entire circuit was transferred to LTspice, because LTspice's MOSFET library has an amount of MOSFET symbol from the different company based on the real product can get a high drain to source voltage. In draft two's design, phase one and phase two were using the same delay circuit. There was only path C for the delay circuit. The buck converter was a synchronous circuit and did not have diodes. Since two phases were used one delay circuit, the output of two phases did not interleave. In this draft, inductors' value was set to be 400 µH, capacitors' value was 200 pF, the load value is 20 Ω. For the delay circuit, the input voltage is 9V, the frequency of the voltage source was set to be 100k Hz, the resistors' value were 50kΩ, capacitors' value was 50pF. However, the output voltage was decreased from 0 to -8.96V, and it had an opposite shade of the correct waveform.

The third draft had improvement based on these problems. The first one added diodes parallel with MOSFETs, the diodes ensure the input current goes in the correct direction. The second one added path D for phase two, in draft three, four delay units were added, the value of resister of path D was 50kΩ, the capacitors' value were 100pF. However, the waveform of the output of path C and path D were overlapped, and Ton for path D was much smaller than path C's. As explained in the delay circuit part, the capacitors need time to fully charge, so that the actual Ton time would decrease as excepted. In this draft, the inductors' value was reduced from 400 µH to 100 µH, and the capacitors' value was decreased from 200 pF to 100 pF, the load resistor changed from 20 Ω to 300 Ω, the frequency adjusted to from 100K Hz to 25K Hz. Resistors and capacitors value form path C were also changed. Resistors' value was increased from 50kΩ to 80kΩ, and the capacitors' value was increased from 50 pF to 100 pF. The reason to increase these two value was to get a larger duty cycle than before, the output of delay circuit also influenced the output voltage of buck converter, when the Ton overlapped, the output voltage of buck converter had more noise than before.

Fourth draft main focus on the delay problems. The delay unit of path D increased from four to six, to make sure the output of the two phases would not be overlapped. Besides this, the components' value of path C also had been adjusted. The resistors' value was keeping increase from 80kΩ to 100kΩ, the capacitors' value was adjusted from 100pF back to 50pF. Resistors from path D also decreased from 50kΩ to 40kΩ, the capacitors' value was reduced from 100pF to 50pF. The reason for this change was to keep the Ton of two-phase as close as they can and ensure the current of two-phase was interleaved.

### 2.5.2 Components selection

Components selection is a significant part for a thesis because each component will influence the circuit in a very different result. For example, without a power diode, the output of the buck converter was negative, after added power diodes, the output became correct.

From each draft, components' value changed to ensure can get a better result, as mentioned in general loss section, each components selection are an import for the converter, with an incorrect choice, the power consumption will increase. In this thesis, a MOSFET model CSD17556Q5B was selected for the buck converter, it is an N-channel MOSFET because the drain to source voltage is 30V, which is big enough for a buck converter. The threshold voltage is 1.4V, for the drain-to-source on-resistance, it dependents co different $V_{GS}$, when $V_{GS} = 4.5V, R_{DS(on)} = 1.5m\Omega$, when $V_{GS} = 1.5V, R_{DS(on)} = 1.2m\Omega$, Qgate is $3*10^{-8}$C. The graph for $R_{DS(on)}$ $vs. V_{GS}$ and the gate charge shows below. [10]

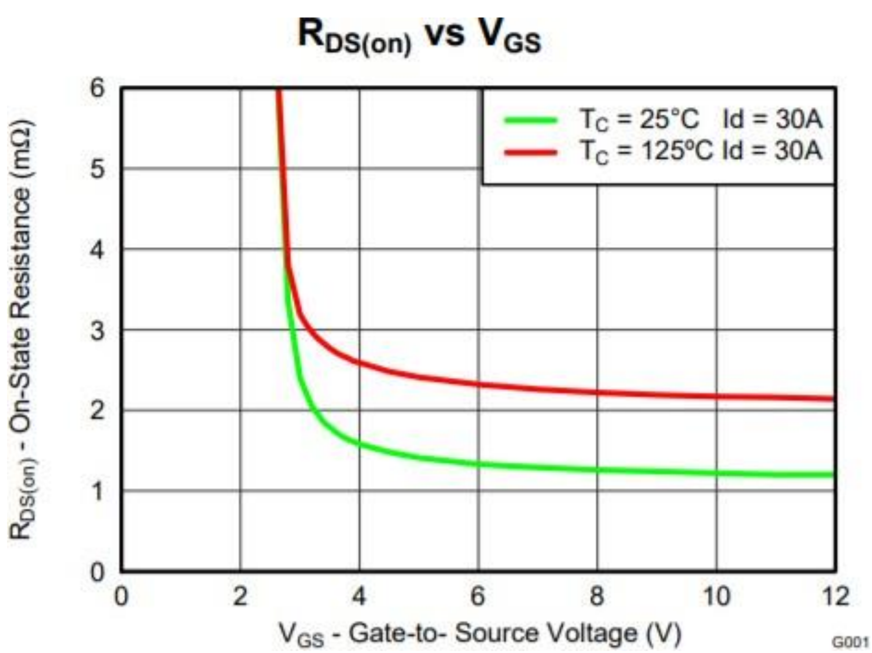


Fig. 2. 12: $R_{DS(on)}$ $vs. V_{GS}$ for MOSFET. Source: CSD17556Q5B Datasheet, Texas Instruments, Nov 2017.

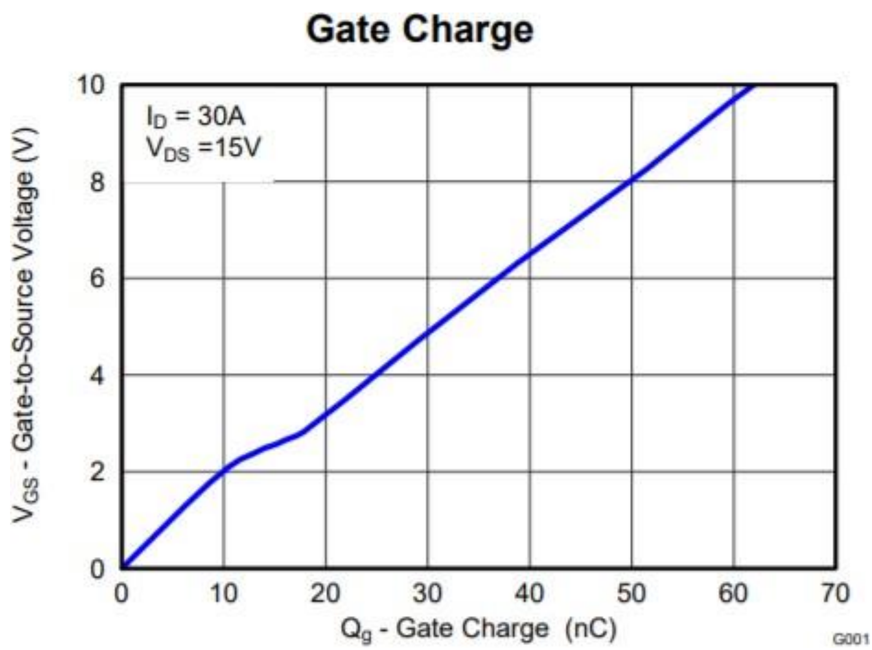


Fig. 2. 13: Gate charge for MOSFET. Source: CSD17556Q5B Datasheet, Texas Instruments, Nov 2017.

As mentioned in the general loss section, DC-Resistance of the inductor will also affect the efficiency of the entire circuit, so that the inductor's selection should also be careful. In this thesis, the DC-Resistance of the inductor was chosen as 0.5Ω, the value will not be too large to affect the efficiency, and it also can ensure the circuit works well.

At draft one, the load value was 2Ω, the output waveform first reached a higher voltage but dropped to a lower voltage quickly, as shown below. After adjusting the load resistor, it was found that the reason was load resistor was too small, so in draft two, the load resistor was increased to 20 Ω.

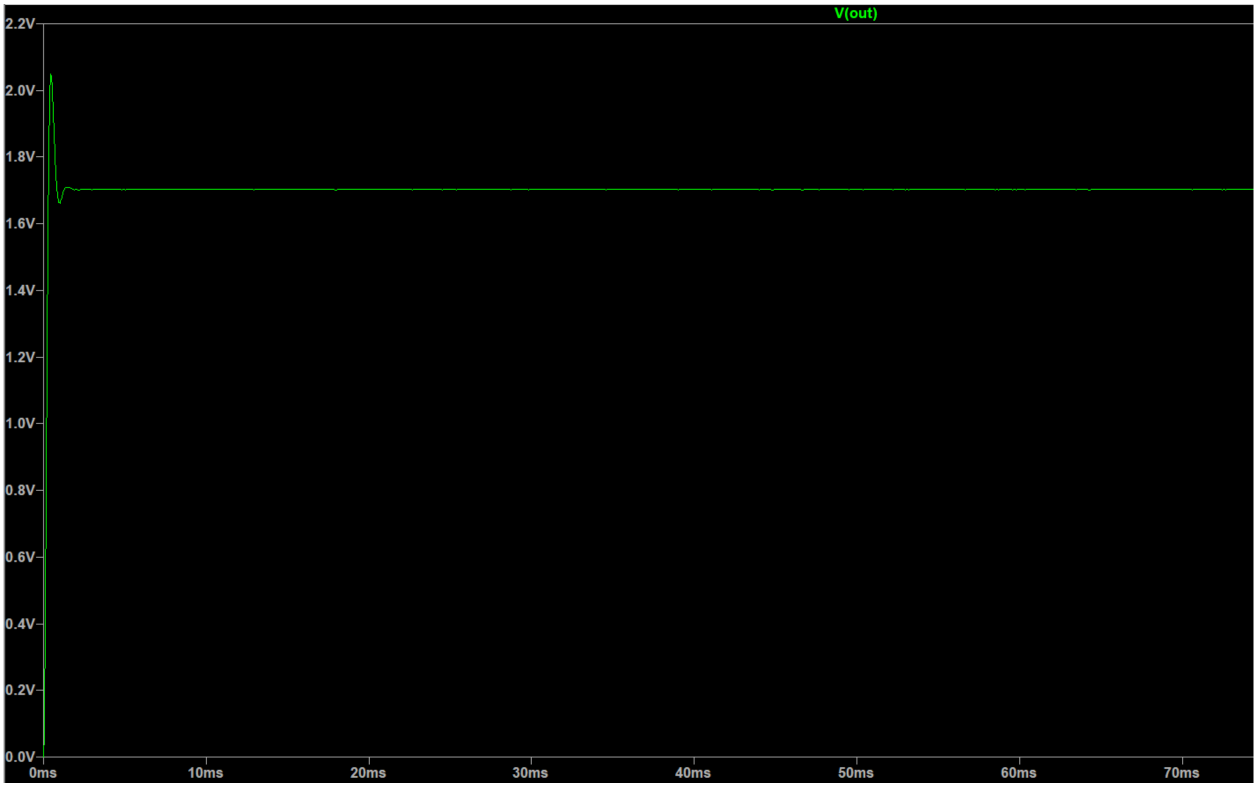


Fig. 2. 14: Output voltage waveform when the load resistor was 2Ω.

However, when the load increased to 20 Ω, the output waveform was not smooth, it had some sharp voltage. Keep increasing the load to 100 Ω, and the output waveform was getting smooth, adjust the load's value until it reaches the highest efficiency. After tests, turns out when the load is 300 Ω, the circuit can achieve the highest efficiency.

Similar in the RC delay circuit, the value of path C and path D adjusted several times. As mentioned in the design approach section, when the value of resistor and capacitor was too small, the output would be overlapped, but if the value of the resistor and capacitor were too big, the output waveform would also be changed into an incorrect way.

# Chapter 3

# Application of Neural Network to Buck Converter

## 3.1 Introduction of Neural Network

### 3.1.1 Neuron and synapse in the biological brain

A neuron is a specialized cell process and transmitting nerve impulses by electrochemical signaling. Transiting information in a brain is a very complicated process which implicates more steps. During the transiting information, it combines chemicals and electricity. Dendrites, a soma, and a single axon are three parts of a representative neural. Dendrites are long and feathery filaments that attached to the cell body in a complex branching called dendritic tree. A single axon could be thousands of times the length of the soma with a special, extra-long, branched cellular filament. The bulbous cell body, which contains the cell nucleus, is a soma. Different from other cells, neurons neither die off to be replaced by new ones, or nor split. For this reason, most of the neurons cannot be replaced after being lost. [11]

The differential driving of sodium, potassium, chloride, and calcium in the cells drives each neuron to maintain a voltage gradient across its membrane, causing each ion to have a different charge. An action pule is generated when the voltage changes significantly, which is an electrochemical pulse. Based on the movement, this electrical activity can be measured and the waveform of the activity called brainwave or brain rhythm. These pules travel quickly along the cell's axon, and it transferred to another neuron through a synapse.

A neuron connects with another neuron by synapse, and a synapse is a junction or gap between two neuron cell, it let neuron pass an electrical or chemical signal to another neuron and a target cell, such as muscle or a gland. In a synapse, an action potential is emitted in one neuron, it could be presynaptic, or sending neuron, and it will lead the signal transmission to another neuron, this neuron could be a post-synaptic or receiving neurons, the transmission will make the post-synaptic possible to play its own potential for action. Figure 15 shows the relationship between neuron and synapse [8].

There is a huge number of neurons in a human brain, an average of 100 billion and a greater number of glial cells used to support and protect these neurons. Each neuron can be connected to more than 10,000 other neurons, and all these connections are made through synapses, the number of synapses can reach to 1,000 trillion which is equal a computer with a one trillion bit per second processor[11].

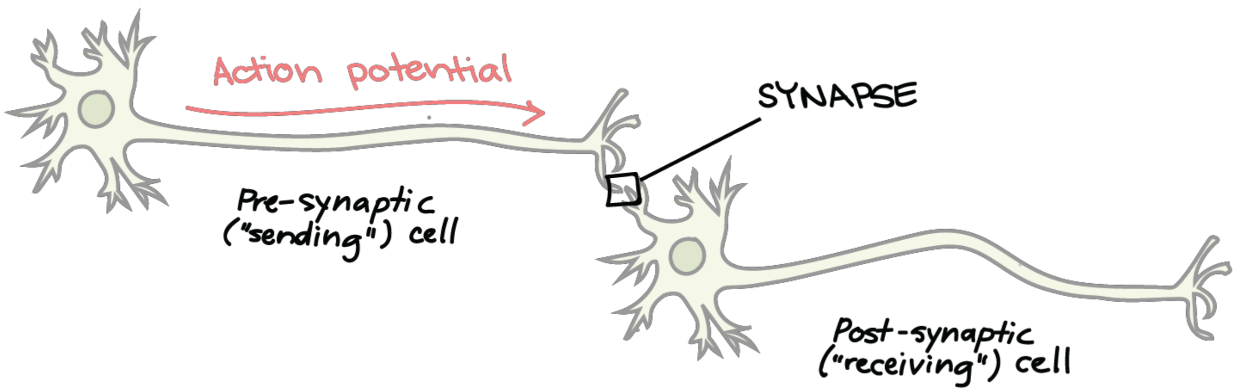


Fig.3. 1: Neuron and synapse diagram. Source: Khan Academy. (2018). The synapse.

Each neuron is connected to a function-related neuron to form a powerful neural network. However, the connections between each neuron are not static. They change based on the connections and time. For example, as more and more signals are sent between them, the connection will become stronger. So whenever the brain accepts something new of forms a new memory, the brain will reconnect the neural network. For this reason, it is hard for people to imitate a real neural network.

## 3.1.2 Neural network

Neurons in the biological brain give the idea about a neural network, the neural network generates an excellent work in Machine Learning and computer vision area. A neural network has self-learning ability, like the biological brain, a neural network also has "neuron" and "synapse".

Similar to the biological brain, the basic unit of computation in a neural network is also a neuron which called a node or a unit. The working methods of the neural network are also basically flowed how biological brain works. The unit receives input from other modes, or from an external source and computes an output. Different from the biological brain, each of the input has an associated weight, it depends on its relative importance to other inputs. Graph below shows how single neuron works. [12]

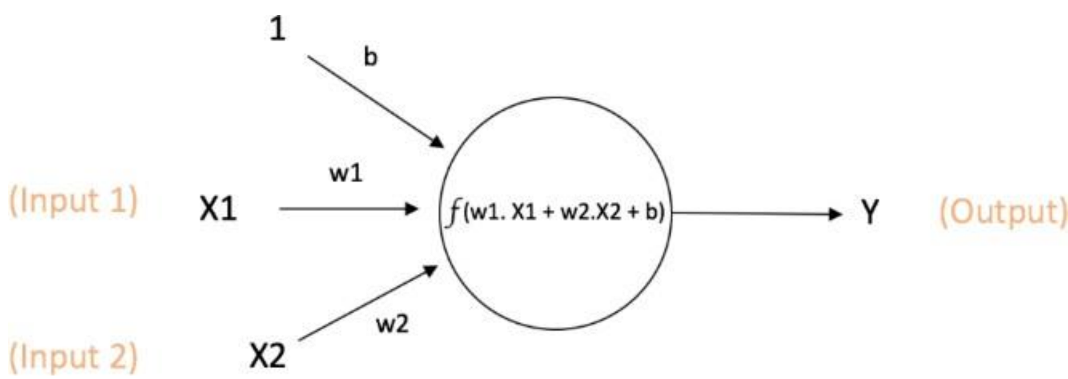


Fig.3. 2: Single neuron. Source: Walkarn, U. (2016). A Quick Introduction to Neural Networks.

Figure 16 is a single neuron's diagram, and it has input 1 and input 2, mark as X1 and X2 respectively, weight W1 and W2 associated with the inputs. The output function of the neuron is f(w1*x1+w2*x2+b), b is a bias input in this neuron, it will be explained later. This function is called an Activation function, and it is a non-linear function. In a real word, most of the data is non-linear, in order to let the neuron network works well, neurons need to learn these non-linear representations, which is the purpose of the activation function. It needs introducing ono-linear into the output of the neurons.

In input with weight, b is called a bias input, and it is an "extra" neuron added to each input layer. Different from other input, a bias input will not connect with the previous layer, which means the previous layer does not have any influence of bias input. Another characteristic is a bias input is only in input layer or hidden layers, the output layer does not have a bias input. Figure 17 shows how bias input connects with each layer in multi-layer neural networks. [12]

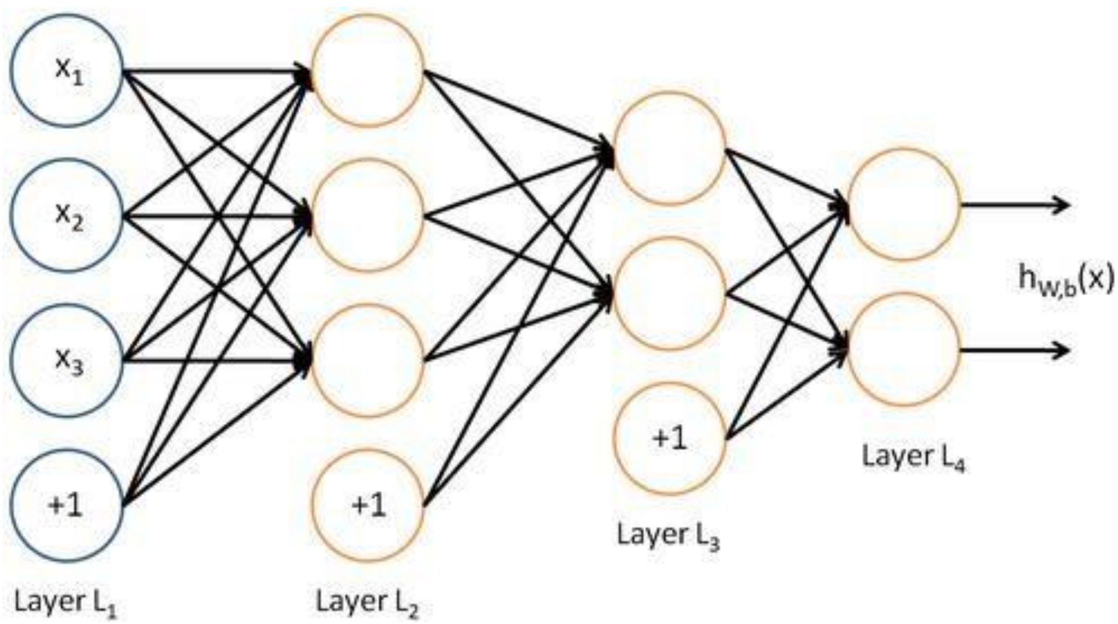


Fig.3. 3: Multi-layer neural network with bias input. Source: Walkarn, U. (2016). A Quick Introduction to Neural Networks.

Without the bias unit, the function of the output will be $f = w_1 * x_1 + w_2 * x_2$, when the weight of inputs change, the gradient of the function will either go steeper or flatter. However, the function will not go vertically, on the other words, the function cannot move in the y-axis. Therefore, a bias unit is needed to add on the output function to help the function move vertically. After adding the bias unit, the function becomes

$$f = w_1 * x_1 + w_2 * x_2 + w_b \tag{22}$$

Where $w_b$ is the weight of a bias unit, it can be seen as a constant term in this equation. The use for bias unit is not only in helping output function move vertically but also in actual computation of neural network.

In a neural network, linear algebra, matrix arithmetic, dot-product, and multiplications are used for the computation. For a weighted sum, weights and activities should have a matching number. Therefore, a bias unit is needed to act as a constant term in the neural network. [

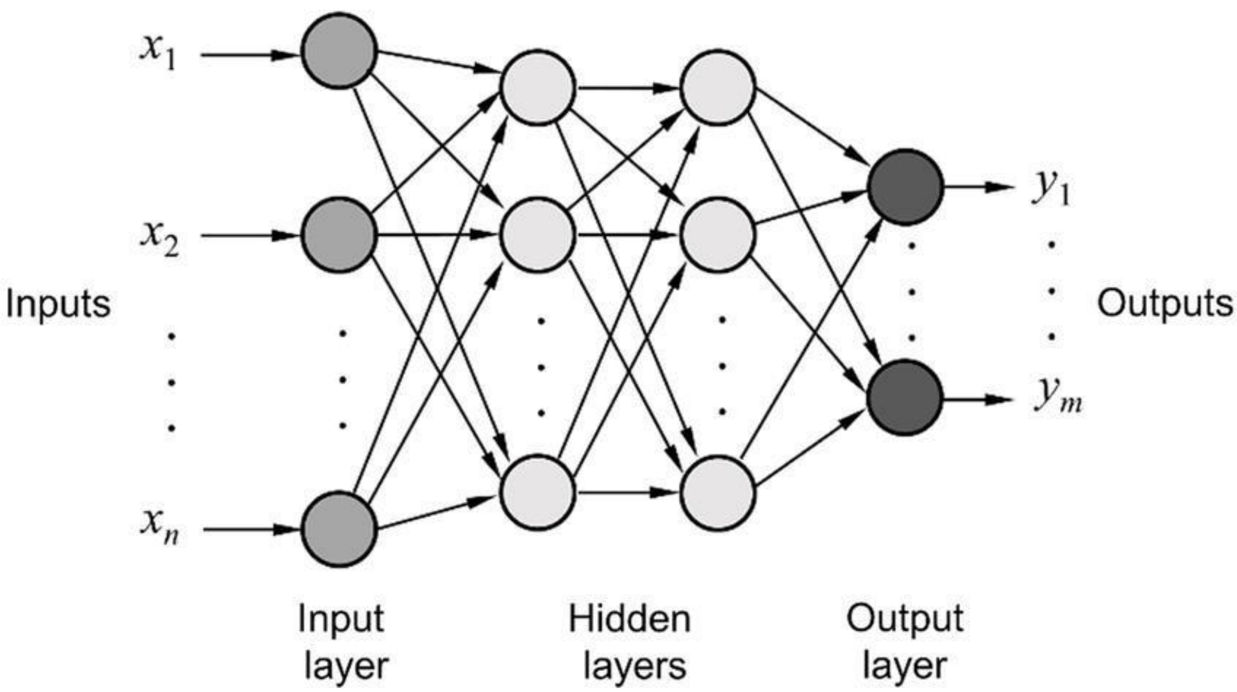


Fig.3. 4: multi-layer neural networks. Source: Kang, N. (2018). Multi-Layer Neural Networks with Sigmoid Function— Deep Learning for Rookies (2).

Most of the neural network now is multi-layer neural different with a single neuron, and it has hidden layer[13]. Hidden layers are neuron node that is stacked between the input layer and output layer, allowing the neural network to learn more complicated stuff. Without the hidden layer, a neural network can only have a single-layer perceptron, but with it, the single-layer perceptron can be transformed into a multi-layer perceptron[14]. There can be more than one hidden layers in a neural network, and the number of the hidden layer neuron is not necessarily the same as the number of input neurons. So that to mark each hidden layer, it always labeled as h with subscripts 1,2,3…n.

The process of repeatedly adjusting the weights to minimize the difference between the actual output and the desired output is called backpropagation. Backpropagation algorithm is often used in neural work. The basic step for backpropagation is first feeding forward the values, next, calculate the error and propagate it back to the earlier layers. Compared with a feedforward neural network, the benefit of backpropagation is it can fix the value of each layer to make the neural network more accurate. [15]

## 3.1.3 Echo State Network

Reservoir computing is a relatively new approach of a neural network training. Reservoir computing contains two methods; one is Liquid State Machine(LSM) another one is Echo State Network(ESN). Usually, the input signal is sent to a fixed dynamical system called a reservoir, and the input will be mapped to a higher dimension by the dynamics of the reservoir. Next step is training the state of the reservoir by a readout mechanism and map it to the desired output. Compared with a neural network, the main benefit of reservoir computing is it only need adjust the readout state, and all other layers are fixed [16].

Echo State Network(ESN) is a recurrent neural network with a sparse connected hidden layer. As mentioned before, the hidden connectivity and weights of the input layer and hidden layer are randomly assigned and fixed. ESN only train output weights during the training, and it can be modified during training [17].

Figure 3.5 shows the basic ESN architecture, there are K input layers, N internal units, and L output layers, the arrow means weight for each layer, in a dynamical reservoir, the neuron could connect any neuron in the reservoir, however, the direction of each weight should be the same [18]. For the output layer, the orange arrow is output weight, and the black arrow is feedback weights. A large RNN has over 10 hidden neurons, is used as a "Dynamic Reservoir (DR)" to maintain the high modeling capability of the ordinary recurrent neural network.

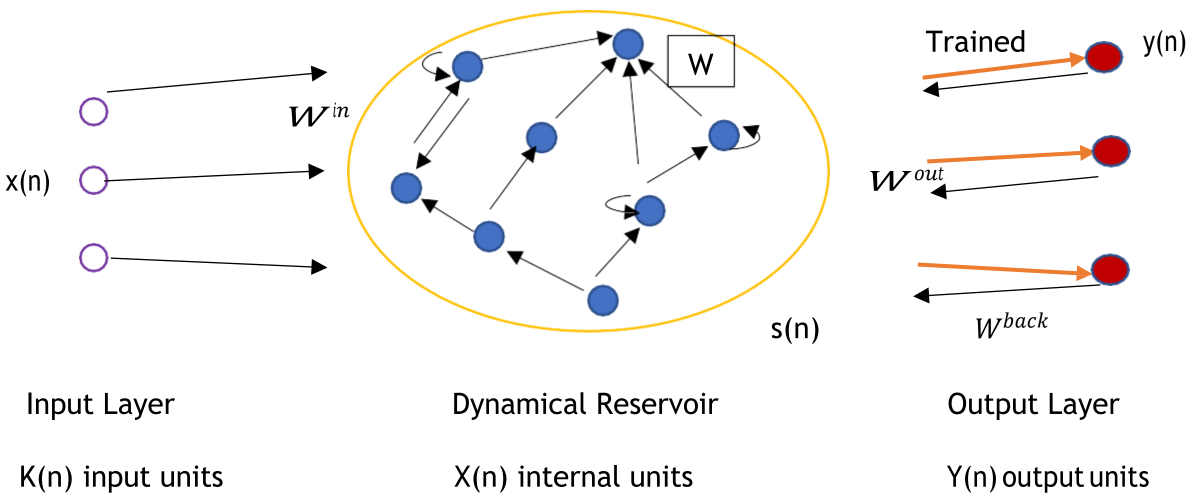


Fig.3. 5: Basic ESN architecture.

In ESN, an interval of [-1, 1] is sampled uniformly for the synaptic weights within the reservoir layer. In order to satisfy the ESN property, the spectral radius, λ, is set to be less than 1. The general node state of the reservoir computing could be expressed as

$$s(t) = f[W * s(t-1) +* W^{in} x(t-1)] \qquad (23)$$

Where s(t) is the node state at time t, x(t-1) is input patterns, W is randomly generated synaptic weights of the reservoir, and $W^{in}$ is the input weights. The output could be express as

$$y(t) = W^{out} * s(t) + W^{back} * x(t-1) + W^{bias} \qquad (24)$$

Where $W^{out}$ is output weights from the reservoir layer, and $W^{back}$ is the feedback from the output layer to the reservoir layer, and $W^{bias}$ is a bias weigh.

There are two algorithms used in ESN, the first one is offline training, another one is online training. There are four steps for an offline training, first is to generate three weight matrix, they are weight matrix $W^{in}$, internal weight matrix W, and the output feedback matrix

$W^{back}$. Based on the reservoir computing's characteristic, once these three weights are generated, they are fixed during the entire training process.

Even the algebraic properties of the weight matrix decided the echo state property[19], it cannot be decided by algebraic condition whether the network has the echo state property.

However, some conditions that increase the likelihood of an RNN having an Echo State Network still exist. There are several steps to generated W.

The second step is to put teaching target input and output to the ESN. When the data is in the reservoir, it will activate the dynamics of the reservoir so that the internal dynamic reservoir states can be calculated. After getting the reservoir states, a new row in matrix Dr will be created by collecting the states at time n.

The third step is to clean initial memory in DR. The reason is an initial memory was contained in the arbitrarily generated network states. However, input did not cause by the memory, the reason is at the first n times, it is not guaranteed that the influence of an initial state has disappeared, and the response of teaching target of input and output is the network states. So the memory before n times needs to be removed to get a new matrix.

The last step is to calculate the output weights. With the same reason, the first n rows of the output teaching target are also removed to get a new matrix, and after that, the output weights can be computed.

Different from offline training, there is one more weights $W^{back}$ called feedback weight. shown in a black arrow in figure 19. There are also four steps for online training, instead of generating three weights matrixes in offline training, the first step for online training is to generate a recurrent neural network. The reason is the new feedback weight. Follow the basic rules in Echo State Network, the feedback weights is also randomly generated and fixed at the beginning.

The second step is to calculate the states in the DR, this step is basically the same with offline training, however, compared with offline training, the online training does not require removing the nth row to generate a new state matrix DR. The third step is calculated the desired output of the ESN. The last step is also different from offline training, in online training, it updates the output weights.

Based on both offline and online training algorithm, only output weights are updated during training, and other weighs are randomly generated, this guarantee the low computation of the ESN. However, the randomly generated weights will decide the overall performance of the ESN. In order to achieve satisfactory performance, both offline and online training algorithm are alternatives.

## 3.2 Application of ESN

ESN has been applied to many power system applications. In this thesis, the ESN has been applied on two-phase buck converter to train switch's frequency to increase the system's efficiency. The main idea for this application is to use the self-learning ability of ESN to compute the output voltage and train the output voltage based on the principle of the ESN and increase the efficiency of the two-phase buck converter.

The data need first collect from buck converter, then read by ESN. The data including input voltage, output voltage, a period of the switched, the value of the inductor, capacitor and load resistor. The basic idea of ESN applied on buck converter is based on the input voltage and the period of the switched to train the output, and check if the output is in the teaching target, if not, ESN will train it again, until the output reaches the teaching target. Figure 20 shows the flow chart of how the ESN applied to the two-phase buck converter.

First, need to set up each parameter, in this program, input, output and reservoir numbers should be decided, and decided initial value. The number of input, output, and reservoir were set to be 200, and the spectral radius is 0.95, sparsity equals 0, the noise is 0.001. The second step is to check the state of the project. Since it is randomly selected, it could be a random state, none state or a seed. If it is a random state, initial weights can be defined randomly. The last step is to compute the output, and then check if the output is in the teaching target.

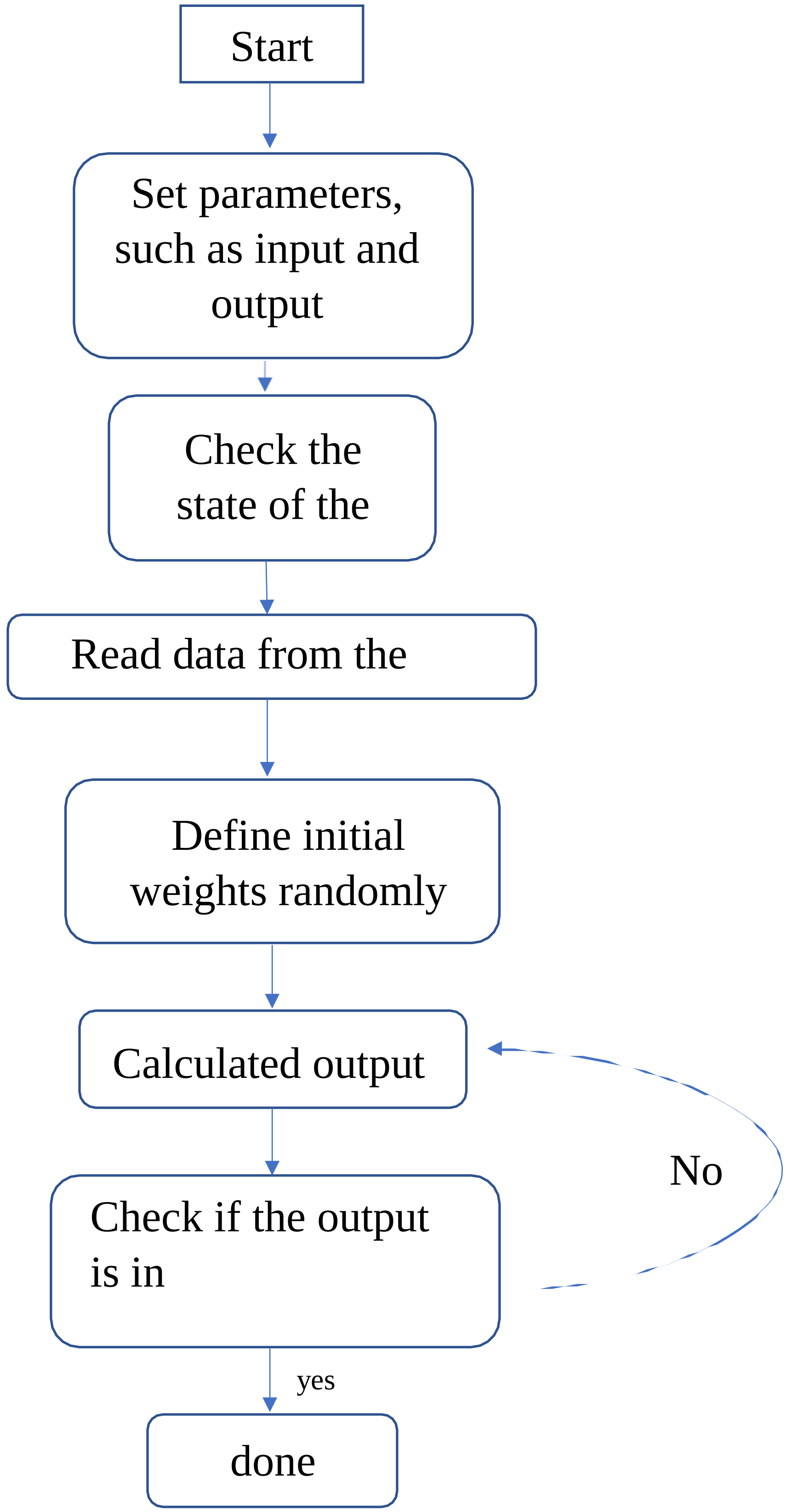


Fig.3. 6: Flowchart of ESN.

The activation of internal units is updated according to the equation below [20]:

$$x(n+1) = f(W^{in}u(n+1) + Wx(n) + W^{back}y(n)) \quad (25)$$

Where $f = (f_1, f_2, ..., f_n)$ are the internal unit's output functions. They are typically sigmoid functions(tanh). The equation for outputs is based on [20]

$$y(n+1) = f^{out}(W^{out}(u(n+1), x(n+1), y(n)) \quad (26)$$

Where $f^{out} = f_1^{out}, f_2^{out}, ..., f_l^{out}$ are the output unit's output functions and (u(n + 1), x(n + 1), y(n))is the concatenation of the input, internal, and previous output activation vectors.

$$W^{out} = y^{target}X^T(XX^T + \alpha^2 I)^{-1} \quad (27)$$

where I is the identity matrix, α is a regularization factor, X are all x(n) produced by presenting the reservoir with u(n), $y^{target}$ are all $y^{target}(n)$ which is the desired output, both collected into respective matrices over the training period n=1,…, T.

After all, data go through the ESN, it will get a result about which output is in the teaching target and which is not. For the output is not in the teaching target, it will go back the step four to recalculate the output, and recheck it to see if the output satisfied the requirement.

# Chapter 4

## Simulation and measurement result

### 4.1 The steady state measurement result

The two-phase buck converter is shown below, there are two parts in the schematic, the first part the two-phase converter, the second part is delay circuit as maintained previously. A half- bridge regulator is connected with two-phase buck converter so that AC voltage can be converted to DC voltage. A diode was parallel with the lower-side MOSFET to ensure the current goes in a correct way.

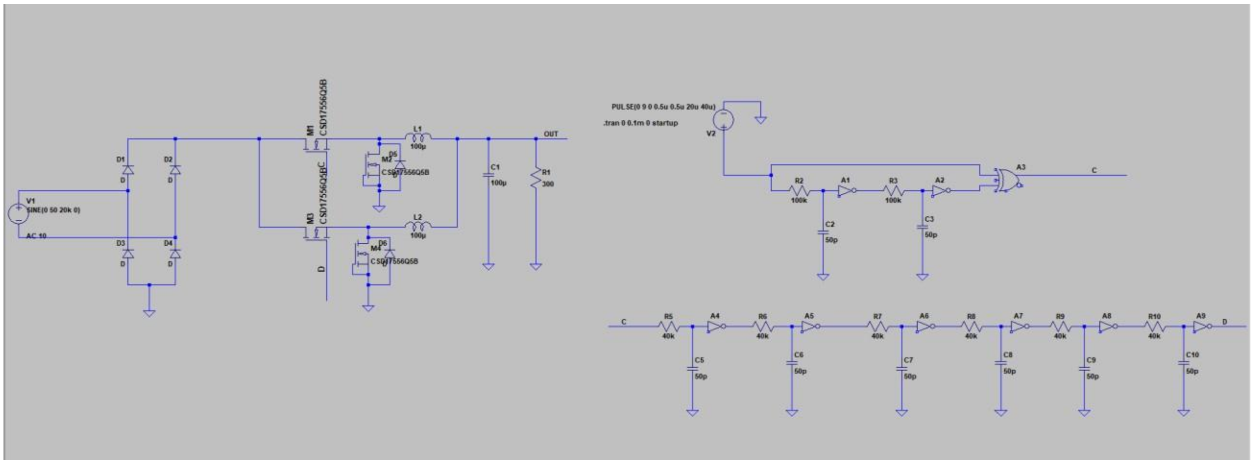

Fig. 4. 1: Schematic for a two-phase buck converter.

Data record when the circuit reached steady state, from the simulation, from 0 – 2.5ms, output voltage increase fast, from 2.5 – 7.5ms, output voltage increase slowly than before, and after 7.5ms, it increases much more slowly, with time increase, the output is almost reached steady state. After 50ms, the output voltage reaches steady states.

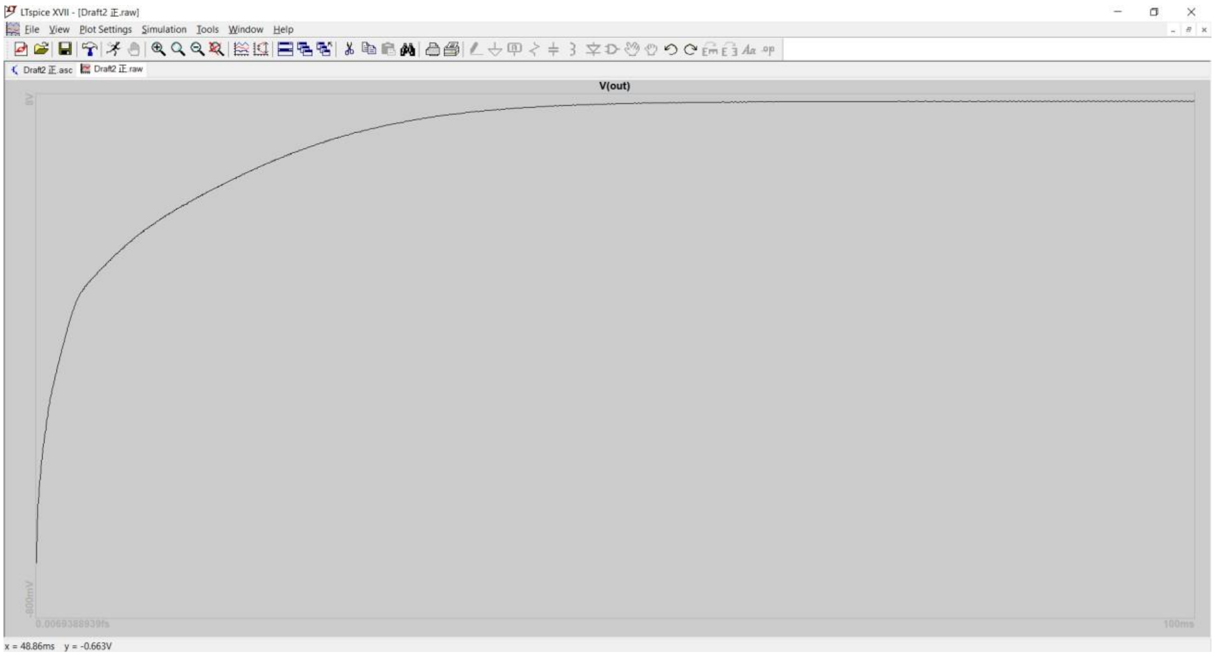

Fig. 4. 2: output voltage

The output voltage when it reaches steady states is 8V, and the input voltage is 30V, the current through two MOSFET was the same, were 101.82mA. The input voltage of the switch is 9V, the pulse period is set to be 40us, and the Ton is half of the period, which is 20us.

Table 4.1 shows the partial output of the two-phase buck converter, it including input voltage, input current, output voltage, switches frequency power dissipated for MOSFETs, inductor and conductor and frequency of RC delay circuit. The power dissipated for each component and efficiency. From the table can see, output voltage related to the frequency of RC delay, and power dissipated for each component will also be changed with the switches' frequency.

| Period(us) | ΔI(mA) | Vout(V) | ESN output | ESN output | Pout | ΔI | Pfet(mW) | Ptotal | Efficiency |
|---|---|---|---|---|---|---|---|---|---|
| 100 | 5419.667 | 6.1 | 100 | 6.35 | 127.9525 | 5.005916667 | 3.133009243 | 3.33602 | 0.95044 |
| 99 | 5096.52 | 5.6 | 99 | 5.87 | 109.8277 | 4.6742223 | 2.73156936 | 2.906601 | 0.949731 |
| 98 | 5185.52 | 5.86 | 98 | 6.04 | 117.9612 | 4.727467733 | 2.794191028 | 2.984901 | 0.95183 |
| 97 | 5221.158 | 6.03 | 97 | 5.98 | 120.0784 | 4.644347067 | 2.696849769 | 2.898453 | 0.953947 |
| 96 | 5292.851 | 6.28 | 96 | 6.14 | 128.5716 | 4.6880128 | 2.747840727 | 2.967083 | 0.955882 |
| 95 | 5372.136 | 6.56 | 95 | 6.6 | 144.342 | 4.8906 | 2.99046349 | 3.229612 | 0.957167 |
| 94 | 5443.678 | 6.84 | 94 | 6.77 | 154.4914 | 4.927702467 | 3.036062579 | 3.296439 | 0.959072 |
| 93 | 5403.474 | 6.88 | 93 | 5.05 | 115.847 | 3.9059225 | 1.907818187 | 2.17094 | 0.963875 |
| 92 | 5551.988 | 7.37 | 92 | 6.9 | 169.533 | 4.88796 | 2.987424648 | 3.289267 | 0.962646 |
| 91 | 5578.661 | 7.59 | 91 | 7.31 | 184.8699 | 5.031204967 | 3.165087303 | 3.484879 | 0.963669 |
| 90 | 5435.268 | 7.38 | 90 | 7.4 | 181.892 | 5.0172 | 3.147443245 | 3.449531 | 0.963457 |
| 89 | 5149.869 | 6.83 | 89 | 6.83 | 155.3825 | 4.694782633 | 2.755899341 | 3.014681 | 0.962646 |
| 88 | 4856.306 | 6.29 | 88 | 6.84 | 143.5716 | 4.6468224 | 2.699780672 | 2.920071 | 0.960912 |
| 87 | 4546.4 | 5.74 | 87 | 6.04 | 115.7868 | 4.1968336 | 2.202227767 | 2.385972 | 0.960418 |
| 86 | 4619.917 | 6.01 | 86 | 6.21 | 124.5105 | 4.2350958 | 2.242607558 | 2.443609 | 0.962231 |
| 85 | 4651.2 | 6.2 | 85 | 5.98 | 123.6066 | 4.069788667 | 2.071038347 | 2.284663 | 0.964351 |
| 84 | 4712.375 | 6.47 | 84 | 8 | 172.64 | 4.928 | 3.036346545 | 3.269195 | 0.963509 |
| 83 | 4782.781 | 6.78 | 83 | 6.99 | 158.1138 | 4.4499039 | 2.475973087 | 2.731805 | 0.966599 |
| 82 | 4829.732 | 7.05 | 82 | 7.07 | 166.2157 | 4.431146067 | 2.455211013 | 2.731571 | 0.968178 |
| 81 | 4916.633 | 7.45 | 81 | 7.99 | 198.4716 | 4.7482173 | 2.819121479 | 3.127634 | 0.969446 |
| 80 | 4938.237 | 7.69 | 80 | 7.88 | 201.9644 | 4.648149333 | 2.701646873 | 3.030095 | 0.970868 |
| 79 | 4973.837 | 7.99 | 79 | 8.21 | 218.7144 | 4.710925367 | 2.775166761 | 3.130012 | 0.972175 |
| 78 | 4856.998 | 7.82 | 78 | 7.99 | 208.2194 | 4.5723574 | 2.61432521 | 2.953887 | 0.97241 |
| 77 | 4643.367 | 7.36 | 77 | 7.85 | 192.5605 | 4.462855833 | 2.490537855 | 2.791398 | 0.971824 |
| 76 | 4308.995 | 6.59 | 76 | 7.51 | 164.8445 | 4.278797467 | 2.289236174 | 2.530137 | 0.970217 |
| 75 | 3988.798 | 5.91 | 75 | 6.04 | 118.9276 | 3.61796 | 1.636785864 | 1.830634 | 0.970134 |
| 74 | 4045.43 | 6.19 | 74 | 6.58 | 135.8112 | 3.801222133 | 1.806800228 | 2.019805 | 0.971115 |
| 73 | 4069.507 | 6.4 | 73 | 6.89 | 147.0326 | 3.874545567 | 1.877196012 | 2.104894 | 0.972165 |
| 72 | 4121.04 | 6.7 | 72 | 7.01 | 156.5333 | 3.8678376 | 1.870768906 | 2.120083 | 0.973626 |
| 71 | 4148.708 | 6.95 | 71 | 7.22 | 167.3596 | 3.892494533 | 1.89474518 | 2.163401 | 0.974798 |
| 70 | 4193.166 | 7.27 | 70 | 7.56 | 183.1032 | 3.958416 | 1.959512066 | 2.252816 | 0.975984 |
| 69 | 4244.659 | 7.64 | 69 | 7.65 | 187.0425 | 3.9324825 | 1.93394903 | 2.23285 | 0.976681 |
| 68 | 4273.084 | 7.96 | 68 | 7.88 | 208.9776 | 3.950926933 | 1.95228292 | 2.303938 | 0.978426 |
| 67 | 4296.842 | 8.29 | 67 | 8.4 | 232.26 | 4.05216 | 2.053646867 | 2.435908 | 0.979455 |
| 66 | 4235.22 | 8.3 | 66 | 8.64 | 239.2416 | 4.0601088 | 2.061710538 | 2.445079 | 0.979969 |
| 65 | 4087.181 | 7.97 | 65 | 8.15 | 216.3825 | 3.858345833 | 1.861911425 | 2.214363 | 0.979943 |
| 64 | 3715.479 | 6.87 | 64 | 7.57 | 173.353 | 3.622295467 | 1.640914671 | 1.90312 | 0.978515 |
| 63 | 3407.746 | 6.08 | 63 | 5.4 | 109.458 | 2.78964 | 0.973377726 | 1.178814 | 0.978915 |
| 62 | 3453.15 | 6.39 | 62 | 6.48 | 138.0888 | 3.1497984 | 1.240834919 | 1.467893 | 0.979182 |
| 61 | 3464.554 | 6.61 | 61 | 6.98 | 153.8392 | 3.267151867 | 1.335013807 | 1.577895 | 0.979899 |
| 60 | 3511.582 | 6.97 | 60 | 7.06 | 164.0038 | 3.239128 | 1.312303224 | 1.58212 | 0.981072 |
| 59 | 3523.62 | 7.23 | 59 | 7.33 | 176.5797 | 3.268031633 | 1.335874337 | 1.626038 | 0.981916 |
| 58 | 3545.685 | 7.55 | 58 | 7.65 | 154.1475 | 3.305565 | 1.36645403 | 1.569465 | 0.980043 |
| 57 | 3574.947 | 7.93 | 57 | 8.05 | 212.7615 | 3.3572525 | 1.409940861 | 1.759213 | 0.983732 |
| 56 | 3587.119 | 8.27 | 56 | 8.65 | 238.4805 | 3.447313333 | 1.48663631 | 1.866689 | 0.984586 |
| 55 | 3590.4 | 8.6 | 55 | 8.97 | 257.2596 | 3.4583835 | 1.496285868 | 1.907557 | 0.985387 |
| 54 | 3534.795 | 8.65 | 54 | 9.5 | 273.79 | 3.5055 | 1.53731217 | 1.952608 | 0.985937 |
| 53 | 3456.017 | 8.58 | 53 | 8.75 | 250.3375 | 3.284895833 | 1.350045378 | 1.759311 | 0.986139 |
| 52 | 3103.214 | 7.22 | 52 | 7.35 | 177.135 | 2.88561 | 1.041714349 | 1.332119 | 0.985182 |
| 51 | 2809.201 | 6.27 | 51 | 6.54 | 136.7514 | 2.6082828 | 0.851048238 | 1.069662 | 0.984597 |
| 50 | 2837.333 | 6.6 | 50 | 6.9 | 151.731 | 2.6565 | 0.882849371 | 1.124629 | 0.985393 |
| 49 | 2837.685 | 6.84 | 49 | 7.05 | 160.74 | 2.642713642 | 0.873771684 | 1.133692 | 0.98609 |
| 48 | 2860.16 | 7.2 | 48 | 7.6 | 182.4 | 2.72384 | 0.928277043 | 1.216277 | 0.986839 |
| 47 | 2867.15 | 7.52 | 47 | 8.5 | 213.01 | 2.863083333 | 1.025597777 | 1.3396 | 0.987578 |
| 46 | 2879.447 | 7.9 | 46 | 8.09 | 213.1715 | 2.717862467 | 0.924388532 | 1.27155 | 0.988211 |
| 45 | 2885.939 | 8.29 | 45 | 8.37 | 231.2631 | 2.7156465 | 0.922987114 | 1.304696 | 0.988843 |
| 44 | 2867.555 | 8.57 | 44 | 8.66 | 247.5028 | 2.710464533 | 0.919552473 | 1.327961 | 0.989383 |
| 43 | 2865.232 | 8.99 | 43 | 9.06 | 271.4376 | 2.7192684 | 0.925648981 | 1.37445 | 0.989974 |
| 42 | 2816.598 | 9.12 | 42 | 9.42 | 286.5564 | 2.7140904 | 0.922173902 | 1.384862 | 0.990427 |
| 41 | 2760.12 | 9.2 | 41 | 9.5 | 291.365 | 2.661583333 | 0.886914203 | 1.357239 | 0.99077 |
| 40 | 2521.599 | 8.01 | 40 | 9 | 240.3 | 2.52 | 0.794869335 | 1.151314 | 0.990509 |

Table 4. 1: A Partial result of the two-phase buck converter.

Changing the switch's period but keep Ton was half of the period. The period changes from 40us to 100us, after 40us, the output voltage will first increase and then dropped, as shown in figure 14. With the period of change, the output voltage increase from 6V to 8V, the highest output voltage is 9.2V when the period is 40us.

Let ESN read the dataset collected from the circuit, use a sine wave as the input to calculate output voltage. From the graph, most of the output voltages are in the teaching target, but some of the output was out of the teaching target. Figure 23 shows the result.

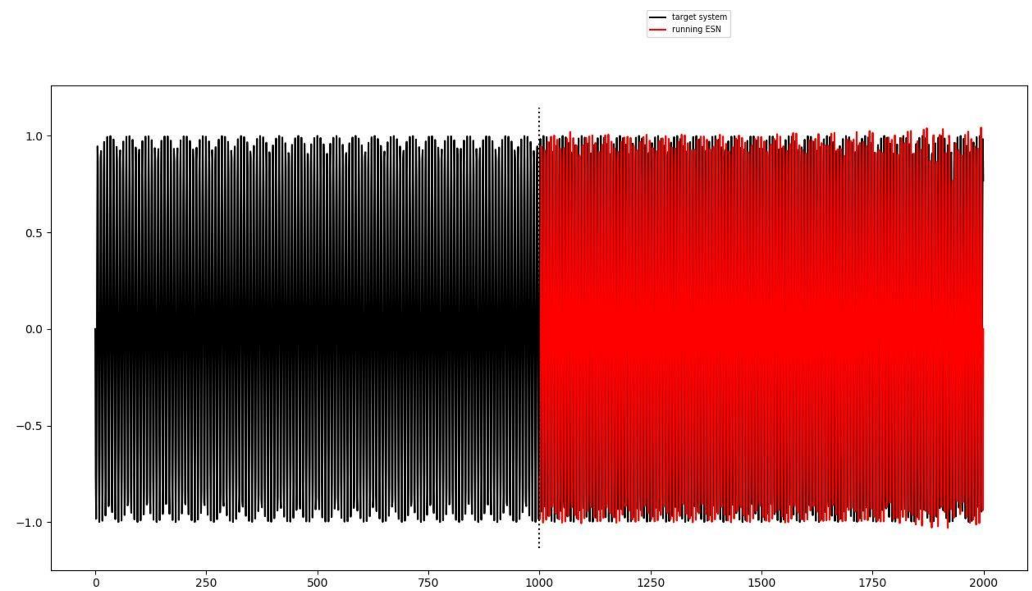


Fig. 4. 3: Result for ESN.

Y-axis is the amplitude of the output, while X-axis is the time. The black figure is the target system, and the red one is the result of running ESN. Figure 24 is a zoom in of the output, from the figure, it is easy to see that the most of the red wave is in the range of the teaching system, the part out of the teaching system will go back to calculated again until it reaches the teaching target.

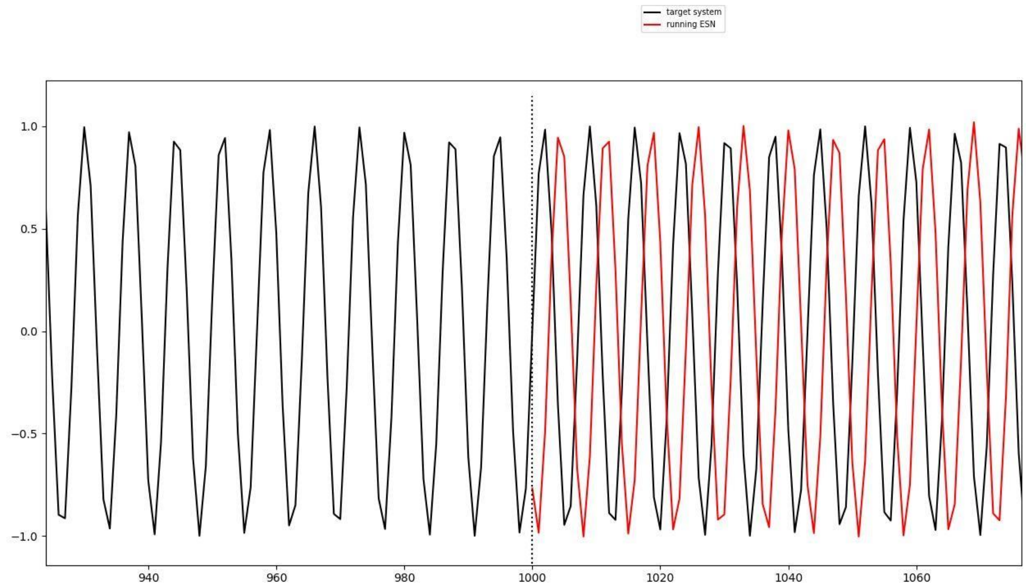


Fig. 4. 4: zoom in of ESN output.

Figure 4.5 shows the comparison of the two-phase buck converter and the ESN. The orange one is a two-phase buck converter, and the x-axis is the period in μs, the y-axis is the efficiency. When the period is small, two output is almost the same, but when the period is increased, the efficiency of ESN is higher than the efficiency of the two-phase buck converter. Another benefit of the ESN is it save much more time than the traditional two-phase buck converter. Instead of using a whole day to collect the data, the ESN only take a few seconds to get the output and te

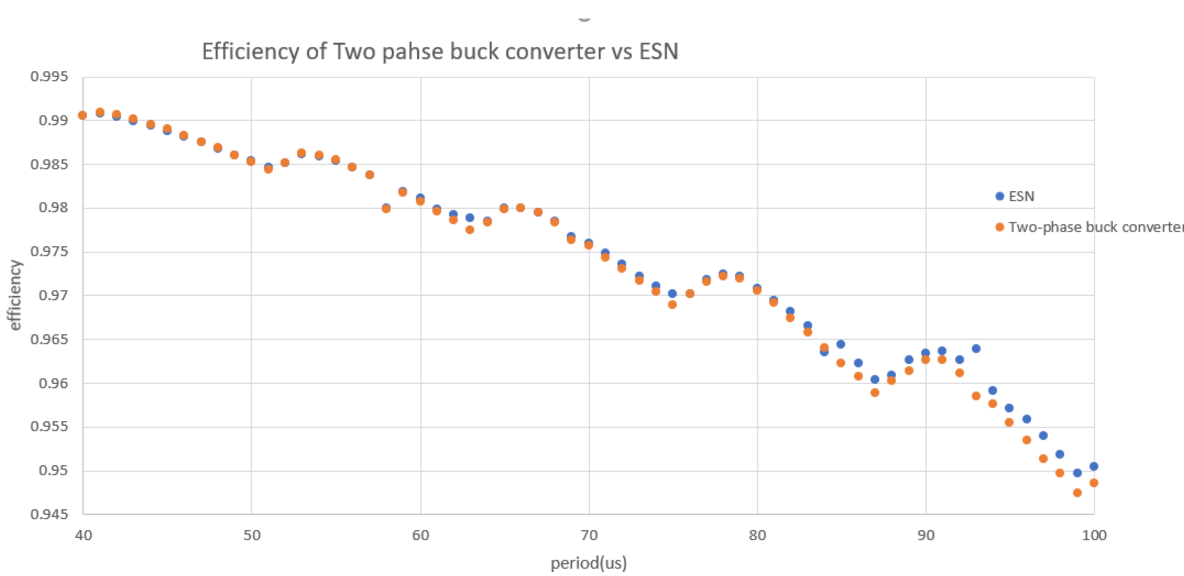


Fig. 4. 5 Comparison of the Two-phase buck converter and Echo State Network

## 4.2 Future Improvement

Right now, the ESN is only read data from the datasheet of the two-phase buck converter. In the future, it can be tried to connect the ESN with the MOSFETs to let ESN control the frequency so that when it trains the output and see there isn output out of the teaching target, it can change the frequency on time. However, how to connect the ESN to the two-phase buck converter is still a problem, because right now, the frequency is changed by change the value of the capacitors and resister of the delay circuit. Another challenge is about the other components; power dissipate. Right now, ESN only generates the output voltage. When calculating the efficiency, other components were used from the dataset, however, during the frequency changed, not only the output voltage changed, but also the other value changed, such as the power dissipated of each component. So that, the efficiency of the ESN's output is not exactly accurate. Since that, the next step is to get compute the power dissipated for each component in ESN, so that when calculating the efficiency, it can get an accurate result.

# Chapter 5

## Summary

In this thesis, a two-phase buck converter connect with echo state network has bend purposed, the purpose of this thesis is to find a way to optimize the buck converter without a PID controller or PWM controller. The reason use two-phase buck converter is compared with single-phase converter, two-phase buck converter has less power consumption and higher efficiency. Besides this, a two-phase buck converter can converter high voltage to low voltage in a higher current. The third benefit is two-phase buck converter can reduce the ripple voltage, reduce ripple current, improve thermal performance and efficiency, and improve transient response compared with the single-phase buck converter.

There is four draft total for the two-phase buck converter design because the selection of components will lead an effect of the result. The model of MOSFET is CSD17556Q5B, Vds is 30v, Rds(on) is 0.0015mΩ. The resistance of the inductor is 0.5Ω. The capacitor is 100 pF, and Rload is 300Ω. For the RC delay circuit, there are two parts, and path C is connected to phase one, path D is connected to phase two. For part A, the resister is 100kΩ, the value of the capacitor is 50pF. For part B, the resistor is 40kΩ, and the capacitor is 50p. Path C only had two delay units, but path D had six delay unit, this is because the capacitor needs time to fully charged. So that the actual turn-on time will be decreased, more delay unit will be needed to keep the turn-on time same with path C. With the switching changed, the highest efficiency of the buck converter is 95.44% when the period is 40µs, the load resistor was 300Ω, the inductor was 100µH, the capacitor was 100µF.

Neural network has been used widely in many application, reservoir computing is one of the neural network, different with the neural network, the reservoir computing only changes weights of output layers, other layers such as input layer and hidden layer are fixed at the beginning, which keeps the same efficiency but saves more times. Echo state network is one kind of reservoir computing, ESN has two algorithms, one is online algorithm, another one is offline algorithm. These two algorithms basically are the same, the difference is online algorithm has one more weight called backward weights.

Based on the flowchart, ESN has trained the dataset step by step, the output shows most of the output are in the teaching target and for the output out of the teaching target, they will go back to recalculate the output to ensure they finally reach the teaching target. Compared with normal controllers such as P.I.D controller and P.W.M. controller, it will increase the efficiency of the buck converter and also decrease the power consumption.

There still have some improvements in this design, such as how to connect ESN with the two-phase buck converter, and how to generate components' power dissipated in ESN. With the improvement, it can help the buck converter change switch smooth and fast. It will also help improve the buck converter's efficiency.

# Reference

[1] Knight, D., PRODUCTS, N., ELECTRONICS, G., PROJECTS, C., MICRO, E., Lectures, V., Webinars, I., Training, I., Search, P., DB, T., Tool, B., Designs, R. and Knight, D. (2015). Buck Converters and Their Cool Applications. [online] Allaboutcircuits.com. Available at: https://www.allaboutcircuits.com/technical-articles/buck-converters-and-their-cool-applications/ [Accessed 7 Dec. 2018].

[2] Ranjan, N. and Prasad, R. (2018). LFNN: Lion fuzzy neural network-based evolutionary model for text classification using context and sense based features. *Applied Soft Computing*, 71, pp.994-1008.

[3] Carlos Andrés González-Amarillo, Juan Carlos Corrales-Muñoz, Miguel Ángel Mendoza-Moreno, Angela maría González Amarillo, Ahmed Faeq Hussein, N. Arunkumar, Gustavo Ramirez-González, "An IoT-Based Traceability System for Greenhouse Seedling Crops", Access IEEE, vol. 6, pp. 67528-67535, 2018.

[4] Mahesh Gowda N M, Yadu Kiran, Dr. S.S Parthasarthy, "Modelling of Buck DC-DC Converter Using Simulink," IJIRSET, vol. 3, p.14965-p.14975, July 2014.

[5] Carmen Parisi, "Multiphase Buck Design from Start to Finish (part 1)," Texas Instruments Application Report, April 2017.

[6] I.Poole, "PLL Phase Detector / Comparator," Op Amp Gain | Operational Amplifier Calculation Equations | Radio-Electronics.com. [Online]. Available: https://www.radio-electronics.com/info/rf-technology-design/pll-synthesizers/phase-locked-loop-detector.php. [Accessed: 18-Dec-2018].

[7] Kae Wong, David Evans, "Merits of Multiphase Buck DC/DC Converter in Small Form Factor Applications" Texas Instruments, March 2015.

[8] Arvind Raj, "Calculating efficiency", Texas Instruments Application Report Feb 2010

[9] Chauhan, P., Rajpurohit, B., Singh, S. and Gonzalez-Longatt, F. (2014). RENEWABLE ENERGY INTEGRATION. [Place of publication not identified]: SPRINGER.

[10] Knight, D. (2018). Improving Efficiency in DC-DC Converters Through Careful Component Selection. [online] Digikey.com. Available at: https://www.digikey.com/en/maker/blogs/improving-efficiency-in-dc-dc-converters-through-careful-component-selection [Accessed 7 Dec. 2018].

[11] CSD17556Q5B Datasheet, Texas Instruments, Nov 2017.

[12] Human-memory.net. (2018). Neurons & Synapses - Memory & the Brain - The Human Memory. [online] Available at: http://www.human-memory.net/brain_neurons.html [Accessed 7 Dec. 2018].

[13] Khan Academy. (2018). *The synapse*. [online] Available at: https://www.khanacademy.org/science/biology/human-biology/neuron-nervous-system/a/the-synapse.

[14] Walkarn, U. (2016). A Quick Introduction to Neural Networks. [online] the data science blog. Available at: https://ujjwalkarn.me/2016/08/09/quick-intro-neural-networks/.

[15] Schmidt, A. (2018). Multilayer Neural Network. [online] Teco.edu. Available at: https://www.teco.edu/~albrecht/neuro/html/node18.html [Accessed 7 Dec. 2018].

[16] Kang, N. (2018). Multi-Layer Neural Networks with Sigmoid Function— Deep Learning for Rookies (2). [online] Towards Data Science. Available at: https://towardsdatascience.com/multi-layer-neural-networks-with-sigmoid-function-deep-learning-for-rookies-2-bf464f09eb7f [Accessed 7 Dec. 2018].

[17] H. Jaeger, "Echo state network," Scholarpedia. [Online]. Available: http://www.scholarpedia.org/article/Echo_state_network. [Accessed: 07-Dec-2018].

[18] J. Dai, G. K. Venayagamoorthy, and R. G. Harley, "Harmonic identification using an Echo State Network for adaptive control of an active filter in an electric ship," 2009 International Joint Conference on Neural Networks, 2009.

[19] Jubayer Alam Rabin, Safayet Hossain, Solaiman Ahsan, Abu Shahab Mollan, N. M Enamul Kabir, Shahjahan, "Electrical load forecasting using echo state network" *International Conference on Computer and Information Technology*, p. 22-24, Dec 2012.

[20] Jinbang Xu, Jun Yang, Feng Liu, Zhixiong Zhang, Anwen Shen "Echo State Networks Based Method for Harmonic Extraction in Shunt Active Power Filters" *International Conference on Bio-Inspired Computing.* P.27-29, Sept 2011.

[21] Jubayer Alam Rabin, Safayet Hossain, Solaiman Ahsan, Abu Shahab Mollah, Tawabur Rahman, "Sensitivity learning oriented nonmonotonic multi reservoir echo state network for short-term load forecasting" *International Conference on Informatics, Electronics and Vision*, p. 17-18, May 2013.