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Wang et al.

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(45) **Date of Patent: May 23, 2017**

(54) **METHOD AND APPARATUS TO IMPROVE POWER DEVICE RELIABILITY**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **15/178,278**

(22) Filed: **Jun. 9, 2016**

(65) **Prior Publication Data**

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Related U.S. Application Data

(63) Continuation-in-part of application No. 15/009,867, filed on Jan. 29, 2016, which is a continuation-in-part of application No. 14/724,408, filed on May 28, 2015, now Pat. No. 9,503,079.

(51) **Int. Cl.**
H03B 1/00 (2006.01)
H03K 17/687 (2006.01)

(52) **U.S. Cl.**
CPC ***H03K 17/687*** (2013.01)

(58) **Field of Classification Search**
CPC H03K 17/687
See application file for complete search history.

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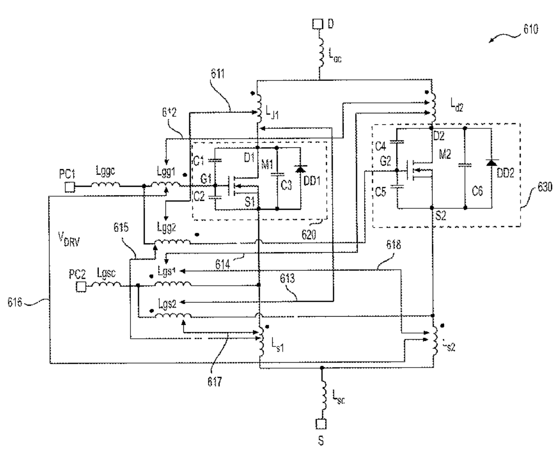
Primary Examiner — Daniel Puentes
(74) *Attorney, Agent, or Firm* — Oblon, McClelland, Maier & Neustadt, L.L.P.

(57) **ABSTRACT**

Aspects of the disclosure provide a power device that includes an upper power module and a lower power module. The upper power module and the lower power module are coupled in series between two supply voltages, and are respectively controlled by a first control signal and a second control signal. Interconnections of the power device are inductively coupled to prevent reliability issues, such as crosstalk, self turn on, self sustained oscillation, and the like.

19 Claims, 19 Drawing Sheets



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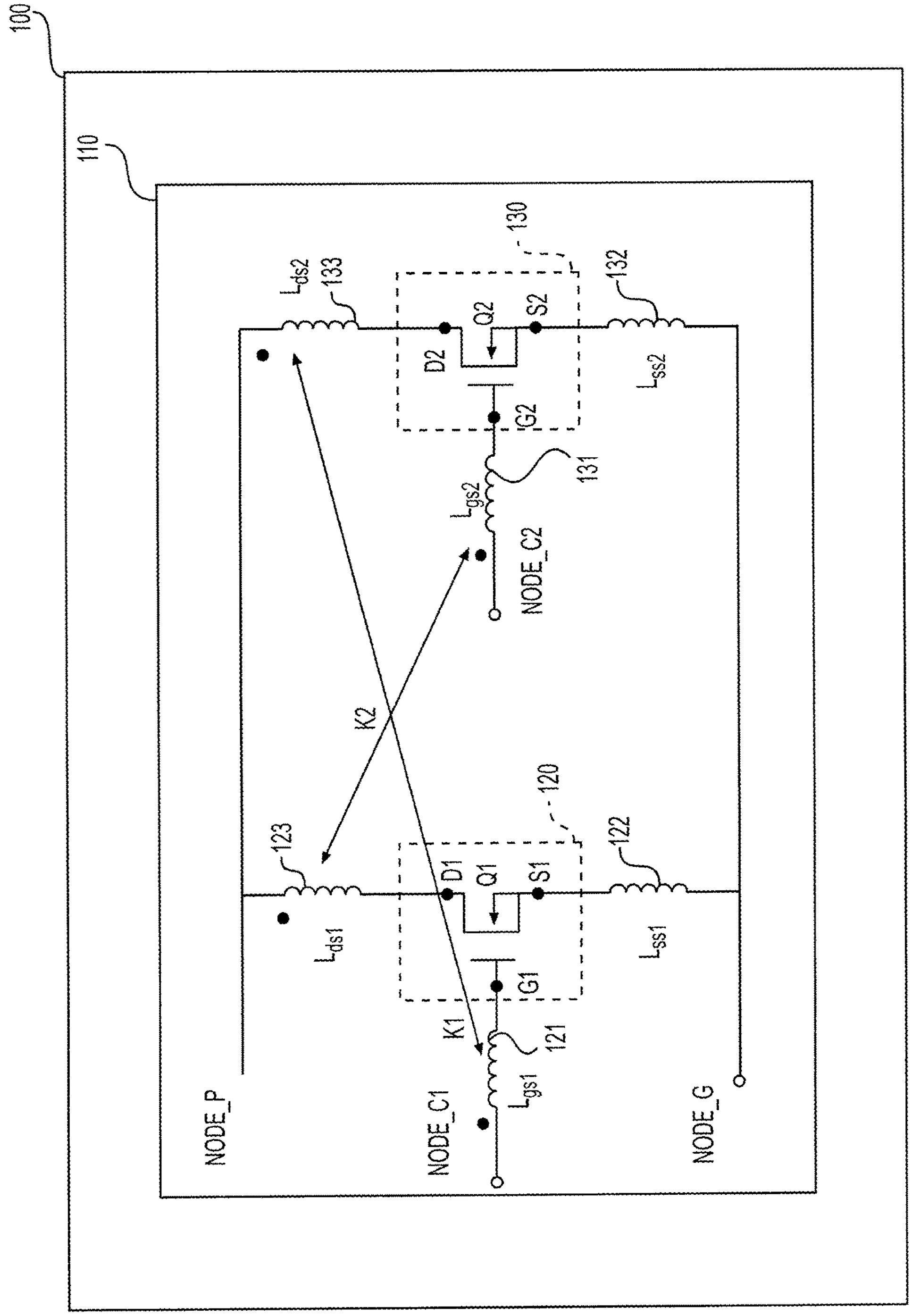

100
110
130
120
Lds2
133
132
Q2
S2
D2
G2
Lss2
131
Lgs2
NODE_C2
K2
123
122
D1
Q1
S1
Lds1
Lss1
G1
K1
121
Lgs1
NODE_P
NODE_C1
NODE_G

FIG. 1

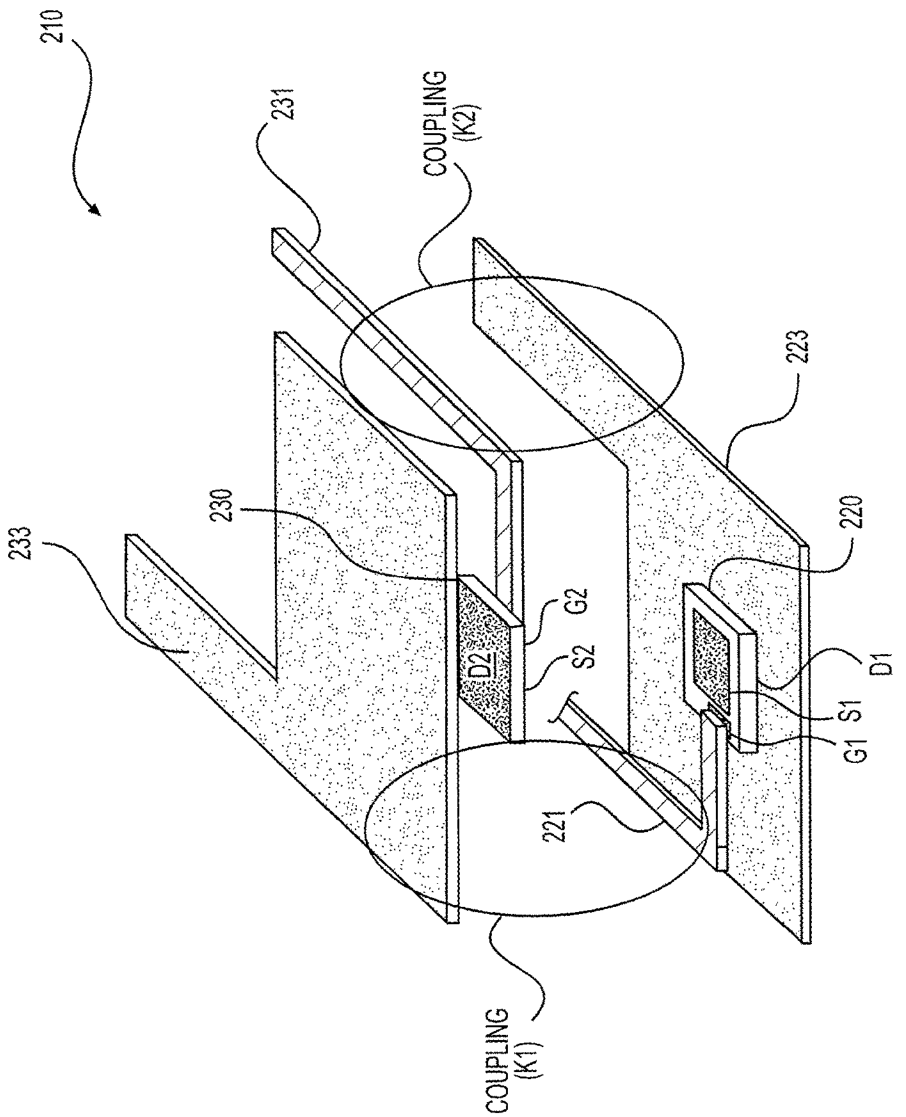

210
231
COUPLING
(K2)
223
233
230
G2
S2
D2
220
D1
S1
G1
221
COUPLING
(K1)

FIG. 2

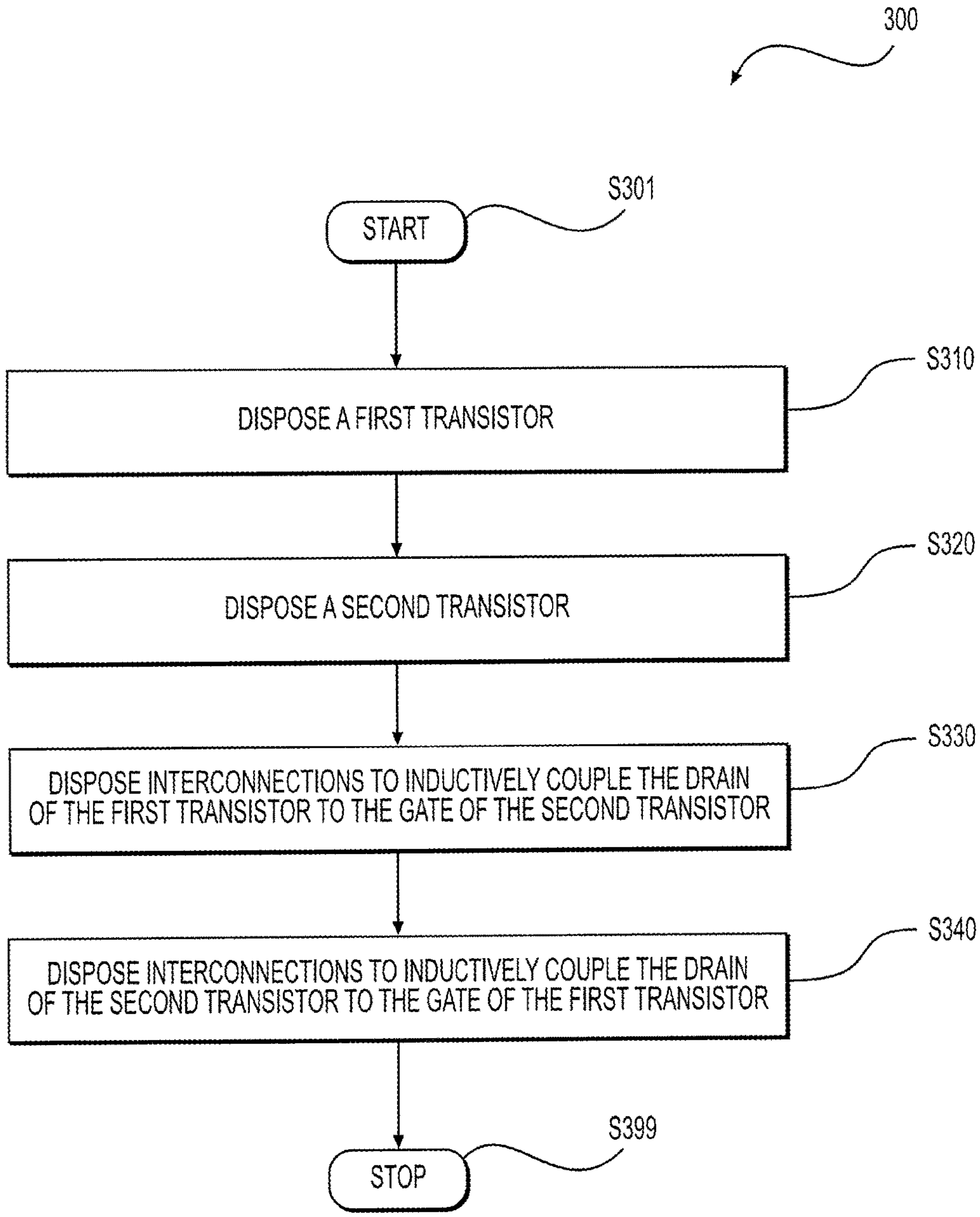

300
S301
START
S310
DISPOSE A FIRST TRANSISTOR
S320
DISPOSE A SECOND TRANSISTOR
S330
DISPOSE INTERCONNECTIONS TO INDUCTIVELY COUPLE THE DRAIN OF THE FIRST TRANSISTOR TO THE GATE OF THE SECOND TRANSISTOR
S340
DISPOSE INTERCONNECTIONS TO INDUCTIVELY COUPLE THE DRAIN OF THE SECOND TRANSISTOR TO THE GATE OF THE FIRST TRANSISTOR
S399
STOP

FIG. 3

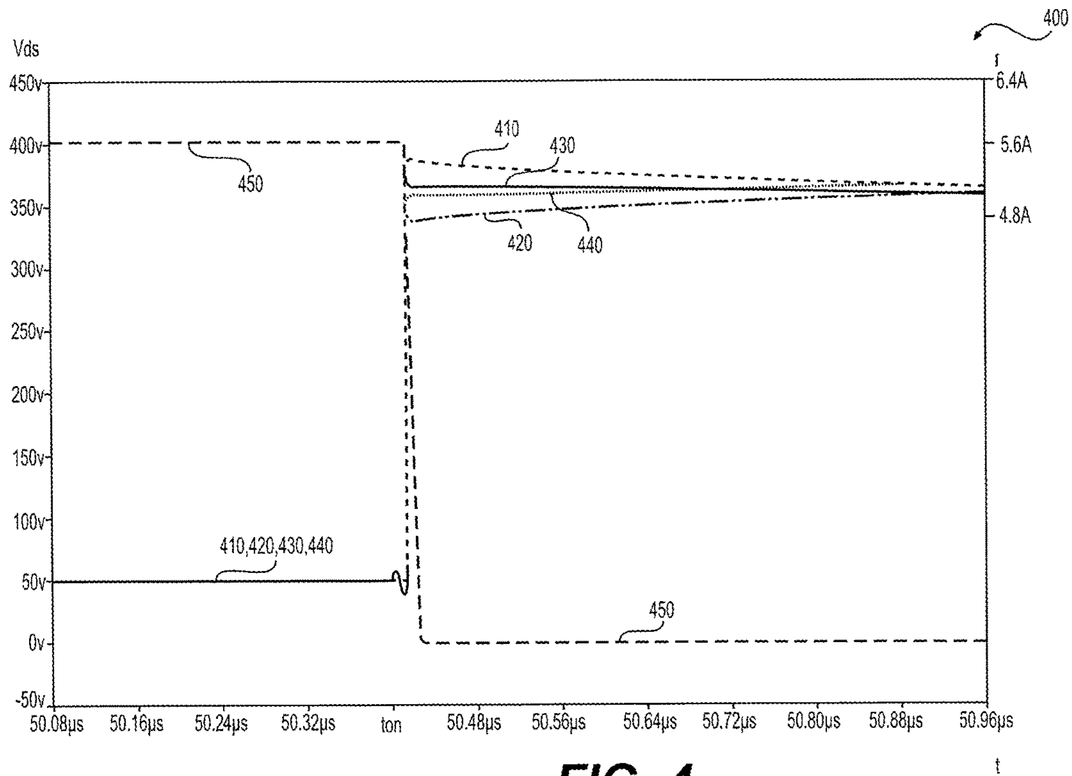

400
Vds
I
450v
400v
350v
300v
250v
200v
150v
100v
50v
0v
-50v
6.4A
5.6A
4.8A
410
430
450
420
440
410,420,430,440
450
50.08µs
50.16µs
50.24µs
50.32µs
ton
50.48µs
50.56µs
50.64µs
50.72µs
50.80µs
50.88µs
50.96µs
t

FIG. 4

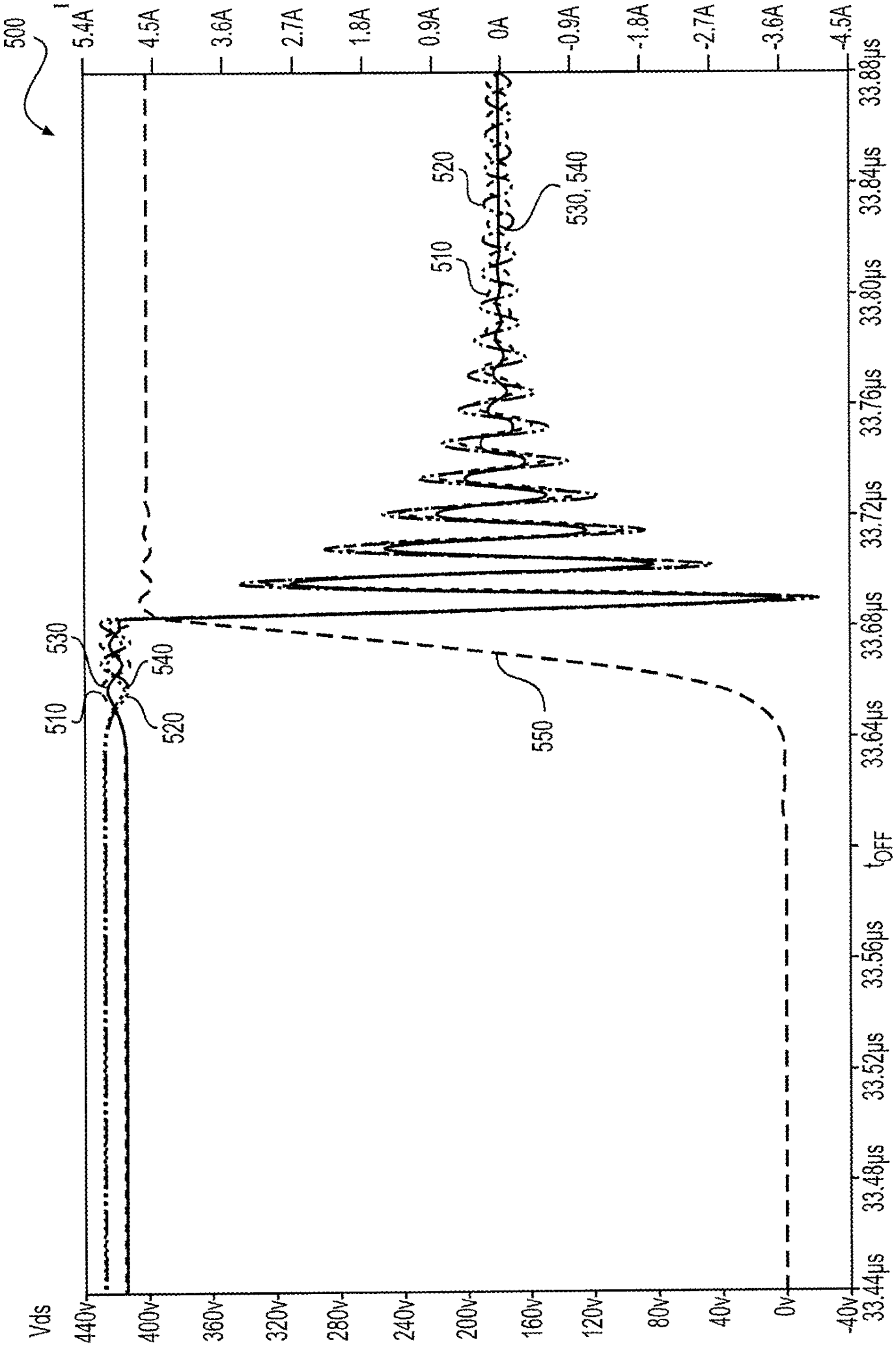

500
Vds
440v
400v
360v
320v
280v
240v
200v
160v
120v
80v
40v
0v
-40v
I
5.4A
4.5A
3.6A
2.7A
1.8A
0.9A
0A
-0.9A
-1.8A
-2.7A
-3.6A
-4.5A
33.44µs
33.48µs
33.52µs
33.56µs
t_{OFF}
33.64µs
33.68µs
33.72µs
33.76µs
33.80µs
33.84µs
33.88µs
510
530
540
520
550
510
520
530, 540

FIG. 5

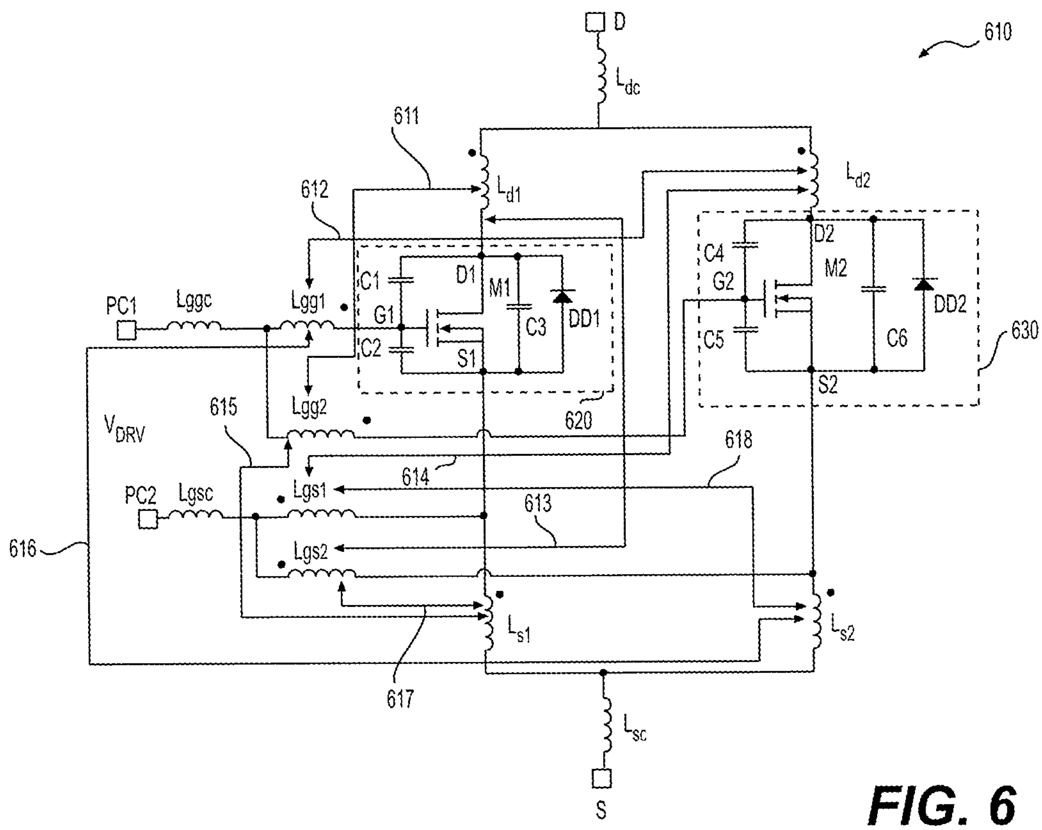
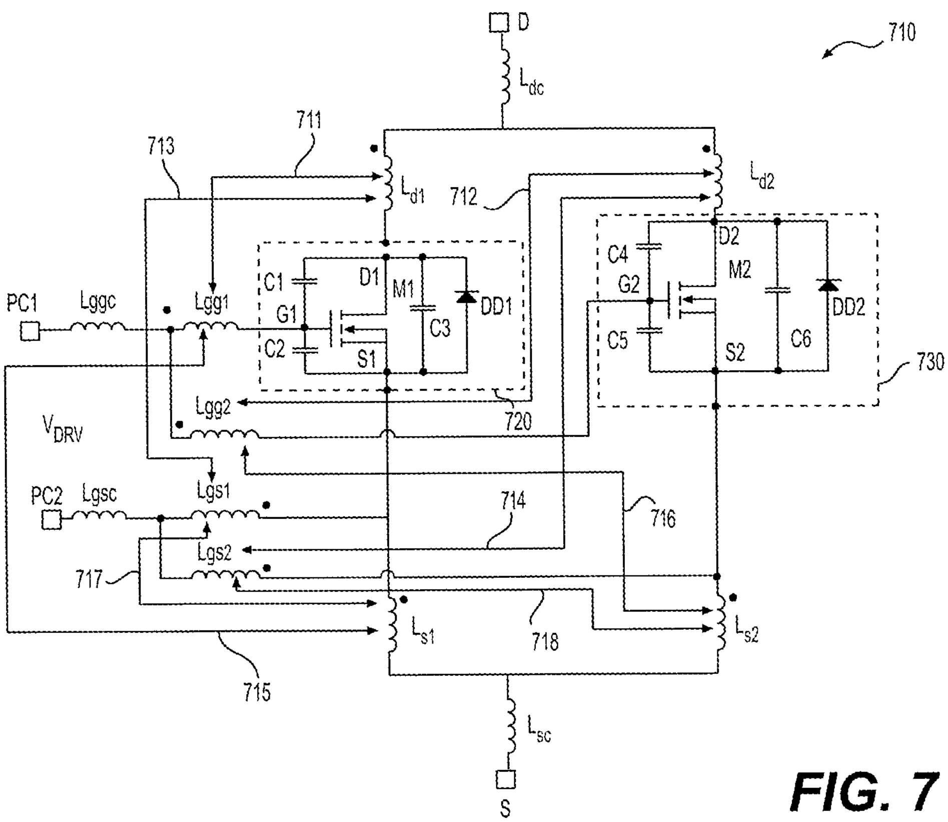

D
610
L_{dc}
611
L_{d1}
L_{d2}
612
D2
C4
C1
D1
M1
M2
G2
PC1
Lggc
Lgg1
G1
DD1
DD2
C3
C5
C6
630
C2
S1
S2
Lgg2
620
V_{DRV}
615
618
614
Lgs1
PC2
Lgsc
613
616
Lgs2
L_{s1}
L_{s2}
617
L_{sc}
S

FIG. 6



D
710
Ldc
711
713
Ld1
712
Ld2
D2
C4
C1
D1
M1
M2
G2
PC1
Lggc
Lgg1
G1
C3
DD1
DD2
C2
S1
C5
S2
C6
730
Lgg2
720
VDRV
716
714
PC2
Lgsc
Lgs1
Lgs2
717
Ls1
718
Ls2
715
Lsc
S

FIG. 7

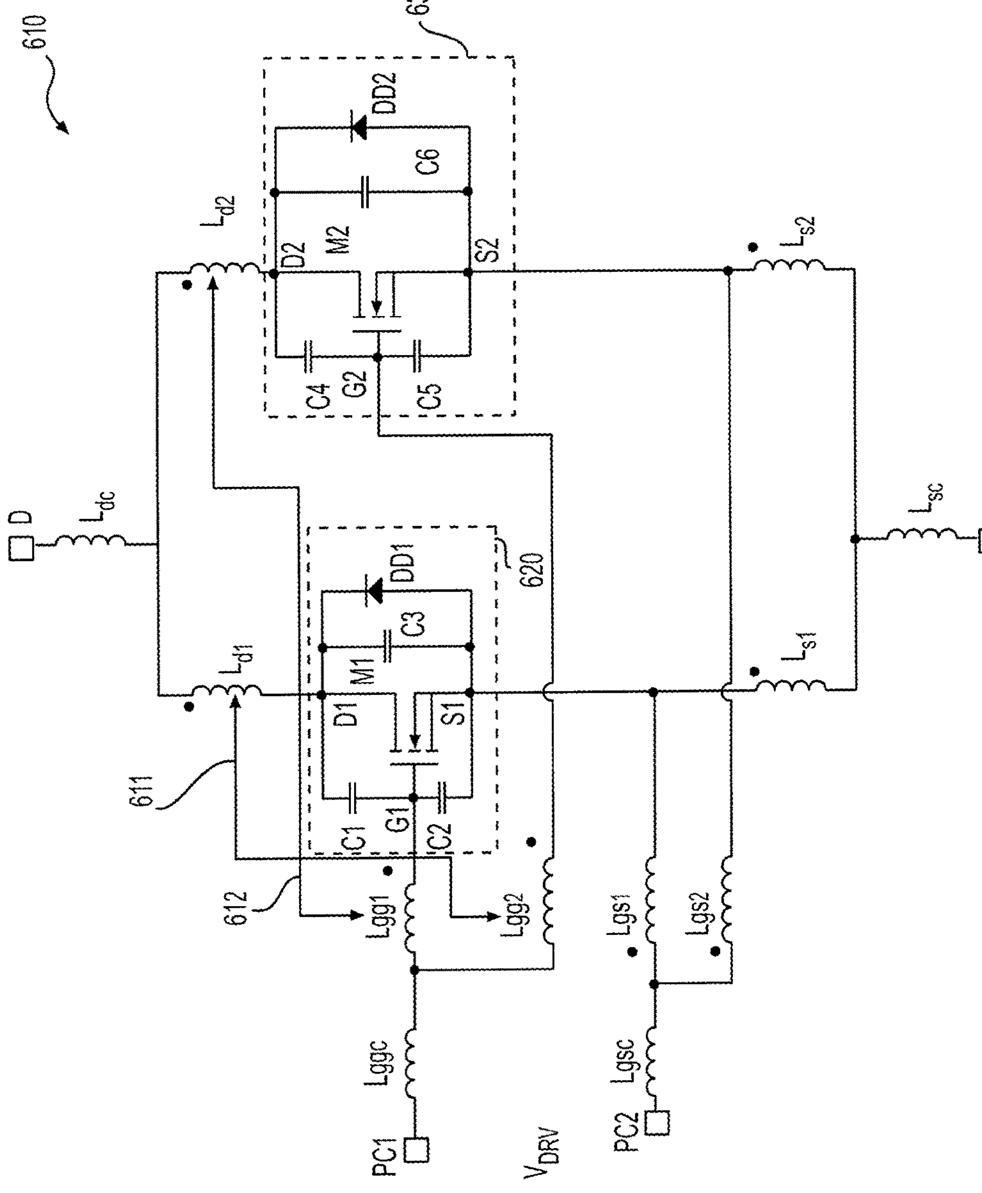

610
630
620
611
612
DD2
C6
D2
M2
S2
C4
G2
C5
DD1
C3
D1
M1
S1
C1
G1
C2
D
S
PC1
PC2
Lggc
Lgsc
Lgg1
Lgg2
Lgs1
Lgs2
V_{DRV}
L_{dc}
L_{d1}
L_{d2}
L_{s1}
L_{s2}
L_{sc}

FIG. 8A

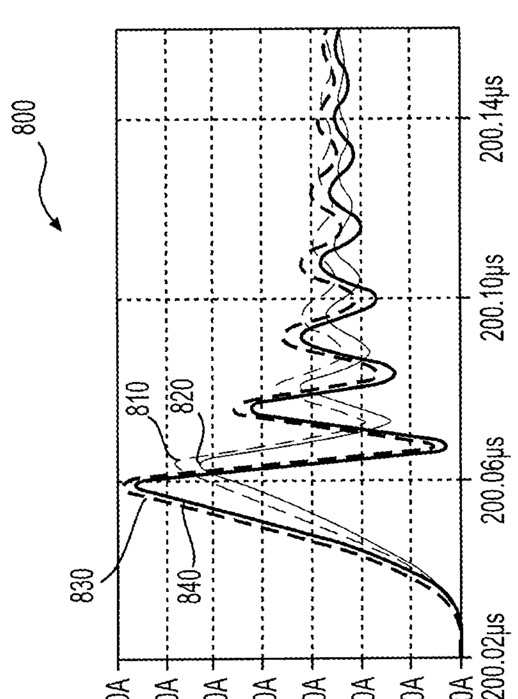

800
810
820
830
840
140A
120A
100A
80A
60A
40A
20A
0A
200.02µs
200.06µs
200.10µs
200.14µs

FIG. 8B

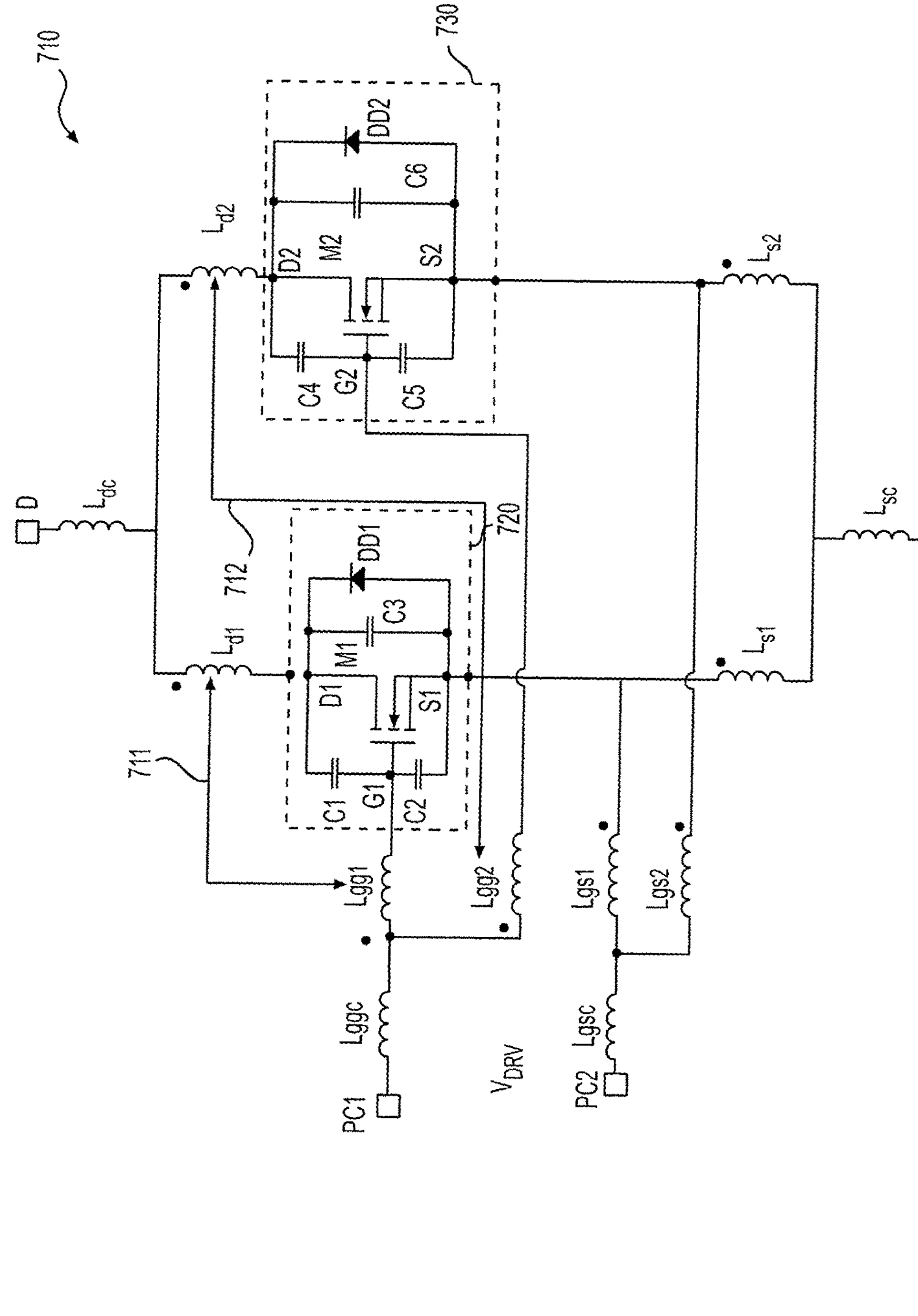

710
730
DD2
C6
L_{d2}
D2
M2
S2
C4
G2
C5
D
L_{dc}
712
720
DD1
C3
M1
L_{d1}
D1
S1
711
C1
G1
C2
L_{s2}
L_{sc}
S
L_{s1}
Lgg1
Lgg2
Lgs1
Lgs2
Lggc
Lgsc
V_{DRV}
PC1
PC2

FIG. 9A

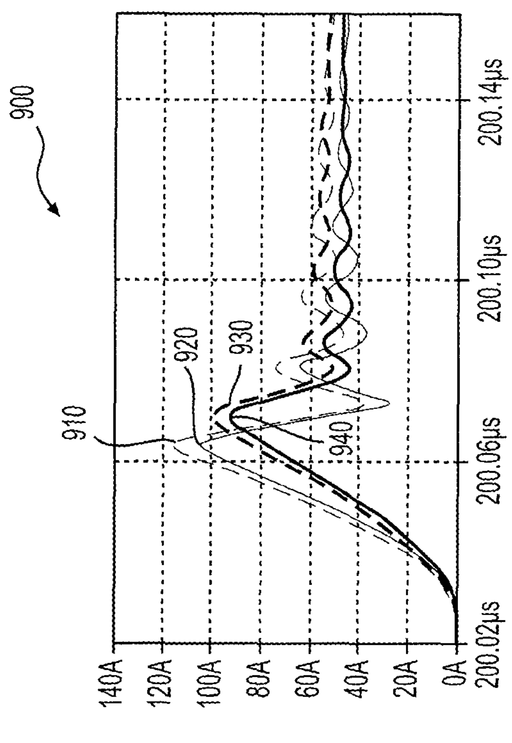

900
910
920
930
940
140A
120A
100A
80A
60A
40A
20A
0A
200.02µs
200.06µs
200.10µs
200.14µs

FIG. 9B

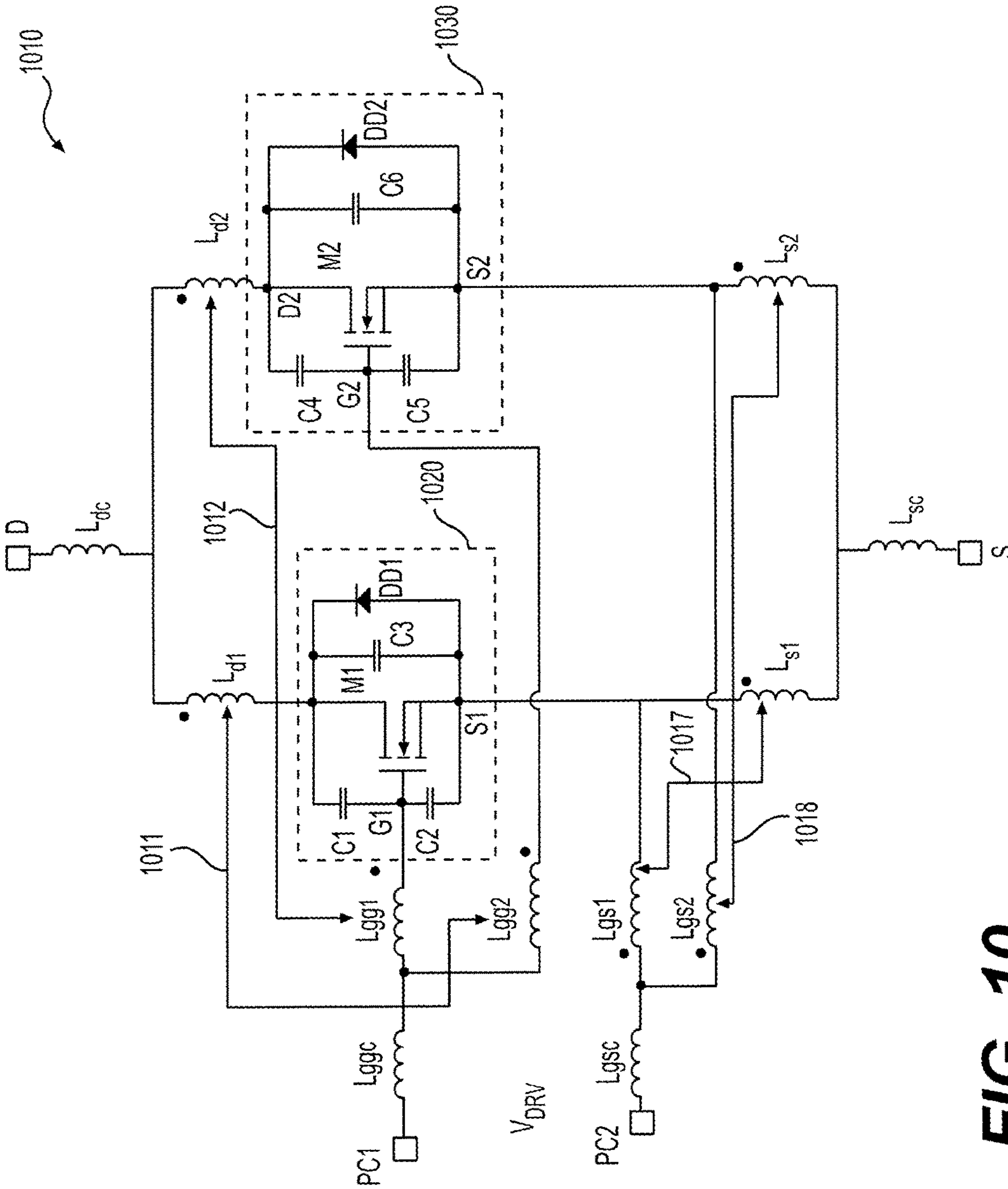

1010
1030
DD2
C6
M2
S2
D2
L_{d2}
C4
G2
C5
1020
DD1
C3
M1
S1
L_{d1}
C1
G1
C2
1011
1012
D
L_{dc}
L_{s2}
L_{s1}
L_{sc}
S
1017
1018
Lgg1
Lgg2
Lgs1
Lgs2
Lggc
Lgsc
PC1
PC2
V_{DRV}

FIG. 10

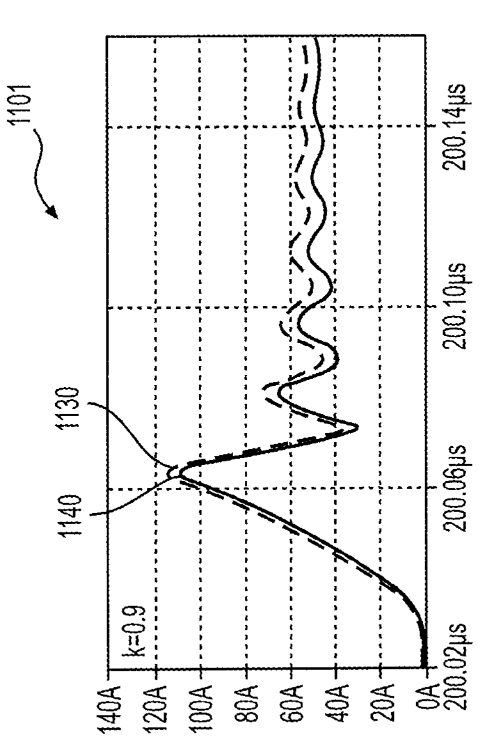


FIG. 11B

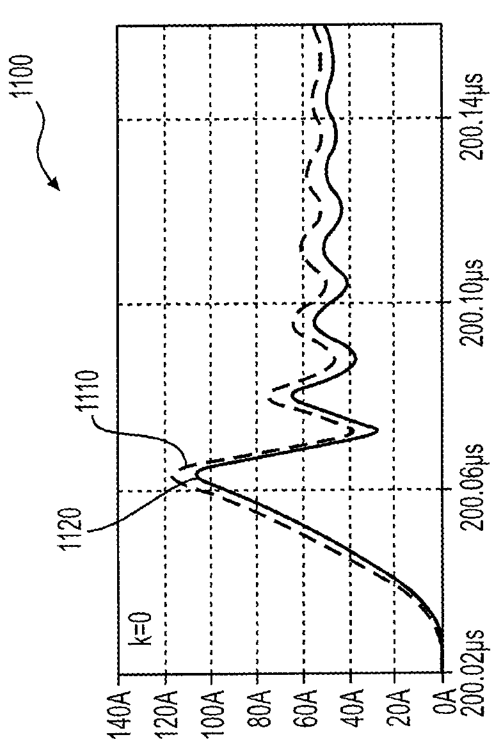


FIG. 11A

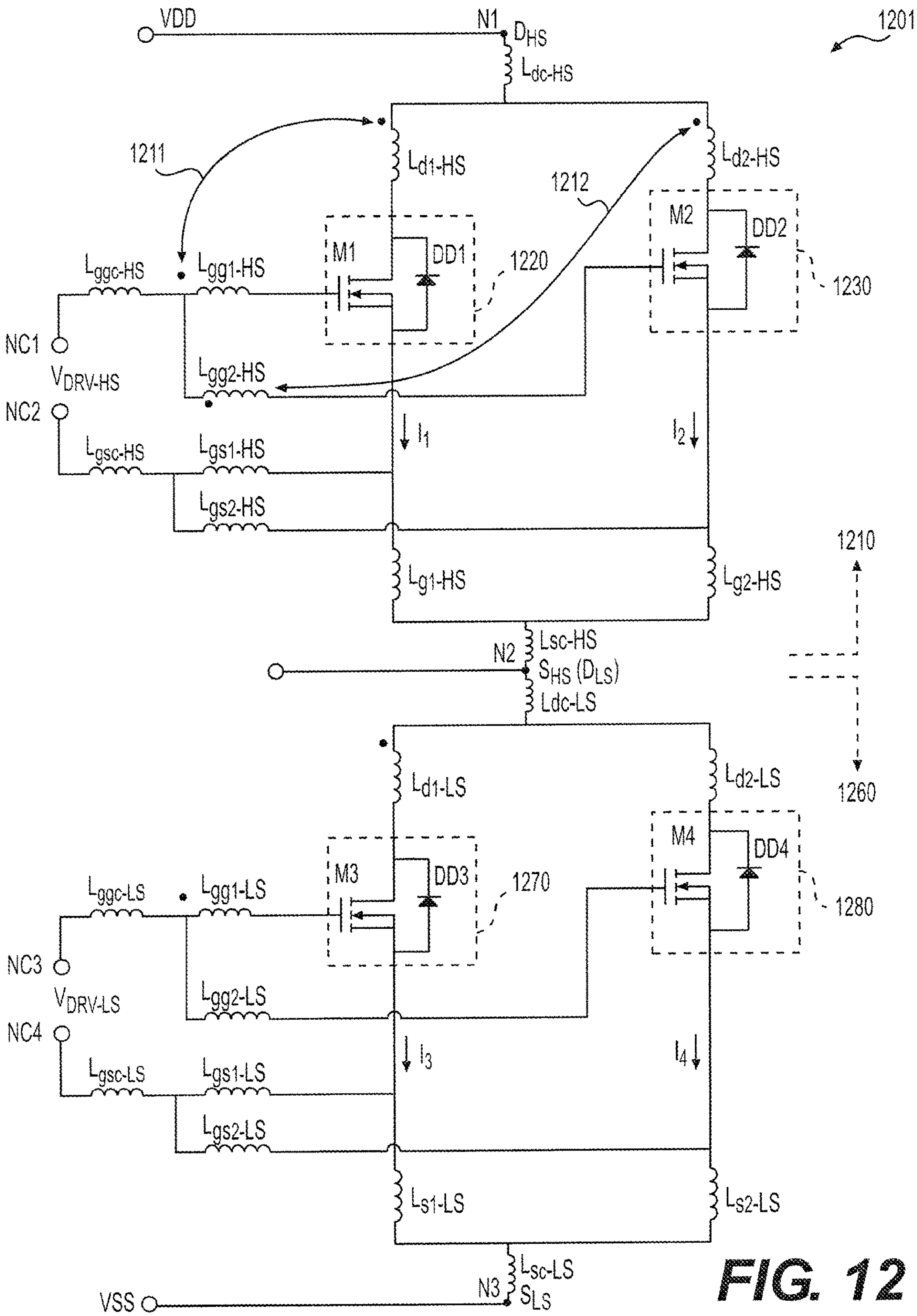

VDD
N1
D_{HS}
L_{dc-HS}
1201
1211
L_{d1-HS}
L_{d2-HS}
1212
M2
DD2
M1
DD1
1220
1230
L_{ggc-HS}
L_{gg1-HS}
NC1
V_{DRV-HS}
L_{gg2-HS}
NC2
I_1
I_2
L_{gsc-HS}
L_{gs1-HS}
L_{gs2-HS}
1210
L_{g1-HS}
L_{g2-HS}
Lsc-HS
N2
S_{HS} (D_{LS})
Ldc-LS
L_{d1-LS}
L_{d2-LS}
1260
M4
DD4
M3
DD3
1270
1280
L_{ggc-LS}
L_{gg1-LS}
NC3
V_{DRV-LS}
L_{gg2-LS}
NC4
I_3
I_4
L_{gsc-LS}
L_{gs1-LS}
L_{gs2-LS}
L_{s1-LS}
L_{s2-LS}
L_{sc-LS}
N3
S_{LS}
VSS

FIG. 12

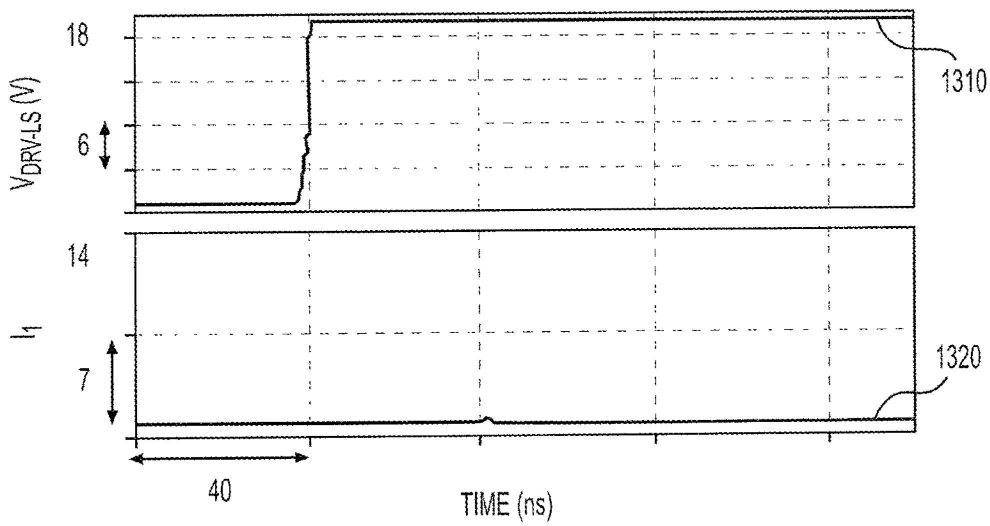


FIG. 13A

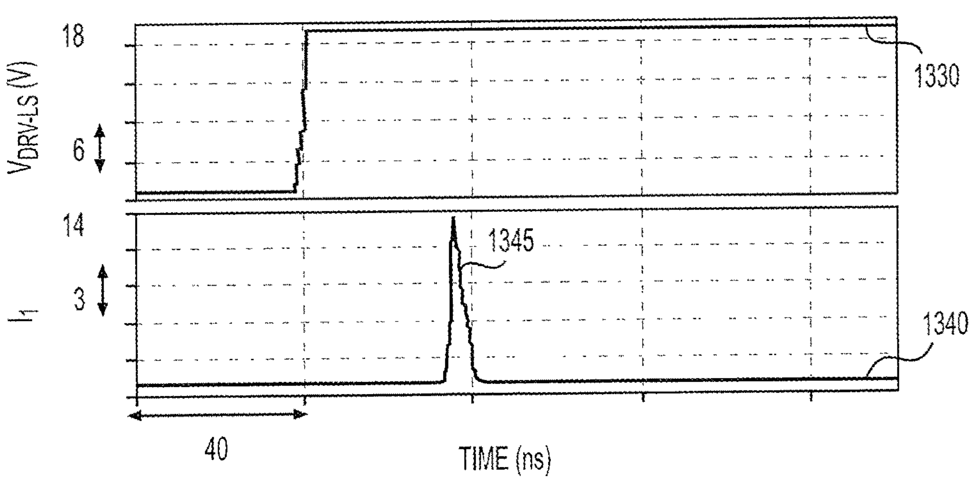
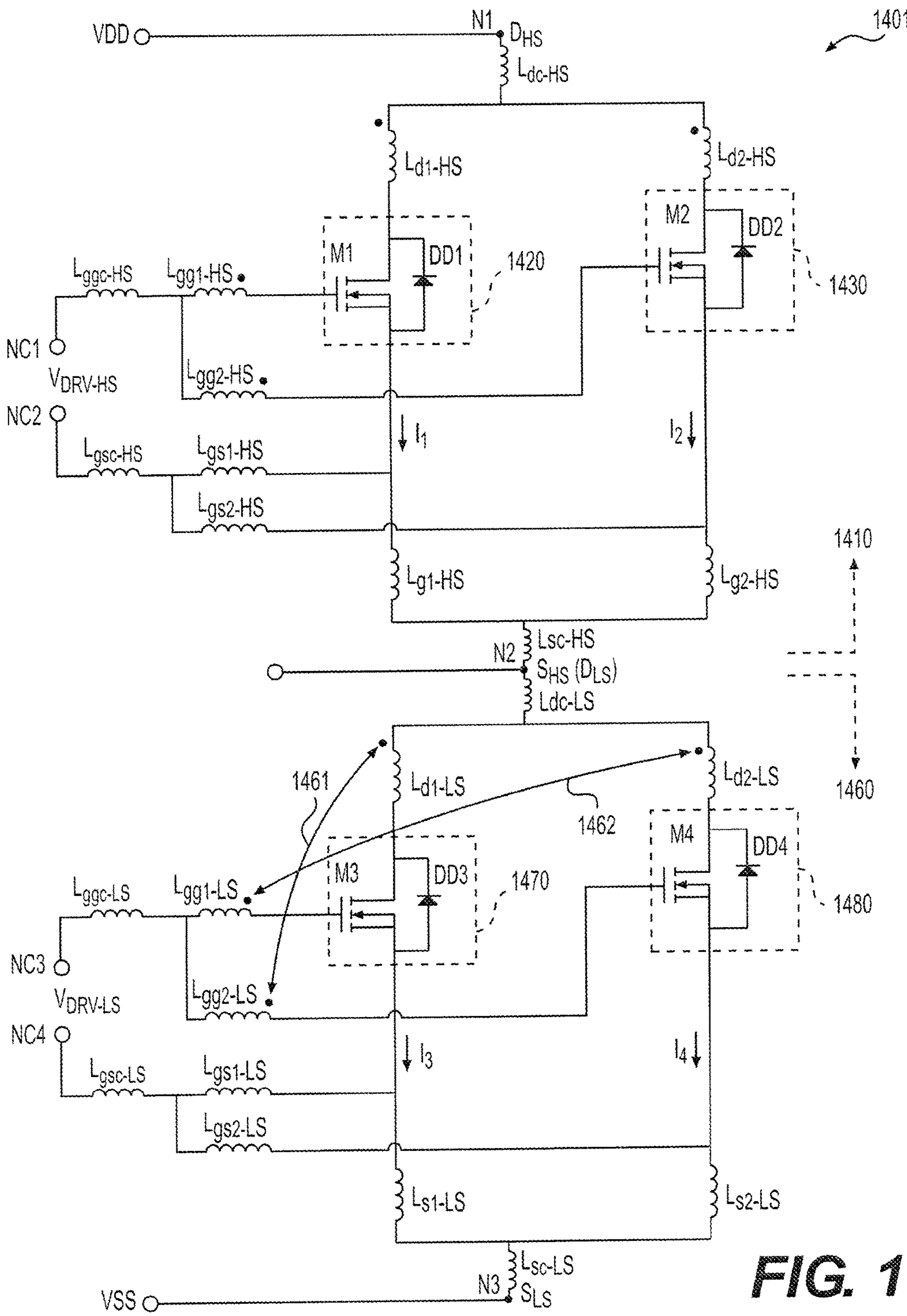


FIG. 13B



1401
VDD
N1
D_HS
L_dc-HS
L_d1-HS
L_d2-HS
M1
DD1
1420
M2
DD2
1430
L_ggc-HS
L_gg1-HS
L_gg2-HS
NC1
V_DRV-HS
NC2
L_gsc-HS
L_gs1-HS
L_gs2-HS
I_1
I_2
L_g1-HS
L_g2-HS
1410
Lsc-HS
N2
S_HS (D_LS)
Ldc-LS
L_d1-LS
L_d2-LS
1461
1462
1460
M3
DD3
1470
M4
DD4
1480
L_ggc-LS
L_gg1-LS
L_gg2-LS
NC3
V_DRV-LS
NC4
L_gsc-LS
L_gs1-LS
L_gs2-LS
I_3
I_4
L_s1-LS
L_s2-LS
L_sc-LS
N3
S_LS
VSS

FIG. 14

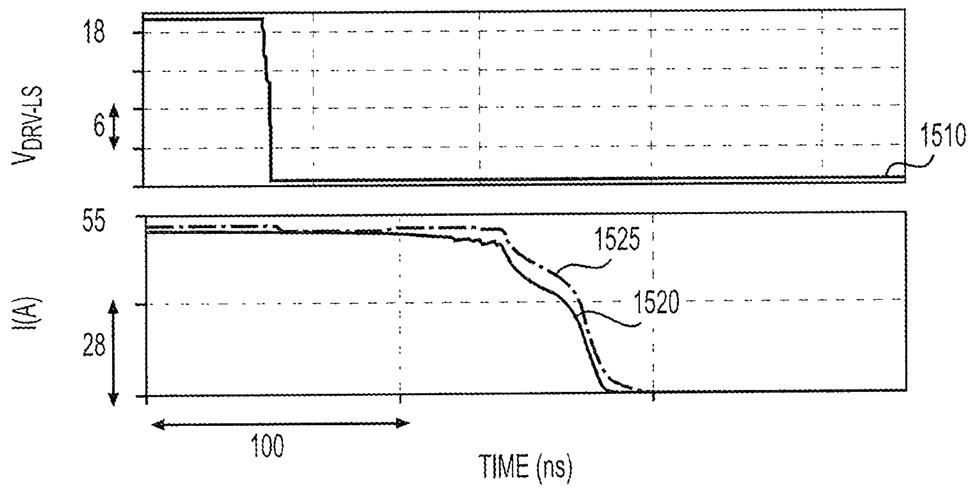


FIG. 15A

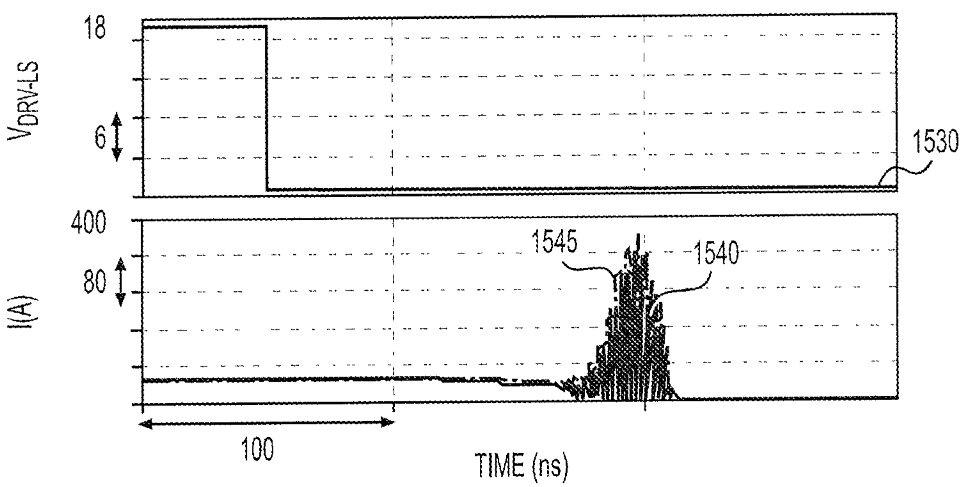


FIG. 15B

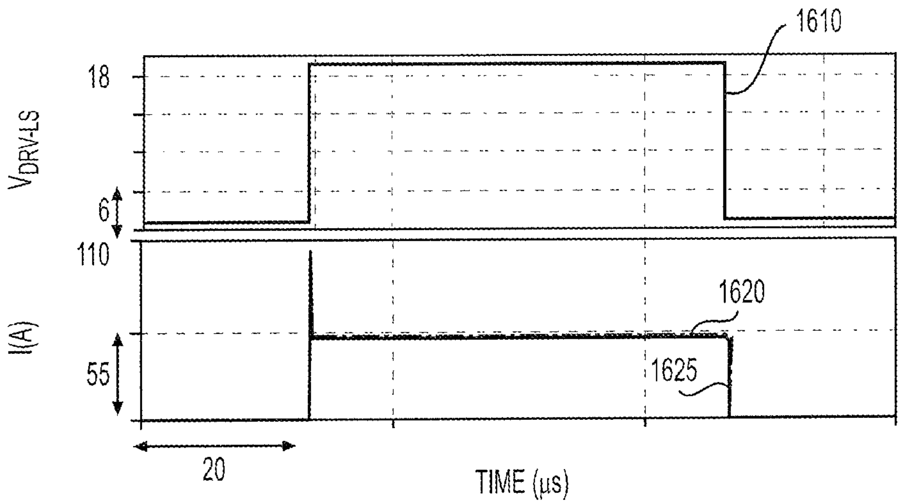


FIG. 16A

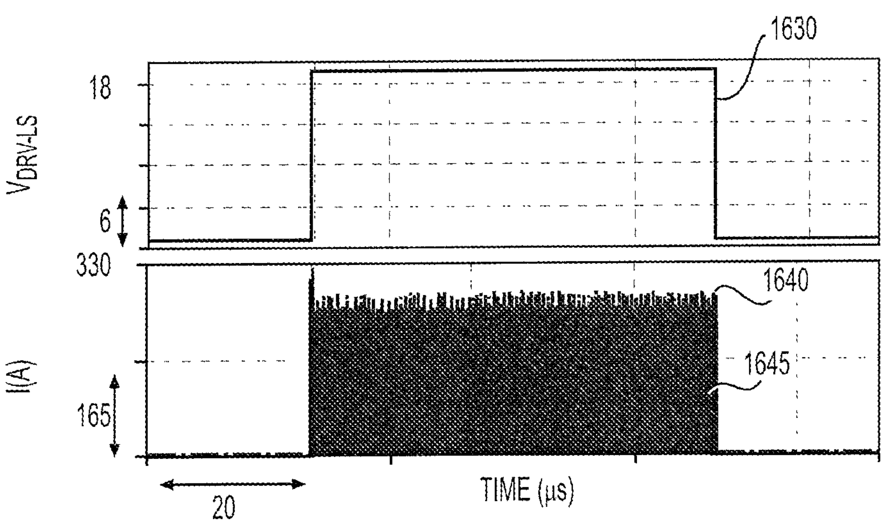


FIG. 16B

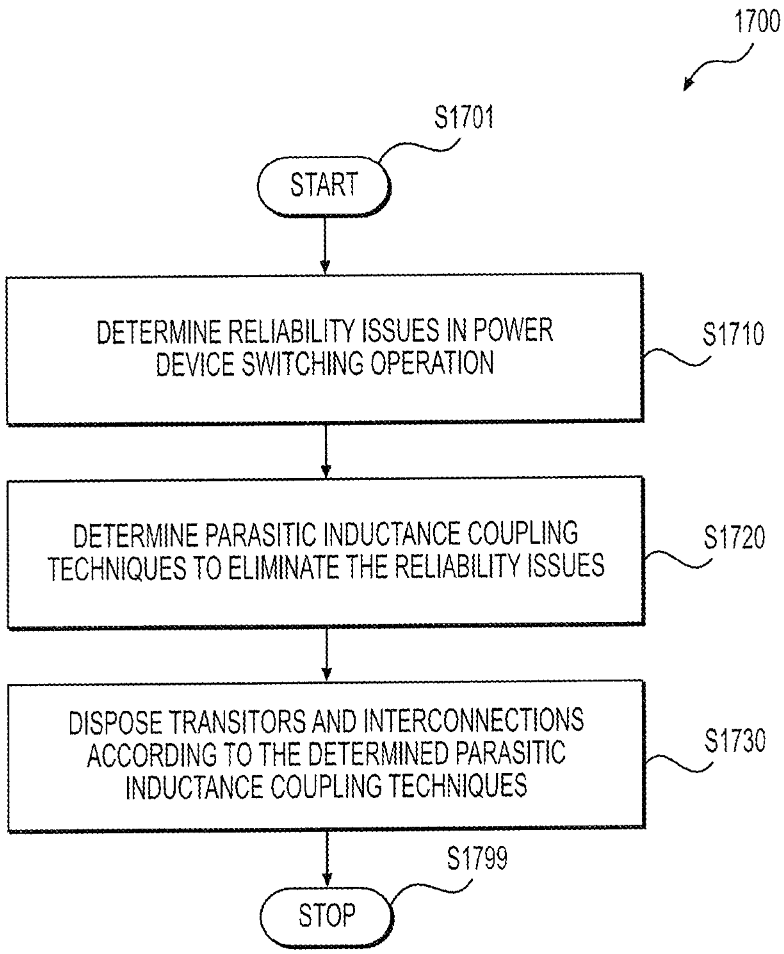

1700
S1701
START
DETERMINE RELIABILITY ISSUES IN POWER DEVICE SWITCHING OPERATION
S1710
DETERMINE PARASITIC INDUCTANCE COUPLING TECHNIQUES TO ELIMINATE THE RELIABILITY ISSUES
S1720
DISPOSE TRANSITORS AND INTERCONNECTIONS ACCORDING TO THE DETERMINED PARASITIC INDUCTANCE COUPLING TECHNIQUES
S1730
S1799
STOP

FIG. 17

METHOD AND APPARATUS TO IMPROVE POWER DEVICE RELIABILITY

INCORPORATION BY REFERENCE

This application is a continuation-in-part (CIP) application of U.S. patent application Ser. No. 15/009,867, "METHOD AND APPARATUS FOR CURRENT/POWER BALANCING", filed Jan. 29, 2016, which in turn is a continuation-in-part (CIP) application of U.S. patent application Ser. No. 14/724,408, "Method and Apparatus for Current/Power Balancing" filed on May 28, 2015. The entire disclosure of the above-identified applications is incorporated herein by reference in their entirety.

BACKGROUND

The background description provided herein is for the purpose of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent the work is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present disclosure.

A power module may use parallel power components to increase power capacity. For the parallel power components, equalizing current/power among the power components provides various benefits, such as improving component utilization, saving cost, improving system reliability. In an example, to equalize current/power among parallel power components, U.S. Patent Application Publication 2012/0235663 discloses a driver circuit to provide respective gate driver signals to drive the parallel power components.

SUMMARY

Aspects of the disclosure provide a power device that includes an upper power module and a lower power module. The upper power module is coupled to a first node, a second node and a first control node via first interconnections. The upper power module is controlled by a first driving signal at the first control node to turn on/off a first current path between the first node that receives a first supply voltage and the second node. The lower power module is coupled to the second node, a third node and a second control node via second interconnections. The lower power module is controlled by a second driving signal at the second control node to turn on/off a second path between the second node and the third node that receives a second supply voltage that is lower than the first voltage. A first interconnection and a second interconnection of the first interconnections are inductively coupled to prevent a turn-on of the upper power module when the first driving signal is at a first voltage level to turn off the upper power module and the second control signal is at a second voltage level to turn on the lower power module. In an example, the first driving signal transits to the first voltage level to turn off the upper power module before the second driving signal transits to the second voltage level to turn on the lower power module.

According to an aspect of the disclosure, the upper power module includes a first switch circuit in parallel with a second switch circuit. The first switch circuit and the second switch circuit are coupled to the first node, the second node and the first control node via the first interconnections. The lower power module includes a third switch circuit in parallel with a fourth switch circuit. The third switch circuit and the fourth switch circuit are coupled to the second node, the third node and the second control node via the second interconnections.

In an example, the first switch circuit includes a first SiC metal-oxide-semiconductor field effect transistor, the second switch circuit includes a second SiC metal-oxide-semiconductor field effect transistor, the third switch circuit includes a third SiC metal-oxide-semiconductor field effect transistor, and the fourth switch circuit includes a fourth SiC metal-oxide-semiconductor field effect transistor.

In an embodiment, the first interconnection and the second interconnection are among interconnections that interconnect the first switch circuit to the first node, the second node, and the first control node. In an example, parasitic inductances introduced by the first interconnection and the second interconnection are in an inversely coupled state. Further, the first interconnection interconnects a gate terminal of the first switch circuit to the first control node, and the second interconnection interconnects a drain terminal of the first switch circuit to the first node.

Aspects of the disclosure provide a power device that includes an upper power module and a lower power module. The upper power module is coupled to a first node, a second node and a first control node via first interconnections. The upper power module is controlled by a first driving signal at the first control node to turn on/off a first current path between the first node that receives a first supply voltage and the second node. The lower power module is coupled to the second node, a third node and a second control node via second interconnections. The lower power module is controlled by a second driving signal at the second control node to turn on/off a second path between the second node and the third node that receives a second supply voltage that is lower than the first voltage. In an example, the second supply voltage is ground. In an embodiment, a first interconnection and a second interconnection of the second interconnections are inductively coupled to prevent self turn-on of the lower power module when the second driving signal is at a voltage level to turn off the lower power module. In another embodiment, a first interconnection and a second interconnection of the second interconnections are inductively coupled to prevent self sustained oscillation of the lower power module when the second driving signal is at a voltage level to turn on the lower power module.

According to an aspect of the disclosure, the upper power module includes a first switch circuit in parallel with a second switch circuit, the first switch circuit and the second switch circuit being coupled to the first node, the second node and the first control node via the first interconnections, and the lower power module includes a third switch circuit in parallel with a fourth switch circuit, the third switch circuit and the fourth switch circuit being coupled to the second node, the third node and the second control node via the second interconnections.

In an embodiment, the first switch circuit includes a first SiC metal-oxide-semiconductor field effect transistor, the second switch circuit includes a second SiC metal-oxide-semiconductor field effect transistor, the third switch circuit includes a third SiC metal-oxide-semiconductor field effect transistor, and the fourth switch circuit includes a fourth SiC metal-oxide-semiconductor field effect transistor.

In an example, the first interconnection and the second interconnection are among interconnections that interconnect the third switch circuit and the fourth switch to the second node, the third node, and the second control node. For example, parasitic inductances introduced by the first interconnection and the second interconnection are in a directly coupled state. Further, the first interconnection interconnects a gate terminal of the third switch circuit to the second control node, and the second interconnection interconnects a drain terminal of the fourth switch circuit to the second node.

BRIEF DESCRIPTION OF THE DRAWINGS

Various embodiments of this disclosure that are proposed as examples will be described in detail with reference to the following figures, wherein like numerals reference like elements, and wherein:

FIG. **1** shows a diagram of a system **100** according to an embodiment of the disclosure;

FIG. **2** shows an exploded view in a power module **210** according to an embodiment of the disclosure;

FIG. **3** shows a flow chart outlining a process example according to an embodiment of the disclosure;

FIGS. **4** and **5** show plots of simulation results according to an embodiment of the disclosure;

FIG. **6** shows a diagram of a power module **610** according to an embodiment of the disclosure;

FIG. **7** shows a diagram of a power module **710** according to an embodiment of the disclosure;

FIG. **8**A shows a diagram of the power module **610** for a simulation;

FIG. **8**B shows a plot of simulation results for the power module **610** in FIG. **8**A;

FIG. **9**A shows a diagram of the power module **710** for a simulation;

FIG. **9**B shows a plot of simulation results for the power module **710** in FIG. **9**A;

FIG. **10** shows a diagram of a power module **1010** according to an embodiment of the disclosure;

FIGS. **11**A-**11**B show plots of simulation results according to an embodiment of the disclosure;

FIG. **12** shows a diagram of a power device **1201** according to an embodiment of the disclosure;

FIGS. **13**A-**13**B show plots of simulation results according to an embodiment of the disclosure;

FIG. **14** shows a diagram of a power device **1401** according to an embodiment of the disclosure;

FIGS. **15**A-**15**B show plots of simulation results according to an embodiment of the disclosure;

FIGS. **16**A-**16**B show plots of simulation results according to an embodiment of the disclosure; and

FIG. **17** shows a flow chart outlining a process example according to an embodiment of the disclosure.

DETAILED DESCRIPTION OF EMBODIMENTS

FIG. **1** shows a diagram of a system **100** according to an embodiment of the disclosure. The system **100** includes a power module **110** that uses mutual inductance coupling to balance current and/or power in parallel components.

The system **100** can be any suitable system that requires a relatively large power, such as a hybrid vehicle, an electric vehicle, a wind energy system, a printing system, and the like. During operation, in an example, the power module **110** needs to provide a relatively large current, such as in the order of Ampere, in the order of tens of Amperes, in the order of hundreds of Amperes, more than hundreds of Amperes, and the like. In an embodiment, the power module **110** is configured to use parallel components to share the relatively large current load.

In an embodiment, the power module **110** includes a power converter circuit, such as a DC-to-AC inverter, an AC-to-DC rectifier, and the like, and is implemented using semiconductor switching devices. The semiconductor switching devices form a plurality of switchable current paths to share the current load. According to an aspect of the disclosure, the semiconductor switching devices may have wide parameter variations, such as threshold voltage (Vth) variations, on-resistance Rds(on) variations, and the like due to manufacturing process. The parameter variations can cause unbalanced current/power on the plurality of switchable current paths. According to an aspect of the disclosure, mutual inductance coupling is used to improve current/power balance among the plurality of switchable current paths.

In the FIG. **1** example, the power module **110** has one or more control nodes NODE_C**1**-NODE_C**2**, a first power node NODE_P and a second power node NODE_P. Further, the power module **110** includes a plurality of switch modules, such as a first switch module **120**, a second switch module **130** and the like that. The switch modules are coupled in parallel to the control nodes and the power nodes using interconnection components, such as wirebonds, busbars and the like. The switch modules are configured to switch on/off current paths between the first power node NODE_P and the second power node NODE_G based on control signals received at the control nodes NODE_C**1**-NODE_C**2**. In an example, the control nodes NODE_C**1**-NODE_C**2** are coupled, fbr example directly connected, together to receive a same control signal. In another example, the control nodes NODE_C**1**-NODE_C**2** are separate nodes to receive different control signals.

Each switch module can include one or more transistors. When multiple transistors are used in a switch module, the multiple transistors can be arranged in various topologies to act as a switch.

Specifically, in the FIG. **1** example, the first switch module **120** includes a first transistor Q**1**, and the second switch module **130** includes a second transistor Q**2**. The first transistor Q**1** and the second transistor Q**2** can be any suitable transistors, such as metal-oxide-semiconductor field effect transistors (MOSFET) and the like. In an example, the first transistor Q**1** and the second transistor Q**2** are SiC MOSFET transistors that may have relatively wide parameter variations due to manufacturing process.

Further, in the FIG. **1** example, the first transistor Q**1** has a gate terminal G**1**, a source terminal S**1** and a drain terminal D**1**. The gate terminal G**1** is coupled to the first control node NODE_C**1** via an interconnection component **121**, the drain terminal D**1** is coupled to the first power node NODE_P via an interconnection component **123**, and the source terminal S**1** is coupled to the second power node NODE_G via an interconnection component **122**. Similarly, the second transistor Q**2** has a gate terminal G**2**, a source terminal S**2** and a drain terminal D**2**. The gate terminal G**2** is coupled to the first control node NODE_C**2** via an interconnection component **131**, the drain terminal D**2** is coupled to the first power node NODE_P via an interconnection component **133**, and the source terminal S**2** is coupled to the second power node NODE_G via an interconnection component **132**.

According to an aspect of the disclosure, the interconnection components introduce parasitic inductances that influence the switching operation of the power module **110**. For example, the interconnection component **121** introduces an inductance L_{gs1}, the interconnection component **122** introduces an inductance L_{ss1}, the interconnection components **123** introduces an inductance L_{ds1}, the interconnection component **131** introduces an inductance L_{gs2}, the interconnection component **132** introduces an inductance L_{ss2} and the interconnection component **133** introduces an inductance L_{ds2}.

In addition, according to an aspect of the disclosure, the interconnection components are purposely mutual coupled to introduce mutual coupling parasitic inductances to balance current/power among the switch modules in the power module **110**. Specifically, in the FIG. **1** example, the interconnection component **121** and the interconnection component **133** are purposely mutually coupled to introduce a mutual coupling parasitic inductance having a mutual coupling coefficient K**1**; and the interconnection component **123** and the interconnection component **131** are purposely mutually coupled to introduce a mutual coupling parasitic inductance having a mutual coupling coefficient K**2**.

According to an aspect of the disclosure, the mutual coupling is suitably designed such as the mutual coupling parasitic inductance improves current/power balance among the switch modules. In the FIG. **1** example, when the mutual coupling coefficients K**1** and K**2** are negative values, the mutual coupling parasitic inductances can improve current/power balance among the switch modules in the power module **110**. In an example, at a time to switch on the first transistor Q**1** and the second transistor Q**2**, a first current flowing through the first transistor Q**1** (also flowing through the interconnection module **123**) increases faster and is larger than a second current flowing through the second transistor Q**2**. The mutual coupling inductance between the interconnection component **123** and the interconnection component **131** then causes a voltage increase at the gate terminal G**2** of the second transistor Q**2**, and thus turns on the second transistor Q**2** more, and increases the second current flowing through the second transistor Q**2**. When the second current flowing through the second transistor Q**2** (also flowing through the interconnection module **133**) increases faster and is larger than the first current flowing through the first transistor Q**1**, the mutual coupling inductance between the interconnection component **133** and the interconnection component **121** causes a voltage increase at the gate terminal G**1**, and thus turns on the first transistor Q**1** more, and increases the first current flowing through the first transistor Q**1**.

Similarly, at a time to switch off the first transistor Q**1** and the second transistor Q**2**, the transient current flowing through the first transistor Q**1** and the second transistor Q**2** is balanced due to the mutual inductance coupling.

According to an aspect of the disclosure, when the first transistor Q**1** and the second transistor Q**2** are SiC MOSFET transistors, the on-resistance Rds(on) of the SiC MOSFET transistor has positive temperature coefficient, and thus the SiC MOSFET transistors intrinsically have negative feedback. Variations of the on-resistance Rds(on) may cause unbalance in the steady-state current, and the negative feedback of the on-resistance Rds(on) self-balances the steady-state current in the first transistor Q**1** and the second transistor Q**2**.

Further, variations in the threshold voltage Vth may cause unbalance in the transient current. The threshold voltage Vth has negative temperature coefficient, and thus can cause a positive feedback and the unbalance in the transient current. The mutual inductance coupling technique can be used to balance the transient current at switching on/off time.

It is noted that the power module **110** can be implemented by various technology. In an example, switch modules, such as the first switch module **120**, the second switch module **130**, and the like, are implemented as bare dies, and the interconnection modules are implemented as wirebonds and/or busbars. The switch modules, the interconnection modules and other suitable components are assembled in a package to form the power module **110**. In another example, the switch modules are discrete devices that are assembled in separate packages, and the switch modules are interconnected by wirebonds and busbars. In another example, the switch modules are integrated on an integrated circuit (IC) chip, and the interconnection modules are implemented as wirebonds on the IC chip using IC manufacturing technology.

FIG. **2** shows a plot for an exploded view in a power module **210** according to an embodiment of the disclosure. In an embodiment, the power module **110** in FIG. **1** is implemented as the power module **210** in FIG. **2**. The power module **210** includes switch modules, such as a first switch module **220**, a second switch module **230**, and the like that are implemented using bare dies. Further, the power module **210** includes interconnection modules, such as interconnection modules **221**, **223**, **231**, **233** and the like, that are implemented using busbars. The power module **210** is implemented in the form of a package in an example.

For example, the first switch module **220** is a first bare die having a first transistor implemented using a SiC MOSFET technology. Thus, the drain terminal D**1** of the first transistor is formed, for example as a bond pad, on the substrate of the first bare die, and the gate terminal G**1** and the source terminal S**1** of the first transistor are formed, for example as bond pads on the face side (opposite side of the substrate) of the first bare die.

Similarly, the second switch module **230** is a second bare die having a second transistor implemented using the SiC MOSFET technology. Thus, the drain terminal D**2** of the second transistor is formed, for example as a bond pad, on the substrate of the second bare die, and the gate terminal G**2** and the source terminal S**2** of the second transistor are formed, for example as bond pads, on the face side (opposite side of the substrate) of the second bare die.

In an embodiment, the first bare die and the second bare die are disposed face to face. The interconnection module **221** is connected to the gate terminal G**1** of the first transistor, the interconnection module **231** is connected to the gate terminal G**2** of the second transistor, the interconnection module **223** is connected to the drain terminal D**1** of the first transistor, and the interconnection module **231** is connected to the drain terminal D**2** of the second transistor.

Further, in the embodiment, the interconnection module **221** and the interconnection module **233** are disposed to have a mutual coupling parasitic inductance having a mutual coupling coefficient K**1**. For example, the interconnection module **221** and the interconnection module **233** are disposed nearby, such that a current change in one of the interconnection modules can induce a voltage on the other interconnection module. In addition, the interconnection module **231** and the interconnection module **223** are disposed to have a mutual coupling parasitic inductance having a mutual coupling coefficient K**2**. For example, the interconnection module **223** and the interconnection module **231** are disposed nearby, such that a current change in one of the interconnection modules can induce a voltage in the other interconnection module. In an example, the mutual coupling parasitic inductance is suitably designed to improve transient current/power balance at the time of switching on/off the first and second transistors.

It is noted that, for ease and simplicity, the power module **210** includes other suitable components that are not shown in FIG. **2**. For example, the source terminals S**1** and S**2** are connected by a suitable interconnection module not shown, such as a wirebond, a busbar and the like. It is also noted that, the configuration of the dies and the busbars in FIG. **2** can be suitably modified. For example, the two dies can be disposed in a back to back manner in an example, or can be disposed side by side in an example.

FIG. **3** shows a flow chart outlining a process **300** according to an embodiment of the disclosure. In an example, the process **300** is executed to implement the power module **210**. The process starts at S**301**, and proceeds to S**310**.

At S**310**, a first transistor is disposed. For example, the first transistor is implemented on a first bare die using the SiC MOSFET technology.

At S**320**, a second transistor is disposed. For example, the second transistor is implemented on a second bare die using the SiC MOSFET technology.

At S**330**, interconnections are disposed to inductively couple the drain terminal of the first transistor to the gate terminal of the second transistor. In the FIG. **2** example, the interconnection module **223** connects with the drain terminal of the first transistor, and the interconnection module **231** connects with the gate terminal of the second transistor. The interconnection module **223** and the interconnection module **231** are disposed, for example nearby, to be inductively coupled.

At S**340**, interconnections are disposed to inductively couple the drain terminal of the second transistor to the gate terminal of the first transistor. In the FIG. **2** example, the interconnection **233** module connects with the drain terminal of the second transistor, and the interconnection module **221** connects with the gate terminal of the first transistor. The interconnection module **233** and the interconnection module **221** are disposed, for example nearby, to be inductively coupled. Then the process proceeds to S**399** and terminates.

It is noted that the process **300** can include other suitable steps to implement a power module. Further, the steps in the process **300** can be executed at the same time or in a different order.

FIG. **4** shows a plot **400** of simulation result according to an embodiment of the disclosure. For example, the plot **400** shows voltage and current changes with or without mutual coupling parasitic inductance when a power module with parallel transistors is switched on. The X-axis shows time, and the Y-axis shows voltage and current values.

The plot **400** includes five waveforms **410-450**. The waveform **410** (in medium dashed line) shows drain current of the first transistor without mutual coupling parasitic inductance, the waveform **420** (in long-short dashed line) shows drain current of the second transistor without mutual coupling parasitic inductance, the waveform **430** (in solid line) shows drain current of the first transistor with mutual coupling parasitic inductance, the waveform **440** (in short dashed line) shows drain current of the second transistor with mutual coupling parasitic inductance, and the waveform **450** (in long dashed line) shows the drain-source voltage Vds.

As shown in FIG. **4**, at time ton, the first transistor and the second transistor are switched on. Without mutual coupling parasitic inductance, the transient current in the first transistor and the transient current in the second transistor have relatively large difference. With mutual coupling parasitic inductance, the transient current difference in the first transistor and the second transistor is reduced.

FIG. **5** shows a plot **500** of simulation result according to an embodiment of the disclosure. For example, the plot **500** shows voltage and current changes with or without mutual coupling parasitic inductance when a power module with parallel transistors is switched off. The X-axis shows time, and the Y-axis shows voltage and current values.

The plot **500** includes five waveforms **510-550**. The waveform **510** (in medium dashed line) shows drain current of the first transistor without mutual coupling parasitic inductance, the waveform **520** (in long-short dashed line) shows drain current of the second transistor without mutual coupling parasitic inductance, the waveform **530** (in solid line) shows drain current of the first transistor with mutual coupling parasitic inductance, the waveform **540** (in short dashed line) shows drain current of the second transistor with mutual coupling parasitic inductance, and the waveform **550** (in long dashed line) shows the drain-source voltage Vds.

As shown in FIG. **5**, at time toff, the first transistor and the second transistor are switched off. Without mutual coupling parasitic inductance, the transient current in the first transistor and the transient current in the second transistor have relatively large difference as shown by the waveforms **510** and **520**. With mutual coupling parasitic inductance, the transient current difference in the first transistor and the second transistor is reduced as shown by the waveforms **530** and **540**.

FIG. **6** shows a circuit diagram of a power module **610** for simulation according to an embodiment of the disclosure. The power module **610** operates similarly to the power module **110** described above, and also utilizes certain components that are identical or equivalent to those used in the power module **110**; the description of these components has been provided above and will be omitted here for clarity purposes.

In the FIG. **6** example, the power module **610** includes two driving nodes PC**1** and PC**2** to receive a control signal V_{DRV}. Further, the power module **610** includes a drain node D and a source node S. In an example, the drain node D and the source node S are connected to a power source. The power module **610** conducts a current flowing from the drain node D to the source node S in response to the control signal V_{DRV}.

According to an aspect of the disclosure, the power module **610** includes a plurality of switch modules, such as a first switch module **620**, a second switch module **630** and the like. The switch modules are in parallel coupled to the driving nodes PC**1** and PC**2**, the drain node D and the source node S using interconnection components, such as wirebonds, busbars and the like. The switch modules are configured to switch on/off current paths between the drain node D and the source node S based on the control signal Vrmv received at the driving nodes PC**1** and PC**2**.

Each switch module can include one or more transistors. When multiple transistors are used in a switch module, the multiple transistors can be arranged in various topologies to act as a switch.

Specifically, in the FIG. **6** example, the first switch module **620** includes a first transistor, and the second switch module **630** includes a second transistor. The first transistor and the second transistor can be any suitable transistors, such as metal-oxide-semiconductor field effect transistors (MOSFET) and the like. In an example, the first transistor and the second transistor are SiC MOSFET transistors that may have relatively wide parameter variations due to manufacturing process.

It is noted that real transistors can possess various parasitic elements, and are generally modeled using equivalent circuits in simulation. In the FIG. **6** example, the first transistor has a gate terminal G**1**, a source terminal S**1** and a drain terminal D**1**, and is modeled using a transistor model

M1, capacitors C1-C3, and a diode DD1 coupled together as shown in FIG. 6. Similarly, the second transistor has a gate terminal G2, a source terminal S2 and a drain terminal D2, and is modeled using a transistor model M2, capacitors C4-C6 and a diode DD2 coupled together as shown in FIG. 6.

According to an aspect of the disclosure, the terminals of the first transistor and the second transistors are coupled to the driving nodes PC1-PC2, the drain node D, and the source node S by interconnection components, and the interconnection components introduce parasitic inductances that influence the switching operation of the power module 610. The interconnection components can be modeled using inductances. For example, in the FIG. 6 example, the interconnection components between the driving node PC1 and the gate terminals G1 and G2 are modeled using inductances L_{ggc}, L_{gg1}, and L_{gg2} coupled together as shown in FIG. 6; the interconnection components between the driving node PC2 and the source terminals S1 and S2 are modeled using inductances L_{gsc}, L_{gs1}, and L_{gs2} coupled together as shown in FIG. 6; the interconnection components between the source node S and the source terminals S1 and S2 are modeled using inductances L_{sc}, L_{s1} and L_{s2} coupled together as shown in FIG. 6; the interconnection components between the drain node D and the drain terminals D1 and D2 are modeled using inductances L_{dc}, L_{d1}, and L_{d2} coupled together as shown in FIG. 6.

According to an aspect of the disclosure, the interconnection components can be purposely mutual coupled to introduce mutual coupling parasitic inductances to balance current/power among the switch modules in a power module. According to an aspect of the disclosure, parasitic inductances can be in a directly coupled state or an inverse coupled state. When the parasitic inductances are in the directly coupled state, cross coupling techniques can be used to reduce current/power unbalance, and when the parasitic inductances are in the inversely coupled state, self-coupling techniques can be used to reduce current/power unbalance.

In the FIG. 6 example, the direction of the drain inductance (e.g., the direction of L_{d1} and L_{d2}) and the direction of the gate inductance (e.g., the direction of L_{gg1} and L_{gg2}) of transistors make the drain inductance and the gate inductance in the directly coupled state (assuming positive mutual coupling coefficient). In the directly coupled state, when the drain current increases, the coupling of the drain inductance and the gate inductance can cause an increase in the gate voltage. In order to have a negative feedback to reduce the current/power unbalance for the directly coupled state, the drain inductance L_{d1} of the first switch module 620 is cross coupled to the gate inductance L_{gg2} of the second switch module 630 with a first mutual coupling coefficient, and the drain inductance L_{d2} of the second switch module 630 is cross coupled to the gate inductance L_{gg1} of the first switch module 620 with a second mutual coupling coefficient. In the example, positive mutual coupling coefficients are used. Further, in an example, with higher mutual coupling coefficients (e.g., 0.9), the difference between the different current paths is smaller, the switching speed is faster, but the transistors may have higher current overshoot peak.

According to an aspect of the disclosure, four cross coupling techniques (drain-gate cross coupling, drain-Kelvin gate cross coupling, source-gate cross coupling, and source-Kelvin gate cross coupling) can be used to introduce mutual coupling parasitic inductances between parallel switch modules.

For example, for the drain-gate cross coupling, the interconnection component modeled by the drain inductance L_{d1} of the first switch module 620 and the interconnection component modeled by the gate inductance L_{gg2} of the second switch module 630 are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by 611, and the interconnection component modeled by the drain inductance L_{d2} of the second switch module 630 and the interconnection component modeled by the gate inductance L_{gg1}, of the first switch module 620 are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by 612.

For the drain-Kelvin gate cross coupling, the interconnection component modeled by the drain inductance L_{d1} of the first switch module 620 and the interconnection component modeled by the Kelvin gate inductance L_{gs2} of the second switch module 630 are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by 613, and the interconnection component modeled by the drain inductance L_{d2} of the second switch module 630 and the interconnection component modeled by the Kelvin gate inductance L_{gs1} of the first switch module 620 are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by 614.

For the source-gate cross coupling, the interconnection component modeled by the source inductance L_{s1} of the first switch module 620 and the interconnection component modeled by the gate inductance L_{gg2} of the second switch module 630 are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by 615, and the interconnection component modeled by the source inductance L_{s2} of the second switch module 630 and the interconnection component modeled by the gate inductance L_{gg1} of the first switch module 620 are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by 616.

For the source-Kelvin gate cross coupling, the interconnection component modeled by the drain inductance L_{s1} of the first switch module 620 and the interconnection component modeled by the Kelvin gate inductance L_{gs2} of the second switch module 630 are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by 617, and the interconnection component modeled by the source inductance L_{s2} of the second switch module 630 and the interconnection component modeled by the Kelvin gate inductance L_{gs1} of the first switch module 620 are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by 618.

FIG. 7 shows a diagram of a power module 710 for circuit simulation according to an embodiment of the disclosure. The power module 710 operates similarly to the power module 610 described above, and also utilizes certain components that are identical or equivalent to those used in the power module 610; the description of these components has been provided above and will be omitted here for clarity purposes.

In the FIG. 7 example, the direction of the drain inductance (e.g., the direction of L_{d1} and L_{d2}) and the direction of the gate inductance (e.g., the direction of L_{gg1} and L_{gg2}) are configured in the inversely coupled state (assuming positive mutual coupling coefficient). In the inversely coupled state, when the drain current increases, the coupling of the drain inductance and the gate inductance can cause a decrease in the gate voltage. In order to have a negative feedback to reduce the current unbalance for the inversely coupled state, self-coupling techniques can be used. For example, the drain inductance L_{d1} of the first switch module 720 is self-coupled to the gate inductance L_{gg1} of the first switch module 720, and the drain inductance L_{d2} of the second switch module

730 is self-coupled to the gate inductance L_{gg2} of the second switch module 730 with positive mutual coupling coefficients to reduce power/current unbalance.

According to an aspect of the disclosure, four self-coupling techniques (drain-gate self-coupling, drain-Kelvin gate self-coupling, source-gate self-coupling, and source-Kelvin gate self-coupling) can be used to introduce mutual coupling parasitic inductances within each switch module.

For example, for the drain-gate self-coupling, the interconnection component modeled by the drain inductance L_{d1} of the first switch module 720 and the interconnection component modeled by the gate inductance L_{gg1} of the first switch module 720 are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by 711, and the interconnection component modeled by the drain inductance L_{d2} of the second switch module 730 and the interconnection component modeled by the gate inductance L_{gg2} of the second switch module 730 are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by 712.

For the drain-Kelvin gate self-coupling, the interconnection component modeled by the drain inductance L_{d1} of the first switch module 720 and the interconnection component modeled by the Kelvin gate inductance L_{gs1} of the first switch module 720 are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by 713, and the interconnection component modeled by the drain inductance L_{d2} of the second switch module 730 and the interconnection component modeled by the Kelvin gate inductance L_{gs2} of the second switch module 730 are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by 714.

For the source-gate self-coupling, the interconnection component modeled by the source inductance L_{s1} of the first switch module 720 and the interconnection component modeled by the gate inductance L_{gg1} of the first switch module 720 are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by 715, and the interconnection component modeled by the source inductance L_{s1} of the second switch module 730 and the interconnection component modeled by the gate inductance L_{gg2} of the second switch module 730 are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by 716.

For the source-Kelvin gate self-coupling, the interconnection component modeled by the drain inductance L_{s1} of the first switch module 720 and the interconnection component modeled by the Kelvin gate inductance L_{gs1} of the first switch module 730 are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by 717, and the interconnection component modeled by the source inductance L_{s2} of the second switch module 730 and the interconnection component modeled by the Kelvin gate inductance L_{gs2} of the second switch module 720 are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by 718.

FIG. 8A shows a diagram of the power module 610 for a simulation. In the FIG. 8A example, the power module 610 is in a directly coupled state that uses a cross coupling technique to improve current balance according to an embodiment of the disclosure.

FIG. 8B shows a plot of simulation result for the power module 610 in FIG. 8A. In the power module 610 of FIG. 8A, the direction of the drain inductance (e.g., the direction of L_{d2} and L_{d2}) and the direction of the gate inductance (e.g., the direction of L_{gg1} and L_{gg2}) are configured in the directly coupled state. With the directly coupled state, cross-coupling techniques, such as the drain-gate cross coupling technique as shown by 611 and 612, are used to reduce current unbalance.

In FIG. 8B, the X-axis shows time and the Y-axis shows drain current for switch modules. The plot 800 compares the drain current during switching for a first simulation using a first mutual coupling coefficient of zero (without using cross coupling technique) and a second simulation using a second mutual coupling coefficient of 0.9 (using a cross coupling technique). The plot 800 includes a first curve 810 and a second current 820 of drain current for the first simulation without using cross-coupling technique, and a third curve 830 and a fourth curve 840 of drain current for the second simulation that uses cross coupling technique.

As seen in FIG. 8B, the drain current difference between the third curve 830 and the fourth curve 840 is relatively smaller than the drain current difference between the first curve 810 and the second curve 820. Thus, the cross-coupling technique for the directly coupled state reduces current unbalance. Also seen in FIG. 8B, with the cross coupling technique, the switching current is larger, the switching speed is faster, and the current overshoot peak is higher.

FIG. 9A shows a diagram of the power module 710 for a simulation. In the FIG. 9A example, the power module 710 is in an inversely coupled state that uses a self-coupling technique to improve current balance according to an embodiment of the disclosure.

FIG. 9B shows a plot of simulation result for the power module 710 in FIG. 9A. In the FIG. 9A example, the direction of the drain inductance (e.g., the direction of L_{d2} and L_{d2}) and the direction of the gate inductance (e.g., the direction of L_{gg1} and L_{gg2}) are configured in the inversely coupled state. With the inversely coupled state, self-coupling techniques, such as the drain-gate self-coupling technique as shown by 711 and 712, are used to reduce current unbalance.

In FIG. 9B, the X-axis shows time and the Y-axis shows drain current for switch modules. The plot 900 compares the drain current during switching for a first simulation using a first mutual coupling coefficient of zero (without using self-coupling technique) and a second simulation using a second mutual coupling coefficient of 0.9 (using a self-coupling technique). The plot 900 includes a first curve 910 and a second current 920 of drain current for the first simulation without using self-coupling technique, and a third curve 930 and a fourth curve 940 of drain current for the second simulation that uses self-coupling technique.

As seen in FIG. 9B, the drain current difference between the third curve 930 and the fourth curve 940 is relatively smaller than the drain current difference between the first curve 910 and the second curve 920. Thus, the self-coupling techniques for the inversely coupled state can reduce current unbalance. Also seen in FIG. 9B, with the self-coupling technique, the switching current is smaller, the switching speed is slower, and the current overshoot peak is lower.

According to an aspect of the disclosure, the cross-coupling techniques for the directly coupled state and the self-coupling techniques for the inversely coupled state can be suitably combined to improve current balance.

FIG. 10 shows a diagram of a power module 1010 for circuit simulation according to an embodiment of the disclosure. The power module 1010 operates similarly to the power module 610 and the power module 710 described above, and also utilizes certain components that are identical or equivalent to those used in the power module 610 and the power module 710; the description of these components has been provided above and will be omitted here for clarity purposes. In the power module **1010**, the drain inductance and the gate inductance are in the directly coupled state while the source inductance and the Kelvin gate inductance are in the inversely coupled state.

In the FIG. **10** example, the interconnection component modeled by the drain inductance L_{d1} of the first switch module **1020** and the interconnection component modeled by the gate inductance L_{gg2} of the second switch module **1030** are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by **1011**, and the interconnection component modeled by the drain inductance L_{d2} of the second switch module **1030** and the interconnection component modeled by the gate inductance L_{gg1} of the first switch module **1020** are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by **1012**.

Further, in the FIG. **10** example, the interconnection component modeled by the drain inductance L_{s1} of the first switch module **1020** and the interconnection component modeled by the Kelvin gate inductance L_{gs1} of the first switch module **1030** are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by **1017**, and the interconnection component modeled by the source inductance L_{s2} of the second switch module **1030** and the interconnection component modeled by the Kelvin gate inductance L_{gs2} of the second switch module **1020** are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by **1018**.

FIGS. **11**A-**11**B show simulation result for the power module **1010** according to an embodiment of the disclosure. FIG. **11**A shows drain current during switching for a first simulation using a first mutual coupling coefficient of zero (without using any of the cross coupling technique and self-coupling technique) and FIG. **11**B shows the drain current during switching for a second simulation using a second mutual coupling coefficient of 0.9 (for both cross coupling and self-coupling techniques).

As seen in FIGS. **11**A and **11**B, the switching speed and peak current are about the same for the first simulation and the second simulation; however, the current unbalance is significantly reduced, specifically in the first few oscillation cycles.

Further, according to an aspect of the disclosure, the parasitic inductance coupling can be used to eliminate reliability issues, such as crosstalk, self turn on, self sustained oscillation and the like, for switching operations of power devices, and to improve reliability without sacrificing switching speed or increasing complexity.

FIG. **12** shows a diagram of a power device **1201** according to an embodiment of the disclosure. The power device **1201** is configured to use a half-bridge topology that includes an upper power module **1210** and a lower power module **1260** coupled in series between a first power supply voltage VDD (high voltage of a power supply) and a second power supply voltage VSS (low voltage of the power supply). In the FIG. **12** example, the upper power module **1210** is configured to use parasitic inductance couplings to eliminate cross-talk and improve switching reliability.

The upper power module **1210** includes one switch module or multiple switch modules (e.g., a first switch module **1220** and a second switch module **1230**) coupled in parallel. The one or more switch modules are coupled to a first node (N**1**), a second node (N**2**), and control nodes (NC**1** and NC**2**) via interconnections. The control nodes NC**1** and NC**2** receive a first driving signal $V_{DRV\text{-}HS}$ to control the upper power module **1210**. The first driving signal $V_{DRV\text{-}HS}$ is generated to turn on/off a first current path between the first node (N**1**) and the second node (N**2**). The lower power module **1260** includes one switch module or multiple switch modules (e.g., a third switch module **1270** and a fourth switch module **1280**) coupled in parallel. The one or more switch circuits are coupled to the second node (N**2**), a third node (N**3**), and control nodes (NC**3** and NC**4**) via interconnections. The control nodes NC**3** and NC**4** receive a second driving signal $V_{DRV\text{-}LS}$. The second driving signal $V_{DRV\text{-}LS}$ is generated to turn on/off a second current path between the second node (N**2**) and the third node (N**3**).

Specifically, in the FIG. **12** example, the upper power module **1210** operates similarly to the power modules described above, such as the power module **110**, the power module **610**, the power module **710** and the like. The upper power module **1210** also utilizes certain components that are identical or equivalent to those used in the power modules described above; the description of these components has been provided above and will be omitted here for clarity purposes.

Similarly, in the FIG. **12** example, the lower power module **1260** operates similarly to the power modules described above, such as the power module **110**, the power module **610**, the power module **710** and the like. The lower power module **1260** also utilizes certain components that are identical or equivalent to those used in the power modules described above; the description of these components has been provided above and will be omitted here for clarity purposes.

It is noted that, in an example, the power device **1201** includes a control circuit (not shown) suitably configured to generate the first driving signal $V_{DRV\text{-}HS}$ and the second driving signal $V_{DRV\text{-}LS}$. In an embodiment, the first driving signal $V_{DRV\text{-}HS}$ and the second driving signal $V_{DRV\text{-}LS}$ are generated to be complementary to each other with a positive non-overlapping dead-time.

In the FIG. **12** example, the upper power module **1210** is configured similarly to the power module **710** in the inversely coupled state. Specifically, the direction of the drain inductance (e.g., the direction of $L_{d1\text{-}HS}$ and $L_{d2\text{-}HS}$) and the direction of the gate inductance (e.g., the direction of $L_{gg1\text{-}HS}$ and $L_{gg2\text{-}HS}$) are configured in the inversely coupled state (assuming positive mutual coupling coefficient). In the inversely coupled state, when the drain current increases, the coupling of the drain inductance and the gate inductance can cause a decrease in the gate voltage. Further, self-coupling techniques can be used to improve switching reliability. For example, in the upper power module **1210**, the interconnection component modeled by the drain inductance $L_{d1\text{-}HS}$ of the first switch module **1220** and the interconnection component modeled by the gate inductance $L_{gg1\text{-}HS}$ of the first switch module **1220** are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by **1211**, and the interconnection component modeled by the drain inductance $L_{d2\text{-}HS}$ of the second switch module **1230** and the interconnection component modeled by the gate inductance $L_{gg2\text{-}HS}$ of the second switch module **1230** are purposely mutually coupled to introduce a mutual coupling parasitic inductance as shown by **1212**.

According to an aspect of the disclosure, the parasitic inductance introduced by the mutual coupling of interconnection components (e.g., **1211** and **1212**) can be used to eliminate cross-talk and improve switching reliability.

During operation, in an example, before a switching off of the upper power module **1210**, the first driving signal $V_{DRV\text{-}HS}$ is of a relatively high voltage to maintain the upper power module **1210** to be turned on, and the second driving signal $V_{DRV\text{-}LS}$ is of a relatively low voltage to turn off the lower power module **1260**. Specifically, before the switching off of the upper power module **1210**, the first switch module **1220** and the second switch module **1230** are turned on and the third switch module **1270** and the fourth switch module **1280** are turned off. Thus, the first switch module **1220** and the second switch module **1230** form a current path between the first node **N1** and the second node **N2**, and the second node **N2** has a relatively high voltage, for example about the level of VDD.

At the switching off time of the upper power module **1210**, the first driving signal $V_{DRV\text{-}HS}$ is controlled to switch from the relatively high voltage to the relatively low voltage to turn off the upper power module **1210**, e.g., turn off the first switch module **1220** and the second switch module **1230**.

Then, the first driving signal $V_{DRV\text{-}HS}$ and the second driving signal $V_{DRV\text{-}LS}$ are of the relatively low voltage for the positive non-overlapping dead-time after the switching off time of the upper power module **1210** and before a switching on time of the lower power module **1260**.

At the switching on time of the lower power module **1260**, the first driving signal $V_{DRV\text{-}HS}$ is maintained at the relatively low voltage to keep the upper power module **1210** to be turned off, and the second driving signal $V_{DRV\text{-}LS}$ is controlled to switch from the relatively low voltage to the relatively high voltage to turn on the lower power module **1260**.

After the switching on of the lower power module **1260**, the first driving signal $V_{DRV\text{-}HS}$ is of the relatively low voltage to maintain the upper power module **1210** to be turned off, and the second driving signal $V_{DRV\text{-}LS}$ is of the relatively high voltage to turn on the lower power module **1260**. Specifically, after the switching on of the lower power module **1260**, the first switch module **1220** and the second switch module **1230** are turned off and the third switch module **1270** and the fourth switch module **1280** are turned on. Thus, the third switch module **1270** and the fourth switch module **1280** form a current path between the second node **N2** and the third node **N3**, and the second node **N2** has a relatively low voltage, for example about the level of VSS.

According to an aspect of the disclosure, at the time to switch on the lower power module **1260**, the voltage at the second node **N2** drops from the relatively high voltage (e.g., VDD) to the relatively low voltage (e.g., VSS) in a relatively short time, the change of the voltage in the short time (a relatively large dv/dt) can cause a relatively large gate current to the switch modules **1220** and **1230** to cause an increase of the gate voltages of the switch module **1220** and the switch module **1230**. The gate voltage increase can turn on the switch module **1220** and the switch module **1230** for a short time, and the unintentional turn-on of the upper power module **1210** is referred to as crosstalk and can cause reliability issue, for example, large leakage current I**1** and I**2** during the short time. However, due to the inversely coupled state and the self-coupling techniques (e.g., **1211** and **1212**) used in the upper power module **1210**, when the drain current I**1**/I**2** increases, the coupling of the drain inductance and the gate inductance can cause a decrease in the gate voltage, and thus to turn off the switch modules **1220** and **1230** to prevent the crosstalk.

It is noted that while the power device **1201** uses a self-coupling technique in the inversely coupled state to eliminate the crosstalk, the power device **1201** can be suitably modified to use other suitable parasitic inductance coupling techniques to eliminate crosstalk type of reliability issues.

FIGS. **13**A and **13**B show plots of waveforms of simulation for the power device **1201** according to an embodiment of the disclosure. FIG. **13**A shows results from a first simulation using non-zero mutual coupling coefficient for **1211** and **1212**. FIG. **13**A includes a first waveform **1310** for the second driving signal $V_{DRV\text{-}LS}$ and a second waveform **1320** for the drain current I**1** of the first switch module **1220**. FIG. **13**B shows results from a second simulation using zero mutual coupling coefficient for **1211** and **1212**. FIG. **13**B includes a third waveform **1330** for the second driving signal $V_{DRV\text{-}LS}$ and a fourth waveform **1340** for the drain current I**1** of the first switch module **1220**.

As seen in FIG. **13**B, without the mutual coupling (zero mutual coupling coefficient), when the second driving signal $V_{DRV\text{-}LS}$ switches from the relatively low voltage to the relatively high voltage to switch on the lower power module **1260**, a relatively large current (shown by **1345**) flows through the first switch module **1220**. The relatively large current is caused by the voltage change at the second node **N2** at the time of switching on the lower power module **1260**.

As seen in FIG. **13**A, with the mutual coupling (non-zero mutual coupling coefficient), when the second driving signal $V_{DRV\text{-}LS}$ switches from the relatively low voltage to the relatively high voltage to switch on the lower power module **1260**, the current flows through the first switch module **1220** can be kept low.

FIG. **14** shows a diagram of a power device **1401** according to an embodiment of the disclosure. The power device **1401** operates similarly to the power device **1201** described above. The power device **1401** also utilizes certain components that are identical or equivalent to those used in the power device **1201**; the description of these components has been provided above and will be omitted here for clarity purposes. In the FIG. **14** example, the lower power module **1460** is configured to use parasitic inductance couplings to prevent self turn-on and/or self-sustained oscillation and improve switching reliability.

In the FIG. **14** example, the lower power module **1460** is configured similarly to the power module **610** in the directly coupled state. Specifically, the direction of the drain inductance (e.g., the direction of LDRV-LS and $L_{d2\text{-}LS}$) and the direction of the gate inductance (e.g., the direction of $L_{gg1\text{-}LS}$ and $L_{gg2\text{-}LS}$) of transistors make the drain inductance and the gate inductance in the directly coupled state (assuming positive mutual coupling coefficient). In the directly coupled state, when the drain current increases, the coupling of the drain inductance and the gate inductance can cause an increase in the gate voltage.

In the FIG. **14** example, to prevent self turn-on and/or self sustained oscillation, a cross-coupling technique can be used. In the example, the drain inductance $L_{d1\text{-}LS}$ of the third switch module **1470** is cross-coupled to the gate inductance $L_{gg2\text{-}LS}$ of the fourth switch module **1480** with a first mutual coupling coefficient as shown by **1461**, and the drain inductance $L_{d2\text{-}LS}$ of the fourth switch module **1480** is cross coupled to the gate inductance $L_{gg1\text{-}LS}$ of the third switch module **1470** with a second mutual coupling coefficient as shown by **1462**. In the example, positive mutual coupling coefficients are used.

According to an aspect of the disclosure, the parasitic induced introduced by the mutual coupling of interconnection components (e.g., **1461** and **1462**) can be used to prevent self turn-on and improve switching reliability.

During operation, in an example, before a switching off of the lower power module **1460**, the second driving signal $V_{DRV\text{-}LS}$ is of a relatively high voltage to maintain the lower power module **1460** to be turned on, and the first driving signal V_{DRV-HS} is of a relatively low voltage to turn off the upper power module **1410**. Specifically, before the switching off of the lower power module **1460**, the third switch module **1470** and the fourth switch module **1480** are turned on and the first switch module **1420** and the second switch module **1430** are turned off. Thus, the third switch module **1470** and the fourth switch module **1480** form a current path between the second node N**2** and the third node N**3**, and the second node N**2** has a relatively low voltage, for example about the level of VSS.

At the switching off time of the lower power module **1460**, the second driving signal V_{DRV-LS} is controlled to switch from the relatively high voltage to the relatively low voltage to turn off the lower power module **1460**, e.g., turn off the third switch module **1470** and the fourth switch module **1480**.

Then, the first driving signal V_{DRV-HS} and the second driving signal V_{DRV-LS} are of the relatively low voltage for the positive non-overlapping dead-time after the switching off time of the upper power module **1410** and before a switching on time of the lower power module **1460**. However, the lower power module **1460** may turn on itself with very large currents due to the existence of common source inductance induced positive gate voltage. This induced positive gate voltage can subsequently turn on the lower power module **1460** again even though the second driving signal V_{DRV-LS} is low.

According to an aspect of the disclosure, due to the directly coupled state and the cross-coupling techniques used in the lower power module **1460**, when the drain current I**3**/I**4** increases, the cross coupling of the drain inductance and the gate inductance can cause a decrease in the gate voltage, and thus to turn off the switch modules **1470** and **1480**, and prevent the self turn-on.

According to an aspect of the disclosure, the parasitic induced introduced by the mutual coupling of interconnection components (e.g., **1461** and **1462**) can be used to prevent self sustained oscillation and improve switching reliability.

During operation, in an example, when the second driving signal V_{DRV-LS} is of a relatively high voltage to turn on the lower power module **1460**, due to high drain current of the third switch module **1470** and the fourth switch module **1480** and relatively large gate inductance of the third switch module **1470** and the fourth switch module **1480**, the third switch module **1470** and the fourth switch module **1480** can enter a self-sustained oscillation to repetitively turn on and off.

According to an aspect of the disclosure, due to the directly coupled state and the cross-coupling techniques used in the lower power module **1460**, when the drain current I**3**/I**4** changes fast, the cross coupling of the drain inductance and the gate inductance can cause the gate voltage to change in a direction to counteract the drain current change, and thus to prevent the self-sustained oscillation.

It is noted that while the power device **1401** uses a cross-coupling technique in the directly coupled state to prevent the self turn on and/or self sustained oscillation, the power device **1401** can be suitably modified to use other suitable parasitic inductance coupling techniques to prevent the self turn on and/or self sustained oscillation types of reliability issues.

FIGS. **15**A-**15**B show plots of simulation results for the power device **1401** according to an embodiment of the disclosure. FIG. **15**A shows results of a first simulation using non-zero mutual coupling coefficient for **1461** and **1462**. FIG. **15**A includes a first waveform **1510** for the second driving signal V_{DRV-LS}, a second waveform **1520** for the drain current I**3** of the third switch module **1470** and a third waveform **1525** for the drain current I**4** of the fourth switch module **1480**. FIG. **15**B shows results of a second simulation using zero mutual coupling coefficient for **1461** and **1462**. FIG. **15**B includes a fourth waveform **1530** for the second driving signal, a fifth waveform **1540** for the drain current I**3** of the third switch module **1470** and a sixth waveform **1545** for the drain current I**4** of the fourth switch module **1480**.

As seen in FIG. **15**B, without the mutual coupling (coupling coefficients are zero), when the second driving signal V_{DRV-LS} switches from the relatively high voltage to the relatively low voltage to turn off the lower power module **1460**, the third switch module **1470** and the fourth switch module **1480** can turn off and then self turn on with a relatively large current flowing through the third switch module **1470** and the fourth switch module **1480** as shown by the fifth waveform **1540** and the six waveform **1545** at about 200 ns.

As seen in FIG. **15**A, with the mutual coupling (non-zero coupling coefficients), when the second driving signal V_{DRV-LS} switches from the relatively high voltage to the relatively low voltage to switch off the lower power module **1460**, the third switch module **1470** and the fourth switch module **1480** can be turned off and can be kept in the turn-off state.

FIGS. **16**A-**16**B show plots of simulation results for the power device **1401** according to an embodiment of the disclosure. FIG. **16**A shows results of a first simulation using non-zero mutual coupling coefficient for **1461** and **1462**. FIG. **16**A includes a first waveform **1610** for the second driving signal V_{DRV-LS}, a second waveform **1620** for the drain current I**3** of the third switch module **1470** and a third waveform **1625** for the drain current I**4** of the fourth switch module **1480**. FIG. **16**B shows results of a second simulation using zero mutual coupling coefficient for **1461** and **1462**. FIG. **16**B includes a fourth waveform **1630** for the second driving signal V_{DRV-LS}, a fifth waveform **1640** for the drain current I**3** of the third switch module **1470** and a sixth waveform **1645** for the drain current I**4** of the fourth switch module **1480**.

As seen in FIG. **16**B, without the mutual coupling (coupling coefficients are zero), when the second driving signal V_{DRV-LS} switches from the relatively low voltage to the relatively high voltage and stays at the relatively high voltage, the third switch module **1470** and the fourth switch module **1480** can repetitively turn on and off in a self sustained oscillation with a relatively large current flowing through the third switch module **1470** and the fourth switch module **1480** as shown by the fifth waveform **1640** and the six waveform **1645** from 20 ns to 70 ns in FIG. **16**B.

As seen in FIG. **16**A, with the mutual coupling (non-zero coupling coefficients), when the second driving signal V_{DRV-LS} switches from the relatively low voltage to the relatively high voltage and stays at the relatively high voltage to switch on the lower power module **1460**, the third switch module **1470** and the fourth switch module **1480** can be turned on and can be kept in the turn-on state.

FIG. **17** shows a flow chart outlining a process example **1700** according to an embodiment of the disclosure. In an example, the process **1700** is executed to implement a power device, such as the power device **1201**, the power device **1401**, and the like. The process starts at S**1701**, and proceeds to S**1710**.

At S**1710**, reliability issues in the switching operations of a power device are determined. For example, the reliability issues can be identified during a design of the power device based on various information sources, such as feedback from clients of previous implementation, power device simulations, and the like.

At **S1720**, parasitic inductance coupling techniques to eliminate the reliability issues are determined. In an example, when crosstalk is identified as a reliability issue for the power device, the parasitic inductance coupling technique used in the power device **1201** can be determined to eliminate the crosstalk; and when the self turn on or self sustained oscillation is identified as reliability issue for the power device, the parasitic inductance coupling technique used in the power device **1401** can be determined to prevent self turn on or the self sustained oscillation.

At **S1730**, transistors and interconnections are disposed according to the determined parasitic inductance coupling techniques. During manufacturing of the power device, the transistors and the interconnections can be disposed according to the determined parasitic inductance coupling techniques. Then the process proceeds to **S1730** and terminates.

When implemented in hardware, the hardware may comprise one or more of discrete components, an integrated circuit, an application-specific integrated circuit (ASIC), etc.

While aspects of the present disclosure have been described in conjunction with the specific embodiments thereof that are proposed as examples, alternatives, modifications, and variations to the examples may be made. Accordingly, embodiments as set forth herein are intended to be illustrative and not limiting. There are changes that may be made without departing from the scope of the claims set forth below.

What is claimed is:

1. A power device, comprising:

an upper power module coupled to a first node, a second node and a first control node via first interconnections, the upper power module being controlled by a first driving signal at the first control node to turn on/off a first current path between the first node that receives a first supply voltage and the second node;

a lower power module coupled to the second node, a third node and a second control node via second interconnections, the lower power module being controlled by a second driving signal at the second control node to turn on/off a second current path between the second node and the third node that receives a second supply voltage that is lower than the first supply voltage, wherein the first interconnections are inductively coupled to prevent a turn-on of the upper power module when the first driving signal is at a first voltage level to turn off the upper power module and the second driving signal is at a second voltage level to turn on the lower power module.

2. The power device of claim **1**, wherein the upper power module comprises:

a first switch circuit in parallel with a second switch circuit, the first switch circuit and the second switch circuit being coupled to the first node, the second node and the first control node via the first interconnections.

3. The power device of claim **2**, wherein the lower power module comprises:

a third switch circuit in parallel with a fourth switch circuit, the third switch circuit and the fourth switch circuit being coupled to the second node, the third node and the second control node via the second interconnections.

4. The power device of claim **3**, wherein the first switch circuit includes a first SiC metal-oxide-semiconductor field effect transistor, the second switch circuit includes a second SiC metal-oxide-semiconductor field effect transistor, the third switch circuit includes a third SiC metal-oxide-semiconductor field effect transistor, and the fourth switch circuit includes a fourth SiC metal-oxide-semiconductor field effect transistor.

5. The power device of claim **2**, wherein the first interconnection and the second interconnection are among interconnections that interconnect the first switch circuit to the first node, the second node, and the first control node.

6. The power device of claim **5**, wherein parasitic inductances introduced by the first interconnection and the second interconnection are in an inversely coupled state.

7. The power device of claim **5**, wherein the first interconnection interconnects a gate terminal of the first switch circuit to the first control node, and the second interconnection interconnects a drain terminal of the first switch circuit to the first node.

8. A power device, comprising:

an upper power module coupled to a first node, a second node and a first control node via first interconnections, the upper power module being controlled by a first driving signal at the first control node to turn on/off a first current path between the first node that receives a first supply voltage and the second node;

a lower power module coupled to the second node, a third node and a second control node via second interconnections, the lower power module being controlled by a second driving signal at the second control node to turn on/off a second current path between the second node and the third node that receives a second supply voltage that is lower than the first supply voltage, wherein the second interconnections are inductively coupled to prevent self turn-on of the lower power module when the second driving signal is at a voltage level to turn off the lower power module.

9. The power device of claim **8**, wherein

the upper power module comprises:

a first switch circuit in parallel with a second switch circuit, the first switch circuit and the second switch circuit being coupled to the first node, the second node and the first control node via the first interconnections; and

the lower power module comprises:

a third switch circuit in parallel with a fourth switch circuit, the third switch circuit and le fourth switch circuit being coupled to the second node, the third node and the second control node via the second interconnections.

10. The power device of claim **9**, wherein the first switch circuit includes a first SiC metal-oxide-semiconductor field effect transistor, the second switch circuit includes a second SiC metal-oxide-semiconductor field effect transistor, the third switch circuit includes a third SiC metal-oxide-semiconductor field effect transistor, and the fourth switch circuit includes a fourth SiC metal-oxide-semiconductor field effect transistor.

11. The power device of claim **9**, wherein the first interconnection and the second interconnection are among interconnections that interconnect the third switch circuit and the fourth switch circuit to the second node, the third node, and the second control node.

12. The power device of claim **11**, wherein parasitic inductances introduced by the first interconnection and the second interconnection are in a directly coupled state.

13. The power device of claim **12**, wherein the first interconnection interconnects a gate terminal of the third switch circuit to the second control node, and the second interconnection interconnects a drain terminal of the fourth switch circuit to the second node.

14. A power device, comprising:

an upper power module coupled to a first node, a second node and a first control node via first interconnections, the upper power module being controlled by a first driving signal at the first control node to turn on/off a first current path between the first node that receives a first supply voltage and the second node;

a lower power module coupled to the second node, a third node and a second control node via second interconnections, the lower power module being controlled by a second driving signal at the second control node to turn on/off a second current path between the second node and the third node that receives a second supply voltage that is lower than the first supply voltage, wherein the second interconnections are inductively coupled to prevent self sustained oscillation of the lower power module when the second driving signal is at a voltage level to turn on the lower power module.

15. The power device of claim **14**, wherein

the upper power module comprises:

a first switch circuit in parallel with a second switch circuit, the first switch circuit and the second switch circuit being coupled to the first node, the second node and the first control node via the first interconnections; and

the lower power module comprises:

a third switch circuit in parallel with a fourth switch circuit, the third. switch circuit and the fourth switch circuit being coupled to the second node, the third node and the second control node via the second interconnections.

16. The power device of claim **15**, wherein the first switch circuit includes a first SiC metal-oxide-semiconductor field effect transistor, the second switch circuit includes a second SiC metal-oxide-semiconductor field effect transistor, the third switch circuit includes a third SiC metal-oxide-semiconductor field effect transistor, and the fourth switch circuit includes a fourth SiC metal-oxide-semiconductor field effect transistor.

17. The power device of claim **15**, wherein the first interconnection and the second interconnection are among interconnections that interconnect the third switch circuit and the fourth switch circuit to the second node, the third node, and the second control node.

18. The power device of claim **17**, wherein parasitic inductances introduced by the first interconnection and the second interconnection are in a directly coupled state.

19. The power device of claim **18**, wherein the first interconnection interconnects a gate terminal of the third switch circuit to the second control node, and the second interconnection interconnects a drain terminal of the fourth switch circuit to the second node.

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