Multi Resonant Switched-Capacitor Converters

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Dissertation submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Master of Science
in
Electrical Engineering

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January 24, 2019
Blacksburg, Virginia

Keywords: Some Keywords, Subject matter, etc.

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(ABSTRACT)

This thesis presents a novel Resonant Switched-Capacitor Converter with Multiple Resonant Frequencies, abbreviated as MRSCC for both high density and efficiency non-isolated large step-down Intermediate Bus Converter (IBC). Conventional Resonant Switched-Capacitor Converter (RSCC) proposed in [1] and its high voltage conversion ratio derivation such as Switched-Tank Converter (STC) in [2] and [3] employ half sinusoidal-current charge transfer method between capacitors to achieve high efficiency and density operation by adding a small resonant inductor in series to pure switched-capacitor converter's (SCC) flying capacitor. By operating switching frequency to be the same as its resonant frequency, RSCC achieves zero-current turn off operation, however, this cause RSCC and its derivation suffer from component variation issue for high-volume adoption. Derived from RSCC, MRSCC adds additional high frequency resonant component, operates only during its dead-time, by adding small capacitor in parallel to RSCC's resonant inductor. By operating switching frequency higher than its main resonant frequency, MRSCC utilizes double chopped half-sinusoidal current charge transfer method between capacitors to further improve efficiency. In addition, operating switching frequency consistently higher than its resonant frequency, MRSCC provides high immunity towards component variation, making it and its derivation viable for high-volume adoption.

Multi Resonant Switched-Capacitor Converters

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(GENERAL AUDIENCE ABSTRACT)

Following the recent trend, most internet services are moving towards cloud computing. Large data applications and growing popularity of cloud computing require hyperscale data centers and it will contiune to grow rapidly in the next few years to keep up with the demand [4]. These cutting-edge data centers will require higher performance multi-core CPU and GPU installations which translates to higher power consumption. From 10MWatts of power, typical data centers deliver only half of this power to the computing load which includes processors, memory and drives. Unfortunately, the rest goes to losses in power conversion, distribution and cooling [5]. Industry members look into increasing backplane voltage from 12V to 48V in order to reduce distribution loss. This thesis proposes a novel Resonant Switched-Capacitor Converter using Multiple Resonant Frequencies to accommodate this increase of backplane voltage.

Dedication

This work is dedicated to my family,

My Parents: Jong Sin Hoa and Sri Hety

My Brother: Olaf Jong

My Sisters: Maureen Jong and Inesita Jong

Acknowledgments

With completion of this work, I would like to thank my advisor, Dr. Qiang Li for his guidance, encouragement and support, especially the opportunity to be his first master student. I learned many things from him in both technical and research skills. However, one most important thing I will remember is to slow down and think since I was used to do things without careful thought. I believe everything I have learned from Dr. Qiang Li will benefit me in the future.

I am also grateful to the other two members of my advisory committee, Dr. William T. Baumann and Dr. Dan M. Sable for their support, suggestions and encouragement.

In addition, I would like to say thanks to my colleagues in the PMC group for the support during my stay in CPES. I would like to thank: Mohammed Ahmed for his time teaching me about research mentality and how make presentation slides, Dr. Syed Bahri, Virginia Li, Feiyang Zhu, Shuo Wang and Yinsong Cai for their support and encouragement during my stay in CPES. I would also like to thank other CPES staff who were always willing to help me out, Ms Teresa Shaw, Ms Teresa Rose, Ms. Marianne Hawthorne, Ms. Linda Long, Ms. Laurent Shutt and Mr. David Gilham.

With much love, I would like to thank some people I met along my journey in Virginia Tech, Indonesian Student Group Permias, especially Pratama Yudha, Andrianshah Priyadi, Deasy Priadi and Bela Haifa, ECE OPEL crew, Corey Rhodes, Jerry Yue Zhan and Oscar Yu, and from PMIC lab, Erick Aponte. I thank them for their support and encouragement

during my graduate school frustration years and I would not survive without them.

I would also like to thank some special individuals I met in Calpoly, Dr Taufik and Arief Hernadi for their support, encouragement and shared passion in power electronics field, David Beebe, my manager in Linear Tech, for his knowledge and wisdom.

Not to forget, I thank my family as my biggest supporter of my dream.

This work was supported primarily by Power Management Consortium (PMC) members. Last but not least, I would like to say my final thanks to Brian Carpenter from Texas Instrument for his support and trust in me in research.

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Chapter 1

Introduction

1.1 Data Centers and Server Rack Application

Following the recent trend, most Internet services are moving towards cloud computing. Large data applications and growing popularity of cloud computing require hyperscale data centers and it will continue to grow rapidly in the next few years to keep up with the demand [4]. These cutting-edge data centers will require higher performance multi-core CPU and GPU installations which translates to high power consumption.

Data centers with thousand of networked servers collectively use a huge amount of power. According to [11], data centers worldwide are on track to emit 340 metric megatons of CO_2 annually by 2020. A very large data center requires Power on the order of 10 Mega Watts (MW) to support computing infrastructure and is expected keep increasing in the future [5]. Unfortunately, with the increase in performance of a data center, it will result in higher power consumption and loss. From 10 MW of power, typical data centers deliver only half of this power to the computing load which includes processors, memory and drives.

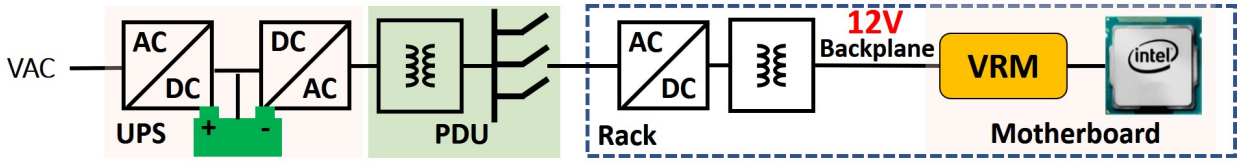


Figure 1.1: Traditional Server Rack 12V Architecture[5]

Unfortunately, the rest goes to losses in power conversion, distribution and cooling [5].

Figure 1.1 shows the conventional server rack application to power CPUs and GPUs in data centers. This approach converts the AC input voltage to DC for storage purposes before converted back to AC for power distribution through PDU to server racks. As power consumption increases, 12V backplane architecture can no longer provides high efficiency operation due to many conversion stages and additional distribution loss along backplane. [5] explored and compared different voltages and topologies for Server Rack applications and found that 400V facility level DC distribution system was found most efficient to deliver energy by reducing number of conversion stages and isolation. However, this proposed idea will require industry to invest more in extensive research and development in power delivery system construction [3]. Looking from 12V conventional approach perspective, [12] suggested that 48V may be more practical for future server rack application. In addition to lower conduction loss, 48V will reduce filter size of VRMs and increase immunity towards load transient effect on the bus voltage.

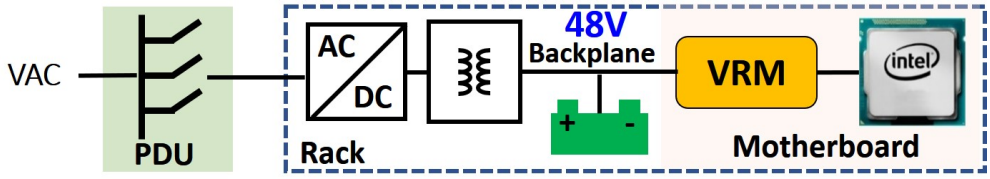


Figure 1.2: The New Server Rack 48V Architecture [3]

In agreement to [12], Industries member such as Facebook and Google® adopt 48V architecture as shown in Figure 1.2. By increasing the voltage to 48V, it reduces the conduction loss by 1/16th along the backplane in comparison to its 12V counterparts assuming the same power going to the load. However, it is important to note that 54V nominal voltage has become more popular [3]. This 48V architecture, however, imposes extra challenges in designing Voltage Regulator Module (VRM) to convert 48V to Vcore (0.8V-2V).

1.2 Single-Stage VRM

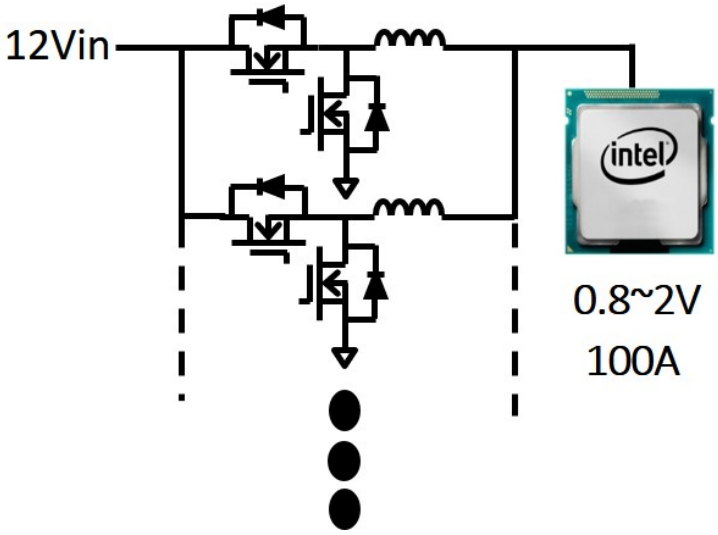


Figure 1.3: Multi-Phase Buck Voltage Regulator Module

Multi-phase Buck Converter shown in Figure 1.3 has dominated VRM solution market in 12V architecture. 12V VRMs have kept up with the dynamic performance, efficiency and scalability requirement of VRMs over the years. However, with 48V bus architecture, Multi-phase buck converter alone is no longer a feasible solution for VRM design. Higher input voltage introduces extra voltage stress on devices used in the buck converter, hence it requires higher drain to source voltage rating (V_{ds}) devices which can increase conversion loss. In order to minimize this additional loss, one may reduce buck converter's switching frequency (f_{sw}). Nevertheless, this approach of lowering f_{sw} is not without consequences of increasing the size of output capacitors and footprint of VRMs.

In this section, we explore many possible solutions done by researchers in order to design high step down converter in a single stage. Generally, it can be divided into two categories; transformer based and transformer-less.

1.2.1 Single Stage Transformer Based

The first investigation of single stage VRMs is done by [12] in 2002. [12] explored many isolated topologies which use transformer in order to obtain larger duty cycle regardless large step down operation. By using current doubler structure on secondary side, it allows lower V_{ds} ratind devices to be used. Although [12] found push-pull forward converter with integral magnetics shows better performance than other solutions, when switching frequency is pushed to 500kHz, [6] found the efficiency decreases by 10% due to high switching and body diode loss. [6] proposed another solution for low voltage high current VRM using self driven phase-shifted full-bridge. The proposed phase-shifted full bridge achieves Zero Voltage Switching (ZVS) naturally, allowing high frequency operation fit for high transient requirement. Figure 1.4 shows the schematic of a phase-shifted full bridge.

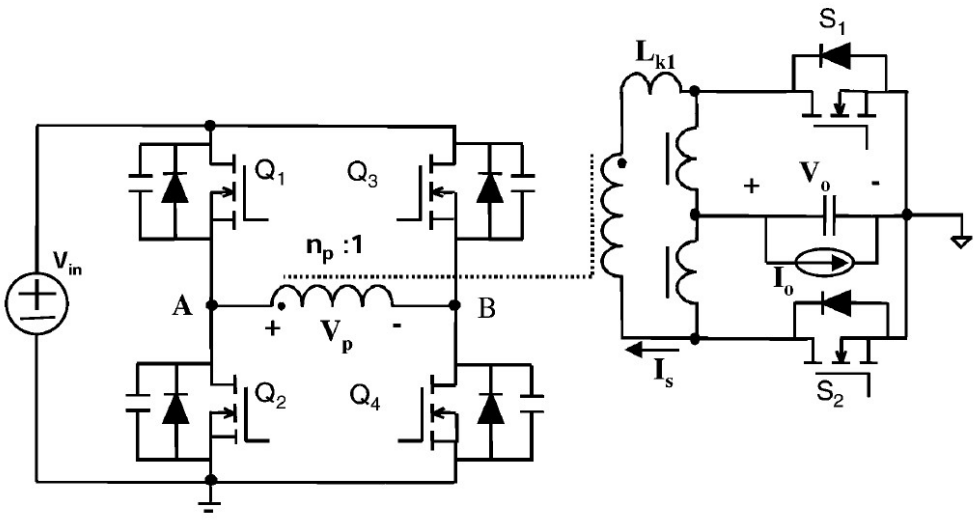


Figure 1.4: Phase-Shifted Full Bridge Schematic [6]

In order to achieve ZVS, phase-shifted full bridge utilizes its energy storage element, such as leakage inductor. The energy stored within the leakage inductor is recycled to charge and discharge output capacitance of devices in the primary side. Unfortunately, the energy

stored is proportional to its output current, hence it can not achieve ZVS operation during light load condition [13].

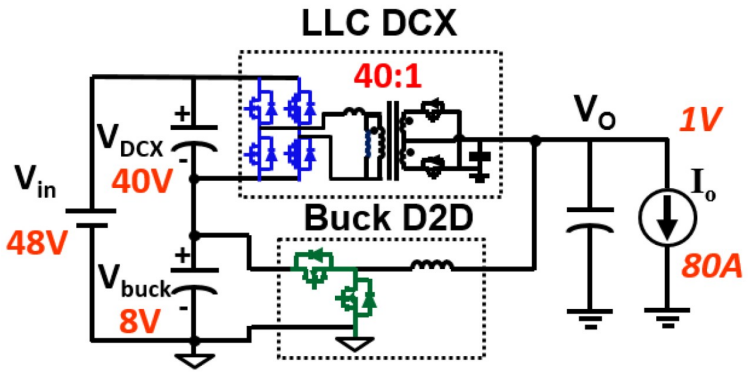


Figure 1.5: Sigma Converter Power Architecture [7]

Based on complications using PWM based converter and phase shifted-full bridge, many researchers start looking into resonant converter such as LLC. Using similar primary and secondary side structure as full bridge or its derivation, LLC offers high efficiency operation across load due to ZVS at the primary and ZCS at the secondary synchronous rectifiers (SRs) [14]. However, in order to achieve the highest efficiency, LLC should operate at one single operation condition of switching frequency equals to its resonant frequency. Utilizing this property, [7] introduces a sigma converter, based on Quasi-Parallel Structure proposed by [15] as shown in Figure 1.5. [7] utilizes LLC and a buck converter in series at the input and in parallel at the output, hence the name Quasi-Parallel. Sigma converter delivers most of its energy to the output through it DCX transformer, in this case LLC converter, while small portion of energy will be delivered through the buck converter which provides regulation at the same time. In order to gain high efficiency and density, sigma converter has to employ a matrix transformer described in [16]. The final solution uses 40 to 1 turn ratio transformer which translates to 14 layers printed circuit board (PCB) and achieves 420W/in^3 of power density. This result illustrates the complication with single stage transformer based solution.

1.2.2 Single Stage Transformer-less

In order to achieve high density, many researchers believe in getting rid of transformer. Many turns to switched-capacitor based circuit in order to gain high step down conversion. [17] and [9] proposed capacitor based hybrid buck converter in order to achieve high step down with larger duty cycle operation. They utilize higher voltage conversion ratio (VCR) switched capacitor circuit combined with interleaved buck converter to obtain regulation at its output.

Interleaved Buck Converter

Derived from multi-phase approach, Interleaved Buck Converter, proposed in [8], utilizes a half input voltage pre-biased capacitor. By having this pre-biased flying capacitor, it reduces effective input voltage to the dual-phase buck converter. Figure 1.6 shows the proposed interleaved buck converter schematic. Unlike regular switched-capacitor converter where all flying capacitors are force balanced in every cycle, Interleaved Buck Converter requires precise control to balance its flying capacitor. One has to monitor the flying capacitor's voltage all the time, especially during transient.

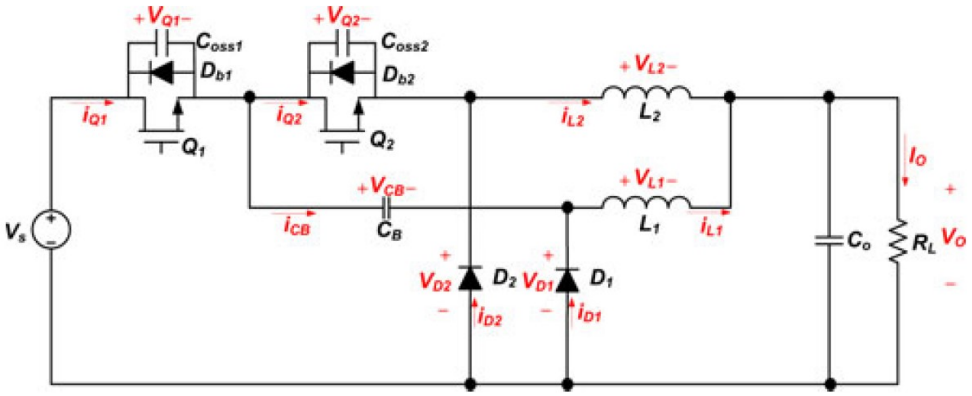


Figure 1.6: Interleaved Buck Converter [8]

Hybrid Converter using Interleaved Dual Inductors [9], [17]

Using Interleaved Buck Converter concept, [9] and [17] expand it using higher voltage conversion ratio Dickson switched-capacitor to obtain higher duty cycle. Figure 1.7 shows the 4 to 1 Dickson Switched-Capacitor Interleaved Buck Converter using two interleaved inductors.

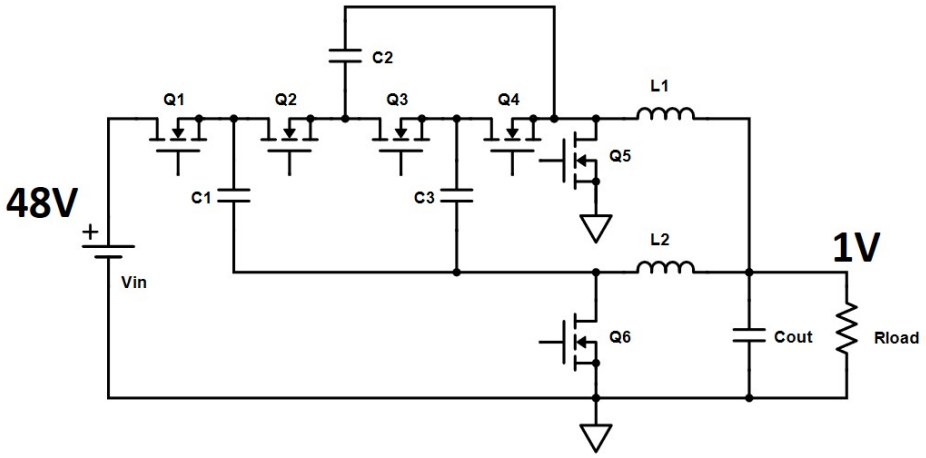


Figure 1.7: 4 to 1 Hybrid Converter using Interleaved Dual Inductors [9]

Table 1.1: Bias Voltage of Flying Capacitors

	SCC Voltage Divider
C_1	3/4 Vin
C_2	1/2 Vin
C_3	1/4 Vin

This approach is expandable also to achieve higher voltage conversion ratio as done by [17]. It utilizes modified 6 to 1 Dickson topology to step down the effective input voltage before the buck converter. Using interleaved buck converter concept, these solutions require voltage monitoring on flying capacitors to ensure proper operation.

1.3 Two-Stage VRM

In 2004, before 48V architecture, [18] proposed two stages approach for 12V VRM and achieves higher efficiency than a single stage approach. Similar technique is also applicable to 48V bus architecture in order to divide and conquer the challenges presented. [19] presented two options in two-stage approach:

1.3.1 Factorized Power Architecture (FPA)

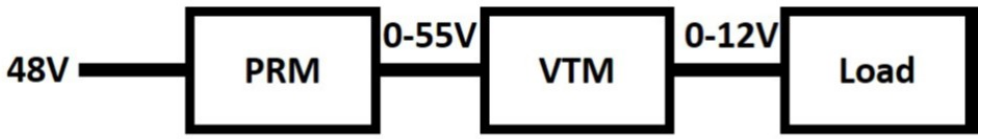


Figure 1.8: Factorized Power Architecture (FPA)

Figure 1.8 shows the basic structure of Factorized Power Architecture (FPA) proposed by VICOR Company in [19]. The first stage of FPA is PRM converter which has input line range of 36V to 55V and outputs a 'factorized bus' that can range from 0 to 55V [19]. PRM converter utilizes Zero-Voltage-Switching Buck-Boost (ZVS-BB) topology in order to provide wide input to output conversion range. By operating at discontinuous conduction mode in addition to precise timing, ZVS-BB eliminates switching loss allowing designers to increase switching frequency and reduce solution size.

FPA utilizes VTM as its second stage converter. VTM is a point of load converter running as a fixed ratio DC transformer to achieve current multiplication and isolation efficiently. VTM utilizes resonant converter such as Sine Amplitude Converter (SAC or LLC) to achieve both zero voltage switching and zero current switching operation allowing high efficient operation at high frequency to reduce solution size. With a fixed ratio conversion

at the second stage, VTM relies on PRM to provide precision regulation at the output from both change in input voltage and output current.

1.3.2 Intermediate Bus Architecture or (IBA)

With the new FPA architecture, industries have to use two new converters and spend more time and money to invest in order to qualify these two converters. However, the conventional Intermediate Bus Architecture (IBA) shown in Figure 1.9 offers an easier way to transition to 48V Bus Architecture.

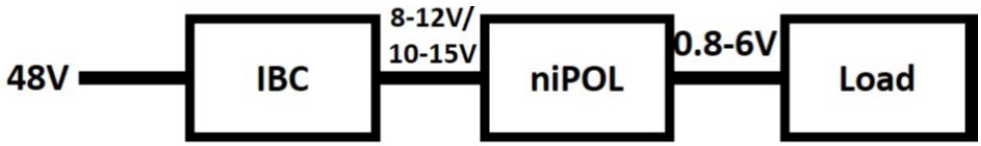


Figure 1.9: Intermediate Bus Architecture (IBA)

Recalling the issue of using a multi-phase buck converter as VRM, the step down ratio is too large, hence the low duty cycle operation. In order to solve such issue, [18] and [20] proposed Intermediate Bus Architecture or IBA. The first stage of IBA is intermediate bus converter or IBC. IBC provides lower intermediate bus voltage for the following point of load converter (POL).

By having lower intermediate bus voltage, IBA allows designers to use multi-phase buck as its point of load converter in order to fulfill the high efficiency and dynamic processor units (CPU or GPU) requirement. Using multi-phase buck converters as POL eases industries to transition to 48V bus architecture. Similar to any series power architecture, in order to achieve high efficiency, IBC has to operate efficiently.

Intermediate Bus Converter

In order to achieve high efficiency step down DC transformer, the CPES in [10] proposed IBC using LLC converter. As discussed previously, when switching frequency f_{sw} is set to its resonant frequency, f_o, LLC achieves ZVS and ZCS across all load range, allowing high frequency and high current operation. The LLC based IBA VRM is shown in Figure 1.10. By operating at high frequency and employing matrix transformer, it makes high density solution possible. However, the complication on designing matrix transformer and high layer counts PCB persist in this approach.

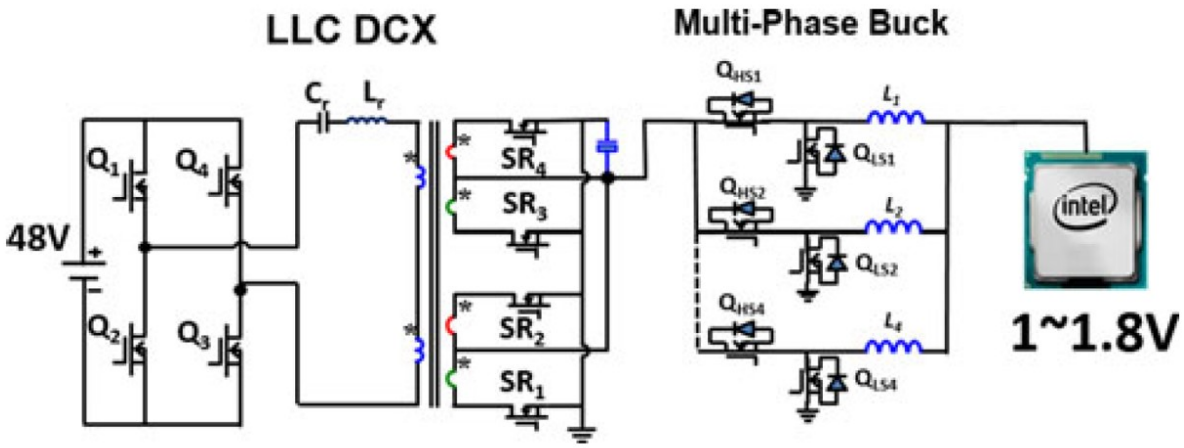


Figure 1.10: 2 Stages Voltage Regulator Module using LLC as IBC [10]

Isolated IBCs are commonly used in both telecommunication and data center application to prevent power spikes that propagates from the front-end ac-dc converter to damage components on the server. However, isolation is only found as an over-provisioned safety requirement for modern IBCs, since there is no spike in modern data center. In addition to that, isolation circuitry limits the power density of IBCs, and as a result, non isolated or transformer-less approach becomes more attractive in the data center [3].

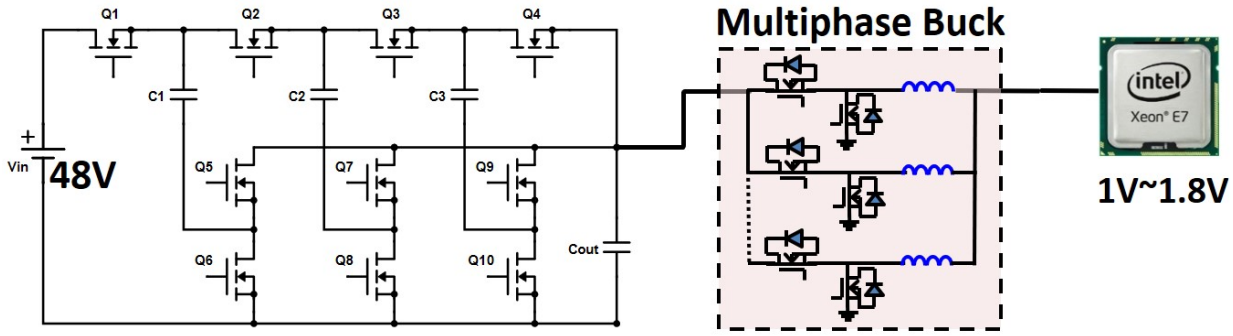


Figure 1.11: 2 Stages Voltage Regulator Module using Switched-Capacitor Voltage Divider as IBC

This thesis focuses on another possible solution using switched-capacitor voltage divider (SCC) as IBC. SCC utilizes only capacitors and it eliminates the use of magnetic, hence it has potential of having higher power density than magnetic based solution. [21] and [22] built IBC for 12V VRMs and found that it can improve VMRs efficiency further. However, with the higher input voltage of 48V, 2 to 1 SCC used in [21] is insufficient. In 48V bus architecture, we need to use SCC with 4 to 1 voltage conversion ratio (VCR) or higher. However, the model developed in [22] only works for 2 to 1 SCC.

[23] provides another approach in analyzing SCC using fast and slow switching limit (FSL and SSL) approximation. SSL assumes the switching frequency to be very slow and the loss is purely charge transfer loss. In the case of FSL, it assumes the capacitors are ideal voltage source, hence the conduction loss is only determined by devices' on resistance.

Both approaches provide a good insight of SCC converters, however in order to acquire accurate loss model and optimization method, it is necessary to derive time domain model of SCC as proposed by [21] and [22]. This thesis expands the timde domain model to provide optimization method for high VCR SCC using Dickson expansion.

In this thesis, I also explore the new Resonant Switched-Capacitor Converter (RSCC)

proposed by [1]. RSCC increases conventional SCC's efficiency and density by the mean of adding a small inductor. I provide the detailed analysis on both conduction and switching loss to illustrates the benefit and issues that come with RSCC. Based on these analysis, I propose a kind of Resonant Switched-Capacitor Converter using Multiple Resonant Frequency or MRSCC.

1.4 Thesis Outline

From the above discussion, the CPES explored both single stage using sigma and two stages solution using IBA approach. However, in this thesis, i will focus on the investigation of intermediate bus converter using transformer-less approach by the means of utilizing switched-capacitor based circuit.

This thesis consists of five chapters organized as follows:

Chapter 1 provides an introduction of the research background. It presents two general approaches done by many researchers and industries. The challenges of each approach are illustrated in detail.

Chapter 2 presents the basic of transformer-less IBC approach using Switched-Capacitor Converter. Switched-Capacitor Converter(SCC) is known to have high density and high efficiency performance, which is fit for data center's Voltage Regulator Modules. The basic cell, 2 to 1 SCC, is expandable to high voltage conversion ratio (VCR) SCC. Dickson star in this case is found to be the most efficient for high VCR and current operation. However, due to hard charging mechanism , it requires high capacitance in order to achieve high efficiency which defeats the purpose of avoiding transformer. The detailed analysis for both 2 to 1 and Hgh VCR Dickson SCC topology are provided in Chapter 2.

Chapter 3 presents state of the art solution of soft-charging switched-capacitor circuit, called Resonant Switched-Capacitor Converter. In order to solve hard charging issue in pure SCC, [1] proposed to insert a small inductor in series to the flying capacitor. By operating this new structure at $f_{sw} = f_o$, it achieves soft charging mechanism between capacitors, hence lowering conduction loss, and lossless transition switching loss. In order to achieve this high efficiency operation, RSCC has to use very low tolerance and variation components or zero current detection control. Hence, it is not fit for high volume production. Chapter 3 provides the loss analysis and analytic explanation on tolerance issues on RSCC.

In Chapter 4, a novel Multi Resonant Switched-Capacitor Converter (MRSCC) is proposed. MRSCC employs two LC resonant tanks to partially replace flying capacitors for energy transfer. During the dead-time in between two states of operation, second resonant tank recycles energy from the main resonant-tank allowing MRSCC to utilize conduction time more effectively to deliver energy while becoming more resilience towards components variation due to voltage coefficient and tolerance of Multi Layer Ceramic Capacitors (MLCC). These attributes of MRSCC make it viable for industry's high-volume adoption. Chapter 4 presents operation principle, loss analysis, optimization and high voltage conversion ratio implementation of MRSCC and compare with state of the art solutions.

Chapter 2

Switched-Capacitor Converter (SCC) Voltage Divider

Due to its simplicity and high density property, many look switched-capacitor converter (SCC) as one of the contenders to be Intermediate Bus Converter (IBC) candidates. [24] proposed 2 to 1 SCC voltage divider as the first stage in a 2 stages 12V Voltage Regulator Module (VRM) and showed that it performed better than its single stage solution counterpart. By having a 2 to 1 SCC voltage divider as the first stage, it allows the second stage to use lower voltage devices, R_{ds} and output capacitance. Additionally, by having effectively lower input voltage, we can further increase switching frequency to reduce inductor size, hence smaller solution. However, for 48V bus architecture, 2 to 1 SCC voltage divider ratio is insufficient and we have to explore higher voltage conversion ratio (VCR) voltage divider in order to utilize the benefit of SCC.

2.1 SCC Principle Operation

Unlike buck converter, SCC voltage divider circuit doesn't use magnetic as the mean to step down input voltage, instead, it only utilizes capacitor networks. This allows high density voltage regulator module (VRM) design as SCC voltage divider as Intermediate Bus Converter (IBC).

Figure 2.1 shows the basic cell of 2 to 1 SCC voltage divider. SCC voltage divider utilizes one flying capacitor, C_2, as mean of delivering energy to the output, and one output filter capacitor, C_o. Two active switches, Q_1 and Q_2 are operated with 50% duty cycle alternately with Q_3 and Q_4 are driven synchronously to Q_1 and Q_2 respectively as synchronous rectifiers (SR).

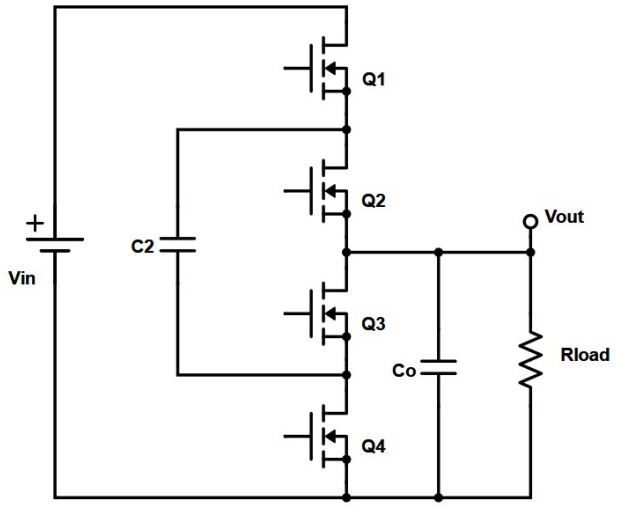


Figure 2.1: Basic Cell of 2 to 1 Switched-Capacitor Voltage Divider

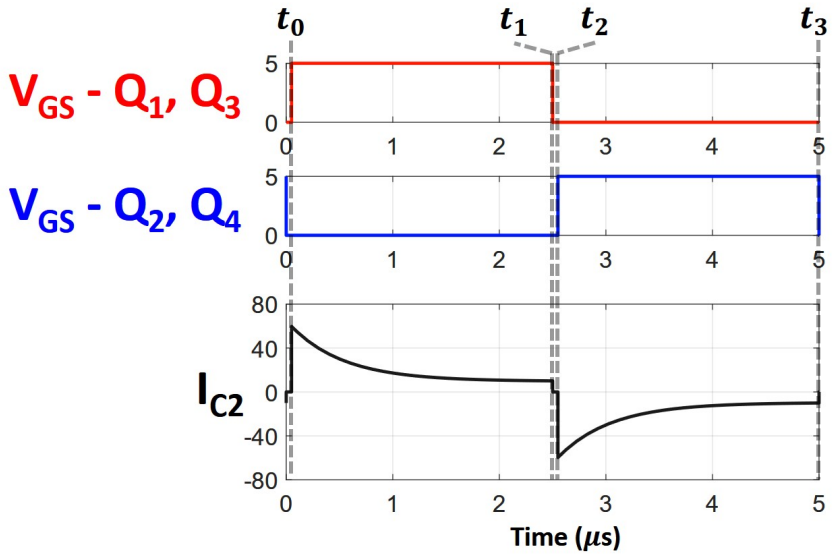


Figure 2.2: 2 to 1 Switched-Capacitor Voltage Divider Steady State Operation Waveform

With 50% duty cycle, SCC comes with two states of operation described bellow.

1. t_0 to t_1

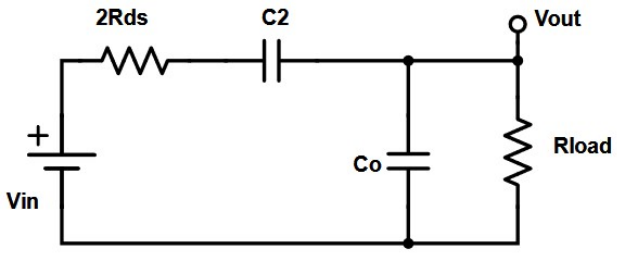


Figure 2.3: SCC Voltage Divider 1st State of Operation

The first state of SCC is marked by t_0 to t_1 in Figure 2.2. At this state, Q_1 and Q_3 are 'on' making Capacitors C_2 and C_o in series to each other. The input voltage delivers energy to the output at the same time charging C_2 for the next state. In steady state, the sum of C_2's and C_o's voltages should equal to its input voltage.

$$V_{in} = V_{C_2} + V_{C_o} \tag{2.1}$$

2. t_2 to t_3

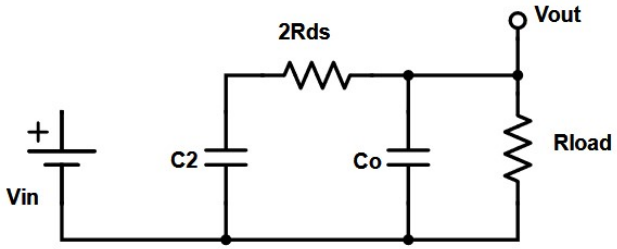


Figure 2.4: SCC Voltage Divider 2nd State of Operation

The second state of operation is marked by t_2 to t_3 in Figure 2.2. Q_2 and Q_4 are 'on' in this state making C_2 and C_o in parallel supporting output current. C_2, pre-charged during

first state, deliver its energy to load. The difference in voltage of C_2 and C_o divided by two devices' R_{ds} creates pulse current of C_2, hence SCC utilizes hard-charging and discharging mechanism. In steady state, the bias voltage of C_2 will be equal to C_o's.

$$V_{C_2} = V_{C_o} \tag{2.2}$$

Between t_1 and $_2$, all switches are 'off' disconnecting the capacitors from each other. With two states of operation, the voltage gain of 2 to 1 SCC voltage divider can be calculated to be 0.5, hence the name 2 to 1 SCC voltage divider.

$$V_{out}/V_{in} = 0.5 \tag{2.3}$$

2.1.1 Loss Analysis of SCC Voltage Divider

Similar to other converters, we can separate the loss in SCC into conduction and switching related loss. In this subsection we will analyze both types of loss.

Switching Loss Analysis

Unlike buck converter, absent inductor, SCC voltage divider provides some advantages in regards of switching mechanism. Below are the analysis of both turn 'off' and 'on' mechanisms of SCC voltage divider.

Figure 2.5 shows the event when Q_1 and Q_3 are turning off marked between t_0 to t_1. Drain to source current of Q_1 and Q_3 go to zero following the flying capacitor's, C_2, current. However, due to the absence of inductor, there is no charging or discharging C_{oss} keeping the voltages across devices persist. Hence, between t_0 and t_1, drain to source voltage of Q_1 and

Q_3 ($V_{ds\text{-}Q1}$ and $V_{ds\text{-}Q3}$) stay at 0, eliminates transition loss of voltage and current overlap. Due to symmetrical operation, this lossless turn off mechanism also exists during Q_1 and Q_2 turn off operation.

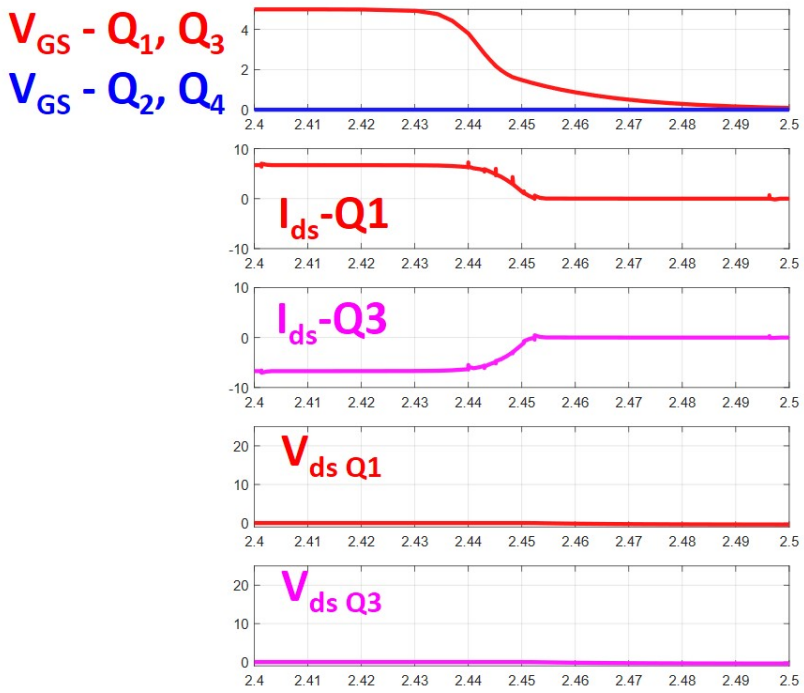


Figure 2.5: 2 to 1 Switched-Capacitor Voltage Divider Q_1 and Q_3 Turn 'Off'

Figure 2.7 shows the event of Q_2 and Q_4 turning 'on', marked by t_2 and t_3. When the gate to source voltage ($V_{gs\text{-}Q2 \text{ and } Q4}$) pass their threshold, V_{th}, at t_2, Q_2 and Q_4 start to discharge their drain to source capacitances and current from V_{in} will charge Q_1's and Q_3's drain to source capacitances through Q_2's and Q_4's channels, hence the spike on drain to source current of Q_2 and Q_4 between t_2 and t_3. During this process, C_2 doesn't deliver any charge to the output. Due to its symmetrical operation, it will have the same mechanism for Q_1 and Q_3 turn 'on' event. Hence this show SCC voltage divider's turn on loss is determined only by its charging and discharging of devices' output capacitance, C_{oss}.

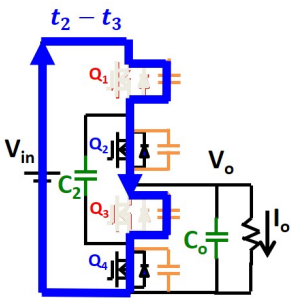


Figure 2.6: Q_2 and Q_4 Turn 'On' Equivalent Circuit of 2 to 1 SCC Voltage Divider

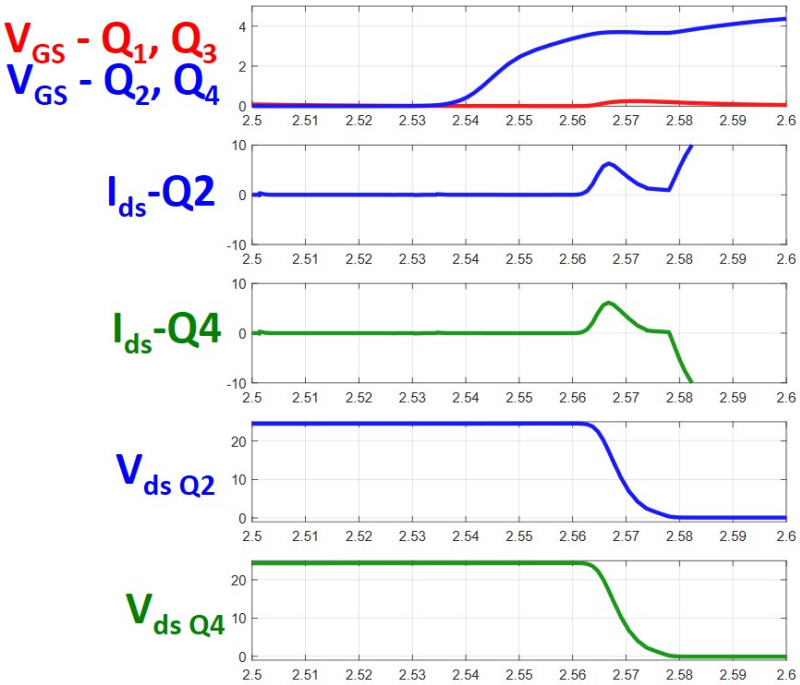


Figure 2.7: Q_2 and Q_4 Turn 'On' Waveform of 2 to 1 SCC Voltage Divider

With the lossless turn off and C_{oss} driven turn on loss, 2 to 1 SCC Voltage Divider's switching loss can be calculated as follow:

$$P_{sw} = (Q_{oss1} + Q_{oss2} + Q_{oss3} + Q_{oss4})V_{out}f_{sw} \tag{2.4}$$

Conduction Loss

[23] presented two ways to model conduction loss in a SCC; Slow Switching Limit (SSL) and Fast Switching Limit (FSL). These two methods simplify the conduction loss analysis based on its operating frequency relative to its time constant of the RC circuit. When operated at such a low frequency, the conduction loss is dominated by SSL. SSL assumes the resistance along the current path is very small and the loss comes from charge transfer between capacitors in a form of impulsive current. In FSL, the switching frequency is higher than its time constant, where the capacitors are considered effectively perfect voltage sources, hence the conduction loss only comes from the interconnect resistance along the current path. Designing SCC in FSL will give the best efficiency performance, however it also means over designing SCC and it will reduce the density of total solution. Hence, in order to understand the region between FSL and SSL, [22] proposed time domain analysis of SCC voltage divider.

For the sake of simplicity, the parasitic inductor and equivalent series resistor (esr) in the capacitors are ignored in this analysis. Both equivalent circuits in Figure 2.3 and 2.4 show the flying capacitor C_2 is always in series with the devices' on resistance (R_{ds}), hence we are able to utilize C_2's current to represent system's conduction loss. Therefore, it is necessary to obtain $i_{C_2}(t)$.

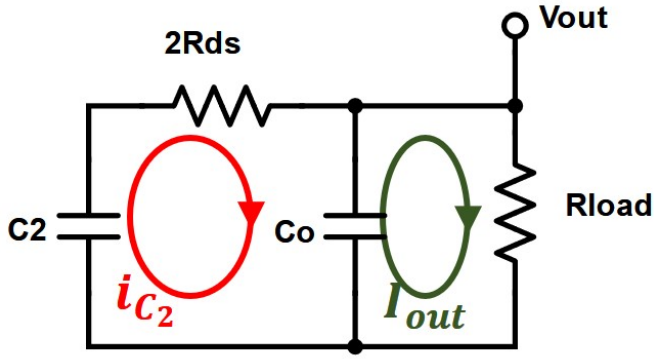


Figure 2.8: Final Equivalent Circuit for 2 to 1 SCC Voltage Divider

Assuming ideal input voltage, both equivalent circuits can be simplified to Figure 2.8. Using Kirchoff's Voltage Law (KVL) we can obtain:

$$V_{C_2} + i_{C_2} R + V_{C_o} = 0 \tag{2.5}$$

It is important to note that:

$$R = 2R_{ds} \tag{2.6}$$

Taking a derivative of equation 2.5, we obtain differential equation (ODE) equation 2.7.

$$R\frac{\partial i_{C_2}}{\partial t} + \frac{C_2 + C_o}{C_2 C_o} i_{C_2} - \frac{I_{out}}{C_o} = 0 \tag{2.7}$$

By solving ODE 2.7, we obtain general solution as shown:

$$i_{C_2}(t) = (Ke^{-t/\tau} + \frac{C_2}{C_2 + C_o}) I_{out} \tag{2.8}$$

with τ is defined to be:

$$\tau = RC_2C_o/(C_2 + C_o) \tag{2.9}$$

Based on conservation of energy, input energy should equal to output energy, hence

$$Q_{in}V_{in} = Q_{out}V_{out} \tag{2.10}$$

SCC's input voltage only conducts of half of its period, therefore

$$V_{in}\int_0^{T_{sw}/2} i_{V_{in}}(t)dt = V_{out}\int_0^{T_{sw}} i_{out}(t)dt \rightarrow \bar{I}_{V_{in}} = I_{out} \tag{2.11}$$

In order to solve K, we can utilize conservation of energy equations 2.10 and 2.11.

Figure 2.3 shows that the input current is the flying capacitor's current, hence the average of $i_{C_2}(t)$ for half a period will equal to output current. Using this property, we can then solve K to be:

$$\frac{2}{T_{sw}}\int_0^{T_{sw}/2} i_{C_2}(t)dt = I_{out} \rightarrow K = \frac{T_{sw}}{2RC_2(1-e^{-T_{sw}/2\tau})} \tag{2.12}$$

The final solution of C_2's current in time domain will be:

$$i_{C_2}(t) = (\frac{T_{sw}}{2RC_2(1-e^{-T_{sw}/2\tau})}e^{-t/\tau} + \frac{C_2}{C_2+C_o})I_{out} \tag{2.13}$$

It is to be noted that $i_{C_2}(t)$ equation described above is only for half a period cycle, however, due to symmetrical operation, the rest of half cycle will have the same shape with negative magnitude. With the solved time domain equation of C_2's current eq 2.13, we can calculate the RMS of each devices current as

$$I_{Q_{RMS}} = I_{C_{2_{RMS}}}/\sqrt{2} \tag{2.14}$$

Assuming same devices for all 4 switches, we then can simplify the conduction loss to:

$$P_{Conduction} = 4I_{Q_{RMS}}^2 R_{ds} = 2(I_{C_{2_{RMS}}})^2 R_{ds} \tag{2.15}$$

Hence, the total loss can be calculated as:

$$P_{loss} = 2(I_{C_{2_{RMS}}})^2 R_{ds} + 4Q_{oss}V_{out}f_{sw} \tag{2.16}$$

2.1.2 SCC Optimization

When optimizing SCC, we can focus the optimization method based on its application. For instance, it is important to choose lowest output capacitance devices for high voltage and low current application because the conduction loss is negligible. However, in this section, we will focus the optimization method on minimizing conduction loss for high current applications such as server rack VRMs.

There are many factors affecting the RMS current of C_2 in SCC such as C_2, C_o, R_{ds} and switching frequency. Hence, in order to understand these parameters, we normalize C_2's RMS current to its output load with normalization terms as follow:

$$k_n = C_2/C_o \tag{2.17}$$

$$\tau_n = RC_o/T_{sw} = RC_o f_{sw} \tag{2.18}$$

$$I_N = I_{C_{2_{RMS}}}/I_{out} \tag{2.19}$$

Using the terms defined, we can obtain the normalized C_2's RMS current to be:

$$I_N = \frac{1}{k_n+1}\sqrt{k_n^2 + 2k_n + \frac{k_n+1}{4\tau_n k_n}\frac{1-exp(-\frac{k_n+1}{k_n\tau_n})}{(1-exp(-\frac{k_n+1}{2k_n\tau_n}))^2}} \tag{2.20}$$

Based on equation 2.20, Figure 2.9 illustrates the relationship between I_N, τ_n and k_n.

Figure 2.9 shows larger value of τ_n and k_n is desirable for high efficiency operation. However, the value of τ_n is usually fixed in most server rack VRMs due to its buck converter

second stage. $f_s w$ of SCC usually runs at the same frequency as the buck converter in order to simplify the EMI filter design, while the C_o of SCC should accommodate as the input filter of the buck converter. In term of switches, we choose the best figure of merit devices with lowest R_{ds} to minimize conduction loss. Therefore, with a fixed τ_n, the only parameter to adjust is C_2's capacitance.

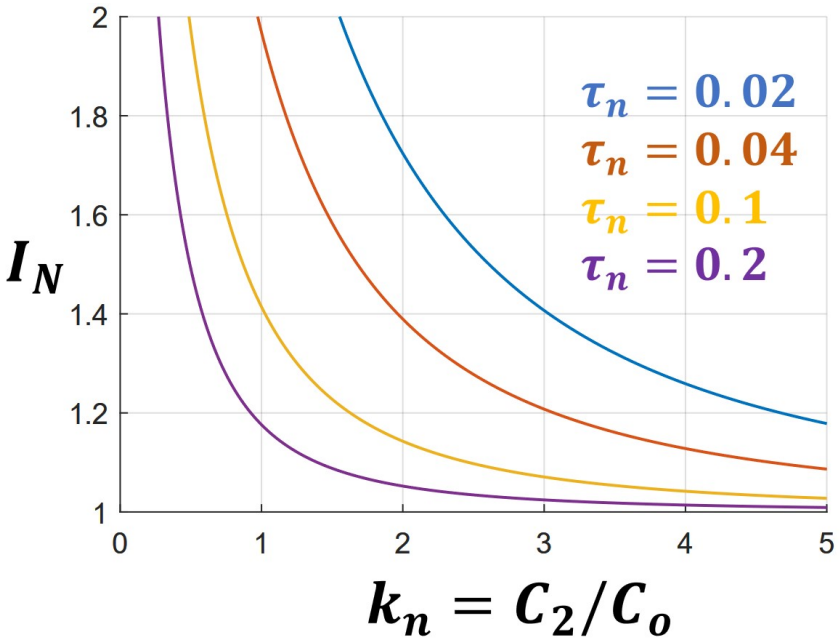
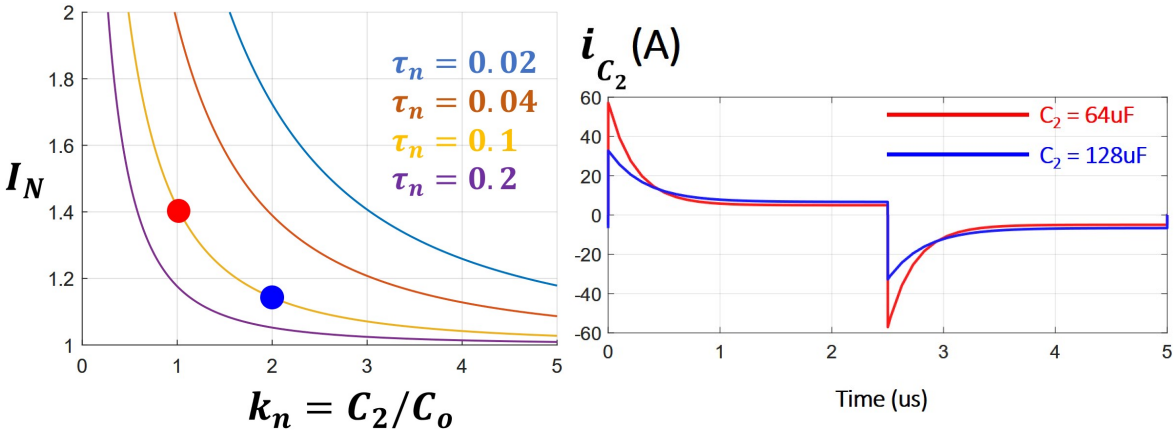


Figure 2.9: 2 to 1 SCC Voltage Divider Normalized Current of C_2 vs. k_n

Table 2.1: 2 to 1 SCC Voltage Divider Specification

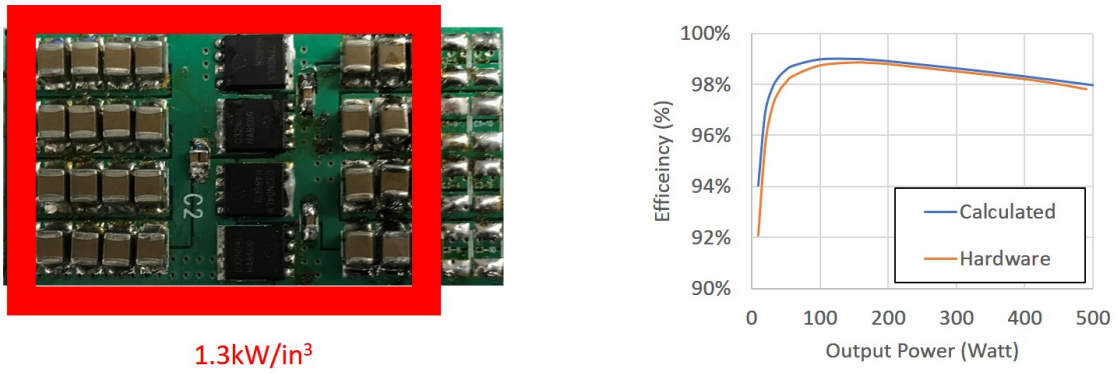
	SCC Voltage Divider
C_o	64μF
F_{sw}	200kHz
R_{ds}	4mΩ
Max Load	20A
Vin Range	40-60V



(a) Doubling C_2 vs. I_N (b) Doubling C_2 vs. Time Domain of i_{C_2}

Figure 2.10: SCC - Capacitance of C_2 vs. I_{C_2}'s RMS

Consider Table 2.1, the specification operates at 0.1 τ_n. As discussed previously, we can only change the value of C_2 to reduce the conduction loss of SCC. Figure 2.10 illustrates the effect of doubling C_2's capacitance to reduce SCC's conduction loss by 40%. It is possible to further reduce conduction loss, however SCC will requires large capacitance of C_2 and it will reduce the power density of total solution.



(a) Hardware (b) Efficiency at Vin = 48V

Figure 2.11: 2 to 1 Switched-Capacitor Converter Verification Hardware

A hardware with specification in Table 2.1 was built to verify the loss model based on the optimization method using 128μF C_2. N-Mosfet from Infenion, BSC032N04LS, was

chosen for SCC verification hardware with 3 to $4m\Omega$ of on resistance. Generally, multi-layers ceramic capacitor (MLCC) is chosen for SCC voltage divider due to its low equivalent series inductance (esl) and low equivalent series resistance (esr).

Figure 2.11 presents the verification hardware for 2 to 1 SCC and its efficiency. The loss model presented in previous section matches well with the hardware results. With the presented optimization method, we can achieve 99% peak efficiency with power density of 1.3kW/in^3. 2 to 1 SCC voltage dividers prove to be very efficient and have high density, however, server rack VRM applications requires higher voltage conversion ratio (VCR) SCC which will be presented in the next section.

2.2 High Conversion Ratio SCC Voltage Divider

2.2.1 Dickson Star SCC

In previous section, 2 to 1 SCC voltage divider is discussed extensively, however in reality, when designing VRMs for 48V bus architecture, it is necessary to utilize higher voltage conversion ratio (VCR) voltage divider. There are many topologies available to do step down conversion, however only one structure shines for high current application, Dickson Star SCC due to low output impedance[23].

Dickson SCC Voltage Divider is an expansion of 2 to 1 SCC Voltage Divider. In order to simplify the analysis, this section only presents 4 to 1 Dickson SCC configuration shown in Figure 4.15. Dickson SCC Voltage divider has similar properties as 2 to 1 SCC voltage divider in regards of its switching frequency and conduction loss. In 4 to 1 configuration, Dickson SCC needs one output capacitor C_{out} and three flying capacitors, C_1, C_2 and C_3, to divide the input voltage by four. Due to its operation, the three flying capacitors are biased

differently in steady state as shown in Table 2.2.

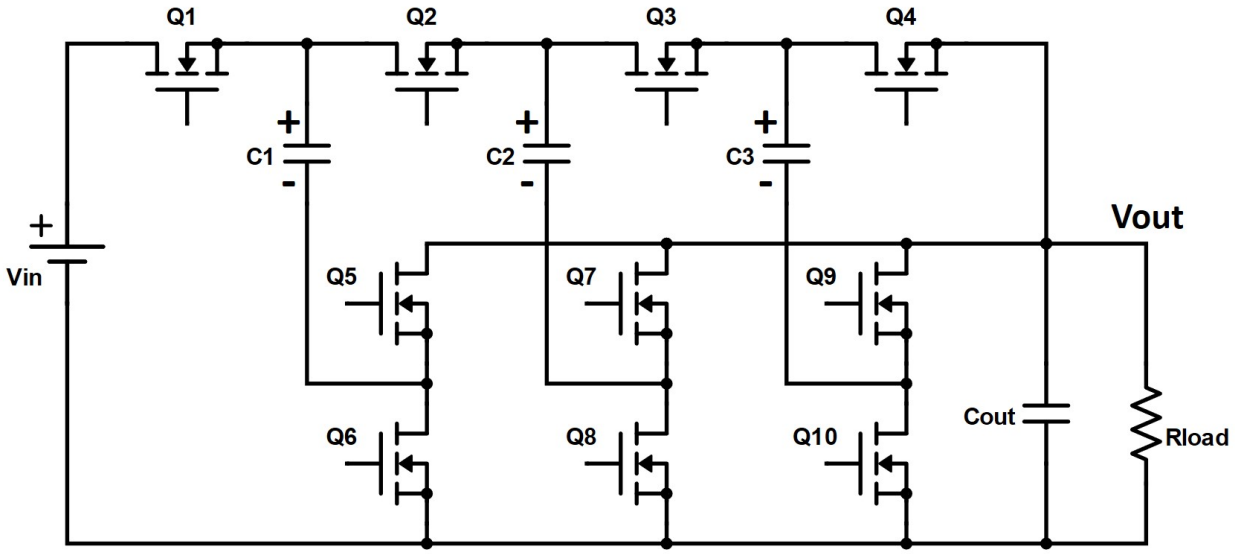
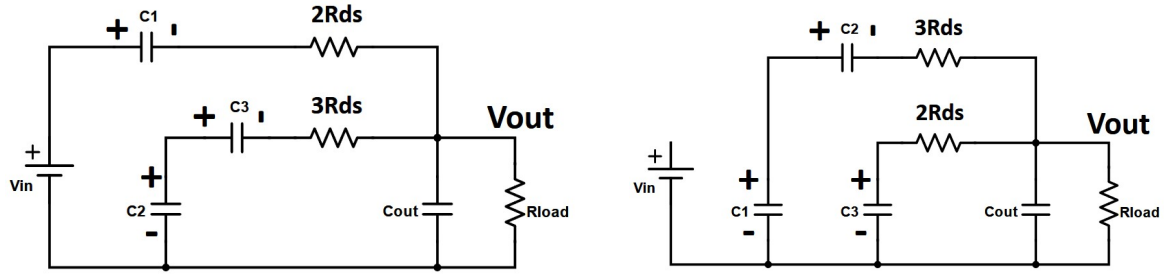


Figure 2.12: 4 to 1 Dickson SCC Voltage Divider

Table 2.2: DC Bias of 4 to 1 Dickson SCC Voltage Divider

Capacitor	Voltage Bias
C_1	$3V_{out}$
C_2	$2V_{out}$
C_3	$1V_{out}$



(a) Q_1, Q_3, Q_5, Q_8 and Q_9 are 'on' (b) Q_2, Q_4, Q_6, Q_7 and Q_{10} are 'on'

Figure 2.13: 4 to 1 Dickson SCC Equivalent Circuits

With 50% duty cycle operation, Dickson SCC has two states of operation as shown in Figure 2.13. The first state is when Q_1, Q_3, Q_5, Q_8 and Q_9 are 'on' as shown in Figure 2.13a. Within this state 4 to 1 Dickson SCC has two power conduction paths in supporting its output load. First loop being the input voltage in series with C_1 and the second loop being C_2 in series with C_3. While supporting load, both input voltage and C_2 are charging C_1 and C_3 respectively preparing for the next state.

The second state of operation is when Q_2, Q_4, Q_6, Q_7 and Q_{10} are 'on' as shown in Figure 2.13b. In this state, C_1, being pre-charged from the previous state, in series with C_2 supporting output load. While supporting load, C_1 is also charging C_2 in preparation for the next state. C_3 in the other loop supporting the output load. Both states show two conduction paths and each path only supplies half of output power, therefore it reduces the current stress on devices and lower impedance seen at the output.

With the discussion in regards of the 4 to 1 Dickson SCC's two states of operations, we can see that there are two power conduction paths. Effectively each devices is stressed only by half of its output average current. This number of power paths increases as VCR goes up. For instance, in 6 to 1 Dickson SCC it has three power paths. Due to this property, Dickson SCC has the lowest output impedance in comparison to other topologies for high current applications, such as server rack VRMs.

2.2.2 Dickson SCC Flying Capacitors' Current

Having multiple conduction paths is definitely an advantage of Dickson SCC to reduce the conduction loss, however it also complicates the Dickson SCC design. To simplify the analysis, this section only provides 4 to 1 Dickson SCC. In 4 to 1 Dickson SCC, we have three different capacitors with three different value, however we have to ensure symmetrical

operation in order to optimize the stress distribution on devices. Assuming the input is ideal voltage source, we can define:

$$C_1 = C_3 = C_x \tag{2.21}$$

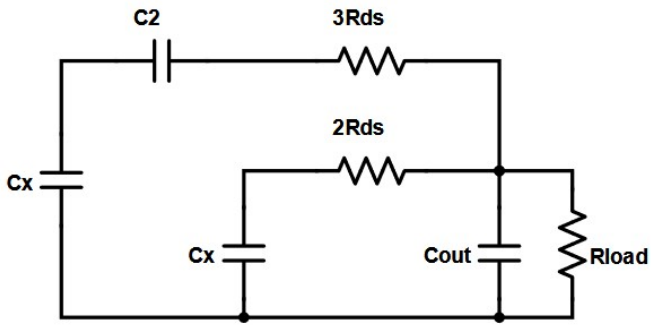


Figure 2.14: Equivalent Circuit of 4 to 1 Dickson SCC

By having the same value of capacitance for C_1 and C_3, we can simplify both states of operation into a single equivalent circuit shown in Figure 2.14. Once simplified, we now have two loops. Having more than 2 loops, the system has become higher order system due to interaction between loop. Although the two loops are interacting with one another, we can use super position in order to isolate and analyze the extra loop. we define:

$$C_{eff} = (1/C_2 + 1/C_x)^{-1} \tag{2.22}$$

Considering the extra loop in Figure 2.15. The extra loop it self is a RC circuit with charge balancing mechanism between the two capacitors. Time domain solution of the extra loop current can be solved as equation 2.23.

$$i_{loop} = i_o e^{-t/\tau_l} \tag{2.23}$$

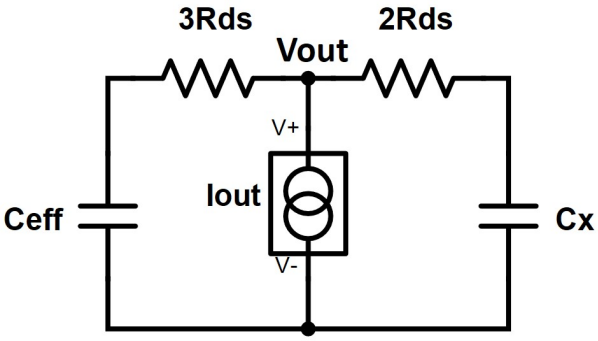


Figure 2.15: Isolated Interacting Loop of Dickson SCC

$$\tau_l = 5R_{ds}C_{eff}C_x/(C_{eff} + C_x) \tag{2.24}$$

$$i_o = V_{C_{eff}}(0)/3R_{ds} - V_{C_x}(0)/2R_{ds} \tag{2.25}$$

Based on equation 2.23-2.25, although the loop will be damped by the $5R_{ds}$, initial current of i_o has to be minimized by ensuring the two initial voltages are equal in magnitude. Only by doing so we can isolate the two main power loop from interacting each other. Using the energy balance, each power path conducts half of average output current, hence:

$$\frac{I_o/2}{C_{eff}3R_{ds}} = \frac{I_o/2}{C_x 2R_{ds}} \rightarrow C_{eff} = \frac{2}{3}C_x \tag{2.26}$$

Recall that C_{eff} is C_2 in series with C_x, hence we can recalculate C_2 in term of C_x:

$$C_{eff} = \frac{C_2 C_x}{C_2 + C_x} = \frac{2}{3}C_x \rightarrow C_2 = 2C_x \tag{2.27}$$

Once we have built the relationship between C_1, C_2 and C_3, we can now model the time domain solution. Since two power paths have been isolated using capacitance relationship,

we can assume a first order solution for C_2's current as:

$$i_{C_2}(t) = I_{pk}e^{-t/\tau} + I_{DC} \tag{2.28}$$

Using capacitor current divider, we can calculate I_{DC} as:

$$I_{DC} = \frac{C_{eff}}{C_{eff} + C_x + C_o} I_{out} = \frac{2C_x}{5C_x + 3C_o} I_{out} \tag{2.29}$$

At the end of half period, Dickson SCC has accumulated energy within capacitors in a form of voltage ripple. This ripple determines the peak current on the next state as shown in eq 2.30.

$$\Delta V = i_{C_2}(@T_{sw}/2)R + \Delta V_{C_{eff}} \tag{2.30}$$

Using conservation of energy equation 2.10, we can obtain the ripple of C_{eff}:

$$\Delta V_{C_{eff}} = \frac{I_{out}/2}{C_{eff}}(T_{sw}/2) \tag{2.31}$$

Dividing eq 2.30 by the series resistance, we obtain:

$$I_{pk} + I_{DC} = \frac{(I_{pk}e^{-T_{sw}/2\tau} + I_{DC})R + \Delta V_{C_{eff}}}{R} \tag{2.32}$$

note that:

$$R = 3R_{ds} \tag{2.33}$$

Hence, using the equation 2.30-2.32, we can calculate the I_{pk} value:

$$I_{pk} = \frac{3T_{sw}}{8RC_x(1 - e^{-T_{sw}/2\tau})} I_{out} \tag{2.34}$$

In order to solve for the time constant, we have to use energy balance property one more time:

$$\frac{2}{T_{sw}}\int_0^{T_{sw}/2} i_{C_2}(t)dt = I_{out}/2 \rightarrow \tau = \frac{2}{3}RC_x\frac{C_x+3C_o}{5C_x+3C_o} \tag{2.35}$$

Figure 2.16 shows model verification by simulation. The condition of the simulation is $C_x = C_o = 100\mu F$, switching frequency of 400kHz, R_{ds} of 1mΩ and I_{out} of 41.67A. The model gives 31.68A RMS vs. 29.9A RMS for C_1 and C_3 and 30.7A RMS for C_2 from simulation. Although there is a minuscule discrepancy on C_1 and C_3's current, the derived time domain capacitor current model of Dickson 4 to 1 matches well with the simulation, hence it can be utilized for Dickson 4 to 1 SCC optimization. C_2 oriented model derivation introduces small discrepancy in C_1 and C_3's current. With this model verification by simulation, this concludes the analysis and model of flying capacitor's current.

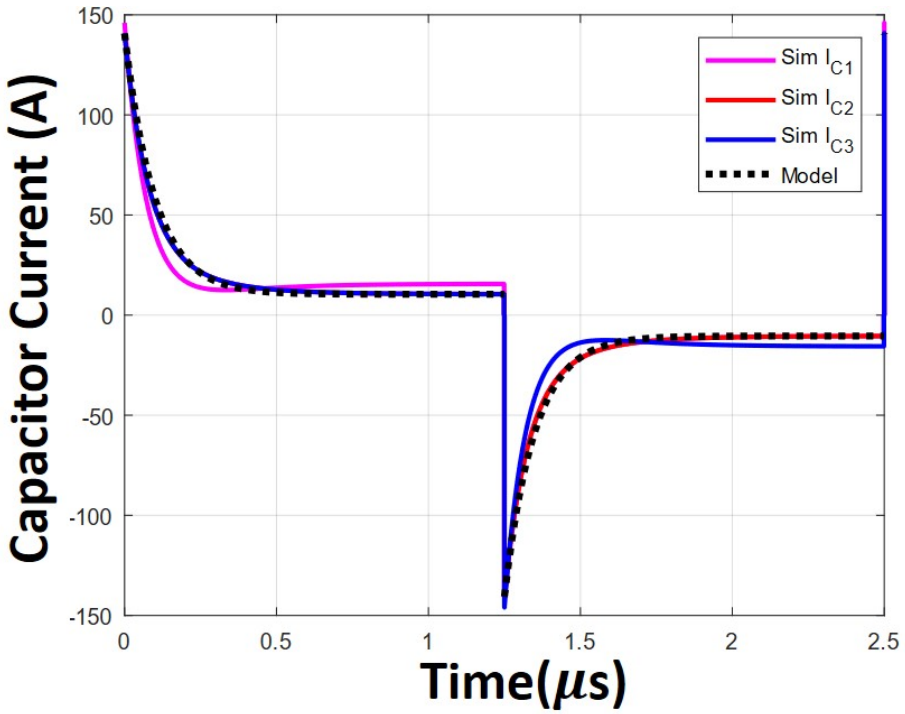


Figure 2.16: Model Verification by Simulation of 4 to 1 Dickson SCC

2.2.3 Dickson Star SCC Optimization

Similarly as 2 to 1 SCC Voltage divider, during light load condition the efficiency of Dickson SCC Voltage Divider is driven by devices' output capacitance of C_{oss}, however during heavy load condition, the switching loss becomes negligible. Therefore, in this section we can focus our analysis on conduction loss for high current applications, such as server rack VRMs.

Using similar normalization method as 2 to 1 SCC voltage divider, we obtain the normalized current of 4 to 1 Dickson Switched Capacitor:

$$\tau_n = RC_o/T_{sw} = RC_o f_{sw} \tag{2.36}$$

$$k_n = C_x/C_o \tag{2.37}$$

$$I_N = I_{C_{2_{RMS}}}/I_{out} \tag{2.38}$$

$$I_N = \frac{1}{5k_n+3}\sqrt{6k_n^2+6k_n+\frac{3(k_n+3)(5k_n+3)}{32k_n\tau_n}\frac{(1-e^{-1/c})}{(1-e^{-1/2c})^2}} \tag{2.39}$$

with c to be:

$$c = \frac{2}{3}\frac{k_n+3}{5k_n+3}\tau_n k_n \tag{2.40}$$

Figure 2.17 illustrates the relationship between I_N, τ_n and k_n based on eq 2.39. Similar to 2 to 1 SCC, Dickson SCC requires large flying capacitors, in this case, represented by C_x. Including C_1, C_2 and C_3, the required flying capacitors will be 4 times of C_x value. In addition, when using multi-layers ceramic capacitor (MLCC) for Dickson SCC, such as X7R

MLCCs, we have to include the voltage bias effect on capacitance as it decreases when bias voltage increases. Therefore, using Dickson SCC in server rack VRMs will diminish its high density property because it will requires large physical space for capacitors.

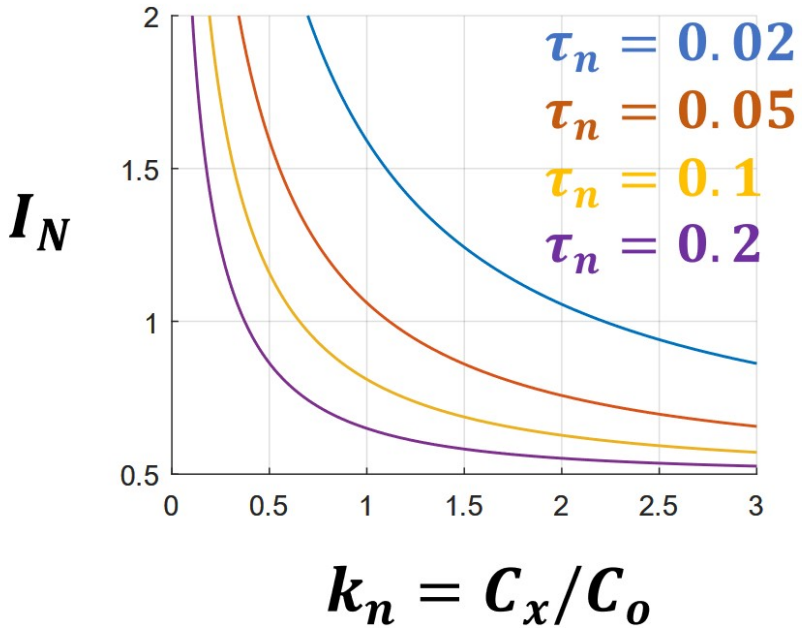
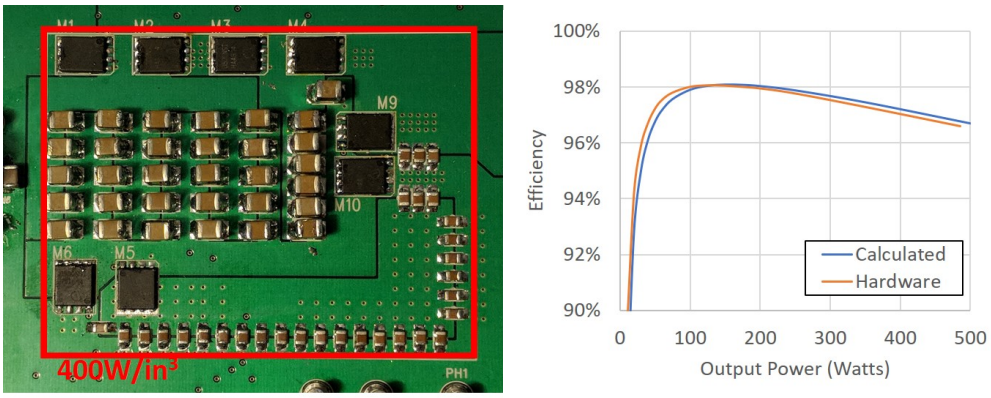


Figure 2.17: Normalized Capacitor Current of 4 to 1 Dickson SCC Voltage Divider

Table 2.3: 4 to 1 Dickson SCC Voltage Divider Specification

	SCC Voltage Divider
C_o	60μF
C_1	140μF
C_2	400μF
C_3	500μF
F_{sw}	200kHz
R_{ds}	1.5mΩ
Max Load	40A
Vin Range	40-60V



(a) Hardware

(b) Efficiency at Vin = 48V

Figure 2.18: 4 to 1 Dickson Switched-Capacitor Converter Verification Hardware

Figure 2.18 shows model verification hardware for 4 to 1 Dickson SCC with parameters shown in Table 2.3. The capacitors are designed higher than intended in order to compensate voltage bias effect on X7R MLCCs. Regardless the model matches well with the calculated result, Dickson SCC is not suitable for server rack VRMs due to its high volume capacitors requirement to achieve high efficiency. This concludes the analysis of Dickson SCC.

Chapter 3

Resonant Switched-Capacitor Converter

3.1 RSCC Principle Operation

Based on the analysis in previous section, Switched-Capacitor Converter(SCC) requires a large amount of capacitors in order to reduce conduction loss. [1] introduces a hybrid SCC by inserting a resonant inductor in series to its flying capacitor, hence the title Resonant Switched-Capacitor Converter (RSCC). Figure 3.1 shows the basic cell of 2 to 1 RSCC voltage divider.

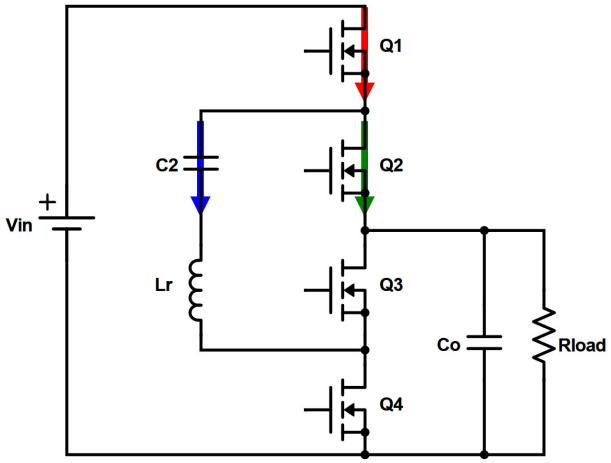


Figure 3.1: Resonant Switched-Capacitor 2 to 1 Voltage Divider Schematic

In order to reduce the density of SCC, it is necessary to reduce C_2's capacitance. However, due to hard charging mechanism, it only increases the peak C_2's current and its RMS value. Modifying SCC, RSCC inserts a small inductor L_r in series to its flying capacitor forming a resonant tank with resonant frequency of f_o. Two active switches of Q_1 and Q_2 operate with 50% duty cycle alternately, while Q_3 and Q_4 run synchronously to Q_1 and Q_2 respectively as synchronous rectifier (SR).

C_2 in RSCC operates as resonant capacitor and C_o is an output capacitor and assumed to be very large [1]. Hence the resonant frequency is determined only by C_2 and L_r. Figure 3.2 shows the steady state operation of RSCC. RSCC employs zero-current turn off mechanism by running its switching frequency exactly at its resonant frequency.

$$C_2 \ll C_o \tag{3.1}$$

$$f_{sw} = f_o = \frac{1}{2\pi\sqrt{L_r C_2}} \tag{3.2}$$

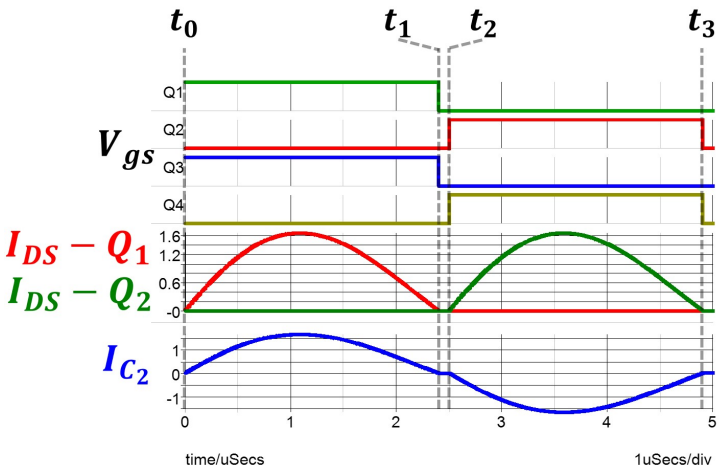
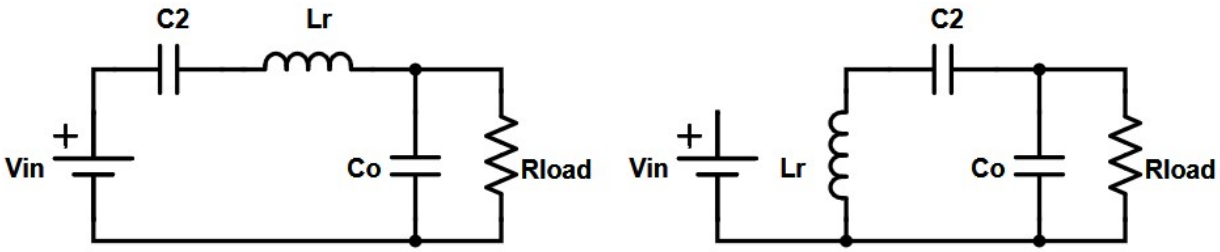


Figure 3.2: RSCC 2 to 1 Voltage Divider Operational Waveform

1. First State of Operation: t_0 to t_1

RSCC's first state of operation is marked by by t_0 to t_1 in Figure 3.2 and with Q_1 and Q_3 are 'on' RSCC will has equivalent circuit as shown in Figure 3.3a. Although the difference in voltage between C_2 and output voltage exists as conventional SCC, the inductor L_r resists sudden change in current and eliminates hard charging mechanism between capacitors. The difference in voltage between C_2 and output becomes 90° phase lead to the inductor current, which starts from zero. RSCC delivers energy in this state for half of its resonant period of L_rC_2 and Q_1 and Q_3 are turned 'off' once the inductor current crosses zero, hence it utilizes zero current turn off mechanism.



(a) t_0 to t_1: 1st State of Operation (b) t_2 to t_3: 2nd State of Operation

Figure 3.3: Two State of Operation Equivalent Circuits of 2 to 1 RSCC Voltage Divider

2. Second State of Operation: t_2 to t_3

The second state of RSCC is marked by t_2 to t_3 in Figure 3.2 and its equivalent circuit shown in Figure 3.3b. In this state, Q_2 and Q_4 are 'on' putting the resonant tank in parallel to the output. During this state, capacitor C_2, pre-charged from previous state, releases its energy through the inductor for half of its resonant period. In the similar manner to the first state, once the inductor current crosses zero, Q_2 and Q_4 are turned 'off' achieving zero current turn off.

3.2 Loss Analysis of RSCC

In this section, we explore the loss analysis of 2 to 1 RSCC voltage divider. However, one has to keep in mind that it is expandable to higher voltage conversion ratio RSCC, such as DIckson RSCC or Switched-Tank Converter (STC) [2].

3.2.1 Conduction Loss

Following the work of conventional SCC, we follow the same approach by deriving time domain equation of RSCC flying capacitor's current in order to model its conduction loss. One has to understand that the resistance along its traces, including devices' on resistance, has to be very small, in other words, RL time constant is much larger than its resonant period, in order to simplify modeling process.

As long as its RL time constant is much larger than its resonant period, regardless its series resistance, RSCC reshapes its flying capacitor's current into sinusoidal waveform when switching frequency is operated at its resonant frequency. Hence,

$$i_{C_2}(t) = I_{pk} sin(t) \tag{3.3}$$

As discussed in Chapter 2, by using conservation of energy property described in equation 2.10 and 2.11, we obtain that the average of 2 to 1 RSCC voltage divider flying capacitor's current for half period will be equal to its output current. By using this property, we can then calculate I_{pk} to be:

$$\frac{1}{\pi}\int_0^{\pi} I_{pk} sin(t) dt = I_{out} \rightarrow I_{pk} = \frac{\pi}{2} I_{out} \tag{3.4}$$

Hence, the RMS of its flying capacitor is:

$$I_{C_{2_{RMS}}} = I_{pk}/\sqrt{2} = 1.11 I_{out} \tag{3.5}$$

In order to understand the effect of output current to its flying capacitor's current, we can then normalize its RMS value using output current to be its normalizing factor. Hence,

$$I_N = \frac{I_{C_{2_{RMS}}}}{I_{out}} = \pi/2\sqrt{2} = 1.11 \tag{3.6}$$

it is notable that its flying capacitor's RMS current is solely dependent on its output current regardless its component choice. In conventional SCC, choosing smaller on resistance devices will result in lowering effective τ_n and it will increase the flying capacitor's RMS current, meanwhile in RSCC, it will only push the RL time constant to be further away than its switching frequency and it does not increase flying capacitor's RMS current.

Similar to conventional SCC, resonant tank of C_2 and L_r are always series to RSCC devices and each devices only conducts for half of its switching period, each RMS current can be calculated based on its flying capacitor's RMS current.

$$I_{Q_{RMS}} = (I_N/\sqrt{2}) I_{out} = 0.785 I_{out} \tag{3.7}$$

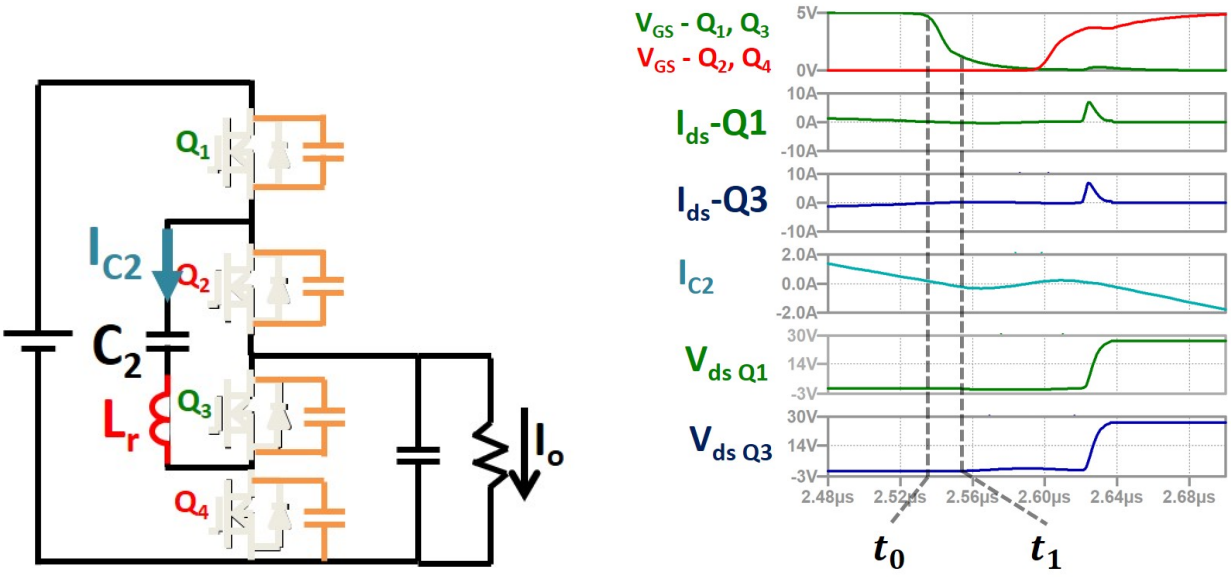
Assuming same devices for Q_1-Q_4, the total conduction loss can be calculated as:

$$P_{cond} = 4(\frac{I_N}{\sqrt{2}})^2 I_{out}^2 R_{ds} = 2 I_N I_{out}^2 R_{ds} \tag{3.8}$$

3.2.2 Switching Related Loss

1. Turn Off

RSCC operates with lossless turn off mechanism. By turning off devices once the inductor reaches zero, RSCC eliminates any current source from charging or discharging devices' output capacitances, C_{oss}. Figure 3.4b shows the turn off mechanism of Q_1 and Q_3. At t_0, after the inductor current reaches zero, gate to source voltages of Q_1 and Q_3 starts to descent until they completely turned 'off' at t_1. Between t_0 and t_1, absence energy in the inductor keeps the drain to source voltages of Q_1 and Q_3 remain unchanged, hence RSCC eliminates turn off transition loss. Due to symmetrical operation, Q_2 and Q_4 turn off event has the same property.



(a) Q_1 and Q_3 turn off Equivalent Circuit

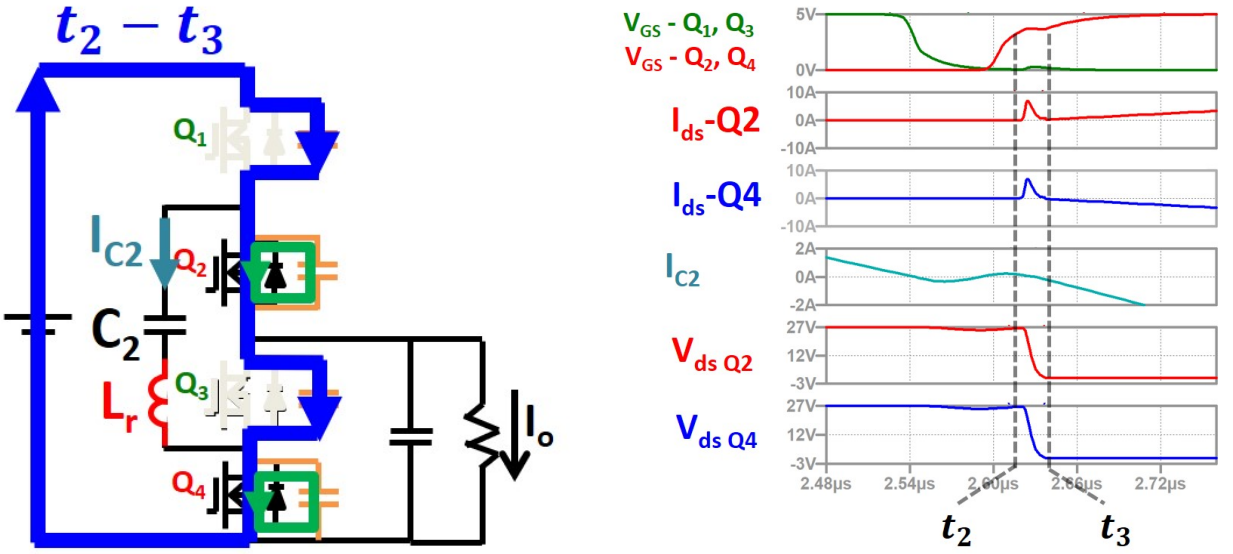
(b) Q_1 and Q_3 turn off Waveform

Figure 3.4: RSCC turn off Mechanism

2. Turn On

RSCC eliminates transition loss during its turn 'on' however it doesnt eliminate output capacitances charging and discharging loss. Figure 3.5b shows Q_2 and Q_4 turning 'on' marked by t_2 to t_3. Once gate to source voltages of Q_2 and Q_4 pass their threshold voltage of V_{th} at t_2, their channel resistances drop to zero. Similar to SCC, Q_2 and Q_4's C_{oss} are being discharged through their own channel while at the same time providing current path for the input voltage to charge output capacitances of Q_1 and Q_3. Once drain to source voltages of Q_2 and Q_4 reach zero at t_3, the inductor current can start to rise from zero. With such turn on mechanism, RSCC eliminates its transition loss however C_{oss} charging and discharging loss still persists as shown in equation 3.9. Due to symmetrical operation, the same turn on mechanism exists during Q_1 and Q_3 turn 'on' event.

$$P_{sw} = (Q_{oss1} + Q_{oss2} + Q_{oss3} + Q_{oss4})V_{out}f_{sw} \tag{3.9}$$



(a) Q_2 and Q_4 turn on Equivalent Circuit (b) RSCC Q_2 and Q_4 turn on Waveform

Figure 3.5: RSCC turn on Mechanism

3.3 Component Variation

3.3.1 Capacitor Material Consideration

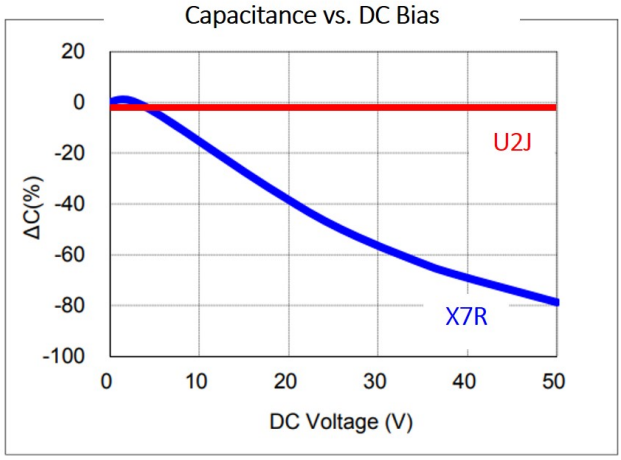


Figure 3.6: DC Bias Effect on U2J vs. X7R

Table 3.1: Class I vs. Class II Multi-layer Ceramic Capacitors

Parameter	Class I	Class II
Type	U2J	X7R
Capacitance	0.27μF	10μF
Part Number	C1210C274M5JAC7800	CL32B106KBJNFNE
Package	1210	1210
Price/pcs at 2000pcs	$0.52	$0.33

Similar as SCC, RSCC utilizes multi-layers ceramic capacitors, MLCC due ot its low equivalent series resistance (ESR) and inductance (ESL). However, Class II ceramic capacitors, such as (X7R, X5R, X7S, etc) is not fit for RSCC due to very wide tolerance band over temperature, DC bias and part to part variance[2]. Figure 3.6 illustrates the change in capacitance of Class II capacitors, such as X7R, in comparison to Class I capacitors, such as

U2J, based on its DC bias voltage. Although X7R has more capacitance over volume, its capacitance drops as bias voltage increases. RSCC requires precise capacitance in order to achieve particular resonant frequency, hence when using X7R, it introduces a wide range of resonant frequency dependent on its input voltage, therefore one has to equipe RSCC with zero current detection control to ensure optimum operation. Class I capacitor, such as C0G, U2J or NP0 utilizes low dielectric materials in order to provide the required stable capacitance for RSCC.

3.3.2 The Effect of Component Variation on RSCC

Using Class I capacitors, such as U2J, only solves one aspect of variation, capacitance over voltage bias. However, Class I capacitors do come with part-to-part variance, and its worst case scenario, it will be 20% of capacitance variation. In addition to capacitance, one has to include part-to-part variation on inductors when produced in high volume. Considering worst case scenario for both flying capacitor and resonant inductor, RSCC and its derivation, such as STC voltage divider in [2], [25] and [26], will have to sustain 20% of resonant frequency variation.

Table 3.2: 2 to 1 RSCC Hardware

	RSCC
C_2	5.4uF U2J
L_r	75nH
C_o	160uF
F_{sw}	238kHz

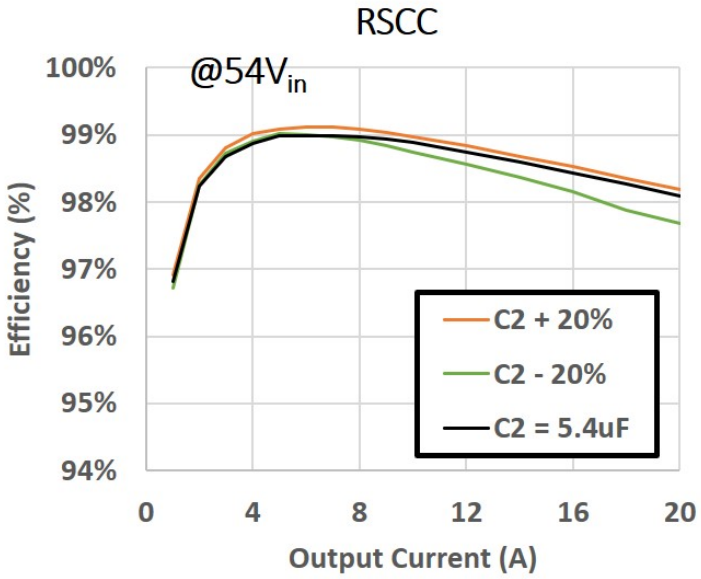
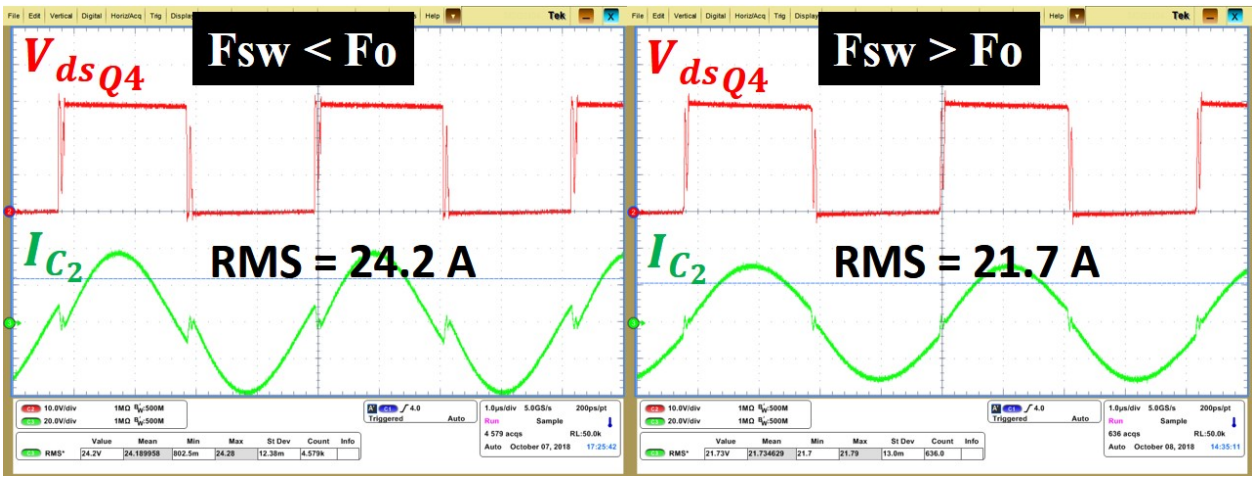


Figure 3.7: RSCC - Efficiency Measurement When C_2 is varied by 20%



(a) $f_{sw} < f_o$ (b) $f_{sw} > f_o$

Figure 3.8: RSCC - Flying Capacitor's Current when $f_{sw} \neq f_o$ at 20A Load, 54 Vin

A 2 to 1 RSCC Verification hardware is built based on the specification in Table 3.2. It is important to note that without zero current crossing turn off control, 20% variation in C_2 capacitance will affect heavy load efficiency of RSCC. When C_2's capacitance is lowered by 20%, its resonant frequency becomes higher, hence $f_{sw} < f_o$. In this condition, the inductor

current will go pass zero, induces negative current turn-off for all switches, therefore it increases the RMS current of each devices as shown in Figure 3.8a

In order to understand the severity of running RSCC without zero current crossing control, we can model the solution of i_{C_2} in time domain. Assuming a mismatch between switching and resonant frequency exists, RSCC will operate with a single sided chopped sinusoidal waveform as shown in Figure 3.9. In this case, we have to implement some dead-time to ensure RSCC can discharge the inductor current back to zero before the next conduction state starts. Hence, the switching period of RSCC contains of two on-times and two dead-times.

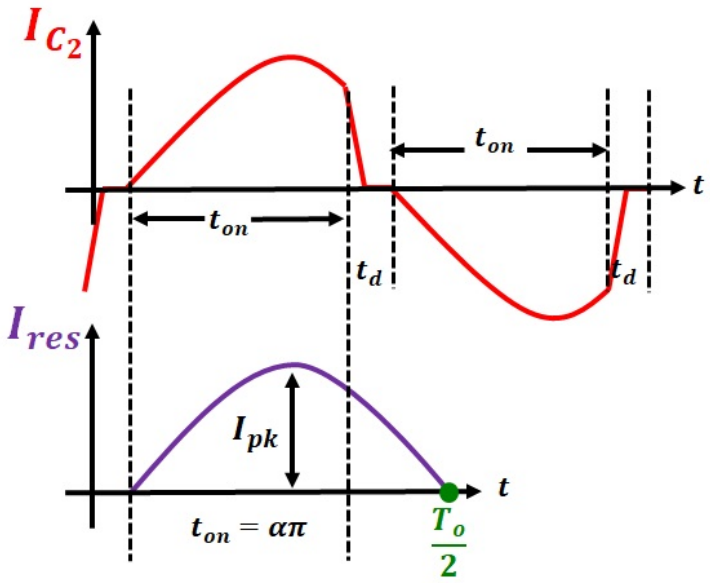


Figure 3.9: RSCC Flying Capacitor's Current Model Derivation

$$T_{sw} = 2t_{on} + 2t_d \tag{3.10}$$

$$\alpha = t_{on}/(T_o/2) \tag{3.11}$$

$$\delta = t_d/T_{sw} \tag{3.12}$$

Based on equation 3.10-3.12, we can obtain piece wise time domain solution of $i_{C_2}(t)$ to be:

$$i_{C_2}(t) = \begin{cases} I_{pk}sin(t), 0 \leq \alpha\pi \\ 0, \alpha\pi < (T_{sw}/T_o)\pi \end{cases} \tag{3.13}$$

Using conservation of energy equation 2.10 and 2.11, the average value of $i_{C_2}(t)$ for half of its period should equal to its output current, hence:

$$I_{pk} = \frac{(f_o/f_{sw})\pi}{1 - cos[(1-2\delta)(f_o/f_{sw})\pi]} I_{out} \tag{3.14}$$

Defining K to be the ratio between switching and resonant frequency,

$$K = f_{sw}/f_o \tag{3.15}$$

we obtain $I_{C_{2_{RMS}}}$ of

$$I_{C_{2_{RMS}}} = \frac{I_{out}}{1 - cos((1-2\delta)\pi/K)} \sqrt{\frac{\pi^2}{2}\frac{1-2\delta}{K^2} - \frac{\pi}{4K}sin(\frac{2\pi(1-2\delta)}{K})} \tag{3.16}$$

Normalizing I_{C2}RMS using normalization factor of I_{out}, Figure 3.10 illustrates the relationship of K and normalized flying capacitor C_2's current. This K-plot explains what happened to RSCC verification hardware's efficiency plot Figure 3.7 when only C_2's capacitance varied. When considering 20% variation of f_o, however, we should analyze K value of 0.833 to 1.25. Figure 3.10 shows that current of flying capacitor C_2 may vary between 1.1 to

1.27 and impacts the efficiency of RSCC. When K falls below 1, the RMS current of C_2 rises and increases conduction loss, therefore the overall system's efficiency drops. This efficiency hit on RSCC may or may not have higher effect on RSCC's derivation with multiple resonant tanks such as STC.

Although efficient, hunting for zero-current crossing, RSCC in its pure form sacrifices its component tolerance immunity. Figure 3.10 clearly shows when K value increases ($f_{sw} > f_o$), immunity towards component tolerance increases. Running RSCC at higher switching frequency than its resonant component will introduce non zero-current turn 'off' operation [22] and reshape the C_2's current to a single sided chopped sinusoidal waveform as shown in Figure 3.9. Eventually when K is too high the current will turn to triangular shape, hence K-plot will go up and converge to 1.15. This single sided chopped sine-wave method will provide the immunity tolerance, however it sacrifices its efficiency.

$$I_N = I_{C_{2_{RMS}}}/I_{out} \tag{3.17}$$

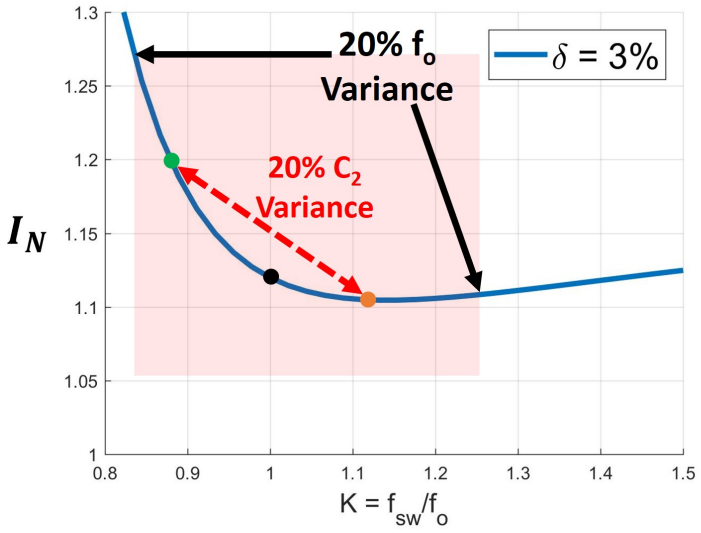


Figure 3.10: K-plot - Flying Capacitor RMS Current Vs. K (f_{sw}/f_o)

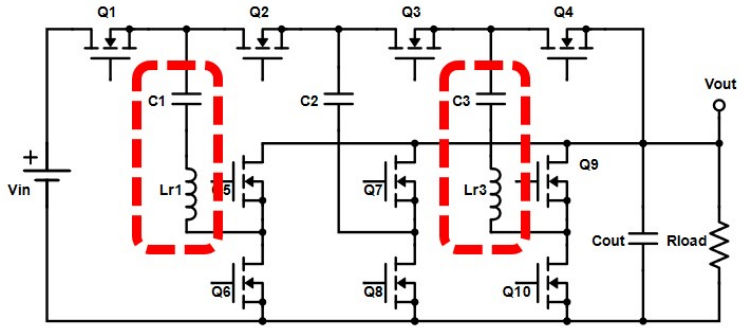


Figure 3.11: Dickson RSCC - 4 to 1 Switched-Tank Converter by [2]

Component variance issue present in RSCC is extendable to higher voltage conversion ratio of RSCC, such as STC by [2] and [25]. Based on similar reason of having lower output impedance, North Dakoda University and Google in [2] and [25] expands 2 to 1 RSCC to Dickson Switched Tank Converter (STC). Figure 3.11 shows the schematic of 4 to 1 STC proposed by [2].

$$C_1 = C_3 = C_x << C_2 \tag{3.18}$$

$$L_{r1} = L_{r3} = L_r \tag{3.19}$$

$$f_{sw} = f_o = \frac{1}{2\pi\sqrt{L_r C_x}} \tag{3.20}$$

Derived from 2 to 1 RSCC, STC uses the same principle operation, such as zero current operation, obtained by running its switching frequency exactly at its resonant frequency. Using conservation of energy equation 2.10 and 2.11, we can calculate that each tank only delivers half of its output current, hence the normalization factor for 4 to 1 STC, is half of its output current.

$$I_{N_{4to1STC}} = \frac{I_{C_{RMS}}}{I_{out}/2} \tag{3.21}$$

However, when it comes to high volume adoption, having two or more perfectly matching resonant tanks is impossible and therefore higher voltage conversion ratio RSCC, such as STC, will encounter component variance issue and may sacrifice its efficiency. Figure 3.12 shows simulation results when there is a missmatch between two resonant tank. Assuming C_3's branch obtains optimum operation, while 20% deviation exists on C_1's branch, it sacrifices the efficiency of C_1 resonant tank. The ideal case of C_3 achieves $0.55I_{out}$ of RMS current, meanwhile C_1's RMS goes higher to $0.635I_{out}$.

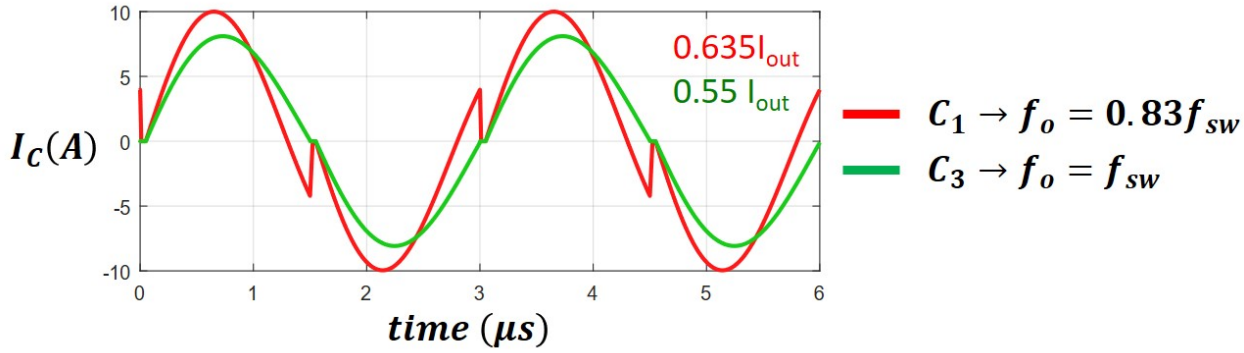
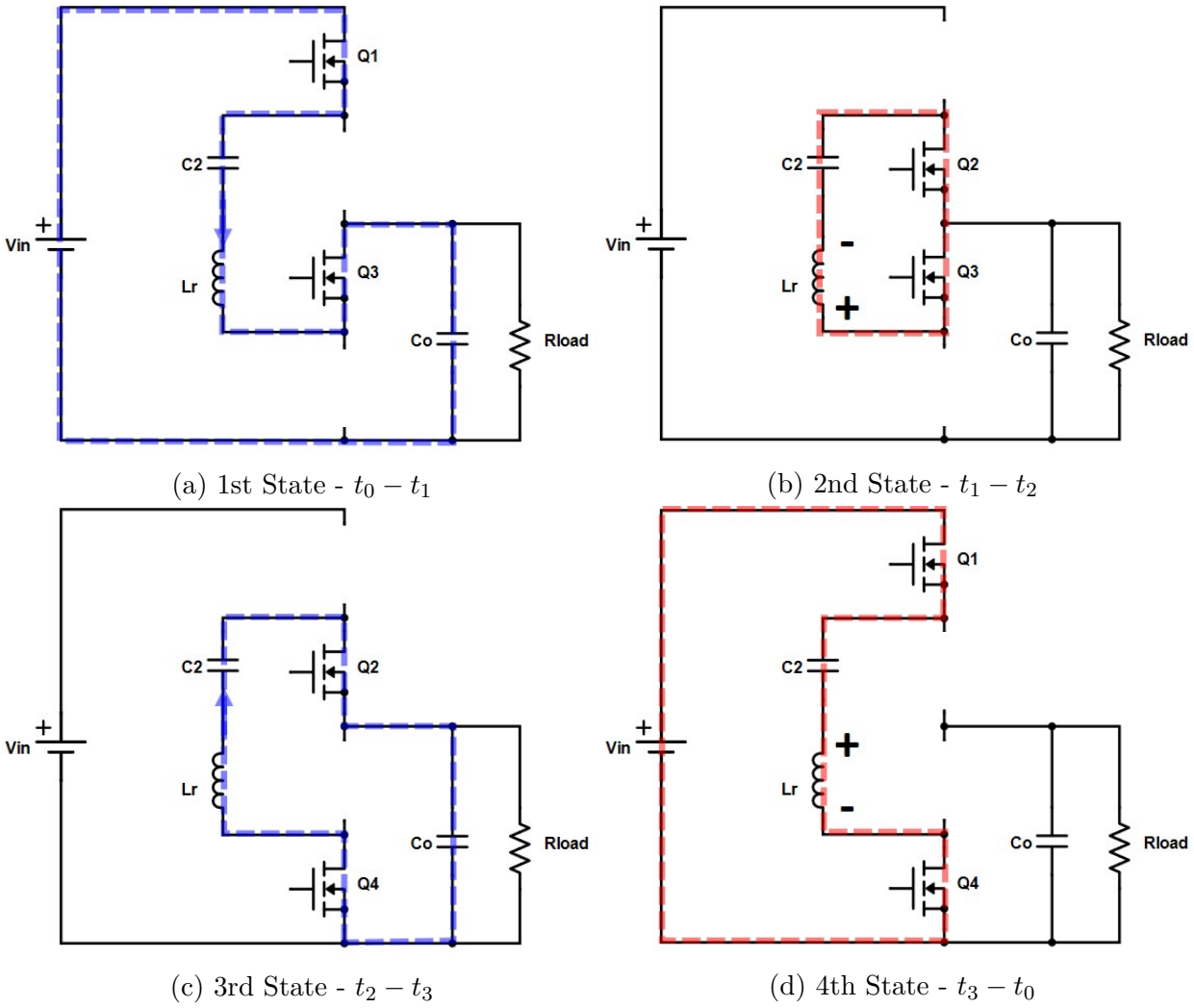


Figure 3.12: STC's capacitor current with Missmatched Resonant Tank

3.4 Phase-Shifted RSCC

Sano and Fujita in [27] propose another method utilizing RSCC structure to achieve both high efficiency operation and immunity towards component variation. Running switching frequency at its resonant frequency causes pure RSCC run into component variation problem, hence, they propose to have RSCC's switching frequency to be always higher than its resonant frequency.



(a) 1st State - $t_0 - t_1$

(b) 2nd State - $t_1 - t_2$

(c) 3rd State - $t_2 - t_3$

(d) 4th State - $t_3 - t_0$

Figure 3.13: Phase Shifted RSCC's Four Different States of Operation

$$f_{sw} > f_o = \frac{1}{2\pi\sqrt{L_r C_2}} \tag{3.22}$$

Phase-Shifted RSCC consists on two half-bridge inverters with four switching devices $Q_1 - Q_4$ and a series resonant circuit L_r and C_2 [27] similar to pure RSCC in [1]. With two half-bridge inverters, phase shifted RSCC has four different states of operation as shown in Figure 3.13 and Figure 3.14.

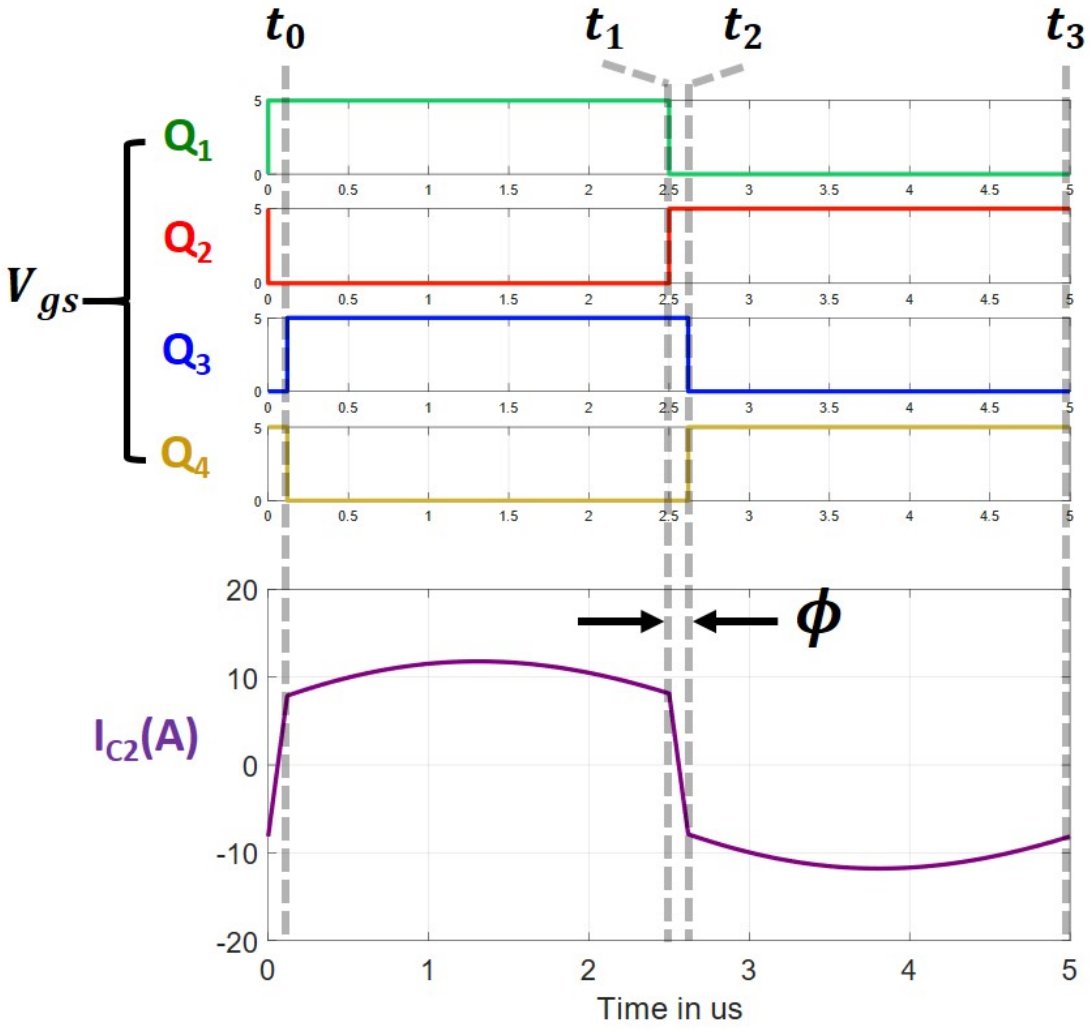


Figure 3.14: Phase-Shifted RSCC Operational Waveform

1st State - $t_0 - t_1$

In this state, input voltage delivers energy to the output through its main resonant tank. Due to the inductor L_r, phase shifted RSCC utilizes soft-charging between capacitors and eliminate current spike in conventional SCC making phase shifted RSCC achieves high efficiency operation. Due to switching higher than its resonant frequency, by the end of this state, there is a remaining energy left in the inductor in a form of a current.

2nd State - $t_1 - t_2$

In this state, Q_1 turns 'off' and Q_2 turns 'on' providing current loop for the inductor to free-wheel. In steady state, flying capacitor C_2 will be biased to half of its input voltage. Therefore, the resonant tank will be excited by half of input voltage during this state. The voltage of C_2 will reverse bias inductor L_r until the inductor current direction is reversed.

3rd State - $t_2 - t_3$

Once the inductor current reaches certain magnitude, Q_4 turns 'on' completing loop of energy conduction to the output. Since the inductor current is pre-charged from the previous state, the resonant tank doesn't need to be pre-charged from zero. Similar to the 1st state, there is a remaining energy left in the inductor in a form of a current.

4th State - $t_3 - t_0$

Due to the direction of the inductor current facing input voltage, Q_1 is then turned 'on' providing free-wheeling path. Similar to 2nd state, L_r is biased by half of input voltage until the inductor current direction is reversed facing its output.

In order to achieve high efficiency, phase shifted RSCC requires additional controller to reshape the flying capacitor C_2's current to a square-waveform. The controller requires the output voltage and current to determine difference in phase between the first (Q_1 and Q_2) and second (Q_3 and Q_4) half-bridges transition, hence its name, marked by ϕ in Figure 3.14.

As output current increases, the phase shift, ϕ, also has to increase. Unfortunately, during these transition states, 2nd and 4th, no energy is delivered to the output, hence, the longer the ϕ, the RMS of flying capacitor increases and effectively reduces efficiency.

Therefore, one has to minimize these transition states (or ϕ) to boost efficiency further. Using a first-order approximation, [27] shows the required phase-shift as shown in equation 3.23.

$$\phi = \frac{I_{out} Z_r T_{sw}}{V_{in} tan(\omega_o T_{sw}/4)} \tag{3.23}$$

where, Z_r is defined to be

$$Z_r = \sqrt{L_r/C_2} \tag{3.24}$$

Based on equation 3.23 and 3.24, one way to reduce ϕ is to reduce the impedance of the resonant tank it self by reducing the inductance of L_r. However, in order to keep the same resonant frequency, C_2 then has to be increased at the same time. Therefore, using such method will only increase the total size of solution in addition to complicated controller requirement.

In conclusion, using RSCC structure is not sufficient to achieve high efficiency operation due to couple reasons. First, pure RSCC is not ready for high volume adoption due to its low immunity towards component tolerance. Second, using phase-shifted RSCC may solve the component variation issues of RSCC structure, however, it has a trade-off between efficiency and total solution size. This conclude the analysis of Resonant Switched-Capacitor Converter.

Chapter 4

Multi Resonant Switched-Capacitor Converter

Based on the analysis in Chapter 3, Resonant Switched-Capacitor Converter (RSCC) has successfully reduced conduction loss of SCC using soft charging mechanism by adding a small inductor in series to its flying capacitor. RSCC further improves its efficiency by operating its switching frequency at its resonant and achieves zero current turn off (ZCS) mechanism. However, hunting zero current to achieve ZCS reduces RSCC's immunity towards component variation. This chapter introduces a novel RSCC with higher efficiency and immunity towards component variance by the mean of second resonant frequency, hence the name Multi-Resonant Switched-Capacitor Converter (MRSCC). In order to improve immunity towards component variation, MRSCC always operates its switching frequency higher than its resonant frequency.

4.1 MRSCC - Operation Principle

Figure 4.1 shows the basic cell of 2 to 1 MRSCC voltage divider. Derived from RSCC structure, a small capacitor, C_r, is inserted in parallel to the resonant inductor, L_r, forming second resonant tank at much higher frequency than its main resonant frequency, f_o which determined by L_r and C_2, hence C_r has to be much smaller than C_2. C_o is output filter

capacitor and is assumed very large. Two active switches, Q_1 and Q_2, are driven alternately with 50% duty cycle while Q_3 and Q_4 operate as synchronous rectifiers (SR) respectively to Q_1 and Q_2. MRSCC operates its switching freqency higher thant its main resonant frequency in order to increase immunity towards component tolerace.

$$C_r << C_2 \tag{4.1}$$

The switching frequency (f_{sw}), in the case of MRSCC, is always operated higher than its f_o to ensure immunity towards component variation, hence:

$$f_{sw} > f_o = \frac{1}{2\pi\sqrt{L_r C_2}} \tag{4.2}$$

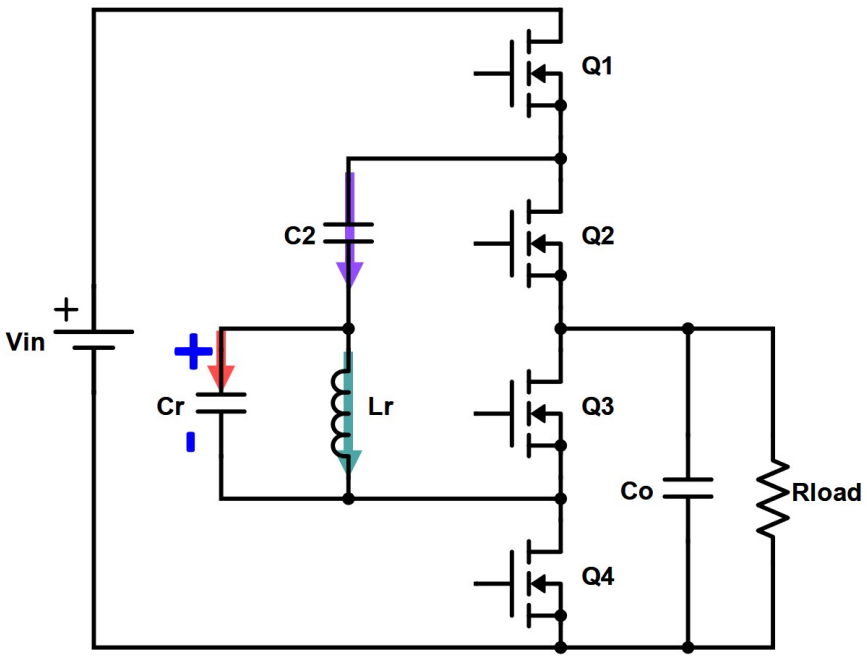


Figure 4.1: 2 to 1 Multi Resonant Switched-Capacitor Voltage Divider Basic Structure

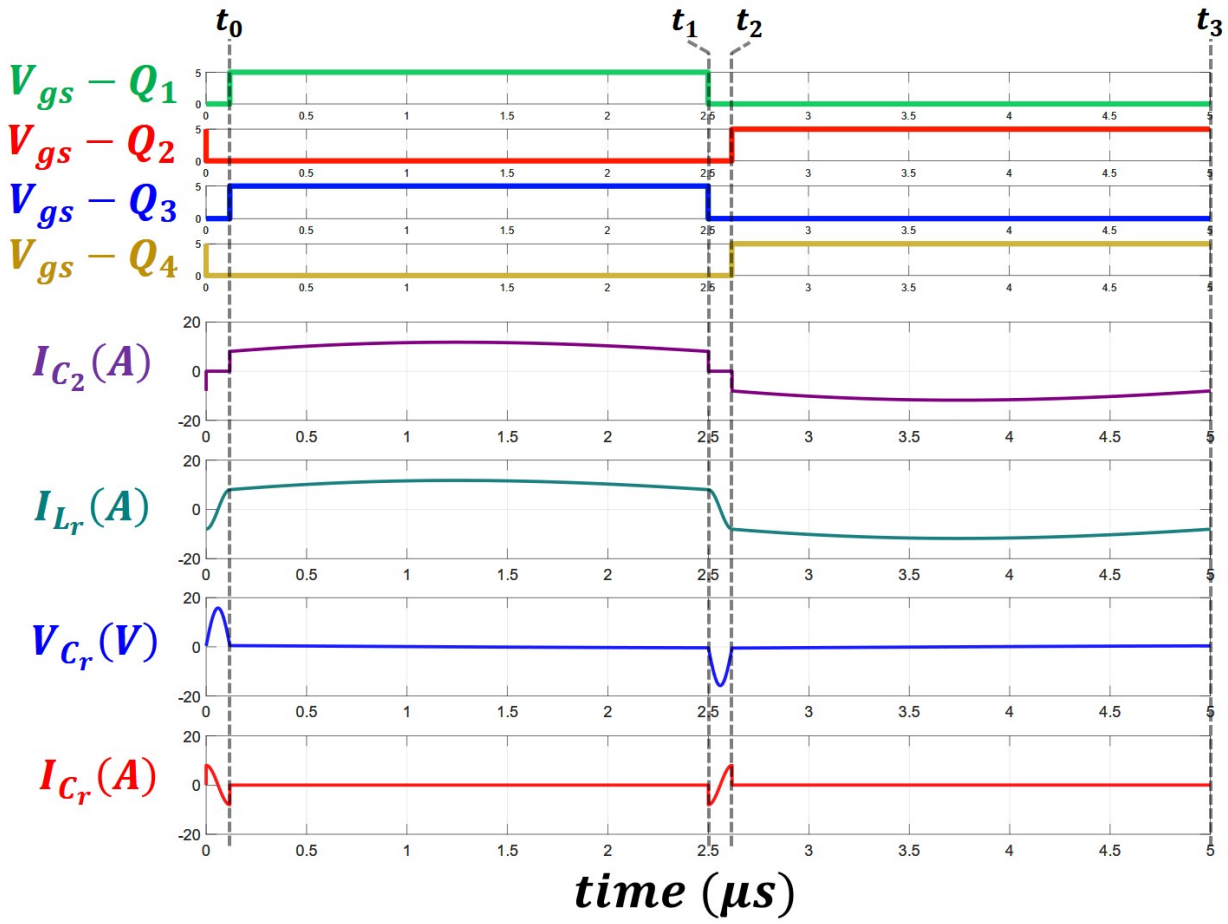
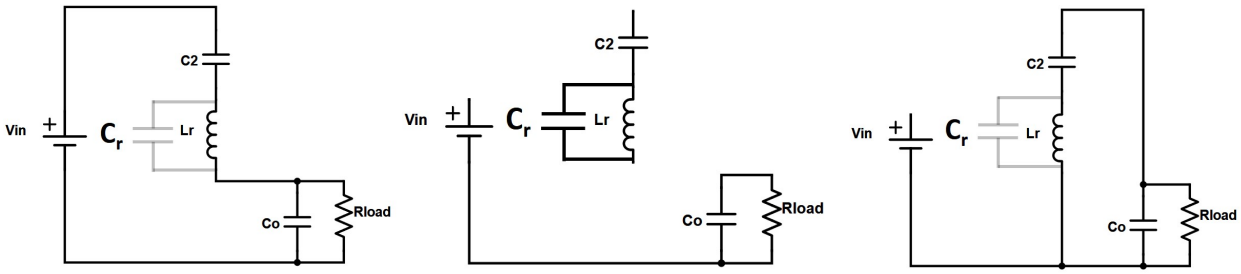


Figure 4.2: MRSCC - Principle Operation Waveform

Figure 4.2 shows the principle operation waveform of MRSCC. Although there are four different states of operation, two states share a common equivalent circuit.



(a) 1st State: t_0 to t_1 (b) 2nd State: t_1 to t_2 & t_3 to t_0 (c) 3rd State: t_2 to t_3

Figure 4.3: MRSCC Three States of Operation Equivalent Circuit

1. t_0 to t_1

The first state of MRSCC is marked by t_0 to t_1 in Figure 4.2 with equivalent circuit shown Figure 4.3a. During this state, Q_1 and Q_3 are 'on' allowing the input voltage to deliver energy to the outout through its main resonant tank. Although C_r exists in parallel to L_r, C_r is too small to affect the main resonant operation. Due to f_{sw} being higher than f_o, at the end of conduction time, t_1, L_r, left-over current in the inductor exists.

2. t_1 to t_2

The second state or transition state of MRSCC is marked by t_1 to t_2 in Figure 4.2 with equivalent circuit shown in Figure 4.3b. During this state, all switches are 'off' isolating the resonant tank from both the input and output. With the current loop disconnected, flying capacitor C_2 is also isolated from the resonant inductor L_r, hence after t_1, the C_2's current drops to zero instantaneously. C_r in parallel to L_r provides path for the left-over inductor current from the previous state to continue flowing for half L_rC_r resonant period. Essentially, this state reverses the inductor current direction in lossless manner. Duration of this transition state is solely determined by L_r and C_r.

$$(t_1 \rightarrow t_2) = t_d = \pi\sqrt{L_rC_r} \tag{4.3}$$

3. t_2 to t_3

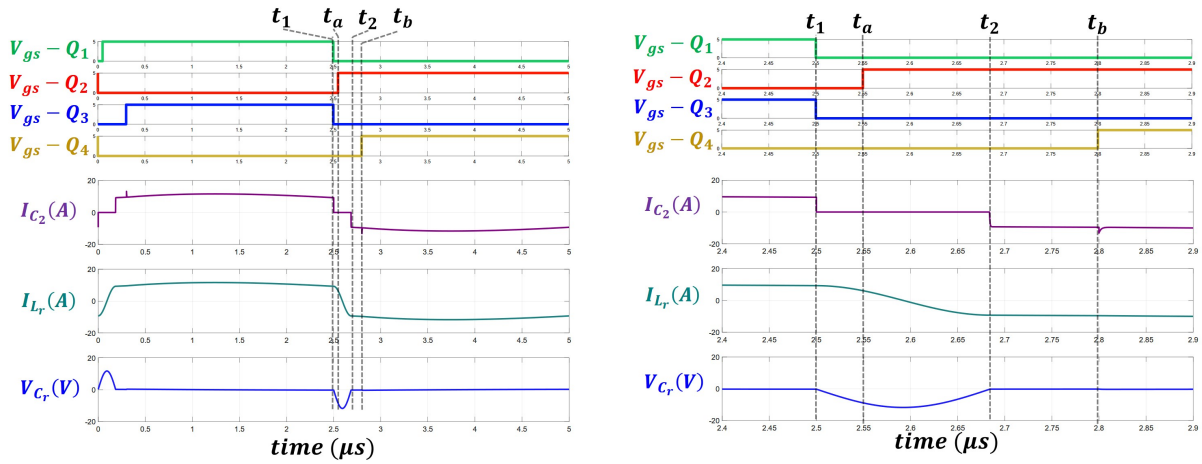
The third state of MRSCC is marked by t_2 to t_3 in Figure 4.2 with equivalent circuit shown in Figure 4.3c. During this state, Q_2 and Q_4 are on connecting the resonant tank in parallel to the output. By doing so, the tank releases energy stored in its flying capacitor C_2 through the series inductor achieving soft-charging mechanism between capacitors.

4. t_3 to t_0

The fourth state of MRSCC is marked by t_3 to t_4 in Figure 4.2 and also represents transition state. This state of operation has the same equivalent circuit as the second state as shown in Figure 4.3b. All the switches are off and isolate the resonant tank from the input and output to reverse the inductor current.

Improved Gate Driving

Driving MRSCC at such manner will provide immunity towards main resonant tank component tolerance, however it can create immunity problem in regards of the additional high frequency resonant tank component variation. In order to solve this issue, MRSCC has to be driven in a manner shown in Figure 4.4b. The improved gate driving turns off both active switches and their corresponding SRs at the same time. However, the adjustment is made during the turn on instant. The active switches, $Q_{1 \text{ and } 2}$, may be turned during transition state (2nd and 4th) shown by marker t_a, while the SR switched ($Q_{3 \text{ and } 4}$) may be turned on after the half resonant period (t_d or $t_1 \rightarrow t_2$) is over, marked by t_b.



(a) Steady State Operation

(b) Zoomed in Gate Driving

Figure 4.4: MRSCC - Improved Gate Driving Sequence

At t_a instant, the active switch Q_2 turns on, however, the resonant tank is still isolated from the input and output due to C_r's voltage. During this transition state, voltage of C_r reverse biases SRs' body diode preventing current loop to complete. Once half resonant period of L_rC_r is completed, the corresponding SR's body diode will automatically conduct and hold V_{Cr} at zero. After t_2 instant, SR can be turned on anytime without timing restriction providing immunity towards the additional resonant component variation.

2nd Configuration of MRSCC

Considering parasitic inductance in series to flying capacitor, C_2, in MRSCC's 1st configuration shown in Figure 4.1, during its dead-time t_d, the parasitic inductance will introduce the third high resonant frequency. This high frequency may introduce additional RMS loss. However, we can minimize this effect by reducing the operating switching frequency.

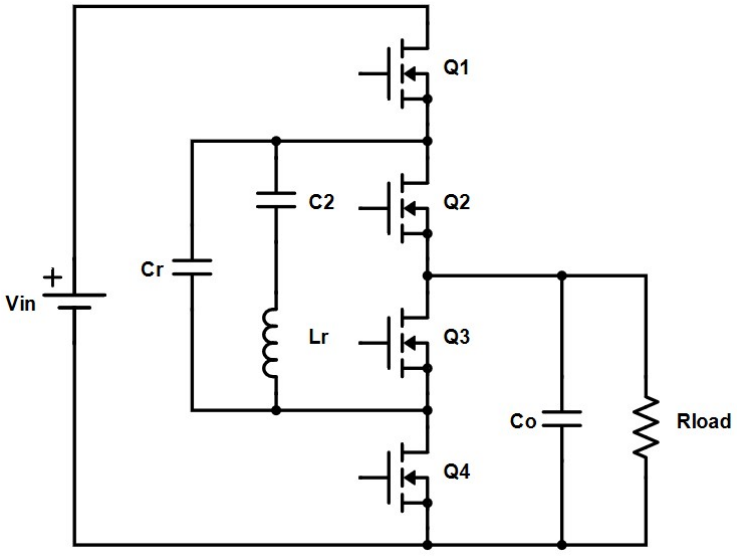


Figure 4.5: 2nd MRSCC's Configuration

Figure 4.5 shows the second configuration of MRSCC. In this case, C_r is in parallel to the main resonant tank, instead of in parallel to only L_r. By doing so, parasitic inductance

along C_2 will be in series to L_r and C_r during dead-time (t_d), hence it eliminates the additional high resonant frequency. However, adding C_r in parallel to the main resonant tank will introduce DC bias voltage to C_r. Hence, we have to consider using Class I capacitor to ensure stable dead-time for all range of operation.

4.2 Loss Analysis of MRSCC

4.2.1 Conduction Loss

Similar to RSCC, conduction loss of MRSCC is determined by flying capacitor's current, hence in this subsection, we focus the analysis on deriving time domain solution of MRSCC's flying capacitor's current.

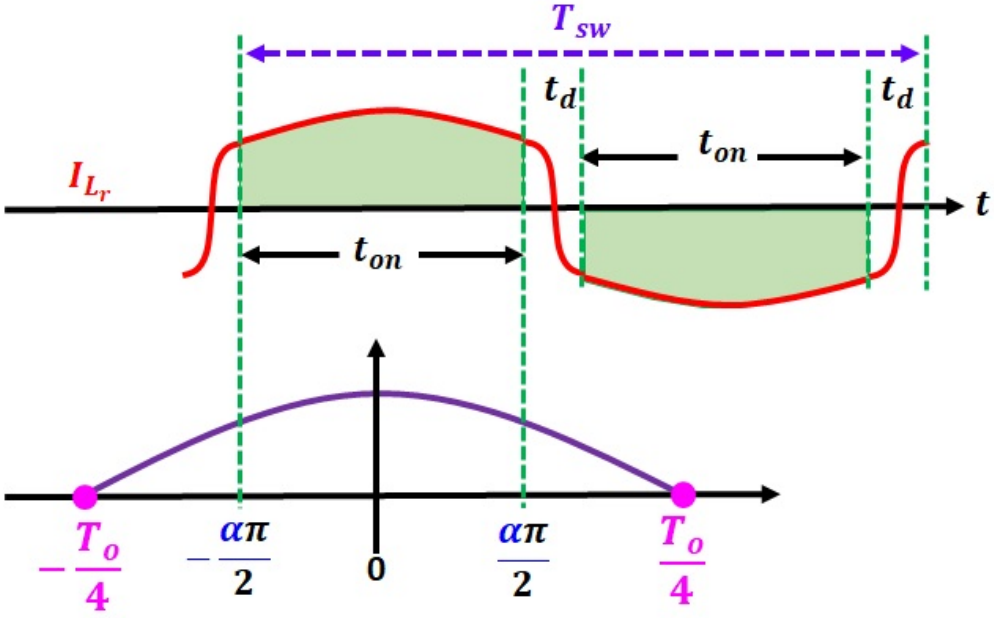


Figure 4.6: MRSCC - Flying Capacitor's Current Waveform Modeling

By applying MRSCC technique, we utilize the center portion of half sinusoidal wave-

form of main resonant period as shown in Figure 4.6, therefore we can model MRSCC's $i_{C_2}(t)$ using cosine. We define,

$$T_{sw} = 2t_{on} + 2t_d \tag{4.4}$$

$$\alpha = t_{on}/(T_o/2) \tag{4.5}$$

$$\delta = t_d/T_{sw} \tag{4.6}$$

With these definitions, then we can model $i_{C_2}(t)$ to be:

$$i_{C_2}(t) = \begin{cases} I_{pk}cos(t), -\alpha\pi/2 \leq \alpha\pi/2 \\ 0, \alpha\pi/2 < (T_{sw}/T_o)\pi \end{cases} \tag{4.7}$$

Using conservation of energy equation 2.10 and 2.11, we obtain I_{pk} to be

$$I_{pk} = \frac{(f_o/f_{sw})\pi/2}{sin[(1-2\delta)(f_o/f_{sw})\pi/2]} I_{out} \tag{4.8}$$

With time domain solution of flying capacitor's current is solved, we can then calculate the RMS of devices conduction current as:

$$I_{Q_{RMS}} = I_{C_{2_{RMS}}}/\sqrt{2} \tag{4.9}$$

Assuming same devices for all switches, we can simplify the conduction loss to be:

$$P_{cond} = 4(I_{Q_{RMS}})^2 R_{ds} = 2I^2_{C_{2_{RMS}}} R_{ds} \tag{4.10}$$

4.2.2 Switching Related Loss

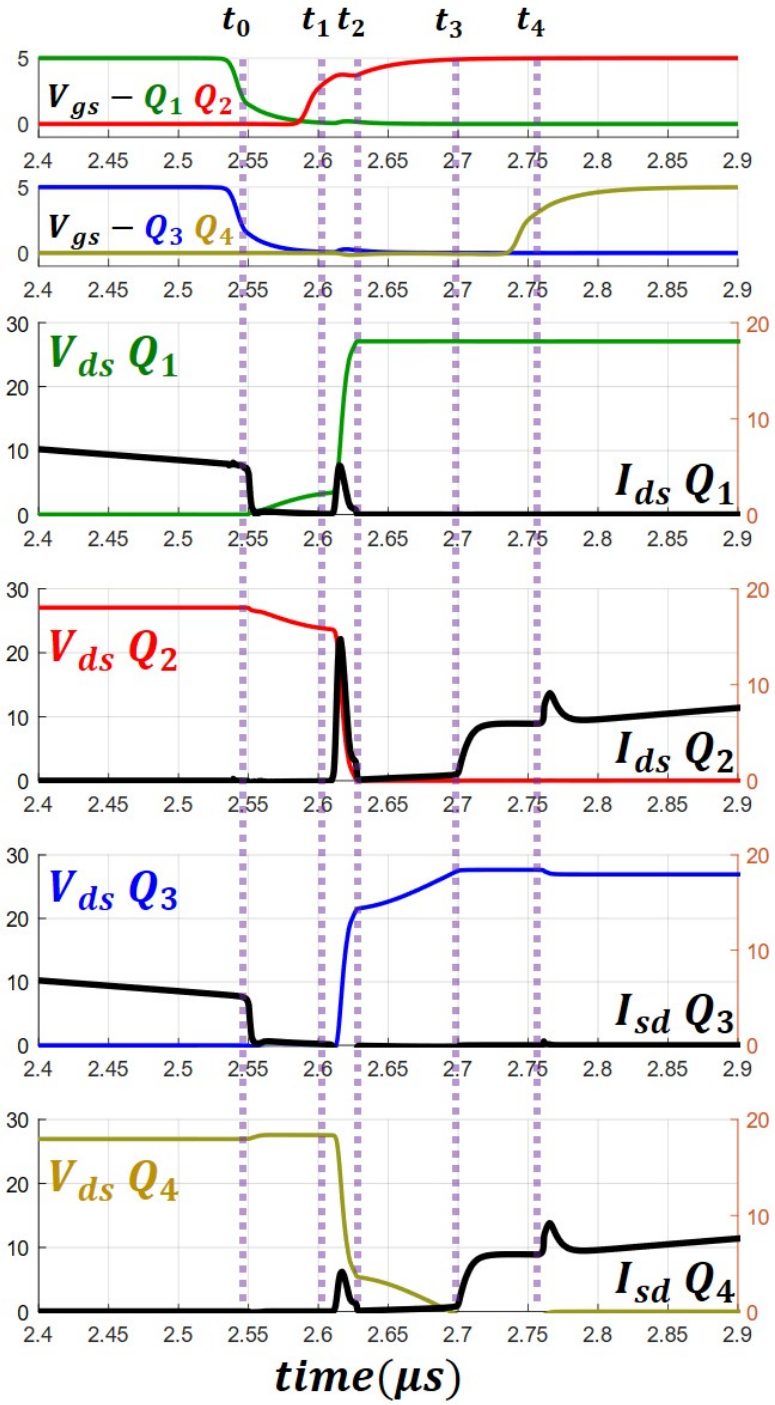


Figure 4.7: MRSCC Switching Transition Waveform

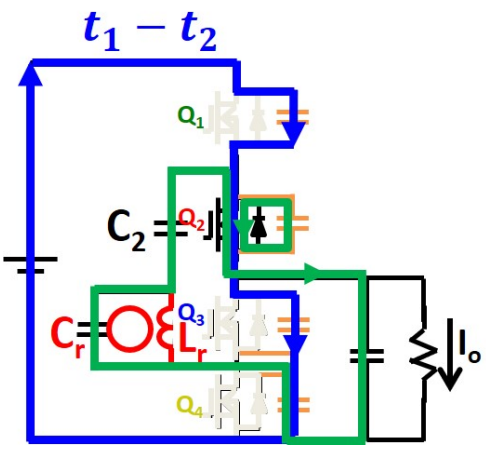


Figure 4.8: MRSCC Q_2 turn on Mechanism

Figure 4.7 shows the complete simulation of MRSCC during its transition between states ($Q_{1,3}$ turn off and $Q_{2,4}$ turn on). At t_0, gate voltages of Q_1 and Q_3 go to zero, current in the channels decreases to zero. Due to C_r's location of being paralleled to L_r, the residue current is not able to charge or discharge devices' Q_{oss}, keeping devices' drain to source voltage (V_{ds}) remain unchanged. By doing so, the improved gate driving sequence eliminates the conventional voltage and current overlap transition loss.

Between t_1 and t_2, Q_2's gate voltage hits its threshold voltage of v_{th} and impedance in its channel depletes quickly to its R_{ds} at the same it discharges its own Coss. Current from input rushes in through Q_1 and Q_3's Coss, while charging them at the same time. Due to Kirchoff's voltage law, Q_{oss} of Q_4 discharges through the least impedance path to the output.

Between t_2 and t_3, L_r is completing its half cycle resonant with C_r. Once it is over, the body diode of Q_4 starts to conduct completing current loop and delivering energy to the output, described by phase t_3 to t_4. At t_4, the gate voltage of Q_4 turns on to reduce the conduction loss of SR and achieve zero voltage switching. Hence, all devices of MRSCC eliminates conventional transition loss, however Q_{oss} charging and discharging loss, as SCC and RSCC, still persists.

4.3 MRSCC Component Variance Immunity

Using flying capacitor's current model derived in Conduction Loss model, we obtain normalized RMS of the rectified current of C_2.

$$I_N = \frac{I_{C2}RMS}{I_{out}} = \sqrt{\frac{[\frac{\pi}{K}(1-2\delta) + sin(\frac{\pi}{K}(1-2\delta))]\pi/K}{8sin^2[(1-2\delta)\frac{\pi}{2K}]}} \tag{4.11}$$

$$K = f_{sw}/f_o \tag{4.12}$$

$$\delta = t_d/T_{sw} \tag{4.13}$$

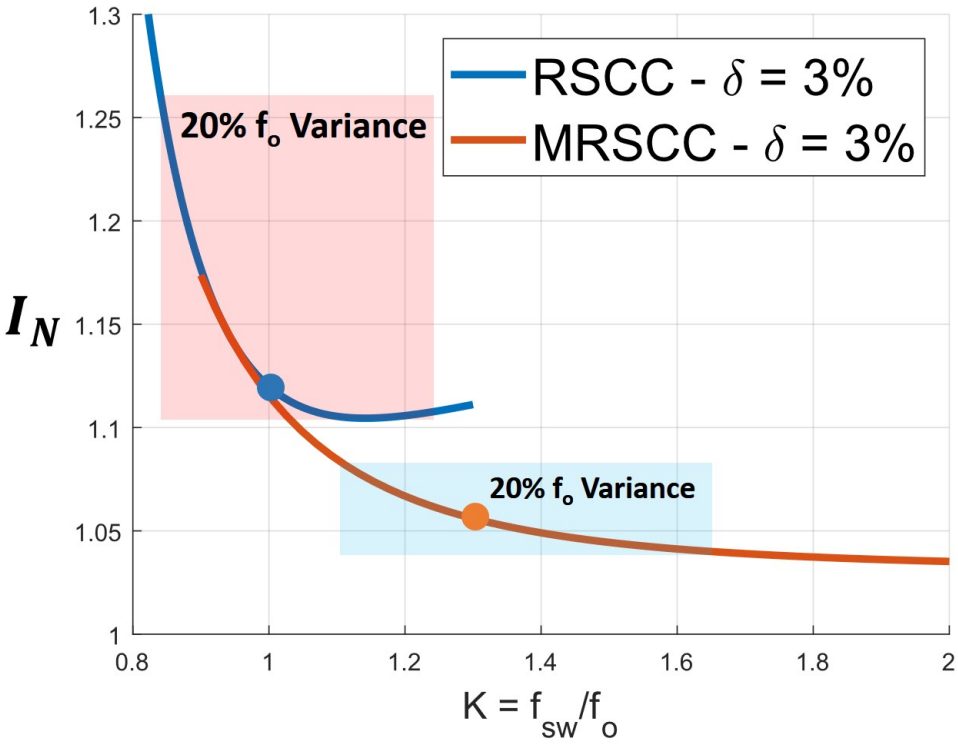


Figure 4.9: KPlot - MRSCC's Flying Capacitor RMS Current Vs. K(f_{sw}/f_o)

Based on equation 4.11, normalized RMS of C_2's current is plotted in Figure 4.9 and compared to RSCC's. Assuming 20% variance of main resonant tank's frequency of f_o, MRSCC outperforms RSCC in term of change in C_2's current and its magnitude. This shows the immunity of MRSCC towards component change and variation.

From 2 to 1 RSCC hardware designed in Section 3, we modified the operating point of K to 1.2 in order to ensure immunity towards capacitance variance by adding C_r of 47nF and moving the f_{sw} to 300kHz as shown in Table 4.1. By keeping the exact essential energy transfer components such as C_2, L_r, C_o, printed circuit boards (PCB) and transistor devices, we are able to provide objective insight of MRSCC's improvement and a fair apple to apple comparison.

Figure 4.10 shows the drain to source voltage of Q_4 and its resonant inductor, L_r's current. When the switching is set to be higher than its resonant frequency, the I_{L_r} changes to be closer to a square-waveform. Figure 4.11 shows illustrates how component variation on flying capacitor affects MRSCC. When C_2 is smaller than intended, the I_{L_r} becomes closer to sine wave, however it still maintains low RMS current, while when C_2 is higher 20%, I_{L_r} becomes closer to square wave.

Table 4.1: Gen I: 2 to 1 MRSCC Hardware

	MRSCC
C_2	5.4uF U2J
L_r	75nH
C_o	160uF
C_r	47nF X7R
F_{sw}	300kHz

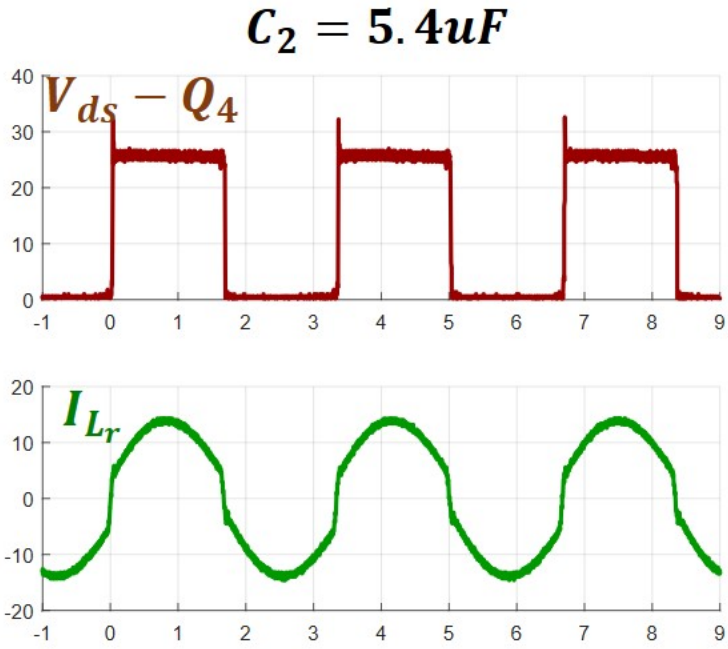
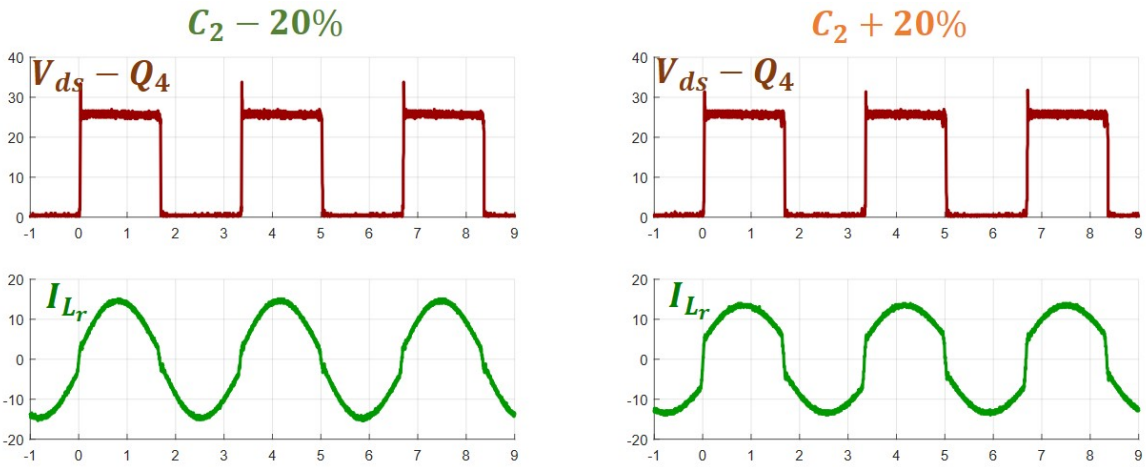


Figure 4.10: MRSCC - Scope Capture of V_{ds} of Q4 and Resonant Inductor L_r's current



(a) C_2 - 20% (b) C_2 + 20%

Figure 4.11: MRSCC - Scope Capture of V_{ds} of Q4 and Resonant Inductor L_r's current with Variation on its flying capacitor

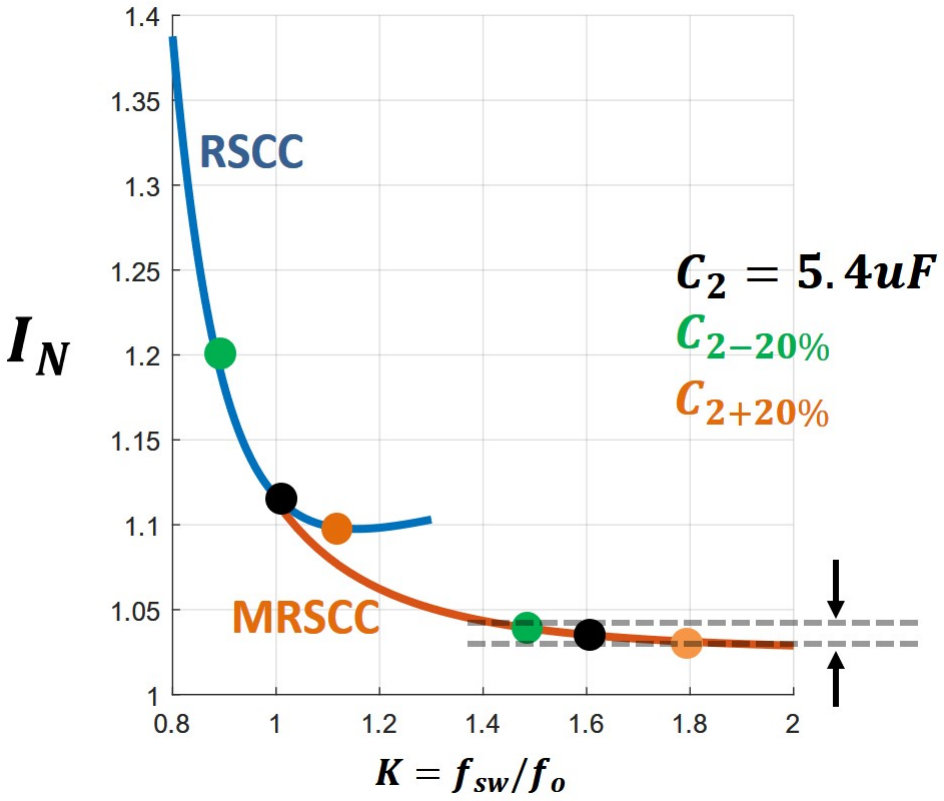
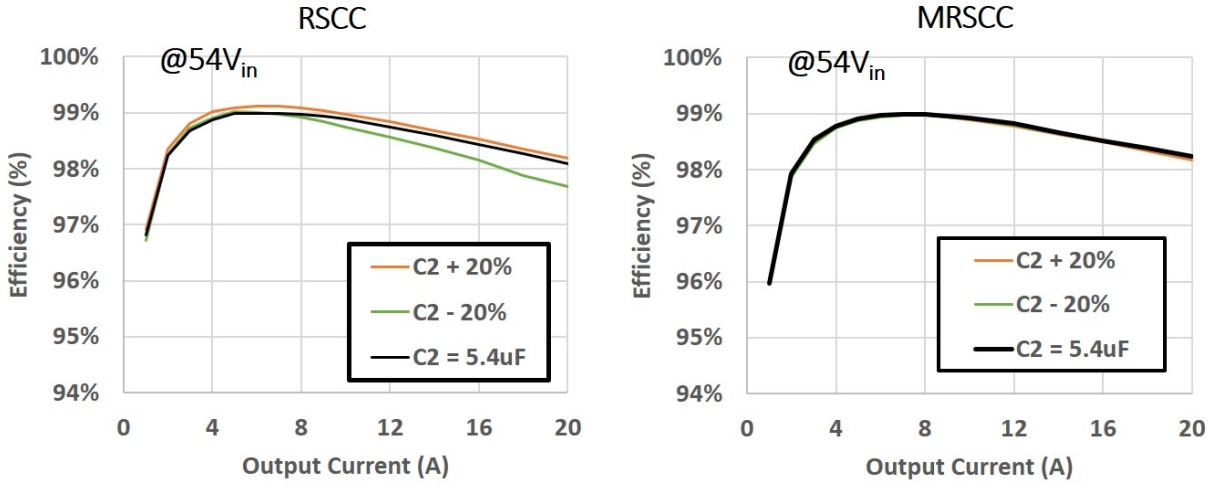


Figure 4.12: KPlot MRSCC vs. RSCC +/-20% C_2



(a) RSCC

(b) MRSCC

Figure 4.13: Efficiency Measurement +/-20% C_2

Based on Figure 4.12 , MRSCC has high immunity towards C_2 variation due to minuscule change in flying capacitor's RMS current. This analysis result correlates to hardware scope capture and efficiency measurement of 2 to 1 MRSCC voltage divider verification hardware shown in Figure and 4.11 and 4.13. When varied by 20%, the efficiency of MRSCC do not vary. This result shows that MRSCC successfully isolates the change in f_o of primary resonant tank from its efficiency. In addition to immunity towards component variance, MRSCC achieves higher efficiency at heavy load in comparison to RSCC's.

As discussed previously in Chapter 3, although capacitance drops over DC bias, Class II capacitors, such as X7R, are appealing due to the fact that they are cheaper in price and have higher capacitance over volume in comparison to their Class I counterpart. Equipped with higher immunity towards component variation, MRSCC allows designers to utilize Class II capacitors to achieve higher peak efficiency while occupying the same volume. Table 4.2 shows the Gen II verification hardware of 2 to 1 MRSCC voltage divider. Notice that the price lowers by $5 for each system built. Hence, using X7R may reduce the production price in addition to higher peak efficiency.

Table 4.2: Gen I Vs. Gen II: 2 to 1 MRSCC Hardware

	MRSCC - Gen I	MRSCC - Gen II
C_2	5.4μF U2J	75μF X7R
L_r	75nH	75nH
C_o	160μF	160μF
C_r	47nF X7R	47nF X7R
F_{sw}	300kHz	200kHz
C_2 Price	$10	$5

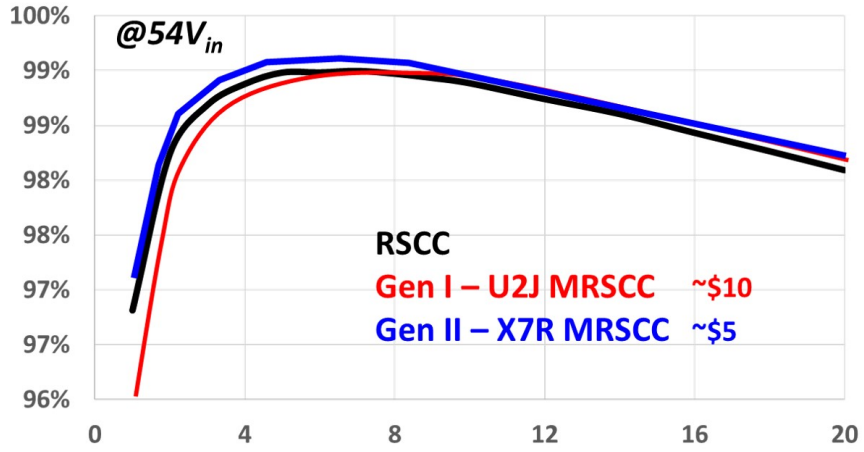


Figure 4.14: Gen II 2 to 1 MRSCC Voltage Divider Efficiency Measurement using Class II Capacitors

Figure 4.14 shows the efficiency of Gen II 2 to 1 MRSCC voltage divider using X7R for its flying capacitor of C_2. Comparing the performance of Gen II, it outperforms both RSCC and Gen I MRSCC using Class I capacitors, U2J. In addition to lowering the price by \$5, Gen II MRSCC achieves higher peak efficiency than the other two.

4.4 High Voltage Conversion Ratio MRSCC

Multi Resonant Concept discussed above is also applicable to higher voltage conversion ratio SCC voltage divider, such as Dickson Star discussed in Section 2. The main component are additional one resonant inductor and capacitor as shown in Figure 4.15

By applying MRSCC on Dickson SCC, it is not necessary to match the two resonant frequencies exactly, as long as the switching frequency, f_{sw}, is set to be higher than both resonant tanks' frequencies (f_o). Dickson MRSCC has the same design equations as 2 to 1 MRSCC voltage divider.

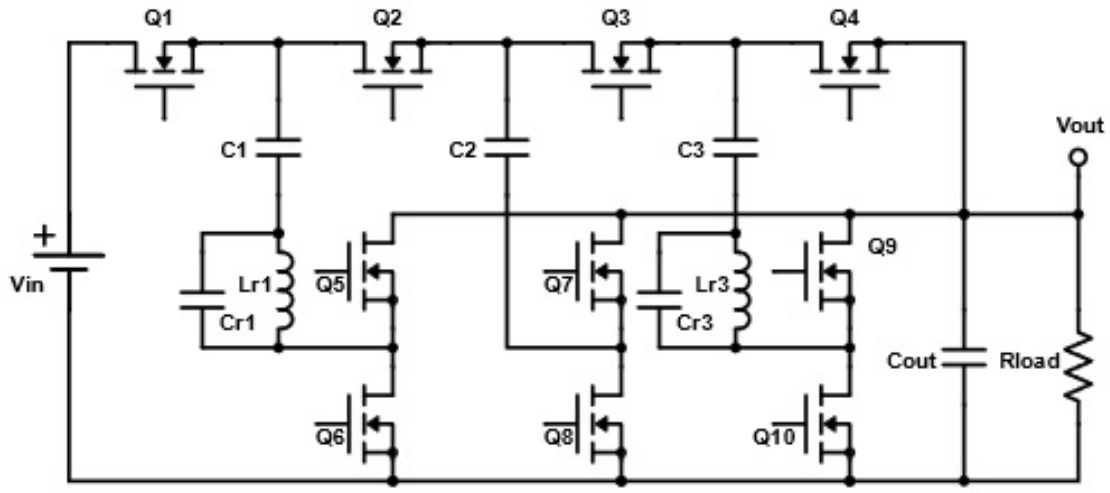


Figure 4.15: 4 to 1 Dickson MRSCC Voltage Divider

$$f_{sw} > f_o \tag{4.14}$$

In order to simplify the design, C_1 should have the same value of capacitance as C_3. Hence,

$$C_1 = C_3 = C_x \ll C_2 \tag{4.15}$$

$$L_{r1} = L_{r3} - L_r \tag{4.16}$$

$$f_o = \frac{1}{2\pi\sqrt{L_r C_x}} \tag{4.17}$$

$$t_d = \pi\sqrt{L_r C_r} \tag{4.18}$$

Using conservation of energy equation 2.10, we obtain that the average of the flying capacitor's current is half of its output current, hence it is to be noted that the normalization factor is not longer I_{out} but $0.5I_{put}$.

When designing MRSCC, it is critical to choose K value in order to avoid tolerance issues due to components variation. K value is determined by the worst case variance of components used in the design. In this paper, we consider 20% variance from L_r and C_x. With 20% variation of resonant inductor and capacitor, we have to consider 20% variance of resonant period, T_o

$$K = f_{sw}/f_o = f_{sw}T_o \tag{4.19}$$

Based on equation 4.19, 20% variation of T_o induces 20% variance of K value. MRSCC needs to avoid K value to drop below 1, hence the optimum design point of K is 1.3 shown in Figure 4.9. Assuming switching frequency of 200kHz, we can then determine the dead time, t_d and resonant frequency values as shown in Parameter Table 4.3.

Table 4.3: 4 to 1 MRSCC Design Parameter

	MRSCC
f_{sw}	200kHz
K	1.3
f_o	150kHz
t_d	150ns

In this design, we use 50nH inductor in the resonant tank. Hence, we can calculate C_x and C_r using equation 4.20 and 4.18 respectively.

$$C_x = (\frac{1}{2\pi f_o})^2/L_r \tag{4.20}$$

Table 4.4: Component of 4 to 1 MRSCC Design

C_1	80 μF	8x10μF 50V X7R
C_2	264 μF	12x22μF 50V X7R
C_3	56.4 μF	12x4.7μF 50V X7R
L_r	50 nH	PA5013, +/-4nH, Pulse
C_r	47nF	50V X7R
$Q_{1\text{-}4}$	BSZ025N04LS	40V, 2.5mΩ
$Q_{5\text{-}10}$	BSZ013NE2LS5I	25V, 1.3mΩ

Table 4.4 shows the components used in the 4 to 1 MRSCC Dickson design. Based on the calculation, C_1 and C_3 are 22μF. However, Table 4.4 shows higher capacitance for C_1 and C_3. These values of capacitances increases when we have to include the DC bias effect on dielectric materials of Class II capacitors. For example, when 45 V is applied on a 50V X7R ceramic capacitor, only 30% of effective capacitance left. While C_3 will have less DC bias (15V), hence it needs lower initial capacitance. Keep in mind that the worst case condition in this design is based on 60V input voltage for server rack application.

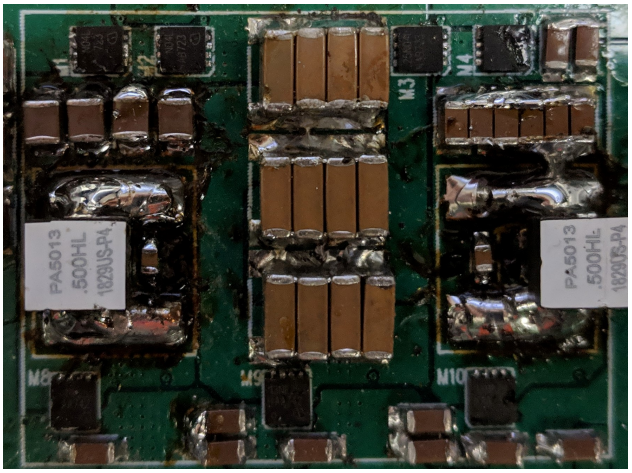
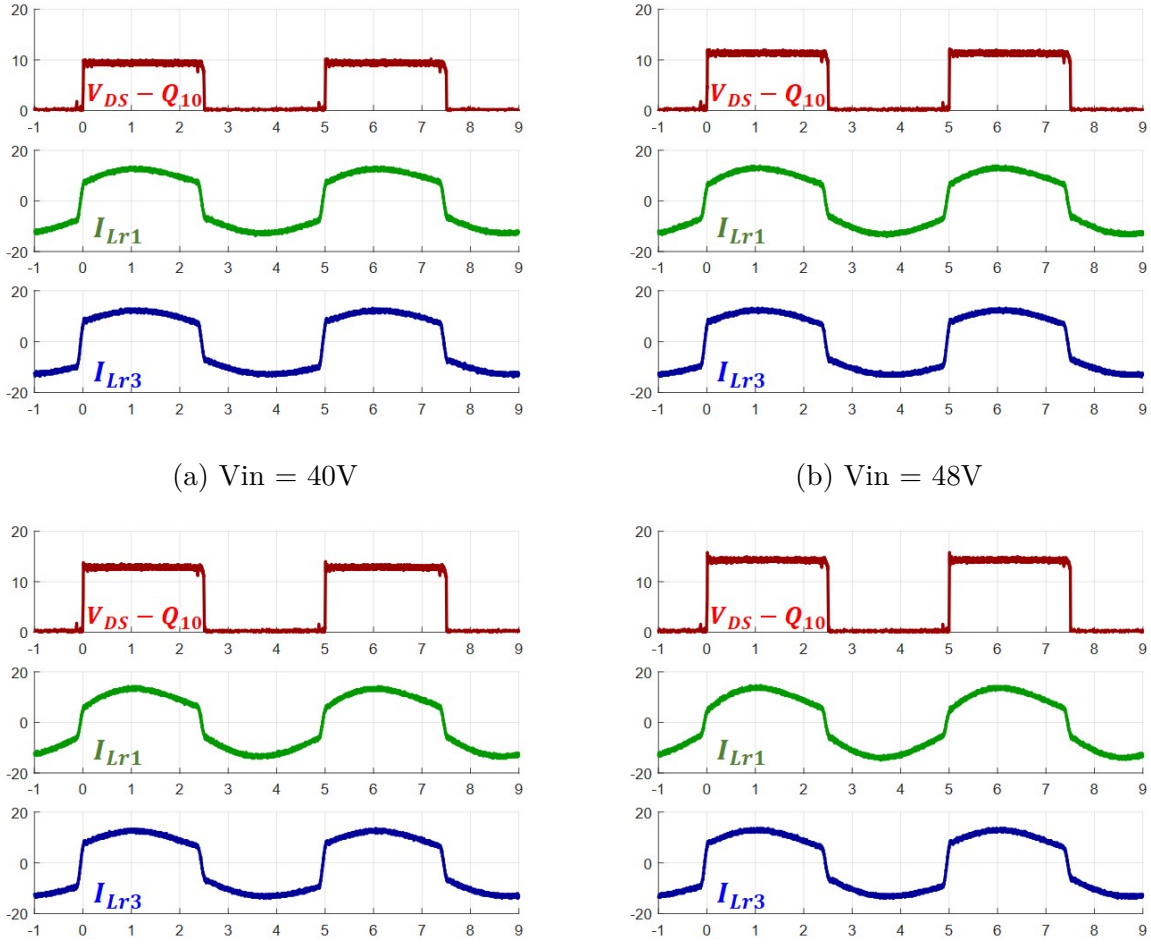


Figure 4.16: 4 to 1 Dickson MRSCC Hardware

Using the component and design parameters in Table 4.3 and 4.4, a PCB is designed and populated as shown in Figure 4.16. Figure 4.17 shows the two resonant inductor current of 4 to 1 MRSCC, which shows square wave like waveform.



(a) Vin = 40V

(b) Vin = 48V

(c) Vin = 54V

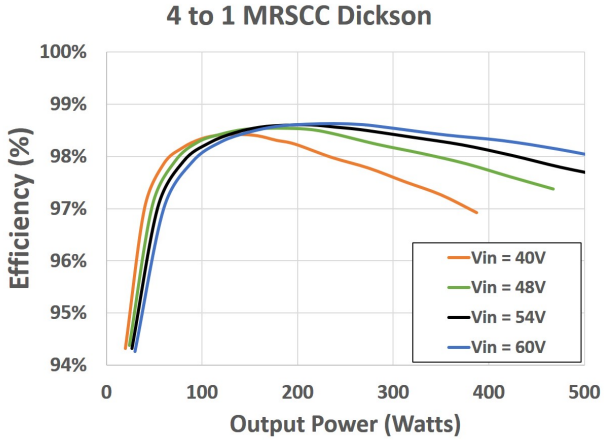
(d) Vin = 60V

Figure 4.17: 4 to 1 Dickson MRSCC Scope Capture $L_{r1 \text{ and } r3}$'s Current

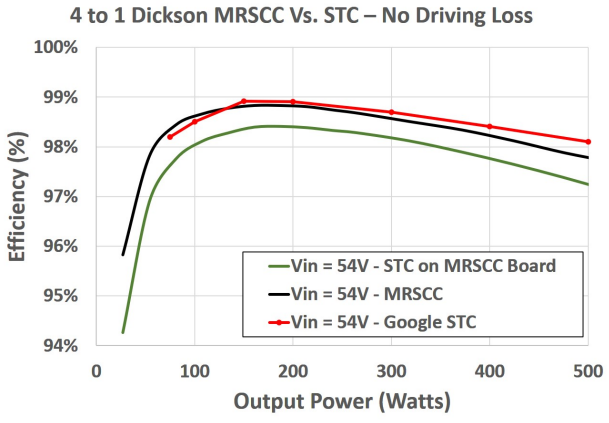
Figure 4.18a shows 4 to 1 Dickson MRSCC Efficiency measurement across load and input voltage. MRSCC achieves 98.63% of peak efficiency, a tad higher than RSCC based Dickson voltage divider, Switched Tank Converter (STC) in [2]. In order to present more objective view, this paper provides STC and MRSCC comparison using the same board hence

it isolates extra losses from PCB design such as extra resistance within traces. Figure 4.18b shows MRSCC achieves higher efficiency across load over RSCC. However, both MRSCC and STC built in the same board don't perform higher efficiency than Google STC's efficiency in [2] at heavy load. This shows PCB design in Switched-Capacitor circuits is very critical when implemented in high current applications. In 4 to 1 MRSCC Dickson, for example, when the output load is 20A, the current in flying capacitors are over 20A AC peak to peak each as shown in Figure 4.17. This high of magnitude AC current introduces extra ac losses in the PCB.

In addition, Figure 4.17 illustrates the capability of MRSCC in utilizing Class-II capacitors such as X7R as its flying capacitors. Comparing the waveform for 40V vs. 60V input voltage, C_1 (in series to L_{r1}) flying capacitor will have 15V change in DC bias voltage, while C_3 (in series to L_{r3}) flying capacitor only sees 5V change in DC bias. As the input voltage increases, the resonant frequency of C_1 and L_{r1} also increases due to change in DC bias voltage. However, when designed properly, MRSCC can handle the change and still perform efficiently.



(a) Over Input Voltage



(b) MRSCC Vs. STC

Figure 4.18: MRSCC 4 to 1 Voltage Divider - Verification Hardware Efficiency Measurement

Based on the analysis, MRSCC outperforms both RSCC and conventional SCC. High immunity towards component variation allows MRSCC to utilize Class II capacitors to reduce the production costs while maintaining power density and efficiency. These benefits make MRSCC and its derivation suitable for high volume adoption. This concludes the analysis and comparison of Multi Resonant Switched-Capacitor Voltage Divider.

Chapter 5

Conclusions and Future Work

This thesis tackles two major challenges in the switched-capacitor based first stage of two stages VRM design: achieving high efficiency and immunity towards component variation. Three different switched-capacitor topologies are studied for this purpose.

5.1 Switched-Capacitor Circuit as Intermediate Bus Converter

Using the concept of 'devide and conquer' proposed by [15], Switched-Capacitor Converter (SCC) becomes a feasible solution as intermediate bus converter (IBC) in IBA architecture due to its high efficiency and density operation. The optimization model available is not suitable for high voltage conversion ratio (VCR) and high current application such as server rack voltage regulator modules (VRMs) based on 48V bus architecture.

This thesis provides the new optimization method for higher VCR SCC for server rack VRM applications. Verification hardware is built and matches the calculated efficiency. However, due to the fact conventional SCC using hard-charging mechanism between capacitors, it requires a large number of capacitors in order to achieve high efficiency operation, therefore it lowers power density of high VCR SCC.

This thesis also explored the proposed Resonant Switched-Capacitor (RSCC) by [1] of

using a small inductor in series to SCC's flying capacitor to create a resonant network. This resonant network introduces soft-charging mechanism between capacitors. By switching at its resonant frequency, RSCC achieves zero current turn off mechanism and achieve very high efficiency. However, due to the fact that RSCC hunts for zero current before it turns off its switches, component variation issues surfaces. It requires stable resonant frequency to achieve optimum operation. When it comes to high volume adoption, one has to anticipate the part to part variation, hence it requires additional controller to ensure high efficiency operation and drives the production price higher.

5.2 Analysis and Comparison on Proposed Multi-Resonant Switched-Capacitor

The two explored SCC imposes extra challenges in designing IBC. However, using similar concept of soft-charging mechanism, switched-capacitor based circuit is still a feasible solution.

In this thesis, i introduce Multi-Resonant Switched-Capacitor (MRSCC) voltage divider. MRSCC utilizes soft-charging mechanism from RSCC, however by operating its switching frequency higher than its resonant frequency, MRSCC achieves high immunity towards component variation. Theoretically, MRSCC achieves higher efficiency than MRSCC. Due to the fact that it has higher immunity towards component variation, MRSCC doesn't require extra controller to ensure proper operation. MRSCC also allows the utilization of Class II capacitors to reduce production cost. Therefore, MRSCC and its derivation are fit for high volume adoption.

5.3 Future Work

There are still some remaining works to be done which are related to this thesis. Based on the fact that switched-capacitor based circuit has high peak to peak AC current, it introduces additional AC losses in the PCB and reduces the efficiency of the whole system. Detailed analysis of MRSCC in this thesis does not include the PCB loss analysis, thus thorough study on it is necessary. In addition, all the verification hardware uses off the shelf inductors. However, magnetic integration is possible to further increase power density of the total solution.

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