A High Temperature RF Front-End of a Transceiver for High Speed Downhole Communications

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(ABSTRACT)

Electronics are normally designed to operate at temperatures less than 125 ^{o}C. For high temperature applications, the use of those normal electronics becomes challenging and sometimes impractical. Conventionally, many industries tried to push the maximum operating temperature of electronics by either using passive/active cooling systems or tolerating degraded performance. Recently, there has been a demand for more robust electronics that can operate at higher temperature without sacrificing the performance or the use of any weighty, power hungry, complex cooling systems.

One of the major industries that need electronics operating at high temperature is the oil and gas industry. Electronics have been used within the field in many areas, such as well logging downhole telemetry systems, power networks, sensors, and actuators. In the past, the industry has managed to use the existing electronics at temperatures up to 150 ^{o}C. However, declining reserves of easily accessible natural resources have motivated the oil and gas industry to drill deeper. The main challenge at deep wells for downhole electronics is the high temperatures as the pressures are handled mechanically. The temperature in deep basins can exceed 210 °C. In addition, existing well logging telemetry systems achieve low data transmission rates of less than 2.0 Mbps at depth of 7.0 Km which do not meet the growing demand for higher data rates due to higher resolution sensors, faster logging speeds, and additional tools available for a single wireline cable. The main issues limiting the speed of the systems are the bandwidth of multi-conductor copper cable and the low speed communication system connecting the tools with the telemetry modem.

The next generation of the well logging telemetry system replaces the multi-conductor wireline between the surface and the downhole with an optical fiber cable and uses a coaxial cable to connect tools with the optical node in downhole to meet the growing needs for higher data rates. However, the downhole communication system between the tools and the optical modulator

remains the bottleneck for the system. The downhole system is required to provide full duplex and simultaneous communications between multiple downhole tools and the surface with high data rates and able to operate reliably at temperatures up to 230 °C.

In this dissertation, a downhole communication system based on radio frequency (RF) transmission is investigated. The major contributions of our research lie in five areas. First, we proposed and designed a downhole communication system that employs RF systems to provide high speed communications between the downhole tools and the surface. The system supports up to six tools and utilizes frequency division multiple access to provide full duplex and simultaneous communications between downhole tools and the surface data acquisition system. The system achieves 20 Mbps per tool for uplink and 6 Mbps per tool for downlink with bit error rate (BER) less than 10^{-6}. Second, a RF front-end of transceiver operating at ambient temperatures up to 230 ^{o}C is designed and prototyped using Gallium Nitride (GaN) high electron mobility transistor (HEMT) devices. Measurement results of the transceiver's front end are reported in this dissertation. To our knowledge, this is the first RF transceiver that operates at this high temperature. Third, current-voltage and S-parameters characterizations of the GaN HEMT at ambient temperatures of 250 ^{o}C are conducted. An analytic model that accurately predicts the behavior of the drain-source resistor (R_{DS}) of the GaN transistor at temperature up to 250 ^{o}C is developed based on these characterizations. The model is verified by the analysis and the performance of the resistive mixer. Fourth, a passive upconversion mixer operating at temperatures of 250 ^{o}C is designed and prototyped. The designed mixer has conversion loss (CL) of 6.5 dB at 25 ^{o}C under local oscillator (LO) power of 2.5 dBm and less than 0.75 dB CL variation at 250 ^{o}C under the optimum biasing condition. Fifth, an active downconversion mixer operating at temperatures up to 250 ^{o}C is designed and prototyped. The proposed mixer adopts a common source topology for a reliable thermal connection to the transistor source plate. The designed active mixer has conversion gain (CG) of 12 dB at 25 ^{o}C under LO power of 2.5 dBm and less than 3.0 dB CG variation at 250 ^{o}C. Finally, a novel high temperature negative adaptive bias voltage circuit for a GaN based RF block is proposed. The proposed design comprises an oscillator, voltage doubler, and temperature dependent bias controller. The voltage offset and temperature coefficient of the generated bias voltage can be adjusted by the bias controller to match the optimum biasing voltage required by a RF building block. The bias controller is designed using a Silicon Carbide (SiC) bipolar junction transistor.

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(GENERAL AUDIENCE ABSTRACT)

A downhole communication system provides two-way communications for multiple tools located in a deep oil well. The main challenge for the downhole communication system as the oil wells get deeper is the high ambient temperatures as the pressures can be handled mechanically. The temperature in deep basins can exceed 210 °C. Cooling and heat extraction techniques with fans are impractical for downhole systems due to increased weight, power, and system complexity. In addition, the current downhole communication systems have low transmission speed, which do not meet the growing demand for higher data rates due to higher resolution sensors, faster logging speeds, and additional tools available for a single wireline cable.

In this work, a downhole communication system based on radio frequency (RF) transmission is designed. The system supports up to six tools and provides high speed simultaneous communications which enable more sensors to be integrated in each tool. A high temperature RF front-end of the transceiver which will be connected to each tool is designed and prototyped using Gallium Nitride (GaN) semiconductor technology. GaN technology is selected due its ability to operate at harsh environment. The measurement results show a reliable performance for the RF front-end at temperatures up to 230 ^{o}C. To our knowledge, this is the first RF front-end that operates at 230 ^{o}C reported in the open literature.

The proposed downhole communication system will enhance the speed and reliability of the oil and gas operations. This also will enable the industry to observe the wells and act in real time which in turns save operation time and bring a significant cost reduction in oil and gas operations. Most importantly, the proposed system will enable the industry to explore deeper untapped wells and add more features to the tools which were not possible before due to speed and high temperature limitations.

To my parents, wife, kids, sisters, and brothers

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Chapter 1 Introduction

Traditionally, many industries tried to operate normal electronics at harsh environment by using costly methods such as passive/active cooling, or tolerating a degraded performance. Recently, there has been a demand for electronics that can operate at higher temperature with performance matches the one obtained at normal room temperature and without the use of weighty, power hungry, complex cooling systems.

The advancement of the wide bandgap (WBG) semiconductor technologies pushes the limit for the maximum operating temperature [1]-[4]. Unlike the commonly used silicon technologies, the WBG technologies have almost zero leakage current at high temperatures and are thermally robust. Further, they are more efficient and can have very low noise figure (NF), while achieving high gain and high linearity. Therefore, WBG technologies are the most promising technology for the high temperature applications.

Furthermore, most of the high temperature research is focusing on power electronics and low frequency circuits and very little RF applications [5]-[12]. Currently, high temperature RF circuits are mostly used for Radar design and at temperatures up to 125 ^{o}C and usually used with one of the cooling techniques [13]. RF systems capable of operating at high temperatures can open the horizon for many more applications and resolve many challenges that industries face.

1.1 High Temperature Applications

There are many applications where high temperature electronics (HTE) are needed. Generally, any hot environment with ambient temperature above 125 ^{o}C and require operation for long hours is considered an area for a high temperature application. The oldest user of high-temperature electronics is the downhole oil & gas industry. In this application, the operating temperature is a function of the underground depth of the well. Worldwide, the typical geothermal gradient is 25 ^{o}C/km depth, but in some areas, it is greater [13]. In the past, drilling operations

have reached their limit at temperatures of 150–175 ^{o}C, but advancing technology has motivated the oil and gas industry to drill deeper, as well as in regions of the world with a higher geothermal gradient. In this field, high temperature electronics can be applied to communications among the tools and RF sensing.

The other important application for HTE is the avionics and aerospace [13]-[16]. Traditionally, engine monitoring and control is a centralized architecture. Many sensors and actuators are placed near the hot engine and connected with heavy hard-wire that has hundreds of conductors to a controller placed at cooler environment. Moving to wireless system or a distributed control system places the engine control and electronics close to the engine which in turns can reduce the complexity of the interconnections and the system. This transition can save hundreds of pounds of aircraft weight [13].

Space mission also another important application for HTE. NASA has been working on developing high temperature wireless RF communications to support Venus missions [1]. Temperature in this application can exceed 480 ^{o}C.

Moreover, HTE can be applied to other areas such as automobile [17]-[18], process monitoring, and geothermal fields [19]. Reliable electronics that provide performance independent of temperature without adding any extra cooling systems can reduce the cost significantly and open the horizon to new features and applications for many industries.

1.2 Well Logging System

In oil and gas exploration, the sophisticated downhole instruments are lowered into a harsh environment well to acquire data about the surrounding geologic formations. This practice, known as well logging, measures resistivity, radioactivity, acoustic travel time, magnetic resonance, and other properties to determine characteristics of the formation, such as lithology, porosity, permeability, and water/hydrocarbon saturation [14]. The sensed data is either recorded in a memory or sent in real time to the surface. For real time transmission, tools convey data to the surface via downhole telemetry system. The data transmission between the surface and the tools in downhole is asymmetric since most of the data is transmitted from the tools to the surface and little data, mostly commands, calibration, and updates, is transmitted from surface to the downhole tools. Next sections elaborate on the conventional and future telemetry systems for well logging.

1.1.1 Conventional Telemetry System for Well Logging

The current telemetry systems achieve data rates of only approximately 2 Mbps with cable length of less than 7.5 Km and at temperatures up to 150 °C [21]-[22]. This speed fails to meet the growing demand for higher data rates due to higher resolution sensors, faster logging speeds, and additional tools available for a single wireline cable.

Figure 1.1 shows the block diagram of the existing telemetry system for well logging. The current telemetry system uses multi-conductor copper wireline to provide real time communications between the surface data acquisition system and downhole tools [21]-[22]. For example, in [22], the multi-conductor cable is configured to multiple orthogonal modes that carry telemetry signals, DC power and AC power. Two modes are being used for telemetry. Each telemetry mode has bandwidth of less than 300 KHz. Asymmetric digital subscriber line (ADSL) technique is used to achieve a maximum data rate of 2 Mbps with both modes at cable length of 7.5 Km. However, data transmission rates are still lagging behind the high data rates and high resolution sensors and tools. The main issues for the current system limiting the speed of the systems are the bandwidth of multi-conductor copper cable and the low speed communication system connecting the tools with the telemetry modem. The maximum bandwidth of the multi-conductor cable is less than 300 kHz for each mode at cable length of 7.5 Km and the bandwidth shrinks further as cable length increases to reach deeper wells.

The other important challenge for the current downhole telemetry system is high temperature, as the pressure can be handled mechanically. The temperatures in deep basins can exceed 210 °C, but the current drilling operations are still around 150 °C [21]-[23]. This is due to the fact that the current electronics used in these systems can operate only up to 150 °C before being retrieved from the well [13]-[25]. Cooling and conventional heat extraction techniques with fans are impractical due to increased weight, power consumption, and added complexity. A more robust and high speed telemetry system that can tolerate higher temperatures becomes necessary.

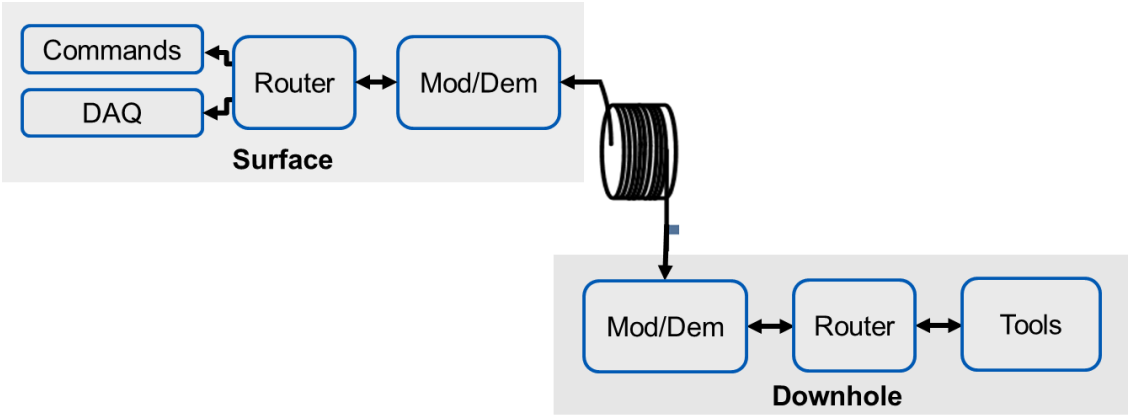


Figure 1.1: Block diagram of a conventional telemetry for well logging.

1.1.2 Next Generation Telemetry for Well Logging

The future telemetry system replaces the multi-conductor copper with optical fiber cable to overcome the bottleneck of the current system. The optical fiber has many advantageous over the copper cables. It is, simple to fabricate, less expensive and has 10,000-time larger bandwidth. With improvement of optical cable capability to operate reliably at high temperature, it becomes feasible to use for well logging telemetry [26]. However, optical fiber sensors are still expensive compare with the electrical sensors and optical fiber need to operate with electrical sensors and tools. Therefore, tools are connected to coaxial cable then interfaced with optical link [27].

Figure 1.2 shows the projected well logging system with multiple tools using hybrid fiber coaxial telemetry. An optical fiber cable ranging from 5 to 15 Km connects the surface with downhole electro-optical convertor. Then, tool bus, a coaxial cable that can operate at ambient temperature of 250^{o}C, connects multiple tools with an electro-optic modulator. The tools should communicate simultaneously with the surface. The communication between the surface and downhole is asymmetric. Large data is from the downhole to the surface and relatively smaller data from surface to the downhole.

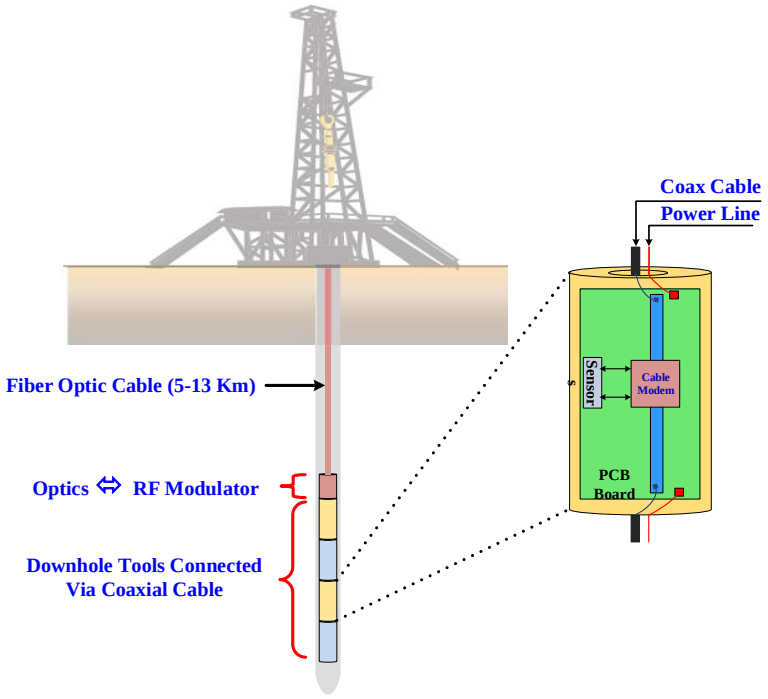


Figure 1.2: Projected hybrid fiber coaxial telemetry for well logging.

1.3 Research Scope and Contributions

The research work of this dissertation was to design a RF front-end for high temperature application and particularly for downhole communications. The major objective of this research is to propose RF system that can provide high performance with higher speed for downhole communications, design RF transceiver's building blocks that can operate at high temperature, and prototype the RF transceiver and measure its performance at high temperature. The main research contributions for this dissertation work as follows.

First, we proposed and designed a downhole communication system that employs RF as a communication mean. The system supports up to six tools and utilizes frequency division multiple access to provide full duplex and simultaneous communications between downhole tools and the surface data acquisition system. The system can achieve 20 Mbps per tool for uplink and 6 Mbps per tool for downlink with bit error rate (BER) less than 10^{-6}.

Second, GaN based RF front-end of transceiver operating at ambient temperatures up to 230 ^{o}C is designed. Measurement results of the transceiver front-end are reported in this dissertation. To our knowledge, this is the first RF transceiver front-end that operate at this high temperature. Figure 1.3 shows the prototyped high temperature GaN based transceiver.

Third, current-voltage (IV) and S-parameters characterizations of a GaN HEMT at ambient temperatures of 250 ^{o}C are conducted. An a nalytic model that can predict the behavior of drain-source resistance (R_{DS}) is developed. The model is verified by the analysis and the performance of the resistive mixer.

Fourth, a tradeoff between the power dissipation of the GaN device and maximum ambient operating temperature is identified through thermal analysis. The analysis is conducted on a packaged GaN device with PCB using ANSYS Icepak. With the thermal analysis, we identified the maximum power limit that can GaN transistor consume to operate below the maximum junction temperature at elevated ambient temperature of 230.0 ^{o}C. The simulated results are reported is this dissertation.

Fifth, a passive mixer operating at ambient temperatures of 250 ^{o}C is designed and prototyped. The mixer adopts resistive topology that utilizes the channel resistance as mixing element. Temperature effects on the conversion loss is analyzed, and the bias voltage that provide optimum conversion loss is predicted through the analysis. The predicted optimum biasing is verified with the measured results. The designed mixer has conversion loss (CL) of 6.5 dB at 25 ^{o}C under local oscillator (LO) power of 2.5 dBm and less than 0.75 dB CL variation at 250 ^{o}C under optimum biasing.

Sixth, an active downconversion mixer operating at temperatures up to 250 ^{o}C is designed and prototyped. The proposed mixer adopts a common source topology for a reliable thermal connection to the transistor source plate. The designed active mixer has conversion gain (CG) of 12 dB at 25 ^{o}C under local oscillator (LO) power of 2.5 dBm and less than 3.0 dB CG variation at 250 ^{o}C.

Last but not least, a novel high temperature adaptive biasing circuit for GaN based RF block is proposed. The proposed design encompasses an oscillator, a voltage doubler, and a bias voltage controller. The circuit provides a negative voltage temperature dependent. The output of the bias voltage controller is function of the V_{BE} of the SiC bipolar junction transistor utilized by the circuit. The voltage level and the temperature coefficient (TC) of the generated bias voltage can be controlled by the resistors ratio of the bias controller to match the bias voltage required by an RF building block. The simulation results show that the TC of the generated bias voltage matches

closely the TC of the optimum bias voltage required by the resistive mixer at temperatures up to 250 ºC.

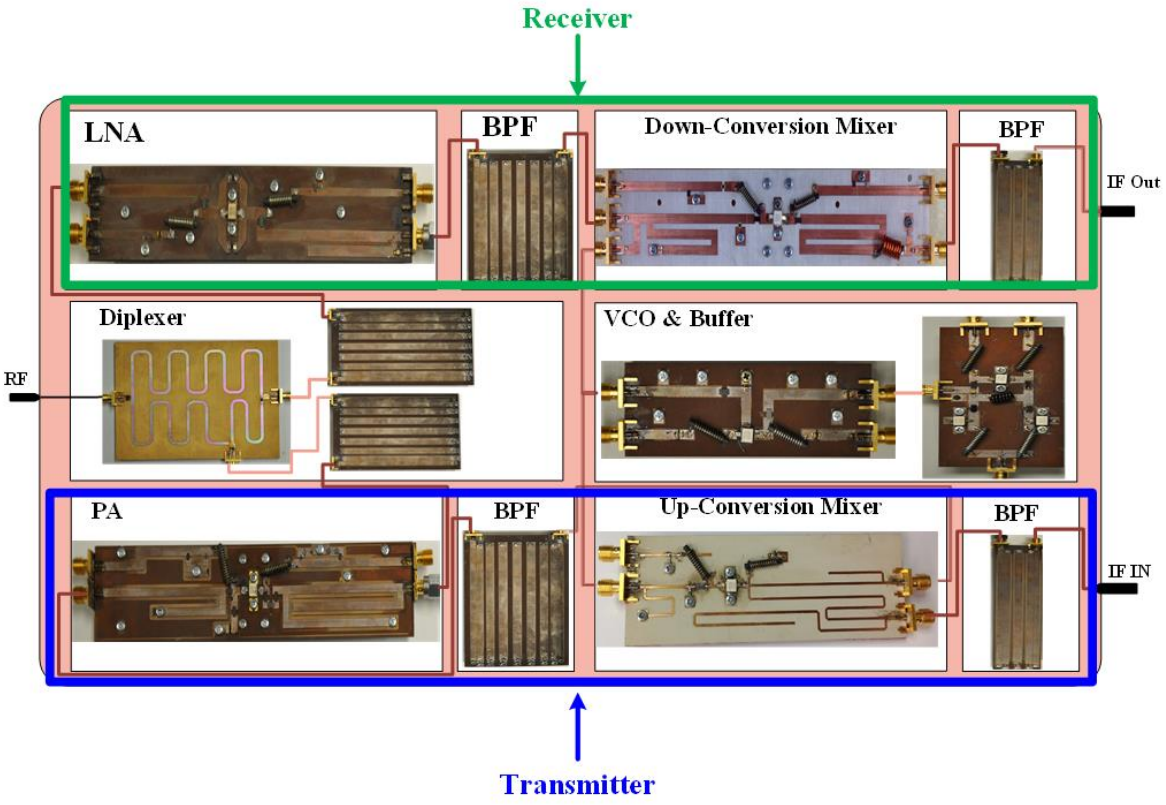


Figure 1.3: Prototype of the high temperature GaN based RF front-end.

1.4 Dissertation Outline

The dissertation is organized as follows; Chapter 2 discusses the necessary preliminaries in regards to the research proposal. Some theoretical background and advantages of radio over fiber (RoF) system are presented, followed by a brief survey on RoF components for high temperature applications. The components investigated are optical fiber, lasers and photodetectors, and modulators. Next, RF transceivers that can operate at high temperature is reviewed. Finally, the temperature effects on the main aspect of the transceiver performance is discussed. The chapter gives insight into the design philosophy for RF front-end transceiver for next generation of downhole communication. This background is necessary to prepare for the system design that will be presented in the next chapter.

In chapter 3, a downhole communication system architecture is proposed. Next, a characterization for the channel employed in downhole is presented. Then, based on the channel characterization, frequency planning for the transmit and receive paths is proposed. Then, transceiver architecture is introduced. Superheterodyne transceiver architecture is adopted for the design. Subsequently, a link budget calculation to find the component specifications is performed. After obtaining the initial specifications of the transceiver's building block, the downhole communication system is modeled and implemented in AWR simulation tool to verify its performance. Then, the components specs are optimized to provide a data rate of 20 Mbps per tool with BER of less than 10^{-6}. The total number of tools included in the design is six. Then, the simulation results with optimized specifications are present. Finally, a summary of the minimum specifications for the RF transceiver's building blocks is presented. With these minimum specifications, the designed downhole communication system provides a full duplex communication with 20 Mbps per tool using 64 quadrature amplitude modulation for six tools with BER less than 10^{-6}.

After obtaining the building blocks' specifications, the technology option to realize these blocks is investigated in chapter 4. Qorvo GaN HEMT technology is selected since it has the highest junction temperature. This technology is intended for high power amplifiers. High power dissipation can rise the junction temperature to 275 ^{o}C at room temperature. We used these transistors to design our transceiver's building blocks at low power but at high temperature. Since these transistors are characterized only at temperatures less than 85 ^{o}C, a new characterization at high temperature is needed. First, we reviewed the open literature to study the impact of temperature on GaN characteristics. Next, high temperature characterization setup is introduced. Then, we performed characterization on the Qorvo GaN HEMT devices at temperatures up to 250 ^{o}C. The temperature effects on drain current, transconductance, small signal parameters, and drain resistance is highlighted. Finally, a high temperature model that predicts the behavior of R_{DS} at temperatures up to 250 ^{o}C is developed.

In chapter 5, the design and analysis of the building blocks are introduced. First, we presented high temperature design consideration that include the thermal analysis for the packaged device along with a PCB/heatsink, and passive component selection. Then, we elaborated on the resistive mixer design which is used in the transmitter design as upconverting stage. Detailed analysis with

measurements validation is presented. The analysis is conducted using the high temperature R_{DS} model was developed in chapter 4. Furthermore, the bias voltage that provides the optimum performance at a wide temperature range is predicted using the analysis and verified though measurements. Next, the active mixer which is used in the receiver as a downconversion stage is also elaborated. The impact of temperature on conversion gain and noise figure is highlighted. Then, bias voltage for the optimum conversion gain and noise figure performances at a wide temperature range is identified through measurements. Then, analysis and measurements for the low noise amplifier, signal generator, power amplifier, filters and diplexers building blocks are presented. Finally, a novel adaptive biasing circuit for depletion mode GaN based RF building block is proposed. The concept is first explained through block diagram. Then, the circuit implementation and temperature analysis is presented. The performance is verified through simulation. The compensation circuit provide temperature dependent bias voltage that closely matches the optimum bias voltage required by the resistive mixer. The temperature coefficient of the output bias voltage can be easily adjusted by changing the resistors ratio of the controller.

Chapter 6 introduces the transceiver prototype and the measurement results at a wide temperature range. First, the high temperature measurement setup is described. Then, the measured results of the signal generator performance at a wide temperature range and different carrier frequencies are presented. Subsequently, the measured results of the receiver are reported. The measurement results include bit error rate (BER), error vector magnitude (EVM) performances with 16 QAM, 64 QAM and 128 QAM at 25 ^{o}C, 150 ^{o}C and 230 ^{o}C. Next, the measured results of the transmitter are presented. The measurement results include EVM and adjacent channel power ratio (ACPR) performances with 16 QAM, 64 QAM and 128 QAM at 25 ^{o}C, 150 ^{o}C and 230 ^{o}C. These results prove the feasibility of using the RF transceiver for downhole communications and high temperature applications.

Chapter 7 summarizes and concludes the work presented in this dissertation. The research presented here is a first-of-its-kind proposal and consequently work can be continued in several different areas of concentration. New and exciting applications can be imagined with high temperature RF circuits and systems.

Chapter 2 Preliminaries

This chapter discusses the necessary preliminaries in regards to downhole communication system design. Some theoretical background and advantages of radio over fiber (RoF) system are presented, followed by a brief survey on RoF components for high temperature applications. The components investigated are optical fiber, lasers and photodetectors, and modulators. Next, RF transceiver that can operate at high temperature is reviewed. Finally, the temperature effects on the main aspect of the transceiver performance is discussed. The chapter gives insight into the design philosophy for RF front-end transceiver for next generation of downhole communication. This background is necessary to prepare for the system design that will be presented in the next chapters.

2.1 Radio over Fiber System

The underlying principle of radio over fiber (RoF) transmission is that it involves conveying analog radio signal through an optical fiber link. The radio signal is used to modulate the lightwave. Figure 2.1 shows the diagram of the radio fiber link. The baseband signal processing stage generates a modulated signal (e.g. QAM). Subsequently, a radio frequency (RF) upconversion stage produces the RF signal, which is applied to the optical link using the electronic-to-optical converter (e.g external optical modulator). At the receiving end, the RF signal is recovered from the optical-to-electronic converter (a photodiode). Then, the recovered RF signal is down converted to a baseband signal. Finally, the baseband signal processing stage at the receiver side demodulate and recover the original signal.

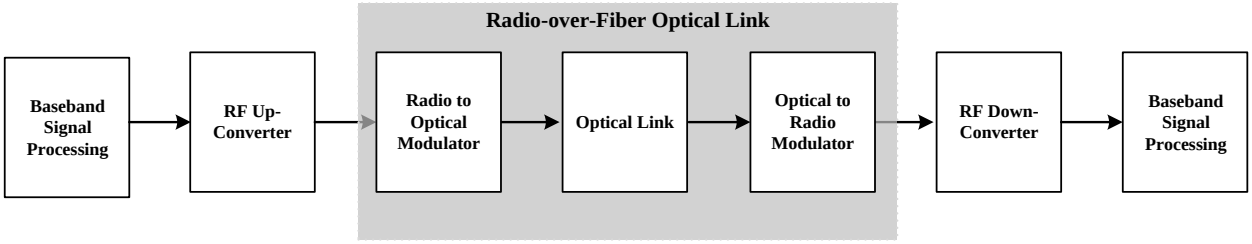


Figure 2.1: Block diagram of a typical radio over fiber system.

The main advantage of the radio over cable system is that it enables multiple transceivers to have simultaneous full duplex communications through one coaxial cable and one optical fiber, which is desirable for a well logging system with multiple tools. The second main advantage is that RoF requires lower link bandwidth to achieve high data rate and this is achieved using bandwidth efficient analog modulation techniques [30]. Therefore, the radio of fiber approach is adopted for the proposed downhole communication system.

2.2 RoF Components for High Temperature Applications

The key components for the RoF are optical fiber, optical source, optical modulator, photodiodes and RF transceivers. There have been commercially available optical fiber cables operating at high temperature. AFLGloble in [31] offers variety of optical fiber cables that can operate up to 300 ^{o}C with low attenuation at different wavelengths. Optical sources, on the other hand, are very sensitive to temperature and their wavelength deviates substantially with temperature. These sources normally located at the surface, where the temperature is fixed at 25 ^{o}C, and a pure light signal is sent from the surface to the downhole external optical modulator. Then, the optical modulator utilizes the pure light signal received from the surface to modulate the downhole RF signals and send it to the surface.

Optical modulators that operate at high temperature have been recently reported. In [32] characterizations for graphene RF optical modulator at temperatures up to 145 ^{o}C are reported. The modulator shows a stable performance up to the specified temperature. In [33], a high sensitivity Mack-Zehnder interferometric that operate at high temperature is reported. The modulator was placed inside a furnace and tested up to 400 ^{o}C. The results show the modulator has 0.070 nm/^{o}C temperature sensitivity at 25 to 400 ^{o}C.

Photodetectors devices based on conventional Si semiconductors are usually unable to operate in high temperature environment. However, photodetectors based on wide bandgap technologies can provide much better capabilities at high temperature. In fact, Clairexa Technologies, Inc has commercially provided high temperature AlGaAS photodetectors that can operate up to 225 ^{o}C [34]. There is also research in utilizing GaN technologies to fabricate avalanche photodetectors [35]. GaN technologies offer much higher temperature capabilities.

Although there are numerous RF transceiver that can operate at room temperature such as [36]-[38], very few transceivers that operate at temperatures up to 90 ^{o}C exist [39]. In [39], a -90 dBm sensitivity transceiver operating at temperature up to 90 ^{o}C is reported. All of these designs are fabricated in Si CMOS technologies which suffer from high leakage currents at high temperature. These leakage currents cause latch up and eventually damage the design. In our research, we design a transceiver using a wide bandgap GaN HEMT technology that endures high temperature environment.

2.3 Subcarrier Multiplexing

Optical subcarrier multiplexing (SCM) is a scheme where multiple signals are multiplexed in the radio frequency (RF) domain and transmitted by a single wavelength. The major advantage of SCM is that RF devices are more mature than optical devices [40]; the stability of a RF oscillator and the frequency selectivity of RF filters are much better than their optical counterparts. In addition, the low phase noise of RF oscillators makes coherent detection in the RF domain easier than optical coherent detection, and advanced modulation formats can be applied easily [40]. SCM has been widely used in analog cable television (CATV) distribution. Due to its simplicity and low-cost implementation, SCM has also been proposed to transmit multichannel digital optical signals using direct detection [41], [42] for local area optical networks. In the proposed downhole communication system, the RF carriers will be used by the tools to transmit and receive data via coaxial cable. Then, these signals with different RF carrier frequencies are combined at the coaxial cable and optically transmitted to the surface using an optical modulator.

2.4 RoF System Characterization

RoF links may be characterized using typical analog RF system performance parameters [41]-[46]. The RoF link may be considered a subsystem in a larger RF system, to which an RF signal is input and from which an RF signal is output, as shown in Figure 2.2.

For a directly modulated laser link, the RF waveform is used to modulated the current through a semiconductor through a semiconductor laser, which in turns modulates the intensity of the emitted light from what corresponds to the radio to optical modulator in Figure 2.2. The intensity of light thus depends on the amplitude of the RF input signal. Externally modulated RoF link transmitters using Mach-Zehnder modulator (MZM) or electro-absorption modulator (EAM)

also produce light output power modulation dependent on the amplitude of the RF signal, although in these cases the modulation is induced by a voltage applied to the modulator. In photodiode receivers, the incident light power is converted to a photocurrent, so the RF signal amplitude is dependent on the light intensity. Thus, overall, an ideal RoF link is linear [41]. A link gain can be defined for the intrinsic RoF link which relates the RF output power from the optical-to-electronic converter to the RF input power to the electronic-to-optical converter. Because of the conversions from amplitude to power and power to amplitude, it should be noted that loss in the optical domain causes the square of this loss for the RF signal − thus a 3 dB optical fiber loss will cause a 6 dB RF loss. The overall RoF link small-signal gain is then also dependent on the "conversion efficiencies" of the electronic-to-optical and optical-to-electronic converters.

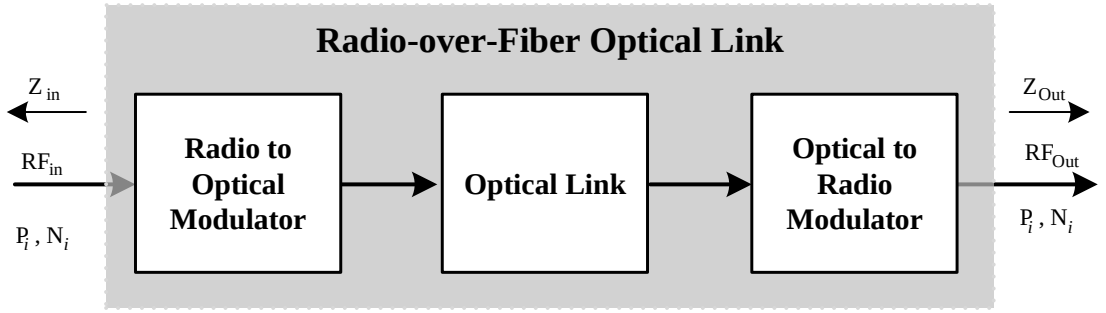


Figure 2.2: A radio over fiber link as subsystem of a large system

For an MZM externally modulated link, the gain is given by [45]:

$$G_e = \left(\frac{P_{opt}\eta_M\Re}{L_{opt}L_M}\right)^2 \frac{Z_{in}}{Z_{out}} \tag{2.1}$$

where P_{opt} is the input optical power to the modulator, L_{opt} is the loss of the optical link, η_M is the slope efficiency of the modulator at the operating point (V^{-1}), L_M is the modulator optical insertion loss, $\Re$ is the photodiode responsivity (A/W), and Z_{in} and Z_{out} are the input and the output impedances as shown in Figure 2.2. For an MZM, the slope efficiency is given by [45]:

$$\eta_M = \frac{\pi \cos\phi}{2V_\pi} \tag{2.2}$$

where V_π is the modulator half-wave or switching voltage and ϕ represents the modulator bias point relative to the quadrature bias.

What notable in Eq (2.1) is that link gain can be increased by increasing the input optical power. However, in downhole communications the optical power remotely pumped and depends on the fiber cable characteristics and length. Also, the photodiode responsivity and the efficiency of the optical modulator drop as temperature increases and their temperature effect should be considered in designing the RoF link.

Another important parameter should be considered is the noise figure, NF, of the RoF link and it can be expressed as following [41]:

$$NF = 10\log\frac{N_o}{N_i G_e} \tag{2.3}$$

where N_o is the output power and N_i is the input noise power, which is typically given by $N_i = K\times T\times B$, where K is Blotzmann's constant, T is ambient temperature, and B is the noise bandwidth. G_e is the link gain using the external modulator. Therefore, the optical link gain (or loss) impact on noise figure performance will be a significant factor in link performance. Additional noise in the output will arise from photodiode noise and the laser relative intensity noise and thermal noise and photodiode shot noise in the receiver, particularly as ambient temperature increases.

A low noise pre amplifier can be used for small signal levels to improve the noise performance. With sufficient gain, through the well-known effect expressed by the Friis cascade equation for system noise factor, the overall system noise factor, F_{sys}, can be reduced. The Friis equation can be expressed as following:

$$F_{sys} = F_1 + \frac{F_2-1}{G_1} + \frac{F_3-1}{G_1 G_2} + \cdots \tag{2.4}$$

where F_1 and G_1 are the noise factor and the gain of the first stage of the system and F_2 and G_2 are the noise figure and the gain of the second stage of the system.

The abovementioned equations show dependence on the frequency of the RF signal for any real RoF link. Laser and modulator slope efficiencies and photodiode responsivity exhibit frequency dependence, and although optical fiber loss does not depend on the RF frequency, the effective loss will have some dependence due to fiber dispersion. Evidently, impedance mismatching with frequency will also cause gain variations.

Nonlinear effects, such as saturation of components, can be expected. As with typical RF system performance [47], these effects can be represented using the compression point, harmonic and intermodulation distortion intercept points, and the dynamic range of the RoF link. These parameters are shown in Figure 2.3, which represents a typical plot of output power against input power for an analog system, such as a RoF link.

The dynamic range of the system can be defined as the ratio between the output compression point and noise floor (compression dynamic range) or as the ratio of the signal (fundamental) power at which distortion products increase above the noise floor and the signal power at which it becomes discernible above the noise floor, the spurious-free dynamic range (SFDR).

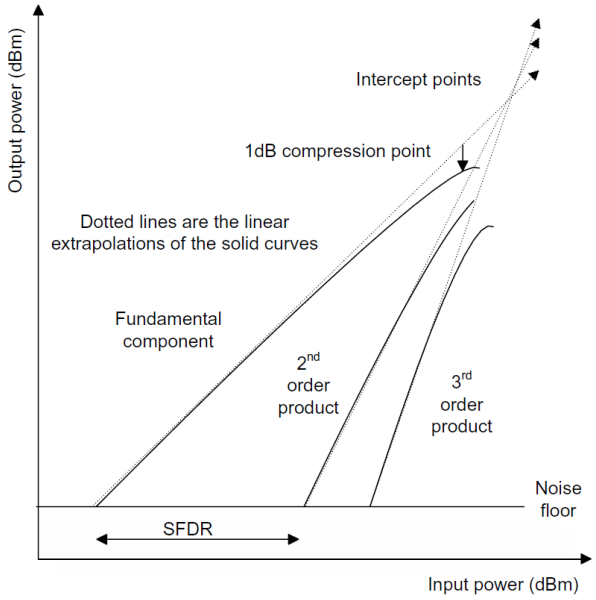


Figure 2.3: Typical plot of output power against input power for an analog RF system, showing compression point, intercept points, noise floor and dynamic range.

When data is modulated onto the RF signals, system performance can be characterized in terms of the quality of the received data. In common with digital systems, a bit-error ratio (BER) can be used and can be related to signal-to-noise ratio (SNR). However, in systems using complex multilevel modulation schemes, wireless system standards often specify the performance in terms of the errors in the received signal constellation points compared to the ideal constellation points. Error vector magnitude (EVM), the ratio of the mean error power to the mean peak power (the power at the outermost signal constellation point), is used here to evaluate the system performance.

2.5 Chapter Summary

In this chapter, we discussed the necessary preliminaries to downhole communication system design. RoF system background and advantages were presented, and it is followed by a brief survey on RoF components for high temperature applications. The components investigated were optical fiber, lasers and photodetectors, and modulators. Next, RF transceiver that can operate at high temperature is reviewed. Finally, RoF system characterizations with emphasis on downhole applications were discussed.

Chapter 3 Proposed Downhole Communication System Design

This chapter describes the architecture of the proposed downhole communication system. First, a characterization for the channel employed in downhole is presented. Next, the radio frequency (RF) transceiver architecture is introduced. A superheterodyne transceiver architecture is adopted for the design. Based on the channel characterizations and the transceiver architecture, frequency allocations for the transmit and receive channels are then proposed. Subsequently, a link budget calculation to find the transceiver's building blocks specifications is performed. After obtaining the initial specifications of the transceiver's building blocks, the proposed downhole communication system is implemented in AWR simulation tool to verify its performance. Then, the simulation results for the system with optimized specs are present. Last but not least, a summary of the minimum specifications of the transceiver's building blocks is presented.

3.1 System Architecture

The system employs SCM technique which uses a single optical single side band (OSSB) source for all RF signals. The RF frequencies can be combined and split at each end of the RoF link using passive components. Figure 3.1 shows the architecture of the full downhole communication system. The surface system is the shaded part and it operates at room temperature. The surface system is out of scope of this work. The downhole system is the highlighted part and it operates at a wide temperature range. In the downhole, multiple tools share one coaxial cable to convey the information to the surface through RoF link. The signals from the tools are injected to the coaxial cable through power combiner then amplified before it is fed to the external optical modulator which in turns send the combined signals (multiplexed signal) optically to the surface. The downlink modulated optical signal is converted to RF signals at the downhole using a photodiode and an RF front end receiver at each tool selects the assigned carrier frequency. The uplink and downlink channels are separated using diplexers to minimize the potential channel interferences. The architecture also incorporates a low-noise preamplifier before the external

modulator to reduce the noise figure effects of the optical link and post-amplifier after the photodiode to increase the RF signal power to an appropriate level required by each tool.

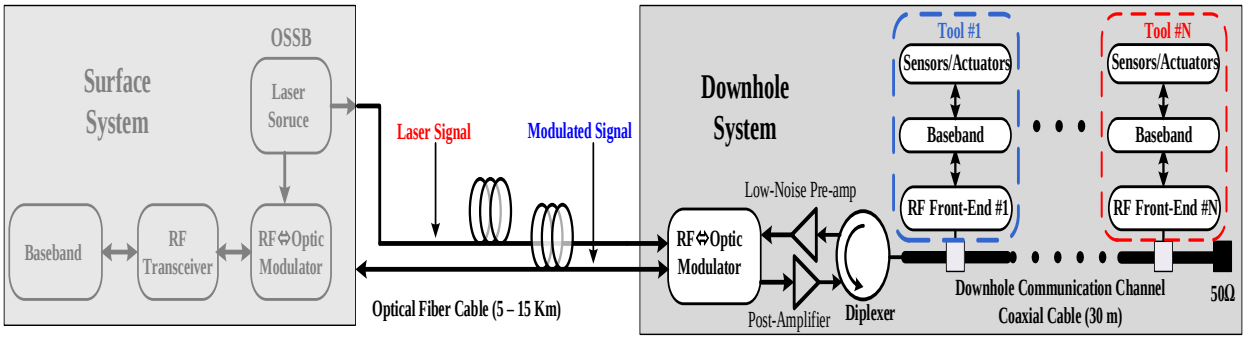


Figure 3.1: The architecture of the proposed downhole communication system.

3.2 Downhole Communication Channel

The downhole channel is a high temperature coaxial cable connecting tools along the line with diplexer before the optical node. The specified coaxial cable has characteristic impedance, Z_o of 50 Ω and it is 30 meters long [48]. The coaxial cable is intended to connect up to six tools. For this purpose, the coaxial cable is divided to multiple 5 meters' segments. Total of six segments connected together with five 3 dB power dividers are characterized at different frequencies. From s-parameters measurements, it is found that each segment has 3.4 dB loss at frequency of 250 MHz and the loss increases as the frequency increases. The overall attenuation at the last segment in the line is 42.0 dB at 250 MHz including the insertion loss resultant from power dividers/combiners and diplexers. Figure 3.2 shows the characterization of one segment and six segments of the coaxial cable. One segment represents the minimum distance between the first tool and the optical node and the six segments represent the distance between the last tool in the line and the optical node.

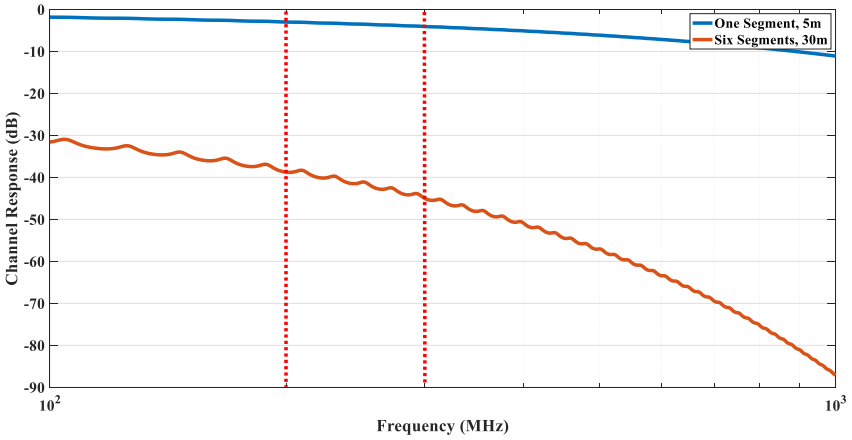


Figure 3.2: The downhole channel characterizations. Blue curve is the response for one segment of 5 meters and red curve is the response of the total six segments plus the loss of the power dividers/combiners.

The downhole channel imposes a tradeoff between the cable attenuation and the maximum frequency can be used by the system. Operating at high frequencies allows for small size boards and designs, with price of increasing attenuation. For this system, the frequency band from 200 to 300 MHz is chosen since the frequency is high enough and offers a reasonably low path loss.

3.3 Proposed RF Transceiver

Figure 3.3 shows the architecture of a single stage superheterodyne transceiver adopted for the downhole communication system. The transceiver enables a tool to transmit the sensed data to the surface system through the coaxial cable and optical fiber using a specific channel and receive a signal from the surface through the same medium but at a different channel. The main advantage for this transceiver is its simplicity. Also it is insensitive to DC offset and IQ mismatch that occur in the direct conversion transceiver, which deteriorate further at high temperatures. The transceiver consists of a diplexer that separates the uplink and downlink bands and connects the transceiver to a 50 Ω coaxial cable. In the receiving path, first comes the low noise amplifier (LNA) then the image band pass filter. The main role for this filter is to filter our any intermodulation products that might be produced from the LNA and to reject any VCO frequencies leaked through the mixer. The intermediate frequency (IF) band pass filter is used to select the desired channel. Then, an automatic gain control stage (AGC) with variable gain amplifier (VGA) is to mitigate any gain variations due to the cable length and temperature variations and ensure an appropriate signal level to the baseband stage. In the transmitting path, IF amplifier boosts the signal to an

appropriate level. Then, the IF band pass filter ensures a clean IF signal delivered to the mixer. Subsequently, the mixer upconverts the IF signal to RF signal after mixing it with the LO frequency. Then, the power amplifier amplifies and delivers the upconverted RF signal to the coaxial cable through the diplexer after the RF filter removes the undesired mixing products. In this transceiver, the same LO frequency is shared by the transmitter and receiver. Therefore, two different IF frequencies for the down-conversion and up-conversion are specified.

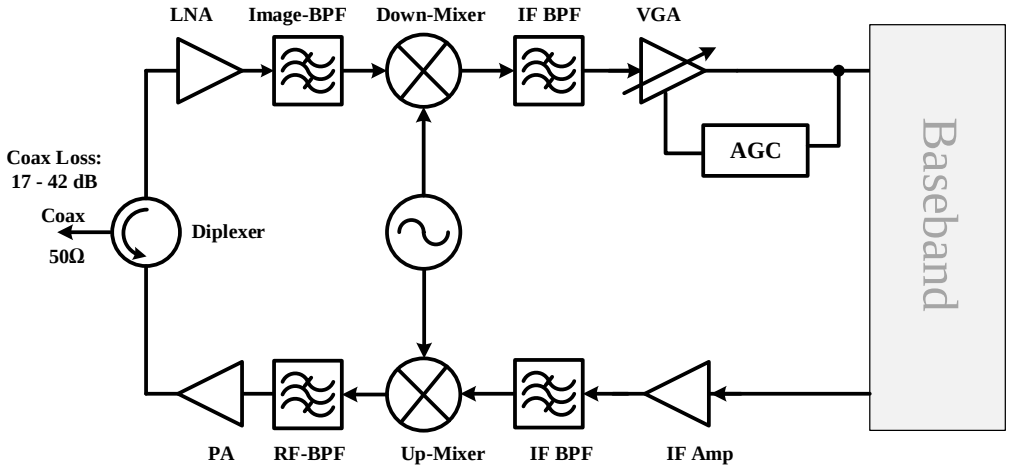


Figure 3.3: The superheterodyne transceiver adopted for the downhole communication system.

3.4 Frequency Planning and Allocation

Before designing the RoF link, uplink and downlink frequency bands are proposed. Based on the downhole channel characterizations, these bands offer minimal attenuation while offering a wide bandwidth per tool and allowing for relatively smaller designs. Also, choosing this VHF bands has the advantages of using laser transmitters and photodiode receivers that operate at RF frequencies while reducing the effects of fiber impairments, most notably that of chromatic dispersion [41].

Figure 3.4 shows the proposed uplink and downlink frequency bands. The lower frequency band is specified to the uplink since this band has lower attenuation and the uplink requires higher SNR for the higher order modulation schemes (64 QAM and 128 QAM). The downlink carries relatively smaller data and uses low order modulation schemes (BPSK and QPSK). Each band has six channels and each channel has 4 MHz bandwidth. The guard bands are typically between 10 % to 25 % of the channel bandwidth in order to minimize the adjacent channel interference [49].

For our design, guard bands of 0.8 MHz among the channels are specified. The guard band between the uplink and downlink bands is 6.0 MHz. The first channel of the band is assigned to last tool which is tool #6, and the last channel which is number 6 is assigned to the first tool.

The local oscillator (LO) is shared by the transmitter and the receiver which leads to having two intermediate frequencies (IF) for the transmit and receive paths. Before the LO frequency is specified, the IF frequencies are determined. The IF frequencies are chosen so that the image filter design is relaxed and possible in-band interferences caused by strong uplink and downline tones are minimized. To ensure that a such problem cannot happen, the uplink and downlink IFs (F_{IF}) are determined based on the following equation [49]:

$$F_{IF} > 2f_{BW} + B_s$$

where f_{BW} is the bandwidth of the uplink/downlink bands and B_s is the guard band between the uplink and downlink bands. For our design, f_{BW} is 28 MHz and B_s is 6.0 MHz which both leads to minimum F_{IF} of 62 MHz. We selected 62.5 MHz as the IF for the downlink band. The LO frequencies are selected to be high side injection which results a LO frequency range from 328 MHz to 352 MHz. Since the LO is shared between the transmitter and the received, the uplink IF is determined to be 97.5 MHz.

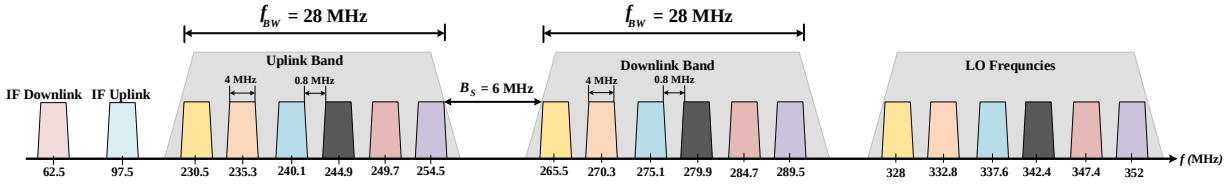


Figure 3.4: Frequency allocations.

3.5 RoF Link Design

Each channel in RoF link must be designed to satisfy the requirements of the downhole system. These links consist of electrical preamplifier, optical source, optical fiber and distribution network, and optical receiver. The performance of the optoelectronic elements such as efficiency, responsivity, noise, P1dB must be specified and based on these specifications RoF link, pre- and post-amplifiers can be designed. Figure 3.4 shows the link budget for the uplink. The total optical link has loss of 34 dB and noise figure of 45 dB at high temperature. The optical modulators at both ends have 1dB compression point of 20 dBm. The minimum loss between the low-noise

preamplifier and the first tool is 17 dB including the losses of the diplexers and power divider, and the maximum loss between the last tool and the preamplifier is 42 dB including the losses of the diplexers and power dividers.

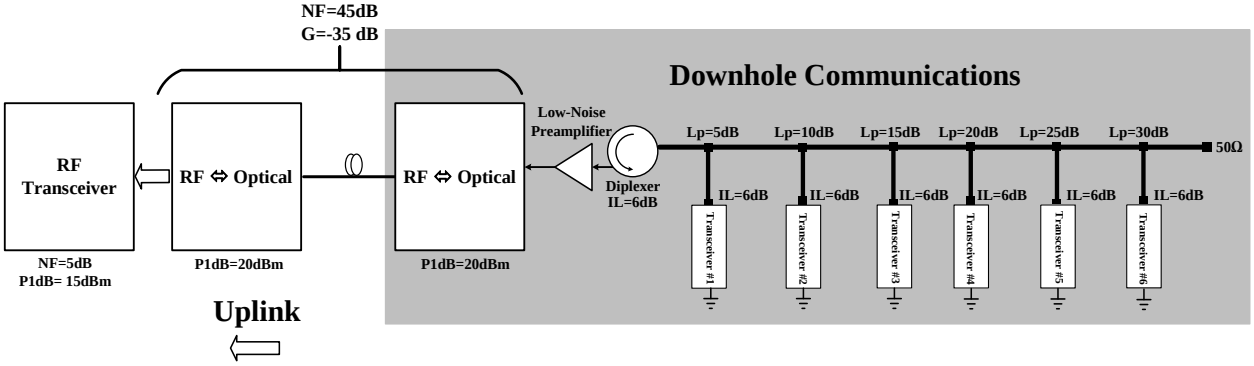


Figure 3.5: Link budget for the uplink RoF. The direction of communication is from downhole to the surface.

For the uplink transmission, an electrical preamplifier must be used to reduce the overall noise figure of the link. The noise figure of the preamplifier is specified to be less 3dB at wide temperature. The gain has to be enough to boost the signal coming from the last tool and reduce the total noise figure introduced by the optical link. On the other hand, the maximum gain is limited by the linearity of the external modulated. The appropriate gain is determined from simulation and Figure 3.6 shows the EVM versus the gain of the low noise preamplifer. It can be seen that maximum gain that provide optimum EVM performance of 3.8% for all tools is 24 dB before the EVM deteriorates due to nonlinearity of the external modulator. However, the effect of the peak-to-the-average should be considered since multiple carries will be employed at the same time. 6 dB back off margin is considered for our design. Therefore, the gain for the low noise amplifier is 18 dB.

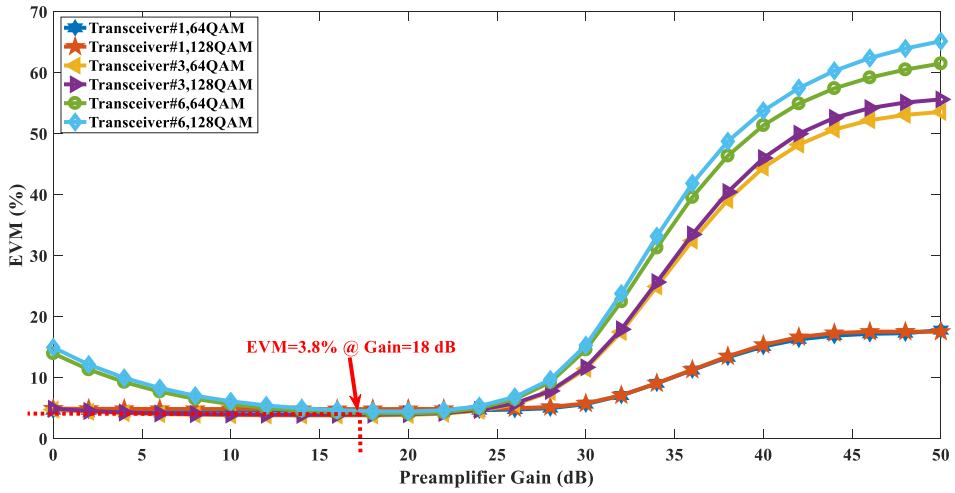


Figure 3.6: EVM versus gain of the low-noise preamplifier for the uplink transmission.

Downlink transmission is data transmitted from the surface to the downhole and it is relatively smaller compared with uplink transmission. Figure 3.7 shows the downlink transmission link budget. The most important design factor is that the gain of the post-amplifier is high enough to provide an appropriate signal level for the last tool in the cable. However, this maximum gain is limited by the linearity of the first tool connected to the cable.

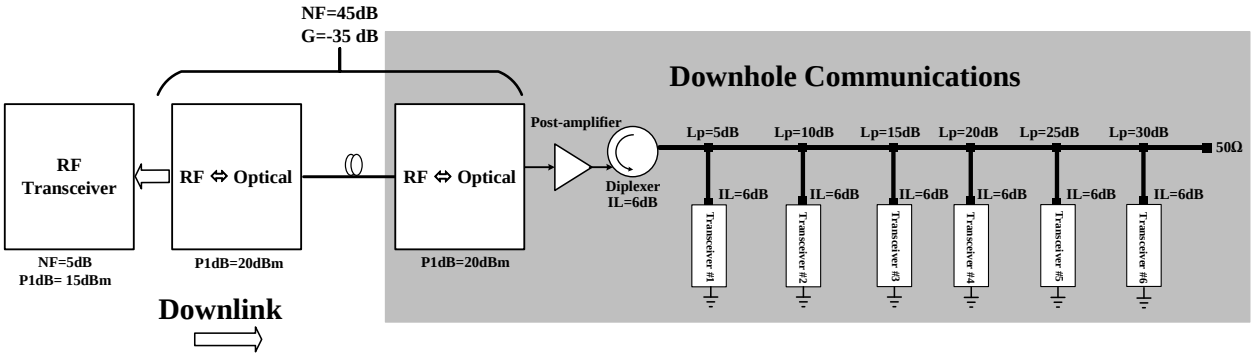


Figure 3.7: Link budget for the uplink RoF. The direction of communication is from surface to downhole.

3.6 Simulation Environment and Simulation result

The complete downhole communication system with the coaxial cable and the fiber link is modeled using AWR tool. The system simulation focuses on developing the minimum specifications of the RF building blocks that provide a sufficient overall performance for the system. All relevant transceiver front-end building blocks, including models of optical

components, are included. 64 QAM and 128 QAM encoders and decoders are used to generate and detect the data for uplink transmission and QPSK encoders and decoders are used to generate and detect the data for downlink transmission.

Figure 3.8 shows the simulation results of the recovered constellation diagram of 64 QAM at the surface for the transmitter #6 which is connected at the far end of the coaxial cable. It can be noticed that the signal quality is satisfactory. The EVM is 3.7% at symbol rate of 3.2 Msym/s.

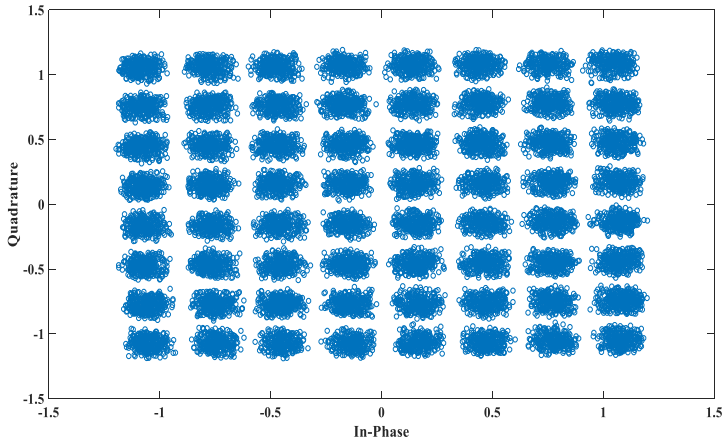


Figure 3.8: Recovered 64 QAM constellation diagram at the surface for tool #6 which is connected at the far end of the downhole cable.

Figure 3.9 shows the simulation results of the recovered constellation diagram of 128 QAM at the surface for the transceiver #6. It can be noticed that the signal quality is also satisfactory. The EVM is 3.85% at symbol rate of 3.2 Msym/s. Figure 3.10 shows the EVM versus the symbol rate. It can be noticed that the EVM of 4% is achieved at 3.2 Msym/s for 64 QAM and EVM of 3.1% is achieved at 3.0 Msym/s for 128 QAM system. EVM of 4% and 3.1% corresponds to bit error rate of 10^{-6} for 64 QAM and 128 QAM, respectively, which is specified for the system.

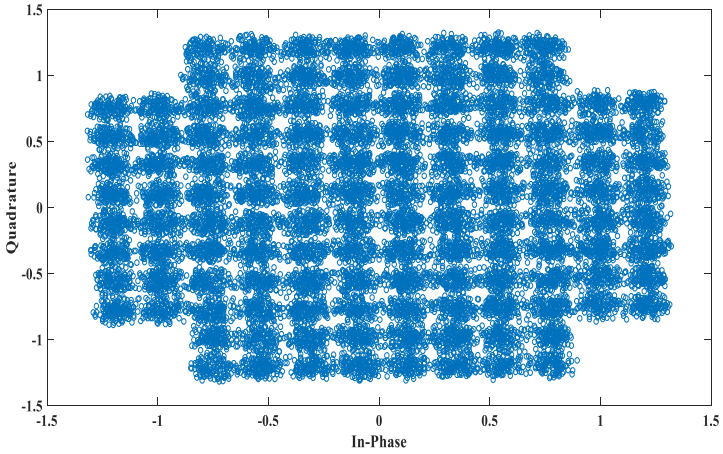


Figure 3.9: 128 QAM constellation diagram received at the surface for tool #6. The symbol rate used in this simulation is 3.3 Msym/s.

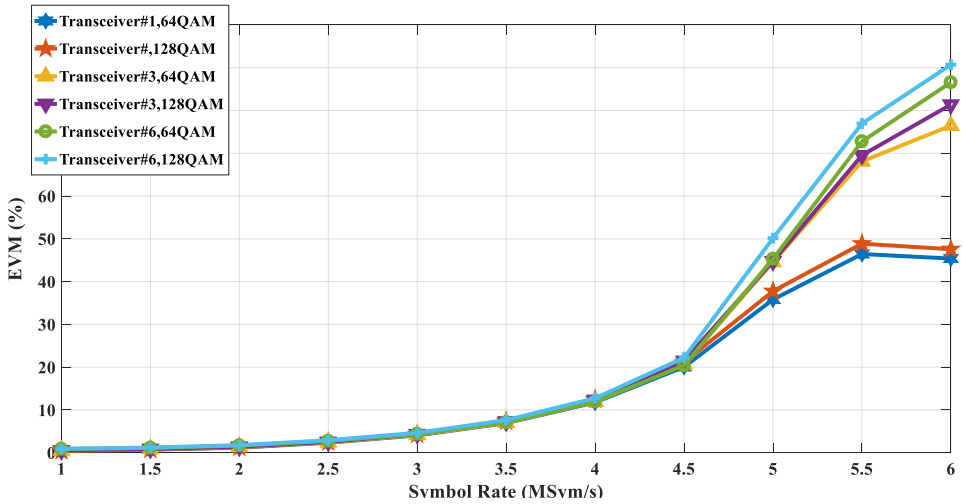


Figure 3.10: EVM versus the symbol rate for multiple tools.

The other important aspect of the transceiver front end is the filtering characteristics. Ensuring minimum adjacent channel effects is crucial for the system design. Hence, an adjacent channel simulation is carried out. Figures 3.11 shows the spectrum of transmitted power for three adjacent tools. The spectrum is taken at the output of each tool's transmitter. It can be noticed that all tools have an equal power. Figure 3.12 shows the spectrum of the transmitted signals before the optical node and after experiencing different coaxial path losses. The tool located further in the line experiences a higher loss. Figure 3.13 show the selected signal at the output of the IF filter. It can be noticed that signal to interference of 51 dBc is achieved, which is satisfactory for the system.

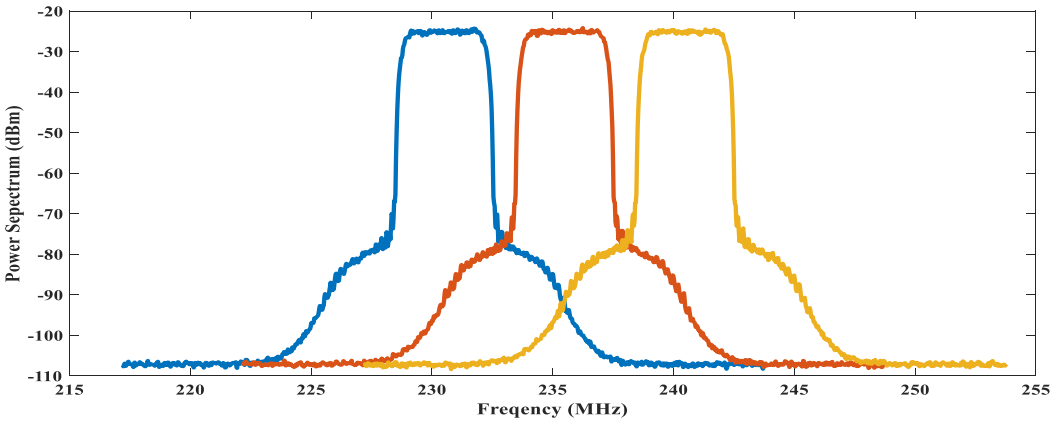


Figure 3.11: Signal power of three 64QAM signals at end of three transmitters and at three different channels.

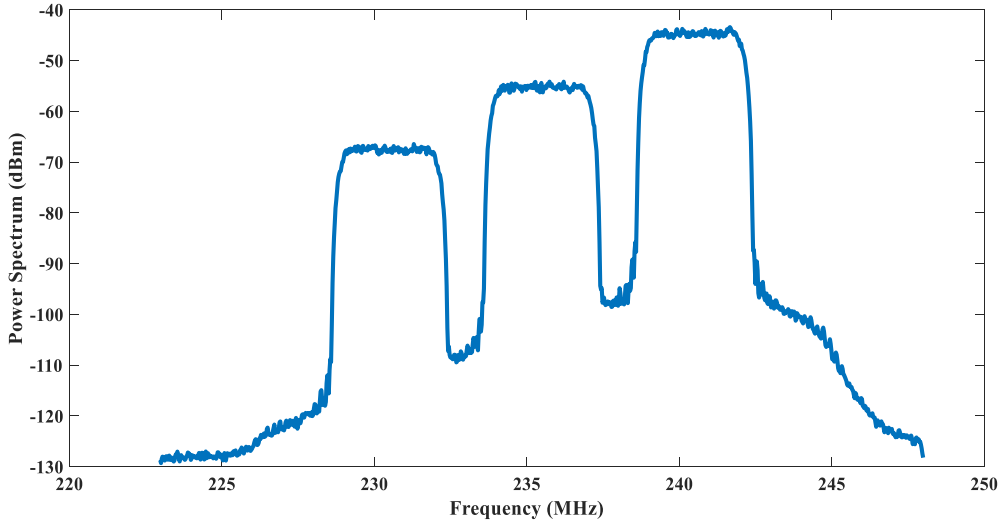


Figure 3.12: Signal power at the end of the coaxial cable and before the input of the RF to optical converter.

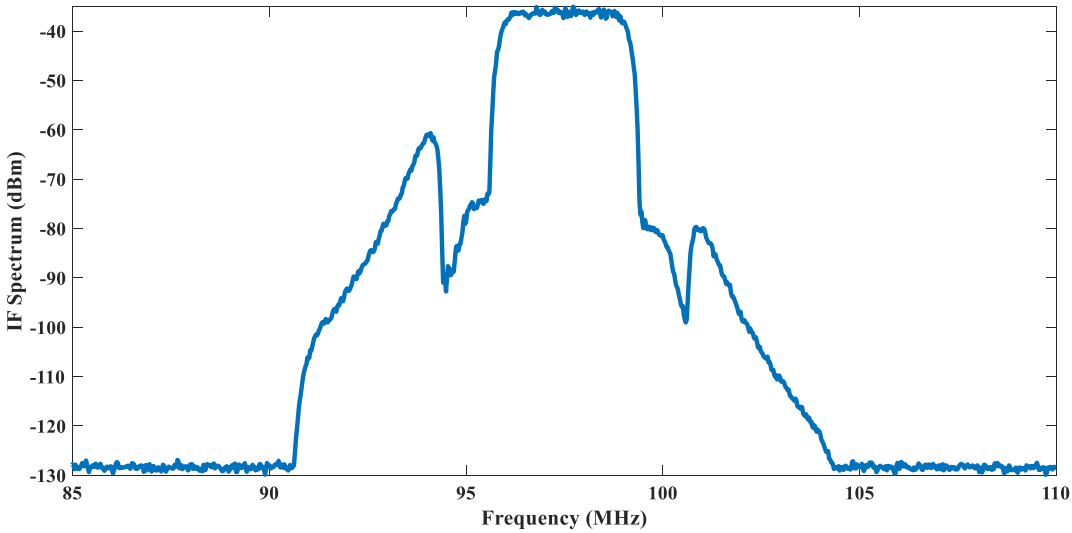


Figure 3.13: Signal power at the output of the IF filter.

The performance of the receiver used at downhole tools is also simulated. QPSK signals are sent from the surface to downhole and receiver front end along with QPSK decoder are used to recover the transmitted data. Figure 3.14 shows the EVM performance versus the received power. It can be noticed that the receiver has dynamic range of 90 dB.

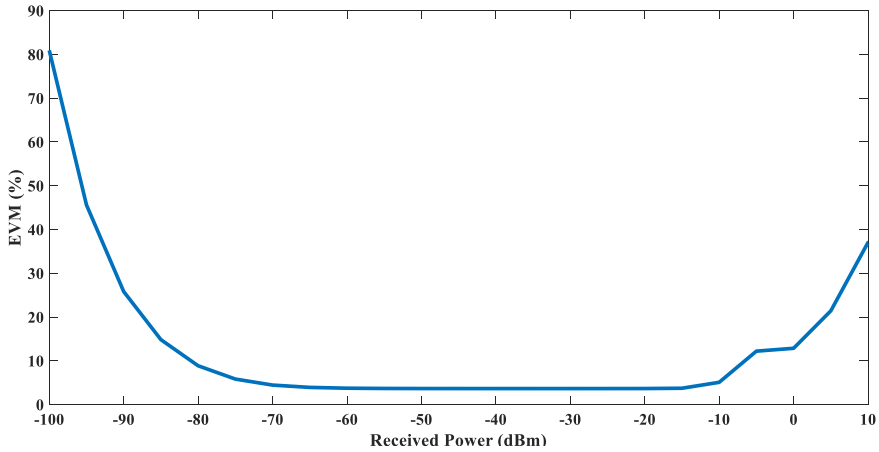


Figure 3.14: EVM versus the received power for QPSK at the receiver in downhole.

Appropriate parameters, compliant with high performance GaN technology, were applied throughout the simulation. The building block parameters were adjusted and their impact on the SCM system and RoF link were observed to ensure data rate of 20 Mbps using 64 QAM with BER of 10^{-6} (EVM<4%) is achieved. Simulation results indicate that building blocks with parameters shown in Table 3.1 should suffice for the complete 120 Mbps for six channels in uplink and 40 Mbps for six channels in downlink.

Table 3.1: Derived minimum specifications for the RF transceiver's building blocks.

Component	Frequency (MHz)	Gain (dB)	NF/PN (dB/dBc)	OP1dB (dBm)
LNA	228.5 ~256.5	20.0	3	10
Image Filter	228.5 ~256.5	-5.0	5	-
Down-Con Mixer	228.5 ~256.5	7	10	12
VCO + Buffer	328 ~353	-	-135 dBc @1 MHz offset	0 (Pout)
Power Amplifier	263.5 ~291.5	18	-	+16
UP-Con Mixer	263.5 ~291.5	-7.1	7.1	- 1
IF Filter	97.5 &62.5	-8	8	-

3.7 Chapter Summary

A downhole communication system architecture was proposed. Then, a characterization for the channel employed in downhole was presented. Next, superheterodyne transceiver architecture was presented. Based on the channel characterization and the transceiver architecture, the frequency planning and allocations for the transmit and receive paths were introduced. Subsequently, a link budget calculation to find the minimum specification for the RF building blocks was performed. After obtaining the initial specs of the transceiver building block, the downhole communication system was implemented in AWR simulation tool to verify the performance. Then, the components specs were optimized to provide a data rate of 20 Mbps per tool with BER of less than 10^{-6}. The total number of tools included in the design was six. Then, the simulation results with optimized specs were presented. Finally, a summary of the minimum specs for the RF building blocks was presented. This system provides a full duplex communication with data rate of 20 Mbps per tool for up to six tools with BER less than 10^{-6}.

Chapter 4 Device Characterization, and Modeling

In the previous chapter, the specifications of the transceiver building blocks are derived. The primary challenge of the proposed design lies in the temperature limitations of available commercial off-the-shelf (COTS) active and passive devices. This chapter presents the technology options for implementing the transceiver's building blocks to operate reliably at high temperatures. Next, the chapter covers device characterizations. These characterizations include for the first time the DC and RF measurements for the Gallium Nitride (GaN) high electron mobility transistor (HEMT) device at temperatures up to 250 ^{o}C. The purpose of these characterizations is to proof that the devices will operate at high temperatures and give more insight of how temperature impacts the device performance. Furthermore, the small signal characterizations are adopted as models and used in the simulation to design the building blocks of the transceiver. Lastly, the chapter introduces an improved analytic model for the drain to source resistance (R_{DS}). This model predicts accurately the performance of R_{DS} at temperatures up to 250 ^{o}C. This model will be used in next chapter to design and analyze the performance of the passive mixer at high temperatures.

4.1 Technology Option for High Temperature

The primary challenge of the proposed design lies in the temperature limitations of available commercial off-the-shelf (COTS) active and passive devices. The most critical consideration is the active devices. Typical bulk silicon (Si) CMOS technologies are rated with maximum operating temperatures of less than 150 °C [50]. The main limitation is that Si suffers from high leakage currents as temperature increases and these leakage currents cause latch up [51]. Adding an insulator to Si substrate helps to extend the operating temperature above the 150 °C [52],[53]. Wide bandgap based power transistors, on the other hand, offer high operating temperatures and low total thermal resistances, [54]-[4]. Silicon Carbide (SiC) can reach high junction temperatures [4]-[56], but due to the low transition frequencies f_T of SiC, it is mostly applied for power electronic and low frequency applications. GaN HEMT offers both high temperature and high frequency capabilities and is the most promising technology for the target application [56]-[57]. Further, it is thermally

robust and can have very low noise figure (NF), while achieving high gain and high linearity. Figure 4.1 shows polygon diagram summarizing a comparison of main semiconductor technologies for high-power RF transistors which are Si, GaAs, SiC and GaN [57][58][59].

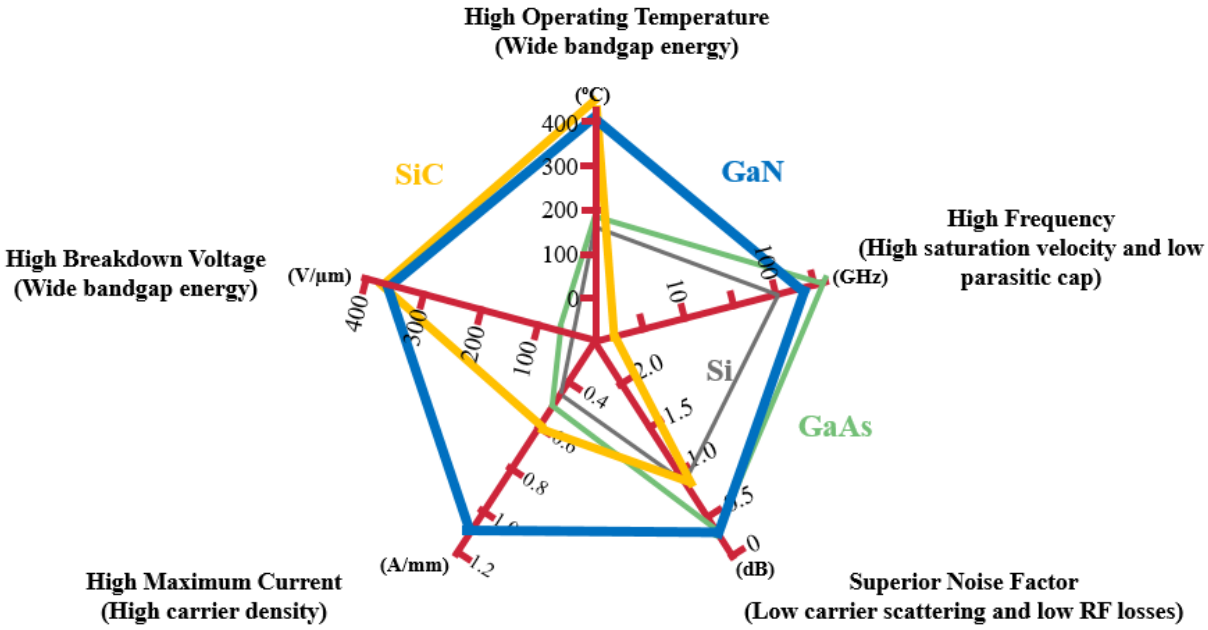


Figure 4.1: Polygon chart shows a summary of Si, GaAs, SiC and GaN materials. SiC is capable of operating at high temperature and GaN is capable of operating at high temperature and high frequency.

4.2 Qorvo GaN HEMT

The active devices selected to implement the transceiver building blocks are Qorvo GaN, namely T2G6000528-Q3 packaged 0.25µ GaN on SiC HEMT (0528-Q3) with pill package [60] and T2G6003028-FL GaN on SiC HEMT (3028-FL) with flange package [61]. Figure 4.2 shows photograph of both packaged transistors. These devices are mainly targeted for high power applications and have the maximum junction temperature, T_J of 275 °C, which is considered the highest among all the available COTS GaN transistors. Furthermore, these transistors have a reasonably low thermal resistance, R_θ of 12.4 °C/W for 0528-Q3 type and 3.82 °C/W for 3028-FL type. Moreover, the Qorvo GaN HEMT transistors have median lifetime expectancy of 10,000 hours at T_J of 275 °C. Figure 4.3 shows the median lifetime expectancy against the channel temperature for both transistor types.

Figure 4.2: Packaged Qorvo (previously TriQuint) GaN transistors selected for our design [60]-[61].

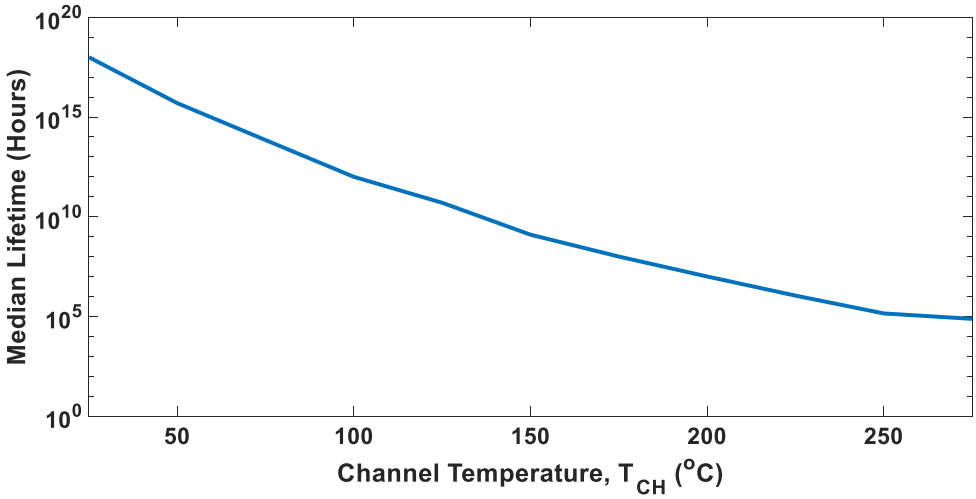


Figure 4.3: Median lifetime expectancy versus channel temperature for Qorvo GaN HEMT devices [28].

4.3 Previous Works on Temperature Impact to GaN and GaN Models

The intended application for the Qorvo GaN HEMT devices is high power RF amplifiers, and the datasheets provided by the manufacturer have characterizations only at V_{ds}=28 V and I_d =200 mA at room temperature and at 85 ^oC. The model provided by Modelithics, Inc works only up to 85 ^oC. For this research, the specified temperature is above 230 °C. Therefore, new device characterizations and modeling are needed at a wide temperature range and at lower drain voltages. However, in this section the state-of-the-art research of high temperature characterizations and modelling of GaN HEMT are reviewed.

Several papers have reported characterization and modelling of GaN HEMT on SiC [62]-[68], and few has investigated the temperature impact on GaN HEMT devices [69]-[72]. Lee et al presented in [64] a large signal model for HEMTs on SiC substrate to model self-heating effects. The approach proposed in their work is to modify the cubic nonlinear model developed by Curtice and Ettenber [73]. Curtice model was originally proposed for GaAs FET, where device characteristics were generated empirically. Such modeling approach have many parameters and complex techniques need to be used to extract these parameters. Angelov et al presented in [65] and [66] a simpler model that also offers improved accuracy over Curtic model in the linear and saturation regions. In this model cubic power series presented in Curtice model replaced by a hyperbolic tangent function that describes the gate voltage dependencies and its derivatives well. The simplified the drain to source current of GaN transistor can be best described as follows:

$$I_{ds} = I_{pk0}\left(1 + \tanh\left(p\left(V_{gs} - V_{pk}\right)\right)\right) \times \tanh(\alpha V_{ds}) \times (1 + \lambda V_{ds}) \quad (4.1)$$

where I_{pk0} is the drain current at the maximum transconductance and *p* is polynomial coefficient for channel current. V_{pk} is the gate voltage for maximum transconductance. λ is the channel length modulation parameter and α is the saturation voltage parameter. Wang et al in [34] presented improved model based on Angelov that includes self-heating and ambient temperature effects up to 175^oC. In their work, I_{pk0} and p were modeled as temperature dependent parameters. However, this model does not account for V_{pk} variation with temperature which is important when V_{gs} is close to V_{pk}. In this region, the V_{pk} play important role compare with *p*.

There are also some efforts found in the open literature to extract the small signal model parameters for GaN HEMT [67]-[68]. Most of these works adopt the famous equivalent circuit

model presented in [74] and shown in Figure 4.4.

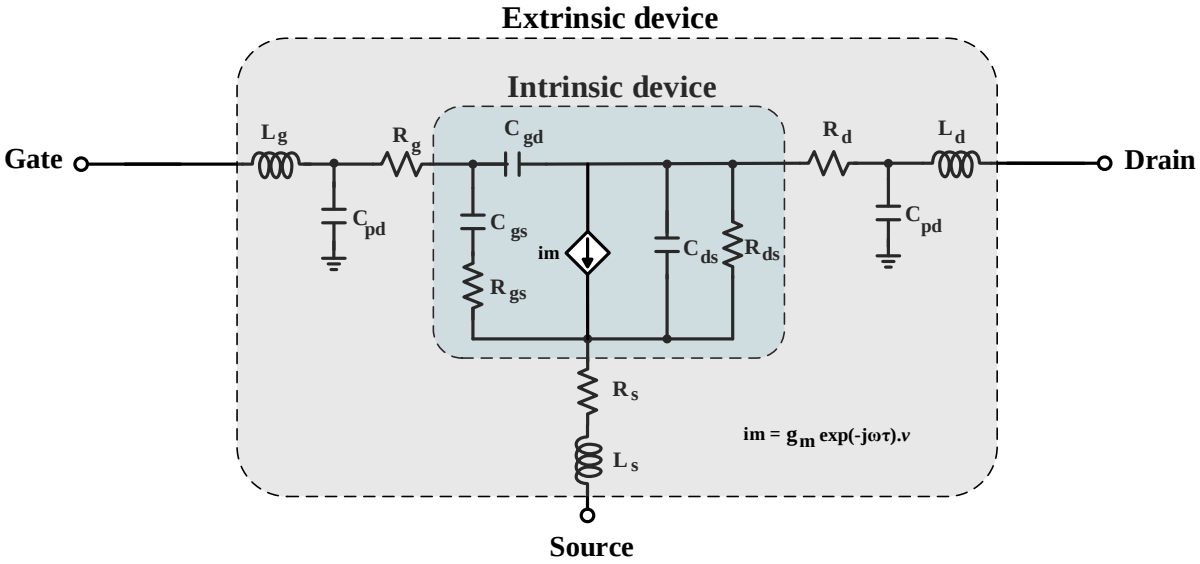


Figure 4.4: HEMT's equivalent circuit model showing the extrinsic and intrinsic parameters [74].

Recent works published in [71]-[72] studied the temperature impact on small signal parameters of GaN devices. In [71], an experimental analysis of temperature effects on a small signal equivalent circuit of GaN HEMT is presented. The maximum temperature that is considered for the experiment is 80 ºC and the work studied the effects at one biasing point which is V_{DS}=19.5 V and V_{GS}=-2 V for 0.7 µm AlGaN/GaN HEMT on SiC. In their experiment, it is found that the g_m slightly decreases with temperature and the parasitic capacitances are almost independent of temperature. In [72], characterizations and modeling of small signal equivalent circuit at temperatures up to 150 °C are presented. The experiment is also conducted on 0.15µm AlGaN/GaN HEMT on SiC at one biasing point which is V_{DS} = 15 V and V_{GS} = -4.8 V. Their results show that I_D, g_m, and C_{GS} decrease as temperature increases, while C_{DS} and C_{GD} increase with temperature. Both of previous works are conducted at one bias point and in all of the aforementioned work, the maximum ambient temperature that characterization or modeling carried at is below 175 °C.

In this work, characterizations of GaN HEMT at temperatures up to 250 °C and at different biasing conditions are conducted. In this characterization the impact of temperature on drain current, leakage currents, transconductance, S-parameters and drain-source resistance are emphasized. Improved high temperature models for R_{DS} that include the temperature effect of V_{pk} are included. By including the temperature effects on V_{pk}, the accuracy of the model at high

temperatures is improved, particularly when V_{gs} is close to V_{pk} and this was verified by the analysis and the performance of the resistive mixer presented in next Chapter. Furthermore, the existence of zero temperature coefficient (ZTC) spots in the drain current and transconductance of the GaN HEMT are highlighted.

4.4 High Temperature Characterizations Setup

The intended application for the Qorvo GaN HEMT devices is high power RF amplifiers, and the datasheets provided by the manufacturer have characterizations at V_{ds}=28 V and I_d =200 mA at room temperature and at 85 ^{o}C. As the devices should operate at lower drain voltages and at ambient temperatures up to 250 °C, new device characterizations and modeling are needed at a wide temperature range and at lower drain voltages. We performed device characterizations from room temperature to 250 °C. Then, we developed large and small signal models for which are used to estimate the performance of the building blocks at a wide temperature range.

Figure 4.5 shows the pulsed current (I) –voltage (V) characterization setup at a wide temperature range. The 0528-Q3 transistor is mounted on RO4003C PCB using a high temperature solders. Rogers 4003C board was selected due to insensitivity of its relative dielectric constant with temperature and negligible expansion of the board with temperature. The board is capable of operating at temperatures of greater than 280°C. The solder was selected based on melting point. Indalloy #151 solder paste offers a melting point of 296°C, and exhibits very low resistivity, so it was used to assemble the test fixture. Then, the test board is placed inside the furnace and connected to Diva D265 dynamic IV analyzer using special high temperature coaxial cables and connecters are used for the measurements [48]. The gate of the transistor is connected to the gate port of the Diva Analyzer and the drain of the transistor is connected to the drain port of the analyzer. The source of the transistor is grounded though screws. Diva analyzer allows for simultaneous pulsing of the gate and drain with pulse widths of 200 ns to 1 mS. The averaging is adjusted 128 samples with pulse length of 200 ns. The pulse separation is 0.5 ms. The bias point is adjusted to V_{DD} = 4 V and V_{GS}= -2.5 V. Next, the maximum V_{DD} is set to 10 V with step size of 0.1 V. The V_{GS} is swept from -3 V to -1 V in step of 0.05 V.

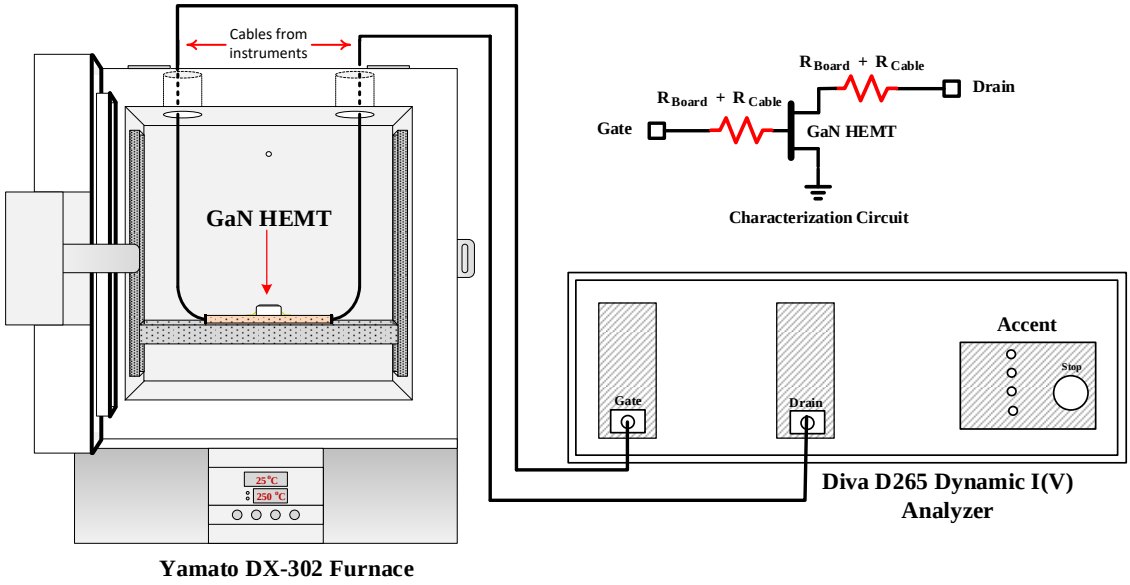


Figure 4.5: Test setup for characterizing the IV relationship of the GaN HEMT (0528-Q3) at a wide temperature range.

Figure 4.6 shows the high temperature S-parameters characterization set up. Rohde & Schwarz ZVL67 network analyzer is used to measure the s-parameters. External bias tees used at the ports to allow for the necessary biasing to the tested device. Calibration is performed up to the red lines showed in the figure to remove the effects of the cable, bias tees, board and SMA connector on the measurements. The parasitic inductance of the screws connected to the source of the transistor is de-embedded from the S-parameters measurements.

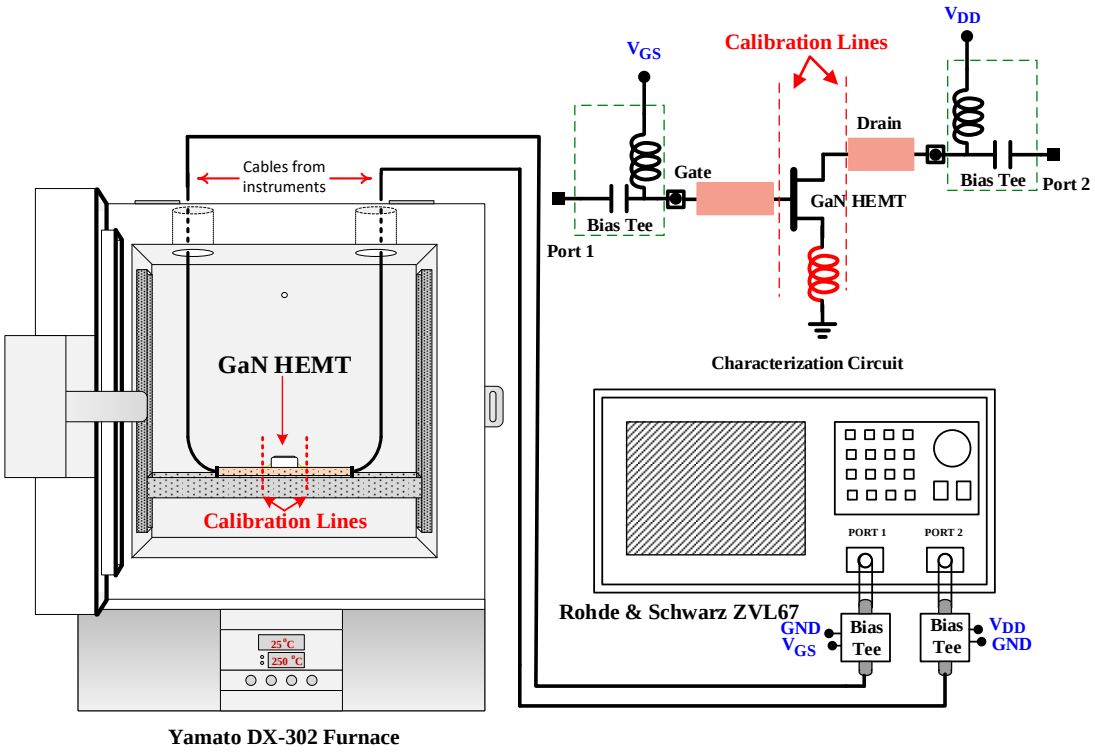


Figure 4.6: Test setup for characterizing the S-parameters and small signal parameters of the GaN HEMT (0528-Q3) at a wide temperature range. The characteristic impedance, $z_{0,}$ is 50 Ω.

4.4.1 Effects of temperature on the drain current

First, the 0528-Q3 GaN transistor is characterized at room temperature. Figure 4.7 shows the measured IV curves for the GaN HEMT device at room temperature. The maximum power consumption is set to 3 W. The maximum current is measured in this setup is 900 mA. It can be seen that the saturation region starts as low as V_{DS}= 1V and V_{GS} =-2.5 V with a minimum current of 15 mA.

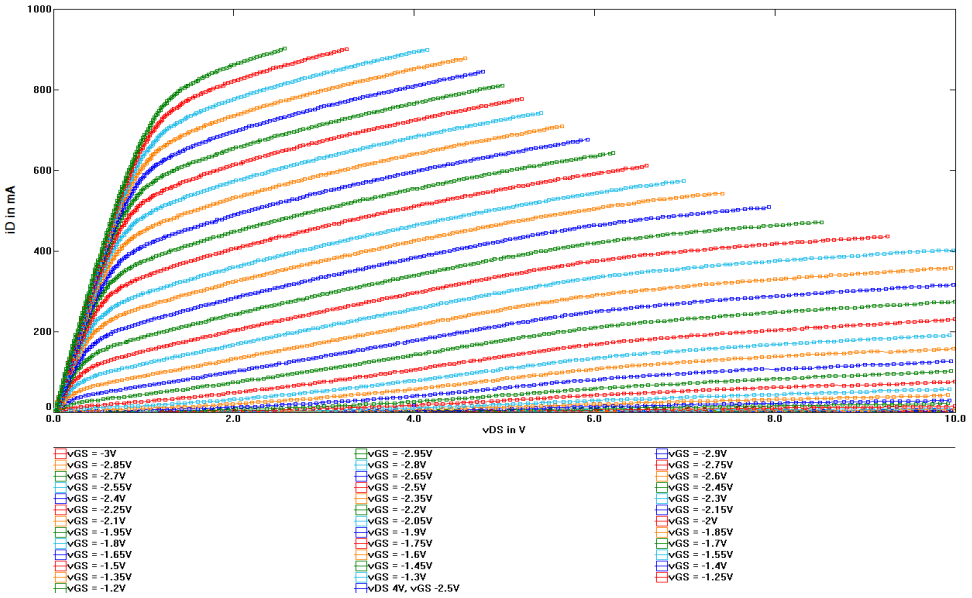


Figure 4.7: Drain current (I_D) characteristics versus drain-source voltage (V_{DS}) with gate-source voltage (V_{GS}) is swept from -3 V to -1 V in step of 0.05 V at room temperature.

Next, the furnace temperature is gradually elevated up to 250 ^oC and IV curves measured at 100 ^oC, 150 ^oC, 200 ^oC and 250 ^oC. Figure 4.8 and 4.9 show the I_D versus V_{GS} at different temperatures and at drain voltage of 0.5 V and 5 V, respectively. It can be noticed at both figures that the current at a specific V_{GS} is independent of temperature, called zero temperature coefficient (ZTC) point. It occurs due to the fact that the decrease in threshold voltage with temperature compensates the decrease in the electron mobility with temperature and this occurs only at a specific V_{GSZTC}. At a gate voltage greater than V_{GSZTC}, the drain current decreases with temperature and this is mainly due to decrease in mobility since the threshold voltage has negligible impact on V_{GS}. On the other hand, at a gate voltage smaller than V_{GSZTC}, the V_{GS} becomes comparable with threshold voltages whose temperature effect dominates the current variations. Therefore, as temperature increases, I_D increases at $V_{GS} < V_{GSZTC}$.

Furthermore, it can be noticed that at V_{DD} =0.5 V (Figure 4.8), the $V_{GSZTC} \approx$ -1.5 V and at V_{DD} =5 V (Figure 4.9), $V_{GSZTC} \approx$ -2.2 V. This indicates that as V_{DD} increases the V_{GSZTC} decreases following the behavior of threshold voltage, which it also decreases. Also, another important observation is that at V_{GS} =-3.0 V, the current stays zero at all temperatures and also at V_{GSZTC} the current stays the same at all temperature. This observation leads to conclude that the leakage currents for the device are negligible at temperatures up to 250 ^oC. This can be observed from both Figures 4.8 and 4.9.

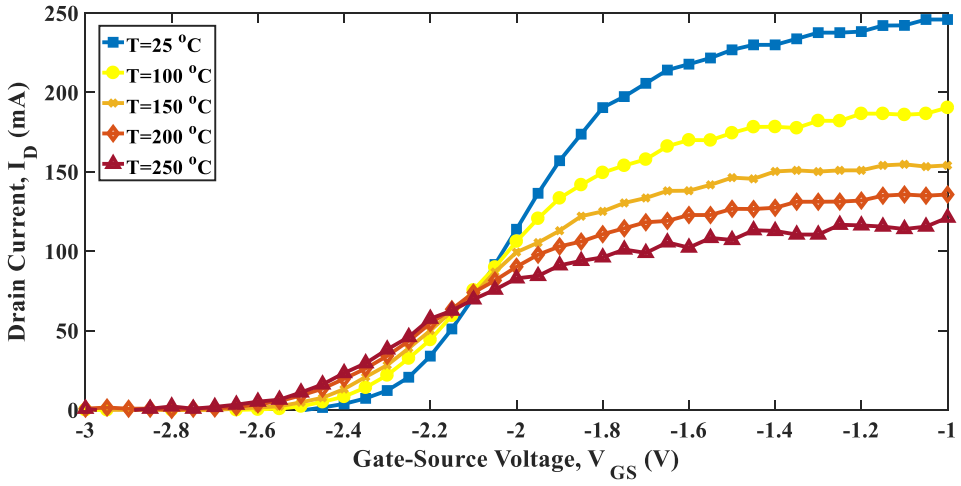


Figure 4.8: Drain current characteristics versus gate-source voltage at different temperatures and at V_{DD}=0.5V.

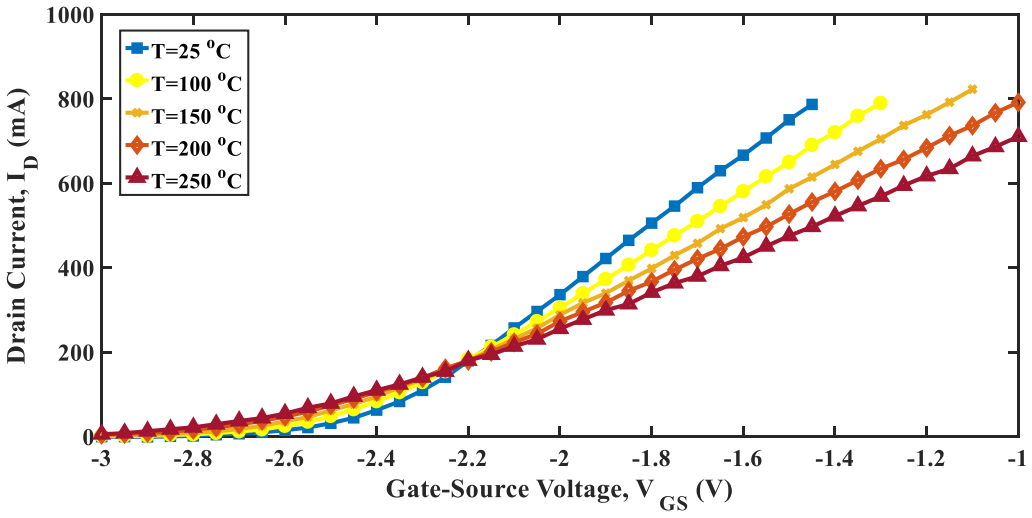


Figure 4.9: Drain current characteristics versus gate-source voltage at different temperatures and at V_{DD}=5 V.

4.4.2 Effect of temperature on transconductance

The transconductance (g_m) of the transistor can be extracted from either IV characteristics or the S-parameters. In our characterization, the g_m is extracted from the measured pulsed IV characteristics shown in Figures 4.8 and 4.9 using:

$$g_m = \frac{\partial I_d}{\partial V_{GS}}\Big|_{V_{DS}=C} \tag{4.2}$$

where C is constant and it is equal 0.5 V and 5 V in this characterization.

Figure 4.10 and 4.11 show the g_m versus V_{gs} at V_{DS} = 0.5 V and 5 V, respectively and at

temperatures up to 250 ^{o}C. It can be noticed that a zero temperature coefficient (ZTC) spot is also exist in the transconductance characteristics. However, it occurs at V_{GS} lower than the V_{GSZTC} presented in the drain current characteristics. For example, the ZTC for g_m occurs at V_{GS}=-2.3 V and -2.45 V at V_{DS} =0.5 V and 5 V, respectively while the ZTC for I_D occurs at V_{GS}=-1.5 V and -2.2 at V_{DS} =0.5 V and 5 V, respectively. Therefore, ZTC cannot happen for the drain current and transconducatce at the same time.

Following the drain characteristics, the g_m also decreases with temperature at a gate voltage greater than $(V_{GSZTC})_{gm}$, the g_m decrease is mainly due to decrease in mobility since the threshold voltage has negligible impact on V_{GS}. At a gate voltage smaller than V_{GSZTC}, the g_m increases with temperature and this is because V_{GS} is comparable with threshold voltages whose temperature effect dominates the transconductance variations. Moreover, it can be noticed the as V_{DS} increases the g_m also increases and the V_{GS} for ZTC g_m decreases.

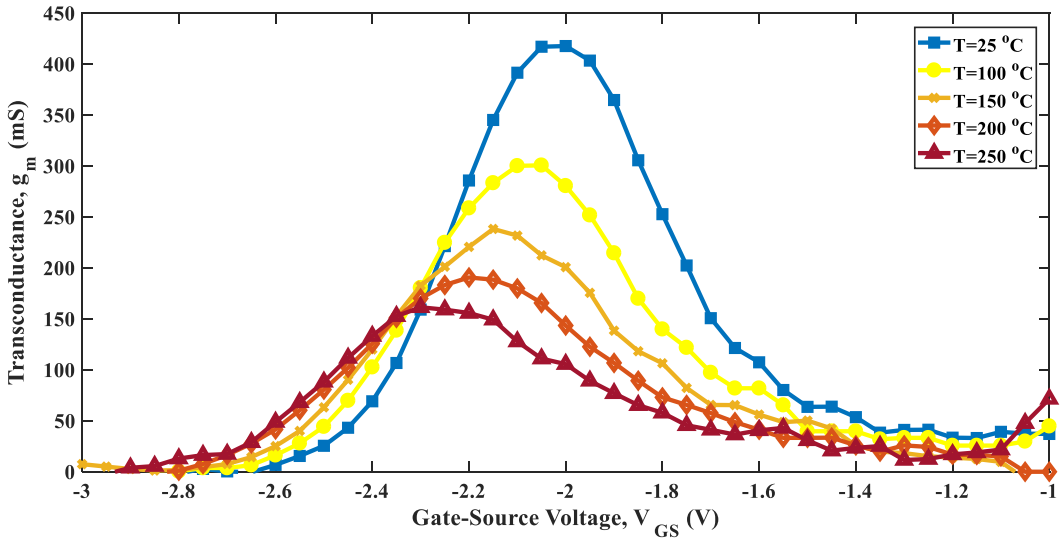


Figure 4.10: Transconductance characteristics versus gate-source voltage, V_{GS}, at different temperatures and at V_{DD}=0.5 V.

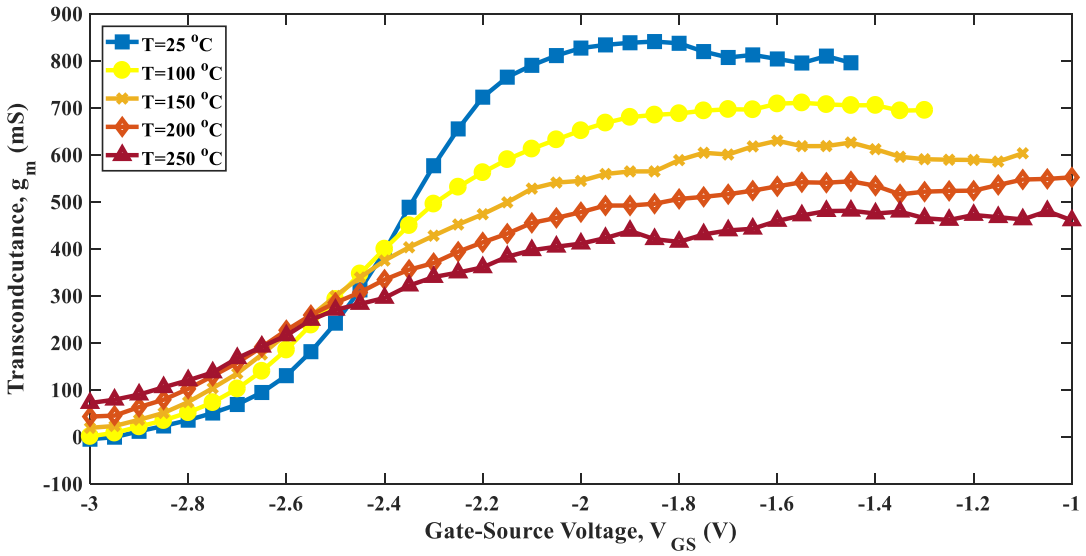


Figure 4.11: Transconductance characteristics versus gate-source voltage, V_{GS}, at different temperatures and at V_{DD}=5 V.

4.4.3 Effect of temperature on S-parameters

Next, the impact of temperature on the S-parameters is studied. Using the test setup shown in Figure 4.5, the S-parameters at a wide temperature range is measured. Figure 4.12 shows the measured S_{11} and S_{22} at V_{DS} = 5 V and V_{GS} = -2.5 V and for 25 ºC, 150 ºC, and 250 ºC. The black dots mark the frequency of interest which is 250 MHz. There is slight change with temperature for the S_{11}. For example, the input impedance at frequency of 250 MHz is 7.306-j 63.944 Ω at 25 ºC, 7.236-j 61.828 Ω at 150.0 ºC and 6.546-j65.191Ω at 250 ºC. It can be noticed that the real part of the impedance slightly decreases with temperature at the specified frequency while it fluctuates the imaginary part up and down with temperature. The main parameters that can affect the input impedance and in turns the S_{11} can be understood clearly from the following equations.

Let us assume the $Y_{12} \approx 0$, then we can write [75]:

$$S_{11} \approx \frac{(1-Y_{11}Z_s^*)}{(1+Y_{11}Z_s)} \tag{4.3}$$

Where Z_s is the source impedance and it is 50 Ω. The Y_{11} for the transistor at frequencies less than 5 GHz can be expressed as [74]:

$$Y_{11} \approx R_i C_{GS}^2 \omega^2 + j\omega(C_{GS} + C_{GD}) \tag{4.4}$$

From eq 4.4 the main parameter that is temperature dependent is C_{GS} since the R_i and C_{GD} are very small. The other important observation is that the temperature variation is frequency dependent in which at higher frequencies, the S_{11} has large variations with temperature.

For S_{22}, on the other hand, the variation with temperature is quite large. It can be seen from Figure 4.12 that as temperature increases the output impedance decreases at the frequency of interest. For example, the output impedance at frequency of 250 MHz is 41.072-j 23.234 Ω at 25 ^{o}C, 34.486-j 14.426 Ω at 150.0 ^{o}C and 33.140-j12.245Ω at 250.0 ^{o}C. The main parameters that can affect the output impedance and in turns the S_{22} can be understood clearly from the following equations.

Again, let us assume the $Y_{12} \approx 0$, then we can write [75]:

$$S_{22} \approx \frac{(1-Y_{22}Z_L^*)}{(1+Y_{22}Z_L)} \tag{4.5}$$

where Z_L is the load impedance and it is 50 Ω. The Y_{22} for the transistor can be expressed as:

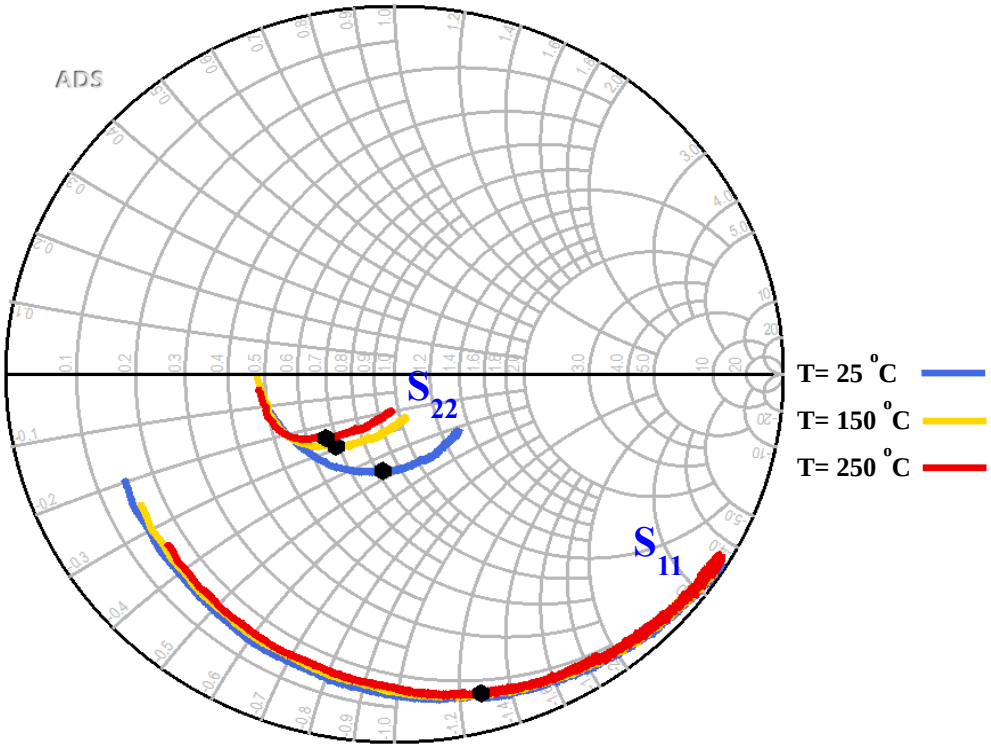


Figure 4.12: S_{11} and S_{22} at V_{DS}=5 V, V_{GS} =-2.5 V and frequency sweep from 100-700 MHz.

$$Y_{22} = g_d + j\omega(C_{DS} + C_{GD}) \tag{4.6}$$

where g_d is channel conductance and it is equal to 1/ R_{CH}.

From eq 4.6 the main parameter that is temperature dependent and affects the output impedance and S_{22} is g_d or the R_{DS}. The C_{DS} and C_{GD} are also temperature dependent but they only have a significant impact at high frequencies. The impact of temperature on R_{DS} will be further

investigated in Section 4.4.4.

Figure 4.13 shows the measured S_{21} which is the power gain of the transistor at V_{DS} = 5V and V_{GS} = -2.5 V. It can be noticed that the gain is almost constant up to 150 °C and then drops by 1 dB at 250 °C. The S_{21} can be expressed as the following:

Again, let us assume the $Y_{12} \approx 0$, and $Z_s = Z_L = 50\ \Omega$, then we can write [75]:

$$S_{21} \approx \frac{-2Y_{21}Z_S}{(1+Y_{11}Z_S)(1+Y_{22}Z_L)} \tag{4.7}$$

where [74]

$$Y_{21} = g_m - j\omega\left(C_{GD} + g_m(R_i C_{GS} + \tau)\right) \tag{4.8}$$

From eq (4.7) & (4.8), it can be understood that S_{21} mainly depends on the matching of both ports and g_m. As we can see from Figure 4.11, the g_m increases slightly with temperature at this biasing point (V_{GS}=-2.5 V) but the increase of R_{DS} and C_{GS} with temperature dominates at 250 °C and causes the gain to drop by 1 dB.

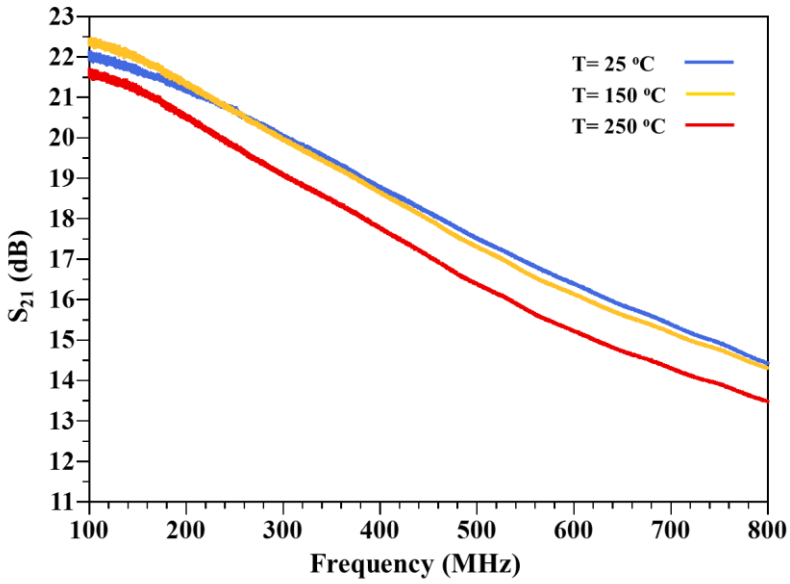


Figure 4.13: S_{21} versus the frequency at V_{DS}=5 V, V_{GS} =-2.5 V.

4.4.4 Effect of temperature on drain to source resistance

A simplified equivalent circuit for Qorvo GaN HEMT device, T2G6000528-Q3, with zero drain bias is shown in Figure 4.15. L_g, L_d, L_s, C_{pd}, R_g, R_d, and R_s are extrinsic parasitic components associated with the three transistor terminals. C_{gd}, C_{gs}, and C_{ds} are intrinsic parasitic capacitors that vary with the gate bias. R_{CH} is the channel resistance that depends on the gate voltage.

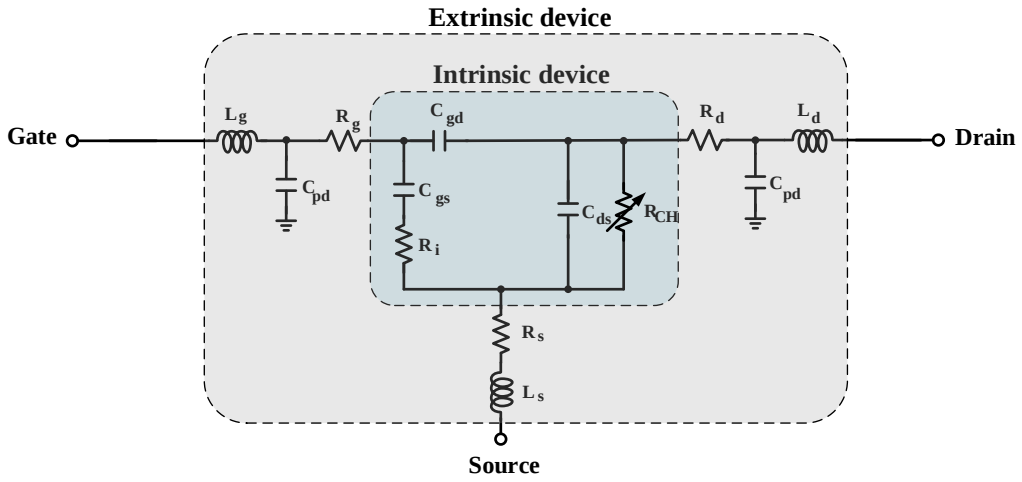


Figure 4.14: A simplified equivalent circuit model for a GaN HEMT device with zero drain bias.

The drain-to-source resistance, R_{DS} can be found using:

$$\boldsymbol{R_{DS} = R_d + R_s + R_{CH}} \quad (4.9)$$

R_d and R_s are equal to 0.84 Ω at room temperature and they are also temperature dependent. As V_{gs} increases from -3.5 V to -2 V, R_{ch} changes significantly from the off-state of around 5 KΩ to the on-state of around 2 Ω. Figure 4.16 shows the measured R_{DS} versus gate voltage at three different temperatures. It can be noticed that as temperature increases, R_{DS} (off- and on-states) increases for a given gate voltage. Also, the transition point from the off-state (high resistance) to the on-state (low resistance) shifts to the left, which mainly attributed to the decrease of the threshold voltage of the device with the temperature. The reflection coefficient seen at the drain port is sensitive to R_{DS}, and changes of R_{DS} implies that ambient temperature affects the reflection coefficient. To mitigate the temperature dependence of the threshold voltage and hence R_{DS}, the bias voltage of V_{DS} can be changed according to the temperature level, discussed in the next Chapter.

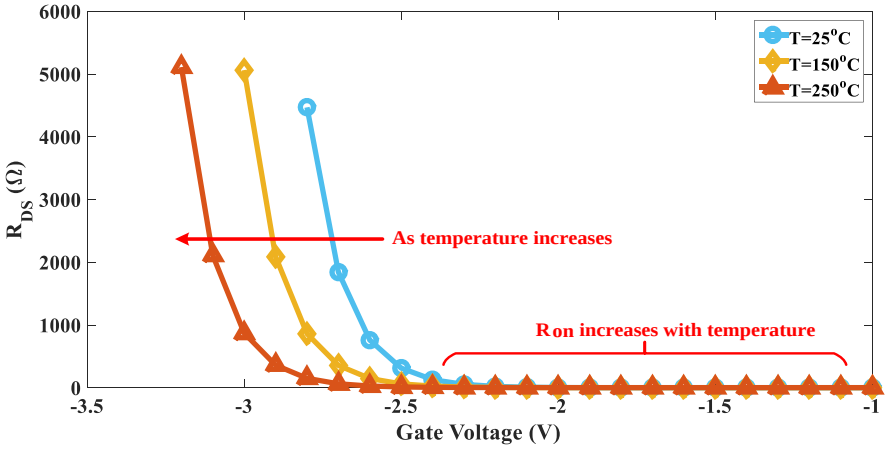


Figure 4.15: The measured R_{DS} versus the gate voltage at different temperatures.

4.4.5 GaN Process Variations

The characterization includes multiple devices to evaluate the intra-device variation. These devices are from different fabrication lines. Figure 4.17 shows the I_D versus V_{GS} for three devices at V_{DS} = 5 V. It can be seen when the V_{GS} is near the pinch off voltage the current variations are small and as V_{GS} increases, the variation in the I_D increases. For example, at V_{GS} =-2.3 the current variation between devices can be as large as 50 mA. These variations are mainly due to the process variation that affected the mobility and the threshold voltage of a particular device. Initial characterizations for the devices are recommended before designing a specific building block.

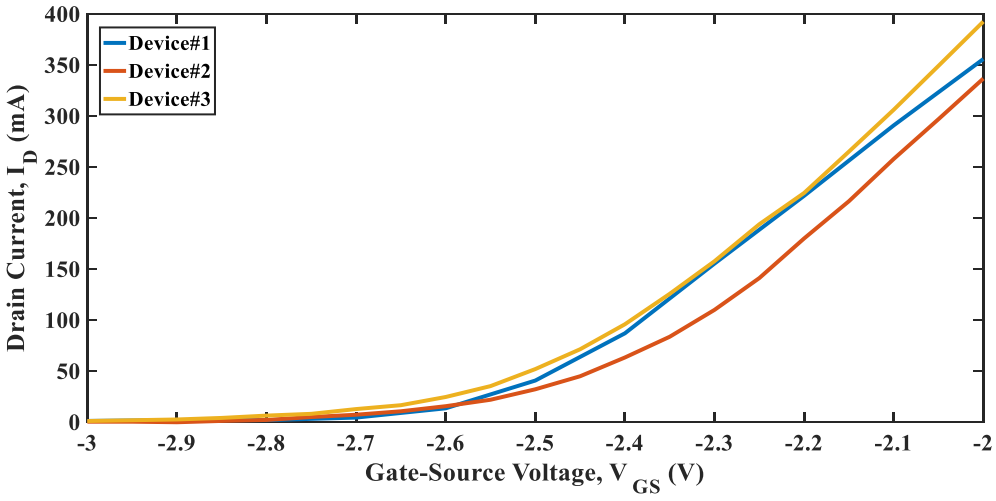


Figure 4.16: Drain current characteristics versus gate-source voltage for three devices at V_{DD}=5 V.

4.5 Improved High Temperature Model for the R_{DS} of GaN HEMT

There are few models of GaN HEMT that model the behavior of the transistor in the linear region (V_{DS} < 0.1V) for resistive mixer application at room temperature reported in [76]-[78] and none that has yet targeted the high temperature operation. Our approach is to provide an analytical model based on Angelov model for transistor in linear region that can be applicable to a resistive mixer design and analysis and predict the performance at high temperatures. For this purpose, modeling of R_{DS} of GaN HEMT is investigated.

The device in the linear region can be modeled using the equivalent circuit shown in Figure. 4.18. R_g, R_d, R_s, L_d, L_s, L_g, and C_p are extrinsic parasitic resistances, inductances and capacitance associated with the three transistor terminals and constant as gate voltage varies. C_{gd}, C_{gs}, and C_{ds} are internsic parasitic capacitors that vary with the gate bias. All of these parameters are extracted using cold FET method presented in [74].

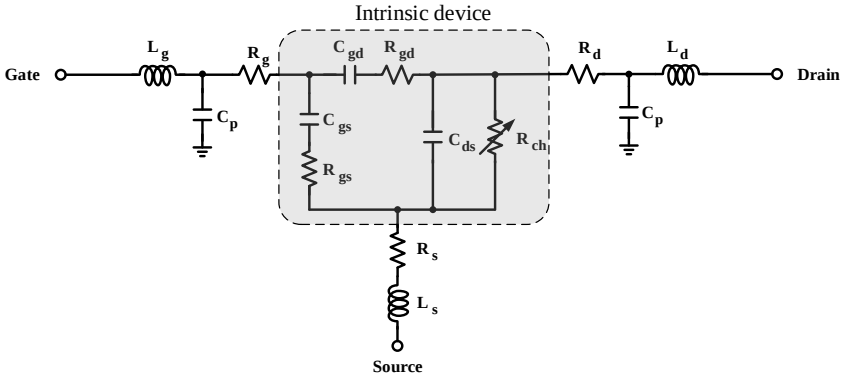


Figure 4.17: A simplified equivalnt circuit model for a GaN HEMT device in the linear region (zero drain bias).

R_{ch} is the channel resistance that depends on the gate voltage and the conversion loss is mainly attributed to it. Therefore, providing a correct model for the R_{ds} (= R_d + R_s + R_{ch}) will provide accurate prediction of CL of the mixer. In this section, model for drain to source channel resistance based on large signal Angelov model is provided.

We are interested in the model of the transistor in the linear region where V_{ds} is very small. Therefore, (4.1) can be rewritten as follows:

$$I_{ds} \approx I_{pk}\left(1+\tanh\left(p\left(V_{gs}-V_{pk}\right)\right)\right)\times \alpha V_{ds} \tag{4.10}$$

Drain to source resistance can be express as follows:

$$R_{ds} = \frac{V_{ds}}{I_{ds}} = \frac{1}{\alpha I_{pk}\left(1+\tanh\left(p\left(V_{gs}-V_{pk}\right)\right)\right)} \tag{4.11}$$

We performed device characterizations for Qorvo T2G6000528-Q3 packaged 0.25µm GaN on SiC HEMT [60] at wide temperature range starting from room temperature up to 250 °C. Then, we developed a model for drain-to-source resistance that depends on temperature based on the model in (4.11). For temperatures below 150°C, a first order polynomial with temperature of I_{pk}, p and V_{pk} provide good accuracy, However, as the temperature increases above 150°C, first order polynomial fails to accurately model the behavior of R_{ds}. To improve the accuracy above 150°C, I_{pk} and p are modeled as quadratic polynomials with temperature. Transistor parameters I_{pk}, p, and V_{pk} are temperature dependents, and their behaviors with temperature can be expressed as follows:

$$I_{pk} = I_{pk0} + \alpha_{I_1} T + \alpha_{I_2} T^2 \tag{4.12}$$

$$p = p_0 + \alpha_{p_1} T + \alpha_{p_2} T^2 \tag{4.13}$$

$$V_{pk} = V_{pk0} + \alpha_V T \tag{4.14}$$

where I_{pk0}, p_0, and V_{pk0} are the parameters at room temperature and α_{In}, α_{pn} and α_V are constants and their values are obtained using curve fitting and shown in Table 4.1. By inserting (4.12) through (4.14) into (4.11), we obtain:

$$R_{ds} = \frac{1}{\alpha\left(I_{pk0}+\alpha_{I_1}T+\alpha_{I_2}T^2\right)\left(1+\tanh\left(\left(p_0+\alpha_{p_1}T+\alpha_{p_2}T^2\right)\left(V_{gs}-V_{pk0}-\alpha_V T\right)\right)\right)} \tag{4.15}$$

Figure 4.19 shows the modeled and the measured R_{ds} versus gate-source voltage, V_{GS}, at a wide temperature range. It can be noticed that the model follows the measured R_{DS} very closely. This model will be used in the next chapter to analyze and design the resistive mixer at high temperature.

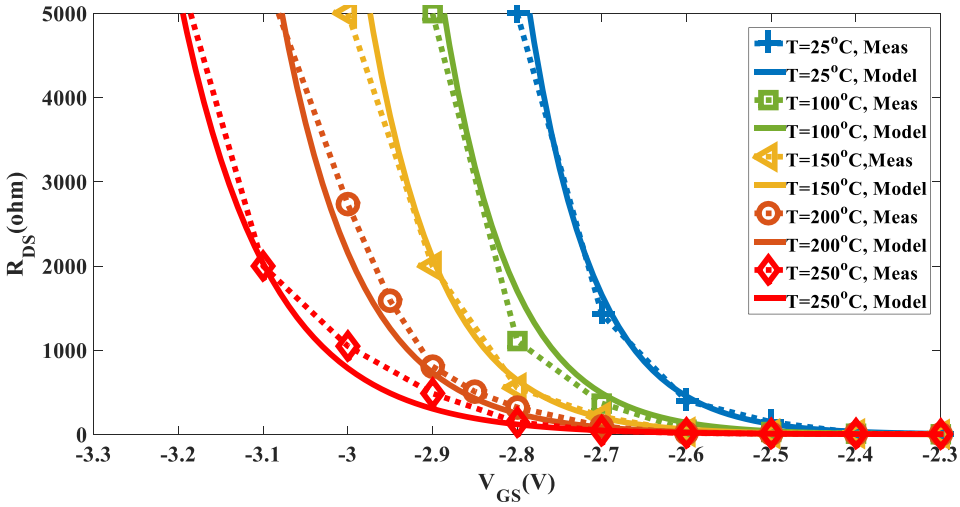


Figure 4.18: Measured and modeled R_{DS} versus gate voltage at different temperatures.

Table 4.1: Extracted parameters for the R_{DS} model.

Parameter	Value	Unit
I_{pk0}	176	mA
α_{I1}	-0.55	mA/C
α_{I2}	0.76	µA/C
p_0	6.47	V^{-1}
α_{p1}	0.68	mV^{-1}/C
α_{p2}	-30.0	$\mu V^{-1}/C$
α	3.68	V^{-1}
V_{pk0}	-2.082	V
α_V	1.247	mV/T

4.6 Chapter Summary

In this chapter, the technology option was investigated. Qorvo GaN HEMT technology was selected since it has highest junction temperature. This technology is intended for high power amplifiers. The high power dissipation can increase the junction temperature to 275 ^oC at room temperature. We used these transistors to design our building block at low power but at high temperature. These transistors are characterized and modeled only at temperatures less than 85 ^oC; hence, a new characterization at high temperature is needed. First, we reviewed the open literature to study the impact of temperature on GaN characteristics. Next, high temperature characterization setups were introduced. Then, we performed characterization on the Qorvo GaN HEMT devices at temperatures up to 250 ^oC. The temperature effects on drain current, transconductance, small signal parameters, gate-source capacitance, and drain resistance were highlighted. Finally, a high temperature model that predicts the behavior of R_{DS} at temperatures up to 250 ^oC was developed.

Chapter 5 Building Blocks Design and Analysis/Measurement Results

After characterizing, and modeling the devices at high temperatures, in this chapter, the design and analysis of the building blocks to meet the specifications of the transceiver at high temperature is carried out. Measurement results for the individual building block at a wide temperature range are presented. This chapter first presents design considerations for high temperature that included thermal analysis at room temperature and high temperature. Next, the chapter elaborates on passive mixer analysis and design at high temperatures. The proposed passive mixer is used as upconversion block for the transmitter. Then, active mixer design is proposed. The high temperature active mixer is adopted as downconversion stage in the receiver frond-end. Afterwards, the analysis and measured results of the low noise amplifier (LNA), signal generator (SG), power amplifier (PA), filters, and diplexer designs are presented. These later blocks are designed with cooperation of my teammates. Lastly, an adaptive biasing circuit for GaN HEMT based designs is proposed.

5.1 Design Considerations

5.2.1 Thermal Design and High Temperature Operation

GaN HEMT devices offers high power, high temperature and high frequency capabilities. Although they are thermally robust, thermal limitations of packages at different power dissipation and high temperature should also be considered. The relationship of the thermal effect is expressed as $T_A = T_J - R_\theta \times P_D$ [79]. The maximum ambient temperature (T_A) that a GaN transistor can operate at depends on the maximum junction temperature (T_J), the thermal resistors (R_θ) of the packaged device, PCB, soldering, vias, heatsink if used, and any other mechanical connection is used with packaged device, and the power dissipation of the device (P_D). T_J and R_θ are fixed device parameters, and hence P_D is the only parameter controllable by the designer. Therefore, a tradeoff between the power dissipation of the GaN device and maximum ambient operating temperature. It is necessary to ensure that material, mechanical connections, and P_D are set properly so that the

maximum T_J of the packaged device is below the maximum limit specified by the manufacturer which is 275 ^{o}C at all ambient temperatures.

In order to ensure thermal robustness at all operating ambient temperatures and identifying the maximum power limit that can GaN transistor consume to operate below the maximum junction temperature at elevated ambient temperature of 230.0 ^{o}C, thermal simulation using ANSYS Icepak is conducted. Icepak uses finite element analysis to find the temperature distribution and maximum junction temperature of an electronic design. The simulation allows to manually set the size and material properties of the components. Table 5.1 lists the size and material properties used to model the components which are taken from the datasheets [60],[80],[81], and [82].

Table 5.1: Size and the material properties used in ANSYS Icepak for thermal analysis.

Component	Size L×W×H (mm)	Material Property
Die (GaN)	1.2×1×0.15	Density:6100.0 kg/m^3 Specific Heat: 490.0 J/Kg-K Conductivity: 130.0 W/m-K
Substrate (SiC)	1.2×1×0.4	Density: 3210.0 kg/m^3 Specific Heat: 677.8 j/Kg-K Conductivity: 490.0 W/m-K
Die Attach	1.2×1×0.04	Density: 1900.0 Kg/cm^3 Specific Heat: 795.0 J/kg-K Conductivity: 2.5W/m-K
Package (Ceramic)	5.08×4.064×2.413	
PCB (RO4003C)	10×4.1×1.559 (attached to source) 20×4.1×1.559 (Connected to Gate/Drain)	Density: 1.79 g/cm^3 Specific Heat: 900.0 J/kg-K Conductivity: 0.71 W/m-K

Figure 5.1 shows a vertical cut of the packaged GaN mounted on Roger RO4003C PCB explaining the thermal stress due to self-heating of the packaged device at room temperature. The maximum junction temperature at dissipation power, P_{Diss} of 0.5 W is 36.63 ^{o} C at room temperature and it increases to 135 ^{o} C at P_{Diss} of 6.5 W. Figure 5.2 shows a cross section of the same packaged device with PCB at 250.0 ^{o} C. The maximum T_J at P_{Diss} of 0.5 W is 261.6 ^{o} C at 250.0 ^{o} C and it increases to 360 ^{o} C at P_{Diss} of 6.5 W which exceed the maximum T_J of 275 ^{o} C

specified by the manufacturer. Figure 5.3 shows the cross section of the packaged device with heat sink at 230.0 ^{o}C and P_{Diss} of 5.5 W. It can be noticed that the maximum T_J is 277 ^{o}C which is very close to the maximum T_J specified by the manufacturer. Therefore, for high ambient temperature, either P_{Diss} has to be low or heat sink has to be used. Figure 5.4 shows the maximum T_J versus P_{Diss} at 25 ^{o}C and 230 ^{o}C with and without heat sink. In our transceiver design, the power dissipation is limited to 0.5 W except for the PA where the P_{Diss} is around 5.5 W and heat sink is used.

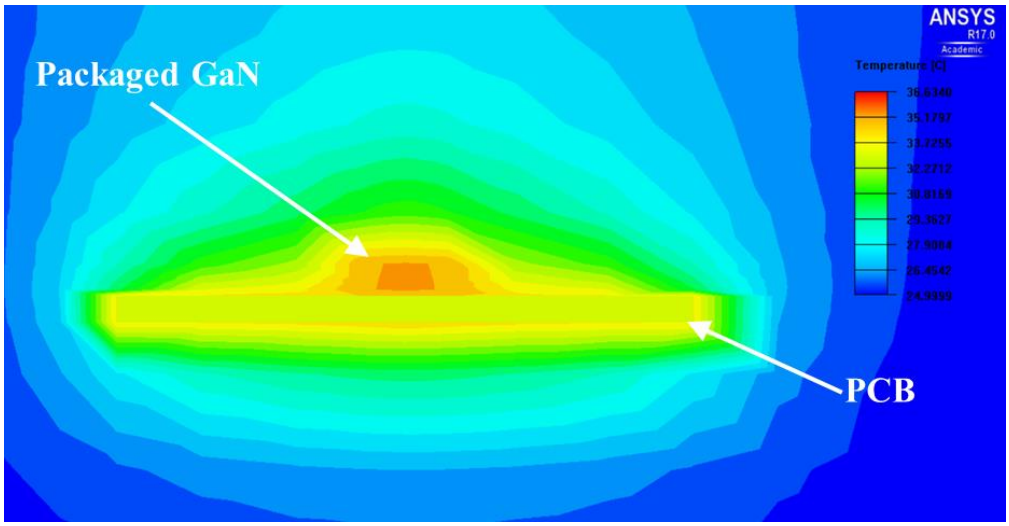


Figure 5.1: A vertical cross-section of the packaged GaN device with RO4003C PCB at P_{Diss}=0.5 and ambient temperature T_A= 25 ^{o}C.

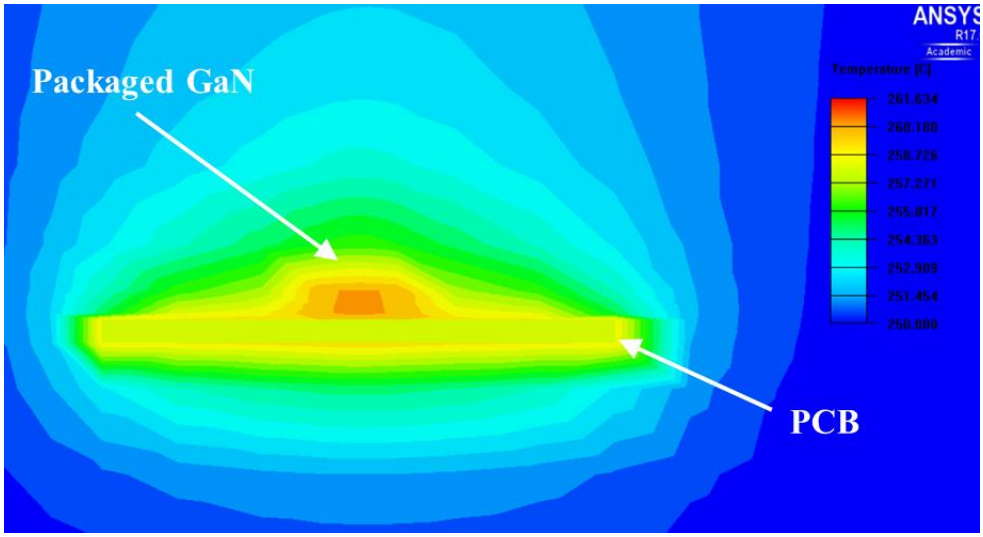


Figure 5.2: A vertical cross section of the packaged GaN device with RO4003C PCB at P_{Diss}=0.5 and ambient temperature T_A= 250 ^{o}C.

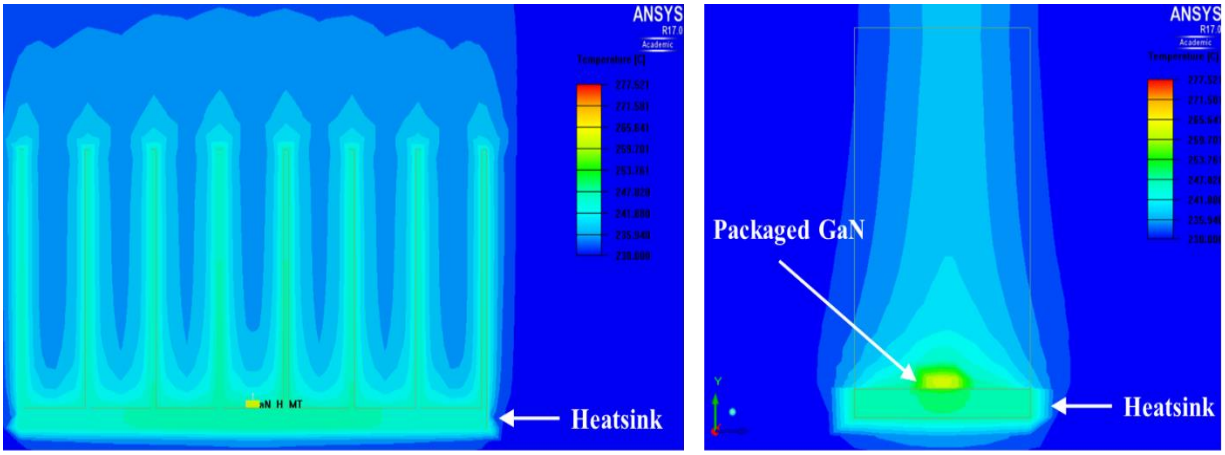


Figure 5.3: Temperature distribution at the packaged GaN device with heat sink at P_{Diss}=5.5 and ambient temperature T_A= 230 ^oC (Left) a side view (Right) a vertical cross section.

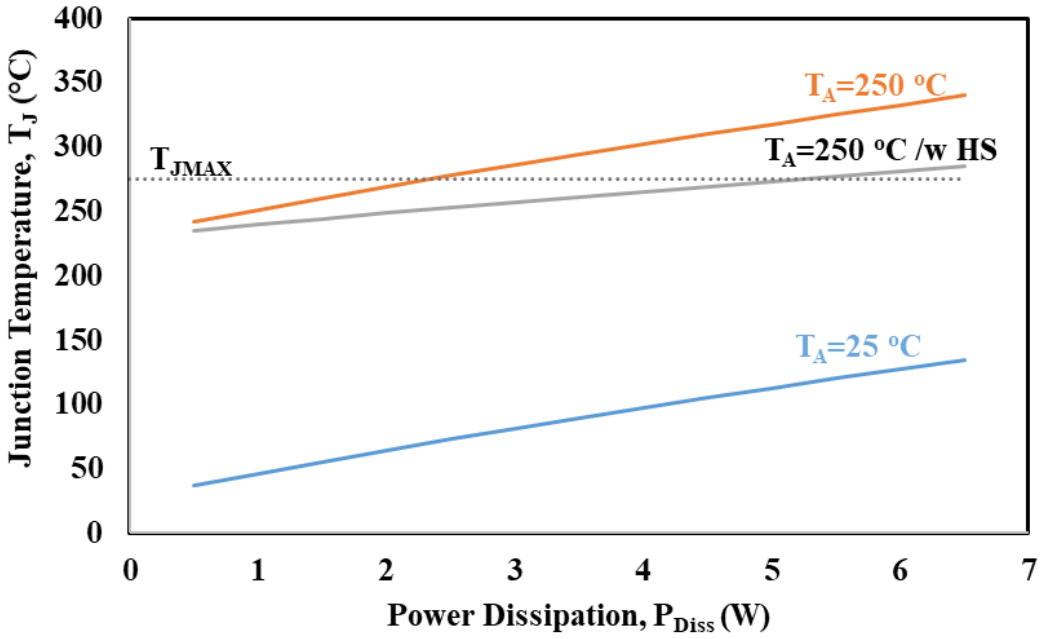


Figure 5.4: Maximum junction temperature versus power dissipation at room temperature, and 230 ^{o}C with and without heat sink.

5.2.1 High Temperature Design Considerations

Typical passive components often exhibit large variances over a wide temperature range. In order to reduce performance variations over temperature, it is desirable to use few passive components. In this regard, filters and matching networks of the mixer may be realized with

transmission and microstrip lines rather than lumped LC components. Some passive device values such as those of RF chokes (RFCs) and DC blocking capacitors are noncritical, and so those components can be used rather freely. Further, note that RFCs and DC blocking capacitors are not easily achievable with microstrip transmission lines.

Temperature variations of active and passive devices can shift the operating point of a transistor to cause performance degradations. One method to mitigate the problem is to adjust the bias point with temperature. All the design considerations mentioned above are adopted for the proposed RF building blocks.

5.2 High Temperature Resistive Passive Mixer

5.2.1 Existing Designs

There are several passive GaN mixer designs that operate at room temperature [76]-[78],[83]-[85] and few mixer designs operating at high temperatures [86]. Wong et al. in [86] investigated a GaN based diode mixer operable up to 250 ^{o}C. Their design suffers from a high conversion loss of 12.9 dB, large conversion loss variations of 4.35 dB with temperature, and the requirement for a high local oscillator (LO) power. Such shortcomings are typical for diode based mixers. In our transceiver design, a resistive mixer based topology is adopted, and the designed mixer can operate up to ambient temperature of 250 ^{o}C with low conversion loss, low temperature variation, and reasonable low LO power. Our results for the proposed high temperature mixer are reported in [87] and expanded in [88]. The proposed mixed is used as upconverting stage in the transmitter design.

5.2.2 Resistive mixer

Resistive mixers based on Field-Effect Transistors (FETs) offer inherently high linearity, good noise performance, and virtually no dc power dissipation. Another important advantage of FET-based passive mixers over their counterpart active mixers is that they are unconditionally stable. A resistive mixer topology is adopted for the proposed mixer design.

A typical resistive mixer topology is shown in Figure 5.5. The basic principle is to use the linear channel resistance as a mixing element. The LO signal applied at the gate switches the transistor on and off, which changes the drain-to-source resistance, R_{ds}, as well as the reflection

coefficient Γ(t) accordingly. The RF signal applied to the drain experiences the time-varying reflection coefficient and reflects a signal containing the IF.

The analysis of a resistive mixer at room temperature is reported in [89]. The analysis is performed based on the reflection coefficient as seen from the drain port. The underlying assumption is that all three mixer I/O ports are matched. It should be noted that R_{ds} changes as temperate changes, and so does the reflection coefficient. The effects of temperature are presented in next section.

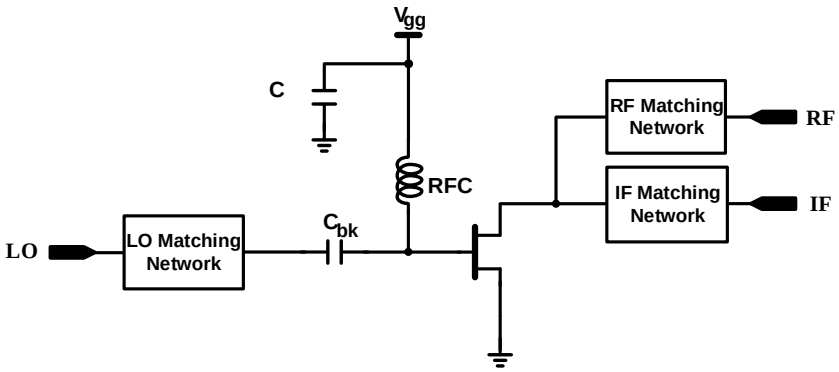


Figure 5.5: A typical resistive FET mixer.

5.2.3 Resistive mixer Analysis with the Proposed Model

In this section, the temperature effect on CL is analyzed with the aid of the developed R_{DS} model. First, the output impedance of the transistor is derived and the temperature effect on CL is evaluated based on the model developed in Section 4.5. Then, optimum gate biasing to compensate for temperature variations is found. The analysis is performed based on the reflection coefficient as seen from the drain port,

$$\Gamma = \frac{Z_{out}-Z_0}{Z_{out}+Z_0} \tag{5.1}$$

Where Z_{out} is the impedance looking into the drain side and Z_0 is the characteristic impedance. It should be noted that Z_{out} changes as temperature changes, and so does the reflection coefficient.

5.2.3.1 Output Impedance

The impedance looking into the drain side (Z_{out}) can be derived from the model shown in Figure 5.1 as follows:

$$Z_{out} = \frac{X\left(\left(1-C_{pd}\omega^2 Z\right)+\omega^2 C_{pd} Z\right)}{\left(1-C_{pd}\omega^2 Z\right)^2+\left(\omega C_{pd} X\right)^2} + j\omega\left[\frac{\left(Z\left(1-C_{pd}\omega^2 Z\right)-C_{pd}X^2\right)}{\left(1-C_{pd}\omega^2 Z\right)^2+\left(\omega C_{pd} X\right)^2} + L_d\right] \tag{5.2}$$

with

$$X = \left(R_s + R_d + \frac{R_{ch}}{1+(\omega C_{ds} R_{ch})^2}\right) \tag{5.3}$$

$$Z = \left(L_s - \frac{C_{ds} {R_{ch}}^2}{1+(\omega C_{ds} R_{ch})^2}\right) \tag{5.4}$$

For frequencies less than 10 GHz, the term $(\omega C_{ds} R_{ch})^2$ is less than 0.01 and it can approximated to zero. Therefore, X becomes equal to (= R_d + R_s + R_{ch}) which is equal to R_{ds}. Also, Z can be approximated to zero. Then, (5.2) can be rewritten as follows:

$$Z_{out} = \frac{R_{ds}}{1+\left(\omega C_{pd} R_{ds}\right)^2} - j\omega \left[\frac{C_{pd} {R_{ds}}^2}{1+\left(\omega C_{pd} R_{ds}\right)^2} - L_d\right] \tag{5.5}$$

Figure 5.6 shows the magnitude of the Z_{out} and R_{ds} versus the gate voltage. The frequency is used to plot the Z_{out} is 243 MHz which represent the RF frequency for our mixer design. It can be noticed that the output impedance saturates at 660 Ω while R_{DS} goes to higher than 800 Ω at low gate voltage (<-2.8V) and this is mainly due to the effect of C_{ds} and C_{pd} where they show up as R_{ds} becomes high. The most important region is where the impedance is equal to the characteristic impedance Z_0 which is 50 Ω at V_{gs}= -2.35V for our design, and it can be seen that both Z_{out} and R_{ds} are in complete alignment. Therefore, the Z_{out} can be further approximated to be equal R_{DS}, which is:

$$R_{ds} = \frac{1}{\alpha\left(I_{pk0}+\alpha_{I_1} T+\alpha_{I_2} T^2\right)\left(1+\tanh\left(\left(p_0+\alpha_{p_1} T+\alpha_{p_2} T^2\right)\left(V_{gs}-V_{pk0}-\alpha_V T\right)\right)\right)} \tag{5.6}$$

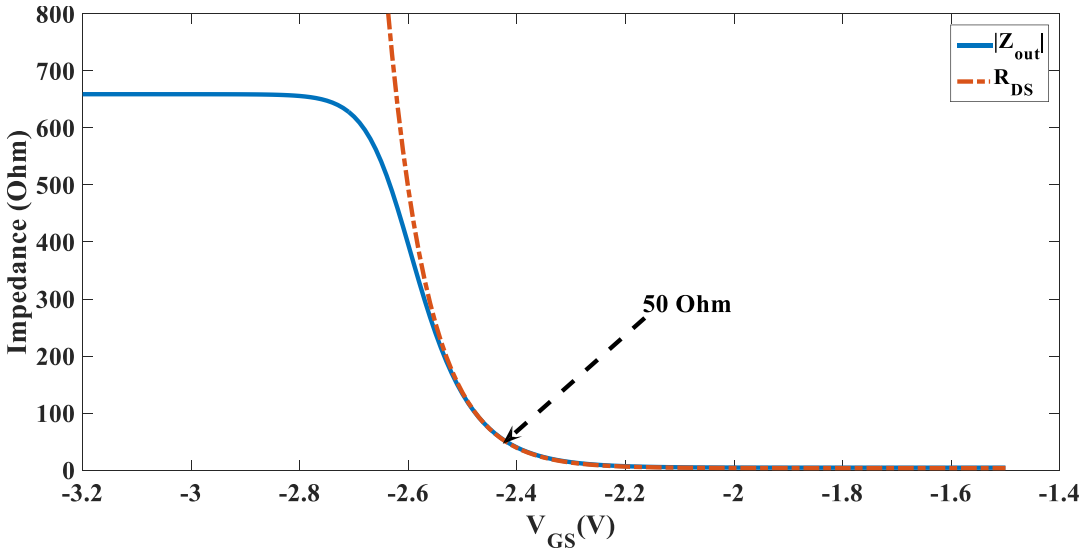


Figure 5.6: Reflection coefficient at drain terminal of the transitory based on R_{DS} model versus gate voltage at different temperatures

Figure 5.7 shows the measured s-parameters for the drain side of the transistor with port being matched to 50 Ω at frequency of 97.5 MHz. It can be noticed that as temperature increases the s-parameters shift to the right with the same trend indicating that as temperature increases real term in s-parameter only increases, which represents the R_{ds} variation with temperature.

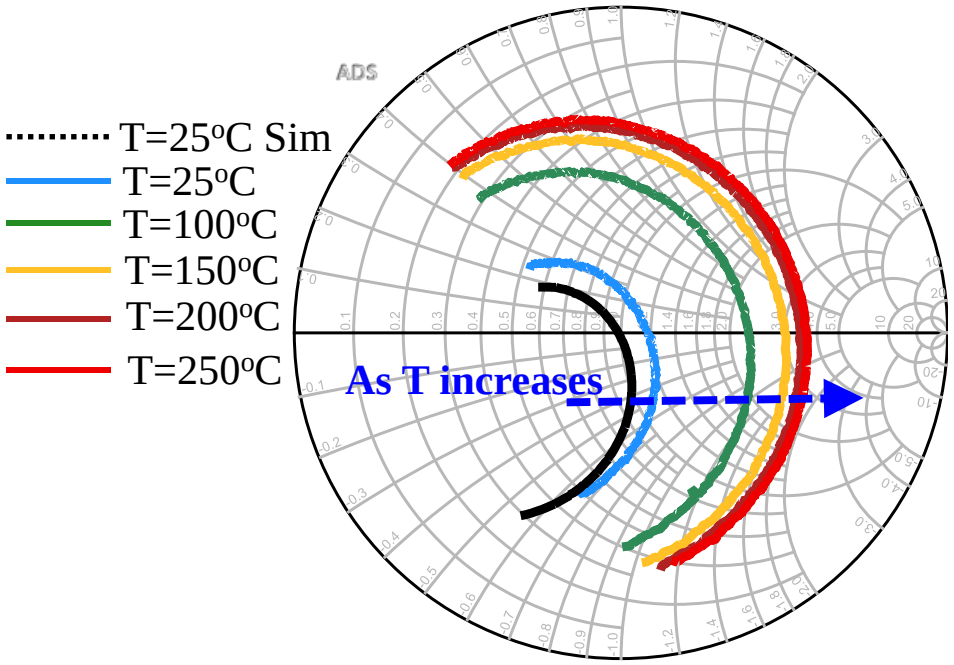


Figure 5.7: Measured s-parameters at drain side at different temperature levels with fixed gate voltage (optimum gate voltage at room temperature which is -2.3V). The frequency sweep is from 10 MHz to 500 MHz.

5.2.3.2 Effect of Temperature on CL

According to [89], the CL can be calculated using the following:

$$CL = \left(\frac{1}{2\pi}\int_{-\pi/\omega_{LO}}^{\pi/\omega_{LO}} \Gamma(t,T)\cos(\omega_{LO}t)\,dt\right)^{-2} \tag{5.7}$$

where ω_{LO} is local oscillator frequency. $\Gamma(t,T)$ is the reflection coefficient at the drain terminal and function of time (t) and temperature (T). Assuming Z_0 is independent of temperature and inserting (5.6) into (5.1) gives the reflection coefficient as seen into the drain terminal of the GaN function of time and temperature:

$$\Gamma(\mathrm{T}) = \frac{1-Z_0\alpha(I_{pk0}+\alpha_{I_1}T+\alpha_{I_2}T^2)\left(1+\tanh\left((p_0+\alpha_p T)(V_{gs}-V_{pk0}-\alpha_V T)\right)\right)}{1+Z_0\alpha(I_{pk0}+\alpha_{I_1}T+\alpha_{I_2}T^2)\left(1+\tanh\left((p_0+\alpha_p T)(V_{gs}-V_{pk0}-\alpha_V T)\right)\right)} \tag{5.8}$$

Figure 5.8 shows the effect of temperature on the reflection coefficient at a given gate voltage. It can be noticed that as temperature increases, the reflection coefficient transition from 1 to -1

shifts to the left, causing the zero reflection point to move from -2.35V to -2.6V.

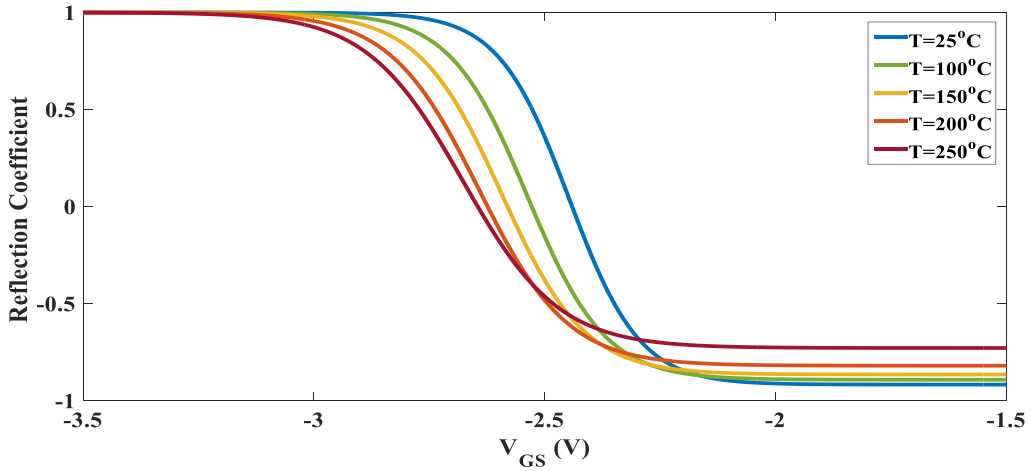


Figure 5.8: Reflection coefficient at drain terminal of the transitory based on R_{DS} model versus gate voltage at different temperatures.

The gate to source voltage is time varying and can be expressed as:

$$V_{gs} = V_{GS} + v_{LO}\cos(\omega_{LO}t) \tag{5.9}$$

where V_{GS} is the gate biasing voltage.

Substituting (5.9) in (5.8) and (5.8) in (5.7) and using numerical integration we can find the CL at different temperatures. Figure 5.9 shows the predicted conversion loss using the developed model at different temperatures. It can be noticed that at small v_{LO} the conversion loss variation is very large while at large value the temperature has a small effect on conversion loss. This due to the fact that temperature variations of V_{pk} has the negligible impact on large v_{LO}.

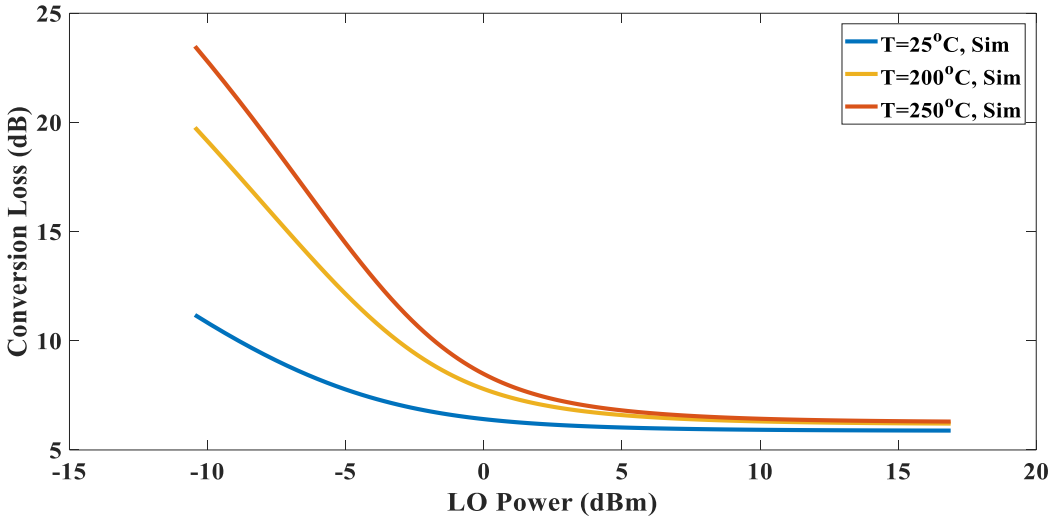


Figure 5.9: Computed conversion loss using the developed model versus LO power at fixed V_{GS} of -2.35 V.

5.2.3.3 CL at Optimum Biasing with Temperature

Temperature effects can be minimized with one of two approaches 1) using high LO power > 5dBm which will impose more challenge on the LO design. The second option is to design optimum biasing voltage that compensate for the temperature variations and in this way, the LO design can be relaxed.

In order to mitigate the conversion loss variations with temperature, the slope of CL with temperature (TC) has to be zero which leads to $\frac{\partial CL(t,T)}{\partial T} = 0$.

By deriving (5.7) and equating it to zero we can find:

$$V_{dc,Opt} = V_{pk0} + \alpha_{Vpk}T - \frac{1}{(p_0+\alpha_{p_1}T+\alpha_{p_2}T^2)}\tanh^{-1}\frac{1}{Z_0\alpha\left(I_{pk0}+\alpha_{I_{pk}}T+\alpha_{I_{pk2}}T^2\right)} \quad (5.10)$$

Eq (5.10) shows the optimum adaptive biasing voltage that can provide zero temperature reflection coefficient. Figure 5.10 shows the optimum biasing voltage versus temperature. It can be noticed that at temperature below 250 ^oC the gate biasing follows the variation of v_{pk}. Therefore, at temperature below 250 ^oC can be approximated to a linear equation:

$$V_{dc,Optimum} = V_{pk0} + \alpha_{Vpk}T \quad (5.11)$$

Biasing voltage with linear behavior with temperature can be easily implemented in analog circuit.

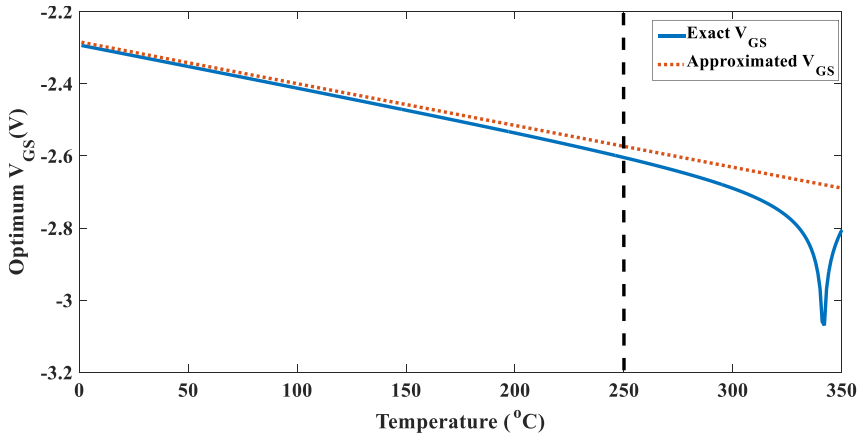


Figure 5.10: Optimum gate-to-source voltage versus temperature based on the developed R_{DS} model. Blue is the exact model and red is the approximated model.

Optimized CL can be obtained by inserting (5.11) in (5.8) and (5.8) in (5.7) solving (5.7) numerically. Figure 5.11 shows the predicted CL after applying the optimum biasing derived in

(5.7). It can be noticed that there is a very small increase in CL with temperature due to the increase of R_{on} with temperature.

The implementation of the adaptive bias circuit that provides the optimum biasing will be discussed in Section 5.9.

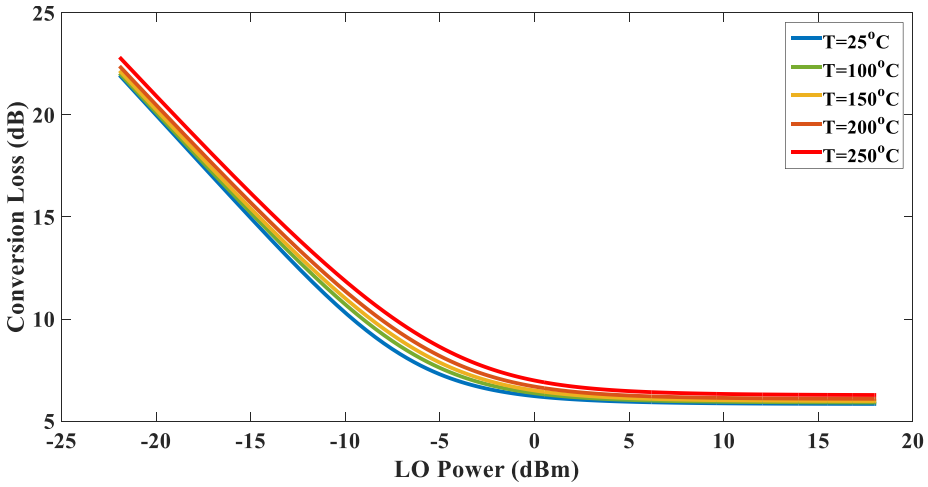


Figure 5.11: Estimated optimized CL at different temperature.

5.2.4 Proposed Mixer Design

The proposed mixer aims to upconvert the IF of 97.5 MHz to 230 MHz – 253 MHz and downconvert the RF band 230 MHz – 253 MHz to the IF of 97.5 MHz with LO frequencies of 328 MHz - 350.5 MHz. The design objective is to operate the mixer reliably at high temperatures while providing low downconversion and upconversion losses and reasonable linearity. The proposed mixer is designed and prototyped on a PCB.

5.2.4.1 Transistor Biasing

Figure 5.12 shows the circuit diagram of the proposed mixer with highlight on the biasing network. RFC denotes an RF choke, C_{bk} a DC blocking capacitor, and C a bypass capacitor. They serve as a bias-T for the gate bias voltage V_{gg}. Another RFC connected at the drain side ensures 0 V at the drain. As there is no drain-source current, the channel behaves as a variable resistor, whose resistance depends on the gate voltage.

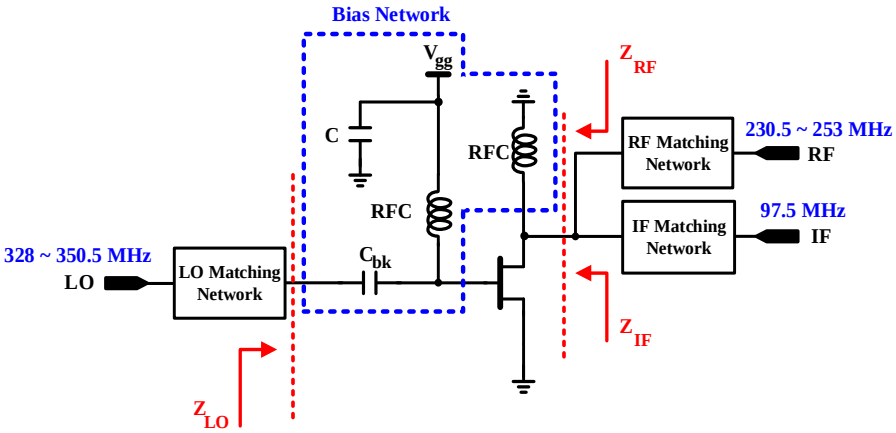


Figure 5.12: Bias network for the resistive FET mixer.

As the first step, the mixer is biased to the optimal gate voltage to minimize the CL. Figure. 5.13 shows a simulation result of the CL versus the gate voltage for the circuit in Figure 5.12 without the matching networks. The CL of 11.5 dB is achieved for the optimum gate voltage of -2.35 V.

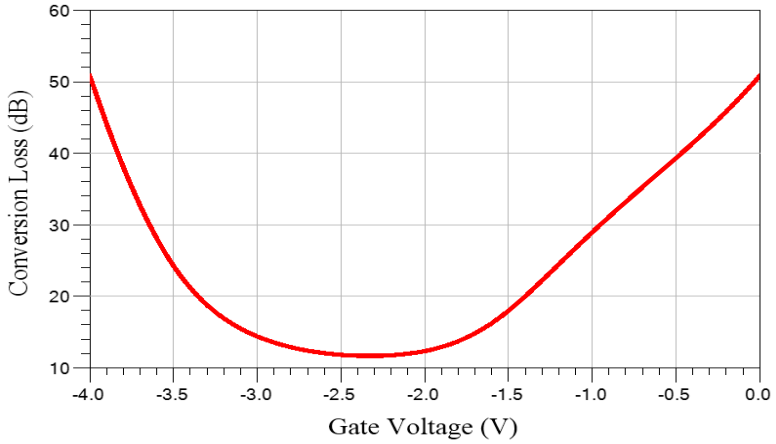


Figure 5.13: Simulated conversion loss versus the gate voltage at room temperature without matching networks at the mixer ports. f_{LO} is fixed to 340.5 MHz, and LO power is 0 dBm. RF power =-30 dBm and f_{IF}= 97.5 MHz. Optimum gate voltage is -2.35V.

5.2.4.2 Matching Networks

The variations of microstrips are negligible with temperature for the frequency bands [80]. Although the operating frequencies are in VHF band for the proposed mixer, microstrip transmission lines are used to match the transistor terminals to 50 Ω.

First, the LO port is matched to 50 Ω at the center frequency (=340.5 MHz) of the LO frequency range and ideally short-circuit for other frequencies. The impedance looking into the gate is mainly capacitive of 0.435-j90.7 Ω. A transmission line TL1 with a shunt resistor R_2 of 100 Ω at the gate makes the gate match to 50 Ω at LO frequencies.

The impedance looking into the drain at the center frequency (=241.5 MHz) of the RF is 22.9-j0.436 Ω. TL2 is used to match the drain to the RF port at the RF. The impedance looking into the drain at the IF port is 21.389 – j1.856 Ω, and TL3 is used to match the IF port. The final schematic of the mixer is shown in Figure 5.14.

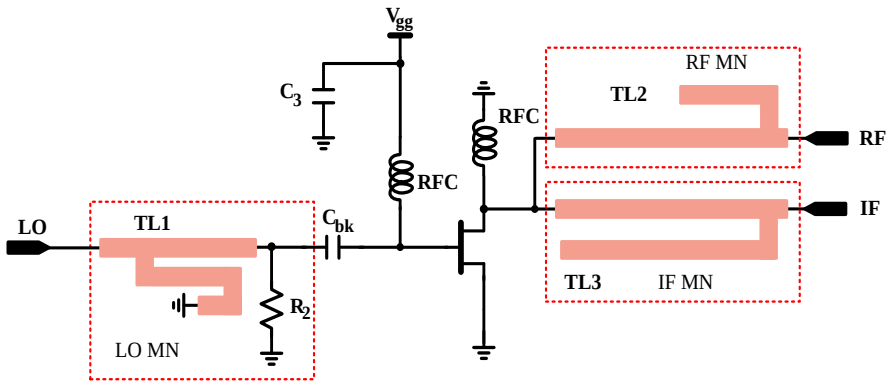


Figure 5.14: Proposed resistive FET mixer with the matching networks.

5.2.4.3 Prototype

The proposed mixer shown in Figure 5.15 is prototyped with Qorvo T2G6000528-Q3, a 0.25µm GaN on SiC HEMT, and assembled on RO3010 PCB board.

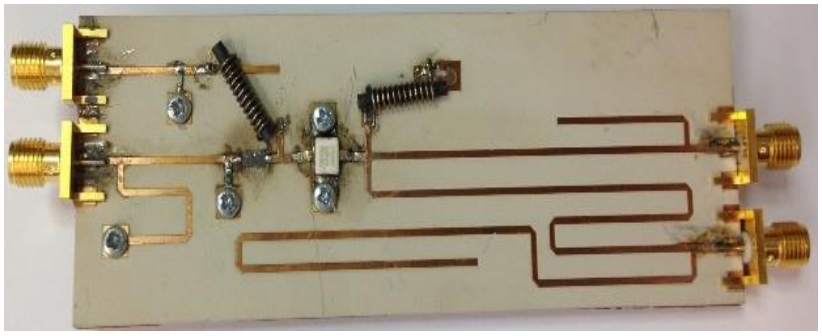


Figure 5.15: A photograph of the mixer prototype.

5.2.5 Resistive Mixer Measurement Results

This section presents measured results for the mixer at temperatures ranging from room temperature to 250 ^{o}C. Also it compares the performance between the room temperature and 250 ^{o}C and suggests how to mitigate the performance variations with temperature.

5.2.5.1 Measurement Objectives and Environment

The main objectives are to test the proposed mixer design at high temperatures and validate the model and analysis carried out in the previous sections. For this purpose, the mixer board is placed inside a Yamato natural convection drying furnace. Special high temperature cables and connecters are used for the measurements. An R&S ZVL network analyzer is used to measure s-parameters. For down CL measurements, the RF port is connected to R&S SMBV100A vector signal generator. The IF port is connected to R&S FSU26 spectrum analyzer. The mixer LO port is connected to Agilent signal generator E4411B, which functions as a variable oscillator. Figure 5.16 shows the test setup for CL measurements. For up CL measurements, the IF and RF ports are swapped. Keysight and R&S signal generators and an Anritsu spectrum analyzer are used for compression measurements. Rigol power supplies are used to set up the required bias.

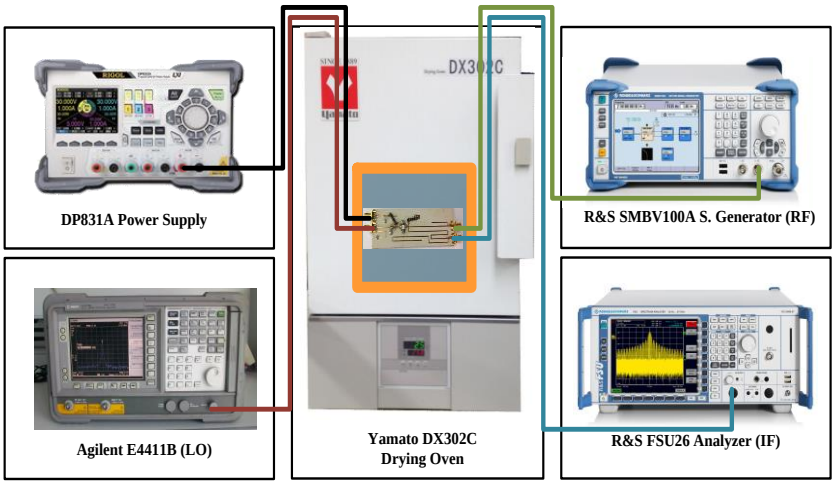


Figure 5.16: A test setup for conversion loss measurements.

5.2.5.2 Resistive Mixer Measurement Results

5.2.5.2.1 Conversion Loss vs. RF Frequency

The mixer is biased initially to minimize down and up conversion losses at room temperature. The measurement results indicate that V_{gg} of -2.35 V provides optimal performance in terms of the CL at room temperature. The furnace temperature is gradually elevated up to 250

^{o}C, while V_{gg} is fixed to -2.35 V. The measured down and up CL versus RF at 25 ^{o}C, 150 ^{o}C, 200 ^{o}C, and 250 ^{o}C are shown in Fig. 9 and 10, respectively. It can be observed that as the temperature increases, the CL increases steadily. The down CL increases by 1.6 dB (from 6.46 dB to 8.06 dB) at 243 MHz for the LO power of 2.5 dBm as shown in Figure 5.17. The up CL increases by 1.4 dB under the same condition as shown in Figure 5.18.

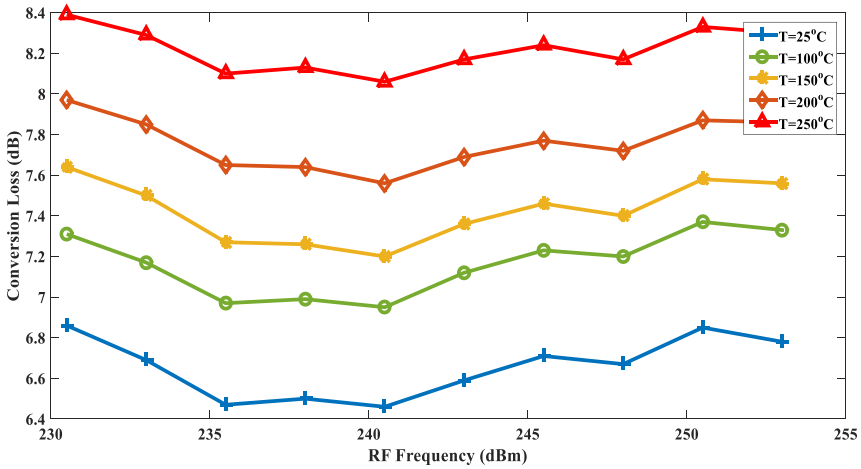


Figure 5.17: Measured downconversion loss versus RF frequency at different temperature levels. V_{gg} is fixed to -2.35 V. f_{LO} varies from 328.0 MHz to 350.5 MHz, and LO power is +2.5 dBm. RF power = -30 dBm and f_{IF}= 97.5 MHz.

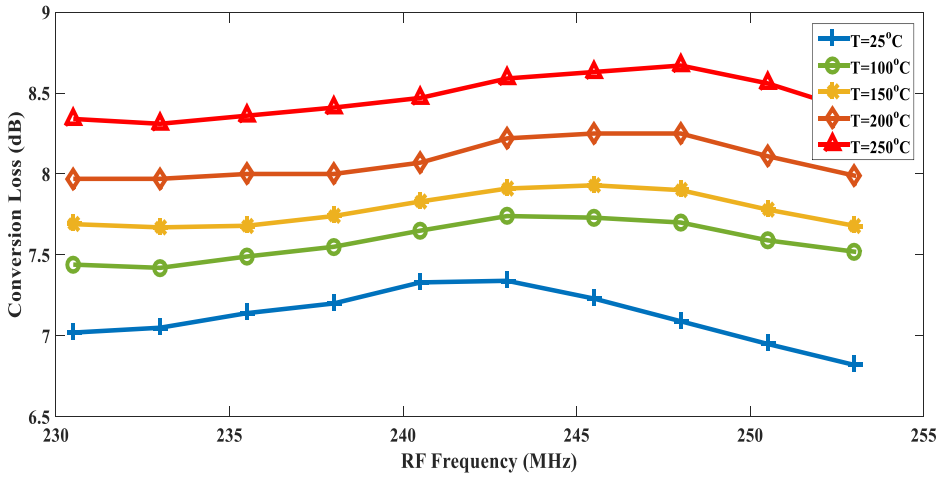


Figure 5.18: Measured upconversion loss versus RF frequency at different temperature levels. V_{gg} is fixed to -2.35 V. f_{LO} varies from 328.0 MHz to 350.5 MHz, and LO power is +2.5 dBm. RF power = -30 dBm and f_{IF}= 97.5 MHz.

5.2.5.2.2 Conversion Loss vs Lo Power

The LO power is swept from -10 dBm to 20 dBm under the fixed RF power of -30.0 dBm, f_{Lo}=340.5 MHz, f_{RF}=243 MHz, and f_{IF}=97.5 MHz. The CL varies largely under a low LO power, but the variance becomes smaller for a high LO power. Figure 5.19 shows the measured and predicted conversion loss using the developed model at different temperatures. It can be noticed that the measured and predicted models match very well at all temperatures. Also, it can be seen that at small v_{LO} the conversion loss variation is very large while at large value the temperature has a small effect on conversion loss. This due to the fact that temperature variations of V_{pk} has the negligible impact on large v_{LO}. The CL is saturated to 6.2 dB at the LO power of around 5 dBm at room temperature and 6.9 dB at the LO power of around 10 dBm at 250 ^{o}C. The CL varies by a factor of 12.7 dB as the temperature changes from room temperature to 250 ^{o}C under the LO power of -10 dBm.

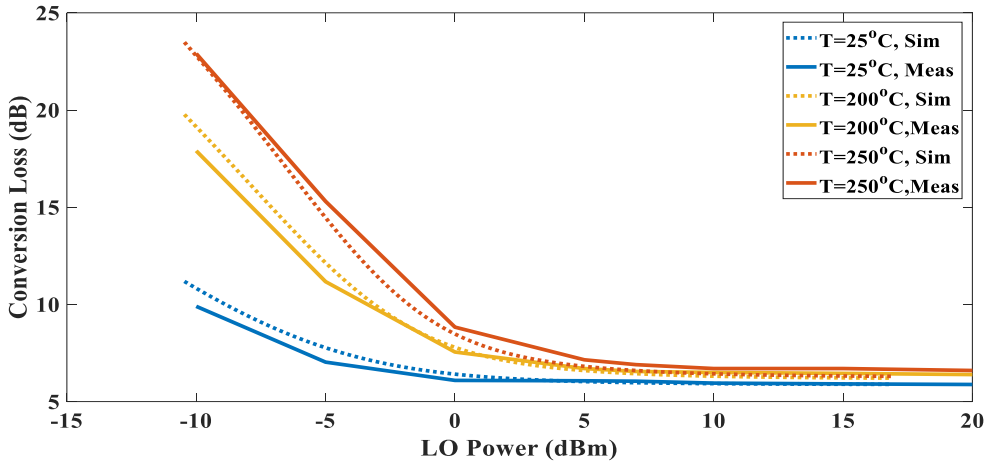


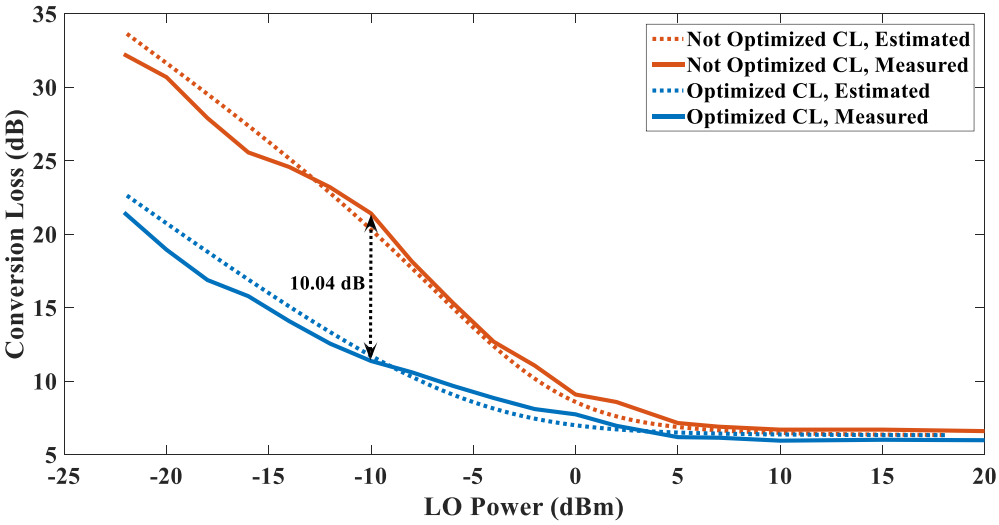
Figure 5.19: Measured and computed conversion loss using the developed model versus LO power at fixed gate voltage at different temperatures.

5.2.5.2.3 Conversion Loss at Optimum Biasing vs LO Power

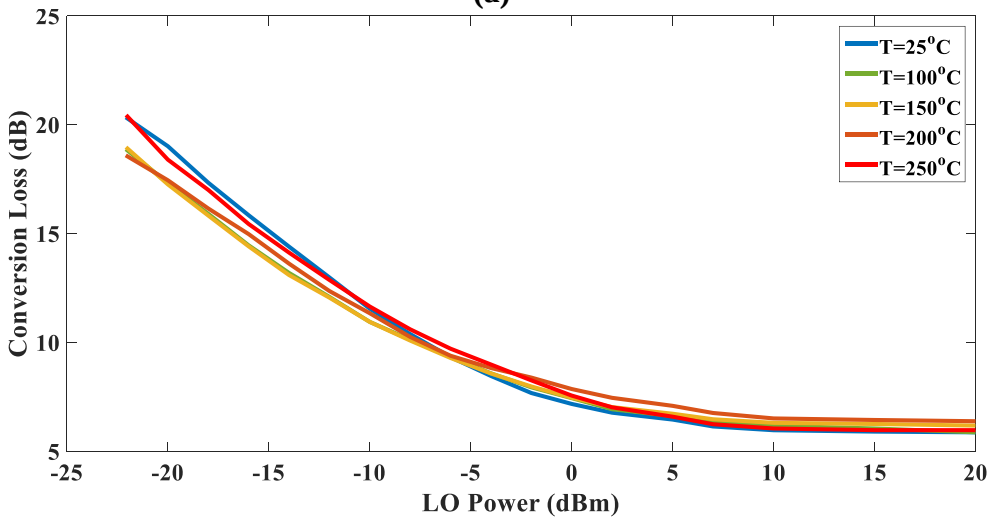
To mitigate CL variations at a low LO power, adaptive gate biasing can be used to compensate the threshold and resistance variations with temperature.

Figure 5.20 (a) shows the predicted and measured optimized CL versus LO power along with non-optimized CL at 250 ^{o}C. It can be noticed the good agreement between the predicted performance and the measured results. Figure 5.20 (b) shows the measured CL versus LO power at different temperatures after applying the optimum biasing derived in eq (5.11). By apply the

optimum biasing voltage the maximum CL variation can be reduced to <0.75 dB over temperature range up to 250 ^{o}C.



(a)



(b)

Figure 5.20: Optimized CL (a) Difference between the optimized and not optimized CL at 250 ^{o}C, (b) Measured optimized CL at different temperature.

5.2.5.2.4 Matching vs Temperature

Mixer impedance matching at different temperature levels is also measured. First, the s-parameters are measured for RF, IF, and LO ports at room temperature. Then, the temperature of the furnace is gradually elevated up to 250 ^{o}C while keeping the gate voltage constant. Figure. 5.21 shows s-parameters for the RF, IF and LO ports at different temperatures with the gate voltage fixed to the optimum at room temperature. It is observed that the LO port stays well matched even

if temperature increases, while the RF and the IF ports move away from the matching points. This is because as temperature increases, the threshold voltage decreases and R_{ds} shifts to the left in the Smith charts, which results in the RF and IF ports mismatching.

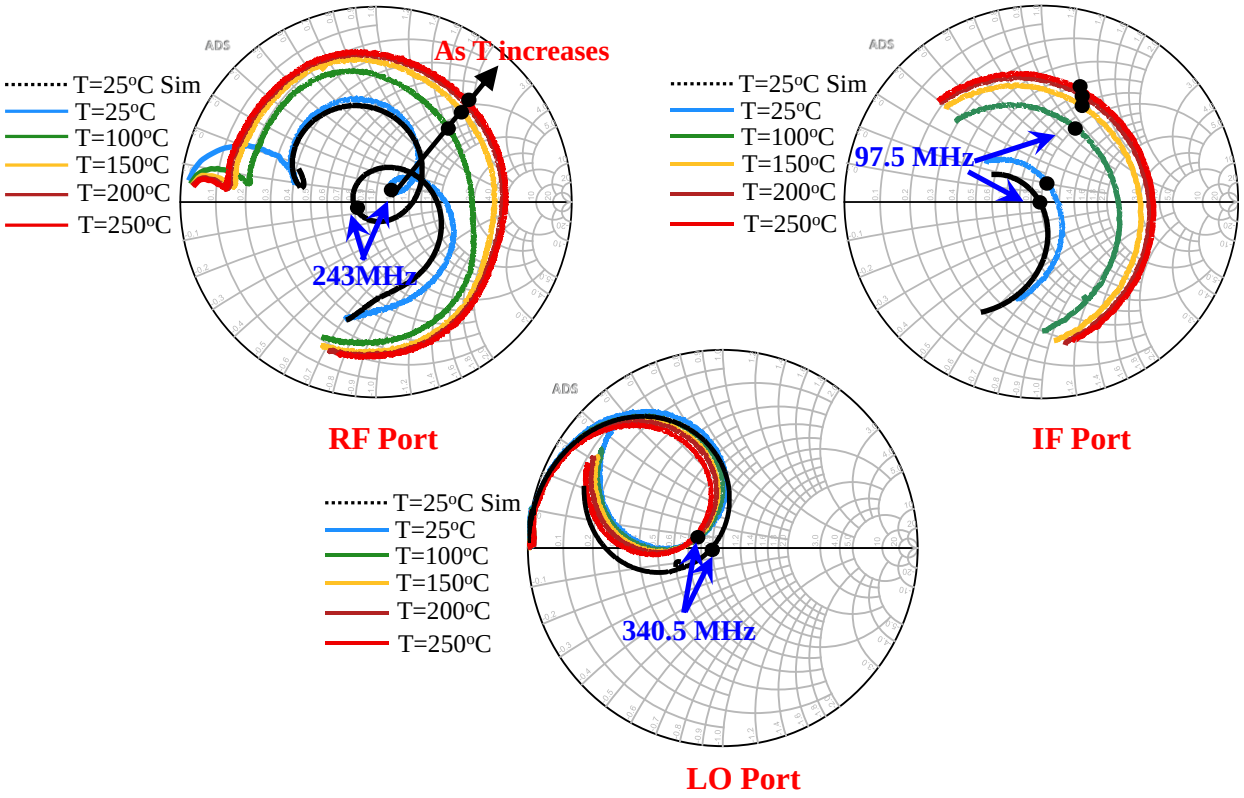
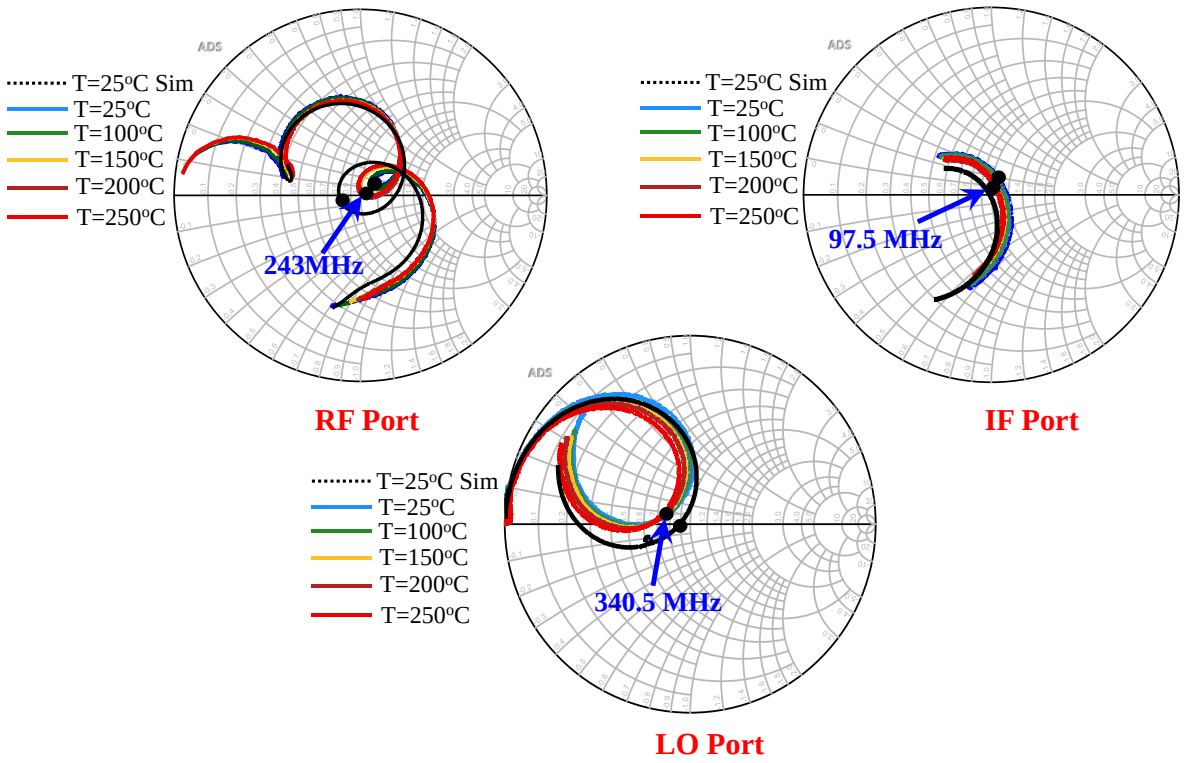
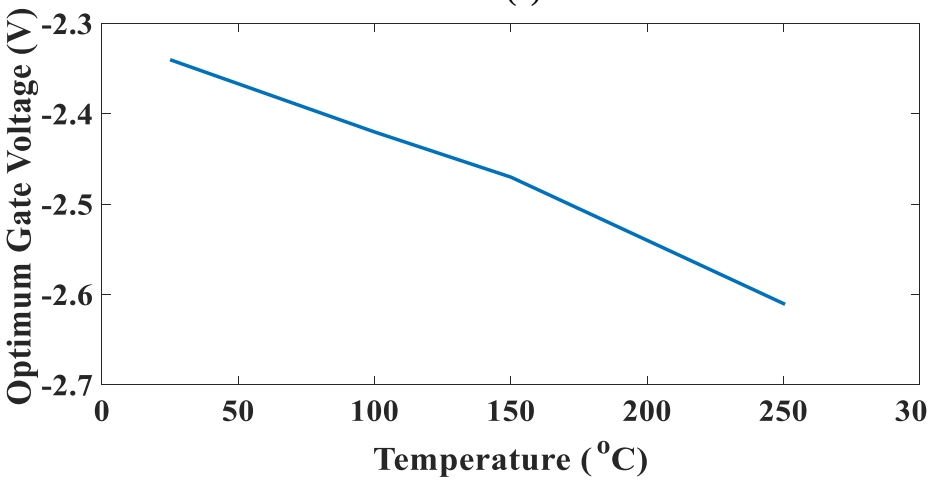


Figure 5.21: Measured s-parameters at different temperature levels with fixed gate voltage (optimum gate voltage at room temperature).

Figure 5.22: (a) shows the s-parameters for the RF, IF and LO ports at different temperatures with the optimal gate voltage for each temperature level. It can be observed that the ports stay well matched when the gate bias is adjusted to the optimal value. This can be explained as the adaptive gate biasing compensates the resistance and threshold voltage variations with temperature. Figure 5.22 (b) shows the optimum gate voltage to maintain ports matching at different temperatures. The implementation of the adaptive bias circuit that provides the optimum biasing will be discussed in Section 5.9.



(a)



(b)

Figure 5.22: (a) Measured s-parameter at different temperatures with adaptive gate voltage (b) measured optimum gate voltage versus temperature.

5.2.5.2.5 Port-to-port Isolation

The leakage from one port to another is also an important aspect for the mixer. Figure 5.23 shows the port to port isolation measurements for the LO to RF ports and the LO to IF ports at 250 ºC. The mixer achieves 24.5 dB isolation between RF and IF ports and 28 dB isolation between the LO and IF ports over the frequency range of 328.0 MHz to 350.5 MHz. The isolation level between ports is satisfactory for the proposed mixer.

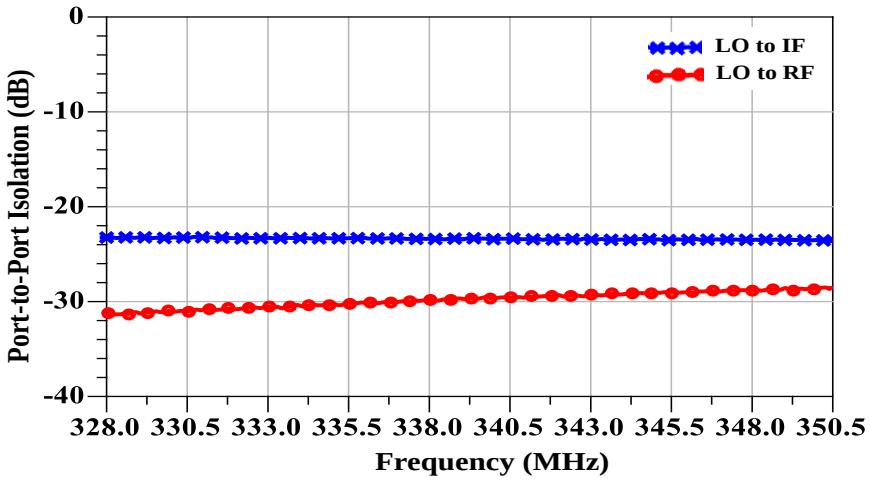


Figure 5.23: Port-to-port isolation.

5.2.5.2.6 Linearity

The linearity is measured at room temperature and 250 ºC. A single-tone test is carried out by sweeping the RF power at f_{RF} = 243 MHz, applying the LO power of 2.5 dBm, and the 1-dB compression points are measured at room temperature and 250 ºC. Figure 5.24 shows the output IF power versus input RF power at room temperature and 250 ºC. As the temperature increases, the linearity degrades. The input 1-dB compression point is 2.0 dBm at room temperature and -1 dBm at 250 ºC.

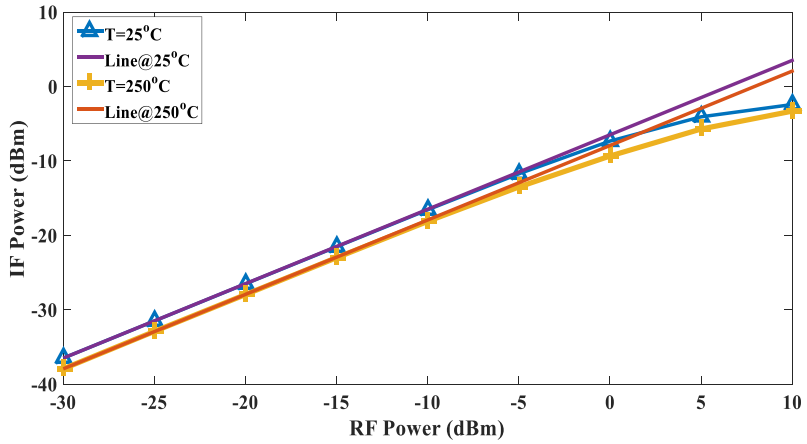


Figure 5.24: Measured IF power versus RF power at 25ºC and 250ºC. f_{LO} = 340.5 MHz to 350.9 MHz, f_{RF} =243 MHz, LO power =2.5 dBm, and f_{IF}= 97.5 MHz.

Table 5.2 shows a comparison of the proposed mixer with the other mixers based on GaN devices. Among them, only the proposed mixer and the one presented by Wong et al. are capable of operating at 250 ºC [86]. The CL of Wong et al.'s mixer is 12.9 dB at 2.5 GHz, while that for the proposed mixer is 6.5 dB at 243 MHz. Also the required LO power for Wong et al.'s mixer is 10 dBm, while the proposed one is only 2.5 dBm. Another advantage of the proposed mixer is a small CL increase of 0.72 dB from room temperature to 250ºC, while the increase for Wong et al.'s mixer is 4.35 dB. Although a fair comparison is difficult due to different technologies used, frequency bands, design objectives and constraints; the proposed mixer shows satisfactory performance for a wide temperature range with a reasonably low LO power of 2.5 dBm.

Table 5.2: A performance comparison with state-of-the-art passive GaN HEMT Mixers.

Parameter	[76]	[77]	[86]	**This work**
Temperature (ºC)	25	25	25 to 250	**25 to 250**
Technology	GaN HEMT	GaN HEMT	GaN diode	**GaN HEMT**
Frequency (GHz)	1.7	8 ~14	2.5	**0.23 ~ 0.25**
LO Power (dBm)	14	19	10	**2.5**
CL (dB)	9.5	7 ~ 8	12.9 @ 25 ºC	**6.5 @ 25 ºC**
CL Variations (dB)	-	-	4.35 @ 250 ºC	**0.72 @ 250ºC**
NF (dB)	-	10 ~ 20	16.35	**7**
Input P1dB (dBm)	11	22	10	**5**

5.3 Downconversion Active Mixer

The design objective of the proposed mixer is to operate reliably at high temperatures while providing a moderate to high conversion gain (CG) and low CG variations with temperature. The design process involves circuit analysis, design, and prototyping, which is described in this section.

There are numerous mixer designs that operate at room temperature, but very few mixer designs operating up to 85 ^{o}C have been reported in open literatures [90]-[92]. To our knowledge, our research published in [93] paper design is the first active mixer design operating at ambient temperature of 250 ^{o}C.

5.3.1 Active GaN HEMT Mixer

The topology of the proposed mixer is selected considering two key requirements, reliability at high temperatures and a moderate conversion gain. The Gilbert cell topology offers high gain, but is eliminated due to a large number of active devices required. A complex circuit is more vulnerable to the temperature variation, which deteriorates reliability at high temperatures. A common source topology with a single transistor shown in Figure 5.25 is adopted for the proposed mixer owing to the low circuit complexity and its thermal robustness. The GaN transistor technology being used to design the mixer has a large gain and able to provide the gain performance required by the transceiver.

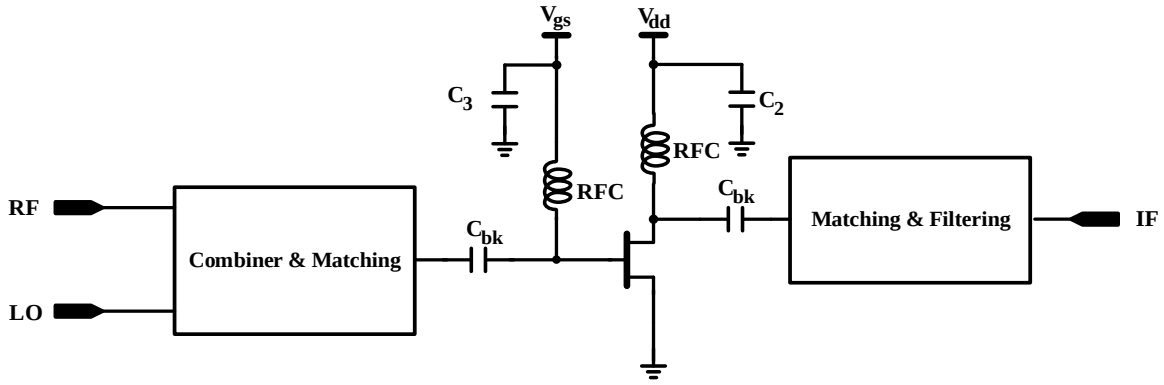


Figure 5.25: A typical common source active mixer.

The conversion gain of the mixer under the matched condition can be estimated using the following equation [94]:

$$G_C = \frac{1}{4}\left(\frac{kg_{MAX}}{\omega_{RF}C_{in}}\right)^2 \frac{R_L}{(R_S+R_i+R_G)} \tag{5.12}$$

where k is a constant around 0.5 for a sinusoidal half-wave rectified g_m or $2/\pi$ for a square wave g_m, and g_{MAX} is the peak value of gm when the transconductance is maximum. R_s is the source resistance of the transistor, R_G is the gate resistance, R_i is the input resistance of the transistor, C_{in} is the equivalent input capacitance that include the gate-source, pad and package capacitances, and R_L the load resistance. Eq (5.12) assumes that the LO power is sufficiently high to drive the device to the peak value of g_m. As the LO voltage swing is reduced, so too is the conversion gain, because the corresponding value of g_{MAX} is reduced proportionally. Also it assumes the mixer ports are matched with lossless components.

From eq (5.11) also, it can be noticed that conversion gain (CG) is temperature dependent since g_m, C_{in} (or C_{GS}), R_i, R_G, and R_S are temperature dependent. The temperature strongly impacts the CG when the LO voltage swing is low (LO power less than 0 dBm) because the g_m variation with temperature becomes large. Another observation is that there is possible mutual compensation between the g_m and C_{in}, R_G, R_S and R_i since their temperature variations have different impact on the CG. However, the mutual compensation for CG is bias and frequency dependent. Lastly, the Q of the input and output matching should be taken into the consideration if lumped components (particularly inductor) are used in the matching networks because the Q tends to decrease with temperature.

5.3.2 Proposed Active Mixer Design

The proposed mixer performs downconversion of RF frequencies of 230.5 – 255.5 MHz to IF frequency of 97.5 MHz with LO frequencies of 328 – 353 MHz. Figure 5.26 shows the circuit diagram of the proposed mixer. The selected GaN transistor is inherently unstable, and the design should provide features to prevent oscillation over a wide frequency range. R_1 (=50Ω) is used for stabilization for low frequencies below 60 MHz. This resistor does not increase noise to the mixer, since the RF choke connected to the resistor has high impedance at the in-band frequencies. A shunt resistor R_2 is connected at the gate to stabilize the device for the in-band frequency of 200 – 300 MHz. A tradeoff has to be made for R_2 between stability and noise. Simulation results show that 100 Ω is adequate for R_2 to make the mixer unconditionally stable while adding relatively small thermal noise.

The RF and LO ports are connected through two series coupling capacitors. The RF port is connected through C_{rf} of 100 pF to the input matching network, which matches the RF port

(=50Ω) to the gate of the transistor using a transmission line TL_1. Microstrip matching is used at the RF port, since it has smaller temperature variation compared with a lumped LC matching network. Capacitor C_1 (=165 pF) resonates with the stub of TL_1 to provide the short circuit effect to the IF frequency of 97.5 MHz. The LO signal is injected through capacitor C_{lo} to transmission line TL_1 followed by the transistor gate. Capacitor C_{lo} (=4 pF) is chosen small to isolate the LO port from the RF port. The IF port is connected to the drain of the transistor via transmission line TL_2 and the output matching network. TL_2 reduces the output power of the IF port for the LO frequency band (328– 350.5 MHz), and inductor L_1 (=175 nH) and two capacitors, C_s (=40 pF) and C_p (=10 pF), form the output matching network. The output matching network matches the output impedance of the transistor to 50 Ω at the IF frequency. Inductor L_1 is an air core coil made from a high temperature copper wire, and the inductor is characterized at higher temperatures. Measurements show that the inductor value drops with increasing temperature, which affects the performance of the mixer. The variation can be compensated by adjusting the bias point at high temperatures.

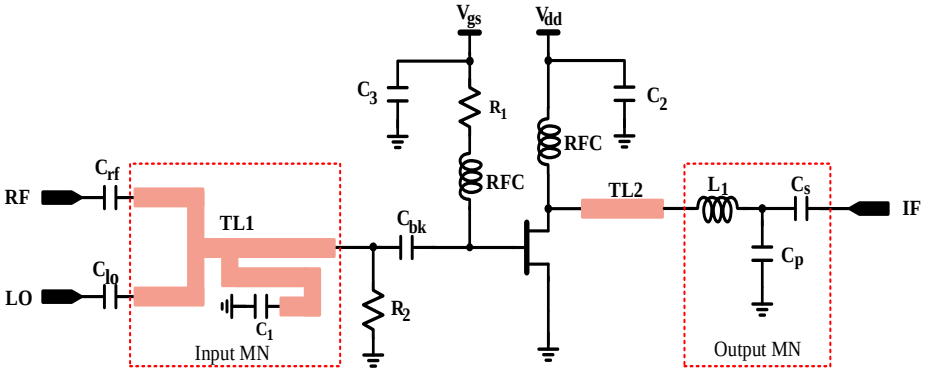


Figure 5.26: Circuit diagram of the proposed mixer.

RF chokes and DC blocking capacitor C_{bk} serve as a bias-T for the gate bias voltage V_{gs}. Capacitor C_s, which is part of the output matching network, also serves to block DC voltage at the output. Capacitors C_2 and C_3 are bypass capacitors.

Figure 5.27 shows the prototype of the mixer. The transistor is shown at the center of the board, and two matching networks are located at low left and right sides.

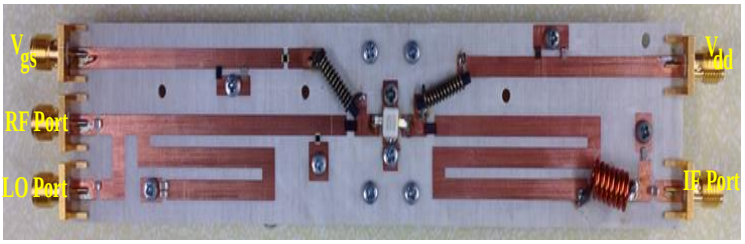


Figure 5.27: A photograph of the mixer prototype.

5.3.3 Active GaN HEMT Mixer Measurement Results

This section presents measurement results of the proposed active mixer at room temperature and up to 250 ºC. Also it compares the performance at different temperatures and discusses adjustment of the bias point to mitigate the performance variations with temperature.

5.3.3.1 Measurement Setup

Measurements with high temperature cables and connecters were carried out at room and high temperatures inside a Yamato natural convection drying furnace. Rohde & Schwarz ZVL network analyzer was used to measure s-parameters and stability, and noise figure analyzer N8975A for CG and noise figure (NF).

5.3.3.2 Measured Results

5.3.3.2.1 Performance vs RF Frequency

Optimum bias point of V_{gs} = -2.57 V, and I_d = 22 mA under V_{dd} = 5 V results in best performance in the CG and NF at room temperature and is obtained through measurements. Then, the furnace temperature is elevated gradually up to 230 ºC under the fixed V_{gs} of -2.57 V. The performance is observed at four different temperatures of 25 ºC, 150 ºC, 200 ºC and 230 ºC. The measured CG versus RF frequency is shown in Figure 5.28. It can be observed that the CG drops with increased temperature. For example, the CG drops by 9 dB from 6 dB at 25 ºC to -3 dB at 230 ºC for the frequency of 243 MHz. It was also observed that the drain current increases to 47 mA at 230 ºC.

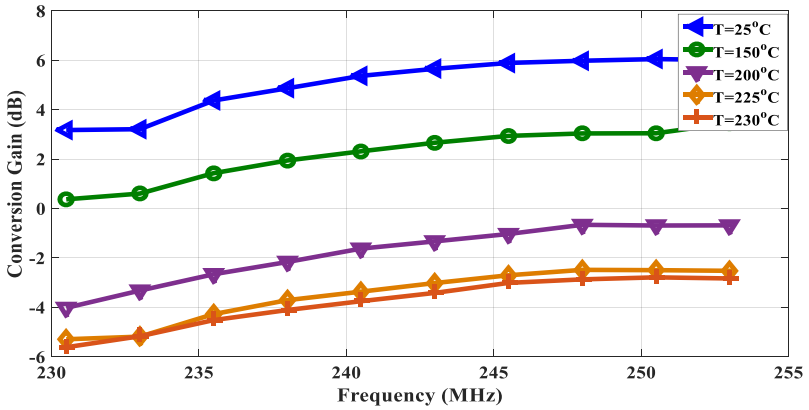


Figure 5.28: Measured conversion gain versus RF frequency at different temperatures. f_{LO} varies from 328.0 MHz to 350.5 MHz, while LO power = -15 dBm. RF power = -30 dBm, and f_{IF}= 97.5 MHz.

Figure 5.29 shows the measured NF at different temperatures. The NF performance deteriorates as the temperature increases. For example, the NF under the frequency of 243 MHz increases by 6 dB from 13.0 dB at 25 ºC to 19.0 dB at 230 ºC.

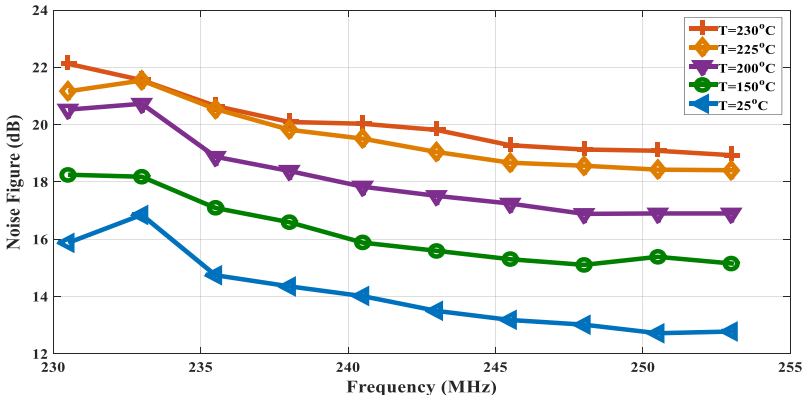


Figure 5.29: Measured noise figure versus RF frequency at differet tempaerature levels. f_{LO} varies from 328.0 MHz to 350.9 MHz, and LO power is -15dBm. RF power =-30 dBm and f_{IF}= 97.5 MHz.

5.3.3.2.2 Performance vs Gate Voltage

Although our initial target temperature is 230 ºC, we noticed that the mixer can operate at a higher temperature of 250 ºC. So we measured the performance at 250 ºC for the following ones. The temperature is fixed at 250 ºC. The bias voltage is swept to find the optimum value. It was observed that when V_{gs} is biased at -2.75 V instead of -2.57 (which is optimum at room temperature), the CG improves by 3.7 dB and NF improves by 1.65 dB. Figure 5.30 & Figure 5.31 show the CG and NF versus V_{gs} at 250 ºC, respectively. The measurement results indicate that

adjustment of the bias voltage according to the ambient temperature improve the performance of the mixer at low LO power.

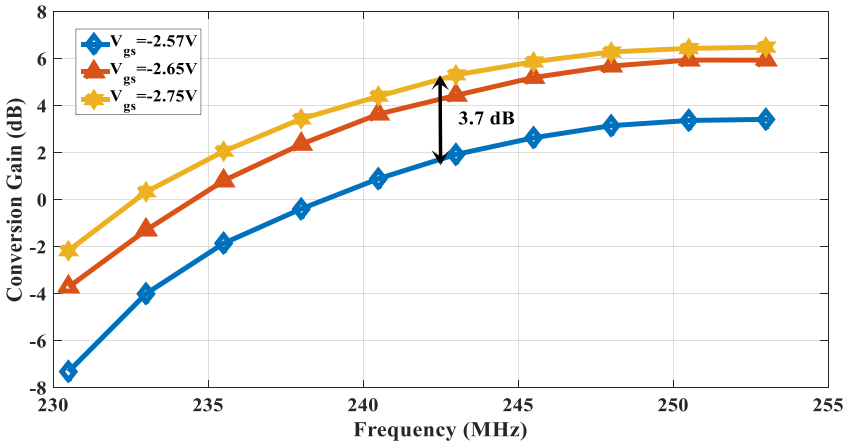


Figure 5.30: Measured CG versus RF frequency for differet gate bias voltages (V_{gs}) at 250°C. f_{LO} varies from 328.0 MHz to 350.5 MHz, while LO power = -15 dBm, RF power = -30 dBm, and f_{IF}= 97.5 MHz.

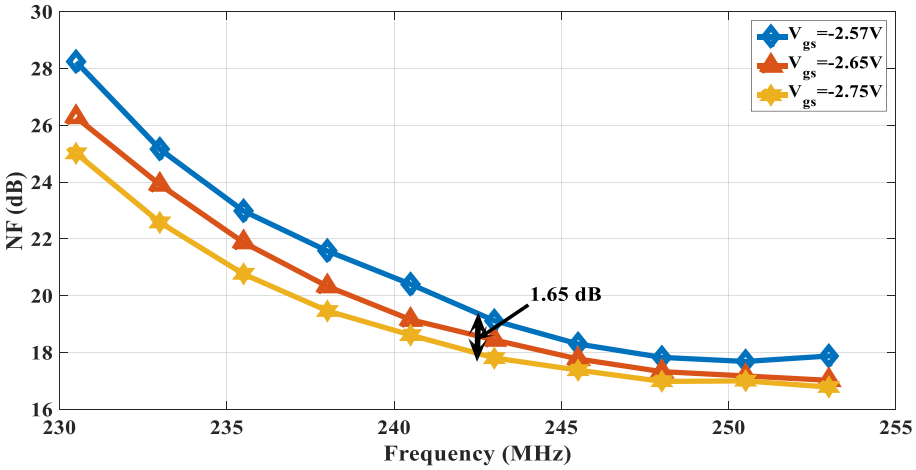


Figure 5.31: Measured NF versus RF frequency for different gate bias voltages (V_{gs}) at 250 °C. f_{LO} varies from 328.0 MHz to 350.9 MHz, while LO power = -10dBm, RF power =-30 dBm, and f_{IF}= 97.5 MHz.

5.3.3.2.3 Performance vs LO power

Now, the LO power is swept from -20 dBm to +12 dBm while RF = -30.0 dBm, f_{Lo}=340.5 MHz, f_{RF}=243 MHz, and f_{IF}=97.5 MHz. Figure 5.32 shows the measured CG for different temperatures as the LO power varies. The CG is saturated at 15.0 dB for LO power of 5 dBm at room temperature and 12.5 dB for LO power of 8 dBm at 250 °C.

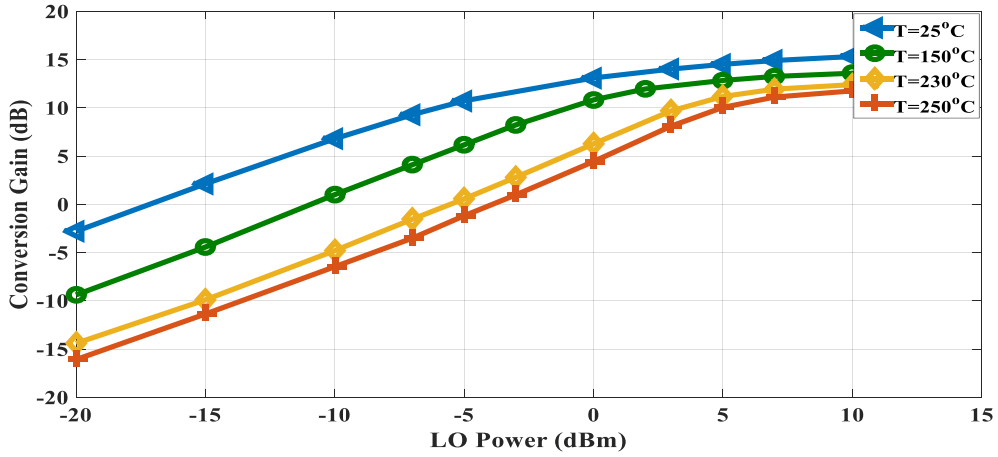


Figure 5.32: Measured CG versus LO power at different temperatures. LO power varies from -20 dBm to 15 dBm, while f_{LO} =340.5 MHz, f_{RF} =243 MHz, RF power = -30 dBm, and f_{IF}= 97.5 MHz.

5.3.3.2.4 Linearity

The linearity of the mixer is also evaluated at room temperature and 250 ºC. A single-tone test is carried out by sweeping the RF power at f_{RF} = 243 MHz and LO power = -10 dBm, and the 1dB compression point is measured at room temperature and 250 ºC. As the temperature increases, the linearity improves at the cost of the CG. The input 1-dB compression point is obtained as -12 dBm at room temperature and -7 dBm at 250 ºC. Figure 5.33 shows the output IF power versus the input RF power at room temperature and 250 ºC.

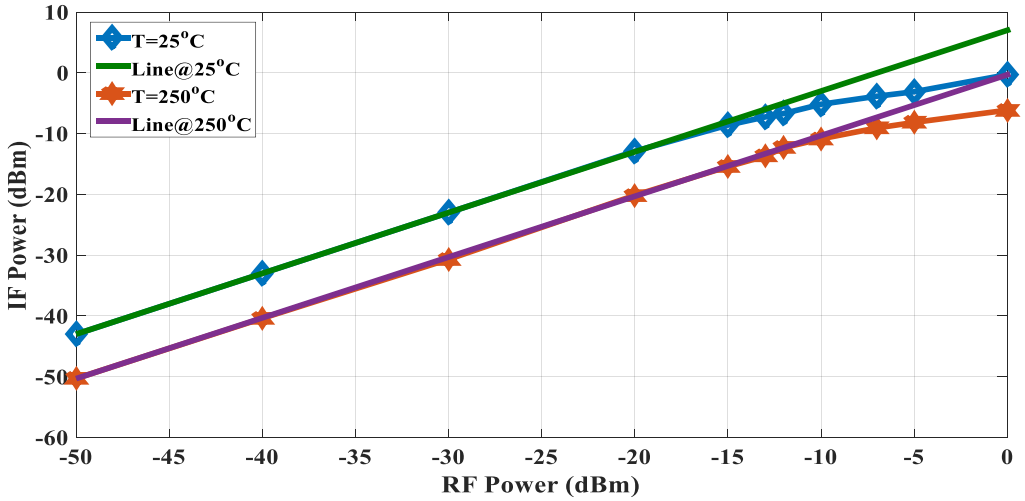


Figure 5.33: Measured IF power versus RF power at 25ºC and 250ºC. f_{LO} varies from 340.5 MHz to 350.9 MHz, while f_{RF} =243 MHz, LO power = -10 dBm, and f_{IF}= 97.5 MHz.

Table 5.3 compares the performance of the proposed mixer with a few relevant active mixers, two at room temperature and one at 85 ^{o}C. The CG of the proposed mixer is lower than the other three mixers. The comparison intends to show only the standing of the proposed mixer performance, but should not be used as a direct comparison of the performance due to different ambient temperature, technology used, and design objectives. Nonetheless, we believe that the proposed mixer achieves good performance with relaxed VCO requirements (LO Power = -10 dBm) at 250 ^{o}C. To our knowledge the proposed mixer is the first one operating at 250 ^{o}C reported in the open literature.

Table 5.3: A performance comparison with state-of-the-art active mixers.

Parameter	[90]	[91]	[92]	This work
Temperature (^{o}C)	25	25	85	**250**
Technology	0.18µm CMOS	0.13µm CMOS	0.18µm CMOS	GaN HEMT
Frequency (GHz)	0.2 ~13	3.1 ~10.6	2.5 -3.5	0.23 ~ 0.25
LO Power (dBm)	5	-3	-	-10
CG (dB)	9.9	9.8 ~14	9.2	6
NF (dB)	11	14.5~19	14	17
Input P1dB (dBm)	-20	-24 ~ -20	-1.5	-7
Power Consumption (mW)	0.88	1.85	5.58	50

5.4 Low Noise Amplifier (LNA)

The low noise amplifier is the main critical building block in the receiver side and the performance of this component determines the overall noise performance of the receiver as we discussed in Section II. The LNA has to provide high gain while adding a little noise. GaN power transistors adopted in this transceiver design have high gain but inherently unstable. Stability techniques need to be considered in designing process. A feedback topology was chosen based on stability and noise tradeoff. This topology unconditionally stabilizes the device over as wide a bandwidth as possible while sacrificing little noise performance. Figure 5.35 shows the proposed

LNA which uses a single-stage common source configuration with resistive feedback and micorstrip matching networks [95].

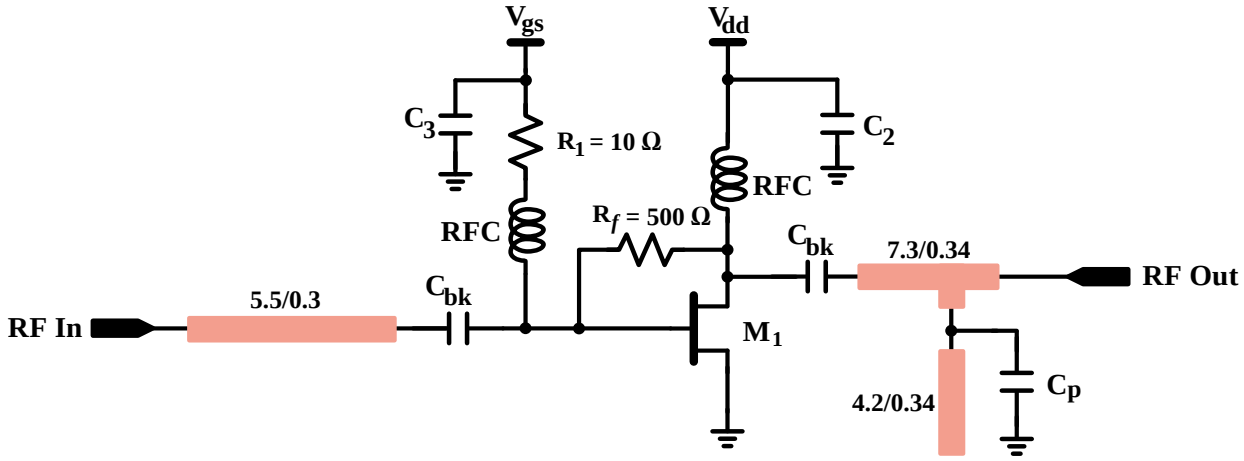


Figure 5.34: Resistive feedback low noise amplifier adopted for the transceiver design. The dimensions are in mm.

5.4.1 Temperature Impact on the LNA Design

For high temperature operation, the design is biased at zero temperature coefficient maximum available gain. At this biasing point the MAG is independent of temperature. MAG for the GaN HEMT device can be expressed as follows:

$$MAG = \frac{{g_m}^2}{4Re(y_{in})Re(y_{out})} \tag{5.13}$$

where g_m is the transcoductance of the transistor, and Re (y_{in}) and Re (y_{out}) are the real input and output impedances of the transistor, respectively. Re (y_{in}) is equal to $R_i C_{gs}^2 \omega^2$ and Re (y_{in}) is equal to drain-source resistance R_{DS}. g_m, R_i, C_{gs} and R_{DS} are temperature dependent. In this design the transistor is biased so that g_m and R_{DS} both increase with temperature and their effects compensate each other and provide stable MAG with temperature. At this bias point the current increases with temperature but it is still below the self-heating limit at 230 ^oC.

The noise figure performance is affected by temperature. The noise factor equations of two-port amplifier giving by [96]:

$$F = F_{min} + \frac{4r_n|\Gamma_s - \Gamma_{opt}|^2}{(1-|\Gamma_s|^2)(1+\Gamma_{opt})^2} \tag{5.14}$$

where r_n is the equivalent normalized noise resistance of the two-port network, Γ_s is the source reflection coefficient, and Γ_{opt} is the optimum source reflection coefficient that results in the minimum noise factor, F_{min}. F_{min} is contributed by the transistor and can be expressed as follows:

$$F_{min} = 1 + K_g \omega C_{gs} \sqrt{\frac{R_s + R_g}{g_m}} \tag{5.15}$$

where K_g is a constant of value 2.5 s/F for HEMT devices, R_s and R_g are the source and gate parasitic resistors, respectively.

The temperature impacts NF mainly in two parts which are the minimum noise figure part and matching part. For F_{min}, as temperature increases, the C_{gs}, g_m, R_s and R_g increase with temperature but the change mostly dominated by the C_{gs} and g_m. The estimated F_{min} for this GaN is ≈ 0.1 dB at 25 ^oC and 0.3 dB at 230 ^oC. The other important effect comes from the matching. As temperature increase the optimum source reflection increases and mainly due to C_{gs} increase with temperature which result in an increase in total noise figure.

5.4.2 LNA Measured Results

Figure 5.35 shows the measured power gain at 25 ^oC, 125 ^oC and 230 ^oC. This average gain at frequency of 250 MHz is 16.142 dB at room temperature and it increases by 0.65 dB at 125 ^oC to reach the maximum gain of 16.808 at the same frequency. Then, it decreases by 0.56 dB at 230 ^oC to reach the gain of 16.25 dB. This temperature variation is mainly attributed to the variation of g_m, C_{GS} and R_{DS} with temperature as we discussed in Chapter 4. For this LNA, the maximum variation of gain across temperature is less than 0.65 dB with average gain of 16.0 dB and therefore the gain performance with temperature is satisfactory.

Figure 5.36 shows the measured NF at 25 ^oC and 230 ^oC. The maximum NF is 1.58 dB at 25 ^oC and 2.8 dB at 230 ^oC, and the performance is also considered satisfactory.

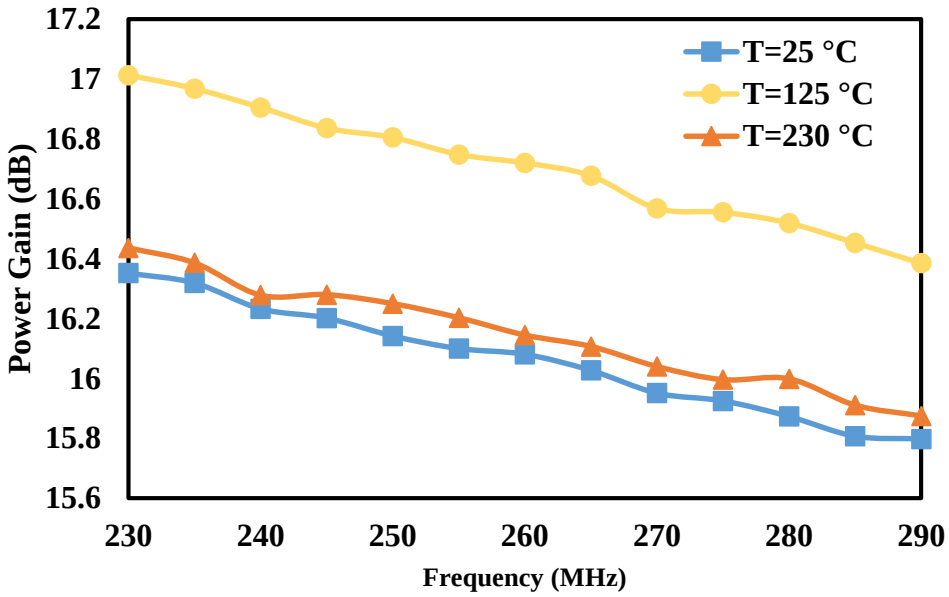


Figure 5.35: Measured power gain for the LNA at 25 ^{o}C, 125 ^{o}C and 230 ^{o}C

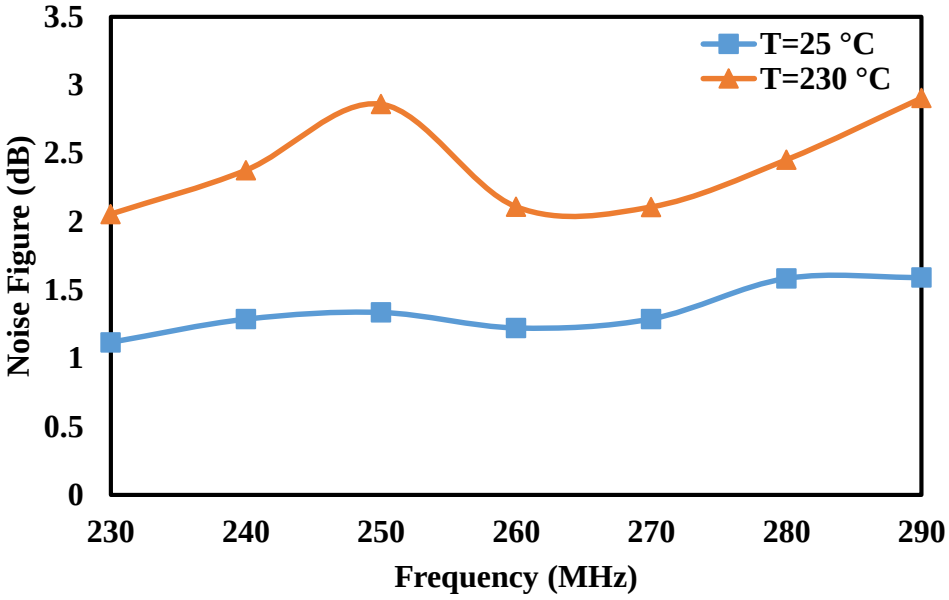


Figure 5.36: Measured NF for the LNA at 25 ^{o}C, 125 ^{o}C and 230 ^{o}C

5.5 Signal Generator

The other important building block for the transceiver design is the signal generator used by the mixers to up and down convert the RF signals. Figure 5.37 shows the proposed signal generator which is a voltage controlled oscillator (VCO) [97]. It is a common source Colpitts

oscillator with two GaN varactors. This topology is chosen mainly due to its simplicity and thermal robustness. A complex circuit is more vulnerable to the temperature variations, which deteriorates reliability at high temperature. A common source configuration enhances the thermal conductivity of the GaN transistor. The biasing condition is chosen so that the thermal effect of the package is minimized and the loop gain of the VCO is large enough to maintain the oscillation at wide temperature range. The transistor is biased at V_{DD} = 2.5 V and V_{gs}=-2.5V and dissipates a maximum current of I_D = 51 mA at RT.

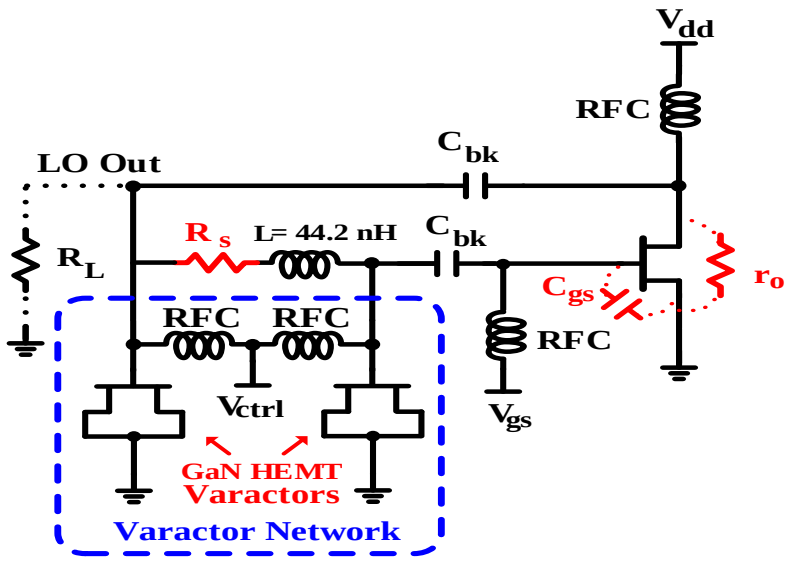


Figure 5.37: Common source Colpitts voltage controlled oscillator with two varactors adopted for the transceiver design.

5.5.1 Temperature Impact on the Signal Generator Design

The loop gain has to be greater than one at all operating temperatures to satisfy the oscillation condition. To ensure the loop gain is equal or greater than unity, the transconductance, g_m, has to be:

$$g_m \geq \frac{C_2}{R_t C_1} \tag{5.16}$$

where R_t is the total resistive loading of the tuned circuit and it comprises the load resistance, R_L, the inductor series resistance, R_s, and transistor output resistance, r_o. C_1 and C_2 are tuning capacitors.

To find the loop gain that allow the transistor to oscillate at wide temperatures, g_m, r_o and R_s are characterized at different temperature ranges. It is found that from the characterization that

the g_m decreases from 159 mS to 114 mS as temperature increases from RT to 230 ^oC. The other temperature dependent parameters are r_o and R_s since the load resistance, $R_{L,}$ is fixed to =50Ω, and assumed temperature independent. It is found that temperature variation of r_o and R_s leads R_t to decrease as temperature increases. R_t is 45 Ω at RT and 30.1 Ω at 230 ^oC. For C_1/C_2 equals to any value between 0.3 and 1, eq (5.16) will be satisfied at all temperatures.

To achieve a wide tuning range, two identical varactors are used in replace of C_1 and C_2. The main motivation for using two varactors is to achieve wide tuning range while minimizing the output power variation over tuning range and with temperature. These varactors are designed using GaN HEMT transistor with their drain and source terminals grounded and gate terminals connected to control voltage through RF chocks. However, it is found that as temperature increases, both the capacitance and quality factor, Q, of the varactrors decrease. These temperature variations affect the oscillation frequency, and the tuning range, and they can be compensated by re-tuning the varactors as temperature increases. In addition, the effect of the gate-source, C_{gs}, which is highlighted in red in Figure 5.37, should be considered. C_{gs} is 2.2 pF at RT and it is connected in parallel with C_2. Therefore, the total C_2 is equal to the capacitance value of the varactor plus C_{gs}. This leads C_1/C_2 =0.77 at all temperatures.

The inductor value is estimated from the oscillation frequency based on the following equation:

$$f_o = \frac{1}{2\pi\sqrt{L\frac{C_1C_2}{C_1+C_2}}} \tag{5.17}$$

At frequency of 340.5 MHz, the inductance value is 44.2 nH. Air coil inductor is designed using high temperature copper wire. However, it is found that as temperature increases, the Q of the inductor decreases. The decline of Q for both the inductor and varactor with temperature degrade the phase noise performance at 230 ^oC.

The temperature effect on phase noise of the VCO design is estimated using (5.18) [98].

$$L\{\Delta\omega\} = 10\log\left[\frac{2FkT}{P_{sig}}\left[1+\left(\frac{\omega_o}{2Q\Delta\omega}\right)^2\right]\left[1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right]\right] \tag{5.18}$$

where $L\{\Delta\omega\}$ is SSB noise spectral in units of dBc/Hz. k is Boltzman's constant, T is temperature in Kelvin, P_{sig} is the power fed to the transistor, ω_o is the oscillation frequency, and $\Delta\omega$ is the offset

from ω_o. Q is the unloaded quality factor of the resonator, F is the noise figure of the oscillator and $\Delta\omega_{1/f}^3$ is the noise corner frequency of the transistor. As temperature, T, increases to 230 ^oC, F increases by 1.5 dB, and P_{sig} decreases by 1.0 dB. Also, Q decreases by 40%. This leads to 6.0 dB increase in the phase noise at 230^{o}C. This increase agrees with the measurements shown later in Figure 5.40. Although there is 6 dB increase at high temperature the performance is still satisfactory since the predicted phase noise at high temperature is better than -109 dBc/Hz at 100KHz offset.

5.5.2 Signal Generator Measured Results

The designed VCO performance is firstly measured at RT. The design is biased at V_{dd} of 2.5 V and gate voltage V_{gs} of -2.5 V. The control voltage, V_{ctrl}, is swept from -6V to 0V. The output frequency changes from 327.5 MHz to 367.7 MHz with tuning range of 40.2 MHz at RT. Then, temperature of the furnace is elevated gradually up to 230 ^oC. As temperature increases the output frequency decreases at given control voltage. Figure 5.38 shows the output frequency versus control voltage at different temperatures. It can be observed that as temperature increases to 230^{o}C, the output frequency ranges from 320.8 MHz to 360.2 MHz, representing frequency shifts by 8 MHz while maintaining the same tuning range of 40 MHz. This frequency shift at high temperatures does not affect the required tuning range for the designed transceiver.

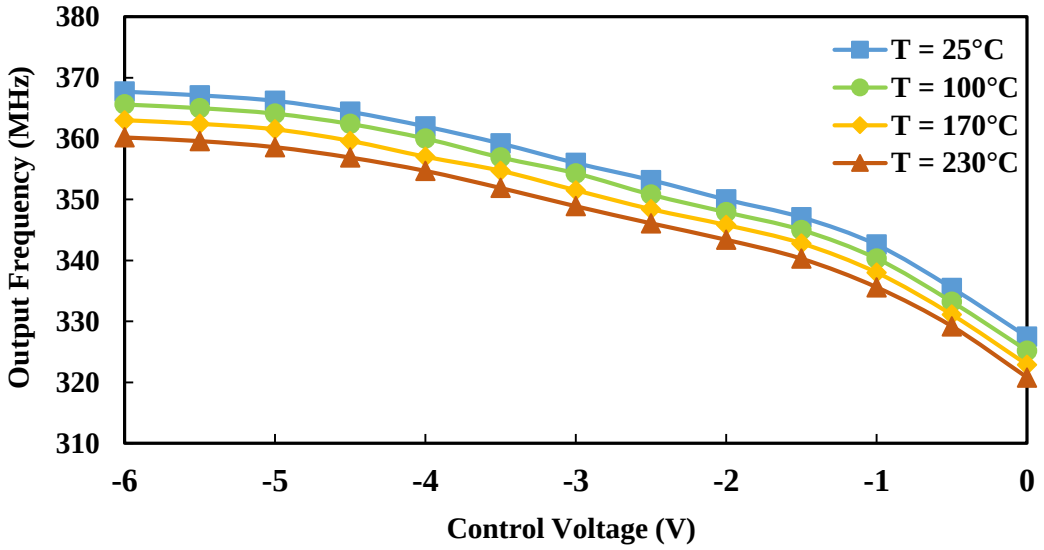


Figure 5.38: Output frequency versus varactor control voltage at different temperatures.

Figure 5.39 shows the output power versus control voltage at 25^{o}C, 100 ^{o}C, 170 ^{o}C and 230 ^{o}C. It can be noticed that the output power of the VCO varies from 18.16 to 19 dBm over the

control voltage at RT, resulting in 0.83 dB maximum variation at RT. This small variation is due to the fact that two varactros being used and tuned at the same time which leads to small variation in the output power. As temperature increases, the output power decreases. The output power of the fundamental frequencies of the VCO varies from 17.11 to 18.0 dBm at 230 ^{o}C, indicating a 0.85 dB variation over the tuning range and 1.5 dB variation with temperature. The amplitude drop with temperature is due to the fact that g_m decreases as the temperature increases.

The harmonics of the VCO has been measured. The second harmonic ranges from -20.46 dB to -25.44 dB below the output power of the fundamental frequency.

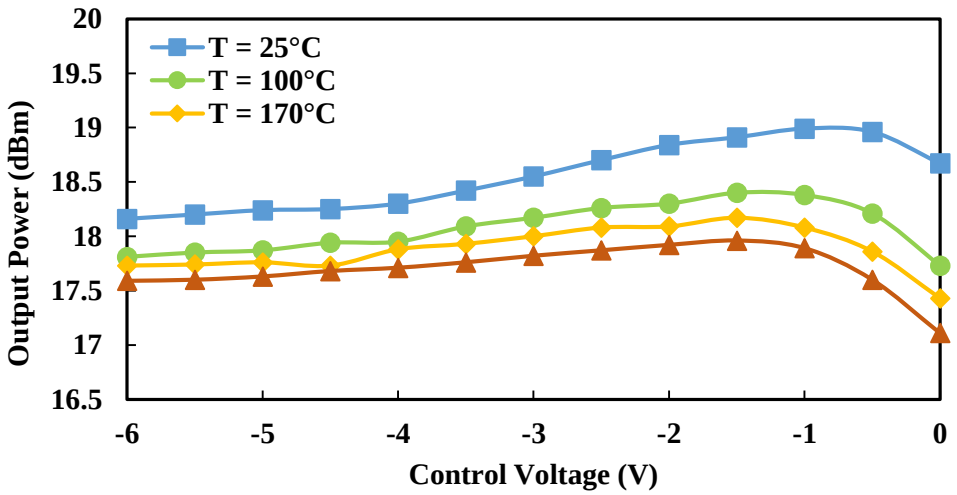


Figure 5.39: Output power versus varactor control voltage at different temperatures.

The phase noise at 100 KHz offset varies from -109 dBc/Hz to-121 dBc/Hz over frequency tuning range. Figure 5.40 shows the phase noise of the VCO at the center of the tuning range at frequency of 340.5 MHz for different temperatures. It can be noticed that as the temperature increases the phase noise increases as it is predicted by (3). The phase noises at frequency offset of 100 KHz are -116.4 dBc/Hz and 110 dBc/Hz at 25 ^{o}C and 230^{o}C, respectively. Although the phase noise deteriorates by 6.4 dB at 230^{o}C, the performance is satisfactory. Also, it can be noticed that there are two peaks in the phase noise between 1 MHz and 10 MHz frequency offset and these are mainly due to the noise generated by the power supply.

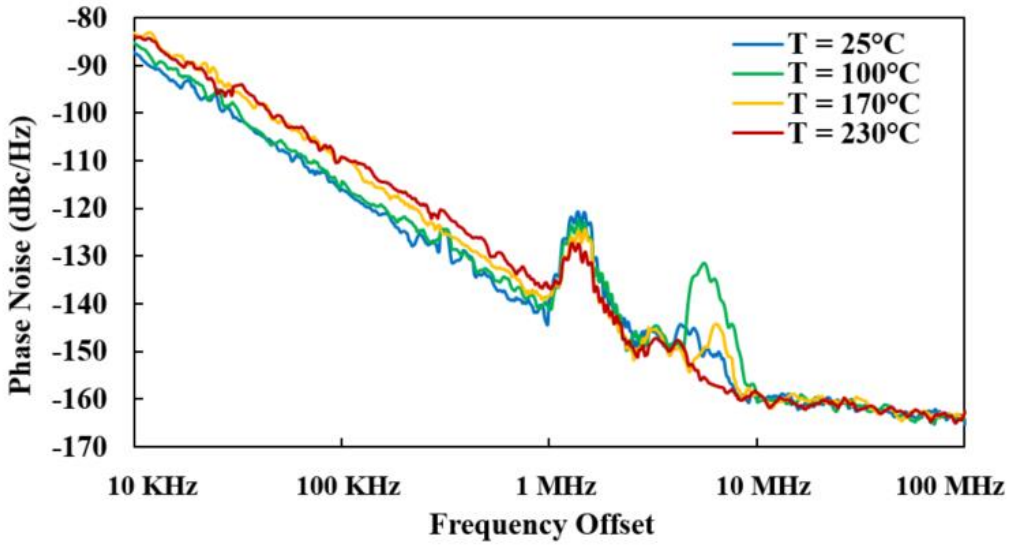


Figure 5.40: Phase noise at different temperatures.

5.6 Power Amplifier (PA)

The proposed PA adopted for transceiver design is shown in Figure 5.41. The PA is designed with a different Qorvo GaN transistor [99]. It is designed with Qorvo T2G6003028-FL GaN on SiC HEMT for its high junction temperature, high gain, and high linearity performance. The suggested bias point in the datasheet is $I_d = 200\ mA$ and $V_d = 28\ V$, which is adopted for the proposed PA. We measured the I-V characteristics for the device at the ambient temperature of 230 °C and verified its ability to operate for class A under the bias point due to a low input signal level.

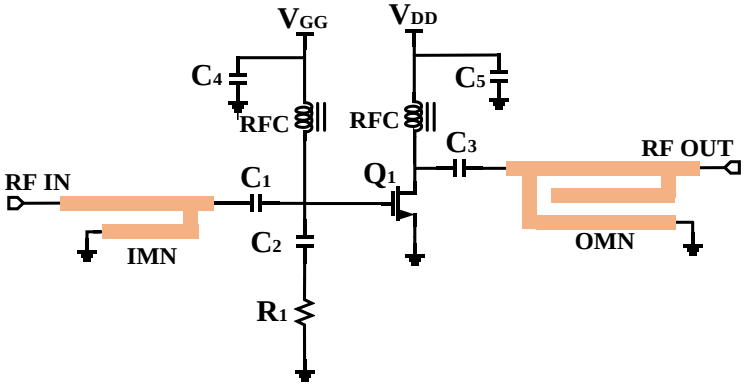


Figure 5.41: Class A power amplifier adopted for the transceiver design

5.6.1 Temperature Impact on the PA Design

The on-board bias tee is formed from the DC blocking capacitors (C_1 through C_3) and RF chokes (RFC). Since there are few choices of COTS passive components for temperatures above 230 °C while meeting the required value, voltage, and/or power rating, some passive components, such as C_3, are implemented with a series connection of three capacitors. The gate resistor R_1 (=50 Ω) intends to increase the stability of the circuit at the cost of a lower gain and an increased noise figure, and the capacitor C_3 is a blocking capacitor.

Due to the temperature stability of the microstrip transmission lines, the input and output matching networks are implemented with microstrips to match impedance to the input and output of the active device. The input and output matching networks is also designed to have a minimal input and output return losses (RL). EM simulations were used to design the networks.

The bias point of the transistor is set to 28 V and 200 mA, which dissipates 5.6 W. Qorvo's T2G6003028-FL GaN on SiC HEMT offers a high $T_J = 275\,°C$ and a low $R_{\theta JC} = 4.0\,°C/W$ among COTS GaN HEMTs. Chemtronics CW7100 thermal paste is chosen for this prototype [100], and it is obtained that $R_{\theta CH} = 0.4\,°C/W$, the thermal resistance from the case to the heat sink, which is estimated using (5.19):

$$R_{\theta CH} = \frac{d}{k \cdot A} \tag{5.19}$$

where d is the thickness of the thermal paste, k is the thermal conductivity, and A is the cross sectional area of the active device. The Wakefield-Vette 423K heat sink is chosen due to its low thermal resistance of $R_{\theta HA} \approx 1.0\,°C/W$. Using those parameters, the ambient temperature T_A = 245 °C can be obtained from (5.1), and the ambient temperature T_A is above the target operating temperature of 230 °C.

5.6.2 PA Measured Results

The bias point of the transistor is dependent on ambient temperature. Figure 5.42 shows the bias gate voltage V_{gs} necessary to maintain the drain current at 200 mA. The gate voltage decreases as the ambient temperature increases. This means that the proposed PA can operate at any temperature below 230 °C by simply adjusting the bias gate voltage.

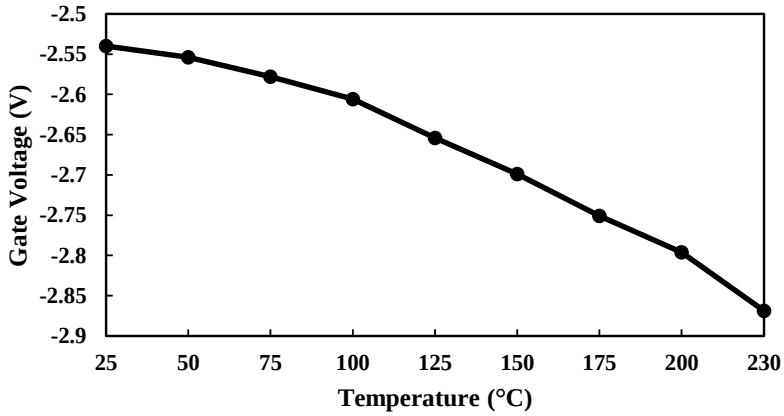


Figure 5.42: V_{gs} versus ambient temperature.

Figure 5.43 shows the gain S_{21}, the input return loss (IRL) S_{11} and the output return loss (ORL) S_{22} at 230 °C. The peak gain is 24 dB at 255 MHz with less than 1 dB ripple in the passband, and the IRL at 230 °C is less than -10 dB for the frequency of interest from 228 MHz to 263 MHz. The ORL at 230 °C is less than -9 dB for the frequency of the interest from 228 MHz to 263 MHz.

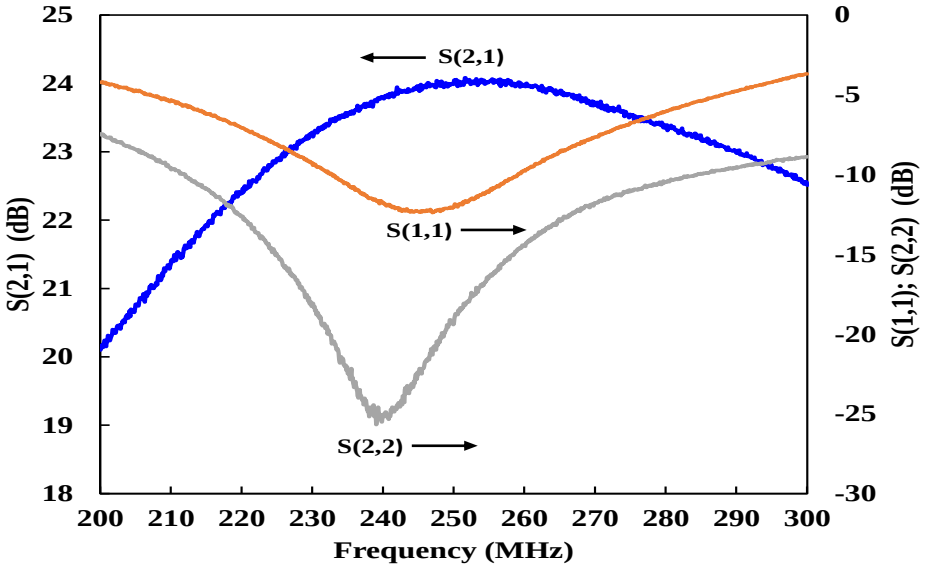


Figure 5.43: Measured gain, IRL, ORL at 230 °C.

Figure 5.44 shows the output and input 1-dB compression (OP1dB and input P1dB) and output and input third intercept points (OIP3 and IIP3) of the PA versus temperature. The linearity performance increases as temperature increases and this is due to the fact the gain of the PA decreases as temperature increases. The OP1dB is about 32 dBm and OIP3 is 38 at 230 °C. The

OIP3 is measured with two tones, 240.4 MHz and 240.6 MHz. The high OP1dB and OIP3 indicate high linearly performance of the proposed PA.

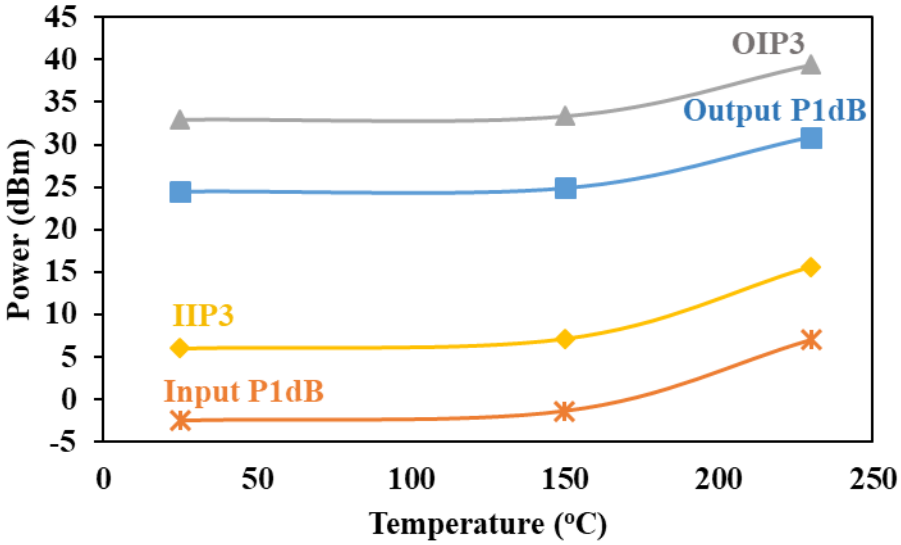


Figure 5.44: Linearity performance of the PA versus temperature.

5.7 Filters

For the proposed transceiver, there will be four filters, which are the image filter and the IF filter for the receiver and the harmonic filter and the IF filter in transmitter. These filters are crucial for the system performance, and they are required to provide stable performance at different temperature in addition to the low insertion loss and high rejection for the out of band frequency requirements. For this work, the RF image and IF filters are designed, with emphasis on temperature insensitive performance while meeting the system requirements [101].

RF and IF filters are critical parts of RF communication systems. Lumped filters suffer from large temperature variations, particularly inductors vary vastly with temperature [102]. Active filter topologies are also undesirable because of the high temperature effects in transistors. Moreover, active filters dissipate power and generate heat. Several passive filter designs were investigated [101]. A combline filter topology shown in Figure 5.45 is selected. Combline filters can be implemented in microstrip, which has less variation with temperature, and also offers compact size, sharp roll-off characteristics, and large separation (about four times of the center frequency) of the second passband from the primary passband [103].

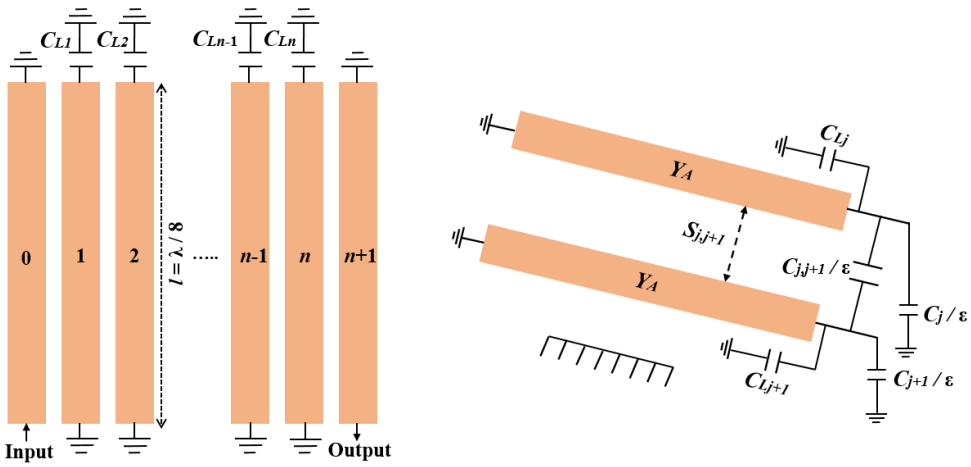


Figure 5.45: Combline filter structure (left) and Self and mutual capacitances of coupled lines in combline filter (right)

Combline filters consist of coupled resonators which are short circuited at one end, with a lumped capacitor between the other end and ground. Lines 0 and *n*+1 provide matching between the input/output ports and the resonators. The order *n* of the filter is equal to the number of resonating stubs. The signal propagates by the means of coupling between those lines. Coupling is achieved through fringing fields that are caused by the mutual capacitance between the lines, and the self-capacitance between the line and ground. The spacing between the lines determines these capacitances, which in turn determines the coupling between lines. The length of the lines is generally $\lambda_0/8$ long, in which the corresponding electrical length is $\pi/4$. Since a $\pi/4$ short circuited stub represents an inductor, the short circuited line with the lumped capacitor can be considered as an inductor and a capacitor in parallel. The resonant frequency is set by the inductance of the stub and the lumped capacitance.

Figure 5.46 shows the RF and IF filters which are designed using Rogers 4003C and 3010 PCBs. The dimensions of the RF filter are 11.5 cm x 5.45 cm shown in Figure 5.46 (a), and the dimensions of the IF filter are 15.7 cm x 2.49 cm shown in Figure 5.46 (b). The third filter shown in Figure 5.46 (c) is designed using 3010 PCBs which has higher dielectric constant ε_r =11.2. The stubs are grounded using screws. The performance of the prototyped filters including insertion loss, return loss, are measured at both at room temperature (25 °C) and 250 °C.

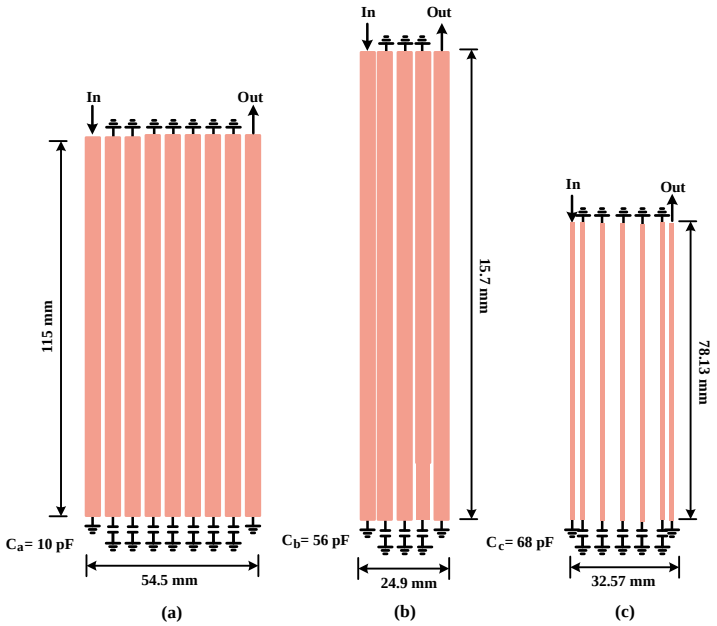


Figure 5.46: Combline filters examples (a) 7th order RF combline filter prototyped with RO4003 PCB that has ε_r =3.55. It has 30 MHz bandwidth (b) 3rd order combline filter operating in IF band prototyped with RO4003 PCB that has ε_r =3.55. It has 10 MHz bandwidth (c) 5th order combline filter operating in IF band prototyped with RO3010 PCB that has ε_r =11.2. It has 4 MHz bandwidth.

The measured insertion and return losses for the RF filter at 25 °C and 250 °C are shown in Figure 5.47. It can be noticed that the 3-dB bandwidth is 30.4 MHz at 25 °C, and 29.1 MHz at 250 °C. The insertion loss increases slightly as the temperature increases. The insertion loss is 3.37 dB at the center frequency of 241.75 MHz at room temperature and 4.55 dB at 250 °C. However, filter rejection improves as temperature increases. The rejection at the frequency of 260 MHz is 40.77 dB at room temperature and 44.28 dB at 250 °C, which represents 4.0 dB improvement at 250 °C. Measured return loss is higher than 12 dB, and it has negligible variation with temperature.

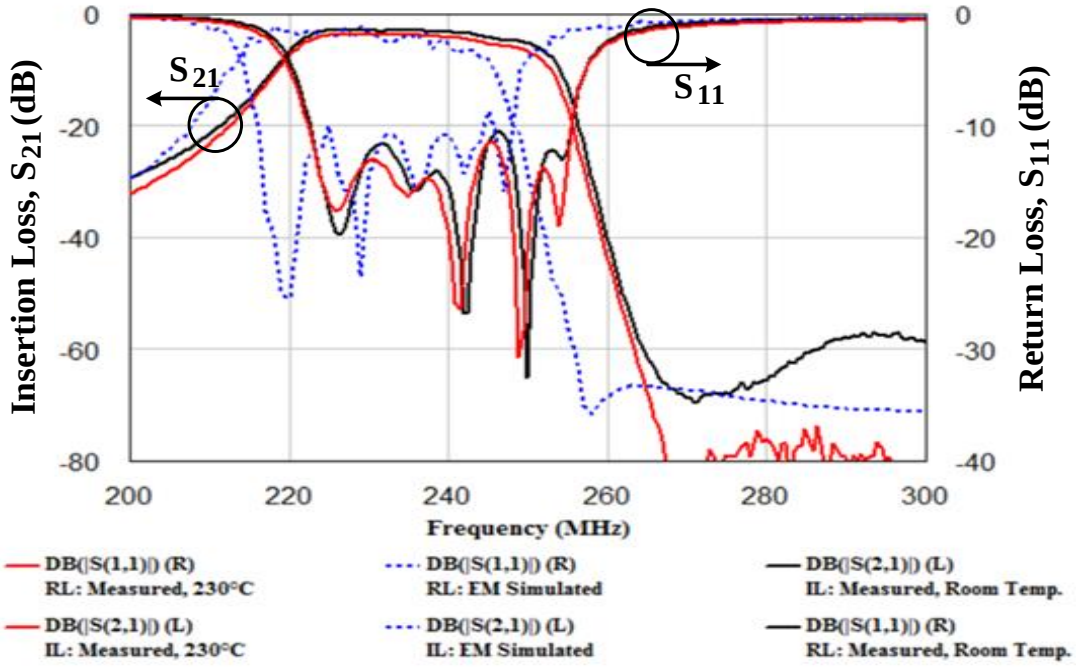


Figure 5.47: Measured insertion and return losses of the RF filter (Figure 5.46 (a)) at 25 °C and 250 °C.

Figure 5.48 shows the measured insertion and return losses for the IF filter. The insertion loss at the center frequency of 97.5 MHz increases by about 0.76 dB from 2.69 dB at room temperature to 3.45 dB at 250 °C. The rejection at the stop band frequency of 125 MHz is 48 dB at room temperature and at 250 °C. Return loss is about 10 dB in the passband and has negligible variation with temperature. Thus, the filters maintain all their characteristics at high temperature.

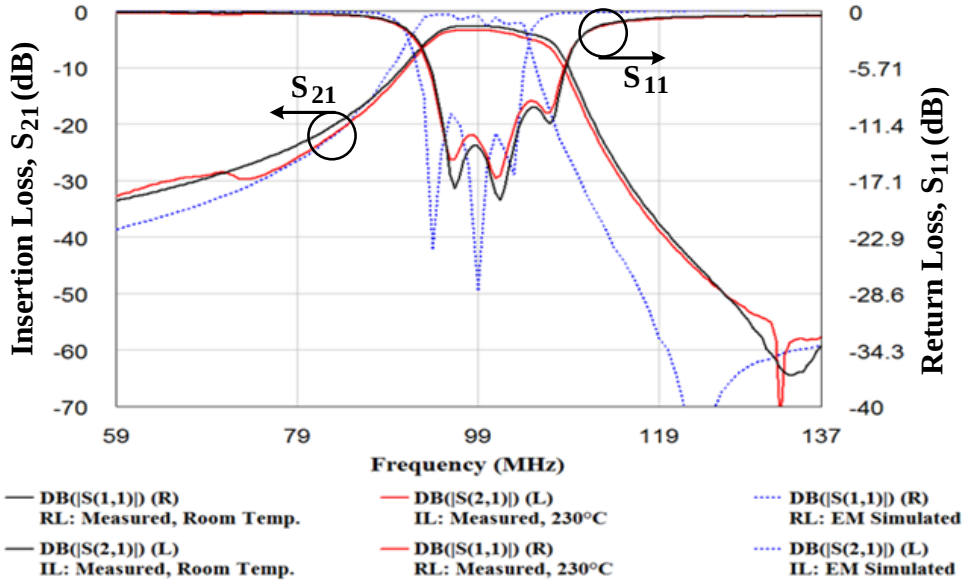


Figure 5.48Figure 5.48: Measured insertion and return loss of IF filter (Figure 5.46 (b)) at 25 °C and 250 °C.

Figure 5.49 shows the simulated insertion and return losses for the 5th order of the IF filter shown in Figure 5.46 (c). The insertion loss at the center frequency of 97.5 MHz is -8.528 dB and the 3-dB bandwidth of this filter is 4 MHz. The rejection at 102 MHz is 40 dB.

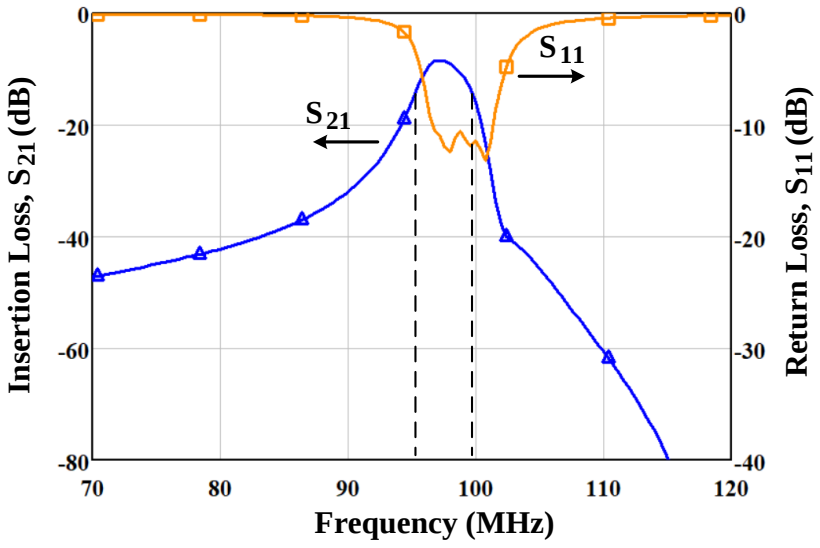


Figure 5.49: Simulated insertion and return loss of IF filter (Figure 5.46 (c)) at 25 °C.

5.8 Diplexer

Figure 5.50 shows the diplexer design adopted for our transceiver. It consists of power divider/combiner and filters for transmit and receive bands to enhance the isolation between the two ports. Both the power divider/combiner and filters are realized in microstrip due to its temperature stability. The power divider/combined adopted for our diplexer is based on unequal power dividing ratio Wilkinson divider presented in [104]. The power division ratio, k, which is the power of the receive band to power of the transmit band is 2. The main motivation for this power division ratio is to reduce the insertion loss for the receive path which improves the total NF of the receiver. The power divider is prototyped using Roger's RO 4003C PCB. The measured results showed that the insertion loss for the power divider's receive port is 1.8 dB and 4 dB for the transmit port. The isolation between the transmit and receive ports is 20 dB. The measured results showed a negligible effect of temperature on the port to port isolation and insertion loss. Figure 5.51. shows the measured insertion loss for the diplexer. The total insertion loss for the diplexer is 5.1 dB in the receive path and 7.3 dB in the transmit path.

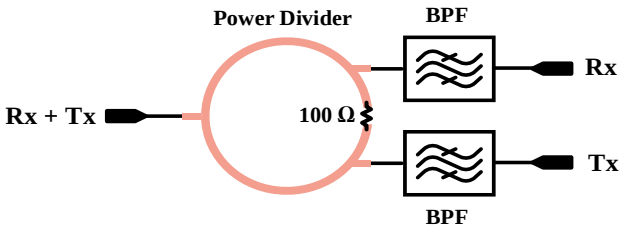


Figure 5.50: Diplexer adopted for the transceiver design.

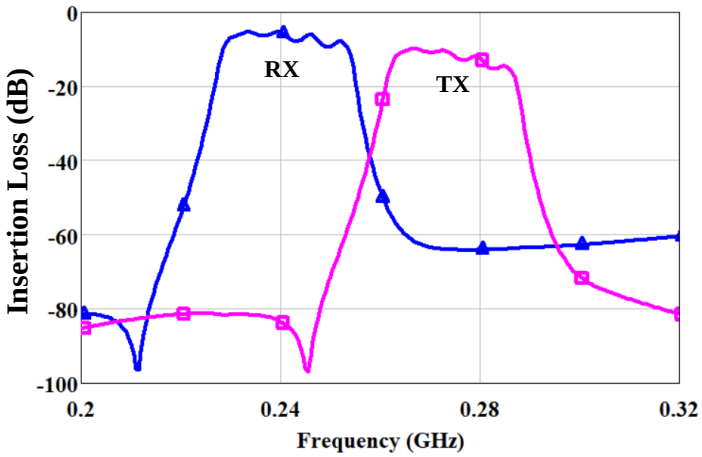


Figure 5.51: Insertion loss for the diplexer.

5.9 Adaptive Bias Circuit

GaN high-electron-mobility-transistor (HEMT) RF devices are used for high temperature RF circuits, and those circuits require temperature compensation techniques to maintain optimum performance at all temperatures. These techniques can be achieved either by optimizing the bias of the design to reach a mutual compensation of the device parameters as we discussed in the LNA design or by applying external temperature dependent biasing that can provide the optimum performance at all operating ambient temperatures. In this section, an adaptive biasing technique and circuit design for GaN HEMT based RF building blocks are proposed.

5.9.1 Block Diagram

Typical GaN transistors operate in depletion mode and require negative bias voltages. Therefore, a DC to DC converter is needed to convert the positive supply voltage to a negative voltage. Then, the generated negative voltage is applied to a temperature dependent bias voltage controller to generate the bias voltage with the required voltage level and temperature coefficient to provide the optimum performance for the RF building block. Figure 5.52 shows the block diagram of the proposed adaptive bias approach.

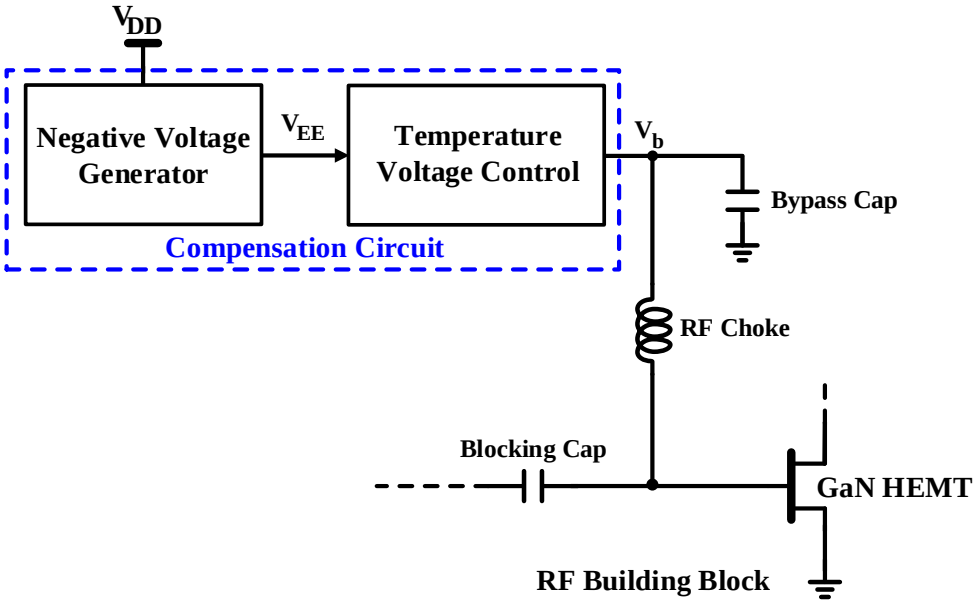


Figure 5.52: Block diagram of the proposed high temperature adaptive bias technique for a GaN HEMT based RF building block.

5.9.2 Circuit Implementation

Figure 5.53 shows the circuit diagram of the adaptive biasing circuit. The negative voltage generator is realized by utilizing multivibrator oscillator to generate a periodic square signal. The periodic signal is then applied to a voltage double to generate a negative voltage. When the oscillator signal is high (V_H) the capacitor C_1 starts to charge. D_1 is shorted while D_2 is open. The maximum voltage on C_1 is the signal amplitude, $V_{H,}$ minus the voltage drop on the diode, D_1. When the oscillator signal is low, the terminal of capacitor C_1 is grounded that makes D_1 open and the D_2 short. Then by applying CVL, V_{EE} becomes:

$$V_{EE} = -(V_H - V_{D1} - V_{D2}) \tag{5.20}$$

Now, V_{EE} is applied to temperature dependent bias voltage control circuit, which will adjust the voltage offset and temperature coefficient of the generated bias voltage. The output bias voltage, V_b can be derived as:

$$V_b = V_{EE} + \left(\frac{R_2}{R_3} + 1\right) V_{BE} \tag{5.21}$$

where V_{BE} is the base-emitter voltage of the BJT and V_{EE} and V_{BE} are temperature dependent.

V_{BE} of the SiC BJT can be expressed by:

$$V_{BE} = V_T \ln\left(\frac{\alpha I_E}{I_S}\right) \tag{5.22}$$

where V_T is thermal voltage, I_S is the saturation current, I_E is the emitter current, and α is the current ratio.

Substituting (5.22) into (5.21), we obtain:

$$V_b = V_{EE} + V_T \left(\frac{R_2}{R_3} + 1\right) \ln\left(\frac{I_C}{I_S}\right) \tag{5.23}$$

The overall temperature coefficient of V_b can be adjusted by controlling the V_T through the resistors ratio of R_2 and R_3 and I_C.

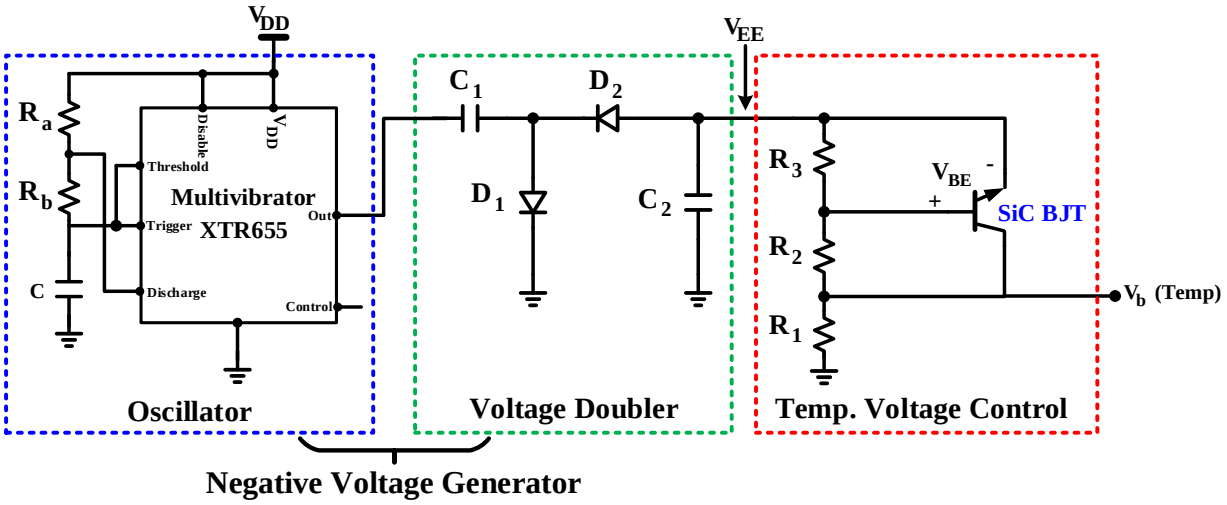


Figure 5.53: Circuit diagram of the proposed high temperature adaptive biasing circuit for a GaN HEMT based RF building block.

For high temperature implantation, XTR655 multivibrator manufactured by XREL semiconductor is used [105]. The specified temperature in the datasheet is up to 230 ^{o}C. Diodes and capacitors high temperature is also used. SiC biploar junction transistor (BJT) from GeneSiC Semiconductor [106] is used and high temperature models used in the simulation. Their model is verified up to 250 ^{o}C. The capacitor values need to be chosen so that they provide small charge time and low ripples. In our design, C_1 = 10 nF and C_2 = 22 nF found to provide reasonable charging time and low ripples. These capacitors are temperature independent and can be found in [107]. Vishay resistors with very low TC is also used [108].

5.9.3 Simulation Environment and Results

A behavioral model for XTR655 multivibrator is used. A SiC transistor GeneSiC GA05JT01-46 is chosen for the design [106], and its temperature effects are investigated. Figure 5.54 shows simulation results on collector current versus temperature under various base currents. As the temperature increases, the collector current decreases for a given base current. It can be noticed that the slope of the I_C changes as I_B changes.

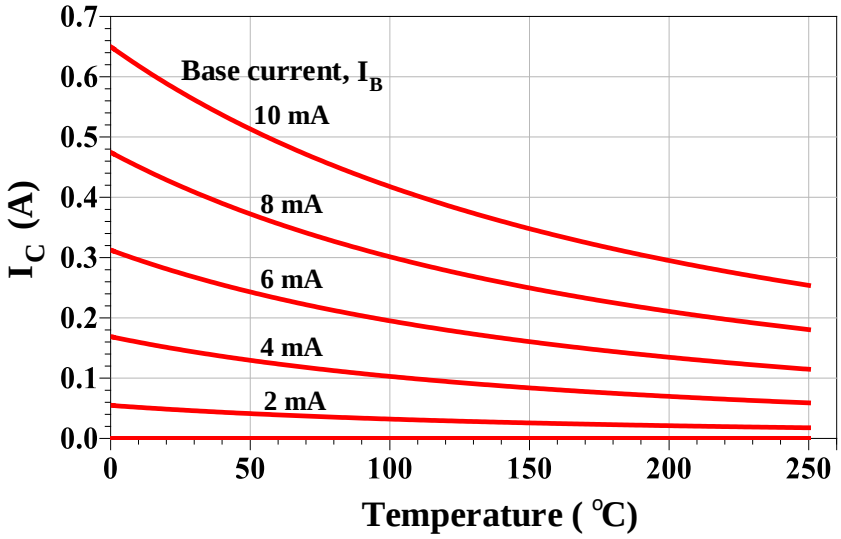


Figure 5.54: Collector current versus temperature at different base current.

Next, the adaptive bias circuit is simulated with different resistors ratios. Figures 5.55 and 5.56 shows the effects of R_1 and R_3 on temperature coefficient of the generated bias voltage. It can be noticed from both figures that R_1 and R_3 can set a wide range of TC value for the V_b.

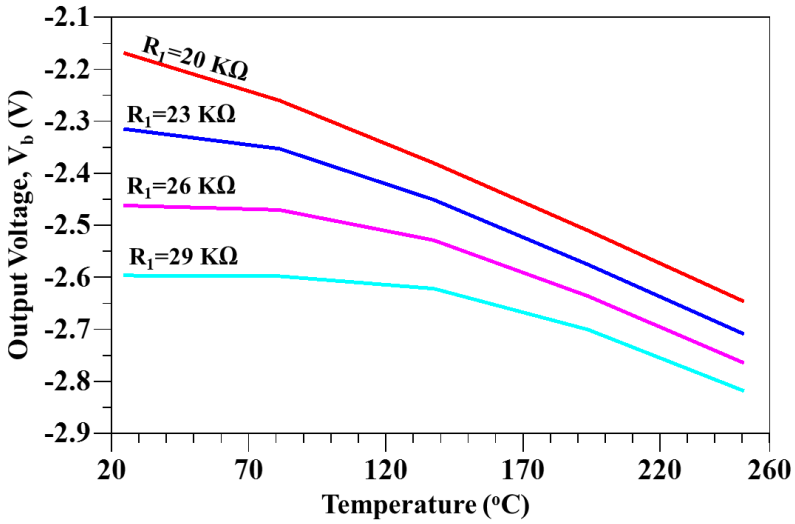


Figure 5.55: The output voltage versus temperature with R_1 being swept from 20 KΩ to 29 KΩ and R_2 and R_3 are fixed to 0.7 KΩ and 23 KΩ, respectively.

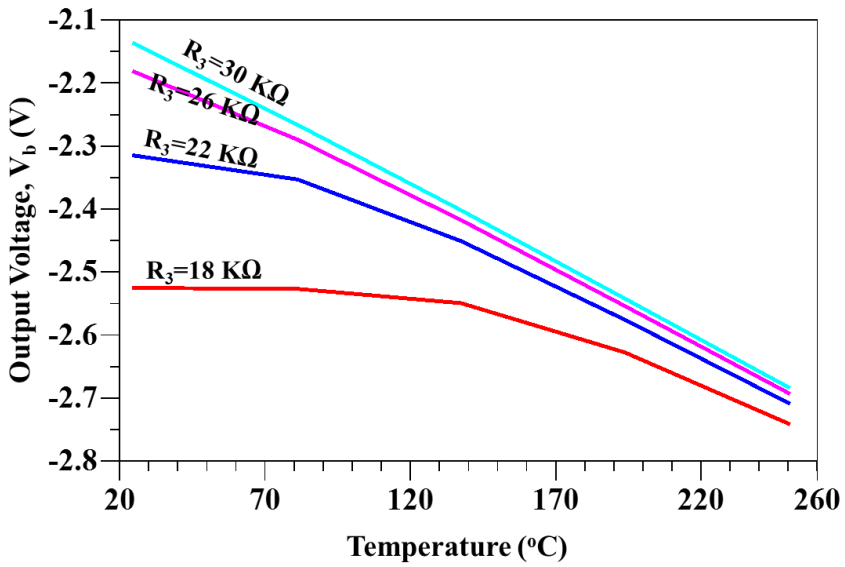


Figure 5.56: The output voltage versus temperature with R_3 being swept from 18 KΩ to 30 KΩ and R_1 and R_2 are fixed to 22 KΩ and 0.7 KΩ, respectively.

The voltage offset of the generated bias voltage can be adjusted by controlling V_{EE} and R_2. Figure 5.57 shows the effect of R_2 on the voltage offset of the V_b. It can be noticed by changing R_2, a fine tuning for the voltage offset can be obtained.

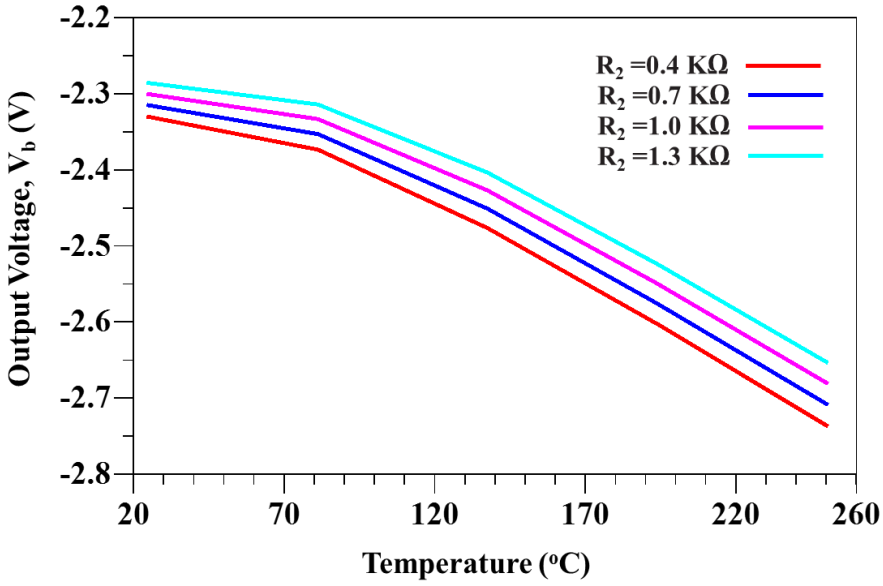


Figure 5.57: The output voltage versus temperature with R_2 being swept from 0.4 KΩ to 1.3 KΩ and R_1 and R_3 are fixed to 22 KΩ and 23 KΩ, respectively.

Next, the adaptive bias circuit is optimized to be applicable to the passive mixer bias presented in section 5.2. Figure 5.58 shows the simulation results of the compensation circuit along with an example of the required bias voltage of an RF building block which is passive mixer. It can be noticed that the simulation and required bias voltage are very close from each other. The resistor values that provide the simulated bias voltages are R_1 = 22 KΩ, R_2=0.7 KΩ, and R_3 = 23 KΩ and temperature independent, Vishay resistors have very small TC [108] and used in this design. The current consumption at V_{DD}=6V and V_{EE} = -4.5V for the temperature voltage bias controller is shown in Figure 5.59. Transient response for the compensation circuit is shown in Figure 5.60. The circuit reached the steady state after 0.15 mS.

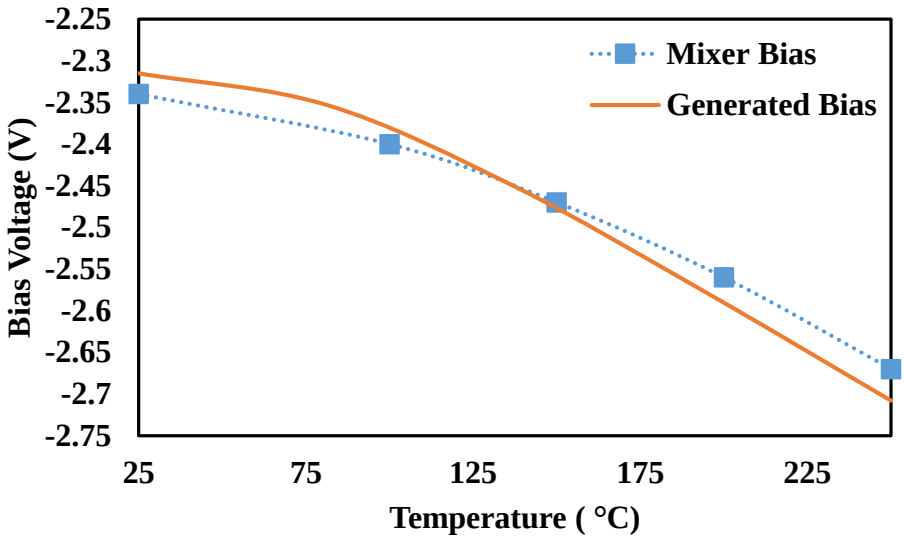


Figure 5.58: An example for a biasing requirement for a RF mixer with the simulation results of the proposed adaptive bias circuit.

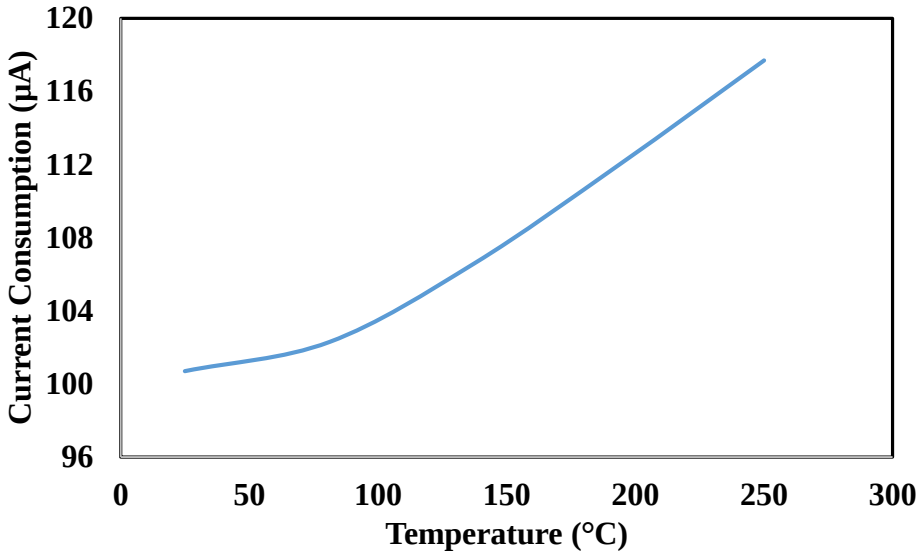


Figure 5.59: The current consumption for the temperature voltage controller circuit.

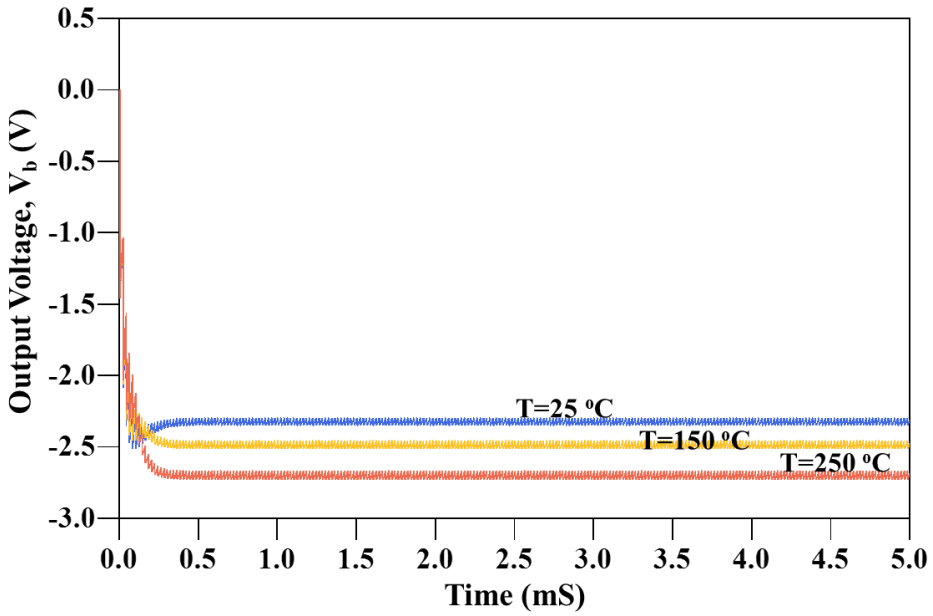


Figure 5.60: Transient response for the adaptive bias circuit.

To summarize, the proposed adaptive bias circuit can be applicable to any of the GaN based RF building blocks up to 250 ºC. The TC of the generated bias can be controlled by the resistors ratio of the bias controller and voltage level can be fine-tuned by controlling R_2.

5.10 Chapter Summary

In this chapter, the design and analysis of the building blocks were introduced. First, we presented high temperature design considerations that include the thermal analysis for the packaged device along with a PCB/heatsink, and passive component selection. Then, we elaborated on the resistive mixer design which is used in the transmitter design as an upcnverting stage. Detailed analysis and verified by measurements was presented. The analysis was carried out using the high temperature R_{DS} model was developed in chapter 4. Furthermore, the bias voltage that provides optimum performance at a wide temperature range was predicted using the analysis and verified though measurements. Next, the active mixer which is used in the receiver as a downconversion stage was also elaborated. The impact of temperature on conversion gain and noise figure was discussed. Then, bias voltage for the optimum conversion gain and noise figure performances at a wide temperature range was identified through measurements. Then, analysis and measurements for the low noise amplifier, signal generator, power amplifier, filters and diplexers were presented. Finally, a novel adaptive bias circuit for depletion mode GaN based RF building block was proposed. The concept was first explained through block diagram. Then, the circuit implementation and temperature analysis was presented. The performance was verified through simulation. The adaptive bias circuit provides temperature dependent bias voltage that closely matches the optimum bias voltage required by the resistive mixer. The temperature coefficient of the output bias voltage can be easily adjusted by changing the resistors ratio of the controller to match the bias voltage for the other building blocks.

Chapter 6 Transceiver Prototype and Measurement Results

This chapter presents the prototyped of the integrated receiver and transmitter. Next, the measurement setup and environment for the prototyped transceiver is introduced. Lastly, the measurement results for the performances of the signal generator, the prototyped receiver and transmitter at temperatures up to 230 ^{o}C are presented.

6.1 Transceiver Prototype

Figure 6.1 shows the final transceiver circuit diagram. Then, the transceiver is prototyped and assembled together. The final transceiver prototype is shown in Figure 6.2. The receiver is highlighted in green and the transmitter is highlighted in blue. The signal generator which is a VCO with buffer is shared by the receiver and transmitter. Both the receiver and transmitter are connected to the diplexer which in turns connected to a coaxial cable. All building block are implemented on Rogers 4003C with dielectric constant of 3.4 and 3010 boards with dielectric constant of 10.2. These board are selected, as they have negligible expansion for increased temperature and <1% change in relative dielectric constant. PA design is prototyped with T2G6003028-FL GaN on SiC HEMT for its high junction temperature, high linearity, and high power capabilities. The other building block are prototyped with Qorvo T2G6000528-Q3 packaged with 0.25µm GaN on SiC HEMT due to low noise and low power consumption characteristics. In order to reduce thermal limits and thermal noise, heat sinks with a thermal resistance of ~1 °C/W are used for the LNA and PA blocks. For example, the heat sink of the LNA reduces the overall junction-to-ambient thermal resistance to about 30 °C/W.

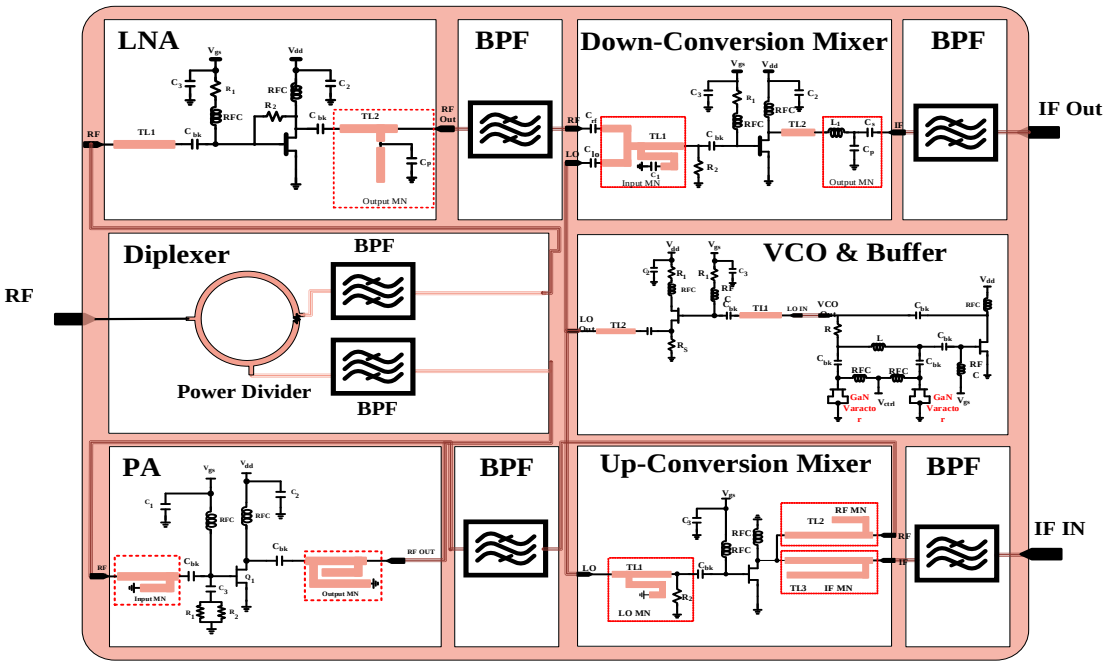


Figure 6.1: The final Circuit diagram for the transceiver.

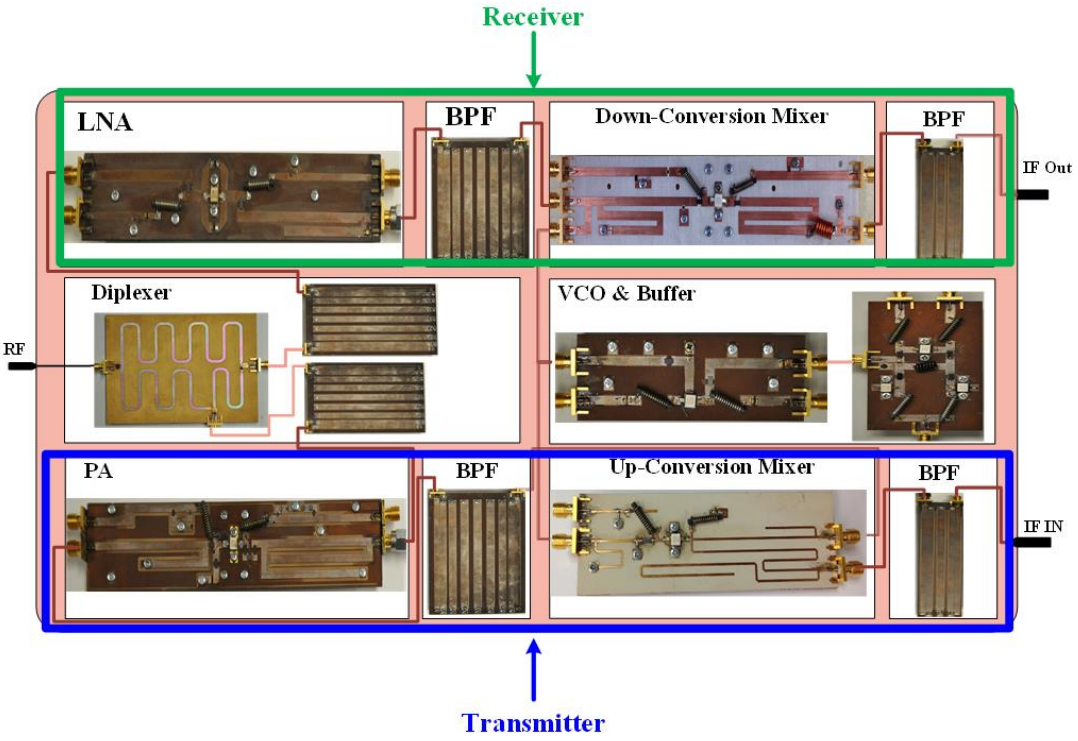


Figure 6.2: The final transceiver prototype.

6.2 Experiment Objective and Setup

After initial testing and tuning for the individual building blocks, the receiver and transmitter boards are integrated and tested. The main goal of this experiment is to investigate the effect of temperature on the transmitter and receiver performances in terms of error vector magnitude (EVM), bit error rate (BER), adjacent channel power ratio (ACPR), and phase noise. For this purpose, each of the receiver and transmitter boards is placed separately inside a Yamato natural convection drying furnace and connected to the instruments through special high temperature cables and connecters. Figure 6.3 shows the measurement setup for the EVM and BER, and ACPR measurements.

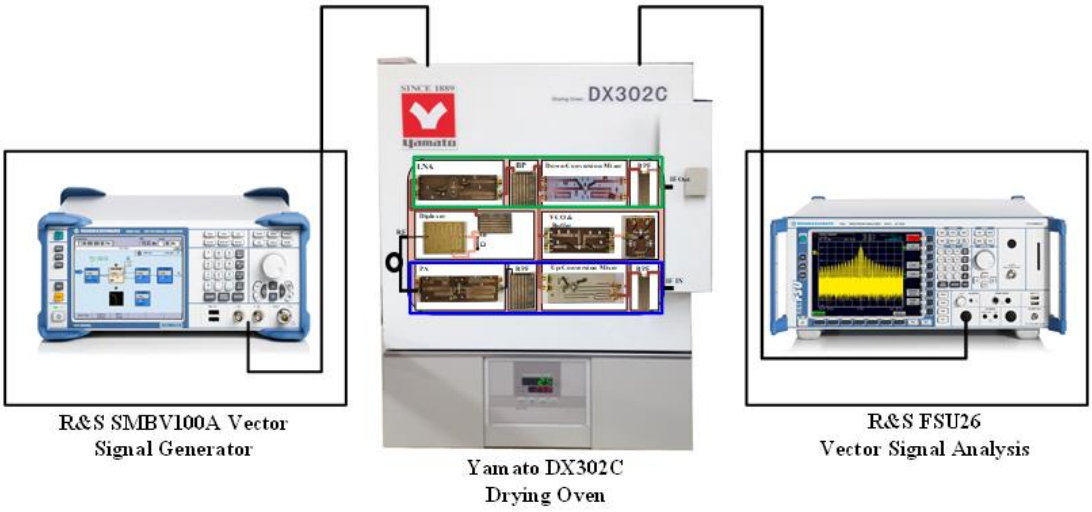


Figure 6.3: The measurement setup for BER, EVM and ACPR.

For the receiver measurements, R&S SMBV100A vector signal generator is connected to the diplexer input and the receiver is connected to the receiver port of the diplexer. The transmitter port of the diplexer is terminated with 50 Ω. The IF port of the receiver is connected to R&S FSU26 spectrum analyzer. Then, the EVM and BER are measured.

For the transmitter measurements, the vector signal generator is connected to the IF input port and the output of the transmitter is connected to the TX port of the diplexer. While the RX port is connected to 50 Ω, the main port of the diplexer is connected to R&S FSU26 spectrum analyzer. The same procedure is for the transmitter measurements.

6.3 Measurement Results

In this section, measurement results at high temperature for the signal generator with different carrier frequencies, the receiver, and transmitter are reported. Then, the temperature impact on the transceiver performance is discussed.

6.3.1 Signal Generator

The signal generator, which consists of Colpitts voltage controlled oscillator and buffer connected to the VCO output, is utilized by the receiver and transmitter. The signal generator is characterized at different channels and at temperatures up to 230 ^{o}C. Figure 6.4 illustrates the measured output power of the signal generator at frequency of 340.0 MHz. The output power after adding the buffer drops to 3.79 dBm with less than 1 dB variation across the frequencies. Figure 6.5 shows the measured phase noise of the signal generator at frequency offset of 100 KHz for different carrier frequencies and temperatures. It can be noticed that as temperature increase the phase noise deteriorates and it degrades by 4 dB at 230 ^{o}C and this aligns with the estimation using eq (5.17). Furthermore, the phase noise improves as the carrier frequencies increase and this is mainly due to the fact that varactor quality factor increases with frequency. Figure 6.6 shows the phase noise at frequency offset of 1 MHz for different carrier frequencies and temperatures. It can be seen that the phase noise increases by 6 dB at 230 ^{o}C

During the measurements, it is found that each carrier frequency is linearly dependent on temperature. Therefore, the control voltage has to be decreased as temperature increases in order to keep the same frequency. For example, the control voltage needed to generate 343.0 MHz is -1.15 V at room temperature and -2.1 V at 230 ^{o}C. Figure 6.6 shows the required control voltage versus temperature for each carrier frequency. It can be observed that the control voltage is linearly dependent on temperature for each carrier frequency.

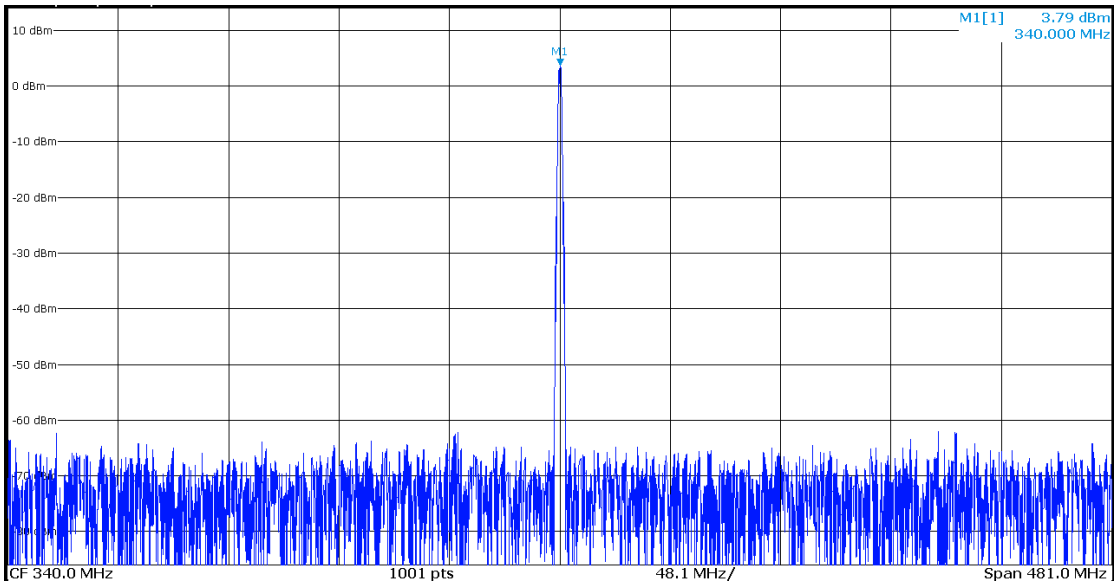


Figure 6.4: The output power for the signal generator (VCO plus buffer) at 230.0 ^{o}C. The output power is 3.79 dBm at f=340.0 MHz.

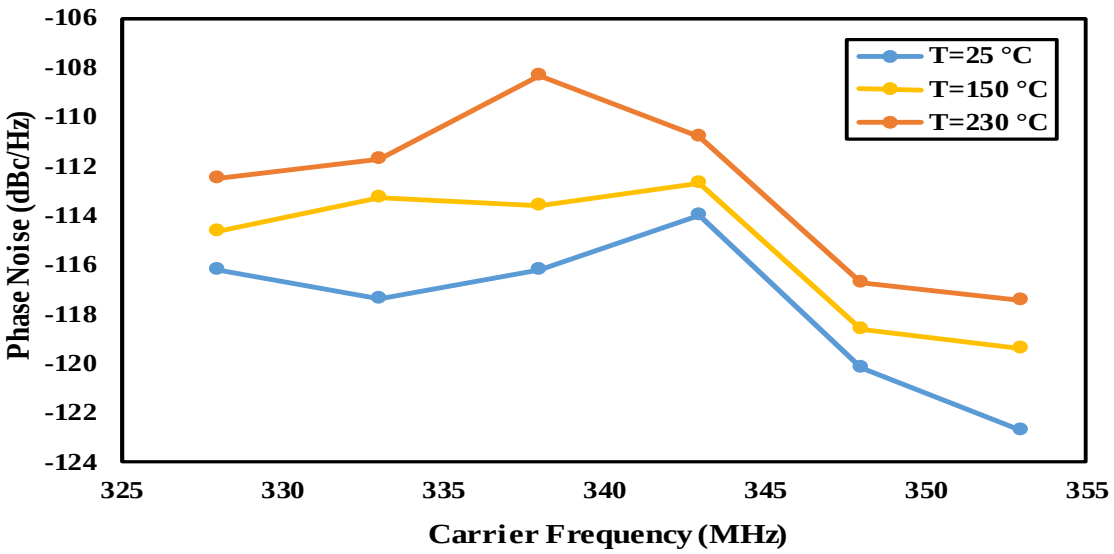


Figure 6.5: Phase noise for different channels at frequency offset of 100 KHz.

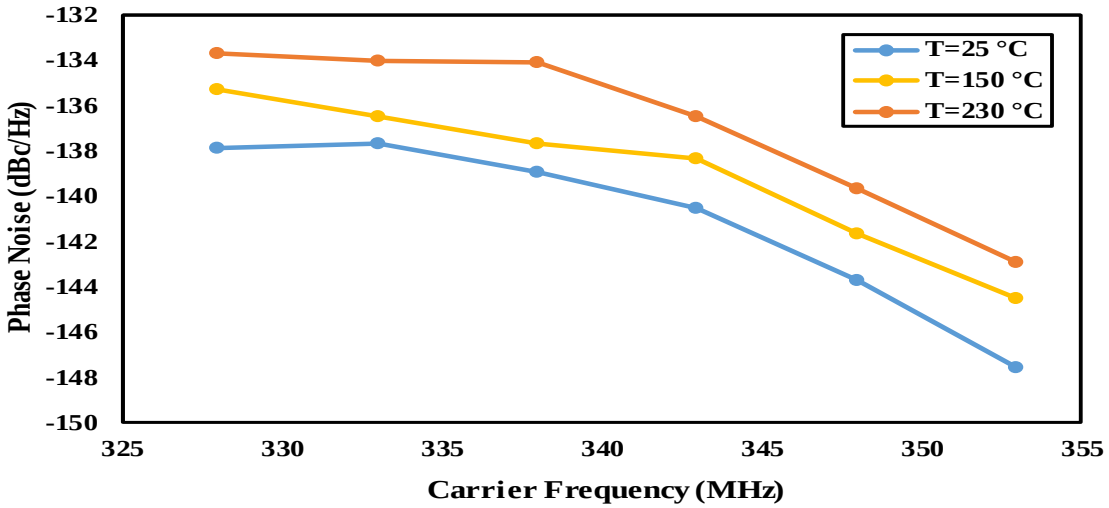


Figure 6.6: Phase noise for different channels at frequency offset of 1.0 MHz.

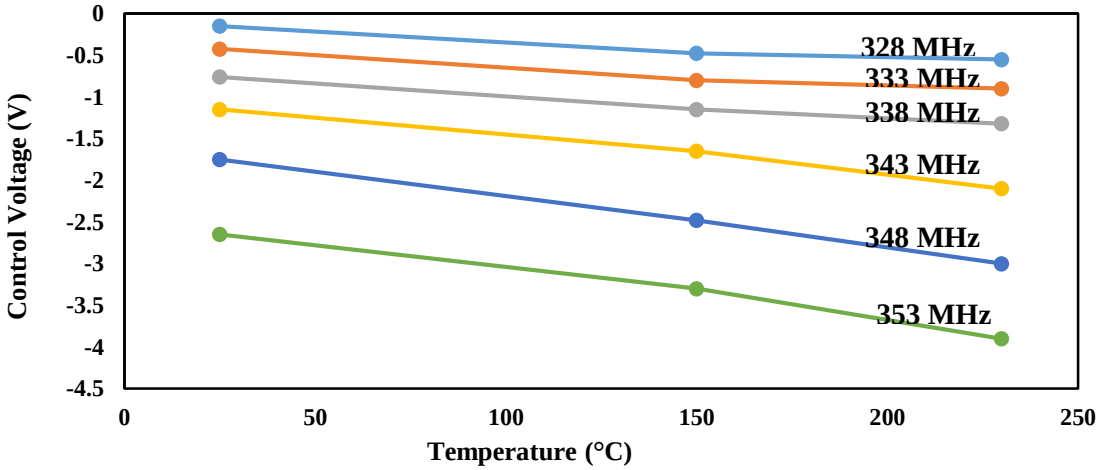


Figure 6.7: Required control voltage to maintain the output frequency of the signal generator at different temperatures.

Another important observation is that we noticed that frequency drift changes based on the control voltage applied. Generally, the drift improves as control voltage become more negative. Also it improves as temperature increase. The measured frequency drift is 55 kHz and 35 KHz at 25 ^{o}C and 230^{o}C, respectively.

6.3.2 Receiver

All building blocks of the receiver are connected together including the signal generator and placed inside the furnace. BER and EVM are measured at different temperatures and input power levels. Figures 6.8 and 6.9 show the measured constellation diagrams, EVM and BER for the receiver front-end with 16 QAM and 64 QAM modulation schemes, respectively at temperatures of 230 ºC. The output of the receiver, the output of the IF filter, is connected to FSU vector signal analyzer. The power level of the input of the receiver is -25 dBm and data rate is 13.2 Mbps for 16 QAM and 19.8 Mbp for 64 QAM. The result length of the FSU is set 148 symbol and the data for the input signal is PRBS 21.

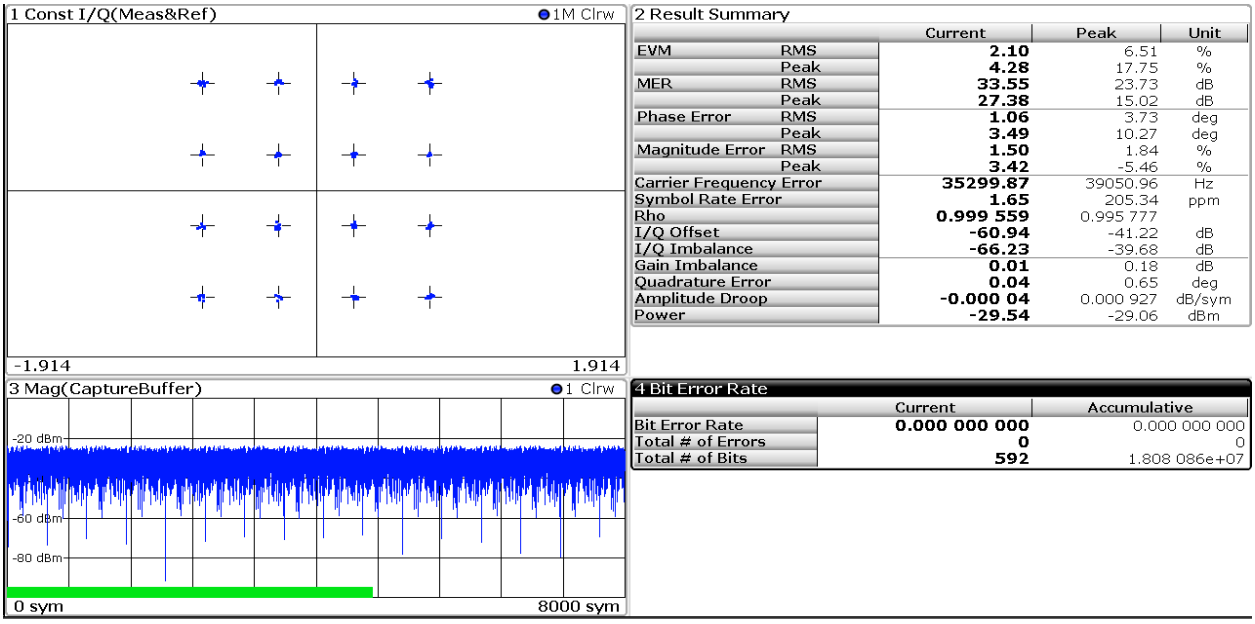


Figure 6.8: The measured constellation diagram and BER for the receiver front end with 16 QAM modulation scheme at temperatures of 230 ºC. The power level at the input of the receiver is -25 dBm and data rate is 13.2 Mbps. This is tested at RF signal of 245.5 MHz, LO frequency of 343.0 MHz and IF frequency of 97.5 MHz.

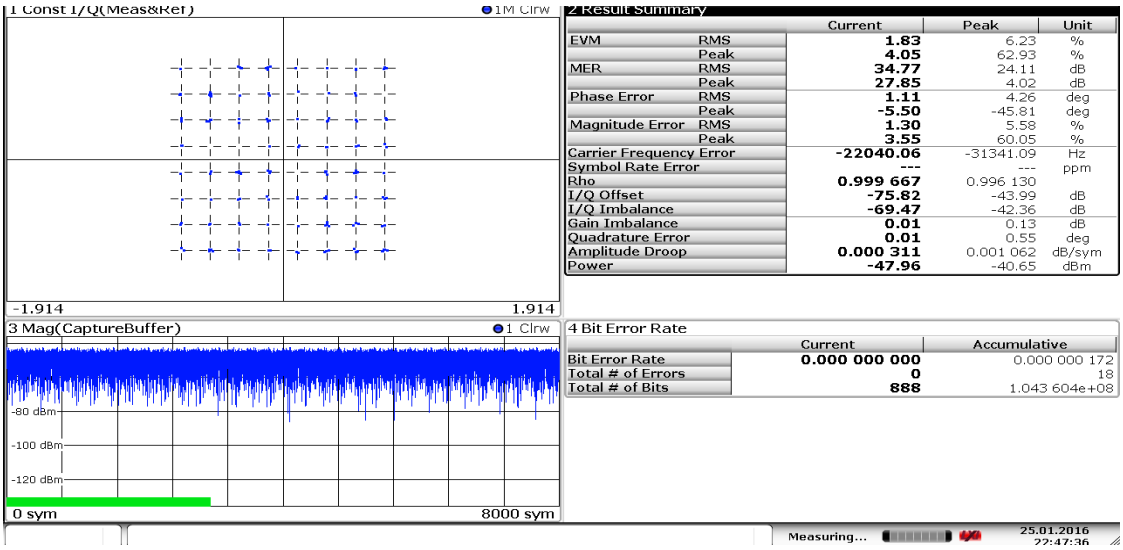


Figure 6.9: The measured constellation diagram and BER for the receiver front end with 64 QAM modulation scheme at temperatures of 230 ºC. The power level at the input of the receiver is -25 dBm and data rate is 19.8 Mbps. This is tested at RF signal of 245.5 MHz, LO frequency of 343.0 MHz and IF frequency of 97.5 MHz.

Figure 6.10 shows the measured spectrum of the signal at the output of the receiver front end. The signal symbol rate is 3.3 and the roll off of the RRC filter is 0.2. The average power is -30 dBm. It can be noticed that the adjacent channel power ratio (ACPR) is -70.0 dB at 3 MHz offset from the center frequency.

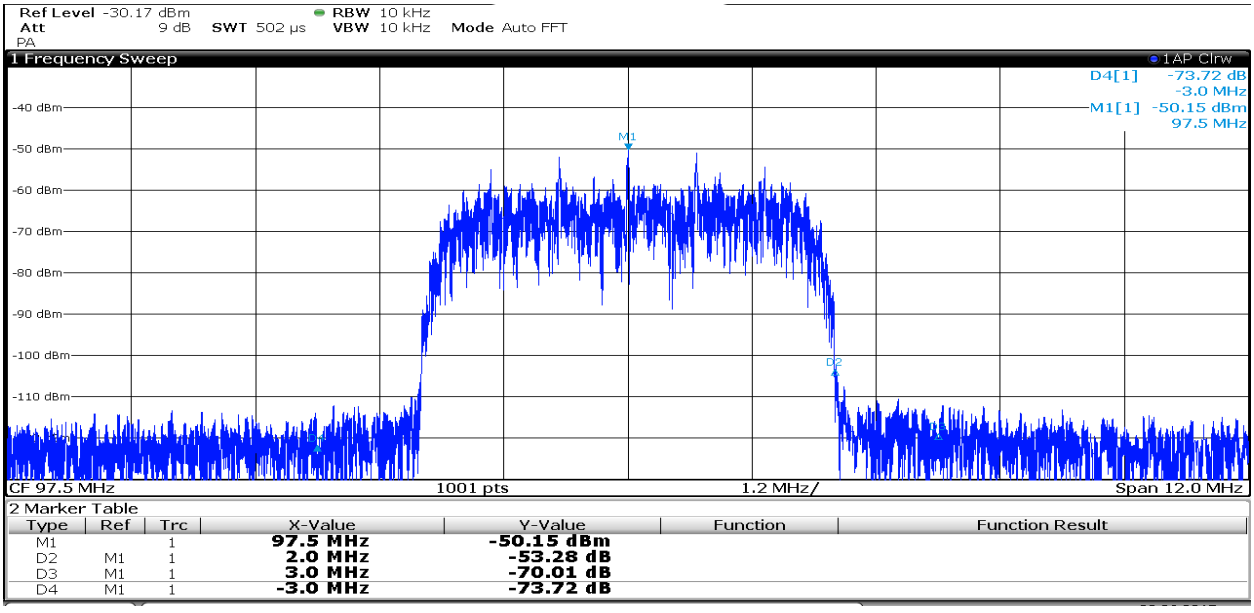


Figure 6.10: The measured spectrum of the received signal at the output of the IF filter. The input signal of the receiver front-end is 64 QAM with average power of -55 dBm.

The BER and EVM of the receiver front-end is measured for the receiver at different received power level with different quadrature modulation (QAM) schemes. This helps to identify the minimum detectable signal that can the receiver front-end detect with minimum BER and EVM and the maximum signal that can the receiver front-end handle without deteriorating the BER and EVM.

Figure 6.11 shows the measured BER versus the average received power level for 16 QAM scheme. The bit rate for the received power signal is 13.2 Mbps. The average received power is swept from -80.0 dBm to 10.0 dBm at different temperature levels. It can be noticed that the minimum received power that provide BER of less than 10^{-6} is -66.0 dBm at room temperature and 230 ^{o}C and increases to -60.0 dBm at 150 ^{o}C. The maximum received power that provides the same targeted BER is -3.0 dBm at room temperature and 230 ^{o}C and drops to -10.0 dBm at 150 ^{o}C. The dynamic range which is the difference between the maximum detectable signal with BER of less than 10^{-6} and the minimum detectable signal with the same BER, is 63 dB at room temperature, 50 dB at 150 ^{o}C, and 61 dB at 230 ^{o}C. The significant performance variations at 150 ^{o}C is mainly due to the fact the matching performance of the LNA is optimized at 230 ^{o}C and the gain of the LNA is observed to be higher at 150 ^{o}C (see Figure 5.35). A higher LNA gain and almost fixed P1dB compression point of the mixer at 150 ^{o}C both leads to the performance to be compressed at lower power level compares with the cases in room temperature and 230.0 ^{o}C

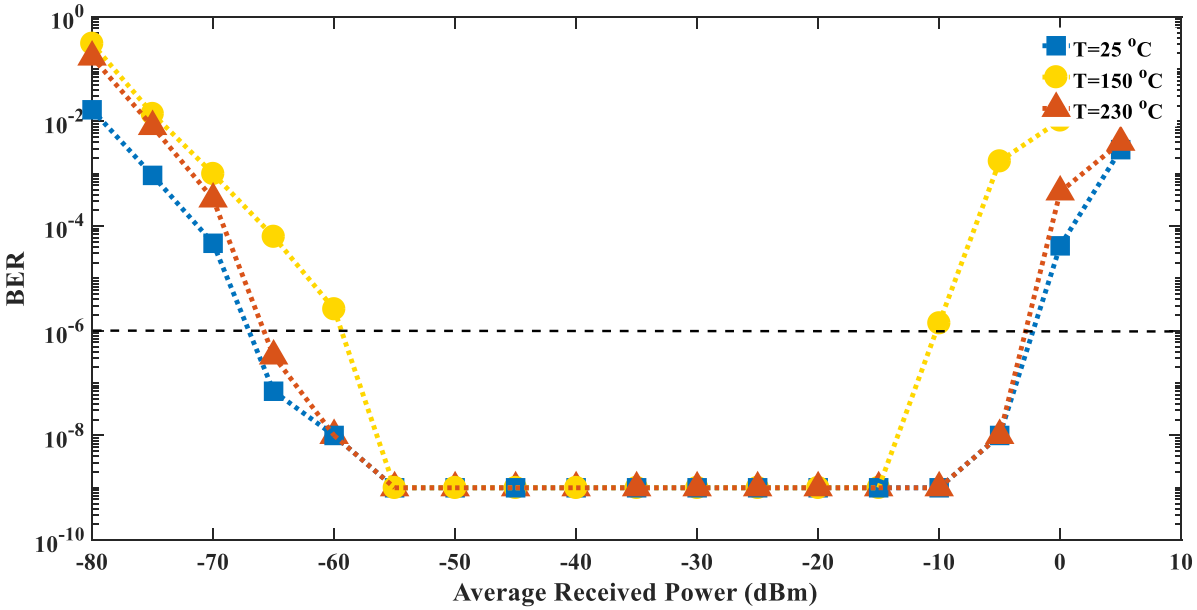


Figure 6.11: Measured BER for the receiver front end with 16 QAM modulation scheme.

It can be noticed also that the minimum BER is 10^{-9} this is due to the fact more than 10^{9} bits were sent through the receiver front end and the accumulative error was zero.

Figure 6.12 shows the EVM versus the average received power level. This is similar to BER measurements. The only difference these measurements show is that EVM improves across the useful dynamic range as the temperature increases. This is because the frequency drift of the signal generator improves as temperature increase. The reason why we could not see this observation in BER is because the BER for 16 QAM is very small.

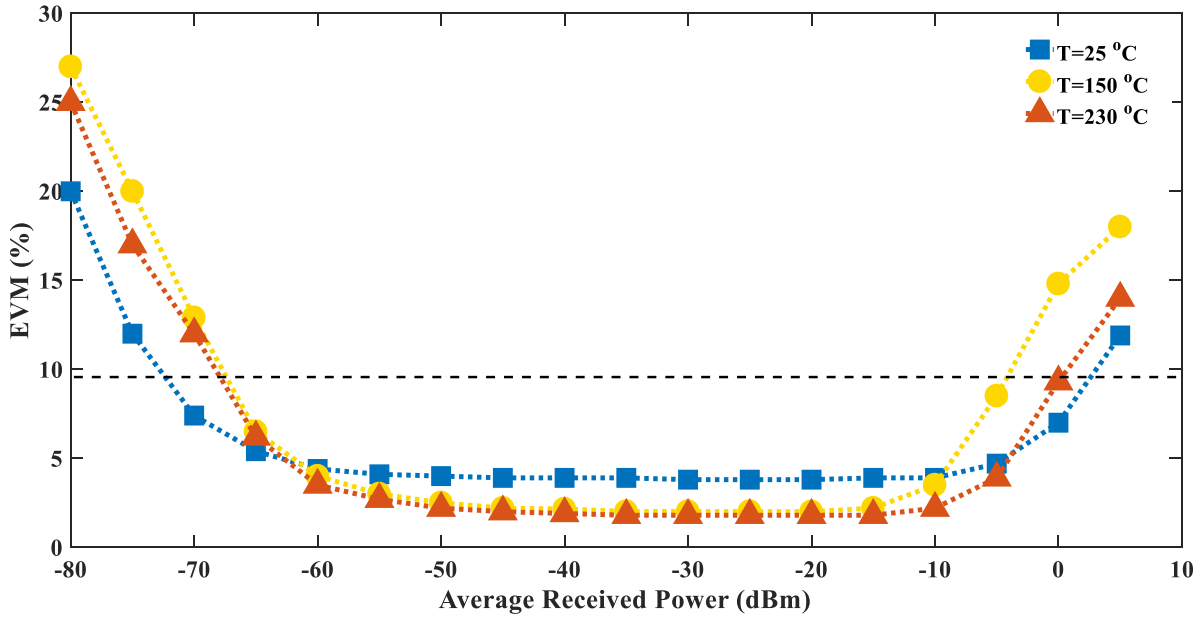


Figure 6.12: Measured EVM for the receiver front end with 16 QAM modulation scheme.

Figure 6.13 shows the measured BER versus the average received power level for 64 QAM scheme. The data rate for the received power signal is 19.8 Mbps. The average received power is swept from -80.0 dBm to 10.0 dBm at different temperature levels. It can be seen that the minimum received power that provides BER of less than 10^{-6} is -50.0 dBm at room temperature and 150 ^{o}C and -53.0 dBm at 230 ^{o}C. The maximum received power that provides the same targeted BER is -15.0 dBm at room temperature, -18 at 150 ^{o}C and -10.0 dBm at 230 ^{o}C. The dynamic range which is the difference between the maximum detectable signal with BER of less than 10^{-6} and the minimum detectable signal with the same BER, is 35 dB at room temperature, 32 dB at 150 ^{o}C, and 43 dB at 230 ^{o}C.

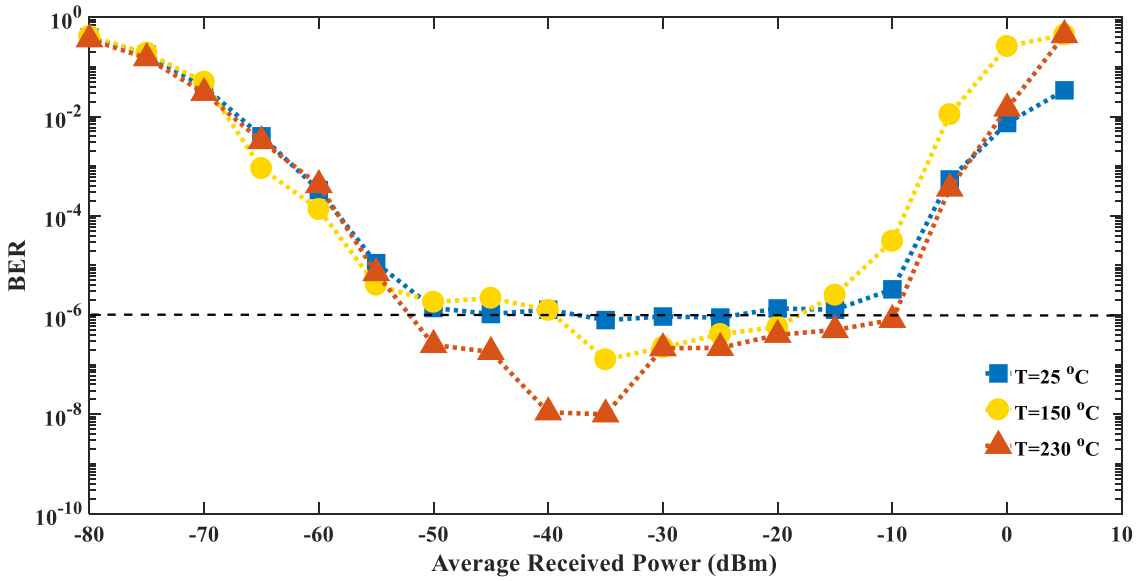


Figure 6.13: Measured BER for the receiver front end with 64QAM modulation scheme.

Figure 6.14 shows the EVM versus the average received power level using 64 QAM scheme. It can be noticed that EVM improves across the useful dynamic range as the temperature increases. This is again because the frequency drift of the signal generator improves as temperature increase which in turns reduce the phase errors, EVM and BER.

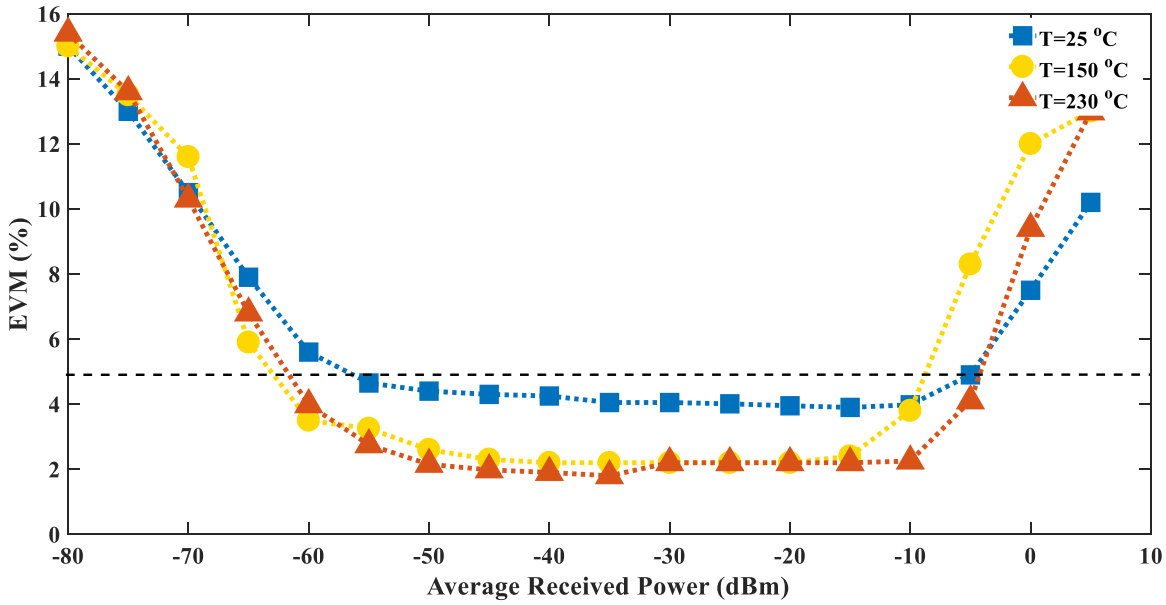


Figure 6.14: Measured EVM for the receiver front end with 64 QAM modulation scheme.

Figure 6.15 shows the measured BER for the receiver front-end versus average received power with 128 QAM scheme. The minimum BERs achieved are 6.3 $\times 10^{-5}$ at 25 ^{o}C, 3.89 $\times 10^{-5}$ at

150 ºC and 2×10^{-5} at 230 ºC. The improvements of BER with temperature is due to improvement of the frequency stability of the signal generator with temperature. However, the minimum BER is still above the required BER of 10^{-6}. For better performance with 128 QAM, a high temperature PLL is needed. This will be further discussed on Future Works section in next chapter.

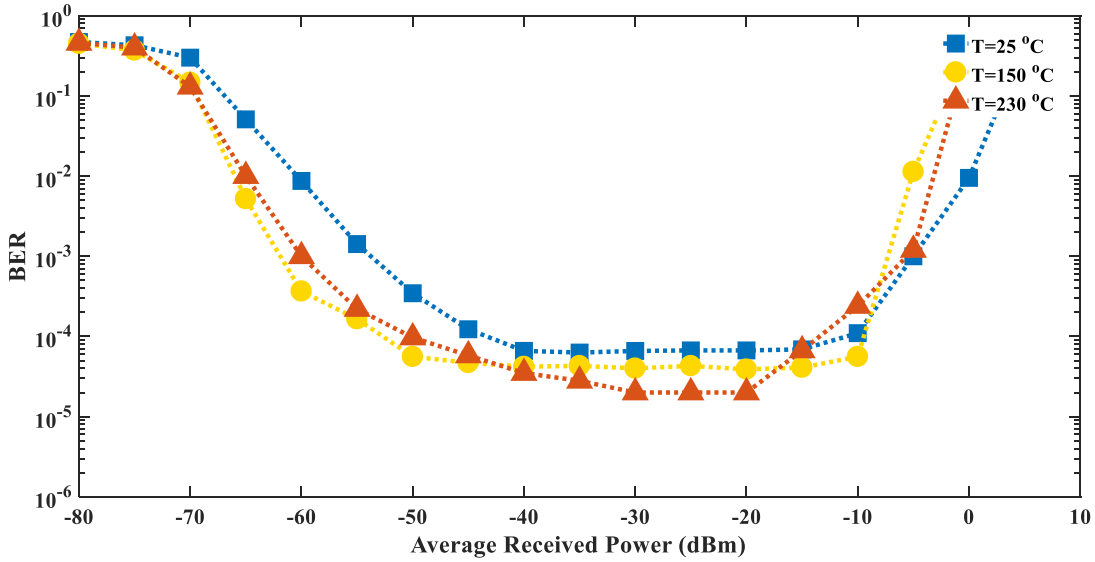


Figure 6.15: Measured BER for the receiver front end with 128 QAM modulation scheme.

Figure 6.16 shows the EVM measurements versus the average received power with 128 QAM. The minimum EVM values are 5.9% at 25 ºC, 4.6% at 150 ºC and 230 ºC.

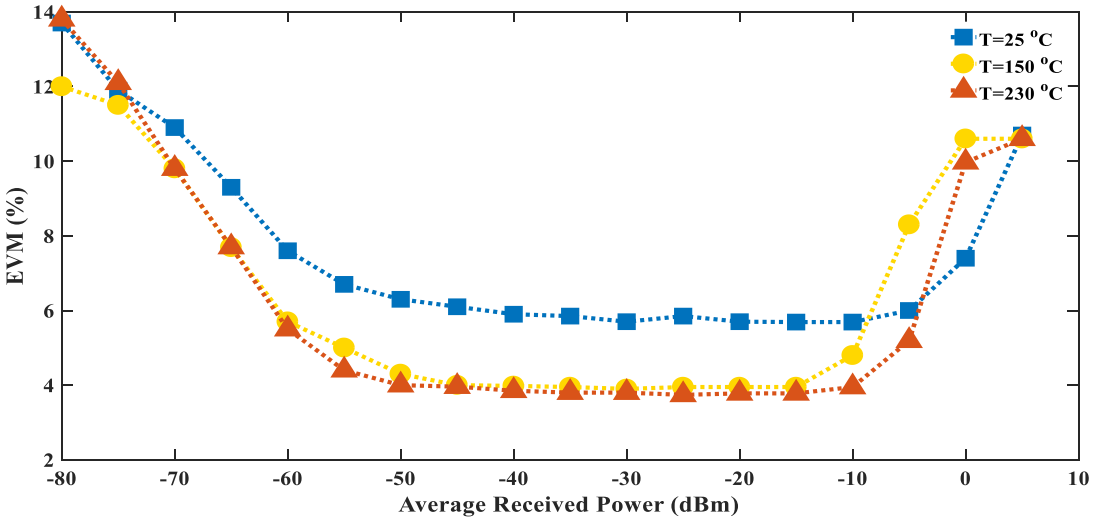


Figure 6.16: Measured EVM for the receiver front end with 128 QAM modulation scheme.

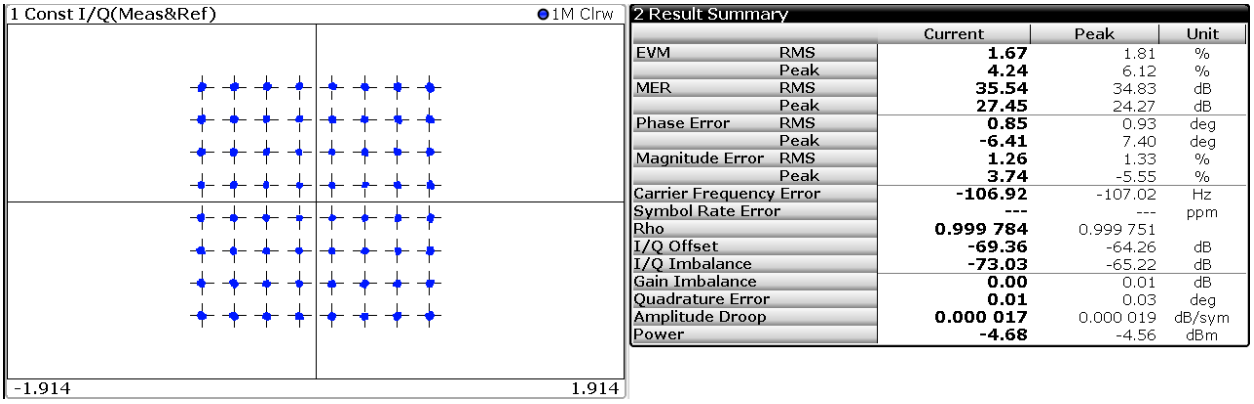
The main factor that affects the performance of the receiver is the frequency drift of the signal generator. Its effect becomes significant if the result length in spectrum analyzer is set to be

very large and at higher modulation order (M >64). With the high frequency instability, the accumulative phase error becomes high and effecting the constellation diagram. To overcome this issue in this measurements, the result length of the spectrum analyzer is set to 2000 symbols. It is observed that as temperature increases, the frequency drifts of the signal generator improve and hence the BER and EVM improve. The frequency stability improvements with temperature are due to the shift of the characteristics of the varactor to operate more in linear region at the intended frequencies.

Although the performance of the receiver is limited by the frequency drifts of the signal generator, the receiver achieves a wide dynamic range which is enough to cover six tools in the downhole with speed of 20 Mbps and at temperatures up 230.0 ^{o}C.

6.3.3 Transmitter

Next, the building blocks for the transmitter which are the IF filter, upconversion passive mixer, signal generator, RF filter, and PA, are connected together and placed inside the oven. Using the same measurement setup shown in Figure 6.3, the EVM and ACPR for the transmitter are measured at 25 ^{o}C, 150 ^{o}C, and 230 ^{o}C and at different power levels. Figure 6.17 shows the measured constellation diagram with a 64 QAM scheme. The measurement is taken at the output of the transmitter back-end.



		Current	Peak	Unit
EVM	RMS	**1.67**	1.81	%
	Peak	**4.24**	6.12	%
MER	RMS	**35.54**	34.83	dB
	Peak	**27.45**	24.27	dB
Phase Error	RMS	**0.85**	0.93	deg
	Peak	**-6.41**	7.40	deg
Magnitude Error	RMS	**1.26**	1.33	%
	Peak	**3.74**	-5.55	%
Carrier Frequency Error		**-106.92**	-107.02	Hz
Symbol Rate Error		**---**	---	ppm
Rho		**0.999 784**	0.999 751	
I/Q Offset		**-69.36**	-64.26	dB
I/Q Imbalance		**-73.03**	-65.22	dB
Gain Imbalance		**0.00**	0.01	dB
Quadrature Error		**0.01**	0.03	deg
Amplitude Droop		**0.000 017**	0.000 019	dB/sym
Power		**-4.68**	-4.56	dBm

Figure 6.17: The measured constellation diagram and EVM for the transmitter back-end with 64 QAM modulation scheme at temperatures of 230 ^{o}C. The power level at the input of transmitter back-end is -14 dBm and data rate is 19.8 Mbps. This is tested at IF signal of 97.5 MHz, LO frequency of 343.0 MHz and IF frequency of 245.5 MHz.

Figure 6.18 shows the measured spectrum of the transmitted signal when -13 dBm is fed to the input of the transmitter back-end. The measured average output power is -3 dBm at room temperature. The ACPR at this power level is -55 dBc.

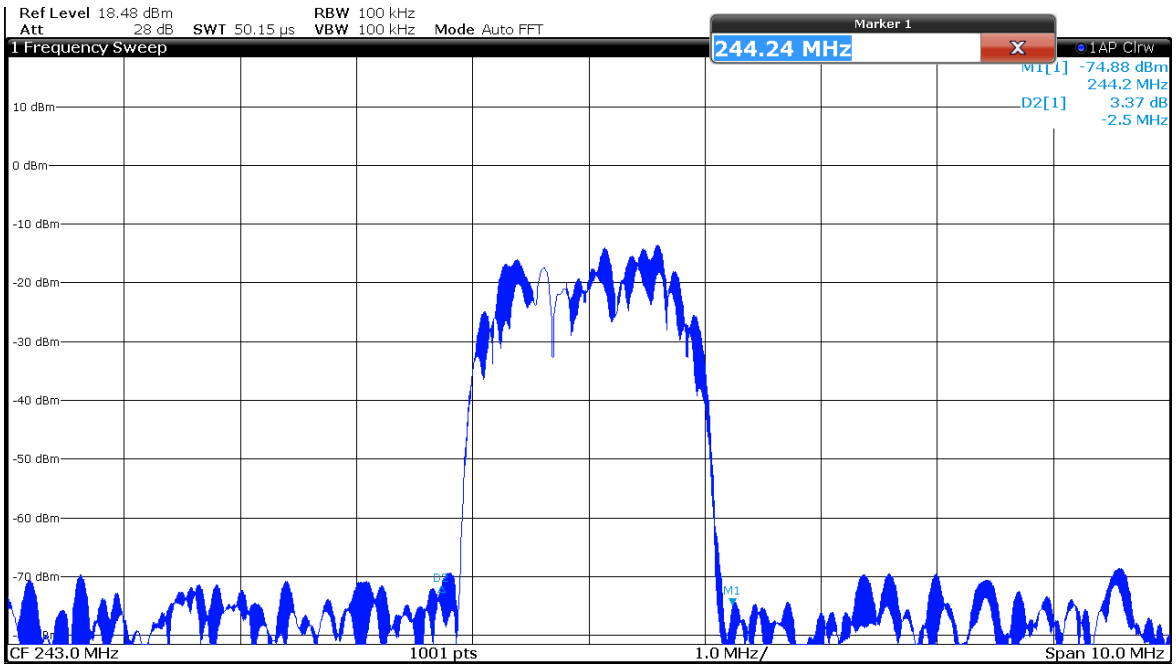


Figure 6.18: The measured spectrum of the transmitted signal at the output of transmitter (PA). The symbol rate for this signal is 1.64 Msps and the roll of the RRC filter is 0.22. The input signal of the transmitter is 64 QAM with average power of -13 dBm. The average power of this signal is -3.0 dB and APCR is -55 dB at 3MHz offset.

The next measurement results show the performance of the transmitter back-end with different modulation schemes and with symbol rate of 3.3 Msps and RRC filter roll of 0.2. Figure 6.19 shows the measured EVM versus the average output power with 16 QAM scheme. It can be noticed that as temperature increases, the maximum average output power decreases. Despite the improvement of the linearity performance of the PA, the degradation of the linearity performance of the passive mixer and PA gain drop are the limiting factors. The maximum average output powers while the EVM is less than 5% are +6.0 dBm at 25 ^{o}C, +5 dBm at 150 ^{o}C, and +2 dBm at 230 ^{o}C. Also, it can be observed that as temperature increases the minimum EVM at average output power of -10 dBm improves. For example, EVM is 4.1 % at room temperature, and it drops to 3.2 % at 230.0 ^{o}C. We have been seeing these improvements consistently with temperature throughout the receiver and transmitter measurements, and these are mainly due to the improvement of the frequency drift of the signal generator frequency.

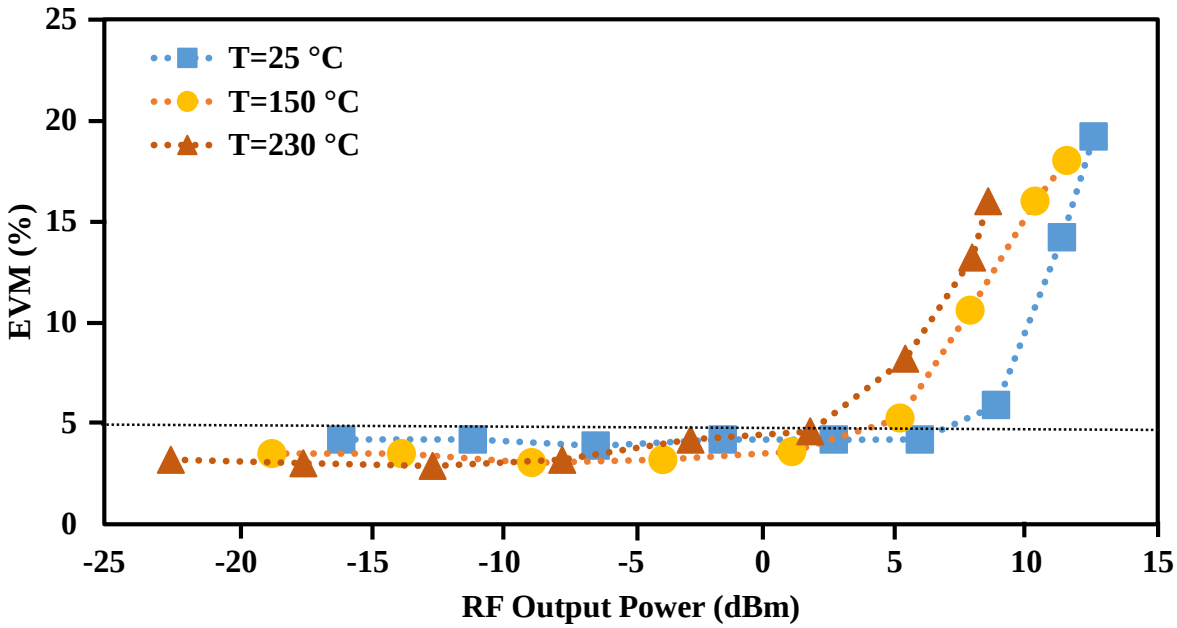


Figure 6.19: Measured EVM for the transmitter back end with 16 QAM modulation scheme.

The other important performance metric for the transmitter back-end is the adjacent channel power ratio (ACPR) measurements. It shows the effects of the transmitter's linearity performance on the adjacent channel. Figure 6.20 presents the ACPR versus the average output power for the 16 QAM scheme. The ACPR is measured at 3 MHz offset from the carrier center frequency. The ACPR at the same values that provide EVM less than 5% are -44 dBc at the average output power of +6.0 dBm and T= 25 ºC, -41.0 dBc at the average output power of +5.0 dBm and T = 150 ºC, and -39.0 dBc at average output power of +2 dBm and T=230.0 ºC. This indicates that ACPR decreases at the maximum average power as temperature increases. This is because the output of the third intercept point (OIP3) for the upconversion passive mixer and the gain of the PA both decrease as temperature increases.

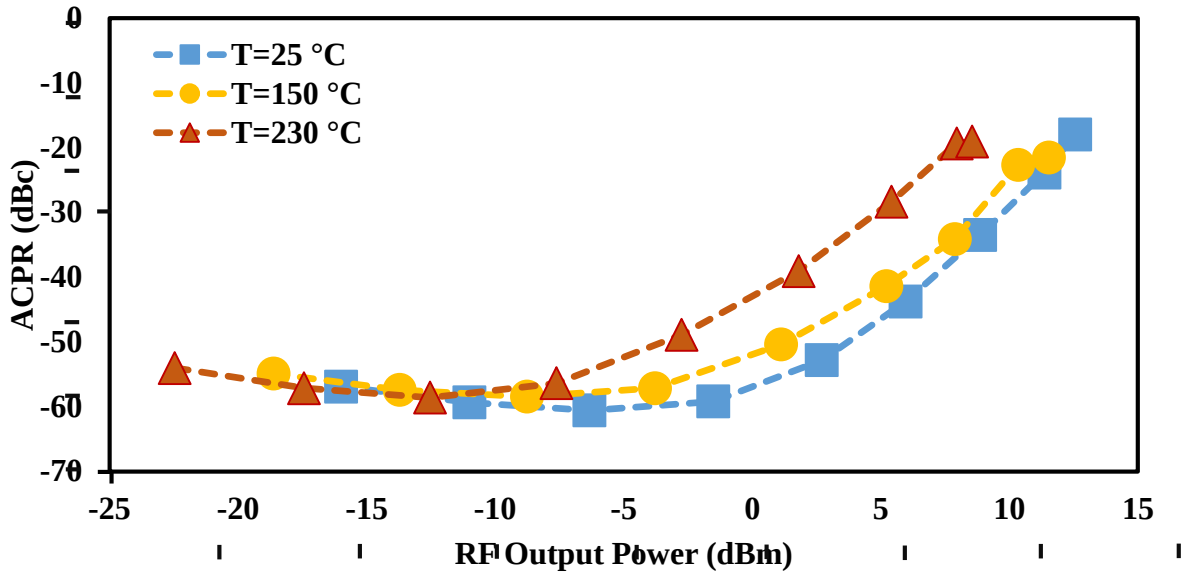


Figure 6.20: Measured ACPR for the transmitter back end with 16 QAM at different temperature levels.

Figure 6.21 shows the measured EVM against the average output power for the transmitter back-end with 64 QAM scheme. The maximum average output powers that provide EVM less than 5% are +3 dBm at 25 ºC and 150 ºC and +1.8 dBm at 230 ºC. It is also observed that minimum EVM which is at average output power less than 0 dBm improves with temperature and this is mainly due to the improvement of the frequency drift of the signal generator frequency.

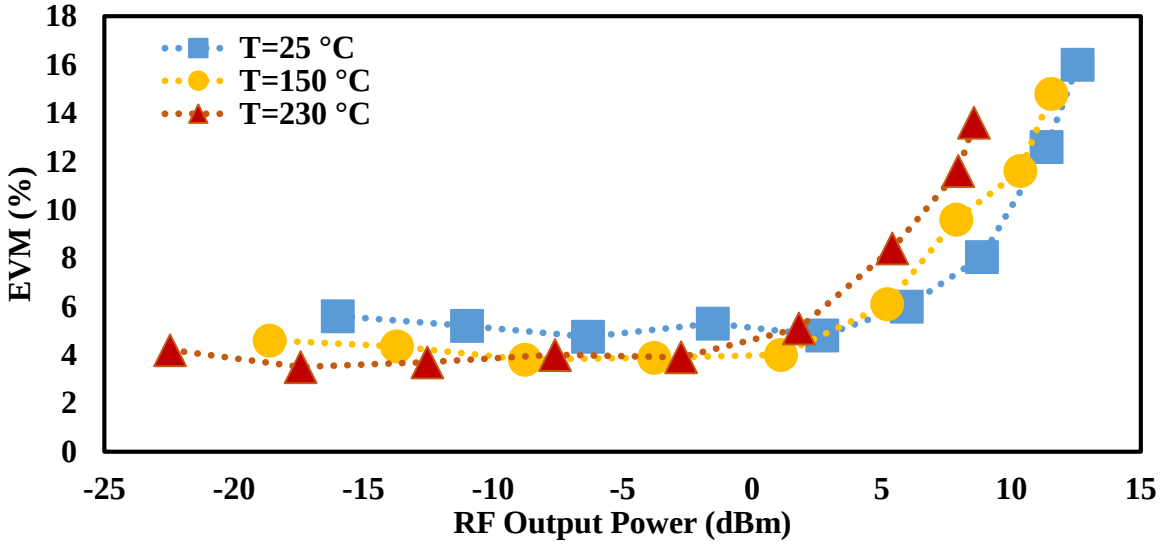


Figure 6.21: Measured EVM for the transmitter back end with 64 QAM at different temperature levels.

Figure 6.22 illustrates the measured ACPR against the average output power for the 64 QAM scheme. The ACPR is also measured at 3 MHz offset from the carrier center frequency. The ACPR at the same values that provide EVM less than 5% are -50 dBc at average output power of +3.0 dBm and T= 25 ^{o}C, -45.0 dBc at average output power of +3.0 dBm and T = 150 ^{o}C, and -40.0 dBc at average output power of +1.8 dBm and T=230.0 ^{o}C.

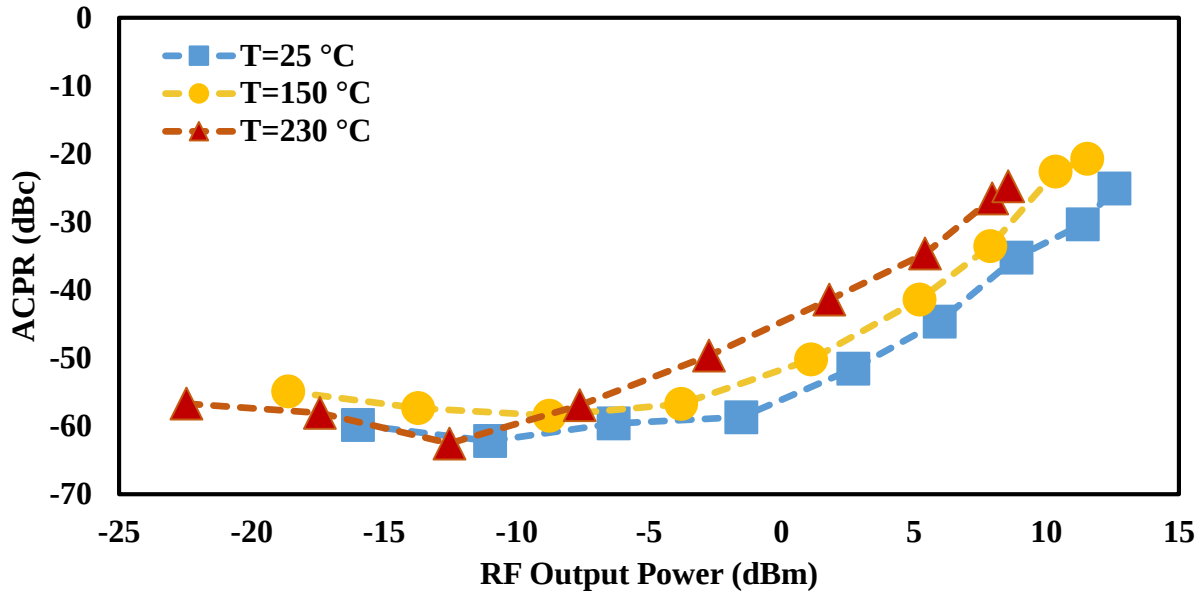


Figure 6.22: Measured ACPR for the transmitter back end with 64 QAM at different temperature levels.

Figure 6.23 shows the measured EVM against the average output power for the transmitter back-end with 128 QAM scheme. The maximum average output powers that provide EVM less than 5% are +2.7 dBm at 25 ^{o}C and 150 ^{o}C and +1.8 dBm at 230 ^{o}C. It is also observed that minimum EVM which is at average output power less than 0 dBm improves with temperature. and this is mainly due to the improvement of the frequency drift of the signal generator frequency.

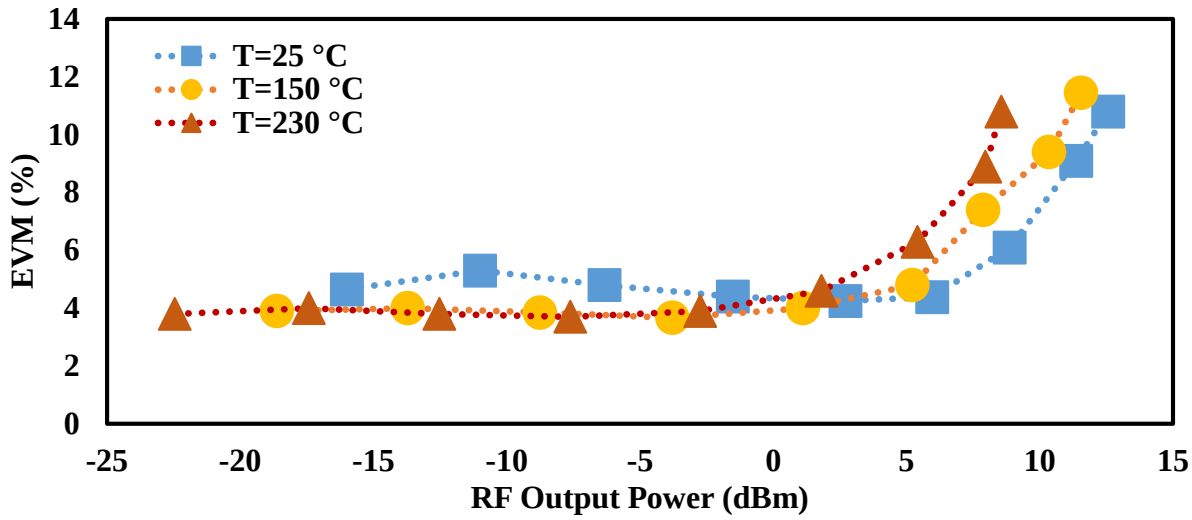


Figure 6.23: Measured EVM for the transmitter back end with 128 QAM at different temperature levels.

Figure 6.22 illustrates the measured ACPR against the average output power for the 128 QAM scheme. The ACPR is also measured at 3 MHz offset from the carrier center frequency. The ACPR at the same values that provide EVM less than 5% are -50 dBc at average output power of +2.7 dBm and T= 25 ^{o}C, -51 dBc at average output power of +2.7 dBm and T = 150 ^{o}C, and -38 dBc at average output power of +1.8 dBm and T=230.0 ^{o}C. Table 6.1 presents a summary for the transceiver performance at 230.0 ^{o}C.

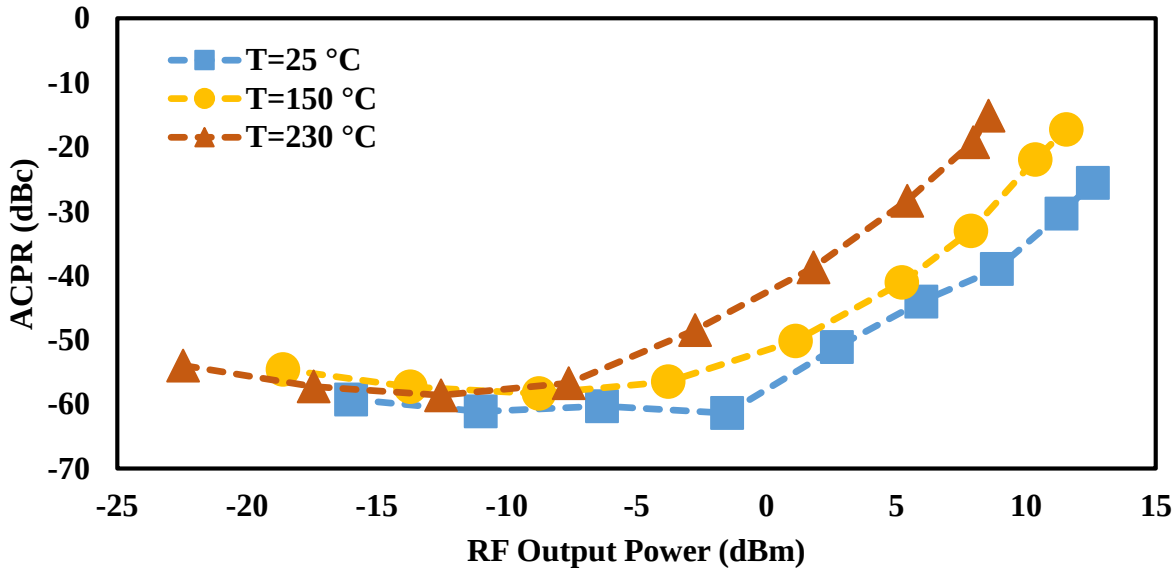


Figure 6.24: Measured ACPR for the transmitter back end with 128 QAM at different temperature levels.

Table 6.1: Summary of the transceiver performance.

Process	GaN HEMT
Supply Voltage	4 V, 5V, 28 V
Frequency Range	230 MHz -300 MHz
Operating Temperature	25 ^{o}C – 230 ^{o}C
Signal Generator	
Tuning Range	320 MHz – 360 MHz
Phase Noise	-118 dB dBc/Hz at 100 KHz offset
Receiver	
Power Gain	16 -18 dB
Noise Figure	7-13 dB
Input P1dB	-4 dBm
IIP3	+5.5 dBm
Sensitivity	-68 dBm
Minimum BER	10^{-9} with 16 QAM 10^{-6} with 64QAM 3.89×10^{-5} with 128 QAM
Dynamic Range	55 dB
Transmitter	
Output Power	20 dBm
P1dB	23 dBm
EVM	4.1% @ Pout=+1.8 with 16 QAM 5% @ Pout=+1.8 dBm with 64QAM 5% @ Pout=+1.8 dBm with 128 QAM
ACPR	-44.0 c with 16 QAM at EVM=5% 40.0 with 64QAM at EVM=5% -38 dBc with 128 QAM EVM=5%

6.4 Chapter Summary

In this chapter, the transceiver prototype and the measured results of the transceiver at a wide temperature range were introduced. First, the high temperature measurement setup and environment was described. Then, the measured results of the signal generator performance at a wide temperature range and different carrier frequencies were presented. Subsequently, the measured results for the receiver's performance with different modulation schemes were reported. The measurement results included the bit error rate (BER), error vector magnitude (EVM) performances with 16 QAM, 64 QAM and 128 QAM at 25 ^{o}C, 150 ^{o}C and 230 ^{o}C. Next, the measured results of the transmitter's performance with different modulation schemes were presented. The measurement results include EVM and adjacent channel power ratio (ACPR) performances with 16 QAM, 64 QAM and 128 QAM at 25 ^{o}C, 150 ^{o}C and 230 ^{o}C. The transceiver has achieved a wide dynamic range which is enough to cover six tools in the downhole system with speed of 20 Mbps and BER of 10^{-6} at temperatures up 230.0 ^{o}C. These results also prove the feasibility of using the RF transceiver for high temperature applications.

Chapter 7 Conclusion and Future Work

A novel downhole communication system that employs RF front end to provide high speed communications between the downhole tools and the surface has been proposed. The system supports up to six tools and utilized a frequency division multiple access technique to provide full duplex and simultaneous communications between downhole tools and the surface data acquisition system. The system achieves 20 Mbps per tool for uplink and 6 Mbps per tool for downlink with bit error rate (BER) less than 10^{-6}.

In addition, characterizations of the GaN HEMT at ambient temperatures of 25 - 250 ^{o}C were conducted. These characterizations verified the possibility of using GaN HEMT for RF designs at high temperatures. Also, analytic model that can predict the behavior of R_{DS} was developed. The model was verified by the analysis and the performance of the resistive mixer.

Further, a GaN based RF front-end of transceiver operating at ambient temperatures up to 230 ^{o}C was designed. Measurement results of the transceiver showed the design has met the specs for downhole communications. To our knowledge, this is the first RF transceiver that operates at this high temperature.

Moreover, RF building blocks such as the resistive upconversion mixer and the active downconversion mixer were designed and prototyped. These blocks record the highest operating temperature in the open literature. Finally, a novel high temperature adaptive bias circuit for GaN based RF block was proposed. The proposed design comprised multiviabrator oscillator, voltage doubler, and temperature dependent bias controller. The adaptive bias circuit provides a negative voltage temperature dependent. The voltage level and temperature coefficient of the generated bias voltage can be controlled by the resistors ratio of the bias controller to match the required biasing voltage for a RF building block. The proposed adaptive bias circuit can be applicable to any of the GaN based RF building blocks up to 250 ^{o}C.

7.1 Summary

Chapter 1 provides the motivation behind the proposal of the RF front-end of a transceiver for downhole communications and presents possible areas where the RF high temperature can be applied. Then, the existing and the projected downhole telemetry systems are reviewed. The current downhole system provides low speed and operates at temperatures of less than 175 ^{o}C. This system is not sufficient to support more sophisticated sensors and reach deeper wells. The next generation for downhole communications utilize optical fiber cables to provide communications between the downhole and surface. However, the communications between the tools and the optical node in the downhole are still the bottleneck. RF transmission using FDMA can provide high speed, full duplex, simultaneous communication between the surface and downhole tools.

Chapter 2 discusses the necessary preliminaries for the proposed downhole communication system design. Some theoretical background and advantages of radio over fiber (RoF) system are presented, followed by a brief survey on RoF components for high temperature applications. The elements investigated are the optical fiber, lasers, modulators, photodetectors, and RF transceivers. Finally, the temperature effects on the main aspect of the transceiver performance is discussed. The chapter gives insight into the design philosophy for RF front-end transceiver for the next generation of downhole communications. This background is necessary to prepare for the system design that will be presented in chapter 3.

Chapter 3 introduces the proposed downhole communication system architecture. Before going to the design details, the downhole channel is characterized. Then, based on the channel characterization, frequency planning and allocations for the transmit and receive paths are proposed. Next, a transceiver architecture is introduced. Superheterodyne transceiver architecture is adopted for the design. Subsequently, a link budget calculation to find the building blocks specifications is performed. After obtaining the initial specs of the transceiver building block, the downhole communication system is implemented in AWR simulation tool to verify the performance. Then, the specs for the RF building blocks are optimized to provide a data rate of 20 Mbps per tool with BER of less than 10^{-6}. The total number of tools included in the design is six. Then, the simulation results with optimized specs are presented. Finally, a summary of the

minimum specs is presented. With 64 QAM, this system provides a full duplex communication with 20 Mbps per tool for six tools with BER less than 10^{-6}.

Chapter 4 reviews the technology option for high temperature applications. Qorvo GaN HEMT technology is selected for our design since it has the highest junction temperature. This technology is intended for high power amplifiers. The high power consumption of the devices can rise the junction temperature to 275 ^{o}C at room temperature. We used these transistors to design our building block at low power but at high temperature. Since these transistors are characterized only at temperatures less than 85 ^{o}C, a new characterization at high temperature is needed. First, we studied the existing work on the impact of temperature on GaN characteristics. Next, the high temperature characterization setup is introduced. Afterwards, we performed characterizations on the Qorvo GaN HEMT devices at temperatures up to 250 ^{o}C. The temperature effects on drain current, transconductance, small signal parameters, and drain resistance are highlighted. Finally, a high temperature model that predicts the behavior of R_{DS} at temperatures up to 250 ^{o}C is developed.

Chapter 5 presents the design and analysis of the building blocks. First, the high temperature design considerations that include the thermal analysis for the packaged device along with a PCB/heatsink, and passive component selection are discussed. Then, the analysis and design of the high temperature RF building blocks are elaborated. The proposed resistive mixer design which is used in the transmitter design as upcnverting stage is presented. Detailed analysis and verified by measurements is described. The analysis is conducted using the high temperature R_{DS} model was developed in chapter 4. Furthermore, the bias voltage that provides optimum performance at a wide temperature range is predicted using the analysis and verified though measurements. Next, the active mixer which is used in the receiver as a downconversion stage is also elaborated. The temperature impacts on conversion gain and noise figure are highlighted. Then, the bias voltage for optimum conversion gain and noise figure performances at a wide temperature range is identified through measurements. Subsequently, the analysis and measurements for the low noise amplifier, signal generator, power amplifier, filters and diplexers are presented. Finally, a new adaptive bias circuit for depletion mode GaN based RF building blocks is proposed. The concept is first explained through block diagram. Then, the circuit implementation and temperature analysis are presented. The performance is verified through simulation. The adaptive bias circuit provides temperature dependent bias voltage that closely matches the optimum bias voltage

required by the resistive mixer at temperatures up to 250 ^{o}C. The voltage level and temperature coefficient of the generated bias voltage can be easily adjusted by changing the resistor ratio of the controller.

Chapter 6 introduces the final prototype and measurement results of the transceiver at a wide temperature range. We begin with describing the measurement environment and test setup. Then, the measured results of the signal generator performance at a wide temperature range and different carrier frequencies are presented. Subsequently, the measured results for the receiver is reported. The measurement results include the bit error rate (BER), error vector magnitude (EVM) performances with 16 QAM, 64 QAM and 128 QAM at 25 ^{o}C, 150 ^{o}C and 230 ^{o}C. Next, the measured results of the transmitter are illustrated. The measurement results include EVM and adjacent channel power ratio (ACPR) performances with 16 QAM, 64 QAM and 128 QAM at 25 ^{o}C, 150 ^{o}C and 230 ^{o}C. The transceiver achieves a wide dynamic range which is enough to cover six tools in the downhole system with speed of 20 Mbps and BER of 10^{-6} at temperatures up 230.0 ^{o}C. These results also prove the feasibility of using the RF transceiver for high temperature applications.

Chapter 7 summarizes and concludes the work presented in this dissertation. The research presented here is a first-of-its-kind proposal and consequently work can be continued in several different areas of concentration. New and exciting applications can be imagined with high temperature RF circuits and systems.

7.2 Future Work

There are multiple ways in which the future work can proceed in this research area. The first and foremost is to miniaturizing the transceiver design. Going for an IC design is an attractive option. This can be possible by increasing the operating frequency. Although the attenuation of the channel will increase substantially, it can be mitigated by having higher gain stages using more complex circuits which will easily fit in a IC.

The other important improvements that may be pursued is designing a phase locked loop system for the transceiver. This will help to improve the frequency drift of the signal generator which in turns will improve the BER for higher order QAM schemes. This eventually will increase further the data rate of the downhole communication system.

Finally, designing a transceiver and RF building blocks that can operate at temperature higher than 250 ^{o}C is a very attainable long-term goal. For example, an application such as Venus explorations requires electronics to operate at ambient temperatures of 480 ^{o}C. As the wide bandgap technology fabrication is improved, the high temperature design will see a tremendous growth. RF circuits and systems capable of operating at high temperature can open the horizon for many harsher environment applications and resolve many technical challenges that many industries face.

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