High-Efficiency and High-Power Density DC-DC Power Conversion Using Wide Bandgap Devices for Modular Photovoltaic Applications

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ABSTRACT

With the development of solar energy, power conversion systems responsible for energy delivering from photovoltaic (PV) modules to ac or dc grid attract wide attentions and have significantly increased installations worldwide. Modular power conversion system has the highest efficiency of maximum power point tacking (MPPT), which can transfer more solar power to electricity. However, this system suffers the drawbacks of low power conversion efficiency and high cost due to a large number of power electronics converters. High-power density can provide potentials to reduce cost through the reduction of components and potting materials. Nowadays, the power electronics converters with the conventional silicon (Si) based power semiconductor devices are developed maturely and have limited improvements regarding in power conversion efficiency and power density. With the availability of wide bandgap devices, the power electronics converters have extended opportunities to achieve higher efficiency and higher power density due to the desirable features of wide bandgap devices, such as low on-state resistance, small junction capacitance and high switching speed.

This dissertation focuses on the application of wide bandgap devices to the dc-dc power conversion for the modular PV applications in an effort to improve the power conversion efficiency and power density.

Firstly, the structure of gallium-nitride (GaN) device is studied theoretically and characteristics of GaN device are evaluated under testing with both hard-switching and soft-switching conditions. The device performance during steady-state and transitions are explored under different power level conditions and compared with Si based devices.

Secondly, an isolated high-efficiency GaN-based dc-dc converter with capability of wide range regulation is proposed for modular PV applications. The circuit configuration of secondary side is a proposed active-boost-rectifier, which merges a Boost circuit and a voltage-doubler rectifier. With implementation of the proposed double-pulse duty cycle modulation method, the active-boost-rectifier can not only serve for synchronous rectification but also achieve the voltage boost function. The proposed converter can achieve zero-voltage-switching (ZVS) of primary side switches and zero-current-switching (ZCS) of secondary side switches regardless of the input voltages or output power levels. Therefore, the proposed converter not only keeps the benefits of highly-efficient series resonant converter (SRC) but also achieves a higher voltage gain than SRC and a wide range regulation ability without adding additional switches while operating under the fixed-frequency condition. GaN devices are utilized in both primary and secondary sides. A 300-W hardware prototype is built to achieve a peak efficiency of 98.9% and a California Energy Commission (CEC) weighted efficiency of 98.7% under nominal input voltage condition.

Finally, the proposed converter is designed and optimized at 1-MHz switching frequency to pursue the feature of high-power density. Considering the ac effects under high frequency, the magnetic components and PCB structure are optimized with finite element method (FEM) simulations. Compared with 140-kHz design, the volume of 1-MHz design can reduce more than 70%, while the CEC efficiency only drops 0.8% at nominal input voltage condition. There are also key findings on circuit design techniques to reduce parasitic effects. The parasitic inductances induced from PCB layout of primary side circuit can cause the unbalanced resonant current between positive and negative half cycles if the power loops of two half cycles have asymmetrical parasitic inductances. Moreover, these parasitic inductances reflecting to secondary side should be considered into the design of resonant inductance. The parasitic capacitances of secondary side could affect ZVS transitions and increase the required magnetizing current. Because of large parasitic capacitances, the dead-time period occupies a large percentage of entire switching period in MHz operations, which should be taken into consideration when designing the resonant frequency of resonant network.

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GENERAL AUDIENCE ABSTRACT

Solar energy is one of the most promising renewable energies to replace the conventional fossils. Power electronics converters are necessary to transfer power from solar panels to dc or ac grid. Since the output of solar panel is low voltage with a wide range and the grid side is high voltage, this power converter should meet the basic requirements of high step up and wide range regulation. Additionally, high power conversion efficiency is an important design purpose in order to save energy. The existing solutions have limitations of narrow regulating range, low efficiency or complicated circuit structure. Recently, the third-generation power semiconductors attract more and more attentions who can help to reduce the power loss. They are named as wide band gap devices. This dissertation proposed a wide band gap devices based power converter with ability of wide regulating range, high power conversion efficiency and simple circuit structure. Moreover, this proposed converter is further designed for high power density, which reduces more than 70% of volume. In this way, small power converter can merge into the junction box of solar panel, which can reduce cost and be convenient for installations.

To my parents:

Yanmin Zhao

Cuiqing Xu

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Chapter 1 Introduction

1. 1 Overview on Photovoltaic Energy Generation

Nowadays, the demand of renewable energy is increasing rapidly due to the limited storage of the fossil fuels and serious environmental pollutions [1], [2]. Solar photovoltaic (PV) energy is one of the fast-growing energy sources because it is easy for installations and converting to electricity and the price of PV modules is decreasing steadily as well. As U.S. Energy Information reported, the electricity generation from solar PV energy is 80 billion kilowatt-hours in the U.S. It is projected to increase more than 10 times by 2050 as shown in the Figure 1.1. The costs of solar PV energy in the U.S. have declined 50% since 2013, which is from $2.2 per watt to $1.1 per watt [3].

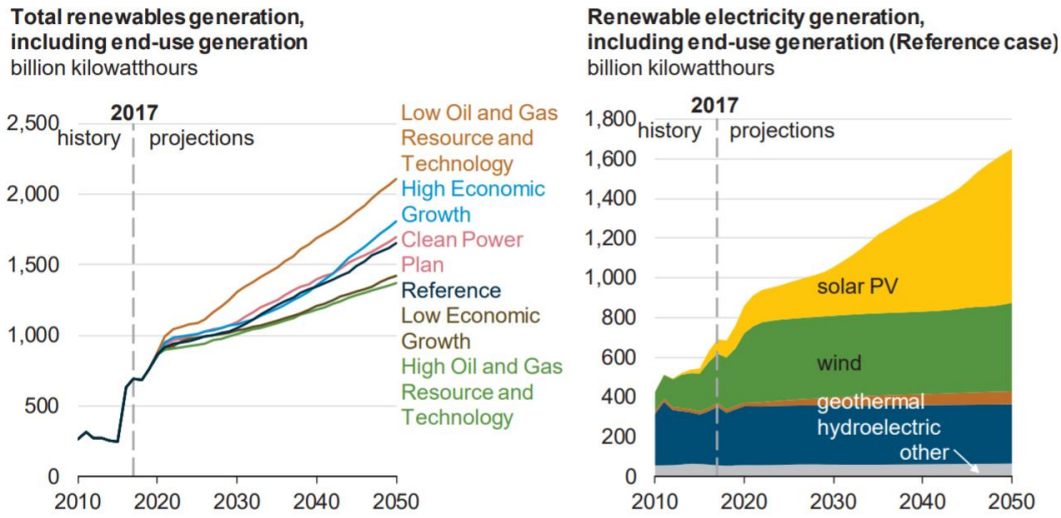


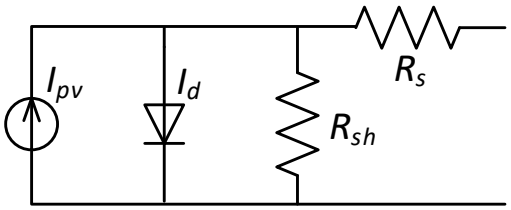
Figure 1.1. Generation from renewable sources, led by growth in wind and solar photovoltaic generation. (Data are from U.S. Energy Information Administration [1]).

The PV module absorbs sunlight as a source of energy to generate direct current (DC) electrical power. A PV module is composed of strings of PV cells, typically, with 60

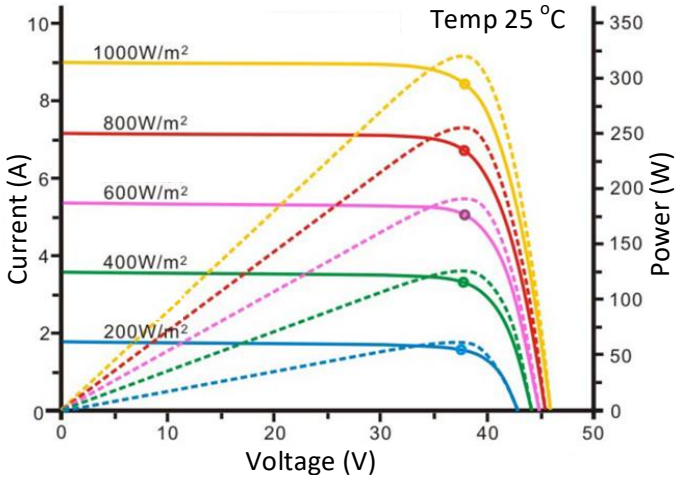
cells or 72 cells in commercial products. Figure 1.2 shows a photograph of 60 and 72 cell PV modules [4]. The power of each PV module varies from 100-400 watts depending on the number of cells [5].

Figure 1.2. Photograph of 60 and 72 cell PV modules. (The picture is from https://sunmetrix.com/solar-panel-size-for-residential-commercial-and-portable-applications/).

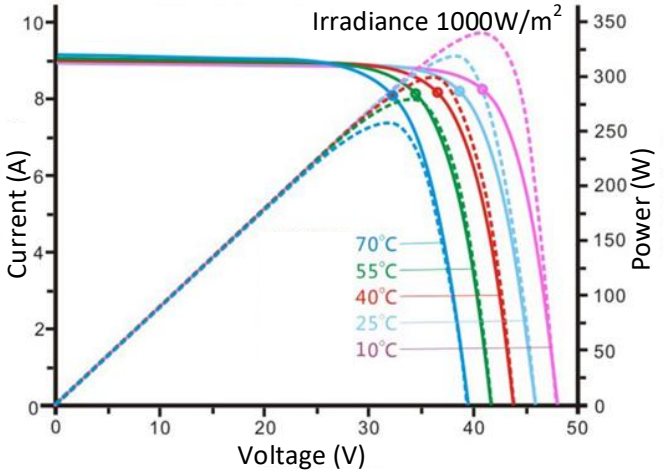
The output of PV module has non-linear characteristics. The output power and output voltage have wide ranges and are highly depended on the PV cell materials, temperature, partial shading and irradiance conditions [6], [7]. The general model circuit of PV modules is shown in Figure 1.3 (a), which behaves as a current source with an internal resistor in series. And the curves of output characteristics based on different irradiance and temperature conditions are shown in Figure 1.3 (b) and (c), where the current-voltage (I-V) characteristics of the PV module and the power-voltage (P-V) characteristics of the PV model derived from I-V characteristics are plotted. As shown in Figure 1.3 (b) and (c), the maximum output power can be generated when the PV module operates at the maximum power point (MPP).



(a) Model of a PV module.



(b) I-V and P-V characteristics of a PV module under different irradiance conditions.



(c) I-V and P-V characteristics of a PV module under different temperature conditions.

Figure 1.3. Model and output characteristics of a single PV module.

The power conversion system (PCS) is an important portion in a PV system, since it delivers energy from PV modules to dc or ac grid. For PCS, the most important responsibility is to deliver the maximum power to the grid. Therefore, the PCS must have

the capability of maximum power point tracking (MPPT) to ensure capturing the maximum power that can be generated from PV module.

1. 2 PV Power Conversion Systems for Utility Grid

According to the different levels of MPPT implementation, the PCS architectures can be classified into three categories, which are centralized PCS, string PCS and modular PCS, [8] - [19].

The centralized PCS is shown in Figure 1.4, which is a single high voltage and high power central inverter, referring to as central inverter [8], [9]. In general, the power level of central inverter is thousand-kilowatts and up. A large number of PV strings are connected in series to generate a high dc voltage, where each PV string is comprised of tons of PV modules in series. The centralized PCS implements a MPPT algorithm to track the maximum power of the entire array of PV. Although this type of architecture features of low cost and high power conversion efficiency due to the single power electronics equipment, it suffers low MPPT efficiency. This is because the entire array of PV shares the same output current, since all of the PV strings connect in series. However, different PV modules have different I-V output characteristics due to the differences in terms of shading area, irradiance conditions, manufacture and other reasons. The output power of entire PV array will be limited by the PV module with the lowest output power. Compared with the case that each PV module has its own MPPT capability, the mismatch power loss resulting from low MPPT efficiency is severe for centralized PCS.

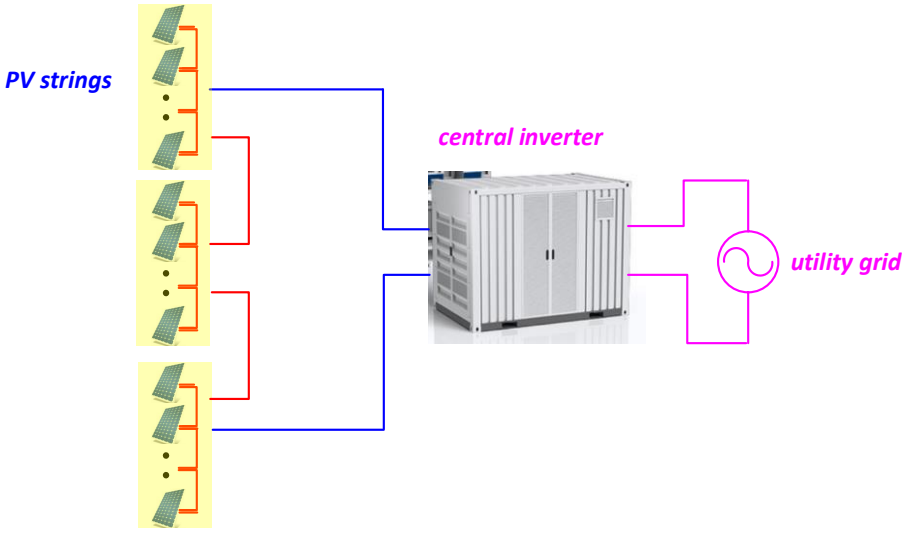


Figure 1.4. Architecture of centralized power conversion system.

Another typical PCS architecture is the string PCS, which consists of a kilowatts power inverter [10], [11], as shown in Figure 1.5. PV array is comprised of a single PV string and each PV string connects with a grid-tie inverter, referring to as string inverter. Differently with centralized PCS, dc power is taken from multiple PV strings to multiple inverters instead of one central inverter. Therefore, the MPPT efficiency is improved, since the each PV string has its individual MPPT capability and cannot be affected by other strings who are in partial shading. However, it still cannot avoid the current mismatch from the PV modules in the same string. The string inverter has high power conversion efficiency, typically 97.5-98.5% for commercial products and it is easier to install and maintain compared with central inverter. However, the string inverter also suffers some disadvantages, such as high cost and mismatch power loss caused by limited MPPT efficiency.

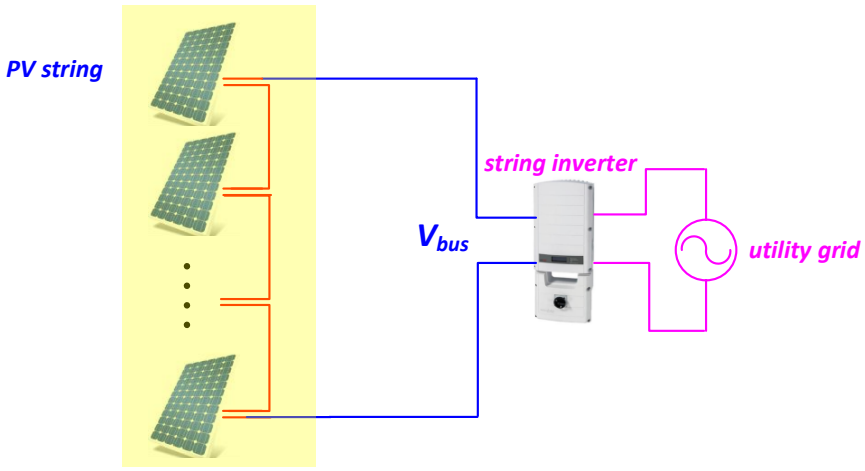


Figure 1.5. Architecture of string power conversion system.

The mismatch power loss between PV modules existing in centralized and string PCS architectures motivates the development of PCS with modular MPPT level. The third type of architecture is modular PCS as shown in Figure 1.6, where each PV module interfaces directly with individual power electronics converter with MPPT ability. There are three types of solutions for modular PCS: (1) series-type dc power optimizer in Figure 1.6 (a) [12] - [14]; (2) parallel-type dc power optimizer in Figure 1.6 (b) [15], [16]; (3) micro-inverter in Figure 1.6 (c) [17], [18].

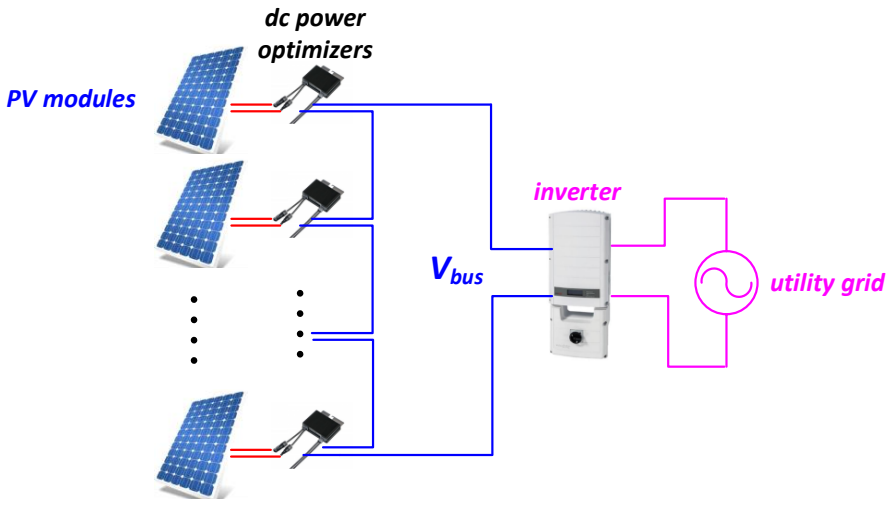
Nowadays, solutions of dc power optimizer architecture are very popular in commercial. For series-type power optimizer, each PV module connects to a dc-dc power converter with capability to track MPP. The outputs of a string of dc-dc power converter connect in series to generate a high voltage dc to be the input of a string inverter. Therefore, the series-type dc power optimizer has low input and output voltages. Even though the individual series-type power optimizer features high-efficiency and low cost, the system architecture has less flexibility since the outputs of dc power optimizers connect in series. It also encounters complicated control strategies and start up issues [13], [14].

In contrary of series-type dc power optimizer, the outputs of a string of parallel-type dc optimizers are in parallel. Thus the input of each parallel-type dc optimizer is low to be well paired with the output voltage of single PV module, while the output is directly connected to the high voltage bus before string inverter. The power electronic converter for parallel-type structure has high step-up ratio. Compared with series-type dc power optimizer, the power flow of each parallel-type dc power optimizer, as well as the control strategy, is independent. If one power optimizer fails, the other units can still work normally.

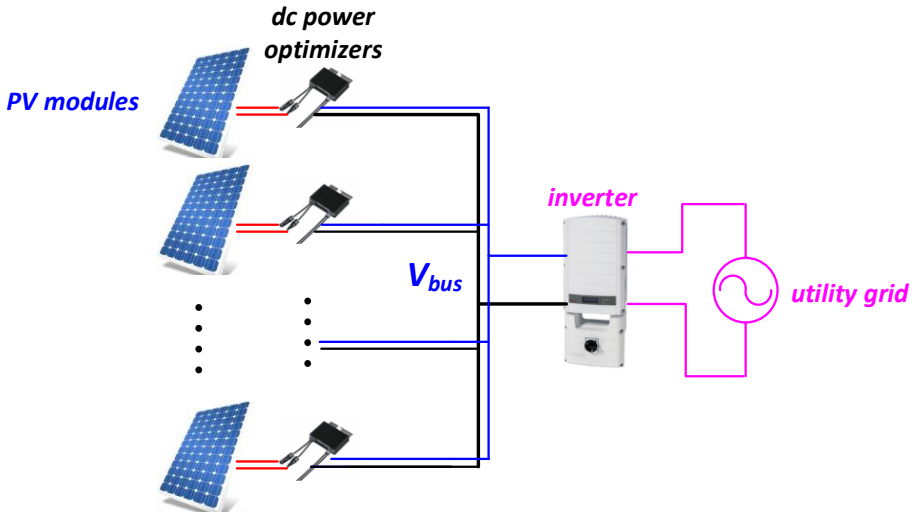
Another mainstream solution of modular PCS is micro-inverter as shown in Figure 1.6 (c). Similarly as dc power optimizer, the input of micro-inverter is connected directly with single PV module. The output of micro-inverter is inverted to ac power interfacing to utility grid instead of dc power. Micro-inverter can be classified as two types, where one is single-stage micro-inverter and the other one is two-stage micro-inverter. Single-stage micro-inverter converts the dc power from PV module to utility grid directly, while two-stage micro-inverter will boost PV module voltage to a high voltage dc bus and the second stage inverts the dc power to ac power. The front-end dc-dc converter between PV module and the inverter stage is not only responsible voltage step-up but also for MPPT. Two-stage micro-inverter has gained wider attractions in terms of MPPT efficiency and inverter lifetime. This is because the inverter system has to eliminate the double line frequency energy of the input side to improve the MPPT efficiency. Single-stage micro-inverter conventionally uses electrolytic capacitors to absorb the double line frequency ripple, however, it adversely accelerates the degradation of inverter lifetime [20]. In a two-stage

micro-inverter, input double line frequency can be rejected by applying control strategies on the front-end dc-dc converter without the usage of electrolytic capacitors [21], [22].

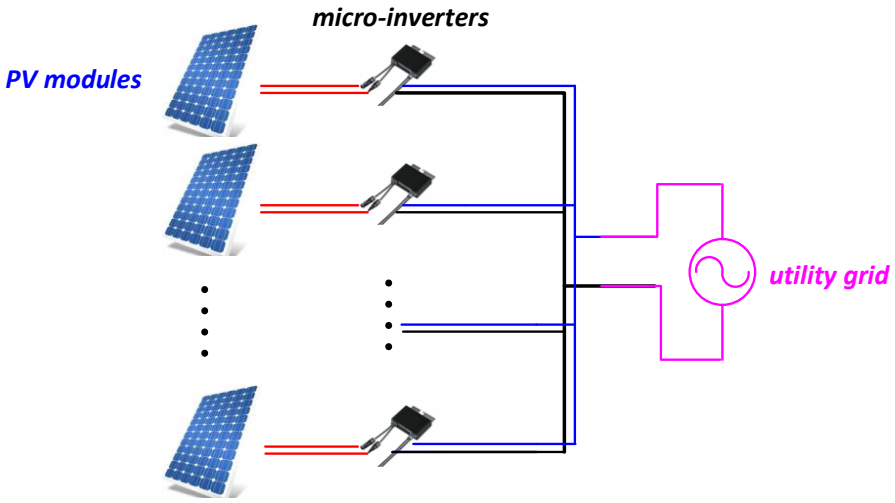
The system configuration of parallel-type dc power optimizer is same as the front-end dc-dc converter, since both of them connect single PV module of input side and generate high output voltage. The combination of each PV module and its converter can be considered as a unit and different units are connected in parallel with independent operation. This configuration features high fault tolerance, easy scalability and high MPPT efficiency. However, the major disadvantages are relatively low power conversion efficiency and high cost compared with other configurations. The reason of low efficiency is because that the energy is processed twice from PV module to utility grid. For example, if the efficiency of both parallel-type dc power optimizer and string inverter is 98%, the efficiency of entire system drops to 96%. Moreover, the cost is higher since there are more power electronics converters. One of feasible solutions to reduce the cost is through the reduction of components and potting materials, which can be achieved by power density improvement.



(a) System architecture of series-type dc power optimizer.



(b) System architecture of parallel-type dc power optimizer.



(c) Micro-inverter.

Figure 1.6. Architectures of modular power converter system.

1. 3 PV Power Conversion Systems for DC Microgrid

DC microgrid systems have great benefits with regard to energy conservation, which has attracted more and more research in the past decades [23]-[26]. Solar, wind and other energies convert to electricity and transfer to DC microgrid. There also have power flows to utility and batteries for energy storage.

Solar energy is considered one of the most important energy sources in dc microgrid system. Modular PV application is one of the mainstreams in dc microgrid, as shown in Figure 1.7. The modular PCS configuration in dc microgrid is similar as parallel-type dc power optimizer for utility application as described before. It directly converts low voltage dc from single PV module to high voltage dc microgrid. Each power electronics converter is independent of others.

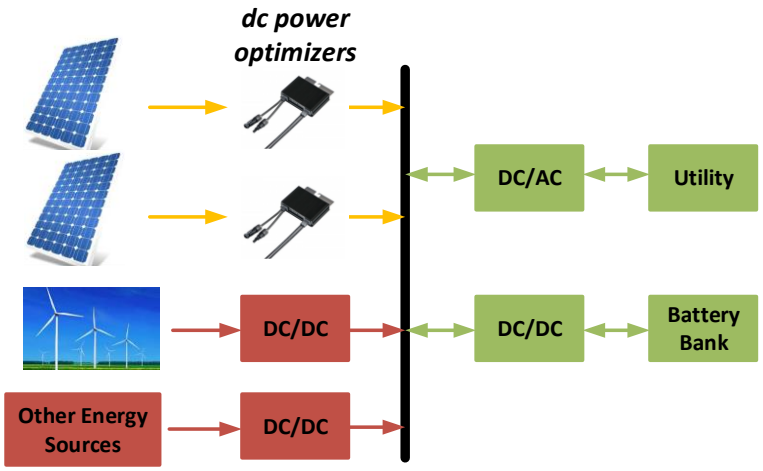


Figure 1.7. DC microgrid system.

Therefore, compared with traditional centralized and string, modular series-type PCS architectures, parallel-type modular configuration such as parallel-type dc optimizer for ac and dc grid and two-stage micro-inverter are receiving more and more attentions in both academic and industry due to their superior MPPT efficiency, scalability, and fault tolerance, however, there are also many challenges on the development of these configurations, such as efficiency, cost and power density.

1. 4 Opportunities of Wide Bandgap Devices on Power Conversion Systems

The comparison of semiconductor materials among Silicon (Si), silicon carbon (SiC) and gallium nitride (GaN) is summarized in Table 1.1. E_G represents the bandgap energy, and high E_G results in a high temperature capability; the E_{BR} is the critical electric field, and high E_{BR} results in high blocking voltage with low on-state resistance; V_s means the saturated drift velocity, which can result in high switching speed capability and μ represents the mobility of electrons of the semiconductor materials [27]-[30].

Compared with Si semiconductor devices, the newly merged wide bandgap semiconductor devices, especially GaN devices, have shown desirable characteristics, such as low on-state resistance, high current capability, high operating frequency and increased junction temperature [31]. The comparison between Si devices and wide bandgap devices is shown in the Figure 1.8. The wide bandgap devices have more potentials to feature with lower conduction loss, lower switching loss and the capability of higher temperature compared with Si devices.

Table 1.1. Semiconductor material comparison.

Characteristics	***Si***	***SiC***	***GaN***
E_G (eV)	1.1	3.3	3.4
E_{BR} (MV/cm)	0.3	3.0	3.3
Vs (x10^7 cm/s)	1.0	2.0	2.5
μ (cm^2/Vs)	1300	650	1500

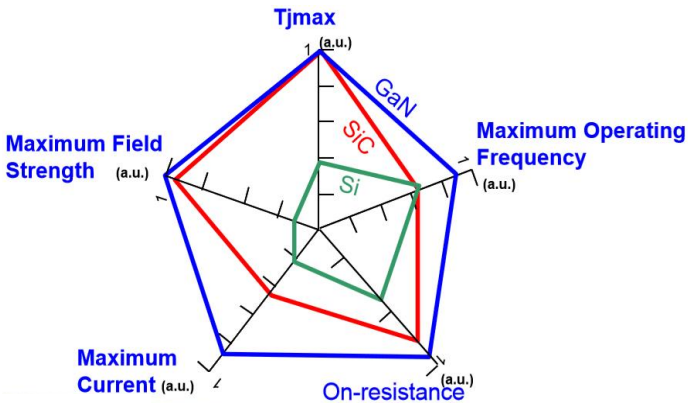


Figure 1.8. Semiconductor devices comparison among Si, SiC and GaN [31].

Now that wide bandgap devices provides the possibility to reduce device loss and increase switching frequency, the power converter will have more opportunities to improve power conversion efficiency and power density. The research work in this dissertation devotes to utilize the wide bandgap devices to improve efficiency and power density of the dc-dc power conversions for parallel-type modular PV applications.

1. 5 Research Objectives

Modular PV generation as one of the most promising alternative energy sources is growing exponentially. Energy saving and cost reduction are substantial for power conversion systems. System volume reduction provides potentials of cost reduction. In order to improve the power conversion efficiency and power density for modular PV applications, the research work in this dissertation evaluates the characteristics of GaN device and proposes a high-efficiency isolated high boost ratio dc-dc converter using GaN devices. The proposed converter can be applied as a parallel-type dc power optimizer for the connection of string inverter in utility grid system or the connection to dc microgrid system directly, or a front-end dc-dc stage of a two-stage micro-inverter. Since these

architecture are all parallel-type, the applications will be uniformed as “parallel-type modular PV applications”. Furthermore, this proposed converter is designed and optimized at megahertz (MHz) switching frequency for the pursuit of high-power density.

The dc-dc converter for parallel-type modular PV applications should be able to meet the following requirements.

(1) Ability to operate at a wide range of input voltage;

(2) High voltage boost ratio;

(3) High-efficiency over wide range operating conditions;

(4) Although isolation is not required because terminals of PV modules may not necessarily be grounded [32], the proposed converter also provides galvanic isolation so that the PV modules can be isolated from the ac or dc grid during fault conditions. This type of isolated design normally results in a poorer efficiency; however, if the converter operates under soft-switching conditions, it is able to achieve ultrahigh-efficiency that is comparable to or even better than most non-isolated designs [33].

1. 6 Outline of the Dissertation

This dissertation includes 6 chapters. The dissertation is organized as follows.

Chapter 1 introduces the development of solar energy in decades and the projected development in the future, and the architectures of associated power conversion systems for utility and dc microgrid applications.

Chapter 2 summaries the state-of-the-art dc-dc topologies for parallel-type modular PV applications in the literatures and commercial.

Chapter 3 explores the characteristics of GaN power semiconductor devices and its impact on modular PV applications. The evaluation of a 650-V GaN device from GaN Systems Inc was given.

Chapter 4 proposes a high-efficiency isolated dc-dc topology with a new modulation method to achieve wide range regulation for parallel-type modular PV applications. This chapter provides the detailed analysis on the circuit operation and hardware design, as well as the digital implementation for the proposed control strategy. A 300-W hardware prototype using GaN devices is presented to validate the performance of the proposed converter.

In chapter 5, the proposed converter is extensionally designed and optimized at MHz switching in an effort to design for high-power density. A comprehensive comparison of hardware design between hundred kilohertz (KHz) and MHz switching frequency is given. The design considerations of reducing parasitics effects under MHz switching is analyzed with finite element method (FEM). The printed circuit board (PCB) layout and transformer design are optimized through simulation and validated with experiments.

Finally, Chapter 6 provides a summary and contributions of the work in this dissertation and plans for future research work.

Chapter 2 State of the Art of DC-DC Topologies for Parallel-type Modular PV Applications

This chapter gives a review of existing isolated dc-dc converter topologies that are suitable for parallel-type modular PV applications. As descripted in Chapter 1, dc-dc converters for parallel-type modular PV applications should at least meet the requirements of high voltage boost ratio, wide range regulation, and high-efficiency, meanwhile, isolation should be considered as a preference. There have been many topologies that were proposed in the previous literatures and used in commercial products suitable for this application.

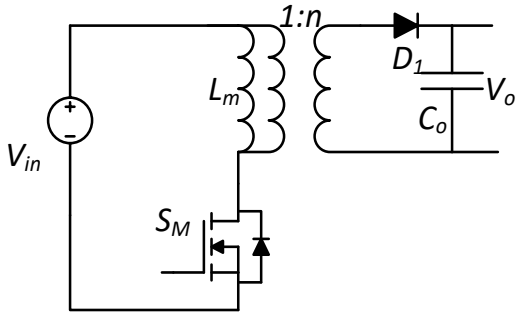
2. 1 Pulse Width Modulation (PWM)-Based Converters

The most conventional category is flyback and the flyback-derived converter with traditional PWM, where regulation is achieved by duty adjustment with fixed-frequency, such as [34]-[38]. The example circuits of flyback and the flyback with active clamp are shown in Figure 2.1 (a) and (b) respectively.

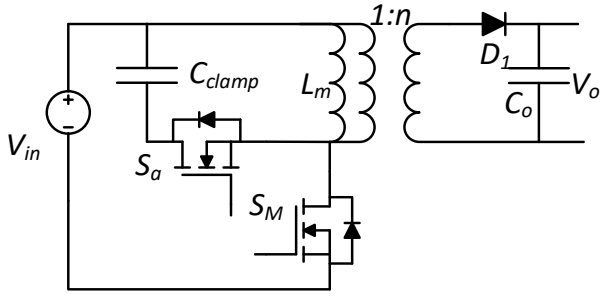
Although flyback converter have the advantages of simple structure, easy control and low cost due to low part count, it suffers from the problems of low magnetics utilization resulting in large magnetics component and high leakage energy of transformer resulting in low efficiency and high voltage spike on main switch. To overcome the limitation of low magnetics utilization, interleaved flyback converter gains attraction from researchers, however, it still has the leakage energy problem.

Some converters were derived based on the traditional flyback converter to improve efficiency. In [35], [36], an active clamp branch is added to the basic flyback circuit and

interleaved flyback, respectively, which serves to recycle transformer leakage energy and minimize switch voltage stress. An optimized control strategy with combination of discontinuous conduction mode (DCM) and boundary conduction mode (BCM) is proposed to improve efficiency over entire operating range in [37]. A quasi-resonant flyback-forward converter is proposed in [38], where the transformer leakage inductance and an added capacitor are resonance to achieve soft-switching feature on the primary switches. Although the efficiencies of these derived converters are improved compared with basic flyback converter, they add many additional components or increase control complexity. The highest efficiency of these converters is still limited due to hard-switching. This is because the output diodes still turn off under high current condition to cause severe reverse recovery issue during certain load range, even though the circuit achieves soft-switching on the primary switches in some of aforementioned literatures.



(a) Conventional flyback converter.

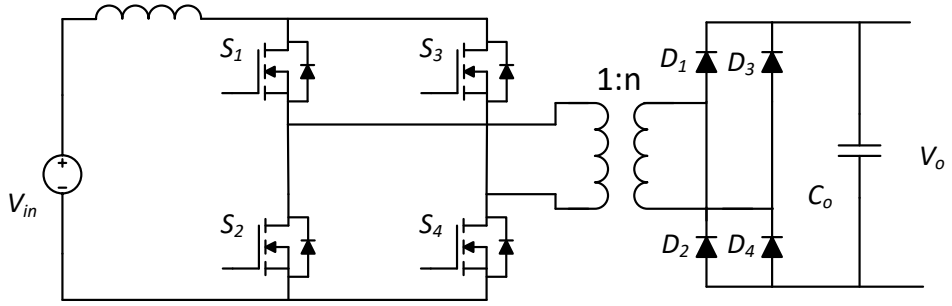


(b) Flyback converter with active clamp circuit.

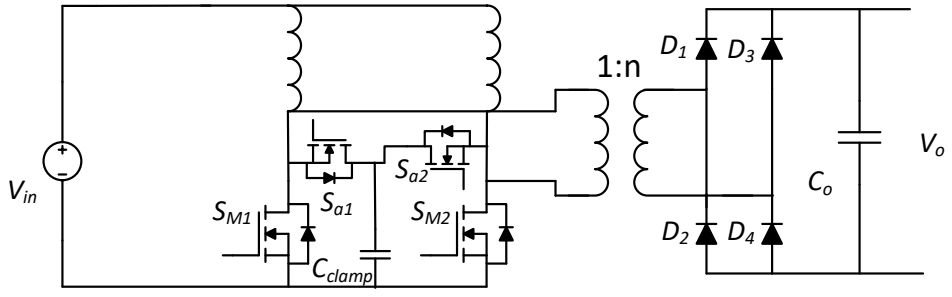
Figure 2.1. Examples of Flyback and flyback-derived topologies.

These drawbacks make the conventional flyback and flyback-derived converters unattractive for modular PV applications.

Besides the flyback converters, bridge-based PWM converters that are suitable for modular PV applications have been presented in the literature [39]-[43]. The examples of current-fed bridge-based converters are shown in Figure 2.2. The current-fed converter has a boost behavior for high voltage gain, which benefits for step-up applications. Similar as flyback converter, the regulation is achieved by duty adjustment with fixed-frequency. However, half-bridge, full-bridge, and upgraded interleaved full-bridge current-fed converters all have the problems of hard-switching, switches ringing, and snubber loss due to the leakage of transformer [39] - [41].



(a) Conventional current-fed full-bridge converter.



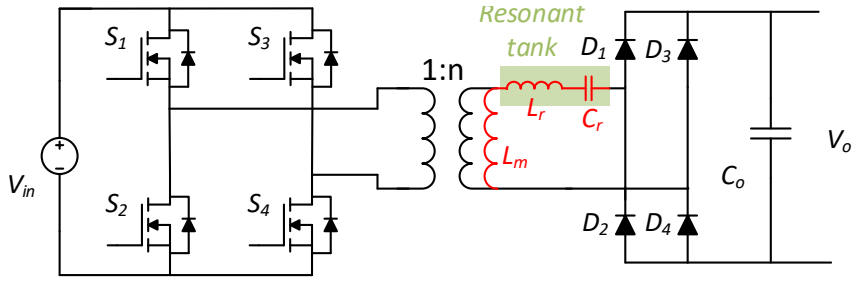
(b) Current-fed half-bridge converter with active clamp circuit.

Figure 2.2. Examples of current-fed bridge-based PWM topologies.

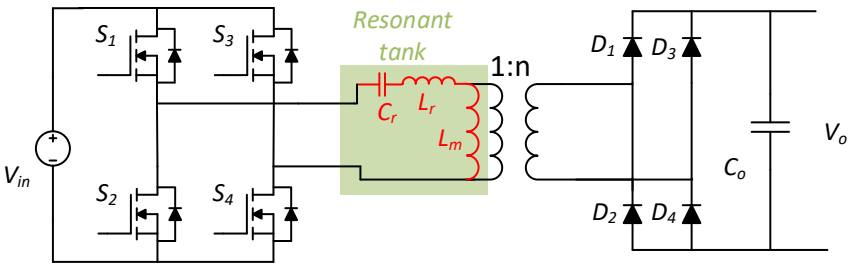
To solve leakage energy problem, auxiliary circuit, such as active-clamp circuit, is added on the conventional current-fed converter [40]. There are also many extended bridge-based current-fed converters. A snubberless current-fed half-bridge converter is proposed in [42]. The topology attains clamping of the device voltage by secondary modulation to eliminate the need of snubber or active-clamp. In [43], an L-L type current-fed converter is presented to achieve zero-voltage-switching (ZVS) at a wide range operation. However, besides the increased circuit complexity, they cannot achieve both ZVS and zero-current-switching (ZCS) during entire load operation. Therefore, the efficiencies of these topologies are also limited.

2. 2 Resonant Converters

Another category is resonant converters with soft-switching feature. Isolated series resonant converter (SRC) and *LLC* resonant converter receive wide attractions in terms of high-efficiency [44]-[60]. The basic topologies are shown in Figure 2.3. The configurations on both primary and secondary sides can be replaced by other networks such as half-bridge, push-pull and etc.



(a) Full-bridge SRC.



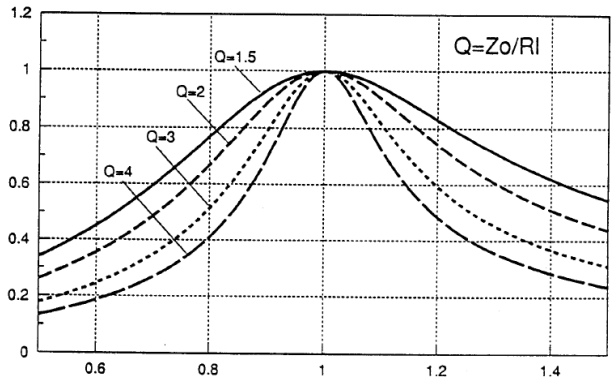
(b) Full-bridge *LLC* resonant converter.

Figure 2.3. Examples of basic SRC and *LLC* resonant converter.

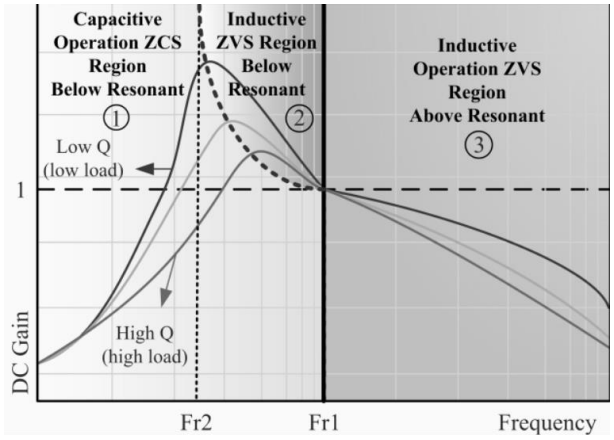
2.2.1 Single-Mode Modulation

The most efficient operating point of SRC is at or slightly below the series resonant frequency [44]. At this point, the energy directly transfers from source to load through the entire switching cycle. The primary switches achieve ZVS turn-on and near ZCS turn-off, while the secondary rectifier achieves ZCS turn-off. However, the voltage gain is fixed at one and it lacks regulation ability, which cannot meet the requirement for PV application. SRC is generally used to operate at or slightly below the series resonant frequency for fixed-input and fixed-output applications due to its high-efficiency.

In order to overcome the inability of regulation, variable-frequency control can be adopted to the SRC. The voltage gain curves based on the switching frequency are plotted in Figure 2.4 (a). Another conventional control method is phase shift control with fixed-frequency [45] - [49]. However, no matter variable-frequency control or phase shift fixed-frequency control can only step down voltage. For the converters designed for modular PV application, the highest efficiency operating point should be designed at nominal input voltage, V_{nom}, which is the nominal output voltage from PV module for the majority of time. Then, it will lack ability for SRC to operate at low input voltage conditions.



(a) Voltage gain curves of SRC.



(b) Voltage gain curves of *LLC* resonant converter.

Figure 2.4. Voltage gain characteristics of SRC and *LLC* resonant converter.

The *LLC* resonant converter is another attractive solution for wide range operation when using variable-frequency control [47] - [48]. Differently with SRC, the magnetizing inductance of transformer involves in the resonant network as shown in Figure 2.3 (b). From the gain curves in Figure 2.4 (b), the *LLC* resonant converter can achieve both voltage step up and step down. Furthermore, the *LLC* resonant converter can achieve soft-switching over a wide operating range. However, to meet the voltage gain range requirement of modular PV application, the ratio of magnetizing inductance to leakage inductance should be selected properly, which increases circuiting current and sacrifices efficiency at the highest efficiency operating point. Additionally, it still has limited operation range and

cannot maintain high-efficiency over a wide range since the circulating energy as well as transformer core loss will be increased significantly when switching frequency is much lower than $f_{r1,}$ and the secondary rectifier has high turn off loss when switching frequency is much higher than $f_{r1.}$ Moreover, it is complicated to model and control the *LLC* resonant converter with frequency modulation.

As aforementioned, although SRC and *LLC* resonant converter can achieve high-efficiency at a certain point or a certain range, they lack ability of wide range operation or high-efficiency over wide range. To extend the advantages of resonant converter topologies, many modified resonant converters were proposed through optimizing primary side bridge-based network, secondary side rectifier or magnetics [50] - [55]. In order to extend the operating range of conventional *LLC* resonant converter, the primary side is replaced with a dual-bridge circuit instead of a conventional bridge-based circuit in [50] and a buck-boost circuit is adopted to the primary side of half-bridge *LLC* resonant converter in [51]. Papers of [52], [53] discusses the modifications on the secondary side rectifier. In [52], the secondary side rectifier is integrated with an interleaved boost converter to make up a voltage multiplier. It could enhance the voltage gain and reduce the voltage stresses of rectifier switches. In [53], *LLC* resonant converter is also modified with reconfigurable voltage multiplier. However, this voltage multiplier contains too many passive and active components. Converters in [54] and [55] modify and improve the magnetic design to obtain the extended operating range of *LLC* resonant converter, where an additional transformer is added in [54] and an additional resonant branch is added in [55]. Although the operating range of these derived resonant converters are improved

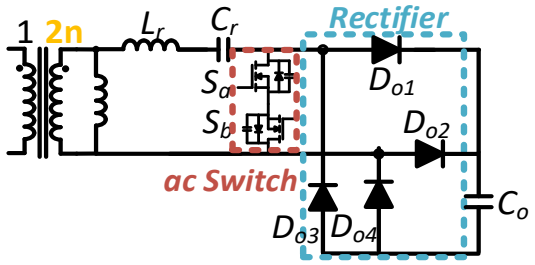
compared with basic resonant converters, they add too many additional components or greatly increase control complexity.

2.2.2 Hybrid-Mode Modulation

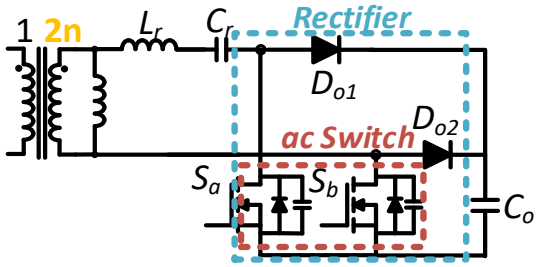
In addition to the modifications on circuit topology, many hybrid modulation schemes were proposed to extend the range of operation in [56]-[60]. A hybrid control combining pulse-frequency modulation and phase shift pulse-width modulation is employed on a full-bridge *LLC* resonant converter, in an effort to achieve high-efficiency over a wide operating range in [56]. In [57], an on-the-fly topology-morphing control based on the efficiency optimization is presented.

Resonant converters with hybrid control method proposed in [58]-[60] employ a boost rectifier in the secondary side with fixed-frequency modulation. The boost rectifier helps to achieve high voltage gain under low input voltage conditions. Under high input voltage conditions, the control scheme for stepping down voltage, such as phase shift control, is applied to the primary side. These converters have shown great performance and high-efficiency over a wide input range because of the ability for direct power transfer over the majority of the switching cycle, low circulating energy with fixed-frequency modulation and soft-switching during the entire operating range. Figure 2.5 summarizes the candidate topologies of boost rectifier presented in [58]-[60]. By controlling the ac switch appropriately, a Boost circuit is built and the converter can achieve high voltage boost ratio. Figure 2.5 (a) shows the most original full-bridge based circuit with separated Boost circuit and rectifier. In Figure 2.5 (b) and (c), Boost circuits are merged into rectifier. However, the rectifier configuration of the converters in Figure 2.5 (a), (b) and (c) is a full-

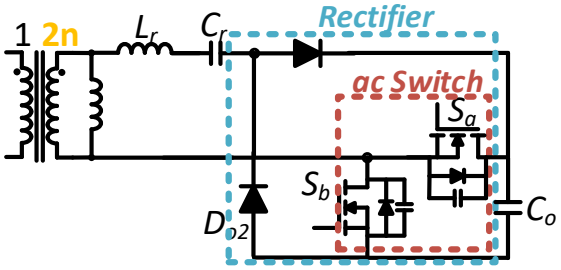
bridge, containing more devices and requiring twice the turns ratio of transformer when compared to the voltage-doubler configuration. Therefore, it results in a higher leakage inductance and more complicated magnetics design. Although the output rectifier configuration is a voltage-doubler as shown in Figure 2.5 (d), the ac switch is added additionally to serve as the switch of Boost circuit, which is separated with rectifier. This ac switch stays off during entire switching cycle when the input voltage is nominal and higher, which is not fully utilized and increases the cost.



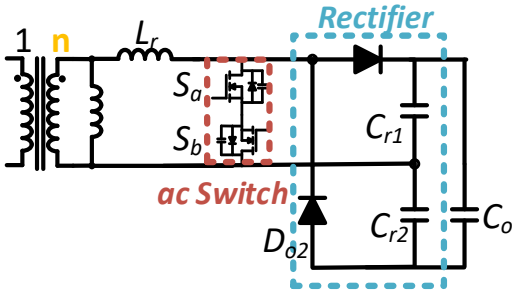
(a) Full-bridge based boost rectifier: Type I.



(b) Full-bridge based boost rectifier: Type II.



(c) Full-bridge based boost rectifier: Type III.



(d) Half-bridge based boost rectifier.

Figure 2.5. Candidate topologies of boost rectifiers.

2. 3 Summary

This chapter explores the existing isolated dc-dc topologies that are suitable for parallel-type modular PV applications.

For the PWM flyback-based converters, the circuit structures and controls are simple, however, they have limitations in terms of efficiency due to leakage energy and low magnetics utilization. For PWM bridge-based converters, they solve the problem of magnetics utilization, however, the efficiency improvements are still limited because of hard-switching transitions.

The most efficient isolated dc-dc converters are SRC and *LLC* resonant converter, since they achieve both ZVS and ZCS. However, they either lack the capability of wide range operation or cannot maintain high-efficiency over a wide range. Modifications on the circuit topologies can extend the operating range of basic resonant converters. However, they add too many components or have complicated control strategies, which are not suitable for hundred-watts PV applications. Hybrid-mode operation is a desirable choice to extend the operating range while keeping on the benefits of highly-efficient conventional SRC and *LLC* resonant converter.

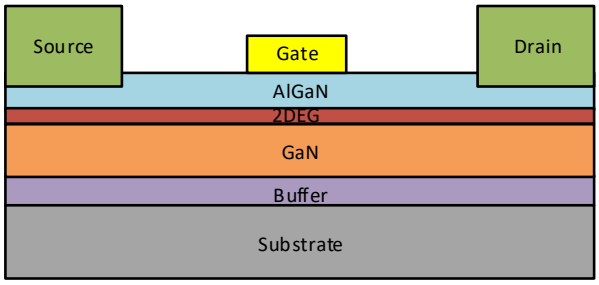
Chapter 3 Impact of GaN Devices

The characteristics and benefits of GaN devices on dc-dc power converter will be discussed in this chapter. It is necessary to acquire the static and switching characteristics of GaN devices before the analysis and design of converter power stage. An evaluation and testing of 650-V GaN power device from GaN Systems Inc will be given. This GaN device is firstly tested with buck converter to obtain switch performance under hard-switching condition and then tested with SRC to obtain switch performance under soft-switching condition.

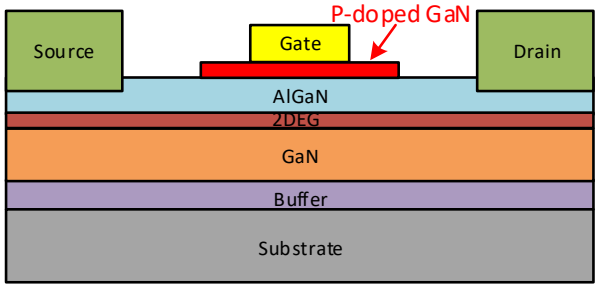
3.1 Characteristics of GaN Devices

Figure 3.1 (a) shows the basic structure of GaN high electron mobility transistors (HEMT), which is a lateral structure [61]. A GaN layer and a multi-layer buffer are deposited on the substrate wafer. The most common material of substrate is typical silicon in commercial products. It also can be silicon carbon or sapphire. The two-dimensional electron gas (2DEG) creates a low-resistance current path between the drain and source terminals, which is in a normally-on state. Therefore, the GaN HEMT is a normally-on device. A Schottky gate is deposited on the AlGaN cap layer, which is used for depleting the 2DEG to turn off the device when negative voltage applies to the gate. Unlike a Si MOSFET, there is no body region connected to the source under the gate electrode, therefore there is no body diode in a GaN HEMT. However, it has self-commutated reverse conduction due to the symmetry structure of the drain and source terminals.

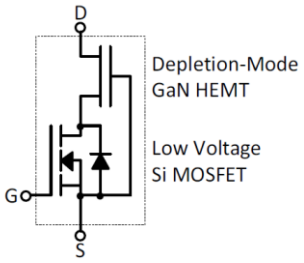
Normally-on device is not desirable considering reliability. It will cause the short circuit when the gate power supply is not working. There are two methods to achieve normally-off. One is enhancement-mode GaN (eGaN), while the other one is cascode structure. Figure 3.1 (b) shows one of eGaN structures, which adopts a p-doped GaN cap beneath the gate to increase the threshold voltage of turning on device to a positive voltage. There are also other methods to lift the threshold voltage to a positive voltage for eGaN devices, such as p-doped AlGaN gate or adding gate insulators. Compared with Si MOSFET, the gate of GaN device has low threshold voltage and drive voltage, and gate drive design is sensitive. Many companies such as EPC Inc and GaN Systems Inc use eGaN structure [62]. The cascode GaN is incorporating a low voltage enhancement-mode Si MOSFET to create a cascode structure, as shown in Figure 3.1 (c). However, the package parasitics of cascode structure is relatively high. Commercialized devices can be found in Transphorm Inc [63]. This work will focus on the exploration and application of eGaN.



(a) Basic structure.



(b) P-dopted GaN under gate to build an enhancement-mode normally-off device.



(c) Circuit model of a cascode GaN HEMT.

Figure 3.1. Structure of GaN HEMT.

The I-V output characteristic of eGaN is shown in Figure 3.2. When gate-to-source voltage, v_{gs}, is higher than threshold voltage, it enters into a FET mode. The devices will be saturated at high current condition. The device can also turn on with reverse condution mode when the gate-to-source voltage is zero, which is aimilar as a diode characterisitc. The main difference is that there is no reverse recovery in self-commutated reverse conduction mode for GaN device.

Back to the FET mode, the output characteristic is mainly affected by gate-to-source voltage, temperature and etc. The output curves with different gate-to-source voltages and different temperatures are usually given in datasheets of released commercial devices [62], [64]. When the gate-to-source voltage becomes higher, the device turns on with a lower drain-to-source voltage under the same current condition and it will be saturated if the current continuously increases. At higher temperature condition, the drain-to-source voltage increases under the same gate-to-source voltage condition and saturated current becomes lower. The on-state resistance of device can be calculated from the I-V output characteristic. Taking GS66504B as an example, Figure 3.3 shows the relationship between on-state resistance and current with different gate-to-source voltages and temperatures conditions. The higher gate-to-source voltage will result in a lower on-state

resistance, which is desirable for low conduction loss. Additionally, the lower temperature also cause a lower on-state resistance.

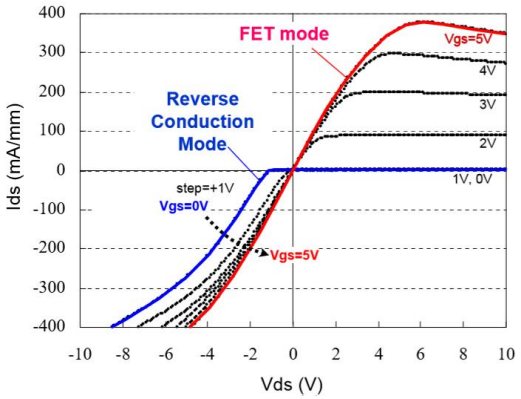
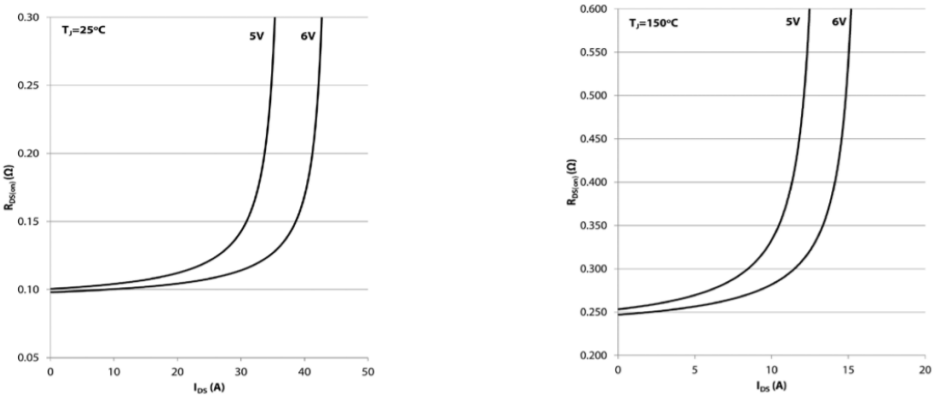


Figure 3.2. On-state I-V characteristic of eGaN at 25 ^{o}C [31].



(a) at 25 ^{o}C (b) at 150 ^{o}C

Figure 3.3. On-state resistance versus current of GS66504B with different gate-to-source voltages at different temperature conditions [64].

The charateristic of the reverse conduction mode is critical when designing soft-switching converters, since the device should turn into the reverse conduction mode before applying the gate-to-source voltage to achieve ZVS. The static reverse-conducting voltage of GS66504B is tested under zero gate-to-source voltage condition, as shown in Figure 3.4. The reverse-conducting voltage of reverse condution mode is much higher than the body diode's forward voltage of conventional Si MOSFET. The reverse-conducting voltage

increases when the current and temperature increase. It reaches up to 2.2-V at 2-A conditions.

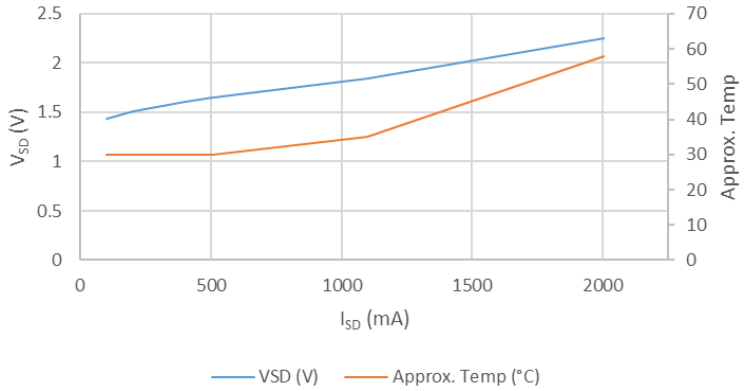


Figure 3.4. Tested reverse-conducting voltage v.s. current of GS66504B.

Compared with super-junction Si MOSFET, GaN has much smaller junction parasitics. Figure 3.5 compares the gate charge between GS65504B from GaN Systems Inc and IPD60R170CFD7 from Infineon Inc [64], [65]. Two devices have similar blocking voltage and current capability to guarantee a fair comparison. The gate charge of GaN device is only a quarter of the gate charge of super-junction Si MOSFET. Figure 3.6 shows the comparison of the parasitic capacitances and the energy storage in output capacitances between super-junction Si MOSFET and eGaN HEMT. To ensure a fair comparison, both selected devices have 600-V blocking voltage and 70 mΩ on-resistance. The output capacitance of GaN device can be as small as one of tenth of the super-junction Si MOSFET. Due to small junction parasitics, GaN devices have features of fast di/dt and dv/dt, which benefits for switching loss reduction.

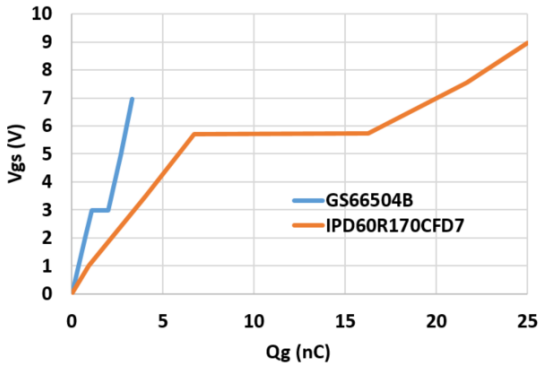


Figure 3.5. Comparison of gate charge between GaN and Si MOSFET.

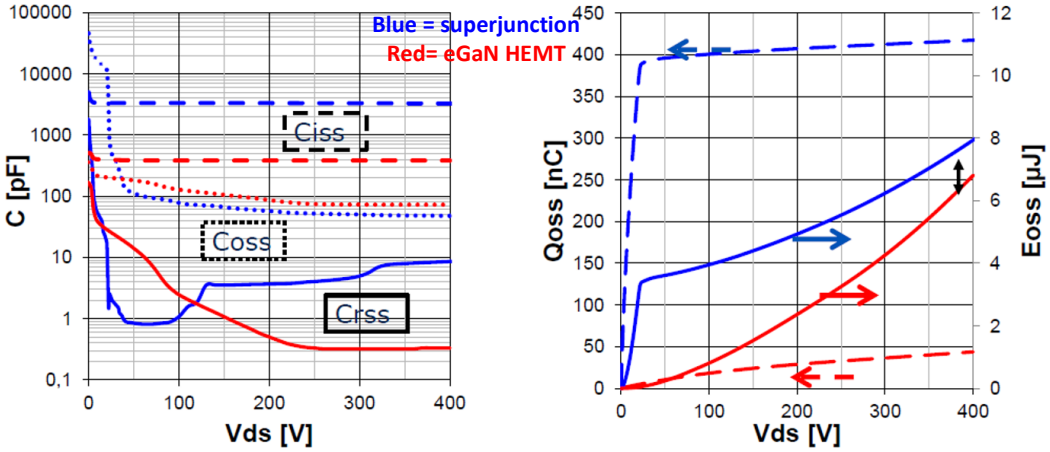


Figure 3.6. Comparison of output parasitics and its energy charge between GaN and Si MOSFET.

3.2 Evaluation and Testing of 650-V eGaN Device

In this section, switching characteristics and thermal performance of a 650-V eGaN device will be evaluated with conventional buck converter and SRC. The picture of hardware evaluation board is shown in Figure 3.7, which is designed from GaN Systems Inc [66]. This board consists of two 650-V eGaN devices for a half-bridge, gate drive circuits, isolated auxiliary power supplies and heatsink. A heatsink with size of 35mm x 35mm is provided as an option to be attached to the bottom side of board for optimum

cooling. GS65504B is designed with 650-V blocking voltage, 15-A continuous drain-to-source current and 100 mΩ on-state resistance.

Figure 3.7. eGaN HEMT evaluation board.

3.2.1 Testing with Buck Converter

Figure 3.8 shows the circuit of tested buck converter. The input voltage, V_{DC}, is set at 400-V, and the switching frequency is fixed at 50-kHz. The gate signal to S_1 and S_2 has 50% duty cycle and they are complementary. The inductance of L is selected as 2.5 mH to guarantee the continuous conduction mode (CCM) operation.

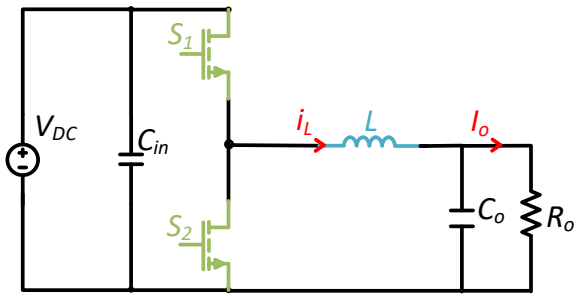


Figure 3.8. The circuit of tested buck converter.

The steady-state testing waveforms under 1-A load condition are shown in Figure 3.9, where the green curve is gate-to-source voltage of S_1, v_{gs1}, blue curve is gate-to-source voltage of S_2, v_{gs2}, light blue curve is drain-to-source voltage of S_2, v_{ds2}, and the purple

curve is current though inductor, i_L. The current ripple is 0.8-A, and the peak current reaches to 1.5-A. The waveforms are pretty clean under the hard-switching condition.

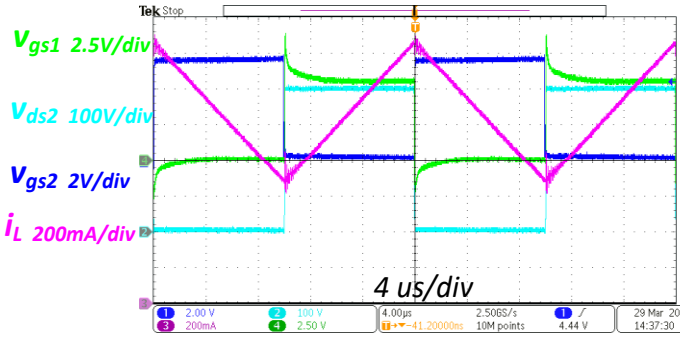
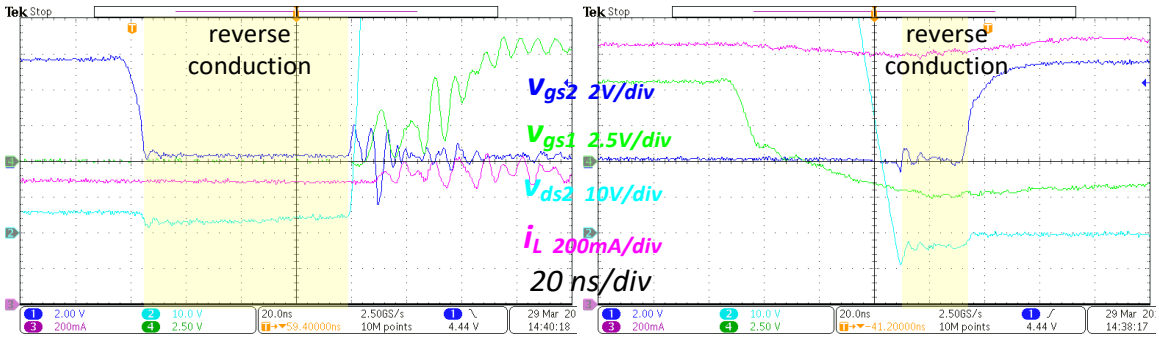


Figure 3.9. Experimental steady-state waveforms under 1-A load condition.



(a) During S_2 turn-off and S_1 turn-on. (b) During S_1 turn-off and S_2 turn-on.

Figure 3.10. Experimental transition waveforms during dead-time period under 1-A load condition.

To further explore the switching performance during the switching transitions, Figure 3.10 shows the waveforms details during the dead-time periods. During the period between S_2 turn-off and S_1 turn-on as shown in Figure 3.10 (a), S_2 continuously conducts with the reverse condition mode, behaving like a “diode”, and then it is forced to turn off when v_{gs1} applies. Both S_1 turns on and S_2 turns off under high current condition. S_2 shows zero reverse recovery. During the period between S_1 turn-off and S_2 turn-on, S_1 turns off and S_2 enters into reverse conduction mode, as shown in Figure 3.10 (b). Therefore, S_2 achieves ZVS, since it conducts before v_{gs2} applies. It can be measured by scope trace that

the dynamic reverse-conducting voltage of reverse conduction mode is around 2-V, which is much higher than body diode of Si MOSFET.

To obtain full understanding of dynamic switching performance, more experiments were conducted under 2-A load condition when other specifications and circuit parameters are kept as same. Figure 3.11 and Figure 3.12 show the steady-state waveforms and detailed waveforms during switching transitions, which are similar as under 1-A condition. The maximum current through inductor is 2.5-A. S_1 switches under hard-switching conditions and S_2 achieves ZVS turn-on. Compared with 1-A load condition, the dynamic reverse-conducting voltage of reverse conduction measured by scope is higher and reaches to near 3-V as shown in Figure 3.12.

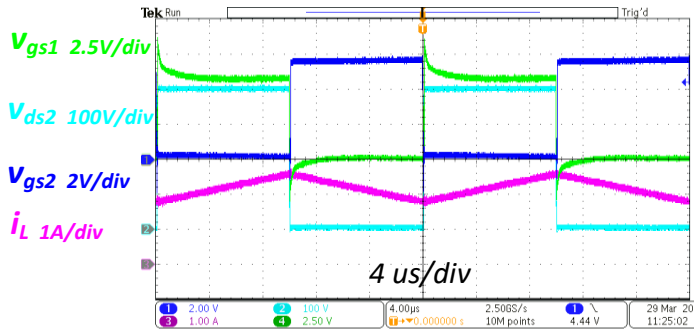
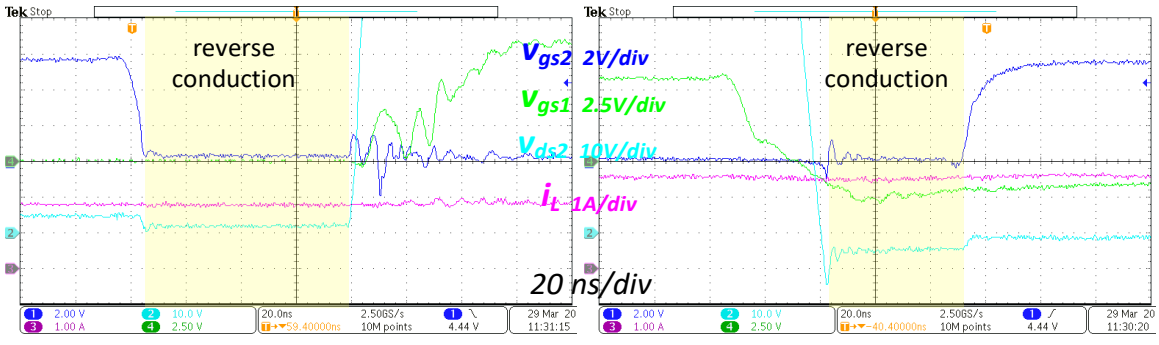


Figure 3.11. Experimental steady-state waveforms under 2-A load condition.



(a) During S_2 turn-off and S_1 turn-on. (b) During S_1 turn-off and S_2 turn-on.

Figure 3.12. Experimental transition waveforms during dead-time period under 2-A load condition.

Since the turn-on and turn-off switching loss is given in the evaluation report from GaN Systems Inc [66], the double-pulse testing were not operated here. Figure 3.13 shows the switching loss measurement of GS66504B. The turn-off switching loss remains at 3.6uJ from 0-A to 10-A, while the turn-on switching loss dominates the overall hard-switching loss, which increases from 12uJ to 42uJ when current changes from 0-A to 15-A.

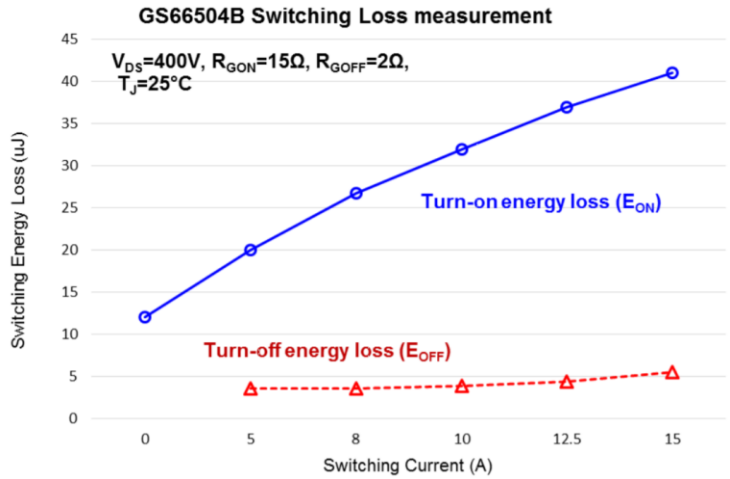


Figure 3.13. Tested turn-on and turn-off switching loss [66].

3.2.2 Testing with Series Resonant Converter

After the investigation of switching characteristics under hard-switching condition, this section will evaluate the switch performance when switch S_1 is under ZVS condition. Figure 3.14 shows the circuit of tested SRC converter. The input voltage, V_{DC}, still keeps at 400-V. The gate signal to S_1 and S_2 has 50% duty cycle and they are complementary, similarly as previous tested buck converter. In order to ensure the ZVS operation of S_1, the switching frequency is designed higher than the resonant frequency. L_r is designed as 95 μH and C_r is selected as 33 nF considering impedance design, so the resonant frequency is 90-kHz. The switching frequency is selected at 100-kHz, which is above the resonant

frequency. Three different conditions are tested with load resistance of 94 Ω, 188 Ω, and 396 Ω, which can cover the range from full ZVS to partial ZVS.

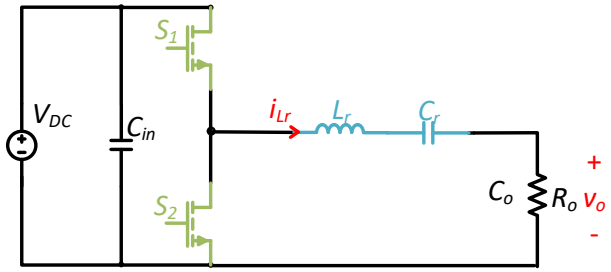
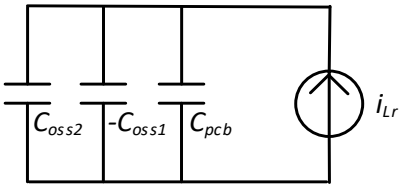


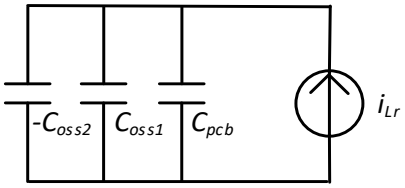
Figure 3.14. The circuit of tested SRC.

The parasitic output capacitance of device is a critical parameter to be considered when designing for ZVS operation. The equivalent circuit during dead-time period is modeled in Figure 3.15, where resonant current, i_{Lr}, acts as a current source to charge and discharge the parasitic output capacitances of two devices and the parasitic capacitance induced from printed circuit board (PCB). Based on the capacitor charge balance, the relationship between current and capacitance can be expressed in (3.1), where t_d is the length of dead-time [67]. Therefore, the total capacitance can be calculated by the waveform measurement during dead-time period.

$$I_{DT} = (2C_{oss} + C_{pcb})\frac{V_{DC}}{t_d} \tag{3.1}$$



(a) During S_2 turn-off and S_1 turn-on.



(b) During S_1 turn-off and S_2 turn-on.

Figure 3.15. Equivalent circuits during dead-time periods.

Figure 3.16 shows the steady-state testing waveforms under 94 Ω load condition. The blue, light blue, purple and green waveforms represent gate-to-source voltage of S_2, v_{gs2}, drain-to-source voltage of S_2, v_{ds2}, current though resonant inductor, i_{Lr}, and the output voltage, v_o, respectively. The peak current reaches to 2.4-A, and the turn-off current of S_1 is 1.5-A. The detailed transition waveforms during the dead-time periods are shown in Figure 3.17. Figure 3.17 (a) shows the period between S_2 turn-off and S_1 turn-on, while Figure 3.17 (b) shows the period between S_1 turn-off and S_2 turn-on. In Figure 3.17 (a), the resonant current discharges the output capacitance of S_1 and charges the output capacitance of S_2. After the output capacitance of S_1 is fully discharged, the switch is reversely conducted with reverse conduction mode. After that, voltage applies to gate of S_1 to turn on the switch, and S_1 achieves ZVS turn-on. It takes 64 *ns* to complete the capacitor charging and discharging at condition of 1.4-A average current. Similarly, S_2 achieves ZVS turn-on since the resonant current fully charges the output capacitance of S_1 and discharges the output capacitance of S_2 in Figure 3.17 (b). The average resonant current also keeps around 1.4-A, and it takes 60 *ns* to charge and discharge the capacitance. According to (3.1), the total capacitance including two parasitic output capacitances of devices and parasitic capacitance from PCB is approximate to 224pF.

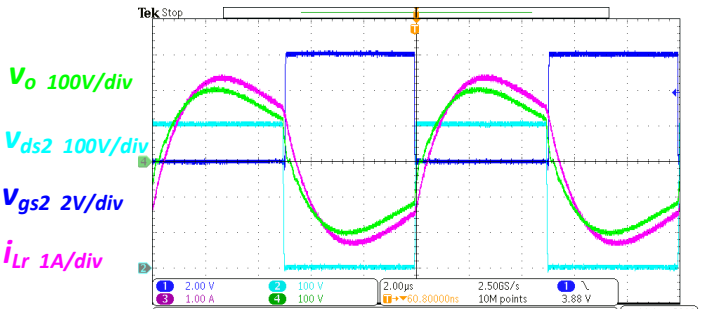
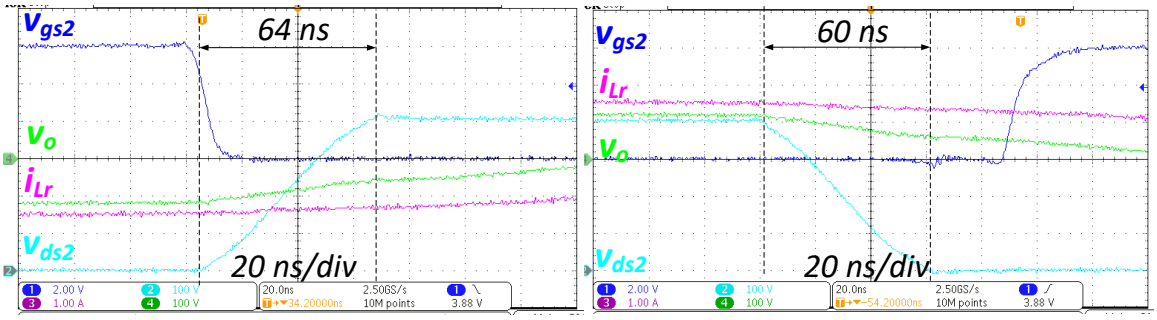


Figure 3.16. Experimental steady-state waveforms under 94 Ω load condition.



(a) During S_2 turn-off and S_1 turn-on. (b) During S_1 turn-off and S_2 turn-on.

Figure 3.17. Experimental transition waveforms during dead-time period under 94 Ω load condition.

The steady-state testing waveforms under 188 Ω and 396 Ω load conditions are shown in Figure 3.18 and Figure 3.20 respectively. Figure 3.19 and Figure 3.21 show the detailed transition waveforms during the dead-time periods under 188 Ω and 396 Ω load conditions. However, under these conditions, the resonant current is too low to fully charge and discharge the parasitic capacitances. S_1 and S_2 are limited at partial ZVS operation. For example, it takes 80 *ns* to have 290-V voltage change across drain-to-source terminals of S_1 and S_2 in Figure 3.19 (a), and the voltage change in Figure 3.19 (b) is 320-V within 89 *ns* time, when the average current during dead-time is 0.8-A. Since the output capacitance of device is nonlinear in reality, it is inaccurate to estimate the capacitance under partial ZVS condition. In Figure 3.21, the average current during dead-time period drops to 0.3-0.4 A, which is too low to provide the required energy.

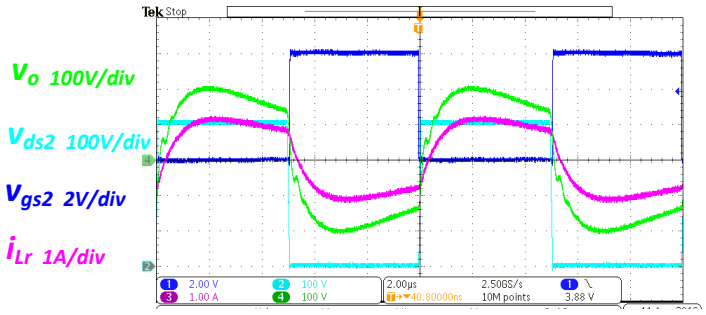
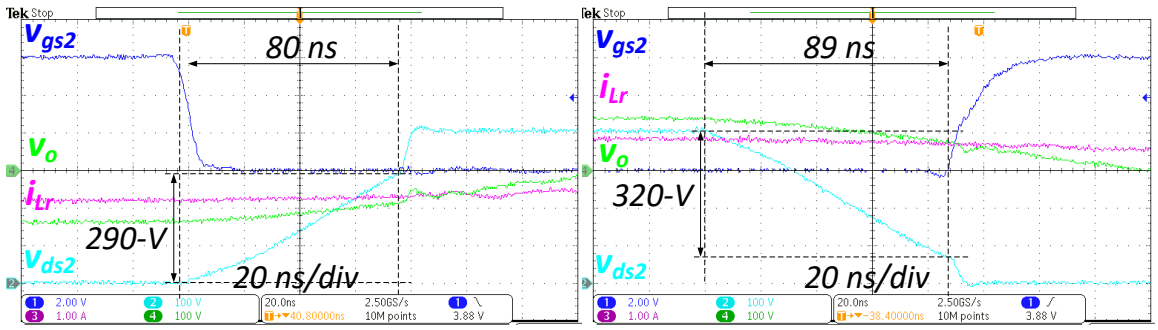


Figure 3.18. Experimental steady-state waveforms under 188 Ω load condition.



(a) During S_2 turn-off and S_1 turn-on. (b) During S_1 turn-off and S_2 turn-on.

Figure 3.19. Experimental transition waveforms during dead-time period under 188 Ω load condition.

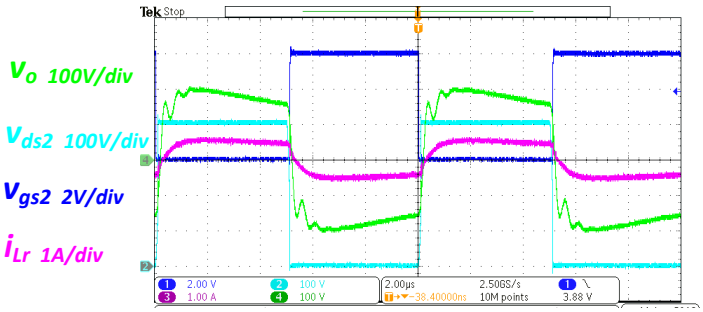
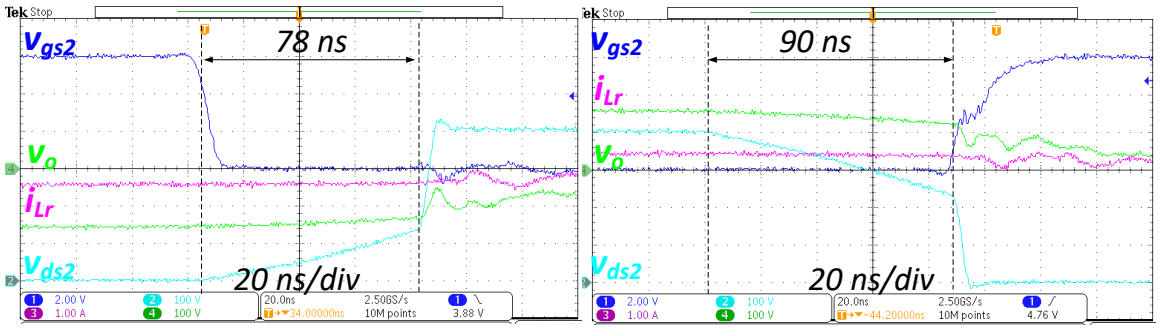


Figure 3.20. Experimental steady-state waveforms under 396 Ω load condition.

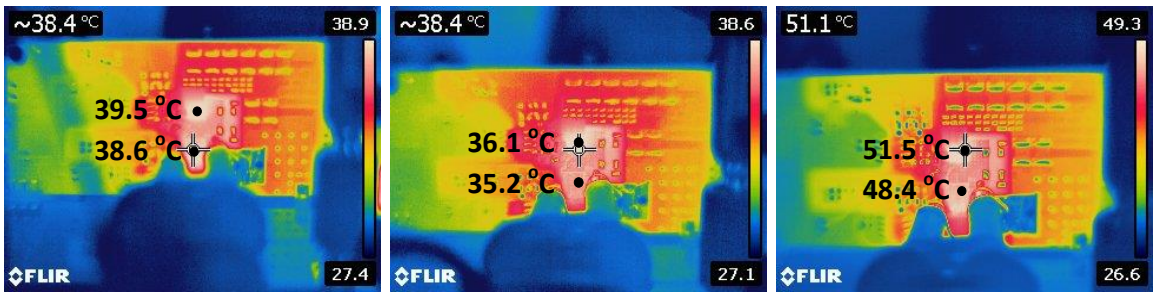


(a) During S_2 turn-off and S_1 turn-on. (b) During S_1 turn-off and S_2 turn-on.

Figure 3.21. Experimental transition waveforms during dead-time period under 396 Ω load condition.

Although the devices cannot fully achieve ZVS under 188 Ω load condition, the switching loss is not high because it already discharges a large portion of capacitance. Therefore, the temperature of devices is lower compared with 94 Ω load condition as

shown in Figure 3.22 (a) and (b), when conduction loss is the largest part in the overall loss. However, in Figure 3.22 (c), the device temperatures rise significantly under 396 Ω load condition, where switching loss dominates the overall loss due to hard-switching turn-on.



(a) 94 Ω load condition. (b) 188 Ω load condition. (c) 396 Ω load condition.

Figure 3.22. Device temperature measurement.

To validate the accuracy of parasitic capacitance estimation, the measurements of dead-time period under different current conditions were completed which is summarized in Table 3.1. The estimated total capacitances are in the range of 220~230 pF.

Table 3.1. Testing and estimation of parasitic capacitances.

I_{Lr_avg} (A)	t_d (ns)	ΔV_c (V)	C_{tot} (pF)
2.55	36	400	230
1.45	64	400	232
0.93	96	400	222

3.3 Summary

In this chapter, the general characteristics of GaN devices are given at first. After this, a 650-V eGaN is tested and evaluated based on conventional buck converter and SRC.

The GaN device has a normally-on structure inevitably. By adopting a certain material cap beneath the gate, the device becomes a normally-off eGaN, however, it has low threshold voltage, which makes the gate drive sensitive. By incorporating a low-voltage Si MOSFET, the device turns into a cascode GaN, however, it induces large package parasitics, which limits the benefits of GaN device. Compared with Si MOSFET, the GaN device features of small parasitics, fast switching, high blocking voltage and potentially low on-state resistance. Although the device doesn't have a body diode, it can inversely conduct, behaving as a "diode" with zero reverse recovery. However, the reverse-conducting voltage of reverse conduction is as high as 2-3 V. Even though the device has high dv/dt and di/dt transitions, the overall loss is still dominated by switching loss under the hard-switching condition. Therefore, even using GaN devices, the soft-switching feature is essential when targeting at high-efficiency.

Chapter 4 Proposed High-Efficiency DC-DC Converter for Parallel-type Modular PV Applications

In this chapter, a GaN-based high-efficiency high step-up isolated dc-dc converter with a novel modulation method is proposed for parallel-type modular PV applications. The proposed modulation method allows the converter to boost low input voltages and regulate wide input voltage range. The converter is designed and optimized based on a SRC which operates at the resonant frequency to achieve highest efficiency under nominal input voltage condition. Under shaded or low irradiance conditions of PV modules, the converter will operate with the proposed modulation method to step up the voltage to the standard output voltage. The proposed converter with employed modulation method allows the converter not only keeping the benefits of highly-efficient SRC converter but also achieving higher voltage boost ratio than SRC without the need of extra switches while operating at fixed-frequency. The detailed analysis of the proposed modulation scheme as well as the derivation of voltage conversion ratio is depicted in section 4.2. Section 4.3 and 4.4 give the design procedure of power stage and digital implementation of the proposed modulation method. In section 4.5, experimental results based on a 300-W GaN-based prototype are presented. This proposed converter is published in [97].

4. 1 Overview on Proposed Topology

As aforementioned in Section 2.2.2, resonant converters in [58] - [60] employ a boost rectifier with the combination of Boost circuit and rectifier in the secondary side to achieve wide operation range with fixed frequency. They have significant advantages

compared with other topologies reviewed in Chapter 2. However, full-bridge configuration contains more devices and needs higher turns ratio of transformer, as shown in Figure 2.5 (a), (b) and (c). Although the circuit is a half-bridge configuration in Figure 2.5 (d), the Boost circuit and rectifier are separated resulting in low utilization of devices and high cost. In this chapter, an active-boost-rectifier based on half-bridge configuration is proposed by merging Boost circuit and rectifier as shown in Figure 4.1. The diodes of rectifier circuit are replaced with active switches. The secondary side switches are for synchronous rectification while serving for voltage boost function, eliminating the need of ac switch. In order to achieve wide input voltage range regulation and obtain high voltage boost ratio, a new modulation method, referred to as "double-pulse duty cycle", is proposed for low input voltage conditions. The regulation is achieved through duty adjustment with fixed-frequency control other than variable-frequency control. The turns ratio of the transformer is halved compared to the full-bridge based rectifier, and the number of power devices can be reduced. Table 4.1 compares the transformer turns ratio and component number among the boost rectifiers in Figure 2.5 and the proposed active-boost-rectifier in Figure 4.1. The proposed active-boost-rectifier requires lowest number of devices while maintaining a low transformer turns ratio.

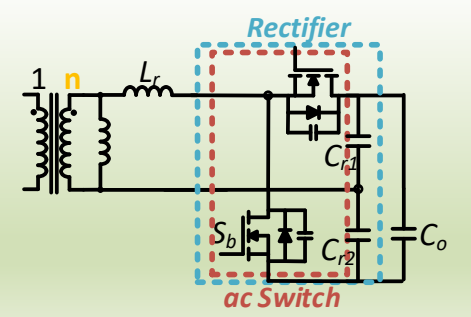


Figure 4.1. Proposed half-bridge based active-boost-rectifier.

Table 4.1. Comparison of boost rectifier circuits.

Boost rectifier topology	*Turns ratio of transformer*	*Number of switches*	*Number of diodes*
Figure 2.5 (a)	1:2n	2	4
Figure 2.5 (b)	1:2n	2	2
Figure 2.5 (c)	1:2n	2	2
Figure 2.5 (d)	1:n	2	2
Figure 4.1 Proposed	1:n	2	0

The presented converter with the proposed secondary rectifier is shown in Figure 4.2. The topology looks identical to a conventional full-bridge bidirectional resonant converter [68]. However, the purpose and design of the proposed converter is entirely different with bidirectional resonant converter. The primary side is a full-bridge comprised of switches $S_{1\text{-}4}$ and secondary side is an active-boost-rectifier comprised of switches $S_{5,6}$. Each switch is modeled with a channel, a "body diode" and a parasitic output capacitance. L_r, C_{r1} and C_{r2} compose of the resonant tank network, where L_r is the summation of transformer leakage inductance and external inductor and C_{r1} is equal to C_{r2}. For the high frequency transformer, n is the turns ratio and L_m is the magnetizing inductance reflected in the secondary side.

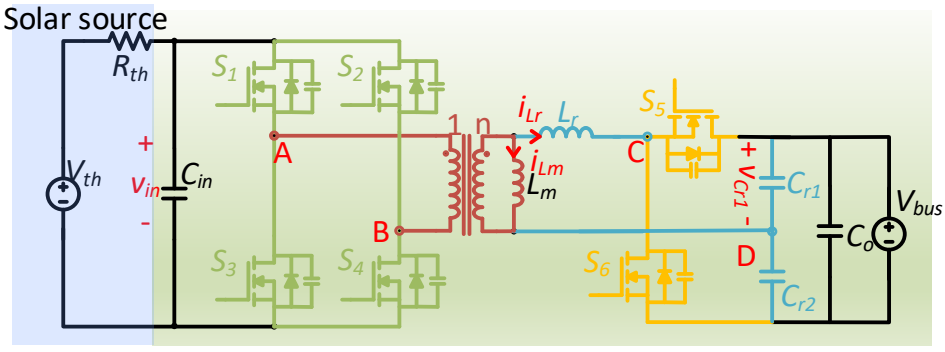


Figure 4.2. Topology of the proposed converter.

Unlike the conventional variable-frequency operation of the *LLC* resonant converter, the proposed converter operates at a fixed switching frequency which equals to the series resonant frequency. Hence, the design of L_m only needs to consider ZVS of the primary side switches but not necessarily to obtain wide voltage gains. Thus, the ratio of L_m/L_r is much larger than conventional *LLC* converter with variable-frequency control. Therefore, the proposed converter has the advantages of low circulating current, low current switching of the primary side switches, and ZCS of the secondary side switches regardless of input voltage or power compared to the traditional variable-frequency *LLC* resonant converter.

To simplify the steady-state analysis of the proposed converter, the assumptions are made as follows.

1. The output voltage is treated as a constant voltage and the output capacitor C_o is large enough.
2. C_o is much larger than the resonant capacitors $C_{r1,2}$.
3. Parasitic output capacitances of switches, $C_{oss,}$ is treated as a constant capacitor during dead-time period.
4. The reverse conduction mode of GaN device is presented as a diode in the circuit figures, since it behaves as a diode characteristic.

The energy is delivered from the input to output side through a pure sinusoidal current during entire switching cycle under nominal input condition, as shown in Figure 4.3. The angular frequency of resonant tank is defined in equation (4.1) and the impedance of resonant tank is defined in (4.2). The switching frequency, f_s, is selected to be equal to the resonant frequency, f_r, as defined in (4.3).

$$\omega_r = \frac{1}{\sqrt{L_r(C_{r1}+C_{r2})}} \tag{4.1}$$

$$Z_r = \sqrt{\frac{L_r}{C_{r1}+C_{r2}}} \tag{4.2}$$

$$f_s = f_r = \frac{1}{2\pi\sqrt{L_r(C_{r1}+C_{r2})}} \tag{4.3}$$

Under nominal input voltage condition, the voltage boost ratio is entirely determined by the turns ratio of the transformer, given as

$$n = \frac{V_o}{2V_{in\_nom}} \tag{4.4}$$

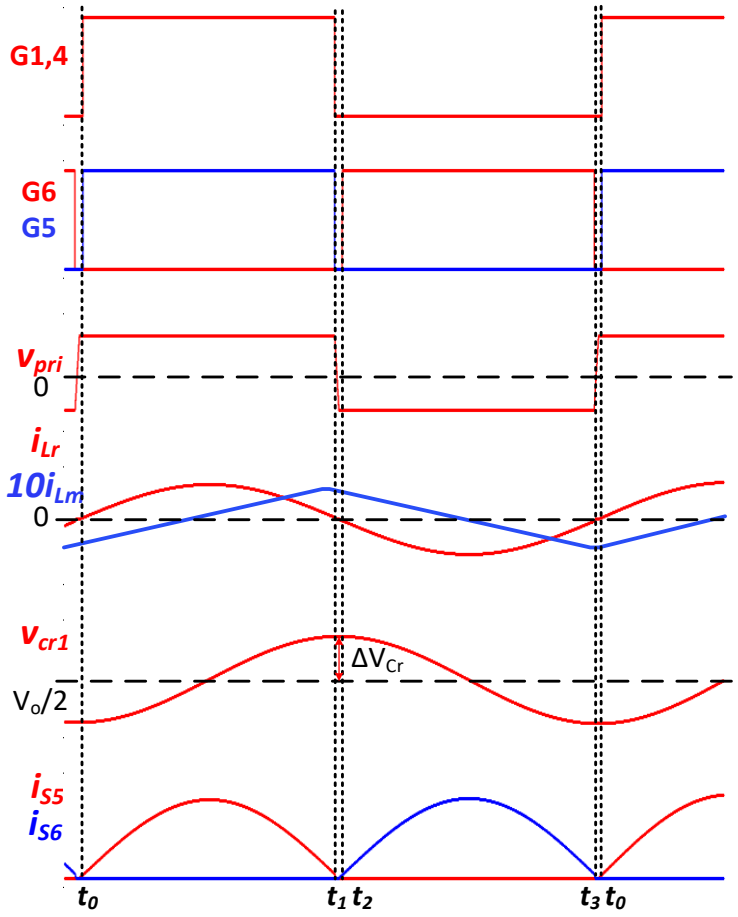


Figure 4.3. Steady-state waveforms under nominal input condition.

The voltage across the transformer winding is pure rectangular since the two legs of primary side full-bridge have 0.5 duty cycle with 180 degree shift. Figure 4.4 shows the trajectory path of resonant tank under nominal input voltage condition, where the average voltage across resonant capacitors is half of output voltage and the average current through resonant inductor is zero. The center of trajectory path is located at ($V_o/2$, 0), and the radius is the half of voltage ripple across resonant capacitors, ΔV_{cr}. The energy is delivered through entire switching cycle.

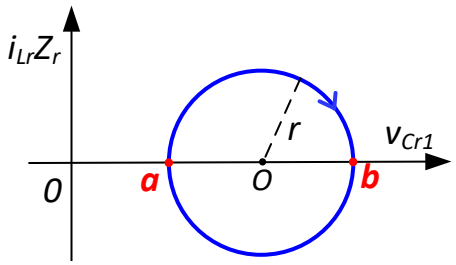


Figure 4.4. State-plane trajectory of resonant tank under nominal input condition.

Both primary and secondary side switches can achieve ZVS turn-on and ZCS turn-off. The magnetizing current during dead-time period reaches its peak value to fully charge and discharge the output capacitance of primary side switches, which make switches achieving ZVS turn-on. The maximum magnetizing current expresses in (4.5). At the end of half switching cycle, the resonant current reaches exactly at zero, thus the secondary side rectifier achieves ZCS turn-off and the switches at primary side turn off under magnetizing current, which is near ZCS turn-off.

$$i_{Lm\_\max} = \frac{nV_{in}T_s}{4L_m} \tag{4.5}$$

Under the high input voltage conditions, such as start-up period, the converter operates as a buck converter so that it can step down the high input voltage to dc bus

voltage. There are two conventional modulation methods to achieve this in pervious literatures: (1) phase-shift control of the primary side full-bridge [69] - [71], (2) variable-frequency control [72], [73]. Since the research and industrial implementations on these methods are mature, the operation under high input voltage conditions will not be emphasized in this dissertation.

4. 2 Converter Operation with Proposed Modulation Scheme

4.2.1 Operation Principle

A double-pulse duty cycle modulation method is proposed to achieve a higher voltage boost ratio than the nominal boost ratio in (4.5) for low input voltage conditions. With the proposed modulation method, the switches in the secondary side can serve not only for the synchronous rectification but also as voltage boost function.

The main steady-state waveforms with double-pulse duty cycle modulation are shown in Figure 4.5. The duty of switch S_5 and S_6 contains two pulses, which are defined as d_b for voltage boost and d_{SR} for synchronous rectification, while the full-bridge of the primary side, $S_{1\text{-}4}$, operates at 0.5 duty with 180 degree phase shift. Under the nominal input condition d_b=0, only d_{SR} is applied to S_5 and S_6, and the converter works as a SRC. When the input voltage drops below nominal voltage d_b>0, S_5 and S_6 serve as an active-boost-rectifier to achieve boost gain. There are 10 operating periods in the whole switching cycle for d_b>0 conditions. The operation of each period is shown in Figure 4.6 and Figure 4.9, from which the first half of the switch cycle and the second half switching cycle are symmetrical. These 10 operating periods in an entire switching cycle will be illustrated in the following paragraphs.

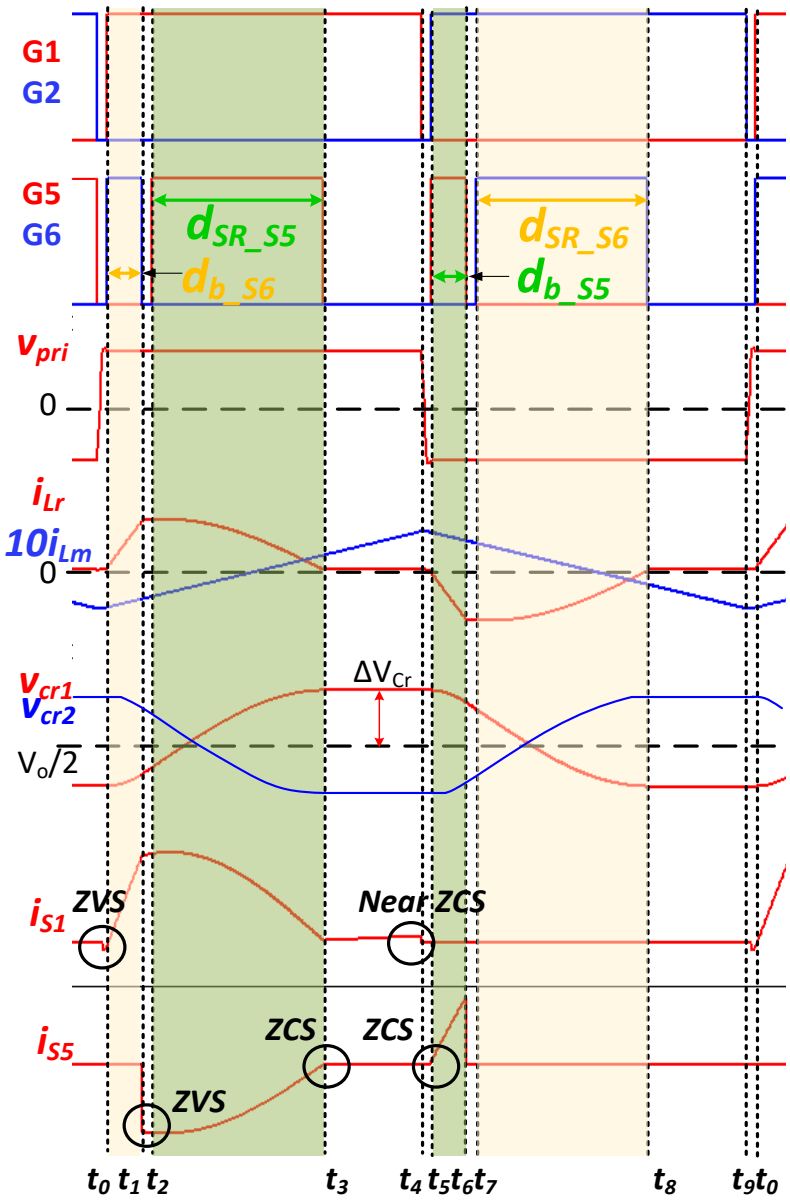


Figure 4.5. Steady-state waveforms under low input condition.

Interval [t_0 - t_1]: t_0 is the beginning of the switching period. At this time, the initial resonant current i_{Lr} is zero and the resonant voltage across C_{r1}, v_{Cr1}, is at minimum value.

$$i_{Lr}(t_0) = 0 \tag{4.6}$$

$$v_{Cr1}(t_0) = \frac{V_o}{2} - \Delta v_{Cr} \tag{4.7}$$

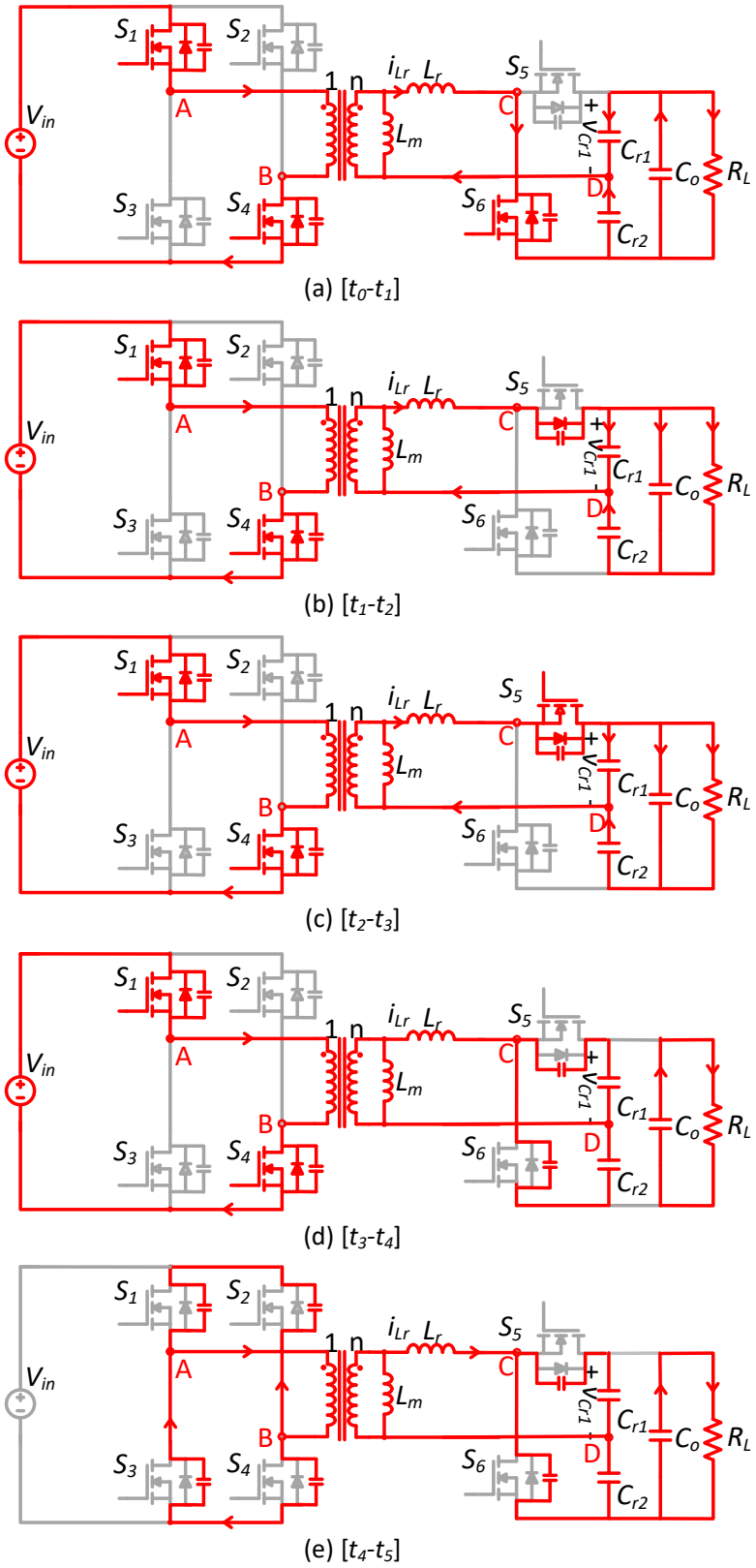


Figure 4.6. Modes of positive switching cycle period.

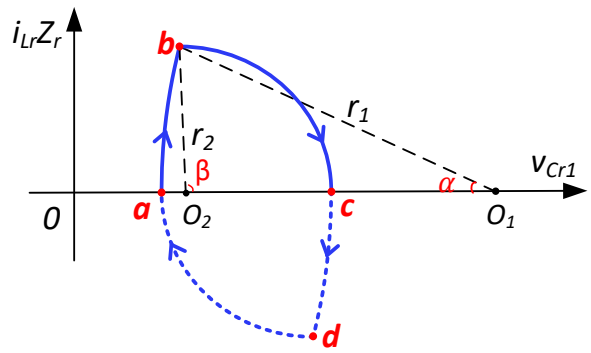


Figure 4.7. State-plane trajectory of resonant tank at positive switching cycle under low input condition.

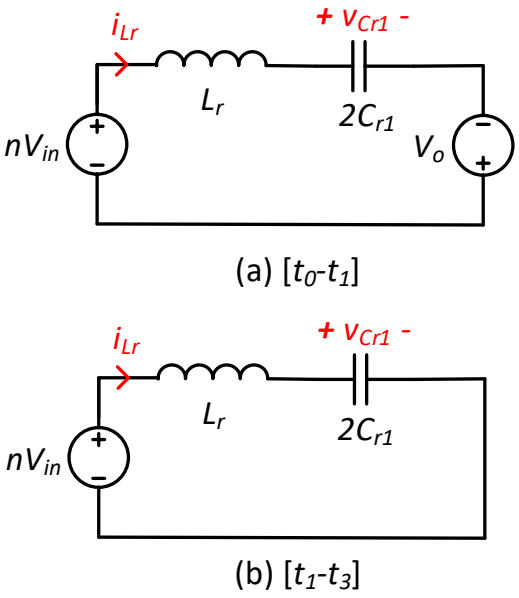


Figure 4.8. Equivalent circuits of [t_0-t_1] and [t_1-t_3] periods.

Where Δv_{Cr} is half of the voltage ripple across the resonant capacitor $C_{r1,2}$.

$$\Delta v_{Cr} = \frac{P_o T_s}{8 n V_{in} C_{r1}} \tag{4.8}$$

During [t_0 - t_1], S_1 and S_4 are on as shown in Figure 4.6 (a), therefore, the positive input voltage is applied to the primary winding of the transformer. For the secondary side, S_6 turns on at a ZCS condition. During this period, a boost duty for S_6, $d_{b\_s6,}$ is applied and a Boost circuit is built. The input voltage source, output capacitor C_o, and resonant

capacitors C_{r1} and C_{r2} provide energy to L_r. The mechanism during the period [t_0-t_1] is similar to a conventional boost converter when main switch is on and the inductor is charged. This period represents point a to point b in the state-plane trajectory path in Figure 4.7, and the equivalent resonant circuit is pictured in Figure 4.8 (a), where input voltage and output capacitor voltage serve as voltage source. L_r and $C_{r1,2}$ make up the series resonant network. In the trajectory path, the center of this period is located at O_1, and the radius is marked as r_1, which can be calculated in (4.9) and (4.10).

$$O_1 = nV_{in} + V_o \tag{4.9}$$

$$r_1 = nV_{in} + \frac{V_o}{2} + \Delta v_{Cr} \tag{4.10}$$

The state variables of i_{Lr} and v_{Cr1} are expressed in the time domain in (4.11) and (4.12), respectively, where Z_r is the impedance of the series resonant network (4.2).

$$i_{Lr}(t) = \frac{r_1}{Z_r}\sin\left(\pi - \omega_r\left(t - t_0\right)\right) \tag{4.11}$$

$$v_{Cr1}(t) = \left(nV_{in} + V_o\right) + r_1\cos\left(\pi - \omega_r\left(t - t_0\right)\right) \tag{4.12}$$

Interval [t_1 - t_2]: This period represents the first dead-time period between S_5 and S_6. The circuit operation is shown in Figure 4.6 (b). At t_1, S_6 turns off and S_5 keeps off. Point b in Figure 4.7 shows the status of the resonant variables at t_1.

$$i_{Lr}(t_1) = \frac{r_1}{Z_r}\sin\left(\pi - \omega_r\left(t_1 - t_0\right)\right) \tag{4.13}$$

$$v_{Cr1}(t_1) = \left(nV_{in} + V_o\right) + r_1\cos\left(\pi - \omega_r\left(t_1 - t_0\right)\right) \tag{4.14}$$

$$\alpha = \sin^{-1}\left(\frac{Z_r i_{Lr}(t_1)}{r_1}\right) \tag{4.15}$$

Since positive voltage is applied across the transformer, the energy is delivered to the load side through the "body diode" of S_5 after the output capacitance of S_5 is fully discharged. Therefore, when S_5 turns on at t_2, ZVS turn-on is achieved.

Interval [t_2 - t_3]: The mode of operation is shown in Figure 4.6 (c). S_5 turns on when the synchronous rectification duty of S_5, d_{SR_S5}, is applied to the gate terminal of S_5, and power continues transferring to the output side through the channel of S_5, instead of "body diode". The equivalent circuit of this interval is shown in Figure 4.8 (b). In the figure of state-plane trajectory path, the center of this period is located at O_2, and the radius is marked as r_2.

$$O_2 = nV_{in} \tag{4.16}$$

$$r_2 = \frac{V_o}{2} - nV_{in} + \Delta v_{Cr} \tag{4.17}$$

The state variables of i_{Lr} and v_{Cr1} in this interval are expressed in the time domain in (4.18) and (4.19), respectively, where β is the initial angle as marked in Figure 4.7. β can be derived from point b in the trajectory path, as expressed in (4.20).

$$i_{Lr}(t) = \frac{r_2}{Z_r}\sin\left(\beta - \omega_r(t - t_1)\right) \tag{4.18}$$

$$v_{Cr1}(t) = (nV_{in}) + r_2\cos\left(\beta - \omega_r(t - t_1)\right) \tag{4.19}$$

$$\beta = \pi - \sin^{-1}\left(\frac{Z_r i_{Lr}(t_1)}{r_2}\right) \tag{4.20}$$

The interval ends when the current sensor senses that the resonant current reaches to zero. At this point, S_5 turns off under ZCS condition.

Interval [t_3 - t_4]: During this period, there is no more energy delivered to the load, as shown in Figure 4.6 (d). The converter runs into the idle state (discontinuous-current-mode DCM period) with the magnetizing current freewheeling and small ringing occurring between L_r and output capacitances of S_5 and S_6. At t_4, S_1 and S_4 turn off under relatively low magnetizing current calculating in (4.21).

$$i_{Lm}(t_4) = \frac{nV_{in}T_s}{4L_m} \tag{4.21}$$

Interval [t_4 - t_5]: As shown in Figure 4.6 (e), the converter enters a dead-time period for the switches on both the primary and secondary side. At this time, there is no gate signal applied to the switches. The magnetizing current appears as a current source to discharge the parasitic output capacitances of $S_{2,3}$ and charge those of $S_{1,4}$. Once the output capacitances are fully charged and discharged, the "body diode" of S_2 and S_3 will be forced to conduct before applying the gate signals. Therefore, the criteria of designing the magnetizing inductance is to guarantee ZVS turn-on for primary side switches.

During t_5 through t_0, the circuit analysis is completely symmetrical to the circuit operating in the period of t_0 to t_5. During [$t_5 - t_0$], S_2 and S_3 are on as shown in Figure 4.9, therefore, the negative voltage is applied to the windings of the transformer.

Interval [$t_5 - t_6$]: As shown in Figure 4.9 (a), this period is when the boost duty of S_5, $d_{b\_s5,}$ is applied for voltage boost. t_5 is the beginning of the negative switching cycle, when i_{Lr} is zero and v_{Cr1} is at its peak value.

$$i_{Lr}(t_5) = 0 \tag{4.22}$$

$$v_{Cr1}(t_5) = \frac{V_o}{2} + \Delta v_{Cr} \tag{4.23}$$

After t_5, S_5 turns on at zero current condition and a Boost circuit is built for voltage boost function. Similarly as positive half cycle, the input voltage source, output capacitor C_o, and resonant capacitors C_{r1} and C_{r2} provide energy to charge L_r. Figure 4.10 shows the state-plane trajectory of resonant tank during negative switching cycle. The period of [t_5-t_6] represents point c to point d in the trajectory path. And the equivalent resonant circuit is pictured in Figure 4.11(a), where input voltage and output capacitor voltage serve as voltage source to charge L_r. In the trajectory path in Figure 4.10, the center of this period is located at O_3, and the radius is marked as r_3, which is same as r_1.

$$O_3 = -nV_{in} \tag{4.24}$$

$$r_3 = nV_{in} + \frac{V_o}{2} + \Delta v_{Cr} \tag{4.25}$$

The state variables of i_{Lr} and v_{Cr1} are expressed in the time domain in (4.26) and (4.27), respectively.

$$i_{Lr}(t) = -\frac{r_3}{Z_r}\sin\left(\pi - \omega_r(t - t_5)\right) \tag{4.26}$$

$$v_{Cr1}(t) = -nV_{in} - r_3\cos\left(\pi - \omega_r(t - t_5)\right) \tag{4.27}$$

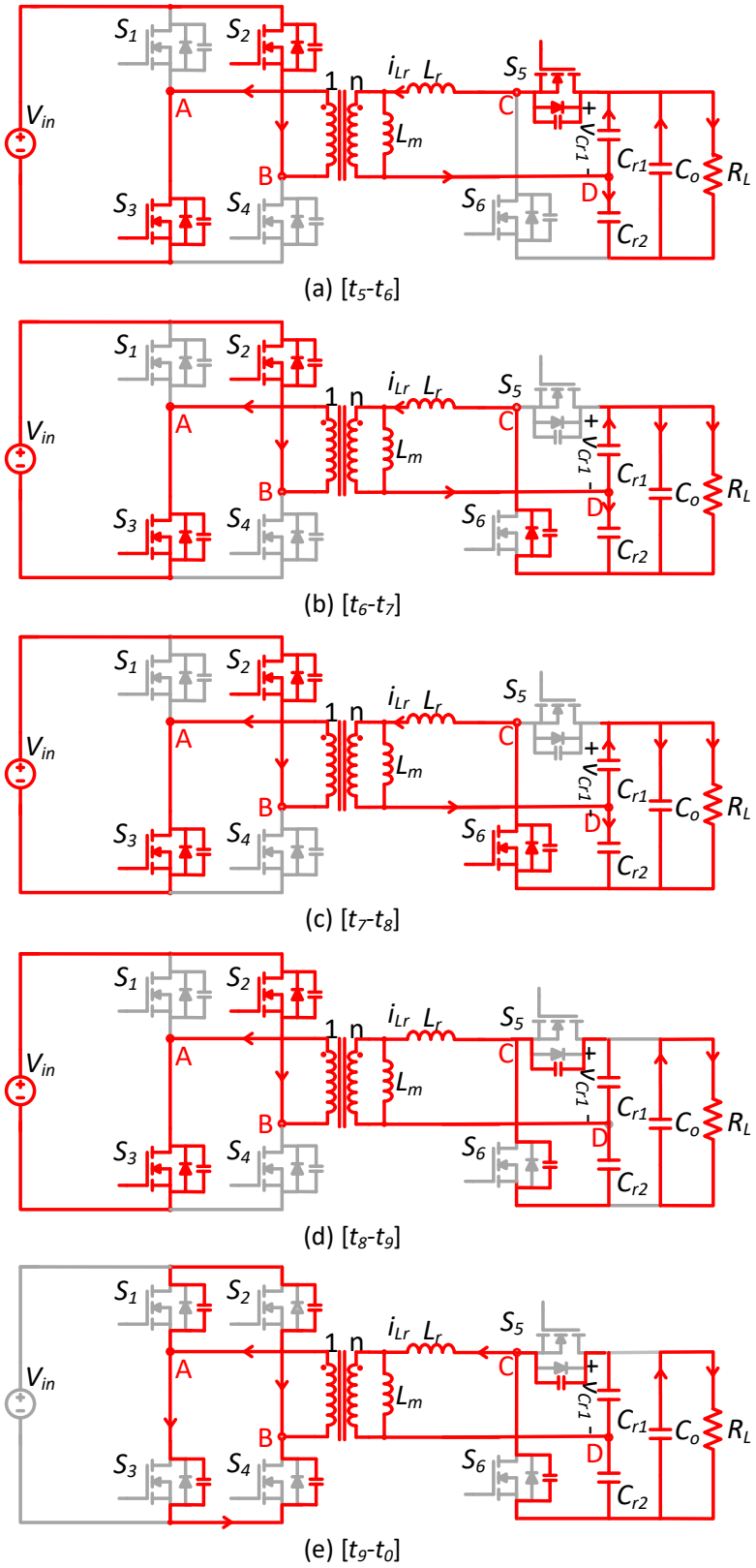


Figure 4.9. Modes of negative switching cycle period.

Interval [$t_6 - t_7$]: It is the second dead-time between S_5 and S_6 as shown in Figure 4.9 (b). Point d in Figure 4.10 represents the status of the resonant variables at t_6, as expressed in (4.28) and (4.29).

$$i_{Lr}(t_6) = -\frac{r_3}{Z_r}\sin\left(\pi - \omega_r\left(t_6 - t_5\right)\right) \tag{4.28}$$

$$v_{Cr1}(t_6) = -nV_{in} - r_3\cos\left(\pi - \omega_r\left(t_6 - t_5\right)\right) \tag{4.29}$$

The current through S_6 is from drain terminal to source terminal during this dead-time period, i_{Lr} will discharge the output capacitance of S_6 at t_6. After t_6, the "body diode" of S_6 conducts, therefore, S_6 achieves ZVS turn-on at t_7.

Interval [t_7 - t_8]: During this interval, the synchronous rectification duty of S_6, d_{SR_S6}, is applied to the gate of the switch. The power transfers to the load through S_6, instead of "body diode". The mode of operation is shown in Figure 4.9 (c) and the equivalent circuit of this interval is in Figure 4.11 (b). In the figure of state-plane trajectory, the center of this period is located at O_4, and the radius is marked as r_4, as shown in Figure 4.10.

$$O_4 = V_o - nV_{in} \tag{4.30}$$

$$r_4 = \frac{V_o}{2} - nV_{in} + \Delta v_{Cr} \tag{4.31}$$

The state variables of i_{Lr} and v_{Cr1} in this interval are expressed in the time domain in (4.32) and (4.33), respectively, where β is the initial angle as marked in Figure 4.10. The initial angle β is exactly same as the initial angle in the positive switching cycle, which is expressed in (4.20).

$$i_{Lr}(t) = \frac{r_4}{Z_r}\sin\left(\beta - \omega_r\left(t - t_6\right)\right) \tag{4.32}$$

$$v_{Cr1}(t) = \left(nV_{in}\right) + r_4\cos\left(\beta - \omega_r\left(t - t_6\right)\right) \tag{4.33}$$

Identically as the positive switching cycle, this interval ends when the current sensor senses that the resonant current reaches to zero. S_5 turns off with ZCS at the end of this period.

Interval [t_8 – t_9]: The mode of operation is shown in Figure 4.9 (d), when the converter operates at idle state with no more energy delivering. The magnetizing current reaches the negative peak value (4.34). At t_4, S_1 and S_4 turn off under magnetizing current condition.

$$i_{Lm}(t_9) = -\frac{nV_{in}T_s}{4L_m} \tag{4.34}$$

Interval [t_9 – t_0]: This period is another dead-time period for switches on both primary and secondary side, as shown in Figure 4.9 (e). The magnetizing current behaves as a current source to discharge the parasitic output capacitances of $S_{1,4}$ and charge those of $S_{2,3}$. Once the output capacitances are fully charged and discharged, the "body diode" of S_1 and S_4 will be forced to conduct before applying the gate signals. Therefore, S_1 and S_4 achieve ZVS turn-on.

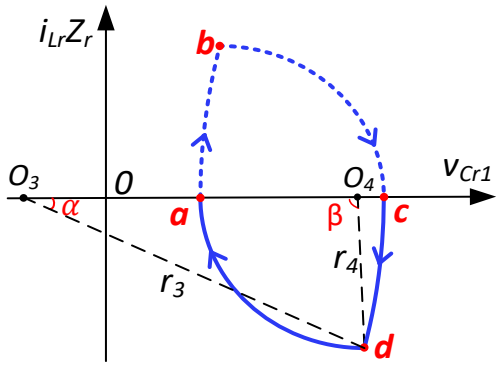


Figure 4.10. State-plane trajectory of resonant tank at negative switching cycle under low input condition.

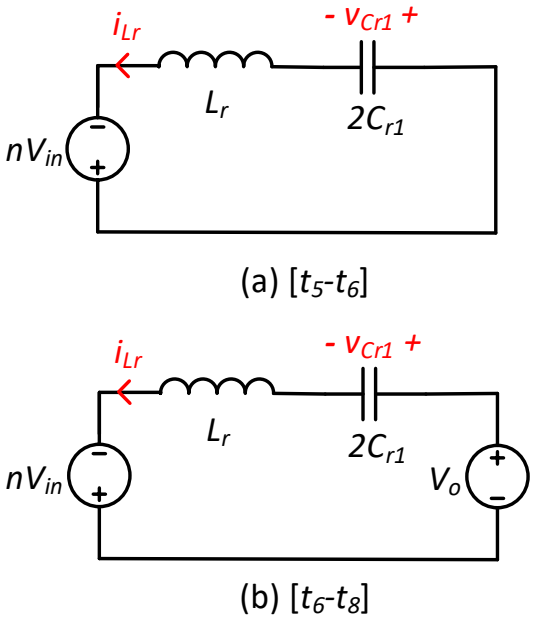


Figure 4.11. Equivalent circuits of [t_5-t_6] and [t_6-t_8] periods.

4.2.2 Voltage Conversion Ratio

In the proposed modulation method for low input voltage conditions, the gate signal of S_5 and S_6 is composed of d_{SR} and d_b as marked in Figure 4.5. d_{SR} is responsible for the synchronous rectification, which replaces the diode in order to minimize conduction loss. d_{SR} has no effect on the voltage gain. With double-pulse duty cycle modulation, the output voltage is regulated only by controlling d_b. In this section, the relationship between d_b,

voltage conversion ratio, and converter parameters is derived for further components design.

The trajectory path is necessary for derivation of the voltage conversion ratio. Since the positive and negative half cycle are entirely symmetrical, the derivation of voltage gain characteristics can be completed only through the analysis of positive switching cycle. Point b represents the intersection of arc ab and arc bc in Figure 4.12. Therefore, the geometric relationship of the state variables at point b can be expressed as (4.35) and (4.36) , respectively.

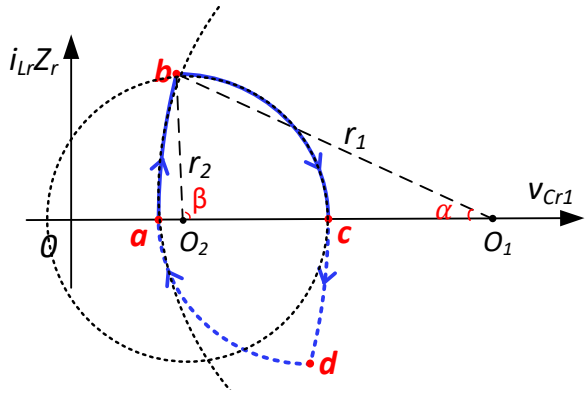


Figure 4.12. State-plane trajectory of resonant tank for derivation of the voltage conversion ratio.

$$\left(v_{Cr1}\left(t_1\right)-nV_{in}-V_o\right)^2+\left(Z_r i_{Lr}\left(t_1\right)\right)^2=r_1^2 \tag{4.35}$$

$$\left(v_{Cr1}\left(t_1\right)-nV_{in}\right)^2+\left(Z_r i_{Lr}\left(t_1\right)\right)^2=r_2^2 \tag{4.36}$$

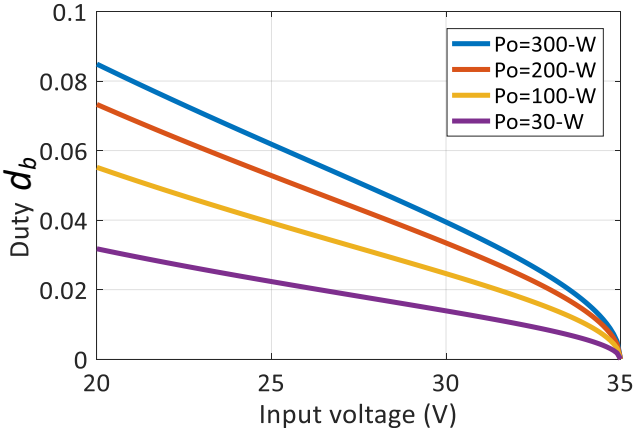
From (4.35) and (4.36), the state variable v_{Cr1} at t_1 can be derived in (4.37), where $t_1=d_bT_s$.

$$v_{Cr}\left(t_1\right)=nV_{in}+\frac{V_o}{2}-\frac{nV_{in}\left(V_o+\Delta V_{Cr}\right)}{V_o} \tag{4.37}$$

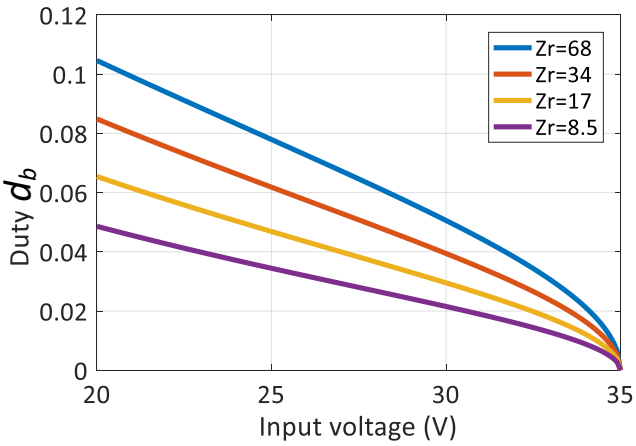
Combined with equations (4.8), (4.10), (4.14) and (4.37), the relationship between duty cycle and voltage conversion ratio can be derived as (4.38).

$$d_b = \frac{\cos^{-1}\left(\dfrac{\dfrac{V_o}{2}+nV_{in}+\dfrac{P_oT_s}{4C_{r1}}}{\dfrac{V_o}{2}+nV_{in}+\dfrac{P_oT_s}{8nV_{in}C_{r1}}}\right)}{\omega_r T_s} \tag{4.38}$$

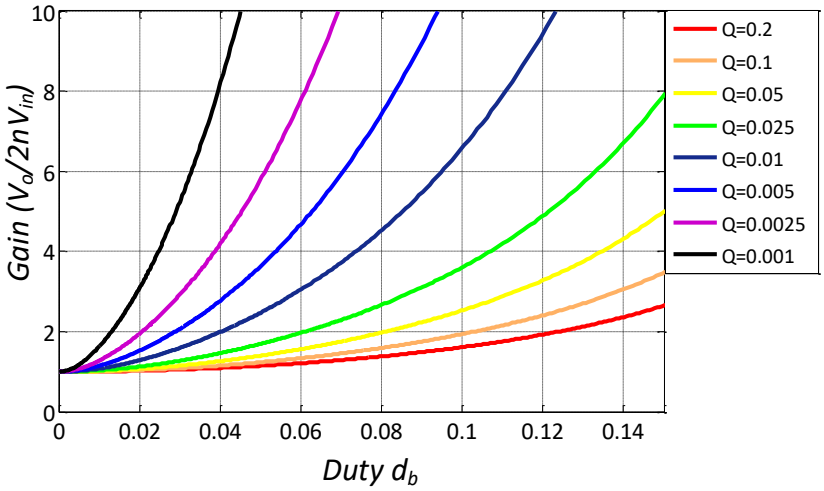
According to (4.38), the relationship between duty cycle and voltage conversion ratio is not only determined by the output power, but also determined by the parameters of resonant tank. Figure 4.13 (a) and (b) show the curves of duty cycle versus the input voltage under different power levels and resonant tanks, where V_o sets as 380-V and V_{in_nom} designs at 35-V. In Figure 4.13 (a), the output impedance is fixed at 34 for all cases, and the output power is fixed as 300-W for all cases in Figure 4.13 (b). Additionally, universal voltage gain curves versus d_b with various qualify factors (Q) are plotted in Figure 4.13 (c), which are not only limited to the application of this dissertation work.



(a) With different output power levels (Z_r=34).



(b) With different resonant tank impedances (P_o=300-W).



(c) Voltage gain characteristics.

Figure 4.13. Voltage conversion ratio curves: The relationship between input voltage and d_b for 380-V fixed output voltage in (a) and (b); The relationship between voltage conversion gain and d_b in (c).

4. 3 Hardware Design Procedure

The converter design process will optimize the converter at the nominal input condition to achieve the highest efficiency, meanwhile, the circuit with designed power stage parameters should operate to meet the gain requirement of entire operating range.

Hardware design includes the transformer design and optimization, resonant tank design, dead-time optimization and power device selection.

4.3.1 Transformer Design

The transformer is designed and optimized at the most efficient point when the converter operates as a pure SRC and d_b is zero under nominal input voltage. The turns ratio is selected in (4.4), which is determined by the nominal input voltage and output voltage.

As mentioned in the Section 4.2, the magnetizing inductance, L_m, is designed to ensure ZVS turn-on of primary side switches with proper length of dead-time [74], [75]. The magnetizing current acts as a current source to provide energy to fully charge and discharge output capacitances of primary side devices during dead-time period. Figure 4.14 shows the equivalent circuit during dead-time period between $S_{1,4}$ turn-off and $S_{2,3}$ turn-on. C_{oss1} and C_{oss4} are in series to equivalent to a capacitor that is half of C_{oss}, and C_{oss2} and C_{oss3} are in series to comprise a capacitor which is half of C_{oss}. Then these two half C_{oss} are in parallel. So the total equivalent capacitance is equal to the parasitic output capacitance of the single switch, and the alternating voltage across this equivalent capacitance is twice of V_{in}.

According to the equation of capacitor charge balance, the minimum magnetizing current should meet the requirement of (4.39), where t_d is the length of dead-time and C_{oss1} is the parasitic output capacitance of S_1.

$$I_{Lm\_pri} > C_{oss1}\frac{2V_{in}}{t_d} \tag{4.39}$$

The magnetizing current reflected to the primary side during dead-time can be derived as (4.40).

$$I_{Lm\_pri} = \frac{n^2 V_{in}}{4 L_m f_s} \tag{4.40}$$

Therefore, L_m should meet the requirement of (4.41) by the combination of (4.39) and (4.40).

$$L_m \le \frac{n^2 t_d}{8 f_s C_{oss1}} \tag{4.41}$$

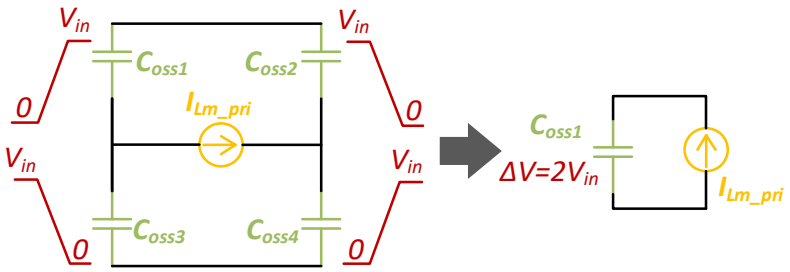


Figure 4.14. Equivalent circuit during dead-time period between $S_{1,4}$ turn-off and $S_{2,3}$ turn-on.

The design of magnetizing inductance is to guarantee the ZVS of primary side switches. However, it represents the circulating current in the circuit, which cannot be delivered to the load and cause additional loss. The lower magnetizing inductance will result in higher circulating current which will hurt the efficiency especially under the light load conditions. Therefore, the magnetizing inductance should be designed exactly for ZVS operation, which can be tuned through adjusting the thickness of transformer gap.

After the selection of turns ratio, the selection of core shape, core size, and material will be the next step for the transformer design. There are quite a few articles and books discussing the optimization of these procedures [76] - [78]. Magnetic material 3C95 from

Ferroxcube or material N95 from Epcos is selected for 100-kHz range operation, since the core loss of these materials are optimized at hundred-kHz range and they also have characteristic of flat curves of power loss versus temperature [79], [80]. The curves of power loss versus temperature of material 3C95 is shown in Figure 4.15. It is important because the converter will be installed together with PV modules on the rooftop of buildings, where the ambient temperature will vary greatly depending on geographical locations, weather, and seasons. Core shape RM14/ILP is selected because of its relatively large window area and low profile compared with other shapes [81].

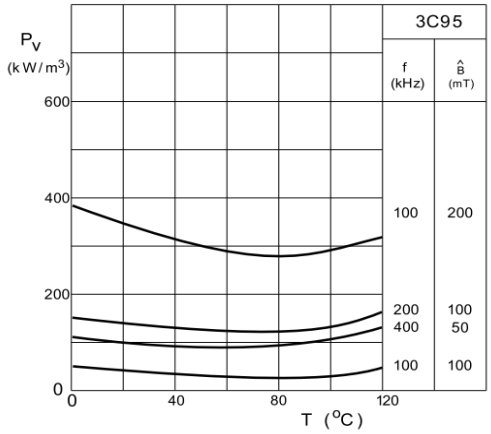


Figure 4.15. Specific power loss for several frequency/flux density combinations as a function of temperature of Ferroxcube 3C95 [79].

The number of turns is determined by the trade-off between core loss and winding loss. The core loss is highly determined by the peak ac flux density, ΔB, which can be derived from total flux, ϕ , and the cross-sectional area of the magnetics core, A_c, (4.42).

$$\Delta B = \frac{\phi}{A_c} \tag{4.42}$$

The formula in (4.43) shows the voltage generation based on the Faraday's law, where V equals to V_{in}, and n is n_1 representing the number of primary side turns, and Δt is a quarter of the switching cycle period in the proposed converter. With the combination of (4.42) and (4.43), ΔB can be calculated in (4.44) where the unit for ΔB is Tesla (T), and A_c is in m^2.

$$V = n\frac{\Delta\phi}{\Delta t} \tag{4.43}$$

$$\Delta B = \frac{V_{in}}{4n_1 f_s A_c} \tag{4.44}$$

The basic requirement for ΔB is to ensure that the magnetic core will be not saturated under the case of maximum flux density. Furthermore, ΔB is one of main factors in the core loss calculation. There are two conventional methods to estimate the core loss, Steinmetz equation and Hysteresis model [82], [83]. As for the Hysteresis model, it requires an intermediate step of calculating B-H loop. Steinmetz parameters are given in most datasheets, which is utilized in this dissertation work. According to Steinmetz equation, an approximation of the core loss density for any combination of operating temperature (T) in [ºC], frequency (f) in [Hz] and flux density (B) in [T] can be obtained from the empirical fit formula in (4.45). C_m, x and y are coefficients that can be acquired from the curve-fittings in Ferroxcube 3C95 datasheet. The core loss can be estimated by the core loss density and core volume in (4.46), where V_e is the effective volume of magnetic core with the unit of m^3 and the unit of P_{core} is W.

$$P_v = C_m f_s^x \Delta B^y \tag{4.45}$$

$$P_{core} = \frac{P_v V_e}{1000} \tag{4.46}$$

In an effort to calculate the winding loss, the rms currents of primary and secondary winding are required. According to the steady-state analysis in Section 4.2, the rms current of secondary winding can be calculated in (4.47). Magnetizing current is too small that can be neglected compared with resonant current. The rms current of primary winding can be derived by the transformer turns ratio, which is expressed in (4.48). Therefore, the total winding loss equation is shown in (3.6), where R_{pri_DC} and R_{sec_DC} are the DC resistance (DCR) of the windings, A and B are the coefficients of AC resistance for litz-wire [84].

$$i_{\text{sec}\_RMS} = \sqrt{\frac{2}{T}\left(\int_0^{t1} \left(\frac{r_1}{Z_r} \sin\left(\omega_r T_s t\right) \right)^2 dt + \int_{t1}^{t3} \left(\frac{r_2}{Z_r} \sin\left(\beta - \omega_r T_s (t - d_b)\right) \right)^2 dt \right)} \tag{4.47}$$

$$i_{pri\_RMS} = n \cdot i_{\text{sec}\_RMS} \tag{4.48}$$

$$P_{wind} = A \cdot {i_{pri\_RMS}}^2 R_{pri\_DC} + B \cdot {i_{\text{sec}\_RMS}}^2 R_{\text{sec\_DC}} \tag{4.49}$$

With the increasing of number of turns, the core loss decreases rapidly and the winding loss increases. The curves of calculated transformer loss are plotted in Figure 4.16, where P_{core}, P_{cu} and P_{total} represent the core loss, winding loss and total loss on transformer. Based off of the curves in Figure 4.16, 4 turns for primary winding and 25 turns for secondary winding were selected to minimize power loss.

After the determination of winding turns, the air gap can be estimated by (4.50) and tuned marginally in order to obtain the required magnetizing inductance.

$$l_g = \frac{\mu_0 A_c {n_2}^2}{L_m} \tag{4.50}$$

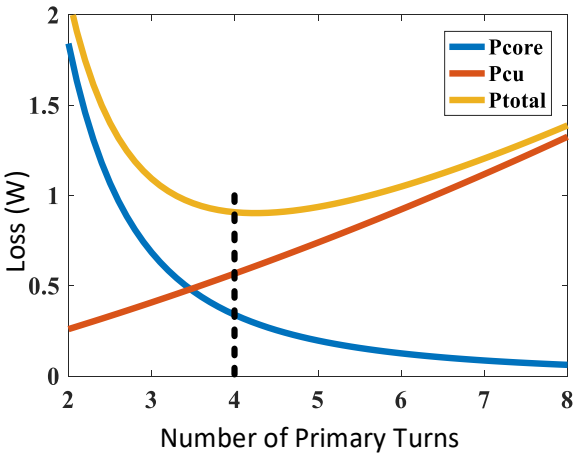


Figure 4.16. Power loss curve of transformer for turns number selection.

Although the proposed converter utilizes leakage inductance for resonant operation, fully interleaved winding structure in order to obtain a tight coupling and minimized leakage inductance can help to improve power converter efficiency [85], [86]. The designed transformer implements interleaved winding structure as shown in Figure 4.17, where the primary winding takes the second layer and the secondary winding takes the first, third and fourth layers. With this structure, the leakage inductance reflecting to the secondary side is minimized as low as 4.65 μH. The designed transformer parameters are summarized in Table 4.2.

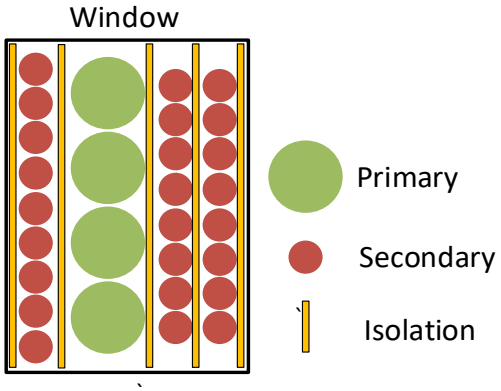


Figure 4.17. Cross-section of transformer window area.

Table 4.2. Transformer design summary.

Description	***Value***
Core shape	RM14/ILP
Core material	N95/3C95
Turns ratio, n	4:22
Winding AWG of primary turns, n_1	1050/44 (14 AWG)
Winding AWG of secondary turns, n_2	330/46 (21 AWG)
Thickness of air gap	3 mil
Magnetizing inductance, L_m	660 µH
Leakage inductance, L_{lk}	4.65 µH

4.3.2 Resonant Tank Design

Basically, the impedance of resonant tank is limited by the length of period [t_0-t_3] in Figure 4.5. The period [t_0-t_3] should be less than $T_s/2$ to guarantee DCM operation of the converter. Equation (4.51) constrains the inductance selection of L_r.

$$T_s / 2 \geq d_b T_s + \frac{(\pi - \sin^{-1}(r_1 \sin(d_b \omega_r T_s)))}{\omega_r} \tag{4.51}$$

Besides the basic constraints of (4.51), the resonant tank design is based on system efficiency optimization at nominal and near-nominal conditions. As shown in Figure 4.13, a larger resonant impedance results in wider duty, lower turn-off current of $S_{5,6}$ and lower rms current. To further demonstrate this relationship, simulations are conducted with different resonant tanks. Resonant inductors are selected as 10 µH, 20 µH and 40 µH, and the criteria selection of resonant capacitor is to keep the resonant frequency at 100 kHz. Figure 4.18 shows the simulated inductor current waveforms under three sets of parameters. With 40 µH inductor, it yields widest duty both for boost and synchronous rectification and lowest rms current and turn-off current of secondary side switches. However, this can

reversely result in a large external inductor and thus higher power loss as well. Practically, the design of the resonant tank considers the trade-off between the turn-off loss of $S_{5,6}$, converter conduction loss, and loss on the external inductor.

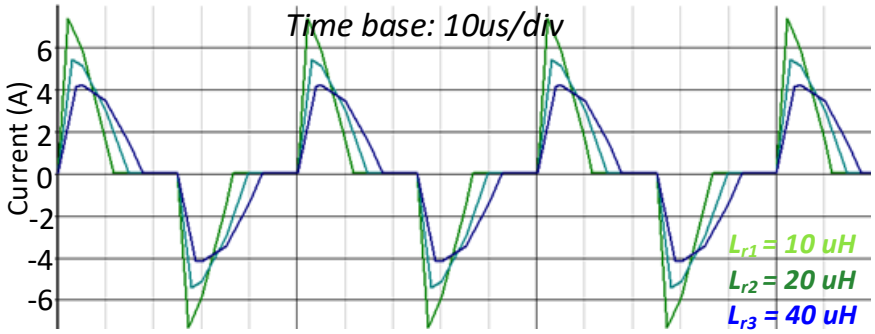
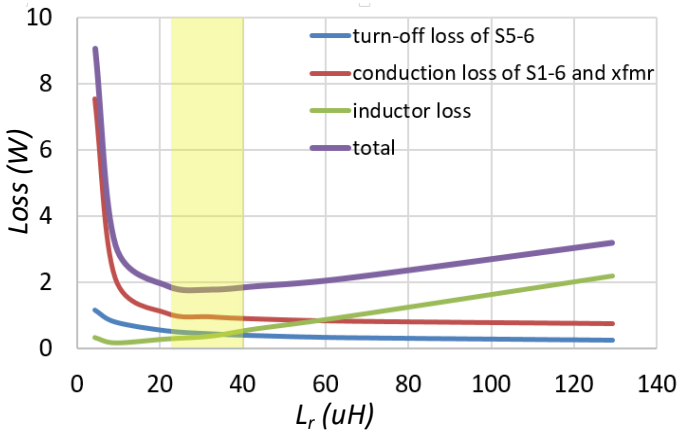


Figure 4.18. Resonant inductor currents with different resonant tank impedances under low input condition.

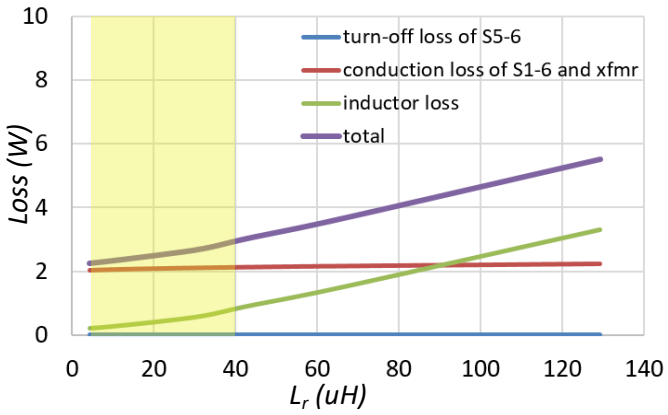
According to the steady-state analysis, the turn-off current of $S_{5,6}$ and the rms current of i_{Lr} are derived in (4.52) and (4.53), respectively.

$$i_{s56\_off} = i_{Lr}(t_1) = \frac{r_1}{Z_r}\sin(\omega_r d_b T_s) \tag{4.52}$$

$$i_{Lr\_RMS} = \sqrt{\frac{2}{T}\left(\int_0^{t1}\left(\frac{r_1}{Z_r}\sin(\omega_r T_s t)\right)^2 dt + \int_{t1}^{t3}\left(\frac{r_2}{Z_r}\sin(\beta - \omega_r T_s (t - d_b))\right)^2 dt\right)} \tag{4.53}$$



(a) Under 32-V input, 150-W conditions.



(b) Under 35-V input, 300-W conditions.

Figure 4.19. Relationship between L_r and converter loss estimation.

Figure 4.19 shows the curves of resonant inductance versus loss, including turn-off loss of $S_{5,6}$, conduction loss of secondary side switches and transformer, and external inductor loss, under 32-V/150-W and 35-V/300-W conditions. The operating conditions are selected based on the PV output characteristic curves under full and half irradiant strength conditions.

According to Figure 4.19, 20 - 40 µH is a proper range for resonant inductance. Once the value for the resonant indutance is decided, the inductance of external inductor is the difference between the total resonant inductance and the transformer leakage inductance. In this work, the external inductor is desiged as 33 µH. The design of external inductor is similar as the design of transformer which is based on the efficiency optimization. According to the projected curves of core loss (P_{core}) and winding loss (P_{cu}) in Figure 4.20, the number of turns is selected as 10 turns to ensure the minimized total inductor loss. Table 4.3 summarizes the designed parameters of the external resonant inductor in this work.

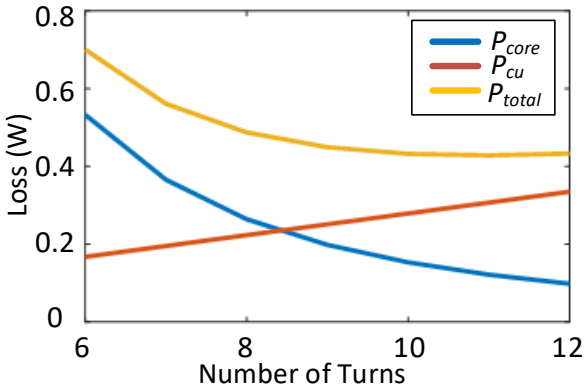


Figure 4.20. Power loss curves of external inductor for turns number selection.

Table 4.3. Design summary of external inductor.

Description	***Value***
Core shape	RM8/ILP
Core material	N95/3C95
Number of turns	10
Winding AWG	330/46 (21 AWG)
Thickness of air gap	5 mil
Inductance	33 μH

The two resonant capacitors can be chosen according to (4.54). When selecting the material of resonant capacitor, there are some tips should be followed. (1) The voltage across the capacitor is high voltage which requires the capacitor with high blocking voltage. (2) The capacitor material should have a low temperature coefficient. (3) The capacitor should have low ESR so that the power dissipation is minimized. In conclusion of requirements above, the 600-V NP0/C0G ceramic capacitor is a desired choice.

$$C_{r1} = C_{r2} = \frac{1}{2 \cdot (2\pi f)^2 L_r} \tag{4.54}$$

4.3.3 Dead-time Design

Dead-time design is critical to achieve soft-switching for the proposed modulation technique under low input voltage conditions. On the other hand, it should avoid to have over-designed dead-time length, since it will cause additional loss during dead-time period and decrease the effective time for energy delivering. As shown in Figure 4.21, there are two dead-time periods for the half switching cycle in the proposed modulation scheme. One is the dead-time between S_1 and S_3, referred to as DT_1, and the other is the dead-time between S_5 and S_6, referred to as DT_2.

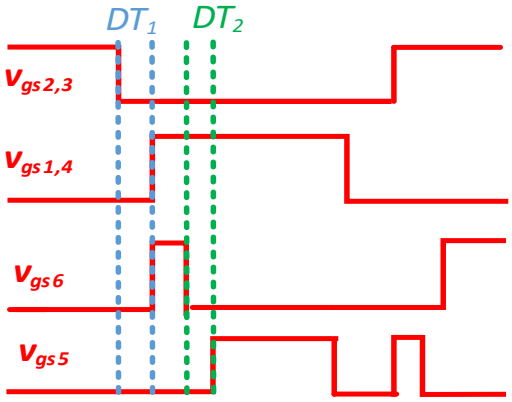


Figure 4.21. PWMs and dead-times during positive switching cycle.

During DT_1, the magnetizing current can be treated as a current source to fully discharge C_{oss} of $S_{1,4}$ and charge C_{oss} of $S_{2,3}$. S_1 and S_4 can then achieve ZVS turn-on when a positive gate signal is applied. Therefore, DT_1 should be designed large enough for this period (4.55).

$$DT_1 \geq \frac{8L_m f_s C_{oss1}}{n^2} \tag{4.55}$$

Unlike $S_{1\text{-}4}$, ZVS turn-on of $S_{5,6}$ is achieved by resonant current. During DT_2, the L_r and C_{oss} of $S_{5,6}$ resonate. When the voltage across C_{oss5} resonates to zero, the "body diode" of S_5 conducts and the voltage is clamped to the "forward voltage" of "body diode". The initial resonant current is the turn-off current of S_6, which is dependent on the operating conditions. The larger the initial current, the shorter time is necessary for C_{oss5} to resonate to 0-V. Therefore, the design of DT_2 is based on the worst case condition when initial current is zero, which means d_b=0 at nominal input voltage condition.

Under nominal input voltage condition, the dead-time period is summation of DT_1 and DT_2, since the turn-off of S_6 is at the same time with the turn-off of $S_{2,3}$ in Figure 4.21. Figure 4.22 and Figure 4.23 show the equivalent circuit and state-plane trajectory path during the dead-time period under nominal input voltage condition. Since nV_{in} is equal to half of output voltage at this condition, the center in the trajectory path is half of output voltage and the radius is also half of the output voltage. Point a in Figure 4.23 represents the initial condition when the resonant current is zero and the voltage across S_5 is equal to output voltage. During entire dead-time period, the voltage across output capacitance of S_5 moves from point a to piont b. Therefore, the DT_2 should be designed to meet the following equation (4.56).

$$\frac{1}{\sqrt{2L_rC_{oss5}}}(DT_1 + DT_2) = \pi \tag{4.56}$$

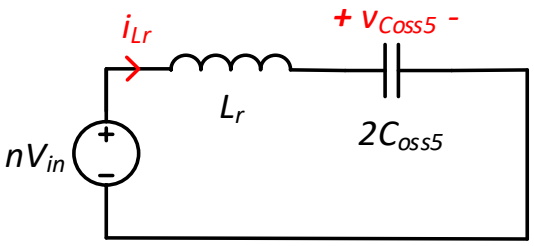


Figure 4.22. Equivalent circuit during the dead-time period DT_2 under nominal input voltage condition.

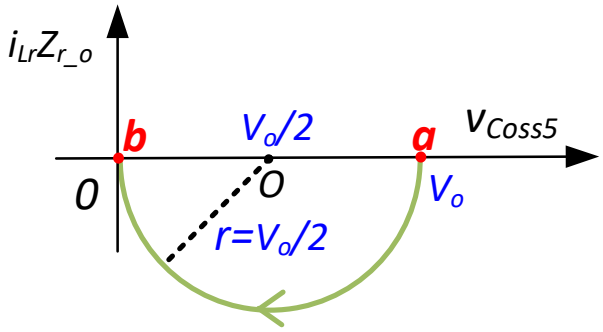


Figure 4.23. State-plane trajectory during the dead-time period DT_2 under nominal input voltage condition.

Table 4.4. Summary of designed dead-time.

Dead-time	***Time***
DT_1	80 ns
DT_2	30 ns

4.3.4 Semiconductor Device Selection

The GaN devices are selected and utilized in this dissertation work. Unlike the Si MOSFETs, the options for GaN devices in the commercial market are limited. However, the principle of GaN device selection is similar to the conventional Si MOSFET, which is based on the voltage and current stresses and the tradeoff between conduction and switching loss [87] - [89].

The voltage stress of the switches in the primary side is the maximum input voltage, which is expressed in (4.57). Considering the open-circuit voltage of single PV model, 80-V device is suitable for the primary side.

$$V_{ds1234\_\max} = V_{in\_\max} \tag{4.57}$$

The conduction loss of the switches in the primary side can be calculated based on the rms current through the device and drain-to-source on-resistance of the device, R_{dson}. The equation is as follows (4.58), where the rms current through the primary side devices is expressed in (4.59).

$$P_{cond\_1234} = (i_{s1234\_RMS})^2 R_{dson} \tag{4.58}$$

$$i_{s1234\_RMS} = n\sqrt{\frac{1}{T}\left(\int_0^{t1}\left(\frac{r_1}{Z_r}\sin\left(\omega_r T_s t\right)\right)^2 dt + \int_{t1}^{t3}\left(\frac{r_2}{Z_r}\sin\left(\beta - \omega_r T_s (t-d_b)\right)\right)^2 dt\right)} \tag{4.59}$$

The primary side switches can achieve ZVS during entire operating region, so there is no turn-on loss on switches $S_{1\text{-}4}$. $S_{1\text{-}4}$ turn off under magnetizing current, which is much lower than resonant current and can be treated as near ZCS turn-off. The turn-off loss of primary side switches is calculated in (4.60), where i_{s1234_off} is equal to the magnetizing current and t_{r1234} is the rise time of switch. Since the switching loss is relatively low under full load or heavy load conditions, the conduction loss dominates the total loss. Theoretically, selection criteria of the primary side device is low R_{dson}. However, the device with lower R_{dson} has higher output capacitance in general, which will require more energy to achieve ZVS and increase the circulating energy. It is a trade-off between R_{dson} and output capacitance.

$$P_{sw\_1234} = \frac{f_s}{2} V_{in} i_{s1234\_off} t_{r1234} \tag{4.60}$$

The gate charging loss is calculated in (4.61), where Q_g is the gate charge of the switch, V_{aux} is the power supply of the gate driver.

$$P_{gate\_1234} = Q_g V_{aux} f_s \tag{4.61}$$

For the secondary side switches S_5 and S_6, the voltage stresses are the output voltage expressing in (4.62). 600-V device is desired in the secondary side due to 380-V standard output voltage bus.

$$V_{ds56\_\max} = V_o \tag{4.62}$$

The conduction loss of secondary side switches is calculated in (4.63), where the rms current is derived in (4.64).

$$P_{cond\_56} = (i_{s56\_RMS})^2 R_{dson} \tag{4.63}$$

$$i_{s56\_RMS} = \sqrt{\frac{1}{T}\left(\int_0^{t1} \left(\frac{r_1}{Z_r} \sin\left(\omega_r T_s t\right) \right)^2 dt + \int_{t1}^{t3} \left(\frac{r_2}{Z_r} \sin\left(\beta - \omega_r T_s (t - d_b)\right) \right)^2 dt \right)} \tag{4.64}$$

As aforementioned in the Section 4.2, the secondary side switches S_5 and S_6 achieve both ZVS turn-on and ZCS turn-off during synchronous rectification. However, it requires to charge the output capacitance at the turn-on with boost duty and has turn-off switching loss at the end of boost duty. The switching loss of $S_{5,6}$ is calculated in (4.65), where t_{r56} is the device rise time and i_{s56_off} is calculated in (4.52).

$$P_{sw\_56} = \frac{f_s}{2}\left(C_{oss} V_o^2 + V_o i_{s56\_off} t_{r56} \right) \tag{4.65}$$

The gate charging loss of $S_{5,6}$ is calculated in (4.66), where V_{aux2} is the power supply of the S_5 and S_6 gate driver.

$$P_{gate56} = Q_g V_{aux2} f_s \tag{4.66}$$

Compared with the GaN devices that have released in the market, the EPC device is used in the primary side and device from GaN Systems is selected for the secondary side, as summarized in Table 4.5.

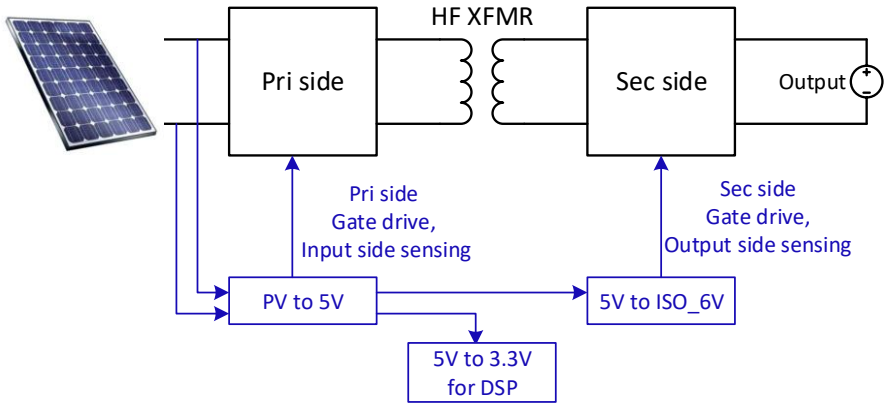
Table 4.5. Summary of selected semiconductor device.

Description	***Part Number***
Primary side switches, $S_{1\text{-}4}$	EPC2021 (80-V, 90-A)
Secondary side switches, $S_{5,6}$	GS66502B (650-V, 7.5-A)

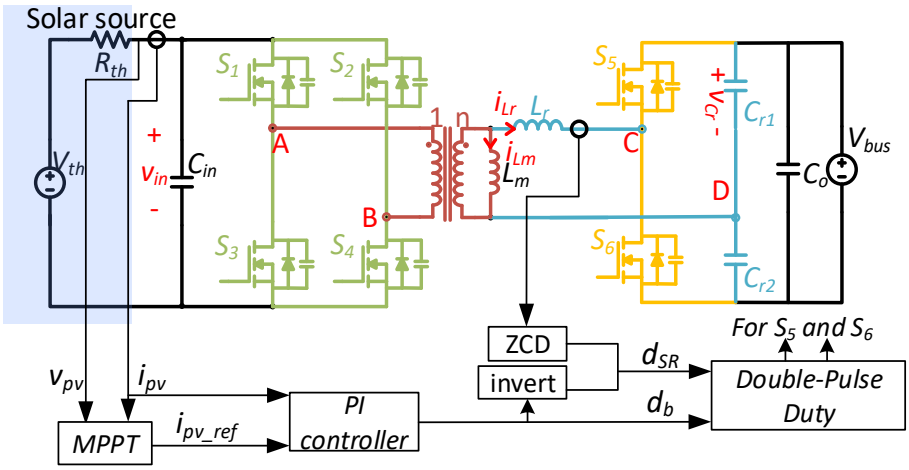
4. 4 Digital Implementation of the Proposed Modulation Scheme

4.4.1 System Control Diagram

Figure 4.25 (a) and (b) show the auxiliary power supply system and system control diagram of the proposed double-pulse duty cycle modulation, respectively. The control focuses on the PWMs of S_5 and S_6. The input voltage and input current of the converter are sensed for MPPT. The MPPT function generates a current reference for the input current control. A proportional-integral (PI) controller is designed to regulate the input current. The output of the current control loop is d_b for S_5 and S_6. d_{SR} is generated from both the inverse of the d_b and the zero current detection (ZCD).



(a) Auxiliary power supply system.



(b) System control diagram.

Figure 4.24. Auxriliary power and control system.

4.4.2 Digital Implementation in Processor

Figure 4.25 shows the details of the implementation of d_{SR} and d_b. Texas Instrument Digital Signal Processor (DSP) 28026 is employed for the digital control implementation because of its small package and low power dissipation. The two analog comparators in the DSP 28026 are used for positive and negative half cycle ZCD. The frequency of carriers of $S_{5,6}$ is double of the carrier of primary side switches.

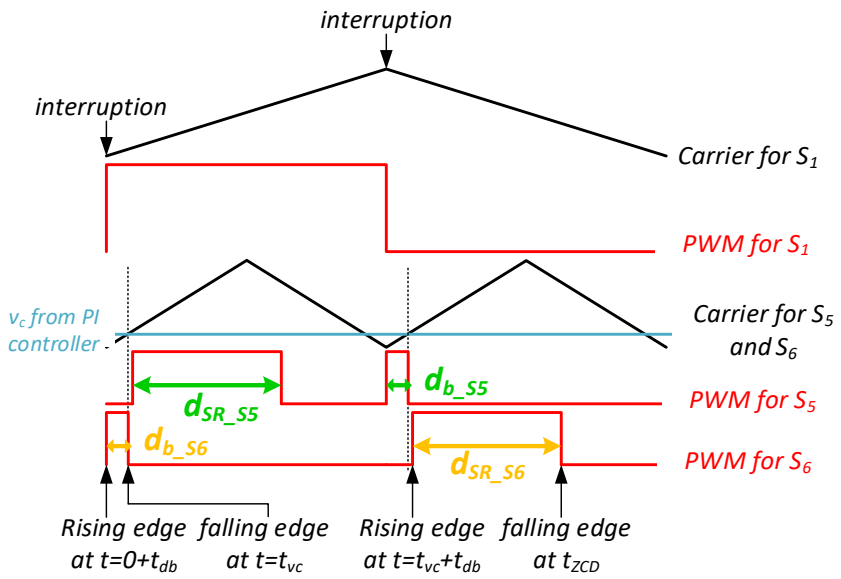


Figure 4.25. Digital implementation of the proposed double-pulse duty cycle modulation.

For each switching cycle of S_1, there are two interrupt events. The first interruption is at the beginning of the switching cycle, and the second is at half of the switching cycle. When the first interruption happens, the PWM of S_6 is set high after dead-time, and then set to low when the carrier wave reaches to the output value of the PI controller. At this period, the PWM setting of S_5 is complementary of S_6. Therefore, the PWM of S_5 is set high after the PWM of S_6 becomes low with dead-time delay. The PWM of S_5 is forced to low when the positive half cycle ZCD circuit senses that the resonant current has reached zero. This is implemented in the DSP with an internal analog comparator and an ePWM trip zone submodule. After the PWM trips to low, it will stay low and is no longer affected by the sensing circuit until the end of half the switching cycle. At the beginning of the other half switching cycle of S_1, the second interruption happens. Now, the output of PI controller is no longer impacting S_6 but S_5. Also, the negative half cycle ZCD will work for the PWM of S_6. The rising edge of the PWM of S_5 is right after the second interruption with dead-

time delay, and the falling edge is controlled by the output of the PI controller. The rising edge of the PWM of S_6 is right after the falling edge of the PWM of S_5 with dead-time delay, and its falling edge is dependent on the ZCD.

4.4.3 Solution of Synchronous Rectification

The circuits to implement the synchronous rectification includes ZCD circuit, analog comparators and DSP ePWM module, as shown in Figure 4.26.

Many ZCD methods targeting on the high frequency for synchronous rectification have been proposed and even implemented maturely in the industry. All of these method can be classified into voltage sensing and current sensing. The voltage sensing methods that have been delivered into chips are usually used for low voltage applications, such as standard 48-V rail, 12-V rail or even lower voltage rails [91], [92]. To revise the voltage sensing method for high voltage applications, more analog circuits need to be added, which not only occupies large space on the PCB but also increases the circuit complexity [93].

Current sensing for ZCD is utilized, which is comprised by current transformer (CT), sensing resistors, low pass filters and clamping diodes. The sensed resonant current and converted voltage has the following relationship (4.67). The two low pass filters, R_1C_1 and R_2C_2, are to filter the current noise, however, it could also cause delay problem and further cause problem of negative current. The parameters design of low pass filter should consider this. The clamping diodes, $D_{1,2}$ are to clamp the sensed voltage to the power supply of DSP under the case that the sensed voltage is higher than power supply of DSP.

$$v_{\text{sense\_iLr}} = \frac{i_{Lr}}{N_{CT}} R_1 \tag{4.67}$$

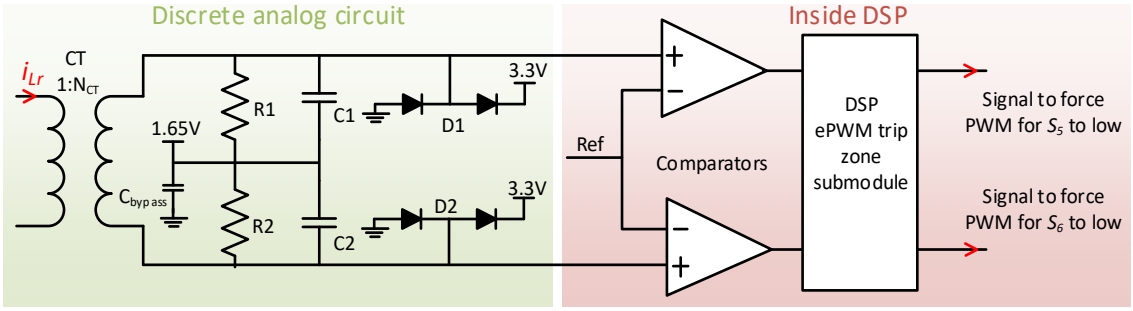


Figure 4.26. Circuit for synchronous rectification.

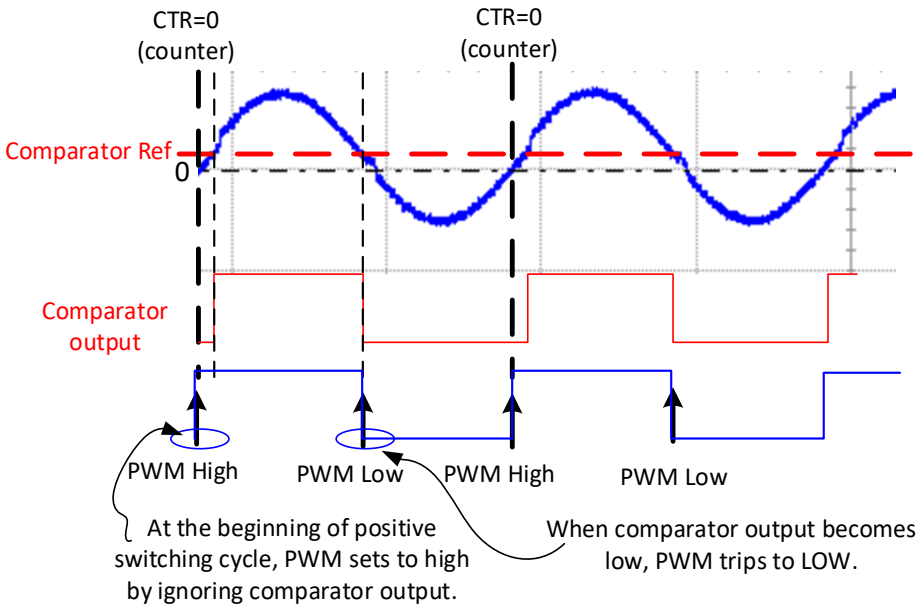


Figure 4.27. The logics of DSP analog comparator and PWMs of positive switching cycle.

The utilization of a pair of comparators integrated inside the DSP gets rid of the necessary of discrete comparators. The sensed voltage is compared with the reference value, and the output of comparator is sent to DSP ePWM module for the trip zone functions. Figure 4.27 shows the logics of DSP analog comparator and PWMs of the positive switching cycle. At the beginning of positive switching cycle, PWM sets to high forcely, although the output of comparator is low. It is achieved by configuration of blanking window. When the resonant current touches to the reference, the comparator

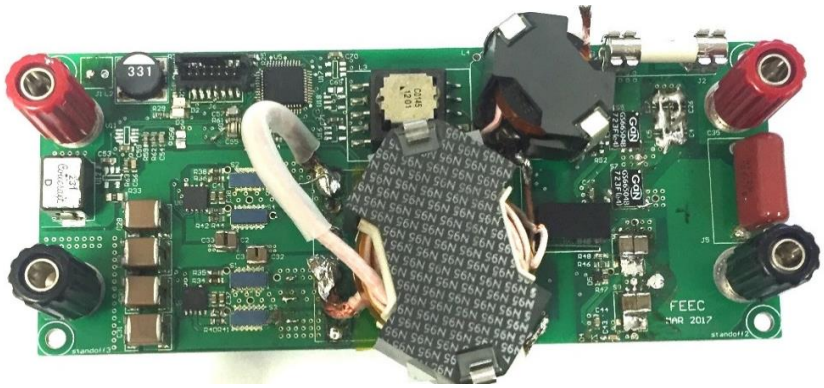
output becomes to low, and then it trips PWM to low. In conclusion, only the falling edge of comparator output is effective for PWM actions.

4. 5 Experimental Verifications

4.5.1 Prototype

A 300-W prototype was built to verify the performance of the proposed converter. Figure 4.28 shows the hardware photograph with case. The case dimension is 5.1” length × 2.4” width × 1.4” height. The nominal input voltage is designed at 35-V and the output voltage is fixed at 380-V. The transformer turns ratio is selected to be 4:22. EPC2021 and GS66502B are selected as the primary and secondary side switches, respectively. The switching frequency and resonant frequency is selected to be 140-kHz for the compliance consideration of electromagnetic interference (EMI) standards which are typically measured from 150 kHz and up. The designed parameters are listed in the Table 4.6.

(a) Case picture.



(b) Board picture.

Figure 4.28. Hardware photograph.

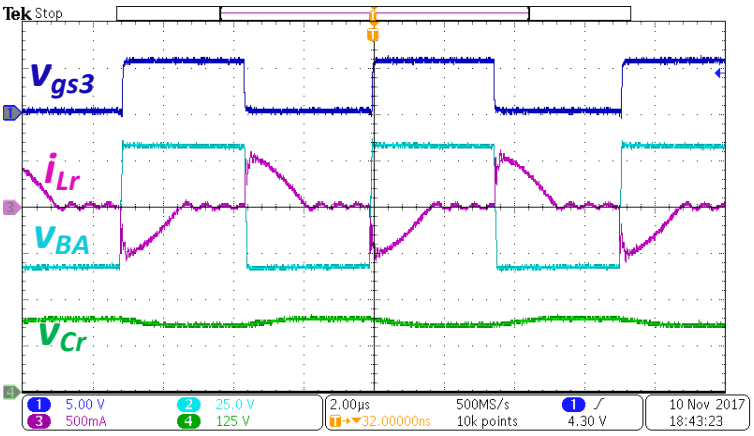
Table 4.6. Prototype design summary.

Description	***Value***
Switching frequency	140-kHz
Resonant inductance, L_r	39.5 µH
Resonant Capacitance, $C_{r1,2}$	16.4 nF (600 V, NP0)
Magnetizing inductance, L_m	660 µH
Transformer turns ratio, n	4:22
Primary side switches, $S_{1\text{-}4}$	EPC2021
Secondary side switches, $S_{5,6}$	GS66502B
Input capacitance, C_{in}	88 µF
Output capacitance, C_o	2.2 µF
Dead-time in primary side legs, DT_1	80 ns
Dead-time in secondary side leg, DT_2	30 ns

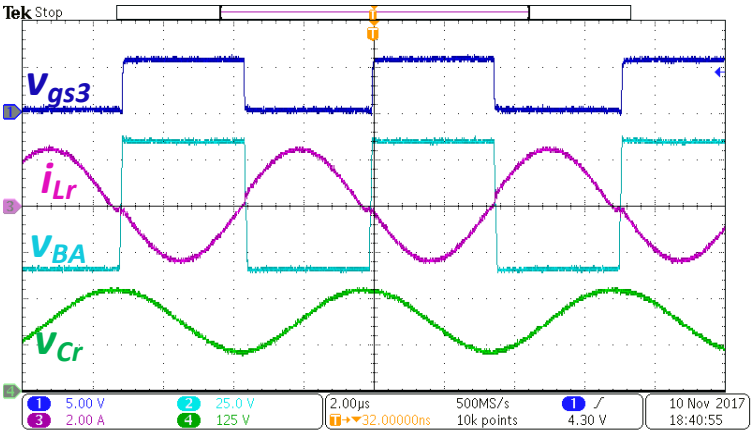
4.5.2 Converter Operation

With nominal input voltage, the converter operates as a pure SRC, as shown in Figure 4.29, where the blue, light blue, purple and green curves are the gate-to-source voltage of S_3, v_{gs3}, resonant current, i_{Lr}, voltage across primary winding of the transformer , v_{BA}, and voltage across resonant capacitor, v_{Cr}, respectively. Because of the 0.5 fixed duty of $S_{1\text{-}4}$, the voltage waveform across the primary winding of the transformer is rectangular.

The dc voltage of resonant capacitor is half of the output voltage, 190-V. Under 30-W condition in Figure 4.29 (a), the peak resonant current is 0.5-A, and the peak resonant voltage is 210-V. Under 300-W condition, the resonant current is purely sinusoidal as shown in Figure 4.29 (b). The peak resonant current is 2.6-A, and the peak resonant voltage is 280-V.



(a) At light load condition (30-W).



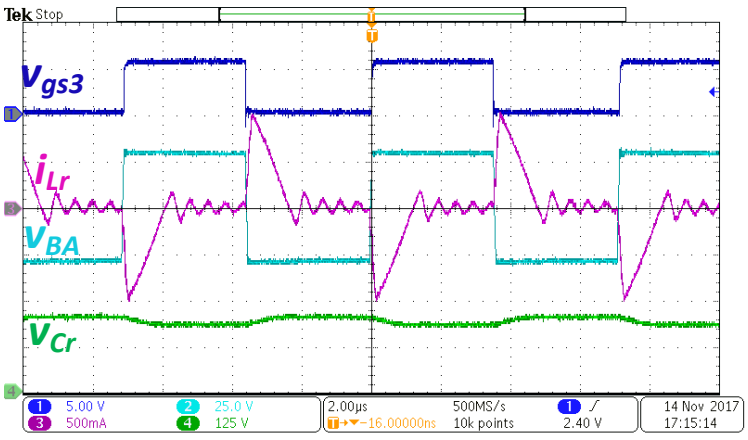
(b) At full load condition (300-W).

Figure 4.29. Experimental steady-state waveforms with nominal input voltage (35-V): gate-to-source voltage of S_3, v_{gs3}, resonant current, i_{Lr}, voltage across primary winding of the transformer , v_{BA}, voltage across resonant capacitor, v_{Cr}.

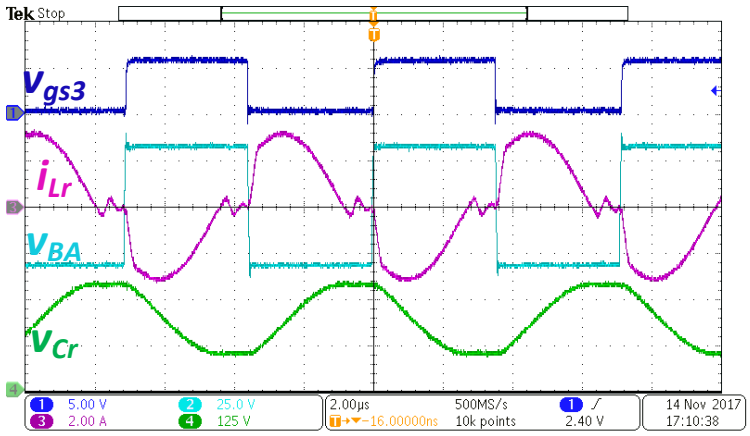
Figure 4.30 shows the experimental waveforms with the proposed double-pulse duty cycle modulation under low input voltage conditions. Similarly as in Figure 4.29, the

blue, light blue, purple and green curves are the gate-to-source voltage of S_3, v_{gs3}, resonant current, i_{Lr}, voltage across primary winding of the transformer , v_{BA}, and voltage across resonant capacitor, v_{Cr}, respectively. With d_b, the resonant current is charged. After that, the resonant current decreases to zero with d_{SR}. Similar to nominal input voltage condition, the voltage waveform across the primary winding of the transformer is rectangular due to a 0.5 duty of the primary side switches. Under 30-W load condition with 32-V input voltage, the d_b is 1.4%, which matches with the voltage conversion ratio analysis. The peak current is 1-A, and the peak resonant voltage is 225-V. The d_b is 3.7% when the input voltage is 32-V and output is 300-W. The resonant peak current is 3.2-A, and the peak resonant voltage is 300-V.

The implementation of double-pulse duty cycle modulation for both S_5 and S_6 is shown in Figure 4.31. At the positive half switching cycle, d_b of S_6 is applied at the beginning of the switching cycle to charge the resonant inductor and d_{SR} of S_5 is applied to deliver the energy to the load until the resonant current reaches to zero. During the DCM period, the gate signals of S_5 and S_6 are both low to keep the switches off. The positive and negative half switching cycles are symmetrical.



(a) At light load condition (30-W).



(b) At full load condition (300-W).

Figure 4.30. Experimental steady-state waveforms with low input voltage (32-V): gate-to-source voltage of S_3, v_{gs3}, resonant current, i_{Lr}, voltage across primary winding of the transformer, v_{BA}, voltage across resonant capacitor, v_{Cr}.

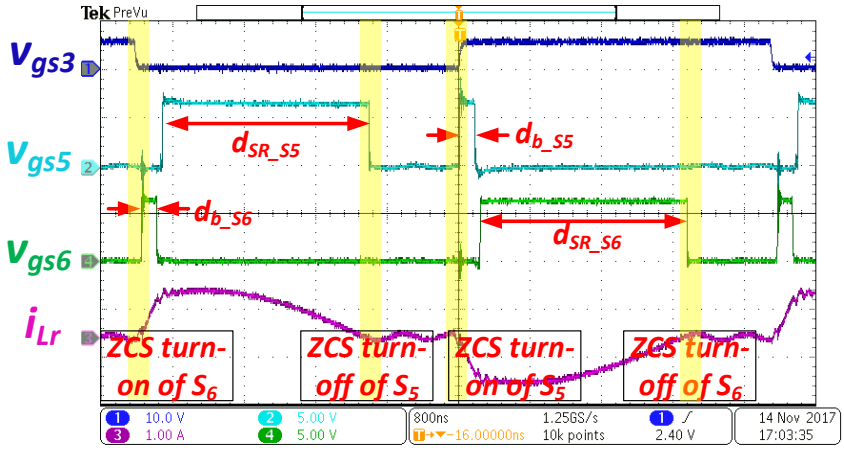
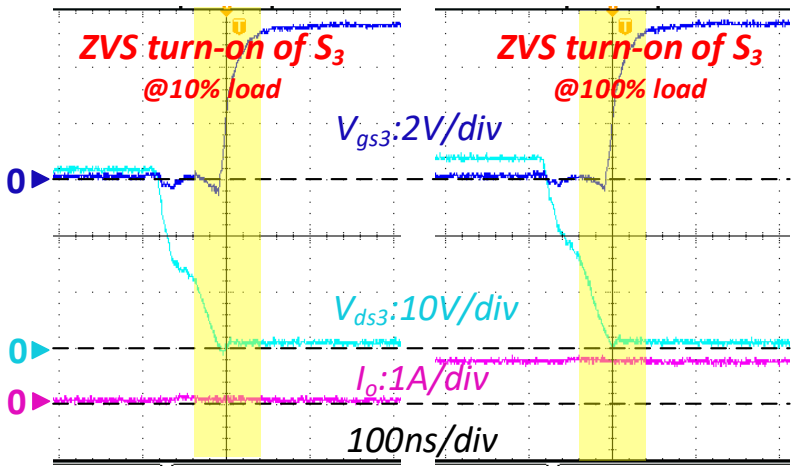
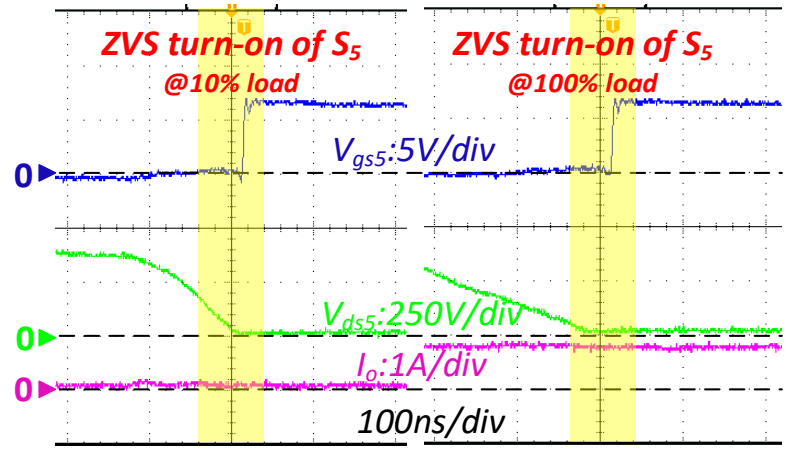


Figure 4.31. Experimental waveforms of double-pulse duty: gate-to-source voltage of S_3, v_{gs3}, gate-to-source voltage of S_5, v_{gs5}, gate-to-source voltage of S_6, v_{gs6}, resonant current, i_{Lr}.

With the proposed converter, all primary side switches can achieve ZVS turn-on and secondary side switches can achieve ZCS turn-off regardless of input voltage or output power. Figure 4.31 shows ZCS turn-on and turn-off waveforms of S_5 and S_6. Figure 4.32 shows ZVS turn-on waveforms of S_3 and S_5. v_{gs3} and v_{gs5} are high after that v_{ds3} and v_{ds5} drops to zero. The turn-on transitions of $S_{1,2,4}$ and S_6 are the same as S_3 and S_5.



(a) Turn-on transition of S_3: gate-to-source voltage of S_3, v_{gs3}, drain-to-source voltage of S_3, v_{ds3}, output current, I_o.



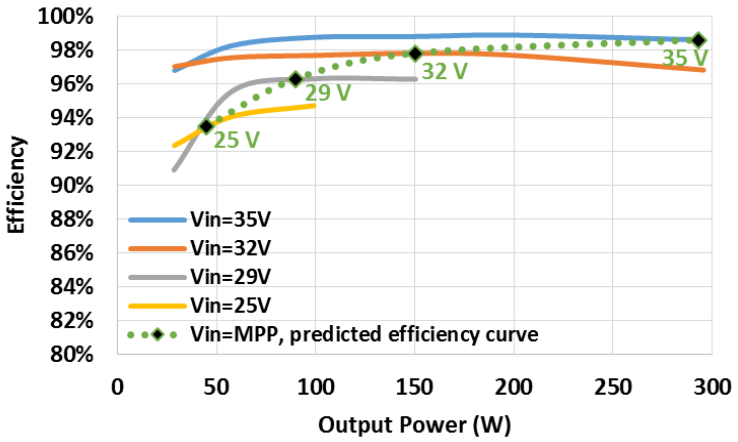
(b) Turn-on transition of S_5: gate-to-source voltage of S_5, v_{gs5}, drain-to-source voltage of S_5, v_{ds5}, output current, I_o.

Figure 4.32. Turn-on transition of primary and secondary side switches with the proposed modulation method: Left is under 30-W load, right is under 300-W load.

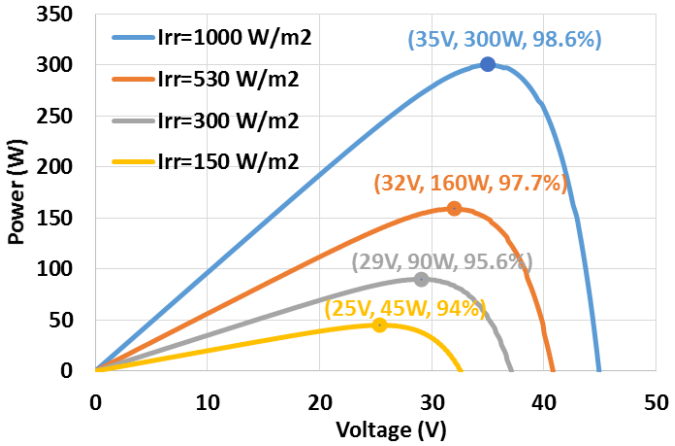
4.5.3 Efficiency and Thermal Testing

The power stage efficiency of the proposed converter is measured for different input voltages and output power levels. The peak efficiency and CEC efficiency under nominal input conditions is 98.9% and 98.72%, respectively, as shown in Figure 4.33 (a). An example with P-V curves generated from Chroma Solar Array Simulator [90] is given in Figure 4.33 (b) to show the efficiency at MPP under different irradiance conditions. The

nominal irradiance condition is set at 1000 W/m^2, where the MPP is 35-V, 300-W. The efficiency at this point is 98.6%. When irradiance is halved, the MPP moves to 32-V, 160-W. The efficiency at this point is 97.7%. Based on the different P-V curves, the predicted efficiency curve with MPP is marked in Figure 4.33 (a) with a dashed line. For the majority of time defined as when irradiance is stronger than 500 W/m^2, the efficiency of the proposed converter is higher than 98%.



(a) Efficiency curves with different input voltages.

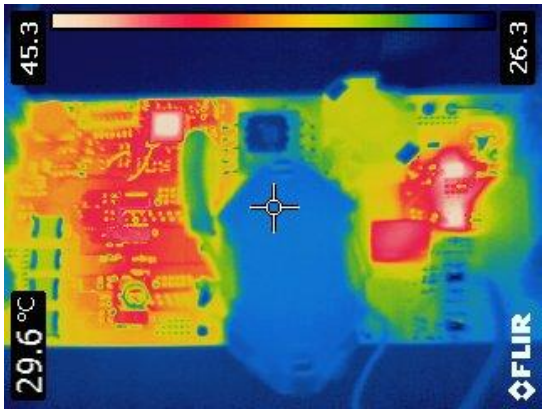


(b) MPP Efficiency at different irradiance conditions.

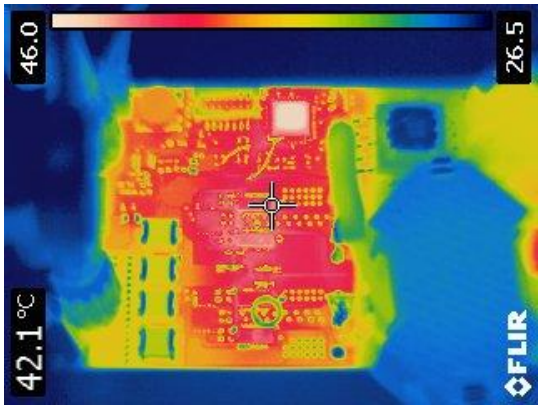
Figure 4.33. Efficiency tesing of the proposed converter.

Under natural convection cooling condition, the thermal performance is tested till steady state and the thermal images are shown in Figure 4.34. This testing is under nominal

input voltage and full load condition. The hottest spot is on the secondary side switches, which has a 47 ^{o}C or 22 °C temperature rise. The temperature of the primary side switches is 32 ^{o}C, or a 7 °C temperature rise. The transformer temperature is measured to be 30 ^{o}C.



(a) Transformer temperature.



(b) Temperature of primary side devices.

(c) Temperature of secondary side devices.

Figure 4.34. Thermal testing under nominal input voltage and full load conditions.

4.5.4 Loss Breakdown Analysis

Section 4.3 gives the loss equations on the transformer and semiconductor devices. This section will give a summary of loss distribution on entire power stage under both nominal and low input voltage conditions.

Table 4.7. Summary of power stage loss distribution under nominal input conditions.

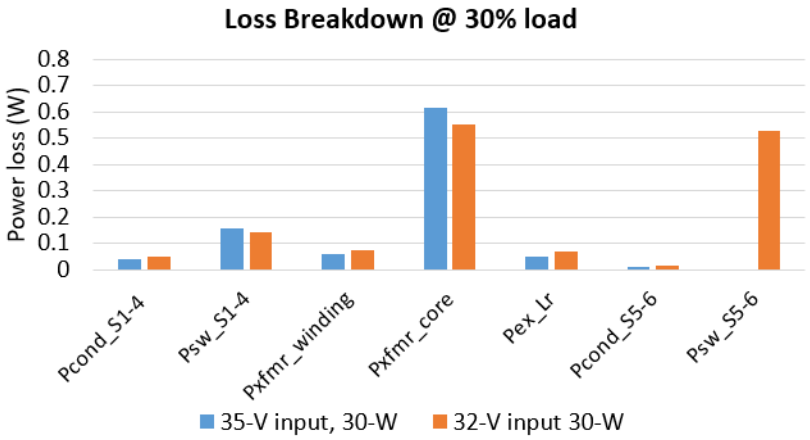
Description	***Equation***
$S_{1\text{-}4}$ conduction loss	$P_{cond\_S1-4} = 4 \cdot (i_{s1\_RMS})^2 R_{dson}$
$S_{1\text{-}4}$ switching loss	$P_{sw\_S1-4} = 2V_{in} i_{Lm} t_{f1} f_s$
$S_{5,6}$ conduction loss	$P_{cond\_S5-6} = 2 \cdot (i_{s5\_RMS})^2 R_{dson}$
Transformer winding loss	$P_{xfmr\_winding} = {i_{pri\_RMS}}^2 R_{pri\_AC} + {i_{sec\_RMS}}^2 R_{sec\_AC}$
Transformer core loss	$P_{xfmr\_core} = C_m {f_s}^x \Delta {B_T}^y \frac{m_{RM14ILP}}{1000} *$
External inductor loss	$P_{ex\_Lr} = {i_{sec\_RMS}}^2 R_{Lr\_AC} + C_m {f_s}^x \Delta {B_{Lr}}^y \frac{m_{RM8ILP}}{1000} *$

Table 4.8. Summary of power stage loss distribution under low input conditions.

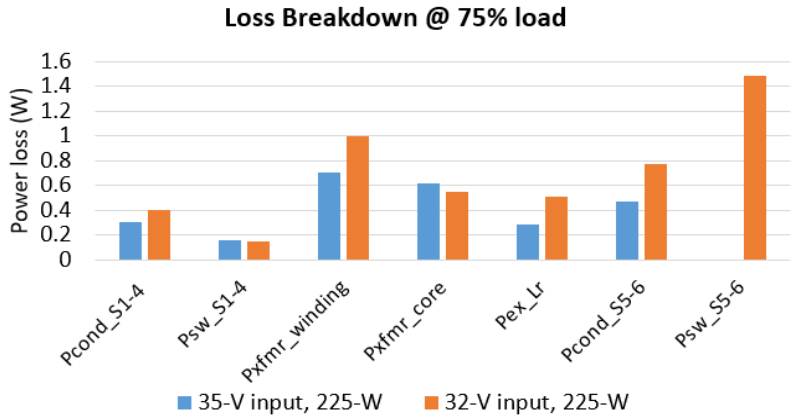
Description	***Equation***
$S_{1\text{-}4}$ conduction loss	$P_{cond\_S1-4} = 4 \cdot (i_{s1\_RMS})^2 R_{dson}$
$S_{1\text{-}4}$ switching loss	$P_{sw\_S1-4} = 2V_o i_{Lm} t_{f1} f_s$
$S_{5,6}$ conduction loss	$P_{cond\_S5-6} = 2 \cdot (i_{s5\_RMS})^2 R_{dson}$
$S_{5,6}$ switching loss	$P_{sw\_S5-6} = \left(C_{oss} V_o^2 + V_o i_{s5\_off} t_{f5}\right) f_s$
Transformer winding loss	$P_{xfmr\_winding} = {i_{pri\_RMS}}^2 R_{pri\_AC} + {i_{sec\_RMS}}^2 R_{sec\_AC}$
Transformer core loss	$P_{xfmr\_core} = C_m {f_s}^x \Delta {B_T}^y \frac{m_{RM14ILP}}{1000} *$
External inductor loss	$P_{ex\_Lr} = {i_{sec\_RMS}}^2 R_{Lr\_AC} + C_m {f_s}^x \Delta {B_{Lr}}^y \frac{m_{RM8ILP}}{1000} *$

Note: * ΔB_T and ΔB_{Lr} is the flux density of transformer and external inductor, respectively. $m_{RM14ILP}$ is the volume of *RM14/ILP* core in m^3; m_{RM8ILP} is the volume of *RM8/ILP* core in m^3.

Under nominal input votlage conditions, a summary of power stage loss is shown in Table 4.7 and power stage loss equations under low input voltage conditions is summarized in Table 4.8.



(a) under 30% load condition.



(b) under 75% load condition.

Figure 4.35. Power stage loss breakdown analysis for 35-V and 32-V input conditions.

Loss breakdown is calculated at 30% and 75% load condition. The CEC efficiency weight under 75% load condition is the highest and is the most important index. Figure 4.35 represents the loss breakdown analysis for different input and output conditions. Under light load conditons, transformer core loss takes a large percentage of total power loss. Under nominal input and full load condition, the main loss are distributed on the conduction loss of switches and magnetics. The switching loss of secodnary switches increase significantly when converter operates under low input voltage conditions with the proposed modulation method.

4. 6 Summary

In this Chapter, a high-efficiency active-boost-rectifier-based converter is proposed for parallel-type modular PVs. A novel double-pulse duty cycle modulation scheme is proposed to ensure that the converter not only keeps the benefits of the highly-efficient SRC converter but also achieves a higher voltage gain than SRC and a wide range regulation ability without adding additional switches while operating under fixed-frequency condition. The proposed converter has the following distinct features.

(1) Compared to the conventional variable-frequency *LLC* resonant converter, it has lower circulating energy due to the fixed-frequency operation.

(2) The converter achieves ZVS turn-on and low-current switching turn-off of primary side switches, and ZCS turn-off of secondary side switches regardless of input voltage or output power.

(3) The proposed active-boost-rectifier merges the Boost circuit and rectifier based on half-bridge configuration, so it reduces the number of power devices compared with

previous literatures. With the proposed double-pulse duty cycle modulation, the output side switches not only serve for synchronous rectification but also for the voltage boost function to achieve high voltage gain.

A 300-W hardware prototype is designed and optimized to verify the performance of the proposed converter. The peak efficiency achieves 98.9% and the CEC efficiency reaches up to 98.7% under nominal input condition.

Chapter 5 High-Power Density MHz-Switching DC-DC Converter for Parallel-type Modular PV Applications

With the availability of wide bandgap devices, power converters can now potentially operate at MHz or higher frequencies while achieving ultrahigh efficiency. Such a high-frequency switching is particularly important for isolated converters to reduce the size of the passive components, achieve high power-density and reduce costs. This chapter presents the proposed converter designed in MHz-switching and compares it with hundred-kHz design in Section 5.2. However, unlike hundred-kHz switching, in MHz-switching, the parasitic components will significantly affect the circuit operation. The exploration on the effects of parasitic inductances and capacitances, as well as the optimization of PCB layout and the planar transformer to reduce these effects, is presented in Section 5.3.

5. 1 Background and Research Motivations

The output of each PV module has a junction box as shown in Figure 5.1 [94]. The diodes to prevent the reversed current and the output terminals are inside the junction box, and the standard cables and connectors are outside of the junction box for the connections to power converters. The size of junction box varies by manufactures. Both for dc optimizer and micro-inverter systems, power converter is in another enclosure with additional wire connection to the PV module. Therefore, the junction box of PV module and power electronics converter are two separated enclosures in the conventional commercialized

systems. Figure 5.2 shows an example of power optimizer system, where the PV modules together with power optimizers are installed on the roof [95].

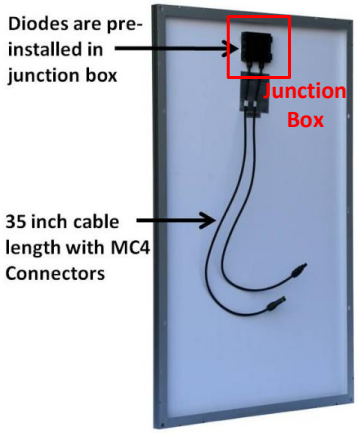


Figure 5.1. Picture of PV module backside.

Figure 5.2. PV modules and power optimizers are installed on the roof.

With the availability of wide bandgap devices, power converters can potentially operate at MHz or higher frequencies to improve power density, especially for isolated converters to reduce the size of the transformer. Therefore, the reduced volume of power converter can have chance to be fixed into the junction box of PV modules, which results in the potentials of cost reduction, space miniaturization, easy transportation and installation convenience. Figure 5.3 shows the proposed concept of merging junction box of PV module and high-power density power converter. Moreover, the converter size

reduction can also provide the potentials of cost reduction by reducing magnetics and potting materials.

Figure 5.3. Proposed merging solution of junction box and power converter.

5. 2 Design of MHz-Switching DC-DC Converter

The specifications of the proposed converter for parallel-type modular PV applications have been presented in Chapter 4 and the circuit of converter to be designed at MHz-switching is shown in Figure 4.2. In this chapter, the targeted switching frequency of proposed converter is 1-MHz.

5.2.1 Basic Design Principles

To design the converter at 1-MHz switching frequency, the nominal input voltage is accommodated from 35-V to 38-V considering the PCB windings design of transformer, while keeping the output voltage at 380-V. The designed converter is optimized for the highest efficiency at nominal input voltage condition to convert the maximum amount of available power. Therefore, the designed converter operates as a series resonant converter at the series resonant frequency in order to achieve the highest efficiency. Since the switching frequency is equal to the resonant frequency, this will occur when the leg comprised of S_1 and S_3 is switched 180° out of phase with the switching leg comprised of S_2 and S_4, resulting in a square wave with peak magnitude of input voltage being applied

to the primary winding of the transformer. The energy is delivered through the entire switching period.

According to the basic principles, the design procedures for operating at resonant frequency have the following steps.

(i) The switching frequency is selected to be the same as the resonant frequency.

$$f_s = f_r = \frac{1}{2\pi\sqrt{L_r\left(C_{r1}+C_{r2}\right)}} \tag{5.1}$$

(ii) The turns ratio of the transformer is entirely determined by the voltage conversion ratio, given as (5.2).

$$n = \frac{V_o}{2V_{in\_nom}} \tag{5.2}$$

(iii) Magnetizing inductance, $L_{m,}$ is designed to provide enough energy to fully charge and discharge the output capacitances of primary side devices during dead-time period. L_m should meet the requirement of (5.3) if i_{Lm} is treated as a constant current source during dead-time period. t_d is the time length of dead-time and C_{oss1} is the output capacitance of S_1. The intra winding capacitance across the primary winding of transformer, C_{Tp}, is considered since the parasitic capacitances of planar transformer is much larger than litz-wire transformer.

$$L_m \le \frac{n^2 t_d}{8 f_s (C_{oss1}+C_{Tp})} \tag{5.3}$$

(iv) Magnetic material P61 is selected for 1-MHz range operation [96]. Core size and PCB winding turns selection is determined through a trade-off between core loss and

winding loss [97]. Furthermore, it should guarantee that the core is unsaturated. The maximum flux density in (5.4) should be lower than B_{sat} which is the flux density for saturation.

$$B_{\max} = \frac{V_{in\_nom}}{4n_1 A_c f_s} \tag{5.4}$$

Where n_1 is the number of turns of primary side winding, and A_c is the cross-section area of core.

(v) The resonant tank design is based on efficiency optimization. L_r is the leakage inductance of the transformer which is determined by the interleaved winding structure. Once the L_r is decided, C_r can be selected by the desired resonant frequency.

(vi) EPC2021 and GS66502B are selected as switches for the primary and secondary sides, respectively, according to the voltage and current stresses.

5.2.2 Magnetics Design at MHz-Switching

Ideally, cross-section area of magnetic core directly related to the core size should be seven times smaller in 1-MHz design compared with 140-kHz design, if the maximum flux density keeps similar to guarantee that the core is unsaturated, according to (5.5).

$$A_c = \frac{V_{in\_nom}}{4n_1 B_{\max} f_s} \tag{5.5}$$

However, the design principle is not only to ensure the core being unsaturated but also to optimize efficiency of magnetic components. Based on Steinmetz equation in (5.6) , the switching frequency is one of main factors on the core loss. C_m, x, y are the coefficients which can be found in the datasheet. Therefore, the designed maximum flux density at 1-

MHz should be no longer similar as 140-kHz. This section will provide the design process of transformer optimization at 1-MHz frequency.

$$P_{core} = C_m f_s^{\ x} B_{\max}^{\ y} \frac{V_e}{1000} \tag{5.6}$$

Among different types of magnetics, the planar magnetics offer great advantages on lower profile, greater surface area, better winding structure interleaving, and lower leakage inductance, which is suitable for MHz designs [98], [99].

The first step is to select the magnetics material. The core loss measurements of different magnetic materials at 1-MHz frequency are compared in Figure 5.4 [100]. P61 and ML91 have relatively low core loss, therefore, they are selected for the manufacturing and experimental comparison.

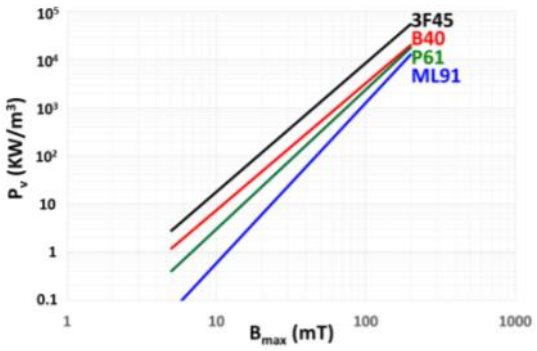


Figure 5.4. Core loss measurement results under 1-MHz excitation [100].

The next step is the core shape selection. A comparison of current distribution in winding between rectangular core pillar and round core pillar was shown in [101]. The winding loss can be reduced effectively by using the round core pillars. DCUT shape is selected because of round core pillar and relative large widow and small volume, as shown in Figure 5.5.

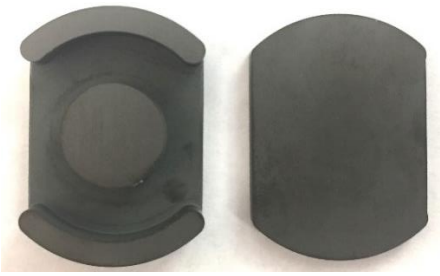
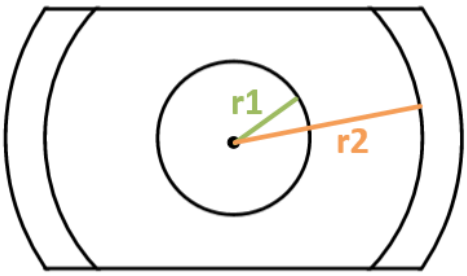


Figure 5.5. Top view of selected DCUT shape core.

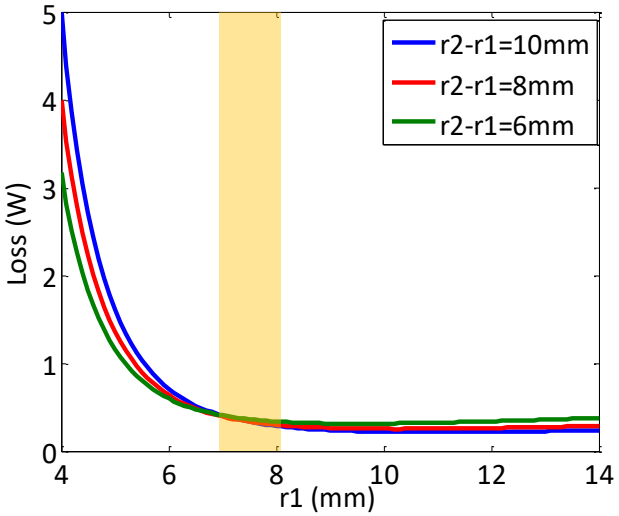
As for the design of PCB windings, skin effect is a key factor to determine the thickness of the winding copper at 1-MHz frequency. The skin effect depth is calculated in (5.7), where ρ is the resistivity of the copper in Ω.m, f is the frequency in Hertz, μ is the absolute magnetic permeability of the conductor. The absolute magnetic permeability $(\mu)=\mu_o$ x μ_r, where μ_o = 4π x 10e-7. 3 oz copper is selected to minimize the skin effect. However, the current density is too high to handle the thermal dissipation if only using single PCB winding. The structure of two PCBs in parallel is adopted to double current capability.

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \tag{5.7}$$

To determine the dimensions of the magetic core, the curves of the transformer loss versus radius of core pillar is calculated in Figure 5.6 (b), when the primary winding is fixed at 2 turns and secondary winding sets at 10 turns. The transformer loss, which is the summation of core loss and winding loss, decreases significantly with the increasing length of r_1 from 0 to 7 mm, regardless of the dimension of window width. When r_1 is longer than 7 mm, the power loss curves become flat, however, the core size is increased. Therefore, the desired dimension of r_1 should be in the range of 7-8 mm for small core size and low transfomer loss.



(a) Designed core with marked geometry dimensions.



(b) Transformer power loss versus geometry of magnetic core.

Figure 5.6. Geometry design of magnetic core based on efficiency optimization.

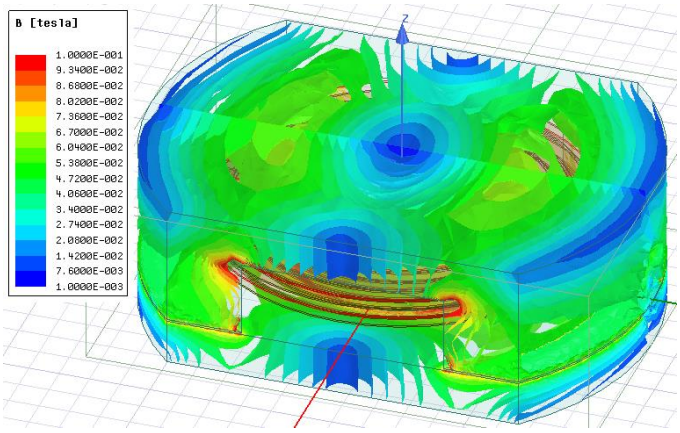


Figure 5.7. Flux density distribution in FEM simulation.

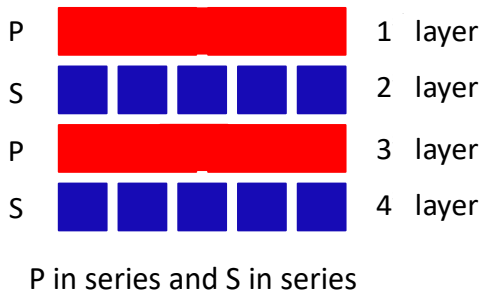


Figure 5.8. PCB winding structure.

With the designed core and PCB windings, the flux density distribution is simulated with Finite Element Method (FEM), which is shown in Figure 5.7. The flux density of majority of the core area is around 30 - 40 mT. Figure 5.8 shows the PCB winding structure, which is a 4-layer PCB with 2 turns of primary winding and 10 turns of secondary winding fully interleaved. The leakage inductance is fully used as the resonant inductance, and the additional external inductor is not necessary, which is different with 140-kHz design. Combined with all the procedures above, the parameters of custom-designed core are summarized in Table 5.1.

Table 5.1. Summary of designed 1-MHz transformer.

Description	***Value***
Core shape	DCUT
Core material	P61/ML91
Cross-section area, A_c	144 mm^2
Turns ratio, n	2:10
Winding AWG of primary turns, n_1	2 turns, 3 oz copper, 5.5 mm width
Winding AWG of secondary turns, n_2	10 turns, 3 oz copper, 0.9 mm width
Thickness of air gap	5 mil
Magnetizing inductance, L_m	60 µH
Leakage inductance, L_{lk}	460 nH

5.2.3 Optimization of PCB Layer Structure

Because of high switching frequency, the ac effects including skin effect and proximity effect will play a significant role at MHz operations. The PCB copper loss at the primary side is a large portion in the distribution of total loss due to the high current through low input side and ac effects, and the copper loss at the secondary side can be neglected even though the ac effects are considered since the current through secondary is low. To minimize the loss on the PCB coppers of the primary side circuit, the PCB layer structure needs to be optimized through FEM simulation. The conventional concepts, such as the thick copper results in low resistance, will not be suitable for MHz designs. The PCB layout of primary side is imported and modified into ANASYS Q3D Extractor for FEM simulation as shown in Figure 5.9.

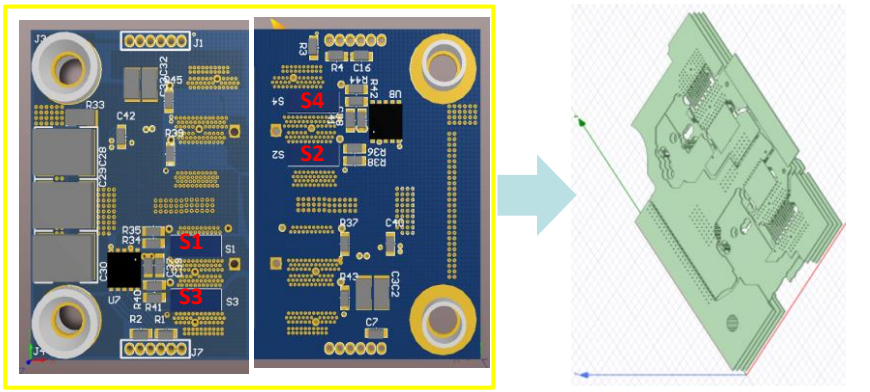


Figure 5.9. Imported PCB layout to FEM simulation software.

Since the loops of primary side full-bridge circuit during positive switching cycle and negative switching cycle are symmetrical, only the power loop during positive switching cycle is simulated in order to simplied the procedures of analysis. The switch of S_1 and S_4 , as well as the transformer primary winding, are replaced with three small pieces

of pure coppers. Therefore, the resistance of entire loop are mainly from the coppers of original PCB layout. Figure 5.10 shows the simulated power loop during positive switching cycle, which is going through the coppers connecting positive terminal of input, S_1, primary side of transformer, S_4 and negative terminal of input.

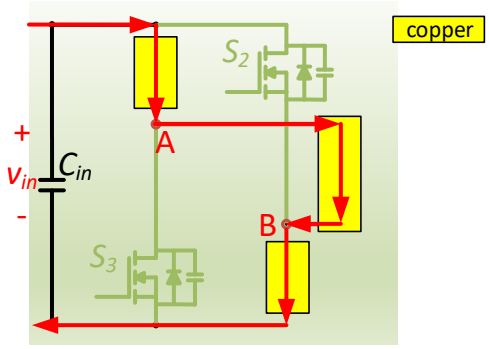


Figure 5.10. Simulated power loop during positive half switching cycle, where switches and transformer winding are replaced with coppers.

4-layer PCB is initially selected considering of cost and manufacture. One of critial concerns is the copper thickness, since the thin copper causes high dc resistance and low ac/dc ratio and the thick copper will result in low dc resistance and high ac/dc ratio due to ac effects at high frequency. The 4-layer PCBs with 1, 2, 3 and 4 oz copper thickness are simulated in ANASYS Q3D Extractor. The distance between the adjacent layers keeps same to have a fair comparison as shown in Figure 5.11.

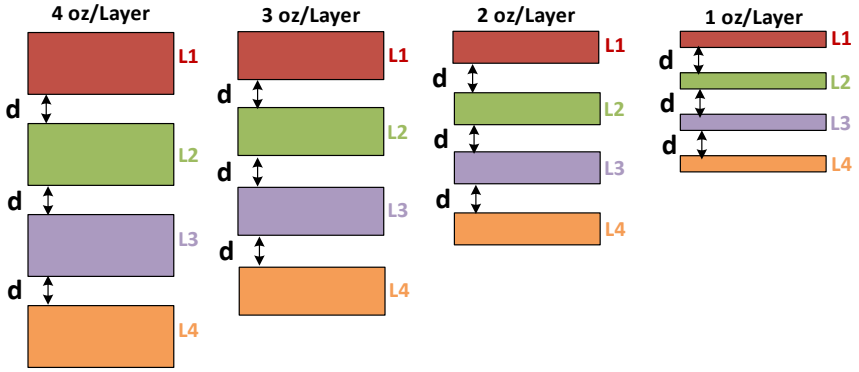
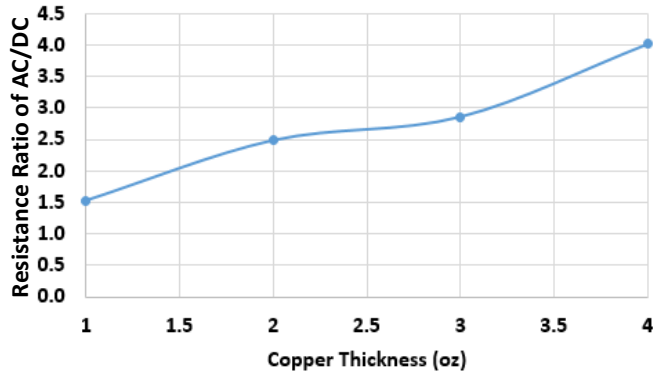
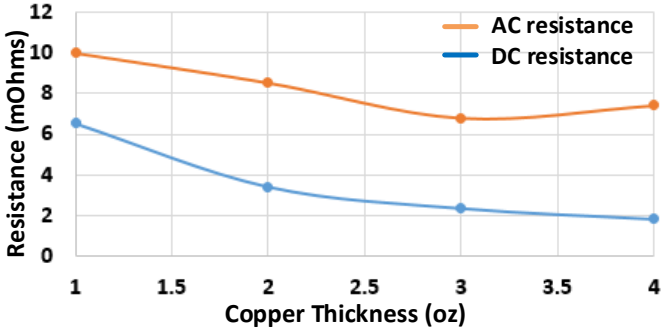


Figure 5.11. Simulated 4-layer PCB sturctures with different copper thickness.

The simulated resistances with four cases are shown in Figure 5.12. The blue curve represents the dc resistance, and it shows that the thinner copper has the higher dc resistance. However, the resistance ratio of ac/dc increases with the increasing of copper thickness. Under the cases of 1, 2 and 3 oz coppers, the total ac resistance is still decreasing even though the resistance ratio of ac/dc increases. This is because the decreasing of dc resistance dominates the change of total resistance. When the copper thickness increases to 4 oz, the weight of increasing of ac/dc resistance ratio is higher than the decreasing of dc resistance, which results in a higher ac resistance. Therefore, the case of 3 oz copper is the best choice for the 4-layer PCB structure.



(a) Simulated resistance ratio of ac/dc.



(b) Simulated dc and ac resistance with different copper thickness.

Figure 5.12. Simulation results of 4-layer PCB sturctures with different copper thickness.

Now that the 3 oz copper is determined, structure with more layers should be considered to compare with 4-layer when the total copper thickness is kept same. For example, as shown in Figure 5.13, each layer is originally configured with 3 oz copper for 4-layer structure, and this 3 oz separates to two layers of 1.5 oz for 8-layer PCB structure and three layers of 1 oz for analysis PCB structure, respectively. The simulation results are summarized in Table 5.2, where both of dc resistance and ac resistance increase with the increasing of number of layers. Since different layers are connected though a large amount of via, the resistance induced from these via increases with number of layers increasing.

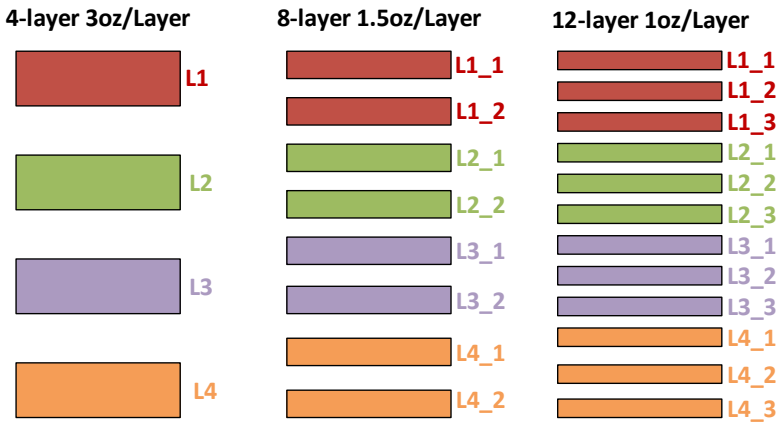


Figure 5.13. Simulated PCB sturctures with different layers.

Table 5.2. Simulation results with different numbers of layers.

Layer Structure	*DC Resistance (mΩ)*	*AC Resistance (mΩ)*
4-layer, 3 oz/layer	2.16	7.79
8-layer, 1.5 oz/layer	2.38	8.96
12-layer, 1 oz/layer	2.59	10.77

In conclusion, the PCB structure with 4 layers and 3 oz copper of each layer is the best case to minimize the PCB copper loss. The total resistance during positive switching cycle is 6.78 mΩ at 1-MHz switching frequency, while the dc resistance is only 2.37 mΩ.

The ac resistance in the power loop is comparable to the total on-state resistance of two switches. Although the PCB layer structure is optimized, the copper loss of primary side circuit is still one of main distributors on the circuit total loss, which is entirely different with the 140-kHz design.

5.2.4 Experimental Verifications

The hardware prototype with a maximum power level of 300-W was built as shown in Figure 5.14. The system adopts sandwich structure, where the top board is the power stage board and the bottom one is the control board. Texas Instrument DSP 280049 is utilized for the control system. The prototype dimensions are 3.3” of length, 1.5” of width and 0.5” of height. The nominal input voltage is designed at 38-V and the output voltage is fixed at 380-V. The designed parameters are listed in the Table 5.3.

Figure 5.14. Hardware photograph.

Table 5.3. 1-MHz prototype design summary.

Description	***Value***
Switching frequency	1-MHz
Resonant inductance, L_r	460 nH
Resonant Capacitance, $C_{r1,2}$	10 nF (600 V, NP0)
Magnetizing inductance, L_m	60 µH
Transformer turns ratio, n	2:10
Primary side switches, $S_{1\text{-}4}$	EPC2021
Secondary side switches, $S_{5,6}$	GS66502B

The steady-state experimental waveforms are shown in Figure 5.15, where the testing condition is 38-V input voltage and 300-W output power. The light blue waveform is the voltage across the primary winding of transformer and the green waveform is the resonant current. The converter operates as a pure series resonant converter and the current is pure sinusoidal with 2.4-A peak value. The ringing during dead-time period is serious causing by the parasitic components.

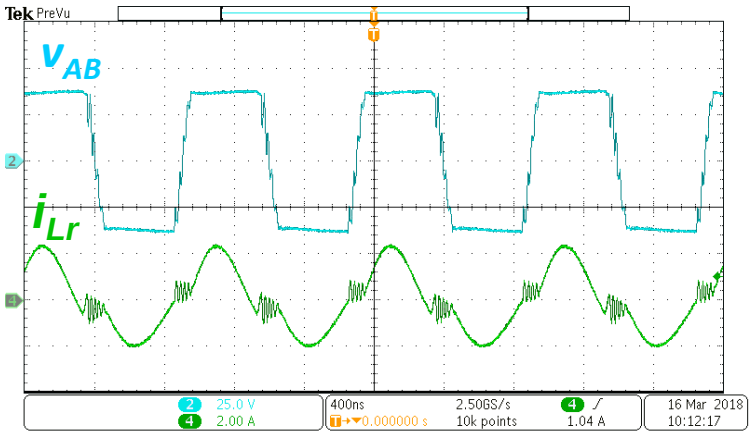


Figure 5.15. Experimental steady-state waveforms under nominal input voltage (38-V) and full load condition: voltage across primary winding of the transformer , v_{AB}, resonant current, i_{Lr}.

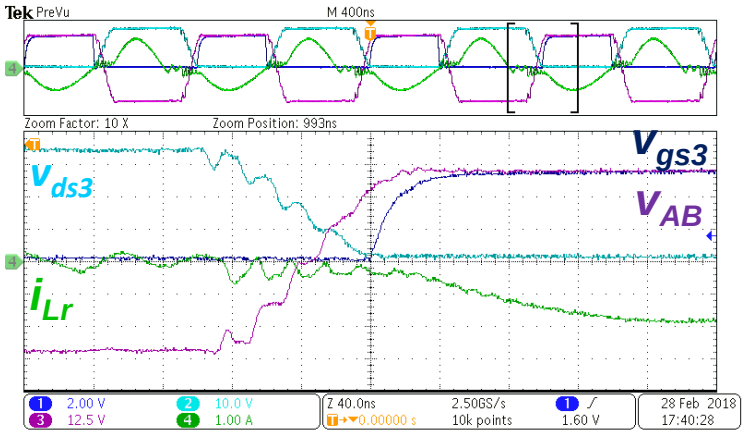


Figure 5.16. Turn-on transition of S_3 under nominal input voltage (38-V) and full load condition: voltage across primary winding of the transformer , v_{AB}, resonant current, i_{Lr}. gate-to-source voltage of S_3, v_{gs3}, drain-to-source voltage of S_3, v_{ds3}.

Figure 5.16 shows the ZVS turn-on transition of S_3, which is similar to turn-on transitions of $S_{1,2,4}$. The turn-on gate is applied after the drain-to-source voltage drops to zero.

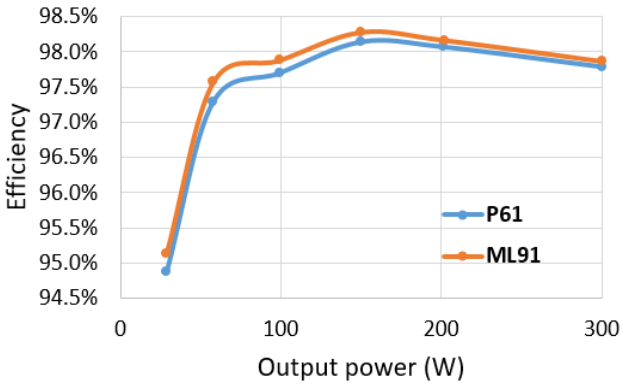


Figure 5.17. Efficiency tesing and comparison with magnetic materials of P61 and ML91 under nominal input condition.

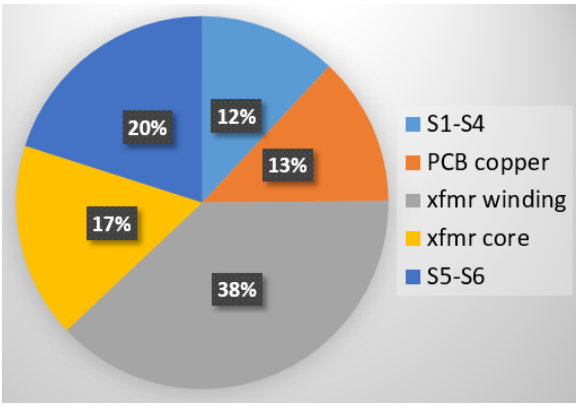


Figure 5.18. Power stage loss breakdown analysis under 38-V input and 300-W load condition.

The power stage efficiency of 1-MHz design is measured for different magnetic materials and output power levels with nominal input condition. Material of ML91 shows a better performance than material of P61. The peak efficiency and CEC efficiency with ML91 achieves 98.3% and 97.9%, respectively, as shown in Figure 5.17. The loss breakdown is analyzed in Figure 5.18, where the main loss is from transformer including

winding loss and core loss. It is noteworthy that loss from PCB copper is also a significant distributor.

5.2.5 Converter Comparison between 140-kHz and 1-MHz Switching

This section gives a comprehensive comparison of between the design of proposed converter in 140-kHz and 1-MHz switching frequency, in terms of the magnetics design, hardware prototype and experimental results.

Figure 5.19 gives the pictures of the magnetics design. In the design of 140-kHz, the external inductor is needed for resonance, since the leakage inductance of transformer is not large enough to provide regulation ability for full operating range. However, the leakage inductance of planar transformer in 1-MHz design can be treated as entire resonant inductance. The litz-wire windings are utilized in 140-kHz design for the efficiency optimization, while the PCB windings are adopted in 1-MHz design for consideration of high-power density. The parameters of transformer are compared in Table 5.4. In terms of transformer effective volume, the design in 1-MHz reduces more than 60% of the design in 140-kHz.

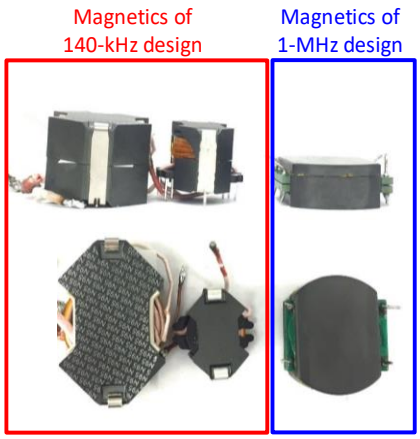


Figure 5.19. Pictures of magnetics of 140-kHz and 1-MHz designs.

Table 5.4. Magnetics Comparison between 140-kHz and 1-MHz designs.

Parameters of Transformer	***140-kHz Design***	***1-MHz Design***
Magnetizing inductance, L_m	660 µH	60 µH
Leakage inductance, L_{lk}	4.65 µH	460 nH
Length	42.2 mm	33.2 mm
Width	20 mm	23.7 mm
Height	20.5 mm	11.1 mm
Cross-section area, A_c	201 mm^2	144 mm^2
Effective volume, V_e	10230 mm^3	3948 mm^3
Core material	3C95/N95	ML91/P61
Maximum flux density, B_{max}	80 mT	33 mT

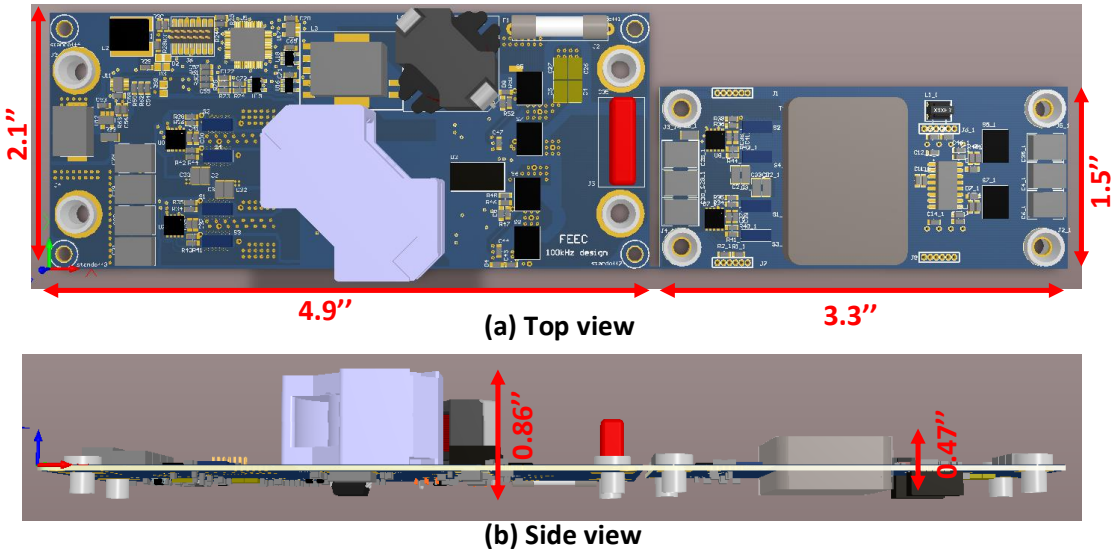


Figure 5.20. 3D PCB board comparison: Left is 140-kHz design and right is 1-MHz design.

The PCB boards of the designed power converter in 3D view are compared in Figure 5.20. The dimensions of 140-kHz design is 4.9” length, 2.1” width and 0.86” height, so the total volume is 8.85 in^3, while the dimensions of 1-MHz design is 3.3” length, 1.5” width and 0.47” height with the total volume of 2.33 in^3. Therefore, the volume of 1-MHz design has 74% volume reduction of 140-kHz design.

Figure 5.21 shows the hardware prototype of two designs. Both use the same EPC GaN device in the primary side and GaN Systems device for the primary side. The testing efficiency curves under nominal input condition are plotted in the Figure 5.22. The peak efficiency of 140-kHz and 1-MHz designs reach to 98.9% and 98.3% respectively, and the CEC efficiency of 140-kHz and 1-MHz designs are 98.7% and 97.9% respectively.

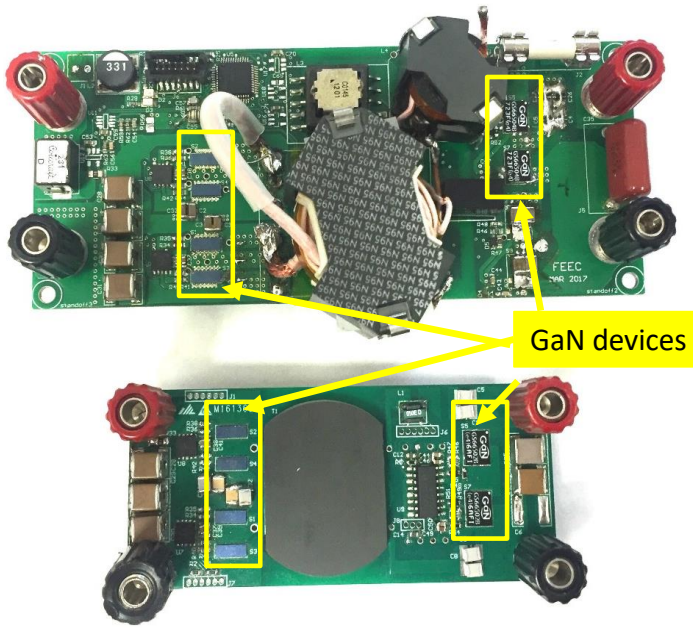


Figure 5.21. Hardware photographs of 140-kHz and 1-MHz designs.

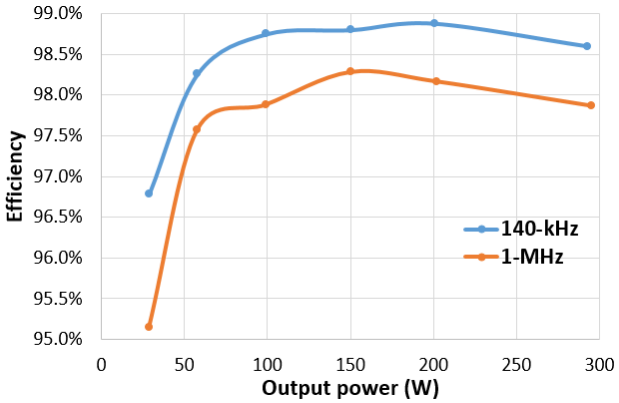


Figure 5.22. Efficiency tesing and comparison with 140-kHz and 1-MHz designs under nominal input condition.

5. 3 Circuit Design Considerations for Reducing Parasitic Effects

Many previous works have been published to explore the design considerations and optimization of resonant converter at MHz switching frequency [102] -[116]. In [102] and [103], a new modulation method were proposed for higher efficiency operation. [104] and [105] improved the digital implementation and performance of synchronous rectification. Circuit integration is also a hot topic at MHz switching. [106] focused on the integration of active components, while passive component integration was designed in [107]. Transformer design and optimization, including core and windings, was researched in [108]. In [109] and [110], EMI performance and reduction techniques were studied. All these papers mainly focused on the control implementation, switch performance, EMI reduction, passive components design and circuit integration. Only few of the papers discussed about the effects and the design considerations of the parasitic components under MHz operations [111] - [116]. The ringing in the circuit operation caused by parasitic inductance was briefly discussed in [111] and the influence of the parasitic capacitance to the voltage gain was presented in [112] - [114]. In [115] and [116], the effect and minimization of parasitics components on gate drive loop were studied with application of GaN devices.

However, the effects of the circuit parasitic components on the steady-state operations at MHz and even higher switching frequencies, especially for high step-up and high step-down converters, have never been presented and always neglected. The main reason that it can severely affect the operation of the resonant converter is because the parasitic inductances will be n^2 higher when it reflects from low voltage (LV) side to high

voltage (HV) side and the parasitic capacitances are also n^2 higher while reflecting from HV side to LV side, where n is defined as the number of turns of HV side over the number of turns of LV side. In many applications of renewable energy systems, such as in photovoltaic systems, n is often higher than 10. Therefore, the reflected parasitic values will be comparable to the originally designed resonant LC component values. They will further influence the circuit operation, such as the resonant frequency, asymmetrical operation between positive and negative cycles, higher voltage and current stresses, and more losses. Therefore, the design considerations relating to parasitic components at MHz switching should receive considerable attention compared to conventional kilohertz (kHz) switching.

In this section, the parasitic effects on circuit steady-state operation and the design techniques to mitigate parasitic effects of high step-up/down resonant converter are illustrated and analyzed. Certain conventional PCB layout of bridge-based circuit may lead to the asymmetrical parasitic inductances between positive and negative half switching cycles, which may further result in the asymmetrical steady-state operation, higher electrical stresses, and higher thermal stresses. Even when the PCB layout is symmetrical, the parasitic inductance should be taken into account as partial resonant inductance when designing parameters of the resonant network. Moreover, the conventional method of stacking up PCB windings to enlarge the current capability for transformer is no longer suitable in MHz operations under some cases, as more winding boards will introduce larger winding capacitances. Then it will require more magnetizing energy and take a longer dead-time to fully achieve ZVS of switches, which hurts the efficiency and reduces the energy delivery period as well.

In the high step-up/down resonant converter topology, the resonant tank is typically placed on the high voltage (HV) side based on power conversion efficiency considerations, since the HV side has lower current. Figure 5.23 is an example topology of the high step-up resonant converter, which is the designed converter in this dissertation for modular PV applications including the parasitic components. The primary side is the low voltage (LV) side which is a full-bridge comprised of switches $S_{1\text{-}4}$, and the secondary side is the HV side which is a half bridge comprised of switches $S_{5,6}$. To extend the range of applications, the configurations on both sides can be replaced by other networks such as full-bridge, half-bridge, push-pull and etc. If power flow goes from the LV to HV side, the topology is an isolated SRC; and if the power flow goes from the HV to LV side, the topology is a *LLC* converter.

Beside the main components, the parasitic components will also impact the converter operation at MHz switching frequency. The parasitic inductances of LV side include the inductances induced from PCB and inductances inside of $S_{1\text{-}4}$ as shown in Figure 5.23. When S_1 and S_4 are on, the period is referring to as positive half cycle. When S_2 and S_3 are on, the period is referring to as negative half cycle. L_{p1}, L_{s1}, L_{s4} and L_{n2} will be involved in the converter operation during the positive half cycle, while L_{p2}, L_{s2}, L_{s3} and L_{n1} will be involved in the converter operation during the negative half cycle. Once these parasitics are considered into the circuit operation, the resonant inductor will no longer be L_r itself. The equivalent resonant inductances are expressed in (5.8) and (5.9) for positive and negative half cycles respectively.

$$L_{r\_eq\_p} = L_r + n^2 \left(L_{p1} + L_{s1} + L_{s4} + L_{n2} \right) \tag{5.8}$$

$$L_{r\_eq\_n} = L_r + n^2 \left(L_{p2} + L_{s2} + L_{s3} + L_{n1} \right) \tag{5.9}$$

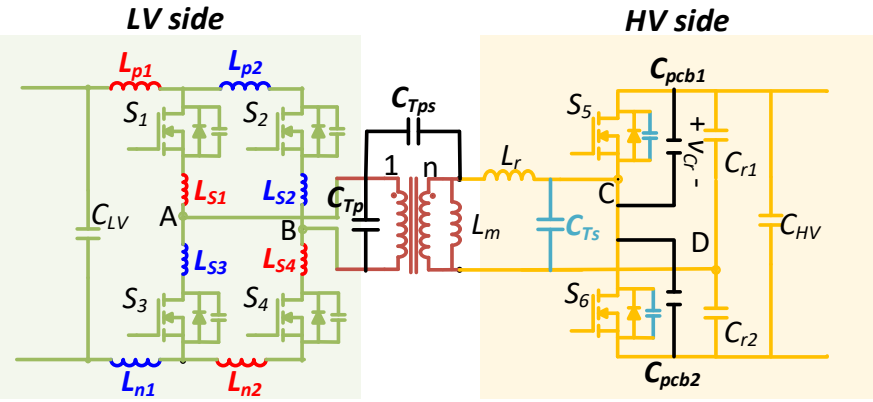


Figure 5.23. High step-up/down resonant converter with parasitic components.

Parasitic capacitances of the HV side include intra winding capacitance across the HV side winding of the transformer C_{Ts}, output capacitances of S_5 and S_6, and the capacitances induced from the PCB. Parasitic capacitances of LV side include intra winding capacitance across transformer LV side winding C_{Tp} and the output capacitances of S_1-S_4. These capacitances will be involved in the switching transitions during dead-time period, which will affect ZVS transitions of the switches.

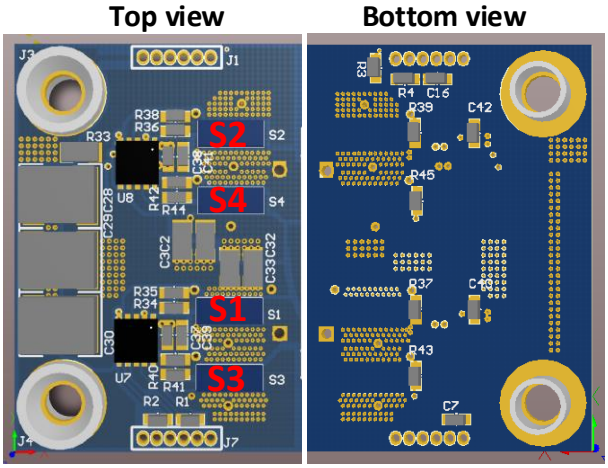
Additionally, inter winding capacitance of the transformer, $C_{Tps.}$ could induce common-mode (CM) noise [117]. However, this work mainly focuses on the impact of parasitics on the circuit in steady-state operation. The effects and reduction of C_{Tps} is not discussed in this dissertation.

5.3.1 Effects of LV Side Parasitic Inductances

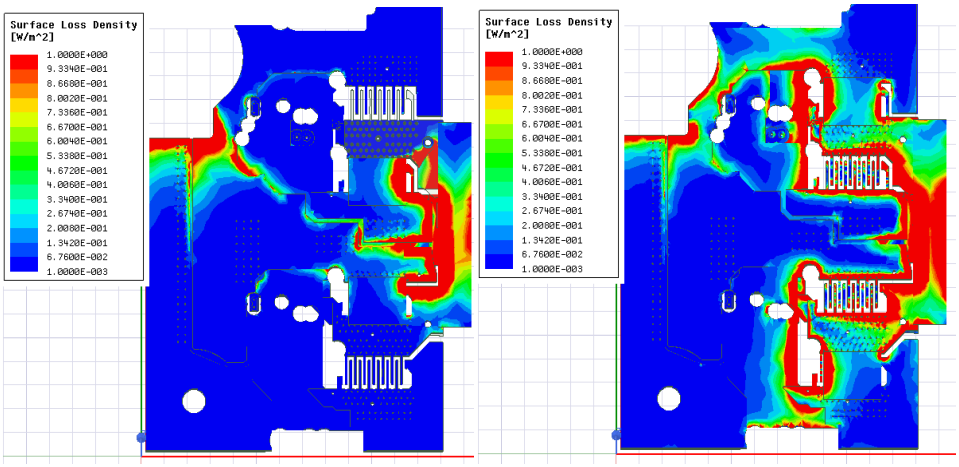
Compared to half-bridge circuit, full-bridge circuit is always selected for applications with high current and conduction loss dominance, since a full-bridge sees half

of the current of what a half-bridge sees. The total conduction loss on the switches and transformer windings of a full-bridge is half of the half-bridges'.

One of the typical layout styles for full-bridge circuit is shown in the Figure 5.24 (a). Both two legs are on the same PCB side, either top layer or bottom layer. Quite a few prototypes and products show their layouts in this way for the convenience of heat sink design and other considerations [118] - [119]. However, the loop length of the positive half cycle is asymmetrical to the loop length of the negative half cycle in this way. Since S_1 and S_4 are close to each other, the loop of the positive half cycle is much shorter, while the loop of the negative half cycle is much longer due to long distance between S_2 and S_3. The asymmetrical layout may cause imbalance of parasitic inductances on the PCB traces. To simulate the parasitic inductances of the PCB traces, the PCB layout is imported to the ANSYS Q3D Extractor for FEM simulation. The simulation results are shown in Figure 5.24 (b), where the high current-density area for the positive half cycle is much larger than the negative half cycle. Moreover, the difference in parasitic inductance between positive and negative half cycles is more than 10.5 nH in the ACL simulation results in Table 5.5.



(a) 3D view of Full-bridge layout 1.



(b) Parasitic simulation results from ANSYS Q3D Extractor with Full-bridge layout 1.

Figure 5.24. FEM simulation of Full-bridge layout 1 with both of two legs on the top or bottom layer.

Table 5.5. Simulated parasitic inductances with two layout styles.

Simulated ACL @ 1-MHz	***Layout 1***	***Layout 2***
Inductance of positive half cycle	9.26 nH	16.47 nH
Inductance of negative half cycle	19.72 nH	15.69 nH
Inductance difference in LV side	10.54 nH	0.82 nH
Inductance difference reflected to HV side	263.5 nH	20.5 nH
Percentage of L_r	57.3%	4.5%

To further prove the effectiveness of the FEM simulation method, experiments and measurements are conducted to compare with the simulation results. Figure 5.25 shows the circuit for testing of the parasitic inductances. The active rectifier is replaced by an external capacitor with 100 nF. Therefore, the series resonant network in Figure 5.25 is comprised of the external capacitor and the total inductance of L_r and the equivalent parasitic inductance reflected from LV to HV side. The experimental waveforms are shown in Figure 5.26, where the resonant frequency of positive half cycle is 25.1-MHz and the resonant frequency of negative half cycle is 17.3-MHz. The resonant frequencies for

positive and negative half cycles are expressed in (5.10) and (5.11) respectively. Thus, the inductance difference between positive and negative half cycle can be calculated in (5.12) which is matched with the simulation results.

$$f_{r\_p} = \frac{1}{2\pi\sqrt{C_{ext}L_{r\_eq\_p}}} = 25.1MHz \tag{5.10}$$

$$f_{r\_n} = \frac{1}{2\pi\sqrt{C_{ext}L_{r\_eq\_n}}} = 17.3MHz \tag{5.11}$$

$$L_{r\_eq\_n} - L_{r\_eq\_p} = 10nH \tag{5.12}$$

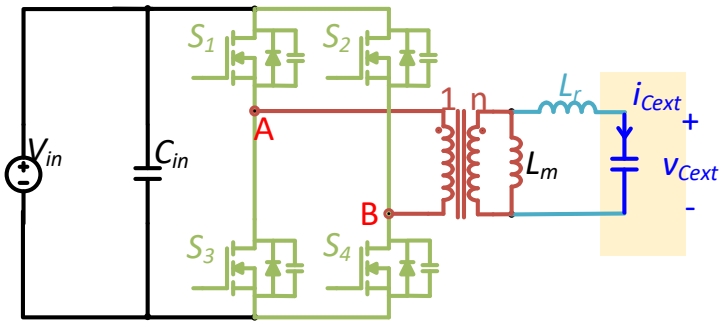
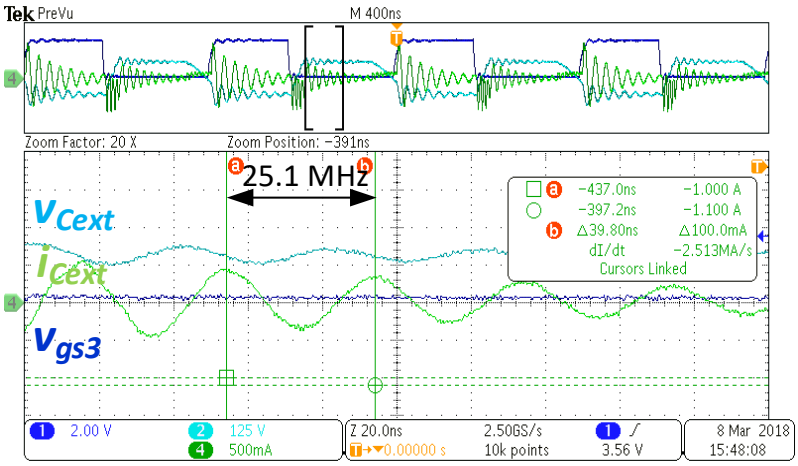
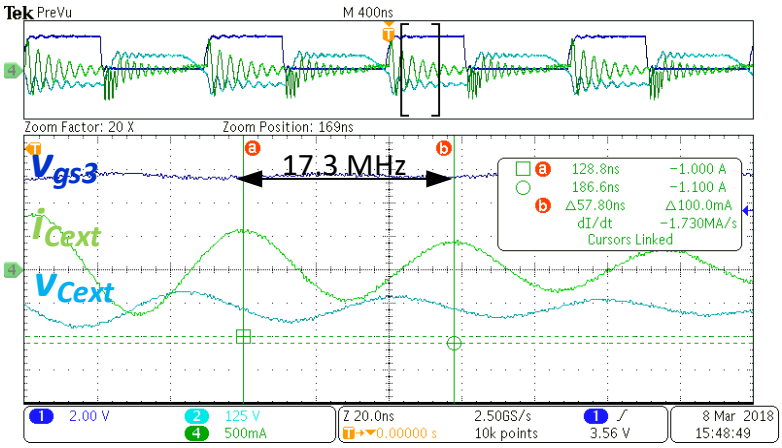


Figure 5.25. Circuit for testing of parasitic inductances distributed in LV side.



(a) Waveforms during positive half cycle.



(b) Waveforms during negative half cycle.

Figure 5.26. Experimental waveforms of the parasitic inductance testing.

The inductance difference of 10 nH is usually neglected in the kHz designs, since the resonant inductor is tens of micro-henry (μH) and higher which is much larger than the inductance difference caused by PCB traces. However, in the MHz designs, it does affect the converter operation, since the equivalent inductance difference is 250 nH when it is reflected to the HV side, which is more than 50% of L_r. Figure 5.27 shows the simulation results of circuit operation with asymmetrical parasitic inductances acquired from the FEM analysis.

(i) i_{Lr} is a narrower pulse with higher peak value during the positive half cycle, and a wider pulse with lower peak value during the negative half cycle. Moreover, the LV side current, i_{pri}, is also unbalanced. Current unbalance typically leads to an increase in the rms current of the active devices, and degrades the performance of the transformer and switches.

(ii) Additionally, the unbalanced i_{Lr} resonates to different current values between the positive and negative half cycles before the dead-time period. During the negative half

cycle, $i_{Lr,}$ resonates to zero when the energy transfer period ends which corresponds to the designed resonant frequency. However, i_{Lr} reaches negative 0.8-A across the same period of time during the positive half cycle. Therefore, the initial currents of i_{pri} at the beginning of dead-time period will be different and further affect the ZVS operation, resulting in asymmetrical ringing during the dead-time periods.

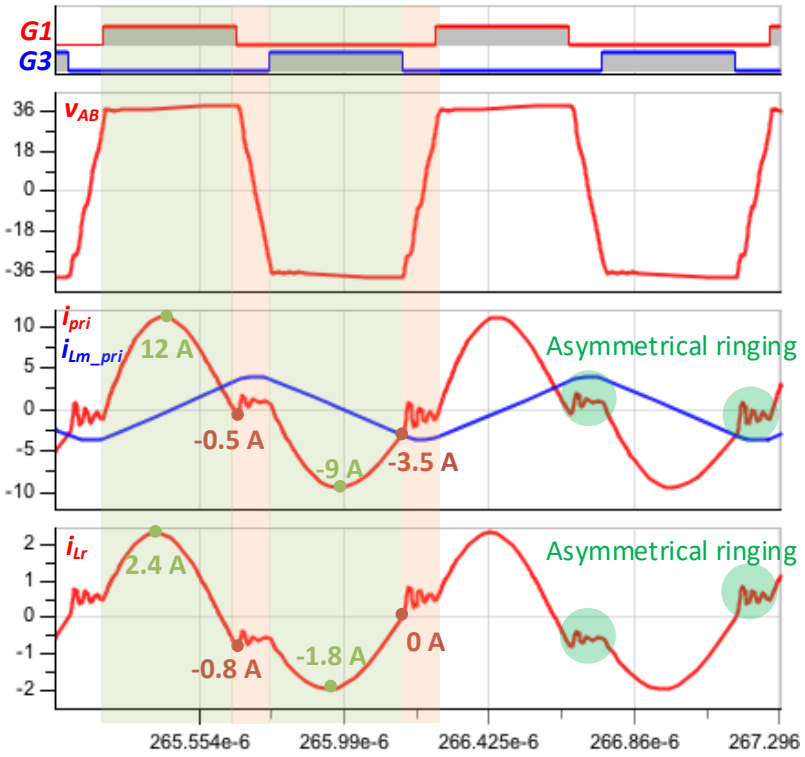
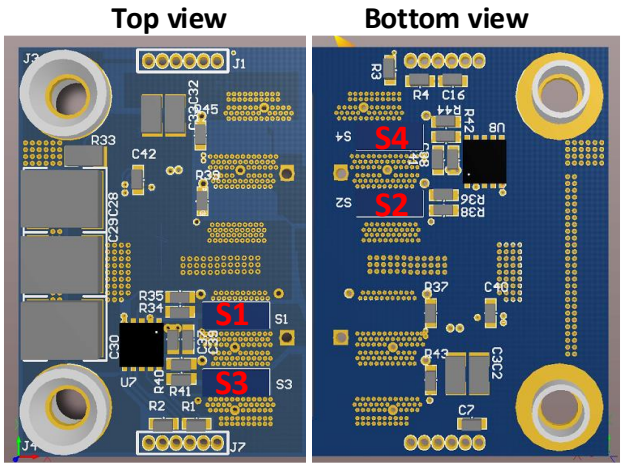


Figure 5.27. Simulation waveforms with 10 nH and 19 nH parasitic inductances of positive and negative half cycles, respectively.

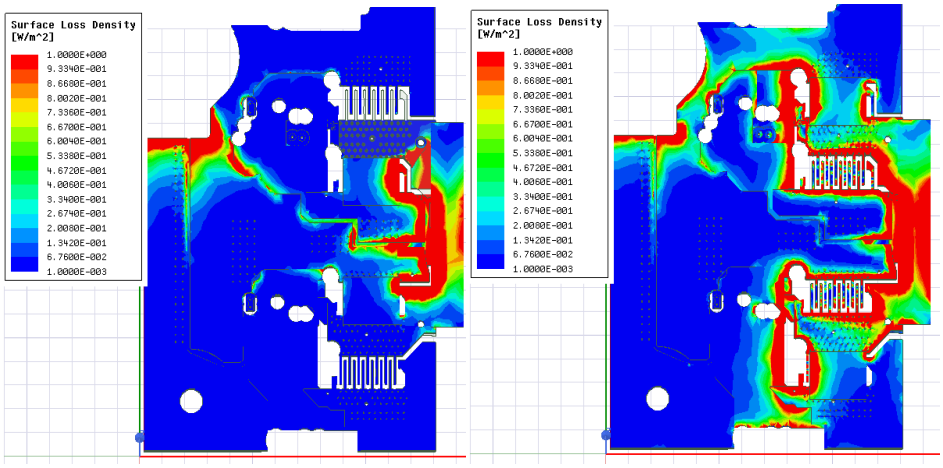
In conclusion, the current unbalance issue induced from asymmetrical PCB layouts in MHz resonant converters hurts the converter performance and power conversion efficiency. In order to overcome the asymmetric current problem, Figure 5.28 (a) shows the revised PCB layout for full-bridge circuit, where one leg is on the top side and the other leg is on the bottom side. This way, similar loop parasitic inductances between positive and negative half cycles can be achieved since the distance between S_1 and S_4 is the same

as the distance between S_2 and S_3. The simulation result is shown in Figure 5.28 (b). The inductance difference between positive and negative half cycles is only 0.82 nH from FEM simulation results, as listed in Table 5.5. This small difference is no longer an issue to the converter operation since the equivalent inductance is only 20.5 nH, 4.5% of L_r when reflected to the HV side. There are alternative options for symmetrical loop inductance design, such as exchanging the positions of S_2 and S_4. However, the gate drive loops for S_2 and S_4 will be longer and asymmetrical to the other leg. The optimized layout design considers both the gate drive loop and power loop.

Besides the asymmetrical issue, the design of resonant tank parameters is also influenced by parasitic inductance for high step-up/down resonant converters. Traditionally, the resonant inductance of converter is the leakage inductance of the transformer if there is no external inductor added. However, in MHz design, the parasitic inductance reflected from the LV to HV side can be up to hundred-nH which is comparable to the leakage inductance of the transformer. In the design of this paper, the parasitic inductance created from the LV side is around 15 nH. It becomes 375 nH when it reflects to the HV side which is about 80% of the leakage inductance. Therefore, the inductance involved in the resonance is no longer the leakage inductance of the transformer itself but the summation of the leakage inductance and the equivalent parasitic inductance reflected from the LV side.



(a) 3D view of Full-bridge layout 2.



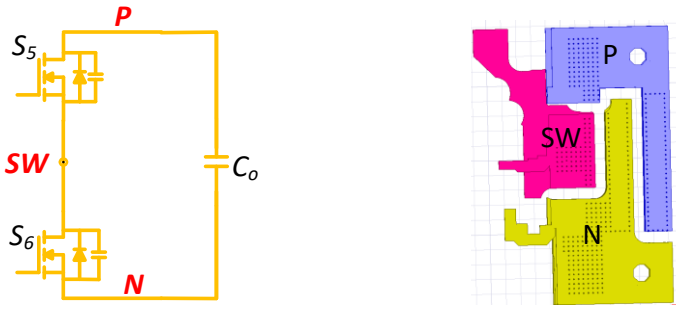
(b) Parasitic simulation results from ANSYS Q3D Extractor with Full-bridge layout 2.

Figure 5.28. FEM simulation of Full-bridge layout 2 with one leg on the top layer and the other leg on the bottom layer.

5.3.2 Effects of HV Side Parasitic Capacitances

To verify the capacitances induced from the PCB layout of HV side circuit, the PCB layout of the HV side circuit is imported into ANSYS Q3D Extractor, as shown in Figure 5.29 (b). The net of positive output, switching node and negative output are named as “P”, “SW” and “N” as shown in Figure 5.29 (a). The simulation results show that the capacitance between “P” and “SW” is 1.4 pF, same as the capacitance between “SW” and

"N". Therefore, both of C_{pcb1} and C_{pb2} are equal to 1.4 pF in Figure 5.23. As $C_{pcb1} << C_{oss5}$ and $C_{pb2} << C_{oss6}$, both are neglected in the following analysis.



(a) Simulated circuit. (b) PCB layout.

Figure 5.29. Simulation of capacitances induced from power loop copper in the secondary side.

It is well known that the switches on the LV side achieve ZVS turn-on by the magnetizing current during the dead-time period, as shown in Figure 5.30. However, the magnetizing energy to charge and discharge the HV side parasitic capacitances cannot be ignored for high step-up/down resonant converters. The revised circuit model for ZVS operation is shown in Figure 5.31. During the dead-time period, the magnetizing current charges and discharges not only the parasitic capacitances of the LV side but also the parasitic capacitances of the HV side which includes the intra winding capacitance across the HV side winding of the transformer C_{Ts} and output capacitances of the active switches' $C_{oss5,6}$. The equivalent capacitance from the HV to LV side is expressed as (5.13). Therefore, the design criteria of the magnetizing inductance is revised to (5.14). From (5.13) and (5.14), C_{Ts} and $C_{oss5,6}$ are critical for ZVS transitions. $C_{oss5,6}$ is a fixed parameter in the circuit once the devices are selected. The following section will illustrate the optimization of transformer design.

$$C_{oss\_LV\_eq} \approx C_{oss1} + C_{Tp} + n^2 \left(C_{Ts} + C_{oss5} \right) \tag{5.13}$$

$$L_m \le \frac{n^2 t_d}{8 f_s C_{oss\_LV\_eq}} \tag{5.14}$$

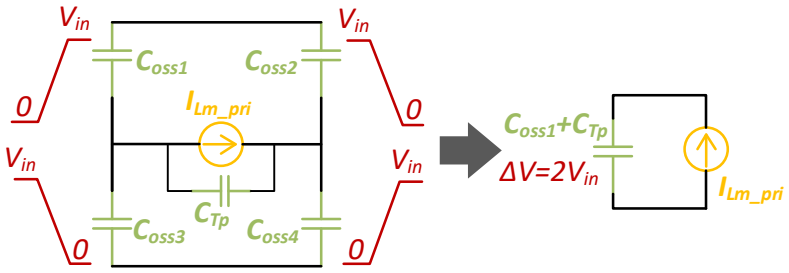


Figure 5.30. Conventional equivalent ZVS circuit model.

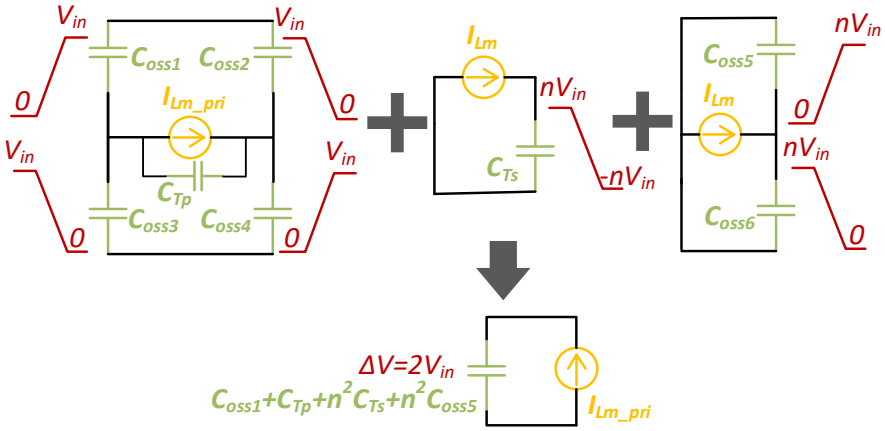


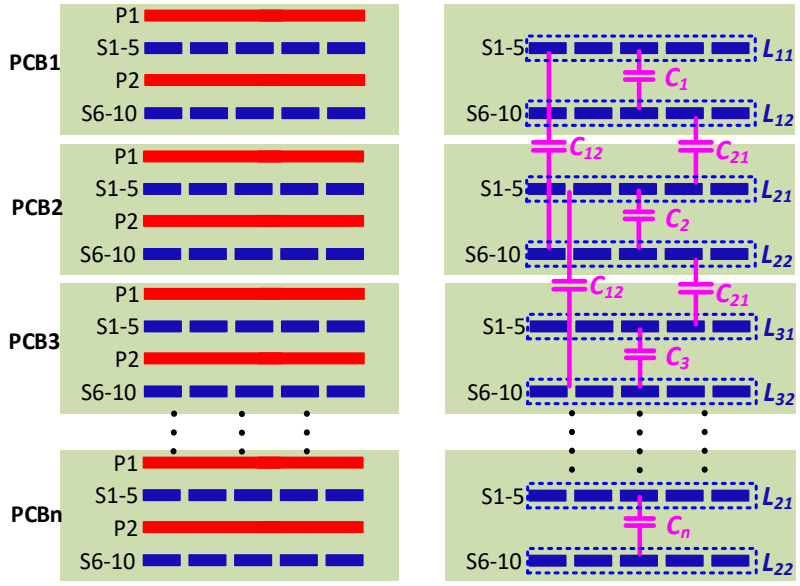
Figure 5.31. Revised equivalent ZVS circuit model for high step-up/down resonant converters.

For MHz designs, planar transformers are generally adopted in the pursuit of high-power density, since they offer low profiles, large surface area and tight winding coupling [120], [121]. However, the intra winding capacitance created by the PCB winding is much larger than litz-wire winding. This is even more severe on the HV side winding of high step-up/down converters, since the HV side winding contains more turns. Additionally, due to the thickness of coppers in PCBs, it is common to stack up multiple PCB windings to decrease current density. However, the stacked PCBs adversely increases the parasitic capacitances generated from board to board. Therefore, it is a trade-off between the

reduction of intra winding capacitance and enlargement of current capability for transformer optimization.

The capacitance created between two turns can be calculated from (5.15). Where ε is the permittivity of the insulation, A is the overlapping surface area of two turns and d is the distance between two turns.

$$C = \varepsilon \frac{A}{d} \tag{5.15}$$



(a) PCB windings stack up. (b) HV side windings with parasitic capacitors.

Figure 5.32. Designed PCB winding structure.

The total capacitance is the summation of n! capacitors for a single PCB winding with n turns. It is quite complicated and time consuming to estimate the intra winding capacitance even for a single PCB winding, not to mention multiple stacked boards. Taking the designed transformer in section 5.2.2 as an example, which has 2 turns at the LV side and 10 turns at the HV side. Figure 5.32 (a) shows the designed PCB winding structure,

where the single PCB is a 4-layer board containing 2-layer for the LV side winding and 2-layer for the HV side winding. The designed winding structure utilizes fully interleaving technology to minimize the proximity effect. There are 15 parasitic capacitors in total of the HV side winding for a single board. The capacitor number increases to 70 for two stacked winding boards.

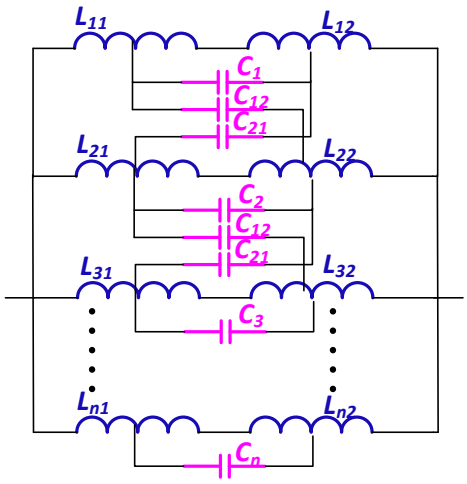


Figure 5.33. Simplified model of HV side winding with multiple boards.

A simplified model is proposed to estimate intra winding capacitance by neglecting certain small capacitors and treating the same-layer turns as a single object. According to (5.15), the capacitors between turns in the same PCB layer can be neglected since the overlapping area *A* is small due to thin copper thickness. Then, the turns in the same layer can be treated as a single object, and only the capacitors created between different layers should be considered, as shown in Figure 5.32 (b). In addition, under the case of multiple boards, only the capacitors created from adjacent boards are taken into consideration. The capacitance between two boards separated by large distances can be neglected. Therefore, the simplified model of HV side winding with multiple stacked boards is shown in Figure 5.33. The total capacitance of C_{Ts} is derived in (5.16), where *N* is the total number of PCB

boards. The complicated model of intra winding capacitance finally converts into the calculation of three capacitors, C_1, C_{12} and C_{21}.

$$C_{Ts} = NC_1 + (N-1)(C_{12} + C_{21}) \tag{5.16}$$

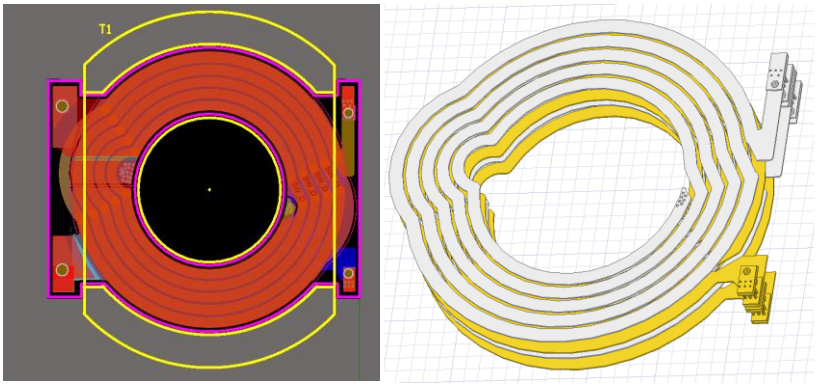


Figure 5.34. Imported 3D model in FEM simulation from PCB layout.

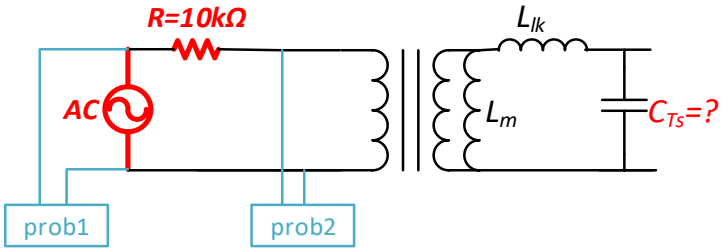


Figure 5.35. Testing of intra winding capacitance.

To verify the proposed simplified model, the capacitance of HV side winding is simulated in ANSYS. The 3D model used in the simulation is shown in Figure 5.34. It is also tested with method shown in Figure 5.35. The testing procedure is to adjust the frequency of the AC excitation until the voltage measured by prob2 is in phase with the voltage measured by prob1. Circuit impedance is purely resistive under this condition. The frequency of AC excitation is the resonant frequency of (L_m+L_{lk}) and C_{Ts}. Therefore, the measured intra capacitance C_{Ts_meas} can be expressed in (5.17).

$$C_{Ts\_meas} = \frac{1}{\left(2\pi f_{AC}\right)^2 \left(L_m + L_{lk}\right)} \tag{5.17}$$

Table 5.6 shows the verification of the proposed simplified modeling method. The calculation results match well with simulation and experiment results.

Table 5.6. Comparison of calculation, simulation and testing results of C_{Ts}.

C_{Ts}	*Calculation*	*Simulation*	*Experiment*
1 PCB (C_{Ts1})	12.1 pF	13.3 pF	15 pF
2 PCB (C_{Ts2})	37 pF	36 pF	38 pF
3 PCB (C_{Ts3})	61.86 pF	68.9 pF	60 pF

Table 5.7. Dead-time comparison with different C_{Ts}.

Parameters	C_{Ts1}	C_{Ts2}	C_{Ts3}
Dead-time	50 ns	70 ns	75 ns
Percentage of period	10%	14%	15%

The effects of parasitic capacitance on the ZVS transitions during the dead-time period is simulated with three separated C_{Ts} parameters listed in Table 5.6**.** The simulation waveforms are shown in Figure 5.36. Table 5.7 summarizes the dead-time percentages of the entire period with different C_{Ts} parameters. The effective period of energy delivery will be reduced with a larger C_{Ts}. Additionally, the desired value of resonant capacitance is greatly reduced compared with the conventional design method. This is not only due to the unneglectable parasitic inductance in LV side, but also because of the change in resonant period. Unlike kHz designs where the resonant period almost equals to the switching period, the dead-time period must be subtracted from the switching period due to the large

ratio of dead-time period to switching period when designing the resonant parameters at MHz switching.

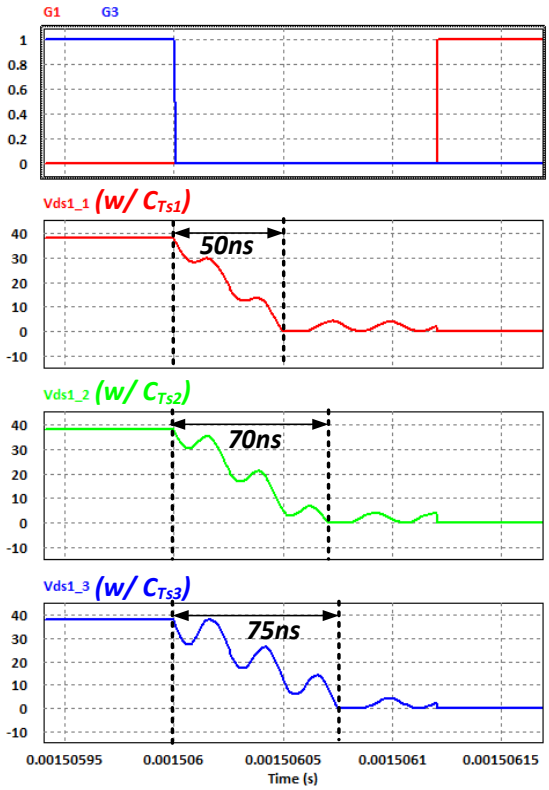
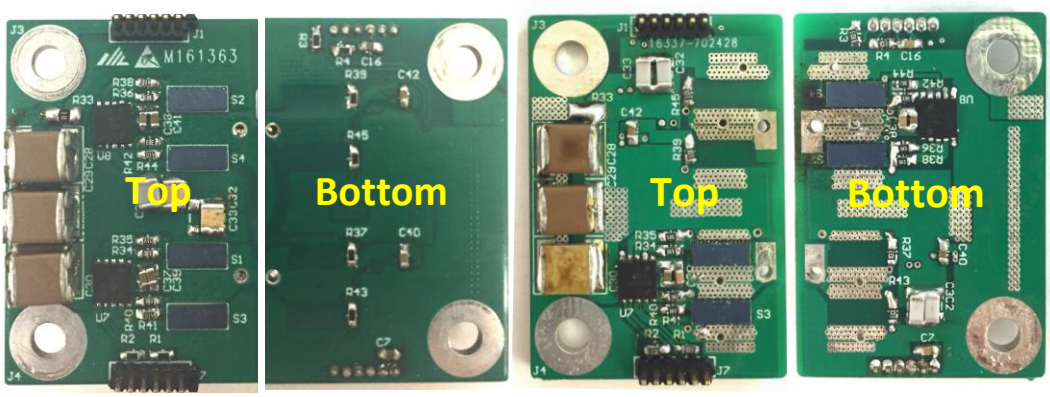


Figure 5.36. Circuit simulations of ZVS transitions with different C_{Ts}.

5.3.3 Circuit Design Experimental Verifications

Multiple 300-W prototypes were built and compared to verify the design and optimization of reducing parasitic effects at MHz operation. Figure 5.37 shows the hardware photograph. The summary of parameters is shown in the Table 5.3. Table 5.4 compares the design of circuit parameters with and without the effects of circuit parasitics. After considering the parasitic inductances of LV side, resonant inductance increases from 460 nH to 835 nH. On the other hand, considering both the dead-time period and the change of resonant inductance, each resonant capacitor reduces from 27.5 nF to 10 nF. Moreover,

compared with the traditional design method, L_m reduces from 80 μH to 60 μH to the charge and discharge of the HV side parasitic capacitances besides the output capacitances of LV side switches.



(a) Full-bridge layout 1. (b) Full-bridge layout 2.

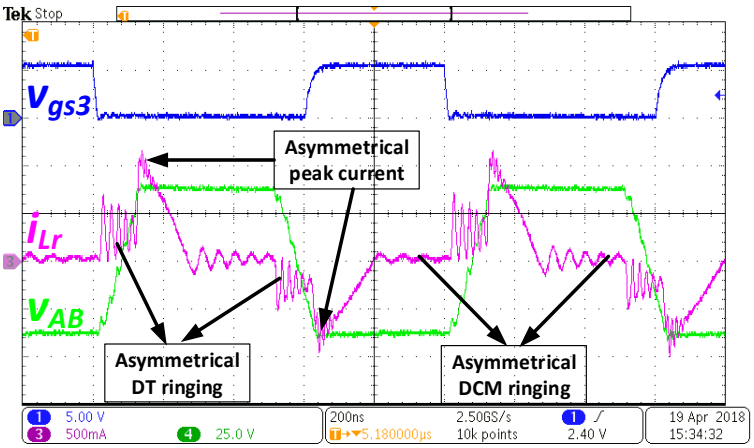
Figure 5.37. Hardware photograph.

Table 5.8. Parameters of passive components w/o and w/ considering parasitics.

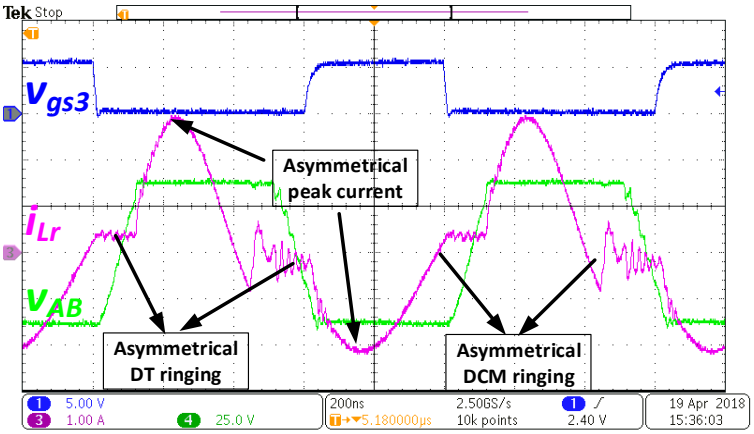
Parameters	L_{r_eq}	$C_{r1,2}$	L_m
w/o considering parasitics	460 nH	27.5 nF	93 μH
w considering parasitics	835 nH	10 nF	60 μH

Figure 5.37 (a) shows the PCB with full-bridge layout 1, and Figure 5.38 shows its testing waveforms under light and heavy load conditions. The peak resonant current reaches 1.2-A during the positive half cycle, while it is only 0.8-A at negative half cycle, in Figure 5.38 (a). Moreover, the ringing during both the dead-time period and discontinuous conduction mode (DCM) period are asymmetrical between positive and negative half cycles which matches with the analysis. This phenomenon is more severe at a 200-W load condition, as shown in Figure 5.38 (b). The peak resonant current of the

positive half cycle is almost 3-A, while the negative half cycle is only 2.25-A. The asymmetrical issues during dead-time period and DCM period are even more severe.



(a) At 30-W condition.

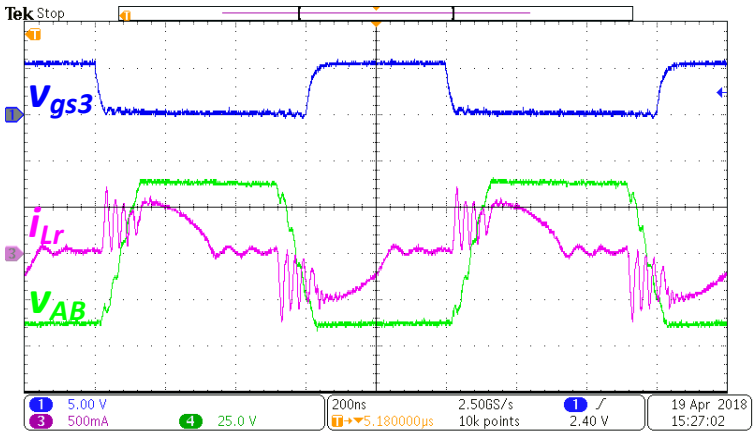


(b) At 200-W condition.

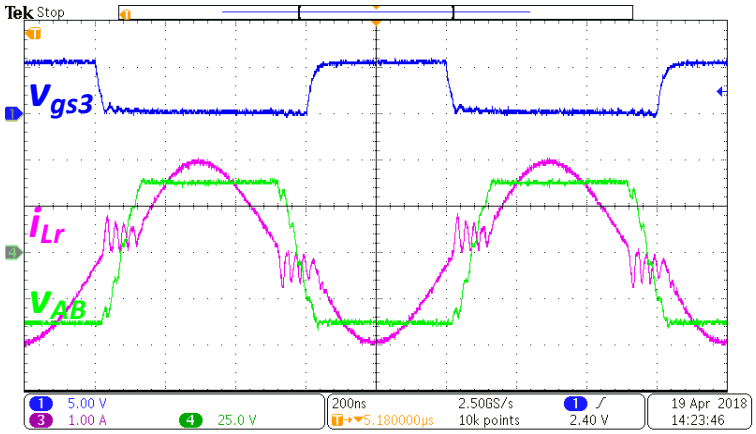
Figure 5.38. Experimental steady-state waveforms with full-bridge layout 1: gate-to-source voltage of S_3, v_{gs3}, resonant current, i_{Lr}, and voltage across LV side winding of the transformer, v_{AB}.

Figure 5.37 (b) shows the PCB with full-bridge layout 2. The testing waveforms under light and heavy load conditions are shown in Figure 5.39. The current waveforms are both symmetrical under 30-W and 200-W load conditions. According to Figure 5.38 and Figure 5.39, the current stress reduces from 1.2 to 0.75 A at 30-W condition and it

reduces from 3 to 2 A at 200-W condition when the PCB layout is revised from Figure 5.37 (a) to (b).



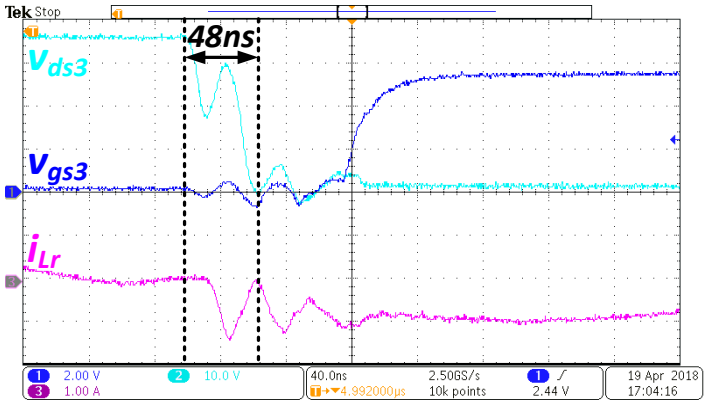
(a) At 30-W condition.



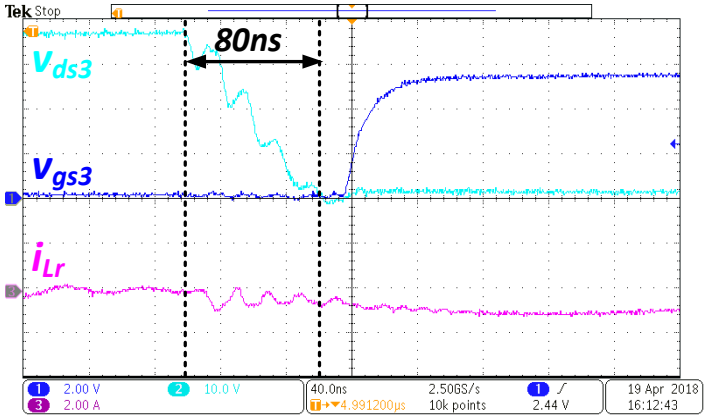
(b) At 200-W condition.

Figure 5.39. Experimental steady-state waveforms with full-bridge layout 2: gate-to-source voltage of S_3, v_{gs3}, resonant current, i_{Lr}, and voltage across LV side winding of the transformer, v_{AB}.

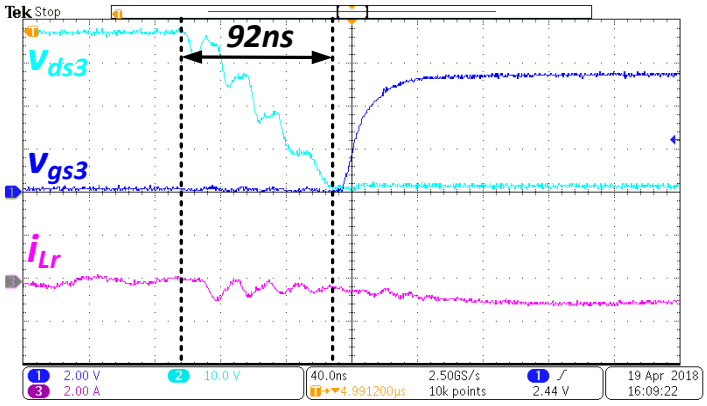
Figure 5.40 verifies the ZVS transitions with different values of C_{Ts}. Figure 5.40 (a), (b) and (c) are the experimental waveforms with single PCB winding, two stacked PCB windings and three stacked PCB windings for transformer, respectively. It takes 48 ns, 80 ns and 92 ns to achieve ZVS for three cases.



(a) ZVS turn-on of S_3 with C_{Ts1}.

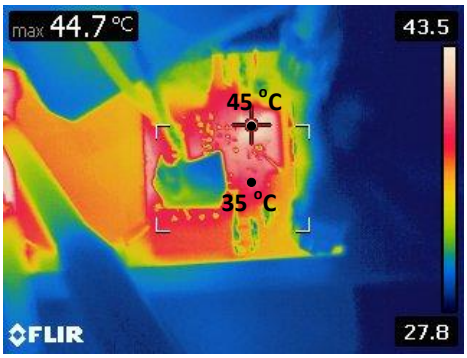


(b) ZVS turn-on of S_3 with C_{Ts2}.

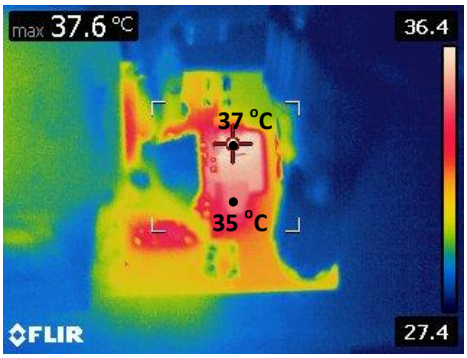


(c) ZVS turn-on of S_3 with C_{Ts3}.

Figure 5.40. Turn-on transition of input side switches: gate-to-source voltage of S_3, v_{gs3}, drain-to-source voltage of S_3, v_{ds3}, and resonant current, i_{Lr}.

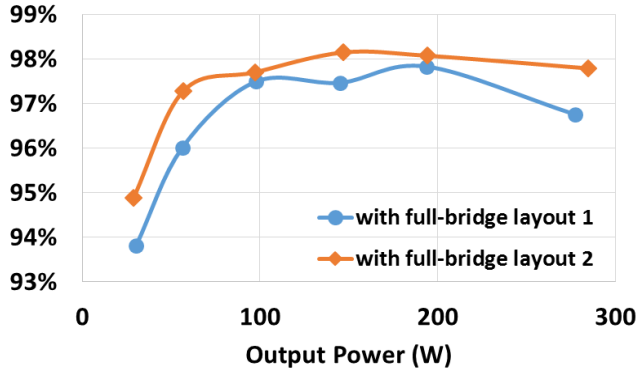


(a) With full-bridge layout 1.

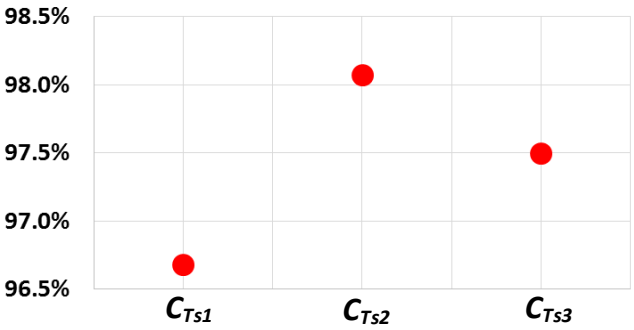


(b) With full-bridge layout 2.

Figure 5.41. Thermal images of HV side switches.



(a) Efficiency comparsion between full-bridge layout 1 and layout 2.



(b) Efficiency comparsion with C_{Ts1}, C_{Ts2} and C_{Ts3} @ 75% load.

Figure 5.42. Efficiency testing with different full-bridge layouts and different PCB winding structures.

Under natural convection cooling, thermal testing images of HV side under full load condition are shown in Figure 5.41, where (a) and (b) are with full-bridge layout 1 and 2 respectively. The temperatures of the two switches are marked in the pictures. The

temperature difference between two switches with full-bridge layout 1 is up to 10 ^{o}C, however, the temperatures of two switches with full-bridge layout 2 are almost the same. The uneven thermal distribution with layout 1 increases the thermal stress.

The power stage efficiency is measured with different full-bridge based layouts and different PCB winding structures. Figure 5.42 (a) shows the efficiency curves with two stacked PCB. The efficiency of full-bridge layout 1 with asymmetrical current is lower, especially under 10%, 20%, 50%, and 100% load conditions. With symmetrical full-bridge layout, the efficiency can improve up to 1.5%. The peak efficiency of full-bridge layout 2 reaches 98.2%. Since 75% load condition takes highest percentage of CEC efficiency for converters in PV applications, the efficiency with different C_{Ts} is compared under 75% load condition. According to Figure 5.42 (b), the efficiency-based optimized design is the C_{Ts2} case, which is the case of two stacked PCBs. The efficiency reaches 98.1% at this condition.

5. 4 Summary

This chapter presents the design of proposed converter at 1-MHz switching frequency for the pursuit of high-power density. Compared with 140-kHz design, the converter volume of 1-MHz design can reduce more than 70%, while the CEC efficiency only drops 0.8% at the nominal input voltage condition.

At 1-MHz switching frequency, the circuit parasitic components will have significant impact on the circuit operation. This chapter also explores the effects of parasitic components on the circuit steady-state operations in resonant converters with high

transformer turns ratio at MHz switching frequency, as well as the circuit design techniques to reduce the parasitic effects. Key findings are discussed as follows.

(1) Parasitic inductances in LV side and parasitic capacitances in HV side can greatly impact the circuit operation due to n^2 relationship between the LV and HV sides. The reflected values are comparable to the original resonant *LC* circuit parameters for MHz designs.

(2) The conventional full-bridge PCB layout with two legs on the same layer of the board is not suitable for MHz designs due to the asymmetrical parasitic inductances in the PCB traces. It will cause unbalanced current between the positive and negative half cycles and further hurt the power conversion efficiency. The PCB layout with one leg on the top side and the other leg on the bottom side is a good way to balance the loop parasitic inductances.

(3) Parasitic inductance also involves in the design of resonant parameters. The resonant inductor is no longer the leakage inductance of the transformer itself under the case of no external inductor. It should contain the leakage inductance of the transformer and the equivalent parasitic inductance reflected from the LV side.

(4) Intra winding capacitance across the HV side winding of the planar transformer is large enough to increase the magnetizing circulating energy and affect ZVS transitions. Therefore, it is a trade-off between a reduction in intra winding capacitance and enlargement of current capability for transformer optimization. Moreover, a simplified model to estimate intra winding capacitance is proposed and verified with FEM simulation and experiments.

(5) Because of large parasitic capacitances, the dead-time period occupies a large percentage of entire switching period in MHz operations. The energy delivery period is shortened as the resonant frequency is no longer equal to switching frequency. Therefore, the designed values of resonant capacitance are reduced compared with conventional kHz design.

Chapter 6 Conclusions and Future Works

6.1 Conclusions

With the limited availability of fossil fuels and serious problems of environment pollutions, renewable energies receive more and more attractions. Solar energy is one of the most promising renewable energies. Modular power conversion system provides desirable features on the superior MPPT efficiency, scalability, fault tolerance and feasible both for utility grid and dc microgrid. This dissertation focuses on the dc-dc power converter in the modular PV architectures which can be applied as a parallel-type dc power optimizer for inverter connection or in a dc microgrid system, or a front-end dc-dc stage of a two-stage micro-inverter.

With the availability of wide bandgap power semiconductor devices, the power converter has more potentials to achieve higher efficiency and higher power density. Since the wide bandgap devices have desirable features of low on-state resistance, small junction capacitance and high switching speed, the device loss can be reduced and the operating switching frequency can be increased. Therefore, these wide bandgap devices can bring the chance for the next generation power converters. This dissertation studies the application of wide bandgap devices to the dc-dc power converter for the modular PV applications in order to improve the power conversion efficiency and power density.

Considering the output characteristics of PV module, the dc-dc converter that connects between single PV module and high voltage bus should have high voltage step-up ratio, the capability of wide input range regulation, and the ability to maintain high-

efficiency over wide range operation. Additionally, isolation is an optional requirement, which can isolate the PV modules from the high voltage bus and protect the PV modules during the fault conditions.

In order to address the innovative breakthroughs of the dc-dc converter for parallel-type modular PV applications, the contributions of this dissertation are summarized as follows.

Firstly, Chapter 2 gives a literature review of the previously proposed isolated dc-dc topologies that are suitable for parallel-type modular PV applications. There are two categories, where one is the PWM-based converter and the other one is the resonant converter. The main limitations for the PWM-based converters are the low efficiency because of the leakage energy of transformer and hard-switching transitions. As for the resonant converters, the leakage energy of transformer can be fully utilized and the soft-switching features are achieved. However, they either lack the capability of wide range operation or have significantly dropped efficiencies when operating point is far away the resonant point. Hybrid-mode operation on the resonant converters has ability to extend the operating range while keeping on the benefits of highly-efficient resonant converters, which is adopted in the proposed converter of this dissertation.

Secondly, the characteristics of GaN device are studied in Chapter 3. Since the normally-on structure is not desirable considering the reliability, the GaN device turns into a normally-off device with the methods of adopting gate or incorporating a low-voltage Si MOSFET in commercial released products. A 650-V GaN device from GaN Systems Inc is evaluated with the testing of buck converter and SRC. Under the testing of hard-switching buck converter, the switching transitions and switching loss are evaluated. The

switching speed is much faster than the conventional Si MOSFETs, which results in low switching loss. Even though the device has reduced switching loss, the switching loss still dominates the overall loss under the hard-switching condition at high switching frequency conditions. The characteristic of reverse conduction is evaluated by the low side switch of buck converter. The reverse conduction mode behaves as a “diode” whose “forward voltage” is much higher than the body diode of Si MOSFET. However, zero reverse recovery of “diode” can be achieved. Under the testing of soft-switching SRC, the output parasitic capacitance of GaN device is estimated by the measurement during ZVS switching transition, which is much smaller than Si MOSFET.

Thirdly, an isolated GaN-based dc-dc converter with an active-boost-rectifier and a novel modulation scheme is proposed for parallel-type modular PV applications. The proposed converter has hybrid operating modes under different input conditions: a buck converter with high input voltage and a boost converter with low input voltage. Under nominal input voltage, the converter operates as a pure SRC to acquire the maximum power delivering. This dissertation focuses on the low input voltage conditions, since the methods to step down voltage are conventional and introduced in the Chapter 2. The active-boost-rectifier is the configuration of the secondary side circuit, which merges a Boost circuit and a voltage-doubler rectifier. Incorporating with the proposed double-pulse duty cycle modulation method, the switches in the active-boost rectifier can not only serve as the synchronous rectification but also achieve the voltage boost function. Therefore, the proposed converter not only keeps the benefits of the highly-efficient SRC converter, but also achieves a higher voltage gain than SRC and a wide range regulation ability without adding additional switches while operating under fixed-frequency condition. The primary

side switches achieve ZVS and the secondary side switches achieve ZCS regardless of input voltage or output power. The fixed-frequency modulation not only simplifies the design and control but also keeps low circulating energy through converter. The converter design is optimized at the nominal input voltage condition in terms of magnetics design, dead-time optimization, GaN power device selection and etc. EPC2021 from EPC Inc and GS66502B from GaN Systems Inc are selected for the primary and secondary side switches respectively. A 300-W hardware prototype is designed and optimized to verify the performance of the proposed converter and modulation method. The converter achieves a peak efficiency of 98.9% and a CEC weighted efficiency of 98.7% under nominal input voltage condition.

Finally, to pursue the high-power density of converter, the proposed converter is designed at 1-MHz switching frequency in Chapter 5. The key of 1-MHz design is the magnetics design. With the assistance of FEM simulations, a planar transformer with a dimension of 33.2 mm of length, 23.7 mm of width and 11.1 mm of height is designed. Differently with 140-kHz design, the leakage inductance of 1-MHz transformer can be utilized as the entire resonant inductance, which gets rid of the need of the external inductor. Considering the ac effects at high frequency, the PCB structure design is also taken into consideration. 4-layer PCB with 3 oz copper in each layer is selected through the FEM simulation and optimization. Compared with 140-kHz design, the volume of 1-MHz design can reduce more than 70%, while the CEC efficiency only drops 0.8% at the nominal input voltage condition.

Additionally, the parasitic components have significant effects on the circuit operation in MHz switching frequency, unlike the kHz switching. This phenomena is

aggravated on high ratio step-up or step-down isolated converters because the parasitic capacitances/inductances are square times the turns ratio of the transformer when reflecting from HV/LV side to LV/HV side. Chapter 5 also explores the effects of parasitic components on the circuit operations at MHz switching frequency, as well as the circuit design techniques to reduce the parasitic effects. The conventional full-bridge PCB layout with two legs on the same layer of the board is no longer suitable since this method will induce the asymmetrical parasitic inductances in the PCB traces between positive and negative half switching cycles. The asymmetrical parasitic inductances will cause unbalanced current and hurt the power conversion efficiency as well. The improved layout with one leg on the top side and the other leg on the bottom side can ensure the balanced the loop parasitic inductances. Moreover, the resonant inductance in the secondary side should be the summation of the leakage inductance of the transformer and the equivalent parasitic inductance reflected from the LV side. The parasitic capacitances of HV side involve in the ZVS transitions and increase the required magnetizing circulating energy. Therefore, it is a trade-off between a reduction in intra winding capacitance and enlargement of current capability. Because of large parasitic capacitances, the dead-time period occupies a large percentage of entire switching period in MHz operations. When designing the resonant capacitor, the energy deliver period should be the difference between entire switching period and dead-time period.

6.2 Future Works

The development of wide bandgap devices is rapid nowadays. More and more semiconductor companies are involving in the market of GaN devices, and more devices are already released commercially with lower on-state resistance or smaller junction

capacitances. Further improvement on the converter efficiency can be done with the utilization of recently released devices. Moreover, the gate of GaN device is sensitive to the noise, especially for eGaN devices, since the threshold gate voltage is pretty low. So it is critical for the PCB layout to minimize the parasitic inductances in the drive loop and the source terminal of device. It is a trend that single or half-bridge GaN device integrates with gate driver into a module to minimize the parasitic loop inductances and improve power density. There are some released products in the market, such as from Texas Instruments, Navitas Semiconductor and etc. More researches can be explored by using the integrated GaN modules.

This dissertation mainly pays attention to the hardware improvement of dc-dc power converter for modular PV applications. A PI controller is implemented for the close loop control. In the future, the precise model of the proposed converter should be derived and the controller with higher bandwidth should be designed to gain fast responses and transitions. Moreover, the control algorithm for MHz switching converters becomes different, since the calculations of the system variables cannot be completed in a single switching period in DSP. It deserves to explore the optimization of control diagram in MHz switching converters in the future.

Another consideration is the system-level control improvement such as MPPT techniques. MPPT algorithm is important for capturing and delivering the solar energy. The total efficiency of dc-dc power conversion is the multiplying of MPPT efficiency and power conversion efficiency. Currently, the basic MPPT method is utilized which is not fast and accurate enough.

Last, more research can be made on the system-level integrations, such as the communications between different units, as well as the control panel. Wifi module is a good choice to achieve the wireless and long distance communications, however, the commercial wifi module usually takes a large space. Thus, the research on this topic is worth to be investigated. Additionally, since the proposed converter will serve as dc optimizer or the front-end dc-dc stage of micro-inverter, it will interface to the ac or dc grid. Some issues involves in the distributed power system need to be investigated, such as the protections of solar converters, the influence of grid perturbations on solar converters, and etc.

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