Modeling and Controller Design of a Bidirectional Resonant Converter Battery Charger

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ABSTRACT In this paper, a controller design methodology is proposed for a *CLLLC*-type bidirectional resonant converter. The soft switching of all devices in this topology and the very high operating frequency lead to increased overall system efficiency. However, the dynamic nature of this converter is highly dependent on loading conditions, which proves challenging when designing the voltage and current closed-loop controllers. System instability is mainly due to the high-Q resonant peaking, which is observed in the open-loop bode-plots. In this paper, the controller design methodology is proposed, which accounts for the dynamics behavior due to load variations. The controller stability will be evaluated against the entire range of operating switching frequency. Both battery charging and regeneration modes will be described and analyzed. The focal contribution of this paper will focus on defining the worst operating scenarios for the converter using system-level modeling and analysis. In addition, the controller will be defined based on these operating points. To validate and verify the controller design methodology proposed, a 3.5-kW converter is designed with the appropriate output voltage and current loop controllers. The step response verified a stable system designed and thus proving the proposed controller design methodology.

INDEX TERMS DC-DC power converters, bidirectional power flow, resonant converters, control design, battery charger, closed-loop systems.

I. INTRODUCTION

Electric vehicles (EVs) have recently become increasingly popular, and penetration levels dramatically increased, mainly due to the many advancements in enabling technological aspects of manufacturing, resulting in greener and more reliable EVs [1]. EV technology development compliments the efforts being exerted on techniques to minimize vehicle fuel consumption, ranging from Eco-driving education to advanced engine control techniques [2], [3], and even advanced efforts were proposed on cyber-physical predictive control schemes to minimize vehicle fuel consumption [4].

EVs are considered green when powered from renewables, which is the main theme of new infrastructure support installations. The energy storage system (ESS) is key element to EVs, and usually it defines the capabilities of the EV [5]. Defining and optimizing the ESS continues to be of huge interest to researchers and manufacturers. Lithium-ion batteries represent the main choice thus far due to its advantages in terms of energy density and durability [6]. Hybridizing options with super-capacitors and fuel cells were investigated

and reported as well to enhance the operational characteristics and minimize the ESS sizing [7]. Accompanying energy and power management controllers and algorithms were proposed to regulate and facilitate the hybrid systems [8]–[11].

As vital as it is for the ESS, charging technologies are of utmost importance in this regard and are in the focus of this work. On-board EV battery chargers can be either conductive [12]–[20] or inductive [20]–[27]. A front-end stage is essential for any on-board charger, in addition to the required regulating dc-dc power stage that manages the bidirectional energy transfer between the battery and the EV. A wide range selection of dc-dc converters have been adapted for EV battery management systems. Due to their higher efficiency and performance, resonant converters have become the topologies of choice. In addition to that, resonant converters have higher operating switching frequencies that are enabled by advanced semiconductor switches industry [12]–[19], [25]–[28]. One of the most appealing features of resonant converters is the ability to implement soft-switching in all switches, which results in the minimization of switching

energy losses, in addition to reduced electromagnetic interference.

Control implementation in resonant converters' topologies is completely different from the traditional PWM converters wherein the output filter's cutoff frequency is much lower than that of the switching frequency (usually a ratio of 10 is used). In PWM converters, different modeling methods such as state-space averaging [29], [30] and PWM switch model [31]–[33] techniques where they are utilized to formulate the average converter model over one switching period to capture the dynamic behavior of the converter. These methods cannot be directly used in resonant converters' dynamic modeling since the switching frequency is close to the tank circuit resonant frequency. Several methods have been proposed for the derivation of the small-signal models of resonant converters in literature [34]–[41]. However, most of these methods are too complex [34], [35] or not accurate enough [36]–[40]. The Generalized State-Space Averaging (GSSA) method [42], [43] and the envelope modeling method [44] are tools used to predict the dynamics of resonant converters. These techniques are not suitable for higher order converters, as they become very complex and less accurate. The Extended Describing Functions (EDF) is another time-domain and frequency-domain analysis modeling technique, which uses multivariable describing functions to approximate the non-linear terms, [41], [45]–[48]. This method is accurate and not as complex. Circuit simulation softwares and CAD tools can be used as well to generate the open-loop bode-plots to design compensators [49], [25].

In this paper, a controller design methodology for a *CLLLC*-type resonant converter is proposed, which is valid for a wide range of input and output voltages. As the dynamics of resonant converters change due to changing loading conditions, it is essential that the controller is properly designed, otherwise, at some operating points, the closed-loop system might become unstable. Defining the worst case operating condition scenario is the main challenge when targeting a globally stable controller design. Frequency response will be used to define the worst case operating scenario and to design the stable controller. Both, voltage and current loops will be designed and the stability guarantee margins will be shown. The steady-state and the small-signal models derivation for the IPT system [47] are applicable for this converter as well. Hardware prototype for a 3.5kW system is designed and built to validate the design methodology proposed in this manuscript, and experimental test results prove the effectiveness of the proposed approach. This work has been presented initially at [50] and an extension and detailed analysis is included here as well.

II. FUNDAMENTAL ANALYSIS AND CONVERTER MODELING

A. CONVERTER POWER STAGE

The *CLLLC* resonant converter is shown in Fig. 1. The converter is capable of bidirectional operation. The high
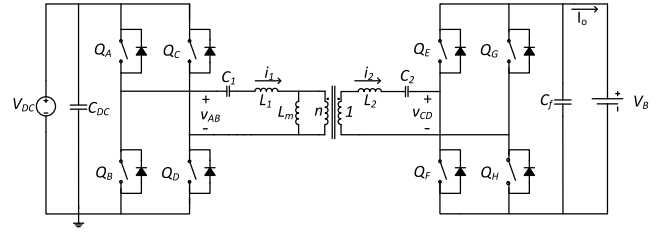

FIGURE 1. Bidirectional resonant converter circuit topology.

frequency signal generated by the primary stage is filtered by the resonant tank circuit to only pass the fundamental component to the secondary side, where it is rectified before being supplied to the load. The transformer provides galvanic isolation, and turns ration may be set to enhance the conversion ratio if required.

B. STEADY-STATE AND SMALL-SIGNAL MODELS

Fig. 2 shows the equivalent circuit representation for the *CLLLC* converter with the battery load represented by a dynamic resistance [47]. The dynamic analysis shown in [47] will be applied here. The large-signal, steady-state and small-signal models for the IPT system are formulated based on Extended Describing Functions (EDF). This basically elevates the harmonic balance to derive the system dynamics. Assuming that all state variables are described with sinusoidal functions as can be excluded from Fourier series analysis, harmonic balance can be applied at the fundamental frequency ω_s. (1) to (8) describe the derived model.

$$v_{AB} = \frac{4\,V_{DC}}{\pi} \cdot \sin\left(\omega_s t\right) \tag{1}$$

$$v_{CD} = sign\left(i_2\right) \cdot V_o \tag{2}$$
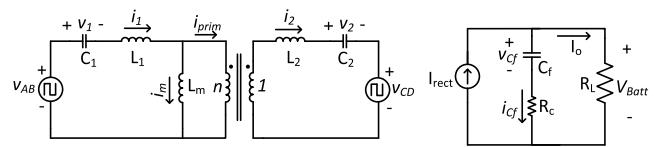
$$i_{rect} = |i_2| \tag{3}$$

FIGURE 2. Equivalent circuit for the CLLLC converter.

The voltages and currents can be approximated at the fundamental frequency using Fourier series analysis as follows:

$$i_1 = I_{1s} \cdot \sin\left(\omega_s t\right) + I_{1c} \cdot \cos\left(\omega_s t\right) \tag{4}$$

$$v_1 = V_{1s} \cdot \sin\left(\omega_s t\right) + V_{1c} \cdot \cos\left(\omega_s t\right) \tag{5}$$

$$i_2 = I_{2s} \cdot \sin\left(\omega_s t\right) + I_{2c} \cdot \cos\left(\omega_s t\right) \tag{6}$$

$$v_2 = V_{2s} \cdot \sin\left(\omega_s t\right) + V_{2c} \cdot \cos\left(\omega_s t\right) \tag{7}$$

The steady-state equations are derived as (8) and (9), as shown at the bottom of the next page.

The output current and voltage at the steady-state can be calculated as in (10) and (11).

$$V_o = V_{Cf} = \frac{2}{\pi} I_{pk} R_L \qquad (10)$$

$$I_o = \frac{V_o}{R_L} = \frac{2}{\pi} I_{pk}$$

$$I_{pk}^2 = (I_{2s})^2 + (I_{2c})^2 \qquad (11)$$

The converter output voltage and current versus the operating switching frequency curves are plotted using (10) and (11). The linearized small-signal model derived from (8) is (12) and (13), as shown at the bottom of the next page.

The variables $K_1 \sim K_{22}$ are listed in the appendix. The ($\wedge$) stands for the small signal perturbation from the linearization process. The Transfer functions can be found using Equations (12) and (13) as following:

$$G_p (s) = C \cdot [sI - A]^{-1} \cdot B = \begin{bmatrix} G_{vf} (s) & G_{vvg} (s) & G_{vd} (s) \end{bmatrix} \qquad (14)$$

Both, the frequency and the phase-shift control are included in the small-signal model in (12) and (13). With the phase-shift control, the ZVS range for the primary side switches depend on the series leakage inductance. Thus, ZVS operation cannot be guaranteed at all load conditions if phase shift control is adapted. If frequency control is utilized, then ZVS can be guaranteed at all line and load conditions if the

primary-side current lags the primary-side bridge voltage. Therefore, frequency control will be adapted here.

C. SMALL-SIGNAL MODEL VERIFICATION

The transfer functions can be deduced from (14), where they are used to design the closed loop controllers of the current and voltage, given that the control input is the frequency. So, the control-to-output current transfer function, $G_{if}(s)$ and the control-to-output voltage transfer function, $G_{vf}(s)$ are derived in both *BCM* and *RM*. In Fig. 3, the voltage gain is shown versus the switching frequency for the converter with a resistive load R_L of 45 Ω. The remaining circuit parameters are listed below:
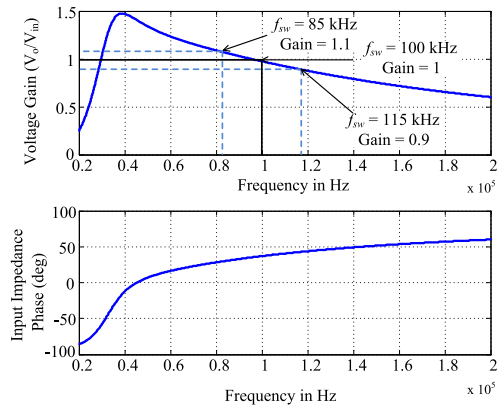
FIGURE 3. Voltage gain versus switching frequency.

$$B_{st} = A_{st} \cdot X_{st}$$

$$A_{st} = \begin{bmatrix} 1 & \dfrac{L_{eq2}}{L_{eqm}} & 0 & \dfrac{L_{eq2} R_e}{L_{eqm}} & 0 & 0 & -\Omega_s L_{eq2} & 0 \\ 1 & \dfrac{L_{eqm}}{L_{eq1}} & 0 & \dfrac{L_{eqm} R_e}{L_{eq1}} & 0 & 0 & 0 & -\Omega_s L_{eqm} \\ 0 & 0 & 1 & 0 & \Omega_s C_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & \Omega_s C_2 & 0 & 0 \\ 0 & 0 & \Omega_s L_{eq2} & 0 & 1 & \dfrac{L_{eq2}}{L_{eqm}} & 0 & \dfrac{L_{eq2} R_e}{L_{eqm}} \\ 0 & 0 & 0 & \Omega_s L_{eqm} & 1 & \dfrac{L_{eqm}}{L_{eq1}} & 0 & \dfrac{L_{eqm} R_e}{L_{eq1}} \\ -\Omega_s C_1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & -\Omega_s C_2 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \qquad (8)$$

$$B_{st} = \begin{bmatrix} V_e & V_e & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T$$

$$X_{st} = \begin{bmatrix} V_{1s} & V_{2s} & I_{1s} & I_{2s} & V_{1c} & V_{2c} & I_{1c} & I_{2c} \end{bmatrix}^T$$

$$V_e = \frac{4}{\pi} \cdot V_{DC}, \quad R_e = \frac{8}{\pi^2} R_L, \quad \Omega_s = 2 \cdot \pi \cdot f_{sw}$$

$$L_{eq1} = \frac{n^2 L_{11} L_{22} - L_m^2}{n^2 L_{11}}, \quad L_{eq2} = \frac{n^2 L_{11} L_{22} - L_m^2}{n^2 L_{22}}$$

$$L_{eqm} = \frac{n^2 L_{11} L_{22} - L_m^2}{n L_m}.$$

$$X_{st} = A_{st}^{-1} \cdot B_{st} \qquad (9)$$

TABLE 1. Converter Circuit Parameters

(L_1, L_2)	(L_m)	(C_1)	(C_2)	(n)	(C_f)
20 µH	100 µH	136 nF	200 nF	1	30 µF

The converter gain is unity at the primary side series resonant frequency f_{ser} of 100 kHz, boost operation for $f_s > f_{ser}$, and buck operation for $f_s < f_{ser}$. Since, the voltage-controlled oscillator (VCO) is implemented in the DSP, it cannot be perturbed and hence, it is not possible to measure the open-loop
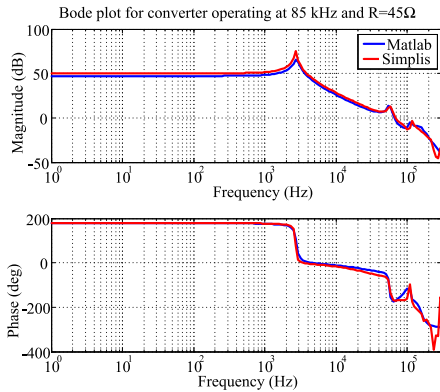

FIGURE 4. Open-loop of $G_{vf}(s)$, for the converter operating at $f_s = 80kHz$.
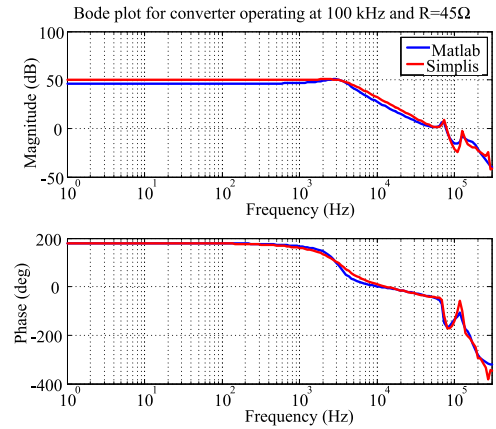

FIGURE 5. $G_{vf}(s)$ of the converter at unity gain operation at $f_S = 100kHz$.

transfer function. However, circuit simulation software can be used to carry the AC analysis [22].The open-loop bode-plot will be compared with the simulation results using SIMPLIS to validate the model in (12-13) as show in Figs. 4-6, where the MatLab generated plots are the predicted responses shown in (12-13). It is clearly shown that the model in (12-13) is validated at different switching frequencies.

III. WORST-CASE SCENARIOS FOR CONTROLLER DESIGN
The small-signal model in (12) and (13) will be used to design both the voltage and current controllers for

$$\frac{d}{dt}\hat{x} = A \cdot \hat{x} + B \cdot \hat{u}$$
$$\hat{y} = C \cdot \hat{x}$$

$$A = \begin{bmatrix}
0 & \Omega_s & -K_1 & K_2 & \frac{-1}{L_{eq2}} & 0 & \frac{-1}{L_{eqm}} & 0 & -K_3 \\
-\Omega_s & 0 & K_{11} & -K_{12} & 0 & \frac{-1}{L_{eq2}} & 0 & \frac{-1}{L_{eqm}} & -K_{13} \\
0 & 0 & -K_6 & \Omega_s + K_7 & \frac{-1}{L_{eqm}} & 0 & \frac{-1}{L_{eq1}} & 0 & -K_8 \\
0 & 0 & -\Omega_s + K_{14} & -K_{15} & 0 & \frac{-1}{L_{eqm}} & 0 & \frac{-1}{L_{eq1}} & -K_{16} \\
\frac{1}{C_1} & 0 & 0 & 0 & 0 & \Omega_s & 0 & 0 & 0 \\
0 & \frac{1}{C_1} & 0 & 0 & -\Omega_s & 0 & 0 & 0 & 0 \\
0 & 0 & \frac{1}{C_2} & 0 & 0 & 0 & 0 & \Omega_s & 0 \\
0 & 0 & 0 & \frac{1}{C_2} & 0 & 0 & -\Omega_s & 0 & 0 \\
0 & 0 & K_{17} & K_{18} & 0 & 0 & 0 & 0 & -K_{19}
\end{bmatrix}$$

$$B = \begin{bmatrix}
\omega_o I_{1c} & -\omega_o I_{1s} & \omega_o I_{2c} & -\omega_o I_{2s} & \omega_o V_{1c} & -\omega_o V_{1s} & \omega_o V_{2c} & -\omega_o V_{2s} & 0 \\
K_4 & 0 & K_9 & 0 & 0 & 0 & 0 & 0 & 0 \\
K_5 & 0 & K_{10} & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}^T$$

$$C = \begin{bmatrix} 0 & 0 & K_{20} & K_{21} & 0 & 0 & 0 & 0 & K_{22} \end{bmatrix}$$

$$\hat{x} = \begin{bmatrix} \widehat{i_{1s}} & \widehat{i_{1c}} & \widehat{i_{2s}} & \widehat{i_{2c}} & \widehat{v_{1s}} & \widehat{v_{1c}} & \widehat{v_{2s}} & \widehat{v_{2c}} & \widehat{v_{Cf}} \end{bmatrix}^T$$

$$\hat{u} = \begin{bmatrix} \widehat{\omega_n} & \widehat{v_g} & \widehat{d} \end{bmatrix}^T, \quad \hat{y} = \hat{v_o}, \omega_o = \frac{1}{\sqrt{L_1 C_1}}$$

(12)

(13)

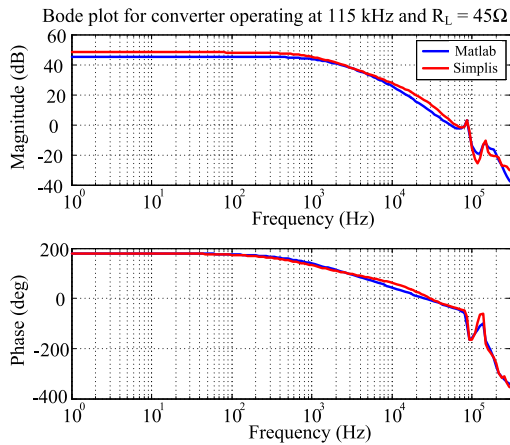Bode plot for converter operating at 115 kHz and $R_L = 45\Omega$

FIGURE 6. Bode plot of $G_{vf}(s)$ in the buck mode at $f_s = 115kHz$.

TABLE 2. Converter Design Parameters

Component	Value	Component	Value
V_{DC}	400 V	C_{DC}	1.8 mF
L_1, L_2	20 μH	L_m	100 μH
C_1	136 nF	C_2	200 nF
C_f	30 μF	$V_{Batt\text{-}}(V)$	250 ~ 450
C_1	136 nF	C_f	30 μF

a bidirectional 3.5kW resonant converter. The design parameters are listed in Table (2). The system dynamics depend on the operating point, which rapidly varies as the battery voltage changes. To design a globally stable controller for all operating points, the worst case operating conditions must be defined and designed for, which by itself, is not an easy task.

In *BCM*, constant current and constant voltage modes are both needed depending on the battery state of charge. In the *RM*, the converter only operates in the constant voltage mode with DC bus voltage regulation for a wide range of battery voltage.

The first step in the controller design process is to determine the equivalent load resistance. The operating switching frequency range then needs to be defined. These information allow for the definition of the controller worst-case scenario.

To determine the equivalent load resistance, R_L, Fig. 7 is used. The equivalent load resistance during $BCM \left(R_L = \frac{V_{Batt}}{I_{Batt}} \right)$ and during $RM \left(R_L = \frac{V_{DC}^2}{P_o} = \frac{V_{DC}}{I_{DC}} \right)$. The output voltage and current at the steady-state and at
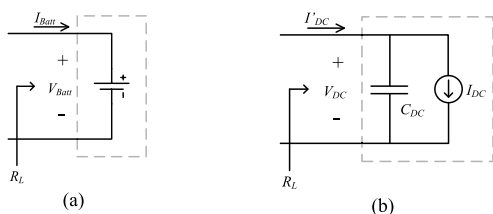

FIGURE 7. Converter equivalent output load resistance for *BCM* and in the *RM*. (a) R_L during the *BCM*. (b) R_L during the *RM*.

different load conditions are plotted vs. the operating switching frequency using (10) – (11) in order to determine the operating frequency range. It is important that the gain curves be monotonic at different load conditions for proper PID controller operation. Therefore, it is essential to plot these gain curves at all load conditions while checking the slope of the curves. This is achieved using 3-D plots (output current or voltage vs. R_L vs. the switching frequency) over the entire operating switching frequency and load resistance defined ranges.

As mentioned earlier, the converter operating point move during the charging and discharging process. The zero-crossing and low-frequency gain of the open-loop bode-plot also change as the operating point changes. The worst-case is found by plotting the open-loop bode-plot at the operating switching frequencies and load resistances.

A. BCM CURRENT LOOP CONTROLLER WORST-CASE OPERATING CONDITIONS

The range of the equivalent load resistance R_L depends on the charging profile which is defined as shown in Fig. 8. The charging power is maintained at 3.5 kW. During constant current mode:

$$R_{L\_I} = \frac{V_{Batt}}{I_{Batt}} = \frac{250\ V}{10\ A} \sim \frac{450\ V}{7.5\ A} = 25\Omega \sim 60\Omega.$$
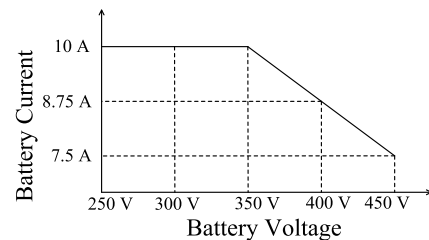

FIGURE 8. Battery current vs. voltage for the converter operating in the *BCM*.

During nominal operating conditions, battery voltage and current are 350V and 10A, resulting in a nominal load resistance of $R_{L\_Inom} = 35\Omega$. The operating frequency range is determined by plotting the output current under steady-state conditions against the converter operating switching frequency at different load conditions. Fig. 9, shows the steady-state output current vs. the operating switching frequency for $R_{L-I_{min}}$, $R_{L-I_{nom}}$ and $R_{L-I_{max}}$. By tracing the desired charging current on Fig. 9, it can be noted that the range of switching frequency permitted in the *BCM* is $f_{sw\_BCM} = 80\ kHz \sim 140\ kHz$.

The battery voltage vs. the operating switching frequency for the entire range of permitted load resistance is shown in Fig. 10. The enclosed surface within the yellow polygon represents the valid operating points. The PID controller is applicable, as the surface is monotonically decreasing.

The worst-case conditions for the current loop controller design are found next. Fig. 11 shows the open-loop bode
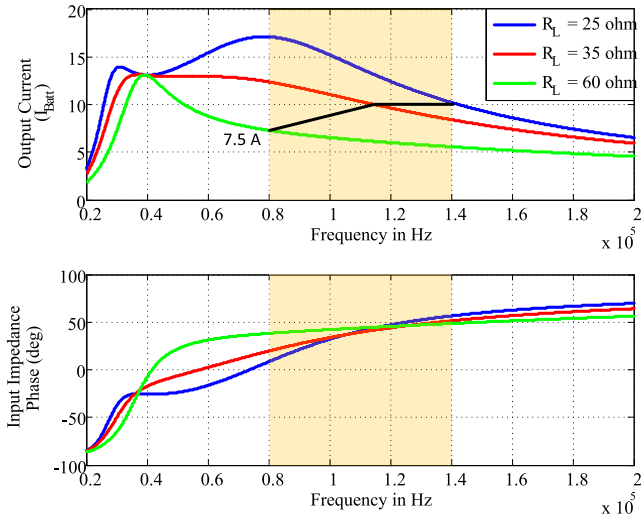
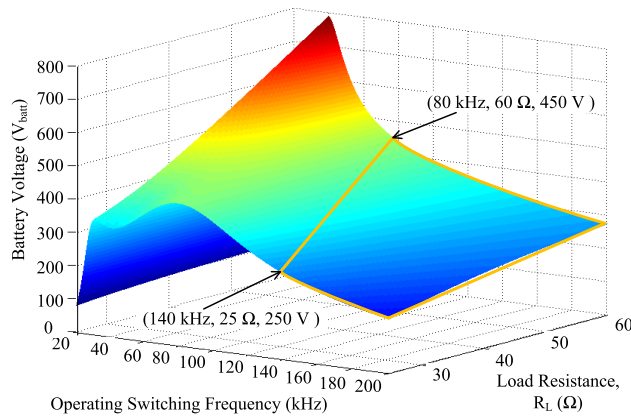FIGURE 9. Output current vs. switching frequency at different load conditions.

FIGURE 10. Battery voltage vs. switching frequency at different load conditions.

FIGURE 11. Bode-plot for $G_{if}(s)$ under different switching frequencies.
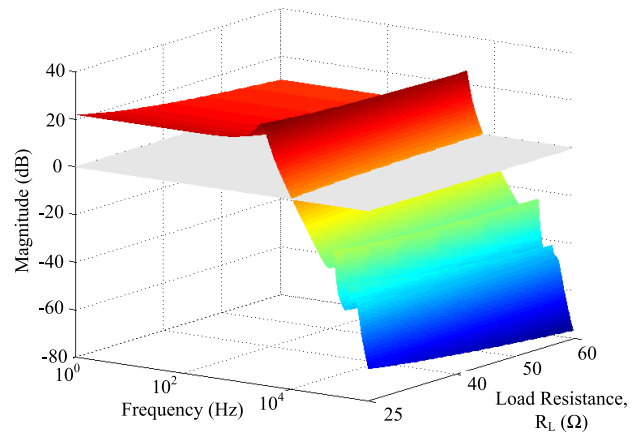
FIGURE 12. Converter $G_{if}(s)$ Bode plot at $f_s = 90kHz$.

plot for $G_{if}(s)$ for a 60 Ω load resistance. The operating switching frequency is swept from 80 to 200 kHz. It can be noted that the open-loop crossover frequency increases as the converter switching frequency decreases. A maximum open-loop bode-plot crossover frequency is achieved at a switching frequency of 90 kHz. Therefore, the worst-case for a fixed load resistance occurs at 90 kHz. The open-loop control-to-output current, $G_{if}(s)$ is shown in Fig. 12 for a converter operating at a switching frequency of 90 kHz. The output load resistance is varied from 25 Ω to 60 Ω. It can be concluded that the crossover frequency of the open-loop bode-plot remains nearly constant. It can be concluded from Fig. 9 that the converter will operate at a switching frequency of 90 kHz only for an equivalent load resistance of 35 Ω or more. Therefore, the worst-case for the current loop controller design is when the output load resistance is between 35 Ω and 60 Ω.
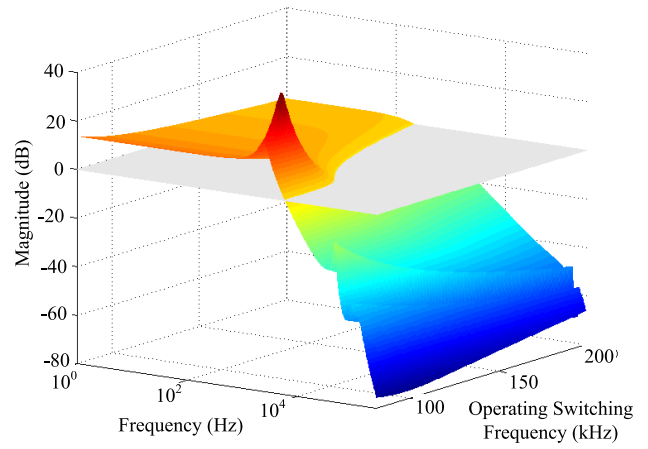
B. WORST-CASE OPERATING CONDITIONS FOR VOLTAGE LOOP CONTROLLER DURING BCM OPERATION

During constant voltage mode, the converter keeps the battery voltage constant at the reference voltage. In this operating mode, the battery charging current drops to a minimum value, and the equivalent output resistance, R_L, becomes very large. In this example, a 450 V battery reference voltage is chosen, and since the minimum charging current is set to 100 mA, then during constant voltage mode, the charging current drops from 7.5 A to 100 mA. So: $R_{L\_V} = \frac{V_{Batt}}{I_{Batt}} = 60\Omega \sim 4.5\,k\Omega$

The steady-state output battery voltage vs. the operating switching frequency curves are plotted in order to determine the operating frequency range in constant voltage mode as show in Fig. 13 for R_{L_Vmin}, and at selected larger values using (10) – (11). As can be concluded from Fig. 13, the operating switching frequency range for a converter operating in the constant voltage mode during the *BCM* is: $f_{sw_C VM} = 78\,kHz \sim 82\,kHz$. Fig. 13 also shows that PID control can be used to close the voltage loop, since all the curves are monotonically decreasing.
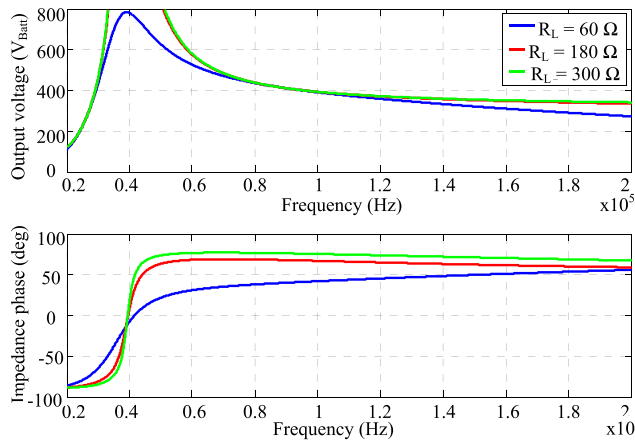
FIGURE 13. *BCM* operating converter output voltage vs. operating switching frequency under different load conditions.
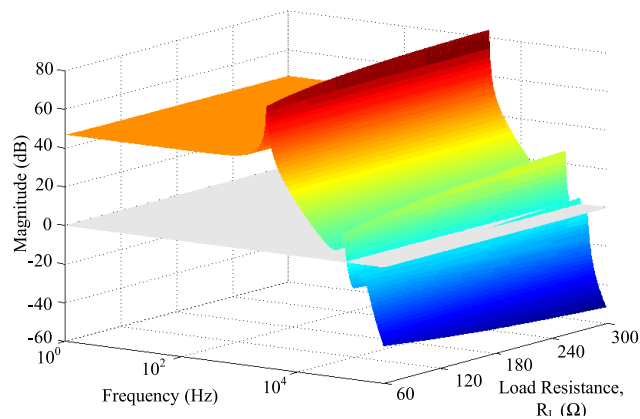

FIGURE 14. $G_{vf}(s)$ open-loop bode-plot with $f_s = 80 kHz$.

The control-to-output voltage, $G_{vf}(s)$, bode-plot for a load resistance range of 60 Ω ∼ 300 Ω and switching frequency of 80 kHz is shown in Fig. 14, and is used to find the worst-case operating conditions. It can be seen that the crossover frequency is fixed while the load is changing, however, only the resonant peak increases when R_L increases. Keeping the closed loop bandwidth less than the resonant peak frequency, in addition to the existence of the magnetics equivalent resistance, the resonant peak will be considerably attenuated. Therefore, the worst-case operating conditions in the constant voltage mode under *BCM operation*, is when the output resistance is 60 Ω, and the switching frequency is 80 kHz.

C. RM VOLTAGE LOOP CONTROLLER WORST-CASE OPERATING CONDITIONS

Under *RM operation*, the DC bus voltage is held constant by converter controls for a wide range of battery input conditions. The converter rms current, i_2, can become very large for higher output power conditions. To limit this current magnitude, the converter's output power is reduced at lower battery voltages. The proposed converter output power profile vs. battery voltage while operating in *RM* is shown in Fig. 15.
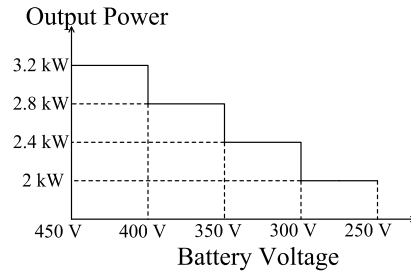

FIGURE 15. *RM* operating Converter output power vs. the battery voltage.

For the chosen dc bus voltage of 400 V, the equivalent load resistance is: $R_L = \frac{V_{DC}^2}{P_o} = \frac{400^2}{3200} \sim \frac{400^2}{2000} = 50\,\Omega \sim 80\,\Omega$.

To find the operating frequency range in this mode, the steady-state voltage gain vs. the operating switching frequency is plotted for different load resistances using (10) – (11). Fig. 16 shows these curves and it can be determined that the operating switching frequency range for the converter operating in the *RM* is: $f_{sw_C VM} = 45\, kHz \sim 110\, kHz$.
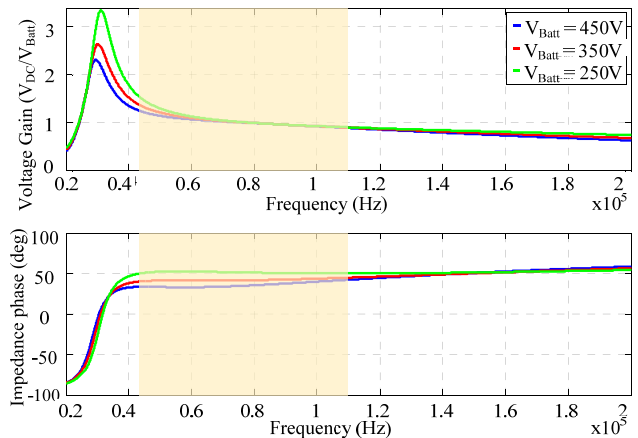

FIGURE 16. *BCM* operating converter's output voltage vs. operating switching frequency under different load conditions.

The voltage gain vs. the operating switching frequency for the entire range of load resistance is plotted in Fig. 17. The yellow polygon encloses the operating surface. As can be noted from the figure, the enclosed surface decreases monotonically, and a PID controller may be used to close the voltage loop.

The worst-case conditions for the voltage loop controller design is found next. Fig. 18 shows the open-loop control-to-output voltage, $G_{vf}(s)$, for a 50 Ω load resistance. The operating switching frequency is swept from 45 kHz to 110 kHz. It can be observed that the open-loop crossover frequency is constant with the variation of the switching frequency. However, at 90 kHz, the open-loop bode-plot shows high resonant peak, therefore it is considered as the worst-case.

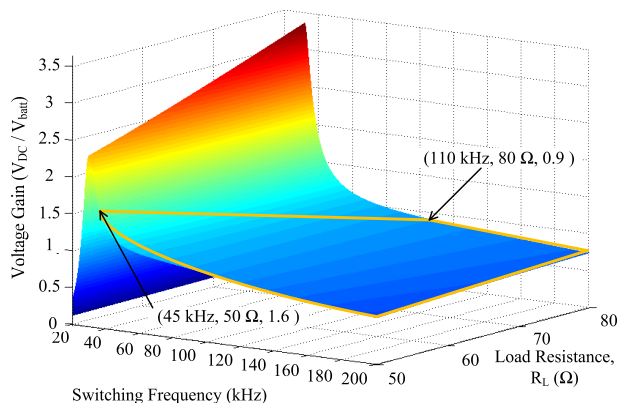Fig. 19 shows the open-loop control-to-output voltage, $G_{vf}(s)$, at a switching frequency of 90 kHz. The output

FIGURE 17. *BCM* battery voltage vs. switching frequency at different load conditions.
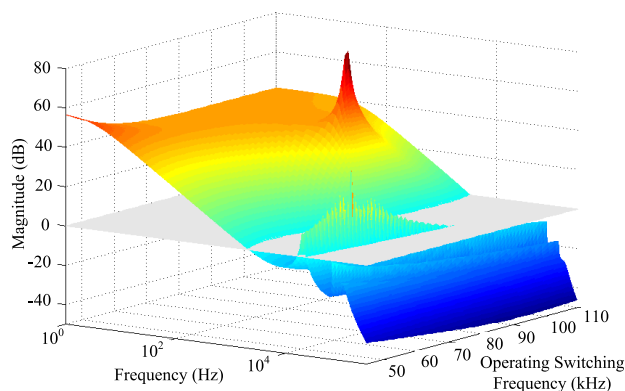

FIGURE 18. *RM* operating converter open-loop bode-plot for control-to-output voltage, $G_{vf}(s)$, under different switching frequencies.
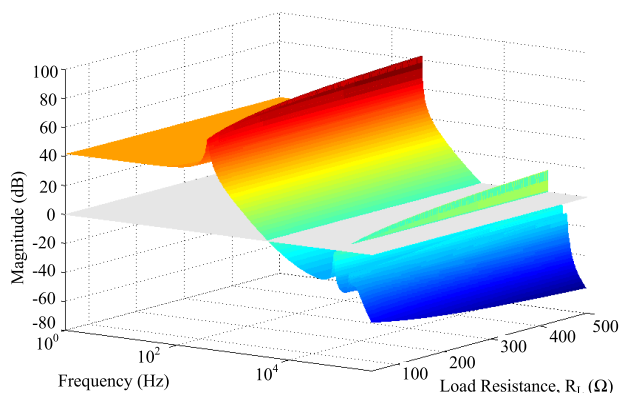

FIGURE 19. *RM* operating converter open-loop bode-plot $G_{vf}(s)$, at switching frequency of 90 kHz under different load conditions.

load resistance is varied from 50 Ω to 500 Ω. It can be noted that the crossover frequency of the open-loop bode plot remains constant, and all the plots are exactly alike. The only difference is that the resonant peak gets higher as R_L increases. However, the DCR of magnetics' winding and the controller will attenuate this resonant peak considerably if the closed loop bandwidth is much less than the resonant

peak frequency. The worst-case operating conditions during constant voltage more RM, are determined to be at output load resistance of 50 Ω, and an operating switching frequency of 90 kHz.

IV. CONVERTER OPERATION NEAR THE SERIES RESONANT FREQUENCIES

The efficiency of the power stage of the converter is maximum at the series resonant frequency [28]. Under nominal operating conditions, the converter is designed to operate at this point. However, as shown in the previous section, the worst-case operating conditions for the current and voltage loop controller occur at this frequency, due to the high quality-factor (Q) peak in the open-loop bode. To study this high peak Q in the bode-plots, the zeros and poles of the converter transfer function must be observed when the converter is operating close to the resonant frequencies. The two series resonant frequencies of this converter are;

$$f_{ser1} = \frac{1}{2\pi\sqrt{L_1 C_1}} = 96.5\ kHz \tag{15}$$

$$f_{ser2} = \frac{1}{2\pi\sqrt{L_2 C_2}} = 79.58\ kHz \tag{16}$$

The small-signal model in (12) and (13) show that this resonant converter is a 9th order system. This means there are nine poles in each transfer function. But since most of the poles and zeros occur at a very high frequency, they can be ignored.
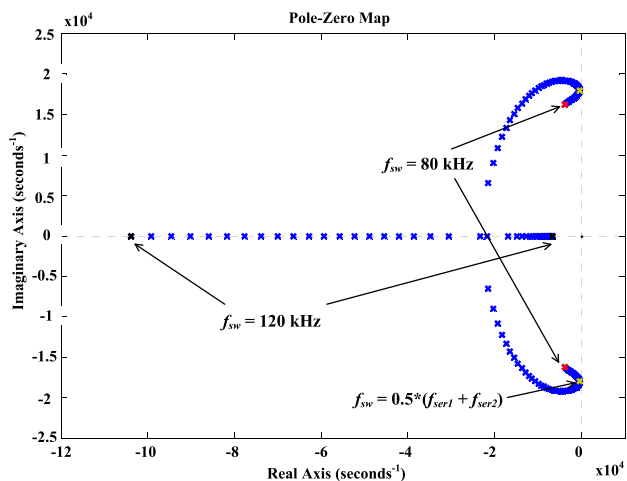

FIGURE 20. Location of the low frequency poles, frequency is varied from 120 kHz to 80 kHz.

Fig. 20 shows the dominant poles as the switching frequency is varied from 80 kHz to 120 kHz. The dominant poles are on the real axis for higher switching frequencies, and there is no resonant peaking in the bode-plot. As the switching frequency decreases, the two poles are close on the real axis, until they reach the breakaway point. If the switching frequency is further reduced, the two poles break away from the real axis, and move towards the imaginary axis. This is

when the resonant peaking starts to appear. The damping is minimum (and Q is maximum) at the mid-point between the two resonant frequencies, where the magnitude of the resonant peak is maximum. A yellow cross in Fig. 20 represents this point.
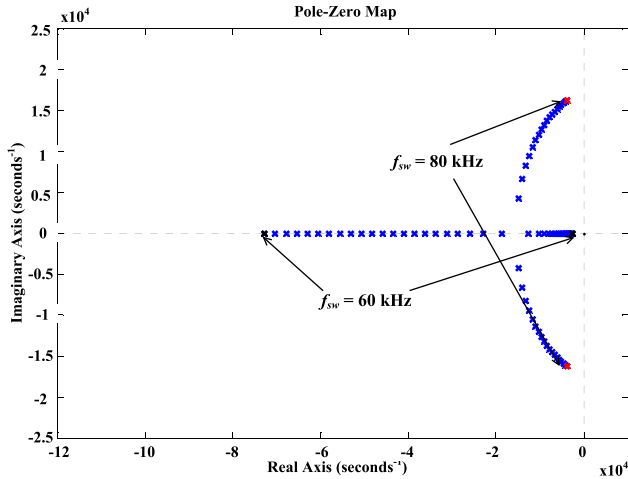

FIGURE 21. Location of the low frequency poles, frequency is varied from 80 kHz to 60 kHz.

As can be seen in Fig. 21, if the converter operating frequency is between the two resonant frequencies; the dominant poles are located close to the imaginary axis, which results in resonant peaking in the open-loop bode-plot. However, if the converter switching frequency is reduced, the dominant poles move towards the real axis until they reach the break-in point. If the switching frequency is reduced further, the two dominant poles move away from each other on the real axis, and no resonant peaking occurs in the open-loop bode-plots.

From the above discussion, it can be concluded that no resonant peaking will occur in the open-loop bode plot if the converter operating switching frequency is kept higher than f_{ser1} or lower than f_{ser2}. If the converter operating switching frequency is between the two series resonant frequencies, peaking will occur in the bode-plot due to lower damping and higher Q.

V. CONTROLLER DESIGN AND EXPERIMENTAL RESULTS

The worst-case operating conditions were determined in the previous sections for the converter operating in both *BCM* and *RM*. The controllers will now be designed for these worst-case conditions. The closed loop system block diagram is shown in Fig. 22 where:

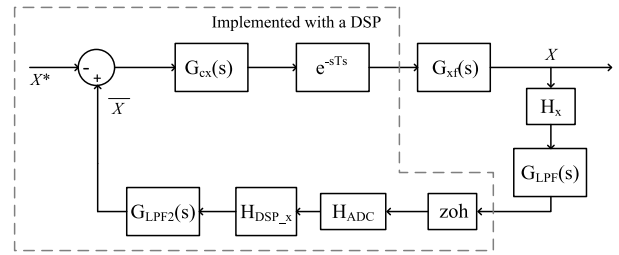|	
X	= Output current or voltage to be regulated,
$\bar{X}$	= Averaged output current or voltage,
$X*$	= Output current or voltage reference,
H_x	= sensor gain,
$G_{LPF}(s)$	= Low-pass filter implemented the hardware,
H_{ADC}	= Analog-to-digital converter (ADC) gain,

FIGURE 22. Closed-loop system block diagram.

H_{DSP_x}	= Digital Signal Processor (DSP) gain,
$G_{LPF2}(s)$	= Low-pass filter implemented in DSP,
$G_{cx}(s)$	= Designed controller,
e^{-sTs}	= Single sampling period delay

The loop-gain of the closed-loop system is,

$$T_x(s) = H_x G_{xf}(s) G_{LPF}(s) H_{ADC} H_{DSP\_i} G_{LPF2}(s) G_{cx}(s) e^{-sTs} \qquad (17)$$

The chosen DSP gain ensures that the product of all gains is equal to unity, i.e. $H_x \cdot H_{DSP_x} \cdot H_{ADC} = 1$. So, the loop gain becomes,

$$T_x(s) = G_{xf}(s) \cdot G_{LPF}(s) \cdot G_{LPF2}(s) \cdot G_{cx}(s) \cdot e^{-sTs} \qquad (18)$$

The hardware implemented low-pass filter is a sallen-key 2nd order filter. The cut-off frequency is 10 kHz. The transfer function t is:

$$G_{LPF}(s) = \frac{1}{1 + \frac{s}{2\pi \times 10000} + (\frac{s}{2\pi \times 10000})^2} \qquad (19)$$

And, the DSP implemented low-pass filter is,

$$G_{LPF2}(s) = \frac{1}{1 + \frac{s}{2\pi \times 1000}} \qquad (20)$$

A Texas Instruments TMS320F28335 DSP is used for control implementation. The sampling frequency is 30 kHz, and a 33.33 μs delay is added in the loop.

$$e^{-sTs} = \frac{1 - \frac{T_s}{2}s + \frac{T_s^2}{12}s^2}{1 + \frac{T_s}{2}s + \frac{T_s^2}{12}s^2} \qquad (21)$$

A 5kW BK Precision 8526 programmable electronic load is used for testing. The programmable load is configured as a battery, where the voltage is varied from 250V to 450V for BCM testing. And configured as a current source that varies from 0.1A to 8.5A to emulate the ac-dc stage for RM testing.

The loop-gain of the converter operating in the constant current mode in the *BCM* is:

$$T_{i\_BCM}(s) = G_{if}(s) \cdot G_{LPF}(s) \cdot G_{LPF2}(s) \cdot G_{ci}(s) \cdot e^{-sTs} \qquad (22)$$

The current loop bandwidth is 515 Hz, with a phase margin of 52.8° at the worst-case operating conditions.
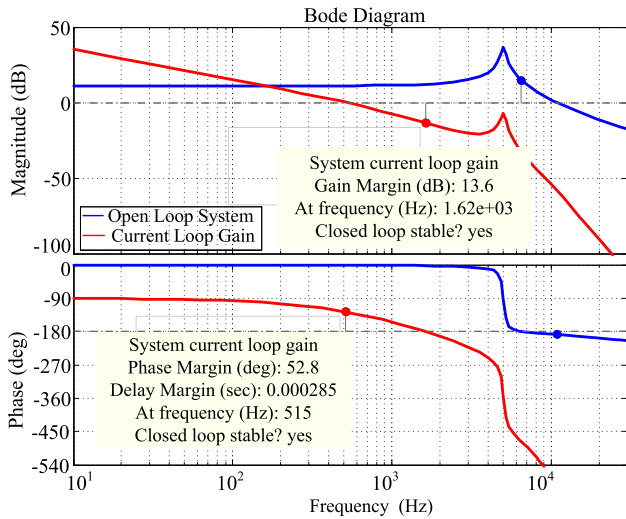
$$G_{ci}(s) = \frac{10}{s} \quad (23)$$

FIGURE 23. Worst-case open-Loop bode-plot and loop gain for *BCM* operating converter in the constant current mode.

The worst-case open-loop bode-plot and the closed-loop current gain are shown in Fig. 23. A step change to the output battery voltage from 250 V up to 325 V and back down to 250V was applied to check the closed-loop system stability. The system is stable, with minimal overshoot or undershoot for both step increase and decrease in the battery voltage as shown in Figs. 24 and 25.
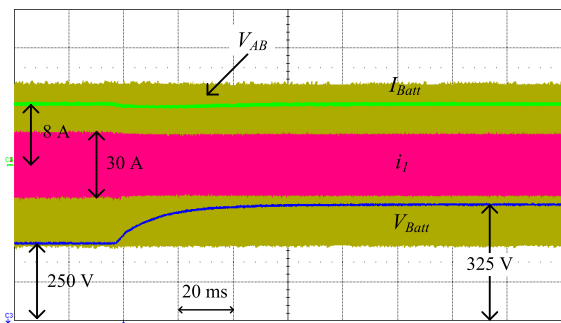

FIGURE 24. Battery voltage step change from 250 V to 325 V for *BCM* constant current mode.

The loop-gain of the converter operating in the constant voltage mode in the *BCM* is,

$$T_{v\_BCM}(s) = G_{vf}(s) \cdot G_{LPF}(s) \cdot G_{LPF2}(s) \cdot G_{cv}(s) \cdot e^{-sTs} \quad (24)$$

The controller is designed with a 103 Hz bandwidth, and a phase margin of 82.2°.

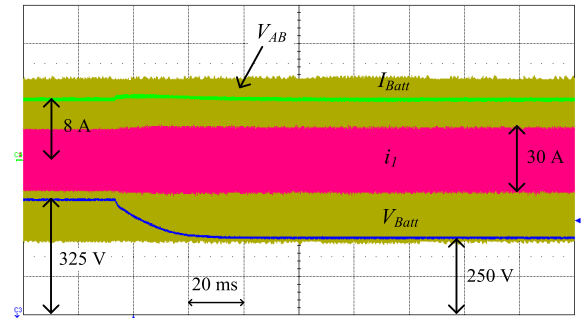$$G_{cv}(s) = \frac{0.3}{s} \quad (25)$$

FIGURE 25. Battery voltage step change from 325 V to 250 V for *BCM* constant current mode.
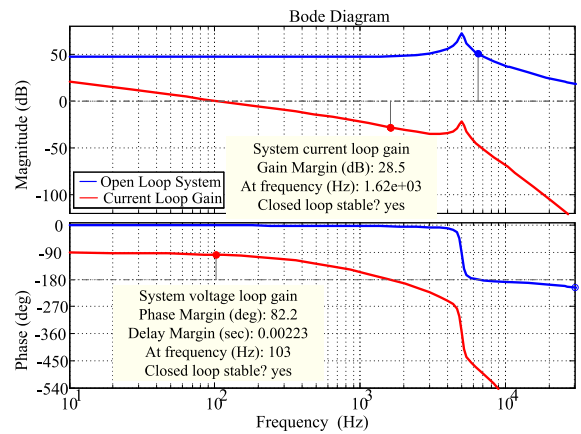
FIGURE 26. The worst-case open-Loop bode-plot and loop gain for converter operating in the constant voltage mode in the *BCM*.

The worst-case open-loop bode-plot and the closed-loop current gain are shown in Fig. 26. A step change to the output voltage reference from 315V to 420V and back to 315V was applied with a resistive load of 57Ω to check the system stability. The system is stable, with no overshoot or undershoot for both step changes in the reference voltage as shown in Fig. 27 and Fig. 28.

FIGURE 27. Battery voltage step change from 315 V to 420 V for *BCM* constant current mode converter with R_L = 57 Ω.

The loop-gain of the converter operating in the constant voltage mode in the *RM* is,

$$T_{v\_RM}(s) = G_{vf}(s) \cdot G_{LPF}(s) \cdot G_{LPF2}(s) \cdot G_{cv}(s) \cdot e^{-sTs} \quad (26)$$

FIGURE 28. Battery voltage step change from 420 V to 315 V for *BCM* constant current mode converter with $R_L = 57\ \Omega$.
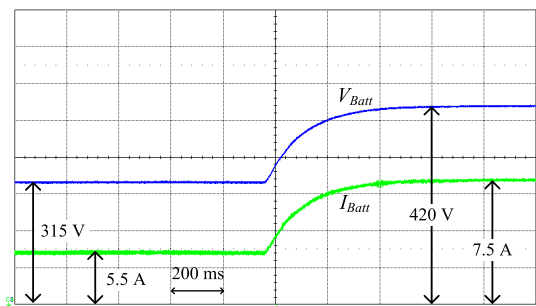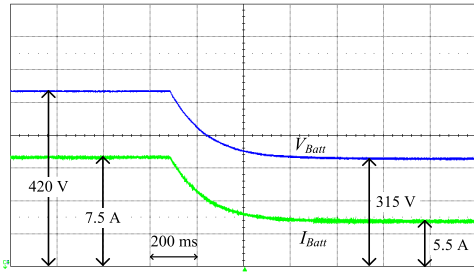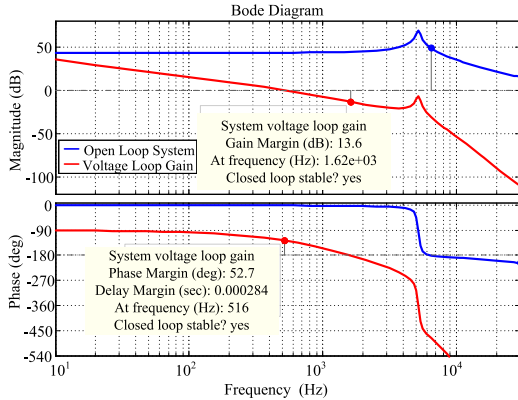

FIGURE 29. Worst-case open-Loop bode-plot and loop gain for *RM* operating converter in the constant voltage mode.
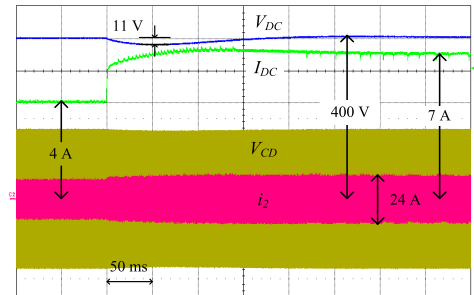

FIGURE 30. Step change in the dc bus current from 4 A to 7 A for *RM* operating converter in the constant voltage mode.
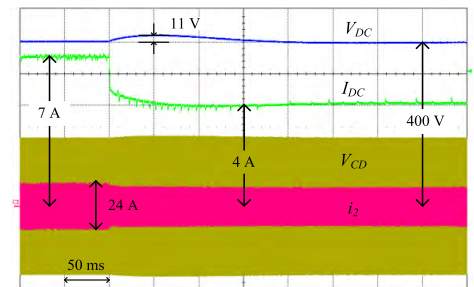

FIGURE 31. Step change in the dc bus current from 7 A to 4 A for *RM* operating converter in the constant voltage mode.

The following controller is designed for a 516 Hz bandwidth, and a phase margin of 52.7°.

$$G_{cv}(s) = \frac{2.5}{s} \qquad (27)$$

The worst-case open-loop bode-plot and the closed-loop current gain are shown in Fig. 29. A step change to the output current reference from 4A to 7A and back to 4A was applied to check the system stability. The system is stable, with nearly no overshoot or undershoot for the step change in the reference current as shown in Fig. 30 and Fig. 31.

VI. CONCLUSIONS

The *CLLLC*-type resonant converter is a promising topology that gives high conversion efficiency backed by soft switching capability on the primary and secondary sides of the isolation transformer. Due to the variable dynamics at different loading conditions, the stability of the governing controllers becomes an issue, and a globally stable controller for all working scenarios becomes important. The definition of worst case scenario conditions was presented in this manuscript and a controller design methodology accordingly was devised. The stability margins for all working conditions was graphically presented to firm the design outputs.

Controllers' design in both BCM and RM modes were presented and verified by both simulation and experimental results. The results showed that the designed controllers can account to all operating conditions and the analysis provided priori introduces thorough insight on the dynamic modeling of the CLLLC-type resonant converters.

As future extension of this work, it might be suggested to implement dynamic controllers to maximize the bandwidth at all operating conditions. Scheduled gain controllers are examples of such controllers that might be adapted.

APPENDIX
See Table 2.

$K_1 = \dfrac{4\,(I_{2c})^2 \cdot V_{Cf}}{\pi\,L_{eqm}\,I_{pk}{}^3}$	$K_2 = \dfrac{4\,I_{2s}I_{2c} \cdot V_{Cf}}{\pi\,L_{eqm}\,I_{pk}{}^3}$	$K_3 = \dfrac{4\,I_{2s}}{\pi\,L_{eqm}\,I_{pk}}$
$K_4 = \dfrac{4}{\pi\,L_{eq2}}\sin\!\left(\dfrac{\pi}{2}D\right)$	$K_5 = \dfrac{2\,V_g}{L_{eq2}}\cos\!\left(\dfrac{\pi}{2}D\right)$	$K_6 = \dfrac{4\,(I_{2c})^2 \cdot V_{Cf}}{\pi\,L_{eq1}\,I_{pk}{}^3}$
$K_7 = \dfrac{4\,I_{2s}I_{2c} \cdot V_{Cf}}{\pi\,L_{eq1}\,I_{pk}{}^3}$	$K_8 = \dfrac{4\,I_{2s}}{\pi\,L_{eq1}\,I_{pk}}$	$K_9 = \dfrac{4}{\pi\,L_{eqm}}\sin\!\left(\dfrac{\pi}{2}D\right)$
$K_{10} = \dfrac{2V_g}{L_{eqm}}\cos\!\left(\dfrac{\pi}{2}D\right)$	$K_{11} = \dfrac{4\,I_{2s}I_{2c} \cdot V_{Cf}}{\pi\,L_{eqm}\,I_{pk}{}^3}$	$K_{12} = \dfrac{4\,(I_{2s})^2 \cdot V_{Cf}}{\pi\,L_{eqm}\,I_{pk}{}^3}$
$K_{13} = \dfrac{4\,I_{2c}}{\pi\,L_{eqm}\,I_{pk}}$	$K_{14} = \dfrac{4\,I_{2s}I_{2c} \cdot V_{Cf}}{\pi\,L_{eq1}\,I_{pk}{}^3}$	$K_{15} = \dfrac{4\,(I_{2s})^2 \cdot V_{Cf}}{\pi\,L_{eq1}\,I_{pk}{}^3}$
$K_{16} = \dfrac{4\,I_{2c}}{\pi\,L_{eq1}\,I_{pk}}$	$K_{17} = \dfrac{2}{\pi C_f}\dfrac{R_L}{R_L+R_c}\dfrac{I_{2s}}{I_{pk}}$	$K_{18} = \dfrac{2}{\pi C_f}\dfrac{R_L}{R_L+R_c}\dfrac{I_{2c}}{I_{pk}}$
$K_{19} = \dfrac{1}{C_f}\dfrac{1}{R_L+R_c}$	$K_{20} = \dfrac{2}{\pi}\dfrac{R_c R_L}{R_L+R_c}\dfrac{I_{2s}}{I_{pk}}$	$K_{21} = \dfrac{2}{\pi}\dfrac{R_c R_L}{R_L+R_c}\dfrac{I_{2c}}{I_{pk}}$
	$K_{22} = \dfrac{R_L}{R_L+R_c}$	

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