Two-dimensional Mapping of Interface Thermal Resistance

by Transient Thermal Measurement

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Abstract

Interconnects in power module result in thermal interfaces. The thermal interfaces degrade under thermal cycling, or chemical loading. Moreover, the reliability of thermal interfaces can be especially problematic when the interconnecting area is large, which increases its predisposition to generate defects (voids, delamination, or nonuniform quality) during processing. In order to improve the quality of the bonding process, as well as to be able to accurately assess interface reliability, it would be desirable to have a simple, reliable, and nondestructive measurement technique that would produce a 2-d map of the interface thermal resistance across a large bonded area. Based on the transient thermal method of JEDEC standard 51-14, we developed a measurement technique that involves moving a thermal sensor discretely across a large-area bonded substrate and acquiring the interface thermal resistance at each location. As detailed herein, the sensor was fabricated by packaging an IGBT bare die.

An analytical thermal model was built to investigate the effects of thermal sensor packaging materials and structural parameters on the sensitivity of the measurement technique. Based on this model, we increased the detection sensitivity of the sensor by modifying the size of the sensor substrate, the material of the sensor substrate, the size of the IGBT bare die, the size of the heat sink, and the thermal resistance between sample and the heat sink. The prototype of the thermal sensor was fabricated by mounting Si IGBT on copper substrate, after which the Al wires were
ultrasonic bonded to connect the terminals to the electrodes. The sensor was also well protected with a 3-d printed fixture. Then the edge effect was investigated, indicating the application of the thermal sensor is suitable for samples thinner than the value in TABLE 2-3.

The working principle of the movable thermal sensor – \( Z_{th} \) measurement and its structure function analysis – was then evaluated by sequence. The \( Z_{th} \) measurement was evaluated by measuring the \( Z_{th} \) change of devices induced by degradation in sintered silver die-attach layer during temperature cycling. At the end of the temperature cycling, failure modes of the sintered silver layer were investigated by scanning electron microscope (SEM) and X-ray scanning, to construct a thermal model for FEA simulation. The simulation results showed good agreement with the measured \( Z_{th} \) result, which verified the accuracy of the test setup. The sensitivity of structure function analysis was then evaluated by measuring thermal resistance (\( R_{th} \)) of interface layers with different thermal properties. The structure function analysis approach successfully detected the \( R_{th} \) change in the thermal interface layer.

The movable thermal sensor was then applied for 2d-mapping of the interface \( R_{th} \) of a large-area bonded substrate. Examining the test coupons bonded by sintered silver showed good and uniform bonding quality. The standard deviation of \( R_{th} \) is about 0.005 K/W, indicating the 95% confidence interval is about 0.01 K/W, which is commonly chosen as the error of measurement. The sensitivity of the movable thermal sensor was evaluated by detecting defects/heat channels of differing sizes. The 2-d mapping confirmed that the thermal sensor was able to detect defect/heat channel sizes larger than 1x1 mm\(^2\). The accuracy of the sensitivity was verified by FEA simulation. Moreover, the simulated results were consistent with the measured results, which indicates that the movable sensor is accurate for assessing interface thermal resistance.
In summary, based on structure function analysis of the transient thermal impedance, the concept of a movable thermal sensor was proposed for two-dimensional mapping of interface thermal resistance. (1) Preliminary evaluation of this method indicated both transient thermal impedance and structure function analysis were sensitive enough to detect the thermal resistance change of thermal interface layers. With the help of transient thermal impedance measurement, we non-destructively tested the reliability of sintered silver die-attach layer bonded on either Si₃N₄ AMB or AlN DBA substrates. (2) An analytical thermal model was constructed to evaluate the design parameters on the sensitivity and resolution of the movable thermal sensor. A detailed design flow chart was provided in this thesis. To avoid edge effect, requirements on thickness and materials of test coupon also existed. Test coupon with smaller thermal conductivity and larger thickness had a more severe edge effect. (3) The application of the movable sensor was demonstrated by measuring the 2-d thermal resistance map of interface layers. The results indicated for bonded copper plates (k = 400 W/mK) with thickness of 2 mm, the sensor was able to detect defect/heat channel with size larger than 1x1 mm².
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General Audience Abstract

Interconnects in power module result in thermal interfaces. The thermal interfaces degrade during operation and their reliability can be especially problematic when the interconnecting area is large. In order to improve the quality of the bonding process, as well as to be able to accurately assess interface reliability, it would be desirable to have a simple, reliable, and nondestructive measurement technique that would produce a 2-d map of the interface thermal resistance across a large bonded area.

Based on the transient thermal method of JEDEC standard 51-14, we developed a measurement technique that involves moving a thermal sensor discretely across a large-area bonded substrate and acquiring the interface thermal resistance at each location. As detailed herein, the sensor was fabricated by packaging an IGBT bare die, which allowed us to get a 2-d map of the interface thermal resistance. A thermal model was also constructed to guide the design of the sensor, to increase its performance. Moreover, the preliminary test of the test setup was conducted to prove its feasibility for the sensor. Eventually, the sensor’s performance and application was demonstrated by measuring the 2-d thermal resistance map of the bonded interfaces.
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Chapter 1. INTRODUCTION

1.1 Background

1.1.1 Thermal interface materials in power modules

Thermal interface materials (TIMs) are critical components that fill the gaps between different layers to help dissipate any unwanted heat to the ambient environment. Taking power module as an example, as shown in Fig. 1.1, the thermal interface layers include the die-attach layer, the substrate-attach layer, and the baseplate-attach layer [1]. Based on their differing physical properties, TIMs can generally be classified into six distinct categories: thermal greases, thermal pads, thermal adhesives, solders, phase-change materials, and sintered silver [2].

![Fig. 1.1. Schematic of a conventional power module.](image)

(a) Thermal greases

Thermal greases are typically composed of two parts: a polymer matrix and thermal conductive fillers [3]. Due to its good thermal stability and low modulus, silicone is most
commonly used as the matrix. Ceramic fillers such as alumina, aluminum nitride, zinc oxide, silicon dioxide and beryllium oxides—or metallic fillers such as silver and aluminum—are often used to increase the thermal conductivity of the compound [4]. In general, a material with a higher filler content will feature higher thermal conductivity and lower thermal resistivity. When applied to interfaces, thermal greases tend to be pressed to enable the compound to flow into all the voids. However, too high pressure will result in squeezing-out problem [5]. In addition, a thermal grease also suffers from drying-out problem. Typically, their operating temperature is limited by the polymer, which is -40°C to 200°C. It is reported that thermal resistance increases by 4 to 6 times after 7500 cycles between 0°C and 100°C.

(b) Thermal pads

Thermal pads are also composed of two components: the polymer matrix and a thermal conductive filler [6]. Unlike thermal greases, thermal pads are solid and firm in pad shape. With pressure, the thermal pad can be deformed to fill air gaps and small voids, thereby decreasing thermal resistance. Unlike thermal greases, they do not suffer from the drying and squeezing problem [7]. However, due to their similar chemical composition, the operating temperature of a thermal pad is similar to thermal greases, and the solid phase requires higher clamping pressure during installation.

(c) Thermal adhesives

Like thermal greases and pads, a thermal adhesive also comprises two components: the resin and the hardener. Both resin and hardener are mixed with thermally conductive fillers to increase the material’s thermal performance [8, 9]. The resin parts are silicone or an epoxy-based polymer matrix, while the hardener is used to cure the resin after mixing in order to form a relatively firm shape [10, 11]. Prior to curing, low viscosity ensures that the thermal adhesive will fill any gaps
in order to decrease contact thermal resistance. Operation temperature of most thermal adhesive products is below 200°C [12].

(d) Solders

Solders are alloys composed of two or more metals. The distinctive feature of an alloy is that its melting point is lower than either of its constituent metals. This phenomenon enables the soldering process to occur at approximately 200°C. During the soldering process, the solder paste or solder preform is placed between the die and substrates with a solderable metallization surface [13, 14]. When heat is applied to melt the solder alloy, the molten solder dissolves a portion of both adjacent surfaces. Once cooled, a solder joint is formed that bonds the two metal surfaces. The melting point of most solders is below 300°C [15-17]. As a rule of thumb, solder materials can be reliably used up to a homologous temperature of 80% of their absolute melting point; beyond that approximate percentage, however, the creep effect will lead to rapid degradation. Thus, the reliable operating temperature of most solders is below 200°C [18]. It must be noted that during temperature cycling, high-modulus intermetallics formed in solder joints decreases the reliability of the interface layer [19-21]. This reliability issue becomes even more severe when the operating temperature gets close to the melting temperature.

(e) Phase change materials

Phase change materials (PCMs) refer to a group of materials that melt at a certain temperature, which are capable of storing and releasing a large amount of energy [22]. When used as TIMs, PCMs are usually mixed with thermally conductive fillers, such as ceramics and metal particles, in order to achieve low thermal resistance [23]. Unlike other thermal interface materials, the melting temperature of PCMs is usually below the maximum operation temperature. During the melting process, large amount of heat is absorbed when the phase changes from solid to liquid,
which can decrease the transient thermal impedance of the system. It should also be noted that PCMs do not suffer from some conventional failure modes of TIMs, such like delamination. However, the disadvantage of a PCM is its relatively high thermal resistance [24].

(f) Sintered silver

A so-called “low-temperature joining technique” (LTJT), which is based on sintering the silver particles in a conductive adhesive, is also being investigated for use in devices intended for high-temperature operation [25, 26]. The paste-form material, which is comprised of silver powders or flakes coupled with organic or inorganic additives, is then processed at temperature below 250°C, after which it forms a sintered silver joint between the different surfaces. The sintered silver layer displays superior properties, such as high thermal and electrical conductivity, high reliability, and the ability to withstand high operation temperature (greater than 700°C). The state-of-the-art LTJT silver paste is made up of nano-size silver particles. Based on the Mackenzie-Shuttleworth sintering model [27], the small size of the silver particles increases the sintering driving force, which, in return, decreases the sintering temperature and pressure. To protect the nano particles from agglomeration, organic or inorganic binders and surfactants have been introduced. As a result, a nanosilver paste can serve as the thermal interface layer under low processing temperature (lower than 250°C) [17, 26, 28, 29]. Because the porous microstructure of the sintered silver joint is able to release any accumulated stress during operation, it can be noted that the reliability of sintered silver when exposed to cyclic temperature changes is better than traditional solders and other thermal interface materials [30, 31].

1.1.2 Requirements and challenges for thermal interface materials

Over recent decades, the demand for power modules featuring increased power density has intensified [32-34]. On the one hand, increasing power density results in a concurrent increase in
power loss density, which exists and dissipates in the form of heat. In some application conditions, such as electric vehicle drive inverters, heat flux density can be as high as 400 W/cm$^2$ under certain critical working conditions [35]. Therefore, thermal interface materials with high thermal conductivity are becoming increasingly important for reducing the overall thermal resistance [36, 37]. On the other hand, with the development of wide-bandgap devices such like silicon carbide (SiC) and gallium nitride (GaN) devices, the intrinsic carrier becomes much less, which pushes the operation temperature beyond 250$^\circ$C [38, 39]. This relatively high operation temperature has resulted in a growing demand for high-temperature thermal interface materials. Generally, sintered silver and solder both feature much higher thermal conductivity, which reinforce the need to replace traditional thermal greases and gels in power modules. In addition, sintered silver also affords very high operation temperature (over 700$^\circ$C), coupled with good reliability and performance [28].

However, at least three challenges must be addressed for the wider application of thermal interface materials. First, the performance properties of thermal interface materials tend to degrade during high-temperature operation. In the case of thermal pastes or gels, the use of higher temperature will dry out the composite and result in the generation of defects, such as voids or air bubbles, which increases the thermal resistance [40, 41]. For solder, the close-to-melting-point high temperature will induce the creep effect, which leads to rapid degradation. Moreover, high-temperature operation provides the driving force of recrystallization, which changes the intrinsic thermal properties. Second, thermo-mechanical stress is accumulated in thermal interface materials during cycling because of the coefficient of thermal expansion (CTE) mismatch, which generates defects such as cracks or delamination. These defects behave as heat flux barrier, thereby increasing overall thermal resistance [42]. Third, during the attaching process, both solder and
sintered silver undergo a high-temperature profile. During this profile, evaporation and decomposition of the chemical additives generate gases and may introduce voids in the bond line [43]. This issue becomes worse when it comes to large area such like substrate attach interface or base plate attach interface [44]. In addition to the trapping of gases, the distortion and roughness of large area mating surface will cause nonuniform bonding quality. Particularly for sintered silver, which needs pressure assistance for better bonding quality, uneven pressure distribution is also likely to introduce nonuniformity of bonding quality. Unfortunately, voids, gas bubbles, or nonuniform bonding generates ‘hot spot’ in the thermal interface layer, potentially resulting in reliability problems [45].

1.2 Review of thermal characterization methods

As-prepared thermal interface materials may suffer from nonuniform thermal quality, which causes ‘hot spot’; after operation, thermal interface materials may suffer from thermal degradation, which increases total thermal resistance. Therefore, there is a stringent need for thermal characterization methods that can non-destructively measure the spatial-resolved thermal properties of the thermal interface layer.

1.2.1 Comparative steady-state technique

The comparative steady-state technique is used to measure samples with rectangular or cylindrical shape. During the measurement, the test sample is placed between two standard samples whose thermal conductivity are known, as shown in Fig. 1.2 [46, 47]. The test sample and the standard samples are heated by an upper heater with known power input. The temperature drop across each sample is then measured by thermal couples after the whole setup reaches its thermal
steady state. Generally, the thermal conductivity of a sample can be determined by Fourier’s law of heat conduction:

\[ k = \frac{QL}{A\Delta T} \]  

(1.1)

where Q is the input power, A is the cross-section area, L is the length and \( \Delta T \) is temperature different across the sample. Because the input power is interfered by convection and radiation, standard samples are used to determine the Q across the test sample:

\[ k = \frac{k_r(T_6-T_5+T_2-T_1)L_r}{2L(T_4-T_3)} \]  

(1.2)

Fig. 1.2. Schedule of comparative steady-state technique [47].

The drawback, however, is that this technique requires samples of a bulkier shape and thus is less effective for thin films. In addition, this approach achieves optimal accuracy when the temperature difference across the test sample is larger than 2°C [48].

### 1.2.2 Laser flash method

The laser flash method is a non-contact, non-destructive method. Because there is no contact, the error from contact resistance is eliminated. In this approach, a laser pulse is flashed on the
bottom side of the sample, and a thermographic technique is used to detect the temperature as shown in Fig. 1.3. The test sample is generally in disk shape with a coating layer on both sides. This coating layer serves as an absorber on the bottom side and as an emitter on the top side. The dynamic top side temperature response curve can be used to calculate thermal diffusivity [49]:

\[ \alpha = \frac{1.38d^2}{\pi^2 t_{0.5}} \]  

(1.3)

where \( d \) is the thickness of the disk and \( t_{0.5} \) is the time that takes for the sample to reach one half of the maximum steady-state temperature. Based on ASTM E1461, to obtain accurate thermal conductivity, material density and specific heat are needed [50]:

\[ k = \alpha \rho c_p \]  

(1.4)

However, this method requires a disk-shaped sample to fit in the laser equipment. Also, for ease of laser-energy absorption and heat emission, surface coating by corresponding materials is necessary. Furthermore, for unknown materials, additional measurements of specific heat and density are needed, which increase the complexity of the test. Because this method is a rapid-response test, the recommended samples thickness should be no less than 100 \( \mu \text{m} \).

Fig. 1.3. Schematic of laser flash method.
1.2.3 Transient plane source (TPS) method

The transient plane source method utilizes a thin spiral circuit with polyimide insulation, which serves as both heat source (V1) and temperature sensor (V2), as shown in Fig. 1.4 (a) [51-53]. In one test, the sensor is placed between two test samples. Because temperature-increase performance is dependent on the heating power and the specific thermal properties of the test samples, one can determine thermal properties by measuring the temperature response in just a few seconds. Typically, the temperature increase curve as a function of time can be measured, which then is fitted by:

\[
\Delta T(\phi) = \frac{Q}{\pi r^2 k} D(\phi)
\]

\[
\phi = \sqrt{\frac{\varepsilon\alpha}{r^2}}
\]

where \( r \) is the sensor radius, \( D(\phi) \) is a dimensionless expression that describes the heat conduction of the sensor, as shown in Fig. 1.4 (b). It is reported that the TPS method is capable for measuring materials featuring thermal conductivity between 0.005 to 500 W/mK [51]. However, four principal disadvantages are associated with this approach: (1) the surface of both samples needs to be flat; (2) the test sample should ideally be homogenous; (3) this measurement technique is essentially a surface-characterization method, which means it can only indicate thermal properties of the close-to-surface area [54, 55].
1.2.4 3ω method

The 3ω method is used to measure thermal conductivity of thin films. The schematic of 3ω is illustrated in Fig. 1.5. Metallic strip is deposited on the thin film, which measures approximately 20-100 μm in width and 1000-10000 μm in length. This metallic strip serves as both heater and temperature sensor. This method utilizes an alternating current (AC) source at frequency ω on a strip [56-58]:

\[ I(t) = I_0 \cos(\omega t) \]  \hspace{1cm} (1.7)

![Schematic of transient plane source method.](image)

**Fig. 1.4.** (a)Schematic of transient plane source method. (b) Plot of D(∅) as a function of ∅.
Fig. 1.5. Schematic of 3ω method.

Where $I_0$ is the amplitude. As a result, the power, which leads to temperature change, is a function of $\cos^2(\omega t)$, or $\cos(2\omega t)$:

$$\Delta T(t) = \Delta T_0 (2\omega t + \phi)$$  (1.8)

where $\phi$ is the phase delay caused by capacitance. The thermal resistance changes along with temperature as a function of:

$$R(t) = R_0 (1 + \alpha \Delta T) = R_0 [1 + \alpha \Delta T_0 (2\omega t + \phi)]$$  (1.9)

Thus, the voltage signal across the strip is with $3\omega$ frequency:

$$V(t) = R(t)I(t) = R_0 I_0 \cos(\omega t) + \frac{1}{2} R_0 I_0 \alpha \Delta T_0 \cos(\omega t + \phi) + \frac{1}{2} R_0 I_0 \alpha \Delta T_0 (3\omega t + \phi)$$  (1.10)

The first term is just the normal ac voltage across the metal strip and lacks any thermal information. The other two terms that induced by mixing the current at frequency $\omega$ with the resistance oscillations at frequency $2\omega$, which contain thermal information of the thin film below the metal strip. Because the second term is at the same frequency as the current, it is difficult to extract. Thanks to the lock-in amplifier, the $3\omega$ signal can be extracted [59]. Depending on the width of the strip, both in-plane and cross-plane thermal conductivity can be measured by an approximate
analytical expression. If the width of the strip is small enough to ensure the penetration depth, and 

\[ L_p = \sqrt{\frac{\alpha}{2 \omega}} \]

is much larger than half the width, the material underneath can be treated as isotropic and the heat source can be treated as a line source. The temperature increase of the strip can be expressed as [56, 60]:

\[
\Delta T_S = \frac{p}{\pi L k_S} \left[ 0.5 \left( \frac{\alpha}{a^2} \right) - 0.5 \ln(\omega) + m \right] - i \left( \frac{p}{4 L k_S} \right) \quad (1.11)
\]

Thus, the temperature increase is a linear function of \( \ln(\omega) \) and the slope can be used to derive thermal conductivity.

One drawback of this method is that the preparation process includes deposition of the metallic strip, which is used as heater and sensor. Another challenge is that the measured surface should be electrically isolated; if not, additional insulating materials need should be added between the strip and the sample, which inevitably influence its sensitivity and accuracy. It should also be noted that this is a surface characterization method, and thus can only measure the thermal conductivity right below the metal strip [61]. Finally, for unknown materials one must first determine specific heat and density, which increase the complexity of the test.

### 1.2.5 Transient thermo-reflectance (TTR) technique

The transient thermo-reflectance technique (TTR) technique, which is a non-contact and non-destructive optical method, is used to measure thermal properties such as thermal conductivity and heat capacity of both bulky and thin-film materials. Typically, samples are coated with a thin metal film as shown in Fig. 1.6. When a pump beam is injected into the sample, the temperature at the transducer increases, which alters the reflectance of the laser. This approach enables one to obtain thermal information by monitoring changes in reflectance. This method can be classified by two categories: the time-domain thermoreflectance (TDTR) and frequency-domain thermoreflectance (FDTR). TDTR is implemented by detecting the reflectance change as a function of time delay.
between the pump and probe beam. FDTR is implemented by detecting the reflectance change as a function of the modulated frequency of the pump beam. The standard measurement scheme is illustrated in Fig. 1.7 [62-65]. The pulsed laser has a frequency of $\omega_s$ and is modulated into a sinusoidal signal with frequency of $\omega_0$. The surface thermoreflectance response $Z$ at modulation frequency $\omega_0$ is expressed as:

$$Z(\omega_0, \tau_d) = V_{in} + iV_{out}$$ \hspace{1cm} (1.12)

where $V_{in}$ represents the change of surface temperature, and $V_{out}$ represents the sinusoidal heating of the sample at frequency $\omega_0$. For TDTR:

$$Z(\omega_0, \tau_d)_{TDTR} = \beta \frac{2\pi}{\omega_s} \sum_{n=0}^{\infty} h(n \frac{2\pi}{\omega_s} + \tau_d) e^{-i\omega_0 (n\tau_s + \tau_d)}$$ \hspace{1cm} (1.13)

For FDTR:

$$Z(\omega_0, \tau_d)_{FDTR} = \beta \sum_{l=-\infty}^{\infty} H(l\omega_s + \omega_0) e^{il\omega_d\tau_d}$$ \hspace{1cm} (1.14)

$h(\tau_d)$ and $H(\omega_0)$ are functions of thermal conductivity and thermal and heat capacity, which can be determined by $\phi = \arctan(V_{out}/V_{in})$. By curve fitting the measured data into the equation, thermal properties of different layers can be derived [66, 67].

![Fig. 1.6. Schematic for the transient thermo-reflectance technique.](image)
The main drawback of this approach lies in the complexity of the steps needed to derive thermal properties. To calculate thermal conductivity, for example, one first must obtain specific heat and density, which will add to the intricacy of this approach—especially for unknown materials. Another challenge is that the samples need to be coated with a metal film, which is the transducer to transfer the thermal information to optical signals, which also increases the difficulty and limits operation condition.

Fig. 1.7. Illustration of TDTR measurement.
1.2.6 Structure function analysis method

The so-called structure function analysis method is a non-destructive approach based on evaluating the transient thermal response of an IC package, which depicts a detailed heat-flow map of the package structure [68-70]. As shown in Fig. 1.8, the heat-flow map shows how thermal capacitance accumulated against the increase of thermal resistance along heat flow path and subsequent interpretation of the heat-flow map will establish the thermal resistance and capacitance of each component. The key point of this method is to accurately and rapidly record the transient thermal response of the package [71]. To satisfy requirements for accuracy and recording speed, the electrical based method is typically used, which involves attaching a semiconductor to the package. The semiconductor serves to heat up device, but also can be used as a temperature sensor by utilizing its temperature-sensitive parameter [72]. In so doing, the transient thermal response, usually referred to as thermal impedance, can be recorded and then transferred to structure function plot.

The challenge of this method is that, conventionally, the semiconductor is bonded on the sample—indicating that the characterization location is fixed. This means that it is difficult to obtain a spatial-resolved characterization of thermal properties.

Fig. 1.8. Schematic of structure function analysis and its interpretation.
1.3 Significance and objectives

The increasing demand for high-power density devices requires good TIMs to lower thermal resistance of the package. As reviewed in Chapter 1.1.2, currently available TIMs tend to suffer from reliability issues, which increase thermal resistance after high-temperature operation. The other principal drawback of today’s TIMs is that they can be challenging to process on relative large areas—the result of which will be the introduction of hot spots upon preparation. Therefore, it is essential to develop effective thermal characterization technique to spatial-resolved and non-destructively characterize the thermal resistance of thermal interface materials. TABLE 1-1 provides a comparison of these various approaches. Structure function method can non-destructively characterize thermal resistance, which makes is more desirable. However, the main drawback of structure-function analysis method is that it is difficult to obtain accurate spatial-resolved characterization. In short, there is a pressing need to modify the structure function method with the goal of extending its application to spatial-resolved characterization. As illustrated in Fig. 1.9, we proposed the thermal sensor concept, which is a device packaged with a semiconductor that can be moved freely on the sample, and enable multiple measurements. In this dissertation, several issues focused on the design and application of the thermal sensor were investigated.

Performance of the sensor is usually addressed by sensitivity, which is the ability of a sensor to detect the thermal resistance change induced by defects. The sensitivity is influenced by heat flux distribution in interface layer and its corresponding effect area of heat transfer. In this dissertation, an analytical model is proposed for evaluating the effects of different parameters on heat flux and effective area. Compared with the finite element analysis (FEA) simulation, the analytical model significantly reduces the computing time and can be operated by free software.
Fig. 1.9. Schematic of the movable thermal sensor.

### TABLE 1-1. COMPARISON OF DIFFERENT THERMAL CHARACTERIZATION METHOD

<table>
<thead>
<tr>
<th>Thermal characterization method</th>
<th>Measurement depth (mm)</th>
<th>Measurement time (s)</th>
<th>Properties to measure</th>
<th>Destructive?</th>
<th>Spatial-resolved?</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comparative steady-state technique</td>
<td>10-100</td>
<td>500</td>
<td>Thermal resistance</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Laser flash method</td>
<td>0.1-10</td>
<td>1</td>
<td>Thermal diffusivity</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Transient plane source method</td>
<td>1-100</td>
<td>1</td>
<td>Thermal conductivity</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>$3\omega$ method</td>
<td>0.0001-0.1</td>
<td>0.1</td>
<td>Thermal conductivity</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Transient thermo-reflectance technique</td>
<td>0.0001-10</td>
<td>0.0000001</td>
<td>Thermal diffusivity</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Structure function method</td>
<td>NA</td>
<td>200-1000</td>
<td>Thermal resistance</td>
<td>No</td>
<td>Partially</td>
</tr>
</tbody>
</table>

However, characterization of $R_{th}$ using the movable thermal sensor may be inaccurate when it approaches to the edge, named the edge effect. This is because the heat flux bounds back at the
edge boundary, which decreases the heat spreading area and increases the thermal resistance [73]. So there is limitation of thickness and thermal conductivity for the test coupons.

The working principle, which is structure function analysis of thermal impedance, is evaluated. It is important that before assembling the sensor, the conventional structure function analysis as well as thermal impedance measurement is accurate and sensitive enough to detect the thermal degradation in the interface layer. The measured values were then compared with the simulation values, the models of which were extracted from failure modes analysis from SEM and X-ray images. It showed both thermal impedance measurement and structure function analysis can accurately detect the thermal degradation in the interface layer induced by defects.

As mentioned earlier, spatial-resolved thermal resistance characterization for large area interface is desired. In this dissertation, we used the thermal sensor to 2-d map the thermal resistance of interfaces bonded by different kinds of materials. Results show the sintered silver has lower thermal resistance than thermal grease. Sensitivity of the thermal sensor is also evaluated to determine the defect size limitation for the sensor to detect.

### 1.4 Outline of dissertation

This dissertation details the design, fabrication, evaluation, and application of a movable thermal sensor based on structure function analysis technique, which is intended to non-destructively generate a 2-d mapping of the thermal resistance of TIMs.

Chapter 2 addresses the design of the sensor to increase its sensitivity and accuracy. To control heat flux density with the goal of manipulating the sensitivity of the thermal sensor, a 3-d analytical thermal model was constructed by deriving the analytical solution for the 3-d heat transfer equation. The analytical solution was obtained by separating the variables, after which the unknown coefficients were calculated using Fourier expansions of the boundary conditions. The analytical
model was verified using finite element analysis (FEA), of which the error was below 1 %. Six parameters including size of the semiconductor chip, thermal conductivity of sensor substrate, thickness of sensor substrate, footprint of sensor substrate, size of heat sink, and thermal resistance of between heat sink and test coupon, were evaluated and modified. Subsequently, the prototype of the movable thermal sensor was fabricated.

Chapter 3 provides the accuracy and sensitivity validation of the working principle of the thermal sensor: the transient thermal impedance measurement and its structure function analysis. To conduct thermal impedance measurement, a lab-built circuit board and the LabVIEW setup were used to control the input power and record the temperature response of the semiconductor junction. Due to its high temperature sensitivity (about 10 mV/K), gate-to-emitter voltage was utilized as the temperature-sensitive parameter to measure the temperature response. The application and validation of the thermal impedance measurement was demonstrated by testing the thermal impedance of samples assembled by silver sintering on both AlN-DBA and Si₃N₄-AMB substrates. The samples were temperature cycled between -55°c to 250 °C, after which failure were found in sintered silver interface. Meantime, we found an increase of thermal impedance against temperature cycling. To investigate the accuracy of the thermal impedance measurement, we conducted failure modes analysis by scanning electron microscope (SEM) and X-ray scanning and observed two failure modes - the vertical oriented crack and the horizontal oriented crack – in sintered silver interface layer. The sintered silver interface of the Si₃N₄-AMB sample displayed only horizontal cracks, while the interface of the AlN-DBA sample showed relatively fewer horizontal cracks but some vertical cracks. Subsequent FEA thermal simulation on the impact of the two types of cracks on thermal impedance showed good agreement with measured results, which verified the accuracy of the thermal impedance measurement.
Subsequently, conventional structure function analysis was conducted via the evaluation of transient thermal impedance. To demonstrate the accuracy of measuring interface thermal resistance, structure function analysis was applied on the sintered silver bonded sample. The measured thermal resistance is consistent with the reference value, which verified the accuracy of thermal resistance measurement using structure function approach. To examine the sensitivity of structure function approach in detecting the thermal degradation in TIM layer, we measured the thermal resistance of sintered silver layer with purposely implanted defects. The results showed good agreement with anticipated outcomes, which verified the sensitivity of the structure function analysis approach.

Chapter 4 illustrates the application and evaluation of the movable thermal sensor for measuring the interface thermal resistance. Prior to the measurement, the edge effect was evaluated using the analytical thermal model, with results confirming that the error caused by edge effect was no greater than 0.46%. We demonstrated the use of the movable-probe technique for 2d-mapping of the interface thermal resistance of a large-area bonded substrate. Test coupons bonded by thermal grease and sintered silver were fabricated and then characterized by the thermal sensor. Experimental results showed that the interface thermal resistance for thermal grease and sintered silver were 0.199 K/W, with a deviation of 0.005 K/W (2.5%) and 0.073 K/W, with standard deviation of 0.005 K/W (6.8%), respectively. This data confirmed good and uniform bonding quality for the large-area bonded sintered silver interface layer. To investigate the sensitivity of the thermal sensor for detecting defects/heat channels of differing sizes, test coupons were fabricated by implanting Kapton tape or thermal grease windows of various dimensions into the thermal interface layers. The 2-d mapping confirmed that the thermal sensor was able to successfully detect defect/heat channel sizes as small as 2x2 mm². The accuracy of the sensitivity
was verified by FEA simulation. Moreover, the shapes of the simulated results were consistent with the measured results, which indicates that the movable sensor is accurate for assessing interface thermal resistance.

Chapter 5 is the summary of this work and suggestions for future work. The main contributions of this dissertation is:

1. A movable thermal sensor concept was proposed and realized. For test coupon made by copper with thickness of 2 mm, the sensor can be applied to 2-d map of interface thermal resistance, with error of 0.01 K/W (95% confidence interval), and can detect defect size larger than 1 mm². To avoid edge effect, there are limitations for thickness and thermal conductivity of the test coupon. Generally, test coupon made by a more thermally conductive material or with smaller thickness has a less severe edge effect. To increase the sensitivity and resolution of the sensor, one can decrease the size and thickness of the sensor substrate, size of the sensor chip, thermal conductivity of the sensor substrate, or size of the heat sink.

2. An analytical thermal model was proposed. The model predicts the temperature distribution, thermal resistance, and heat flux distribution, and effective heat spreading area. Because the sensitivity and resolution of the thermal sensor highly dependent on the heat flux and effective heat spreading area, the analytical thermal model was used to design and modify the performance of thermal sensor. It was found the sensitivity and resolution of the sensor can be improved by decreasing one or more of the following parameters: chip size, sensor substrate size, sensor substrate thickness, sensor substrate thermal conductivity, and heat sink size.
3. During evaluation of thermal impedance, reliability of the sintered silver attachment on 
$\text{Si}_3\text{N}_4$ AMB and AlN DBA substrates were characterized. Because of larger thermal stress, 
horizontal oriented cracks were mainly observed in $\text{Si}_3\text{N}_4$ AMB sintered silver attachment, 
which was the major contribution to the thermal degradation. In contrary, because of 
smaller thermal stress, very little horizontal cracks were observed in AlN DBA sintered 
silver attachment. However, the larger surface roughness of DBA resulted in severe 
vertical cracks. It is found that the vertical cracks contribute very little to the thermal 
degradation.
Chapter 2. SENSITIVITY IMPROVEMENT OF THE MOVABLE THERMAL SENSOR BY ANALYTICAL THERMAL MODELLING

This chapter primarily describes an analytical thermal model for the design of the sensor. In this section, we mainly talked about the sensitivity and resolution of the sensor. The sensitivity of the sensor is defined as the smallest change of thermal resistance a sensor can detect as indicated in equation 2.34. The resolution of the sensor is defined as the capability of the sensor to distinguish the defect of a given type.

Although the package of the sensor allows it to move free on the test coupon, its substrate serves as a buffer layer that enhances the heat spreading. This heat spreading decreases the contribution of the interface layer to the temperature response of the semiconductor chip, and thus decreases overall sensitivity and resolution. The design process is mainly focused on concentrating the heat flux over the interface layer to increase the resolution of the movable thermal sensor.

2.1 Modification of structure function analysis test setup

2.1.1 Literature review of the effect of heat spreading on structure function analysis

In power devices, buffer layers are usually used to increase the heat spreading and decrease the transient and steady-state thermal resistance. However, in structure function analysis, heat spreading makes it difficult to evaluate the thermal properties of the deeper structure. Accordingly, the heat spreading effect on structure function analysis was investigated, as reported in [74]. Fig. 2.1 (a) shows the structure for simulation, which consisted of a sample footprint of 5 mm x 5 mm, with four Si dies and four layers glued on each other. Transient thermal simulation was conducted
to derive the Zth data, which was further transformed to a differential structure function plot. The thermal conductivity of the Si dies and glue were 100 W/mK and 1 W/mK, respectively. In the differential structure function plot, the peaks represent the layer with high thermal capacitance but low thermal resistance, which corresponds to the Si die layer. One can read the thermal resistance of the glue layer between two peaks. By changing the thermal resistance of the second glue layer from 1 W/mK to 0.75 W/mK, the third peak shifts, from which one can detect the thermal resistance increase in the second glue layer via structure function analysis, as shown in Fig. 2.1 (b). However, when the thermal conductivity of the third glue layer changes, it is hard to identify the shift of the fourth peak as shown in Fig. 2.1 (c). The low sensitivity of structure function to characterize the third glue layer is caused by heat spreading.
Fig. 2.1. Influence of heat spreading on structure function analysis. (a) schematic of sample, (b) comparison of differential structure function of different second glue layer, and (c) comparison of differential structure function of different third glue layer. [73]
2.1.2 Modification of test setup

Heat spreading decreases heat flux density in a given layer. Based on the following definition of thermal resistance:

\[ \Delta T = R_{th} \times P = q \frac{d}{k} \]  

(2.1)

in which \( R_{th} \) is thermal resistance; \( P \) is the power; \( q \) is heat flux density; \( d \) is thickness; \( k \) is thermal conductivity. Smaller heat flux density affords a smaller temperature difference across the test coupon. In other words, the thermal sensor is less sensitive to any changes in thermal resistance when applied with a smaller heat flux density. To overcome this issue, we decreased the heat sink contact area, as shown in Fig. 2.2 (a). The smaller contact area of the heat sink narrows the heat flux and thus decreases heat spreading. Fig. 2.2 (b) shows the comparison of heat flux density using big and small heat sink contact area. The heat flux density in the test coupon became larger when changed to smaller heat sink.

![Comparison of heat flux density](image)
2.2 Analytical thermal model

To control heat flux density with the goal of manipulating the resolution of the thermal sensor, a three-dimensional analytical thermal model was proposed. The solution of this model generates the steady-state temperature distribution within the thermal sensor and test coupon, from which we can calculate the heat flux density in order to guide the sensor design. Another function of the model is to calculate the thermal resistance distribution, which can help to evaluate the edge effect.

2.2.1 Introduction of analytical thermal model

The steady state temperature response of a package can generally be evaluated by two means: FEA thermal simulation and analytical thermal modelling. The FEA thermal simulation approach generates a numerical solution that can be used to simulate the relative complex structure. The principal drawback of the FEA approach is that it can be time consuming; a reasonable simulation will take from several tens to several hundred seconds. For parametric analysis with multiple input variables, it is hard to effectively derive the results—not to mention the try-and-error process.
An analytical thermal model was constructed based on the solution of heat transfer equation. Typically, the model structure is usually simplified for ease of calculation, and thus is relatively efficient for deriving temperature distribution using available software (e.g., C++, Python, MATLAB, etc.) within seconds. M. Krane provided a solution of centric heat source on isotropic sample[75]; Y. S. Muzychka and M. Yovanovich reported the solution of multiple rectangular heat sources on a multi-layer rectangular sample with heat convection[76-78]; P. Wang reported the solution of centric heat source on isotropic sample with both convection and power dissipation[79]. However, in our case, both the sensor and the heat sink need to move around the test coupon and the positions of the sensor and heat sink are eccentric. In addition, there is also air convection at the boundary. So all these methods are not suitable for our case, which contains both eccentric heat source, eccentric power dissipation, and heat convection. In this work, we extended the application of analytical thermal model and derived the solution for eccentric heat source on simplified isotropic samples with both heat convection and eccentric power dissipation.

### 2.2.2 Thermal model for movable thermal sensor test system

In this section, we describe the thermal sensor and test coupon, which were modeled separately and then thermally coupled with each other. The input parameters of the model are shown in Fig. 2.3. The nomenclature definitions are listed as follows:

- \( c \) and \( d \): Size of the semiconductor chip
- \( a \) and \( b \), and \( t_1 \): Size of copper substrate
- \( X_{ch} \) and \( Y_{ch} \): Location of chip
- \( k_1 \): Thermal conductivity of sensor substrate
- \( X_h \) and \( Y_h \): Location of sensor
- \( h_{off} \): Heat convection of the test coupon
- \( e, f, \) and \( t_2 \): Size of the test coupon
- \( k_2 \): Thermal conductivity of test coupon
- \( a' \) and \( b' \): Size of heat sink
- \( X_c \) and \( Y_c \): Location of heat sink
- \( h_c \): Heat convection between sensor and coupon
(1) Analytical thermal model for the thermal sensor

The thermal sensor was composed of a Si IGBT chip, substrate, electrodes, and case. To simplify the modelling work, we chose to eliminate the electrodes and case since these parts feature low thermal capacity and low thermal resistance. Thus, in both the steady and transient state, their influence on the thermal performance of the package is negligible. The analytical thermal model for thermal sensor was simplified and illustrated in Fig. 2.4, where $P$ is the input power; $c$ and $d$ are the dimension of Si chip; $a$ and $b$ are the dimension of thermal sensor; $X_{ch}$ and $Y_{ch}$ are coordinate of chip center; $t_1$ is the thickness of thermal sensor; $k_1$ is the thermal conductivity; and $T_{ref}$ is the average temperature of top surface of test coupon. We assumed that the power would be uniformly injected into the thermal sensor, given that the relatively high thermal conductivity and low profile ensure a uniform heat flux distribution within the Si chip. Additionally, heat dissipation through the bottom of the sensor was also assumed as heat convection with coefficient of $h_c$. 

Fig. 2.3. Schematic of thermal model for movable sensor and test coupon.
Based on the work by Muzychka et al. [78], the governing equation of temperature $T_{tp}$ for the thermal sensor is a Poisson’s equation:

$$\nabla^2 T_{tp} = \frac{1}{k} \left[ \frac{\partial^2 T_{tp}}{\partial x^2} + \frac{\partial^2 T_{tp}}{\partial y^2} + \frac{\partial^2 T_{tp}}{\partial z^2} \right] + \frac{Q_v}{k} = 0 \quad (2.2)$$

where $Q_v$ is the power density distribution. In most cases, heat flux through the chip is uniformly distributed on top of chip. Thus, we can replace $Q_v$ with a uniform heat flux $q = P/cd$ at the $z = 0$ surface, which was established as the boundary condition. Accordingly, the problem can be described using Laplace’s equation:

$$\nabla^2 T_{tp} = \frac{\partial^2 T_{tp}}{\partial x^2} + \frac{\partial^2 T_{tp}}{\partial y^2} + \frac{\partial^2 T_{tp}}{\partial z^2} = 0 \quad (2.3)$$

The boundary condition on top surface of substrate can be written as:

$$\left. \frac{\partial T_{tp}}{\partial z} \right|_{z=0} = -\frac{P}{cdk_1} \quad ; \quad \text{inside heat source area}$$

$$\left. \frac{\partial T_{tp}}{\partial z} \right|_{z=0} = 0 \quad ; \quad \text{outside heat source area} \quad (2.4)$$

The boundary condition at the edge can be written as:
\[
\frac{\partial T_{tp}}{\partial x} \bigg|_{x=0,a} = 0
\]
\[
\frac{\partial T_{tp}}{\partial y} \bigg|_{y=0,b} = 0
\]

(2.5)

The boundary condition at the bottom surface of substrate can be written as:

\[
\frac{\partial T_{tp}}{\partial z} \bigg|_{z=t_1} = -\frac{h_c}{k_1} (T_{tp} - T_{ref})
\]

(2.6)

In our case, the thermal sensor was placed on a test coupon, which can be treated as a heat spreader, so the value of \( h_c \) can be calculated by:

\[
h_c = \frac{1}{A_{conta} R_{int}}
\]

(2.7)

in which the \( A_{conta} \) is the contact area, and \( R_{int} \) is the thermal interface resistance between the sensor and test coupon.

The analytical solution of the steady-state temperature distribution in this case can be derived by separating the variables, with the assumption that the general solution has the form of \( T_{tp}(x,y,z) = X(x) \times Y(y) \times Z(z) \). By applying the boundary condition (3.4) and (3.5), we can derive the general solution of Laplace’s equation accordingly:

\[
T_{tp}(x,y,z) = T_{ref} + A_{00} + B_{00}z + \sum_{m=1}^{\infty} \cos(\lambda x) [A_{m0} \cosh(\lambda z) + B_{m0} \sinh(\lambda z)] \\
+ \sum_{n=1}^{\infty} \cos(\delta x) [A_{0n} \cosh(\delta z) + B_{0j} \sinh(\delta z)] \\
+ \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \cos(\lambda x) \cos(\delta x) [A_{mn} \cosh(\gamma z) + B_{mn} \sinh(\gamma z)]
\]
where \( \lambda = m\pi/a, \delta = n\pi/b, \) and \( \gamma = \sqrt{\lambda^2 + \delta^2} \) are the eigenvalues. To obtain the unknown constants, we applied the boundary condition at \( z = t_1 \) and got

\[
B_{mn} = -\varnothing(\xi)A_{mn} \text{ and } \xi \in (\lambda, \delta, \text{ and } \gamma); \text{ when } mn \neq 0
\]

\[
B_{00} = -(t_1 + \frac{k_1}{h_c})A_{00}; \text{ when } mn = 0
\]  

(2.9)

where

\[
\varnothing(\xi) = \frac{\xi \sinh(\xi t_1) + \frac{h_c}{k_1} \cosh(\xi t_1)}{\xi \cosh(\xi t_1) + \frac{h_c}{k_1} \sinh(\xi t_1)}
\]  

(2.10)

By considering Fourier series expansion of the boundary condition at \( z = 0 \), we obtained the Fourier coefficient:

\[
B_{00} = -\frac{p}{k_1 ab}
\]  

(2.11)

\[
B_{m0} = -\frac{4P \sin\left(\frac{\lambda}{2}\right) \cos(X_{ch}\lambda)}{abc k_1 \lambda^2}
\]  

(2.12)

\[
B_{0n} = -\frac{4P \sin\left(\frac{\delta}{2}\right) \cos(Y_{ch}\delta)}{abcd k_1 \delta^2}
\]  

(2.13)

\[
B_{mn} = -\frac{16P \sin\left(\frac{\lambda}{2}\right) \cos(X_{ch}\lambda) \sin\left(\frac{\delta}{2}\right) \cos(Y_{ch}\delta)}{abc d k_1 \lambda \delta \gamma}
\]  

(2.14)

The application of the analytical model including calculating the temperature distribution, thermal resistance, and heat flux distribution. Detailed work will be presented in the following sections.

(2) Analytical thermal model for test coupon

To simplify the modelling work for the test coupon, we firstly assumed that the power would be uniformly injected from the top surface of test coupon within the sensor footprint. Of course,
this does not occur in actuality; thus, the issue of the non-uniformity of heat flux will be considered later using the superposition method. The injected power will be dissipated via the heat sink and air convection. Based on experience, the power dissipated by air convection is about 10%, while the remaining power is dissipated via the heat sink. The thermal model of the test coupon is shown in Fig. 2.5, where \( e \) and \( f \) represent the dimensions of the test coupon (which was simplified as an isotropic rectangular plate with thermal conductivity of \( k_z \)); \( a \) and \( b \) represent the dimensions of the heat source area, which is also the size of thermal sensor; and \( X_h \) and \( Y_h \) serve as the coordinates for the center of the heat source. \( P \) represents the power injection, which is assumed to be the same as the power on IGBT chip; \( a' \) and \( b' \) represent the dimensions of the heat sink, and \( X_c \) and \( Y_c \) signify the coordinates for the center of the heat sink. \( P' \) represents the power dissipation through the heat sink, and \( h_{eff} \) is the effective air convection coefficient at the bottom surface. \( T_r \) indicates room temperature.

The governing equation for this structure is also a Laplace’s equation, as follows:

\[
\nabla^2 T_{tc}(x, y, z) = \frac{\partial^2 T_{tc}}{\partial x^2} + \frac{\partial^2 T_{tc}}{\partial y^2} + \frac{\partial^2 T_{tc}}{\partial z^2} = 0
\]

The boundary condition on the top surface of the test coupon can be written as:

\[
\frac{\partial T_{tc}}{\partial z} \bigg|_{z=0} = -\frac{P}{k_z ab} ; \text{ inside heat source area}
\]
The boundary condition on the bottom surface of the test coupon can be written as:

$$\frac{\partial T_{tc}}{\partial z} \bigg|_{z=0} = 0 \quad ; \quad \text{outside heat source area} \quad (2.16)$$

The boundary condition at the edge can be written as:

$$\frac{\partial T_{tc}}{\partial x} \bigg|_{x=0,e} = 0 \quad (2.18)$$

$$\frac{\partial T_{tc}}{\partial y} \bigg|_{y=0,f} = 0 \quad (2.19)$$

Similar to the method used in the thermal sensor model, we were able to obtain the general solution for the test coupon in the form of:
\[ T_{tc}(x, y, z) = T_r + F_{00} + E_{00}z + \sum_{m=1}^{\infty} \cos(\lambda x) \left[ F_{m0} \cosh(\lambda z) + E_{m0} \sinh(\lambda z) \right] \]

\[ + \sum_{n=1}^{\infty} \cos(\delta x) \left[ F_{0n} \cosh(\delta z) + E_{0j} \sinh(\delta z) \right] \]

\[ + \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \cos(\lambda x) \cos(\delta x) \left[ F_{mn} \cosh(\gamma z) + E_{mn} \sinh(\gamma z) \right] \]

(2.20)

The eigenvalue here is presented by the dimension of the test coupon and replaced to \( \lambda = m\pi/e \), \( \delta = n\pi/f \). By determining the Fourier series expansion at the boundary condition at \( z = 0 \), we obtained the following Fourier coefficient:

\[ E_{00} = \frac{P}{k_2 e f} \]  

(2.21)

\[ E_{m0} = \frac{4P \sin\left(\frac{a\lambda}{2}\right) \cos(X_h \lambda)}{ef a k_2 \lambda^2} \]

(2.22)

\[ E_{0n} = \frac{4P \sin\left(\frac{b\delta}{2}\right) \cos(Y_h \delta)}{ef b k_2 \delta^2} \]

(2.23)

\[ E_{mn} = \frac{16P \sin\left(\frac{a\lambda}{2}\right) \cos(X_h \lambda) \sin\left(\frac{b\delta}{2}\right) \cos(Y_h \delta)}{ef a b k_2 \lambda \delta \gamma} \]

(2.24)

By obtaining the Fourier series expansion at the boundary condition at \( z = t_2 \), we obtained the following coefficient:

\[ F_{00} = -\left( t_2 + \frac{k_2}{h_{\text{eff}}} \right) E_{00} - \frac{P'}{ef h_{\text{eff}}} \]

(2.25)

\[ F_{m0} = -\frac{\lambda \cosh(\lambda t_2) + \frac{h_{\text{eff}}}{k_2} \sinh(\lambda t_2)}{\lambda \sinh(\lambda t_2) + \frac{h_{\text{eff}}}{k_2} \cosh(\lambda t_2)} E_{m0} - \frac{4P' \sin\left(\frac{a'\lambda}{2}\right) \cos(X_c \lambda)}{ef a' k_2 \lambda} \]

(2.26)
\begin{align}
F_{0n} &= -\frac{\delta \cosh(\delta t_2) + \frac{h_{\text{eff}}}{k_2} \sinh(\delta t_2)}{\delta \sinh(\delta t_2) + \frac{h_{\text{eff}}}{k_2} \cosh(\delta t_2)} E_{0n} - \frac{4P' \sin\left(\frac{b'\delta}{2}\right) \cos(Y \delta)}{efb'k_2\delta} \quad (2.27) \\
F_{mn} &= -\frac{\gamma \cosh(\gamma t_2) + \frac{h_{\text{eff}}}{k_2} \sinh(\gamma t_2)}{\gamma \sinh(\gamma t_2) + \frac{h_{\text{eff}}}{k_2} \cosh(\gamma t_2)} E_{0n} - \frac{16P' \sin\left(\frac{a'\lambda}{2}\right) \cos(X \lambda) \sin\left(\frac{b'\delta}{2}\right) \cos(Y \delta)}{ef a' b' k_2 \delta} \quad (2.28)
\end{align}

(3) Thermal coupling

To determine the actual flux distribution on the top surface of the test coupon, we calculated the heat flux at the bottom surface via thermal sensor, by taking a derivative of temperature

\[ q(x, y, z) = -k_1 \frac{\partial T_{tp}}{\partial z} \]

\[ = -k_1 [B_{00} + \sum_{m=1}^{\infty} \lambda \cos(\lambda x) [A_{m0} \sinh(\lambda z) + B_{m0} \cosh(\lambda z)] + \sum_{n=1}^{\infty} \delta \cos(\delta x) [A_{0n} \sinh(\delta z) + B_{0j} \cosh(\delta z)] + \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \gamma \cos(\lambda x) \cos(\delta x) [A_{mn} \sinh(\gamma z) + B_{mn} \cosh(\gamma z)]] \]

(2.29)

The heat flux at the top surface of the test coupon is shown in Fig. 2.6 (a). Because heat flux is continuous and difficult to be substituted into the analytical thermal model shown in (3.20), we divided the heat flux into eleven discrete heat flux levels, as shown in Fig. 2.6 (b), for ease of calculation. The spacing between two level can be expressed as:

\[ q_{sp} = (q_{\text{max}} - q_{\text{min}})/10 \]

(2.30)

where the base heat flux level is \( q_{\text{min}} \) and the maximum heat flux level is \( q_{\text{max}} \). Each energy level \( q_i \) occupies an analogous rectangular shape with area of \( A_i \), to ensure the following relationship:

\[ q_1 A_1 + \sum_{i=2}^{11} q_i A_i = P \]

(2.31)
where \( q_1 = q_{\text{min}} \) and \( q_{i=2,3...11} = q_{sp} \). Then based on (3.20), by replacing \( P \) with \( P_i = q_i \times A_i \) and \( P'_i = P'/11 \), the solution can be obtained using superposition method [76]. The temperature distribution can be expressed as:

\[
T_{tc}(x, y, z) - T_r = \sum_{i=1}^{11} (T_i - T_r)
\]  

(2.32)

Accordingly, one can easily obtain the average temperature in the heat source area, \( \bar{T} \), via the following equation:

---

Fig. 2.6. (a) Heat flux density distribution at the bottom surface of thermal sensor and (b) analogous flux level.

---

Accordingly, one can easily obtain the average temperature in the heat source area, \( \bar{T} \), via the following equation:
\[ \bar{T} = \frac{1}{ab} \iint T_{tc}(x, y, 0) dA \]

\[ = T_r + F_{00} + 2 \sum_{m=1}^{\infty} F_{m0} \frac{\cos(\lambda X) \sin(\frac{1}{2} \lambda a)}{\lambda a} \]

\[ + 2 \sum_{n=1}^{\infty} F_{0n} \frac{\cos(\delta Y) \sin(\frac{1}{2} \delta b)}{\delta b} \]

\[ + 4 \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} F_{mn} \frac{\cos(\lambda X) \sin(\frac{1}{2} \lambda a) \cos(\delta Y) \sin(\frac{1}{2} \delta b)}{\lambda a \delta b} \]

(2.33)

which is the reference temperature, \( T_{ref} \) in the analytical thermal sensor model (3.8). Then, the solution can be calculated by summation of 100 terms. The Python codes to derive the analytical models are listed in Appendix A.

### 2.2.3 Validation of our analytical thermal model

FEA thermal simulation was conducted by ANSYS workbench to compare our findings with the analytical solution. The dimensions and material properties for both the simulation model and our analytical model are identical, as shown in TABLE 2-1.

Fig. 2.7 (a) and (b) displays the steady-state temperature distribution derived from the analytical model and the FEA simulation, respectively. The calculated difference in the hot spots between the two methods was less than 1%, which verified the accuracy of the analytical model. Therefore, this model can be used to guide the design of the thermal sensor, as well as to identify the appropriate area for avoiding undesirable effects, such as the edge effect which extrinsically increases thermal resistance between the top and bottom surfaces.
Fig. 2.7. Comparison of temperature distribution on top surface of test coupon: (a) analytical modeling solution and (b) FEA simulation.
<table>
<thead>
<tr>
<th>$a$</th>
<th>8 mm</th>
<th>$b$</th>
<th>10 mm</th>
<th>$c$</th>
<th>5 mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>$d$</td>
<td>3 mm</td>
<td>$e$</td>
<td>25 mm</td>
<td>$f$</td>
<td>50 mm</td>
</tr>
<tr>
<td>$a'$</td>
<td>10 mm</td>
<td>$b'$</td>
<td>10 mm</td>
<td>$X_{ch}$</td>
<td>6 mm</td>
</tr>
<tr>
<td>$Y_{ch}$</td>
<td>4 mm</td>
<td>$X_h$</td>
<td>15 mm</td>
<td>$Y_h$</td>
<td>15 mm</td>
</tr>
<tr>
<td>$X_c$</td>
<td>15 mm</td>
<td>$Y_c$</td>
<td>15 mm</td>
<td>$t_1$</td>
<td>0.2 mm</td>
</tr>
<tr>
<td>$t_2$</td>
<td>3 mm</td>
<td>$k_j$</td>
<td>400 W/mK</td>
<td>$k_2$</td>
<td>100 W/mK</td>
</tr>
<tr>
<td>$h_c$</td>
<td>20000 W/m$^2$K</td>
<td>$h_{eff}$</td>
<td>20 W/m$^2$K</td>
<td>$P$</td>
<td>20 W</td>
</tr>
<tr>
<td>$P'$</td>
<td>18 W</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 2.3 Design of movable thermal sensor

#### 2.3.1 Design principle

Sensitivity of the thermal sensor is the ability of the sensor to detect the defects. Here we define the sensitivity as the thermal resistance change caused by the defect:

$$S = R' - R^0 = \alpha \frac{A_d}{A_{eff}}$$ (2.34)

Where $R'$ is the thermal resistance with defect; $R^0$ is the thermal resistance without defect; $A_d$ is the area of defect; $A_{eff}$ is the effect area of heat transfer; and $\alpha$ is a coefficient dependent on thermal resistance difference between interface material and its defect. The lowest $A_d$ the sensor can detect is the resolution. Heat spreading increases the effective area. So to increase the sensitivity, one needs to reduce heat spreading and decrease the effective area. Generally, the error is 95% confidence interval, which is about twice the standard deviation [80]. In Chapter 4, we derived the
standard deviation of the measurement is 0.005 K/W. So the error for this technique is about 0.01 K/W.

One can derive the heat flux at a given layer by obtaining the derivative on the temperature function of test coupon using the following equation:

\[ q(x,y,z) = -k_2 \frac{\partial T_{tc}}{\partial z} \]

\[ = -k_2 \left[ E_{00} + \sum_{m=1}^{\infty} \lambda \cos(\lambda x) \left[ F_{m0} \sinh(\lambda z) + E_{m0} \cosh(\lambda z) \right] \right. \]

\[ + \left. \sum_{n=1}^{\infty} \delta \cos(\delta x) \left[ F_{0n} \sinh(\delta z) + E_{0j} \cosh(\delta z) \right] \right] \]

\[ + \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \gamma \cos(\lambda x) \cos(\delta x) \left[ F_{mn} \sinh(\gamma z) + E_{mn} \cosh(\gamma z) \right] \}

(2.35)

One can also derive the average effective area of a component based on the following equation:

\[ R_{th} = \frac{\Delta T}{P} = \frac{\Delta t}{kA_{eff}} \]

(2.36)

where \( \Delta T \) is the temperature difference between a component with \( \Delta t \) thickness. When \( \Delta t \) approaches to zero, the effective area \( A_{eff} \) for a given layer \( z \) equals to:

\[ A_{eff}(z) = \frac{P}{k} / \frac{\partial r}{\partial t} \]

(2.37)

in which \( \frac{\partial r}{\partial t} \) can be calculated using equation (3.20).

In the following section, we are going to evaluate the impact of six parameters—(a)size of the semiconductor chip; (b) thermal conductivity; (c)thickness; (d)size of sensor substrate; (e)size of heat sink; and (f) thermal resistance of between heat sink and test coupon—on heat flux and
effective area of the interface layer. Values in TABLE 2-1 were used as the standard value. Note that we changed one variable each time to evaluate its influence on the heat flux and effective area.

2.3.2 Evaluation of different parameters on heat flux density and effective area

(a) Size of semiconductor chip

Fig. 2.8 shows the heat flux distribution and its corresponding effective area at the center of the test coupon (the cross line of plane z=0.5t2 and plane x=Xc). We evaluated the impact of chip size on heat flux and effective area. For chip size of 30 mm², 15 mm², 6 mm², and 3 mm², the corresponding flux peak values were 0.26 W/mm², 0.28 W/mm², 0.29 W/mm², and 0.31 W/mm², respectively. The corresponding effective areas are 76.9 mm², 71.4 mm², 69.0 mm², and 64.5 mm². In other words, a smaller chip afforded a more concentrated heat flux and thus decreases the effective area. However, because of heat spreading effect, when chip size decreased by 5 times from 15 mm² to 3 mm², the heat flux density only increased by 15%, which is not significant. So in this project, we chose the Si IGBT chip (IRG4CH30K), which has been evaluated in Section 2.

![Graph showing heat flux distribution and effective area for different chip sizes.](image_url)

Fig. 2.8. Analytical solution of heat flux density distribution of interface layer for different thermal chip size.
(b) Thermal conductivity of thermal sensor substrate

In Fig. 2.9, we evaluated the impact of thermal conductivity on heat flux distribution. For thermal conductivities of 600 W/mK, 400 W/mK, 200 W/mK, and 50 W/mK, the corresponding flux peak values were 0.27 W/mm², 0.28 W/mm², 0.31 W/mm², and 0.33 W/mm², respectively. The corresponding effective areas are 74.1 mm², 71.4 mm², 64.5 mm², and 60.6 mm². The reason is that low thermally conductive material inhibits the heat spreading which increases heat flux and thus decreases the effective area. It must be noted, however, that poor thermally conductive materials generate larger thermal resistance in the substrate layer, which may cause overheating issues for the package. Here, we used copper as the substrate material. The heat flux for copper is relatively high, and its good thermal conductivity ensures an acceptable operating temperature.

![Graph showing analytical solution of heat flux density distribution of interface layer for different thermal conductivity of substrate.](image)

(c) Thickness of thermal sensor substrate
By changing the sensor substrate from 2 mm to 0.1 mm, we were able to determine the influence of thickness on heat flux distribution, as shown in Fig. 2.10. For a 2 mm substrate, the heat flux peak value was 0.23 W/mm², with the effective area of 86.2 mm². If the substrate was trimmed down to 0.5 mm, 0.2 mm, and 0.1 mm, the thermal flux peak value increased to 0.26 W/mm², 0.28 W/mm², and 0.31 W/mm², respectively. Meantime the effective area decreased to 76.5 mm², 71.4 mm², and 64.9 mm², respectively. The reason is a thinner substrate will decrease heat spreading, and thus increase heat flux and decrease the effective area. On the other hand, a thinner substrate reduces thermal resistance and thus will decrease operating temperature, which may increase reliability. Considering that copper is a rather soft material, to ensure the strength of the substrate we polished the thickness down to 0.2 mm to provide sufficient protection for the internal devices.

![Analytical solution of heat flux density distribution of interface layer for different substrate thickness](image)

Fig. 2.10. Analytical solution of heat flux density distribution of interface layer for different substrate thickness

(d) Size of the thermal sensor
As illustrated in Fig. 2.11, we evaluated the influence of substrate size on heat flux distribution in the test coupon. Our resulting heat flux density values for the sensor substrate size of 120 mm$^2$, 80 mm$^2$, 63 mm$^2$, and 48 mm$^2$ were 0.26 W/mm$^2$, 0.28 W/mm$^2$, 0.30 W/mm$^2$, and 0.31 W/mm$^2$, respectively. The corresponding effective areas were 76.9 mm$^2$, 71.4 mm$^2$, 66.7 mm$^2$, and 64.2 mm$^2$. Thus, a smaller size substrate was shown to increase heat flux density. The size of the substrate is principally limited by the other components, such as the case and electrodes. Consequently, the substrate size utilized herein was 10 mm x 8 mm, which leaves sufficient room for the electrodes and case.

![Graph showing heat flux density distribution](image)

**Fig. 2.11.** Analytical solution of heat flux density distribution of interface layer for different thermal sensor footprint.

(e) Heat sink contact area

As indicated in Fig. 2.12, we evaluated the influence of heat sink size on heat flux distribution in the test coupon. Heat flux density values for heat sink size of 120 mm$^2$, 80 mm$^2$, 63 mm$^2$, and 48 mm$^2$ were 0.25 W/mm$^2$, 0.28 W/mm$^2$, 0.31 W/mm$^2$, and 0.35 W/mm$^2$, respectively. The corresponding effective areas were 81.6 mm$^2$, 71.4 mm$^2$, 65.3 mm$^2$, and 56.9 mm$^2$. That is because
a smaller heat sink contact area will further focus the heat flux distribution and thus increase heat flux and decrease the effective area. It is noticeable that compared with the sensor substrate size, the heat sink size exerts a greater impact on heat flux density. The reason for this relationship is due to the fact that the heat sink serves as the main heat-dissipation path, which dominates the thermal performance of the system. As a result, heat sink size is critical to heat dissipation; thus, the junction temperature of an IGBT chip with a heat sink that is too small may cause overheating issues. Accordingly, the size of the heat sink utilized for this investigation was also 10 mm x 8 mm, which was identical to the sensor substrate. This correspondence makes it easier to align the sensor coaxially with the heat sink, which helps ensure consistent measurement conditions.

![Graph showing heat flux density distribution for different heat sink contact areas](image)

Fig. 2.12. Analytical solution of heat flux density distribution of interface layer for different heat sink contact area.

(f) Thermal resistance between test coupon and heat sink

As illustrated in Fig. 2.13, we evaluated the influence of thermal resistance between heat sink and test coupon on heat flux distribution in the test coupon. By changing the thermal resistance value, the portion of heat dissipation via heat sink and air will change. The heat flux density for
thermal resistance of 200 mm²K/W, 50 mm²K/W, 25 mm²K/W, and 10 mm²K/W resulted in heat flux density values of 0.265 W/mm², 0.275 W/mm², 0.28 W/mm², and 0.285 W/mm², respectively. The corresponding effective areas were 75.4 mm², 72.7 mm², 71.4 mm², and 70.2 mm². In other words, a larger convection coefficient afforded higher heat flux and smaller effective area. It should also be noted that the convection coefficient was impacted by both choice of thermal interface material and applied pressure. To increase the convection, one can use a more thermally conductive material or apply more pressure to the sample. Note that the influence of convection coefficient on heat flux density was very small. By changing the specific thermal resistance from 10 mm²K/W (the case with thermal grease) to 20 mm²K/W, 50 mm²K/W (the case with no thermal grease), and 200 mm²K/W (the case with Kapton tape as thermal interface), effective area only increased by 1.7%, 3.6%, and 7.4%. So even if the heat convection between test coupon and heat sink changes during the move of the sensor, the change of sensitivity of the sensor should be at most 3.6%.

Fig. 2.13. Analytical solution of heat flux density distribution of interface layer for different thermal resistance between heat sink and test coupon.
2.4 Fabrication of movable thermal sensor

Fig. 2.14 shows the fabrication process of a thermal sensor. The design dimensions of the sensor and the heat sink are shown in TABLE 2-2. The substrate of the sensor was fabricated by machining a copper nugget to a rectangular flake with a dimension of 10 mm x 8 mm. The copper substrate was then polished to a thickness of 0.2 mm to decrease thermal resistance and concentrate heat flux. After polishing, the surface roughness of the copper was smaller than 0.1 μm. The value of the contact thermal resistance between sensor and test coupon decreases as the surface roughness decrease, however in this case, the contact thermal resistance is hard to quantify because lack of equipment. An Si IGBT (IRG4CH30K) bare die was attached to the copper substrate by solder. The dimension of the chip was 3 mm x 5 mm x 0.4 mm. The IGBT terminals were then wire-bonded with aluminum wires to the electrode pads. For ease of connecting the sensor to an external circuit, a three-pin connector was soldered on the electrode pads. Finally, the sensor was enclosed in a 3D-printed plastic case for physical protection.

<table>
<thead>
<tr>
<th><strong>TABLE 2-2. DESIGN OF MOVABLE THERMAL SENSOR AND HEAT SINK</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Semiconductor part number</strong></td>
</tr>
<tr>
<td>Semiconductor size</td>
</tr>
<tr>
<td>Thermal sensor size</td>
</tr>
<tr>
<td>Thermal sensor substrate</td>
</tr>
<tr>
<td>Heat sink size</td>
</tr>
<tr>
<td>Electrodes</td>
</tr>
<tr>
<td>Case</td>
</tr>
</tbody>
</table>
The aluminum heat sink was machined to a specific structure to ensure that the contact area of the test coupon would be precisely 10 mm x 8 mm. The heat sink contact area and the sensor size were designed to be the same for ease of alignment during testing. Although the thermal resistance between test coupon and heat sink has only negligible effect on the sensitivity of the sensor, thermal interface material still needs in between. That is because the small heat sink contact area decreases the efficiency of heat dissipation, which increases the overall thermal resistance. Thermal interface material decreases the overall thermal resistance and also helps to maintain a stable measurement environment.

![Fabrication process of movable thermal sensor.](image)

**Fig. 2.14. Fabrication process of movable thermal sensor.**

### 2.5 Edge effect evaluation

The edge effect will occur when the heat source is close to the edge of the package, where the heat flux is inhibited by the edge and thus increases thermal resistance externally [81]. Thus, in order to obtain an accurate intrinsic characterization of a material’s thermal properties, the edge effect must be evaluated and eliminated. To analyze the edge effect influence in one measurement,
we used the analytical thermal model to calculate spatially-resolved thermal resistance. The thermal resistance for a given location on a test coupon can be expressed as:

\[ R_{tc}(x, y) = \frac{T_{tc}(x, y, 0) - T_{tc}(x, y, t_2)}{P} \]  

which represents the temperature difference between the top and bottom surface over input power.

In one measurement, the sensor should completely cover the test coupon, which means the center of sensor should be at least 0.5 \( a \) and 0.5 \( b \) (4 mm and 5 mm) away from the corresponding edge. The edge effect can be presented by calculating the difference of thermal resistance when sensor moves from the center to the corner. Fig. 2.15 (a) shows the edge effect versus the thickness of
Fig. 2.15. (a) Thermal resistance change when sensor moves from at center to corner. (b) heat flux distribution at middle layer of sample (k = 50 W/mK and t = 2 mm), and (c) heat flux distribution at middle layer of sample (k = 50 W/mK and t = 7 mm)

Sample for different kinds of materials derived from analytical thermal model. The edge effect becomes significant when the sample thickness is larger than 4 mm. Fig. 2.15 (b) and (c) shows the heat flux distribution at the middle of the sample (k=50 W/mK) with thickness of 2 mm and 7 mm, respectively. For thickness of 2 mm, the edge effect is small with thermal resistance difference of 0.01 K/W, and very little heat flux bounds back at the corner. While, for thickness of 7 mm, the edge effect becomes significant with thermal resistance difference of 0.2 K/W and a lot heat flux bounds back at the corner. Samples with high thermal conductivity has merely no edge effect, while samples with low thermal conductivity has significant edge effect. Another observation is although the edge effect varies among different materials, the relative change of thermal resistance remains the same, as shown in the dashed line in Fig. 2.15 (a). If we want to maintain the edge effect within the error (0.01 K/W), there will be different thickness limitations for different thermal conductivity as shown in TABLE 2-3. It should be noted that, in the analytical model, the material is homogeneous. However, in the case that there is thermal interface in the sample, there will be additional edge effect induced in the interface layer. The edge effect in interface layer is mainly
effected by the interface thermal properties and the thickness of the sample. One can calculate the interface edge effect based on the relative thermal resistance change curve in Fig. 2.15 (a).

**TABLE 2-3. THICKNESS LIMITATION FOR DIFFERENT MATERIALS**

<table>
<thead>
<tr>
<th>Thermal conductivity (W/mK)</th>
<th>10</th>
<th>50</th>
<th>100</th>
<th>400</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness to avoid edge effect (mm)</td>
<td>1</td>
<td>2</td>
<td>4.2</td>
<td>7</td>
</tr>
</tbody>
</table>

The edge effect will also change as we change the sensor design. It can be predicted that, the design with smaller effective area of the interface layer has smaller edge effect, because less heat flux bounds back at the edge. One can easily use the analytical thermal model to evaluate the edge effect for a specific case.

### 2.6 Conclusions

This chapter illustrates the design principles and methodology utilized in this investigation. To control the sensitivity and resolution of structure function analysis by manipulating the heat flux density, an analytical thermal model was constructed by solving heat transfer equation. This analytical thermal model afforded the temperature distribution, heat flux density distribution, and thermal resistance of the thermal sensor and test coupon. We also evaluated the influence of semiconductor chip size, the size of the sensor substrate, the thermal conductivity of the sensor substrate, the size of the heat sink, and the thermal resistance of the TIM for the heat sink. Based on resulting data, a movable thermal sensor was designed and fabricated. In addition, the edge effect was thoroughly evaluated based on the sensor design. The edge effect becomes more significant when sample thickness increases and when thermal conductivity of the sample decreases. For accurate characterization, the edge effect should not be larger than the standard deviation of the thermal resistance measurement.
Chapter 3. STRUCTURE FUNCTION ANALYSIS OF TRANSIENT THERMAL IMPEDANCE MEASUREMENT

This chapter presents the working principle associated with measuring interface thermal resistance, which corresponds to the structure function analysis of the transient thermal impedance ($Z_{th}$) measurement. The process of analyzing thermal impedance data involves transferring the $Z_{th}$-time curve to thermal capacitance-thermal resistance curve, from which one can derive interface thermal resistance.

$Z_{th}$ measurement was firstly evaluated to check its ability to detect the defects in the interface layer. The evaluation was conducted by testing $Z_{th}$ change induced by the degradation of die-attach layer during the temperature cycling. To ensure reliability is only affected by die-attach layer, we used both high-temperature SiC chips, which are designed to operate at over 250°C, and robust $Si_3N_4$ AMB and AlN DBA substrates, which has much more reliable than the die-attach layer. The die-attach layer degradation can be observed and quantified via scanning electron microscopy (SEM) and X-ray scanning, which was can be used to construct the FEA thermal model for simulation of $Z_{th}$. Comparison between simulation and measurement will verify the accuracy of the $Z_{th}$ measurement.

Structure function analysis was then evaluated to check its ability to detect the thermal resistance change of interface layer induced by defects. The structure function analysis was applied to measure the thermal resistance of interface layer between two substrates. Defects such like Kapton tape and voids were purposely implanted into the interface layer to manipulate the thermal
properties. The accuracy of thermal resistance measurement by structure function analysis can be examined by comparing the interface thermal resistance with different kinds of defects.

3.1 Validation and application of transient thermal impedance measurement

3.1.1 Introduction of transient thermal impedance measurement

Transient thermal impedance ($Z_{th}$) measurement is a non-equilibrium thermal characterization method. Unlike conventional thermal resistance ($R_{th}$) measurement, $Z_{th}$ measurement contains not only $R_{th}$ information, but also thermal capacitance ($C_{th}$) information. $Z_{th}$ is defined as the temperature difference between junction and ambient divided by heat flow power, and is a time-dependent parameter, as shown in equation (2.1)

$$Z_{th} = \frac{T_j - T_a}{P}$$

in which $T_j$ and $T_a$ represent the temperature of the junction and the ambient temperature, respectively [82, 83]. Usually, the ambient temperature is equal to the junction temperature prior to heating pulse. In an electrical system, the thermal impedance of a device can be defined by two approaches, as shown in Fig. 3.1. One involves measuring the response of junction temperature as a function of turn-on time or heating pulse time delivered to the device [84]. The other involves turning on the device and running it continuously until its junction temperature reaches the steady state [84]. Once this level is attained, the device is turned off and its junction temperature response as a function of turn-off time or cooling phase time is recorded. Both methods deliver the $Z_{th}$ of the system.

3.1.1 Thermal impedance measurement setup

An electric method was implemented to measure the junction temperature of the semiconductor devices. This technique utilizes self-heating and the temperature dependence of the
temperature-sensitive parameter (TSP) of a semiconductor device to obtain the temperature response of the junction. The use of the electric method has specific advantages, including rapid response, no additional thermal interferences, and accuracy. Because temperature dependency of TSP exhibits in all power device junctions, this relationship—or in other words the K-factor—can be measured and utilized to calculate the $T_j$ in response to the power dissipation. This relationship can be expressed in the following equation:

$$T_j = K \times TSP + C$$

Fig. 3.1. Schematic of thermal impedance measurements (a) during heating phase and (b) during cooling phase.

In this project, the gate threshold voltage, $V_g$, was selected as the TSP because of the high K-factor of 10 mV/K, which is 4 to 10 times higher than other TSPs, resulting in more accurate
measurements [85]. A test system, as shown in Fig. 3.2, was used to measure temperature response under a given power level. The system included (1) a custom-designed circuit board to manipulate the current and voltage across the device under testing (DUT) [85, 86], (2) a LabVIEW system to control and collect signals, and (3) sample fixtures to maintain a consistent measurement environment. Fig. 3.3 (a) shows the working principle of the circuit board, whose function is to adjust the gate voltage to regulate the current at a given level via the feedback loop. The constant current ensures constant power dissipation during the heating phase, as well as accurate temperature measurement during the sensing phase. As shown in Fig. 3.3 (b), the control circuit has two output current levels: the sensing current at 2.6 mA and the heating current at 3 A. The LabVIEW system contains a data-acquisition box (NI USB-6211), which is controlled by the LabVIEW program. This system outputs modulated signals to regulate the waveforms on the semiconductor; it also records the TSP signal and transfers to junction temperature response. The recorded temperature response was used to calculate the $Z_{th}$ by:

$$Z_{th} = \frac{V_{g,f} - V_{g,i}}{K \times P}$$

(3.3)

where $V_{g,f}$ is the gate threshold voltage after heating pulse and $V_{g,i}$ is the gate threshold voltage before heating.
Fig. 3.2. Overview of temperature measurement setup.

Fig. 3.3. (a) Schematic of power stage of control circuit and (b) equivalent test circuit.

3.1.2 Characterization of K-factor for gate threshold voltage

Fig. 3.4 (a) shows the test setup for measuring the K-factor. Specifically, a semiconductor was bonded on an insulated metal substrate, with a K-type thermal couple attached to the package. The bonded sample was immersed in the dielectric liquid for temperature uniformity, whose temperature was increased using a hot plate at a rate of 1 K/min. The data acquisition frequency was 4 Hz. A cap was placed on top to minimize any temperature interference from the environment. Taking the Si IGBT (PCFG75N60SMW from Fairchild) as an example, as shown in Fig. 3.4 (b),
the K-factor was determined to be 9.28 mV/K, while the standard deviation within five samples was less than 0.5%.

![Diagram of dielectric liquid]

**Fig. 3.4.** (a) Setup for K-factor measurement. (b) K-factor data and its least square fit.

### 3.1.3 $Z_{th}$ measurement for reliability testing of the die-attach layer with different substrates

This section describes the application of $Z_{th}$ measurement for the reliability testing (in a temperature range of -55°C to 250°C) of a sintered silver die-attach layer on two kinds of substrates: A Si$_3$N$_4$ active metal brazing (AMB) substrate, and an AlN direct bonded aluminum (DBA) substrate. Fig. 3.5 shows the cross-section of the test coupon, which is composed of the top three layer of a power module. SiC MOSFET was used because its suitability for high temperature operation (>250°C). Different substrates yielded different stress levels within the die-attach layer during temperature cycling—thereby impacting reliability performance. $Z_{th}$ was adopted to non-destructively detect the die-attach layer thermal quality, after which SEM and X-ray scanning were conducted to investigate the failure modes.
(a) Review of substrates

Al₂O₃ direct bond copper (DBC) substrates are most widely used in industry due to their good performance and affordability. However, when they are exposed to extreme temperature swings, e.g., from -55°C to 250°C, these substrates can only survive 10-20 cycles due to the relatively low toughness of Al₂O₃ [87]. One viable alternative is the Si₃N₄ AMB substrate. Due to the toughness of the Si₃N₄ ceramic, these substrates can survive from between 600 to 3000 cycles, and under temperatures ranging from -55°C to 250°C [88]. Another likely choice is the AlN DBA substrate—principally due to the low yield stress and low rate of strain hardening of aluminum, which can withstand more than 1500 cycles under the same temperature swing without any evidence of delamination in either the metal or ceramic layers [89]. Compared with Al₂O₃ DBC substrates, Si₃N₄ AMB and AlN DBA exhibit higher thermal conductivity and dielectric strength, which contribute to the high temperature and high voltage operation and, thus, high power density.

TABLE 3-1 provides a summary of the properties of different types of substrates. Both Si₃N₄ AMB and AlN DBA display relative high reliability. Moreover, AlN DBA features the highest thermal conductivity, which is critical for high-power applications. However, the phenomenon of metal surface roughening occurs when these metal-ceramic substrates are exposed to temperature cycling; this outcome was found to be especially true for aluminum, which was reported to suffer
from a greater rate of increase in surface roughness compared to copper, as shown in Fig. 3.6 [88]. This phenomenon is of particular concern since it might damage the die-attach layer.

<table>
<thead>
<tr>
<th>TABLE 3-1. SUMMARY OF PROPERTIES OF DIFFERENT SUBSTRATES.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al₂O₃ DBC</td>
</tr>
<tr>
<td>Thermal conductivity of ceramic (W/m·K)</td>
</tr>
<tr>
<td>Dielectric strength (kV/mm)</td>
</tr>
<tr>
<td>Elastic modulus of metal (GPa)</td>
</tr>
<tr>
<td>Flexural strength of ceramic (MPa)</td>
</tr>
<tr>
<td>Reliability (-55 to 250°C)</td>
</tr>
<tr>
<td>Price</td>
</tr>
</tbody>
</table>

Fig. 3.6. Surface roughness versus number of cycles from -55°C to 250°C

(b) Sample fabrication

Si₃N₄ AMB and AIN DBA substrates were obtained from DOWA Metaltech Co., Ltd. The substrates came with a sinter-ready surface finish of silver and a circuit pattern on one side for ease
of obtaining transient thermal measurement samples. TABLE 3-2 lists the dimensions and materials of the two substrates, and shows the dimensions and patterns of the substrates.

**TABLE 3-2. CONFIGURATIONS OF TWO TYPES OF SUBSTRATES.**

<table>
<thead>
<tr>
<th></th>
<th>Si₃N₄ AMB</th>
<th>AlN DBA</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Top side metal</strong></td>
<td>0.25 mm Cu</td>
<td>0.4 mm Al</td>
</tr>
<tr>
<td><strong>Ceramic</strong></td>
<td>0.38 mm Si₃N₄</td>
<td>0.635 mm AlN</td>
</tr>
<tr>
<td><strong>Bottom side metal</strong></td>
<td>0.25 mm Cu</td>
<td>0.4 mm Al</td>
</tr>
<tr>
<td><strong>Surface finishing</strong></td>
<td>Electroless plating, 0.4 µm Ag</td>
<td>Electroless plating, 4 µm Ni and then 0.1 µm Ag</td>
</tr>
</tbody>
</table>

![Fig. 3.7. Schematic of Si₃N₄-AMB and AlN-DBA substrates.](image)

Due to its relatively high power density and high operating temperature, a SiC MOSFET (CPM2-1200-0160B from Cree) was used to assemble the test coupon for reliability testing. An
X-series nanosilver paste capable of pressure-less bonding was obtained from NBE Technologies, LLC. To assemble each SiC test coupon, the silver paste was stencil-printed on a substrate followed by chip mounting. Then, the chip assembly was heated on an open-air hot plate from room temperature to 250°C at a rate of 5°C/min, and then sintered at 250°C for 10 minutes. After the device was bonded, its source and gate pads were wire-bonded to the corresponding pads on the substrate. Four test samples with Si₃N₄ AMB substrates and five with AlN DBA substrates were fabricated, as shown in Fig. 3.8. The sintered-silver bond-line thickness was determined using a profilometer (DektakXT, Bruker) by measuring the height of the attached chip, and then subtracting the chip thickness. The average thickness of the sintered bond-line was found to be 32 µm with a standard deviation of about 7 µm. The surface roughness of the substrate was measured using the same profilometer with a stylus radius of 2 µm and scan length of 4 mm. After each scan, the arithmetic mean surface roughness, Ra, was calculated based on ISO 4287 standards.

![Fig. 3.8. Test coupons fabricated by (a) Si₃N₄ AMB substrate and (b) AlN DBA substrate.](image)

(c) Temperature cycling
Temperature cycling was conducted in a Tenney environmental chamber, as shown in Fig. 3.9 (a). To shorten the temperature cycle, a hot plate was placed in the chamber that increased the heat of the test samples through an on/off temperature controller, while the chamber ambient temperature was kept at -70°C as shown in Fig. 3.9 (b). The test samples were mounted on the hot plate with a silicone thermal grease. The temperature was measured by a K-type thermocouple attached to the plate surface. The on/off controller set the heating rate and recorded the number of cycles. Fig. 3.10 provides a typical profile of a temperature cycle measured by the thermocouple. The temperature ranged from -55°C to 250°C over a standard period of one hour.

Fig. 3.9. (a) Temperature cycling setup and (b) test coupons on hot plate.
After the samples were exposed to specific number of temperature cycles, they were taken out of the chamber in order to measure any changes in substrate surface roughness and transient thermal impedance or $Z_{th}$. It should be noted that the $Z_{th}$ measurement was conducted during the heating phase due to the fact that the die-attach layer was in close proximity to the semiconductor chip, which does not require a thorough characterization, thus saving some time. A more detailed $Z_{th}$ measurement process especially for SiC MOSFET was illustrated in Appendix B. By adjusting the duration of the heating pulse, one can determine the individual contributions of the layers to $Z_{th}$. Since we were mainly interested in the thermal performance of the sintered-silver bond-line, we used a heating pulse of 40 ms, which was long enough for the heat to transfer to the bottom of the substrates, but not so long that we had to factor in the contributions of the other layers of the package.
Fig. 3.11 provide plots of measured $Z_{th}$ versus number of temperature cycles from MOSFETs mounted on (a) the DBA substrates, and (b) the AMB substrates. An increase in $Z_{th}$ is attributed to degradation in the bond-line. In general, a 20% increase in $Z_{th}$ was considered to be the principal criterion for bond-line failure. As shown in this figure, nearly all of the bond-lines failed after 1200 cycles. Weibull distribution plots of the failure data were determined from the plots in Fig. 3.12. The Weibull distribution analysis was conducted using the following equation:

$$F(x) = 1 - \exp\left(-\left(\frac{x}{\eta}\right)^m\right)$$  \hspace{1cm} (3.4)

where $F(x)$ is defined as the proportion of failed samples and $x$ is cycles-to-failure. The shape parameter $m$ and scale parameter $\eta$ were determined by least squares fitting. From Weibull distribution, one can estimate the failure proportion at a given cycle number. It should be noted that one of the AlN DBA samples failed after 400 cycles because a bond wire connecting the MOSFET broke. This sample point is shown in the figure, but not included in the dataset for fitting to the Weibull distribution function [90]. After the fitting analysis, we estimated the number of cycles at 50% failure to be 1039 cycles for the DBA samples and 832 cycles for the $\text{Si}_3\text{N}_4$ samples. It is interesting to note that the sintered-silver bond-lines on DBA substrates exhibited about 24.9% higher lifetime than those on the $\text{Si}_3\text{N}_4$ substrates—despite the fact that the DBA substrates experienced two times higher surface-roughening rate.
Shown in Fig. 3.13 are plots of surface roughness versus number of temperature cycles from -55°C to 250°C measured on the two types of insulated metal substrates. The rate of surface-roughness increase on the DBA substrate was nearly twice that of the Si₃N₄ AMB. Moreover, the results for the Si₃N₄ AMB samples are comparable to our previous results reported in [89]. However, the surface roughening rate found for the DBA substrates was one-sixth of that reported earlier in [88]. This difference is likely due to the different ways used to make the DBA substrates:
one by diffusion bonding and the other by casting and solidification. According to Dowa, the manufacturer of the cast DBA used in this study, the aluminum layer on their substrates has a coarser grain microstructure in comparison to diffusion-bonded DBA. In [91, 92], it was reported that under cyclic loading, the deformation of polycrystalline aluminum can result in significant surface roughness due to grain-boundary sliding. Since grain-boundary sliding is more likely to occur in a finer microstructure, this would lead to a higher surface roughening rate in the diffusion-bonded DBA than that in the Dowa DBA with a coarser microstructure, which is consistent with our observations.

Fig. 3.12. Weibull analysis of temperature cycling tests
3.1.4 Failure modes analysis

As detailed in this section, both FEA simulation (ANSYS workbench) and materials characterization methods (SEM and X-ray scanning) were utilized to investigate failure modes and why they occurred. The FEA simulation derived a numerical solution for the accumulated thermo-mechanical strain during temperature cycling. SEM and X-ray scanning depicted the bond line images and micro structure. We utilized this data to investigate failure modes and build a thermal model for thermal simulation.

The model for either the Si₃N₄ AMB package or the AlN DBA package is shown in Fig. 3.14 (a). The necessary properties for the SiC chip and the substrates were obtained from the ANSYS database. The sintered silver properties were calculated using Anand model based on published data [93]. It should be noted that the sintered silver area was larger than the SiC chip (0.5 mm away from chip edge), because the sintered silver was stencil-printed on the substrate with a 0.5 mm margin for ease of bonding. The accumulated plastic strain in the sintered silver layer was
simulated under temperature cycling from -55°C to 250°C. The lifetime of the silver layer can be calculated based on Coffin-Manson equation [94, 95]:

\[ \frac{\Delta \varepsilon_p}{2} = \varepsilon_f'(2N)^c \]  

(3.5)

where \( \Delta \varepsilon_p \) is the plastic strain amplitude, \( \varepsilon_f' \) is an empirical constant known as the fatigue ductility coefficient, \( N \) is the number of reversals to failure, and \( c \) is an empirical constant. Usually, \( c \) is negative, meaning that lifetime has a negative correlation with strain. Fig. 3.14 (b) illustrates the accumulated strain in the sintered silver layer for these two packages. As shown, the strain in Si3N4 AMB package accumulated faster in comparison to the AlN DBA package, which indicates that the AlN DBA package should be more reliable. This outcome is consistent with the results from Zth measurement.

![Diagram of simulation](image)

(a)

![Graph of accumulated strain](image)

(b)

Fig. 3.14. Simulation of strain in sintered silver bond line during temperature cycling. (a) model for simulation and (b) accumulated maximum strain in sintered silver bond line.

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However, the effects of surface roughening still had to be determined. To understand the reasons for the higher die-attach reliability found on the DBA substrate, which had a higher roughening rate, we examined the bond-line microstructures after 1200 cycles by SEM and X-ray scanning. The samples with high Zth increase were firstly scanned via non-destructive X-ray tomography. Shown in Fig. 3.15 are (a) transmission x-ray image of a SiC MOSFET bonded on AlN DBA, and (b) one bonded on Si3N4 AMB. Crack lines are clearly visible in the bond-line on DBA; conversely, the bond-line on Si3N4 appears to be crack-free. We do, however, recommend some caution on interpreting the X-ray images. Since the X-ray images were obtained with the X-ray beam penetrating through the samples in the direction perpendicular to the substrate plane, the imaging technique is only sensitive to bond-line cracks perpendicular to the substrate—i.e., vertical cracks, not horizontal cracks, in the substrate plane. In addition, the x-ray imaging technique also has limited spatial resolution of hundreds of micrometers.

Fig. 3.16 provides cross-sectional SEM images of (a) the 1200-cycled bond-line on AlN DBA, and (b) comparative data for Si3N4 AMB. The bond-line on DBA displayed two types of cracks: vertical and horizontal; in contrast, the bond-line cracks on Si3N4 were exclusively horizontal. The horizontal cracks in the latter case were also more extensive, i.e. longer and wider than those found on DBA.

Cracks form in bond-lines because of thermo-mechanical stresses resulting from mismatched coefficients of thermal expansion between the die and substrate. Normally, the local stress state in the bond-line is dominated by a shear component leading to the growth of horizontal cracks. Roughening of substrate surface would add a significant tensile component to the local stress state to cause vertical cracks. The fact that the aluminum surface on DBA roughened at twice the rate in comparison to the copper surface on Si3N4 was likely the reason for the vertical cracks found in
the former, but not in the latter. Formation of vertical cracks helped to relieve stresses and blocked or lessened the growth of horizontal cracks. We believe that the vertical cracks formed prior to formation of the horizontal cracks and limited their propagation. This phenomenon may also explain the reduced severity of the horizontal cracks in the DBA bond-line.

Fig. 3.15. Transmission x-ray images of bonded MOSFETs on the two different types of substrates after 1200 temperature cycles: (a) on AlN-DBA; and (b) on Si$_3$N$_4$-AMB.
Fig. 3.16. SEM cross-sectional images of bonded MOSFETs on the two different types of substrates after 1200 temperature cycles: (a) on AlN-DBA; and (b) on Si$_3$N$_4$-AMB
3.1.5 Validation of $Z_{th}$ measurement by thermal simulation

As heat generated by the device is conducted away through the bond-line to the substrate, one may argue that vertical cracks have a reduced impact on thermal performance in comparison to the effects of horizontal cracks. This factor may offer an explanation for the longer lifetime (determined by change in $Z_{th}$) found in the bond-line on DBA in contrast to comparative data for the AMB substrate. To verify this, we ran transient thermal simulations to examine the effects of the two types of bond-line defects on $Z_{th}$.

To simulate transient thermal behavior, we would need structural models of the test coupons with bond-line defect patterns resembling those observed in the x-ray and SEM images. Fig. 3.17 (a) shows a binary x-ray image of an AlN DBA test sample. The total length of the vertical cracks is about 40 mm. Given the dimension of the bonding area to be 2.63x2.39 mm$^2$, the total length is equivalent to a pattern of an 8 row x 8 column square matrix. The width of each crack is about 5 μm obtained from measurements of the X-ray and SEM images. Fig. 3.17 (b) shows a cross-sectional laser microscopic image of an Si$_3$N$_4$ AMB sample with the largest $Z_{th}$ increase. Specifically, the image shows the horizontal crack area to be around 60% of the bond-line and the thickness of the horizontal crack is about 10 μm, which is about half of the bond-line thickness.

Fig. 3.18 illustrates a pair of schematics for the structural models constructed for simulating the effects on $Z_{th}$ from two different types of bond-line defect patterns: (a) horizontal cracks covering a certain percentage of the bonding area on Si$_3$N$_4$ AMB; and (b) an n x n square matrix of vertical cracks distributed in the bond-line on DBA. For each defect pattern, we ran simulations to obtain the dependence of $Z_{th}$ on the extent of defect coverage. For the horizontal cracks, we simulated a series of defective area coverages from 10% to 60% while keeping the air gap of the...
horizontal cracks fixed at 10 μm. For the vertical cracks, we varied the number of rows of vertical crack lines from 2 to 8 while keeping the crack width at 5 μm.

Fig. 3.17. Analysis of vertical crack length and horizontal crack area: (a) Binary x-ray image and calculation of vertical crack length; and (b) Cross-sectional laser microscope image and calculation of horizontal crack area.

An ANSYS-workbench software package was used to run 2D finite-element simulations of the structural models. Because the semiconductor junction, where most power loss is generated, is close to the surface of the chip. In the simulation, the heat flux with value of P/A was dissipated from top of the SiC chip. The thermal conductivity of sintered silver was assumed to equal
240W/m·K, while the thermal properties of other the components were obtained from the software database. Transient thermal behavior was simulated by applying 40 ms heating pulse. The heating flux was uniformly injected on top of the SiC MOSFET, which is what typically occurs in actuality. At the end of the heating pulse, the average temperature on the surface was recorded in order to calculate the $Z_{th}$. TABLE 3-3 lists the simulated $Z_{th}$ values for all the samples investigated. For the horizontal crack pattern in the AMB sample, we see that a 20% area coverage by cracks resulted in a 20% increase in $Z_{th}$, with a 60% area coverage leading to a 188% increase in $Z_{th}$. On the other hand, for the vertical crack pattern in the DBA sample, its effect on $Z_{th}$ turned out to be much less profound. With an 8 x 8 matrix of vertical cracks having a total length similar to that found in a sample, the increase in $Z_{th}$ was only 4%. Even when we added a horizontal crack pattern covering 10% of the area to the 8 x 8 vertical crack pattern, we only observed a 15% increase in the value of $Z_{th}$, which is significantly smaller than comparable data for the 60% horizontal crack area. This outcome clearly shows that horizontal cracks in the bond-line are far more effective in blocking heat flux through the die-attach layer.

It should be noted that for the Si$_3$N$_4$ AMB package, the worst case $Z_{th}$ increase was 105%, as shown in Fig. 3.11 (b); while simulation results indicate that a 50% delamination area affords a 105% increase in $Z_{th}$. As documented in Fig. 3.17, the delamination area was about 60%, which is relatively consistent with simulated findings. Additionally, for the AlN DBA package, simulation data show that the combination of 10% of delamination area and an 8 x 8 matrix of vertical cracks afford a 15% increase in $Z_{th}$, which is also consistent with the $Z_{th}$ measurement value in Fig. 3.11 (a). As a result, we have confidence in the accuracy of the $Z_{th}$ measurement setup utilized herein.
Fig. 3.18. Structural model for simulation of defects influence on $Z_{th}$: (a) by horizontal cracks, and (b) by vertical cracks.
### TABLE 3-3. EFFECT OF TYPE AND DENSITY OF BOND LINE DEFECT ON $Z_{th}$

<table>
<thead>
<tr>
<th>Vertical crack density</th>
<th>1x1</th>
<th>2x2</th>
<th>3x3</th>
<th>4x4</th>
<th>6x6</th>
<th>8x8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Percent of $Z_{th}$ (40 ms) increase over a defect-free joint</td>
<td>0.5%</td>
<td>1%</td>
<td>1.5%</td>
<td>2%</td>
<td>3%</td>
<td>4%</td>
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</table>

<table>
<thead>
<tr>
<th>Horizontal crack area</th>
<th>10%</th>
<th>20%</th>
<th>30%</th>
<th>40%</th>
<th>50%</th>
<th>60%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Percent of $Z_{th}$ (40 ms) increase over a defect-free joint</td>
<td>10%</td>
<td>20%</td>
<td>26%</td>
<td>58%</td>
<td>99%</td>
<td>188%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Horizontal crack area</th>
<th>10%</th>
<th>Vertical crack density</th>
<th>8x8</th>
</tr>
</thead>
</table>
| Percent of $Z_{th}$ (40 ms) increase over a defect-free joint | 15% |}

### 3.2 Validation and application of structure function analysis

#### 3.2.1 Introduction of structure function analysis

Transient thermal measurement plays a vital role in the thermal characterization of semiconductor device packaging. This method involves recording the temperature response, which is a function of the structure along the heat flow path, which is then analyzed based on certain thermal models. Normally, the thermal model is equivalent to an electric $RC$ model, as show in Fig. 3.19. In the thermal model, power $P$ is equivalent to current; temperature $T$ is equivalent to voltage; and thermal resistance and thermal capacitance are equivalent to electrical resistance and electrical capacitance. Because the Cauer network includes node-to-ground thermal capacitance, it features real thermal properties. Usually, for ease of calculation, Cauer network is transferred to its equivalent and exclusive Foster network.

![Cauer network](image1.png) ![Foster network](image2.png)

**Fig. 3.19.** Schematic of thermal RC models: (a) Cauer network and (b) Foster network.
The temperature response function based on Foster network can be calculated in the summation form [96]:

\[
Z_{th}(t) = \frac{\Delta T(t)}{P} = \sum_{i=1}^{n} R_i[1 - \exp \left(-\frac{t}{\tau_i}\right)]
\]

(3.6)

where \( Z_{th} \) is the thermal impedance as a function of time, \( R_i \) is thermal resistance of component \( i \), and \( \tau_i = \sum_{i=1}^{n} R_i C_i \) is the time constant, which is defined as the time for power to dissipate to the \( i \) component. Methods such as least square fitting can be applied on \( Z_{th}(t) \) function data to derive the corresponding \( R_i \) and \( C_i \). Because this method generates the thermal properties of lumped components, only finite layers can be modelled. During the modelling and analysis, one should define the number of components, which limits its application for unknown or irregular device packages.

To overcome this disadvantage, a continuous analysis was proposed. In this analysis, the temperature response is calculated in integration form:

\[
Z_{th}(z) = \frac{\Delta T(t)}{P} = \int_{-\infty}^{\infty} R(\zeta)[1 - \exp(-\exp(z - \zeta))]d\zeta
\]

(3.7)

\[
z = \ln(t) \text{ and } \zeta = \ln(\tau)
\]

(3.8)

Here, for mathematical convenience and for ease of recording over a long period of time, a logarithmic variable is introduced. And the derivation of both sides of equation 2.6 yield:

\[
\frac{Z_{th}(z)}{dz} = \int_{-\infty}^{\infty} R(\zeta)\exp(1 - \exp(z - \zeta))]d\zeta = R(z) * W(z)
\]

(3.9)

Equation 2.8 express the convolution operation of \( R \) and \( W \), where \( W \) is defined as:

\[
W(z) = \exp[1 - \exp(z)]
\]

(3.10)

Thus, \( R(\zeta) \) or \( R(\tau) \) can be derived from \( Z_{th} \) data by a deconvolution operation. The function \( R(\tau) \) can be further transformed to cumulative thermal capacitance as a function of cumulative thermal
resistance. Because this function depicts the structure parameter changes along the heat flow path, it is known as the structure function.

In this work, structure function analysis was conducted by TDIM-master as illustrated in JEDEC standard 51-14. This approach requires a fairly high data-acquisition rate at the onset of the $Z_{th}$ measurement. Thus, for structure function analysis, the cooling phase method described in Section 2.1.1 was utilized to measure the $Z_{th}$ response, with the data-acquisition rate of 250 kHz, which is the maximum of the LabVIEW DAQ box.

**3.2.2 Validation of structure function analysis for $R_{th}$ measurement**

Heat dissipation represents an important function served by packaging power devices or modules. In the power package shown in Fig. 1.1, heat generated by the device has to be conducted away through multiple layers of materials and bonded interfaces. The two most important bonded interfaces are (a) the die-attach layer between the device and its substrate, and (b) the substrate-attach between the substrate and a heat spreader or heat-sinking plate. Significant progress has been made recently in die-attach technologies. The emerging sintered silver die-attach technology has been shown to yield significantly higher thermal and electrical conduction and higher reliability than traditional soldering technologies. With respect to the substrate-attach interface, advances in developing thermal interface materials have been slow [97]. The widely used thermal greases or gels are easy to apply but typically feature high thermal resistance. Additionally, phase change materials (PCMs) tend to degrade when exposed to elevated temperatures over prolonged period of time, causing reliability concerns. While solders (both lead-tin and lead-free) can produce bonded interfaces with a much lower thermal resistance, the soldered joints are prone to fatigue failure from brittle intermetallic phases. The reliability of soldered interfaces over large areas is especially problematic [37]. Sintered silver, however, has both low thermal resistance and high reliability,
which is promising for bonding large area interfaces. Because large area interfaces may trap gas, which generates voids within the bond line. In addition, the curvature across the large area interface may cause nonuniform bonding quality for the sintered silver joint. In this section, we measured the thermal resistance of sintered silver substrate attach layer by investigating structure function analysis. The accuracy of the structure function analysis for thermal resistance measurement was verified.

(a) Sample preparation

To simplify the fabrication and the measurement process, a sandwich structure sample was prepared as shown in Fig. 3.20. The under substrate served as the baseplate as in a power module. AlN DBA substrates measured at 25 mm wide x 50 mm long x 1.6 mm thick were obtained from DOWA. The size of these substrates are similar to those used in commercial half-bridge power modules. The DBA substrate was composed of a 1 mm thick of AlN plate sandwiched between two 0.3 mm thick aluminum sheets. The substrate was fabricated via a proprietary process of casting and solidification to afford a strong and reliable interface between the aluminum and the ceramic. The aluminum surface was topped with electroplated nickel and silver for subsequent bonding by silver sintering. The surface roughness, measured by a DekTek profilometer, was 1.46 μm, and the substrate flatness, measured from the height differences at the substrate center and its four corners, was about 8 μm.

![Fig. 3.20. Schematic of large area sintered silver bonded sample.](image-url)
An X-series nanosilver material from NBE Technologies was used to bond the DBA substrates. To make each bonded sample, we followed a previously reported two-print process [98]. The DBA substrates were first cleaned with acetone and alcohol to remove any organic contaminants. Then, a 100-µm thick layer of the nanosilver paste was stencil-printed on one substrate at a time. The sintering profile is shown in Fig. 3.21. The paste layer was dried on a hot plate at about 120°C for 90 min to evaporate any solvents in the paste. After drying, the layer thickness shrank by about 30 to 35%. On the dried layer, a fresh paste layer of about 30-µm thick was added by stencil-printing. While the latter layer was still wet, we placed another DBA substrate on its surface, after which the entire assembly was heated in a Carver hydraulic press for sintering below 270°C under 5 MPa. As described in [98], the addition of a fresh paste layer ensures intimate contact between the top substrate and the bonding material. The rationale behind drying the first layer is to cut down the amount of solvents that would escape from beneath the large substrate, as well as to prevent the fresh layer from squeezing out.

Fig. 3.21. Sintering profile for sintered silver substrate attachment.
The power device we selected for transient thermal characterization was an Si-insulated gate bipolar transistor (IGBT) (IRG4CH30K, which served as a heat source and a temperature sensor. The dimensions of the device chip were 3 mm x 5 mm x 0.5 mm (thick). The K-factor of the Si device was measured at The Si chip was 10 mV/K. The Si chip was bonded on top of the large area sample by solder to measure the $Z_{th}$.

(b) Validation of structure function analysis

Prior to applying this characterization technique for determining the thermal resistance of the sintered silver interface, we tested its sensitivity by fabricating bonded substrates with deliberately planted defects within the bond-line. Fig. 3.22 shows a schematic of a test sample consisting of three IGBT chips soldered on a bonded substrate with the planted defects. At Location 1, the chip was placed above a part of the bond-line with large voids introduced by removing some of the silver paste in the bonding process. At Location 2, no defect was introduced. At Location 3, a piece of Kapton tape was embedded in the silver paste. One would expect the interface thermal resistances at Locations 1 and 3 to be much larger than that at Location 2.
Fig. 3.22. Schematic of a test sample with IGBT devices mounted at three different locations to test the sensitivity of the transient thermal characterization approach: (a) top view; and (b) cross-sectional view showing two locations with deliberately added defects, voids, or Kapton tape.

The effects of the bond-line defects on the cumulative structure function are shown in Fig. 4. Plotted in Fig. 3.23 (a) are the curves of the structure function from Location 1, the place of the bond-line with voids, and Location 2, the bond-line section without any defect. Shown in Fig. 3.23 (b) are the curve of the structure function from Location 3, the section of the bond-line with a buried Kapton tape and that from Location 2 replotted. Each of the curves in Fig. 4 features five distinctive segments as defined by significant changes in the slope of the curve. The segments represent different contributions from the main elements of the package: silicon die, die-attach, top DBA substrate, substrate attach, and bottom DBA substrate. Beyond the bottom DBA, the measurement technique is insensitive to reveal detailed features of the rest of the cooling path because of the large thermal resistance of the thermal interface material and heat spreading from the source.
Fig. 3.23. Plots of cumulative structure functions obtained at (a) Location 2 (no defect) and 1 (with void) and (b) Location 2 (no defect) and Location 3 (with Kapton tape) of the sample in Fig. 2.

Based on the structure function plots shown in Fig. 3.23, the thermal resistance of the substrate-attach layers at Location 1, 2, and 3 were found to be 0.43 K/W, 0.12 K/W, and 0.22 K/W,
respectively. The thermal resistance of the die attach and the substrate in the test sample were also determined from the plots, which were 0.15 W/K and 0.25 W/K, respectively. However, in order to capture the specific thermal resistance data for the different layers and compare those results against those published by others [99], we needed to estimate the active area of each layer. Using a simple 45° heat spreading model, we roughly identified the active areas, followed by determining the specific thermal resistance. TABLE 3-4 provides a list of the thermal resistance results and the specific thermal resistance of the layers from the measurements at Location 2 and the specific thermal resistances reported in the literature. The thermal resistance data measured by structure function analysis were in good agreement with comparable data reported in the literature, which verified the accuracy.

<table>
<thead>
<tr>
<th></th>
<th>Measured thermal resistance (K/W)</th>
<th>Active area (mm²)</th>
<th>Measured specific thermal resistance (mm²K/W)</th>
<th>Specific thermal resistance in reference (mm²K/W)</th>
<th>Difference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die attach layer</td>
<td>0.15</td>
<td>15</td>
<td>2.3</td>
<td>2.7</td>
<td>17.4%</td>
</tr>
<tr>
<td>Top substrate</td>
<td>0.25</td>
<td>29</td>
<td>7.3</td>
<td>8.4</td>
<td>15.1%</td>
</tr>
<tr>
<td>Substrate-attach layer</td>
<td>0.12</td>
<td>48</td>
<td>5.8</td>
<td>5.4</td>
<td>6.9%</td>
</tr>
</tbody>
</table>

### 3.2.3 Structure function analysis for R_th measurement of sintered silver substrate attach layer

A large sintered-silver bonded sample was fabricated, as previously described. Because the bonding area was fairly large, defects could exist in the bond line, resulting in nonuniform quality. To quantify variations in the quality of the large sintered-silver substrate-attach layer, we soldered eleven IGBT devices on the substrate, as shown in Fig. 3.24. By measuring the junction-
temperature response separately at each device location, we obtained plots of the eleven cumulative structure functions successively. Then, the interface thermal resistances were extracted. As shown in this figure, we were able to determine the specific thermal resistance of the sintered-silver interface for each device location in mm²K/W. The average value from the eleven locations was determined to be 5.20 mm²K/W with a variation of 6%. However, without the movable sensor, the IGBT chip has to be re-mount at different locations for multi-measurement. This re-mounting process increases the difficulty and limited the resolution of the 2-d map of interface thermal resistance.

![Image of thermal map](image)

**Fig. 3.24.** A two-dimensional thermal map from devices soldered on a bonded substrate. The number at each location refers to the extracted specific thermal resistance at the device site.

To investigate the bond-line condition, the bonded sample was cut and mounted using an epoxy resin for SEM imaging. **Fig. 3.25 (a)** presents a cross-sectional SEM image of the bonded interface showing a continuous bond-line without delamination or large voids. The dark spots in the aluminum layers and cracks in the silver coatings on the DBA substrates are likely caused by grinding and polishing during sample preparation. The sintered silver layer features a porous microstructure, typical of sintered joints. Shown in **Fig. 3.25 (b)** is a binary image of the sintered
silver bond-line within the red box of Fig. 3.25 (a). An analysis of the image confirmed the porosity to be about 17.6%. The density of the sintered bond-line depends on sintering temperature and pressure. One expects a higher sintered density to afford better thermal performance. However, higher density would also require higher pressure and/or higher sintering temperature.

Fig. 3.25. (a) A cross-sectional SEM image of a bonded substrate showing the sintered silver joint; and (b) a binary image of the bond-line used for porosity estimation.
3.3 Conclusions

This chapter describes the validation and application of $Z_{th}$ measurement and its structure function analysis to derive thermal resistance. First, the $Z_{th}$ measurement working principle and test procedures were introduced. Then, the accuracy of $Z_{th}$ measurement was investigated by applying the reliability measurement of sintered silver die-attach layer on Si$_3$N$_4$ AMB and AlN DBA substrates. Due to the fact that material and mechanical properties differ between Si$_3$N$_4$ AMB and AlN DBA, different failure modes were obtained. The failure modes were then analyzed and quantified to construct a thermal model of the sintered silver layer. The proposed model was utilized to verify the accuracy of $Z_{th}$ measurement by comparing the FEA simulation result with $Z_{th}$ measurement result. The sintered silver layer in the DBA package contained both horizontal delamination that covered 10% of the bonding area, and vertical cracks with a total length of 40 mm. The sintered silver layer in the AMB package contained only horizontal delamination that covered about 60% of the bonding area. Based on these models, the FEA simulation showed a 15% increase in $Z_{th}$ of the DBA package (versus a 15% increase in $Z_{th}$ measurement). And to achieve the same among of $Z_{th}$ of AMB package, FEA simulation required 50% horizontal delamination (versus 60% by analysis of failed sample). This result verified the accuracy of $Z_{th}$ measurement using our system.

The sensitivity and accuracy of structure function analysis were then evaluated and verified. The working principle behind the use of structure function to derive thermal resistance was introduced. The sensitivity of this approach was investigated by applying structure function at the thermal-interface layers with purposely implanted defects to modify their thermal resistance. The structure function analysis approach successfully detected the thermal resistance change in the
thermal-interface layer. In addition, the accuracy of structure function analysis was investigated by measuring the thermal resistance of the sintered silver interface layer. The measured results showed good agreement with the value obtained via the other technique, thereby verifying the sensitivity and accuracy of structure function analysis for measuring interface thermal resistance. Moreover, structure function analysis was used to measure the uniformity of a large-area bonded interface, which generated a low-resolution 2-d thermal map. The obtained resolution was limited by the original technique, which suggested the application the movable thermal sensor, as detailed in the following chapter.
Chapter 4. TWO-DIMENSIONAL MAPPING OF THERMAL RESISTANCE MEASUREMENT USING THE MOVAUDBBLE THERMAL SENSOR

This chapter presents the application of the movable thermal sensor for two-dimensional mapping of interface thermal resistance. The method detailed herein was developed to accurately derive the thermal resistance from structure function by dual measurements with different convection condition. Then, sensitivity and resolution were evaluated by measuring thermal resistance for different types and sizes of thermal interface materials.

4.1 Demonstration of thermal resistance measurement for interface layer

As described in this section, measuring interface thermal resistance is based on an analysis of structure function plot. One needs to identify the segment that represents the interface layer from structure function plot, as discussed in Section 2.2. It must be noted, however, that it is sometimes difficult to precisely identify the corresponding segment because the adjacent materials have similar thermal properties, which can blur the boundary of the segment. To overcome this dilemma, a dual measurement approach was proposed to distinguish the boundary of the desired segment.

4.1.1 \( R_{th} \) measurement of test coupon stack

To demonstrate the interface thermal resistance measurement process, we fabricated a test coupon by attaching two rectangular copper plates (25 mm x 44 mm x 1.0 mm) with Kapton tape interface, as shown in Fig. 4.1 (a). The surface of the copper plates was coated with silver finishing to avoid oxidization. The thickness of the Kapton tape was 50 \( \mu \)m. The steady-state thermal model
is shown in Fig. 4.1 (b), indicating that the thermal resistances of the different layers were connected in series.

![Diagram of thermal resistance model](image)

**Fig. 4.1.** (a) Test coupon for demonstrating thermal resistance measurement by thermal sensor, and (b) steady-state thermal model for the test coupon.

The first step was to measure the thermal resistance of the test coupon stack. To identify the segment in structure function that represents the test coupon stack, we either used, or did not use, thermal grease at the interface between the thermal sensor and test coupon, and the interface between test coupon and heat sink. Because thermal grease becomes a fairly thin layer under pressure, it features high thermal conductivity and low thermal capacity. There should be a shift in structure function plot and the separation point, indicating the boundary of the test coupon. As shown in Fig. 4.2 (a), we compared structure function data with and without thermal grease between the thermal sensor and test coupon. At the beginning, the structure function plot for the test without thermal grease was identical to the one we obtained with thermal grease, indicating
that the thermal properties for this area were the same for both measurements. The shape did begin to change after a given point, indicating a change in thermal properties. The point of separation corresponded to the location between the thermal sensor and the test coupon. In the end, the
thermal resistance from chip junction to thermal sensor case was approximately 0.64 K/W. As indicated in Fig. 4.2 (b), we used the same method to identify the location between the test coupon and the heat sink; thermal resistance from the chip junction to bottom of the test coupon was approximately 1.20 K/W. Using subtraction, we calculated the thermal resistance for the test coupon to be 0.56 K/W.

4.1.2 Interface layer $R_{th}$ calculation

The test coupon stack consisted of two copper layers and one interface layer. To derive the thermal resistance of the interface layer, the thermal resistance of the copper layers needs to be subtracted. FEA simulation was utilized to calculate the thermal resistance of the copper layers, as shown in Fig. 4.3. Heat flux was injected from the Si IGBT surface and dissipated via heat sink bottom by convection. The result of the simulation afforded the temperature distribution of the system. To simulate the thermal resistance of the copper layers, we first simulated the junction temperature $T_{j-0}$ with default thermal properties. We then changed the thermal conductivity of the copper layers from its original value (400 W/mK) to a very large value (10000 W/mK), which resulted in the junction temperature $T_{j-1}$. This junction temperature can be expressed as:

$$T_j = T_r + P \times (R_{copper} + R_{interface} + \cdots)$$

(4.1)

The very large thermal conductivity would ensure that the thermal resistance of the “copper layers” would be negligible. Accordingly, thermal resistance was calculated by dividing the temperature difference $T_{j-0} - T_{j-1}$ by the input power $P$. It should be noted that, as discussed in Section 3.3.2, any change in thermal conductivity would influence the heat flux density distribution, which will cause a change in thermal resistance of the interface layer. Under simulation testing, therefore, the thermal conductivity of the interface layer was set to be large enough (10000W/mK) to ensure that the thermal resistance of the interface layer was both negligible and independent of the heat flux.
density distribution. From FEA simulation, the thermal resistance of the copper layers was 0.14 K/W. Therefore, we were able to determine that the thermal resistance of the interface layer in the test coupon was 0.42 K/W.

Fig. 4.3. FEA model for calculating copper layer thermal resistance.

4.2 2-d thermal resistance characterization on bonded samples

Based on procedures detailed in Section 4.1, we used the sensor to scan the interface thermal resistance at different locations, resulting in the generation of a 2-d interface thermal resistance map. As described in this section, we measured the 2-d thermal resistance map for bonded samples with various kinds of interface materials.

4.2.1 Sample preparation

We fabricated two test coupons with two kinds of thermal interface materials to demonstrate the application of the movable thermal sensor. Test Coupon 1 was composed of two copper plates
(25 mm x 44 mm x 1.0 mm) and thermal grease (Dow Corning 340). The copper plates were coated with silver to prevent oxidation and provide surface finishing for soldering or sintering. To ensure good attachment, we dispersed the thermal grease between the copper plates, and then applied 1 MPa pressure. Rubber buffers were used around the test coupon to ensure uniform pressure. A uniformly thick grease interface was generated with the extrusion of any additional grease. Test Coupon 2 was composed of the same type of copper plates, but with sintered silver serving as the bonded interface. Based on the same sintering profile as described in Section 2.2.2, we bonded the two copper plates together by silver sintering. To examine the bonding quality, we conducted X-ray scanning on Test Coupon 2. As shown in Fig. 4.4, the X-ray image confirmed crack-free and void-free bonding conditions.

Fig. 4.4. X-ray images of Test Coupon 2

4.2.2 2-d thermal resistance map characterization

Fig. 4.5 (b) and (b) illustrate 2-d thermal resistance maps for the thermal grease interface and the sintered silver interface, respectively. The step size of the probe movement was 2 mm in the X direction and 3 mm in the Y direction. The discrete data points were transferred into a thermal
resistance map using Mathematica. The average thermal resistance for the thermal grease interface was found to be 0.199 K/W, with a deviation of 0.0050 K/W (2.5%). The average thermal resistance for the sintered silver interface was found to be 0.073 K/W, with a standard deviation of 0.0053 K/W (6.8%). The low standard deviation indicated uniform thermal properties for both the thermal grease and sintered silver interfaces. Note that the thermal resistance value for the sintered silver layer was significantly lower in comparison to the thermal grease layer, and was consistent with their thermal conductivities.
resolution evaluation

In a device, different kinds of defects may exist in the interface layer. Thus, it was necessary to evaluate the resolution of the movable sensor, as described in this section.

4.3.1 Sample preparation

To evaluate the resolution of the movable sensor to inhomogeneity in the bond-line, we fabricated two kinds of samples. One kind, to which Test Coupons 3 and 4 belong, was used to evaluate the sample’s sensitivity to thermal degradation, as shown in Fig. 4.6 (a) and (b). Test Coupons 3 and 4 were made by bonding two plates of copper, each measuring 25 mm x 44 mm x 1 mm. The plates were bonded by thermal grease (Dow Corning 340). We deliberately implanted
pieces of Kapton tape at five locations along the interface, with a size of 1x1 mm$^2$, 2x2 mm$^2$, 3x3 mm$^2$, 4x4 mm$^2$, and 6x6 mm$^2$, respectively. The regions with larger-sized Kapton tape were expected to display higher thermal resistances. Test Coupon 5 and 6 belong to another kind of test coupon, which were used to evaluate the sensitivity of the movable sensor to thermal conductivity increase. As shown in Fig. 4.7, we attached Kapton tape on one copper plate, with window size of 1x1 mm$^2$, 2x2 mm$^2$, 3x3 mm$^2$, 5x5 mm$^2$, and 6x6 mm$^2$, respectively. Then we stencil-printed thermal grease (Dow Corning 340) to fill the windows. Thus, the regions with thermal grease were expected to display low thermal resistance.

![Fig. 4.6. Implanted Kapton tape of differing sizes in (a) Test Coupon 3 and (b) Test Coupon 4 for sensitivity evaluation.](image)

![Fig. 4.7. Implanted heat channel of differing sizes in (a) Test Coupon 5 and (b) Test Coupon 6 for sensitivity evaluation.](image)
4.3.2 High resolution 2-d thermal resistance map

Shown in Fig. 4.8 (a) and (b) are 2-d maps of the interface thermal resistance measured by moving the thermal sensor across the top surface of Test Coupons 3 and 4, respectively. The step size of the probe movement was 2 mm in the X direction and 3 mm in the Y direction. The discrete data points were transferred into a thermal resistance map using Mathematica. The background interface thermal resistance for thermal grease was assessed to be about 0.20 K/W, as measured using procedures detailed in Section 4.2.2. The peak values for locations measuring 1x1 mm², 2x2 mm², 3x3 mm², 4x4 mm², and 6x6 mm² were 0.22 K/W, 0.24 K/W, 0.29 K/W, 0.35 K/W, and 0.38 K/W, respectively. In addition to peak value, peak width also increased with increasing Kapton tape size. Moreover, the probe was successful in detecting significantly higher thermal resistance values at locations with Kapton tape that was larger than 1x1 mm². Indeed, at the location with the 1x1 mm² Kapton tape, the rise in thermal resistance was barely visible, which seems to suggest that this might represent the lower limit for the thermal probe technique intended to assess the interface thermal resistance of bonded samples with 1 mm thick for each plate.

Shown in Fig. 4.9 (a) and (b) are 2-d maps of the interface thermal resistance for Test Coupons 5 and 6, respectively. The background interface thermal resistance for the Kapton tape was about 0.53 K/W. The valley values for locations with 1x1 mm², 2x2 mm², 3x3 mm², 4x4 mm², and 6x6 mm² were 0.54 K/W, 0.50 K/W, 0.47 K/W, 0.37 K/W, and 0.30 K/W, respectively. Similar to the evaluation of resolution for defects, the movable sensor was able to sense low thermal resistance at the locations with heat dissipation channels larger than 1x1 mm². At the location with the 1x1 mm² Kapton tape, the decrease in thermal resistance was barely visible, which verified the limit of the thermal probe technique for measuring interface thermal resistance of samples.
Fig. 4.8. (a) thermal resistance map of Test Coupon 3, and (b) thermal resistance map of Test Coupon 4.
Fig. 4.9. (a) thermal resistance map of Test Coupon 5, and (b) thermal resistance map of Test Coupon 6.
4.4 Analysis of 2-d thermal resistance map

As demonstrated in Section 4.3, local thermal degradation will generate a peak on a 2-d thermal resistance map, while local thermal enhancement will generate a valley on a 2-d thermal resistance map. The shapes of those peaks and valleys are principally influenced by two factors: size and thermal resistance. The size influences the peak/valley valley width, and the thermal resistance influences the peak/valley height. As detailed in this section, we used parametric simulation to investigate the relationship between the defect/heat channel and the resulting 2-d thermal resistance map. We verified the measured results by comparing with simulation results.

4.4.1 Parametric simulation

For this investigation, parametric thermal simulation was applied to investigate the influence of size of defect/heat channel and its thermal resistance on the 2-d interface thermal resistance map. As shown in Fig. 4.10, the thermal model was built in ANSYS based on the parameters of the movable thermal sensor and test coupon, which are described in Section 2.4 and Section 4.2. For simplicity, the shape of the defect/heat channel was square, which corresponds to the shape of the test coupons (see Section 4.3), thereby enabling us to compare simulation result with actual measurement. It is well known that different types of defects—notably delamination, cracks, voids, microstructure change, and others—feature high thermal resistance. Additionally, there are different types of heat channels that display relatively low specific thermal resistance. Given that it was not possible to simulate all of types of defect/heat channels, in this study we concentrated on changing the thermal conductivity of the interface layer in order to change its specific thermal resistance.

In total three parameters were investigated: $a$ (the size of the defect/heat channel), $D$ (the distance from the center of defect/heat channel to the center of movable sensor), and $R_s$ (specific
thermal resistance of the defect/heat channel). By moving the sensor along the X axis, we were able to simulate the interface thermal resistance at each location.

Fig. 4.10. Model for parametric simulation of interface thermal resistance. $D$ is the distance from the center of defect to the center of the movable sensor; $a$ is the size of the defect.

4.4.2 Comparison between simulation and measurement

Fig. 4.11 provides a comparison of the interface thermal resistance increase caused by different sizes and types of defects. The background thermal interface material utilized was thermal grease, which is the same material used for the Test Coupons 3 and 4. For defect simulation, we simulated the defect size of 1x1 mm$^2$, 3x3 mm$^2$, and 6x6 mm$^2$, with defect type of air and Kapton tape. Resulting thermal conductivity measurements for air and Kapton tape were calculated to be 0.026 W/mK and 0.12 W/mK, respectively, while their specific thermal resistance was determined to be 420 mm$^2$K/W for air, and 1920 mm$^2$K/W for Kapton tape. The solid lines in Figure 4.11, depict the simulated interface thermal resistance increase as the movable sensor scanned along the X axis. For comparison, actual thermal resistance increases in measured
interface thermal resistance associated with the Kapton tape defect are depicted as the dots marks on Figure 4.11. We found that compared with the simulation result, the measured values are larger than the simulated values. This outcome was not surprising given the fact that there is contact thermal resistance between Kapton tape and copper substrates, which further increases its thermal resistance. Another finding of note is the trend toward increasing interface thermal resistance as we moved the sensor along the X axis is consistent with simulation results. This verified the accuracy of the movable sensor in detecting thermal degradations. In comparison, regardless of whether one considers simulated findings or actual experimental results, it was difficult for the sensor to detect defect sizes as small as 1x1 mm².

Fig. 4.11. Comparison between FEA simulation and measurements of interface thermal resistance change for different defect sizes.
Fig. 4.12 provides a comparison of decreases in interface thermal resistance caused by different sizes and types of heat channels. Similarly, we simulated heat channel sizes of 1x1 mm$^2$, 3x3 mm$^2$, and 6x6 mm$^2$ using heat channel factors of thermal grease and aluminum. The background thermal interface material was Kapton tape, which is the same as used for Test Coupons 5 and 6. The thermal conductivities for the thermal grease and aluminum were found to be 0.6 W/mK and 205 W/mK, respectively, while their specific thermal resistance values were determined to be 80 mm$^2$/K/W and 0.24 mm$^2$/K/W, respectively. The solid lines in Figure 4.12 depict increases in simulated interface thermal resistance as the movable sensor scan along the X axis. In comparison to our simulation results, the measured values were larger. We attribute this
difference to the fact that the thermal grease was stencil printed into the Kapton tape windows and in measurement, however the pressure applied on the thermal grease was shared by the Kapton tape. As a result, the thermal resistance of the thermal grease was larger than expected. The observed trend for the decrease in interface thermal resistance as we moved the sensor along the X axis is also consistent with simulation results, which thus verifies the accuracy of the movable sensor for detecting thermal enhancements. For both simulations, we found that the sensor was able to detect heat channel sizes as small as 1x1 mm$^2$. However, under experimental conditions, it remained difficult to identify any significant changes in thermal resistance for heat channels as small as 1x1 mm$^2$.

4.5 Guideline for design of thermal sensor

To help other researchers quickly learn the movable sensor design, fabrication and application, an application process flow chart is provided in Fig. 4.13.

One can firstly derive the effective heat spreading area $A_{eff}$ using the analytical thermal model based the original design of thermal sensor and the specification of test coupon. Then the resolution of the sensor for detecting the defects within the specific test coupon can be estimated based on equation 2.34 and previous evaluation in Section 4.3. One should decide whether this resolution is good enough. If it is good enough, one can use this sensor to generate the 2-d map of thermal resistance. Otherwise, the sensor can be modified until it meets the requirements. Next step is to evaluate the edge effect. If there is no significant edge effect, then the sensor can be used to generate 2-d map of thermal resistance. Otherwise, either the test coupon be modified to meet the requirements, or the researcher leaves enough margin between sensor and coupon edge.
Fig. 4.13. Developing process flow chart of movable thermal sensor.

4.6 Conclusion

This chapter detailed the application of the movable thermal sensor for measuring the spatial-resolved thermal resistance of the interface layer. We demonstrated the use of the movable-probe technique for 2d-mapping of the interface thermal resistance of a large-area bonded substrate. Test coupons bonded by thermal grease and sintered silver were fabricated and then characterized by
the thermal sensor. Experimental results showed that the interface thermal resistance for thermal
grease and sintered silver were 0.199 K/W, with a deviation of 0.0050 K/W (2.5%) and 0.073 K/W,
with standard deviation of 0.0053 K/W (6.8%), respectively. This data confirmed good and
uniform bonding quality for the large-area bonded sintered silver interface layer. To investigate
the sensitivity of the thermal sensor for detecting defects/heat channels of differing sizes, test
coupons were fabricated by implanting Kapton tape or thermal grease windows of various
dimensions into the thermal interface layers. The 2-d mapping confirmed that the thermal sensor
was able to successfully detect defect/heat channel sizes as small as 2x2 mm². The accuracy of the
sensitivity was verified by FEA simulation. Moreover, the simulated results were consistent with
the measured results, which indicates that the movable sensor is accurate for assessing interface
thermal resistance. At last, a process flow chart for sensor design and application was plotted to
help others use this sensor.
Chapter 5. SUMMARY AND FUTURE WORK

5.1 Summary

Interconnects in power converters result in thermal interfaces. These interfaces degrade under cyclic power, temperature, or chemical loading. Reliability of thermal interfaces can be especially problematic when the bonded area is large because the larger the area the more likely it is to have preexisting defects from processing. In order to improve the quality of the bonding process, as well as to be able to accurately quantify interface reliability, it would be desirable to have a simple, reliable, and nondestructive measurement technique that would produce a two-dimensional map of the interface thermal resistance across a large bonded area. Based on the transient thermal method of JEDEC standard 51-14, we developed a measurement technique that involves moving a thermal sensor discretely across a large-area bonded substrate and acquiring the interface thermal resistance under the sensor at each location.

In Chapter 2, to help identify the effects of different materials and structure variables of the thermal sensor on the heat flux down the heat flow path, an analytical thermal model for our measurement technique was constructed. The accuracy of the thermal model was verified by FEA simulation. Specifically, the design principle is to focus the heat flow over a smaller area of the interface to increase the heat flux density at the measurement location, thus the measurement sensitivity. Using the analytical thermal model, the following six parameters were modified to increase the sensitivity of the thermal sensor: (a) size of the semiconductor chip, (b) thermal conductivity, (c) thickness, (d) footprint of sensor substrate, (e) size of heat sink, and (f) thermal resistance between the heat sink and the test coupon. Finally, we fabricated a thermal sensor which is ready for further investigation.
In Chapter 3, the $Z_{th}$ measurement and its structure function analysis to derive thermal resistance were verified. The $Z_{th}$ measurement working principle and test procedures were introduced. Then, the accuracy of $Z_{th}$ measurement was investigated by applying the reliability measurement of sintered silver die-attach layer on Si$_3$N$_4$ AMB and AlN DBA substrates. After temperature cycling, we analyzed the failure modes via X-ray scan and SEM cross-sectional imaging to constructed a thermal model of the sintered silver layer for FEA thermal simulation. The FEA simulation showed a 15% increase in $Z_{th}$ of the DBA package (versus a 15% increase in $Z_{th}$ measurement). Additionally, to achieve the same result for the $Z_{th}$ of the AMB package, FEA simulation required 50% horizontal delamination (versus 60% by analysis of the failed sample). This result verified the accuracy of $Z_{th}$ measurement using our system. Subsequently, the sensitivity and accuracy of structure function analysis were evaluated and verified. The working principle behind the use of structure function to derive thermal resistance was introduced. The sensitivity of this approach was investigated by applying structure function at the thermal-interface layers with purposely implanted defects to modify their thermal resistance. The structure function analysis approach successfully detected the thermal resistance change in the thermal-interface layer. The accuracy of structure function analysis was investigated by measuring the thermal resistance of the sintered silver interface layer. The measured results showed good agreement with the value obtained via the other technique, thereby verifying the sensitivity and accuracy of structure function analysis for measuring interface thermal resistance.

In Chapter 4, the application of the movable thermal sensor for 2d-mapping of the interface thermal resistance of a large-area bonded substrate was firstly demonstrated. Results obtained by scanning the thermal grease bonded sample and the sintered silver bonded sample using the thermal sensor confirmed that the interface thermal resistance of the thermal grease interface was
0.199 K/W, while the interface thermal resistance of the sintered silver interface was 0.073 K/W. For the silver sintered interface, the standard variation of the interface thermal resistance was only 0.0053 K/W (6.8%), which indicated uniform bonding quality. To examine the sensitivity of the thermal sensor in detecting small defects/heat channels, we scanned the bonded sample involving differing sizes of both defects and heat channels. Results indicated that the smallest defect/heat channel size we were able to detect was 2x2 mm², which we believe is the sensitivity limitation of the thermal sensor. Parametric FEA simulation also confirmed this sensitivity data by comparing it with the measured results.

5.2 Future work

In this study, the design and application of the movable thermal sensor was investigated. While initial results are promising, this research can be further extended, and the following topics are suggested for future investigation:

1. Optimization of the thermal sensor using smaller semiconductor chips, thinner substrates, and materials with larger thermal conductive. This will further increase the sensitivity and resolution of the thermal sensor.

2. Evaluation the effect of different kinds of design on sensitivity and resolution to generate a more detailed process flow chart of the sensor.

3. Reliability characterization, which could result in useful modifications to the apparatus.

4. Further investigations should be conducted to determine possible applications of the thermal sensor for reliability characterization of bonded interfaces. In this study, only purposely implanted defects were examined. Accordingly, it would be valuable to use this thermal sensor to non-destructively scan bonded samples after reliability test.
5. Finally, additional work should be conducted to apply the thermal sensor for other power modules with different structures.
References


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Appendix A: Python code for analytical thermal model of movable thermal sensor and test coupon

In this part, the Python codes for the analytical thermal models of movable sensor and test coupon are expressed. The solution of the model yields the temperature distribution. The codes for edge effect analysis and heat flux analysis are not listed here, but can be obtained using the coefficient shown below. All the codes were executed in Python 3.6.

(1) Library used in calculating thermal model.

```python
import numpy as np
import matplotlib.pyplot as plt
import seaborn
import pandas as pd
import math
```

(2) Thermal model for movable thermal sensor

```python
# input parameters for Thermal sensor
k1 = 400
a = 0.008
b = 0.01
c = 0.005
d = 0.003
Xc = 0.004
Yc = 0.005
Q = 20
t1 = 0.0002
h = 10000

# Thermal model for thermal sensor
z=0.000

# number to sum up n, m
n = np.linspace(1,150,150)
m = np.linspace(1,150,150)
Ts = A0 + B0*z

def Temp(x,y):
    Tx = 0
```
\[Ty = 0\]
\[Txy = 0\]
\[A0 = \frac{Q}{a/b}(\frac{t1}{k1} + \frac{1}{h})\]
\[B0 = -\frac{Q}{k1}a/b\]

for \(j\) in \(m\):
\[aa = j * \text{np.pi}/a\]
\[
\text{phy\_m} = (aa * \text{np.sinh}(aa * t1) + h/k1 * \text{np.cosh}(aa * t1)) / (aa * \text{np.cosh}(aa * t1) + h/k1 * \text{np.sinh}(aa * t1))
\]
\[Am = 2 * Q * (\text{np.sin}((2 * Xc + c)/2 * aa) - \text{np.sin}((2 * Xcc)/2 * aa)) / (a*b*c*k1*aa*bb*phy\_m)
\]
\[#Tx = Tx + 2 * Am * \text{np.cos}(aa * Xc) * \text{np.sin}(0.5 * aa * c)/aa/c\]
\[Tx = Tx + \text{np.cos}(aa * x) * (Am * \text{np.cos}(aa * z) - phy\_m * Am * \text{np.sinh}(aa * z))\]

for \(i\) in \(n\):
\[bb = i * \text{np.pi}/b\]
\[
\text{phy\_n} = (bb * \text{np.sinh}(bb * t1) + h/k1 * \text{np.cosh}(bb * t1)) / (bb * \text{np.cosh}(bb * t1) + h/k1 * \text{np.sinh}(bb * t1))
\]
\[An = 2 * Q * (\text{np.sin}((2 * Yc + d)/2 * bb) - \text{np.sin}((2 * Yc - d)/2 * bb)) / (a*b*d*k1*bb*cc*phy\_n)
\]
\[#Ty = Ty + 2 * An * \text{np.cos}(bb * Yc) * \text{np.sin}(0.5 * bb * d)/bb/d\]
\[Ty = Ty + \text{np.cos}(bb * y) * (An * \text{np.cos}(bb * z) - phy\_n * An * \text{np.sinh}(bb * z))\]

for \(j\) in \(m\):
for \(i\) in \(n\):
\[aa = j * \text{np.pi}/a\]
\[bb = i * \text{np.pi}/b\]
\[cc = ((j*np.pi)/a)**2+(i*np.pi)/b)**2**0.5\]
\[
\text{phy\_mn} = (cc * \text{np.sinh}(cc * t1) + h/k1 * \text{np.cosh}(cc * t1)) / (cc * \text{np.cosh}(cc * t1) + h/k1 * \text{np.sinh}(cc * t1))
\]
\[Amn = 16 * Q * \text{np.cos}(aa * Xc) * \text{np.sin}(0.5 * aa * c) * \text{np.cos}(bb * Yc) * \text{np.sin}(0.5 * bb * d) / (a*b*c*d*k1*cc*aa*bb*phy\_mn)\]
\[Txy = Txy + \text{np.cos}(aa * x) * \text{np.cos}(bb * y) * (Amn * \text{np.cosh}(cc * z) - phy\_mn * Amn * \text{np.sinh}(cc * z))\]

\[Ts = A0 + B0 * z + Tx + Ty + Txy\]
\[\text{return } Ts;\]

\[X = \text{np.arange}(0, 0.008, 0.0001)\]
\[Y = \text{np.arange}(0, 0.01, 0.0001)\]
\[X, Y = \text{np.meshgrid}(X, Y)\]
\[\text{fig = plt.figure()}\]
\[ax = \text{fig.add_subplot}(111, projection='3d')\]
print('Ts')
print(Ts)
print('A0')
print(A0)
ax.plot_surface( X , Y , Temp(X,Y),cmap=cm.coolwarm)
plt.show()

(3) Thermal model for test coupon
  # input parameters for test coupon
  k = 100
  #coupon dimension
  a = 0.05
  b = 0.025
  t = 0.003
  #sensor dimension
  c = 0.008
  d = 0.01
  #cooler dimension
  e=0.008
  f=0.01
  #sensor location
  Xc = 0.01
  Yc =0.01
  #cooler location
  Xd= 0.01
  Yd=0.01
  #sensor power
  Q = 20
  #cooler power
  Q1 = 18
  #effective convection
  h = 20
  #set the layer location
  z= 0.000
  # number to sum up n, m
  n = np.linspace(1,100,100)
  m = np.linspace(1,100,100)

  E00 = -Q/k/a/b
  F00 = Q/a/b*(t/k+1/h)- Q1/a/b/h
\[ Ts = F_{00} + E_{00}z \]

```python
def Temp(x, y):
    Tx = 0
    Ty = 0
    Txy = 0
    for j in m:
        aa = j*np.pi/a
        Em0 = -2*Q*(np.sin((2*Xc+c)/2*aa) - np.sin((2*Xc-c)/2*aa))/(a*b*c*k*aa**2)
        Fm0 =
        Em0*(aa*np.cosh(aa*t)+h/k*np.sinh(aa*t))/aa*np.sinh(aa*t)+h/k*np.cosh(aa*t))
        Fm0 =
        for i in n:
            bb = i*np.pi/b
            E0n = -2*Q*(np.sin((2*Yc+d)/2*bb) - np.sin((2*Yc-d)/2*bb))/(a*b*d*k*bb**2)
            F0n =
            for j in m:
                aa = j*np.pi/a
                bb = i*np.pi/b
                cc = ((j*np.pi/a)**2+(i*np.pi/b)**2)**0.5
                Emn = -4*Q*(np.sin((2*Xc+c)/2*aa)-np.sin((2*Xc-c)/2*aa))*(np.sin((2*Yc+d)/2*bb)- np.sin((2*Yc-d)/2*bb))/(a*b*c*d*k*cc*aa*bb)
                Fmn =
                Emn*(cc*np.cosh(cc*t)+h/k*np.sinh(cc*t))/cc*np.sinh(cc*t)+h/k*np.cosh(cc*t))
                Fmn =
                for i in n:
                    aa = j*np.pi/a
                    bb = i*np.pi/b
                    cc = ((j*np.pi/a)**2+(i*np.pi/b)**2)**0.5
                    Emn = -4*Q*(np.sin((2*Xc+c)/2*aa)-np.sin((2*Xc-c)/2*aa))*(np.sin((2*Yc+d)/2*bb)- np.sin((2*Yc-d)/2*bb))/(a*b*c*d*k*cc*aa*bb)
                    Fmn =
                    Txy = Txy np.cos(aa*x)*np.cos(bb*y)*(Emn*np.sinh(cc*z)+Fmn*np.cosh(cc*z))
    return Ts;
```

X = np.arange(0.0, 0.05, 0.001)
Y = np.arange(0.0, 0.025, 0.001)
X, Y = np.meshgrid(X, Y)
Z = Temp(X, Y)
# plot the temperature distribution
fig = plt.figure(figsize=(10,5))
ax = fig.add_subplot(111, projection='3d')
ax.plot_surface(X*1000, Y*1000, Temp(X,Y), cmap=cm.coolwarm)
ax.set_xlabel('X (mm)')
ax.set_ylabel('Y (mm)')
ax.set_zlabel('Temperature (deg C)')
plt.show()
Appendix B: Dual pulse subtraction method for Z\textsubscript{th} measurement of SiC MOSFETs using gate-to-source voltage

Silicon carbide (SiC) have been investigated to replace silicon (Si) for development of high temperature, high power and high efficiency electronic devices. Thermal performance of a package can be characterized by the transient thermal impedance (Z\textsubscript{th}) from chip junction, which influenced by the thermal properties of the structures along heat flow path. For Z\textsubscript{th} measurement using Si IGBT, electrical methods are becoming more popular for reasons that the measurement can record temperature response very fast within 100 μs and do not interfere the power distribution of the device. This method utilizes a voltage or current as temperature sensitive parameters (TSP), which are temperature dependent values, to measure the transient temperature response. Measurements have been carried out by using different kinds of TSP. One of the most used method is to measure junction temperature by monitoring the front-to-end voltage of Si IGBT, which has a negative correlation with junction temperature when apply a constant current. Sofia uses the forward voltage of Si diode under low current to measure the temperature response. Cao et al. and Huang et al. take advantage of the threshold voltage of Si IGBT or MOSFET to measure junction temperature. Compared with drain (collector)-to-source (emitter) voltage of a semiconductor, threshold voltage has a larger sensitivity to temperature, which increases the resolution of the measurement.

However, these methods are not applicable for SiC devices because the abnormal response of temperature sensitive parameter after heating up of the device. Taking the threshold voltage method as an example, the threshold voltage should decrease after heating up the device, because of the negative correlation between the TSP and temperature. The SiC MOSFET signal increases as opposed to the normal decrease. The reason for this abnormal behavior is original in the defects
near SiO2/SiC interface. When SiC MOSFET is turned on, gate is stressed with a positive voltage and current injects through the junction. Charges are trapped at gate interface defects and decay when stress is removed, which causes instability of gate voltage. A solution to overcome the threshold instability is to use the forward voltage of body diode as TSP. When the gate-to-source voltage of SiC MOSFET is negative, the semiconductor works in reverse-diode mode, and the body diode front voltage has a linear negative correlation with temperature, which can be used as TSP. This method works well until in some application where an external diode is paralleled to the MOSFET. The reverse current is injected through both the body diode and the paralleled diode, which causes confusion in determining temperature distribution.

Here we proposed a dual pulse subtraction method to overcome the gate voltage instability issue. Specifically, as shown in Fig. B. 0.1 we separated the TSP response curve into two parts, which are contributed by electric effect and thermal effect, respectively. By subtracting the electric effect from the TSP response, we successfully got the genuine thermal effect and derived the $Z_{th}$. 
SiC MOSFET bare die (Cree CPM2-1200-0160B) was used to demonstrate the transient thermal impedance measurement. As shown in Fig. B. 0.2(a), the SiC chip was bonded on a Si3N4 AMB substrate (DOWA Metaltech Co., Ltd) by a pressure-less silver sintering technique (NBE Technologies, LLC.) and then wire bonded to the corresponding electrode pads. The SiC junction temperature was measured by a customized device as shown in Fig. B. 0.2(b). This method utilized the self-heating of the device at high current level and the linear temperature dependence of gate voltage at low current level to measure the temperature response after a heating pulse. In our test, the drain voltage across the device was 5 V and the current was 2 A and 2 mA for heating and sensing, respectively. The gate voltage was manipulated via the feedback loop in order to maintain constant current. Fig. B. 0.2(c) shows the normal waveforms of Si devices under test. One can
observe a decrease of $V_{gs}$ at the end of heating pulse (as opposed to the abnormal increase for SiC devices) and derive the temperature change based on $\Delta V_{gs}$.

The electric effect that causes the abnormal rise in waveform is caused by charges induced by SiO2/Si interface defects. These charges were trapped at the interface during high gate voltage and high current, and then decay when gate voltage decreases and current level drops. It is reported that the trapped charge was energetically located at the ultra-shallow level below conduction band and its impact on threshold voltage is reversible and repeatable. So the defect-trapped-charge can be presumed to saturate within one millisecond and the corresponding electric effect has a constant
influence on the gate threshold voltage. Fig. B. 0.3 is the waveform after the current was switched from high level to low level. When heating time is short enough, the thermal effect is negligible, so the gate voltage curve was totally caused by electric effect. In our case, we choose the short heating period of 0.2 ms, 0.3 ms, and 0.5 ms. It should be noticed that the decay waveforms for heat time of 0.2 ms, 0.3 ms, and 0.5 ms almost overlap. This indicates the charge density was saturated and will not change along with heating time.

![Waveform of gate voltage during temperature measurement.](image)

The key for this hypothesis is the energy level of the trapped charge is relative low so that the charge can be saturated within a short period of time. After saturation, the defect charge density remains the same, charge decay waveforms are consistent, and thus the electric effect is immutable. To verify this hypothesis, we measured the activation energy of the charge decay curve to find the
typical trapped charge energetic level at the gate interface. To minimize thermal effect, the heating pulse was set as 0.2 ms. This heating time has been proved to minimize self-heating effect, but long enough to saturate the defect charge as demonstrated previously. At the end of heating pulse, we switched the current to 2 mA to record the electric decay curve. An exponential decay curve can be expressed by:

\[ N = N_0 e^{-kt} \]

Where \( k \) is the decay rate constant, \( N_0 \) is the amplitude at beginning, and \( N \) is the amplitude at a given time \( t \). We derived the decay rate constant by applying least squares curve fitting. The decay rate constant is a temperature dependent parameter and can be expressed in Arrhenius equation

\[ k = A e^{-E_a / k_B T} \]

or

\[ \ln k = \ln A - \frac{E_a}{k_B T} \]

Where \( E_a \) is the activation energy, \( k_B \) is Boltzmann constant, \( T \) is absolute temperature, and \( A \) is pre-exponential factor. As shown in Fig. A. (a), tests were conducted at different temperature, from which the decay rate constant changed with temperature. We can get the Arrhenius plot as shown in Fig. A. (b). By applying least square linear fitting, we got the activation energy of the decay curve is averagely located at 0.08 eV, which is consistent with the reported value which ranges between 0.05 eV to 0.2 eV.
Fig. A. B. (a) Charge decay waveform and (b) Arrhenius plot
So we can get thermal effect and derive temperature response of a SiC device by subtracting the electric effect from the abnormal waveform. As shown in Fig. B. 0.4(a), we first applied a very short heating pulse with length of $\tau_1$ to get the $V_{gs}$ sensing waveform caused by intrinsic electric effect. Then the heating pulse period was changed to $\tau_2$. Because the heating time is much longer, the $V_{gs}$ waveform contained both thermal and electric effect. Fig. B. 0.4(b) is the $V_{gs}$ waveform after subtraction, and the intrinsic thermal effect can be expressed in:

$$V_{gs}(\tau_2 - \tau_1) = V_{gs}(\tau_2) - V_{gs}(\tau_1)$$

And the temperature response is:

$$T(\tau_2 - \tau_1) = \frac{V_{gs}(\tau_2) - V_{gs}(\tau_1)}{K}$$

We should notice that length of $\tau_1$ should be based on the dimension of SiC chip. One can simply calculates the temperature increase after heating up for $\tau_1$ by

$$\Delta T(\tau_1) = P \times \frac{h}{kA} \left(1 - e^{-\frac{t}{h^2\rho c/k}}\right)$$

In which P is the heating power, h is the thickness of SiC chip, A is the active heating area of SiC chip, k is thermal conductivity of SiC, $\rho$ is density of SiC, and c is specific heat of SiC.
Fig. B. 0.4. (a) Dual pulse measurement and (b) genuine thermal effect waveform after subtraction.