Modeling and Design of a SiC Zero Common-Mode Voltage Three-Level DC/DC Converter

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Electrical Engineering

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Abstract

As wide-bandgap devices continue to experience deeper penetration in commercial applications, there are still a number of factors which make the adoption of such technologies difficult. One of the most notable issues with the application of wide-bandgap technologies is meeting existing noise requirements and regulations. Due to the faster dv/dt and di/dt of SiC devices, more noise is generated in comparison to Si IGBTs. Therefore, in order to fully experience the benefits offered by this new technology, the noise must either be filtered or mitigated by other means.

A survey of various DC/DC topologies was conducted in order to find a candidate for a battery interface in a UPS system. A three-level NPC topology was explored for its potential benefit in terms of noise, efficiency, and additional features. This converter topology was modeled, simulated, and a hardware prototype constructed for evaluation within a UPS system, although its uses are not limited to such applications. A UPS system is a good example of an application with strict noise requirements which must be fulfilled according to IEC standards.

Based on a newly devised mode of operation, this converter was verified to produce no common-mode voltage under ideal conditions, and was able to provide a 6 dB reduction in common-mode voltage emissions in the UPS prototype. This was done

while achieving a peak efficiency in excess of 99% with the ability to provide bidirectional power flow between the UPS and battery backup. The converter was verified to operate at the rated UPS conditions of 20 kW while converting between a total DC bus voltage of 800 V and a nominal battery voltage of 540 V.

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General Audience Abstract

As material advancements allow for the creation of devices with superior electrical characteristics compared to their predecessors, there are still a number of factors which cause these devices to see limited usage in commercial applications. These devices, typically referred to as wide-bandgap devices, include silicon carbide (SiC) transistors. These SiC devices allow for much faster switching speeds, greater efficiencies, and lower system volume compared to their silicon counterparts.

However, due to the faster switching of these devices, there is more electromagnetic noise generated. In many applications, this noise must be filtered or otherwise mitigated in order to meet international standards for commercial use. Consequently, new converter topologies and configurations are necessary to provide the most benefit of the new wide-bandgap devices while still meeting the strict noise requirements. A survey of topologies was conducted and the modeling, design, and testing of one topology was performed for use in an uninterruptible power supply (UPS).

This converter was able to provide a noticeable reduction in noise compared to standard topologies while still achieving very high efficiency at rated conditions. This converter was also verified to provide power bidirectionally—both when the UPS is charging the battery backup, and when the battery is supplying power to the load.

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Chapter 1. Introduction

1.1. Background

Electromagnetic interference (EMI) is a necessary consideration for almost any converter. In many commercial applications, there are strict regulations which dictate acceptable EMI levels for various systems. To meet these regulations, one must either operate their converters in such a way as to produce very little noise and/or use passive components to filter the remaining noise [1]. This ensures the devices will provide power reliably and that the system and its connected devices will continue to operate.

One application which has such regulations is an uninterruptible power supply. IEC standards have specific rules for acceptable limits for both common-mode and differential-mode noise. Although these noise levels are measured at the AC input of the UPS, it is important to note that each stage of the UPS has an effect on the total system noise profile. The DC/DC converter interface between the DC link of the UPS and the battery backup has a significant adverse effect on the noise profile of the system as a whole. This is due to the internal connections of the UPS as well as external parasitics such as the grounding configuration of the battery cabinet, which worsens the common-mode voltage profile of the system. An example of a UPS configuration which suffers from this issue is shown. [2]
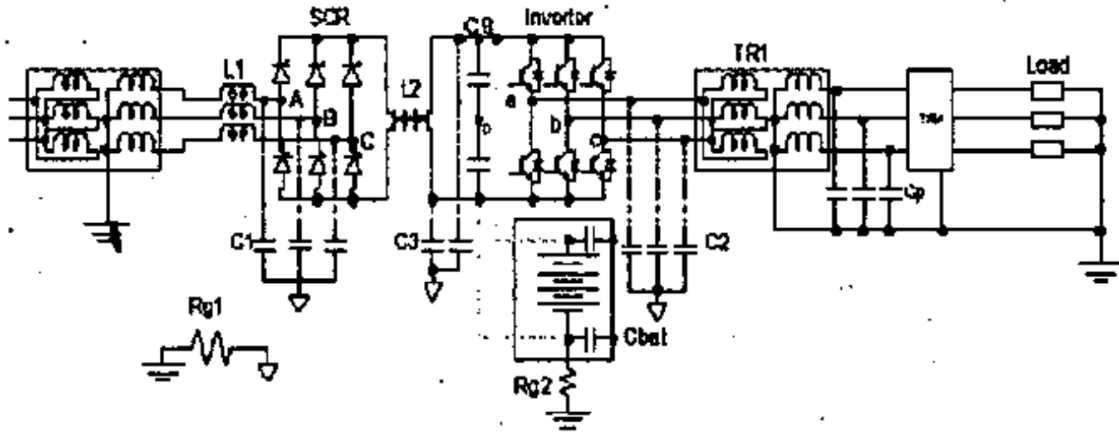
Figure 1.1. Example UPS System with Battery Ground Parasitic Impedance

The figure demonstrates the parasitic impedance between the battery cabinet ground and internal ground of the system. Also included in this work was a comparison of the EMI profile of the system when the battery was connected to the system and when the battery was left disconnected. When the battery is connected, the UPS EMI profile is significantly higher, confirming the adverse effects of the DC/DC stage connections on the system. In the following figure, the case where the battery is connected is shown on the left, and the case where the battery remains disconnected is shown on the right.
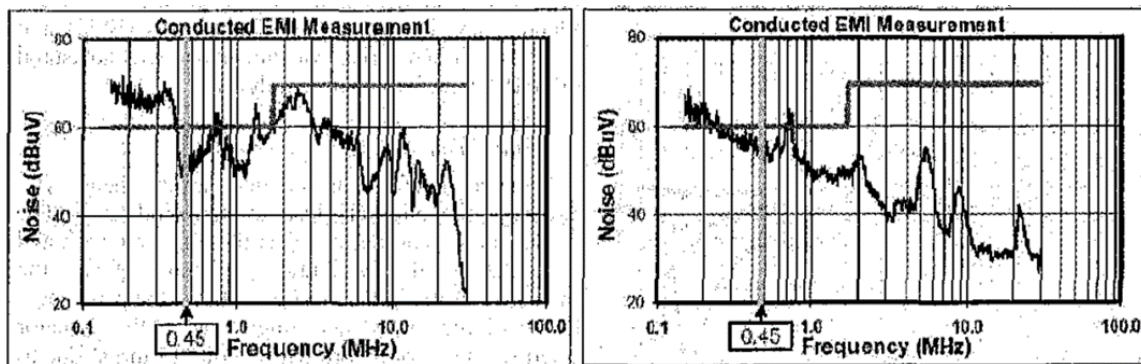
Figure 1.2. Conducted EMI Comparison with and without Battery Connection

The converter detailed in this thesis was designed with a different UPS configuration in mind. However, despite some differences in topology and configuration,

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similar parasitics are still present, and lead to a deterioration in the EMI profile due to the operation and configuration of the DC/DC stage. The UPS for which this topology was designed is a three-phase, three-level, neutral-point-clamped (NPC) system. Figure 1.3 shows a three-terminal model which demonstrates how the three different converters are able to interact with one another to create a single noise profile in the three-level NPC UPS mentioned previously. [3]
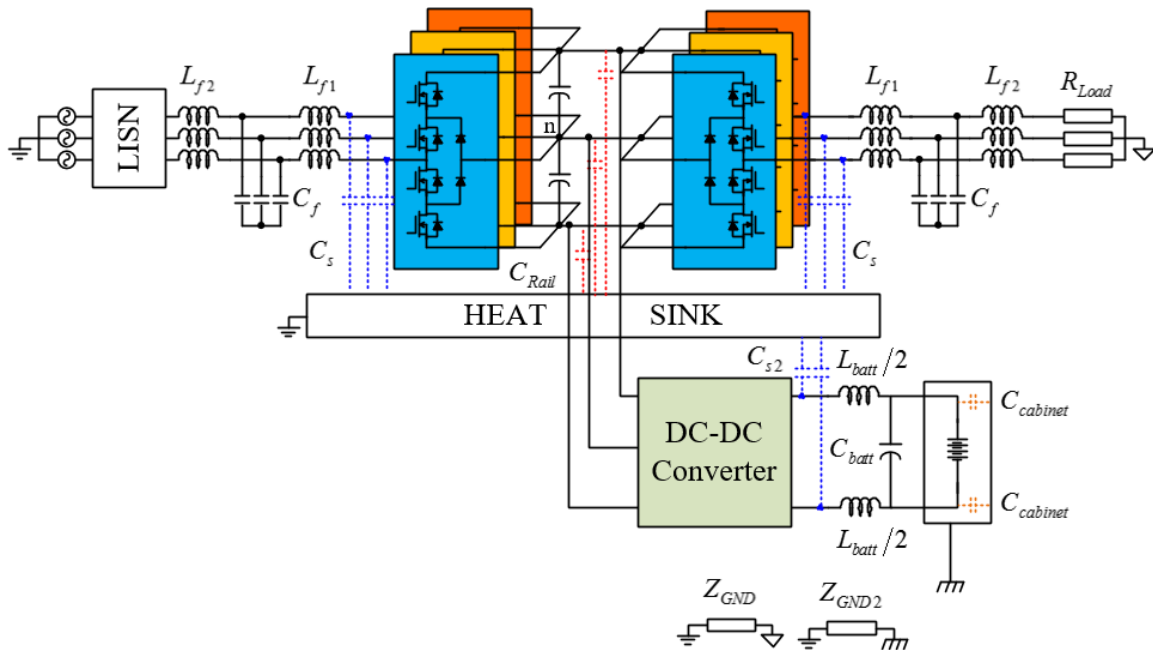
Figure 1.3. Three Terminal UPS Model

In this figure, a complete UPS system is shown. This system represents the system in which the DC/DC converter will be installed, and for which the converter is deigned. The UPS consists of a three-phase, three-level inverter, a DC link, a three-phase, three-level rectifier, and a DC/DC interface between the UPS DC link and the battery backup. It can be seen that the inverter, rectifier, and DC/DC stage each have an impact on the noise profile seen at the input of the UPS not only through the internal

connections of the UPS, but also through external parasitics such as the impedances between electrical and earth grounds, and the capacitances between various potentials and the shared heat sink potential of the system. For these reasons, it is important that the noise profile of the DC/DC converter to be used in such a system is carefully considered.

The benefit of a low emission DC/DC converter may also be applied to various other applications, such as energy storage systems or electric vehicles which may have a DC/DC converter which interfaces with a DC/DC converter. As these applications are largely commercial, additional targets are set for the converter characteristics. It is important that the converter meet EMI standards, but the converter should be able to do so while maintaining the high efficiency and greater power density expected of SiC technologies. ("SiC improves switching losses, power density and volume in UPS,").

The cost of the converter in these applications is also a noteworthy consideration. Additional functionality and greater efficiency are attainable by a number of means, but these should not be sought in such a way that makes the converter impractical to manufacture. For example, the use of more devices allows for more flexibility in the switching sequences and commutation loops of the converter, which may provide some benefit, but if the number of costly SiC devices necessary is too numerous, the topology will not be adopted.

Additionally, due to the operating nature of a UPS, it is important that the topology is capable of providing bidirectional power flow at rated conditions. There are a number of different operating conditions within a UPS, and due to events such as the grid losing power, or the battery needing to charge quickly, it is important that the DC/DC converter is able to provide all power necessary to the battery from the UPS

rectifier using grid power, or that the DC/DC converter can supply rated power to the AC load through the inverter.

One final benefit of this topology which is explored is its ability to provide DC link neutral point regulation to the system. The ability to balance the DC link of a system such as this is crucial, and will realize additional benefits not only limited to noise [4] [5]. The converter is able to regulate the DC link in both buck and boost mode operation, which allows it to provide some benefit to the system while charging the battery, and to provide a balanced DC bus voltage to the system when the battery is supporting the load. Although there are many examples of this type of converter which also detail this balancing process [6] [7] [8], the model I developed independently and its implementation will be shown.

1.2. Thesis Outline

The focus of this thesis is to discuss in detail the steps taken during the design and testing of a bidirectional SiC DC/DC converter for use in a UPS. This converter served as the interface of the UPS DC link and battery, and the topology should be useful for a variety of applications with an energy storage which needs to interface with a DC bus. Topology comparisons, modeling and simulation, hardware design, and experimental evaluation will be included in a comprehensive manner.

In chapter 1, the motivation for an efficient, low noise, high power density DC/DC converter is discussed. The relevant specifications of the converter for a UPS system are also discussed and will be used as part of the basis of the topology discussion in later sections. The importance of EMI and its impact on the UPS from the DC/DC stage are also stressed.

In chapter 2, a number of potential topologies are discussed as candidates for the UPS system and are compared using simulation results. These results include common-mode voltage profiles and preliminary simulation results. The topologies are then evaluated for their various pros and cons and the reasoning is provided for selecting the final topology which is the subject of this thesis.

Chapter 3 goes into more detail regarding the modeling of the converter. The process of deriving an average model and subsequently making a small signal model is shown in complete form. This model is then used to develop equations which govern the design of a simple controller to regulate the neutral midpoint of the DC bus. This model is then simulated alongside a complete switching model to verify its validity, and to test the functionality of a controller based on the equations developed.

Chapter 4 discusses the means by which a more detailed simulation of the converter was performed. This includes performing loss extraction via double pulse testing, using said loss data to model the module more accurately in simulation, and using the more accurate model to determine necessary parameters within the converter. Also, the assembly of the converter by itself, then in conjunction with the UPS is shown.

Chapter 5 discusses experimental results of the converter operating by itself, and in conjunction with the UPS system. In this section, efficiency is measured over a range of operating points, the control methodology developed in section 3 is verified, and the noise benefit to the overall system is examined in more detail.

Chapter 6 includes a brief summary of the work completed and the results of the work. It also reiterates the benefits of the topology, potential uses, and value of work

performed. Also discussed are potential avenues for future work to better understand and utilize this topology in various applications.

1.3. Contributions

This work has been presented and published in a few different ways. The work, and portions of it, has been displayed at the PowerAmerica Annual Review meeting in 2017. It was also shown as a poster at the CPES Annual Conference in 2017 as a poster, and a paper on the project was published at the CPES Annual Conference in 2018 along with a poster presentation. Finally, the work is also published at the IEEE Energy Conversion Congress and Exposition (ECCE) in 2018.

Chapter 2. Topology Comparison and Evaluation

2.1. Project Requirements and Converter Specifications

The motivation for this work, as mentioned in the introduction, is primarily to develop an efficient, bidirectional, low noise DC/DC converter for use in UPS applications. There were a number of different DC/DC topologies considered [9] [10] [11] [12] [13], but due to the nature of the project, there were some topologies which were not considered entirely. For example, due to the time constraints of the project, it was determined that isolated converters would not be considered as these topologies would be too time-consuming to design and construct. Additionally, due to the desire to maximize power density, it was desirable to make the DC/DC converter with as few components as possible in order to easily determine the best physical layout to minimize the volume of the UPS.

Additionally, as the inverter and rectifier stages of the UPS were three-level NPC modules, the DC link of the system consists of two capacitors in series, splitting a total 800 V DC bus into two split buses at 400 V each. For this reason, it was determined that there may be some additional advantage of having a DC/DC converter which would be able to transfer power to and from either of the DC link potentials and battery backup. Finally, the common-mode noise profile of the converters was to be considered. As previously explained, the noise profile of the DC/DC converter will affect the overall noise profile of the UPS. Therefore, it is beneficial to consider the natural noise profile of the DC/DC converter to see if any topologies have an advantage over others simply due to their operation.

2.2. Buck Converter

The first topology considered was a simple buck converter. This converter is the simplest proposed topology as it consists of only two switches. Additionally, due to the limited number of active devices, it was anticipated that the buck converter would have very high efficiency as the conduction losses will be at a minimum compared to other topologies which include multiple devices.
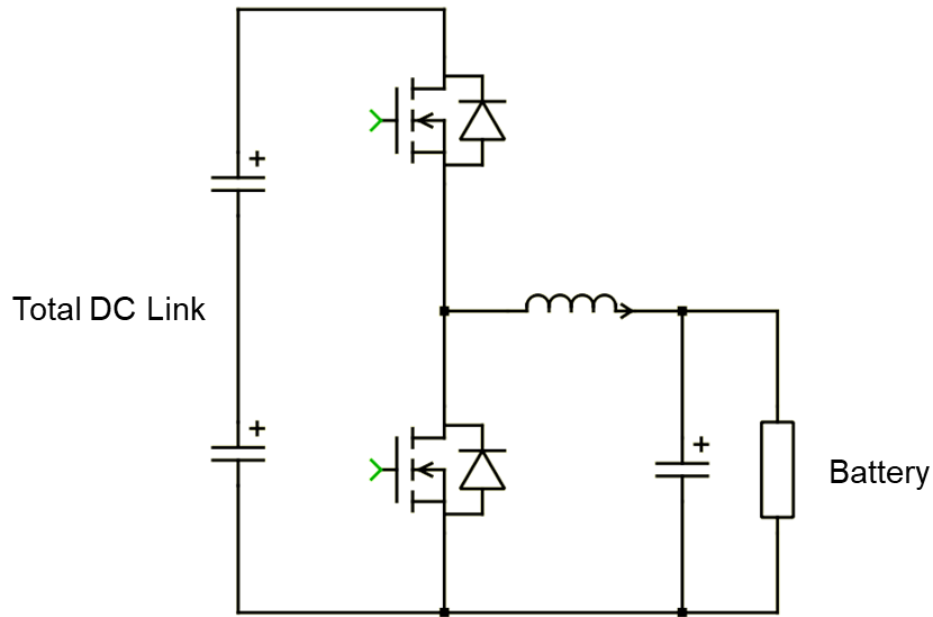
Figure 2.1. Buck Converter

However, the simplicity of the buck converter also comes with some

disadvantages. For example, the buck converter is only able to utilize one input potential

and one output potential. This means that the simple buck converter will only be able to

transfer power from the entire DC link, the upper DC link, or the lower DC link. Also,

due to the natural asymmetry of the buck converter, there is no way to reduce the

common mode voltage profile of the converter without adding filters. As the buck

converter is very well known and there is very little variation available with regards to

the switching sequence of the converter, its operation will not be discussed in detail.

2.3. Three-Level Buck Converter

The next topology considered is a three-level buck converter. This is the topology

which is the main subject of this paper. This topology consists of four SiC MOSFETs

arranged in a three-level neutral-point-clamped configuration. This configuration is the

same as that used by the inverter and rectifier stages of the UPS. In comparison to the

simple buck converter, this topology has the added benefit of additional switching

sequences which may be used for different desired functionality. Also, this converter

does have a connection to the DC neutral point of the DC bus. This means there may be

asymmetrical power flow between the DC link and battery.
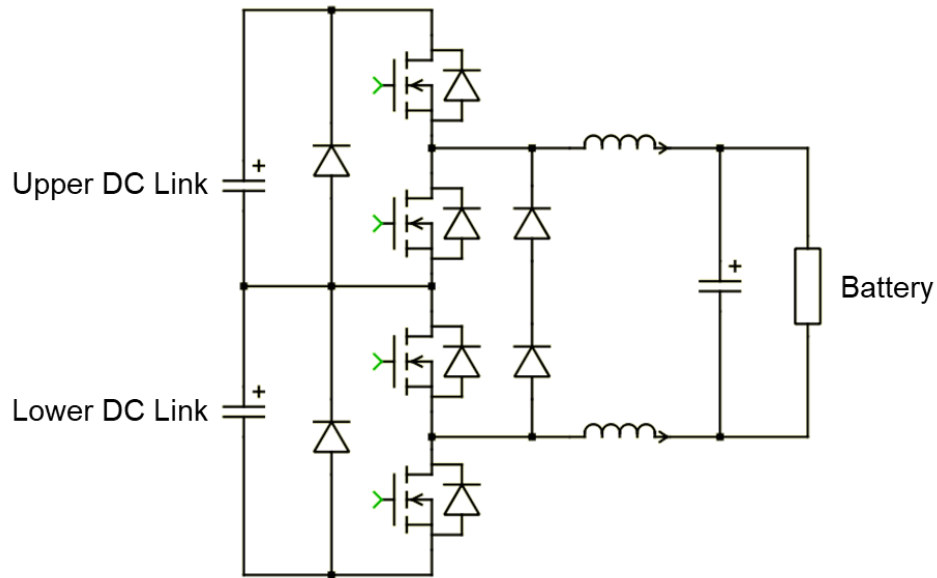
Figure 2.2. Three Level Buck Converter

Note that there are a number of diodes included in the schematic above which do

not appear to be critical to the function of this converter. This is because the topology

shown above is that of the actual NPC module used in the inverter and rectifier stages of

the UPS. Although these diodes are necessary for AC/DC conversion, they are

extraneous in the operation of the three-level buck converter. They are only included

here for the sake of completeness.

One last major benefit of this topology is the ability to decouple each pair of

switches from one another to achieve different results. The upper two switches and lower

two switches must operate in a complementary fashion in order to prevent a short-circuit

condition with the DC bus. However, the switching sequences of each pair with respect

to one another can be anything. This means the duty cycles of the two pairs can operate

synchronously, complementary, or with a phase-shift to achieve different results in each

case. The traditional applications for this type of converter utilize this phase shifted

operation to halve the output current ripple. However, when there is no phase shift and

the two pairs operate synchronously, there is ideally no common-mode voltage generated,

which is beneficial for noise. The synchronous operation is shown below.

Power transfer between
total DC link and battery

Freewheeling state
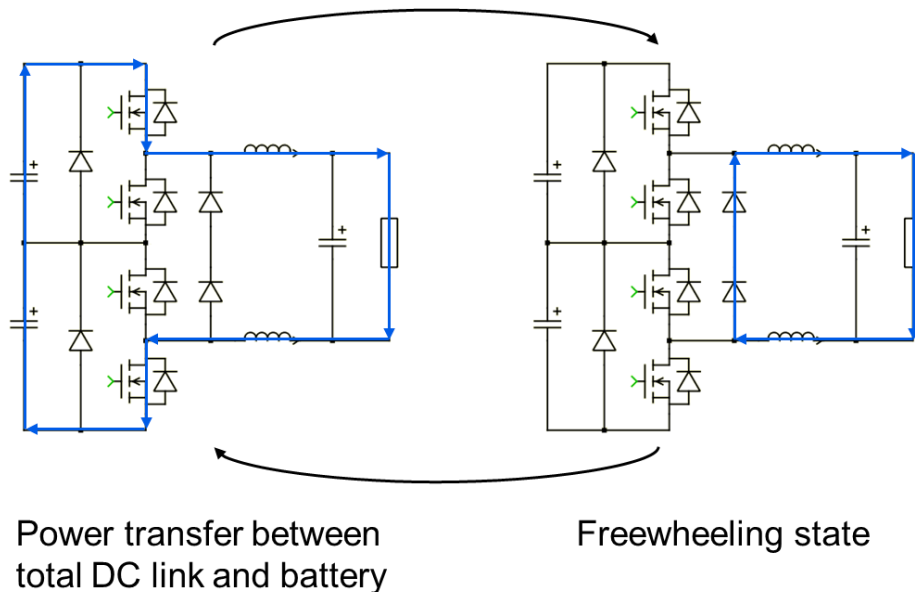
Figure 2.3. Three-Level Buck Converter Synchronous Operation

In this mode of operation, the topmost and bottommost switches operate

synchronously. As the middle devices must operate in a complementary fashion to their

adjacent outermost devices, they also operate synchronously with one another. This

mode of operation allows the converter to maintain a symmetric voltage profile with

respect to the battery, meaning there should be no common-mode voltage output under ideal conditions. The phase-shifted mode of operation is shown below as well.

Power transfer between
upper DC link and battery

Power transfer between
total DC link and battery

Power transfer between
lower DC link and battery
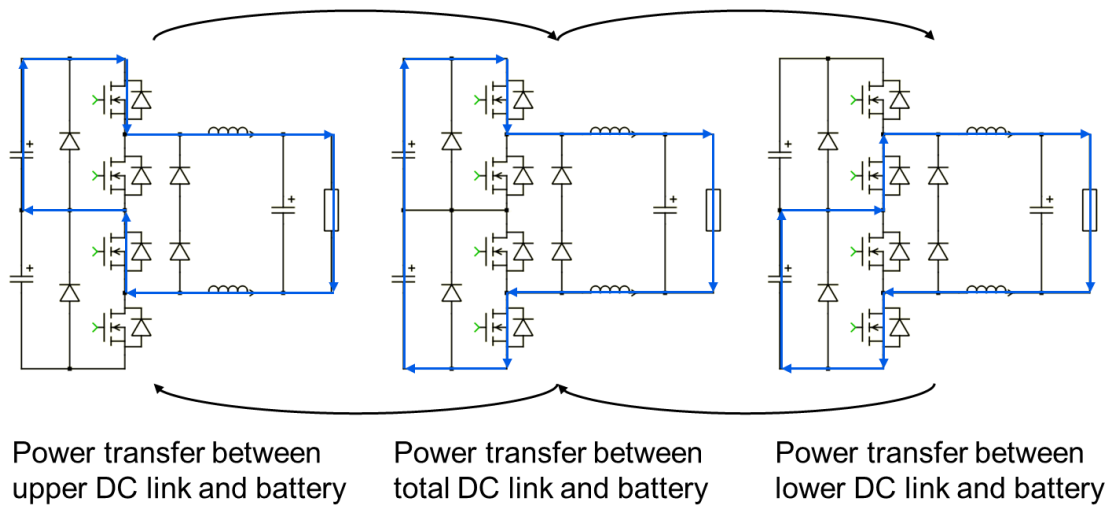
Figure 2.4. Three Level Buck Phase Shifted Operation when Vdc/2 < Vbatt

Power transfer between
upper DC link and battery

Freewheeling state

Power transfer between
lower DC link and battery
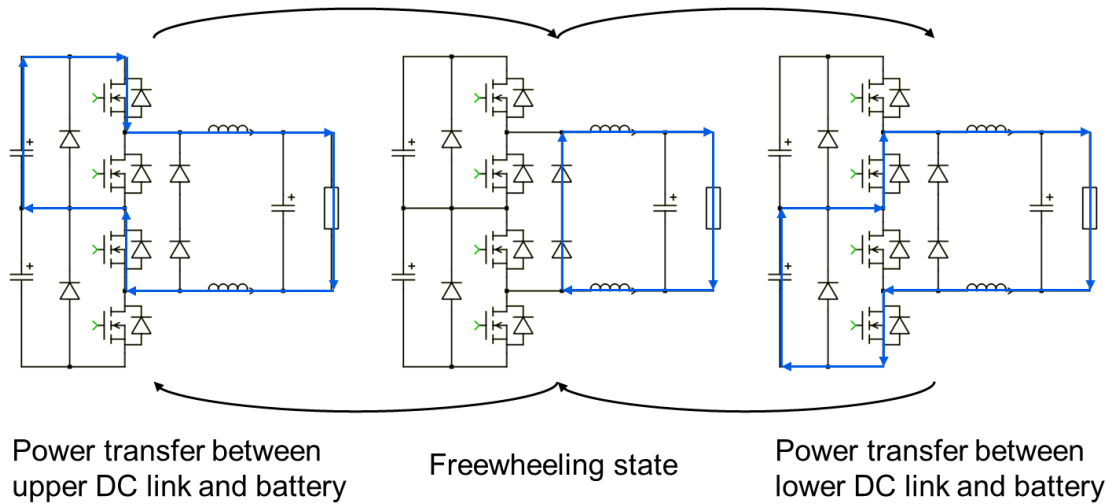
Figure 2.5. Three Level Buck Phase Shifted Operation when Vdc/2 > Vbatt

As demonstrated in the preceding figures, there are two slightly different switching sequences for the phase-shifted operation. This is because the battery voltage is not constant, and will increase or decrease as it is charged or discharged, respectively. When the battery voltage is less than half of the total DC link voltage, a freewheeling

state is necessary to maintain volt-second balance. However, when the battery voltage is greater than half of the total DC link voltage, this freewheeling state is replaced by a state whereby the entire DC link transfers power to the battery.

2.4. PEBB-Based Converter

One of the topologies investigated was a PEBB-based converter which can also be constructed using three-level NPC inverter modules. This converter uses two such modules and the battery is connected between the outputs of each of these converters. This topology was considered as it has a distinct advantage of offering more switching states than any other topology discussed. It was investigated whether this would provide any additional noise and/or output current ripple benefit in comparison to the other topologies discussed.
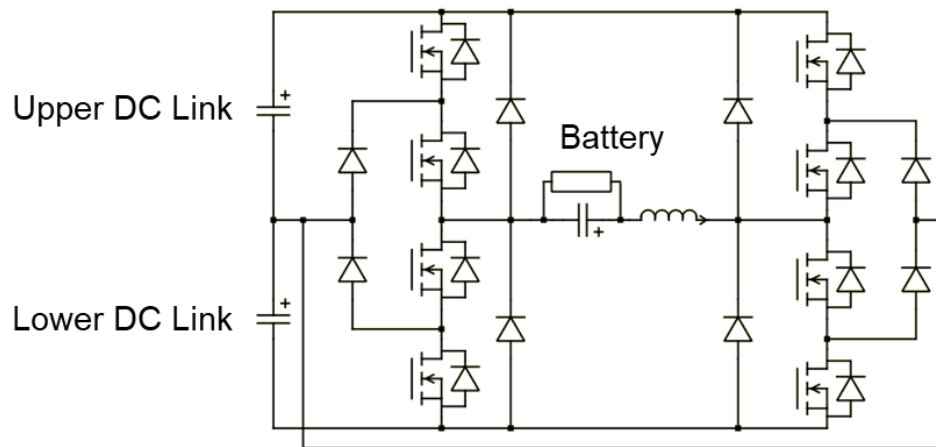
Figure 2.6. PEBB-Based Converter

The two main drawbacks of this converter are efficiency and the number of modules needed to construct it. The efficiency is expected to be low due to high conduction losses. At any given time, this converter will always have more devices conducting current than the simple buck converter. Additionally, 8 devices are needed

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for this topology compared to the two needed by the buck converter and 4 needed by the three-level buck converter.

The operation of this converter is very similar to that of the three-level buck converter as it is also a three-level NPC variant. However, as the battery is connected between the outputs of two NPC phase legs, their switching states are slightly different. Once again, there is a synchronous operation mode and a phase-shifted operation mode. Both operating modes are shown in the following figures.
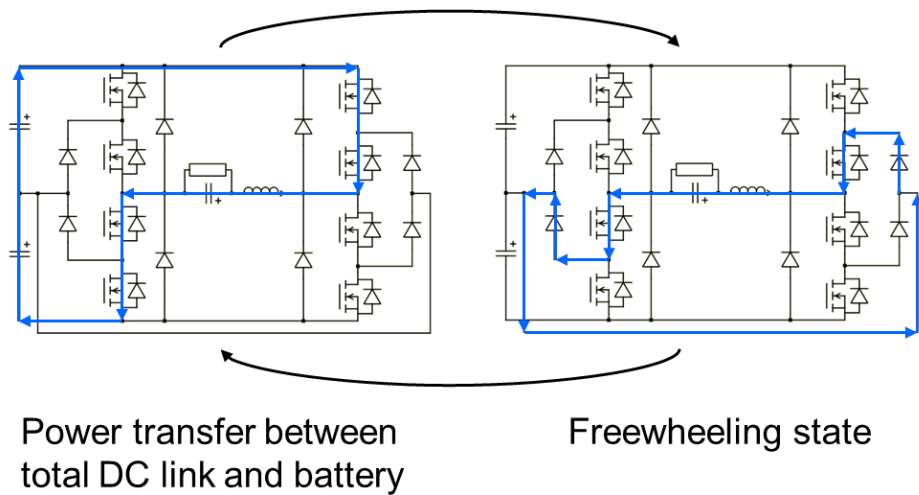
Power transfer between
total DC link and battery

Freewheeling state

Figure 2.7. PEBB-Based Synchronous Operation

Power transfer between
upper DC link and battery

Power transfer between
total DC link and battery

Power transfer between
lower DC link and battery

Figure 2.8. PEBB-Based Phase Shifted Operation when Vdc/2 > Vbatt

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Power transfer between upper DC link and battery   Freewheeling state   Power transfer between lower DC link and battery
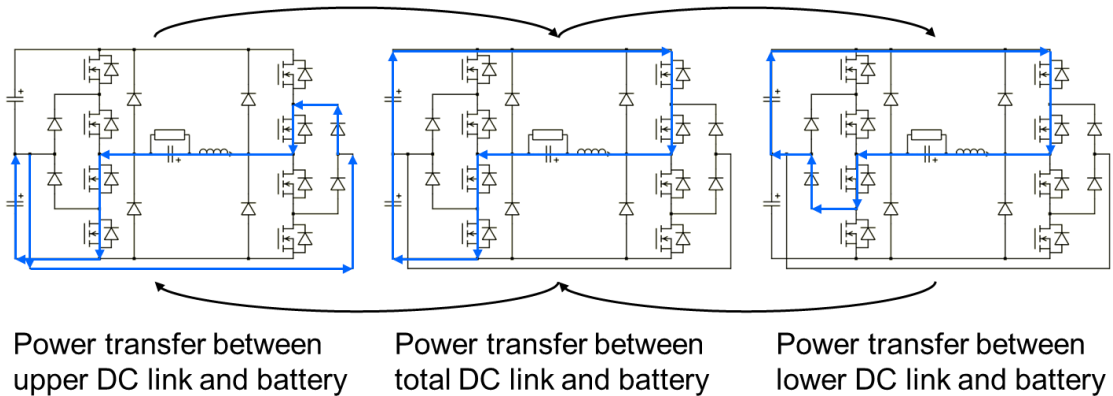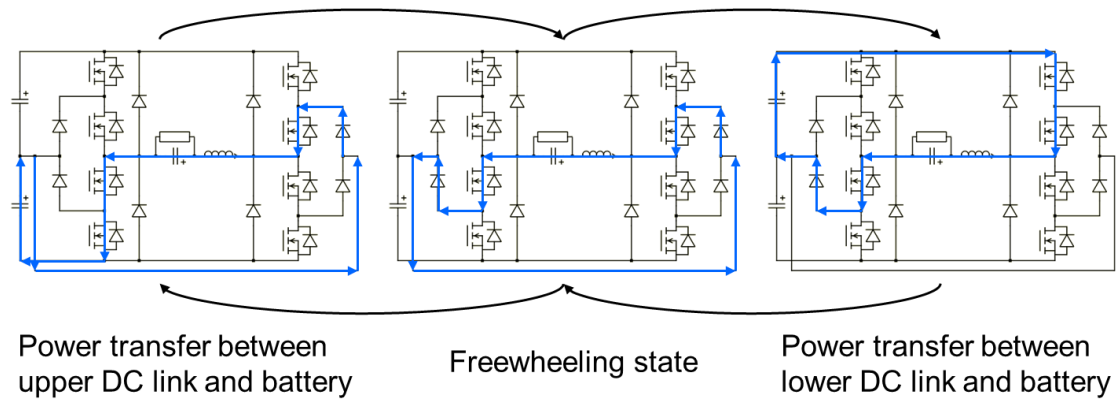
Figure 2.9. PEBB-Based Phase Shifted Operation when Vdc/2 < Vbatt

It is also important to note that the PEBB-based converter has two additional freewheeling states which can be utilized by turning on the upper two or lower two switches of both NPC phase legs. This allows the current stored in the battery filter inductor to freewheel at either the positive or negative DC bus potential. This also comes at the cost of potentially higher conduction losses as two devices must conduct for this freewheeling to occur. The current may also pass through the device antiparallel diodes on one side of the battery for this freewheeling operation.

2.5. Interleaved Three-Level Buck Converter

The last topology considered is an interleaved version of the three-level buck converter discussed in section 2.3. This topology operates under the same principles as the non-interleaved three-level buck converter, but due to interleaving, it is able to halve the output current ripple and provide twice the output power when compared to the single three-level buck converter case. This topology possesses all the same benefits of the three-level buck including asymmetric power transfer between upper and lower DC link.

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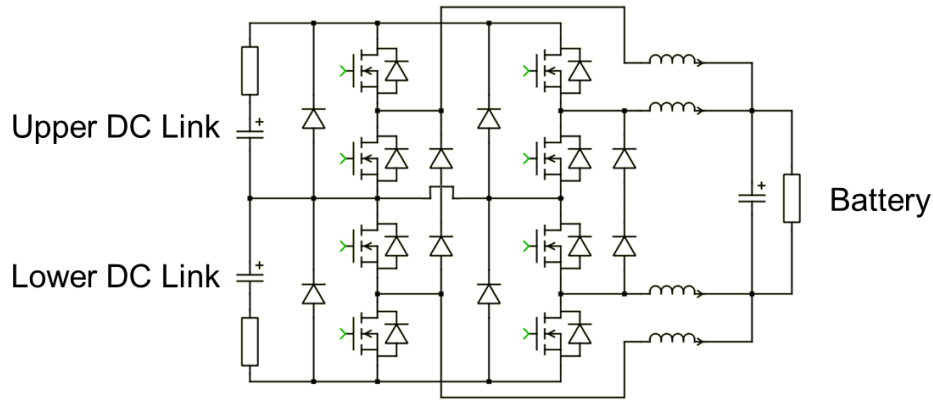
Figure 2.10. Interleaved Three-Level Buck Converter

Despite the benefits of interleaving when compared with the single converter case, there are certainly some disadvantages of using this topology. For example, this topology would likely require more volume when compared to the single converter case due to the additional devices, necessary gate driver components, and additional magnetics. For these reasons, this topology was evaluated not as a direct competition to the single converter case, but as a necessary extension of that topology if the single converter was not able to provide the necessary rated power to support the UPS. Due to the nature of this topology, its switching sequences and basic operation will not be discussed as this converter is simply an interleaved extension of the three-level topology discussed previously.

2.7. Common-Mode Voltage Simulations and Waveforms

In order to determine which converters, if any, provided some benefit in terms of common-mode voltage emissions, it was necessary to simulate the converters to capture their common-mode voltage profiles. To do this, each converter topology was simulated under ideal conditions using the PLECS plugin for MATLAB Simulink. Each converter was simulated under standard operating conditions, as well as with a phase-shifted

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operation to reduce output current ripple if applicable. In each simulation, the total DC

link was 800 V and consisted of two 400 V ideal DC sources in series. The output

voltage was set at a nominal voltage of 540 V. Waveforms of each type of operation for

the various converters are shown.
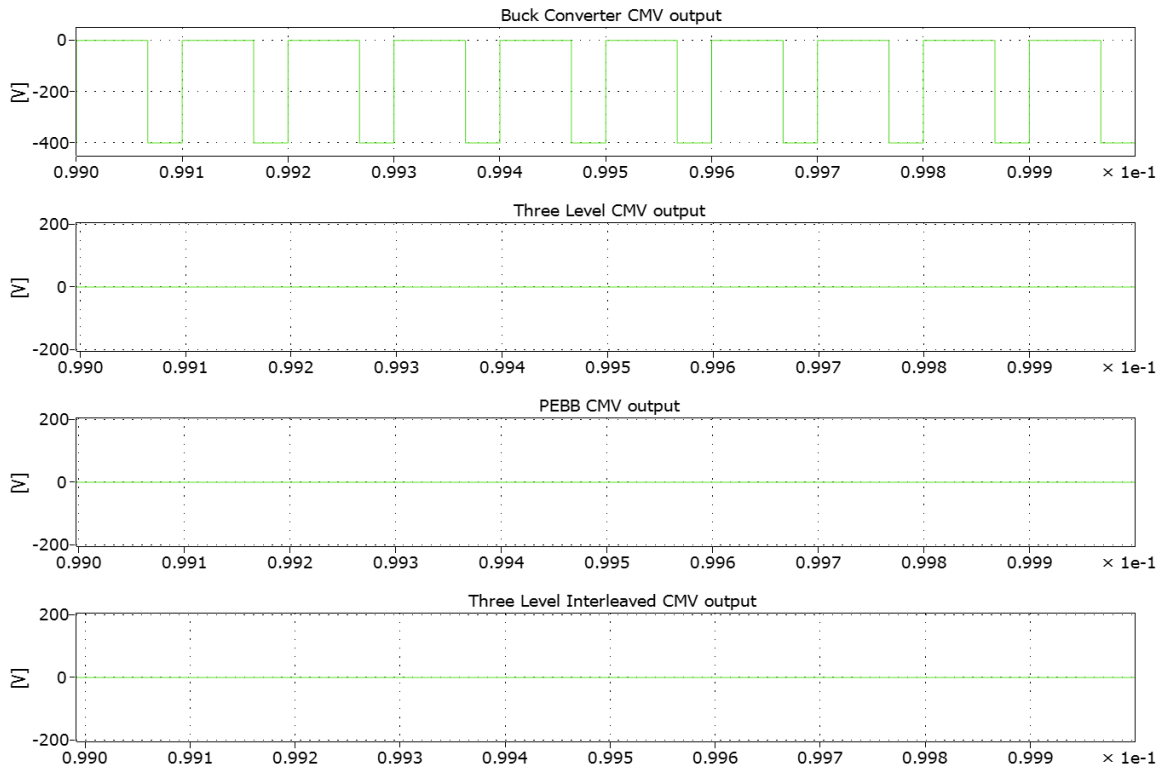
Figure 2.11. Standard Common-Mode Voltage Waveforms
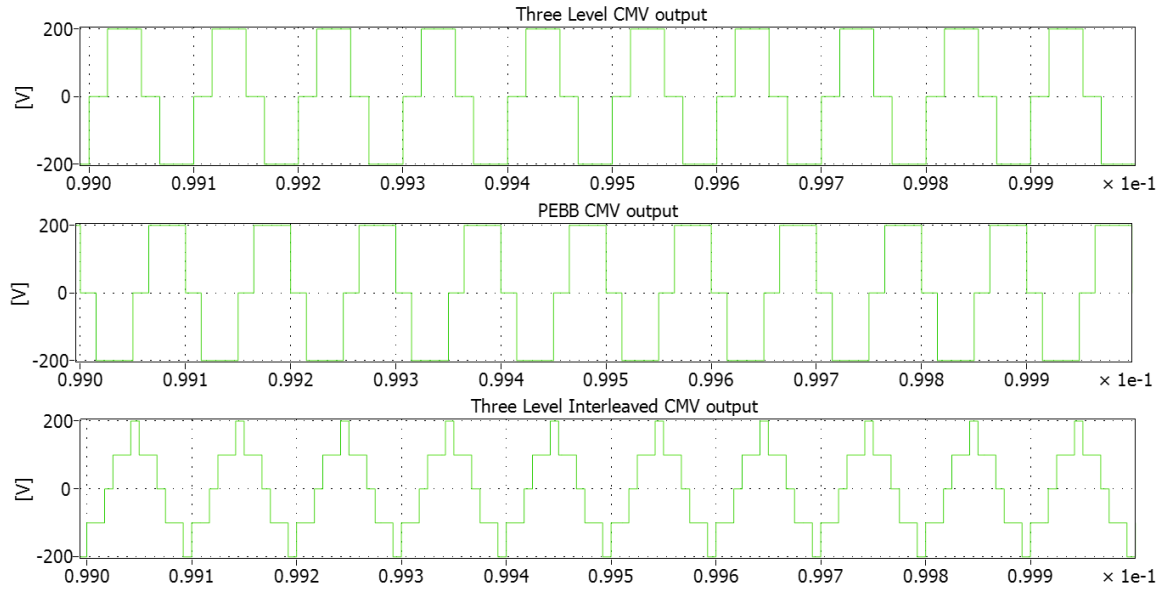
Figure 2.12. Phase Shifted Common-Mode Voltage Waveforms

As demonstrated in the preceding waveforms, the common-mode voltage output of the converters is as expected. The buck converter has a CMV pulse of -400 V which corresponds to the common-mode voltage of the converter while freewheeling. Also, those converters which are able to operate in the symmetrical synchronous switching manner described previously do not produce any common-mode voltage under ideal conditions.

Also, in the phase-shifted operation, some similarities and differences are noted. Recall that this kind of operation is typically used to halve the output current ripple to reduce the output filter components. As the simple buck converter is not capable of such operation, it is excluded from these results. When the converters operate in such a fashion, there is some common-mode voltage generated which corresponds to switching states where power is transferred asymmetrically from only one of the DC link potentials. Although there are more non-zero pulses when compared to the simple buck converter,

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the magnitude of these pulses is only 200 V, meaning that the overall impact of this operation on the UPs is expected to be similar to that of the buck converter.

At this point, the PEBB-based topology was no longer considered. This is because the additional switching states and functionality of the converter are not utilized due to the fixed polarity of the battery. If the battery voltage were to somehow fluctuate in sign as well as magnitude, this topology would be considerably more useful. As it stands, however, it is simply a costlier, less effective version of the three-level buck converter

2.6. Efficiency Simulations and Comparison

Once the benefits and drawbacks of each topology's impact on the UPS noise profile were better understood, it was necessary to evaluate the efficiency of each topology to determine if achieving 99% efficiency would be possible with each topology. Also, if there were any significant concerns regarding the efficiency of a specific topology, those would be better understood through simulation. To simulate the efficiency, datasheet loss values were used for devices, and the converters were assembled in PLECS. The datasheet information was taken from the Microsemi APTMC60TLM55CT3AG inverter datasheet. This is the module which was selected for the inverter and rectifier stages of the UPS, so it was expected that the DC/DC stage of the UPS would use something similar. The junction temperature of the devices was kept constant using a heatsink directly attached to an ambient temperature of 50 °C. A picture of the simulation setup is shown.
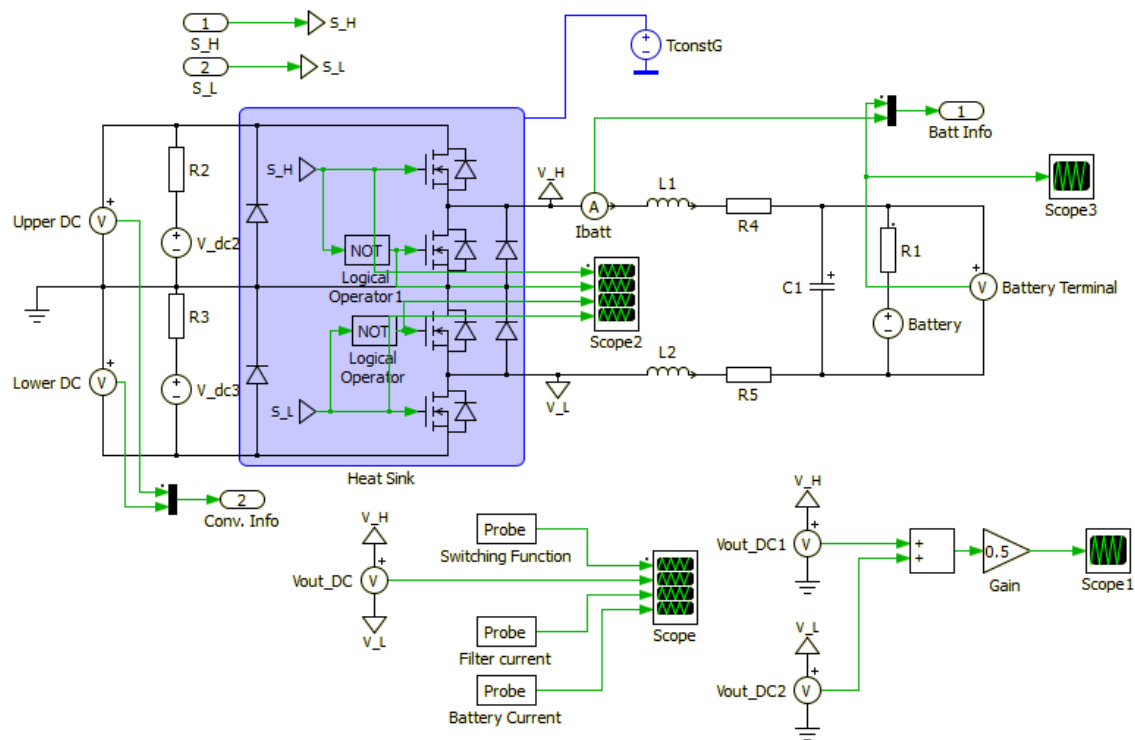
Figure 2.13. Preliminary Efficiency Simulation Configuration

Also seen in this image is the probe setup used to acquire the common-mode

voltage waveforms. Although the image only shows the three-level buck converter, the

setup was nearly identical when other converters were simulated, with the only difference

being the configuration of the devices. In addition to the simulation parameters

mentioned previously, the switching frequency was set at 10 kHz and the converter

power level was set at 20 kW. The loss and efficiency data of each topology is shown in

the following figures and summarized in the table after.
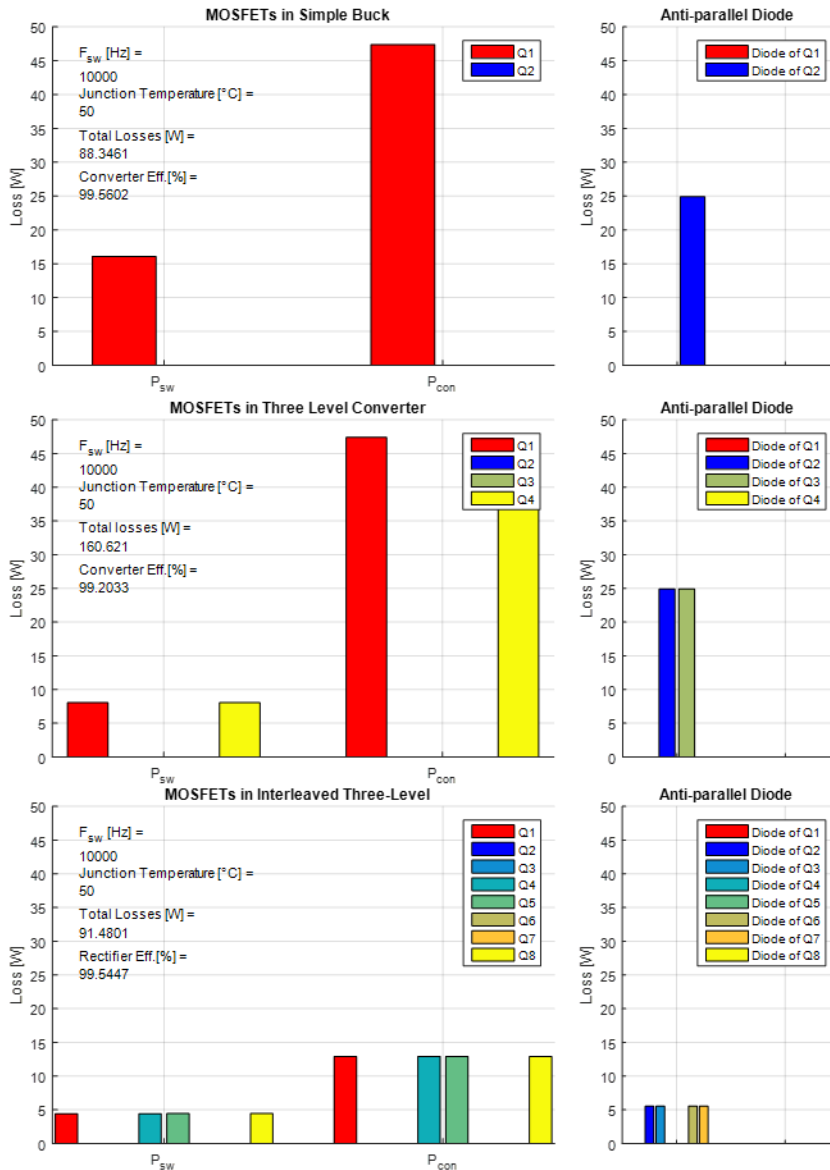
Figure 2.14. Preliminary Efficiency Simulation Results

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Topology	Losses (W)	Efficiency (%)
Simple Buck	88.3	99.56
Three-Level Buck	160.6	99.2
Interleaved Three-Level Buck	91.5	99.54

The simulated results line up well with the expected values. Note that the simulation performed was at a low junction temperature, and that the switching frequency was fairly low. For this reason, the simulated losses are slightly lower than what would be expected in an actual converter made with these devices. The most efficient of the converters simulated is the buck converter. This is due to the significantly lower conduction losses as a result of using only two devices. Also, the interleaved converter has lower losses than the single three-level buck converter as there is less current through the devices to meet the same power rating.

After these comparisons were made, it was determined that the three-level buck converter would be the best topology to investigate further. Based on the loss simulations, it is not necessary to interleave two of these converters to meet the UPS power rating. Also, the three-level buck converter has a significantly better common-mode voltage profile than the simple buck converter while possessing all benefits of the interleaved three-level buck converter.

2.7. UPS Noise Profile Comparison with Three-Terminal Model

Using the three-terminal model discussed in the introduction, the UPS noise

profile can be simulated including the DC/DC stage to determine its effects on the noise

profile of the system. To perform these simulations, a simplified model was used in

PLECS. This simplified model is able to give a good representation of the switching

dynamics of the UPS with less computation time than the complete model. A schematic

of the simplified model is shown.
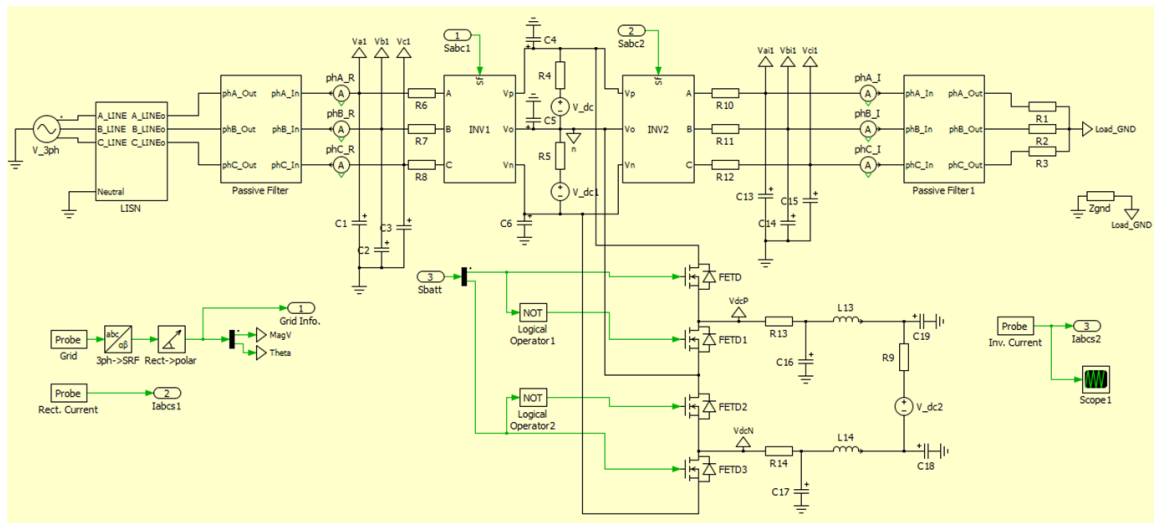
Figure 2.15. UPS EMI Simulation Schematic

The simulation performed using this circuit provides an accurate model of the

complete UPS noise profile including the DC/DC stage. This allowed for simulations to

be performed of the system to evaluate the potential benefit of the proposed topology.

Simulation results of the UPS noise profile are shown which include a basic buck

converter topology, the three-level buck converter operating in synchronous mode, and

the three-level buck converter operating in phase-shifted mode.
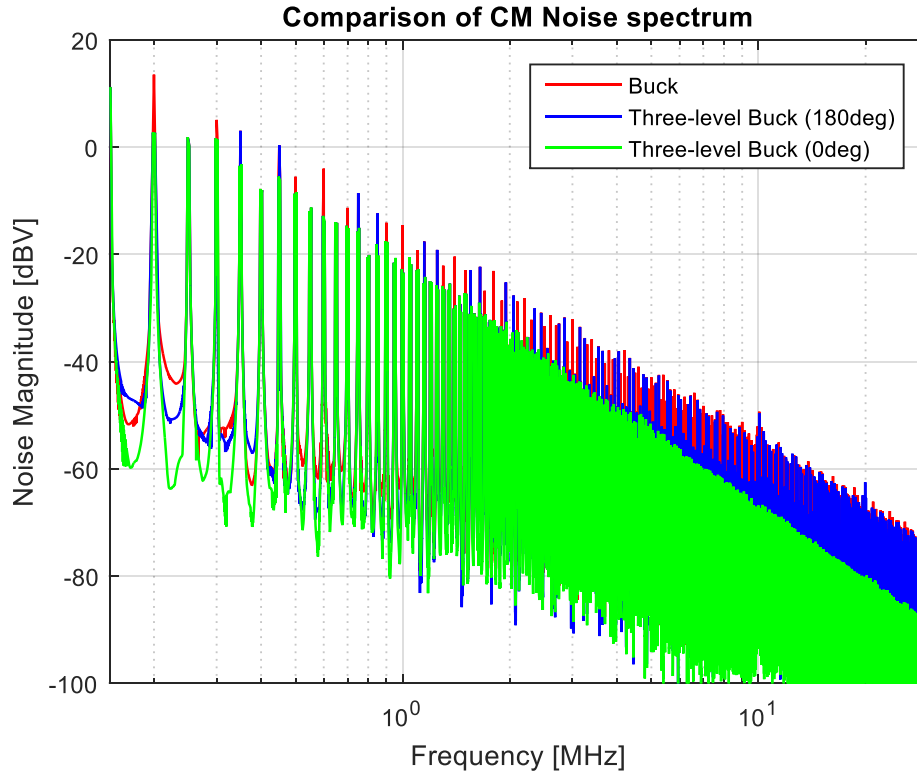
Figure 2.16. UPS Noise Profile Simulation Comparison

These noise profiles are measured at the LISN connected to the UPS AC input.

As such, the waveforms include the inverter and rectifier stage contributions to the

common-mode voltage profile as well as those of the DC/DC stage. As expected, the

buck converter and phase-shifted three-level buck converter have very similar profiles to

the similarities in their common-mode voltage time-domain waveforms. However, the

synchronously operated three-level buck converter provides no additional noise in the

common-mode spectrum of the entire UPS. This allows for a significant drop in the

noise magnitude of the system, which should make it easier to meet IEC standards for

common-mode voltage noise levels.

Chapter 3. Converter Modeling and Simulation

3.1   Converter Average and Small Signal Model

Once the three-level NPC DC/DC converter topology was decided on, it was necessary to develop an average and small signal model to ensure proper control of the converter. The model was developed with the intention of controlling not only the output voltage, but also to control the neutral point voltage imbalance. To this end, all significant parasitic values will be included in the detailed model. During the analysis of the model, these parasitics may be excluded at any step to obtain simplified expressions of the converter's characteristics which are likely still valid for all practical applications.

The derivation of the small signal model of this converter and its control scheme will be discussed in detail. Although this modeling process has been performed successfully by others [14] [15] [16], I have still taken the time to describe my process in more detail. In order to make this model, some assumptions were made about the converter. The first assumption is that the total DC link is held at a constant voltage. In practice, this is typically done by the rectifier stage of the UPS. However, there are certain instances where this may not be the case, such as when the battery is solely supporting the load.
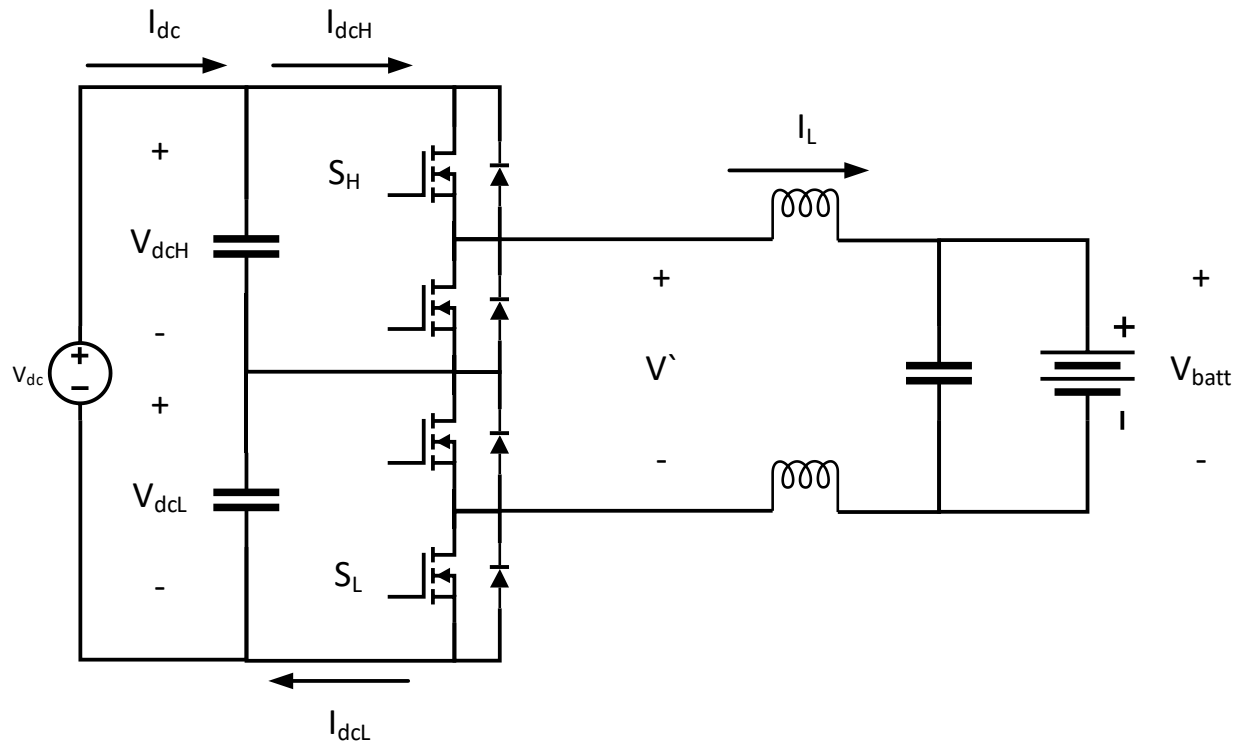
Figure 3.1. Three-Level Buck Converter with Labels

Relate intermediate voltage and currents:

$$I_{dcH} = S_H I_L, \qquad I_{dcL} = S_L I_L, \qquad V' = V_{dcH}S_H + V_{dcL}S_L$$

Redraw circuit with dependent sources:
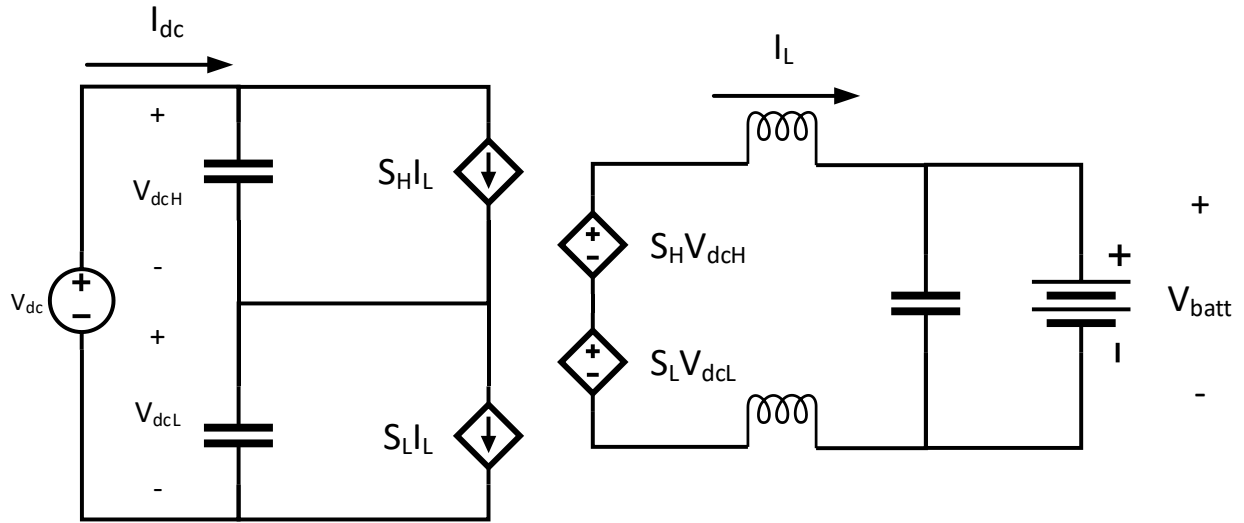
Figure 3.2. Decoupled Three-Level Buck Converter with Switching

After averaging, the switching functions can be replaced with duty cycles:
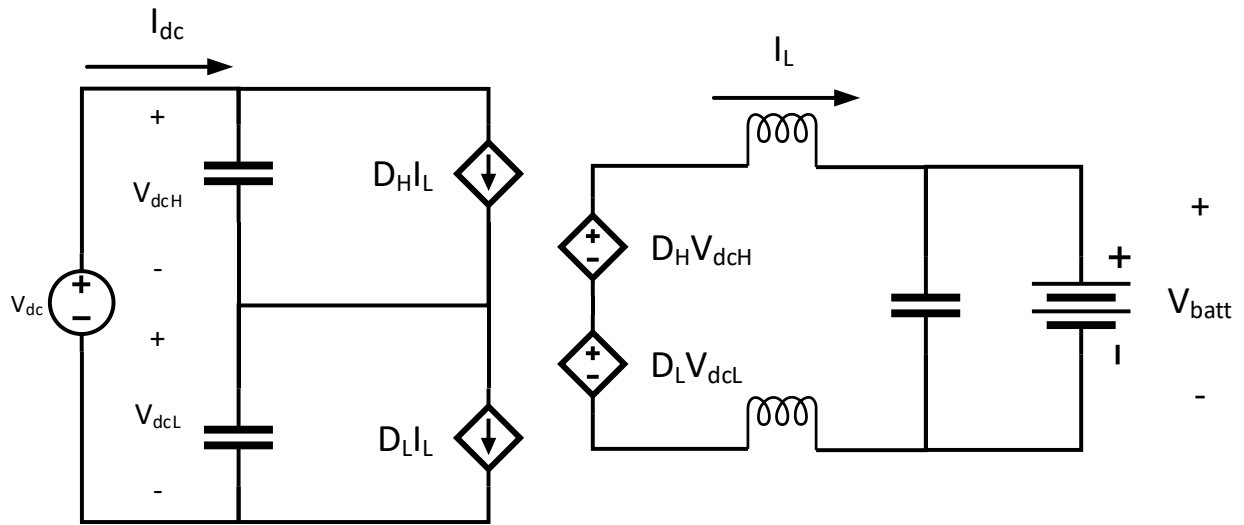
Figure 3.3. Decoupled Three-Level Buck Converter with Duty Cycle

At this point, it is necessary to consider the first part of the circuit separately along with the independent source representing the total DC link voltage balancing provided by the BTB converter:
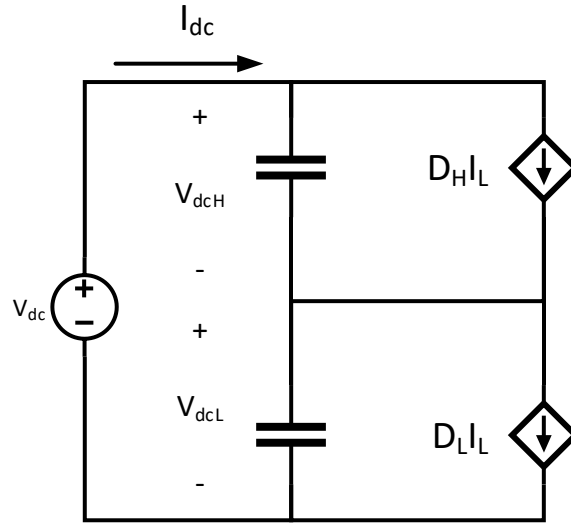
Figure 3.4. DC Bus Decoupled Model

Now, using basic circuit analysis techniques, formulas can be derived to show the change

in the capacitor voltages along with a changing duty cycle. First, some terms will be

defined, then the equations will be derived:

$$\Delta D = D_H - D_L$$

$$D = \frac{D_H + D_L}{2}$$

$$V_{dc} = V_{dcH} + V_{dcL}$$

$$\Delta V_{dc} = 0$$

$$\Delta V_{dcH} + \Delta V_{dcL} = 0$$

At this point, the voltages of the capacitors will be defined in terms of their standard

deltas:

$$\Delta V_{dcH} = \frac{I_{dc}}{C_{dc}} T_{sw} - \frac{D_H I_L}{C_{dc}} T_{sw}$$

$$\Delta V_{dcH} = \frac{I_{dc}}{C_{dc}} T_{sw} - \frac{(D + \frac{1}{2}\Delta D)I_L}{C_{dc}} T_{sw}$$

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$$\Delta V_{dcH} = \frac{I_{dc}}{C_{dc}} T_{sw} - \frac{DI_L}{C_{dc}} T_{sw} - \frac{\Delta DI_L}{2C_{dc}} T_{sw}$$

$$\Delta V_{dcL} = \frac{I_{dc}}{C_{dc}} T_{sw} - \frac{D_L I_L}{C_{dc}} T_{sw}$$

$$\Delta V_{dcL} = \frac{I_{dc}}{C_{dc}} T_{sw} - \frac{(D - \frac{1}{2}\Delta D)I_L}{C_{dc}} T_{sw}$$

$$\Delta V_{dcL} = \frac{I_{dc}}{C_{dc}} T_{sw} - \frac{DI_L}{C_{dc}} T_{sw} + \frac{\Delta DI_L}{2C_{dc}} T_{sw}$$

Next, these equations will be equated to zero. This is done with the goal of eliminating

the passive component from the formulas governing the change of the capacitor voltages.

$$\Delta V_{dcH} + \Delta V_{dcL} = 0$$

$$\frac{I_{dc}}{C_{dc}} T_{sw} - \frac{DI_L}{C_{dc}} T_{sw} - \frac{\Delta DI_L}{2C_{dc}} T_{sw} + \frac{I_{dc}}{C_{dc}} T_{sw} - \frac{DI_L}{C_{dc}} T_{sw} + \frac{\Delta DI_L}{2C_{dc}} T_{sw} = 0$$

$$\frac{2I_{dc}}{C_{dc}} T_{sw} = \frac{2DI_L}{C_{dc}} T_{sw}$$

$$I_{dc} = DI_L$$

$$\Delta V_{dcH} = -\frac{\Delta DI_L}{2C_{dc}} T_{sw}$$

$$\Delta V_{dcL} = \frac{\Delta DI_L}{2C_{dc}} T_{sw}$$

With R$_{Cdc}$:

29
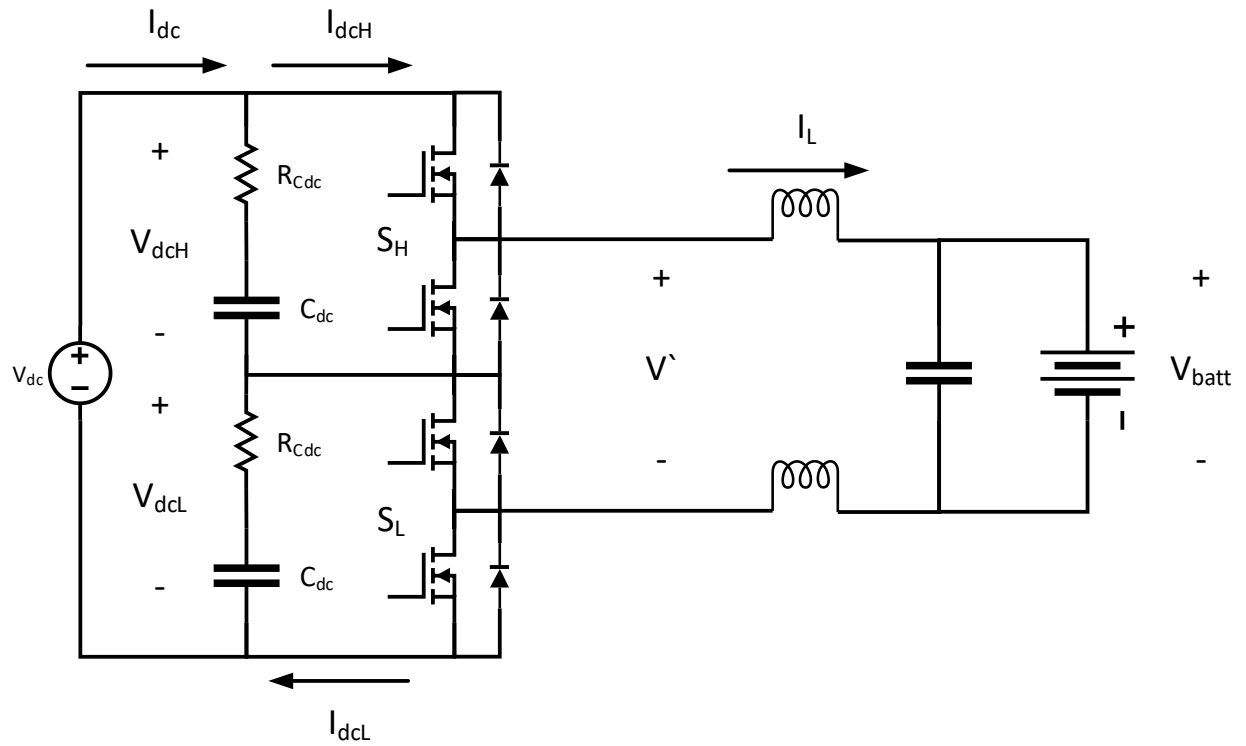
Figure 3.5. Three-Level Buck Converter with Labels and Capacitor ESR

Simplified:
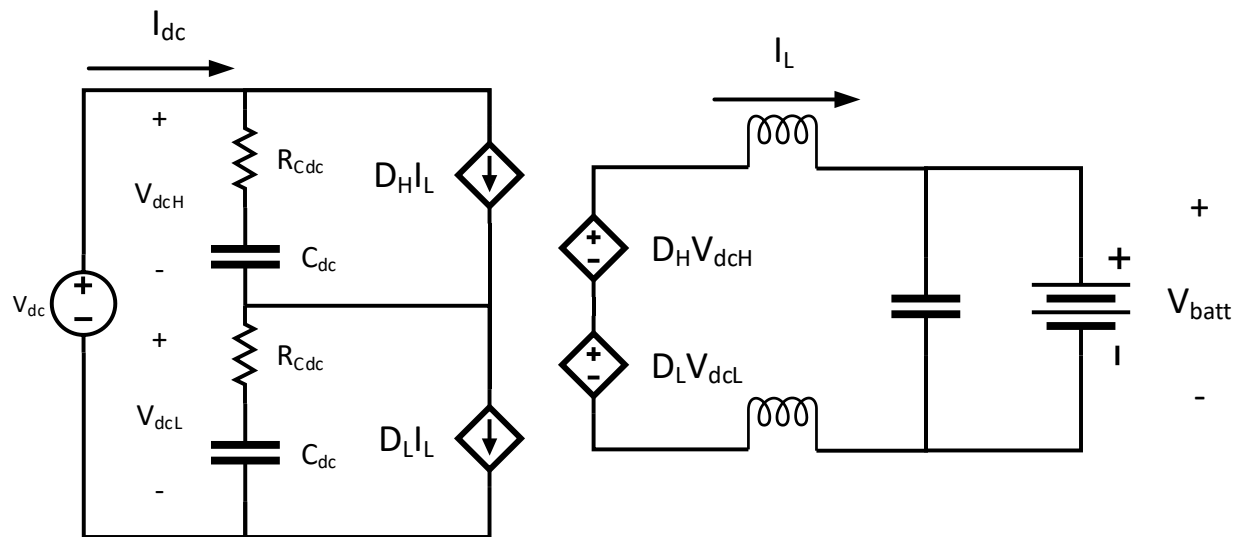
Figure 3.6. Three-Level Buck Average Model with Capacitor ESR

Only DC link side with current sources:

30
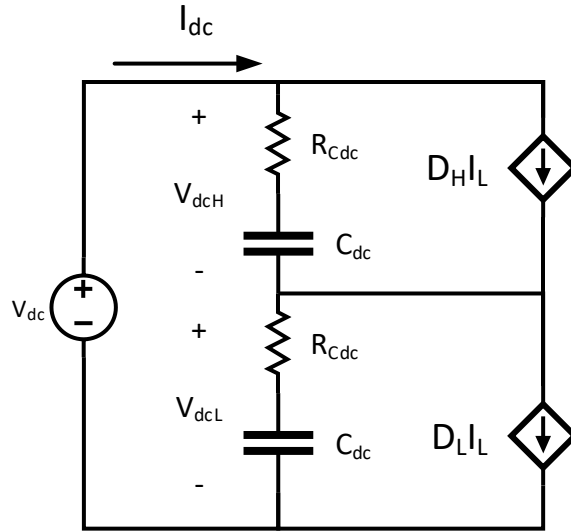
Figure 3.7. Isolated DC Bus with Capacitor ESR

When the sources are perturbed and linearized, the DC components will cancel with each other ($I_{dc} = DI_L$) and only AC terms will be left:
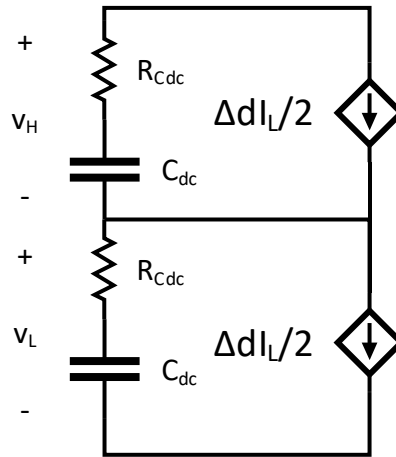
Figure 3.8. Small Signal DC Bus with Capacitor ESR

At this point, a simple calculation will yield a transfer function which relates v_H to Δd:

$$v_H = -\frac{\Delta d}{2} I_L \left(R_{Cdc} + \frac{1}{sC_{dc}} \right)$$

$$\frac{v_H}{\Delta d} = -\frac{I_L}{2}\frac{1 + sR_{Cdc}C_{dc}}{sC_{dc}}$$

When this transfer function is combined with the transfer function of a PI controller, an

effective DC link controller can be designed by determining denominator values:

$$PI = \frac{K_p s + K_i}{s}$$

$$\frac{(PI)(Plant)}{1 + (PI)(Plant)} = \frac{s^2\dfrac{K_p R_{Cdc}C_{dc}}{K_p R_{Cdc}C_{dc} - \dfrac{2C_{dc}}{I_L}} + s\dfrac{K_p + K_i R_{Cdc}C_{dc}}{K_p R_{Cdc}C_{dc} - \dfrac{2C_{dc}}{I_L}} + \dfrac{K_i}{K_p R_{Cdc}C_{dc} - \dfrac{2C_{dc}}{I_L}}}{s^2 + s\dfrac{K_p + K_i R_{Cdc}C_{dc}}{K_p R_{Cdc}C_{dc} - \dfrac{2C_{dc}}{I_L}} + \sqrt{\dfrac{K_i}{K_p R_{Cdc}C_{dc} - \dfrac{2C_{dc}}{I_L}}}^{\,2}}$$

The following equations can then be formed:

$$\omega_n = \sqrt{\frac{K_i}{K_p R_{Cdc}C_{dc} - \dfrac{2C_{dc}}{I_L}}}, \qquad \zeta = \frac{K_p + K_i R_{Cdc}C_{dc}}{2\left(K_p R_{Cdc}C_{dc} - \dfrac{2C_{dc}}{I_L}\right)}\left(\frac{K_i}{K_p R_{Cdc}C_{dc} - \dfrac{2C_{dc}}{I_L}}\right)^{-\frac{1}{2}}$$

If the ideal case is considered ($R_{Cdc} = 0$), these can be simplified further:

$$\omega_n = \sqrt{-\frac{I_L K_i}{2C_{dc}}}, \qquad \zeta = \left(-\frac{I_L K_p}{4C_{dc}}\right)\left(-\frac{I_L K_i}{2C_{dc}}\right)^{-\frac{1}{2}}$$

3.2. Model Verification with Simulation

Now that equations have been derived which may be used to control the DC link

neutral point voltage, another simulation was performed to verify both the average model

and the control scheme developed. This simulation was again performed using PLECS.

First, in order to test that the average model is valid, the complete switching model was

made in PLECS alongside the average model.

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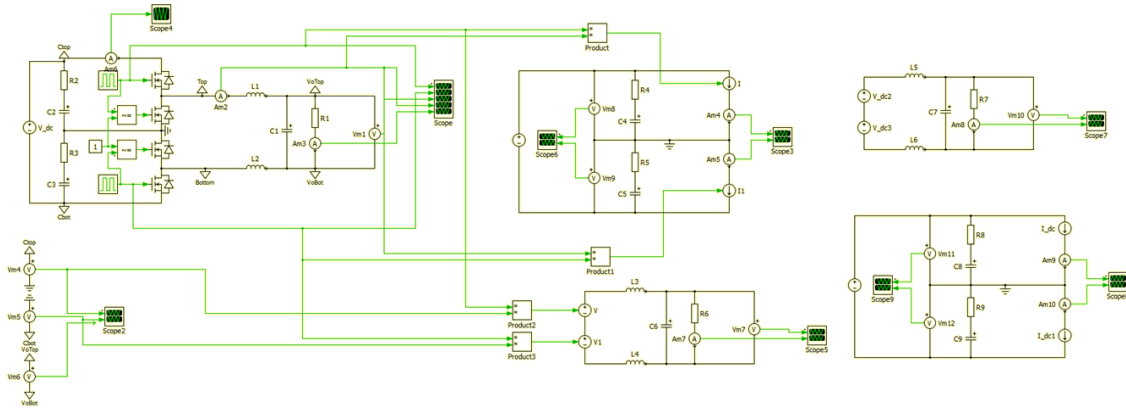
Figure 3.9. Average Model Verification Simulation Schematic

The duty cycles of the two complementary pairs were set to slightly different values so that the power would be transferred to the battery asymmetrically from the DC link. This caused a deviation to occur between the two DC link voltages. This deviation was shown to be identical between the average model and switching model, demonstrating the validity of the average model.
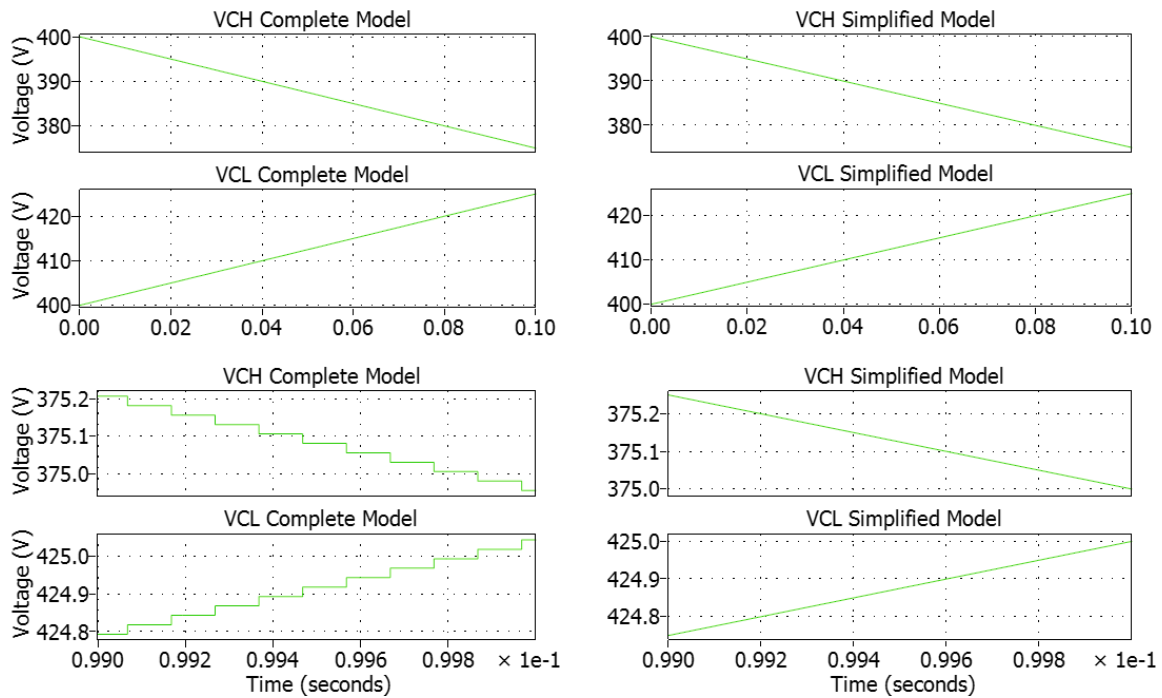
Figure 3.10. Average Model Verification Simulation Waveforms

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The previous figure shows the matching voltages of the DC link capacitors over the course of the simulation. The complete model waveforms on the left side are waveforms of the model which includes the ideal switching dynamics of the system. The simplified model on the right shows the corresponding behavior of the average model. It is shown that over the same time periods, the complete and average model behave identically. Next, a controller was made and added to the simulation based on the PI controller formulas developed previously. In order to verify the operation of this controller, the DC link capacitors were initialized at 500 V and 300 V for the upper and lower DC link, respectively. The PI controller was to then balance these capacitors so they equalize to the same voltage.
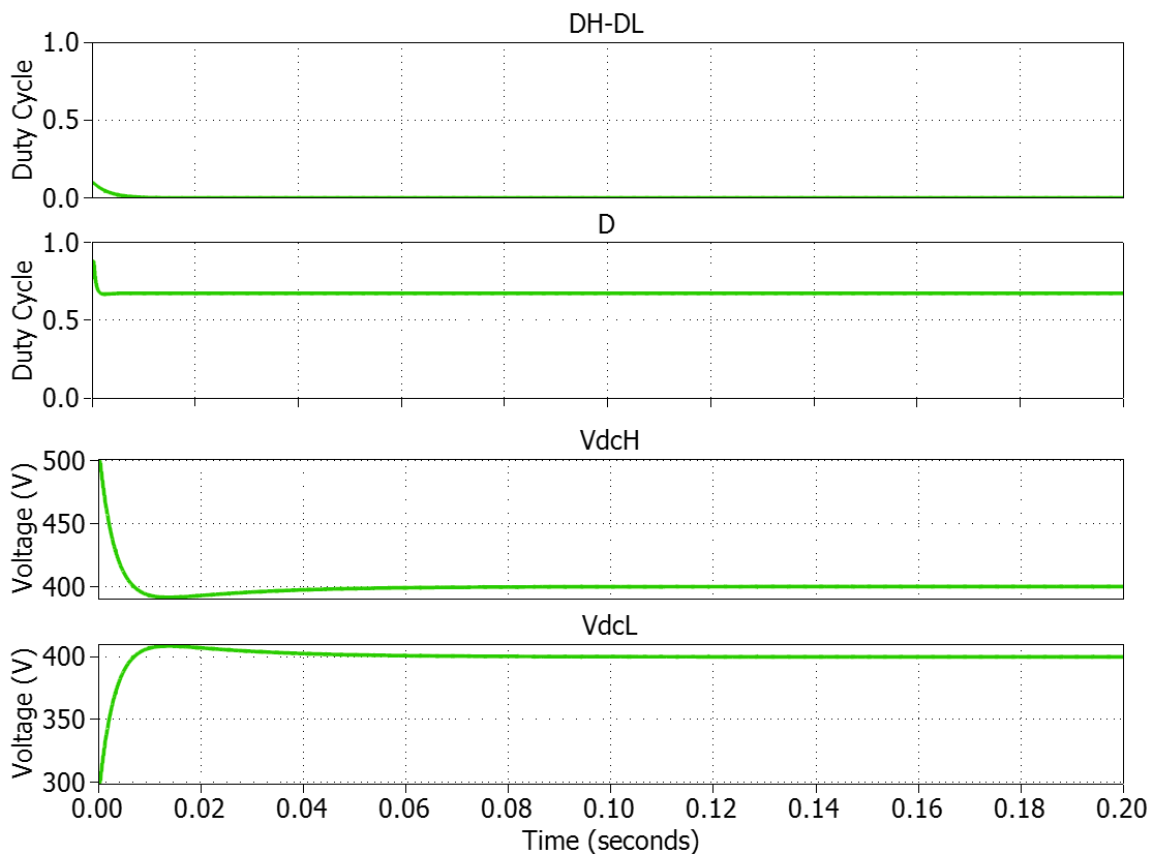
Figure 3.11. Average Model Waveforms with PI Controller

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In the previous figure, four different variables are shown with time. The first variable is the difference between the two duty cycles of the upper and lower pair of devices. When the converter first begins to operate, the upper DC link voltage is much higher than the lower DC link voltage. Because of this, the duty cycle of the upper two switches is increased compared to the lower two switches. This allows power to be transferred asymmetrically to the battery. Because more current flows to the battery from the upper capacitor, its voltage is reduced in comparison to the lower capacitor, thus balancing the DC link.

The second waveform is the overall duty cycle of the converter. This is the value from which the difference between the duty cycles is applied to achieve balancing. Initially this value is higher because power is mostly being transferred from only half of the DC link. This value evens out after balancing to a constant which represents the ratio between the DC link voltage and battery voltage. Finally, the last waveforms show the DC link capacitor voltages. The initial offset is quickly corrected and the converter reaches steady state with identical capacitor voltages for the upper and lower DC link. This shows that the controller functions as intended.

There is, however, a drawback to this voltage balancing method. In order to transfer power asymmetrically, a slight phase shift is necessary between the two pairs of switches. Recalling the simulations of chapter 2, this process introduces a small common-mode voltage pulse. When the common-mode voltage profile of the converter is monitored while the balancing occurs, these pulses can be seen.
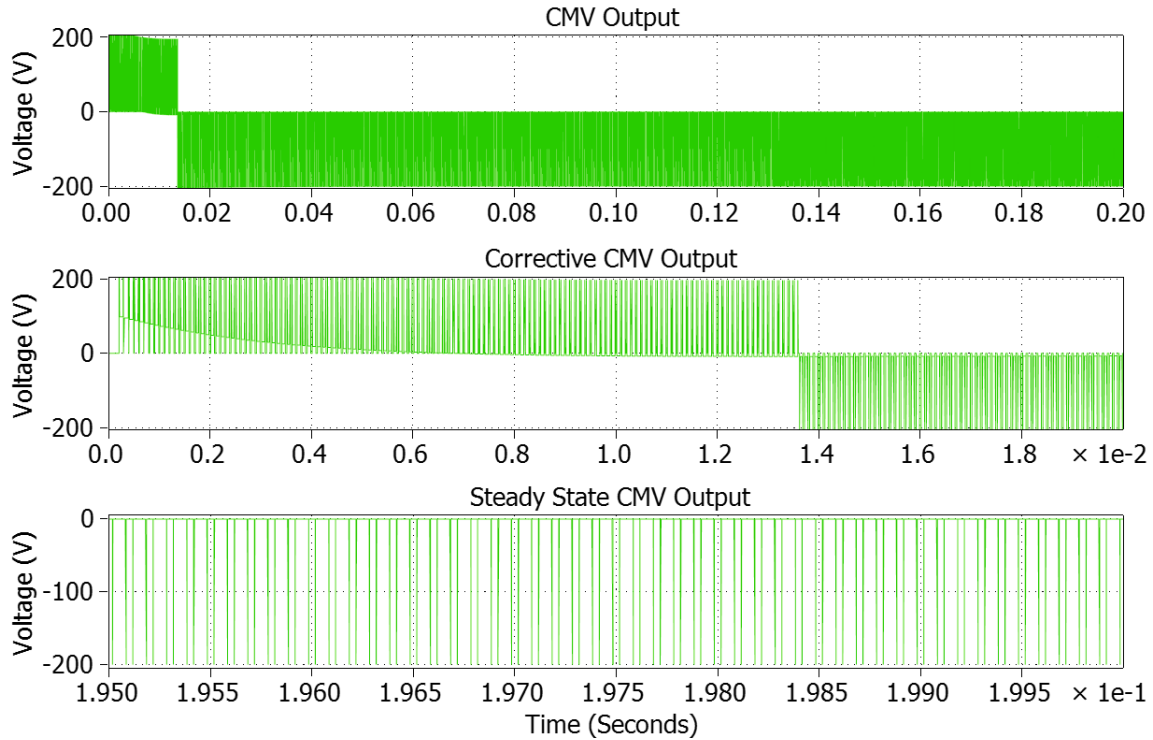
Figure 3.12. Average Model Common-Mode Voltage with PI Controller

The common-mode voltage pulses seen in this figure are actually quite small. The first waveform shows the pulses over the entire simulation. The second waveform shows the pulses during the start of the simulation where the corrective action of the controller is the largest. As the DC link voltages near steady state, the pulses become very short in duration as shown in the last waveform.

Another important note is that all simulations to this point have been performed using ideal devices. Therefore, the effects of dead time and device parasitics are not considered in the simulation results. In hardware implementations and detailed models, it would be seen that the dead time of the converter would have some effect on the output noise configuration [17] as the perfect symmetry of the switching will no longer be

achieved, and the asymmetrical switching states may have their EMI pulses worsened by the dead time of the converter.

Chapter 4. Hardware Design and Construction

4.1. Loss Extraction and Double Pulse Tests

After the modeling and preliminary simulation of the converter was completed, the next step was to perform analysis of the hardware to design the actual converter to be used with the UPS. The first step in the design process was to get an accurate measurement of the expected losses of the devices in the APTMC60TLM55CT3AG module. The device datasheet contained switching and conduction loss information, but there were doubts as to the accuracy of this information. For example, it was believed that the switching losses of the module would be much less than the datasheet value as the testing configuration to determine the datasheet losses included a very large gate resistor. The gate driver designed by a fellow CPES student for this module had a much lower gate resistance of 30 mΩ. This resistance is very low as there is already an internal gate resistance of 1.8 Ω within the module.

Figure 4.1. Double Pulse Test PCB Setup

A PCB was designed and constructed which would allow the testing of the bottommost switch. In order to perform this test, only the lower DC link capacitor was installed. Also, a current shunt probe was added between the bottommost switch and the negative DC bus. This allowed for a very accurate reading of the current through said switch, which would be monitored for loss calculations. A schematic showing the double pulse test setup is shown.

Figure 4.2. Double Pulse Test Circuit Configuration

Once the test setup was assembled, double pulse tests were performed at rated voltage (400 V DC input for the lower capacitor) and various current levels. The voltage and current information of the device under test was saved for each case so that switching losses could be determined at any operating condition. The waveform captured of the double pulse test at the rated current of the device is shown.
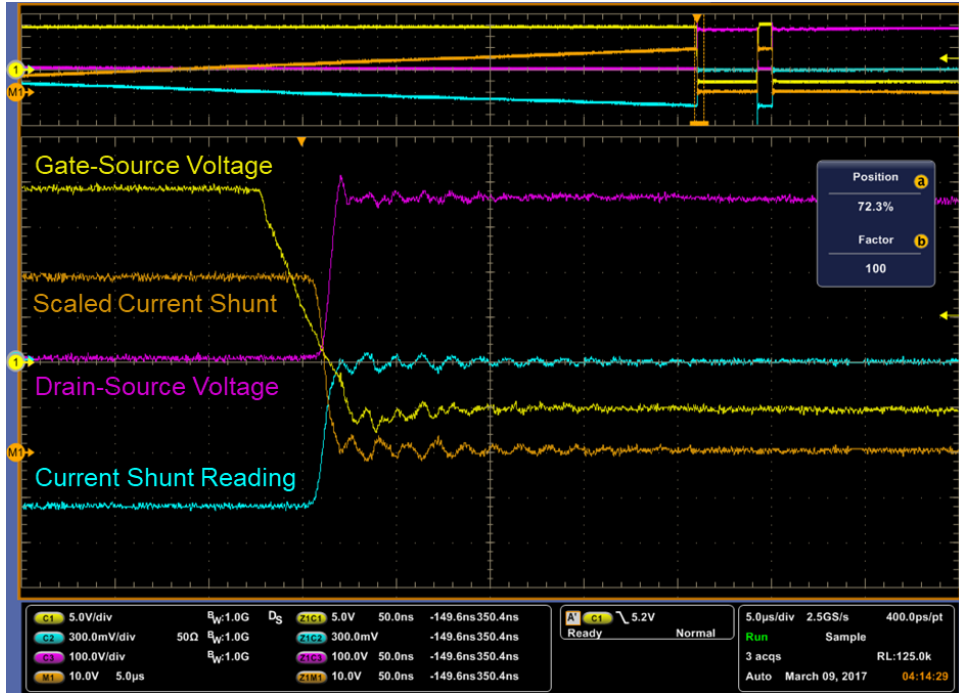
Figure 4.3. Turn Off Waveform at 400 V 40 A
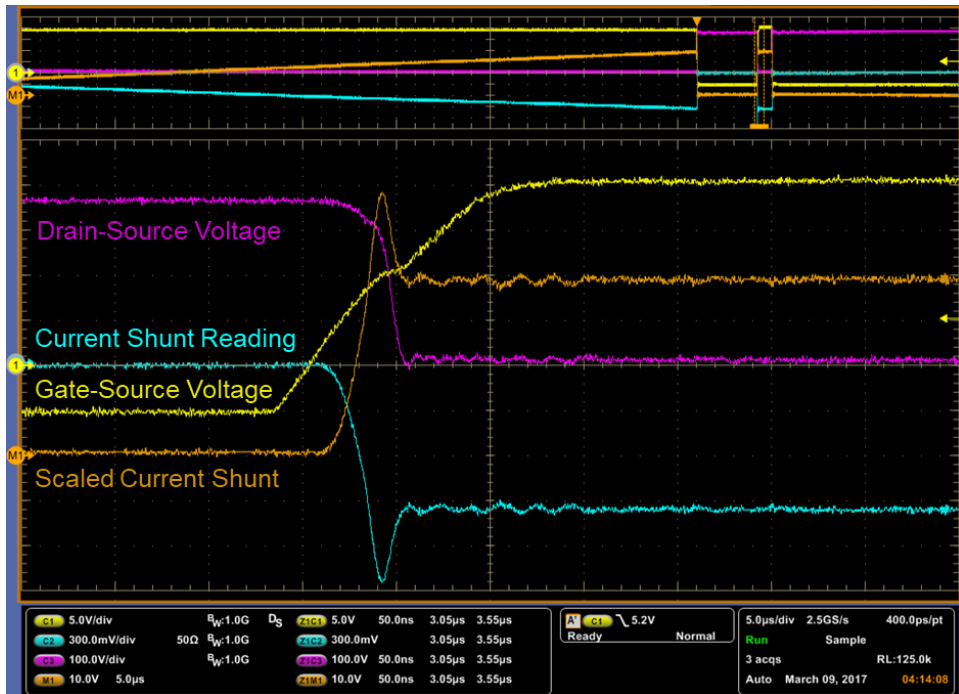
Figure 4.4. Turn On Waveform at 400 V 40 A

Waveforms like the ones shown above were captured for currents up to 60 A. The oscilloscope data was also saved in MATLAB format for analysis. In order to accurately calculate the losses of the device at each current level, the data was imported into MATLAB using PLECS so the instantaneous power at any given point in the captured waveform could be calculated. This power was then integrated to yield switching energy results. By identifying the beginning and end of each switching transition, the switching energy of the device at turn off or turn on could be measured. The process for determining the beginning and end of the switching sequence was to monitor when the drain-source voltage reached 90 % and 10 % of its initial or final values depending on whether the device was turning on or off. The difference in energy dissipated in the device at these two times was determined to be the switching loss.

Vds,Q4 & Ids,Q4

400
200
0

× 1e4
Ploss
1.5
1.0
0.5
0.0

[W]

Eloss
13.3
13.2
13.1

[mJ]

3.9265   3.9270   3.9275   3.9280   3.9285   3.9290   3.9295   3.9300   × 1e-5

Name	Cursor 1	Cursor 2
Time	3.9268e-05	3.93024e-05
Vds,Q4 & I...		
Signal:1	360.859	31.1442
Signal:2	3.42908	40.6627
Ploss		
Eloss		
Signal	13.0967	13.3935

Data
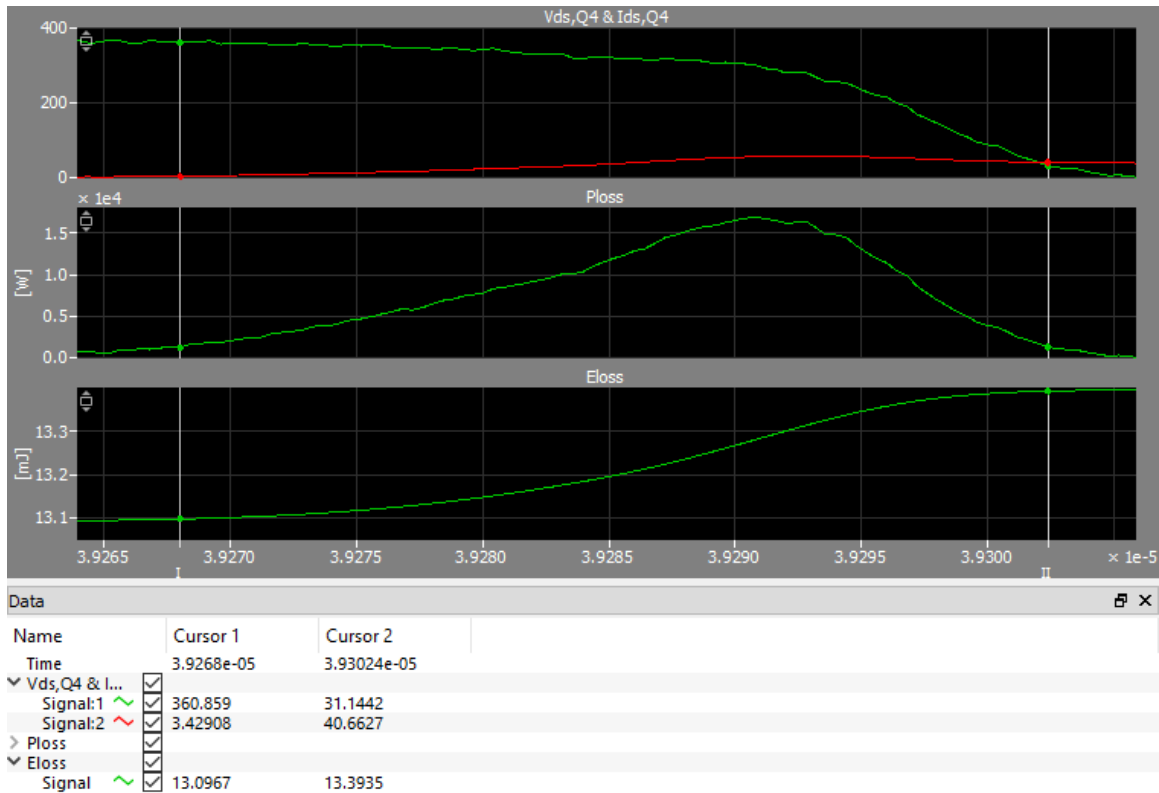
Figure 4.5. Turn On Switching Loss Calculation Example

The waveform shown in figure is an example of the switching loss calculation for the turn on case at rated conditions. The vertical bars were placed at the points where the drain-source voltage reached 90% of its initial value and 10% of its final value. These time stamps were then used as the initial and final energy levels from which the total switching loss is determined by taking the difference between the values. This process was performed for both turn on and turn off losses over a wide current range, and the results of these loss calculations were tabulated. A graph showing the losses over the tested range is shown below.
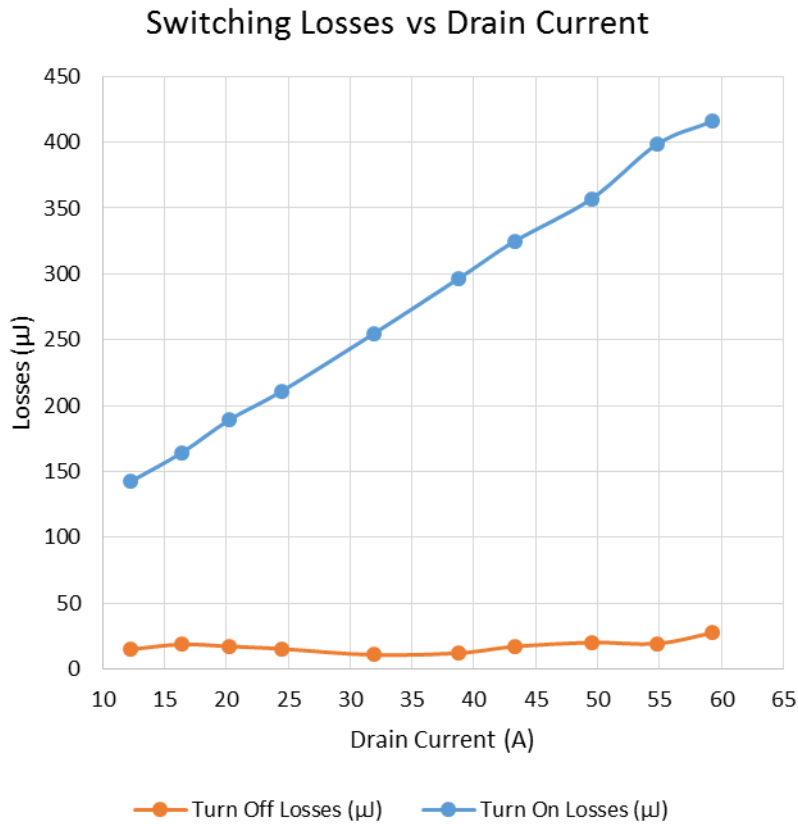
Figure 4.6. APTMC60TLM55CT3AG Measured Switching Loss Data

The data seemed to align well with expectations. The turn on losses of the device increase linearly with the drain current, and are much higher than the turn off losses, which remain at a nearly constant value regardless of the drain current. These characteristics are typical of wide-bandgap devices. Also, the losses are significantly less than those reported in the module datasheet. This is due to the much smaller gate resistor used in this testing.
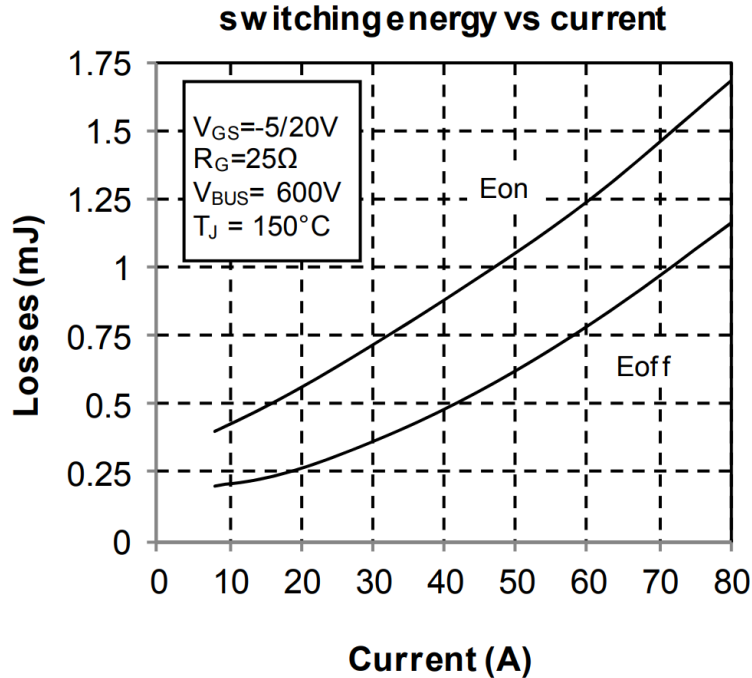
Figure 4.7. APTMC60TLM55CT3AG Datasheet Switching Loss

It can be seen that the measured losses are less than half of the datasheet values due to the change in gate resistance. Accurate switching losses for the UPS system are necessary to design other components.

4.2. Updated Simulation with Extracted Losses

Once the losses were extracted from the device, the next step in the design process was to use these extracted losses in a simulation to size necessary components of the converter. In order to perform an accurate simulation, a number of steps were taken. The first step was to decide on a cooling solution for the converter. A heatsink was selected based on dimensions for a single Microsemi module as well as three modules adjacent to one another (as the setup for the inverter and rectifier stages would be). The heatsink selected was a standard aluminum heatsink upon which two fans would be mounted for enhanced air flow. Based on the physical dimensions of the heatsink as well

as the LFM rating of the two heatsink fans, a thermal impedance could be calculated for

the heatsink. This thermal impedance was used, in conjunction with the device-to-case

thermal properties of the module to set up a thermal circuit within PLECS.
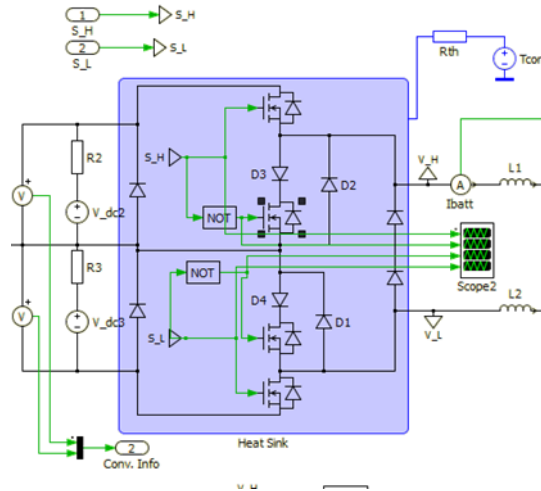
Figure 4.8. PLECS Thermal Circuit

Figure 4.8 shows the extracted switching loss data for the devices after being

placed in a PLECS thermal library. The circuit schematic shown on the right is the

simulation setup with thermal circuitry. This setup allowed the simulation to be

performed at a variety of switching frequencies and power levels to determine the

optimal operating point for the converter while maintaining 99 % efficiency. Initially,

based on simulation results, the converter was set to operate at 40 kHz with a power

rating of 16 kW. This resulted in nearly 99% efficiency when passive losses were

estimated. A distribution of the simulated losses is shown below.
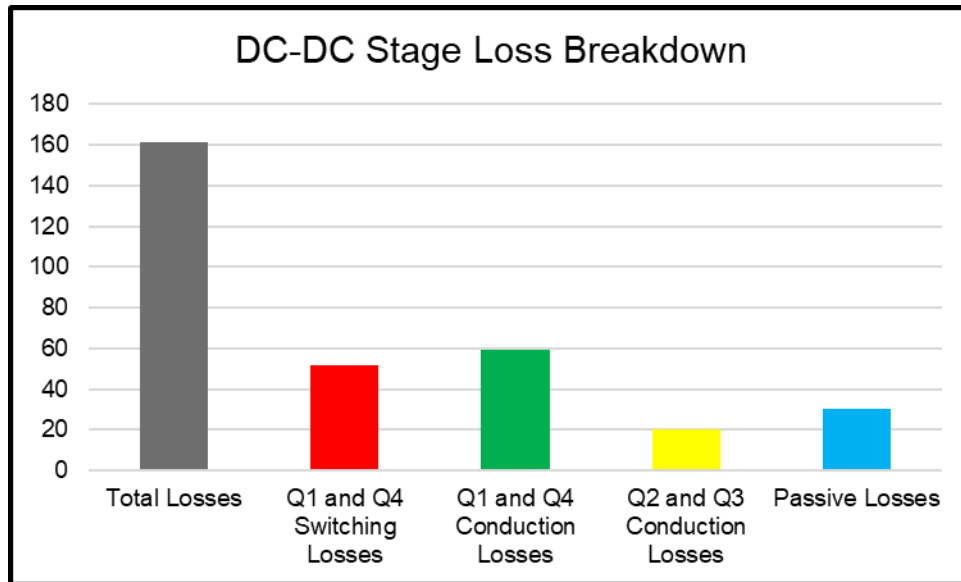
Figure 4.9. Simulated Loss Distribution

As expected based on previous simulations, the conduction losses tend to

dominate the losses within the converter. Although the switching frequency is much

higher than the preliminary simulations, due to the lower extracted switching losses, the

distribution of losses still lines up with expectations. Also, the passive losses were

assumed to be 30 W. This value was selected to ensure that the converter would not be

designed for an efficiency it would never be able to attain. This simulation was also used

to size the output filter components. These components were determined based on the

converter switching frequency and a battery voltage ripple constraint. The inductor was

determined to have a value of 220 µF and the capacitor would have a value of 40 µF.

4.3.   Hardware Assembly

Once all auxiliary components had been decided upon, the hardware was

assembled. The busbar used for the converter was a laminated busbar [18] [19] [20] [21]

embedded in a PCB. This busbar shared connections with the inverter and rectifier stages

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of the UPS. The layout of the busbar was made as similar to the double pulse test board

as possible. The busbar was constructed using 2 oz. copper pours for each layer with a

uniform dielectric thickness between said layers. The top layer of the board was used as

a shielding layer to insulate the devices from any radiated noise from the gate driver

components. The busbar had multiple ceramic decoupling capacitors near each module

as well as small film decoupling capacitors near each module. The DC link was mainly

supported by two large film capacitors.
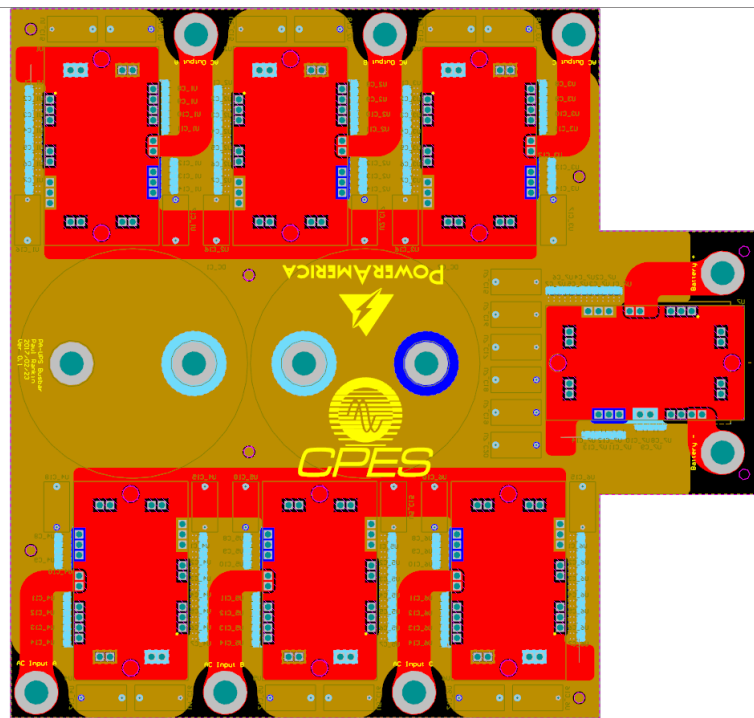
Figure 4.10. UPS Busbar PCB Layout

A diagram showing the layout of the board is shown. The red layer represents the

shielding layer, which would later be connected electrically to the DC neutral midpoint.

The gold layer is the positive DC pour, the light blue layer is the DC neutral pour, and the

blue layer is the negative DC pour. The single module on the right side of the board is

the DC/DC converter stage. It can be seen that due to the unique connections of this

module with respect to the inverter and rectifier, that there are two output ports from this module. These are the positive and negative outputs for the battery filter components.
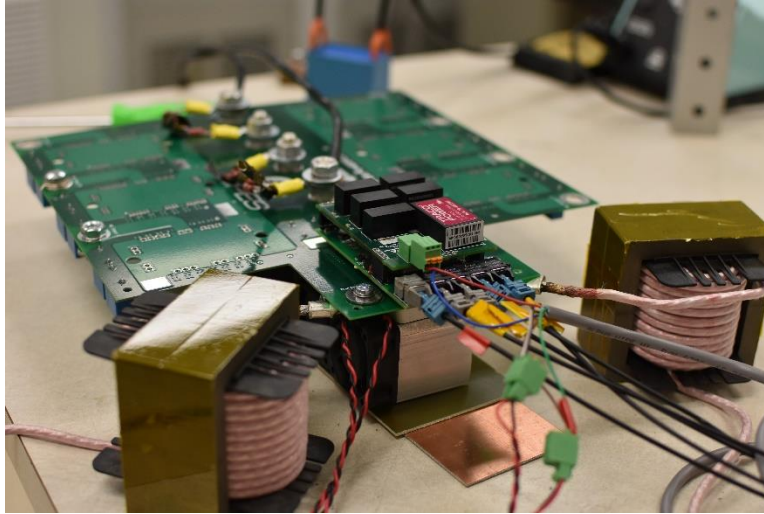
Figure 4.11. Hardware Assembled on Busbar

In order to do preliminary continuous testing, the DC/DC stage was assembled on the busbar prior to the complete assembly of the UPS. This is shown in figure 4.11. Seen are the two output current ripple inductors, sized according to calculations and simulation results [22] [23], the gate driver with fiber optic cables attached on top of the busbar, the module just beneath the PCB, and the heatsink with fans mounted onto the module. After the module was tested for open loop and some closed loop operation, the rest of the UPS was assembled along with this converter. The complete system is shown below.
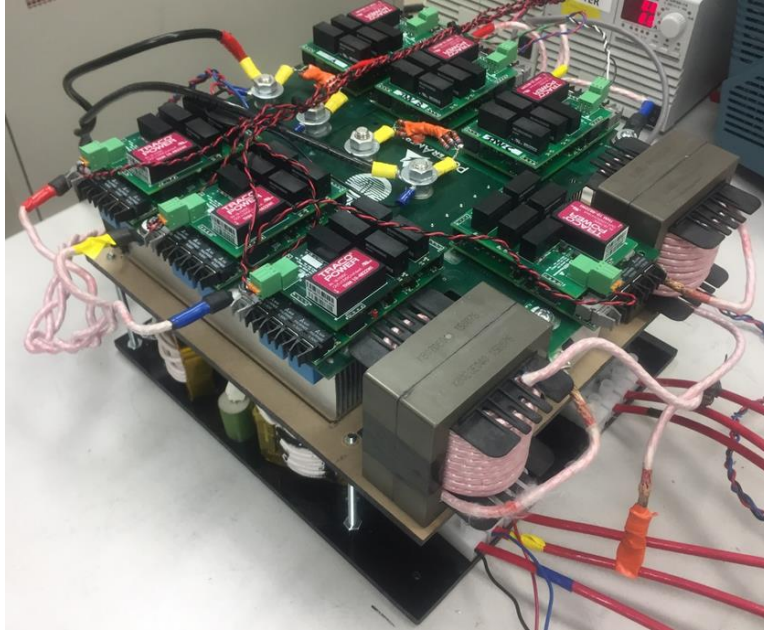
Figure 4.12. Complete UPS Assembly

Chapter 5. Experimental Results

5.1. DC/DC Open Loop Testing and Efficiency Measurement

After the converter was set up as shown in figure 4.11, a number of different open loop tests were performed. First, the converter was verified to operate at full power. This is the 20 kW rating shared by the inverter and rectifier stages of the UPS. In order to do this, 800 V was applied to the DC bus split equally between the DC link capacitors using voltage dividing resistors. The duty cycle was then set to a constant value so the output voltage of the converter would remain constant using a resistive load to simulate a battery. Also, after some testing, it was determined that the converter could operate without issue at 60 kHz, despite the design target of 40 kHz. This allowed the DC/DC stage to operate at the same frequency as the inverter and rectifier stages, which

simplifies the control of the UPS as a whole. The result of this test is shown in the following waveform.
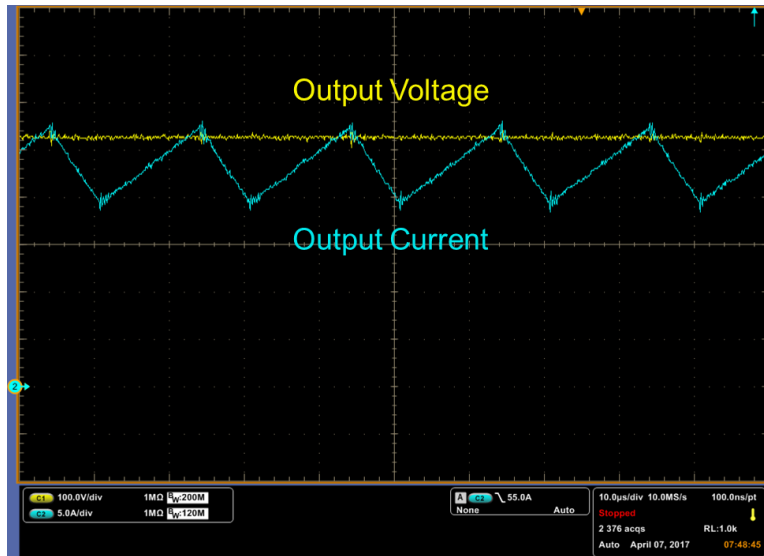
Figure 5.1. Open Loop Output Waveform

The converter operated successfully without any major issues. However, there was a problem identified at the output of the converter. There was a ringing present at the switching instances on the output voltage waveform. This was an issue as the output voltage typically has very strict ripple requirements for use with a battery [24] [25]. It was determined that this ringing was due to the interaction of parasitics within the converter during dead time. To mitigate the ringing, the dead time was reduced from 200 ns to 100 ns, and an additional filter capacitor was added at the resistor load. The resulting waveform is shown.
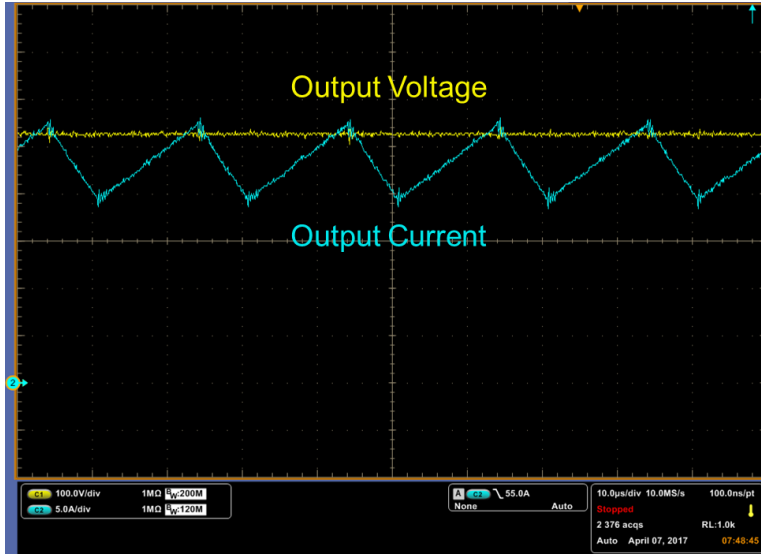
Figure 5.2. Revised Open Loop Output Waveform

Although the difference between the two waveforms is not immediately clear, a comparison of the ringing instances highlights the details effectively.
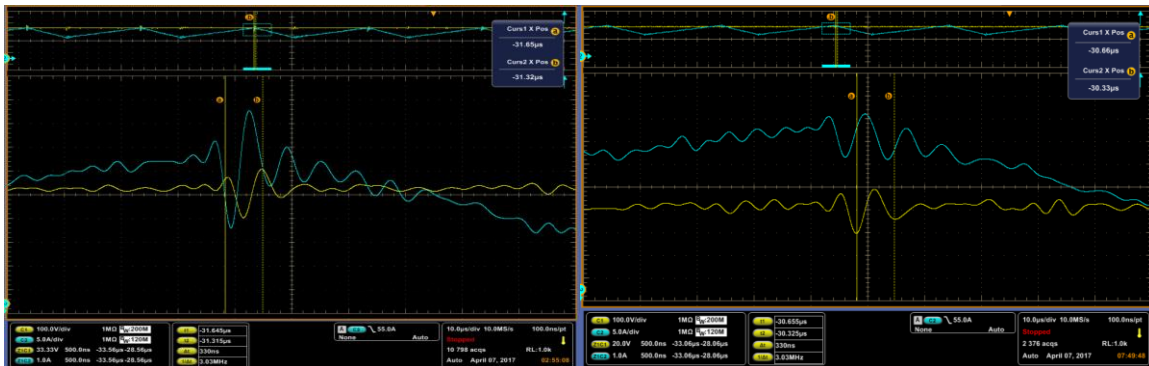
Figure 5.3. Dead Time Ringing Comparison

In the figure, the waveform on the left is the ringing at the output voltage with only one output filter capacitor and 200 ns dead time. The waveform on the right is after the dead time adjustment and filter capacitor addition. Although the exact cause of the ringing remains unknown, it is believed to be due to some interaction of the device miller capacitance and other parasitic components in the test setup.

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Once the converter was verified to operate at the rated power of 20 kW, the converter was set to run for an extended period in order for the module to reach thermal equilibrium to test the cooling of the heat sink. Although the internal junction temperature of the modules was not able to be monitored directly, a thermal camera was used to take readings of the module case temperature and adjacent components.
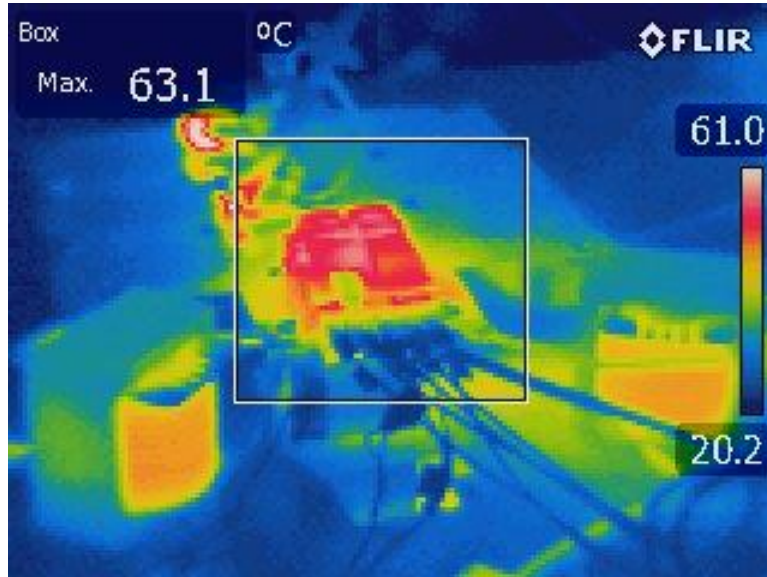
Figure 5.4. Thermal Image of Continuous Operation

The thermal camera image shown above is one example of the readings taken while the converter was in thermal steady state. The highest temperature read by the camera during this operation was 65.8 °C. This is slightly less than the simulated temperature, but is likely less than the actual junction temperature of the module. Ultimately, the temperature measured was close to the simulated temperatures, so the loss extraction and simulation method used for determining heat sink sizing appears to work quite well.

Once the converter was verified to work throughout the necessary power range,

efficiency measurements were taken using a power analyzer. This power analyzer

functions by taking readings of the input voltage and current as well as the output voltage

and current. The efficiency is then calculated including losses of the power stage of the

converter and output filter dynamics. One issue with this method of testing is that the

cables used to measure input and output current were not able to handle the current

passed through the converter. They began to smoke and the tests had to be stopped prior

to reaching the maximum rated power of the converter. However, readings were taken

over a wide range of powers by maintaining a constant DC bus voltage and increasing the

output current. The result of those readings are shown.

Figure 5.5. Measured Efficiency Curve of Converter

The graph above shows that the converter operates with a very high efficiency. It
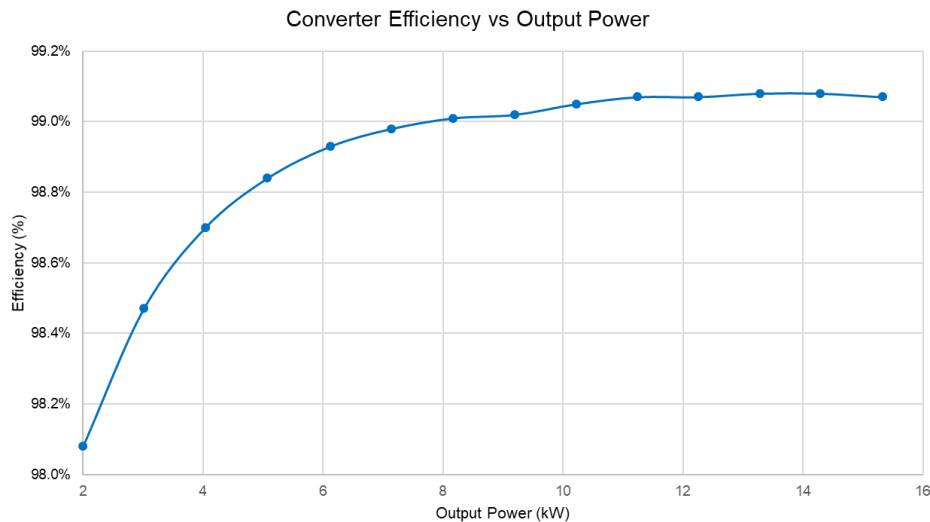
operates in excess of the target efficiency of 99% over the majority of the power range,

and never drops below 98% efficiency. After taking a reading at a power slightly higher

than 15 kW, the next readings were not able to be taken due to the cable issues mentioned previously.

5.2.   DC/DC Closed Loop Testing

After the converter was verified to operate in open loop with no issues, a control loop was implemented which would allow for the control of the output current and DC link balancing. To do this, the controller which would be used with the UPS was assembled. This controller was able to sense the DC link voltages as well as the DC output current. A PI controller was implemented in DSP based on the controller measurements. A slight DC link imbalance was added to the bus to verify the balancing ability of the converter. The converter was operated first in open loop in buck mode, then had the current loop closed to ensure constant power operation, then the DC link balancing loop was closed to resolve the mismatch between capacitor voltage.

The converter was operated at low power with a 200 V DC bus. Also, an additional restriction was added to the controller to limit the duty cycle variation of the converter. The difference between the two duty cycles of the switching pairs was limited to 0.1. This ensured there would not be any short-circuit problems or loop instability issues which may damage the hardware. A screenshot of the oscilloscope measurements of the converter properties before and after the control loops were closed is shown.
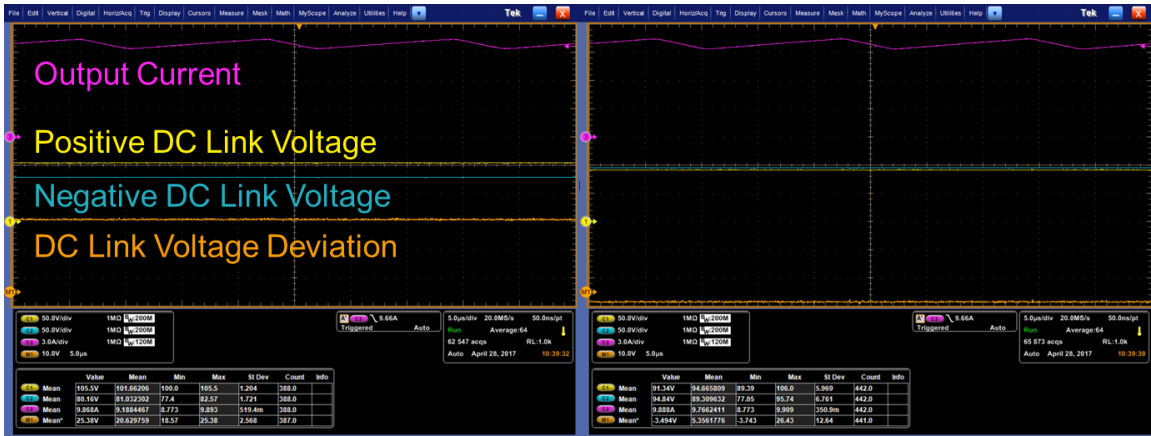
Figure 5.6. Closed Loop Neutral Point Balancing Verification

The figure above shows the two DC link voltages, the output current of the converter, and the difference between the DC link voltages. The difference between the DC link voltages initially is approximately 25 V, but after the voltage loop is close, this difference is reduced to 3.5 V. Although this may not seem like the converter is matching the voltages very closely, it should be noted that this is only due to the discrepancy between the controller voltage sensor readings and the oscilloscope probe readings. When the voltage loop is closed, the difference between the two DC link voltages according to the controller is reduced to a value of effectively zero. This demonstrates that according to the information provided to the controller, the converter is able to quickly and accurately reduce the DC link imbalance to zero.

The DC link balancing was also performed in a similar fashion for operation in boost mode. The controller values all remained the same, but the sign of the PI gain was reversed due to the change in current direction for boost mode operation. This test was also performed with the inverter stage running as a load. To perform this test, the DC/DC converter was connected to a DC power supply, and a resistive load was connected in a

three-phase configuration to the inverter output. The system was operated in open loop with no DC link support from the rectifier stage. The DC/DC converter voltage balancing loop was then closed after the converter reached steady state. The system was only run with the DC bus voltage at 400 V rather than at full power. The waveforms of the DC link voltages and phase A inverter output current are shown.
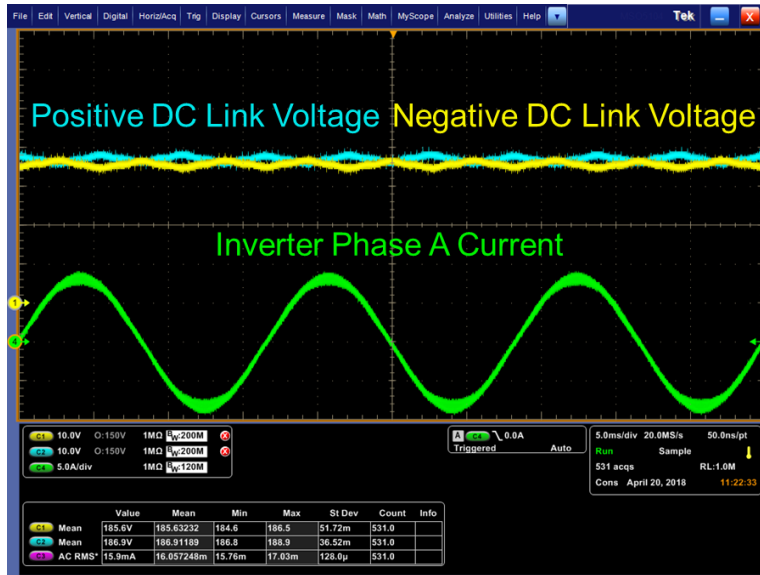
Figure 5.7. DC Link Balancing Boost Mode with Inverter Load

This test represents a much more accurate demonstration of the DC/DC converter balancing capabilities. Although the DC link voltage imbalance reduction would not be apparent when comparing two waveforms, the controller monitoring shows that the DC link voltage average difference is being regulated to zero. When both converters were operating in open loop configuration, the DC link imbalance was approximately 6 V. After closing the loop, this imbalance was reduced to within 1 V. Although this does not seem like a significant difference, recall that the overall DC link voltage is only 400 V, and that any additional DC link imbalance on top of the imbalance caused by the 180 Hz component of the inverter will only cause more issues in the converter's operation.

Finally, it is important to note that the 180 Hz ripple component of the DC link does not appear to be compensated for by the DC/DC stage. This is because the speed of the PI regulator is not fast enough to account for this ripple. There may be some additional work to investigate a faster regulation loop or active PWM methodology to eliminate or further reduce this ripple.

5.2. UPS Noise Profile Comparison

As one of the main benefits of this converter is its contribution to the reduction of the UPS noise profile, its effects were investigated while the UPS was operating. To perform the necessary experiments to evaluate the DC/DC converter effects on EMI, a test setup was made in accordance with IEC UPS testing standards.
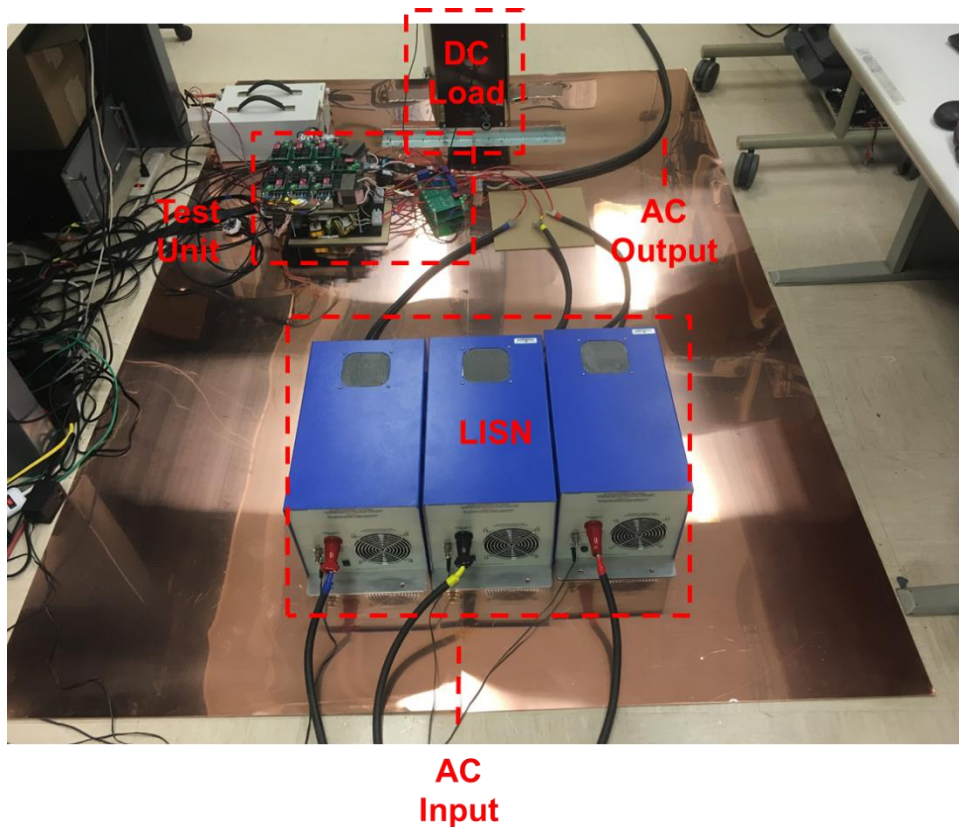
Figure 5.8. UPS EMI Test Setup

The test setup consisted of a LISN on the AC voltage input, a large conducting ground sheet, a small DC load to emulate a battery, and a resistive AC load output. The test setup measured the EMI profile of the converter at the input in accordance with standard IEC testing protocol. In this way, the different operating modes of the DC/DC converter can be tested and their effect on the stage as a whole will be measured.

First, a comparison will be shown which highlights the benefit of the converter operating in synchronous mode versus the traditional phase-shifted operation. In order to conduct this experiment, the UPS was operated at full power with the inverter operating at 80% load and the DC/DC converter operating at 20% load to simulate the battery charging operation. The DC/DC stage was then operated with and without a 180-degree phase shift. Also, the UPS was operated with no DC/DC stage operation, only AC/DC and DC/AC conversion. The EMI profile of the UPS at the LISN for each case is shown.

Figure 5.9. UPS Total Voltage Profile

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Figure 5.10. UPS Differential Mode Voltage Profile

Figure 5.11. UPS Common-Mode Voltage Profile

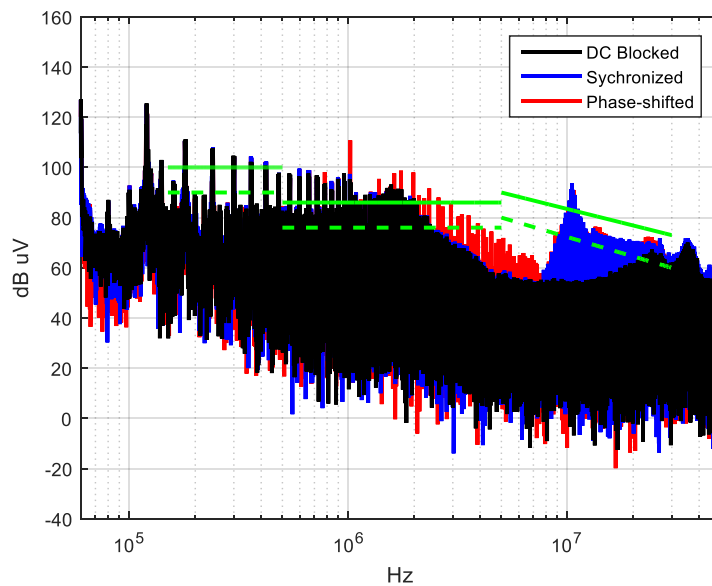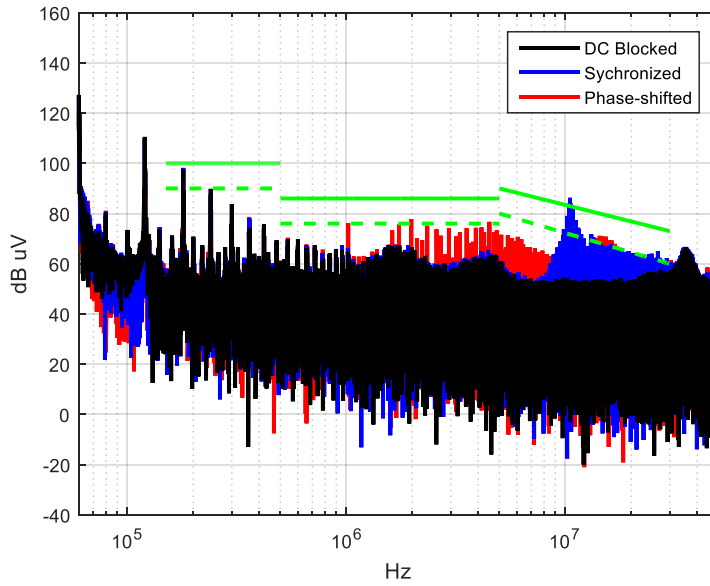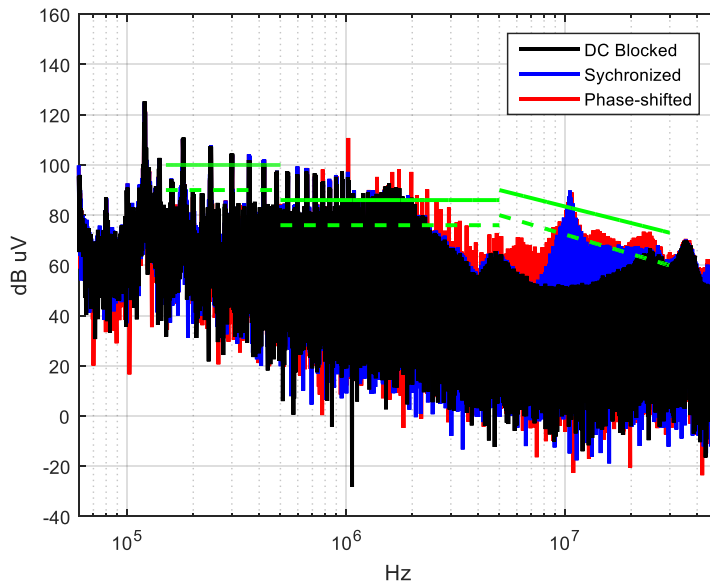In each case, there are three colors on the graph. The black DC blocked profile represents the UPS operating with no DC/DC stage operation. The blue synchronized profile is the reduced noise profile, and the phase shifted operation is the standard mode

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of operation to reduce the output current ripple. The best noise profile, as is expected, is without any battery charging operation. This represents only the noise generated by the inverter and rectifier stages of the UPS. When the DC/DC stage operates—regardless of the mode of operation—there is some additional noise added to the overall profile. However, there is significantly less additional noise when the converter operates in a synchronous switching mode. This is in line with the expected results based on the simulation in chapter 3.

Chapter 6. Conclusions and Future Work

6.1.   Summary and Final Thoughts

The proposed design topology appears to offer a number of benefits to a system with a split DC bus. These advantages are particularly useful in UPS applications, which is the motivation for this work. The process of topology evaluation, modeling and simulation, design, and experimental verification provides a solid groundwork for additional work moving forward into various ways to improve the operation of a UPS or similar system. There are also quite a few areas in which the work described in this thesis may be investigated further. There are certain unresolved minor issues and additional testing configurations which may be explored given additional time and resources.

The converter was designed to meet a target efficiency of 99%, and was experimentally verified to meet this requirement over a large portion of the operating range. This was enabled by the low switching losses of the wide-bandgap SiC devices and effective thermal solution based on calculations and accurate simulation models.

Although the efficiency was only tested in buck mode, it is expected that the results would be similar for boost mode operation. Also, the efficiency of the converter at rated power is likely to still be very high, if not in excess of 99%.

The modeling process and resulting guidelines for controller parameters were verified in simulation and experiment. The modeling process is described in detail including all estimations and assumptions made in the process. This information can be used for this topology, and potentially other similar three-level DC/DC topologies. The DC link voltage was able to be regulated effectively using the DC/DC stage controller properties described in section 3 whether operating in buck or boost mode. This functionality is quite beneficial to the UPS as the imbalance in DC link voltage can have a negative impact on the system as a whole, and depending on the operating mode of the system, the DC/DC stage may be the best candidate to regulate this difference.

The noise profile of the UPS as a whole saw a significant reduction in its noise profile as seen by the LISN at the AC input. This allows for the use of smaller EMI filter components compared to traditional topologies in order to meet IEC standards necessary for commercialization. Also, the three-terminal model was shown to accurately predict effects of different stages and their effects on the voltage profile, which proved to be an essential point in the topology design selection. Although the operation of the converter necessary to attain these benefits does not allow for a reduction of the output ripple properties compared to a traditional buck converter, the overall volume of filter components may be reduced in the system based on EMI filter sizing. This makes the proposed topology and switching sequence a worthwhile candidate in noise-sensitive three-level systems.

6.2.   Future Work

Although the work described is thorough and valuable, there are still a number of areas in which the topology may be improved, understood better, or tested further. For example, the ringing seen at the output of the converter during dead time is not well understood, and may be analyzed further. I believe that a more detailed simulation of the topology including all known parasitics would provide valuable insight into how these parasitics interact, and would explain the ringing seen. Once this has been performed, a slightly different design approach or setup may be utilized to improve the output quality of the converter. This would eliminate the need to add an additional output filter

Although the converter was tested and verified to regulate the DC link voltage, it is possible that the topology would be able to provide additional benefit to the system in certain instances. Also, there are limitations of the converter's usefulness within the system which may need further analysis. One additional feature briefly discussed in section 5.2 is the potential ability of the converter to mitigate the 180 Hz ripple component on the DC bus capacitors due to the inverter load. A more detailed PWM scheme or better control methodology may be proposed to reduce this ripple component.

Also, the converter may not be able to provide any additional functionality to the system when the battery is not in use. For the majority of a UPS's life cycle, the only conversion performed is by the inverter and rectifier stages, and the battery remains charged and unused. Unless the battery has been drained and is being charged, or is being used to support the DC link, the DC/DC stage is not in operation, and its benefits are not provided to the system.

Finally, although the DC link balancing capabilities are shown and may be useful in the system, its effect on the noise profile of the UPS are not well understood. It is demonstrated through simulation and testing that introducing a phase shift in the converter operation has a detrimental impact on the UPS noise profile. Although the DC link balancing capability does not introduce nearly as much of a phase shift as the simulated and experimental results, there should still be some common-mode noise generated as shown in section 3.2. If the noise penalty for the DC link balancing is greater than the penalty when this balancing is performed by the inverter or rectifier stage of the UPS, this functionality may not be very useful in UPS applications. However, this topology needs to be better understood before such a decision can be made.

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