Optimal Design of MHz LLC Converter for 48V Bus Converter Application

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(ABSTRACT)

The intermediate bus architecture employing the 48V bus converter is one of the most popular power architecture. 48V to 12V bus converter has wide applications in telecommunications, networks, aerospace, and military, etc. However, today's state of the art products has low power rating or power density and becomes difficult to satisfy the demand of increasing power of the loads. To improve the current design, a GaN (Gallium Nitride) based two-stage solution is proposed for the bus converter. The first stage Buck converter regulates the 40V to 60V variable input to a fixed 36V bus voltage. The second stage LLC converter convert the 36V to 12V by a 3:1 transformer. The whole solution achieves the fixed frequency control. The thesis focus on the detail design and optimization of LLC converter, especially its transformer. To have high density and high efficiency, the transformer design becomes critical at MHz frequency. The matrix transformer concept is applied and a merged winding structure is used for flux cancellation, which effectively reduces the AC winding losses. A new fully interleaved termination and via design is proposed. It achieves significant reduction in loss and leakage flux. In addition, to study the current sharing of parallel winding layers, a 1-D analytic model is proposed and a symmetrical winding layer scheme is used to balance the current distribution. The hardware is built and tested. The proposed two-stage converter achieves the best performance compared to the current market.

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(GENERAL AUDIENCE ABSTRACT)

Intermediate bus architecture (IBA) has wide applications in telecommunication, server and computing, and military power supplies. The intermediate bus converter (IBC) is the key stage in the IBA, where the DC bus voltage from the front-end power supply is converted to a lower intermediate bus voltage. Traditional IBC suffers from bulky magnetic components including inductors and transformers.

This work illustrates the design and implementation of a two-stage IBC, where the first-stage Buck converter will provide regulation and the second stage LLC converter will provide isolation. Thanks to the soft-switching capability of LLC, the magnetic volume can be significantly reduced by raising the switching frequency of the converter. Therefore, planar magnetics can be used and placed directly inside of the printing circuit board (PCB), which allows for higher power densities and easy manufacturing of the magnetics and overall converter. However, as the frequency goes higher, the AC losses of the transformer caused by the eddy current, skin effect, and proximity effect become dominant. As a result, high-frequency transformer design becomes the key for the converter design. First, matrix transformer concept is applied to distribute the high current and reduce the conduction loss. Second, a novel merged winding structure is proposed for better transformer winding interleaving. Third, a new terminal structure of the transformer is proposed. Finally, the current sharing between parallel windings are modeled and studied. All the efforts result in great loss reduction. The prototype were verified and compared to the current converters that are on the market in the 48V – 12V area of IBCs.

Dedication

This work is dedicated to my family,

My Father: Jiangyong Cai

My Mother: Hong Zhu

Acknowledgments

I would love to take this opportunity to thank my advisor Dr. Qiang Li, for the support and guidance through my experience in the Center for Power Electronics Systems (CPES). I would also love to thank Dr. Fred C. Lee for his guidance.

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Chapter 1

Introduction

1.1 History of Intermediate Bus Architecture

The distributed power system has long been used in the telephone industry. It utilizes a front-end power supply to distribute an approximately -48V bus voltage throughout the telephone equipment loads. The front-end power supply uses AC power as input and has the functions of rectification, filtering, and battery power backup [1, 2].

With the development of electronic switching and on-board DC-DC converters in the 1980s, the telephone society adopted the on-board power supply strategy. The 48V bus was directly connected to each circuit card in the equipment rack. And on each card, the 48V is converted by the isolated DC-DC converters to supply required voltages of electronic loads. This approach became very popular in the 1990s, and has been widely applied in all kinds of telecommunication, networking, and computing applications [3]. An example of this traditional distributed power architecture is illustrated in Figure 1.1.

As the fast development of integrated circuit, however, the telecommunication and computing systems have become more complex [4, 5]. First, various voltages are required by different loads including logics and processors in an individual card. Second, much higher power is demanded by these electronic loads. In a typical server system, thirteen different output voltages and 1kW power are required [3, 6] If we still rely on the traditional architec-

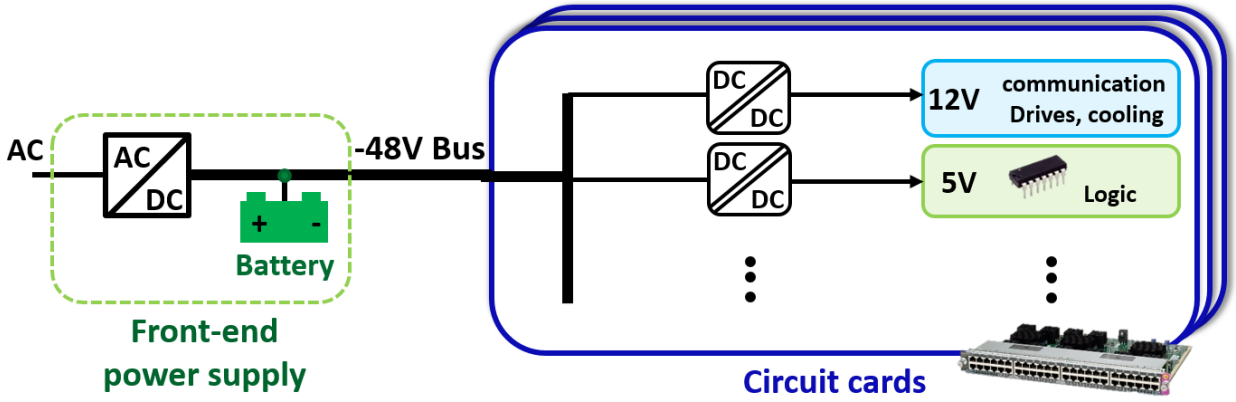


Figure 1.1: The traditional distributed power system in a network switch.

ture, where each electronic load is supplied by a DC-DC converter, many isolated DC-DC converters must be designed and mounted on the cards. For an isolated converter, the design complexity increases as the power demand of the loads increases [7, 8]. As a result, the power system suffers from high cost, large volume, and complexity. To address these issues, the concept of intermediate bus architecture (IBA) was proposed to reduce the large number of isolated DC-DC converters demand [4, 9]. In IBA solution, however, only one or a small number of isolated DC-DC bus converters are employed for the isolation requirement, and supply an intermediate bus voltage, which is typically 12V. The intermediate bus is followed by several non-isolated point-of-load (niPOL) converters for the final regulation to various electronic loads. Without the isolation requirement, these POL converters can be designed much smaller and more efficient. They can be placed close to the target load and hence improve the transient performance. With these benefits, we end up with a more efficient, lower-cost, and more compact overall solution [10]. The IBA approach is widely adopted in all kinds of distributed power systems nowadays [3]. Figure 1.2 shows one example of IBA.

The isolated bus converter plays a very important role in the IBA implementation. A high-power, highly-efficient, and small solution for the intermediate bus converter (IBC) is desired. The isolated bus converter can be regulated or unregulated, depending on the

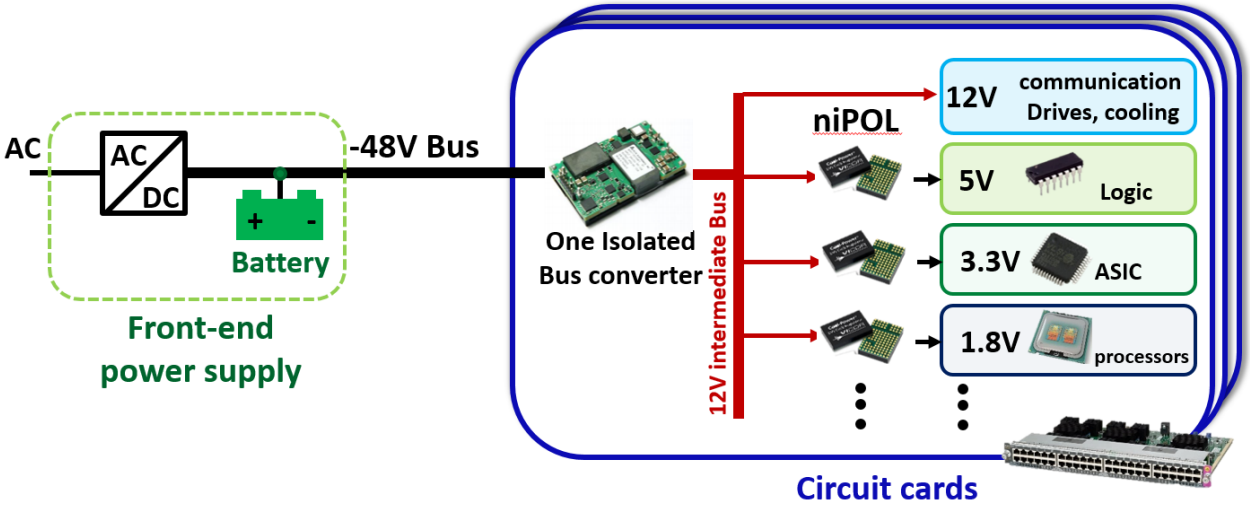


Figure 1.2: The intermediate bus architecture in the new network switch power supply.

requirements of the system. For power supplies with a regulated 48V bus, such as enterprise equipment with Server System Infrastructure initiative [3], an unregulated DC transformer (DCX) can be used for the IBC. For other applications, such as telecom equipment that has wide input voltage range (35V to 72V), regulation is necessary for the IBC to maintain an accurate output voltage, release design burdens for the niPOL, and achieve better overall efficiency. Additionally, for systems that need a strictly regulated voltage on the intermediate 12V bus, e.g. for power fans and disk drives, the regulated IBC is the only choice [11]. This dissertation will focus on the design of regulated IBC.

1.2 Topology of Intermediate Bus Converter

The state-of-the-art IBCs fall into two categories: single-stage solution [12] and two-stage solution [13]. [12] uses a phase-shift-full-bridge converter (PSFB) as a single stage. The first problem with this solution is that PSFB is not a complete soft-switching topology. The high switching loss limits the switching frequency to 150kHz, which leads to bulky

magnetics. To handle the large amount of output current, four synchronous rectifiers (SRs) are connected in parallel. The current sharing between these SRs are critical. Also, the transformer suffers from high termination loss and conduction loss on the secondary side. To improve this solution, an LLC converter can be used instead of the PSFB. Compared with PSFB, LLC can achieve zero to full load ZVS, and ZCS for the SRs. It also has very low turn-off current for primary side devices [14, 15, 16]. Therefore, with the benefits of LLC, the switching frequency can be pushed higher to reduce the magnetic size. However, due to the nature of the resonant converter, LLC converter needs variable frequency control. This is acceptable in some application, but in other applications where there is a stringent EMI (Electromagnetic Interference) specification, the fixed-frequency solution is preferred. With two-stage architecture, it is easier to design a fixed-frequency IBC with high efficiency and power density. The basic idea is to design one isolation stage and one regulation stage. The isolation stage is an unregulated fixed-ratio converter. With an effective duty cycle close to 100%, it can be highly efficient. The regulation stage can be implemented with fixed-frequency control. However, due to the serial connection of the two stages, the overall efficiency of the two-stage solution could be lower than that of the single-stage. Moreover, the regulation stage is usually a PWM converter which requires the inductor. The power density of the whole solution would also suffer from magnetic components in both stages and results in lower power density.

1.3 Transformer Design of Intermediate Bus Converter

In the previous discussion, soft-switching topology like LLC is used to push the switching frequency and shrink the magnetic size. To further improve the efficiency, there are two things to be considered. First, use better devices to further reduce the device conduction

loss and switching loss. This becomes possible with the development of wide-bandgap devices like GaN [17]. Details will be discussed in the device selection and loss analysis. The second possible improvement is the transformer design. The transformer design is significant for both single-stage and two-stage IBC. As we discussed in 1.2, the conduction loss, termination loss, the SRs current sharing have a great impact on the efficiency. All these are related to the transformer design and should be studied carefully and systematically. In effect, at the high switching frequency, the transformer loss becomes much more dominant than that of low frequency.

A comprehensive analysis is made in [18] on the high-frequency transformer loss. The traditional transformer schematic and structure used is shown in Figure 1.3 and Figure 1.4. It uses planar magnetic cores EIR 22 with PCB windings. On the primary side, four turns of primary windings are realized by connecting four primary winding layers in series. On the secondary side, each layer has one turn of secondary windings, and four secondary winding layers are connected in series to handle the large secondary current. Two SRs are paralleled for each rectifier branch. Maxwell 3D FEA simulation is used for the estimation of transformer performance, including leakage inductance, winding resistance, and losses. Figure 1.5 shows the current distribution of primary and secondary windings. Qualitatively speaking, the hot spot on the windings means current crowding in certain areas, which significantly increase the equivalent winding resistance and winding loss. This uneven current distribution is due to the skin effect within one winding and proximity effect between multiple windings. At lower frequency, these effects are relatively small. But in our application, we keep pushing the frequency for higher power density and these effects have great impacts on the copper loss. The simulation data shows that the transformer conduction loss increases 43% when increasing the frequency from 200kHz to 2MHz. The transformer conduction loss at 1MHz and 40A load can be 8W based on simulation, which is about 1.6% total

power. Conventionally, we increase the copper thickness and winding width to reduce the DC conduction loss. However, this approach is useless in high-frequency condition due to the skin effect and proximity effect, which make the AC conduction loss dominant. For PCB windings, it's basically pieces of copper, and hence one cannot reduce the skin effect and proximity effect by the "multi-strand" concept as used in litz wire. To address this issue, [10, 18] proposed a new transformer structure, i.e., the matrix transformer.

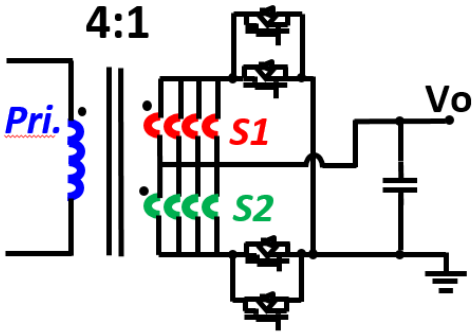


Figure 1.3: Circuit schematic of traditional transformer

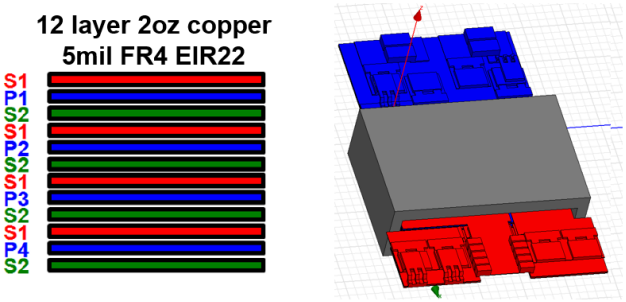
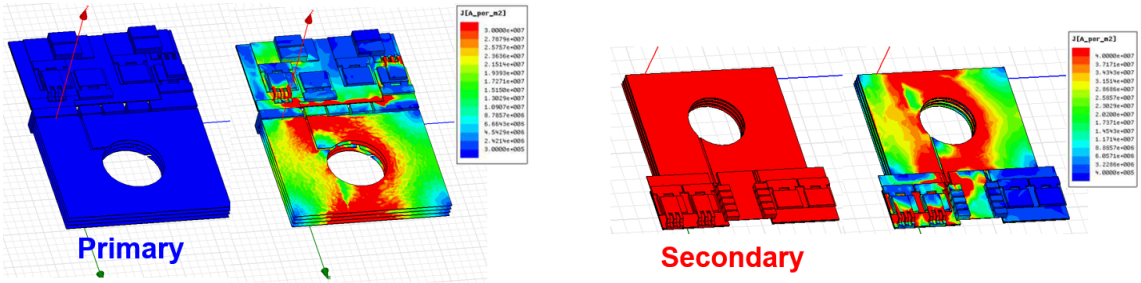


Figure 1.4: Structure of traditional PCB-winding planar transformer

The matrix transformer is an array of elemental transformers interwired in order that the overall works as a single transformer [19]. In other words, the original one transformer is broken down into two or more elemental transformers. The goal is to distribute the high AC current across multiple transformers and at the same time guarantee good current sharing between these transformers. To achieve this goal, the primary windings of all the elemental transformers are connected in series, and the secondary sides of the transformers



(a) Primary winding current.

(b) Secondary winding current.

Figure 1.5: Current distribution of traditional transformer windings at 800kHz

are connected in parallel. Due to the parallel connection, the secondary high AC current is distributed on all transformers. And due to the series connection of primary windings, the secondary current of each transformer, which is reflected from primary, becomes equal naturally. Here it's assumed that each transformer uses the structure and has the same magnetizing inductance. The schematic of matrix transformer proposed in [10] is illustrated in Figure 1.6. Two elemental transformers are used. Simulation data shows that the conduction loss is reduced by half and current crowding is greatly diminished. Another benefit of this structure is the current balancing of the SRs. In the traditional structure, it is difficult to ensure current balancing between the two parallel SRs. In the proposed structure, the SRs of each elemental transformer are naturally paralleled. As long as the current sharing between the transformer is good, there is no current sharing issue between SRs.

However, the drawback of this transformer structure is also apparent. When the number of transformers is increased, so does the core loss. Note that due to the secondary parallel connection, the voltage-second on each elemental transformer is the same as that of the traditional single transformer. Consequently, the core loss becomes much higher. To reduce the core loss, transformer integration concept is proposed with flux cancellation [20]. The integration steps are shown in the flow chart in Figure 1.7. The yellow dot and cross represent the flux direction in the core. The blue and red arrows represent the primary and secondary

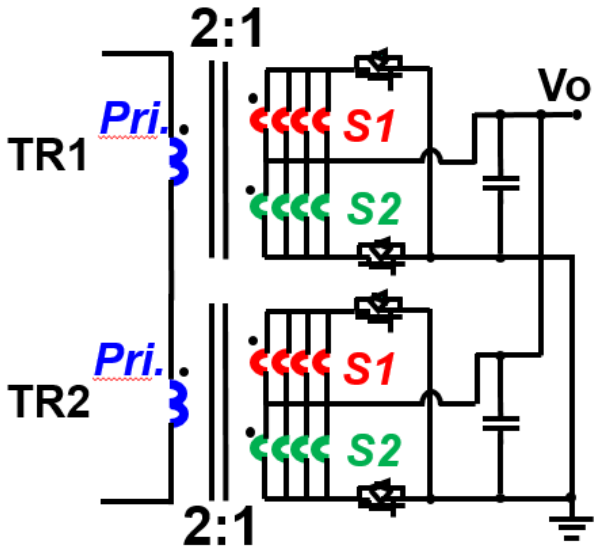


Figure 1.6: Circuit schematic of proposed matrix transformer

current flowing along the windings, respectively. First, the original two EIR cores can be combined into one EI core. This integration helps to simplify the transformer structure and manufacture. But it keeps the same cross-section area of flux and the core loss is still high. Second, by changing the primary winding connections, the current direction is altered and so does the flux direction. The flux created by two transformers now flows in opposite directions in the center leg of the core. Due to the symmetrical structure of the two transformer, the two sets of flux have the same magnitude but flow opposite. Therefore, the flux in the center leg is canceled, and the core loss is reduced by half. The final step is to remove the center leg since there is no flux in it. This gives a simple UI core structure.

Based on the simulation result, it is found out that half of the leakage inductance is created by the transformer termination, and half of the secondary conduction loss is from the secondary termination [10]. In the termination, the windings are connected to the devices and are usually not in the perfect interleaved structure as we have in the winding turns. Therefore, a large amount of leakage flux are created and proximity effect becomes

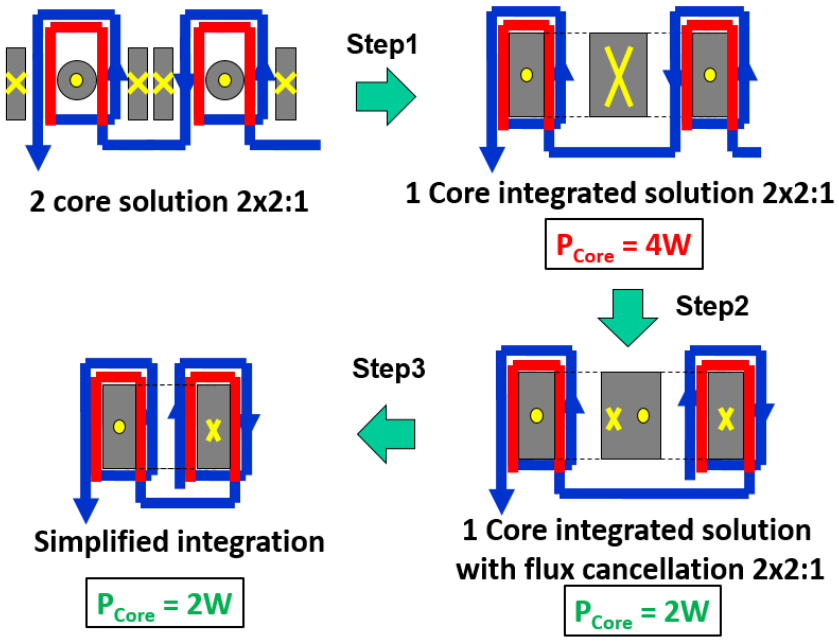


Figure 1.7: Steps of magnetic integration and flux cancellation

severe, which creates eddy current and extra loss on the termination copper. High AC current flowing through the secondary termination loop creates high leakage flux and high AC conduction loss. To improve the design [21], the SRs and output capacitors are re-positioned to form a smaller termination loop. The leakage inductance and equivalent resistance are reduced by around one third with this improvement. Despite that the secondary termination issue is noticed and somehow improved, there could still be better solutions. Moreover, none of the previous works mentioned above carefully studied the primary termination design and current sharing issues of parallel windings in multiple layers. In their applications, these issues should not be a problem. The output current can be high, but the primary side current is small (usually smaller than 15A RMS). However, in the 1kW bus converter design, with 36V bus voltage, the primary current is much higher, which can cause great AC termination and via loss at 1MHz frequency. Also, to handle the large current, more parallel windings are used. The current sharing between these windings becomes another new challenge that

must be solved. All of the above issues are discussed and addressed in the thesis.

1.4 Thesis Outline

Chapter one gives an introduction to the intermediate bus architecture and its application in telecommunications. It also introduces the limitation of today's topology for regulated bus converter and the improvement by using LLC resonant topology. The key issue of the LLC design, the transformer design is discussed. The literature review on the transformer design is done.

Chapter two introduces the proposed two-stage solution for regulated bus converter. The detailed structure of the second stage transformer is discussed. It adopts the matrix transformer concept to distribute the large output current. A novel merged winding structure is proposed to achieve better flux cancellation and reduce AC losses.

Chapter three digs into the challenges of primary side termination design. Traditional primary termination design suffers from high AC loss at high frequency. A new termination structure with interleaved termination layers and vias are proposed achieving great loss reduction.

Chapter four discusses the current sharing of parallel layer windings. The traditional structure suffers from poor current sharing between parallel layers. An analytic model is proposed to calculate the current distribution. A new symmetrical winding layer arrangement is proposed to achieve better current sharing.

Chapter five talks about the optimization process and experimental results, and summarizes the work. Chapter six makes the conclusions.

Chapter 2

Two-Stage Solution for Regulated Intermediate Bus Converter

2.1 Design of the Two-Stage Architecture

The circuit diagram of the two-stage solution is presented in Figure 2.1. The power rating of this design is 1kW. The input voltage range is from 40V to 60V. The output voltage should be regulated at 12V. The first stage is a 4-phase Buck to regulate the voltage. The second

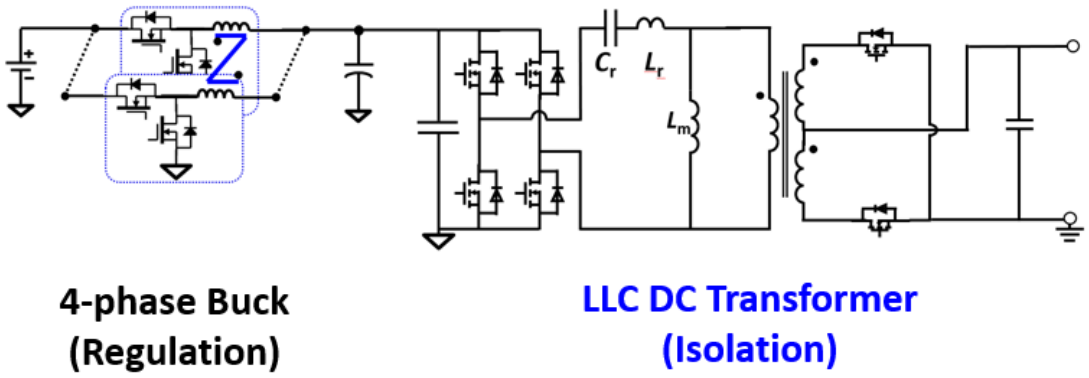


Figure 2.1: Circuit diagram of the two-stage bus converter.

stage would be a resonate LLC DC transformer (LLC-DCX) for isolation. The switching frequency of Buck is optimized at 500kHz per phase. The switching frequency of LLC converter is selected to be 1MHz based on experience. It can be iteratively optimized later.

The first-stage Buck is hard-switched. The reason for using hard switching is because to achieve soft switching, the inductor current would be very large and have a high di/dt for the desired switching frequency. With a large inductor current and high di/dt, the magnetics for the buck would be very large and would hurt the overall size of the converter. In terms of the order of the two stages, we use LLC-DCX as second stage to handle the high output current. The bus voltage of the two-stage converter would be either 36 V or 24 V because the LLC-DCX would be optimally designed around an integer number of turns, so 3:1 or 2:1. With a 24V bus, the Buck would have more switching loss and conduction loss for both devices and inductor coils due to higher output current. It would also have larger magnetics due to higher current ripple. With the same Bmax allowed, the cross-sectional area of the inductor core has to increase. For the LLC converter, it would suffer from higher conduction loss for both primary devices and transformer windings. Even though lower voltage device could be used, it is usually less dominant than the impact of higher input current. As a result, the 36V bus is selected based on the qualitative analysis above.

The duty cycle range of the Buck is 0.60.9. The input of the LLC-DCX would be 36V/27.78A, and the output of LLC would be 12V/83.3A. The simple fixed-frequency average current mode control is implemented for the Buck. The LLC converter will operate at switching frequency at resonant frequency, which is the optimal efficiency frequency for the operation. If the switching frequency is higher than resonant frequency, the RMS current could become a little lower but the turn-off loss becomes higher. Moreover, it loses the zero current turn-off for the secondary side SRs. This causes higher reverse recovery loss, higher voltage stress for devices, and higher noise in the circuit. If the switching frequency is smaller than that of the resonant frequency, the magnetizing inductor participates the resonance and the circulating current will raises the overall RMS current and hence conduction loss for both devices and transformer windings. So with the two-stage architecture, we guarantee that

the LLC converter efficiency is optimized and the whole solution is fixed-frequency. The block diagram of two-stage circuit is presented in Figure 2.2. An isolated regulator is used

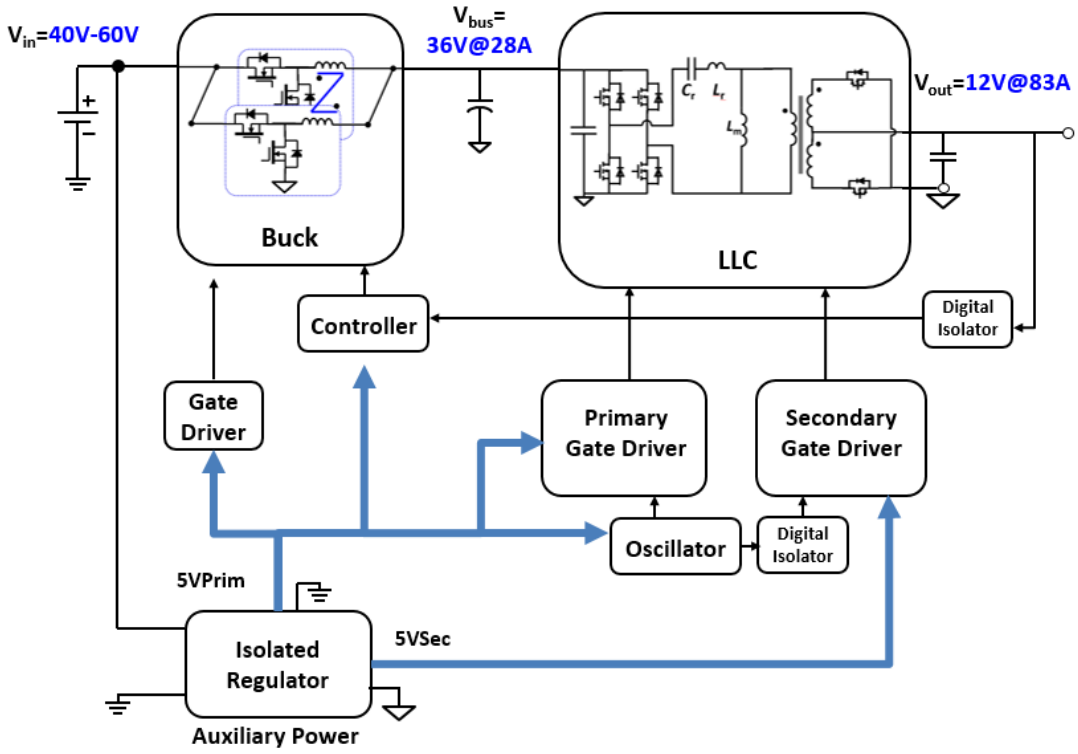


Figure 2.2: Block diagram of the two-stage bus converter.

as the auxiliary power. It uses input voltage of the power stage and has two isolated outputs. The first primary output provides power for the Buck gate drivers and controllers, and primary gate drivers and oscillators of the LLC. The secondary output provides power for the secondary gate drivers of the LLC. The output of LLC is feedback to the controller of Buck through a digital isolator. The focus would be on the LLC converter design. The Buck design is beyond the scope of this thesis.

2.2 Design of the LLC-DCX Converter

2.2.1 LLC Topology and Device Selection

To design the LLC converter, we need to select the device and topology first. The LLC resonant converter is composed of four parts: the primary side switch network (inverter), the resonant tank, the transformer, and the secondary side switch network (rectifier). The design of primary and secondary switch networks will be discussed in this subsection. The transformer design will be studied in the following sections and chapters. After the design above is completed, the leakage inductance, magnetizing inductance, and resonant capacitors of the resonant tank will be determined subsequently.

For the primary side, half-bridge and full-bridge topologies are two most commonly used switch networks. The full bridge and half bridge have the same voltage stress for devices. The full bridge doubles the number of devices used and hence has a larger footprint, higher driving loss, and higher complexity. However, the AC output voltage of half bridge is the half of that of the full bridge, which means two times larger current on primary side. Higher primary side current causes higher conduction losses for both primary devices and transformer windings. Note that although full bridge has more devices, the conduction loss still becomes less severe due to the current square relationship with the ohmic loss.

For either half bridge or full bridge, the voltage stress of the device is 36V input voltage. Although LLC usually has small turn-off current and hence small turn-off voltage overshoot for the device, 40V devices leave a too small margin for the voltage variation. Therefore, 60V devices are used. Compared with Silicon devices, at the same breakdown voltage, GaN devices has a much smaller figure of merit (FOM). Hence, GaN device EPC2020 is selected as the primary device. The primary device loss of EPC2020 using full bridge topology is

calculated by equation 2.1.

$$P_{loss-prim} = (P_{drive} + P_{conduction} + P_{off})N_{device} \tag{2.1}$$

N_{device} is the number of primary devices used. Since LLC converter achieves zero-voltage switching turn on (ZVS) for full load range, the primary device loss is composed of driving loss, turn-off loss, , conduction loss. The driving loss gives by

$$P_{drive} = Q_g V_g f_s \tag{2.2}$$

Where V_g is the gate voltage and f_s is the switching frequency. The conduction loss is given by

$$P_{conduction} = I_{prim}^2 R_{dson} \tag{2.3}$$

Where I_{prim} is the RMS current on the primary device, which can be calculated according to [15] and [16]. The turn-off loss is estimated from the SPICE simulation with the device model from EPC. Finally, the total primary device loss of EPC2020 using full bridge topology is presented in Figure 2.3 curve "EPC2020 single". The temperature impact on the R_{dson} derating is considered using the junction-to-ambient thermal resistance and on-resistance vs. junction temperature curve provided in the datasheet. According to the calculation, the junction temperature at 1kW would rise to 125°C (the ambient temperature is set to 55°C based on the application), which is too close to the 150°C maximum rating. To leave enough margin, two EPC2020 are used in parallel for each leg of the full bridge and the result is shown in Figure 2.3 curve "EPC2020 parallel". The temperature is reduced to 80°C and the loss is also reduced from 9W to 5.5W at full load. A similar process is applied on half bridge design. EPC2020 using half bridge is not considered because the temperature goes too high even with the parallel structure. As a result, the full bridge parallel design is adopted. The

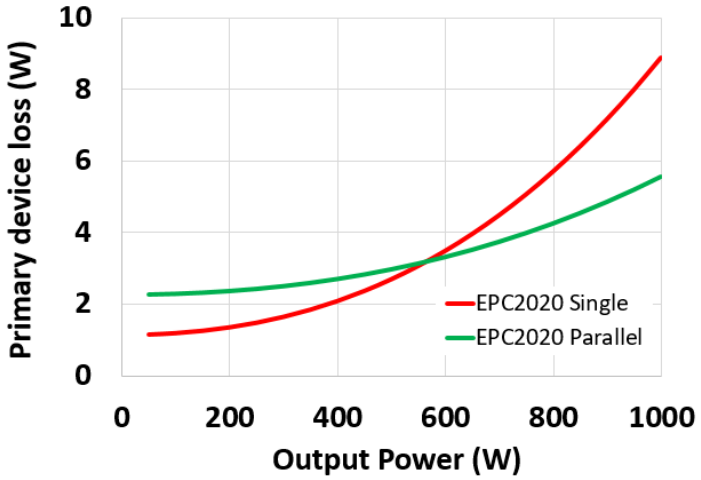


Figure 2.3: Primary device loss curve for full bridge structure using EPC2020.

gate driver used for EPC2020 is LM5113, which is specially designed for GaN FETs driving that can provide fast switching speed and voltage clamping. (Recently Texas Instrument stopped manufacturing this device and now recommend the LMG1205. Both of these devices are very similar with the only difference being in the internal propagation delay.)

The LLC converter that has integrated PCB-winding transformer is shown in Figure 2.4. In this design, the 3:1 transformer is distributed into three 1:1 elemental transformers, which

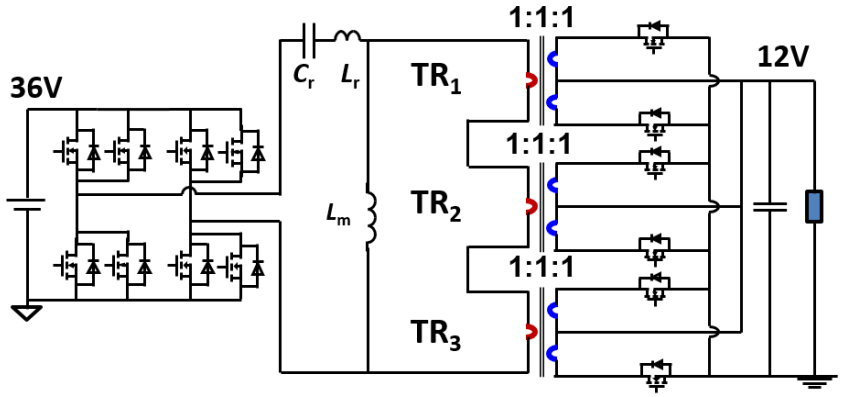


Figure 2.4: Conceptual circuit schematic of LLC-DCX with matrix transformer.

are connected in parallel from secondary sides and in serial from primary sides. The detailed design will be discussed in the following subsection. The center-tapped rectifier is selected as the secondary topology. Compared with the full bridge rectifier, center-tapped topology has a smaller number of devices, which gives lower cost, lower footprint, lower control complexity, and smaller conduction loss and switching related loss. The advantage of full bridge rectifier is that the voltage stress on secondary SRs is half of the center-tapped rectifier. So lower voltage devices could be used. However, for low output voltage application here, the voltage difference is small. So the R_{dson} and Q_g improvement by using the full bridge is also small. For 12V output, the voltage stress on SRs is 24V. 30V device BSZ0500NSI is selected due to its small Rdson, low Qg and small package. To select the gate drive voltage, the trade-off has to be made between driving loss and conduction loss. Two typical Vgs values, 5V and 10V are selected for comparison. Similar as in the primary design, here we can also parallel two SR devices for each center-tapped leg. Finally, we have four combinations of different designs. For LLC-DCX, the secondary SRs achieve ZVS and zero current turn-off (ZCS). So the SR device loss is only composed of driving loss and conduction loss. The loss results are compared in Figure 2.5. Since we care more about the heavy load efficiency in this application, 5V V_{gs} with parallel structure design is selected.

2.2.2 Matrix Transformer Structure

In this design, the 3:1:1 transformer is broke down into three 1:1:1 elemental transformers to distribute the high output current and reduce the winding and termination loss. It also helps the current sharing of SRs. The circuit diagram is shown in Figure 2.4. And we also integrate the three transformers in to one core, as shown in Figure 2.6. The red and blue arrows represents the primary and secondary current path. However, due to the odd number of transformers, it is hard to achieve flux cancellation in the integration. All the flux of

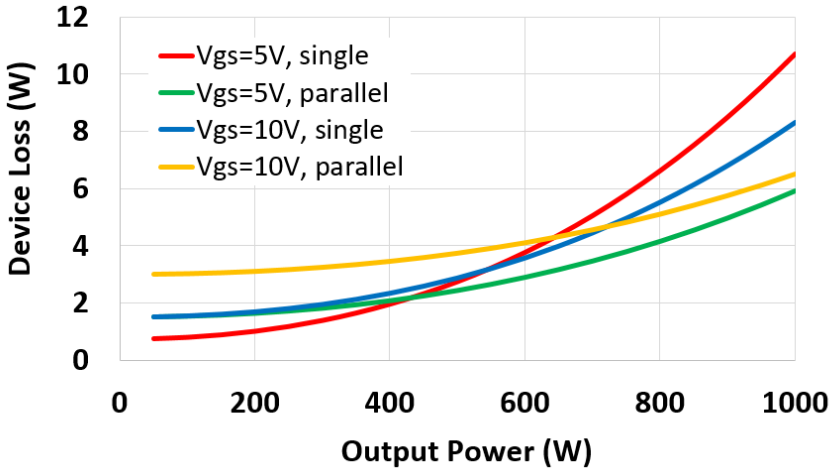
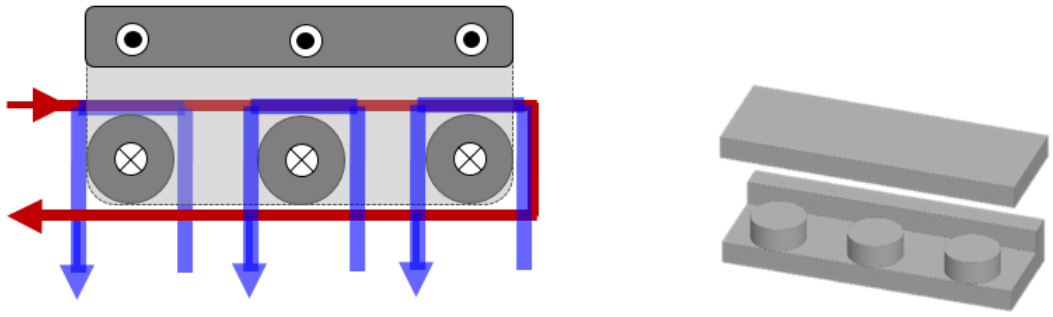


Figure 2.5: Secondary device loss curve for center-tapped structures using different gate voltages.

the three transformers has to flow through the bar of the core, and cannot cancel with each other. The 3D view of the customized core is presented in Figure 2.6b. This integration still can help achieve the same air-gaps and L_m across all the transformer and it also becomes easy for manufacture. The flux distribution are analyzed using the 3D FEA simulation. The 3D view and top view are shown in Figure 2.7. In addition, three cross-section view a, b, and c are examined and presented in Figure 2.8. Although some core areas are not utilized due to the corner effect, the overall distribution is fine. The extended core areas are utilized so that the core thickness can be reduced. In the view c, some flux crowding is observed. Future work could be done to reduce the crowding and further improve the flux distribution.

The complete circuit diagram the LLC-DCX is presented in Figure 2.9. The primary and secondary windings are color-coded. The primary windings are marked by red. There are two groups of secondary windings for the center-tapped rectifier. The secondary windings group #1 are marked by blue, and the secondary windings group #2 are marked by green. The dots on the primary and secondary sides of each transformer refer to the dotted terminals. For each elemental transformer output, the secondary side windings are parallel in four layers to



(a) Top view of three transformer integration. (b) 3D view of integated core with three elemental transformers.

Figure 2.6: Three transformer cells are integrated into one magnetic core.

handle the large current on the secondary. To fully interleave with the secondary windings, the primary windings are also parallel in four layers. It can also help distribute the primary side current and hence reduce the winding loss. With this design, we end up with 12 winding layers in total. The four parallel windings are selected based on experience. In addition, it is a normal practice now to use 12 or more layer PCB for the bus converter design.

The front view of the transformer are shown in Figure 2.10. Two additional layers are placed on the top and bottom of the 12 winding layers. All the devices and components are placed on the top and bottom layers. It can greatly improve the secondary termination structure, which will be discussed in the next chapter. The 12 layers are winding layers and are separated into four groups. Each group has the same layer arrangement. secondary layer number one, primary layer, and secondary layer number two. The first group is circled in the figure. The magneto-motive force (MMF) of the positive half cycle when secondary winding #1 conducts is shown beside the front view. The negative cycle is very similar. Therefore, in the following design to improve the interleaving, it is assumed that the capacitive impact can be ignored. The top view of winding layers is shown in Figure 2.11. The primary winding structure minimizes the DC resistance. The yellow arrows demonstrate the current flow of

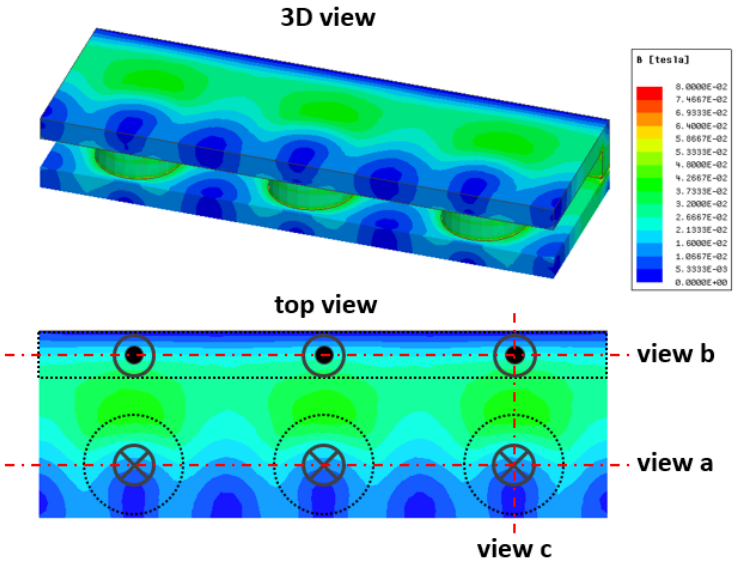


Figure 2.7: 3D view and top view of the flux distribution in the core.

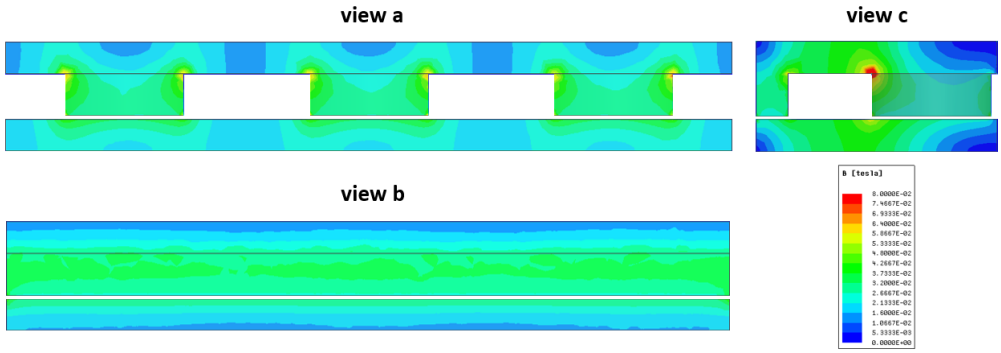


Figure 2.8: Three cross section views of the flux distribution in the core.

the positive half cycle. the cross on the core leg indicates the flux direction. In the negative half cycle, the current changes the direction and the secondary current will flow on the other secondary windings.

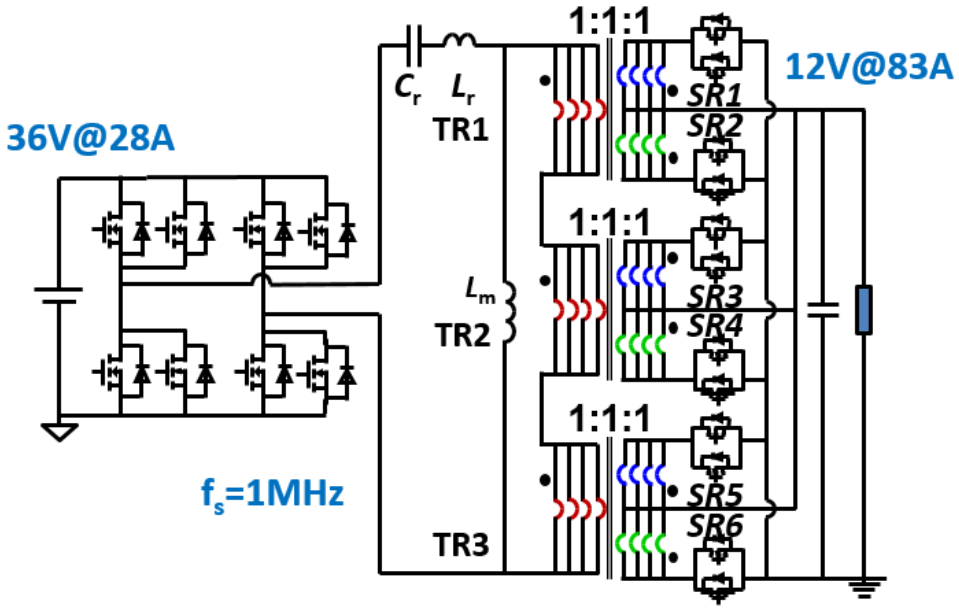


Figure 2.9: Complete circuit diagram of proposed LLC-DCX with matrix transformer structure.

2.2.3 Merged Winding Design for Better Interleaving

However, there is an issue for this simple primary winding structure. Because now the primary windings do not repeat the shape of the secondary windings and cannot be completely overlapped, there are non-interleaved regions, as circled in cross-section view in Figure 2.12a bottom.

In the middle areas, the primary current and secondary current flow in the perpendicular direction, instead of the opposite. Large leakage flux are created because of the non-interleaving. As shown in Figure 2.12b, the non-interleaved regions suffer from much higher current density (hot spot), which would increase the winding loss significantly. If this issue cannot be solved, the benefit of using the simple primary winding structure would be compromised. A new primary winding structure that has better overlapping with secondary windings is then required. For the odd number of transformers in our case, this is hard to

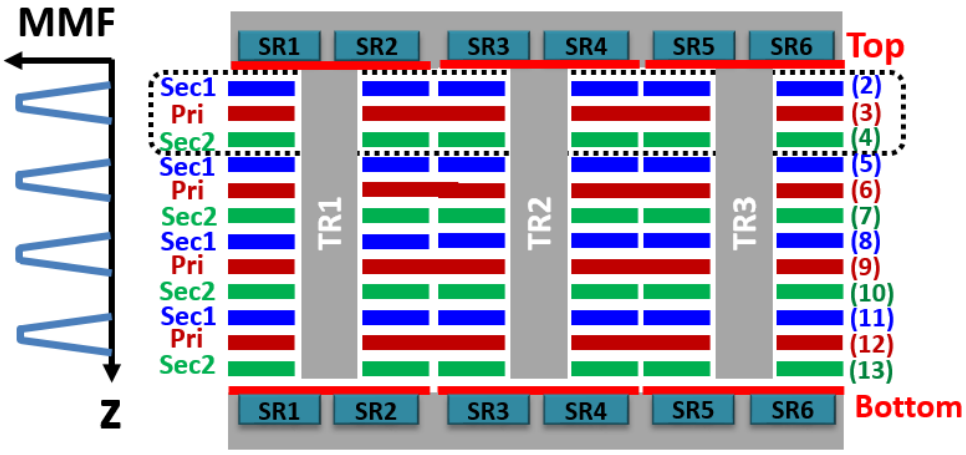


Figure 2.10: Front view of the proposed transformer.

design.

To address this issue, two separate secondary windings number one are merged into one, and similar for secondary number two, as presented in Figure 2.13a, circled by dashed lines. Since the overlapped regions should be connected to output terminal, so this change does not influence the circuit operation. Take the merged winding on secondary #2 as an example. Now the current on secondary #2 is free to flow on part of the winding of the first transformer. Due to this freedom, it will be attracted by two current: current on primary winding and current on secondary #1. As a result, the current on secondary #2 will extend its path to the left, interleaving with both primary current and secondary #1 current. The new current path is presented in Figure 2.14. The black paths represent the opposite flow of two secondary current. The purple paths represent the opposite flow between primary and secondary #2. With all these current flowing oppositely, the leakage flux are canceled, as shown in Figure 2.13b. Figure 2.15 presents the H field comparison. It is shown that the new structure has very good flux cancellation. The other merged area on the right is similar. The current distribution of the proposed structure are shown in Figure 2.13b. The current

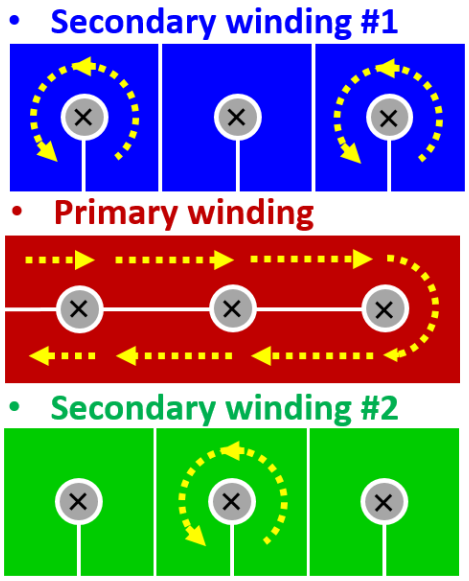
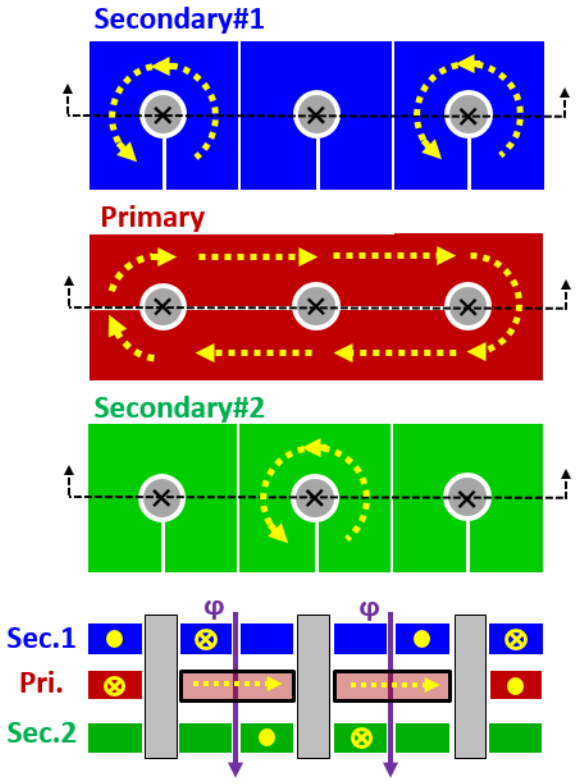
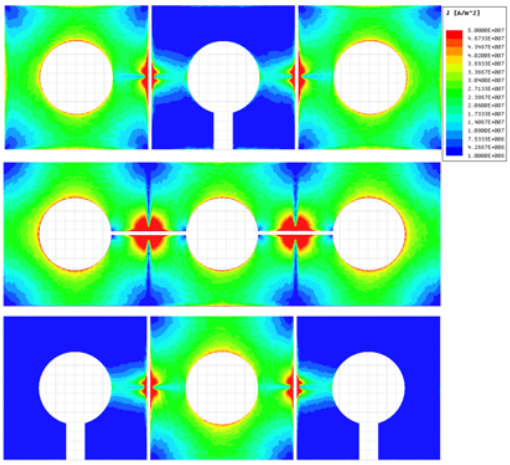


Figure 2.11: Top view of one group of PCB windings.

crowding is sharply reduced. Based on simulation results, the total winding loss is reduced by 40%.

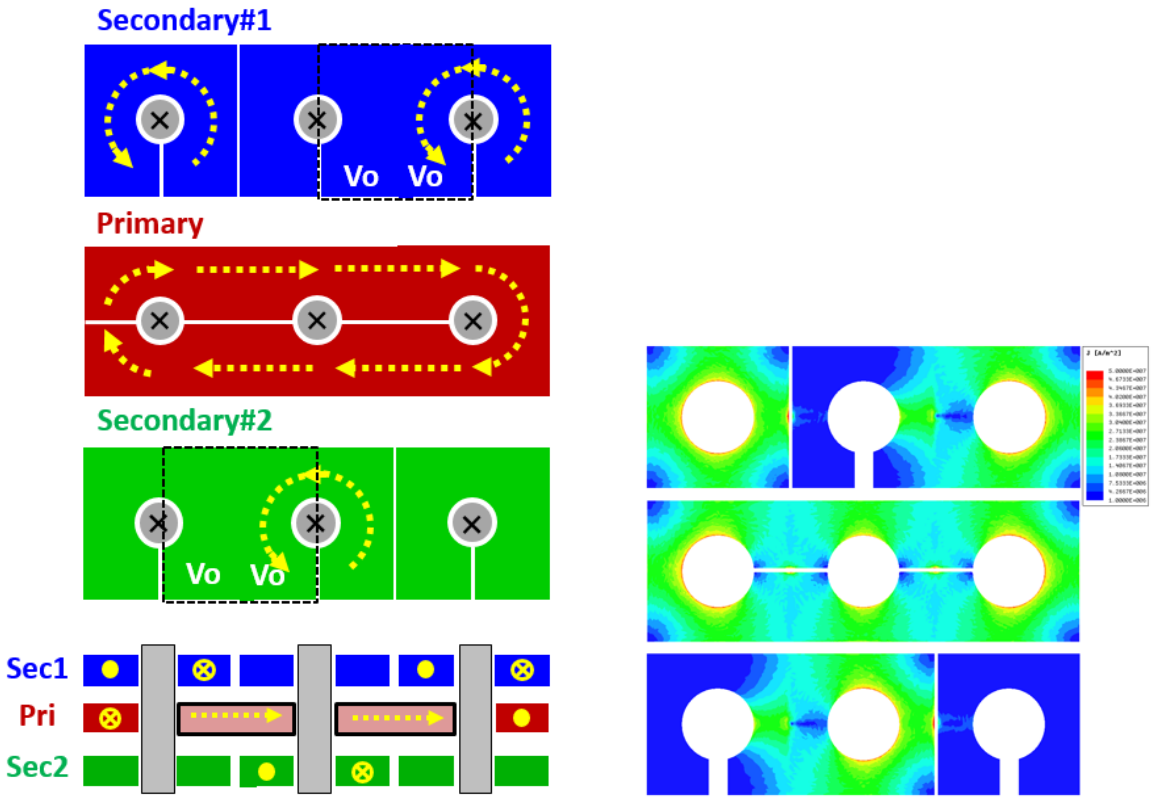


(a) Top view (upper) and cross-section view (lower) of the original winding structure.



(b) Winding current distribution of the original winding structure.

Figure 2.12: PCB winding and current distribution simulation results of the original structure.



(a) Top view (upper) and cross-section view (lower) of the merged winding structure.

(b) Winding current distribution of the merged winding structure.

Figure 2.13: PCB winding and current distribution simulation results of the proposed merged winding structure.

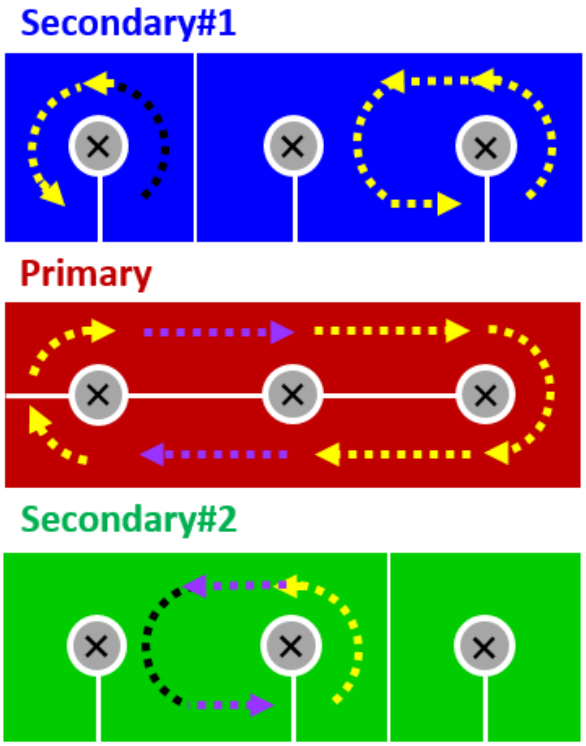
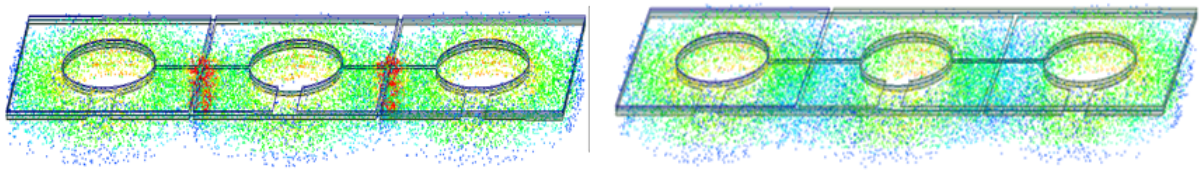


Figure 2.14: New current path in the proposed structure achieving better flux cancellation.



(a) Top view of three transformer integration.

(b) 3D view of integated core with three elemental transformers.

Figure 2.15: H-field comparison of original structure and proposed merged winding structure.

Chapter 3

Transformer Design: Terminations and Vias

3.1 Secondary Termination Design

In Figure 3.1, the secondary AC termination is highlighted in the concept drawing of a matrix transformer, where high AC current flow through. The solid lines are the loop in the positive half cycle and the dashed lines are the loop in the negative half cycle. To connect with SRs

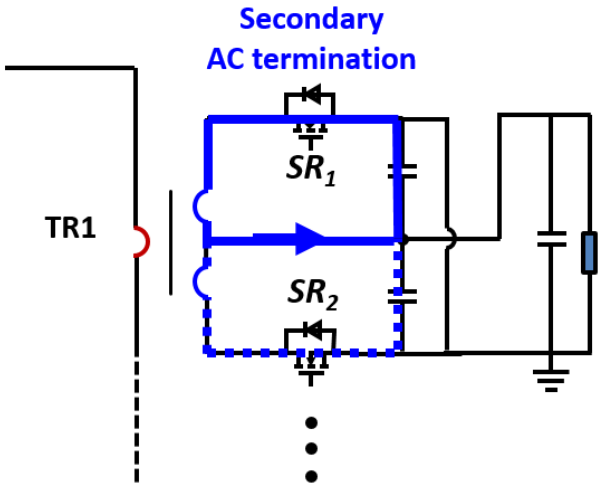
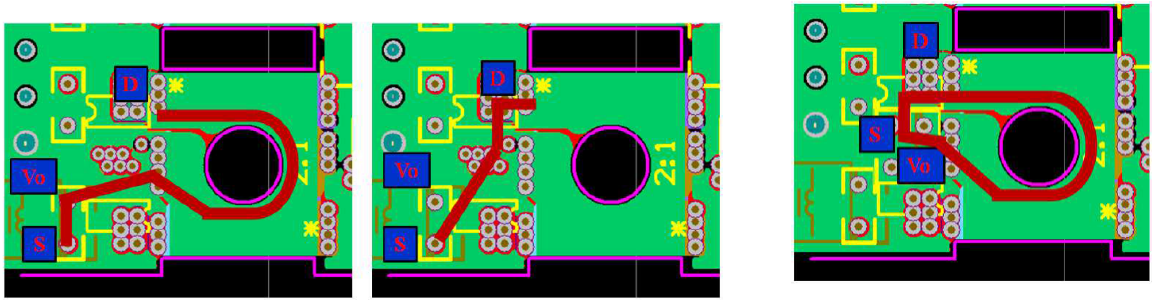


Figure 3.1: Secondary AC termination in a matrix transformer.

and output capacitors, these terminations are usually extended outside the windings, creating a mismatch between primary and secondary windings, which becomes non-interleaved region.

And the current flowing in and out of the terminations are usually not interleaved. Due to the above reasons, in David's work [21], the secondary termination is found to contribute a lot to the total transformer loss and leakage inductance. To reduce the loss, the termination is improved by moving the components in the secondary loop so that the loop becomes smaller. The secondary termination loops before and after the improvement are compared in Figure 3.2. The leakage inductance and equivalent AC resistance are reduced by around 20% with



(a) Original secondary side termination loop.

(b) Improved secondary side termination loop.

Figure 3.2: Secondary termination loop design of matrix transformer

this improvement. However, although it is better than the long loop design, the new design still suffers from high termination loss and leakage inductance. The new secondary winding and termination design is presented in Figure 3.3. Only one elemental transformer is shown for simplicity. The other elemental transformers have the same structure. The arrows in the

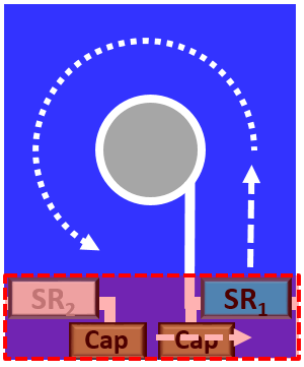
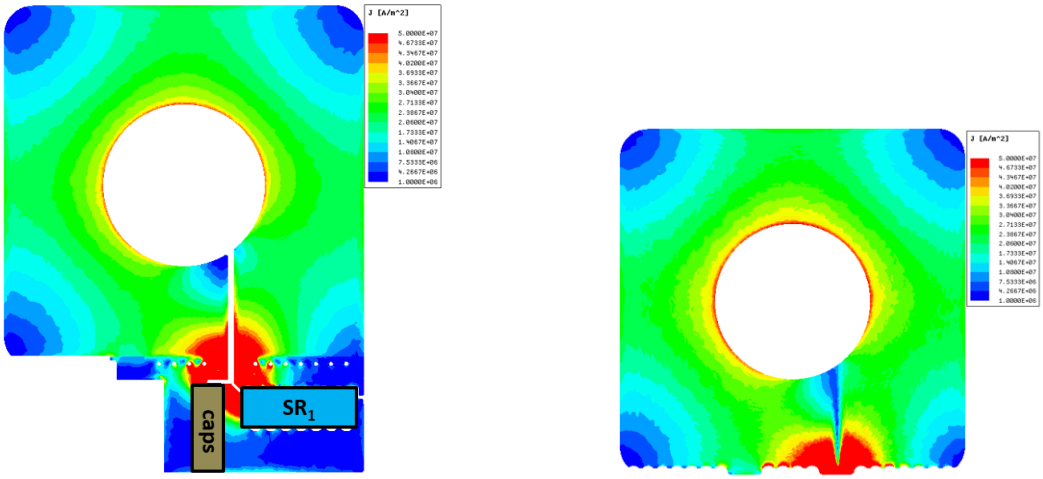


Figure 3.3: Top view of secondary windings and terminations design.

two subfigures indicate the current of the primary half cycle. The red zones in Figure 3.3 are the connections outside the windings, i.e., the AC termination loops. Same as our design, there are also 4 secondary layers in parallel. The parallel secondary winding terminals are connected to the top secondary layer through vias on the two sides of the components. The 3D simulation of this design is done and the current distribution is shown in Figure 3.4. And the H field distribution is shown in Figure 3.11a. Only one layer of four parallel layers are



(a) Current distribution of secondary windings and terminations.

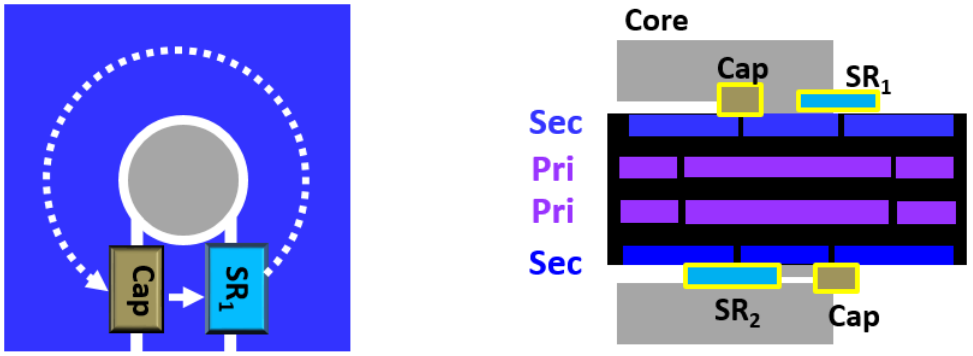
(b) Current distribution of primary windings.

Figure 3.4: Current distribution of the improved design.

shown, but the others are similar. Based on the results, we learn that the AC termination does not only create high current crowding on secondary windings. It also creates high leakage flux around it. This leakage flux in turn creates eddy current on primary windings and thus raising the whole AC copper loss. Moreover, the secondary termination loss itself turns out to be even higher than either primary or secondary winding loss. Therefore, this structure has to be further improved.

In [23], integration concept has been proposed to minimize the secondary termination. It used separate PCBs for different secondary layers. For this kind of structure, the AC termination and vias can be easily minimized by placing devices and components right on

the PCB of each layer. However, it becomes a high profile solution and very complicate for manufacture. Moreover, the terminations are still placed outside the windings which creating the same problem as [21]. In [24], [25], and [26] the integration concept is revisited and improved for low profile PCB-winding design. In [23], the "integration" means integrating SRs and capacitors inside each PCB layer, so that the termination loop is reduced and via connections can be removed. But in [24], the secondary SRs and output capacitors are directly mounted on the secondary windings. They are now integrated with the transformer windings. The structure is presented in Figure 3.5. With this complete integration, all



(a) Top view of the secondary termination structure with components integrated in windings.

(b) Side view of the secondary termination structure with components integrated in windings.

Figure 3.5: Secondary termination structure with components integrated in windings.

the secondary current flow in the complete circular loop that exactly matching the primary windings. The primary and secondary current are interleaved along the whole loop (here we temporarily ignore the primary termination) and the AC termination loops no longer exist on the secondary side. The current flows outside the output capacitors can be seen as DC current and does not create extra AC losses and leakage flux. This concept is easy to implement in [24] and [25] designs because they use only 4-layer PCB in 400V/12V applications. In the 4-layer board, there are two secondary layers and two primary layers. So for each center-tapped termination, there is only one secondary layer. By placing two

secondary windings on top and bottom layers, it is very convenient to do the integration and get rid of the vias. In our design, however, for each secondary termination there are four winding layers in parallel. Vias must be used to connect all the parallel layers. If we directly borrow the design from [25], the termination vias will cut the primary windings [27]. It is possible place vias in a sparse manner so that there is some space for the primary current to flow through. But the equivalent conduction width becomes smaller and current crowding on those areas are inevitable. In addition, it is difficult to parallel devices.

To well apply the integration concept in design where multiple parallel winding layers are used, a novel structure is proposed in [28]. Two non-winding termination layers are added on the top and bottom, as shown in Figure 3.6. Instead of being used as windings, they are

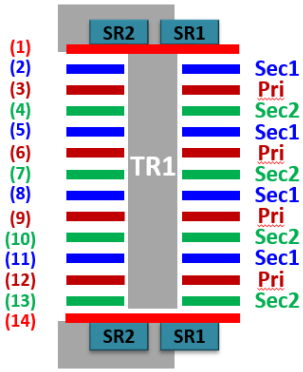


Figure 3.6: Side view of one elemental transformer with top and bottom termination layers and parallel SRs.

just for the connections of all the components. Two parallel devices are placed on the top and bottom layers, overlapping with each other and directly connected through vias. The design structure is presented in Figure 3.7 and Figure 3.8, showing the current in positive and negative half cycle, respectively. Two termination layers share the same layout. Secondary windings #1 conduct during positive half cycle, and secondary winding #2 conduct during negative half cycle. The white dots on the windings represent vias. The current starts from SR1, and flows through vias entering the secondary windings. Then the current completes a

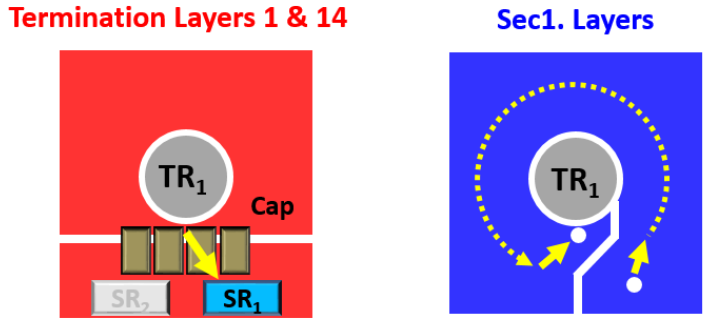


Figure 3.7: Top view of transformer windings with termination layers and current path during positive half cycle.

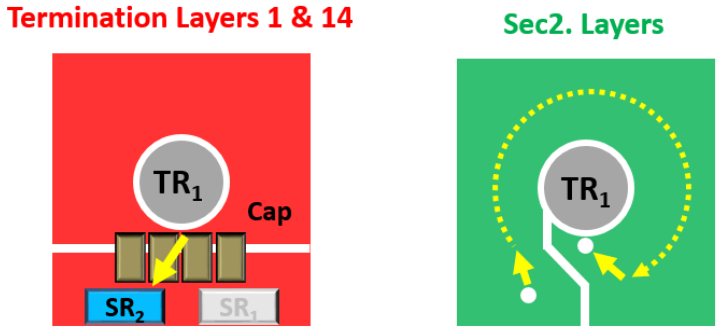


Figure 3.8: Top view of transformer windings with termination layers and current path during negative half cycle.

turn on the secondary windings and going back to top and bottom capacitors through vias. Finally, on the termination layers the current flows back to the SRs. Due to the termination layers, the SRs can be mounted upon the windings and placed with the horizontal direction. There are still some via keep-outs on the primary windings, but due to the horizontal order, the cut-out areas can be easily compensated by extend the winding vertically. In addition, since the SRs are integrated inside the windings, the secondary current loops on windings complete a circle and are well interleaved with primary current. The AC loops are naturally integrated inside the windings, and hence eliminates any extra AC terminations. Due to the symmetrical structure of the secondary side components and connections, the two parallel SRs on top and bottom layers will have good current sharing. And due to the symmetrical

position of SR2 and SR1, the two center-tapped SRs also have good current sharing.

Another benefit of this structure is the capability to mount a large number of output capacitors. In [25], the old integrated termination structure, the space to mount the output capacitors is the winding width. But in the new integrated termination structure, the space expand to the whole elemental transformer width, which is double the winding width plus the diameter of the core. The benefit is clearly illustrated in Figure 3.9. With the same

(a) Output capacitors on the old termination design.

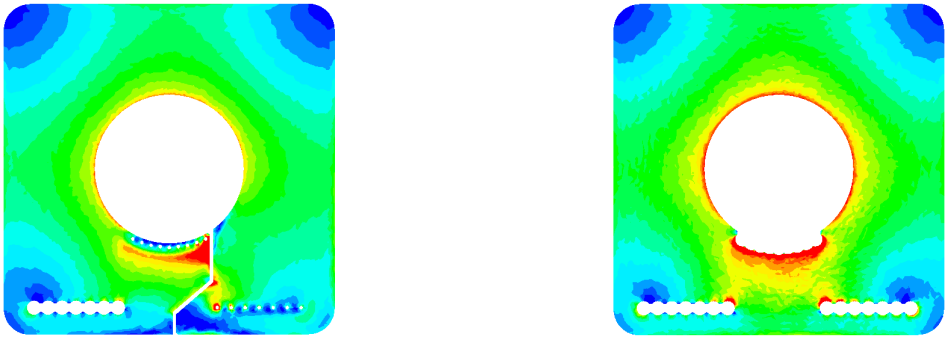
(b) Output capacitors on the new termination design.

Figure 3.9: Comparison of output capacitors on the old and new design.

transformer footprint, the new design allows much more capacitors to be mounted. This becomes very important when the space is not enough for all the output capacitors, as discussed in [25]. Due to the lack of space, some output capacitors have to be placed outside the windings, away from the transformer. The larger these outside capacitors are, the higher AC current will be distributed to the outside large termination loops. And higher loss will be generated. To address this issue, certain capacitance values are combined to minimize the total equivalent AC resistance in [25]. However, this requires the measurement of loop inductance, impedance analysis, and capacitor selection. All these efforts are not good for mass production. This is also true for the old design in [21], where the capacitors is also limited by the termination loss. The more capacitors are mounted, the larger AC termination loop area and the higher termination loss. For the new design, we can easily mount all the

output capacitors inside the windings and all the AC current will be restricted inside the winding loops. So the problem does not exist in the new structure.

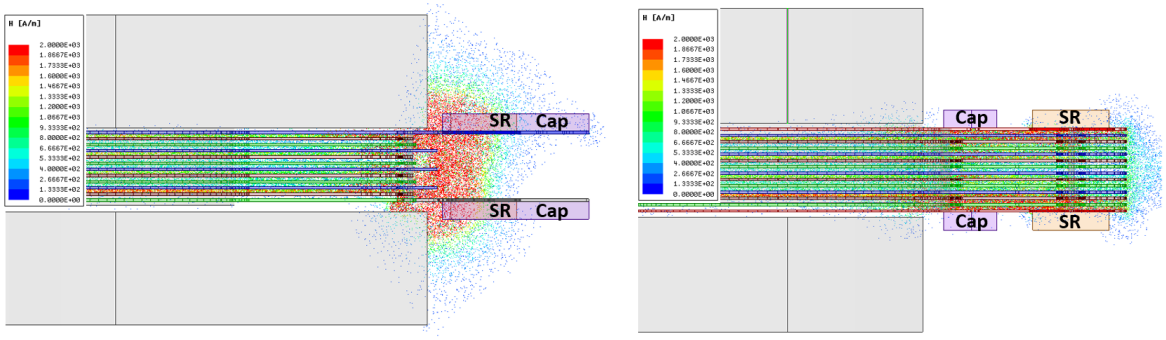
The current distribution of the new design is shown in Figure 3.10. The H field distri-



(a) Current distribution of secondary windings. (b) Current distribution of primary windings.

Figure 3.10: Current distribution of the new design.

bution is shown and compared with the old design in Figure 3.11. The high current crowding



(a) H field distribution of old design with SRs outside windings. (b) H field distribution of new design with SRs inside windings.

Figure 3.11: H field distribution comparison of the old and the new design.

on both secondary and primary windings disappears. The leakage flux is sharply reduced. The loss breakdown of the two termination designs are compared in Figure 3.12. In the old design, the termination loss dominates the total copper loss. The high leakage flux of the termination creates eddy current on both primary and secondary windings. After the

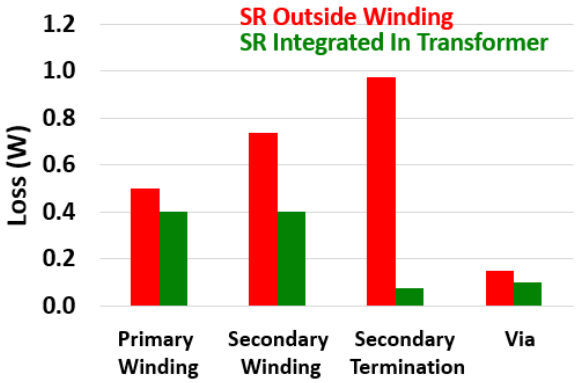


Figure 3.12: Loss breakdown and comparison of the old design and new design.

improvement by [28], the termination loss is reduced by 90% and becomes negligible. And due to the elimination of AC termination loop, the leakage flux is reduced and the secondary and primary winding loss also reduce a lot. The total copper loss is reduced by 60% by this improvement. From this analysis, we learn that the termination design is critical not only because of the termination loss itself, it also impacts the whole transformer AC copper loss. The new structure is directly adopted in our design.

3.2 Primary Termination Design

The primary terminations are highlighted in the circuit diagram in Figure 3.13. Only the primary side circuit is shown for simplicity. The primary termination design was rarely discussed in the literature. In [24, 25, 28, 29], although the transformer design has been studied carefully, none of them mentioned the primary termination. In those applications, the primary side current is usually smaller than 15A RMS. So the loss caused by primary termination is not great. However, in our bus converter, with 36V bus voltage and one thousand watt power, the primary side current becomes much greater RMS current above 30A), which could induce great AC termination loss at high operation frequency. The concept

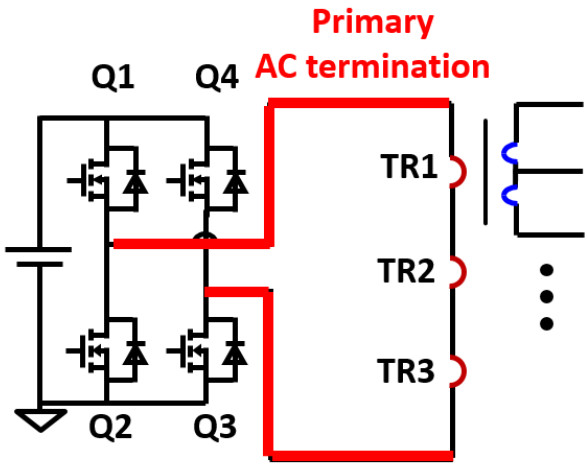


Figure 3.13: Circuit diagram of primary AC termination.

drawings of primary terminal connections are shown in Figure 3.14. In the figure, the yellow

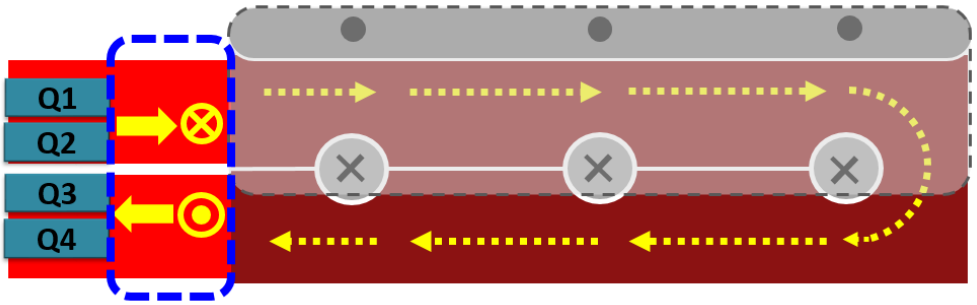


Figure 3.14: Concept PCB layout of primary AC termination and vias.

arrows and dots and crosses indicate the current. The gray area and black dots and crosses represent the core and its flux. Since all the primary devices are on the top layers. The current flowing out of the switch node of one half-bridge (Q1 and Q2) has to go through vias to enter the four primary windings. After the current finishing the turn of three core posts, it comes back and again go through vias to the top layer. And then it flows back to the switch node of the other half-bridge Q3 and Q4). All these terminal connections and vias carrying AC current, as circled in the blue box in the figure, need to be analyzed carefully.

Similar to the secondary termination, primary termination also has the two problems mentioned in the secondary termination discussed in the previous section. First, to connect the windings with the external circuit, e.g., full-bridge network in this case, the terminations need to extend outside the windings. It is usually realized by making a cut in the windings, allowing the current to flow in and out of the windings. As a result, the current on the windings no longer complete a full circle and the non-interleaving areas appear on the windings. Figure 3.15 illustrates an elemental transformer with conventional primary termination design. The region 1 in the figure demonstrates the first problem. Due to the cut and external connections, the current in region 1 flowing in opposite directions and do not overlap the secondary windings. The opposite current flow side by side will attract each other and create high current crowding on these primary windings. Moreover, the non-interleaving in region 1 also creates high current crowding on the secondary windings. The second problem happens

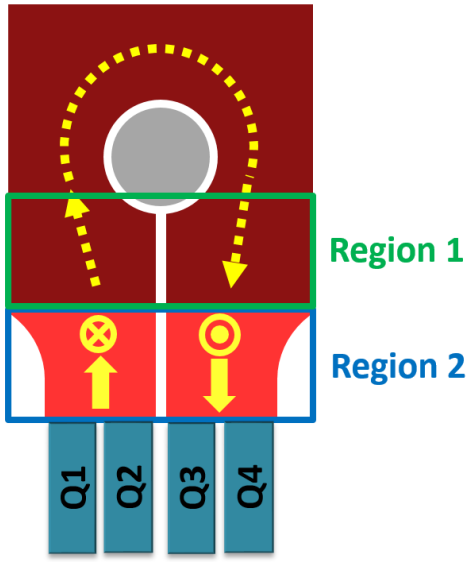
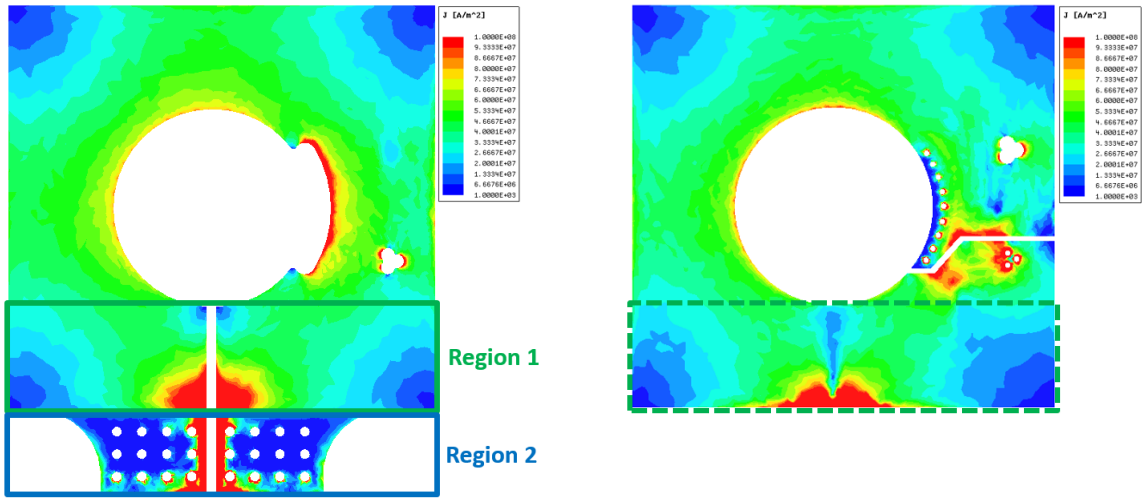


Figure 3.15: Primary AC termination and high loss regions of one elemental transformer.

in region 2 in Figure 3.15. In the conventional design, the two terminal connections of the windings are placed side by side, with opposite current flowing through. As addressed in region 1, this structure would suffer from high AC ohmic loss. And similar as the secondary

termination, it is not only important for its own loss but also impacts the whole windings through leakage flux. From FEA simulation, the current distribution results are obtained and presented in Figure 3.16. The current crowding appears in the regions we expected.



(a) Current distribution of primary windings and terminations. (b) Current distribution of secondary windings.

Figure 3.16: Current distribution of windings and terminations of conventional termination design.

In region 1, the current attracting each other and concentrates in the middle area. This is known as the proximity effect. This current crowding reflects to the secondary windings due to the non-interleaving structure. In region 2, the similar current attraction exists and high current crowding is observed. It also creates eddy current and impacts the current distribution on primary and secondary windings through leakage flux. A side effect of this current crowding is the bad via utilization. Because the current on the termination only concentrate to a small area in the middle. The vias placed on the other areas see few amount of current. In other words, these vias are not utilized to carry current and thus wasted. The current distribution of primary vias are shown in Figure 3.17. The vias on the current crowding area (circled in the red box) on the termination carry most of the current. Half of the vias carry only a very small amount of current. The poor via utilization is harmful in

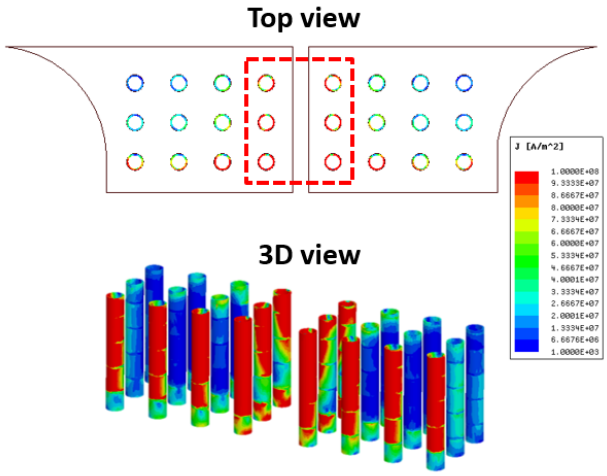


Figure 3.17: Top view and 3D view of current distribution of primary vias.

two aspects and should be improved. First, it means less paralleled vias and hence more via loss. Second, higher equivalent via impedance makes it harder for current to flow through the low winding layers. So the current sharing of the parallel primary windings on lower layers becomes worse. Therefore, the via utilization becomes the third problem that needs to be considered for the termination design. Both region 1 and region 2 create high leakage flux due to non-interleaving. These flux, in turn, create high eddy current loss on coppers. The H field distribution is shown in Figure 3.18. As a summary, the three major problems

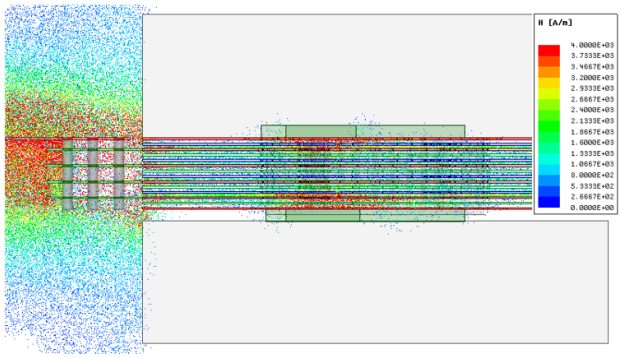


Figure 3.18: H field distribution of the conventional termination design.

are listed as follows.

1. Non-interleaved current within the windings (region 1 in Figure 3.16).
2. AC loss and leakage flux of terminations outside windings (region 2).
3. Via utilization.

The first problem would be very difficult to solve, as long as the external circuit, e.g., full-bridge network in this case, has to be placed outside the windings. The integration concept in the last section can perfectly solve this problem. However, it requires a very simple circuit loop so that all the components in the loop can be physically placed inside the transformer windings. This is achievable in secondary rectifier networks but is not possible for the primary side, where there are too many components including the full-bridge devices, resonant capacitors, and input capacitors. The only possibility would intentionally increase the size of the transformer and its windings. However, it counteracts the benefits of matrix transformer structure. As a result, we have to leave a cut on the windings and this part of the loss is inevitable. The second problem, however, can be improved. As discussed above, the terminations are usually extended outside the windings, creating a mismatch between primary and secondary windings, which becomes non-interleaved regions. And the current flowing in and out of the termination are usually arranged side by side in the same layer and thus not interleaved. Although these AC terminations are unavoidable, we could try to interleave them to reduce the leakage flux and AC losses. If by interleaving the terminations, we can achieve good current distribution on terminations, the third problem, via utilization could be naturally solved.

First, before the current gathers to enter the devices, we use four parallel layers to distribute the current. The task becomes how to interleave these four parallel layers. Illuminated by the interleaving structure of transformer windings, a new structure is proposed in new design #1 where the termination current are interleaved. The new design is illustrated in Figure 3.19. The current from devices enters the top layer and flows to the four primary

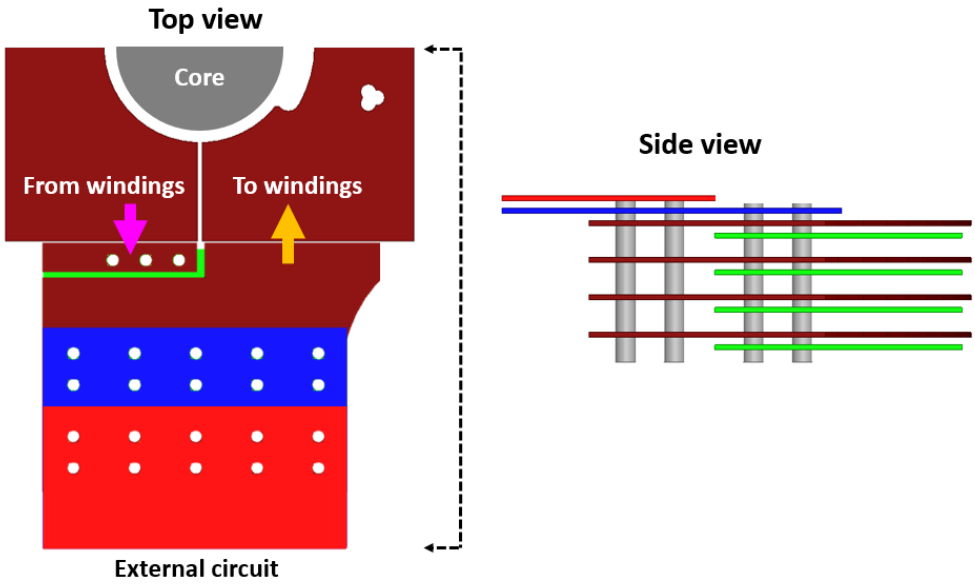
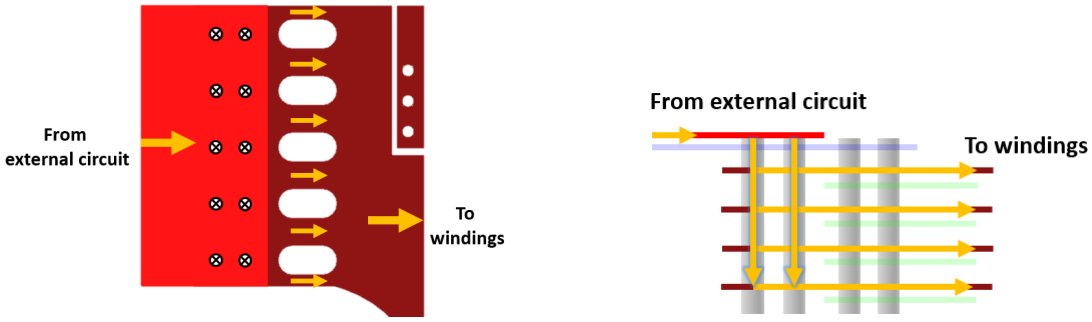


Figure 3.19: Proposed new design 1 for primary termination and via structure.

layer terminations through vias. On the four termination layers, the current continues to flow and to the four primary windings. This process is illustrated in Figure 3.20. Only



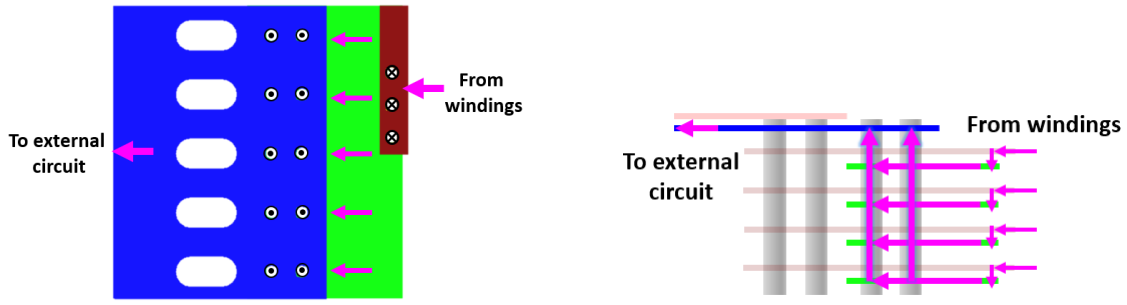
(a) Top view of termination current entering the windings.

(b) Side view of termination current entering the windings.

Figure 3.20: Termination current entering the windings of proposed design 1.

the top layer and one of the primary layers is shown so the current flow can be identified more clearly. After the current finish the winding turns, it returns and through a small connection outside the windings, flows through the vias on the small connection. These vias guide the current to the layer beneath each primary winding layer, which is the green layer.

The green layer is called "auxiliary termination layer" because this termination is used as the current return path. Although it shares the same layer as secondary windings, they are not connected electrically. The current enters the auxiliary termination and continues to flow untill it meets the vias connected to the second layer (blue layer). Then all the four parallel current gather on the blue layer through vias and flow to the devices. This process is illustrated in Figure 3.21. Again, only the small outside winding connection, one of the



(a) Top view of termination current leaving the windings.

(b) Side view of termination current leaving the windings.

Figure 3.21: Termination current leaving the windings of proposed design 1.

green layers, and blue layer are shown so the current flow can be identified more clearly. The termination current of both directions are shown in Figure 3.22. It is clear that in

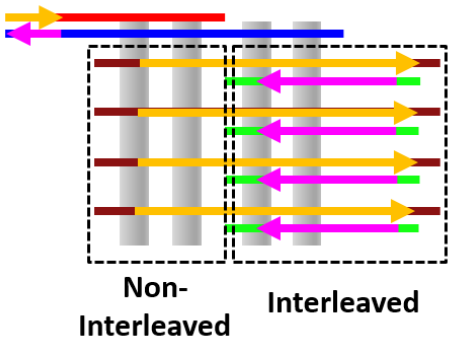


Figure 3.22: Termination current of proposed design 1.

the right boxed region the termination current are interleaved in a similar manner as of the interleaving we have for transformer windings.

The current distribution of the termination is presented in Figure 3.23. Only the ter-

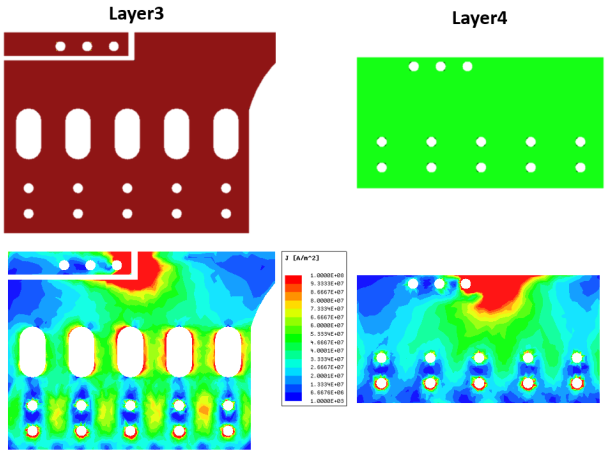


Figure 3.23: Termination current distribution of proposed design 1.

mination part is shown. The current distribution on the windings is very similar to the conventional design since the problem on region 1 remains. However, the current crowding in region 1 becomes a little bit smaller because the impact of termination leakage is reduced. Comparing Figure 3.23 with Figure 3.16a region 2, the current distribution becomes much better. There are still some current crowding near the windings. This is the extension of the opposite current in the windings and cannot be avoided. However, it is alleviated in this design by minimized the connections outside the windings. Here only a small portion is left for via connections. The H field distribution is shown in Figure 3.24. The leakage flux is

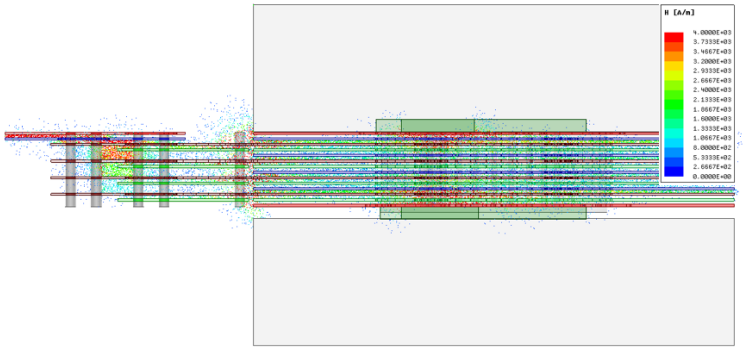


Figure 3.24: H field distribution of proposed design 1.

significantly reduced compared with the conventional design in Figure 3.18. However, there are still some high leakage flux left in the non-interleaved region specified in Figure 3.22. To further improve the structure, we need to fully interleave all the termination. After analyze problem 2, problem 3 needs to be examined. The via current distribution is presented in Figure 3.25. The via utilization becomes much better compared with Figure 3.17. However,

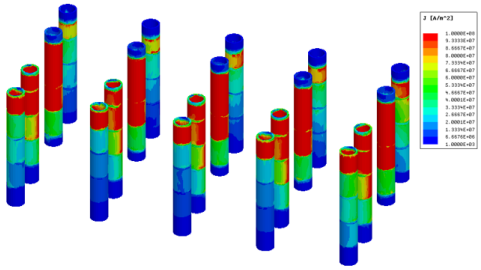


Figure 3.25: Via current distribution of proposed design 1.

there are still half of vias carrying much smaller current than the others. The reason can be explained by Figure 3.26. The current flowing up and down through the vias also have

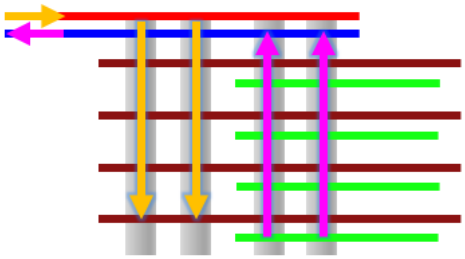


Figure 3.26: Via current flow of proposed design 1.

proximity effect. The current are attracted to the middle two rows of vias, causing uneven distribution among vias, as observed in Figure 3.26. To further improve the via utilization, we can interleave the vias as well.

In design 1, the termination are interleaved laterally. Similarly, the via current can be interleaved vertically. In the end, we find out that once the vias are interleaved, the non-

interleaved regions of terminations are eliminated at the same time. Based on this idea, the new design 2 is proposed and shown in Figure 3.27. The vias are arranged in a finger-shaped

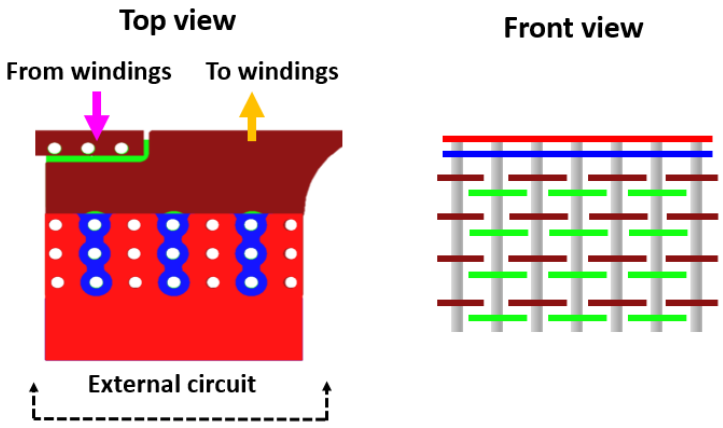
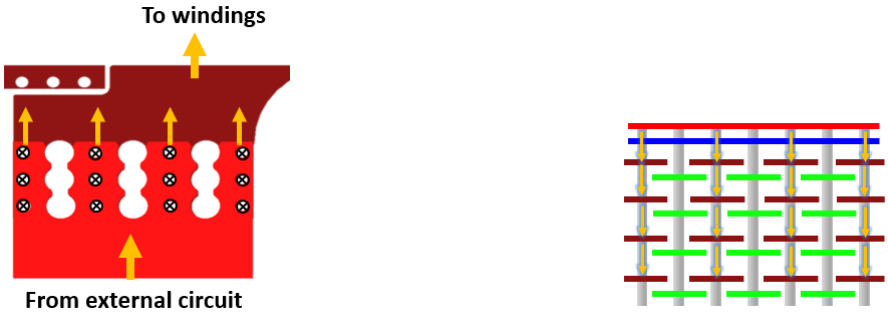


Figure 3.27: Proposed new design 2 for primary termination and via structure.

manner so that the via current are interleaved vertically. The current from devices enters the top layer and flows through part of the vias to the four primary layer terminations, as shown in Figure 3.28. After the current finish the winding turns, it returns and flows to



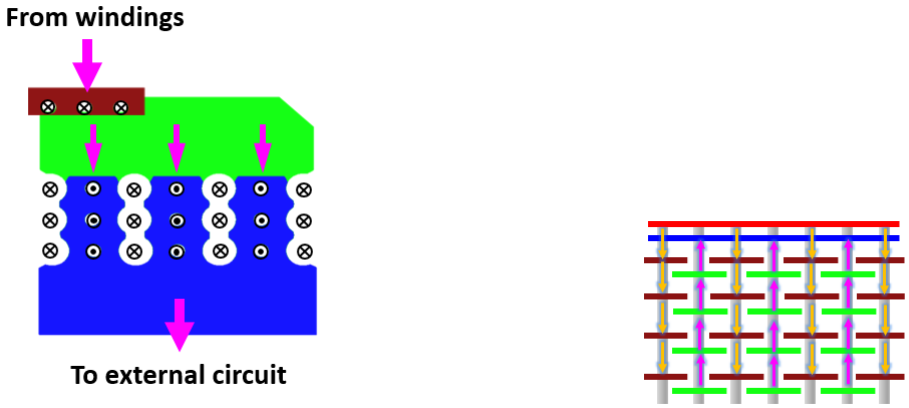
(a) Top view of termination current entering the windings.

(b) Front view of termination current entering the windings.

Figure 3.28: Termination current entering the windings of proposed design 2.

the auxiliary termination through the small connection and vias. This process is the same as design 1. Next, the current continues to flow on the auxiliary termination and then goes to the blue layer through the other groups of vias. This process is shown in Figure 3.29.

Finally, the via current interleaving can be clearly observed in the front view. The via current



(a) Top view of termination current leaving the windings.

(b) Front view of termination current leaving the windings.

Figure 3.29: Termination current leaving the windings of proposed design 2.

distribution is shown in Figure 3.30. The current distribution becomes better then design 1

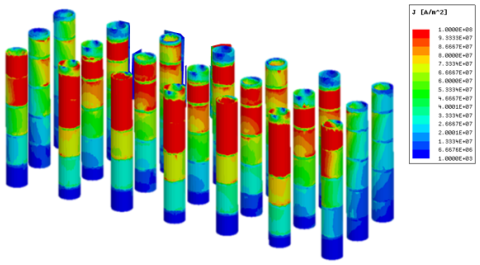


Figure 3.30: Via current distribution of proposed design 2.

thanks to the interleaving structure.

The terminations are still interleaved in the same way as design 1. The only difference is that the terminations are completely overlapped and interleaved due to the new via arrangement. The side view of termination current is shown in Figure 3.31. The current distribution of terminations are shown in Figure 3.32. Similar as design 1, they have good current distribution. The termination area can be separated into two regions: termination 1 and termination 2. In termination 1 is not interleaved. The termination 2 is fully interleaved.

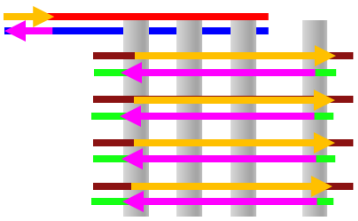


Figure 3.31: Termination current of proposed design 2.

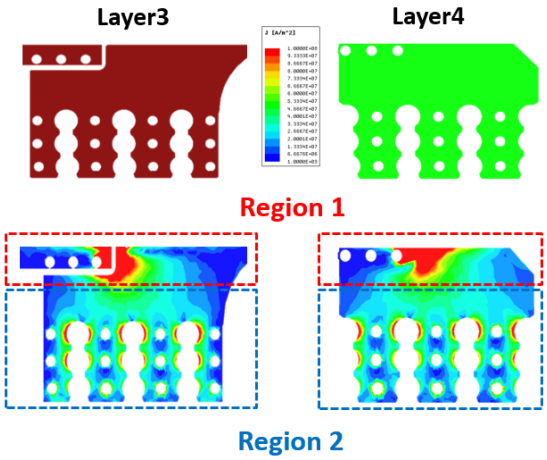


Figure 3.32: Termination current distribution of proposed design 2.

The loss breakdown of the termination regions are shown in Figure 3.33 and compared with the corresponding two regions in the conventional design. Compared with the old design, the new design has a little smaller loss on termination 1 but much lower loss on termination 2. It is clear that the interleaving structure reduces much loss. After the improvement, the loss on non-interleaved termination 1 becomes dominant. Design 1 is not shown since it is very similar as design 2. The H field distribution is shown in Figure 3.34. The leakage flux in design 1 which is caused by non-interleaved vias and partially interleaved terminations are minimized in design 2. The loss breakdown of the three designs are compared in Figure 3.35. For a fair comparison, the via number used is the same for the three designs. For design 1, the via loss is reduced due to the better current distribution on terminations. For design 2, the via loss is further reduced due to the proposed interleaving structure. The termination

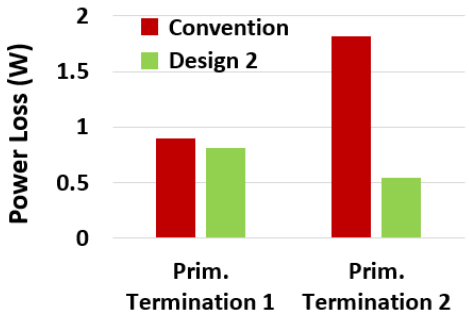


Figure 3.33: Primary termination loss breakdown of conventional design and new design 2.

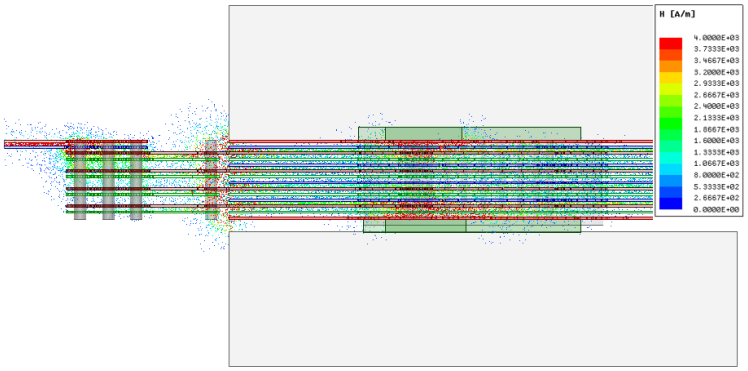


Figure 3.34: H field distribution of proposed design 2.

width in the three designs is also kept the same for a fair comparison. The termination loss is significantly reduced in design 1 and 2 due to the interleaving of the terminations. In the conventional design, the termination loss cannot be reduced by increasing the width due to the proximity effect. In design 1 and design 2, however, because the current distribution becomes good, the conduction loss can be further reduced by increasing the width. In design 1, the termination leakage flux is significantly weakened by the interleaving. This not only reduces the termination loss but also reduces the eddy current on the windings. Therefore, the winding losses are also reduced in design 1. In design 2, due to the further reduction of leakage flux, the terminations also benefits from smaller AC losses. As a summary, the proposed design achieves interleaving for both vias and terminations in both vertical and lateral directions, which minimizes the leakage flux and AC losses.

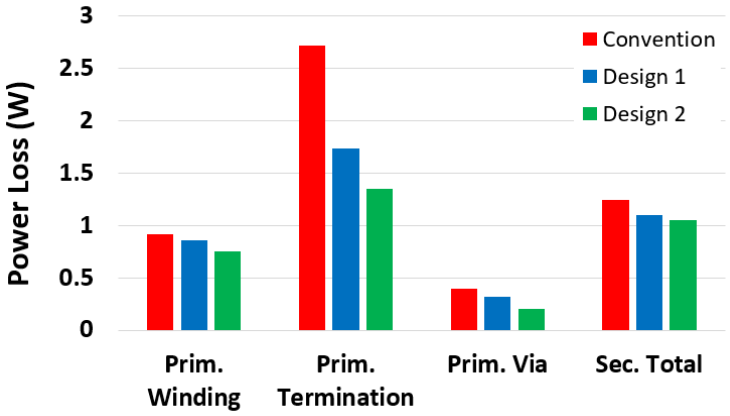


Figure 3.35: Transformer copper loss breakdown comparison of conventional design and two proposed new designs.

Chapter 4

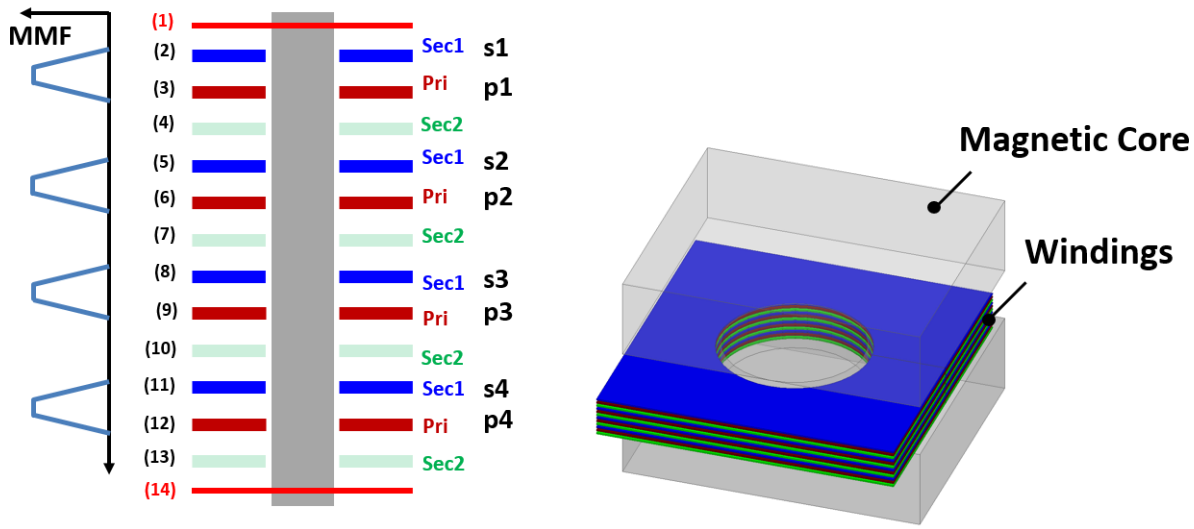
Transformer Design: Current Sharing of Parallel Layers

4.1 Introduction

To minimize the transformer conduction loss, it is important that the current distribution is uniform across all the windings so that all the copper are well utilized. The merged winding method proposed in chapter 2 reduces the current crowding and ensures a good current distribution on every single layer of winding. The interleaved termination and via structure proposed in chapter 3 not only reduces the conduction loss and leakage inductance created by the terminations and vias but also achieve a better utilization of the vias. However, as discussed before, there are four paralleled layers for each winding. To well utilize these layers, good current sharing among them is also critical. In the parallel winding structure, the conventional 1-D analysis [30] which assumes serial connections is no longer valid. The layer arrangement is found to have a very important effect on the current distribution and loss. It can be demonstrated with our design with the original layer arrangement.

First, we still use one elemental transformer for simplicity. The 3D model, the layer arrangement (cross-section view) and its magneto-motive force (MMF) is shown in Figure 4.1. Here only the middle twelve winding layers (layer number 2 to layer number 13) are presented. Note that this is a fully interleaved arrangement. Ideal windings are used in the

model with no termination or vias. An external circuit is used for the current excitation of windings. Figure 4.2 shows the concept drawing of the external circuit used. We simulate the positive half cycle where secondary winding #1 conducts. Ignoring the magnetizing inductance, the current source on the primary I_{prim} and secondary side I_{sec} has the same value. By using ideal windings and parallel layers through the external circuit, the impact of terminations and vias are decoupled. The simulation results are shown in Figure, where the percentage on each layer of winding indicates the current distribution ratio. Similarly, we can do the simulation for the negative half cycle when the secondary winding #2 conducts. The results are shown in Figure 4.3. It is clear that even with a fully interleaved layer arrangement, the current distribution is not uniform. It means that even we have good terminations and vias design so that the via impedance is negligible, the current still tend to have an uneven distribution, which causes higher conduction loss and uneven thermal stress.



(a) Layer arrangement and MMF of original transformer winding design.

(b) 3D model of original transformer winding design.

Figure 4.1: Original transformer winding arrangement.

If we go back to the equivalent circuit, there are two things we ignored. First, although the DC winding resistances of each layer are identical due to the same winding structure,

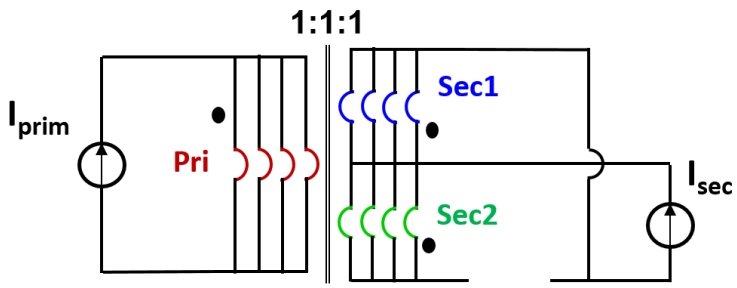
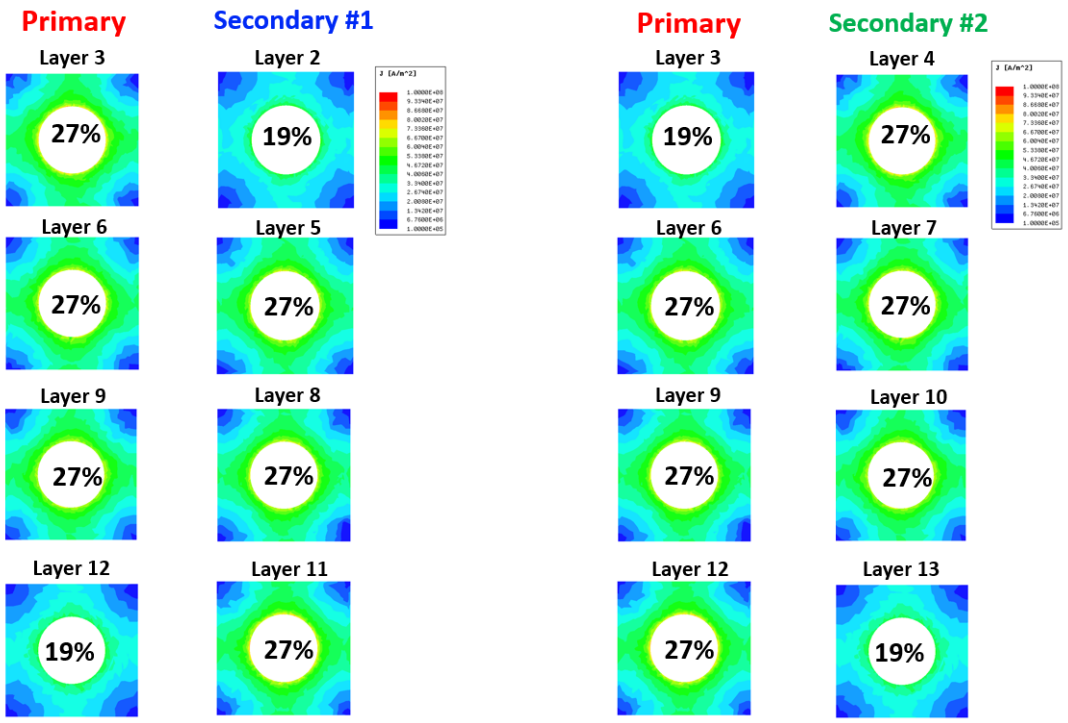


Figure 4.2: External circuit of original winding arrangement.

the AC resistance, which is determined by the skin effect and proximity effect, may not be the same. Second, the leakage inductance of each layer, which is influenced by the electromagnetic field distribution, can also be different. Therefore, we could have different impedance on each layer and hence a non-balanced current distribution. Since these two factors are both related to the electromagnetic field distribution, the circuit model is not adequate for the analysis. Based on the simulation, we learn that the current distribution is related to frequency, layer copper thickness, layer distance (FR-4 thickness), and layer arrangement. So now the question is whether there is a simplified model that can be used to predict the electromagnetic field and current distribution, like the well-known 1-Dimension (1-D) model [30, 31, 32] which is used in transformer structures where both primary and secondary windings are in series.

This problem was noticed in planar magnetics in [33]. Some basic analysis are performed on this issue in [33, 34, 35] and some experimental guidelines according to a number of simulation examples are summarized. But they are completely simulation-based, which is time-consuming and non-convenient for iterative design and analysis. It also lacks physical meanings or intuition. [36] proposed application of the extremum co-energy principle for calculation and prediction of the current distribution and resulting AC resistance. It was verified by the experiments. However, it did not consider the frequency effect on the current distribution results. An analytic model based on Faraday's law and voltage balance was pro-



(a) Current distribution of positive half cycle. (b) Current distribution of negative half cycle.

Figure 4.3: Current distribution of original transformer winding arrangement.

posed in [37]. This model well predicts the AC winding resistance of a wide frequency range. An example of 8:1 transformer with primary windings in series and two secondary windings in parallel is presented to verify the calculation. However, the problem with this approach is that the equations become very complicated when applied to transformer structure with more number of parallel layers, e.g., four parallel primary windings and four parallel secondary windings in our case. Also [37] only showed the concept and two key equations. More detailed works are required if we want to apply this model to a general transformer winding structure.

To study this issue in detail, we will first use the concept proposed in [37] to analyze the problem. And then a simplified method using superposition concept is proposed. It makes some assumptions during the simplification, but these assumptions are satisfied in the

practical design of PCB-winding planar transformer. The method can be easily extended to a larger number of parallel windings and is verified by FEA simulation with two examples.

4.2 Analytic Model for Parallel-Winding Transformer

The method proposed in [37] is still based on the basic 1-D model [30, 32]. So we will first go through the 1-D electromagnetic analysis of the transformer and then introduce the parallel-winding model. In the following analysis, we assume that the electromagnetic field is magneto-quasi-static (MQS), which means the displacement current can be ignored. MQS assumption always holds for most of the power electronics applications [38]. We also assume the field is one dimensional, which means the field strength is constant across the breadth of the winding and changes only along the thickness of the winding [30].

In Dowell's 1-D model [30], an additional assumption is that the primary and secondary windings are both in series. So the current in windings is known and can be used to solve for field distributions. The first step is to solve the J (current density) field in windings. Based on MQS and Maxwell equations, the J field satisfies the following second-order differential equation in the frequency domain:

$$\frac{d^2J}{dx^2} = \alpha^2 J \tag{4.1}$$

$$\alpha^2 = \frac{j\omega\mu_0\eta}{\rho} \tag{4.2}$$

where ω is the frequency, μ_0 is the magnetic permeability of air, and η is the compensation factor for the "layer porosity". For our case where each layer has one turn of winding and the winding fills the whole window area of the core, this factor equals to one. ρ is the resistivity of the conductor, which is copper in this case. X-axis is along the thickness of the winding.

The solution is:

$$J = P\cosh\alpha x + Q\sinh\alpha x \tag{4.3}$$

To solve this equation, two boundary conditions are needed to solve for P and Q. The first boundary condition can be easily obtained based on the knowledge that the integration of J upon the cross-section area of the winding is the current flowing through the winding.

$$\int_0^h \eta J b dx = NI \tag{4.4}$$

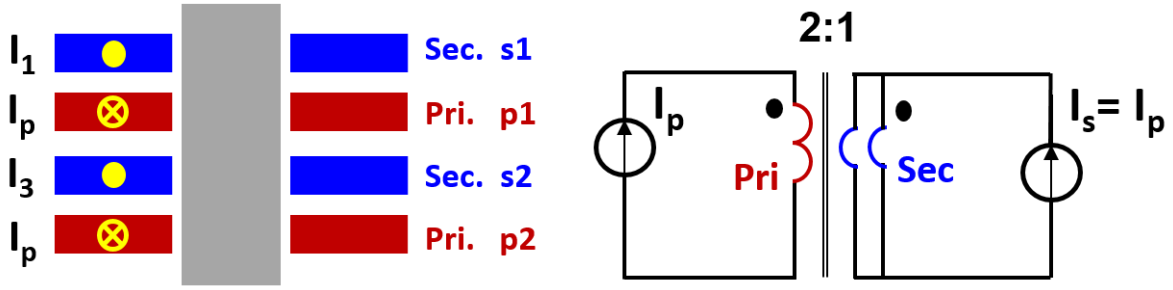
where b is the winding width, h is the thickness of the winding layer and N is the number of turns per layer, which is one in our case. Note that despite the fact that this relationship is always valid, we cannot directly use this equation for boundary condition in parallel-winding case, where the current in each parallel winding is unknown. The other boundary condition used is a Neumann condition:

$$\frac{dJ}{dx} = \frac{j\omega\mu_0}{\rho}\{\frac{IN(p-1)}{b} + \eta\int_0^x Jdx\} \tag{4.5}$$

If we start from the zero MMF position to count layers. The pth layer is the layer where we calculate the J distribution. p always equals zero in a fully interleaved winding structure. The MMF only accumulates within one layer. This equation can be derived by the integral form of Faraday's law, as presented in [30]. After J field is solved, the voltage can be obtained by Ohm's law and Faraday's law. From the voltage across the winding, the AC resistance and leakage inductance information can be extracted. Derivation details can be found in [30] and are not discussed here.

From the previous analysis, we learn that the key to solving the field is the two boundary conditions. In Dowell's model, they are readily obtained because the current I is a known parameter under its series assumption. In parallel-winding case, however, this assumption is

no longer valid. Now all the current term in the two boundary equations becomes unknown variables. As the number of unknowns is increased, more equations are required. One apparent equation is based on Kirchhoff's current law, the summation of the current is the total current on primary or secondary. But one additional relationship is not enough. Consider a simple case where primary windings are in series, and two layers of secondary windings are in parallel, as shown in Figure 4.4.



(a) Cross-section view of the layer arrangement for the given example transformer.

(b) Equivalent circuit the given example transformer.

Figure 4.4: Transformer structure and equivalent circuit of the given simple example.

Each winding has one turn on each layer. For the primary windings, we know the current I_p due to the serial connection. For the secondary windings, the current on layer 1 I_1 and layer 3 I_3 are two unknowns. Ignoring the magnetizing inductance, we have

$$I_1 + I_3 = I_p \tag{4.6}$$

For another equation, [37] select a loop between the two secondary windings (layer 1 and 3). The loop is shown in Figure 4.5 by the dashed circle. The blue and red boxes are partial cut of the secondary and primary windings.

Due the parallel connection of layer 1 and 3, the loop is electrically connected. Therefore, the voltage induced by the flux through the loop plus the resistive voltage drop along the

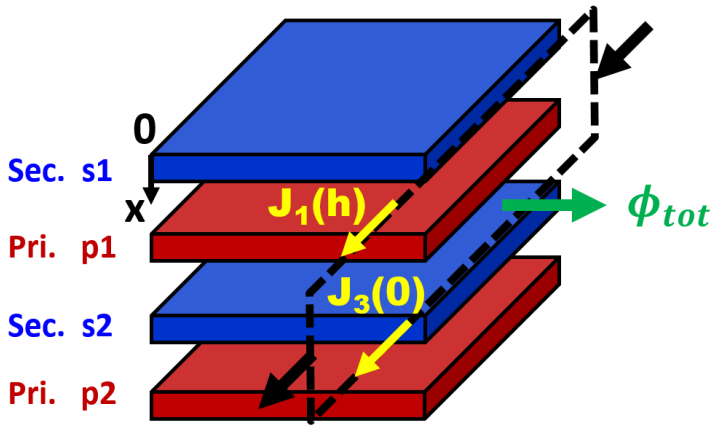


Figure 4.5: Detail structure of the transformer example for analytic model.

windings on the loop should be zero. The directions are determined by the Lenz's law.

$$\rho(J_1(h) - J_3(0))l + j\omega\Phi_{tot} = 0 \tag{4.7}$$

where $J_1(h)$ and $J_3(0)$ are current density at the bottom position of layer 1 and top of layer 3, respectively. Φ_{tot} is the total magnetic flux passing through the loop. l is the length of the winding. Relationships developed in previous Dowell's model can be applied here. To use Dowell's model, first we set the top of layer 1 to MMF starting point. From equations (4.3), (4.4), and (4.5),

$$J_i = P_i \cosh \alpha x + Q_i \sinh \alpha x \quad \text{for} \quad i = 1, ..., 4 \tag{4.8}$$

$$\int_0^h J_1 b dx = I_1 \tag{4.9}$$

$$\int_0^h J_3 b dx = I_3 \tag{4.10}$$

$$\int_0^h J_2 b dx = I_p \tag{4.11}$$

$$\int_0^h J_4 b dx = I_p \tag{4.12}$$

$$\frac{dJ_1}{dx} = \frac{j\omega\mu_0}{\rho}(\int_0^x J_1 dx) \tag{4.13}$$

$$\frac{dJ_2}{dx} = \frac{j\omega\mu_0}{\rho}(-\frac{I_1}{b} + \eta\int_0^x J_2 dx) \tag{4.14}$$

$$\frac{dJ_3}{dx} = \frac{j\omega\mu_0}{\rho}(\frac{I_1 - I_p}{b} + \eta\int_0^x J_3 dx) \tag{4.15}$$

$$\frac{dJ_4}{dx} = \frac{j\omega\mu_0}{\rho}(\frac{-I_1 + I_p - I_3}{b} + \eta\int_0^x J_4 dx) \tag{4.16}$$

where i indicates the number of layer counting from top. The Φ_{tot} in equation (4.7) includes the flux in the gap between two layers and the flux in layer 2.

$$\Phi_{tot} = \Phi_{12} + \Phi_{23} + \Phi_2 \tag{4.17}$$

The field strength in the interlayer gaps is given by [30]

$$\begin{aligned} H_{12} &= \frac{I_1}{b} \\ H_{23} &= \frac{I_1 - I_2}{b} \end{aligned} \tag{4.18}$$

Hence the magnetic flux in the inter-layer gaps is

$$\begin{aligned} \Phi_{12} &= \mu_0 r l \frac{I_1}{b} \\ \Phi_{23} &= \mu_0 r l \frac{I_1 - I_2}{b} \end{aligned} \tag{4.19}$$

where H_{12}, H_{23}, Φ_{12}, and Φ_{23} are the field strength and flux in the interlayer gap between layer 1 and layer2, and layer2 and layer 3, respectively. r is the distance between two layers, which is usually the FR-4 insulation thickness in PCB windings. The flux in layer 2 Φ_2 can

be obtained from equation (35) in [30]

$$\Phi_2 = \mu_0 l \int_0^h (-\frac{I_1}{b} + \eta \int_0^x J_2 dx) dx \tag{4.20}$$

Substitute equations (4.17), (4.19), and (4.20) in equation (4.7) yields

$$\rho(J_1(h) - J_3(h)) + j\omega(\mu_0 r \frac{2I_1 - I_2}{b} + \mu_0 \int_0^h (-\frac{I_1}{b} + \eta \int_0^x J_2 dx) dx) = 0 \tag{4.21}$$

Combine equations (4.6), (4.21), and (4.8) – (4.16), we have 14 equations, and and 14 unknowns: I_1, I_3, J_i, P_i, Q_i $(i = 1, ..., 4)$. Solving these equations we can get the J field in each winding, and following the similar procedure before we can get the current and voltage of the windings. However, even for a simple two-layer parallel structure, this approach requires the solution for 14 differential equations with double integral. In [37], Visual-Basic codes are built to solve this problem. For more complex structure where both primary and secondary windings are in parallel, and more parallel layers are used, the equations are expected to become even more complicated. For a structure with n parallel primary and n parallel secondary layers, 8n equations with 8n unknowns are to be built. Since now the current on each winding is unknown, the MMF distribution also becomes unknown. The only known zero MMF position is the top or the bottom of the windings. Therefore, the "winding portion" concept in [30] does not apply here and the calculation has to be done on the whole windings. For example, for the bottom layer, all the layer current above needs to be considered in the boundary condition, which makes the equations filled with double integrals and differential operations. In a word, the method requires the establishment of a large number of complex equations. And solving the equations takes much time and effort.

4.3 Simplified Model Using Superposition Method

To simplify the previous model, reduce the calculation burden, and gain some physical intuitions, a simplified model using superposition method is proposed. First, two simple structures are studied. Then based on superposition concept, these two structures serve as the building blocks for multi-layer parallel winding structures. When analyzing the structures, we still use the MQS and 1-D assumptions. The first building block structure is shown in Figure 4.6. It has one turn for the primary side winding, and two turns in parallel for

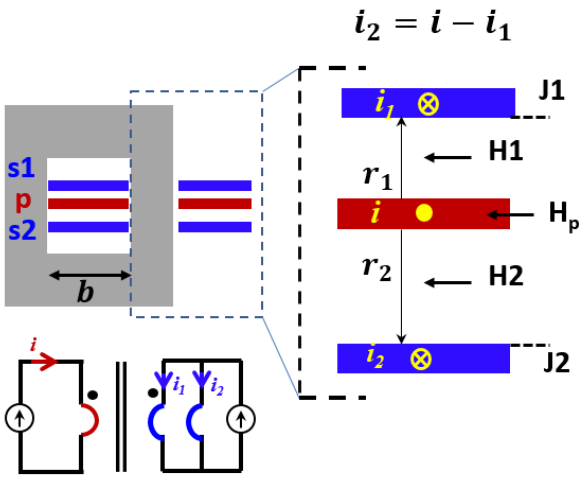


Figure 4.6: Transformer structure and equivalent circuit of the first building block.

the secondary side windings, both around the same core. Suppose we know the primary side current. And ignoring the magnetizing current, we also know the secondary side total current. The goal is to find out the current distribution of the two secondary windings. A similar idea in the previous section can be applied here, where Faraday's law and Ohm's law are combined to build relationships. However, before we go through that process, there is a special thing in our case. In the previous section, the core is an EI core structure, which means almost the whole windings are covered by the core. However, the core we use here is a UI core, and the side view is shown in Figure 4.7. From the figure we can see that some

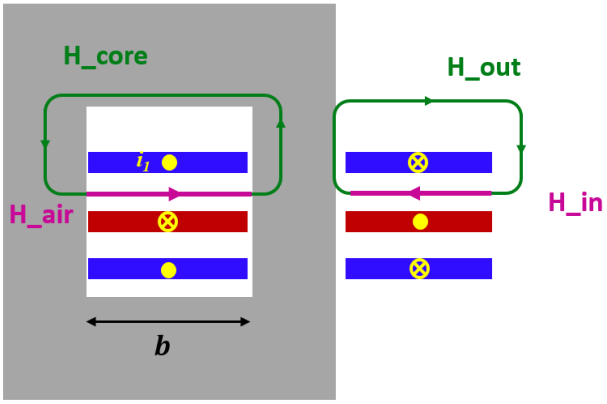


Figure 4.7: H field distribution of the first building block.

parts of the windings are inside the core, while the other parts are outside of the core. For the windings inside the core, we can use previous method to calculate the H field [30]. Based on Ampere's law,

$$I_1 = H_{core} l_{core} + H_{air} b \tag{4.22}$$

Because $\mu_{core} >> \mu_0$, $H_{core} << H_{air}$. Hence,

$$I_1 \approx H_{air} b \tag{4.23}$$

But how about the windings outside the core? In [32], it had the similar problem. For the RM core used in [32], there are also areas where the windings are not covered by the core. Simulation results are presented proving that the field distribution are dominated by the winding arrangement, while the existence of the core has a minor effect. In our case, we also did 3D simulation and made the comparison. The H field plot is shown in Figure 4.8. From results, we know that the H field distribution is identical for the areas inside and outside the core. And for the area outside the core, the H field outside the windings is negligible. In other words, almost all the H field is still constrained inside the windings. The H field outside the windings is canceled out, just like in the area inside the core. Based on the

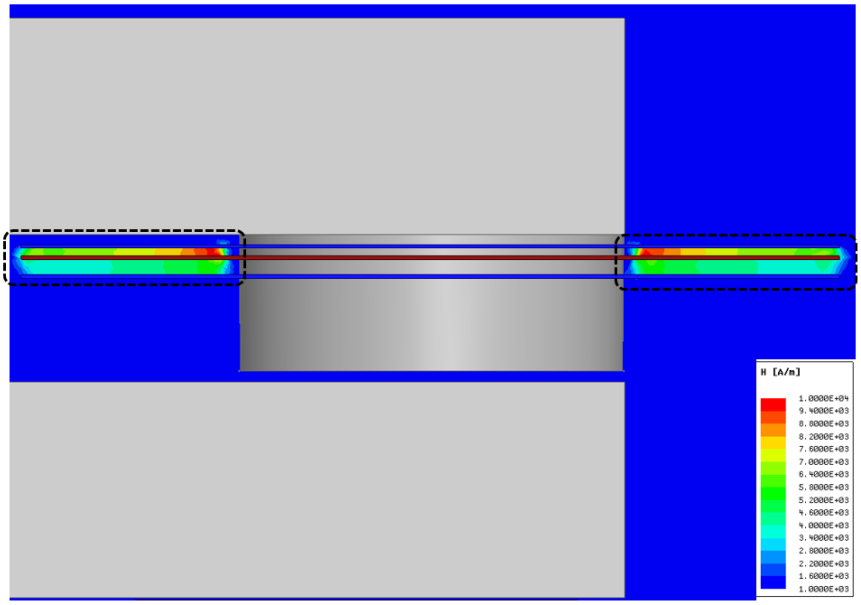


Figure 4.8: Simulation results of H field distribution for the first building block.

simulation result, we can further analyze the H field. Based on Ampere's law,

$$I_1 = H_{out} l_{out} + H_{in} l_{in} \tag{4.24}$$

From simulation we have $H_{out} << Hin$. Hence,

$$I_1 \approx H_{in} b \tag{4.25}$$

The expression is the same as that of the H field inside the core, which also matches with the simulation result. From this analysis, we know the H field inside and outside the core should be the same. This is important in the following calculation because the integration of flux density along the whole winding can be simplified.

First, the H field between top secondary winding and primary winding H_1 and the H field between primary winding and bottom secondary winding H_2 can be obtained through

Ampere's law.

$$H_1 = \frac{I_1}{b} \tag{4.26}$$

$$H_2 = \frac{I_2}{b} = \frac{I_1 - I}{b} \tag{4.27}$$

where I is the primary side current, or the total secondary side current, I_1 and I_2 are the current of first secondary winding s1 and second secondary winding s2, respectively. b is the width of the core window area. For our case where the winding fills the whole window, b is also the winding width. The flux across the gap are given by

$$\Phi_1 = \mu_0 r_1 l \frac{I_1}{b} \tag{4.28}$$

$$\Phi_2 = \mu_0 r_2 l \frac{I_1 - I}{b} \tag{4.29}$$

Where Φ_1 is the flux across the gap between s1 and p, and Φ_2 is the flux across the gap between s2 and p. μ_0 is the permeability of FR-4 insulation, which equals the permeability of air. r_1 and r_2 are the distance between s1 and p, and s2 and p, respectively. l is the equivalent winding length. Define J_1 as the current density at the bottom of s1, and J_2 as the current density at the top of s2. Select the top of s1 as the starting point of MMF, J_1 is given by [30]

$$J_1 = \frac{I_1 \alpha}{b} \coth \alpha h \tag{4.30}$$

Where α is defined in (4.2). Similarly, if we select the bottom of s2 to be the MMF starting point, J_2 is given by

$$J_2 = \frac{(I - I_1)\alpha}{b} \coth \alpha h \tag{4.31}$$

The next step is to solve for the flux across primary winding p. In frequency domain, based on MQS and Maxwell equations, H field satisfies a similar relationship as of current density

J

$$\frac{d^2H}{dx^2} = \alpha^2 H \tag{4.32}$$

And the solution is

$$H_p = A\cosh\alpha x + B\sinh\alpha x \tag{4.33}$$

Where A and B are constants that need to be determined by the boundary conditions, and H_p represents the H field of p. For primary winding p, the two boundary conditions are immediately given by H_1 and H_2. When $x = 0$,

$$H_p(0) = H_1 \tag{4.34}$$

When $x = h$,

$$H_p(h) = H_2 \tag{4.35}$$

Solving A and B from the two boundary conditions yields

$$H_p = \frac{I_1}{b}\cosh\alpha x - (\frac{I_1}{b}\tanh\frac{\alpha h}{2} + \frac{I}{b}\frac{1}{\sinh\alpha h})\sinh\alpha x \tag{4.36}$$

The total flux across p is the integration of B field of p

$$\Phi_p = \int_0^h \mu_0 l H_p dx = \frac{\mu_0 l}{b}\frac{\tanh\frac{\alpha h}{2}}{\alpha}(2I_1 - I) \tag{4.37}$$

Now we can apply the induced voltage and resistive voltage balance of the loop formed by s1 and s2 in parallel [37]

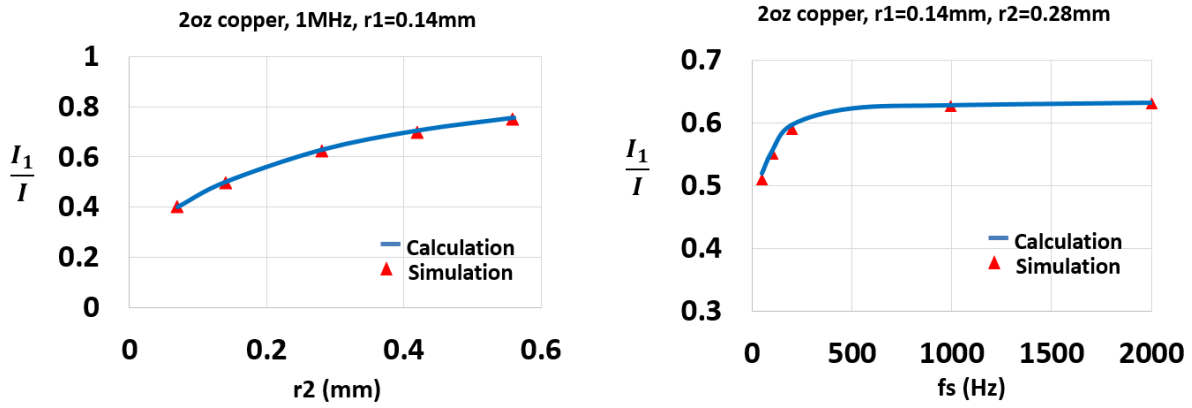
$$\rho(J_1 - J_2)l + j\omega(\Phi_1 + \Phi_p + \Phi_2) = 0 \tag{4.38}$$

Combining equations (4.28) – (4.31), (4.37), and (4.38), we solve for the current distribution

relationship and the result is

$$\frac{I_1}{I} = \frac{\frac{\coth \alpha h + \tanh \frac{\alpha h}{2}}{\alpha} + r_2}{2\frac{\coth \alpha h + \tanh \frac{\alpha h}{2}}{\alpha} + r_1 + r_2} \tag{4.39}$$

To verify the result, 3D FEA simulation model is built following the similar way in section 4.1. The results are compared in Figure 4.9. The calculation match with the simulation results



(a) Calculation and simulation results of current distribution at different r2.

(b) Calculation and simulation results of current distribution at different frequency.

Figure 4.9: Comparison of calculation and simulation results at different r2 and frequency.

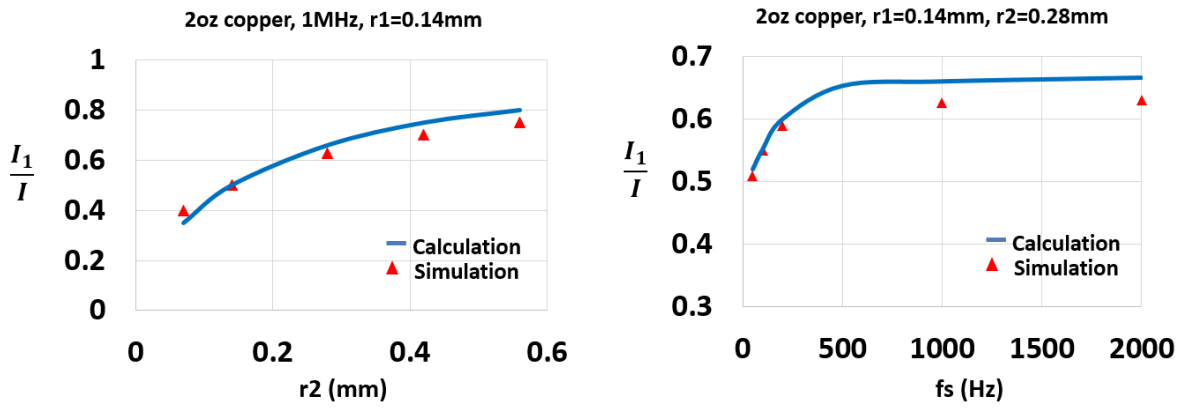
pretty well. First, with given 2oz copper thickness, 1MHz frequency, and r1=0.14mm, the current distribution changes with r2. The further s2 is to p, the higher current is distributed on s1. Second, with given 2oz copper thickness, r1=0.14mm, and r2 = 0.28mm, the current distribution varies with frequency. When the frequency is very low, the current distribution tends to become even. When the frequency is high, the current distribution approaches a ratio determined by the distance.

The calculation above can be further simplified. When design the transformer, the winding thickness is usually optimized to make the skin effect and proximity effect small enough so that the AC conduction loss is minimized. Assuming this optimization is done,

the current density in each winding is approximately even. And based on experience the flux across primary winding Φ_p is very small and can be ignored. With these two assumptions, the derivation becomes very simple. The current distribution result becomes

$$\frac{I_1}{I} = \frac{1 + \alpha^2 h r_2}{2 + \alpha^2 h (r_1 + r_2)} \tag{4.40}$$

The calculation results are compared with simulation in Figure . They still match well. The



(a) Simplified calculation and simulation results of current distribution at different r2.

(b) Simplified calculation and simulation results of current distribution at different frequency.

Figure 4.10: Comparison of simplified calculation and simulation results at different r2 and frequency for the first building block.

error happens at high frequency is because at high frequency, the skin effect and proximity effect become more dominant and the current distribution in one winding can no longer be assumed equal.

The second building block is presented in Figure 4.11. Similarly, the H fields in the gaps are given by

$$H_1 = \frac{I}{b} \tag{4.41}$$

$$H_2 = \frac{I_2}{b} = \frac{I - I_1}{b} \tag{4.42}$$

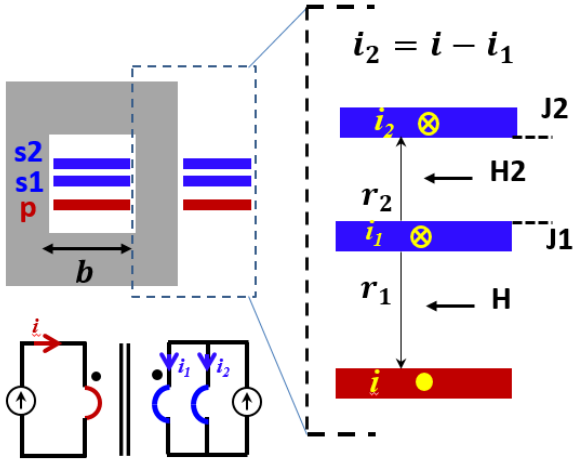


Figure 4.11: Transformer structure and equivalent circuit of the second building block.

The flux across the gap are given by

$$\Phi_2 = \mu_0 r_2 l \frac{I - I_1}{b} \tag{4.43}$$

Refine J_1 as the current density at the top of s1, and J_2 as the current density at the bottom of s2. Select the top of s2 as the starting point of MMF, J_2 is given by

$$J_2 = \frac{(I - I_1)\alpha}{b} \coth \alpha h \tag{4.44}$$

Next, to derive the expression for J_1, H field is solved first. The H field on s1 H_{s1} has the same form as that of the primary winding in equation (4.33)

$$H_{s1} = C \cosh \alpha x + D \sinh \alpha x \tag{4.45}$$

Again, we apply two boundary conditions H_1 and H_2

$$H_{s1}(0) = H_2 \tag{4.46}$$

$$H_{s1}(h) = H_1 \tag{4.47}$$

Solving C and D yields

$$H_{s1} = \frac{I - I_1}{b}\cosh\alpha x + (\frac{I_1}{b}\frac{1}{\sinh\alpha h} - \frac{I - I_1}{b}\tanh\frac{\alpha h}{2})\sinh\alpha x \tag{4.48}$$

From Maxwell equations, MQS, and 1-D approximation, we have

$$J_{s1} = \frac{dH_{s1}}{dx} \tag{4.49}$$

And we know

$$J_1 = J_{s1}(0) \tag{4.50}$$

Solving equations (4.49) and (4.50) yields

$$J_1 = \frac{I_1\alpha}{b}\frac{1}{\sinh\alpha h} - \frac{(I - I_1)\alpha}{b}\tanh\frac{\alpha h}{2} \tag{4.51}$$

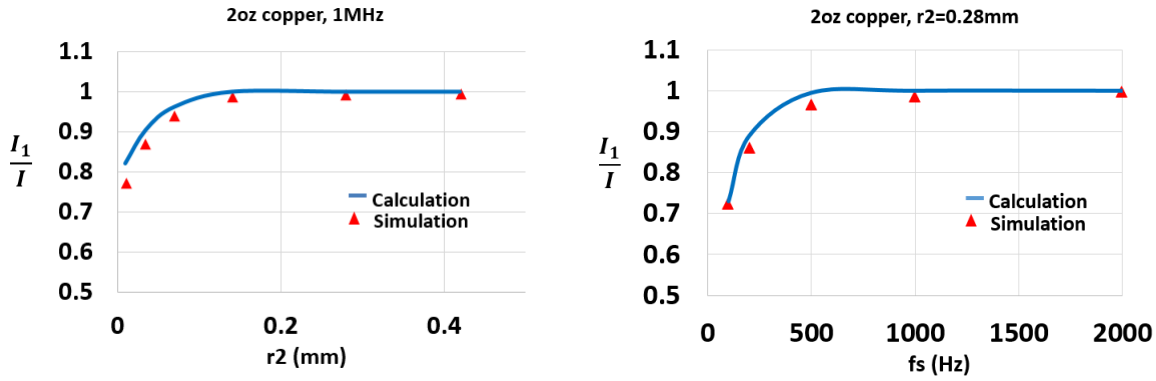
Again, we apply the voltage balance of the loop formed by s1 and s2.

$$\rho(J_2 - J_1)l + j\omega\Phi_2 = 0 \tag{4.52}$$

Combining equations (4.43), (4.44), (4.51), and (4.52), we solve for the current distribution relationship and the result is

$$\frac{I_1}{I} = \frac{\frac{\coth\alpha h + \tanh\frac{\alpha h}{2}}{\alpha} + r_2}{2\frac{\coth\alpha h}{\alpha} + r_2} \tag{4.53}$$

The results are compared in Figure 4.12. First, with given 2oz copper thickness and 1MHz frequency, the current distribution changes with r2. Second, with given 2oz copper thickness



(a) Calculation and simulation results of current distribution at different r2.

(b) Calculation and simulation results of current distribution at different frequency.

Figure 4.12: Comparison of calculation and simulation results at different r2 and frequency for the second building block.

and r2 = 0.28mm, the current distribution varies with frequency. When the frequency is very low, the current distribution tends to become even. When the frequency is high, the current tends to distributes more and more on s1.These results also match with what is obtained from simulation. Note that within certain r2 and fs range, all the current are distributed on the secondary winding that is closer to the primary winding. This is also known as the "shielding effect". The calculation of second building block can also be simplified using the same approximation in building block #1. After we establish the two building blocks, we can combine them to calculate the current distribution of multi-layer winding structures.

4.4 Symmetrical Layer Arrangement

For the layer arrangement in Figure 4.1, first assume there is only one excitation: primary winding p1. Based on the previous model, only the two secondary windings (s1, s2) next to p1 have current, while the other two secondary windings (s3, s4) are blocked by the "shielding effect". And the current distribution on s1 and s2 can be calculated by the equation of

building block #1. Define k equal to the current ratio between the first secondary current and the primary current. The k value can be obtained from equation (4.39), which is $\frac{2}{3}$ in our case. Now the current on all secondary windings due to p1 is obtained.

$$s_1 = k \cdot p_1 \tag{4.54}$$

$$s_2 = (1-k) \cdot p_1 \tag{4.55}$$

$$s_3 = s_4 = 0 \tag{4.56}$$

Where s_i and p_i (i=1,2,3,4) represent the current on that layer. Following the similar manner, we can obtained the secondary winding current caused by p2, p3, p4, separately. For each secondary winding, according to superposition concept, the current is the summation of the current excited from four primary winding excitation individually. The final relationships are presented in equations (4.57) - (4.60).

$$s_1 = k \cdot p_1 \tag{4.57}$$

$$s_2 = (1-k) \cdot p_1 + k \cdot p_2 \tag{4.58}$$

$$s_3 = (1-k) \cdot p_2 + k \cdot p_3 \tag{4.59}$$

$$s_4 = (1-k) \cdot p_3 + p_4 \tag{4.60}$$

Alternatively, secondary windings can be used as excitation. The same method is used to obtain the four primary current.

$$p_1 = s_1 + (1-k) \cdot s_2 \tag{4.61}$$

$$p_2 = k \cdot s_2 + (1-k) \cdot s_3 \tag{4.62}$$

$$p_3 = k \cdot s_3 + (1-k) \cdot s_4 \tag{4.63}$$

$$p_4 = k \cdot S_4 \tag{4.64}$$

Finally, the eight relationships (4.57) – (4.64) can be written in the matrix form (4.65).

$$\begin{bmatrix} 1 & 0 & 0 & 0 & -1 & k-1 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & -k & k-1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & -k & k-1 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & -k \\ -k & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ k-1 & -k & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & k-1 & -k & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & k-1 & -1 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} p_1 \\ p_2 \\ p_3 \\ p_4 \\ s_1 \\ s_2 \\ s_3 \\ s_4 \end{bmatrix} = 0 \tag{4.65}$$

The only thing left is to solve this simple homogeneous linear equations. And note that due to the "shielding effect", the matrix is always highly sparse, which gives immediate solution for current distribution. For this matrix equation, it has a non-zero one-dimensional solution

space (4.66).

$$\begin{bmatrix} p_1 \\ p_2 \\ p_3 \\ p_4 \\ s_1 \\ s_2 \\ s_3 \\ s_4 \end{bmatrix} = \alpha \begin{bmatrix} 1 \\ 1 \\ 1 \\ k \\ k \\ 1 \\ 1 \\ 1 \end{bmatrix} \tag{4.66}$$

Where $\alpha \in \mathbb{R}$. The distribution results of the analytic model are presented in Table 4.1. They exactly match the simulation results (with some round-off error). The proposed simplified

Table 4.1: Current distribution of original layer arrangement by analytic model.

Current Distribution	First Layer	Second Layer	Third Layer	Fourth Layer
Primary	27.2%	27.2%	27.2%	18.4%
Secondary	18.4%	27.2%	27.2%	27.2%

model can be applied to n parallel layer structure. A 2n by 2n matrix needs to be solved. Because the matrix is highly sparse, the solution is simple even n becomes large.

With the simplified analytic model, it becomes easy to do test different layer arrangements. To improve the performance, a symmetrical layer arrangement is proposed and shown in Figure 4.13. Following a similar modeling process, we can get the matrix equation

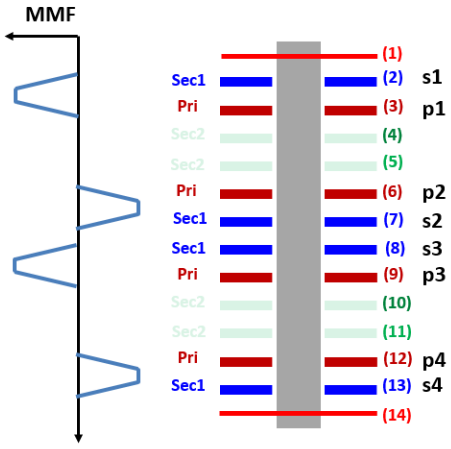


Figure 4.13: Proposed symmetrical transformer winding arrangement.

as follows.

$$\begin{bmatrix} 1 & 0 & 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & -k & k-1 & 0 \\ 0 & 0 & 1 & 0 & 0 & k-1 & -k & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & -1 \\ -m & m-1 & 0 & 0 & 1 & 0 & 0 & 0 \\ m-1 & -m & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -m & m-1 & 0 & 0 & 1 & 0 \\ 0 & 0 & m-1 & -m & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} p_1 \\ p_2 \\ p_3 \\ p_4 \\ s_1 \\ s_2 \\ s_3 \\ s_4 \end{bmatrix} = 0 \qquad (4.67)$$

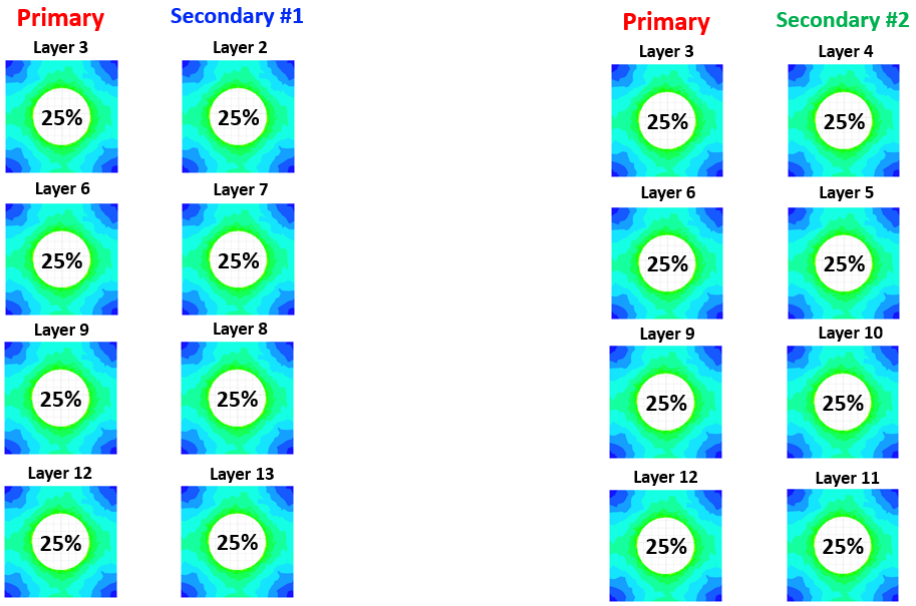
Note that here we have one more ratio m, which is the current distribution ratio of building block #1 of a different dimension. However, if we solve the equation, it has a non-zero

one-dimensional solution space.

$$\begin{bmatrix} p_1 \\ p_2 \\ p_3 \\ p_4 \\ s_1 \\ s_2 \\ s_3 \\ s_4 \end{bmatrix} = \alpha \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \end{bmatrix} \tag{4.68}$$

Where $\alpha \in \mathbb{R}$. This means that the current distribution is always balanced and not related to the ratio k and m. Therefore, no matter what the distance between layers, the current is always evenly distributed among all layers. This makes the solution more robust against FR4 thickness of PCB. In addition, because the current is evenly distributed, the AC resistance calculation in [30] still applies and will be directly used in the optimization process in the following section. The simulation results are presented in Figure 4.14. It verifies the perfect current sharing of the proposed structure. From this design we can also get some intuition that a symmetrical structure means a more symmetrical matrix, which tends to give a uniform solution and hence better current sharing.

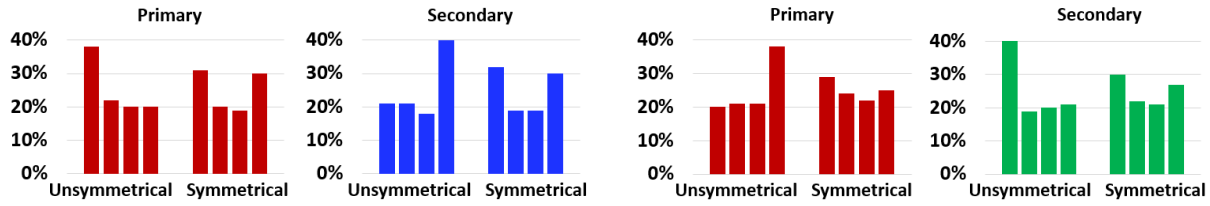
In the previous analysis, we assume ideal via structure. In the simulation, we can apply the termination and via structure proposed in chapter 3 on the new layer scheme. The simulation results of the four parallel layers current distributions in percentage are presented in Figure 4.15a and Figure 4.15b for positive and negative half cycle, respectively. With the via and termination impact, the current distribution of the symmetrical structure is no longer even. But it still has much better current sharing performance than the unsymmetrical structure and the total winding loss is reduced by 10%. This impact is considered in the



(a) Current distribution of positive half cycle. (b) Current distribution of negative half cycle.

Figure 4.14: Current distribution of proposed transformer winding arrangement.

optimization procedure with a correction factor.



(a) Current distribution of positive half cycle. (b) Current distribution of negative half cycle.

Figure 4.15: Comparison of current distributions of unsymmetrical and symmetrical layer arrangement.

Chapter 5

Transformer Optimization and Experimental Results

5.1 Transformer Design Optimization Procedure

With all the above improvements, the design is optimized using the process demonstrated in [25] and [29]. First, magnetic materials used for the transformer core are tested and compared in Figure 5.1. At 1MHz, ML91 from Hitachi has the lowest core loss density and

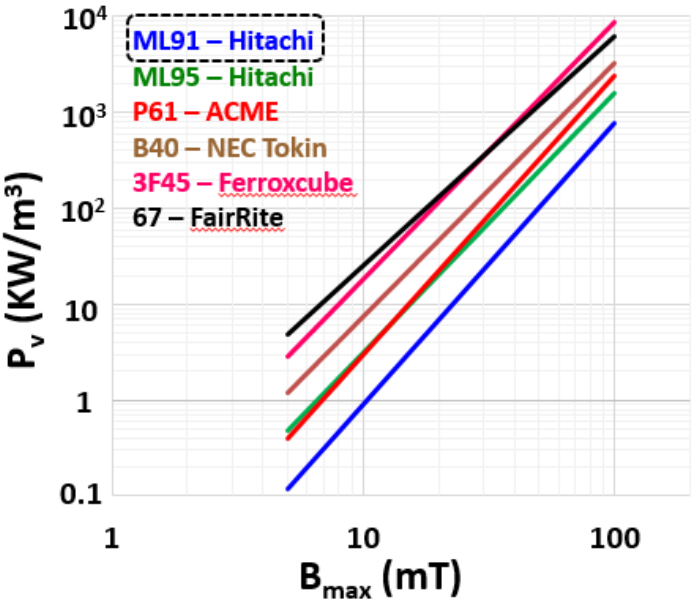


Figure 5.1: Core loss density of different magnetic materials at 1MHz excitation.

is selected. To optimize the transformer dimension, two variables are defined: r, the radius of the core leg, and c, the winding width. The dimensions are shown in Figure 5.2. With these

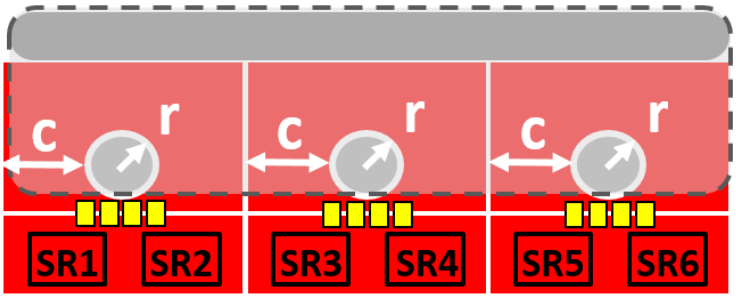


Figure 5.2: Two variables defined for transformer optimization.

two variables, all the transformer dimensions can be derived. Next, we need to estimate the transformer loss. The transformer loss has two parts. First, the core loss is obtained from the model in [39], which provides the modified Steinmetz equation for rectangular voltage excitation. The core loss is expressed in equation (5.1).

$$P_{core} = P_v * Vol_{core} \tag{5.1}$$

Where P_v is the power loss density of the core, and Vol_{core} is the volume of the core.

$$P_v = \frac{8}{\pi^2} k f^{\alpha} B_m^{\beta} \tag{5.2}$$

Where f is the frequency and B_m is the AC flux density magnitude of the core. The k, α, β are the parameters obtained from the curve fitting of the measurement data. The B_m and core volume can be expressed in relationship with r and c. Finally, for different combination of r and c, we can get the core loss results.

Another factor of the core structure is the air gap position. The fringing flux of the air gap would impact the winding current distribution and loss. By changing the air gap

position, the fringing flux impact can be minimized. And after that, the core thickness is determined. In the previous simulations, the magnetizing current is ignored, so there is no flux in the air gap. To consider this effect, we use the simulation model in the previous chapter and add to the excitation the magnitude deviation and phase shift caused by the magnetizing current. Similar as the UI core design, we can place the air gap at the bottom of the PCB winding board. Figure 5.3 shows the flux distribution if the air gap is placed very close to the bottom of the board (only 0.05mm is reserved for tolerance). High fringing

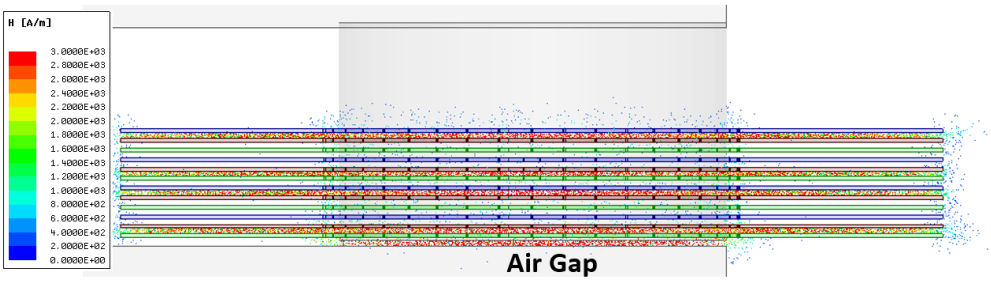


Figure 5.3: Cross-section view of flux distribution with the air gap close to the bottom of the board.

flux appears around the air gap and could impact the current in the windings above it. If we sweep the distance between the air gap to the bottom of the board, we can obtain the total winding loss relationship with this distance. The curve is presented in Figure 5.4. The total winding loss is normalized at infinite distance, or when there is no air gap. In the figure, it is clear that the winding loss is highest when the air gap is closest to the winding. When increasing the distance, the loss becomes smaller as the impact becomes smaller. after certain point the impact becomes negligible and the loss is very close to that without air gap. Keep increasing the distance after that point only increase the total thickness of the converter and no longer reduces the loss. As a result, we choose 1.5mm distance for this design.

Besides the winding loss, we would also like to know the fringing flux impact on the

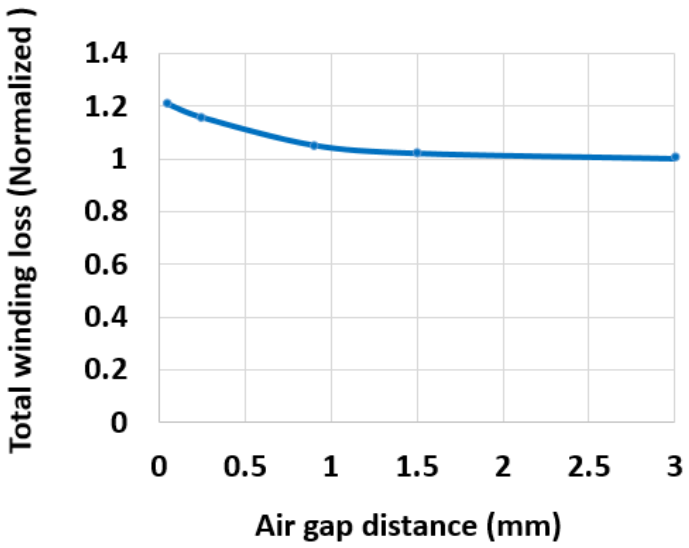


Figure 5.4: Normalized total winding loss versus distance between air gap and the bottom of board.

current distribution, including the current distribution on parallel layers and current distribution on each winding layer. The current distribution of parallel layers for the worst case when the air gap distance is 0.05mm is presented in Figure 5.5. The percentage on each

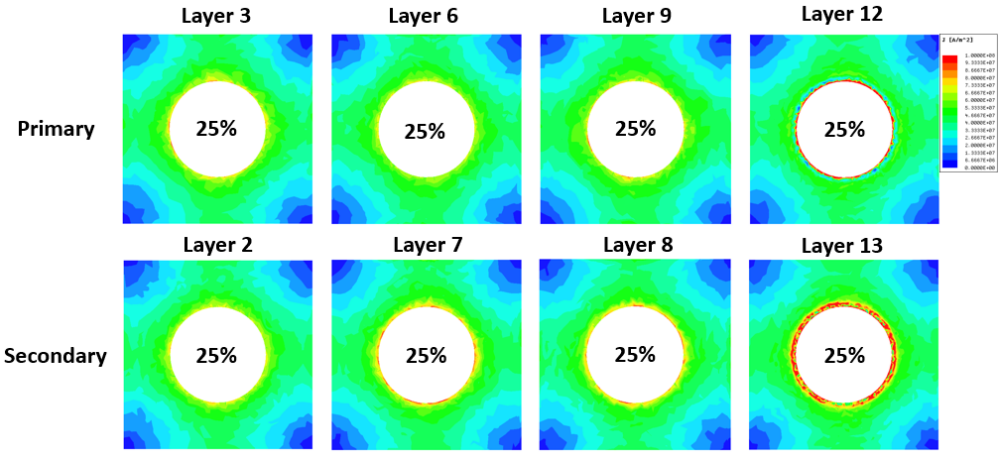


Figure 5.5: Current distribution of windings with fringing effect at 0.05mm distance.

windings refer to the current percentage of that winding layer. The parallel windings still have even current distribution. The parallel distribution is very similar for other distances.

Therefore, the fringing flux does not affect the parallel current distribution. However, notice that the current distribution on the bottom layer of primary and secondary windings becomes very bad. High current crowding appears near the center core region. This is the reason that the winding loss becomes high. Since the fringing effect is minimized by select the appropriate distance, the loss estimation for the winding is still valid. The case where the air gap is placed in the middle of the board is also studied. Now the air gap is roughly between layer 7 and layer 8. The normalized loss is 1.1, which is actually smaller than that of 0.05mm distance when placing the air gap on the bottom. The current distribution is presented in Figure 5.6. We can see the current distribution still follows the similar prin-

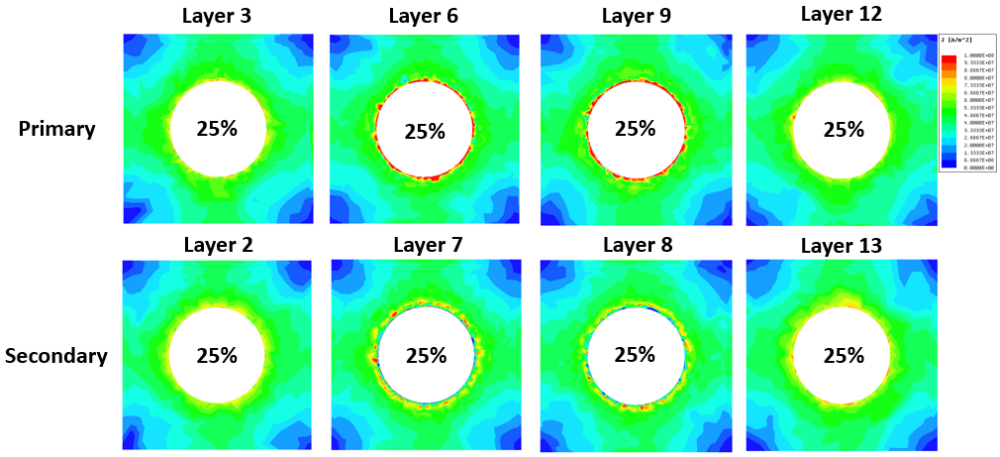


Figure 5.6: Current distribution of windings with fringing effect when the air gap is in the middle of the board.

ciple. First, the parallel distribution is not changed. Second, current crowding appears on the windings that are closed to the air gap and fringing flux, which now becomes the middle winding layers.

After the analysis above, the winding loss can be calculated based on the analytical model in [30]. The AC resistance of the winding is described by equation (5.8).

$$R_{AC} = F_R \cdot R_{DC} \tag{5.3}$$

F_R is the AC resistance coefficient given by

$$F_R = M' + \frac{m^2 - 1}{3} D' \tag{5.4}$$

Where prime means the real part and

$$M = \alpha h \coth \alpha h \tag{5.5}$$

$$D = 2\alpha h \tanh \frac{\alpha h}{2} \tag{5.6}$$

And α is already defined in equation (4.2). m is the layer number in a portion. As discussed previously, for a completely interleaved winding structure like our case, the MMF only builds in one winding layer. So $m = 1$ in our case. The DC resistance of the winding is

$$R_{DC} = \frac{\rho l_e}{chN_{layer}} \tag{5.7}$$

Where l_e is the equivalent winding length that can be calculated from r and c, h is the winding thickness, and N_{layer} is the number of parallel layers. Substitute equations (5.4) - (5.7) into equation (5.8), we can get

$$R_{AC} = M' \frac{\rho l_e}{hcN_{layer}} \tag{5.8}$$

Hence, the winding AC resistance can be described in terms of r, c and h. For a given r, c combination $r = 3.75mm$, $c = 3.8mm$ as an example, the primary and secondary AC resistance at different copper thicknesses is shown in Figure 5.7. From the figure, it is observed that before 2oz thickness, the resistance drops quickly as the thickness increases. After 2oz thickness, the resistance does not change much with higher thickness. Although the curve is plotted under one certain r, c combination, the trend of the curve is the same

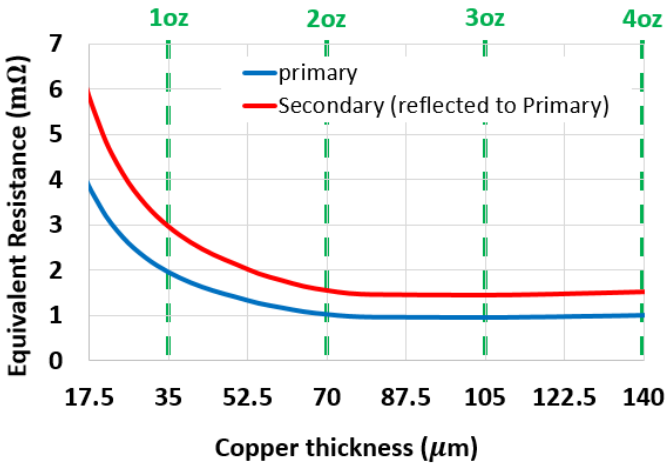


Figure 5.7: Copper thickness optimization.

for all r, c combinations. So the optimized copper thickness is selected to be 2oz. After the selection of copper thickness, the AC winding resistance can be fully described by r and c. Note that the theoretical AC resistances are compensated by a correction factor which is obtained from 3D simulation. It includes the extra losses such as termination and via loss, corner effect loss, and uneven current distribution loss, which are not considered in the theoretical model. With the compensated AC resistance, the winding loss is given by

$$P_{winding} = I_{RMS}^2 \cdot R_{AC} \tag{5.9}$$

Which is also r and c dependent. The total loss

$$P_{TR} = P_{core} + P_{winding} \tag{5.10}$$

can also be expressed in r and c.

Now both transformer loss and transformer footprint are functions of r and c. The contour of total loss is plotted in Figure 5.8. It means that for different combinations of r

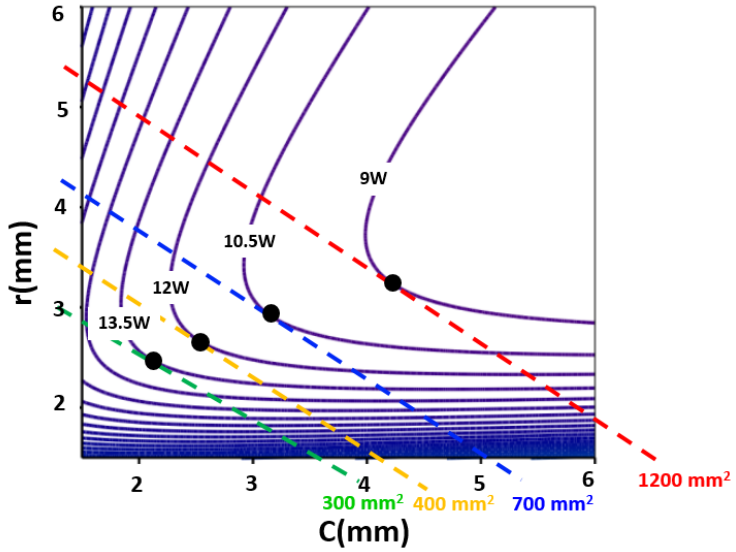


Figure 5.8: Transformer total loss and footprint contours.

and c, we have various transformer total loss. If we connect all the r, c combination with the same transformer total loss, we can get one contour. There are infinite contours on the plane, each representing a certain loss value. For comparison purpose, we only plot some of these contours, which are shown in solid lines in the figure. It is easy to observe the trend from these contours. Roughly speaking, the larger the r and c, the lower the transformer loss. Following a similar manner, we can also plot the contour of transformer footprint, as shown in dashed lines. The tangential points of the two contours are the optimal design points for the given footprint or loss. If we deviate from that point, it means for given footprint we have higher transformer loss, or for given transformer loss, we have a larger footprint.

Each tangential point means one optimal combination of transformer total loss and footprint. We can extract all these tangential point and plot them in Figure 5.9. This becomes the optimal footprint vs. transformer total loss curve, or minimum loss vs. footprint curve. The corresponding winding loss and core loss are also shown in the figure. As the footprint increases, both winding loss and core loss reduce and the total loss reduces.

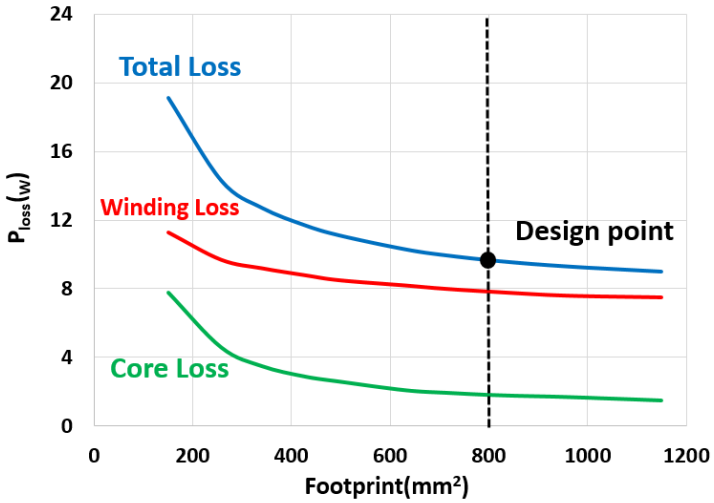


Figure 5.9: Optimal transformer total loss versus footprint.

However, when the footprint becomes very high, the loss reduction from footprint increase is not significant enough. Based on this trend, the footprint is designed at 800mm^2.

After the transformer dimensions are determined, we can trace back and perform the dead-time optimization. The selection of dead-time is a trade-off between conduction loss and turn-off loss [16]. Given the R_{dson} of the devices and resistance of transformer windings, the conduction loss is dependent of the current. The RMS current is influenced by two factors: the magnetizing current and the circulating energy during dead-time. When the dead-time is very small, the circulating energy is small and magnetizing current dominates the impact on RMS current. The smaller the dead-time, the higher magnetizing current is required to discharge the C_{oss} at a short period. So the RMS current becomes larger. The turn-off loss also becomes larger due to higher turn-off current. When the dead-time is large, the circulating energy dominates. Longer dead-time means a longer time for the circulating current to flow without delivering energy to output. So the RMS current becomes larger for the same load. But the turn-off loss reduces. Therefore, there must be a dead-time where the total loss is minimized. The total loss at full load range is plotted with different

dead-time, as presented in Figure 5.10. To achieve minimal loss, the dead-time is chosen to

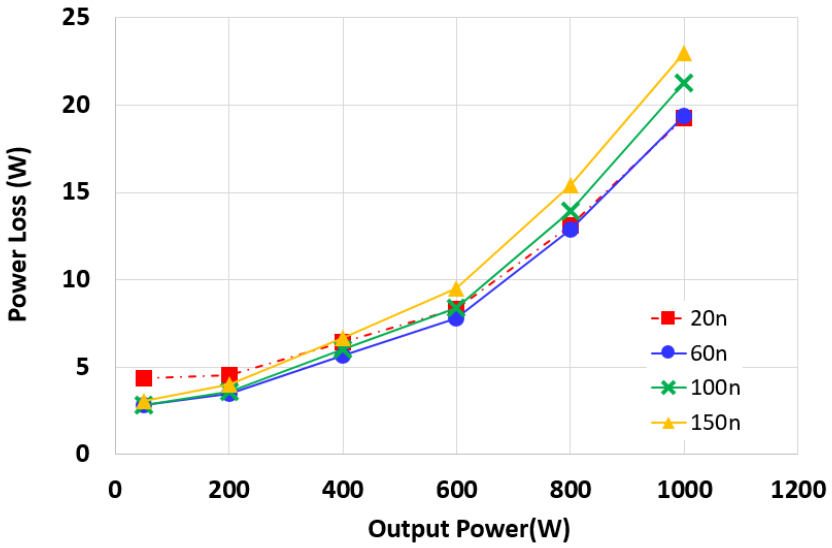


Figure 5.10: Dead-time optimization.

be around 60ns. The corresponding magnetizing inductance Lm can be derived accordingly. This selection is not completely accurate because the estimation of parameters such as C_{oss}, transformer resistance, devices resistance, etc, is not accurate. But it serves as a guideline when we do the hardware adjustment. In this case, fortunately, the dead-time we guess at the beginning is very close to the optimal value. Therefore, the RMS current used in the transformer loss estimation is also reliable.

The estimated total loss breakdown of the LLC converter at full load is presented in Figure 5.11. The shading bar represents the loss reduction from the proposed transformer design including the merged winding structure, interleaved termination and via design, and symmetrical layer arrangement. Before the improvement, the transformer winding loss is dominant and much higher than all other losses. It verifies the previous statement that the transformer design is the key for the converter to achieve high efficiency and high power density. After the improvement, the winding loss is minimized.

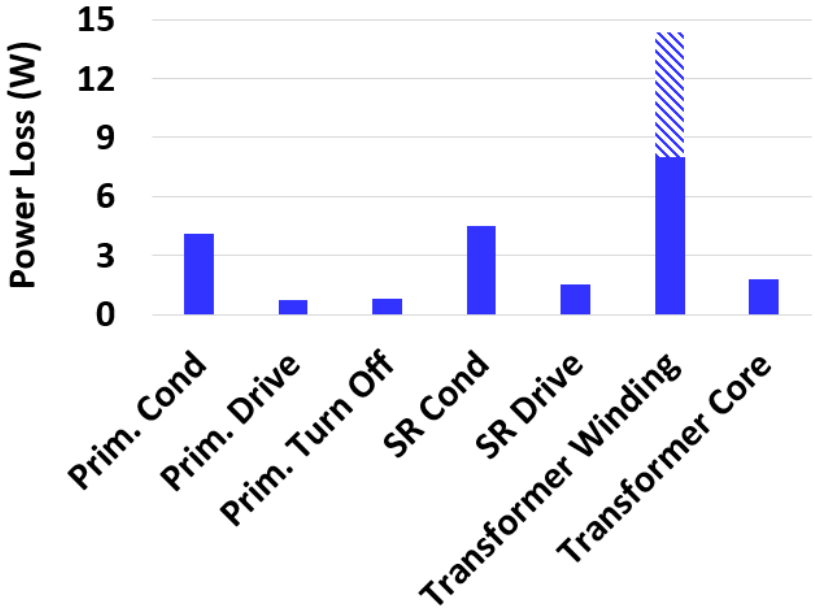


Figure 5.11: Total loss breakdown of the LLC-DCX.

5.2 Hardware and Experimental Results

The prototype for the two-stage bus converter is developed and built, as presented in Figure 5.12. The first stage Buck is in the blue box, with two coupled inductors connected in parallel. The second stage LLC is in the red box. The area on the up left corner is for all the auxiliary circuit including controller, auxiliary power, and oscillator and dead-time delay circuit for LLC. The design parameters are presented in Table 5.1.

The first thing before we test the hardware is to measure the parameters of the transformer. The air gap of the core is calculated based on the previous dead-time optimization. First, the short-circuit test is performed to measure the total leakage inductance and winding resistance. All the secondary side connections in one half cycle are shorted and measurement is done on the primary side. The primary and secondary side can be reversed but due to the 3:1 turns ratio, the secondary side impedance can be amplified when reflected to the

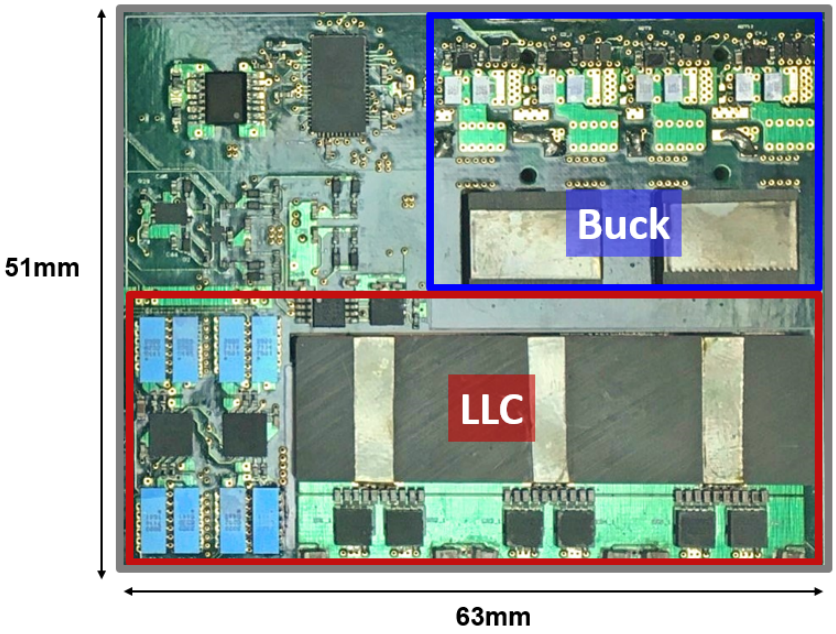


Figure 5.12: The hardware prototype of the proposed two-stage regulated bus converter.

primary. The impedance analyzer used is Agilent 4294A with 42941A Probe. The leakage inductance Lr measured is 8nH. The resistance measured is 9mΩ. Known the Lr value, the resonant capacitor can be obtained from equation (5.11).

$$f_o = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{5.11}$$

Table 5.1: Proposed LLC-DCX converter parameters.

Parameter	Value
Switching Frequency	1.05MHz
Input Voltage	36V
Output Voltage	12V
Output Power	1kW
Primary Devices	EPC2020
Secondary Devices	BSZ0500NSI
Primary Drivers	LM5113
Secondary Drivers	FAN3122

Where f_o is the resonant frequency and can be calculated from equation (5.12)

$$f_o = \frac{1}{\frac{1}{f_s} - 2t_d} \tag{5.12}$$

Where f_s is the switching frequency and t_d is the dead-time. The second step is to measure the magnetizing inductance Lm. The open-circuit test is performed and Lm is measured from the primary side. The measured results match with the calculation. Note that the Cr and the air gap are not the final value and will be adjusted based on the testing results. The switching loss becomes a little higher, but the conduction loss could reduce more due to lower RMS current.

The equipment used in the testing are presented in Table 5.2. The LLC operation

Table 5.2: Hardware testing equipment.

Equipment	Product
Input Voltage Source	TDK-Lambda GEN1500W
Output Load	TDI Dynaload RBL488
Function Generator	Tektronix AFG3102
Power Analyzer	KEYSIGHT PA2203A
Oscilloscope	Tektronix MSO 5104B
Rogowski Coil	PEM CWT03
Thermal Camera	FLIRE49001

waveforms and thermal performance at at light load, half load, and full load are shown in Figure 5.13, to Figure 5.15, respectively. In one half cycle, the primary devices and SRs turns on, Lr and Cr resonates, and we can see the resonating current on the primary side. During the dead-time, the Lr current becomes the magnetizing current which charges and discharges the C_{oss} of the devices on both primary side and secondary side. In the waveform, we can observe the V_{ds} of devices drops with a constant slope during the dead-time. It finally reaches zero before the next cycle, achieving ZVS. For the three operation condition, the

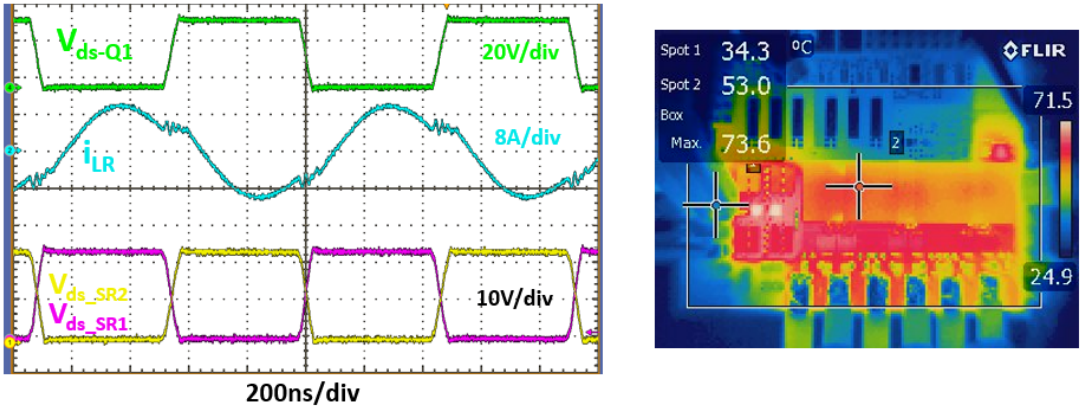


Figure 5.13: Operation waveform and thermal performance of LLC-DCX at 10A light load.

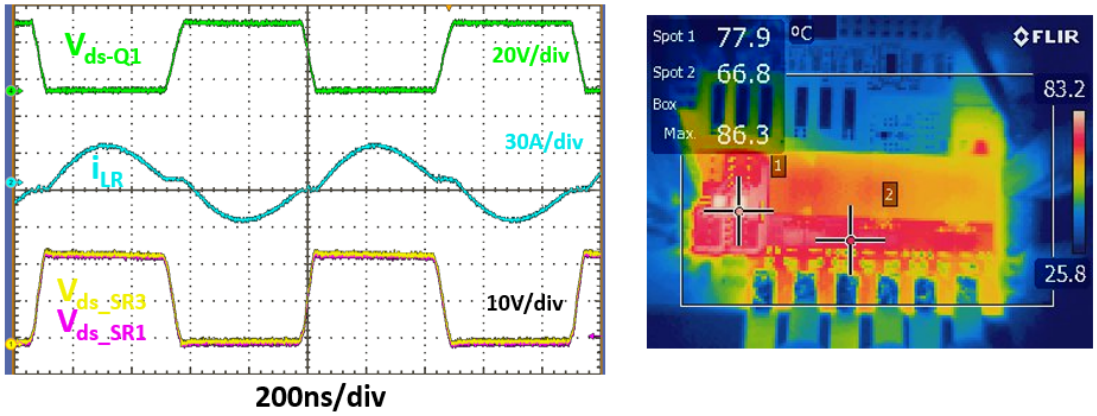


Figure 5.14: Operation waveform and thermal image of LLC-DCX at 50A half load.

waveforms are quite similar, working with switching frequency close to resonant frequency. And ZVS is achieved for all load conditions. They also show good thermal performance at different loads with a fan (wind speed 5m/sec). The efficiency of LLC-DCX is compared in Figure 5.16. The LLC efficiency was able to achieve a peak efficiency of 97.8% and an efficiency of 97.4% at heavy load. The Buck converter efficiency is measured. And the two-stage converter is measured together with open loop condition. The efficiency curve at 48V nominal input is shown in Figure 5.17. The buck converter was operating at 500 kHz per phase and the LLC was operating at 1 MHz. The plot shows the LLC and Buck efficiency

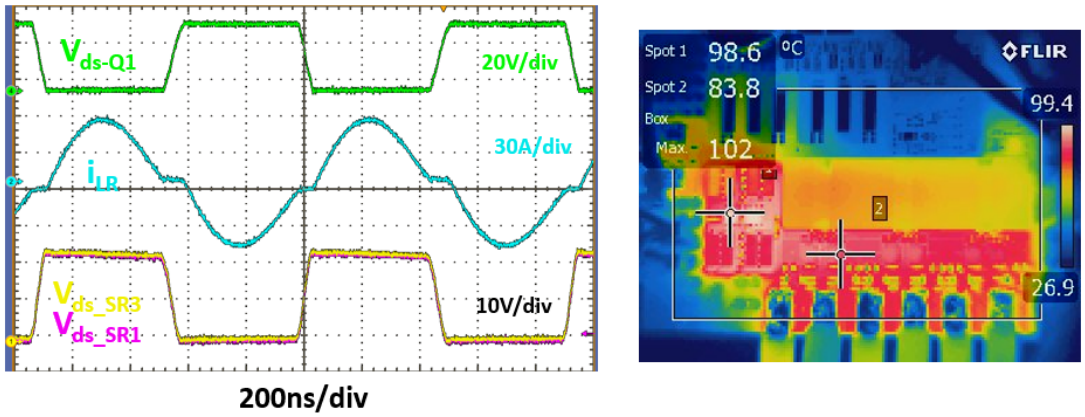


Figure 5.15: Operation waveform and thermal performance of LLC-DCX at 85A full load.

(yellow and red curve) separately and the combined expected efficiency (green curve). The final measured efficiency is shown by the blue curve. The open loop two-stage efficiency was able to achieve a peak efficiency of 96% and an efficiency of 95% at heavy load. The converter was not run all the way to 1kW as there were concerns with the heat on the Buck converter. Note that in the two-stage prototype, the connections between two-stages are not optimized. It still has the potential to improve the efficiency and reduce the footprint. The bus converter is compared with the state of the arts in Table 5.3. With close peak efficiency, this design has the highest power rating and power density.

Table 5.3: Comparison with the state-of-the-arts bus converter.

Prototype	Power Rating	Peak Efficiency	Full-Load Efficiency	Power Density
Proposed Converter	1000W	96%	95%	615W/in^3
GE QBVE067A0B41	800W	96.3%	96%	480W/in^3
Delta Q54SG	600W	96.5%	95.8%	360W/in^3
SynQor PQ60120HZx50	600W	95.5%	94.9%	254W/in^3

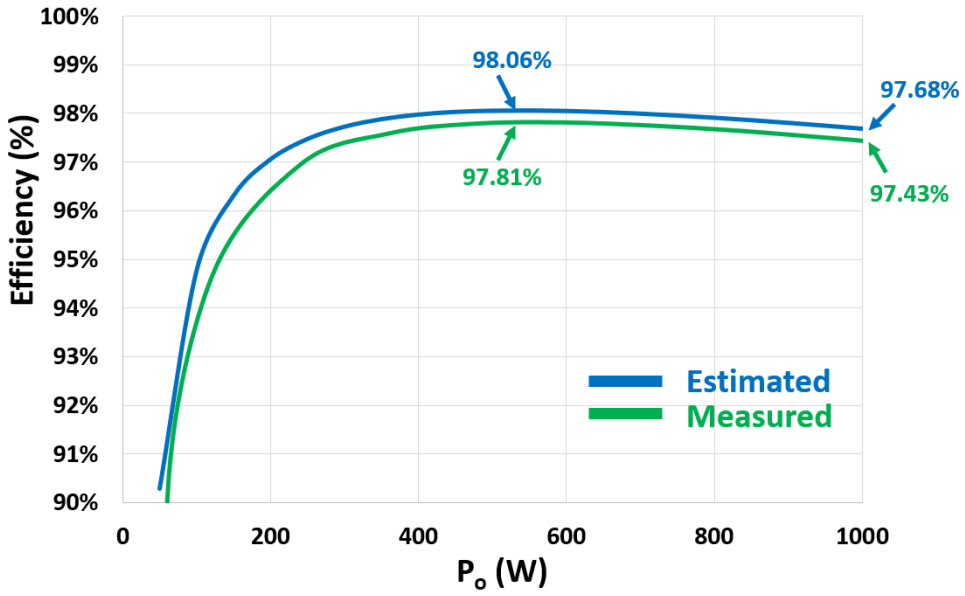


Figure 5.16: Estimated and measured efficiency curve of LLC-DCX.

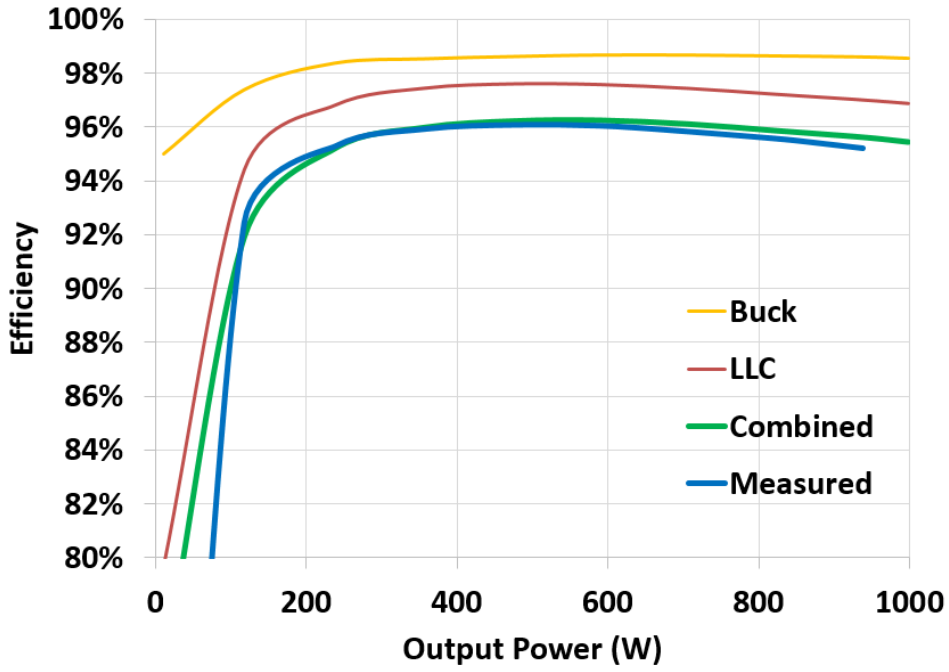


Figure 5.17: Open-loop two-stage efficiency curve at 48V input.

Chapter 6

Conclusions

The previous sections discussed the design, implementation, and verification of the two-stage intermediate bus converter at 1kW. This final chapter will discuss the conclusions from the design.

The thesis focus on the design of a regulated isolated intermediate bus converter. A two-stage architecture is proposed to achieve fixed-frequency control operation. For the second stage, the LLC converter is used for its soft-switching capability. GaN devices are used to further reduce the switching loss and device conduction loss. With the help of LLC topology and GaN devices, the switching frequency is increased to 1MHz. At such high frequency, the transformer design of the LLC converter becomes the major challenge.

At MHz high frequency, the AC losses of the transformer windings become very high. Matrix transformer concept can be applied to distribute the current and achieve more even current distribution on each elemental transformer. In this design, three elemental transformers are connected in series on the primary side and in parallel on the secondary side. It also guarantees good current sharing for secondary side SR devices. In this design, some regions of the windings are not completely interleaved. This induces current crowding and extra loss. A novel merged winding structure is proposed to better cancel the leakage flux in the transformer. Based on 3D FEA simulation, 40% loss reduction is achieved by this improvement.

After the improvement of winding design, termination and via design are studied. This is an important aspect as well because all the transformer windings are connected with the external circuit through termination and vias on the PCB. First, some secondary termination structures are analyzed and compared. The integrated termination design has the best performance and is selected for this design. Second, the primary termination and via structure, which has not been studied carefully in the literature, is discussed in detail. Based on the interleaving concept, a new structure is proposed where the multi-layer termination and via groups are both interleaved. From the simulation, the leakage flux and AC losses are significantly reduced.

The termination and via design concept can be widely applied. They are not restricted to the primary or secondary side respectively. In effect, when the circuit and connections outside the transformer windings are simple, for example, the center-tapped rectifier structure, the integrated termination design can be applied. When the circuit and connections outside the transformer windings are complex, where integrated design is no longer possible, the termination and via interleaving concept can be applied. As a result, a complete solution is provided for the transformer winding termination design. It could be applied based on different external circuits.

The next topic studied is the current distribution of parallel winding layers in PCB-winding transformer. This is important in the high current application, where multiple layers are used to distribute the current. A 1-D analytic model is proposed to estimate the current distribution of multiple parallel winding layers. The model is simple and quick, which can be used to estimate and select different layer arrangements. In addition, a symmetrical winding layer arrangement is proposed to improve the current distribution between layers.

Finally, the hardware for the 1kW two-stage bus converter is built. It is compared with state-of-the-art products and has the best power density.

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