Static and Dynamic Characterization of Silicon Carbide and Gallium Nitride Power Semiconductors

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Thesis submitted to the faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

Master of Science
In
Electrical Engineering

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February 19, 2018
Blacksburg, Virginia

Keywords: SiC MOSFET, vertical GaN, short-circuit, characterization, switching characteristics, static characteristics

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ABSTRACT

Wide-bandgap semiconductors have made and are continuing to make a major impact on the power electronics world. The most common commercially available wide-bandgap semiconductors for power electronics applications are SiC and GaN devices. This paper focuses on the newest devices emerging that are made with these wide-bandgap materials.

The static and dynamic characterization of six different SiC MOSFETs from different manufacturers are presented. The static characterization consists of the output characteristics, transfer characteristics and device capacitances. High temperature (up to 150 °C) static characterization provides an insight into the dependence of threshold voltage and on-state resistance on temperature. The dynamic characterizations of the devices are conducted by performing the double-pulse test. The switching characteristics are also tested at high temperature, with the presented results putting an emphasis on one of the devices. A comparison of the key characterization results summarizes the performance of the different devices.

The characterization of one of the SiC MOSFETs is then continued with a short-circuit failure mode operation test. The device is subjected to non-destructive and destructive pulses to see how the device behaves. The non-destructive tests include a look at the performance under different external gate resistances and drain-source voltages. It is found that as the external gate resistance is increased, the waveforms get noisier. Also, as the drain-source

voltage is increased, the maximum short-circuit current level rises. The destructive tests find the amount of time that the device is able to withstand short-circuit operation. At room temperature the device is able to withstand 4.5 μs whereas at 100 °C, the device is able to withstand 4.2 μs. It is found that despite the different conditions that the device is tested at for destructive tests, the energy that they can withstand is similar.

This paper also presents the static and dynamic characterization of a 600 V, 2A, normally-off, vertical gallium-nitride (GaN) transistor. A description of the fabrication process and the setup used to test the device are presented. The fabricated vertical GaN transistor has a threshold voltage of 3.3 V, a breakdown voltage of 600 V, an on-resistance of 880 mΩ, switching speeds up to 97 V/ns, and turn-on and turn-off switching losses of 8.12 μJ and 3.04 μJ, respectively, demonstrating the great potential of this device.

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GENERAL AUDIENCE ABSTRACT

A key part in a power electronics circuit is the switch component. Currently, the devices usually used as the switch are made from silicon. As the performance limits of silicon are reached though, wide-bandgap semiconductors are proving to be a promising alternative to silicon semiconductors. These wide-bandgap switches will allow for higher powers, higher efficiency and higher temperature operation. The technology is still novel though and so new devices are still being developed. This paper focuses on showing the performance of the newest devices emerging that are made with these wide-bandgap materials.

To demonstrate the performance potential of a switching device, the non-switching and switching behavior need to be tested. These tests are described and the results are shown for both Silicon Carbide (SiC) and Gallium Nitride (GaN) semiconductors which are the most common wide bandgap semiconductors.

The failure mode operation of one of the SiC devices is also tested. A common failure in power electronics is a short circuit failure where the switch is turned on for a long amount of time and kept on for too long, eventually leading to the device breaking destructively. To understand the limits and capabilities of these devices in a short circuit failure, non-destructive and destructive tests are explained and demonstrated.

Acknowledgements

Firstly, I would like to thank Dr. Rolando Burgos. Thank you for your support and guidance over the past two years. You have provided me with the great opportunity of being a part of CPES and I am very grateful for that.

Thank you to my committee members, Dr. G.Q. Lu and Dr. Dushan Boroyevich who have always provided useful insight and feedback that has helped to shape my research.

I would also like to thank the CPES administrative staff, Marianne Hawthorne, Linda Long, Teresa Shaw, Lauren Shutt, Trish Rose and David Gilham for their support.

Also, for the past two years I have worked on two industry projects with HRL and General Motors. I appreciate all of the guidance and insight you have provided. Thank you Rongming Chu, Marko Jaksic, Brian Peaslee, Mehrdad Teimor, John Czubay, Sung Chung, Costin Stancu, Terry Ward, and Bill Ivan.

To my colleagues and friends at CPES, past and present, thank you for making my time here so enjoyable. A few but not all are: Slavko Mocevic, Victor Turriate, Joseph Kozak, Niloofar Rashidi Mehrabadi, Yingying Gui, Alex Chu, Erick Aponte, Paul Rankin, Marianne Wang and Yue Xu. Thank you especially to Christina DiMarino and Ali Marzoughi for helping me get from day one to today, I have learned so much from you both and I appreciate the patience you had with me. Also, thank you Grace Watt for agreeing to continue on with my work and being a great help in my final months.

To my Romero family and my DeWeerth family, thank you for your love and guidance. Finally, thank you Jesse for your endless patience, emotional support, technical support and proofreading skills.

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Chapter 1 Introduction

1.1 Impact of Wide-Bandgap Semiconductors

Semiconductors made from materials with wide-bandgaps have been shown to have better thermal conductivity, lower on-resistances and higher electron mobility than their silicon counterparts [1][2][3]. The higher temperature operation, lower losses and faster switching speeds that ensues means that they are having an enormous impact on the power electronics world. The range of influence is wide, from data centers and automotive applications to grid systems [4].

The first power electronics oriented wide-bandgap (WBG) semiconductor was a SiC Schottky diode in 1992 capable of blocking 400 V [5] and in the decades since then, we now have commercially available discrete SiC Schottky diodes capable of blocking up to 8 kV[6] . Since then, the technology has progressed in terms of power capabilities and devices types [7]. And although there are other materials being researched for power electronics applications, including diamond [8], the most common wide-bandgap semiconductors are Silicon Carbide (SiC) and Gallium Nitride (GaN) devices.

Of the WBG power transistors, the SiC MOSFET has demonstrated the greatest commercial viability thus far. SiC MOSFETs with blocking voltage ratings from 650 - 1700 V are commercially available, and devices with ratings of 3.3–15 kV are fast

approaching. They are even already being used for various different applications [9][10]. This technology will continue to advance with larger breakdown voltages, higher current levels and smaller sizes [11][12]. This paper presents the characteristics of six different SiC MOSFETs which are all pre-commercialization and gives an insight into what is next from this technology.

GaN power transistors have followed suit with devices that have impressively fast switching speeds, even when compared to SiC [13]. Their success, especially in the 100–650 V range, has supported the design of power converters switching in the megahertz range while simultaneously increasing the efficiency to previously unattainable levels. GaN power transistors predominantly have a lateral device structure because it can be fabricated using Si and SiC substrates, which are less expensive than GaN substrates and require an easier process. While lateral GaN transistors have demonstrated high efficiency and fast switching speeds, their current carrying capability and breakdown voltage are limited by this lateral device structure [14], [15]. Recent advances have overcome these barriers, and now more vertical GaN devices are being developed [16], [17]. HRL Laboratories have recently fabricated a 600 V, 2 A, normally-off, vertical GaN transistors and the characterization results are presented in this paper.

The advantages of using wide-bandgap semiconductors are very evident but there are limitations that need to be considered as well. Since wide-bandgap devices are new and are developing quickly, the failure mode operation limitations need to be characterized also. A common factor in power electronics design is short-circuit protection on a gate driver. It has been found that wide-bandgap semiconductors have a shorter short-circuit withstand time and as the technology advances it is going to get shorter [18]. This impacts gate driver

design because when switching WBG devices, there is not as much time to protect against a short-circuit failure. Having an understanding of how failure mode operation is handled is essential.

1.2 Research Motivations

Before we are able to implement this new technology into power electronics systems, it is important to have a very thorough understanding of how they behave. Especially since the technology is advancing very quickly, benchmarking their capabilities helps to determine where everything stands. This is why a static and dynamic characterization is performed on these SiC MOSFETs and vertical GaN transistors. All of the devices herein are pre-commercialization. These SiC MOSFETs are pushing boundaries with their lower on-state resistances and higher current ratings compared to what is currently commercially available. The vertical GaN transistors are starting a new category in power electronics semiconductors with a vertical GaN transistor, whereas currently there are only lateral GaN transistors available.

There is a lot of research being done looking into gate driver design for short-circuit protection [19], [20]. The goal is to detect when a short-circuit failure occurs and safely turn off the device in the shortest amount of time possible. With these advancements in new device technology, the failure mode operation changes though and the time they have to turn-off a short-circuit failure changes also. Therefore, in this study, the highest current rated SiC MOSFET presented in the static and dynamic characterization portion is taken and put under short-circuit operating conditions. The characterization of this device under

short-circuit operation shows what can be expected of this new generation of devices with higher current levels.

1.3 Thesis Organization

This paper starts with an overview of static and dynamic characteristics results for six SiC MOSFETs from four different manufacturers in Chapter 2. The capabilities of these devices range from current ratings of around 30 A (there are commercially available devices at the same current level) up to 100 A at room temperature under continuous operating conditions. A static characterization consisting of output characteristics, transfer characteristics, and device capacitances is included. A dynamic characterization of all of the devices is also performed under different load currents. The characterizations of the devices are performed at room temperature and high temperature up to 150 °C.

The characterization is then continued in Chapter 3 with one of the devices from Chapter 2. This device is characterized in short-circuit operation through a range of tests that include non-destructive and destructive tests. The destructive tests are performed at room temperature and high temperature.

In Chapter 4, the static and dynamic characterization of a new device is presented. This device is a vertical GaN transistor and currently, the only vertical GaN transistor which has been successfully switched up to 450 V. These results are included as well as the introduction of a dynamic on-state resistance measurement board for further testing of this device.

Chapter 2 Static and Dynamic Characterization of Silicon Carbide (SiC) MOSFETs

Acknowledgment: This material is based upon work supported by the U.S. Department of Energy, Vehicle Technologies Office (VTO) under Award Number DE-EE-0007285, Highly Integrated Wide Bandgap Power Module for Next Generation Plug-in Vehicles.

2.1 Background

Currently, the SiC MOSFET market is very competitive. Effort is being put into making the fastest device with the lowest losses. There are many key manufacturers which are leading the way by pushing the expectations of these devices to the next level. To keep up with all of the new devices coming out, the evaluation and comparison of the different capabilities of these new technologies is important. In this chapter, SiC MOSFETs from a four different manufacturers will be characterized and compared to each other. They are evaluated by being characterized in a static and a dynamic state. A detailed explanation of how these two characterizations are performed is also given.

For easy comparison, the devices tested have been split into three different groups, which can be seen in Table 1. The grouping is based on the on-state resistance range of the devices and therefore, the amount of current they are able to handle. The first group

contains two devices, named Device A and Device B. These two devices have the lowest on-state resistances out of all of the devices. Device A is rated for a continuous current of 75 A, and the continuous current rating of Device B has not yet been provided by the manufacturer but it is assumed to be around 75 A during testing. The second group contains two devices with an on-state resistances of 23 mΩ and 25 mΩ, Device C and Device D respectively. Finally, Group III contains the remaining two devices with the two highest on-state resistances. Most of the devices are rated for 1200 V except for the Device A which is rated for 900 V and the Device C which is rated for 850 V.

Table 1: Summary of SiC MOSFETs tested and their grouping

	Manufacturer	Voltage Rating	Continuous Current Rating	Rds-on	$Rg_{internal}$	Gate Drive Voltage	Package
Group I	Device A	900 V	95 A	10 mΩ	1.8 Ω	-4 to 15 V	TO-247
	Device B	1.2 kV	-	15 mΩ	-		TO-247
Group II	Device C	650 V	100 A	23 mΩ	1.5 Ω	-5 to 20 V	HiP-247
	Device D	1.2 kV	70 A	25 mΩ	0.5 Ω	-5 to 20 V	TO-247
Group III	Device E	1.2 kV	48 A	45 mΩ	5 Ω	-5 to 15 V	TO-247
	Device F	1.2 kV	20 A	80 mΩ	1.5 Ω	-5 to 20 V	TO-247

2.2 Static Characterization of SiC MOSFETs from different Manufacturers

2.2.1 Overview of the Static Characterization

The static characteristics are measured using the B1505A Curve Tracer from Keysight. For the static characterization, different parameters of the device are swept while the response of the device is observed. Using the curve tracer allows for high controllability of

the different sweeps performed as well as accurate measurement of the device's currents and voltages. The static characterization can include many different tests but in this case it includes: on-state resistance, output characteristics, transfer characteristics, threshold voltage and device capacitances. High temperature results will also be included for the on-state resistance and the threshold voltage measurement. Fig. 1 shows an image of how the static characterization is performed. The device is inserted into the TO-247 adapter and then different parameters are set using a computer and curve tracer software. A thermocouple is also included for temperature monitoring during the high temperature testing. The high temperature static characterization is performed by heating the device with a hot plate.

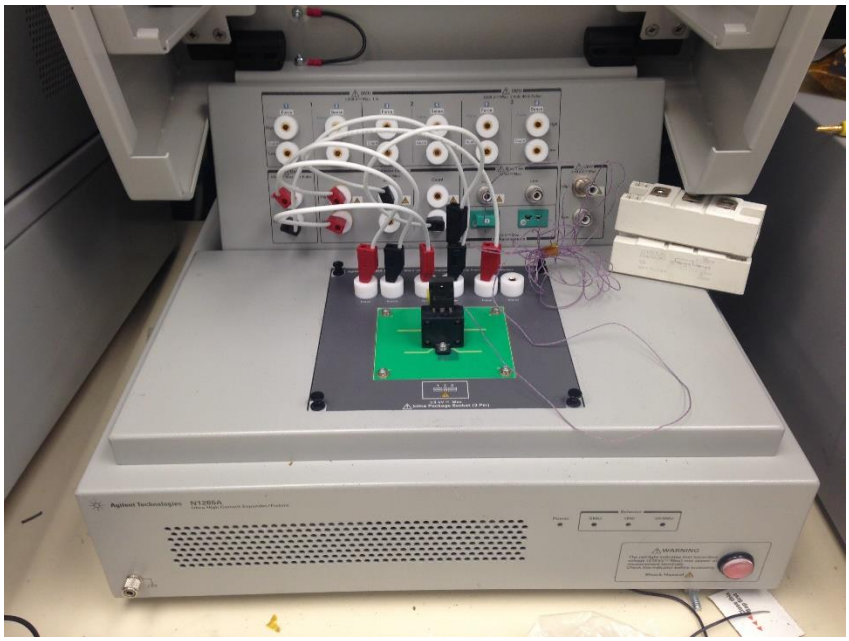

Fig. 1: Curve tracer used to perform the static characterization with the device

2.2.2 Output Characteristics and On-State Resistance

The output characteristics of all of the devices were tested. The output characteristics are obtained by sweeping the drain-source voltage of the device and observing the resultant

drain current. This is usually done for different steps of gate-source voltages to see the response of the current due to changes in drain-source voltage. This plot can also be used to obtain the on-state resistance of the device by dividing the drain-source voltage by the drain current at a specific point.

Fig. 2 shows the output characteristics for the three groups of devices. All of the curves are shown for the gate-source drive voltage recommended by the manufacturer. As mentioned before, the slope of the curve represents the on-state resistance of the device, therefore the devices in Group I have the steepest slopes out of all of the devices.

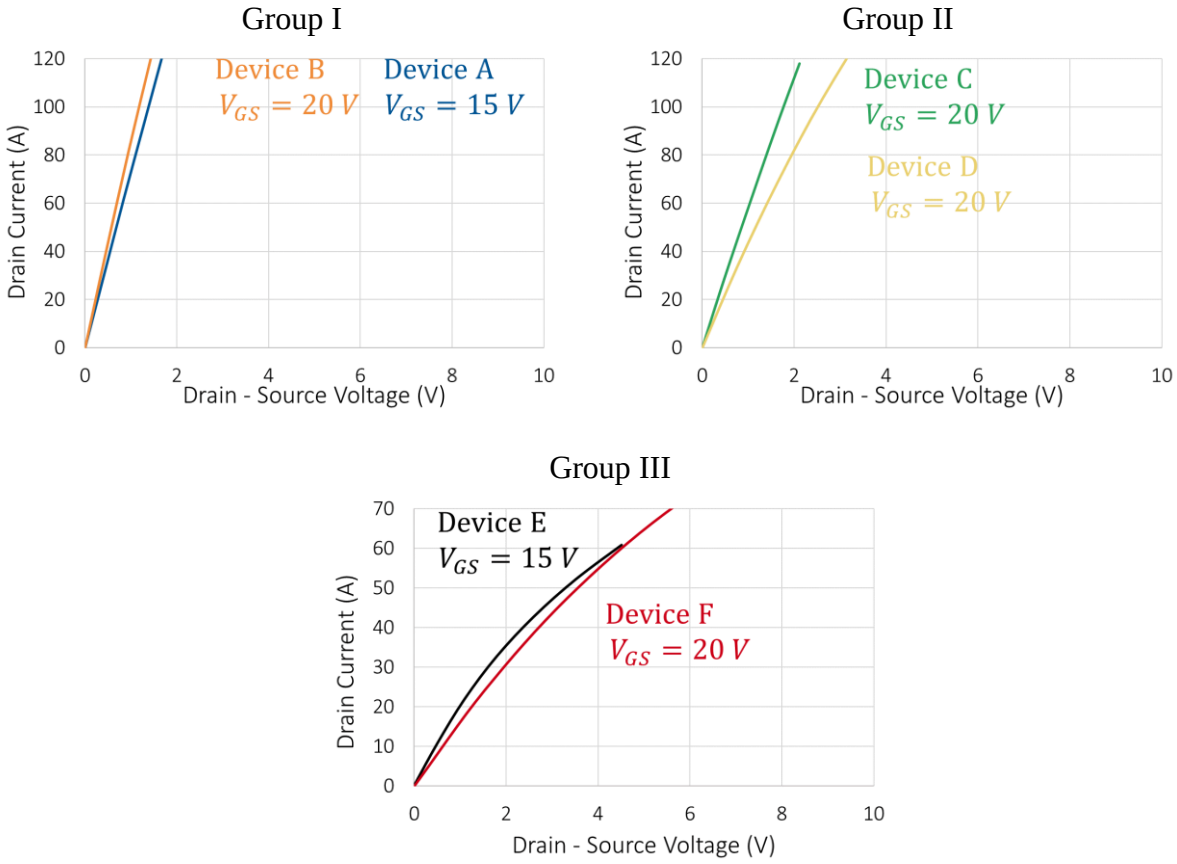

Fig. 2: Output characteristics for all device taken at their recommended gate drive voltage

Fig. 3 shows the on-state resistance of both of the devices from Group I as a function of current. Ten devices of Device A were tested and they had a very small variation. On the other hand, two devices of Device B were tested and the resultant curves for both devices are included in Fig. 3. There is a very significant difference between the two. For the remaining characterization results (static and dynamic), the results shown for Device B will be tests performed on the device with the lower on-state resistance of these two devices.

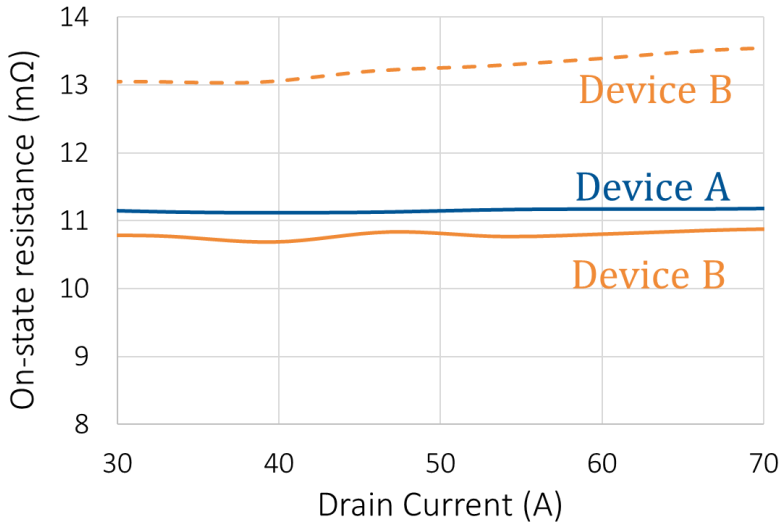

Fig. 3: On-state resistance against current for Group 1, Device A (10 mΩ, 900 V) and Device B (15mΩ, 1.2kV)

Fig. 4 shows the on-state resistances of the devices over temperature. The slope of these curves represents the dependency that the temperature has on the on-state resistance. Device C in Group II has the lowest dependence and the on-state resistance and stays relatively constant and Device F in Group III has the highest temperature dependence where the on-state resistance increases 75%. In real switching conditions, the device has a self-heating affect which in most of the devices will cause an on-state resistance increase, which increases conduction losses. Since Device C is able to keep a constant on-state

resistance at higher temperatures that means in switching conditions, the conduction losses will remain mostly constant.

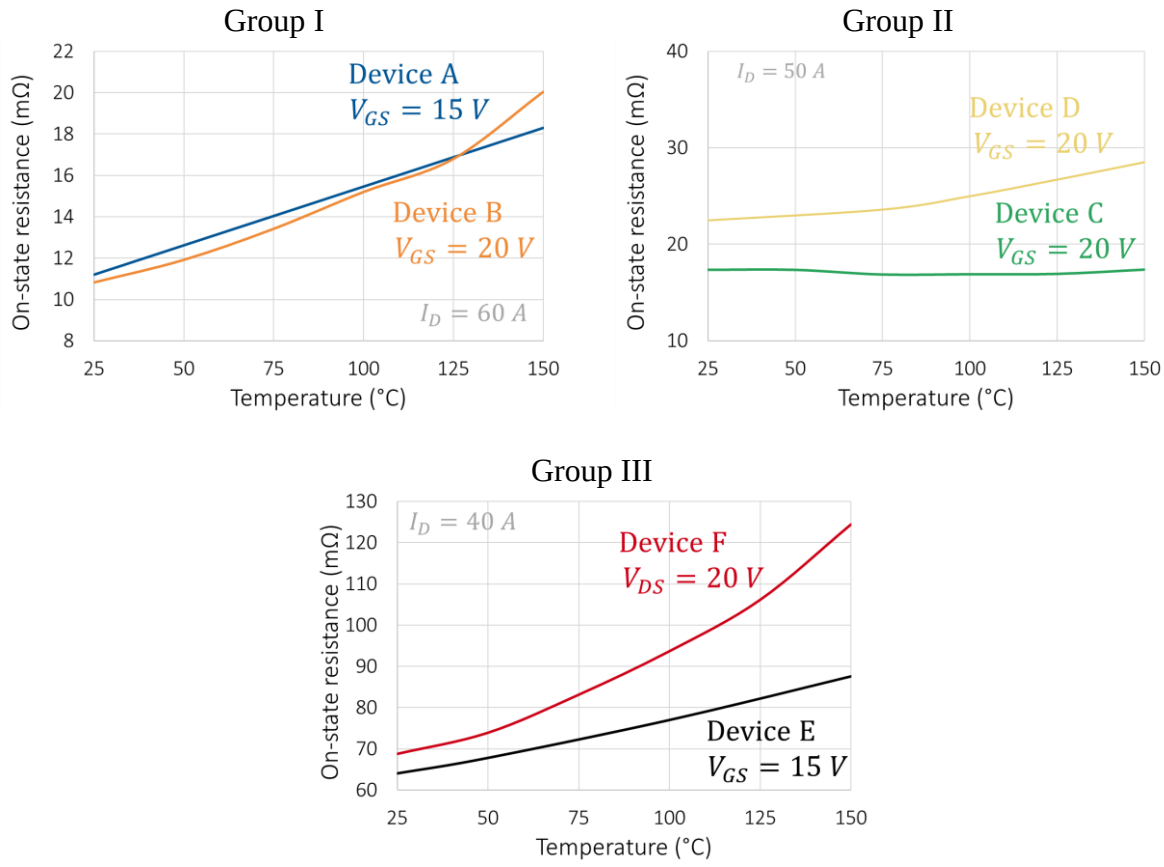

Fig. 4: Temperature dependence of the on-state resistance for all three groups of devices

2.2.3 Transfer Characteristics

The transfer characteristics are found by keeping the drain-source voltage constant and sweeping the gate-source voltage. The slope obtained in this graph shows the sensitivity of the drain current in relation to the gate-source voltage. Fig. 5 shows the transfer characteristics for the three groups. The sweeps are all performed at a drain-source voltage of 20 V.

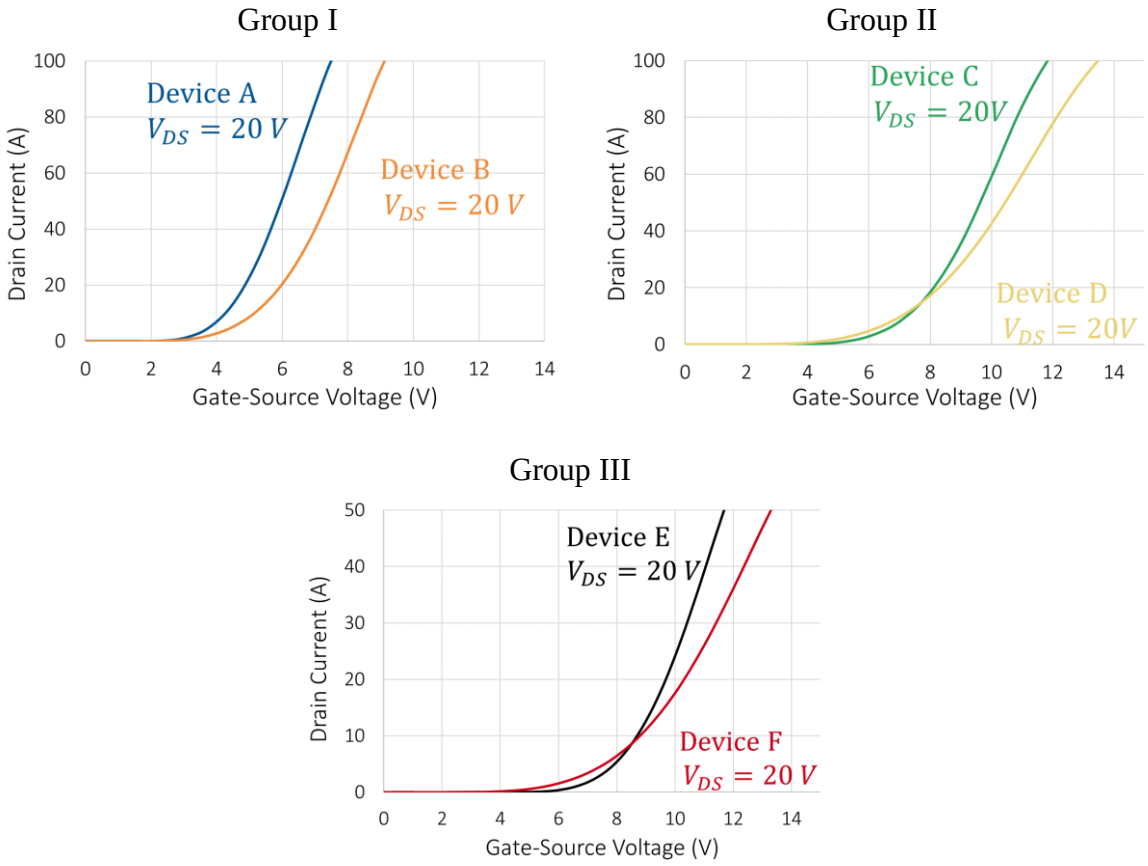

Fig. 5: Transfer characteristics tested at a constant drain-source voltage of 20 V

The threshold voltage is also found similarly to the transfer characteristics by sweeping the gate-source voltage at a constant drain-source voltage. In this case though, the gate-source voltage is pulsed more often as to not overheat the device. Heating the device would result in a different threshold voltages. The threshold voltage is then found by looking at what voltage the drain current reaches a specified value. The threshold voltage is the voltage at which the device is considered on. This current therefore, varies from manufacturer to manufacturer. For consistency, in this case, the threshold voltage is defined as the gate-source voltage for which the device current reaches 10 mA. This was done at a room temperature of 25°C and up to 150°C and the results for the devices are shown in

Fig. 6. As the temperature increases, the threshold voltage decreases. This is the opposite effect that temperature has on the on-state resistance.

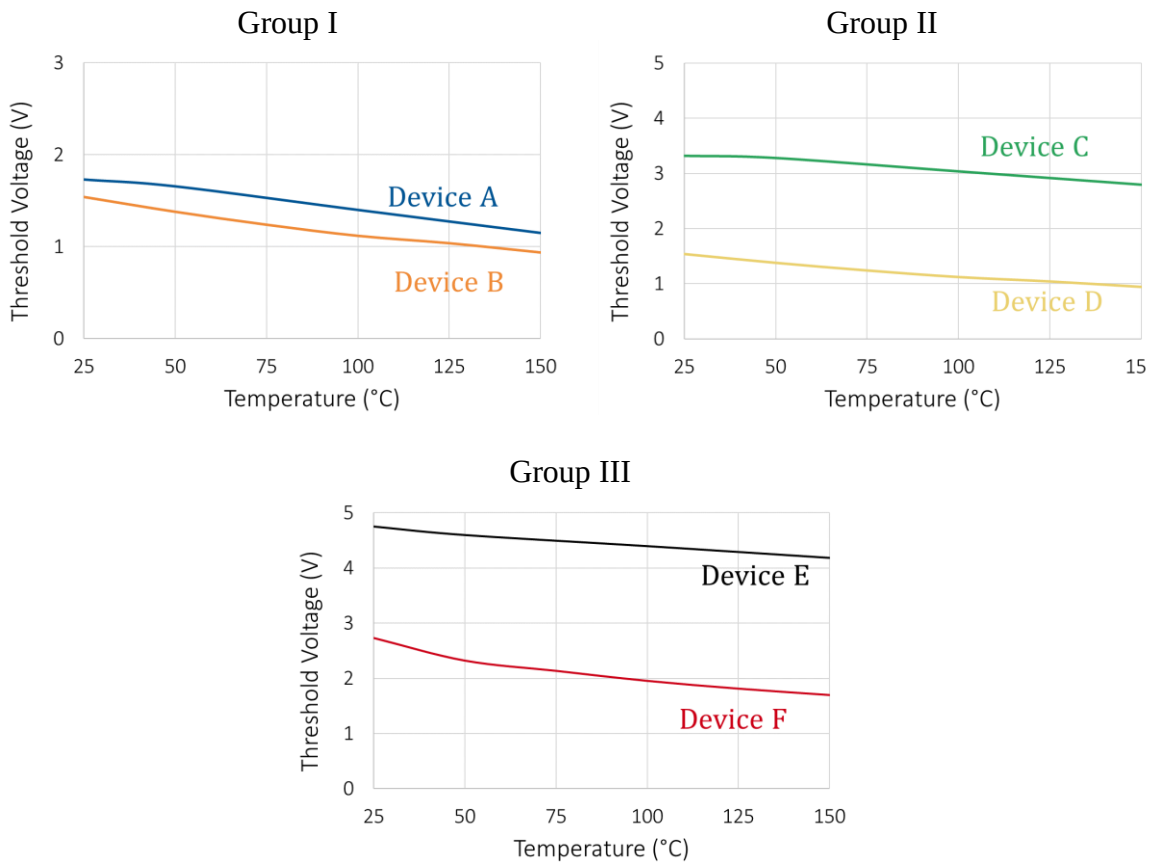

Fig. 6: Threshold voltage over temperature measured at a drain current of 10 mA

2.2.4 Devices Capacitances

The capacitances were measured at 100 kHz. Fig. 7 shows the set-up configuration used to find the capacitances in the curve tracer [21]. The capacitance results for the devices is shown in Fig. 8. The capacitances affect the switching speeds of the devices [22]. Smaller capacitances are preferred, especially for the input capacitances because then less time is needed to charge up the capacitor before it turns on or to discharge before it turns off. The

device capacitances are all tested up to 600 V, except for Device C which was only tested up to 400 V because of its rated voltage of 650 V.

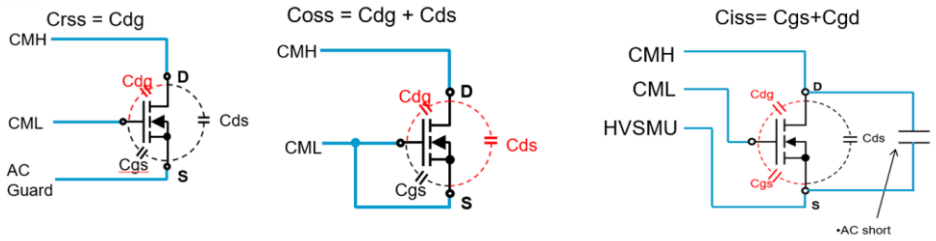

Fig. 7: Capacitance Measurement Set-ups

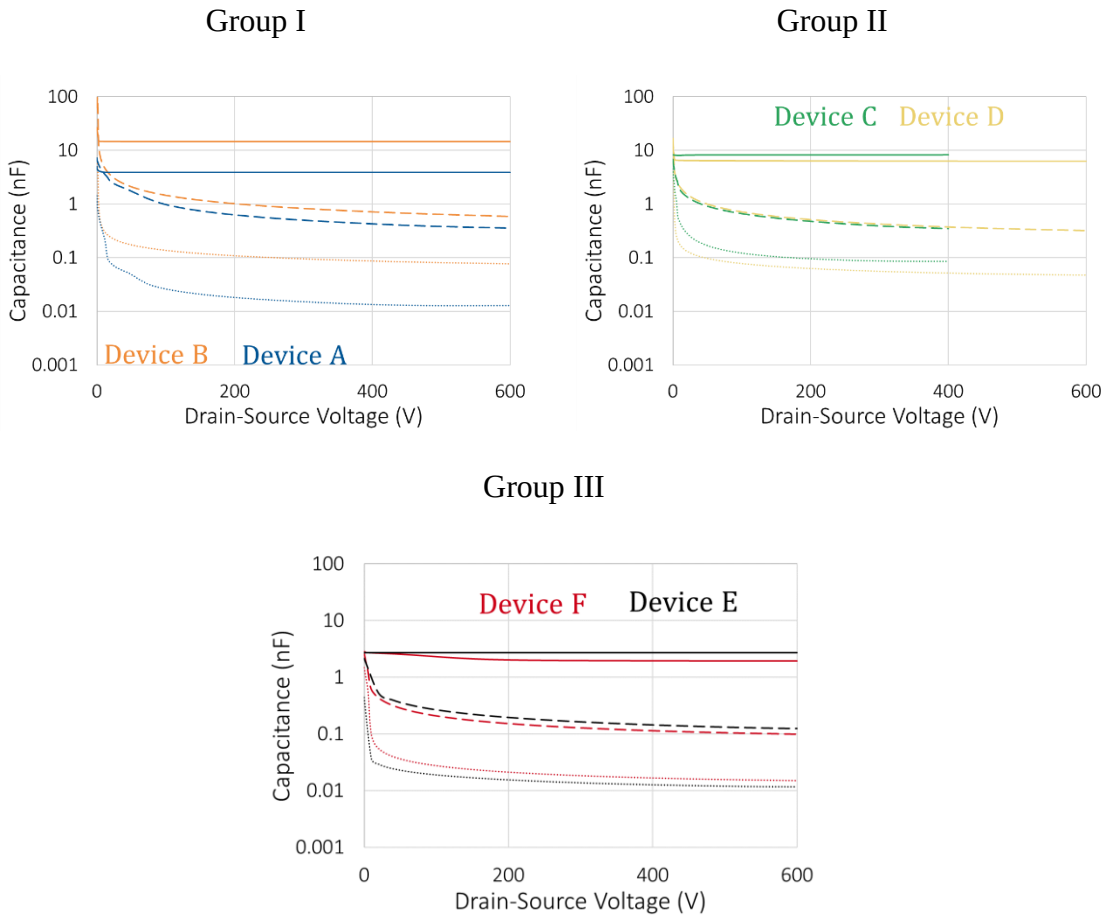

Fig. 8 : Input (solid line), Output (dashed line) and Miller (dotted line) capacitances measured at a frequency of 100 kHz for all three groups

2.3 Dynamic Characterization of SiC MOSFETs from Different Manufacturers

So far, the static characteristics have shown an overview of what the devices are capable of at room temperature and high temperatures. Dynamic characterizations are a necessary addition to the assessment of the devices because it allows a look at the devices under switching operation. When in switching operation, the devices are put under a lot more stress than the static characteristics because they are tested at higher voltages and higher currents. These tests give insight into the switching speeds of the device, as well the losses the device exhibits when switching. This information is useful when selecting the most efficient devices for power converter designs.

2.3.1 Overview of Dynamic Characterization Test Set-up

To test the switching of the devices, a clamped inductive load test is used. Essentially, this test circuit consists of a single device in series with an inductor and an antiparallel SiC Schottky diode. A simplified version of the circuit is shown in Fig. 9.

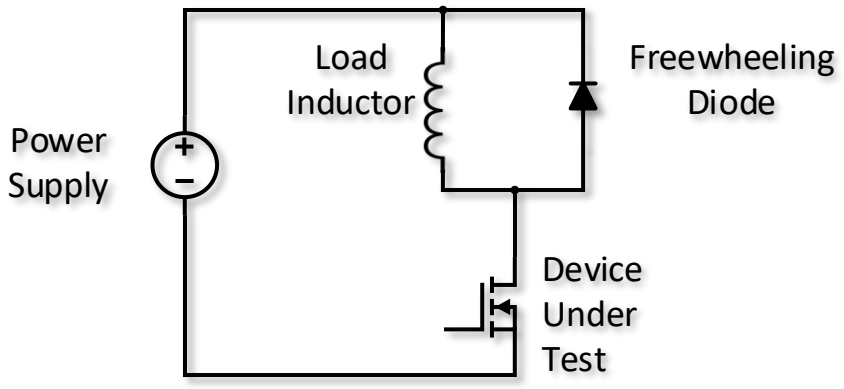

Fig. 9: Simplified circuit for the clamped inductive load test

A double pulse is used to turn the device on and off, therefore the test is also called the "Double Pulse Test". The expected waveforms for this test are shown in Fig. 10. As can be seen from the figure, two pulses are given to the device via the gate terminal. The first pulse is usually longer as it is used to charge the inductor up to the desired current. The device is then turned off and the current, which was stored in the inductor, freewheels between the inductor and the anti-parallel diode. Ideally, this will keep the current at the same level but due to inductor and diode losses, it will decrease a little bit. After a short amount of time, the device is then turned back on at around the same current level and then the device is turned off again. These two transients are used to calculate the different switching characteristics. [23]

The length of the first pulse is chosen based on the current load needed. The equations below show how the time is calculated where the drain voltage, current load level, and inductance of the inductor are all taken into consideration. The time between the pulses is kept as short as possible so that the current doesn't drop too much but it needs to be long enough that the voltage and current waveforms reach steady-state. The second pulse is also kept short so that the inductor doesn't keep charging up and change the current level but again it is also kept long enough that the waveforms have time to settle.

$$\boldsymbol{V = L\frac{di}{dt}} \quad \textbf{(2-1)}$$

$$\boldsymbol{di = dt \times \frac{V}{L}} \quad \textbf{(2-2)}$$

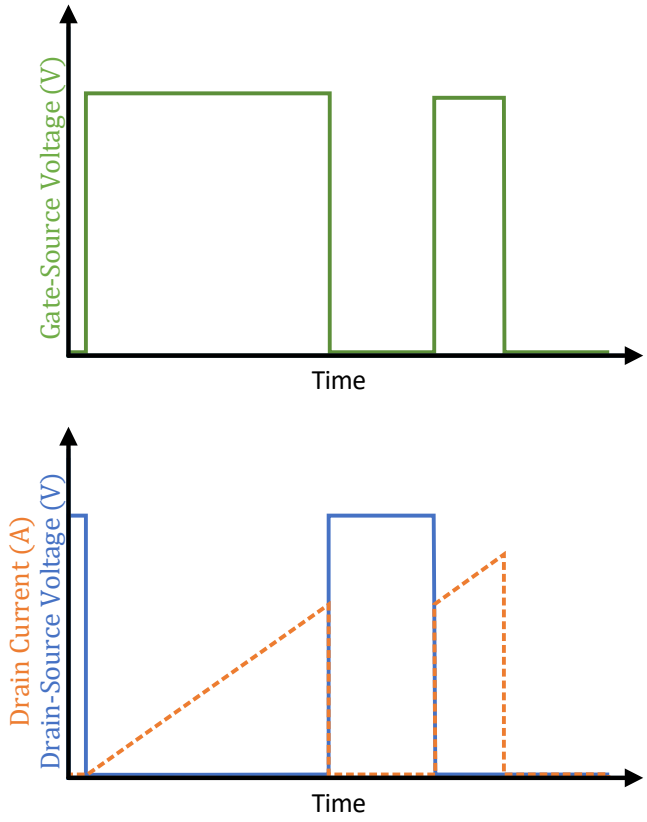

Fig. 10: Sample waveforms for the double-pulse test operation

The sample waveforms in Fig. 11 and Fig. 12 show a closer up view of the turn-on and turn-off behavior of the device respectively. These waveforms are taken from tests performed on Device B. They also show the different definitions during the switching transients. In this paper, the turn-on time is measured from 10% of the gate-source voltage to 10 % of the drain-source voltage. The turn-off time is measured from 90% of the gate-source voltage to 90% of the drain-source voltage. [24]

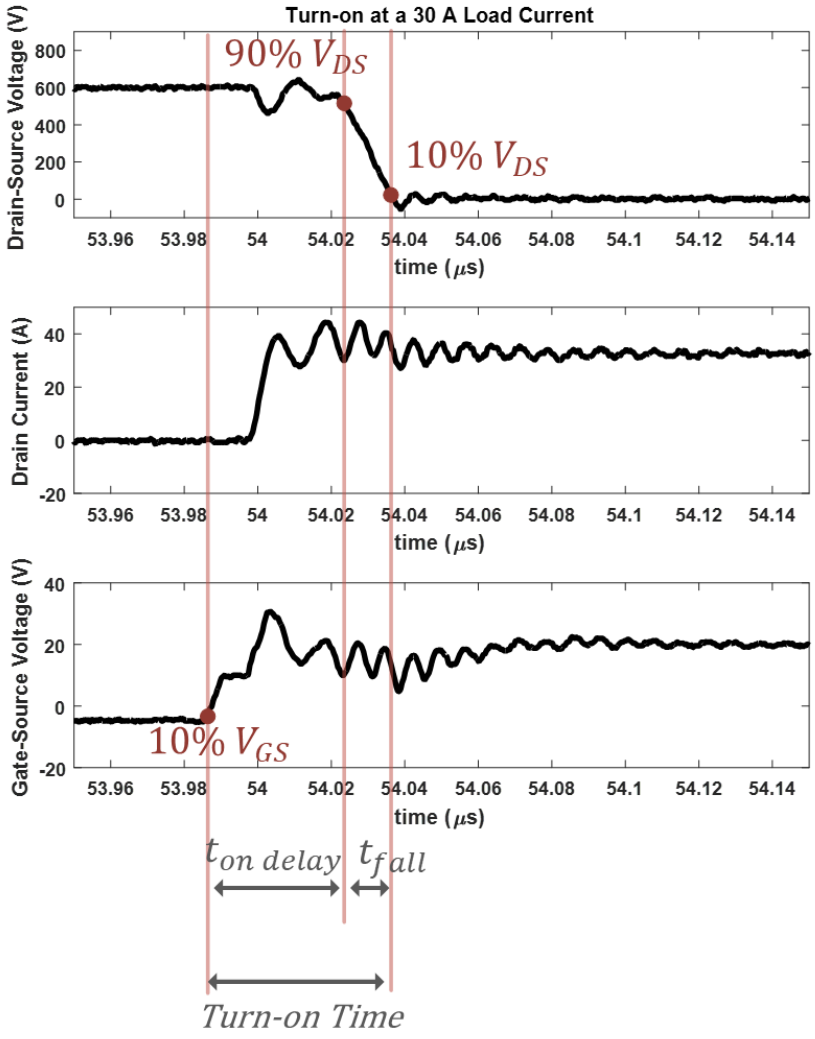

Fig. 11: Turn-on time definitions using a Device B waveform at 600 V, 30 A

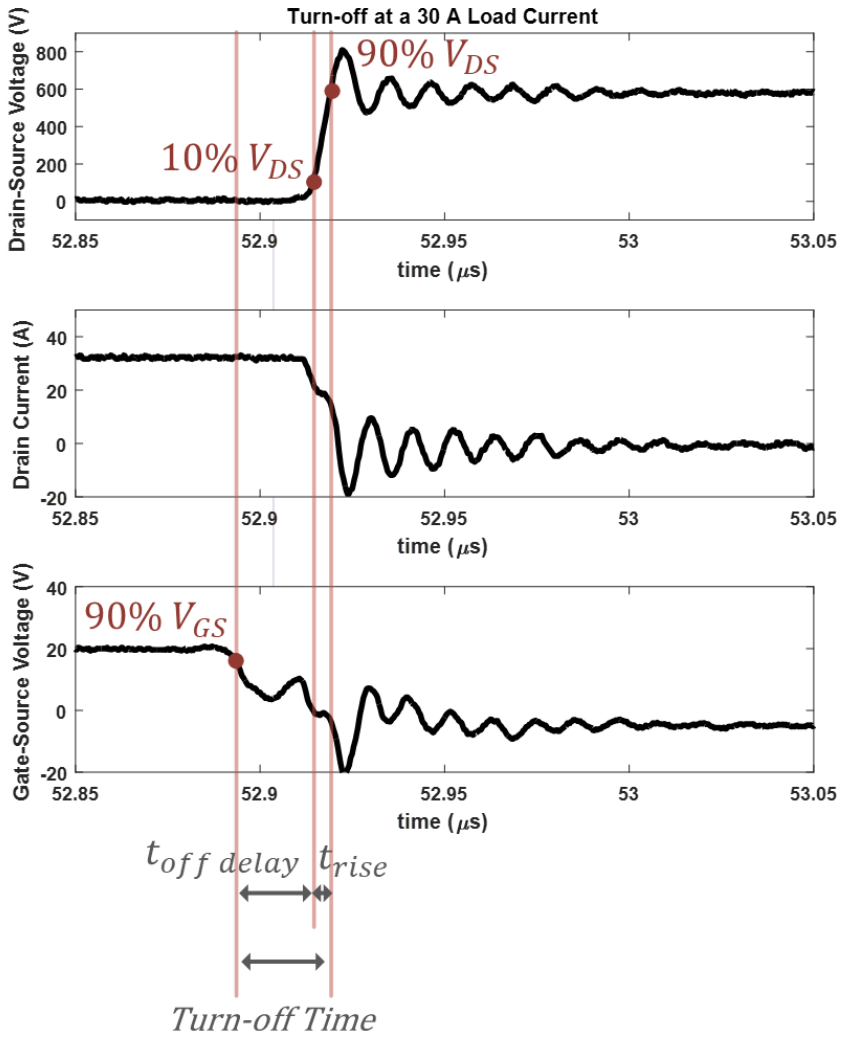

Fig. 12: Turn-off time definitions using a Device B waveform at 600 V, 30 A

To calculate the switching losses, the instantaneous power is needed. This is found by taking the drain current and the drain-source voltage waveforms and multiplying them by each other. Fig. 13 shows the mentioned current and voltage waveforms and Fig. 14 shows the instantaneous power waveforms at turn-on and turn-off. There is a large increase in the power as the device switches. The areas under the curves are taken from 10 % max power on both sides using the trapz function in MATLAB. This calculates the area under the curve

using trapezoidal summations. These values then represent the switching losses in joules at turn-on and turn-off.

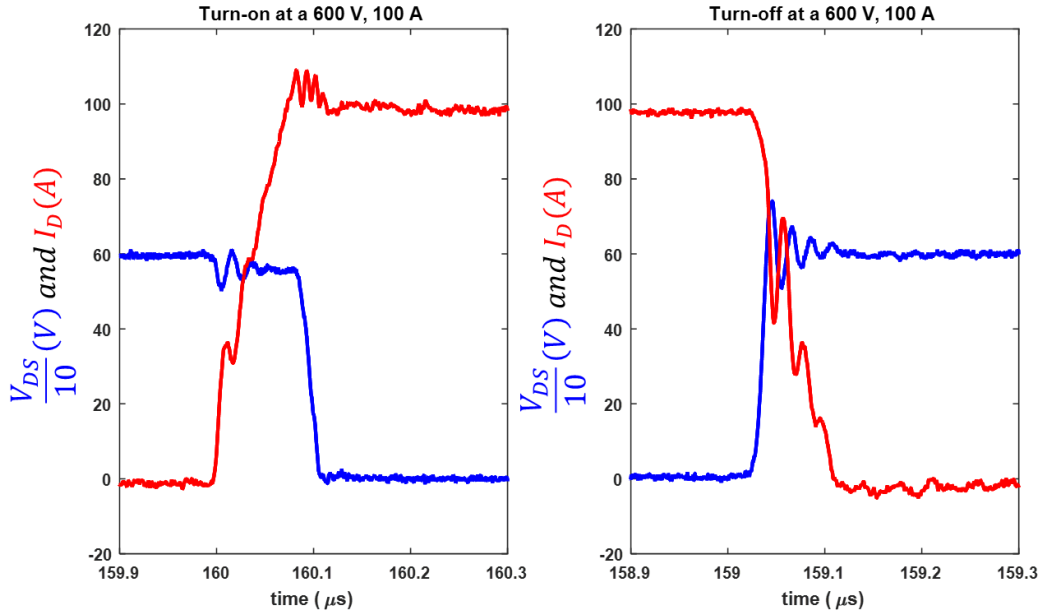

Fig. 13: Example waveforms during turn-on and turn-off to show how the switching parameters are calculated

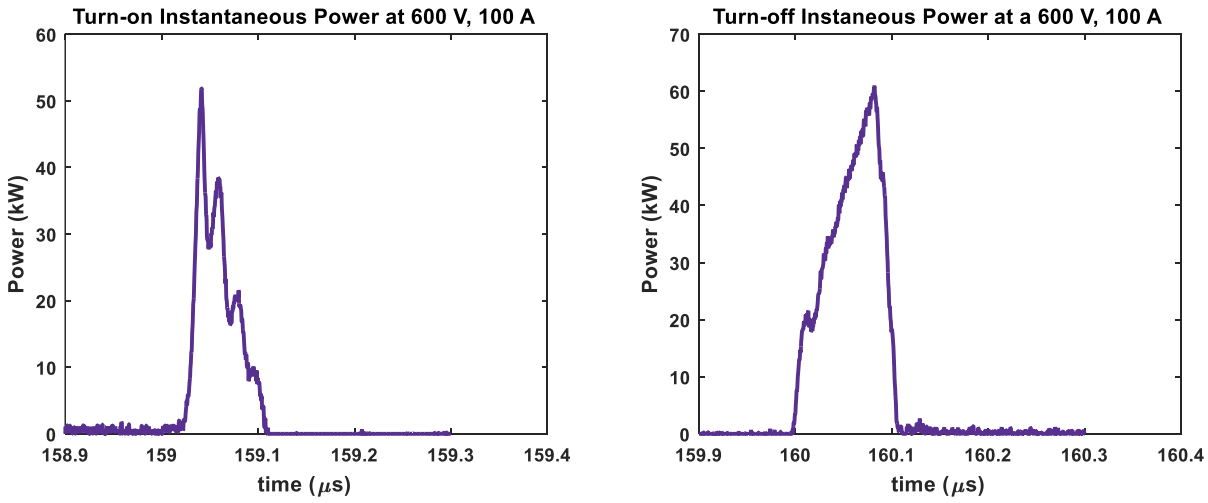

Fig. 14: Using the instantanteous power of Device A to calculate the switching losses during turn-on and turn-off

A more detailed overview of the double pulse test set-up is shown in Fig. 15. It highlights the gate driving stage and the power stage. The power stage consists of the power supply which is used to set the bus voltage. There are also capacitors included which are on the actual PCB. The capacitors make sure that there is enough immediate energy being supplied to the circuit. If the capacitor bank is too small, a lot of ringing can be seen in the output waveforms. In the gate driving stage, an input signal is fed through a digital isolator (ISO7221 MDR) so that the control signal is isolated. This signal then goes through the current booster IXDN630 which provides the driving signal from the negative gate voltage to the positive gate voltage recommended by the manufacturer. These rail voltages for the output gate voltage are set using Zener diodes on the PCB after being isolated via the isolated DC-DC converter (THB 3-2415).

The inductor is a 1 mH inductor which saturates above 100 A so it is suitable for testing these high current devices. The SiC Schottky diode is from Wolfspeed and has a rated continuous current of 20 A. Since the devices are being pulsed for short amounts of time, this current rating is not an issue.

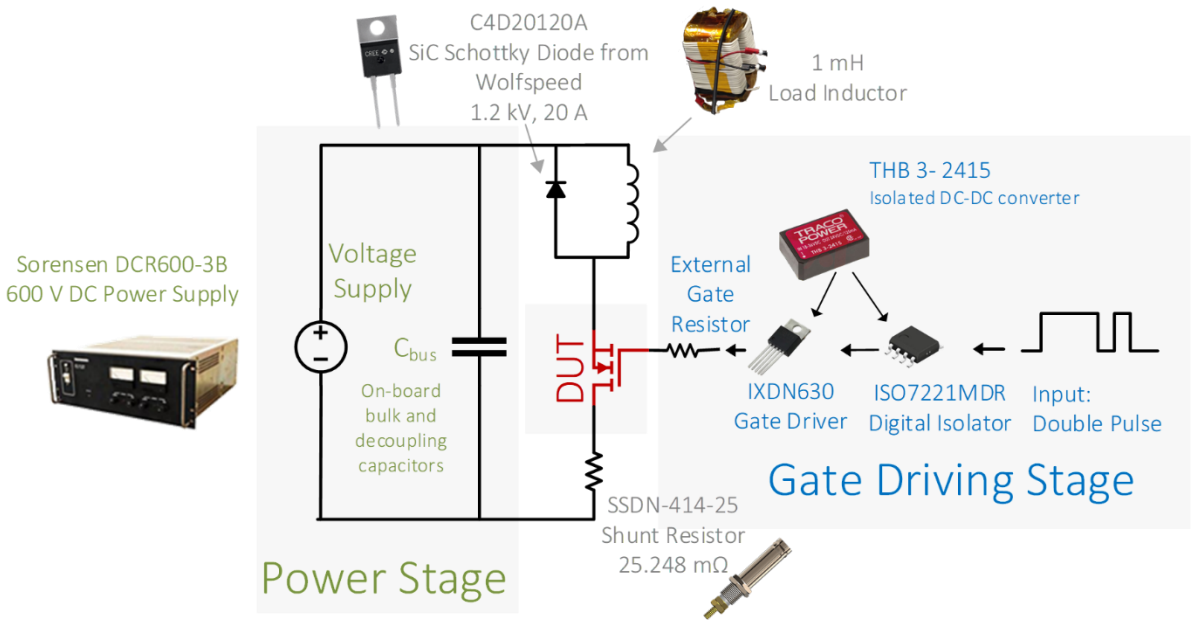

Fig. 15: Overview of the double pulse test set-up and PCB components

Fig. 16 shows the actual test set-up used for the double pulse test. The main components of the test set-up are labeled. The PCB used for testing is found in the middle of the figure. It contains the device under test, and the gate driver circuit as well as decoupling capacitors. The bulk capacitor bank is located externally and connected to the test board using cables. The load inductor is a 1 mH inductor with a current limit of 30 A. This inductor was only used for the lower current devices. The 1 mH inductor shown in Fig. 15 was used for the current devices with higher current ratings because it doesn't saturate at low currents.

The thermocouple monitor allows for the temperature of multiple different components on the PCB to be monitored. This is useful during high temperature characterization so that the device temperature can be seen but also the other PCB components can be observed so that they do not overheat. The fan is also included in the set-up for the same reason. The PCB cannot overheat or some of the components may fail. The high temperature test set-

up is also shown in Fig. 17. In this figure, the hotplate is positioned so that it heats up the device with little heat going towards the PCB (and other components).

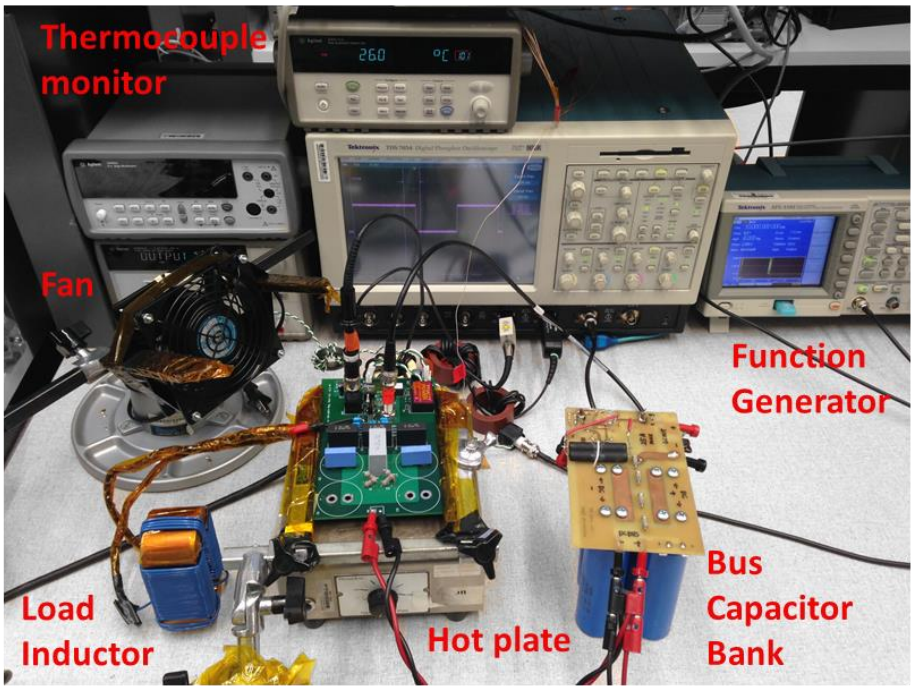

Fig. 16: Double pulse test set-up used to characterize the switching of the SiC devices with key components labeled

Fig. 17: Test set-up for high temperature switching characterization of the SiC MOSFETs

The actual device under test is connected so that it is hanging from the bottom of the PCB. It is then bent so that it can sit flat against the hot plate. This is shown in Fig. 18.

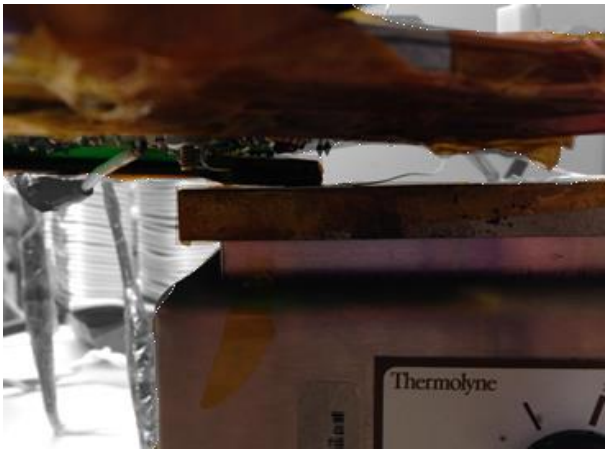

Fig. 18: Location of the device under test on the hot plate used for high temperature switching characterization

2.3.2 Dynamic Characterization Test Results

The dynamic characterization tests are performed under different current load conditions. Once the bus voltage is brought up to 600 V, the device is pulsed for different current loads up to a certain current based on the rating of the device. For example, for Device A (900 V, 10 mΩ), the device was pulsed for 5 A, 10 A, 15 A, 20 A, 25 A, 30 A and then every 10 A up until its rating of 100 A. This is first done at room temperature and then it is repeated for 50°C, 100°C, and 150°C. All of the dynamic tests are performed with an external gate resistance of 3 Ω. This is so that there is a uniform measurement between all of the devices. They all have different internal gate resistances but that is a factor of the device which is evaluated during the dynamic tests. The 3 Ω external gate resistance should slow all of the devices down the same amount and will make sure there are no high voltage overshoots.

During the testing, the drain-source voltage, gate-source voltage and the drain current are all monitored. The drain-source voltage is measured using a 2.5 kV single-ended passive probe (Tektronix P5100) that has a low parasitic capacitance. In this way, more precise measurements of the drain source voltages are performed. The high voltage probe is connected to the board through a BNC connector, minimizing unwanted electrical parasitics in the test set-up.

Similarly, the gate-source voltage is measured using a 300 V single-ended passive probe (Tektronix P6139B) with a low parasitic capacitance, providing accurate measurements of the gate voltages during turn-on and turn-off transients. In this case, it is important to monitor the gate voltage precisely and make sure voltage overshoots and undershoots during switching do not exceed the device gate voltage rating. The low voltage probe is connected to the board through an adapter that minimizes electrical parasitics in the set-up.

The drain current is measured using a 25 mΩ current shunt resistor from T&M research. The current shunt resistor is used because it provides accurate measurements and it has a high bandwidth. This specific shunt resistor has a bandwidth of 1200 MHz which is much higher than a Rogowski coil's bandwidth. A Rogowski coil from CWT which is capable of measuring the same current levels has a low frequency bandwidth of 9.2 MHz and a high frequency bandwidth of 30 MHz [25]. Current shunt resistors are able to measure DC currents so they don't have a low frequency bandwidth. Also, the high frequency bandwidth allows for accurate measurements during fast transitions.

Fig. 19 shows the total losses for all of the devices for different currents. As the current increases, the losses increase for all devices as expected. The total losses are the turn-on and turn-off losses added together. This gives an overview of the losses of all of the devices

and allows for comparison. At the lower currents, Device F and Device E have lower losses than the others, but they cannot reach the current levels that the other devices can. Device C has consistently the lowest losses because it was tested at 400 V, instead of 600 V like the others.

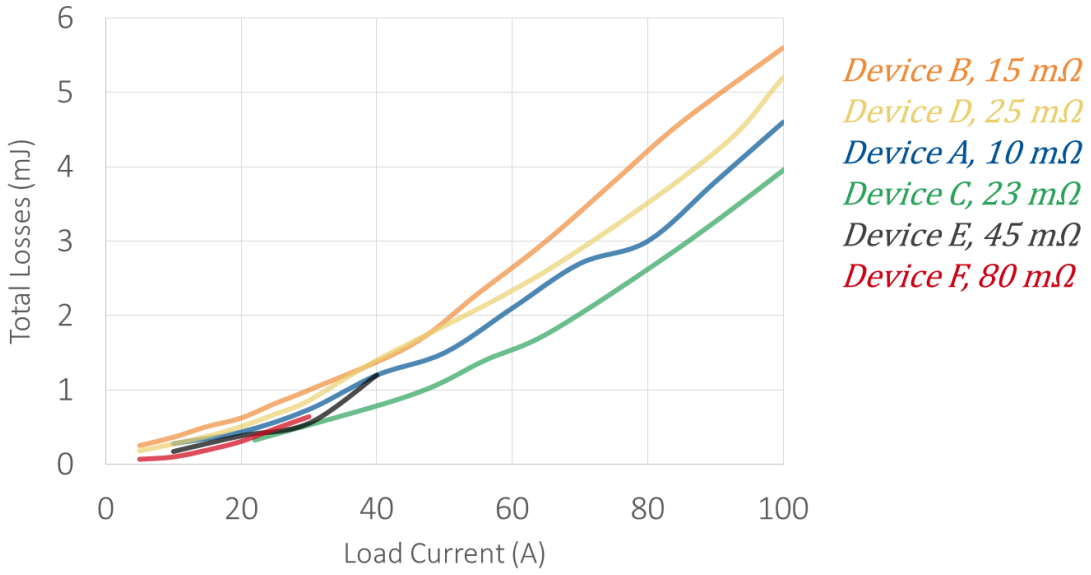

Fig. 19: Summary of total losses for all device tested, all at a bus voltage of 600 V (except Device C which was at a bus voltage of 400 V)

Fig. 20 and Fig. 21 show the high temperature turn-on and turn-off waveforms for Device A at a load current of 80 A, respectively. From the static characterization it is known that as the device gets hotter, the threshold voltage will get smaller. This can also be seen in these waveforms, as the device gets hotter, the device turns on faster due to the lower threshold voltage. This also affects the losses, Fig. 22 shows the turn-on and turn-off losses for the same high temperature waveforms. It can be seen that when the temperature is increased to 150 °C, the losses are lower for the turn-on. Alternatively, the turn-off losses slightly increase when the temperature is increased.

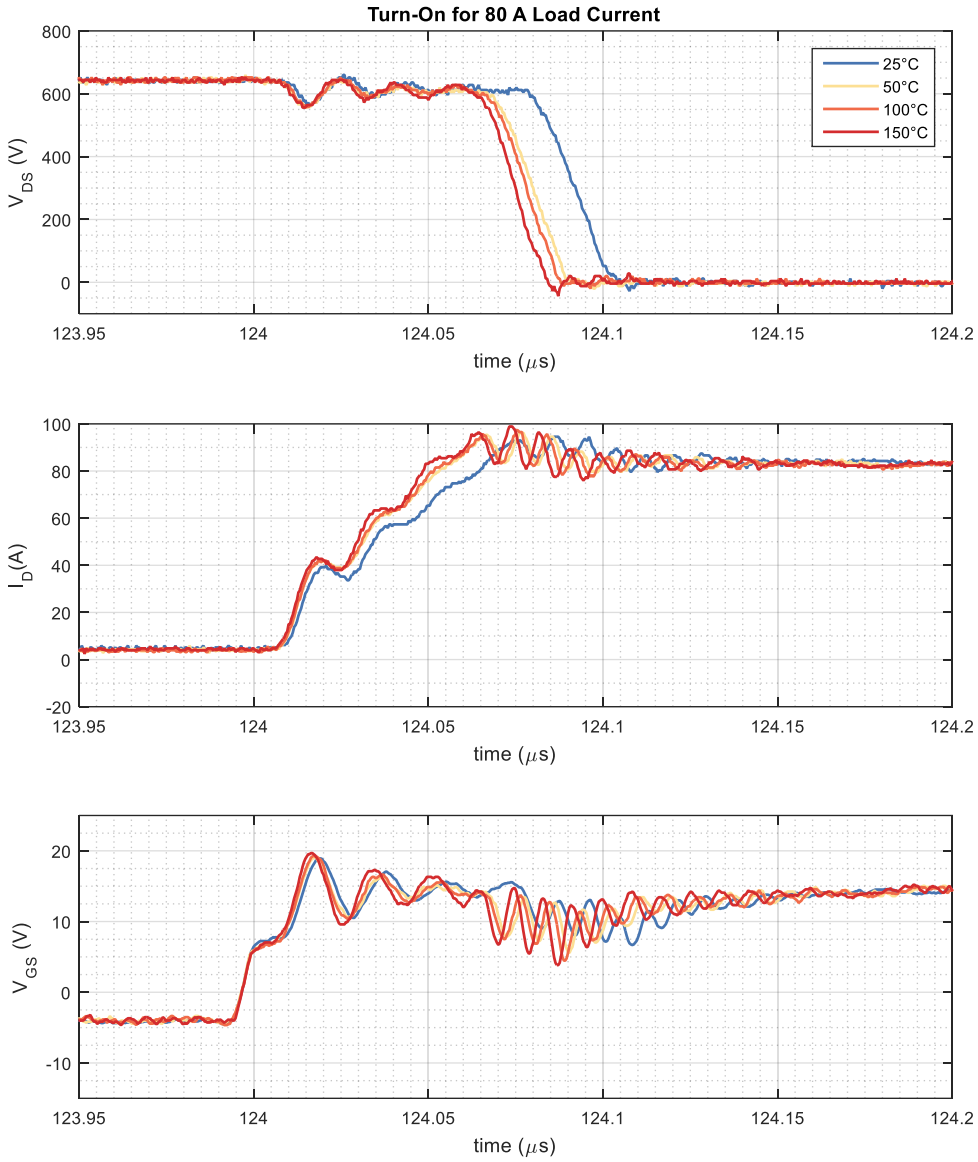

Fig. 20: Turn-on waveforms for Device A at a bus voltage of 600 V and a load current of 80 A at different temperatures

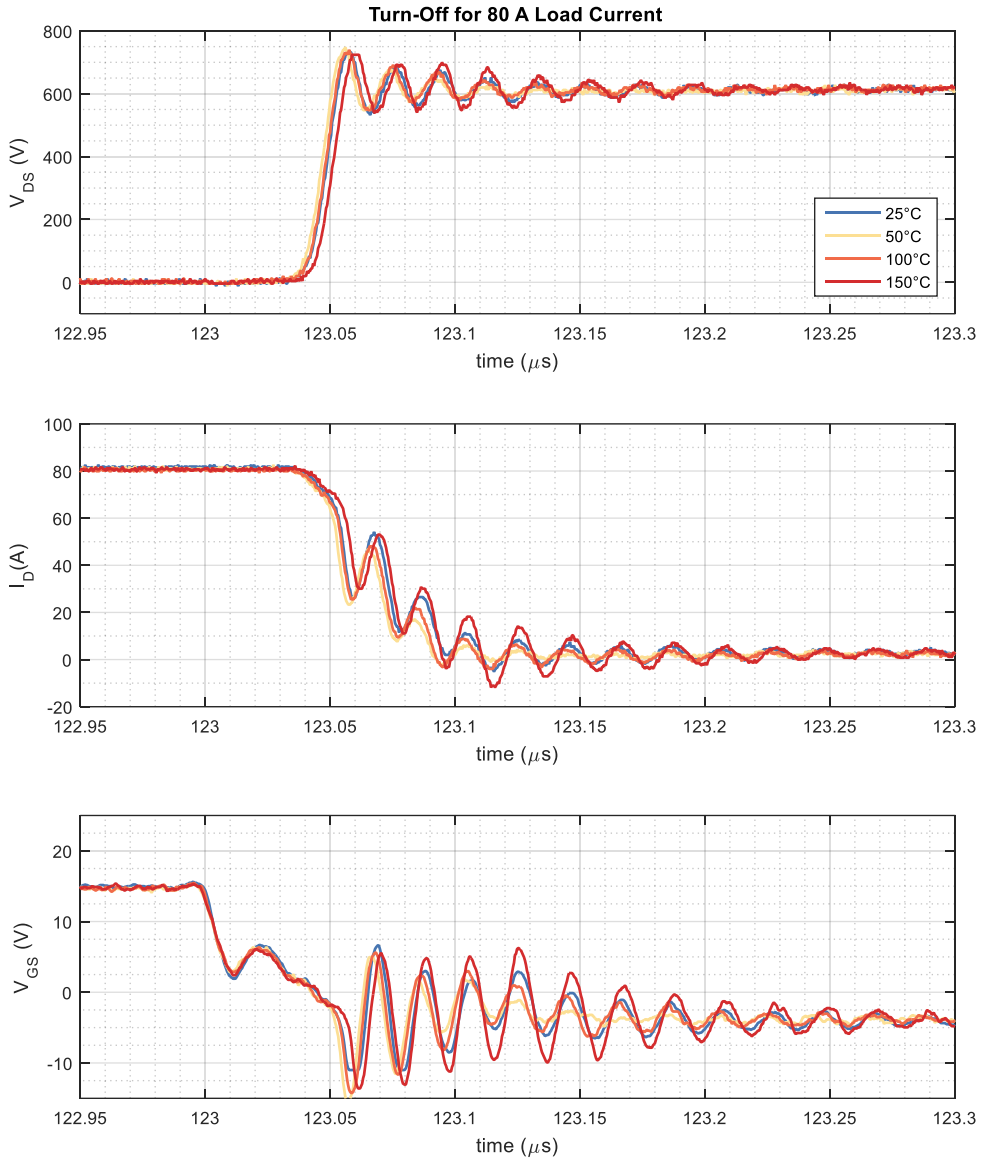

Fig. 21: Turn-off waveforms for Device A at a bus voltage of 600 V and a load current of 80 A at different temperatures

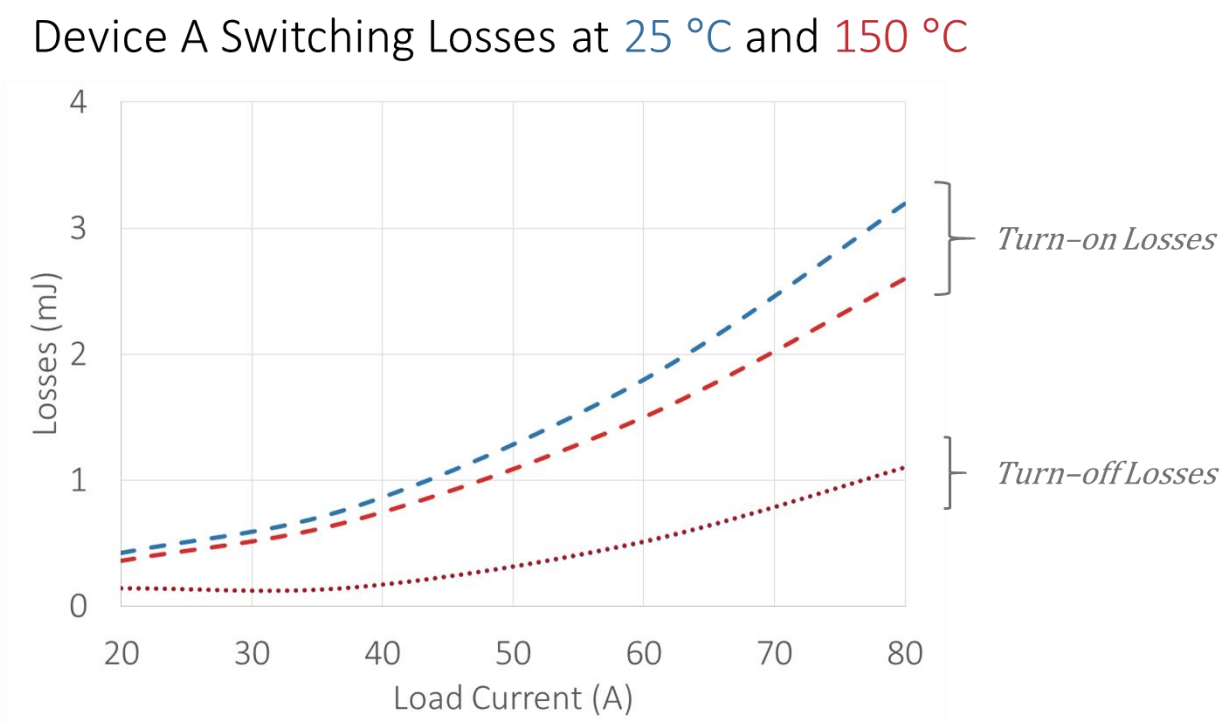

Fig. 22: Room temperature and high temperature switching losses for Device A at 600 V and varying currents

Fig. 23, Fig. 24, and Fig. 25 provide an overview comparison for all of the devices. Again, they are split into the three groups for comparison. All of the measurements are normalized to the data of Device A. The on-state measurement is useful because it gives a good idea of what losses are expected from the device and therefore the current carrying capability. The value is given at 100 °C because that is closer to operating temperature than room temperature. The breakdown voltage is included because there are three different rated voltages for the devices which are 650 V, 900 V and 1.2 kV. The turn-on and turn-off *dv/dt* demonstrate the switching speeds that the devices are capable of. The total losses provide an insight into the expected losses to be seen by the device during turn-on and turn off and allows for a direct comparison between the devices.

Group I

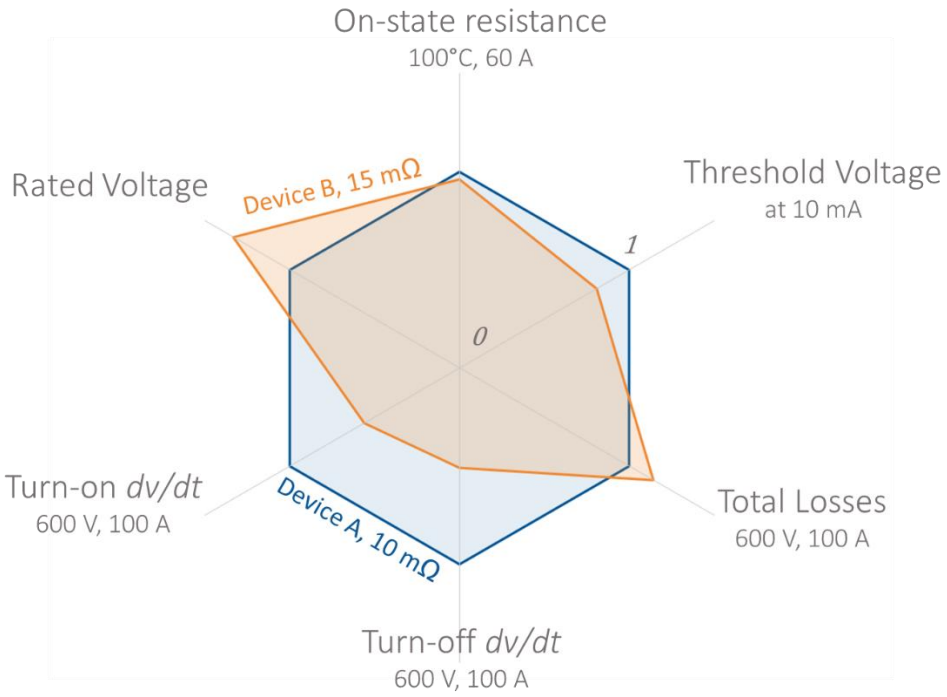

Fig. 23: Radar chart comparing different characteristics in Group I (normalized to Device A)

Group II

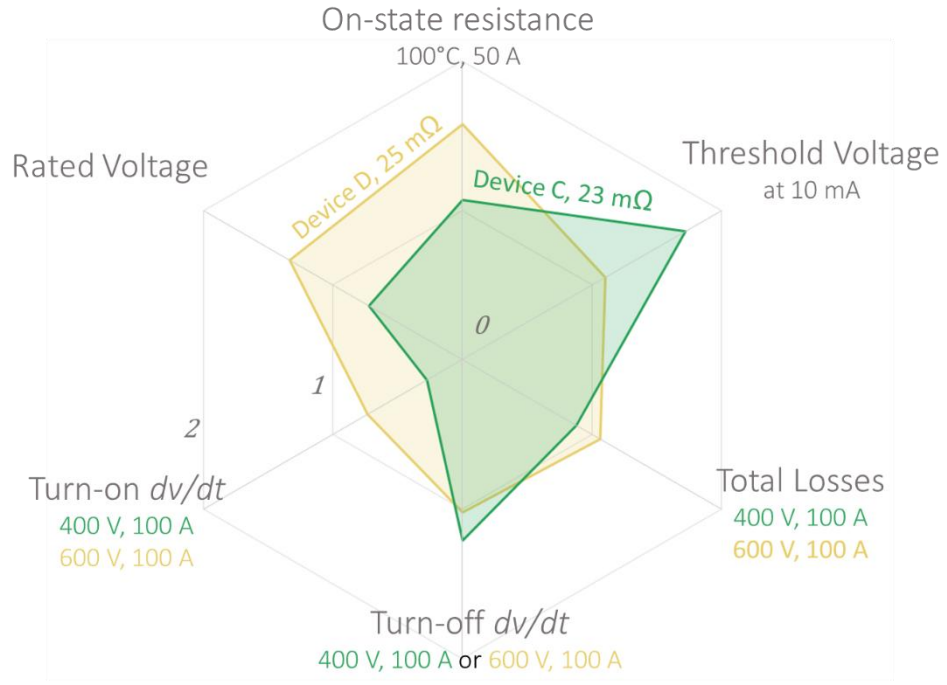

Fig. 24: Radar chart comparing different characteristics in Group II (normalized to Device A)

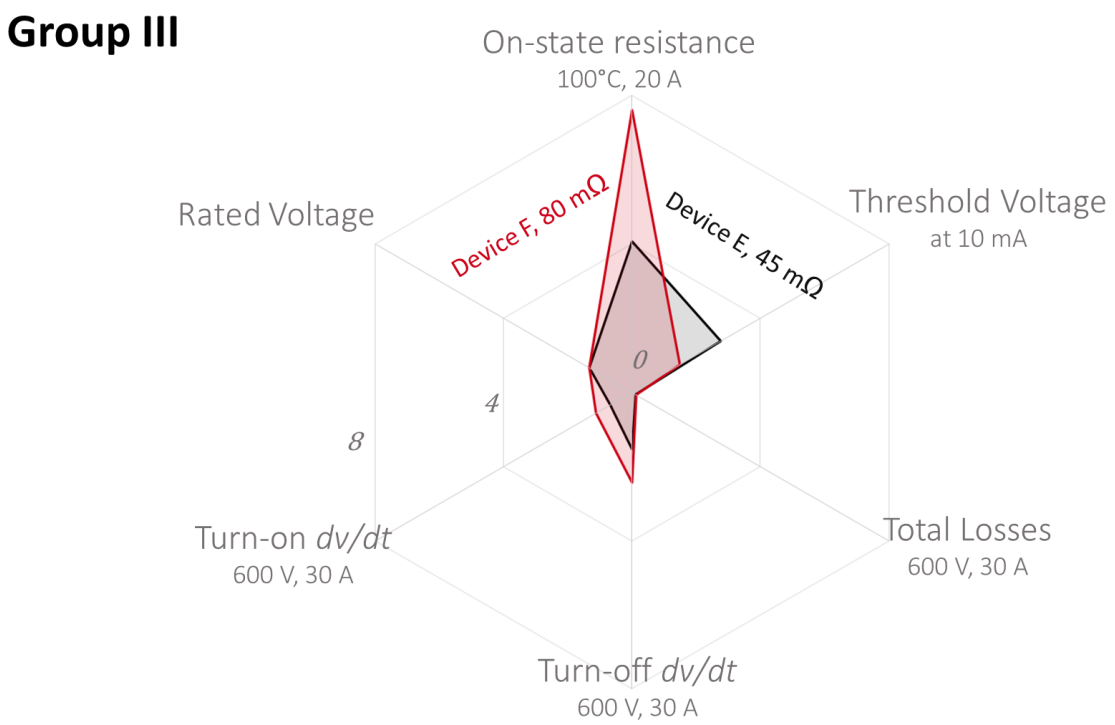

Fig. 25: Radar chart comparing different characteristics in Group III (normalized to Device A)

In terms of static characteristics results, Device A, Device C, Device D, Device E and Device F, have datasheet information which was provided by the manufacturer. The threshold voltages and on-state resistances for these devices were reported as ranges and the tested results fell within the reported range.

For the dynamic results, Device C and Device E have switching loss information provided up to the same bus voltage as tested in this study. Device C includes the turn-on and turn-off energy losses at 400 V and 50 A in their preliminary datasheet. The total switching losses add up to 550 µJ where as in this testing, the total losses were concluded

to be 1.2 mJ. One thing to note is that different external gate resistances were used (2.2 Ω contrary to the 3 Ω used for experimental data as stated previously). This difference in external gate resistance could slow down the turn-on and turn-off of the device and increases the losses. At 40 A and 800 V, for Device E, the datasheet reports total losses which are 37% different from the results shown above which were taken at 40 A and 800 V. Since the gate resistance in the datasheet test was 1.5 Ω higher than in this case and the results shown above are at 600 V instead of 800 V, the difference can be attributed to differences in the unit capabilities as well as differences between the test set-ups.

Due to these devices being so new, their datasheets are still preliminary. As seen with Device B, there is still some variation between individual devices and so creating a datasheet is premature.

Chapter 3 Short-Circuit Characterization of Silicon Carbide MOSFETs

Acknowledgment: This material is based upon work supported by the U.S. Department of Energy, Vehicle Technologies Office (VTO) under Award Number DE-EE-0007285, Highly Integrated Wide Bandgap Power Module for Next Generation Plug-in Vehicles.

3.1 Background on Short-circuit Testing

Up until this point, this paper has demonstrated test results for a newer generation of SiC devices. In comparison to Si devices, as well as the currently commercially available SiC devices, some of the data is showing significantly larger current capabilities, higher voltage levels and higher temperature operation abilities. In the case of the GaN devices demonstrated in the next chapter, faster switching speeds and the potential for higher powers are also shown. As the advancement of these technologies continue in terms of power capabilities and size reduction, the reliability and failure mode expectations will have to be updated also.

An important failure mode to be considered, especially in automotive applications, is short-circuit failure. This failure occurs when the MOSFET is shorted either through controls or a physical short and causes a surge in current through the device. This causes the device to heat up and usually the device is not able to handle this temperature range and it breaks. According to [26], some of the most dominant external causes of short-circuit failure are high temperature operation, thermal shock, vibration, shock, high humidity, as well as some others. These factors are all very relevant in most power electronics applications including automotive and aerospace.

There are different ways to deal with a short-circuit failure. One consideration is to have a packaging design that is more durable and can help the devices withstand the external influences described above that may cause a short-circuit failure, this is a preventive solution. Although this better design will help to decrease the risk of short circuit failure, there will still be the risk. The other method of dealing with a short-circuit failure is being able to lessen the damage by sensing when a failure occurs and stopping it. This corrective measure is usually implemented into the gate driver of a switch. By detecting the short-circuit, the gate driver can turn the device off before there is any destructive outcome. For this method to work though, a thorough understanding of how the specific device operates under short-circuit operation and how long it can withstand this condition is very important.

Since SiC has become more significant in the power electronics industry, there have been many different characterizations of these new devices operating in short-circuit conditions. When considering the difference between how the short-circuit robustness of silicon carbide and gallium nitride compare to silicon, one study found that out of three

similarly rated devices, the silicon device had the longest withstand time, with the SiC device coming in second. The shortest withstand was for the normally-off GaN HEMT and a cascade GaN HEMT was just slightly longer than that one [18]. Another study looking at a SiC MOSFET and a Si IGBT with similarly rated currents and voltages found that the SiC MOSFET had a considerably shorter short-circuit withstand time as well, due to the SiC MOSFET having a lower short-circuit current density and high electric fields at the p-n junction [27]. These two studies both show results that conclude that by abandoning silicon devices for more advanced devices like silicon carbide and gallium nitride, we also reduce the response time for short-circuit failure.

Knowing that different material devices have varying short-circuit withstand times is something to keep in mind when switching designs from one device to the other, another comparison of interest is looking at similar devices from different manufacturers to see if different production methods can have a large effect on the failure mode operation. When comparing different SiC MOSFETs with the same on-state resistance to each other [28], it was found that they have a similar peak short-circuit current in the range of 160 A – 200 A, which amounts to around 4 times the rated current of the three devices. The three devices were shown to have varying short-circuit withstand times with the shortest time being 12.5 μs and the longest being 18 μs. Similarly, the device type can also affect the short-circuit withstand time. SiC JFETs have been found to have a much longer short-circuit withstand time than SiC MOSFETs [29]. These various characterization studies have helped to define the parameters that are needed to design an effective gate driver short-circuit protection circuit for safe use of SiC MOSFETs, for example in [29][30].

The smaller size and higher power capability of SiC MOSFETs make them desirable but may make designing for failure operation mode harder. With a new generation of higher current SiC MOSFETs, as shown in Chapter 2, a new characterization is needed. As well as a new short-circuit characterization test set-up. The short-circuit currents that will be seen with lower on-state resistance devices are much higher than the studies mentioned. When looking at testing SiC MOSFETS, under short-circuit operation of SiC devices, specific boards are needed that can withstand the current levels that are being tested [31], new standards are also being developed on how to test short-circuit characteristics.

This chapter focuses on a short-circuit characterization of Device A which is a 900 V, 10 mΩ SiC MOSFET. A safe short-circuit test set-up is designed so that high currents can be tested without much damage to the test equipment. The tests conducted are split into two categories: non-destructive and destructive tests. The non-destructive tests consist of testing the devices in short-circuit operation for short pulses, for different drain-source voltages and gate resistances. The destructive tests subject the device to short-circuit operation for pulses long enough to destroy the device. These tests were done under room temperature and high temperature conditions.

3.2 Design and Verification of Test Set-up

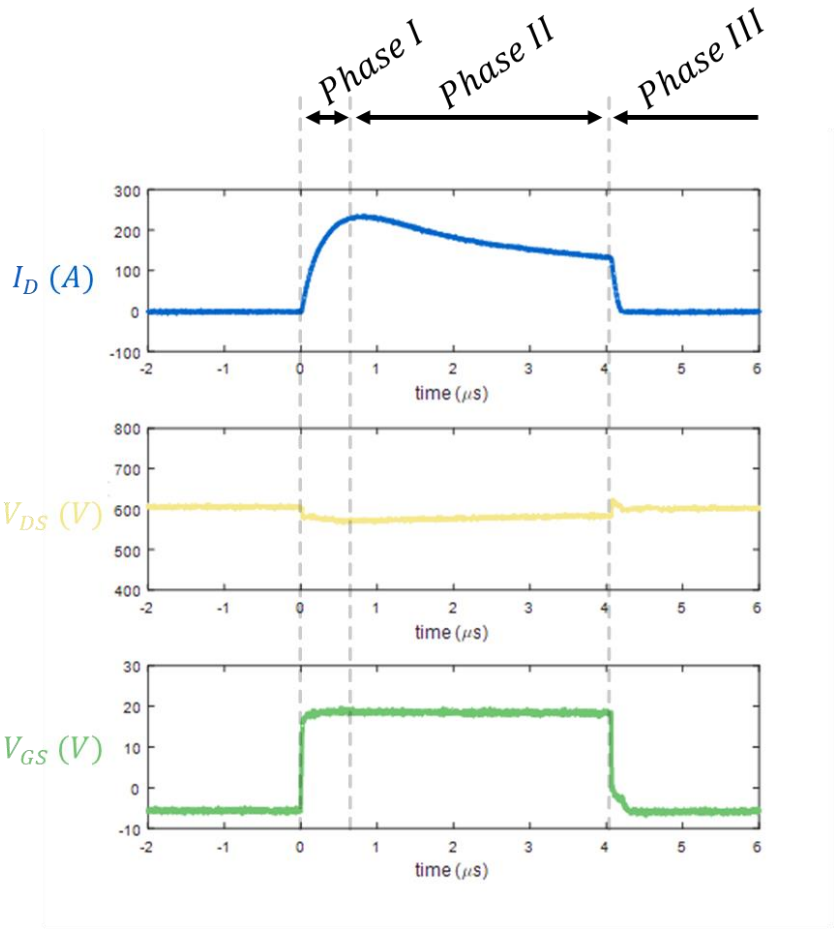

Fig. 26: Phases of short-circuit operation

Fig. 26 shows the different stages during short-circuit operation for a SiC MOSFET. These waveforms are from a short-circuit test on Woldspeed's 1200 V, 80 mΩ SiC MOSFET. For the remainder of this chapter, Wolfspeed's 1200 V, 80 mΩ SiC MOSFET will be referred to frequently due to the extensive availability of short-circuit characterizations of this device in literature.

During Phase I is when the device enters short-circuit mode. At this point, the current rises rapidly. There is also a little drop in the drain-source voltage due to the stray inductance in the set-up. Since this waveform is for an 80 mΩ SiC MOSFET, the current

caps off at a little over 200 A and then starts to saturate. In Phase II, the current starts decreasing, this is because the device is heating up. Because of the relationship between the on-state resistance of a SiC MOSFET and temperature, as the device heats up the on-state resistance starts to increase and therefore the current decreases. This creates a self-regulating system. If there is enough energy available to the device and the inductance of the test set-up is low, the drain-source voltage remains relatively constant throughout this phase. At Phase III, the device is safely turned off without destructive results. Throughout the short-circuit operation, the gate-source voltage behaves as would be expected. In some studies [30] [32], small variations have been found in the gate voltage which leads to destructive results but in this non-destructive test, this is not the case.

The test set-up for the short-circuit characterization is based on the double pulse test board described in the previous chapter which was used for characterizing the switching of the SiC MOSFETs. The main difference is that instead of including an inductor and an anti-parallel diode in the circuit there is a short instead. A simplified circuit for this new set-up is shown in Fig. 27. Although the load inductor is removed there is still stray inductance in the PCB denoted as Ls in the diagram. By removing the inductor and diode, the MOSFET load current is no longer controlled and the device will be able to draw as much current as it needs with little limitation. This change to the set-up requires further additions to the test set-up because conducting at high currents creates safety concerns.

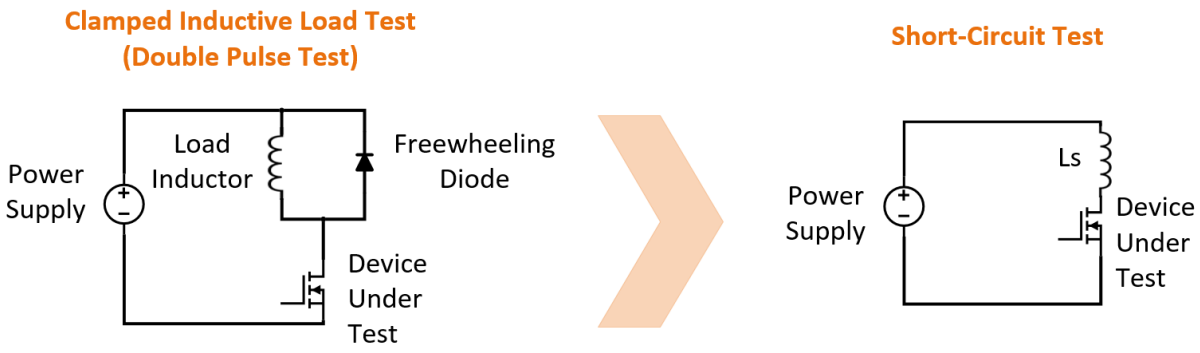

Fig. 27: Schematic showing the differences between the double pulse test and the short-circuit test circuits

To characterize the device under short-circuit operation, the tests were split up in to two categories: non-destructive and destructive tests. During the non-destructive tests, the MOSFET was still put under short-circuit operation conditions but the device was able to shut-off without breaking by control of the length of the on-time of the device. Since the device won't break, the main safety considerations for these tests is making sure that the rest of the board can withstand the high currents. For the destructive tests, it was expected that the devices would fail. When the device fails, it is important to stop the power from flowing through the device which would risk further damage to the test set-up. For this reason, a protection method during the destructive tests was found.

3.2.1 Creating a safe, high current testing set-up

To design a functional overcurrent protection scheme, the short-circuit current expected during testing was estimated to be around 1060 A (See Appendix A).

It is important to protect the testing set-up without affecting the testing results. Most gate drivers have overcurrent protection but for this case, since we want to let the

overcurrent occur, a different solution needs to be implemented. The first solution was to use an IGBT in-line with the shorted device and after the capacitor bank so that when the current spikes after the device breaks a comparator would sense the high current and turn off the IGBT. It was also planned for the IGBT to saturate at a current that would only be reached if the device had broken as a second source of protection. Fig. 28 shows the output characteristics of the IGBT taken using the B1505A curve tracer and Fig. 29 shows the actual saturation current based on the voltage applied to the gate driver to the IGBT.

The short-circuit test set-up is very sensitive to added inductance and by putting such a large IGBT in line, the results were altered and the device was not able to reach its full potential in short-circuit operation. Instead, the IGBT was placed before the capacitor bank (instead of after) so that the capacitors would have enough charge for the tests and the IGBT was set to saturate at a low current so that the capacitors could not quickly recharge during failure. The capacitor bank is 820 μF which was calculated to be enough energy supplied to the device during a destructive test. Therefore, to set such a low saturation current in the IGBT, the gate voltage was set to 5 V, using the curve shown in Fig. 29.

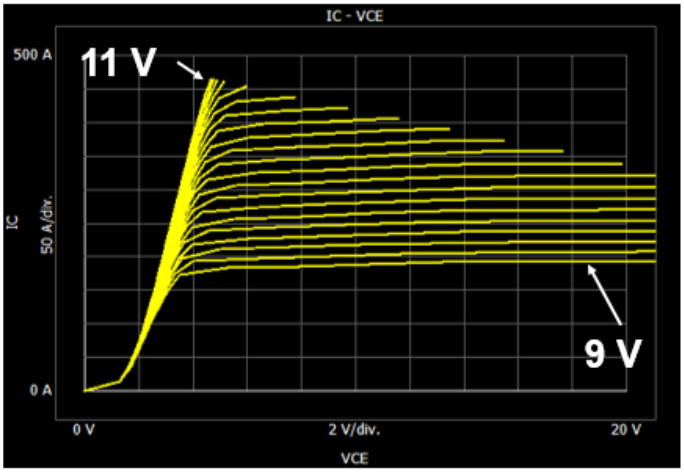

Fig. 28: Output Characteristics of the IGBT used for protection for different gate to emmiter voltages

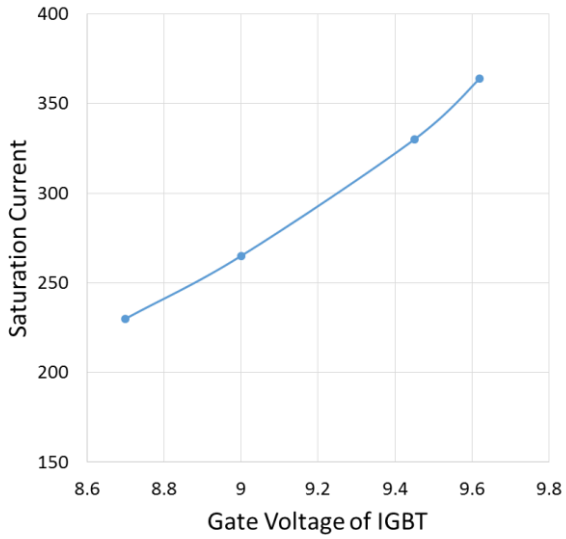

Fig. 29: Gate voltage applied to the IGBT and how this actually affects the saturation current

The final test set-up for the short-circuit characterization is shown in Fig. 30. The test circuit is in a high power bay and the fiber optic controller for the gate driver is outside of the high power bay. When using a fiber optic controller for the PCB, the device can be controlled from a different room during testing, for safety during destructive testing. Fig. 31 shows a picture of the test set-up in the high power bay. Note there is also a plastic barrier included in the set-up to catch any pieces of the device that come off during the destructive test. Also a fan is added for air flow.

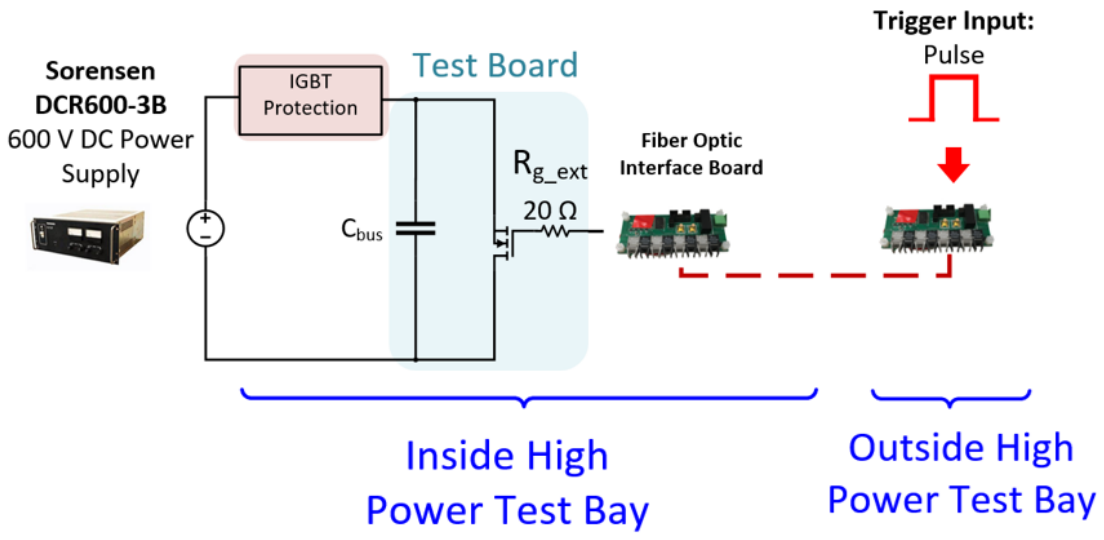

Fig. 30: Final Test set-up used for the short-circuit characterization

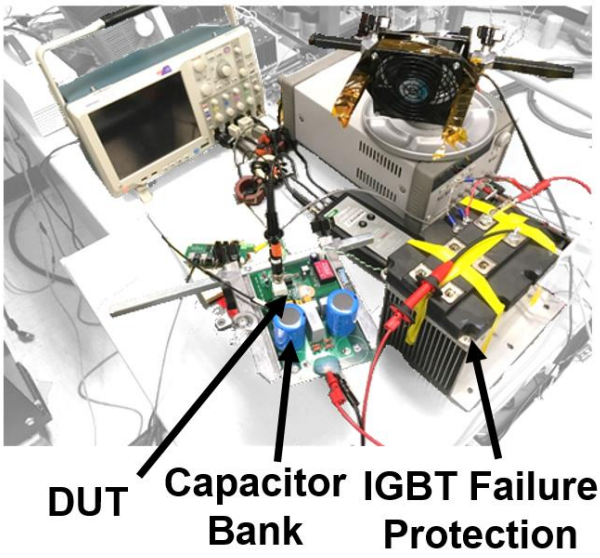

Fig. 31: Test set-up of short-circuit characterization in the high power bay

3.2.2 Verification of the test set-up using simulations

After running initial short-circuit tests, a trend was seen where a drop in the drain-source voltage occurred during turn-on and a voltage rise during turn-off. This happened even

though the capacitor bank was designed to be large enough to supply enough energy for the tests.

Fig. 32 shows this drop in the drain-source voltage. It was expected that this change in the drain-source voltage was due to the loop inductance. The change in current and change in voltage during this dip in the drain-source voltage are labeled. These values are used in the equation below to find the value of the inductance causing this change.

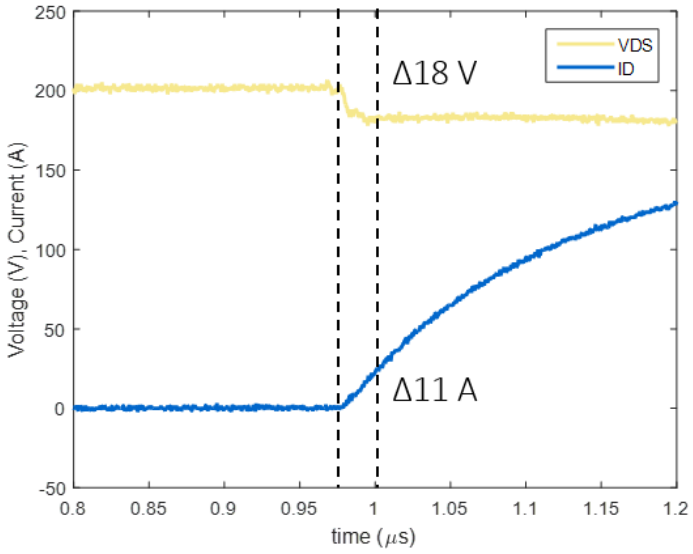

Fig. 32: Using results to look at the overshoot voltage and validate the power loop inductance

Using the change in current, voltage and time from the waveforms, the loop inductance is calculated to be 32.7 nH below.

$$\boldsymbol{V = L\frac{di}{dt}} \quad \textbf{(3-1)}$$

$$L = 18 \times \frac{1}{11} \times 20ns = 32.7\ nH \quad \textbf{(3-2)}$$

The inductance of the device package is 15 nH ((L_{source} = 9 nH) + (L_{drain}= 6 nH)) and the board inductance is 16 nH which adds up to 31 nH. These calculations validate that the drop in voltage is a factor of the inductance in the PCB and device. This was also verified with simulations (where the board inductance is added in the simulation circuit) in Fig. 33 and the actual test results in Fig. 34, the overshoot voltages match.

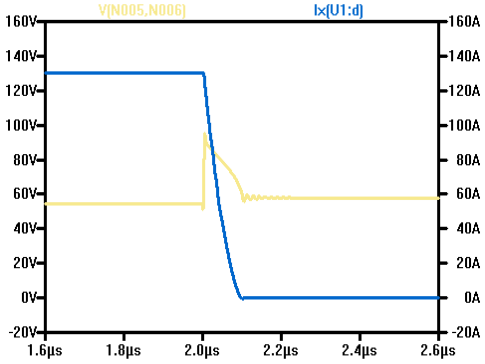

Fig. 33: Overshoot voltage from simulations

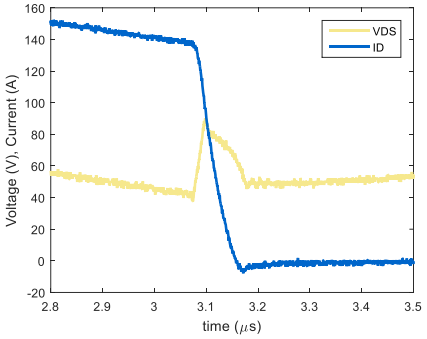

Fig. 34: Overshoot voltage from initial short circuit results

Another part of the testing set-up which needed to be verified was the accuracy of using a Rogowski coil in comparison to a shunt resistor. A shunt resistor was used for measuring the drain current during the dynamic characterization. Shunt resistors allow for accurate current measurement but they are not as robust under high currents. Therefore, it is desirable to measure the current using a Rogowski coil for measuring up to 1000 A and for destructive measurements. Rogowski coils are able to measure the current non-invasively so during destructive tests, the Rogowski coil will not break. A test was run on the 80 mΩ device to determine whether the Rogowski coil measurements are as accurate as the current shunt resistor for short-circuit measurements. To do this, the current was measured using

both the Rogowski coil and the current shunt. The waveforms are plotted on top of each other in Fig. 35 for a comparison. From these measurements the Rogowski seemed to align with the current shunt measurements enough that the tests were continued with the use of a 6 kA Rogowski coil from PEM. The drain-source voltage and the gate-source voltage are measured in the same way as the dynamic characterization tests.

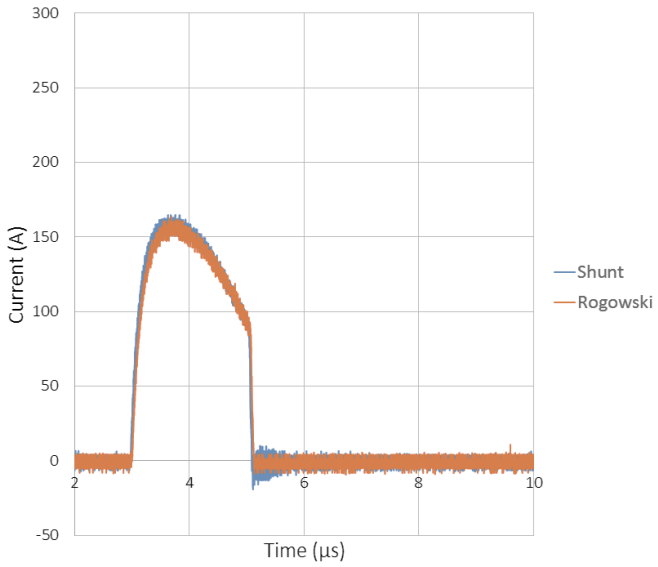

Fig. 35: Comparison between measurements using the Rogowski coil and the Shunt Resistor

After the test set-up was finished, initial testing on the 80 mΩ device was started. For the 80 mΩ device, the short-circuit current was measured for many different drain to source voltages at a pulse width of 4 µs. These are all shown in Fig. 36. From around 20 V to 200 V, the current saturates and becomes relatively constant. At the higher voltages, there is a more prominent decrease in the short-circuit current after it reaches its saturation. The drain-source voltage waveforms as well as the short-circuit current waveforms can be seen for 100 V and 600 V below in Fig. 37 and Fig. 38 respectively.

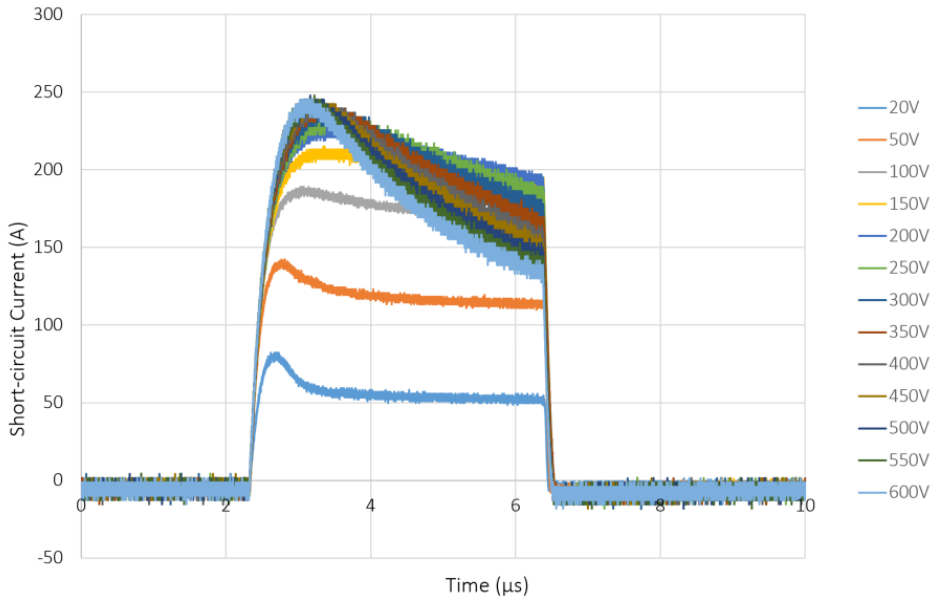

Fig. 36: Short-circuit current of 80 mΩ SiC device from Wolfspeed tested at different drain voltages

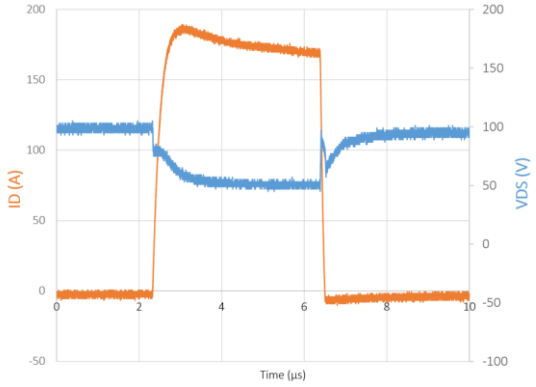

Fig. 37: VDS and ID of the 80 mΩ SiC device from Cree measured at a drain voltage of 100 V

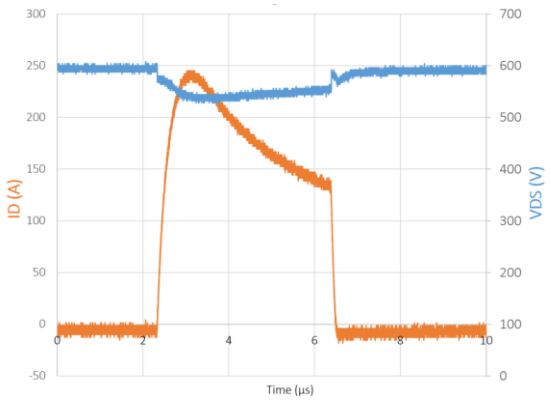

Fig. 38: VDS and ID of the 80 mΩ SiC device from Cree measured at a drain voltage of 600 V

After verifying that the test circuit worked with the smaller current device, the testing moved onto the 10 mΩ device.

3.3 Shortcircuit Test Results for a 900 V, 10 mΩ SiC MOSFET

3.3.1 Non-Destructive Test Results

As mentioned before, a few different tests were performed for the non-destructive short-circuit tests. These tests include changing the drain-source voltage and changing the external gate resistance. The first set of tests where the bus voltage (and therefore the drain-source voltage) is varied at an external gate resistance of 10 Ω are shown in Fig. 39, Fig. 40, and

Fig. 41. The short-circuit conditions were tested at drain-source voltages of 50 V, 200 V, 400 V and 600 V. The drain-source voltages measured across the device using the high voltage probe are shown in Fig. 39. The gate-source voltages are shown in Fig. 40. The device was turned on for 1 µs pulses. The resulting current waveforms are shown in Fig. 41.

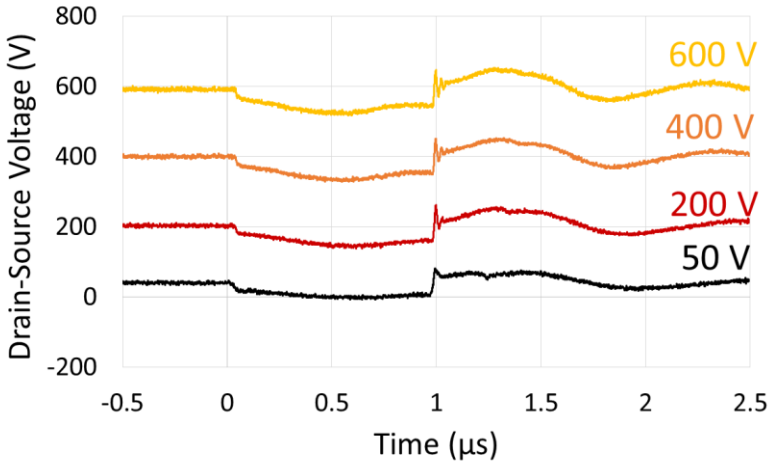

Fig. 39: Drain to source voltage waveforms for the 10 mΩ short-circuit tests

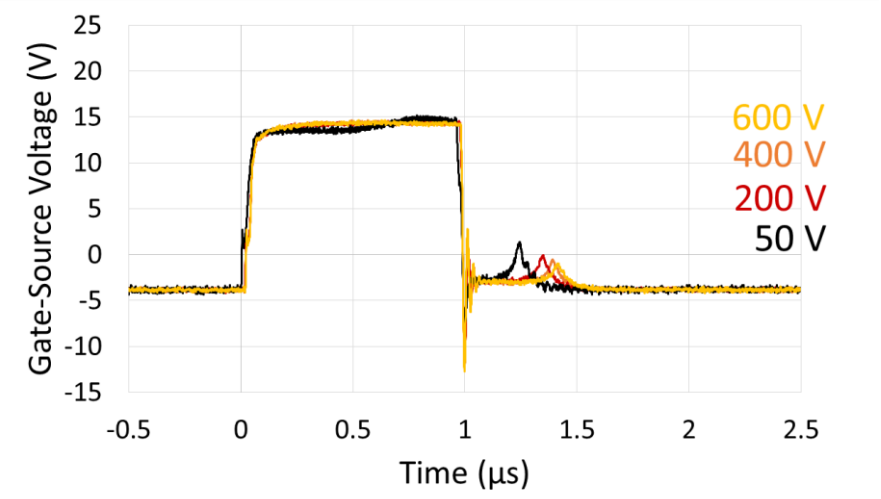

Fig. 40: Gate-source voltage for the 10 mΩ short-circuit tests

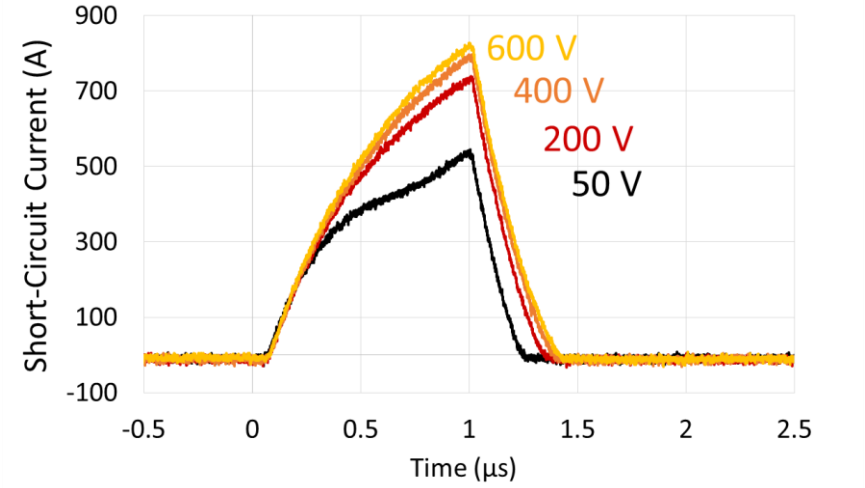

Fig. 41: Short-circuit current of the 10 mΩ device at varying drain to source voltages

Fig. 42 includes a table which summarizes the maximum current readings for the different drain to source voltages. At 400 V, the current reaches 840 A. This is very close to the current of 1060 A which was estimated earlier. Also, from this table it can be seen that at the higher voltages, the current values are closer together. This is again because of

the self-heating of the device which increases the on-state resistance to the point where the current starts decreasing.

VDS	Max Current
50 V	560 A
200 V	760 A
400 V	816 A
600 V	840 A

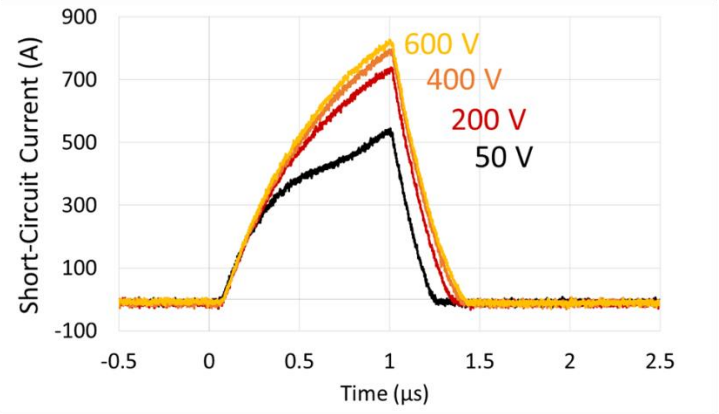

Fig. 42: Maximum short-circuit current of the 10 mΩ device for the different drain to source voltages

The non-destructive tests for the 10 mΩ device performed at different external gate resistances are shown in Fig. 43, Fig. 44, and Fig. 45. For these tests, the device was turned on for a 1 µs long pulse, a length known to not destroy the device. It was driven at the recommended gate drive voltage of -4 V to 15 V. Three different tests were done, each with a different external gate resistance. The three external gate resistance values tested were 3 Ω, 10 Ω and 30 Ω. These are relatively conservative values as to not stress the device. The gate pulse is shown in Fig. 43. As expected, as the gate resistance increases, both the turn-on and the turn-off get slower. Also, the turn-off of the gate signal has a tail, which as the gate resistance gets larger, gets longer and the voltage it reaches gets larger. The corresponding drain-source voltage and drain current measurements are shown in Fig. 44 and Fig. 45 respectively. The 3 Ω gate resistance case results in the highest short-circuit current as well as the largest magnitude overshoots and undershoots for both the gate-source and drain-source voltages. A lot more ringing also occurs in the 3 Ω case.

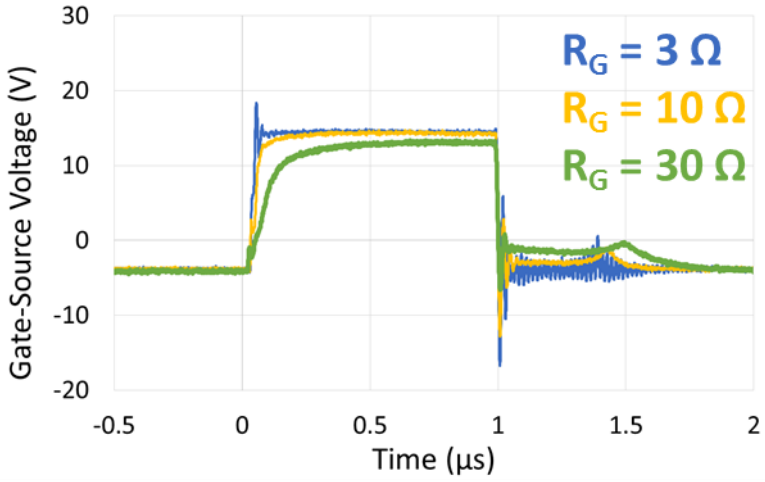

Fig. 43: Short-circuit gate-source signals for different external gate resistances

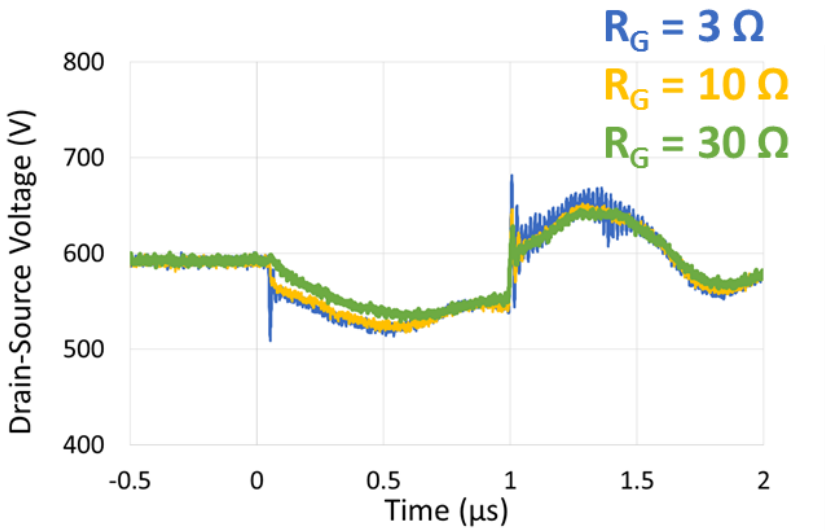

Fig. 44: Short-circuit drain-source voltage for different external gate resistances

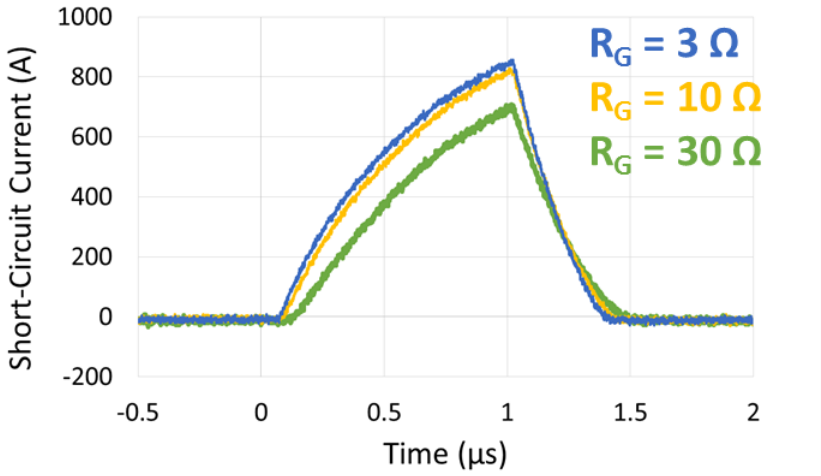

Fig. 45: Short-circuit drain current measurements for different external gate resistances

3.3.2 Destructive Test Results

The destructive tests were performed in the same way as the non-destructive tests but this time, the device was given a pulse long enough to break it. Fig. 46 shows the waveforms where the device was pulsed for multiple different lengths and it was determined by the final waveform that the device could withstand 4.5 µs before a destructive failure. This test was done at a drain-source voltage of 600 V. The resulting device after the destructive test is shown in Fig. 47.

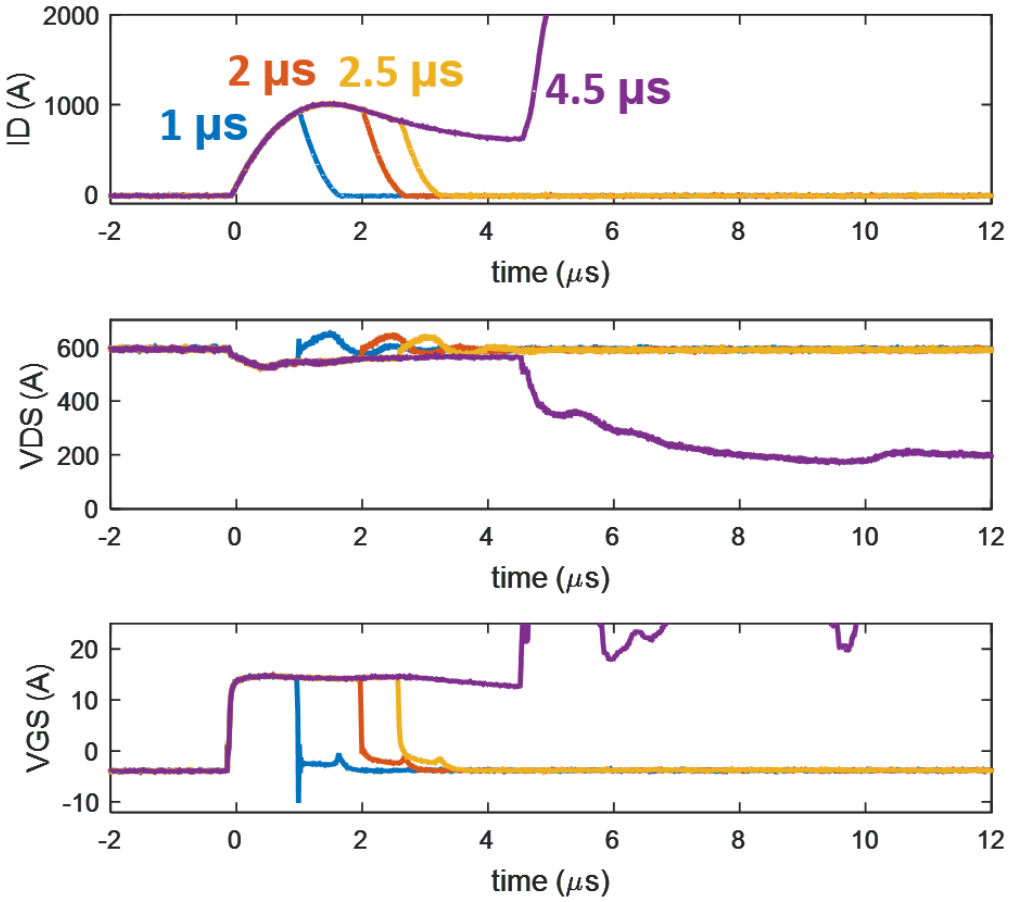

Fig. 46: Destructive test waveforms where the device breaks after being subjected to a pulse for 4.5 µs

Fig. 47: 10 mΩ device after the destructive test

After performing a test with increasing pulse widths to get an idea of how the device performs, the rest of the destructive tests were conducted by giving the device a pulse long enough that the device could not withstand the pulse. This is so that the device is not deteriorated during the lead up pulses to the actual destructive pulse.

The destructive tests were also performed at high temperature. Fig. 48 shows the test set-up where a copper piece was bent and connected to the hot plate so that it could sit behind the device and heat it up. A few destructive tests were performed at high temperature and the results are summarized in Table 2.

A destructive test under similar conditions to the room temperature destructive test are shown in Fig. 49, where the two tests are compared. As expected, the device can withstand short-circuit operation in room temperature longer than it could withstand in high temperature conditions.

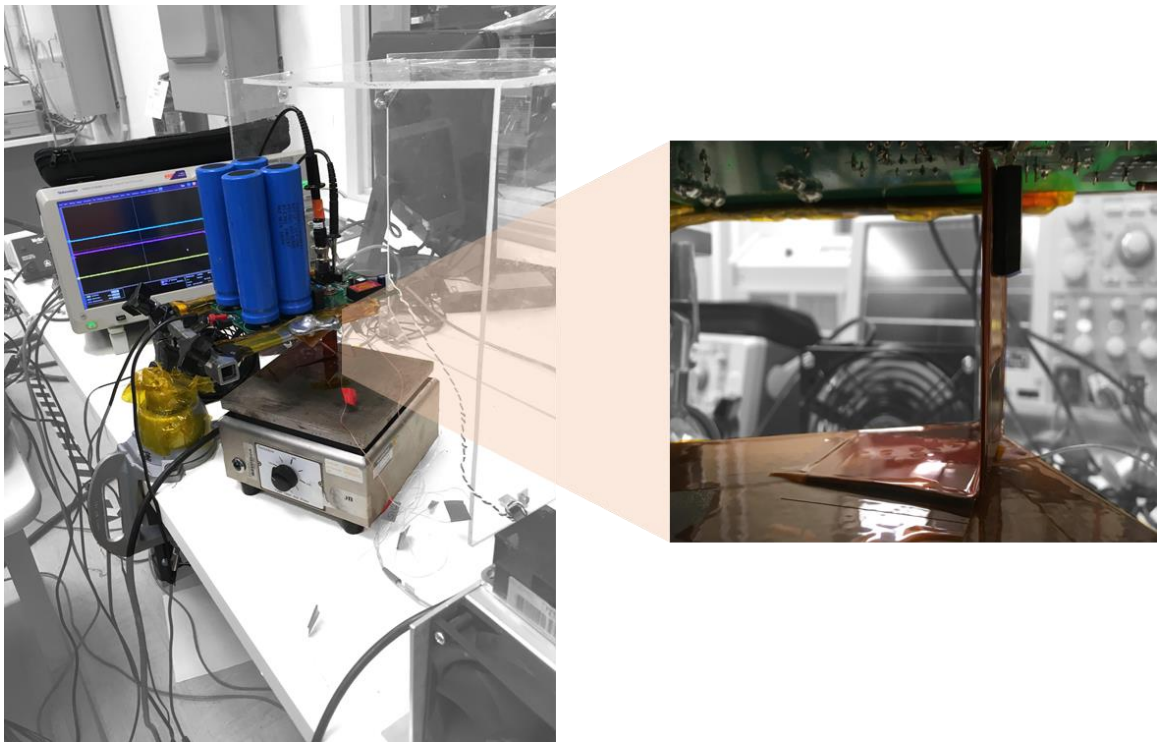

Fig. 48: High temperature set-up for destructive short-circuit test

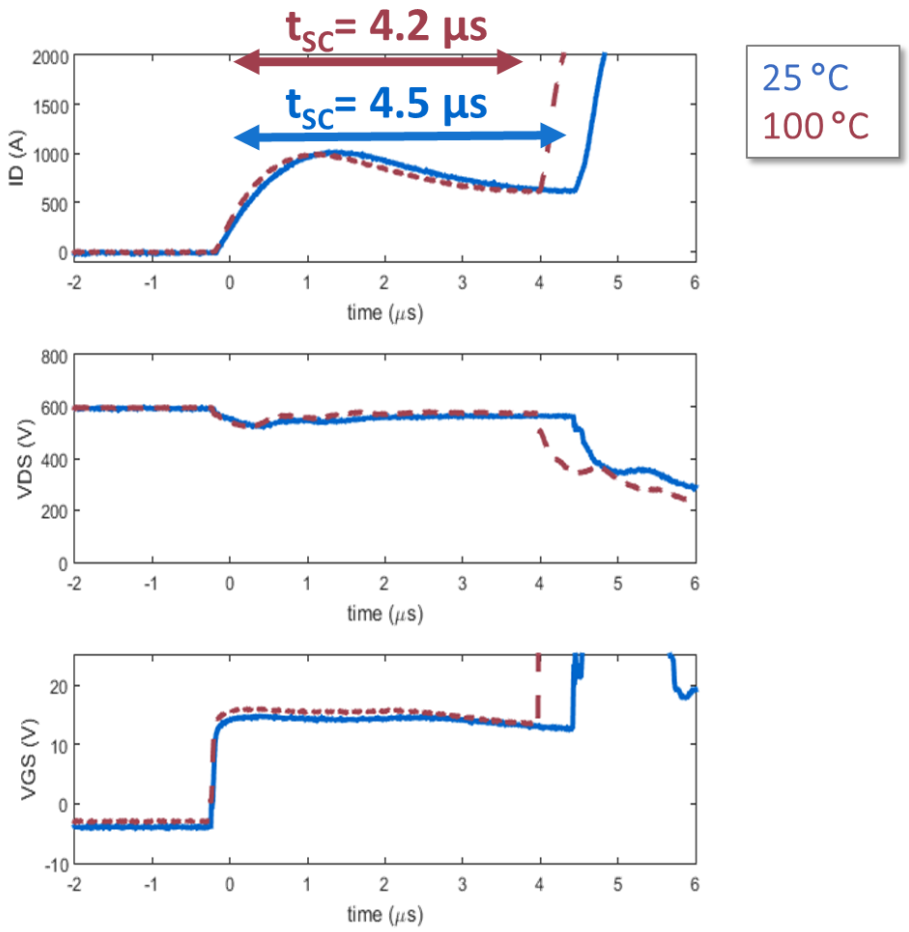

Fig. 49: Destructive short-circuit waveform comparison for room temperaure (25°C) and high temperature (100°C) tests

The critical energy of the short-circuit test is the energy it takes to destroy the device [18]. In this case, this critical energy is found by taking the results from the destructive tests where the device is given a pulse long enough to break. The waveforms from this destructive test are then used to calculate the energy that the device saw before it broke. An example of this is shown in Fig. 50. The energy was calculated by first taking the power and plotting it in MATLAB. This waveform was then integrated used the trapz function in

MATLAB which calculates the area under the instantaneous power curve using a trapezoidal method.

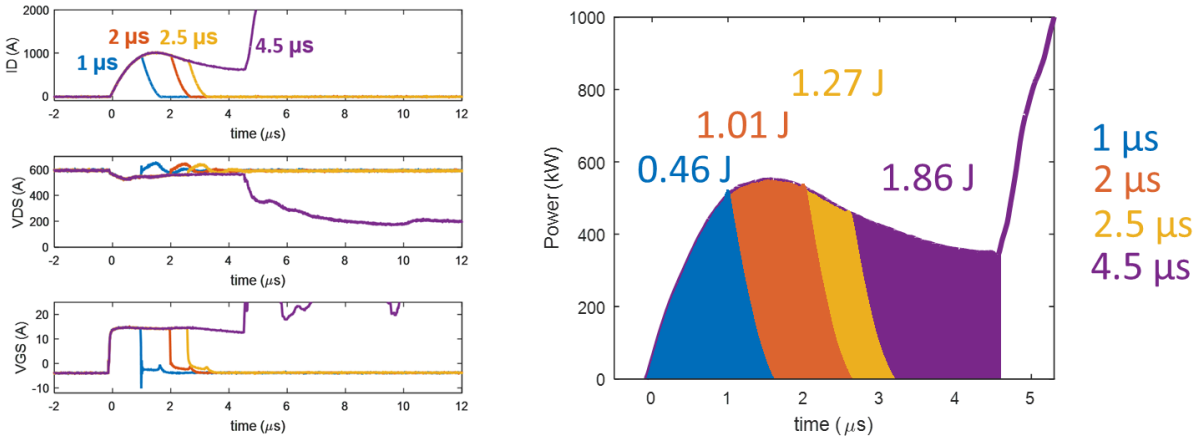

Fig. 50: Comparison of the energy for both destructive tests

As shown in Table 2, although the different tests were at different drain-source voltages and temperatures, they had very similar short-circuit energies. The short-circuit withstand time varied significantly between 4.2 µs to 6.6 µs which is a 57% difference. The short-circuit energies had a much smaller difference which was only 6.8%.

Table 2: Overview of short-circuit destructive tests

	Test 1	Test 2	Test 3	Test 4
Bus voltage	600 V	600 V	450 V	520 V
Temperature	25 °C	100 °C	100 °C	120 °C
Short-circuit withstand time	4.5 µs	4.2 µs	6.6 µs	5.2 µs

Short-circuit energy	1.86 J	1.76 J	1.82 J	1.88 J

In the destructive short-circuit waveforms in Fig. 49, it can be seen that the current saturates after about 1 μs and then starts decreasing. This is because the on-state resistance of SiC MOSFETs have a positive temperature coefficient. This means that as the temperature increases, the on-state resistance also increases. When the device is subjected to short-circuit operation, it is exposed to a lot of energy. This causes the device to heat up and when this happens, the on-state resistance also increases, which in turn decreases the current. Essentially, this creates a self-regulating system during short-circuit operation but as can be seen from the results, it does not regulate well enough and eventually the heat becomes too much and the device breaks. To try and evaluate this system in terms of junction temperature that the device experiences, the junction temperature during testing was estimated. This data has to be estimated instead of measured because there isn't equipment with a sample rate fast enough for these tests. To estimate the junction temperature, the method described in [33] was used.

For this method the equation of the thermal impedance is found, taken from the thermal impedance graph for this particular device, provided by the manufacturer. To get the equation of the thermal impedance the points of the curve for the single pulse are extracted and plotted in excel as in Fig. 51. From there, points smaller than 10 μs are used to estimate an equation for the fitted line. Generally, this line will follow the format of equation (1). Where Zth is the thermal impedance, K is a constant, t is time, and x is also a constant.

$$Z_{th} = K \cdot t^{x} \quad \textbf{(3-3)}$$

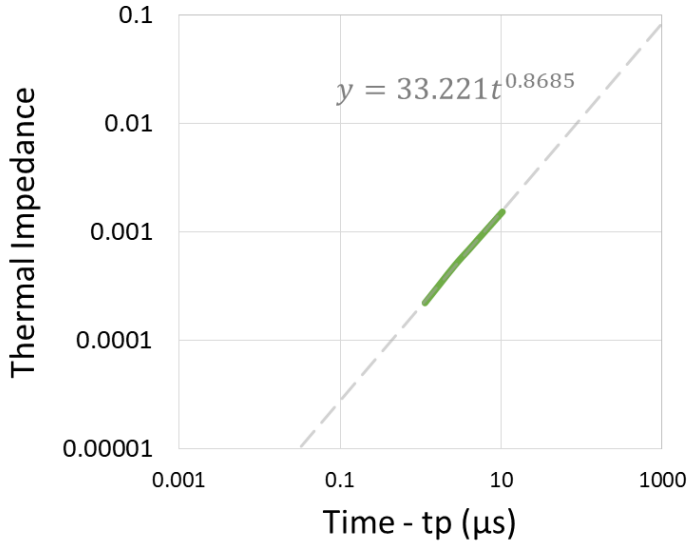

Fig. 51: Extrapolated thermal impedance with the line equation displayed

The extrapolated equation is then used with the basic thermal impedance formula to get the equation displayed in Fig. 51. This equation takes the instantaneous power curve (drain current multiplied by the drain-source voltage) and then relates it to temperature at each instant in time.

$$\boldsymbol{T_{rise} = T_{initial} + P_n \cdot K \cdot t^{x}} \quad \textbf{(3-4)}$$

By using the thermal impedance as a function of time and the energy the device was subjected to, the estimated junction temperature compared to the short-circuit current is shown for both the high temperature and room temperature cases in Fig. 52. As expected,

the temperature rapidly increases when the device is turned on but then the gradient decreases when the device starts to self-regulate and the short-circuit current decreases. When the device breaks a little after 4 µs, the model becomes inaccurate.

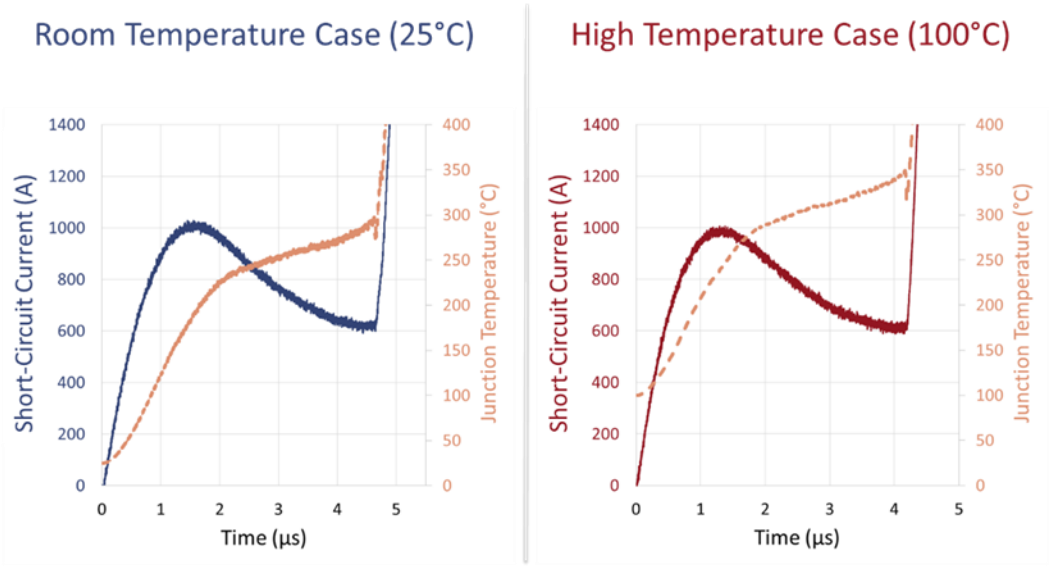

Fig. 52: Estimation of the device junction temperature under short-circuit operation for both the room temperature and high temperature destructive tests

Chapter 4 Static and Dynamic Characterization of Vertical Gallium Nitride Transistors

Acknowledgment: The information, data, or work presented herein was funded in part by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award Number DE-AR000450, managed by Dr. Isik Kizilyalli.

4.1 Introduction to Vertical GaN Transistors

In the push towards having higher power and higher efficiency in power electronics, the development of gallium nitride (GaN) technologies has become increasingly significant. Wide-bandgap devices, including GaN, have been shown to allow for higher temperature operation, higher voltages and currents, all while still having better operating efficiency than silicon devices [34], [35].

However, at this point in time, the market for GaN power semiconductors is dominated by devices with a lateral structure. This is due to constraints with GaN substrates, such as expense and maturity. Whereas the development of lateral GaN devices is less problematic as they are made with alternate substrates such as silicon or silicon carbide (SiC) [23], [14]. Despite the difficulties, it is beneficial to develop vertical GaN technology because it will

open up even higher voltage levels and utilize the fast switching characteristics that have become expected of GaN.

This chapter begins with a brief description of the device fabrication process, which was developed by HRL Laboratories. A static and dynamic characterization is then perfomed on the device in the next two sections. These sections include the test setup as well as the results for the characterizations. This chapter also includes a description of the design of the PCB used for testing the vertical GaN devices.

4.2 Device Fabrication Process

An in-depth look into the device fabrication process of the vertical GaN die can be found in [36]. In summary, the process starts by depositing an n^- GaN drift layer of 8 µm and a p GaN base layer of 800 nm onto the bulk GaN substrate using a metal-organic chemical vapor deposition (MOCVD) growth process. Then after the base layer, by using a patterned SiO_2 mask, an n^+ GaN layer of 200 to 400 nm is added onto select parts. Then an inductively coupled plasma (ICP) etch is performed again with the use of a SiO_2 mask to open the gate trenches which are 2 µm wide. The process then includes a Tetramethylammonium hydroxide (TMAH) wet etch treatment. Then using MOCVD, the 50 nm thick AlN/SiN dielectric is grown on the gate. After this, the contact vias are opened and metallized and the bottom of the wafer is also metallized. This was the process used to develop the devices being described in the remainder of the chapter

4.3 Static Characterization of the Vertical GaN devices

The vertical GaN devices are being tested in bare die form. Therefore, a PCB to allow for the testing of the unpackaged devices was designed and is described in the next section. For the static characterization, the device was mounted, wire bonded and encapsulated onto this test PCB and connected to Keysight's B1505A power device analyzer. Due to the device already being mounted onto the PCB, extra wires were added so that the device could be connected to the TO-247 adapter on the curve tracer. This setup is shown in Fig. 53. Adding these wires to the set-up add inductance and resistance to the static characterization results. Five vertical GaN transistors from HRL were tested, the static and dynamic characteristics following will show the results for the best performing device.

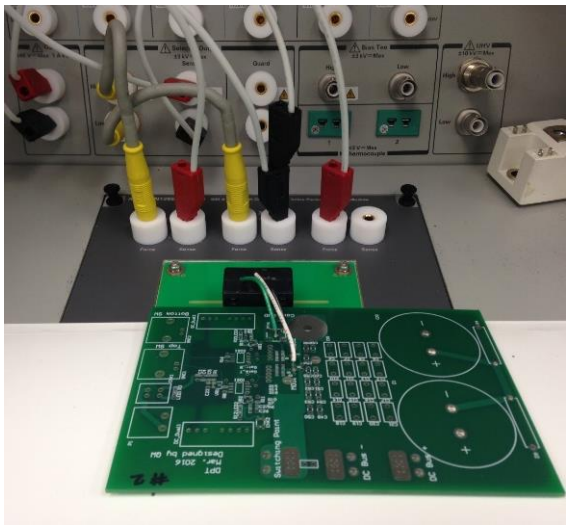

Fig. 53: Connection from device to curve tracer for the static characterization

The static characterization consisted of the measurement of the transfer characteristics, output characteristics, breakdown voltage and the on-state resistance, all at room temperature.

Fig. 54 shows the transfer characteristics of the device at a drain-source voltage of 1 V and 10 V. From this curve, it can be seen that the device starts turning on at a gate-source voltage of 3.3 V for both drain-source voltages. Having a relatively high threshold voltage is favorable so that there are no false turn-ons.

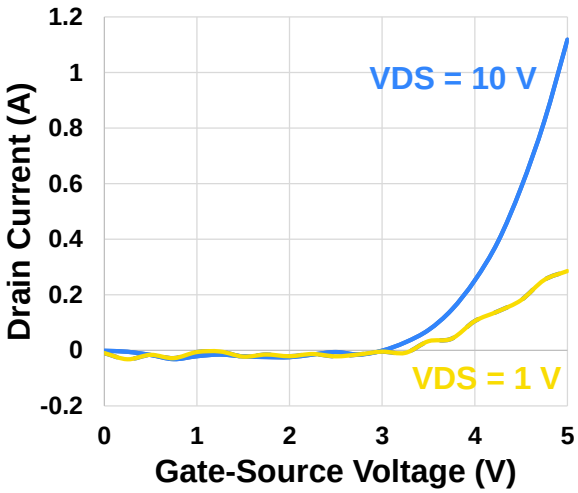

Fig. 54: Transfer characteristics curves at a drain-source voltage of 1 V and 10 V at 25 °C

The output characteristics are shown in

Fig. 55. The curves are measured for gate-source voltages ranging from 0 V to 10 V as specified in the figure. When the gate-source voltage is set to 4 V, the current starts to saturate due to a pinch-off effect. When operating at a gate-source voltage from 6 V to 10 V the device is fully enhanced. From this, it was determined to drive the GaN transistor at 0 V in the off-state and 8 V in the on-state for the dynamic characterization.

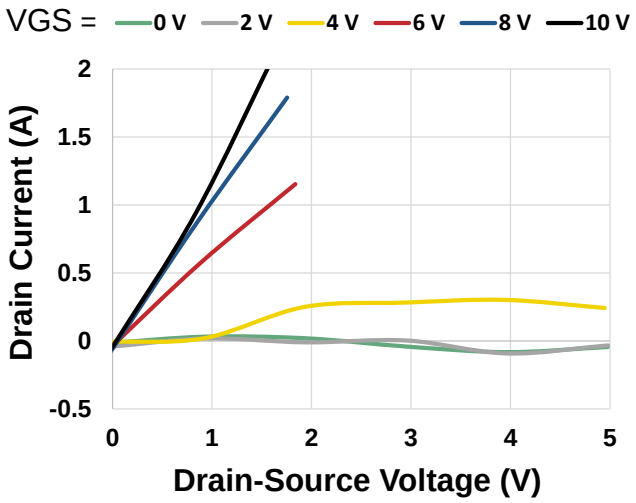

Fig. 55: Output characteristics at 25 °C

The breakdown voltage is the drain-source voltage level which creates a certain amount of leakage current through the device [37]. The breakdown of the device shown in Fig. 56, is measured up to a drain-source voltage of 600 V which resulted in leakage current of less than 10 µA. This was measured with a gate-source voltage of 0 V.

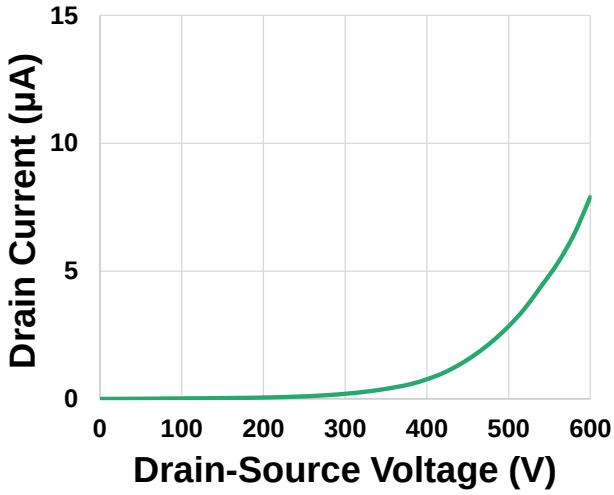

Fig. 56: Breakdown voltage measured up to 600 V for a gate-source voltage of 0 V and at 25 °C

Finally, Fig. 57 shows the on-state resistance for various drain current values. At 2 A drain current, 10 V gate-source voltage and 25 °C, the on-state resistance is 880 mΩ.

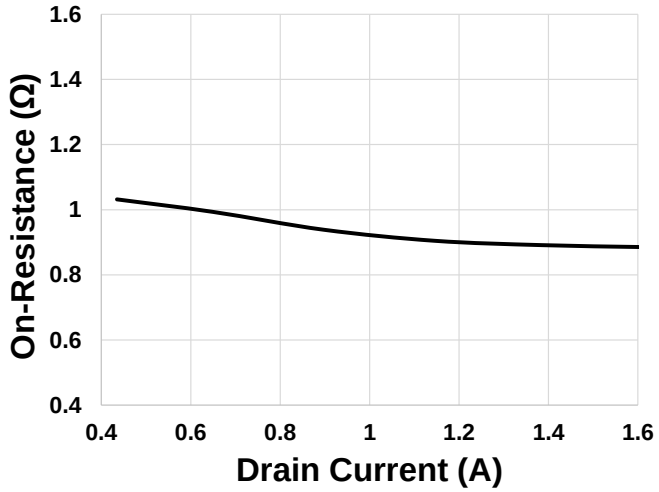

Fig. 57: On-state resistance measured at a gate-source voltage of 10 V and at 25 °C

4.4 Dynamic Characterization of the Vertical GaN Devices

As mentioned earlier, to successfully perform the switching characterization of the device, a special PCB was designed. The main attributes of this board are: a footprint which allow for the bare die to be mounted onto the board, minimized gate loop and power loop inductances, and lastly the ability to test the characteristics of one GaN transistor with either a freewheeling SiC Schottky diode or another GaN transistor as the high-side switch in a phase leg configuration.

Fig. 58 and Fig. 59 show images of the vertical GaN transistor and SiC Schottky diode, respectively, after they have been mounted onto the PCB, wire bonded and encapsulated. The GaN transistor die is directly mounted onto the board where it makes the connection

to the drain trace. The transistor is then connected to the gate and source traces by using 0.7 mil gold wire bonds. A Kelvin source connection is included in the same way.

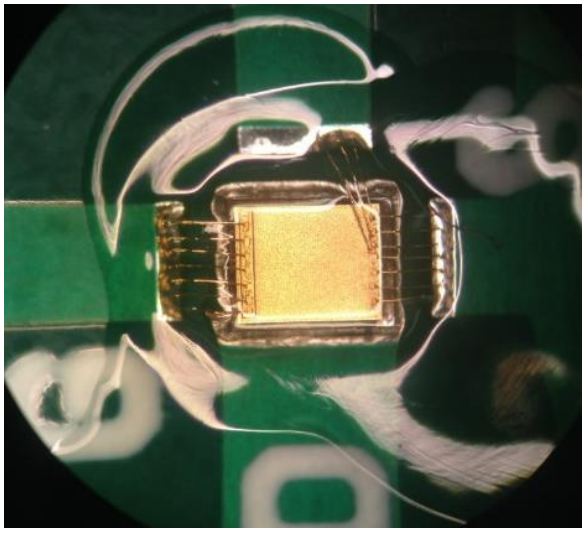

Fig. 58: Vertical GaN transistor after being mounted, wire bonded and encapsulated

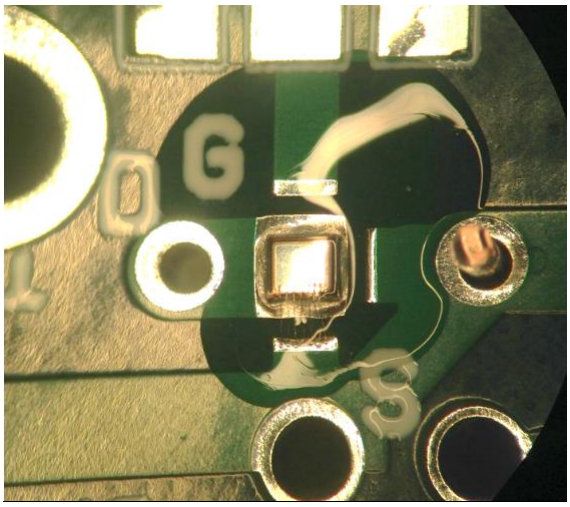

Fig. 59: SiC Schottky diode after being mounted, wire bonded and encapsulated

When attempting to minimize the gate and power loop inductances, careful consideration was put into keeping the two loops separated while also having a compact design. Large loop inductances in the system could result in large overshoots, due to the

fast switching capabilities of the device, and unwanted ringing. These effects could end up destroying the device [38]. To separate the power loop and the gate loop, the bulk and decoupling capacitors were placed on one side of the PCB while the gate driver components were placed on the opposite side of the board. The transistors were then placed in the middle allowing easy access to both loops without creating overlap. This layout design can be seen from the PCB layout which is shown in

Fig. 60. From ANSYS Q3D simulations of the PCB, the power loop inductance was determined to be 12.8 nH and the gate loop inductance was 5.5 nH.

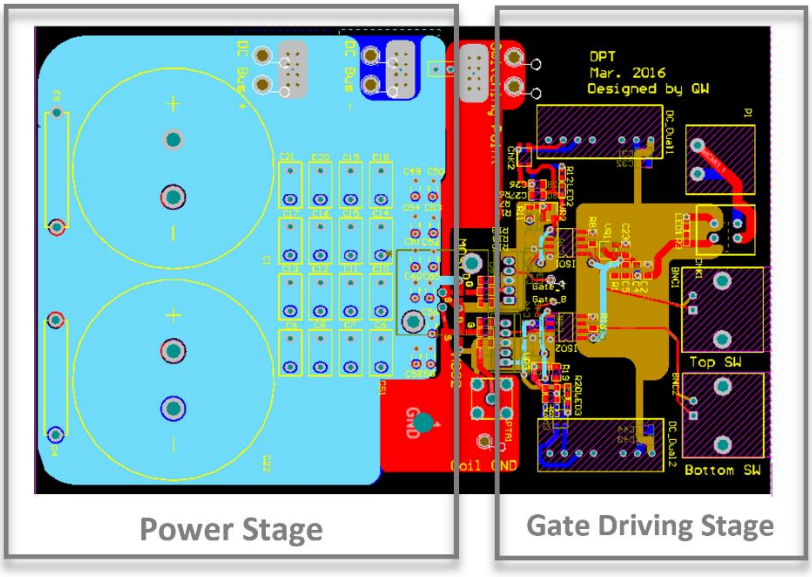

Fig. 60: Board layout used for the dynamic testing of the GaN transistor

The final feature of the board, which is the ability to test one device with a freewheeling diode or two devices in phase leg configuration, was achieved using the design of the PCB footprint of the device. This footprint not only fits the vertical GaN transistor, but it also fits Wolfspeed's 600 V, 3 A SiC Schottky diode (CPW3-0600S003). Based on the

configuration being used, the vertical GaN transistor or the diode can be mounted onto the footprint on the board. For example, when only testing one device, the diode will be mounted in the top switch position and the wire bonds to the gate loop will be omitted, but the anode and cathode of the diode will be connected to the power loop. Only the configuration just described was used in the results that follow. The phase leg configuration option is included in the design for future testing.

After the PCB was fabricated, it was populated with Wolfspeed's SiC Schottky diode (CPW3-0600S003) and HRL's vertical GaN transistor. These devices were also wire bonded and encapsulated using Super Corona Dope. The transistor and the diode can be seen in Fig. 58 and Fig. 59 respectively.

An overview of the test set-up including the gate components and the load inductor can be seen in Fig. 61. A 100 µH inductor was used as the load inductor and was designed to have a low equivalent parallel capacitance (EPC) of 5 pF by having a large core and few windings to limit current overshoot. To reduce ringing in the system and allow for an immediate supply of energy to the device when switching, ten surface mount capacitors rated for 1000 V were added to the power loop and were placed directly next to the device. The gate driver circuitry consists of an isolated power supply from Recom Power (RSO-2415S) which is split into 0 V and 8 V and supplied to the gate driver chip which uses these voltages to drive the gate of the device. The input signal goes through a high speed digital isolator and then is also fed to the current booster chip. The gate driver chip used is the IXDN614. It was selected because it is a high speed gate driver designed for the switching of power devices. It boasts rise and fall times of less than 30 ns. Also,

in comparison to the other gate drivers in this family, this one has no under voltage lockout (UVLO), which was needed for driving the device to 8 V [39].

A photo of the actual test set-up with key components labeled can be seen in Fig. 62.

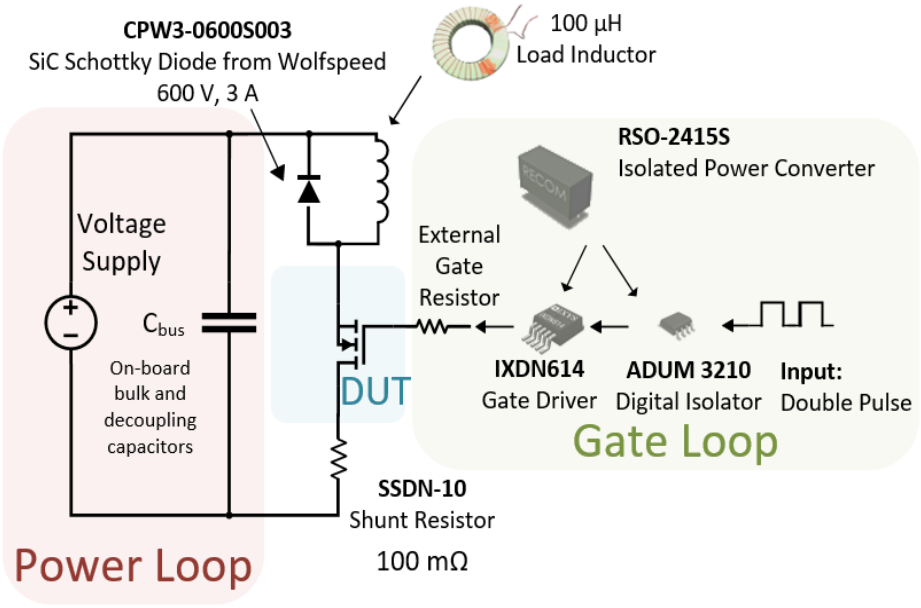

Fig. 61: Diagram showing the test set-up for the dynamic characterization

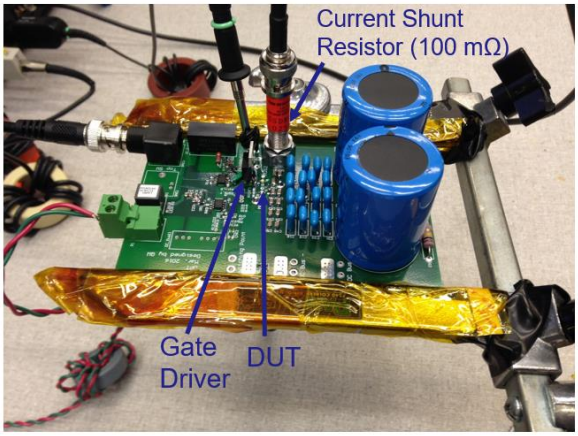

Fig. 62: Test set-up of the dynamic characterization with key features labeled

Consideration was put into the measurement of the switching waveforms. The current was measured using a 100 mΩ coaxial shunt (SSDN-10) with a bandwidth of 2 GHz. The

gate-source voltage was measured using a 300 V single-ended passive probe (Tektronix P6139B) and the drain-source voltage was measured using a 2.5 kV single-ended passive probe (Tektronix P5100) [40] [22].

Initially, a 25 mΩ coaxial shunt (SSDN-414-25) was being used instead of the 100 mΩ shunt. This resulted in large amounts of ringing and overshoot in the results. Fig. 63 shows the comparison of these two shunt resistors on the waveforms. These were two different devices but measured in the same conditions and it can even be seen that they are behaving similarly in terms of performance. The main difference is in the current waveform for the 25 mΩ shunt where there is a large current overshoot and a lot of ringing in the waveform. When selecting current shunt resistors for test, it is important to keep in mind the resistance to inductance ratio [41]. Although the 25 mΩ shunt resistor worked for the SiC MOSFETs shown previously, they were being measured at much higher currents so a smaller resistance was needed. In this case with the vertical GaN device, a larger resistance is needed so that the inductance does not affect the measurement as much. This was verified when testing with the 100 mΩ coaxial shunt, so the rest of the tests were performed using this method.

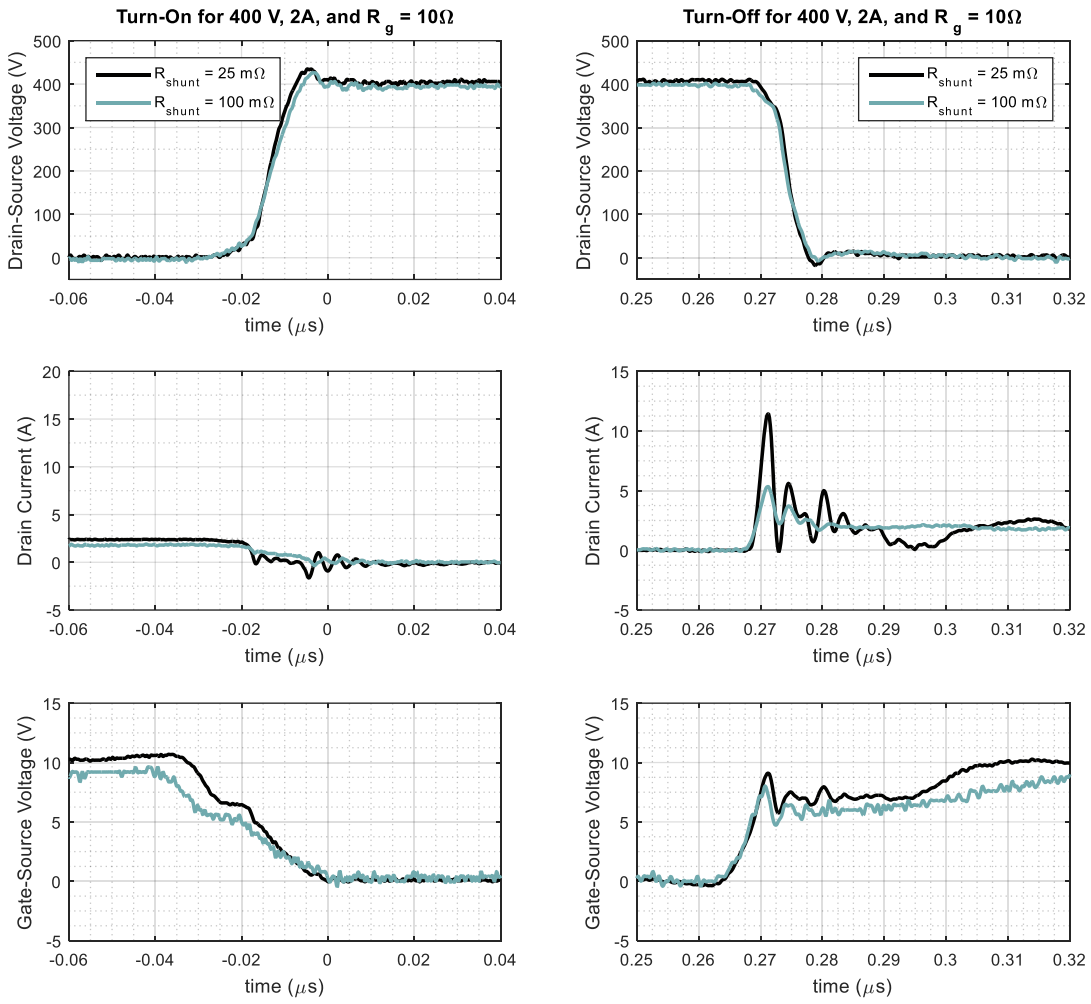

Fig. 63: Comparison of two shunt resistors on the ringing in the switching characteristics of the vertical GaN transistor

The external gate resistance used started at 10 Ω and the device was tested up to a drain-source voltage of 450 V and a load current of 2 A. These tests were then repeated for a 5 Ω and 2.5 Ω gate resistance making sure to carefully monitor the overshoot voltages and current. The switching waveforms for all three gate resistances at a 400 V drain-source voltage and a load current of 2 A is shown in Fig. 64.

Turn-on Turn-off

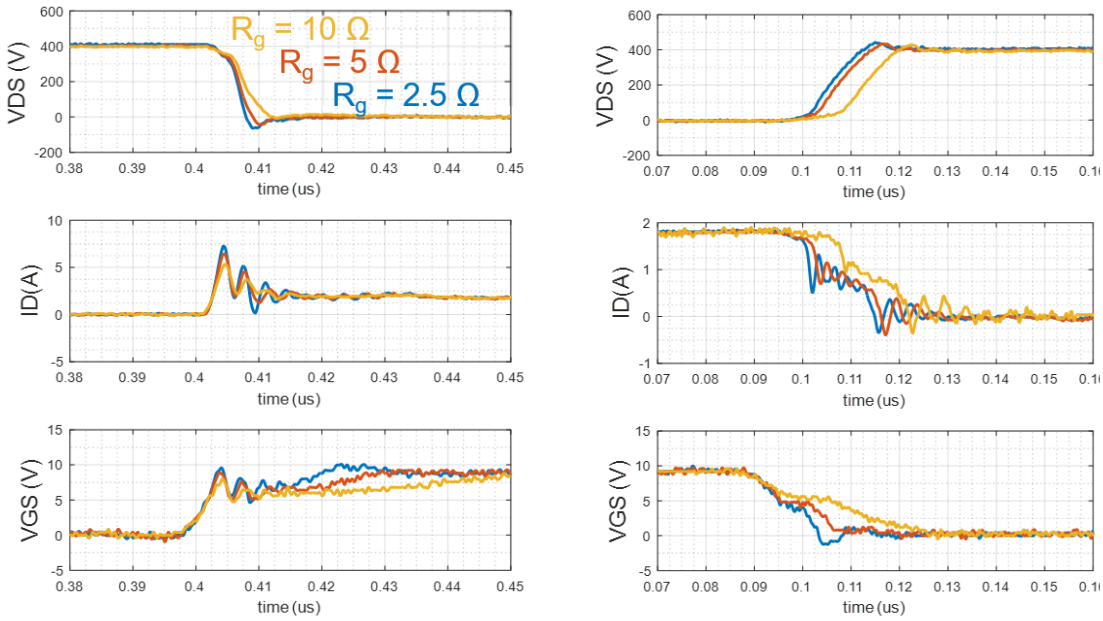

Fig. 64: Switching waveforms at a 400 V drain-source voltage and a 2 A load current for the three different external gate resistances tested at 25 °C

The switching waveforms at 450 V and a 2 A load current with a gate resistance of 5 Ω are shown in Fig. 65. This waveform shows a voltage turn-on speed of 70 V/ns and a turn-off speed of 33 V/ns. This results in switching energies of 8.12 µJ and 3.04 µJ at turn-on at turn-off respectively. The overall switching losses for the lowest external gate resistor case (2.5 Ω) are shown in Fig. 66 for the various drain-source voltages at a 2 A load current. The total losses at 400 V are 9 µJ, with the corresponding turn-on and turn-off losses being 6.7 µJ and 2.3 µJ respectively.

Turn-on Turn-off

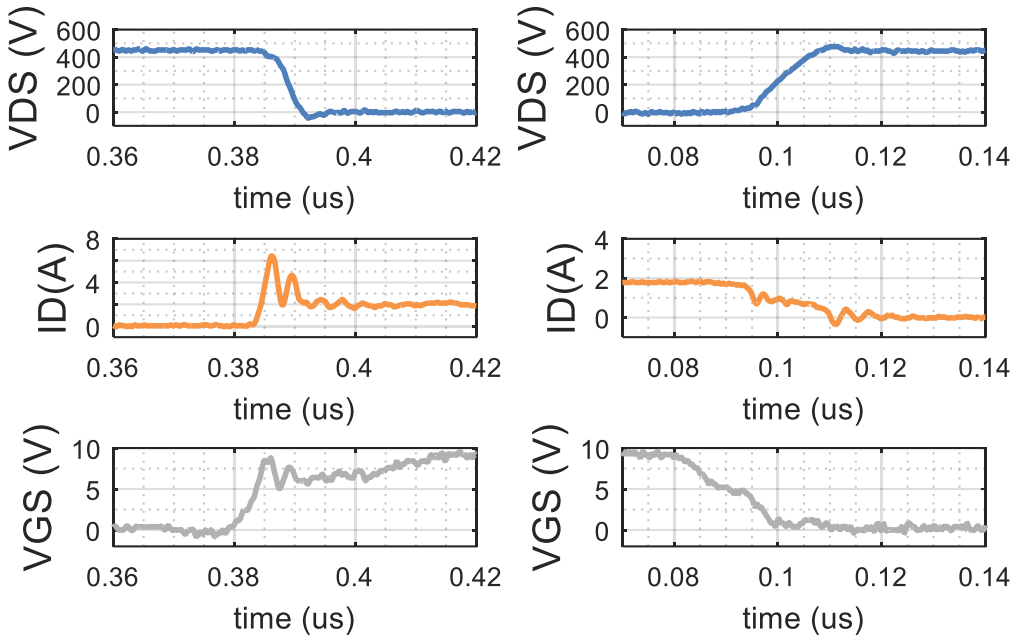

Fig. 65: Switching waveforms at a 450 V drain-source voltage and a 2 A load current at 25 °C

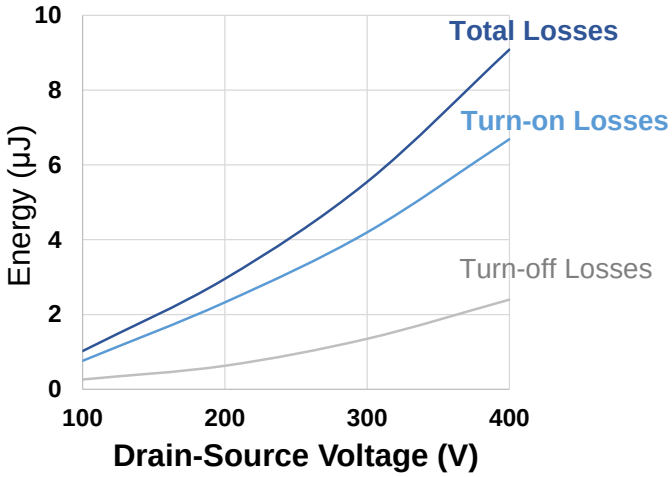

Fig. 66: Switching losses of the device at different drain-source voltages with an external gate resistance of 2.5 Ω and a 2 A load current

A comparison of the switching losses for different gate resistances is shown in Fig. 67. As the external gate resistance is decreased, the losses also decrease. Therefore, it is ideal to use the lowest external gate resistance, but a higher external gate voltage is sometimes needs to allow for a lower voltage overshoot.

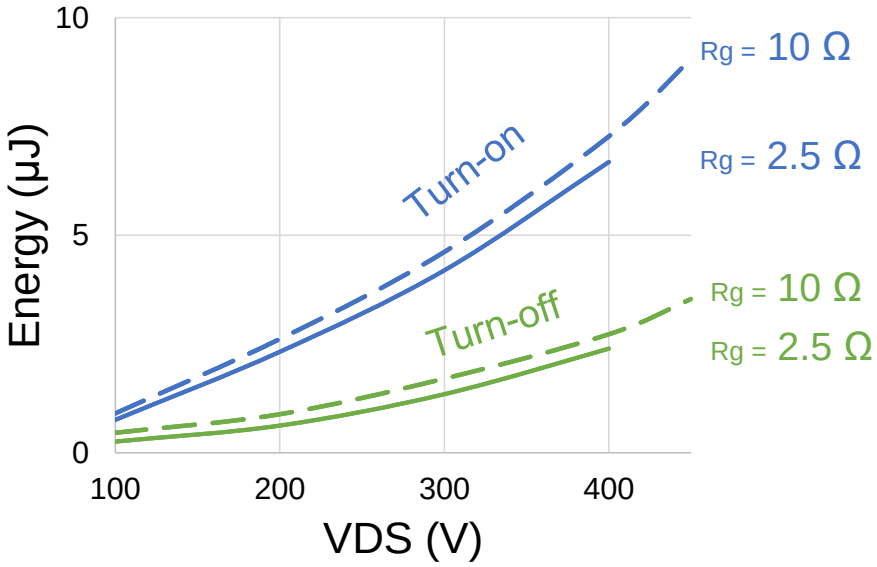

Fig. 67: Comparison of the turn-on (blue) and turn-off (green) losses at gate resistances of 10 and 2.5 Ω, and 2 A load current.

At a gate resistance of 2.5 Ω and a load current of 2 A, the voltage is switching 450 V at a speed of 86 V/ns at turn-on. Even more notably, at a load current of 1 A under the same conditions it is switching at 97 V/ns (or 56 V/ns for 10 Ω). To put this into perspective, Infineon's Si MOSFET (IPS70R2K0CE) has a voltage switching speed of 14.8 V/ns at turn-on at a load of 1.1 A and 400 V with an external gate resistance of 10.2 Ω [42] . The rates of the turn-on voltage transients (*dv/dt*) at 2 A for the different external gate resistances are shown in Fig. 68.

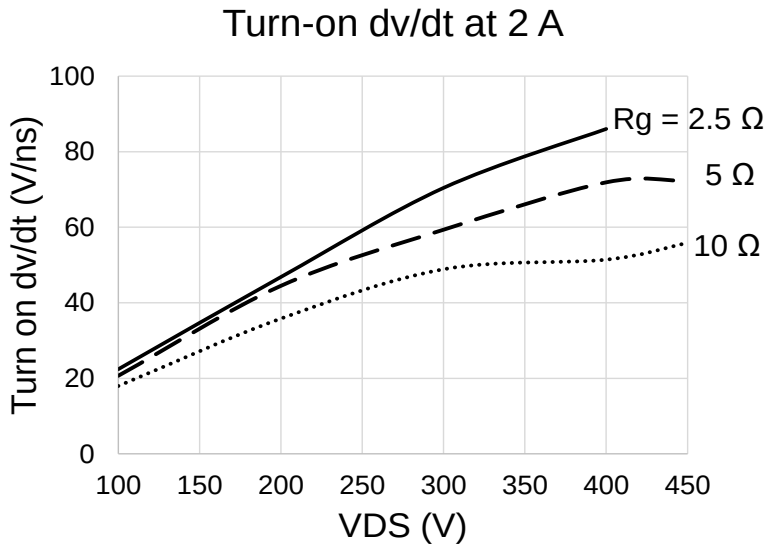

Fig. 68: Turn on dv/dt versus drain-source voltage at a load current of 2 A for different external gate resistances.

4.5 Dynamic On-Resistance Measurement

Trapped charge is a common problem in GaN HEMT devices [43]–[46], which occurs in the device when a high voltage is applied across it. Although this can phenomen can lead to reliability issues, it also has more immediate effects including higher losses because the trapped charge increases the on-state resistance [47]. Therefore, measuring the dynamic on-resistance has become common practice to determine if the dynamic on-resistance is affected by this condition during switching. Measuring the dynamic on-resistance requires accurate measurement of the drain-source voltage when the device is in the 'on-state'. The normal high voltage passive probe currently used to measure the drain-source voltage does not provide enough resolution at these lower voltages because it has such a large magnitude range to measure. To overcome this, many clamping circuits are

available that will clamp the drain-source voltage to a low voltage when the device is on for more accurate measurements. The clamping circuit to be used is shown in Fig. 69. This circuit was specifically made for testing GaN HEMT devices which are also fast devices so using it for the vertical GaN should be sufficient.

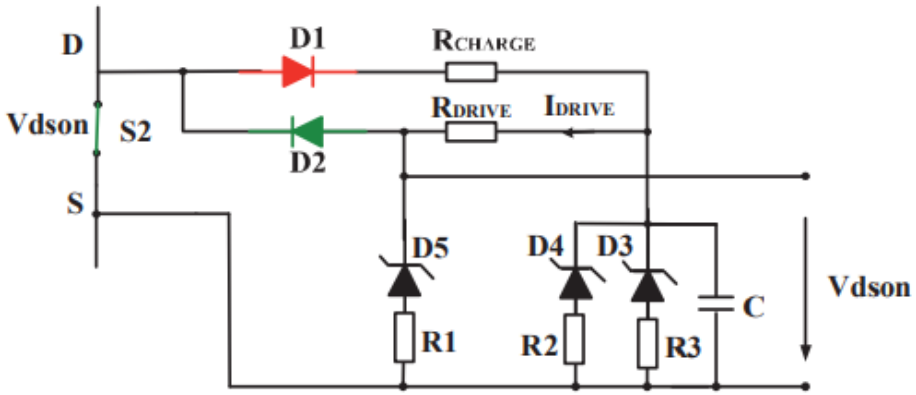

Fig. 69: Dynamic on-resistance measurement circuit from [48]

When the device is in the off-state, current flows through D1 to charge C which, in this case, is a 100 μF electrolytic capacitor. This stores charge which is used to supply the rest of the circuit when the device is in the on-state. The voltage measured across this measurement circuit is the clamped voltage which is set by the Zener diodes D3 and D4. During the on-state, the current flows out of the capacitor and out through Schottky diode D2. This means that by measuring the voltage over Zener D5, and subtracting the voltage dropped over Schottky diode D2, the on-state drain-source voltage can be found. Then by using the measured drain current, the on-state resistance can be calculated.

R_{DRIVE} is set to 100 Ω as suggested by the paper as to supply enough current to the SiC Schottky diode D2 that the voltage dropped across it won't change. R_{CHARGE} is set to 750 kΩ to keep a low current flow throughout the circuit during the on-state.

To verify the functionality of this circuit, it was tested on one of Wolfspeed's 1200 V, 80 mΩ SiC MOSFETs. The components were soldered onto a perforated board and attached to the bottom of a double pulse test board for SiC devices, as shown in Fig. 70. The measurements are taken using a low voltage passive probe. The same probe used for measuring the gate-source voltage (TPP0500).

Fig. 70: Attachment of the dynamic-on resistance board for measurement

Fig. 71 shows the comparison of the drain-source voltage being measured using the high voltage probe (TPP0850) with the measurement using the clamping circuit. It shows just how much of a different there is when measuring the drain-source voltage is with and without the clamping circuit at the lower voltages. Because the measurement is much more precise, an accurate on-state resistance can be calculated using the drain current waveform.

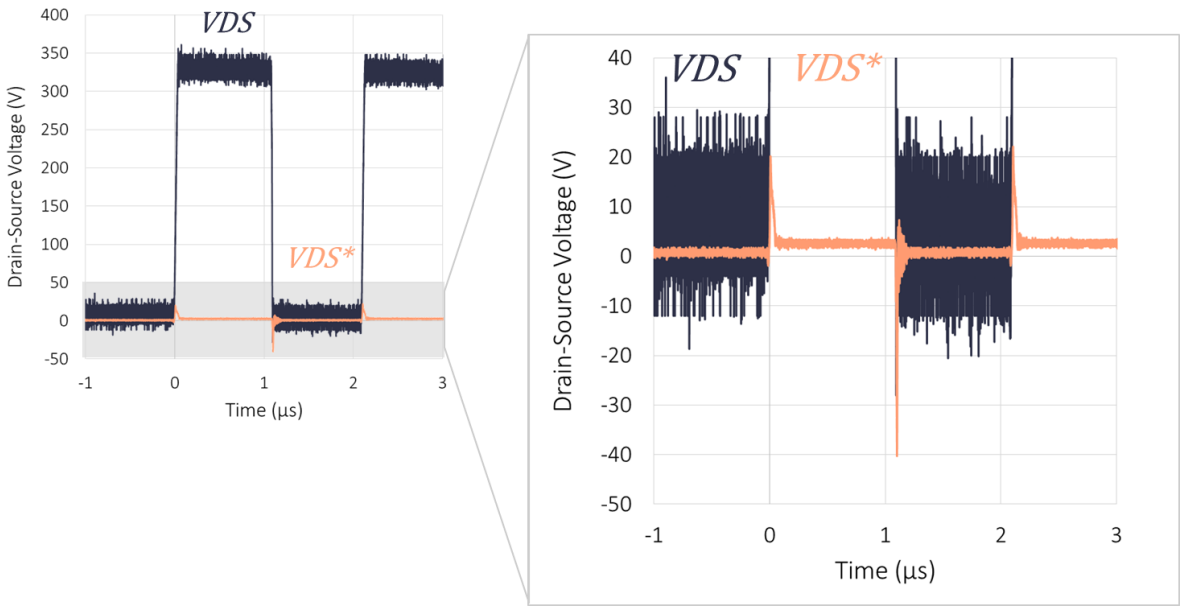

Fig. 71: Comparison of measurement of VDS using clamping circuit

A problem seen with the circuit is that there are large peaks in the measurements due to the capacitance of the SiC Schottky diodes (D1 and D2 in Fig. 69) which stores charge and causes those spikes by releasing it.

Fig. 71 shows that there is a very large peak in the orange curve that was not picked up in the overall drain-source voltage. This peak should be reduced to get the most accurate results over the duration of the on-state. Different sized diodes were tested, each with different capacitances and the results are shown in Fig. 72. As the capacitance got smaller, the peak also got smaller so the diodes to be used are the C3D03060.

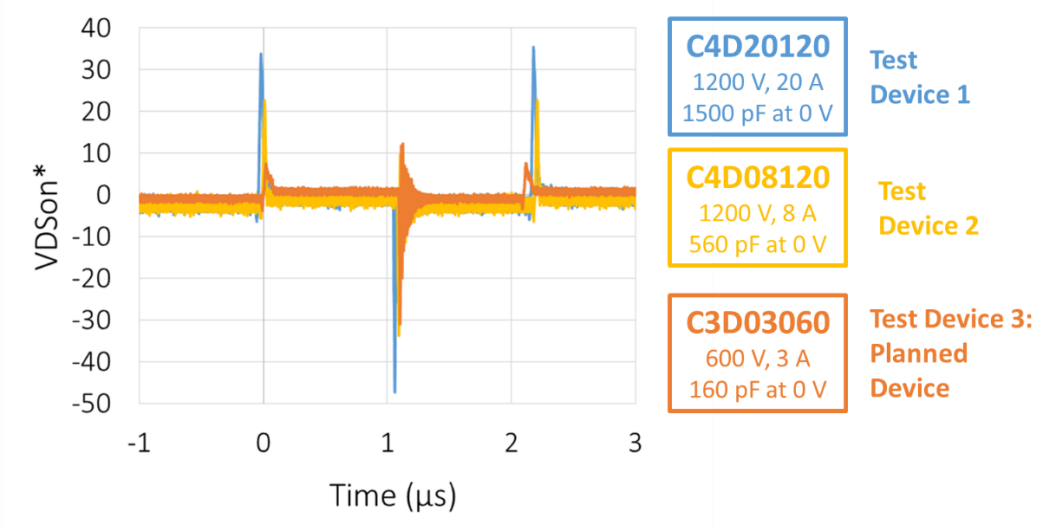

Fig. 72: Comparison of spikes in measurement based on diode selection

After minimizing the spike in the measurement, the voltage of the clamping circuit was measured again. This measurement was taken at 200 V and 7 A. The current was then used to calculate the on-state resistance and the corresponding curve is shown in Fig. 73. It shows that at steady state when the device is on, the resistance is 70 mΩ, which is around what is expected. Fig. 74 shows the static on-state measurement of this device and at a current of 7 A is it a little less than 70 mΩ. This is smaller than the dynamic measurement due to trace resistances that are added on the PCB.

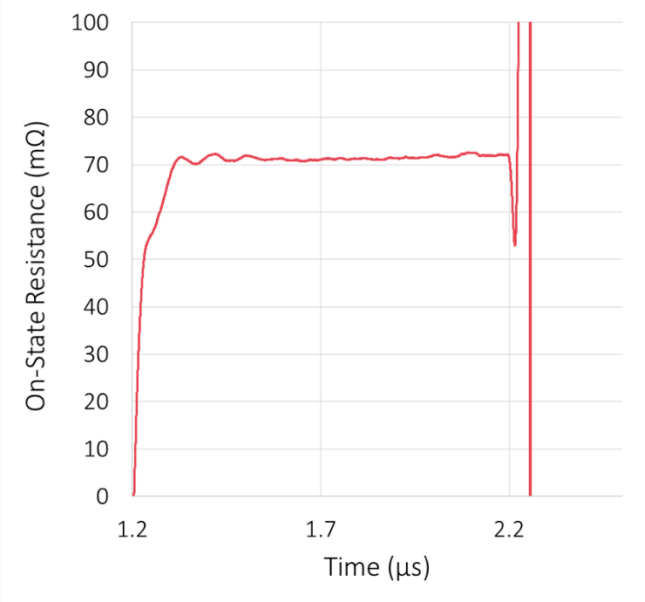

Fig. 73: Dynamic On-state Resistance measurement for 80 mΩ SiC device

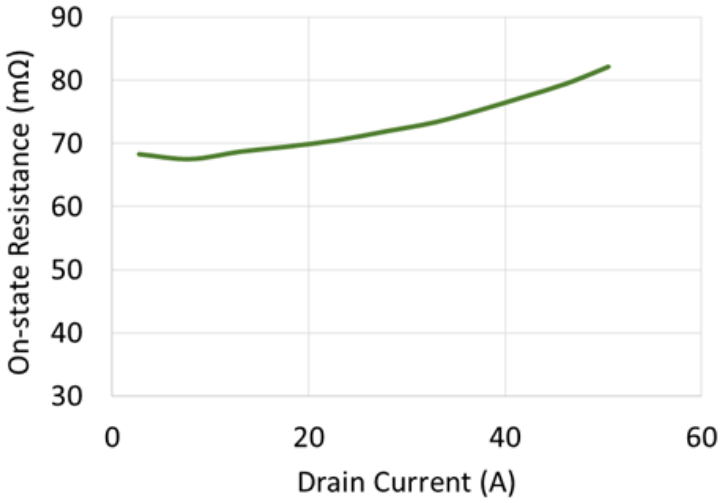

Fig. 74: Static measurement of the dynamic on-resistance at a gate-source voltage of 20 V

Since the test circuit was shown to be functional and accurate, it was integrated into the PCB used to perform the double pulse testing of the vertical GaN transistor. The new PCB is shown in Fig. 75, the clamping circuit is circled in red. The diode is shown coming out

of the bottom of the PCB, this was done to conserve space on top of the PCB so that the circuit could be placed as close to the device under test as possible.

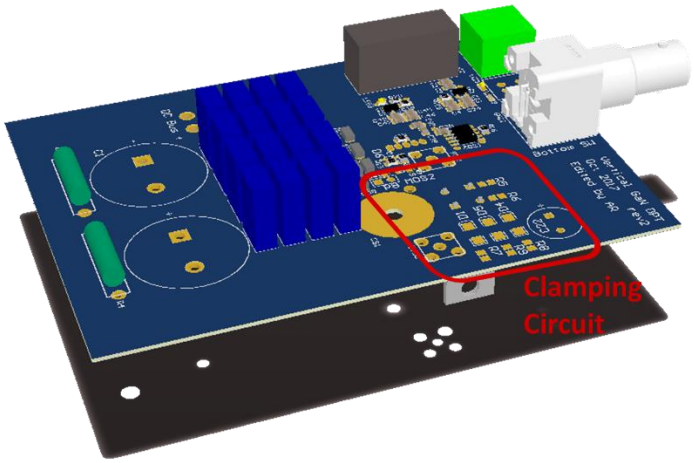

Fig. 75: Clamping circuit integrated into the double pulse test board

Chapter 5 Conclusion

5.1 Summary

This paper has shown the characterization of a variety of SiC MOSFETs from different manufacturers. These devices have current ratings ranging from 30 A up to 75 A and voltage ratings from 650 V to 1.2 kV. A comparison of the different performances of the devices was also included.

A short-circuit characterization of a 900 V, 10 mΩ SiC MOSFET was presented. This study found that when subjected to short-circuit operation, the device can withstand 4.5 μs at room temperature or 4.2 μs at 100 °C before it breaks. It was also found that as the external gate resistance is changed, the waveforms start to get noisier which could also add more stress to the device.

The characterization of HRL's 600 V, 2A, normally-off, vertical GaN transistor under static and dynamic testing was also presented. The fabrication process as well as the method used to test such a particular device were described. From the static characterization, it was shown that the device has a 3.3 V threshold voltage, a blocking voltage of 600 V, and an on-state resistance of 880 mΩ. Also, a recommended gate drive voltage of 8 V, which was determined from the output characteristics, was carried over into

the dynamic testing. In the switching tests, the device was subjected to drain-source voltages up to 450 V and load currents up to 2 A. This was done for three different external gate resistor values which showed faster switching as the resistance was decreased. At a drain-source voltage of 450 V and a load current of 2 A, the device switched at 77 V/ns at turn-on, and 33 V/ns at turn-off. This results in turn-on and turn-off losses of 8.12 µJ and 3.04 µJ respectively. These results show the great potential that vertical GaN has, while still not approaching the theoretical performance limits.

5.2 Future Work

This study has shown the characterization of many different newly developed SiC MOSFETs. To build upon this study, characterizations of new devices can be performed. Newer and greater wide-bandgap semiconductors are quickly being developed and it is important to have a benchmark of the devices coming out so that when they are being selected for power converter design, there is a good understanding of how the devices will actually perform.

Further short-circuit characterization tests can be performed also. There is a new version of Device A which has a Kelvin source connection included. It is expected that the Kelvin source connection will allow the device to withstand short-circuit operation longer than it's 3 pin version. A characterization and comparison of this new device would give an example of how different packaging methods may now be required for wide-bandgap semiconductors [49].

Future work for the vertical GaN transistor includes testing the dynamic on-state resistance of the devices using the method explained previously. Also, as the device technology advances, switching characterization at higher drain-source voltages will also be needed.

After this characterization Device A was selected to be used in a half-bridge power module design as a continuation of this project. The details are included in Appendix B.

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Appendix A Estimating the Short-Circuit Current Capabilities

To estimate the short circuit current capability of the device, the transfer characteristics were used. The transfer characteristics show how much current the device will transfer with respect to the gate voltage at a fixed drain-source voltage. On the transfer characteristics curve there is a linear region which shows a direct relationship between the current and the gate-source voltage. By using this relationship, a good estimate of how much current will be transferred during short-circuit operation can be found. This is under the assumption that the drain-source voltage magnitude does not affect this relationship. The expected short-circuit current is then found by looking at the current at the operating gate voltage, if only operating under this relationship. In the transfer characteristics curve, the relationship between the gate-source voltage and the drain current is found. The basic relationship is that after the threshold voltage is reached on the gate-source voltage, the current increases linearly and then saturates at a certain point.

To find the expected current level at the operating gate voltage, the slope of the current rise is found in the linear region and extrapolated further. To do this, the transfer

characteristics curves were plotted in MATLAB (as can be seen in Fig. 76 for the 80 mΩ, 1.2kV, Wolfspeed device) and a polynomial was fit to this curve, which can been seen in Fig. 77 by the dotted green line. This method was first tested with the 80 mΩ device because the short-circuit current is available in many different publications due to extensive short-circuit characterization of this device. According to studies the expected short-circuit current should be around 180 A [28].

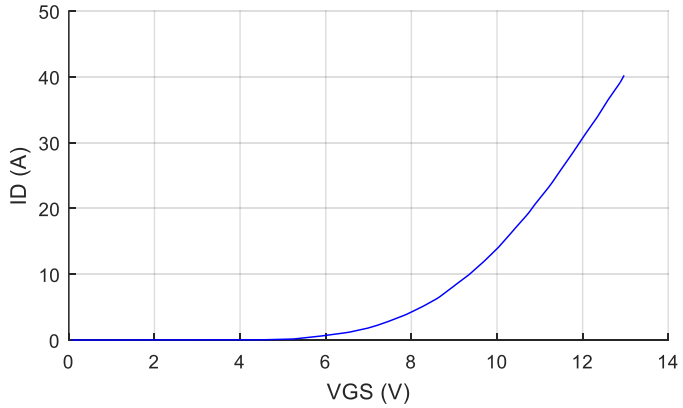

Fig. 76: Transfer Characteristics curve of the 1.2 kV, 80 mΩ SiC MOSFET from Cree

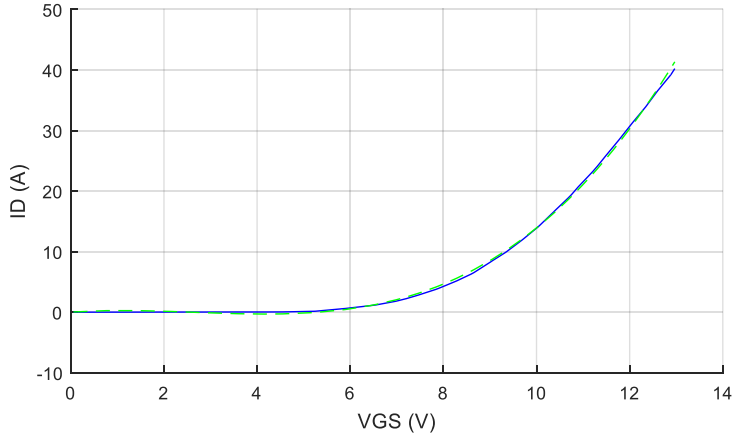

Fig. 77: Fitted polynomial to transfer characteristics curve of 1.2 kV, 80 mΩ SiC MOSFET from Cree

Fig. 78 shows how the line that was fit to the curve in MATLAB is extrapolated to the gate voltage that the device will be held at during short circuit operation (20 V for the 80 mΩ device). This results in an estimated 205 A during short circuit operation. This is similar to the actual measured results in the paper at 180 A. The actual current during test is expected to be lower because of physical limitations during testing for example stray parasitics of the PCB. Since the results were similar to the calculated estimate, this method was repeated for the 900 V, 10 mΩ SiC MOSFET. The results, shown in Fig. 79, show that the estimated short circuit current of this device as 1060 A.

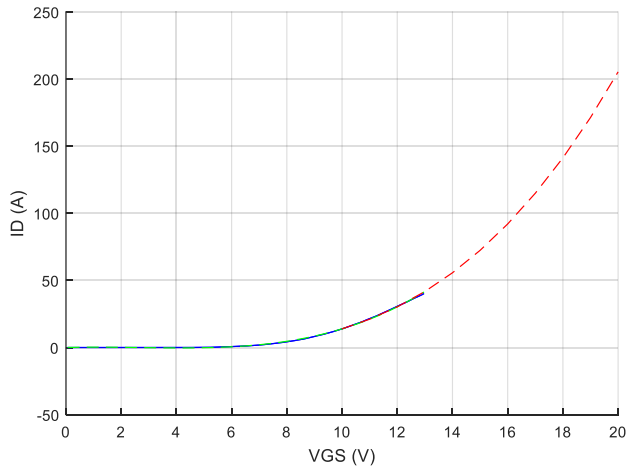

Fig. 78: Extrapolated transfer characteristic curve to estimate the short circuit current for the 1.2 kV, 80 mΩ SiC MOSFET from Wolfspeed

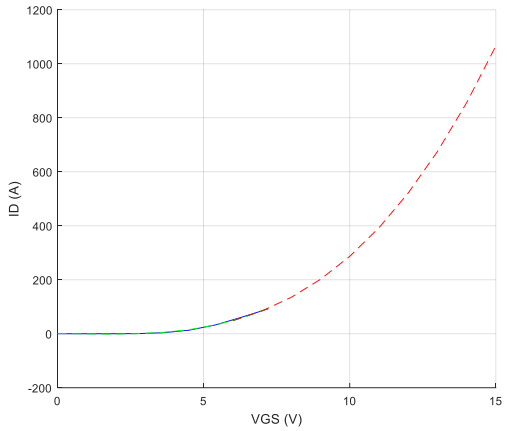

Fig. 79: Estimated short circuit current of the 900 V, 10 mΩ SiC MOSFET

Appendix B Current Sharing in a Compact, Low Inductance 900 V, 5 mΩ SiC Half-Bridge Power Module

This section discusses the design and fabrication of a 900 V, 5 mΩ SiC half-bridge power module. The design of the power module includes a MOSFET only design and introduces the use of a flexible circuit to connect to the gate and source of the die. Also included is an analysis of the symmetrical design of the power module by looking at the current sharing of balanced and unbalanced die. The switching properties of the power module are tested using a clamped inductive load tester and the effects of current load imbalance among the die are measured.

B. 1 Module Design and Simulations

In order to get a compact power module, Device A, a 900 V, 10 mΩ SiC MOSFET is used. The device's high current carrying capability allows for higher power capabilities with the need for fewer die. Some studies have found power module designs that have better power commutation based on the placement of the SiC MOSFETs and the

antiparallel diodes [50], [51]. By using the body diode in the SiC MOSFET instead of external antiparallel diodes, this problem can be eliminated.

Due to the faster switching of SiC devices, the inductance in a power module needs to be as low as possible. High inductances cause overshoots and ringing in the operation of the module. In this case, a flexible circuit is utilized for the gate loop and with this method, a gate loop inductance of 0.3 nH is achieved. The power loop inductance was also minimized through multiple design iterations with the final inductance being 3.9 nH.

The last design feature is the use of a symmetrical design. Having a balanced/symmetrical DBC pattern in the power module is important so that every die shares the load evenly. If the DBC is not balanced, each die will experience different current loads especially during turn-on [53]. The symmetry was observed by simulating the module design in LTSpice. The module parasitics and the flexible gate circuit were extracted and exported into LTSpice where the simulation models for the 900 V, 10 mΩ die were also included. Fig. 80 shows the configuration of the power module. The two bottom positions in the half-bridge were analyzed. The current was simulated before the power module design was balanced completely and then again after the module had been determined to be balanced by ANSYS Q3D simulations. The current simulations shown in Fig. 80 indicate that not only is the power module balanced but there is less stress on the die in position C due to having a more balanced design.

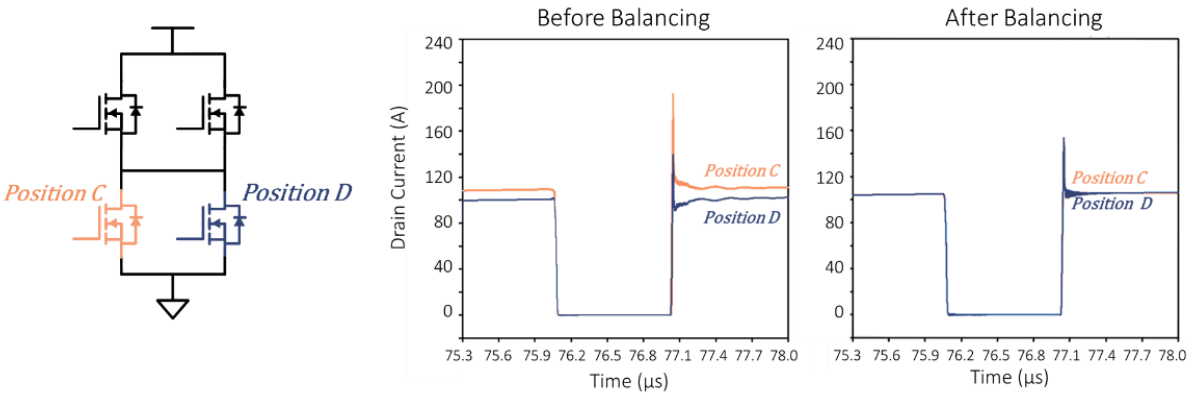

Fig. 80: Simulation of the current sharing characteristics for a symmetrical and non-symmetrical design

A 3D render of the final design is shown in Fig. 81. The patterned DBC is shown with the die on top. The base plate and housing are also included. A large current return path allows for the positive and negative power terminals to be closer together, which decreases the inductance between the two.

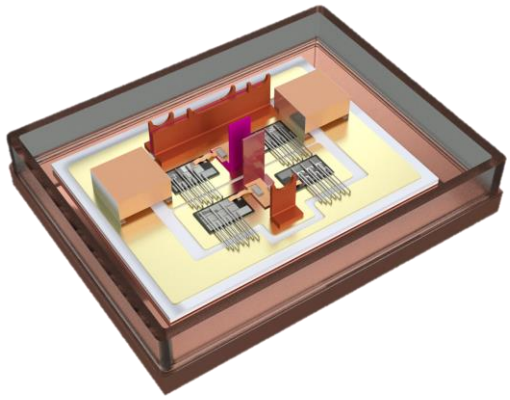

Fig. 81: 3D model of half-bridge power module design

B. 2 Module Fabrication

The fabrication of the power module starts with the substrate which is an AlN DBC with a gold coating. An AlN substrate is being used because it has better thermal conductivity

than Alumina and is more readily available than other substrates like Silicon Nitride [54]. Fig. 83 shows the patterned substrate. To pattern the substrate, the designed pattern is cut into Kapton tape using a laser cutter. The parts of the pattern to be etched are then exposed by removing the Kapton tape in that area. The gold and copper on the substrate are then etched away using a ferric chloride etch. To attach the die to the gold coated substrate, a nanosilver sintering paste from Kyocera was used in pressure-less conditions. The silver sinter paste is extruded in squares, again using Kapton as a stencil. After the die are placed onto the silver paste, the substrate is put through a heating profile. The power terminals and the flexible gate are connected using solder paste. The copper base plate is connected using a solder preform so that there is a uniform connection which will result in a better thermal impedance. The die are connected by using 10 mil wire bonds. To allow for high currents to flow through the power module, nine wire bonds are needed per die.

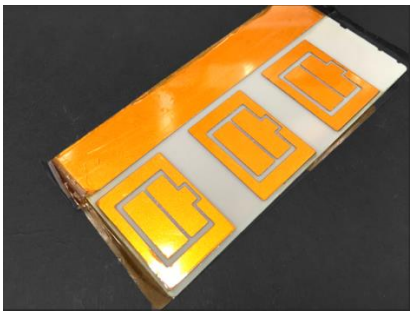

Fig. 82: Patternend substrate with Kapton tape on top

The first power module has die with on-state resistances that vary so that the power module is unbalanced. Fig. 83 shows the static characteristics of some of the die which were measured using a B1505a curve tracer from Keysight. The resulting layout with the unmatched die is shown in Fig. 83. Die 5 and Die 6 (which are in top switch position of

the module) have similar on-state resistances. Die 2 has the highest on-state resistance measured and Die 8 has the lowest on-state resistance measured. These two were both placed in parallel in the bottom switch position so that the current imbalance during switching can be tested. The actual power module after fabrication is shown in Fig. 84.

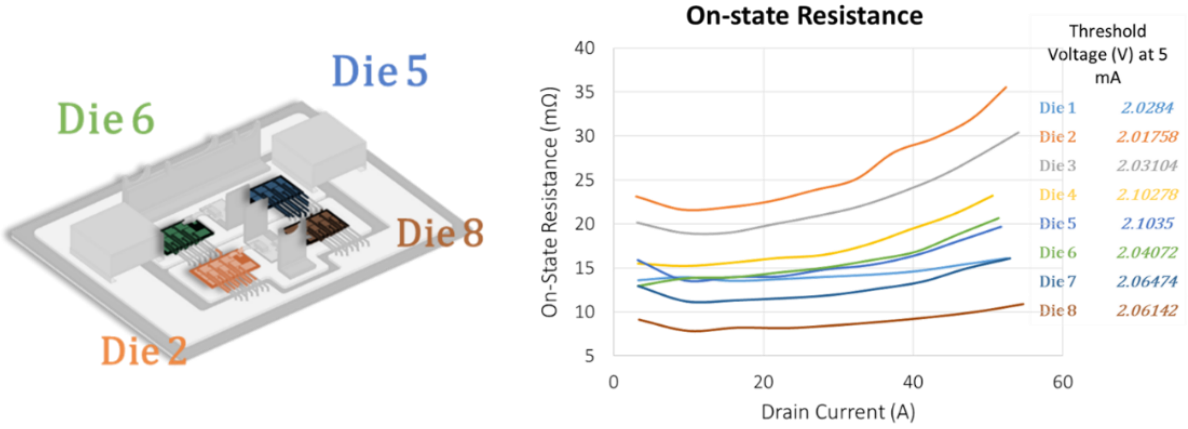

Fig. 83: Die selection for the power module based on on-state resistance characteristics

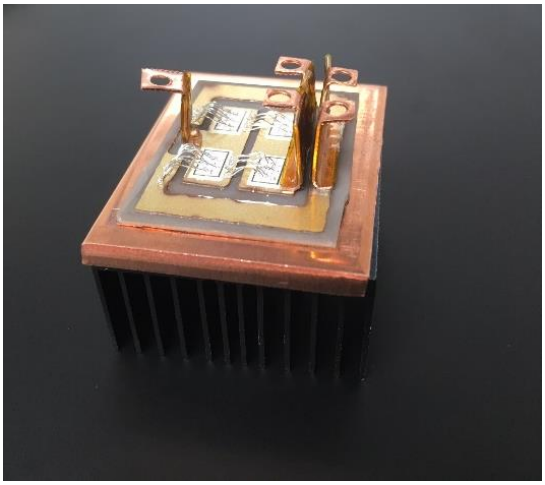

Fig. 84: Fabricated power module for testing

B. 3 Static and Dynamic Characterization

To test the functionality of the half-bridge SiC power module, after fabrication a static and dynamic characterization will be performed. The static characterization will include output and transfer curves of the power module. To test the dynamic performance of the power module, it will be tested using a clamped inductive load tester. Two PCBs were designed to test the power module and are shown in Fig. 85. The capacitor bank is for the power loop and connects to a 600 V power supply. The gate driver PCB has dual gate driver functionality so that the top devices and bottom devices can be switched independently. These boards were both designed to easily attach to the power module for testing via pins coming off of the power module.

During the dynamic tests, the power module will be tested under different load currents. Also, as mentioned before, the individual die currents in the bottom position (position C and D from Fig. 80) for both the balanced and unbalanced power module will be monitored. These currents will be measured using a Rogowski coil which will be put around the wire bonds of the die. With this data, it can be seen how the die behave in both the balanced and unbalanced power module to determine how much of an affect it has on the performance of the power module in terms of losses and switching speeds. The gate-source voltage will be measured using a 300 V single-ended passive probe (Tektronix P6139B) and the drain-source voltage will be measured using a 2.5 kV single-ended passive probe (Tektronix P5100). Both of these measurements will be made on the PCBs.

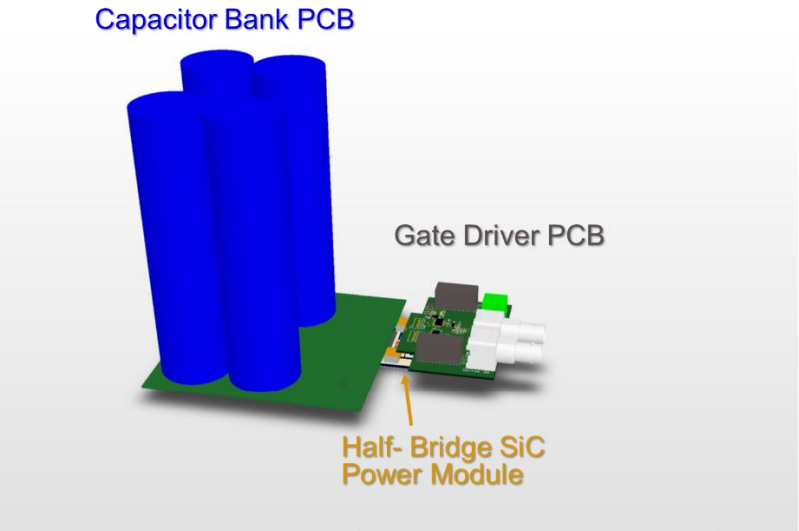

Fig. 85: Tester for the half-bridge power module

During the dynamic tests, the temperature of the power module will also be monitored using thermocouples and a thermal camera to see how well the power module handles thermal dissipation.