Linearity Enhancement of High Power GaN HEMT Amplifier Circuits

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Abstract

Gallium Nitride (GaN) technology is capable of very high power levels but suffers from high non-linearity. With the advent of 5G technologies, high linearity is in greater demand due to complex modulation schemes and crowded Radio Frequency (RF) spectrum. Because of the non-linearity issue, GaN power amplifiers have to be operated at back-off input power levels. Operating at back-off reduces the efficiency of the power amplifier along-with the output power. This research presents a technique to linearize GaN amplifiers. The linearity can be improved by splitting a large device into multiple smaller devices and biasing them individually. This leads to the cancellation of the Third-order Intermodulation Distortion (IMD3) components at the output of the FETs and hence higher linearity performance.

This technique has been demonstrated in Silicon technology but has not been previously implemented in GaN. This research work presents for the first time the implementation of this technique in GaN Technology.

By the application of this technique, improvement in IMD3 of 4 dBc has been shown for a 0.8-1.0 GHz Power Amplifier (PA), and 9.5 dBm in Third-order Intercept Point (OIP3) for an S-Band GaN Low Noise Amplifier (LNA), with linearity Figure Of Merit (IP3/DC power) reaching up to 20.

Large-signal simulation and analysis have been done to demonstrate linearity improvement for two parallel and four parallel FETs. A simulation methodology has been discussed in detail using commercial CAD software. A power sampler element is used to compute the

IMD3 currents coming out of various FETs due to various bias currents. Simulation results show by biasing one device in Class AB and others in deep Class AB, IMD3 components of parallel FETs can be made out of phase of each other, leading to cancellation and improvement in linearity. Improvement in IMD3 up to 20 dBc has been reported through large-signal simulation when four parallel FETs with optimum bias were used.

This technique has also been demonstrated in simulation for an X-Band MMIC PA from 8-10 GHz in GaN technology. Improvements up to 25-30 dBc were shown using the technique of biasing one device with Class AB and other with deep class AB/class B. The proposed amplifier achieves broadband linearization over the entire frequency compared to state-of-the-art PAs. The linearization technique demonstrated is simple, straight forward, and low cost to implement. No additional circuitry is needed. This technique finds its application in high dynamic range RF amplifier circuits for communications and sensing applications.

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General Audience Abstract

Power amplifiers (PAs) and Low Noise Amplifiers (LNAs) form the front end of the Radio Frequency (RF) transceiver systems. With the advent of complex modulation schemes, it is becoming imperative to improve their linearity. Through this dissertation, we propose a technique for improving the linearity of amplifier circuits used for communication systems. Meanwhile, Gallium Nitride (GaN) is becoming a technology of choice for high-power amplifier circuits due to its higher power handling capability and higher breakdown voltage compared with Gallium Arsenide (GaAs), Silicon Germanium (SiGe) and Complementary Metal-Oxide-Semiconductor (CMOS) technologies.

A circuit design technique of using multiple parallel GaN FETs is presented. In this technique, the multiple parallel FETs have independently controllable gate voltages. Compared to a large single FET, using multiple FETs and biasing them individually helps to improve the linearity through the cancellation of nonlinear distortion components. Experimental results show the highest linearity improvement compared with the other state-of-the-art linearization schemes. The technique demonstrated is the first time implementation in GaN technology.

The technique is a simple and cost-effective solution for improving the linearity of the amplifier circuits. Applications include base station amplifiers, mobile handsets, radars, satellite communication, etc.

गुरुब्रह्मा गुरुविष्णुः गुरुदेव महेश्वर।
गुरुसाक्षात परब्रह्मा तस्मै श्रीगुरवे नमः॥

ऋषि वेद व्यास (गुरु गीता)

The Guru is Brahma, the Guru is Vishnu, the Guru is Siva.
Indeed, the Guru is the Supreme Absolute.
To that Guru, I offer my reverent salutations.

Rishi Ved Vyas (Guru Gita)

I dedicate this dissertation to all my teachers and mentors.

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Chapter 1

Introduction

1.1 Motivation

1.1.1 RF Communication System

Fig. 1-1 shows a block diagram of a generic transceiver in a Radio Frequency (RF) communications system. It consists of two sections: receiver (for receiving RF signals) and transmitter (for transmitting) which are separated by a duplexer or a switch depending on the multiple access scheme used for communication purposes. The function of the transmitter is to drive the antenna to generate sufficiently high power electromagnetic waves so that the signal can travel sufficient distances for the given application. The receiver must sense a small received signal and must amplify the signal with low noise for subsequent processing [1]. Linearity is critical for systems transmitting carriers with complex modulation schemes and also for the receivers [2].

The Power Amplifier (PA) in the transmitter part and the Low Noise Amplifier (LNA) in the receiver part form the most critical blocks. With the advent of 5G communications and signals with high Peak to Average Power Ratio (PAPR), there is an increasing demand for highly linear PAs [3], [4].

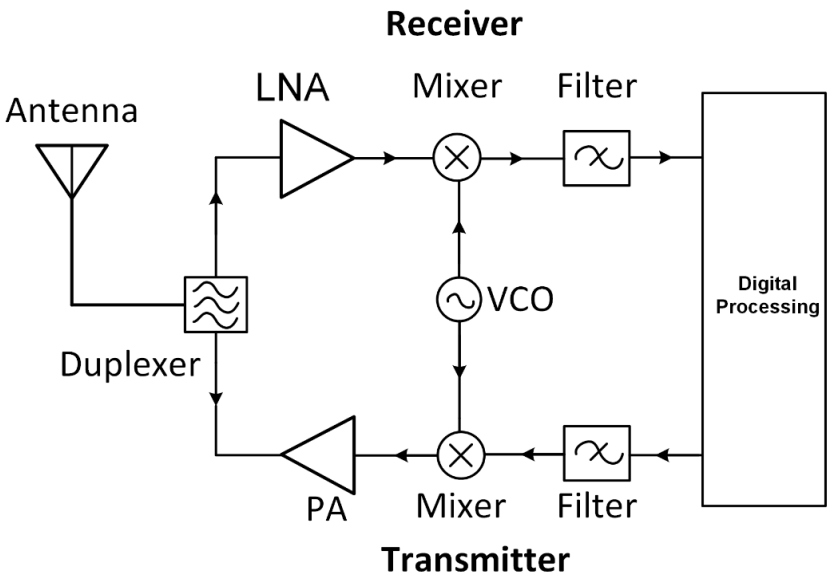


Fig. 1-1: Generic block diagram of a transceiver in a RF system.

High linearity is also needed for LNA's and the mixers. Parameters such as Third-order intercept point (IP3), Second-order intercept point (IP2) are used to characterize their linearity.

1.1.2 GaN Semiconductor Technology

Gallium Nitride (GaN) has emerged as the technology of choice for high-power RF/ microwave applications because of its multiple material advantages compared to conventional technologies, such as Gallium Arsenide (GaAs), Silicon Germanium (SiGe) and Complementary Metal-Oxide-Semiconductor (CMOS) technologies, etc. as shown in Table 1-1[5].

Table 1-1: Comparison of properties of semiconductor materials as presented in [5] .

Material Properties	**Si**	**GaAs**	**GaN**
Band Gap Energy (eV)	1.1	1.4	3.4
Electron Mobility (cm^2/V-s)	1100	6000	1350
Breakdown Electric Field (V/cm)	3.0×10^5	$4\text{-}5 \times 10^5$	4.0×10^6
Saturation Velocity (cm/s)	1.0×10^7	2.0×10^7	2.7×10^7
Power Density (W/mm)	0.8	1.0-1.5	7
FET Technology	LDMOS	HFET	HFET

GaN has significantly higher bandgap energy and higher breakdown field intensity. This translates to higher operating voltages and output impedance closer to 50 ohm for the GaN devices, resulting

in easier matching, wider bandwidth, and higher efficiency [6]. Commercial systems operate at 28 V, and a low-voltage technology would need to step down from 28 V to its required voltage. However, GaN devices can easily operate at 28 V, and up to 42 V potentially. This reduces power requirements and simplifies cooling, which is another advantage for GaN-based systems [7]. However, GaN devices suffer from a significant challenge of high non-linearity because of the inherent device structure. This can be attributed to the presence of traps and significant gate leakage currents due to the presence of the Schottky barrier caused by a large input swing. GaN devices have softer compression characteristics compared to other technologies, showing greater separation between 1-dB compression point (P_{1dB}) and saturated output power (P_{sat}). These devices are usually operated at back off to achieve sufficient linearity, but this reduces the efficiency [6]. GaN MMIC's are now being developed and used for space [8]–[11], ground-based commercial applications [12]–[14], millimeter wave [15]–[17], power electronics [18]–[20], etc.

1.2 Linearity Metrics

An amplifier is considered to be linear if the output increases linearly with input power. However, real amplifiers begin to saturate at certain input power levels, i.e., the output no longer increases linearly with input power. The following metrics are typically used to describe the linearity of RF/microwave amplifiers. Among these metrics: IMD (Intermodulation Distortion), ACPR (Adjacent Channel Power Ratio) and EVM (Error Vector Magnitude) are typically used to characterize PA linearity, and IP3 (Third-order intercept point) is used for characterization of LNA. 1-dB compression point can be used for both PA and LNA. They are discussed in the following sections.

1.2.1 1-dB Compression Point

The 1-dB compression point refers to the output power level at which the amplifier's transfer characteristic (gain) deviates from ideal linear characteristic by 1-dB [21]. The output power at this point is typically designated as OP_{1dB} or P_{1dB} and the input power is designated by IP_{1dB}. This compression is due to the nonlinearities that are generated as the output signal starts clipping [22]. This is illustrated in Fig. 1-2. With the increase in linearity of the amplifier, the P_{1dB} characteristic can be raised [22]. This means that the amplifier will compress at a higher value of Pin (Input Power).

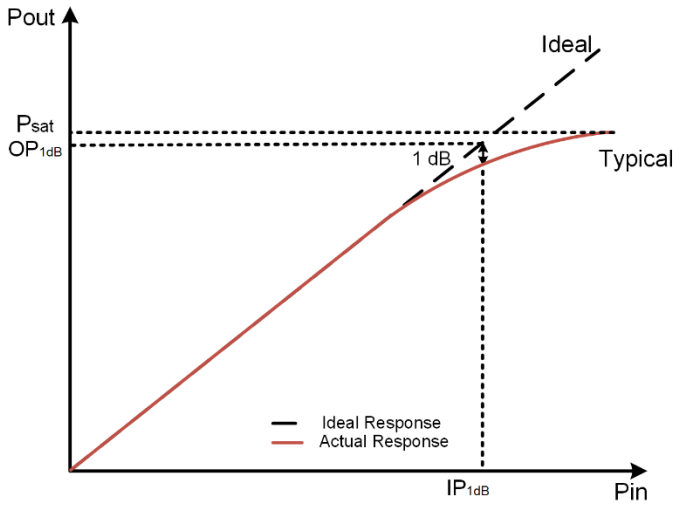


Fig. 1-2: 1-dB compression point and saturated power amplifier characteristic.

After certain power level, the output power does not increase with increase in input power. At this point, the amplifier is known as saturated and output power is known as P_{sat} as shown in Fig. 1-2. This is the maximum output power which can be achieved from an amplifier. P_{sat} is a typical characteristic of power amplifiers.

1.2.2 Two-tone Test and Intermodulation Distortion (IMD)

A two-tone test is often used to characterize the linearity of an RF/microwave amplifier. Two-tones with a frequency spacing of a few MHz or kHz are injected to Device Under Test (DUT). When the tones are applied to a non-linear amplifier, the nonlinearity causes them to mix, producing Intermodulation Distortion (IMD) products at the various sum and difference frequencies [23].

The power series expansion of output voltage from an amplifier is given by the following equation:

$$V_{out} = a_1 V_{in} + a_2 V_{in}^{\ 2} + a_3 V_{in}^{\ 3} + \ldots\ldots\ldots\ldots\ldots \quad (1)$$

Two-tone input signal is given by

$$V_{in} = V\left(\cos\omega_1 t + \cos\omega_2 t\right) \quad (2)$$

On substituting equation (2) in equation (1), the following expression is obtained:

$$V_{out} = a_1 V(\cos\omega_1 t + \cos\omega_2 t) + a_2 V^2(\cos\omega_1 t + \cos\omega_2 t)^2 + a_3 V^3(\cos\omega_1 t + \cos\omega_2 t)^3 + \ldots\ldots\ldots \quad (3)$$

Typically, the expansion is truncated at the third-order component. On substituting and solving, the output voltage is derived as shown in Appendix A.

$$V_{out} = a_1 V(\cos\omega_1 t + \cos\omega_2 t) + a_2 V^2 + \frac{a_2 V^2}{2}\left(\cos 2\omega_1 t + \cos 2\omega_2 t\right) + a_2 V^2\left(\cos(\omega_1 + \omega_2)t + \cos(\omega_1 - \omega_2)t\right) +$$
$$\frac{9a_3 V^3}{4}\left(\cos\omega_1 t + \cos\omega_2 t\right) + \frac{a_3 V^3}{4}\left(\cos 3\omega_1 t + \cos 3\omega_2 t\right) + \frac{3a_3 V^3}{4}\left(\cos\left(2\omega_1 + \omega_2\right)t + \cos\left(\omega_1 + 2\omega_2\right)t\right) +$$
$$\frac{3a_3 V^3}{4}\left(\cos\left(\omega_1 - 2\omega_2\right)t + \cos\left(2\omega_1 - \omega_2\right)t\right) \tag{4}$$

Equation (4) can be simplified as below:

$$V_{out} = a_2 V^2 + \left(a_1 V + \frac{9a_3 V^3}{4}\right)(\cos\omega_1 t + \cos\omega_2 t) + \frac{a_2 V^2}{2}\left(\cos 2\omega_1 t + \cos 2\omega_2 t\right) + a_2 V^2\left(\cos(\omega_1 + \omega_2)t + \cos(\omega_1 - \omega_2)t\right)$$
$$+ \frac{a_3 V^3}{4}\left(\cos 3\omega_1 t + \cos 3\omega_2 t\right) + \frac{3a_3 V^3}{4}\left(\cos\left(2\omega_1 + \omega_2\right)t + \cos\left(\omega_1 + 2\omega_2\right)t\right) + \frac{3a_3 V^3}{4}\left(\cos\left(\omega_1 - 2\omega_2\right)t + \cos\left(2\omega_1 - \omega_2\right)t\right) \tag{5}$$

The following products occur at the various frequencies as shown in Fig. 1-3.

- DC Term : $a_2 V^2$
- Fundamental Tone (ω_1, ω_2) : $a_1 V$
- Second-order Terms $(\omega_1 + \omega_2, \omega_2 - \omega_1)$: $a_2 V^2$
- Third-order Terms $(2\omega_2 - \omega_1, 2\omega_1 - \omega_2, 2\omega_2 + \omega_1, 2\omega_1 + \omega_2)$: $\frac{3}{4} a_3 V^3$
- Second-order harmonics $(2\omega_1, 2\omega_2)$: $\frac{1}{2} a_2 V^2$
- Third-order harmonics $(3\omega_1, 3\omega_2)$: $\frac{1}{4} a_3 V^3$

From the output spectrum as shown in Fig. 1-3, it is easy to filter out the second order terms and harmonics because they are spaced apart from the main signal in the frequency domain. However, the products occurring at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ frequencies are not easy to filter. These products cause in-band interference in the receiver. Hence, the third-order intermodulation distortion is referred by the following expression as shown in Fig. 1-4.

$$\text{IM3} = \frac{\text{Magnitude of the third order component}}{\text{Magnitude of the first order component}} \tag{6}$$

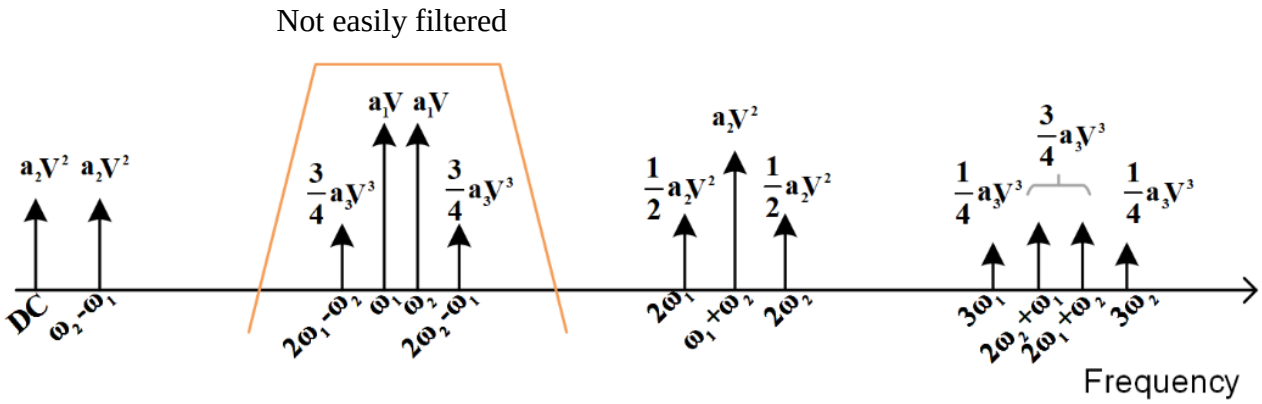


Fig. 1-3: Output spectrum of an amplifier when excited by two-tones at frequencies ω_1 and ω_2.

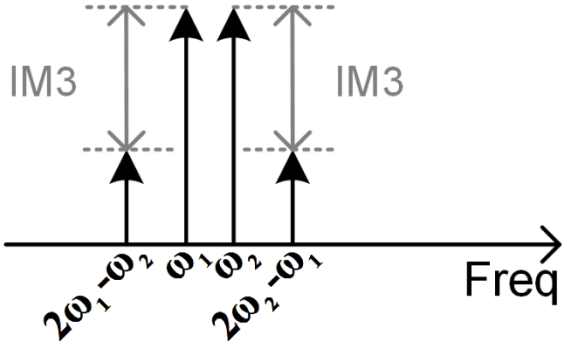


Fig. 1-4: Third-order intermodulation distortion.

$$IM3 = \frac{\frac{3}{4}a_3V^3}{a_1V} = \frac{3a_3V^2}{4a_1} \tag{7}$$

On a logarithmic scale, IMD3 is given by

$$IMD3 = 10\log\left[\frac{IM3@P_{out}}{P_{out}}\right] \tag{8}$$

The aim of the linearizing an amplifier is to lower the magnitude of IMD3 term. This can be done if the magnitude of the components occurring at frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ is reduced.

1.2.3 Third-order Intercept Point

In Fig. 1-5, the fundamental signal (with slope =1) and the third-order IMD signal (with slope =3) are shown. Typically, the amplitude of third-order IMD signal increases by 3 dB for every 1 dB increase of fundamental signal.

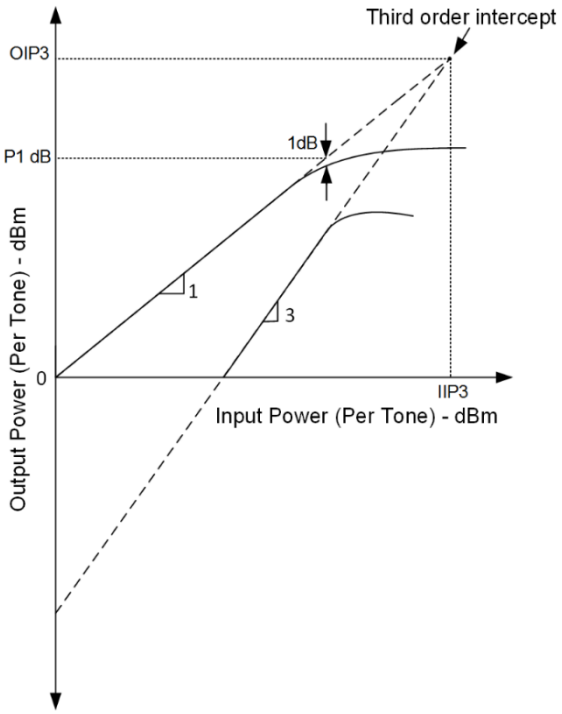


Fig. 1-5: Plot of output power of fundamental signal, IMD3 signal vs. input power.

After a certain limit, both the fundamental and third-order IMD signals began to compress. However, if we extend these slope lines, they meet at an intersection known as the third-order intercept. The output power at this point is known as the output referred third-order intercept, OIP3, and the corresponding input power is known as the input-referred third-order intercept, IIP3 [23].

A simple relation between the OIP3 and the IMD3 is given by [24]:

$$\begin{aligned} IMD3 &= 2(P_{out} - OIP3) \\ &= 2(P_{in} - IIP3) \end{aligned} \tag{9}$$

1.2.4 Adjacent Channel Power Ratio

Fig. 1-6 provides a graphical description of Adjacent Channel Power Ratio (ACPR). When a modulated wideband signal is incident on a non-linear DUT, spectral regrowth in adjacent channels may occur. ACPR is the measure of degree of signal spreading into adjacent channels caused by the non-linearities in the power amplifier.

ACPR is defined as

$$\text{ACPR} = \frac{\text{power spectral density in the main channel 1}}{\text{power spectral density in the offset channel 2 or 3}} \tag{10}$$

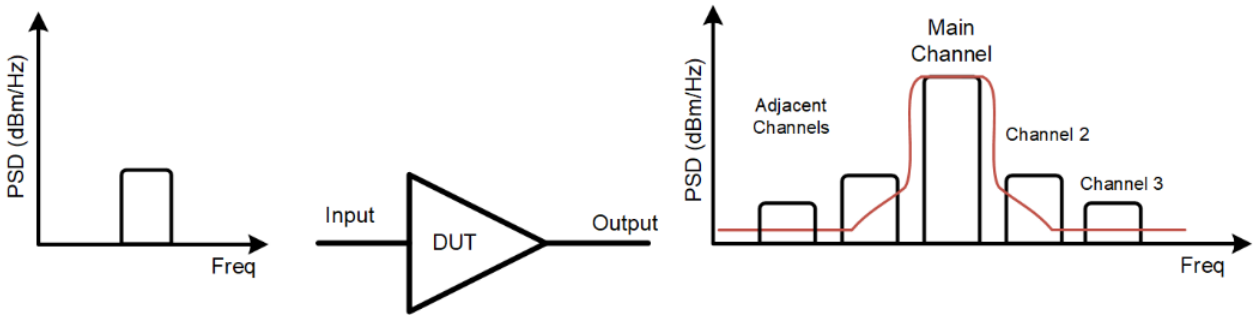


Fig. 1-6: Graphical description of ACPR measurement.

1.2.5 Error Vector Magnitude

This figure of merit is used to characterize the distortion of digitally modulated signals. A signal sent by a transmitter or received by a receiver would have all the constellation points precisely at the ideal locations. Due to the distortion of the signal, the actual constellation deviates from the ideal location as shown in Fig. 1-7. An error vector is a vector in the I-Q plane between the ideal constellation point and the point received by the receiver. Its average length is defined as the Euclidean distance between the two points, also known as Error Vector Magnitude (EVM).

EVM is equal to the ratio of the power of the error vector to the root mean square (RMS) power of the reference. It is defined in dB as

$$EVM\,(dB) = 10\log_{10}\left(\frac{P_{error}}{P_{reference}}\right) \tag{11}$$

where P_{error} is the RMS power of the error vector and $P_{reference}$ is the RMS power of the ideal transmitted signal.

EVM is defined as a percentage in a compatible way with the same definitions [25]:

$$EVM\,(\%) = \sqrt{\frac{P_{error}}{P_{reference}}}\ \text{x}\ 100\% \tag{12}$$

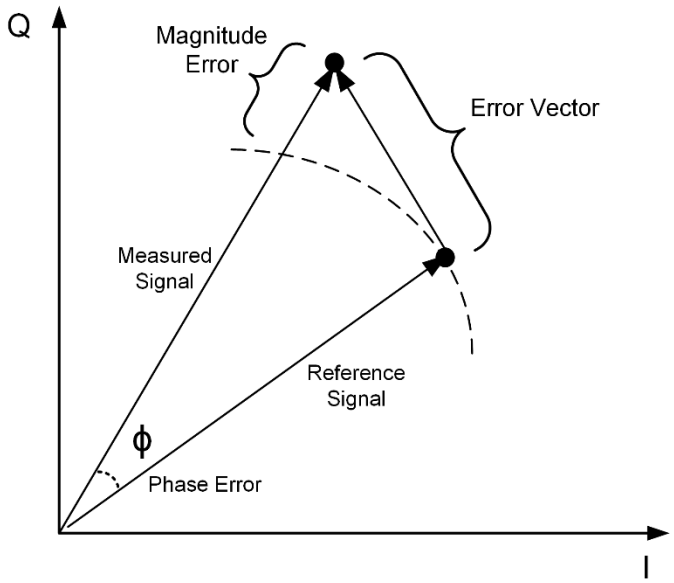


Fig. 1-7: Vector components defining Error Vector Magnitude (EVM).

1.3 Linearization

1.3.1 Operation at Back-Off

An amplifier is often operated at Back-off (BO) to obtain the desired linearity. To Back-off means to operate the PA at an input power level sufficiently lower than its 1dB compression point to obtain the desired linearity.

$$BO = P_{1dB} - P_{out} \tag{13}$$

This results in high linearity but significantly lower efficiency. Various linearization techniques aim to operate the amplifier near saturation to get higher efficiency while still achieving the desired linearity performance [22], [24].

Researchers have suggested different kinds of linearization techniques in order to achieve the required linearity. They are summarized in the following categories.

1. Feedforward
2. Feedback
3. Predistortion
4. Gm-linearization

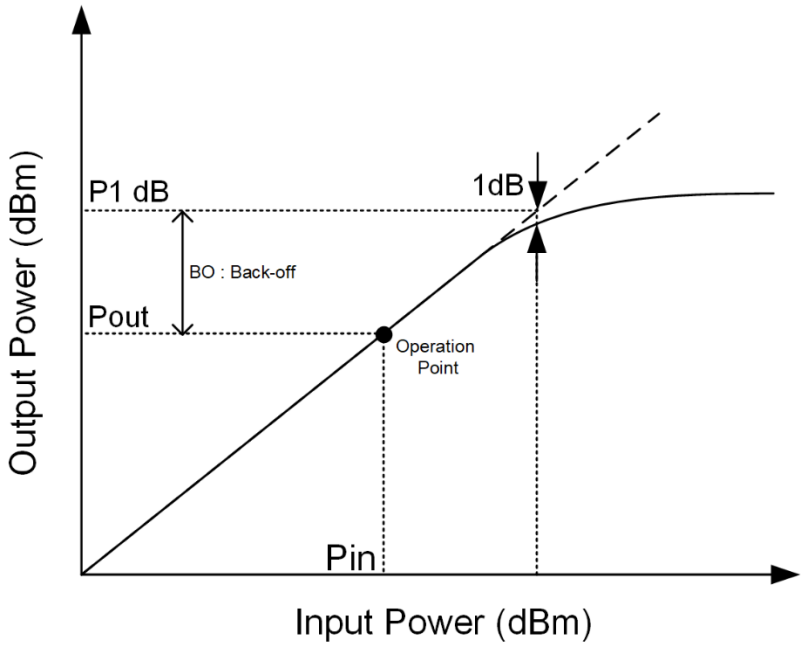


Fig. 1-8: RF power amplifier operation in Back-off.

1.3.2 Feedforward Linearization

The block diagram of feedforward system is shown in Fig. 1-9. It consists of two signal paths: one with a main amplifier and other with an error amplifier. The source signal is divided into the two paths by the power divider. The main amplifier amplifies the signal and generates intermodulation distortion products along with the amplified signal. The amplified signal is then subtracted from the main signal in the second path, such that only distortion products remain. The distortion is then amplified by the error amplifier. At the output, the amplified distortion products are subtracted from the main signal, and an undistorted version of the amplified input signal remains.

Feedforward linearization is an open-loop system and is unconditionally stable. It has a wideband operation. However, this scheme is vulnerable to temperature and process variations. Additional compensation and monitoring circuitry are needed in order to maintain good linearity over different conditions. This makes the design complex in nature. Also, the error amplifier needs to be very linear; otherwise, additional unwanted non-linearities will be generated and added to the output. The gain of the error amplifier needs to high, which degrades the overall efficiency of the system [22]. The feedforward amplifier technique has been implemented for satellite and cellular communications [26], [27].

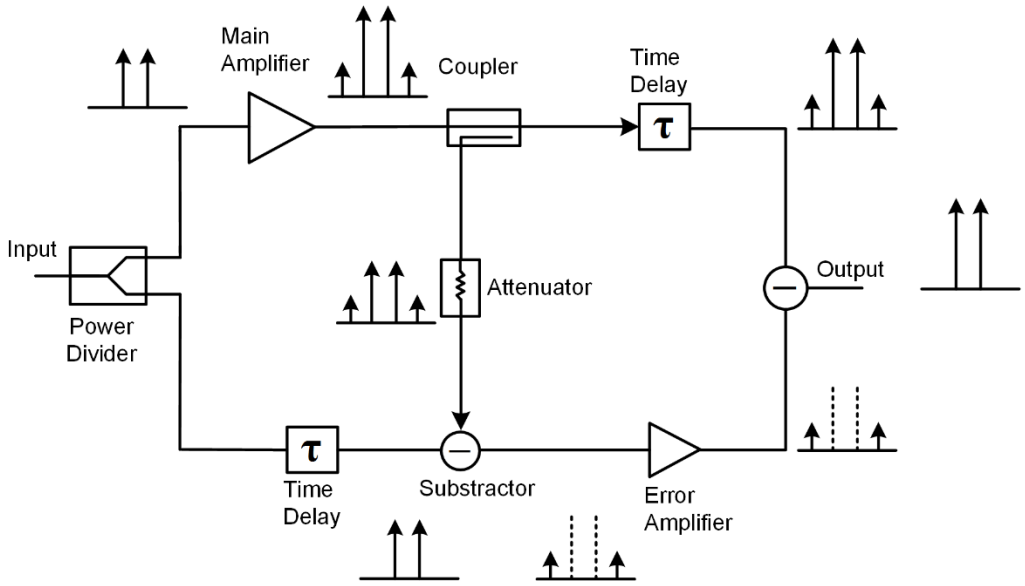


Fig. 1-9: Configuration of a basic feedforward amplifier as illustrated in [21].

1.3.3 Feedback Linearization

In this linearization scheme, the output signal is compared with the input signal to calculate the error; then, the error is fed back to the input to minimize the difference between input and output. With no feedback applied, the open loop transfer function (or amplifier gain) is given by

$$A = \frac{V_{out}}{V_{in}} \tag{14}$$

In a feedback (closed loop) configuration, the output signal is fed back to the input by the scaling factor β.

$$V_f = \beta V_{out} \tag{15}$$

The feedback signal is subtracted from the source signal V_s generating a different signal V_{in} that becomes the input signal to the amplifier.

$$V_{in} = V_s - V_f \tag{16}$$

On substituting, the closed loop transfer function A_{fb} can be solved as

$$A_{fb} = \frac{V_{out}}{V_s} = \frac{A}{1 + A\beta} \tag{17}$$

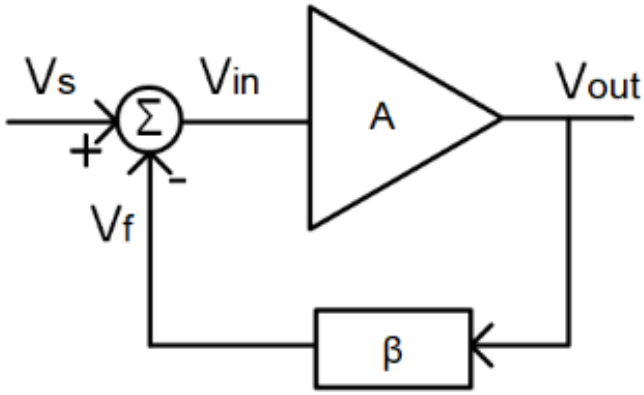


Fig. 1-10: Schematic of negative feedback amplifier.

The gain of the amplifier is reduced by the factor $1+A\beta$ which helps to linearize the amplifier. However, this scheme suffers from the drawback that if the feedback is not properly done, it will cause an increase in the gain of the amplifier, making the feedback to be positive, resulting in the oscillations. Also, this technique is suitable for narrowband applications [21], [22].
Amplifiers employing feedback have been developed for satellite communications [28].

1.3.4 Predistortion Linearization

Predistortion linearization consists in cascading a predistorter and the RF-PA. The predistorter operates in a manner that the distortion generated by predistorter is opposite to the distortion generated by the non-linear PA, as shown in Fig. 1-11. The output signal is an amplified undistorted replica of the input signal. The resulting system has little or no output distortion. Various types of predistortion techniques include analog predistortion (using diode or FET based predistorters), digital predistortion, etc.
Analog predistortion is typically more straightforward and easier to use [29], [30] than digital predistortion. The system is unconditionally stable because of the open-loop characteristic. However, real predistorters do not result in an output characteristic which is complementary to the amplifier characteristic. Hence, this technique typically results in a small improvement. Some predistorters attempt to reduce the third-order intermodulation products, but this process may increase the higher-order distortion products [21].

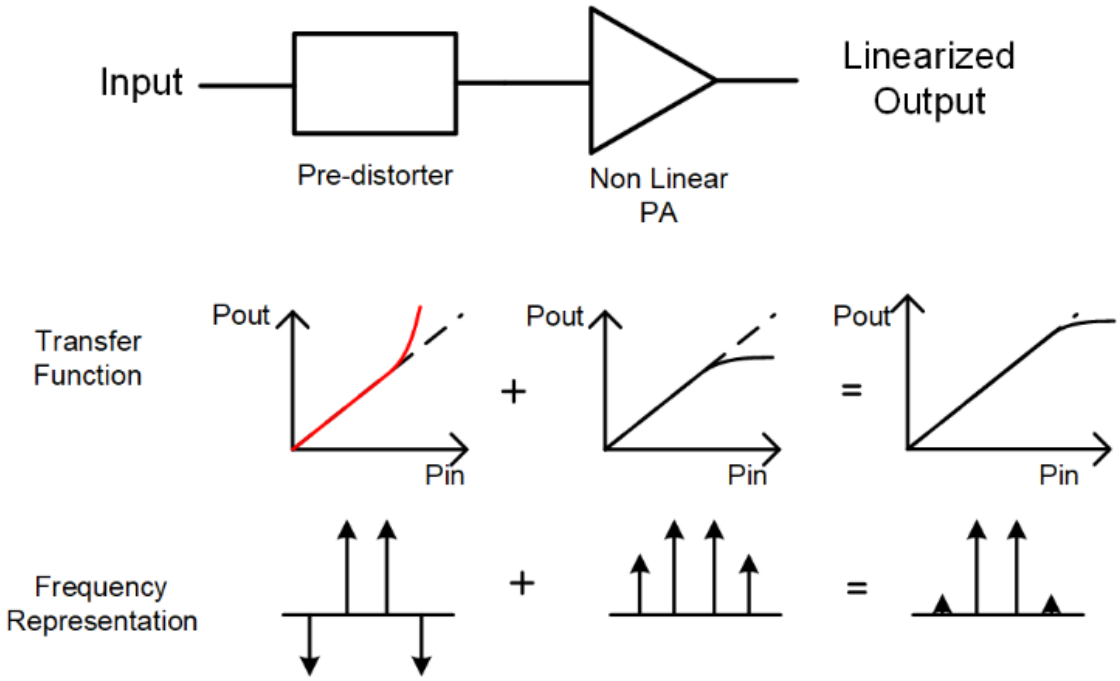


Fig. 1-11: Operation of a predistortion linearization scheme.

1.3.5 Trans-conductance Linearization

The Taylor series expansion of a common source FET is given by

$$i_{DS} = I_{dc} + g_m v_{gs} + \frac{g_m'}{2!} v_{gs}^{\ 2} + g_m'' v_{gs}^{\ 3} + \ldots\ldots\ldots \tag{18}$$

Compared with the conventional single gate transistor, an improvement in linearity performance can be achieved by using multiple transistors and biasing them individually [31]. As seen in Fig. 1-12, the negative g_m'' of the main transistor (M1) is cancelled by the positive g_m'' of the auxiliary transistor (M2) which is further cancelled by g_m'' of the third transistor (M3). The authors have reported about 6 dB improvement in IMD3.

This technique is simple and has been implemented in CMOS technology with good linearity improvement [32], [33]. This technique has been used for the lower power levels and has not been previously implemented in GaN technology.

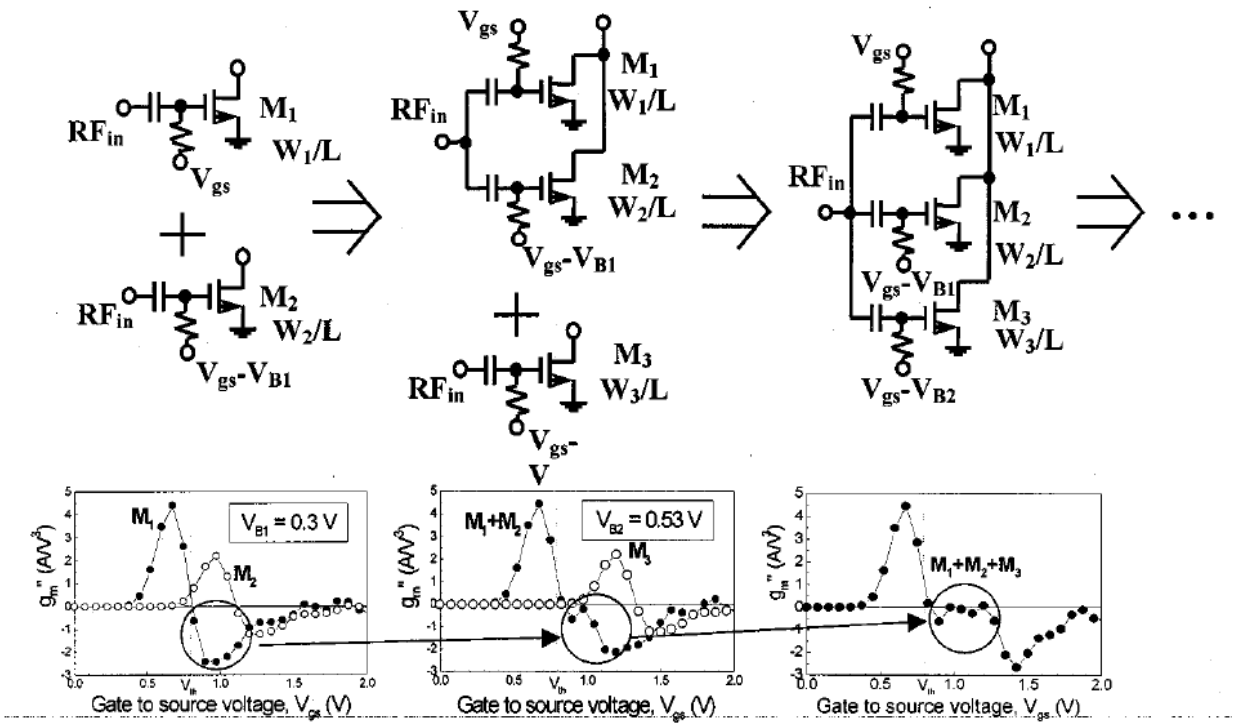


Fig. 1-12: Circuit topology for the gm linearization technique as illustrated in [31].

1.4 Dissertation Organization

The dissertation aims to improve the linearity of GaN amplifier circuits using parallel gate techniques. The approach used is to divide a large FET into multiple smaller parallel FETs and to bias them individually to cancel intermodulation products. This technique has been explored in this work for both GaN PA and GaN LNA circuits. This dissertation has been organized in the following chapters.

In Chapter 2, analysis for the proof of concept of the g_m linearization for GaN devices. The second derivative of g_m which is g_m" is computed from the measured IV characteristics, and it is found that by varying the bias, the linearity can be improved. This technique is implemented experimentally in the frequency range of 0.8 -1.0 GHz.

In Chapter 3, design of a hybrid GaN LNA is presented in S-band frequency range using parallel FETs. It has been demonstrated that if one device is biased in Class AB and other in deep Class AB, phase cancellation between the IMD3 components occur which leads to improvement in OIP3 with no effect on noise figure.

In Chapter 4, large-signal simulations are performed using parallel transistors. A detailed simulation methodology using commercial CAD software is presented. Three types of circuits are considered. In first, a single FET is used, in second two parallel FETs are used and in third four parallel FETs are used such that the total gate periphery is same in all the cases. Simulation results show that by varying the biases of the devices, IMD3 components can be made out of phase with each other leading to cancellation and improvement in linearity as discussed in the chapter.

In Chapter 5, the technique of improving the linearity of GaN amplifier is demonstrated through MMIC design for X-Band (8 – 10 GHz). Two circuits are designed (a) using a single 8 x125 um FET (b) using four parallel 2 x 125 um FETs for a total gate periphery of 1 mm. Simulation results show improvement in IMD3 by application of various combinations of bias currents.

Chapter 6 concludes the research work with a summary of contributions and future work.

Chapter 2

Linearity Enhancement for GaN HEMT Amplifiers Using g_m Linearization

2.1 Introduction and Motivation

This chapter discusses g_m linearization using common source FETs in parallel. Specifically, a GaN HEMT is divided into several sub-cells in parallel with drain bias voltages kept the same for all the cells. The gate bias voltages are adjusted independently of each other. Because each sub-cell has a different bias voltage, its g_m peaks at slightly different output power point. By adding (paralleling) the output of sub-cells, total g_m is kept linear over the range of output powers resulting in lower intermodulation products. This g_m helps in minimizing the magnitude of g_m'' as discussed in further sections. Previously, this technique has been applied to silicon devices, and improvement up to 6 dB was achieved in IMD3 within a small range of gate bias values at lower power levels [31].

2.2 Linearity Discussion

The Taylor series expansion for the drain current for the common source transistor is expressed as

$$i_{DS} = I_{dc} + g_m v_{gs} + \frac{g_m'}{2!} v_{gs}^{\ 2} + \frac{g_m''}{3!} v_{gs}^{\ 3} + ... \qquad (1)$$

where g_m' and g_m'' are the first and second order derivatives of i_{DS} w.r.t v_{gs} (Gate to Source Voltage) respectively. The co-efficient of v_{gs}^3 plays an important role in the third-order intermodulation distortion of an RF amplifier.

As discussed in chapter 1, IMD3 can be expressed as

$$IMD3 = \frac{3}{4}\frac{g_m''}{g_m}v_{gs}^2 \tag{2}$$

From equation (2), it can be seen that g_m'' plays and important role in the non-linearity. If the magnitude of g_m'' can be minimized over the operating region, linearity performance should be improved.

Fig. 2-1 shows the measured DC-IV characteristics (blue) of a GaN HEMT size of 4 x 125 um; 0.5 mm at V_{ds} = 28 V and I_{ds} of 150 mA/mm (75 mA). The first derivative of i_{DS} w.r.t to V_{gs} is shown as the red dotted curve. Also, the second (g_m') and the third derivatives (g_m'') shown in light green color and magenta color respectively were also computed at an operating voltage of 28 V. The transistors are usually biased in the region of V_{gs} from -3 V to -2 V for the given semiconductor technology. This region is closer to the pinch-off. In this range, g_m'' has a negative characteristic. This negative characteristic of g_m'' exacerbates the non-linearity significantly. Hence, if the magnitude of g_m'' is reduced in the area of operation, the linearity increases. The aim of this experiment is to minimize g_m'' in the region of operation. One way to flatten g_m'' is to break the transistor into parallel subsections by independently biasing each transistor separately. This approach has been demonstrated previously in CMOS technology. In [31], it was proposed that the negative g_m'' of the gate transistor can be cancelled by the positive g_m'' of another auxiliary MOSFET which is biased at a smaller gate drive. The author assumes that since the auxiliary transistor is smaller than the main transistor and is biased below the threshold voltage, the proposed topology consumes no additional DC current. Through this method, it is shown that the IMD3 of the device is suppressed by 6 dB with similar gain, dc power consumption and fundamental output power. This work expands this approach to GaN devices.

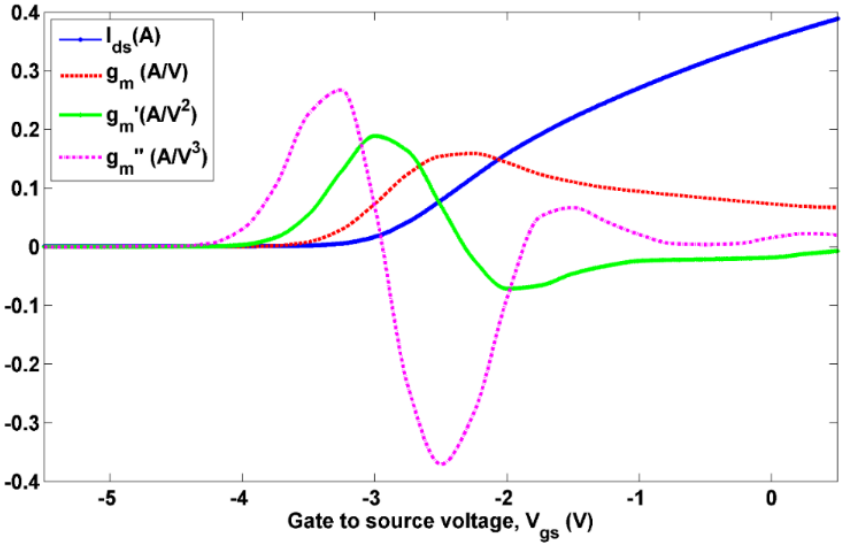


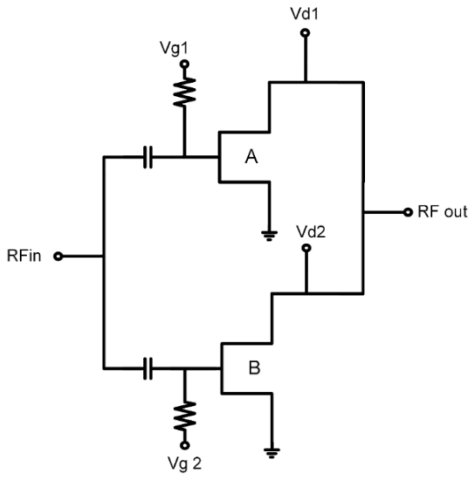
Fig. 2-1: Measured DC characteristics and computed small signal g_m, g_m' and g_m'' for 0.5 mm GaN HEMT at V_{ds} = 28 V and I_{ds} = 150 mA/mm.

2.3 Matlab Program

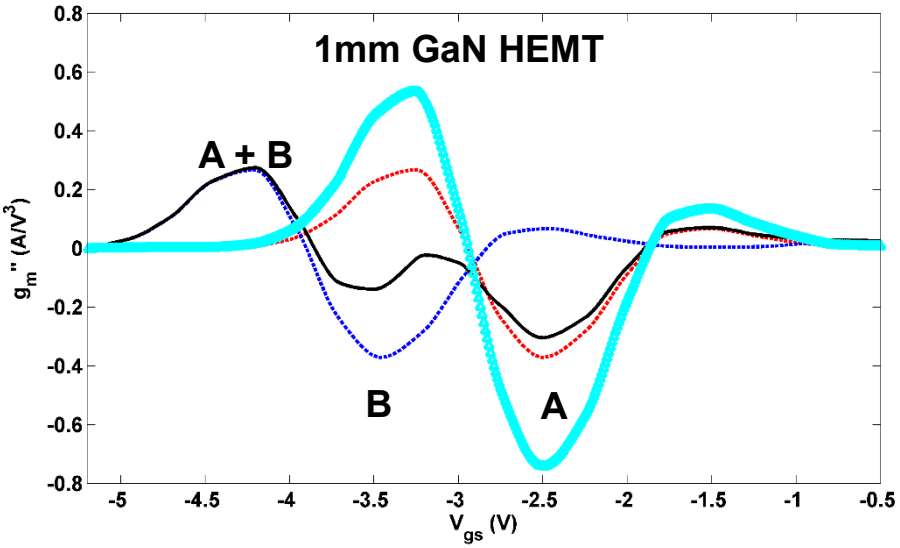
A program was written in MATLAB (Appendix B) to shift the $g_m''(V_{gs})$ curve of the second device / transistor w.r.t. first one and estimate the required gate bias values which minimizes the g_m'' in the target range. The RMS (Root Mean Square) value of the g_m'' was calculated in the range while applying different shifts in V_{gs}. A minimization function (M_f) was defined to compute g_m'' in the operation range of V_{gs} = -4.0 V to -1.0 V given by the following expression.

$$M_f = \sqrt{\frac{1}{N}\Sigma\left(g_{mi}''\right)^2} \tag{3}$$

where g_{mi}'' is the i^{th} value of computed g_m'' in the target range. An optimal solution was reached for the least value for the minimization function obtained in the target range. Fig. 2-2(a) shows the schematic of two parallel 0.5 mm devices A and B. Fig. 2-2(b) shows the plot of g_m'' of the transistor A and the shifted plot of g_m'' of the transistor B, and the combined sum of the two transistors (A + B) in black. This is compared to the combined g_m'' of 1 mm device without shifting (cyan).



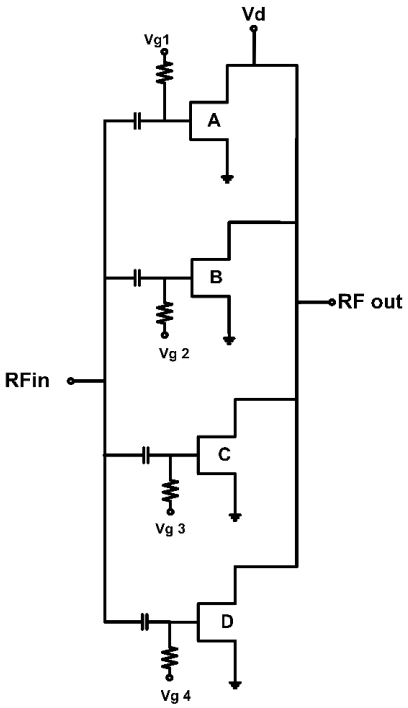
(a)



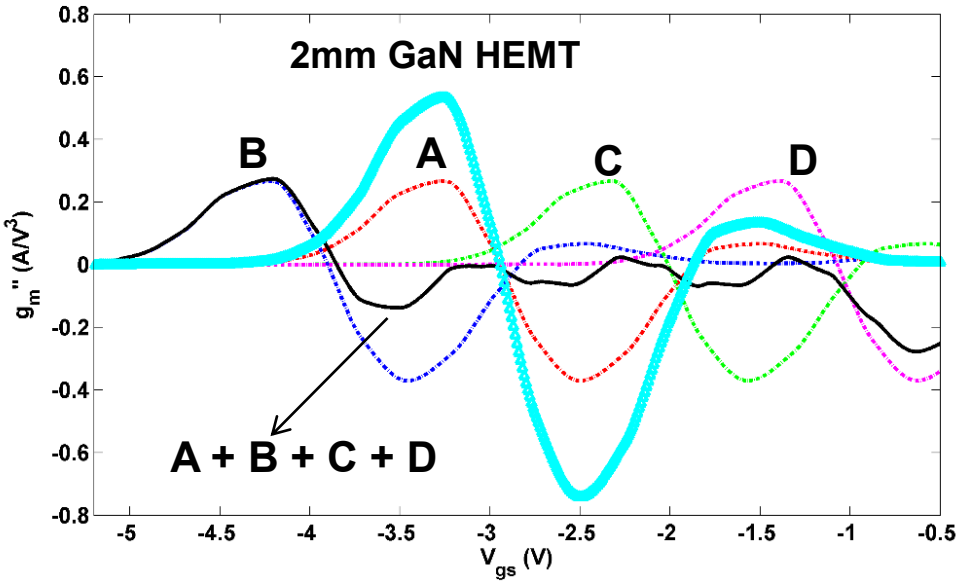
(b)

Fig. 2-2: (a) Schematic for two parallel devices with separate gate bias. (b) Plot of g_m" vs. V_{gs} for 1 mm device, two 0.5 mm devices individually biased at -1.5 V and -2.5 V and the combined g_m" of the two devices.

It is clear that g_m" of combined two parallel devices has lower magnitude over a broader range than a single 1 mm device. If V_{gs1} = -2.5 V and V_{gs2} = -1.5 V, then the improvement in the minimization function was found to be 62%. A similar simulation analysis was performed with four devices in parallel. The schematic of four devices in parallel is shown in Fig. 2-3 (a) and Fig. 2-3 (b) shows the plot of g_m" of four devices with and without shifting.



(a)



(b)

Fig. 2-3: (a) Schematic for four parallel devices with separate gate bias. (b) Plot of g_m" vs. V_{gs} for four 0.5 mm devices in parallel. When the four gates are biased with different gate bias voltages, the g_m" is minimized (black) than g_m" of a single 2 mm device (cyan).

Table 2-1 shows the value of minimization function computed with and without shift of the devices in parallel. It can be seen that by placing four devices in parallel, the percentage improvement in minimization function is 91% compared to 75% with three and 63% with two parallel devices. It was observed that beyond the four devices, the non-linearity starts to increase again. Hence, this simulation was limited to four devices only.

Table 2-1: Error values computed by bias shifting and percentage improvement.

# of devices	M_f **w/o shift**	M_f **with shift**	V_{gs} **Value of device**	**Percentage Improvement**
1	0.187	N/A	-2.5 V	N/A
2	0.374	0.1396	-1.54 V	62.72%
3	0.5609	0.1356	-3.43 V	75.82%
4	0.7479	0.0628	-4.37 V	91.60%

2.4 Amplifier Prototype Design

For the experimental validation of the technique, a prototype hybrid amplifier using two parallel transistors was designed using AMCOM's 1.25 mm discrete devices (AM012WN-00-R). Discrete GaN transistors were wire bonded to the PCB board of 508 um thickness Rogers 4350 substrate. The prototype circuit was designed over the frequency range of 0.8-1.0 GHz. The schematic diagram of the amplifier design is as shown below in Fig. 2-4.

Fig. 2-5 shows the photograph of the assembled prototype amplifier circuit. The comparison of the performance of the circuit measured vs. simulated is as shown below in Fig. 2-6. The amplifier has a saturated output power of 39 dBm at Ids of 350 mA with PAE of about 40%.

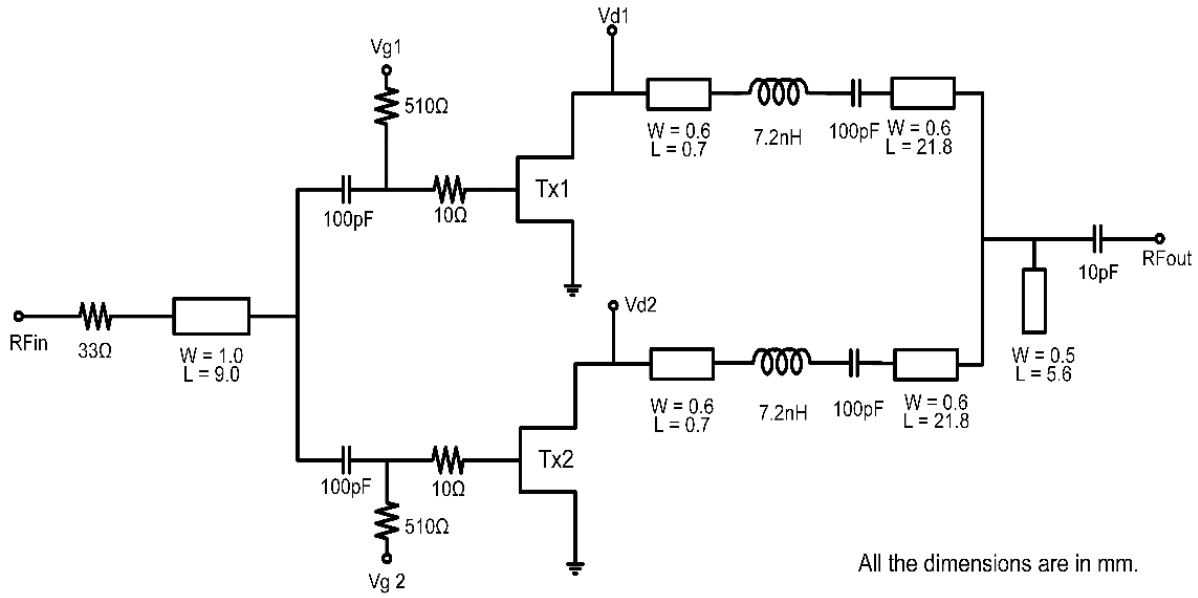


Fig. 2-4: Schematic of amplifier prototype with two parallel GaN transistors of size 1.25 mm each.

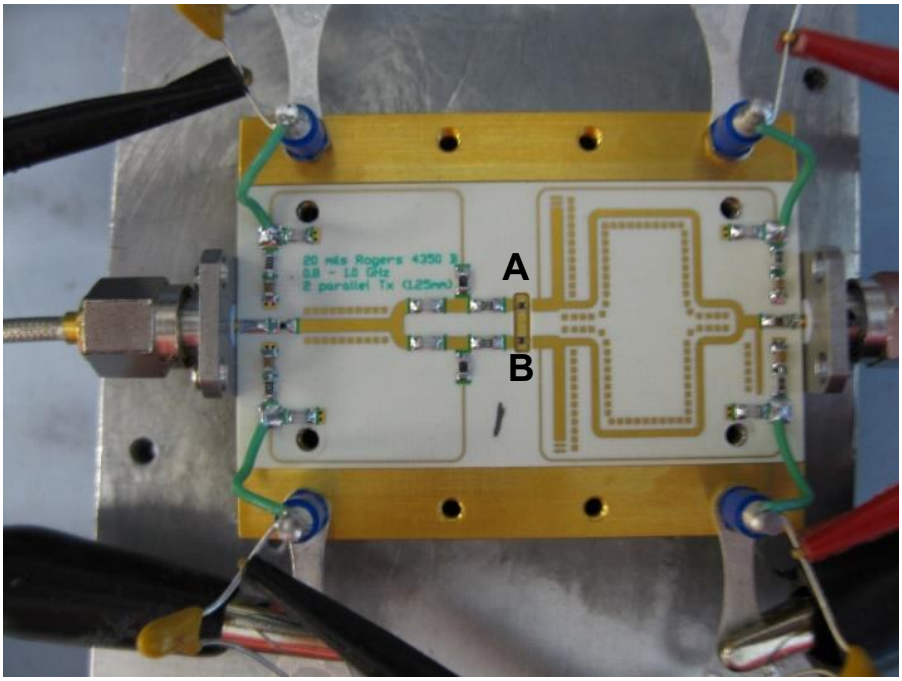


Fig. 2-5: Photograph of the assembled prototype 0.8-1.0 GHz amplifier circuit on Printed Circuit Board (PCB) mounted on a test carrier.

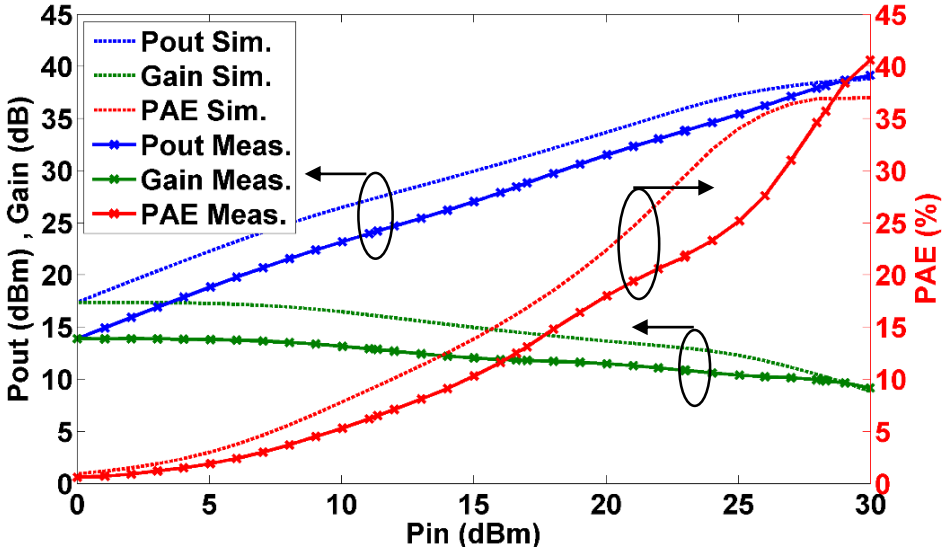


Fig. 2-6: Plot of the Pout, Gain and PAE of the amplifier circuit (simulated and measured).

2.5 Measurement Results

A two-tone signal with carrier spacing of 0.9 MHz was applied to the amplifier circuit at a center frequency of 900 MHz. The IMD3 (dBc) vs. Pout (dBm) was measured up to the P3 dB compression point. V_{gs} of the first transistor was kept constant to -2.5 V and V_{gs} of the second transistor was varied. IMD3 vs. Pout is as plotted in Fig. 2-7. The black curve acts as a baseline. For the baseline bias, both transistors were biased at the same V_{gs} bias (-2.5 V). V_{gs} of the second transistor is varied by $\pm$ 1V. If the second device is biased at the V_{gs2} = -2.0V, then the IMD3 improves by up to 4 dBc up to Pout of 30 dBm. If transistor 2 is biased at V_{gs} = -3.0V, the IMD3 improves by 2 dBc for the higher output power level. The same experiment was repeated by varying the bias of the second transistor from -3.5 V (pinch off) to -1.5 V.

Fig. 2-8 compares the PAE (%) with Pout (dBm) for different V_{gs2} bias values and Fig. 2-9 compares PAE (%) with IMD3 (dBm) for different biases. The amplifier can be linearized at different power levels by tuning the bias of the second transistor (V_{gs2}). For moderate output power levels and V_{gs2} = -1.5 V, IMD3 can be decreased by 4 dBc with loss in PAE about 1.5%. For output power above 30 dBm and V_{gs2} = -3.0 V, IMD3 decreases by approximately 2 dBc with an increase in PAE by 5%. Table 2-2 summarizes and compares IMD3 improvement and PAE change for the different V_{gs2} values.

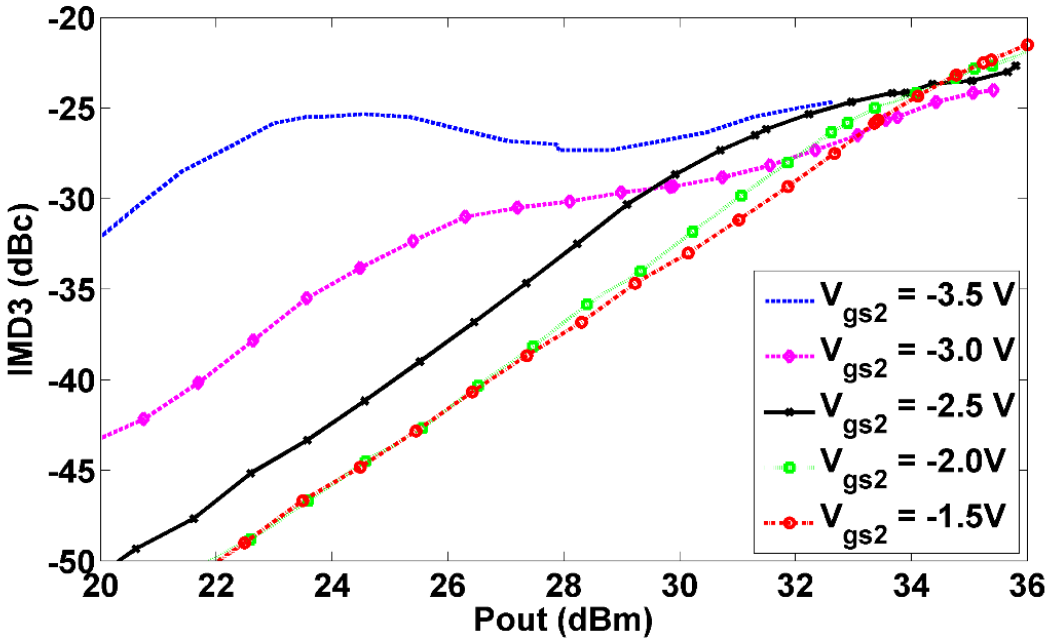


Fig. 2-7: Plot of IMD3 vs. Pout for different values of V_{gs2} bias.

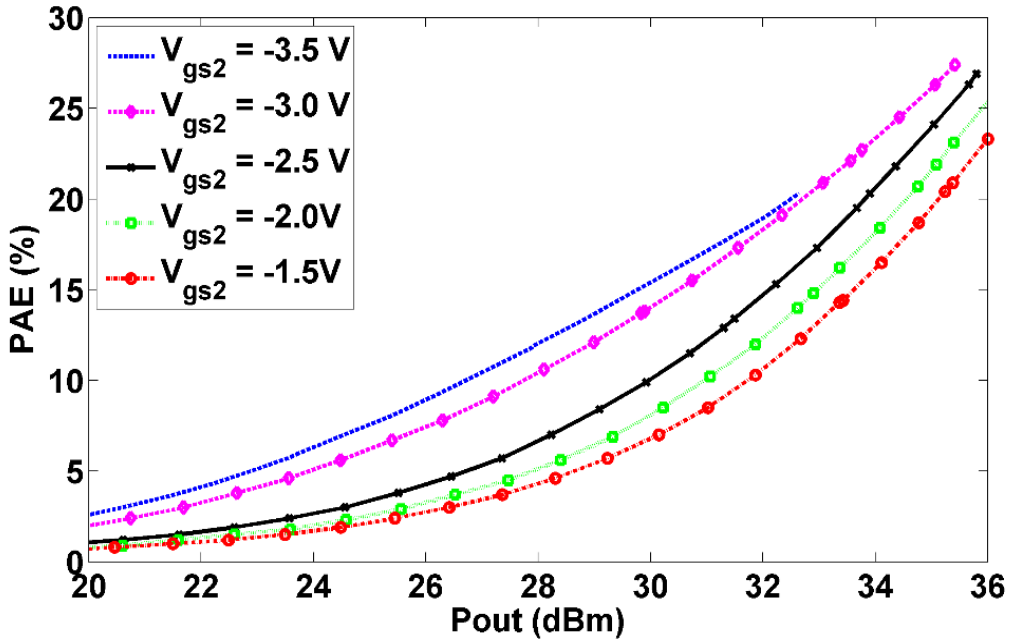


Fig. 2-8: Plot of PAE vs. Pout for different values of V_{gs2} bias.

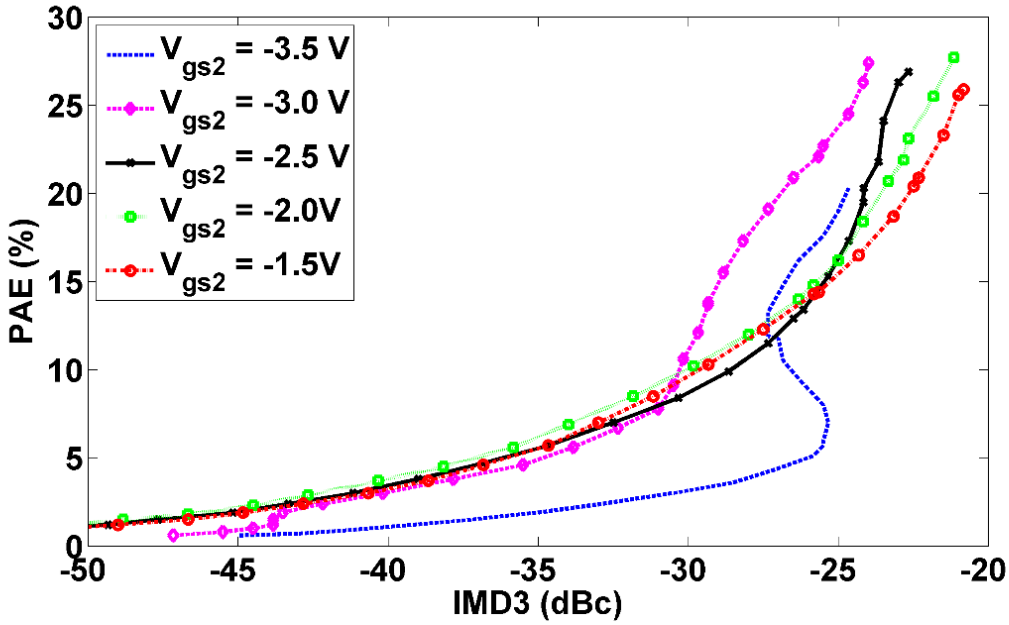


Fig. 2-9: Plot of PAE vs. IMD3 for different values of V_{gs2} bias.

Table 2-2: Comparison of IMD3 and PAE for different V_{gs} values.

Gate Bias of 2nd Transistor (V_{gs2})	**Pout range**	**IMD3 improvement**	**PAE change**
-3.5 V	N/A	None	None
-3.0 V	30 – 34 dBm	2 dBc	5%
-2.5 V	Baseline	--	--
-2.0 V	18 - 31 dBm	~ 3.5 dBc	-1.5%
-1.5 V	20 - 32 dBm	~ 3.5 to 4.3 dBc	-1.5 to -2%

2.6 Summary

This chapter demonstrates a method of improving linearity of amplifier based on GaN devices by applying different gate bias voltages. For moderate output power levels and V_{gs} bias of the second transistor to be -1.5 V, IMD3 is decreased by 4 dBc with loss in PAE compared to the baseline case. For higher output power level and V_{gs2} bias = -3.0 V, the IMD3, and PAE are improved by 2 dBc and 5% respectively. This technique is simple and widely applicable in RF transmitter systems.

Chapter 3

S-Band GaN LNA with OIP3>50 dBm using Parallel Independently Biased Gates

3.1 Introduction and Motivation

Fig. 3-1 shows the generic receiver schematic diagram. After the antenna, there is an LNA circuit followed by filter and mixer, after which, the circuit is sent for processing. If the LNA circuit is made using GaN technology, the limiter circuitry is eliminated. Higher bandgap for Gallium Nitride (GaN) devices makes it capable of withstanding higher input power [34], [35].

Fig. 3-2 shows the plot of minimum noise figure vs. frequency for various technologies [36]. GaN devices have similar noise figures compared to Gallium Arsenide (GaAs), Silicon (Si), Silicon Germanium (SiGe), etc. LNA linearity is a challenge for radar, satellite systems, base stations, etc [37], [38]. The objective of this work is to develop a high linearity GaN LNA (Low Noise Amplifier) for microwave frequencies. This chapter presents a linearized GaN LNA with high Third-order Intercept Point (OIP3). The primary approach is to divide the transistor into multiple smaller parallel gates and bias them individually. By varying the bias of each of the transistors independently, the linearity can be improved. In this chapter, this technique is applied to GaN LNA, and improvement is seen at lower and higher output power levels with similar noise figures. To the best of authors' knowledge, this is the first demonstration of linearity improvement using this technique for GaN LNAs.

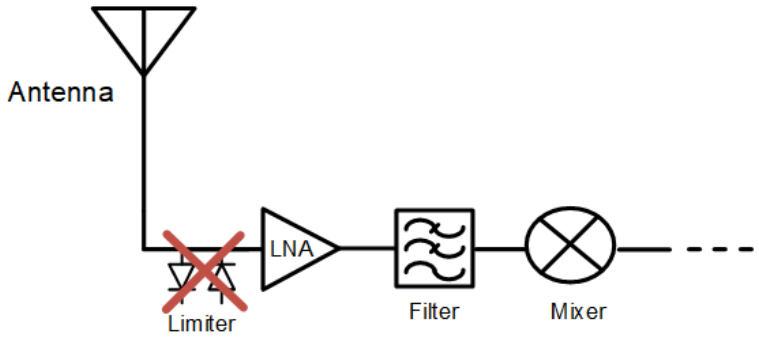


Fig. 3-1: Illustration of elimination of the limiter circuitry with GaN LNA in a generic receiver.

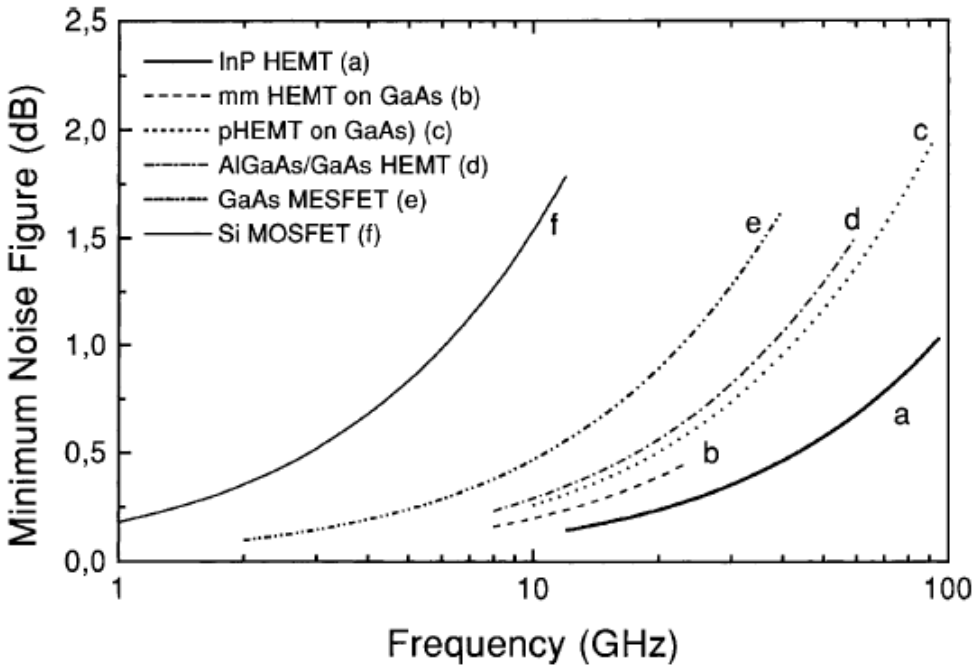


Fig. 3-2: Plot of minimum Noise Figure vs. frequency (GHz) for different technologies as illustrated in [36].

3.2 Linearization Approach

The basic approach is to divide a single FET into multiple gates and bias them independently. The linearity of the circuit is simulated by applying a two-tone signal to the amplifier around the frequency of interest. To obtain a circuit with better OIP3, the idea is to reduce the power level of third-order intermodulation products through phase cancellation. If one device is biased in Class AB mode and another in deep Class AB mode, then the intermods can be adjusted to be out of

phase with each other and get cancelled. This is in contrast to the g_m flattening approach presented in the previous chapter. As a prototype, an LNA circuit with two independently biased gates was investigated; for more than the two gates, it can be challenging to bias them individually leading to increased complexity in the design.

In the following discussion, the third-order intermodulation distortion current $\left(i_{ds}\,|_{2\omega_1-\omega_2,\ 2\omega_2-\omega_1}\right)$ generated at the frequencies $2\omega_1-\omega_2$, $2\omega_2-\omega_1$ will be referred to as IMD3 current. Fig. 3-3(a) shows a FET of width w with appropriately designed input and output matching networks. In Fig. 3-3(b), the FET is divided into two FETs of individual width w/2 (total width = w). In both the figures, IMN refers to the Input Matching Network and OMN to Output Matching Network.

If same bias current is applied to two parallel FETs (Case1), then the phase of the IMD3 current of one FET is same as the phase of IMD3 current of other FET (Fig. 3-3(b)). However, if one FET is biased in Class AB and another FET is biased in deep Class AB mode (Case2), then the phase of the IMD3 current of second FET could be adjusted to be out of phase with the first one. This can lead to cancellation of IMD3 current and improvement of Carrier to third-order Intermodulation ratio (C/I3), which leads to the improvement of OIP3.

As proof of this concept, two amplifier circuits were designed in AWR Microwave Office software using a fitted non-linear foundry model. The input and output matching networks in the two cases were kept similar. In the simulation, the two FETs were biased at the same bias current 40 mA/mm (100 mA for 2.5 mm total width, 50 mA each) and then a gradient bias was applied, i.e., one was biased at 20 mA/mm (25 mA for 1.25 mm, deep Class AB) and the other was biased at 60 mA/mm (75 mA for 1.25 mm, Class AB). The total bias current in both cases is 100 mA. The magnitude (Fig. 3-4) and phase (Fig. 3-5) of IMD3 current w.r.t input power were plotted. The red dashed curves show the magnitude and phase of IMD3 current of a single FET with 40 mA/mm. The blue and green curve shows the plot with 20 mA/mm and 60 mA/mm bias, respectively. The yellow curve shows the summation of IMD3 currents at the output power level when FETs are biased at 20 mA/mm and 60 mA/mm respectively (20_60), the black dashed curve shows summation when the FETs are biased with the same current, i.e., 40 mA/mm (40_40).

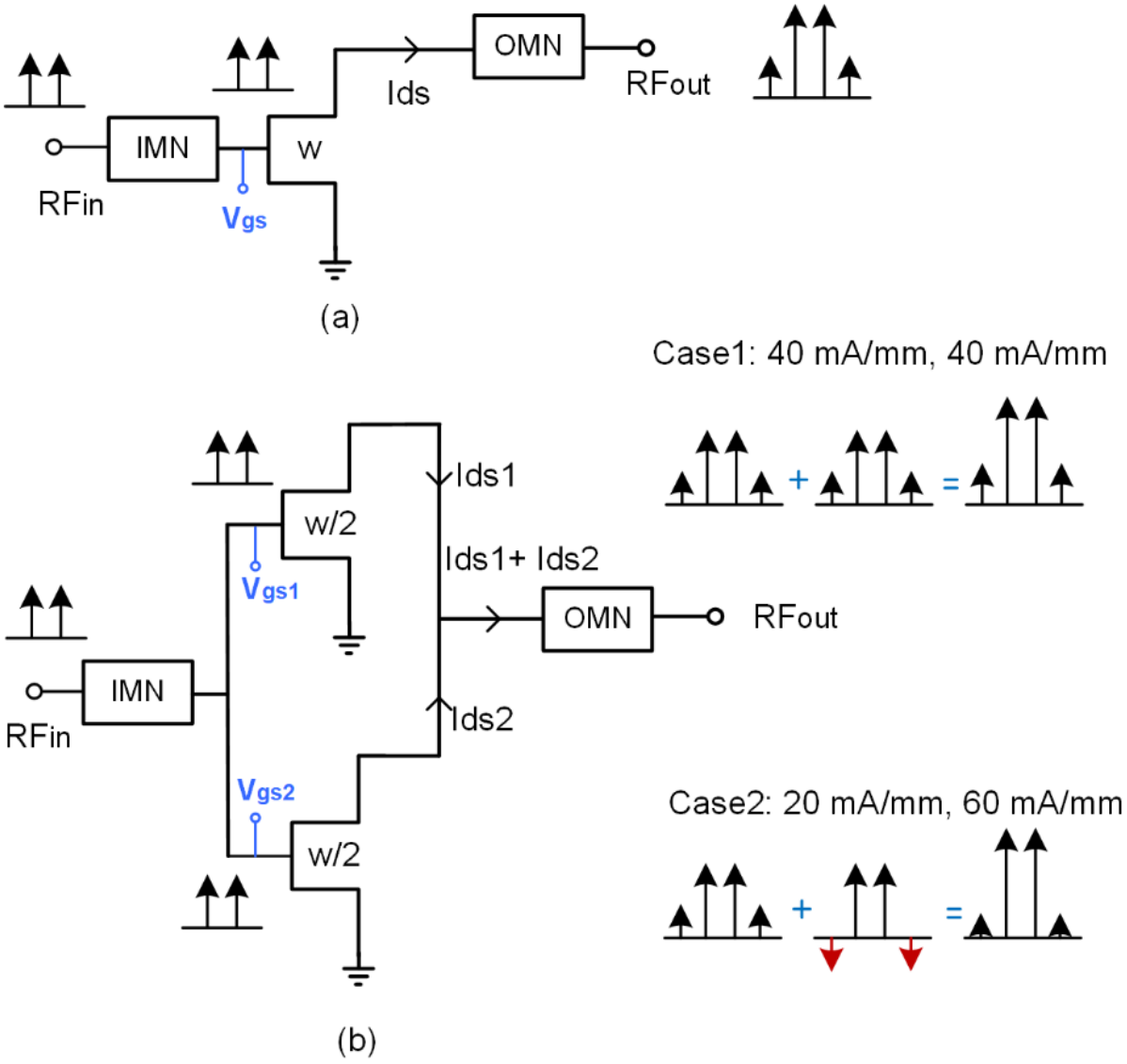


Fig. 3-3: Concept of dividing a single FET (w) into two parallel FETs (w/2). (a) Single FET of width w and its IMD products. (b) Two parallel FETs of width w/2 and intermodulation products for two cases. Case1: after biasing the two parallel FETs with the same bias current, Case2: after biasing two parallel FETs with different bias current.

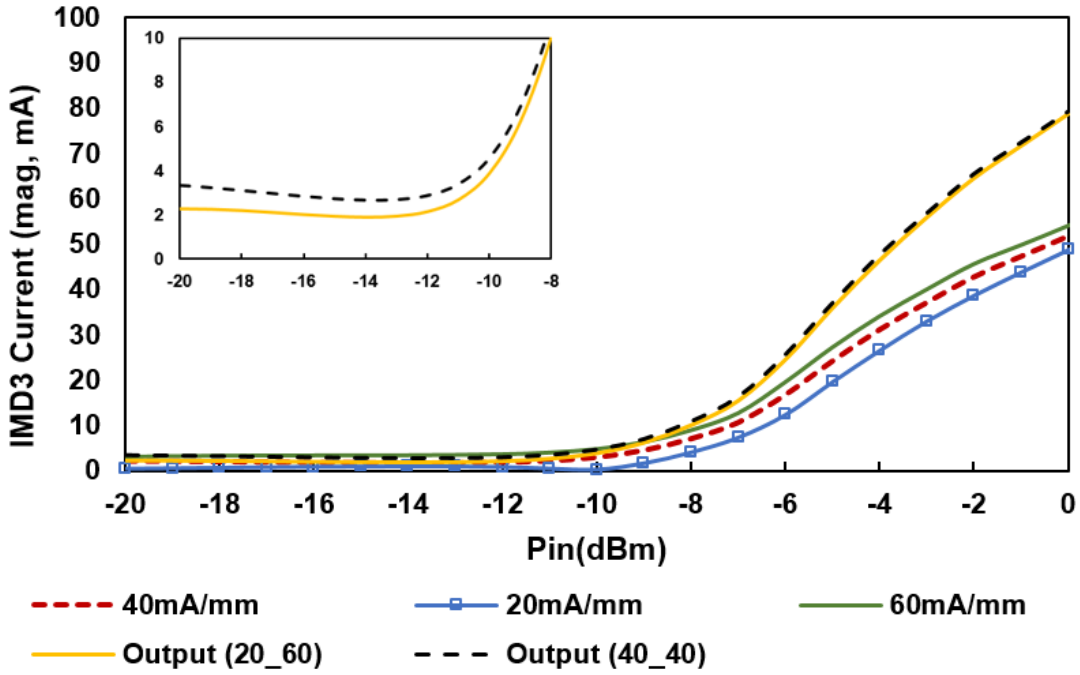


Fig. 3-4: Plot of the simulated magnitude of IMD3 current (mA) w.r.t Pin (dBm) with individual bias currents and summation at the output (subplot: zoomed-in curve IMD3 current vs. Pin from -20 dBm to -8 dBm).

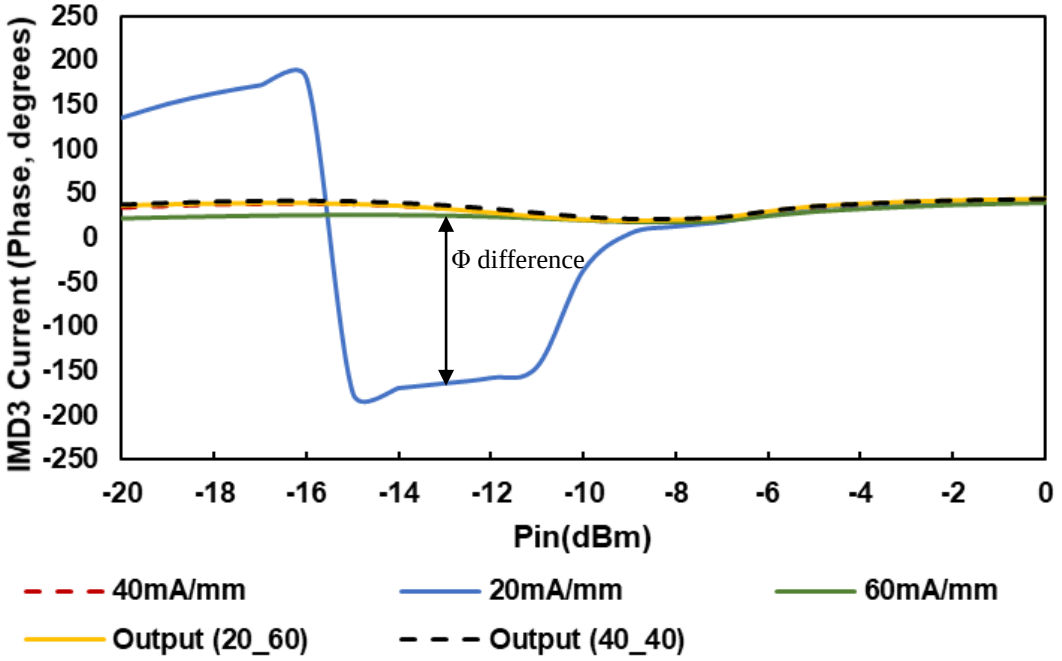


Fig. 3-5: Plot of simulated phase of the IMD3 current (degrees) w.r.t Pin (dBm). The blue and green curves are out of phase of each other until Pin = -9 dBm.

In Fig. 3-5, it can be seen that when the two FETs are biased with the same current, the IMD3 current has the same phase (red curve). However, when the parallel devices are biased differently, the output IMD3 current of each FET is at a different phase (blue and green) in a particular range of Pin (in this case, the currents are out of phase from Pin = -20 dBm to Pin = -9 dBm, after which they are in-phase with each other).

When combined, these currents can cancel each other and, thereby improve the OIP3 performance. It can be seen from the zoomed-in curve in Fig. 3-4 that at lower power levels (Pin) the net output IMD3 current is lower when the FETs are combined with different bias (yellow, 20_60) compared to when FETs are biased with same bias (dashed black, 40_40). Meanwhile, varying the bias of parallel FETs in the third stage with the same overall current has minimal effect on the noise figure and output power.

3.3 Circuit Design and Simulation

In order to obtain an optimum match for the noise figure, on-wafer source pull for a 0.5 mm GaN HEMT chip was done using the Focus Microwave tuners. Fig. 3-6 shows the plot of optimum Noise Figure, Gain and Noise Figure at 50 ohm impedance (NF50) vs. frequency for a 0.5 mm GaN FET. Fig. 3-7 shows the plot of optimum source impedance on the smith chart from source pull measurement for minimum noise figure. The optimum impedance was computed for the packaged device (red) by adding package parasitics in AWR.

Two prototype amplifiers were designed in the frequency range of 2-4 GHz using AMCOM's discrete GaN packaged transistors. The amplifier consists of three stages; the first stage is a FET of gate width 0.5 mm (W_1) followed by the second stage of 1.25 mm (W_2) and third stage FET (W_3) of 2.5 mm. In the second circuit (Ckt2), the third stage was divided into two parts of 1.25 mm each ($W_3/2$, total gate periphery = 2.5 mm). The PCB was fabricated using 254 µm thick Rogers 4350 substrate material.

The schematic diagram of the two amplifiers and zoomed-in layout plot is shown in Fig. 3-8. The circuits were made as similar to each other as possible. The input matching was designed according to optimum impedance for the noise. The input and the inter-stage matching circuits were kept the same for each design.

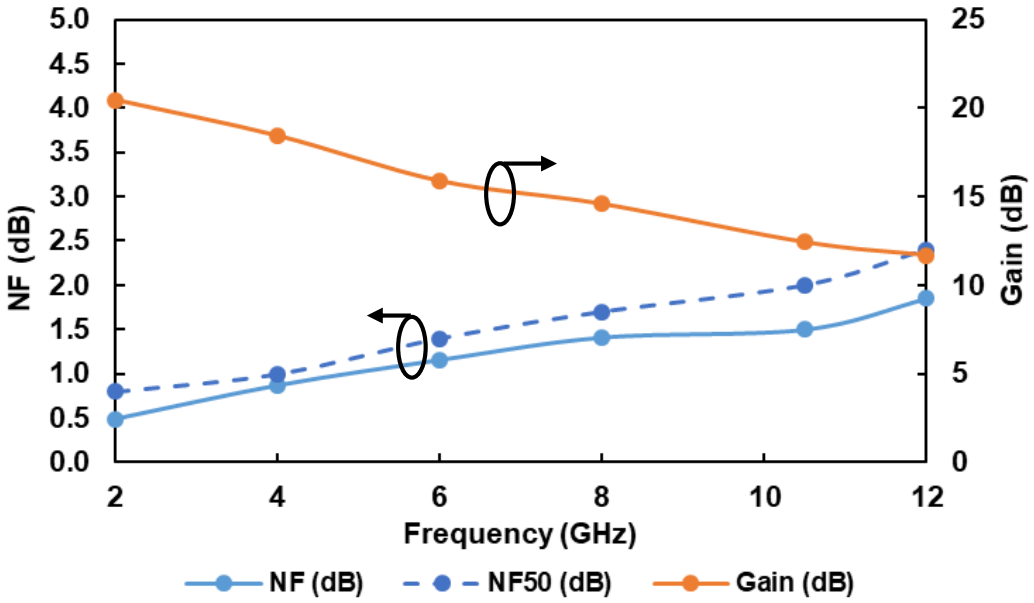


Fig. 3-6: Plot of optimum Noise Figure (NF), Gain (dB) and Noise Figure at 50 ohm impedance (NF50) vs. frequency for a 0.5 mm GaN FET.

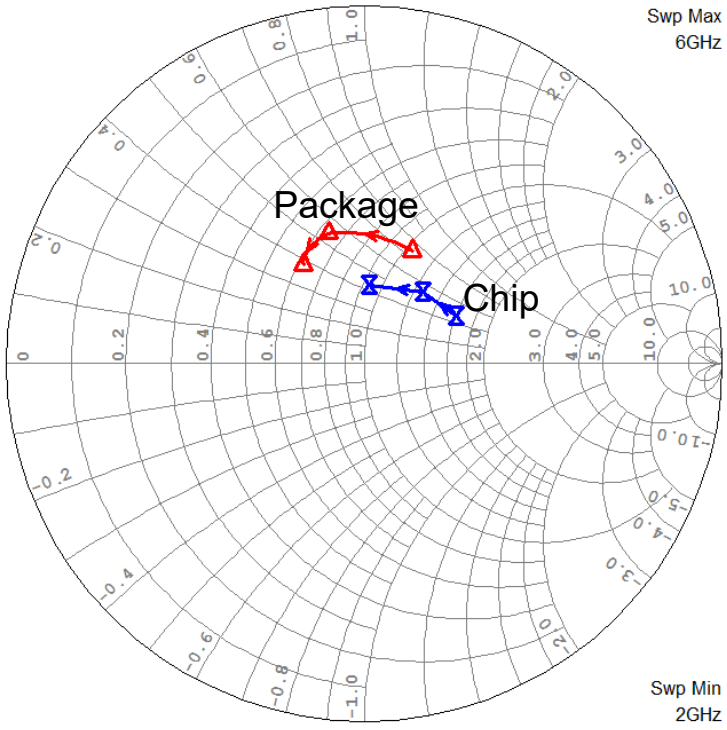
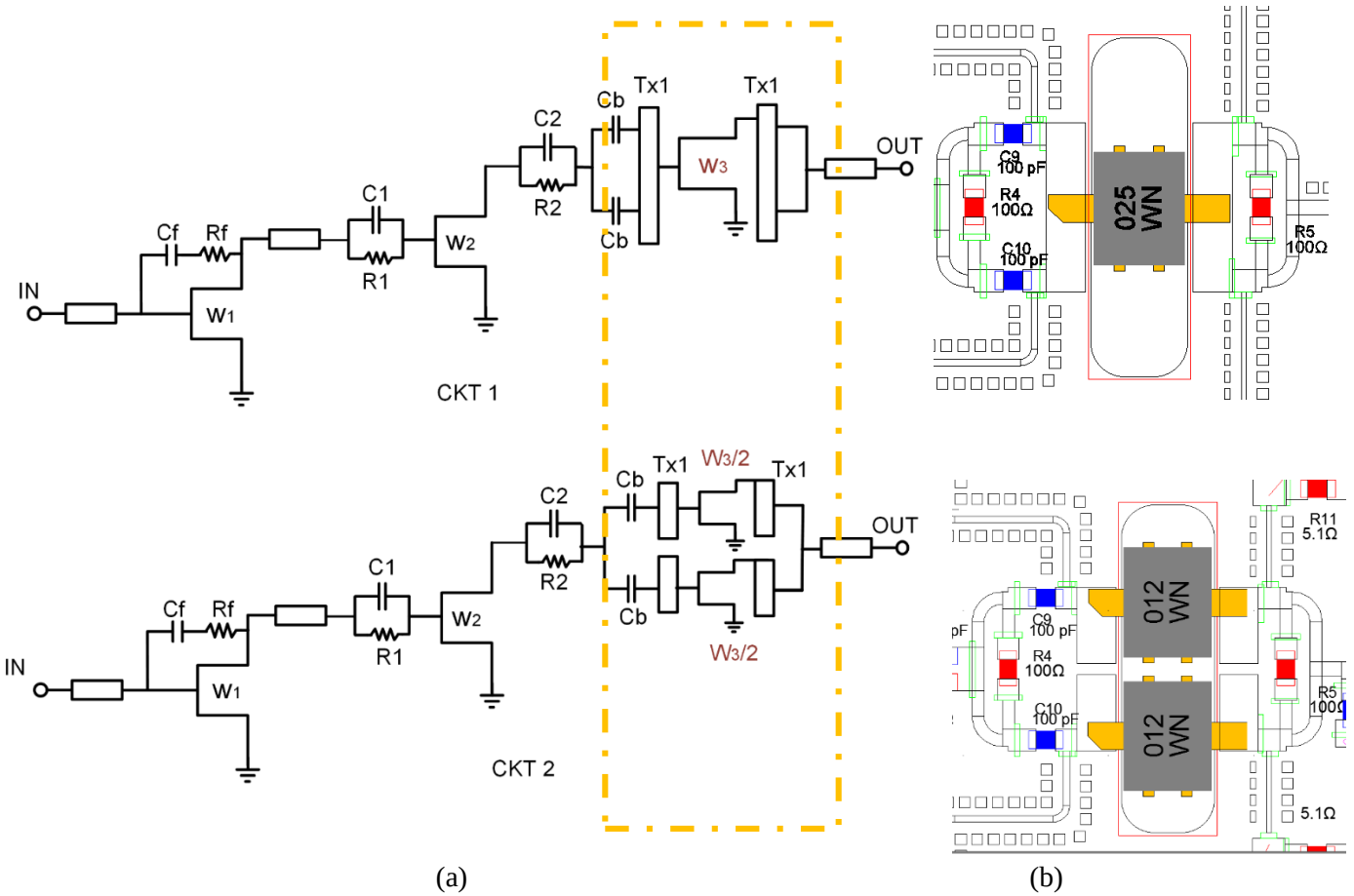


Fig. 3-7: Smith chart plot for the optimum source load for minimum noise figure for both chip and package for a 0.5 mm GaN FET.



(a) (b)

Fig. 3-8: (a) Schematic of the two amplifier circuits (Ckt 1) and (Ckt 2), (b) Zoomed-in layout of the third stage.

For the output stage, the circuits were designed with a transmission line (Tx1) of width = 1778 µm as shown in Fig. 3-8. The transmission line acts as a virtual open because of symmetry. For Ckt2, using two parallel FETs, this line was split into two parts to accommodate separate bias for two parallel FETs (Fig. 3-8(a)). Blocking capacitors (Cb = 100 pF) were used to keep the bias of the two FETs separate from each other. The output stage of Ckt2 with two parallel FETs (W3/2), was tuned slightly to include the effect of the additional package. The first stage was designed to have a high gain (13 dB approx.) so that the effect of the second and the third stage on the noise figure of the total amplifier was minimized.

According to the Friis Formula, noise factor of the cascaded stages in an amplifier is given by

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots\ldots \quad (1)$$

where F_i and G_i is the noise factor and available power gain respectively of the ith stage [39].

Noise Figure of the amplifier circuit is the logarithm of the noise factor expressed in decibels.

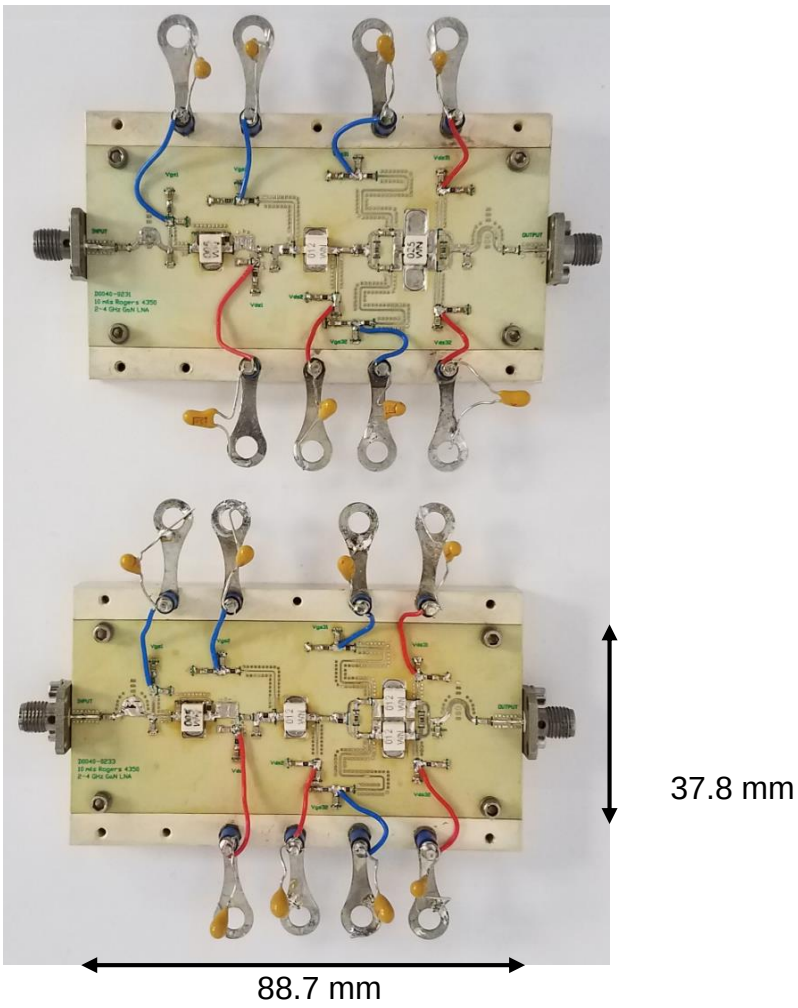


Fig. 3-9: Photograph of two fabricated S-Band GaN LNA circuits on a PCB mounted on a test carrier.

The LNA was stabilized with the RC feedback (Rf = 220 Ω, Cf = 0.3 pF). Resistors (R1 = 5 Ω, R2 = 22 Ω) in parallel with capacitors (C1 = 1 pF, C2 = 2.7 pF) were used in parallel for stabilization. They have minimal effect on the overall noise figure because they are at the intermediate stage and final output stage. Fig. 3-9 shows photograph of fabricated circuit. The size of the Printed Circuit Board (PCB) is 88.7 mm x 37.8 mm. It was mounted on a test carrier for measurement as shown in above figure.

3.4 Measurement Results

The saturated power (P5 dB) and noise figure performance comparison of the two amplifiers are shown in Fig. 3-10, and Fig. 3-11 respectively. The P5dB performance is about 35-38 dBm with PAE >15% at bias value of 28 V, Ids = 150 mA/mm and NF is in the range of 1.8-3.5 dB.

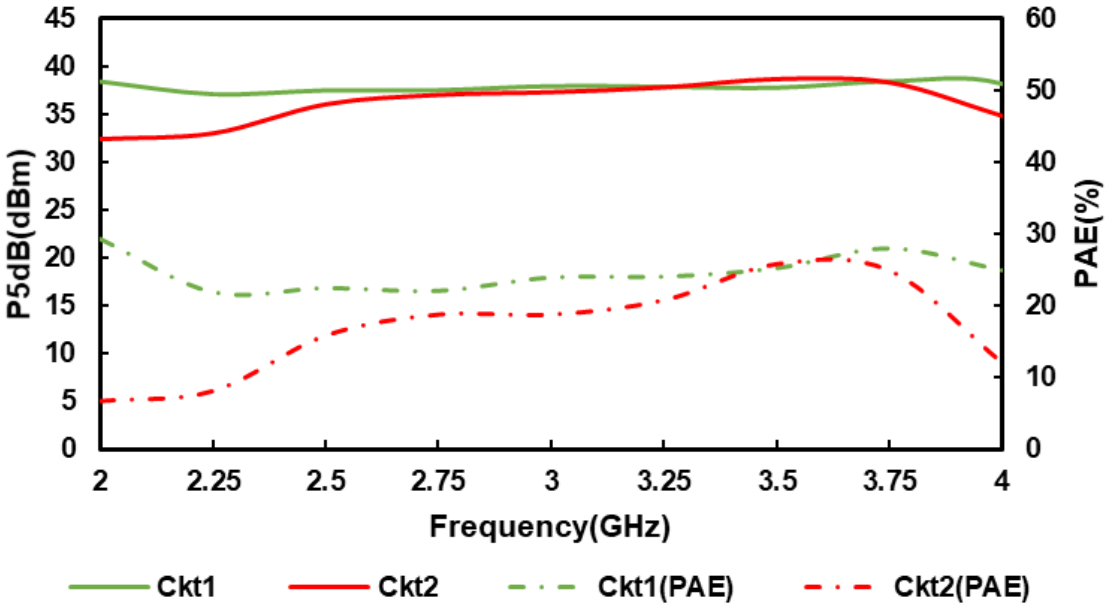


Fig. 3-10: Measured P5 dB and PAE vs. frequency over the complete band (2-4 GHz).

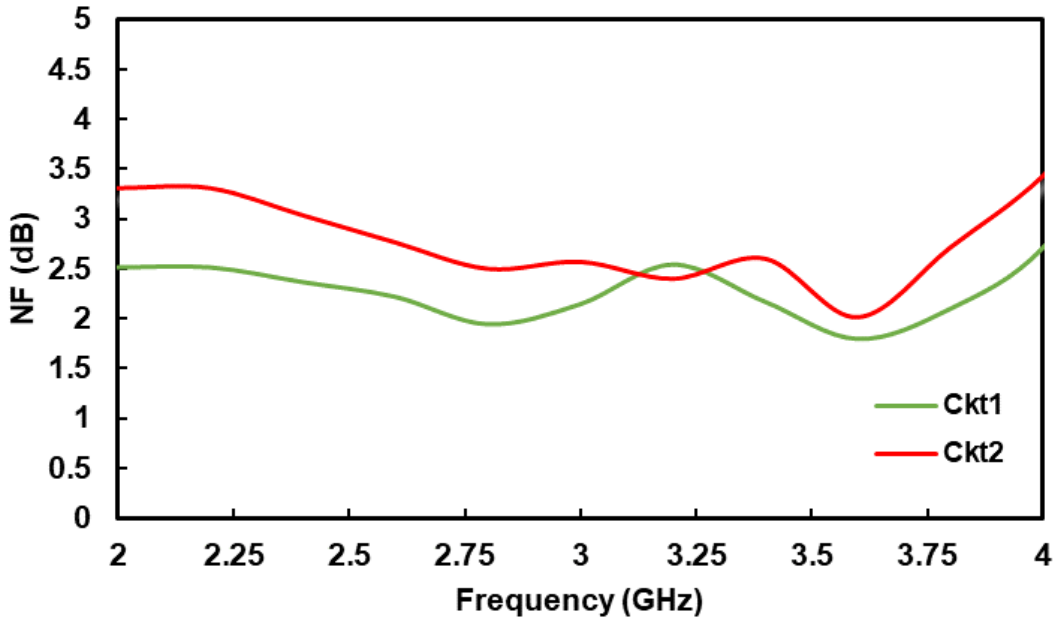


Fig. 3-11: Measured Noise Figure vs. frequency over the complete band (2-4 GHz).

The OIP3 of the two prototype circuits was measured from 2.75 - 3.75 GHz frequency range where both amplifier circuits have similar noise performance. A two-tone signal with a spacing of 5 MHz was applied around the center frequency. The OIP3 was measured from output power of 10 dBm until P2 dB compression point. It was found that if one device is biased in Class AB and the other is in deep Class AB, improvement in OIP3 is seen.

It is desirable to have high OIP3 in the circuits with lower power consumption - the lower the DC power, the lower the heating and higher PAE of the circuit. The linearity Figure Of Merit (FOM) is defined as

$$FOM = \frac{OIP3(W)}{P_{DC}(W)} \tag{2}$$

where P_{DC} is DC power consumption [32]. This quantity is dimensionless.

Fig. 3-12 shows the comparison of the OIP3 and FOM at center frequency of 3 GHz. The curves are plotted for the following two cases: Case1: when both the FETs in Ckt2 are biased at 40 mA/mm (40_40), Case2: when two FETs are biased at 20 mA/mm and 60 mA/mm (20_60) respectively which is deep Class AB mode and Class AB mode. From the figure, it can be seen that OIP3 performance improves from Pout = 10 dBm (linear region) to Pout = 29 dBm (saturation region) up to 8 dBm. The linearity FOM improves at lower and higher power levels.

The net improvement/increase in OIP3 by biasing the FETs differently (Case1 and Case2) at various frequencies is recorded in Table 3-1. By varying the bias values, the OIP3 increases up to 9.5. FOM was computed for the both the cases and the net comparison is shown in Table 3-2. The FOM is seen to increase up to 14.

Table 3-3 provides a performance comparison of this work with various SOA GaN LNAs[40]–[42]. Higher OIP3 is obtained by splitting a single large FET into two smaller FETs and biasing them separately. As compared with [40], the LNA demonstrated gives better FOM ($OIP3/P_{DC}$). The LNA demonstrated is hybrid design while others are implemented as MMIC. The splitting of a single device in two FETs helps in achieving higher OIP3 for the same amount of DC power consumption.

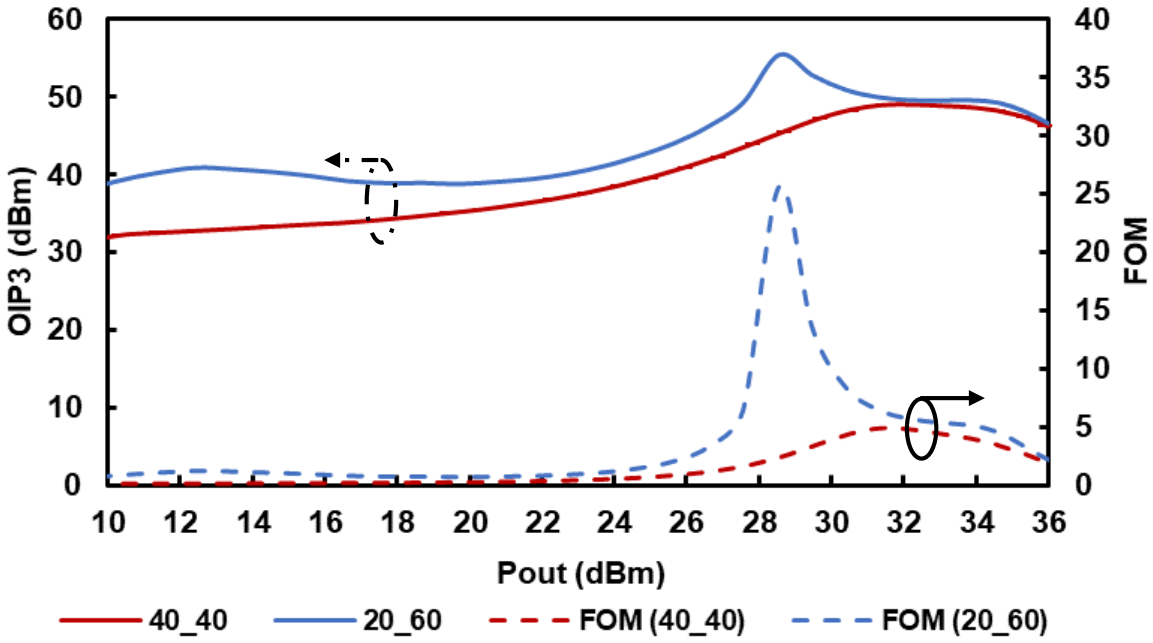


Fig. 3-12: OIP3 and FOM performance comparison between Ckt1 and Ckt2 at 3 GHz frequency.

Table 3-1: Comparison of OIP3 performance for S-Band LNA for Case 1 and Case 2.

Freq (GHz)	@Pout = 15 dBm			@Pout = 33 dBm		
	Case1 OIP3 (dBm)	Case2 OIP3 (dBm)	OIP3 Increase (dBm)	Case1 OIP3 (dBm)	Case2 OIP3 (dBm)	OIP3 Increase (dBm)
2.75	34.0	42.0	8.0	50.5	50.5	0.0
3.00	34.0	40.0	6.0	49.6	50.0	0.4
3.25	34.0	43.5	9.5	48.7	48.7	0.0
3.50	35.0	38.0	3.0	49.2	49.5	0.3
3.75	35.7	36.5	0.8	50.2	54.0	3.8

Table 3-2: Comparison of FOM performance of S-Band LNA for Case 1 and Case 2.

Freq (GHz)	@Pout = 15 dBm			@Pout = 33 dBm		
	Case1 FOM	**Case2 FOM**	**FOM Increase**	**Case1 FOM**	**Case2 FOM**	**FOM Increase**
2.75	0.25	1.50	1.25	5.9	6.8	0.9
3.00	0.27	1.20	0.90	4.4	5.3	0.9
3.25	0.37	2.20	1.80	4.5	4.5	0.0
3.50	0.35	0.65	0.30	3.8	5.5	1.7
3.75	0.46	0.46	0.00	6.0	20.0	14.0

Table 3-3: Summary of S Band GaN LNA performance and comparison with state-of-the-art LNAs.

Reference	[41]	[42]	[40]	This Work
Freq (GHz)	0.1 - 5.1	0.3 - 4	0.25 - 3	2 - 4
NF (dB)	1.6 - 2.5	1.6	2.5	1.8- 3.25
SS Gain(dB)	10 - 20	18	20	43
Pout (dBm)	33	25	38.5	37
OIP3(dBm)	43 (2 GHz)	-	51.9	48 - 54
DC Power	-	1 W	30 W	25W
FOM (OIP3/P_{DC})	-	-	5.2	4.5 - 20
Topology	dual gate / cascode	dual gate / cascode	cascode/ feedback	cascade / feedback
# of stages	2	2	2	3
Device Size	-	8 x 400 um	2 x 500 um	2 x 1250 um
MMIC/ Hybrid	MMIC	MMIC	MMIC	Hybrid

3.5 Conclusion

Hybrid S-Band GaN LNA circuits were designed to demonstrate linearization through biasing independent parallel gates at the output stage of the amplifier. If the two FETs are individually biased such that one is Class AB and the other is biased in deep Class AB, improvement in linearity is seen in both linear region and saturation region. This can be attributed to the partial phase cancellation of the third-order IMD currents generated by the two FETs. Through this method, the OIP3 performance was improved up to 9.5 dBm, and linearity FOM improved by up to 14. The current work is a hybrid design which has an inherent advantage of tuning it to the desired frequency compared to an MMIC. On the other hand, the proposed technique leads to difficulty in obtaining a flat gain and flat output power characteristics, but this should be able to be mitigated with a more integrated MMIC design.

Chapter 4

Computer Aided Design Methodology for Linearity Enhancement of GaN HEMT Amplifiers

4.1 Introduction

In this chapter, a design methodology for linearizing GaN HEMT amplifiers based on splitting a large FET into multiple parallel FETs with same total gate periphery and by biasing them individually is presented. By varying the biases, the magnitude and the phase of the IMD3 components at the output of FET changes. A detailed simulation methodology using commercial microwave CAD software is shown. The primary approach is to divide a single device into sub-cells and bias each cell individually. With the change of the gate bias voltage (V_{gs}), the phase of the third-order intermodulation (IMD3) current changes, which can be leveraged to provide cancellation at the combined FET outputs. This results in an enhancement of linearity performance. This method of IMD3 cancellation has been used for cascaded amplifiers [43] and for feedforward amplifiers [44], [45], but it has not been previously explored for parallel FET circuits.

The proposed approach has the following advantages:

1. Simplicity of the design technique, only adjustment in the bias voltages of the parallel FETs is required.
2. Low cost of implementation as compared to other techniques. No additional circuity is needed for linearity improvement [44]–[46].
3. As the gate width of the combined parallel FETs is same as one single FET, the total circuit area occupied is similar in both the cases, i.e., when a single FET is used compared to when multiple parallel FETs are used.
4. The magnitude and the phase of the IMD3 currents at the output of each FET and the output of the circuit can be simulated using power sampler elements in commercial harmonic balance simulations. The optimum value of bias voltages of each FET for which the cancellation of IMD3 components will occur can be computed.

To demonstrate the proposed methodology, three prototype circuits were designed in AWR microwave software (a) using a single 5 mm FET (1 x 5 mm) (b) two parallel 2.5 mm FETs (2 x 2.5 mm) (c) four parallel 1.25 mm FETs (4 x 1.25 mm) for a total gate periphery of 5 mm. The circuits were designed in the frequency range from 0.8-1.0 GHz. Analysis was done for the various current levels and improvement is seen for many bias current levels. To the best of the authors' knowledge, this is the first demonstration of a computer-aided design methodology for linearity improvement of parallelized, independently biased GaN devices.

4.2 Linearization Approach

4.2.1 Analysis of Parallel FETs

The well-known Taylor series expansion of the output current from the N^{th} parallel FET of a non-linear amplifier circuit is given by

$$I_{oN} = a_{1N} I_{iN} + a_{2N} I_{iN}{}^2 + a_{3N} I_{iN}{}^3 + ... \quad (1)$$

where I_{oN} is the output current and I_{iN} is the input current of the N^{th} parallel FET .

In this analysis, it is assumed that Taylor series coefficients are complex quantities, given by:

$$a_{1N} = A_{1N} e^{j\theta_{1N}}, a_{2N} = A_{2N} e^{j\theta_{2N}}, a_{2N} = A_{2N} e^{j\theta_{2N}} \quad (2)$$

The magnitude and phase of these quantities depends on the bias condition of each individual parallel FETs. On the application of two-tone excitation signal to the circuit, the input current I_{iN} through each of the parallel FET can be expressed as

$$I_{iN} = I_N\left(\cos\left(\omega_1 t + \phi_1\right) + \cos\left(\omega_2 t + \phi_2\right)\right) \tag{3}$$

where, the ϕ_1 and ϕ_2 are the phases of the two input signals at frequencies ω_1 and ω_2, respectively.

When the parallel FETs are biased with the same bias current, then, the current flowing through them is identical. However, when they are not biased in the same manner, then, the amplitude I_N will vary.

The total output current is the complex sum of output currents from each of the parallel FETs given by the following expression:

$$I_o = I_{o1} + I_{o2} + ...I_{oN} \tag{4}$$

On substituting the equation (2) and (3) in equation (1), as shown in Appendix C, output current N[th] parallel FET can be expressed as

$$\begin{aligned}
&I_{oN} = A_2 {I_N}^2 e^{j\theta_{2N}} + \frac{A_{1N} I_N}{2}\left(e^{j(\omega_1 t+\phi_1+\theta_{1N})} + e^{-j(\omega_1 t+\phi_1-\theta_{1N})} + e^{j(\omega_2 t+\phi_2+\theta_{1N})} + e^{-j(\omega_2 t+\phi_2-\theta_{1N})}\right) + \\
&\frac{9A_{3N}{I_N}^3}{8}\left(e^{j(\omega_1 t+\phi_1+\theta_{3N})} + e^{-j(\omega_1 t+\phi_1-\theta_{3N})} + e^{j(\omega_2 t+\phi_2+\theta_{3N})} + e^{-j(\omega_2 t+\phi_2-\theta_{3N})}\right) + \\
&\frac{A_{2N}{I_N}^2}{4}\left(\begin{array}{l} e^{j(2\omega_1 t+2\phi_1+\theta_{2N})} + e^{-j(2\omega_1 t+2\phi_1-\theta_{2N})} + e^{j(2\omega_2 t+2\phi_2+\theta_{2N})} + e^{-j(2\omega_2 t+2\phi_2-\theta_{2N})} + 2e^{-j(\omega_1 t-\omega_2 t+\phi_1-\phi_2-\theta_{2N})} + \\ 2e^{j(\omega_1 t-\omega_2 t+\phi_1-\phi_2+\theta_{2N})} + 2e^{j(\omega_1 t+\omega_2 t+\phi_1+\phi_2+\theta_{2N})} + 2e^{-j(\omega_1 t+\omega_2 t+\phi_1+\phi_2-\theta_{2N})} \end{array}\right) + \\
&\frac{A_3{I_N}^3}{8}\left(\begin{array}{l} e^{j(3\omega_1 t+3\phi_1+\theta_{3N})} + e^{-j(3\omega_1 t+3\phi_1-\theta_{3N})} + e^{j(3\omega_2 t+3\phi_2+\theta_{3N})} + e^{-j(3\omega_2 t+3\phi_2-\theta_{3N})} + \\ 3e^{j(2\omega_1 t+\omega_2 t+2\phi_1+\phi_2+\theta_{3N})} + 3e^{-j(2\omega_1 t+\omega_2 t+2\phi_1+\phi_2-\theta_{3N})} + 3e^{j(2\omega_1 t-\omega_2 t+2\phi_1-\phi_2+\theta_{3N})} + 3e^{-j(2\omega_1 t-\omega_2 t+2\phi_1-\phi_2-\theta_{3N})} + \\ 3e^{j(\omega_1 t-2\omega_2 t+\phi_1-2\phi_2+\theta_{3N})} + 3e^{-j(\omega_1 t-2\omega_2 t+\phi_1-2\phi_2-\theta_{3N})} + 3e^{j(\omega_1 t+2\omega_2 t+\phi_1+2\phi_2+\theta_{3N})} + 3e^{-j(\omega_1 t+2\omega_2 t+\phi_1+2\phi_2-\theta_{3N})} \end{array}\right)
\end{aligned} \tag{5}$$

where, the first-order (fundamental) terms are given by

$$\begin{aligned}
&\frac{A_{1N} I_N}{2}\left(e^{j(\omega_1 t+\phi_1+\theta_{1N})} + e^{-j(\omega_1 t+\phi_1-\theta_{1N})} + e^{j(\omega_2 t+\phi_2+\theta_{1N})} + e^{-j(\omega_2 t+\phi_2-\theta_{1N})}\right) + \\
&\frac{9A_3{I_N}^3}{8}\left(e^{j(\omega_1 t+\phi_1+\theta_{3N})} + e^{-j(\omega_1 t+\phi_1-\theta_{3N})} + e^{j(\omega_2 t+\phi_2+\theta_{3N})} + e^{-j(\omega_2 t+\phi_2-\theta_{3N})}\right)
\end{aligned} \tag{6}$$

and the IMD3 components at frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are given by

$$\frac{3A_{3N}{I_N}^3}{8}\begin{pmatrix} e^{j(2\omega_1 t-\omega_2 t+2\phi_1-\phi_2+\theta_{3N})}+e^{-j(2\omega_1 t-\omega_2 t+2\phi_1-\phi_2-\theta_{3N})}+ \\ e^{j(-\omega_1 t+2\omega_2 t-\phi_1+2\phi_2+\theta_{3N})}+e^{-j(-\omega_1 t+2\omega_2 t-\phi_1+2\phi_2+\theta_{3N})} \end{pmatrix} \quad (7)$$

The magnitude co-efficient given by $\frac{3A_{3N}{I_N}^3}{8}$ and the phase co-efficient given by θ_{3N} is dependent on the bias condition of each individual FET. The IMD3 components add at the output of the combiner in the amplifier circuit. Depending on the bias condition of each FET, the magnitude and phase of the IMD3 components generated by it can be varied. Hence, at the output these can be added or made to cancel out with each other with the variation of the bias. This is further explored in the following sections.

4.2.2 IMD3 Cancellation with Two Parallel FETs

Fig. 4-1 gives the illustration of phase cancellation using two parallel FETs in an amplifier circuit. The input and output large-signal currents are given by I_i and I_o respectively. With the application of two-tone input signal, both fundamental and IMD3 components are generated. The fundamental current component is shown in blue, and the IMD3 current component is shown in red in the form of phasor diagram at different stages of the circuit. The X-axis is the Real (Re) axis, and Y-axis is the Imaginary (Im) axis. IMN refers to the Input Matching Network, and OMN refers to the Output Matching Network.

In Fig. 4-1, the current gets phase-shifted from the input of the amplifier circuit to the input of the FETs due to the effect of the input matching network. For two parallel FETs circuit, there are two conditions: Case 1 is when both the FETs are biased at the same bias current, and case 2 is when they are biased at different bias currents. Depending on the bias condition of the FETs, the input current to the FETs varies. In the following discussion, the third-order intermodulation distortion currents will be generated at frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ will be referred to as IMD3 current. Each FET generates its own IMD3 current phase component which is given by θ_{3N} .

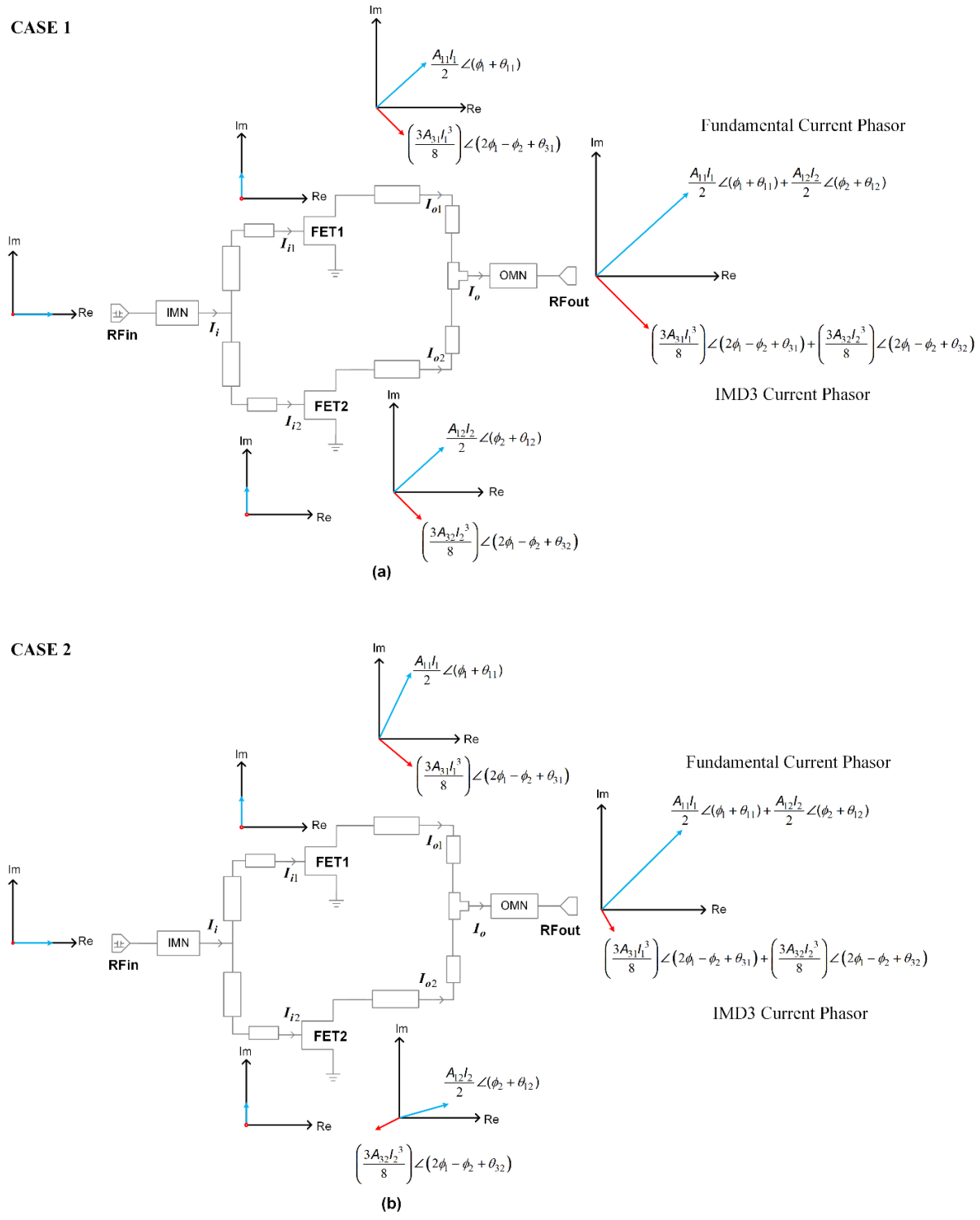


Fig. 4-1: Illustration of the phasor diagram of fundamental (blue) and IMD3 (red) current at various stages of two parallel FETs amplifier circuit. (a) Case 1: Both the FETs are biased with same bias current resulting in increase in magnitude of the IMD3 components at the output. (b) Case 2: Both the FETs are biased with different bias current. They generate different IMD3 components which could result in cancellation as depicted. Note: only one sideband is used for the purposes of illustration.

For the intermodulation products to decrease in magnitude, the phase of the IMD3 currents at frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ which are $2\phi_1 - \phi_2 \pm \theta_{3N}$ and $2\phi_2 - \phi_1 \pm \theta_{3N}$ respectively, must be made to cancel out each other. By varying the bias current of the individual FETs, the phase component of the second FET, θ_{32}, can be made out of phase with the first FET, θ_{31}. This is illustrated in Fig. 4-1.

For Case 1, the magnitude and the phase (θ_{31}) of IMD3 component generated by FET1 is same as the magnitude and phase (θ_{32}) of IMD3 component generated by FET2. At the output of the FET, the IMD3 and the fundamental output currents add in-phase i.e., $2\phi_1 + \theta_{11} + \theta_{12}$ for the fundamental and $4\phi_1 - 2\phi_2 + \theta_{31} + \theta_{32}$ for the IMD3 component, respectively, and increase in magnitude as shown in Fig. 4-1(a). Only one side band is used for the purposes of illustration for fundamental and IMD3 component occurring at frequencies $2\omega_1 - \omega_2$ and ω_1 , respectively.

However, for case 2, when both FETs are biased in such a way that FET2 generates out of phase IMD3 components compared to the IMD3 components from FET1, then, at the output the magnitude of the total IMD3 is reduced (Fig. 4-1(b)). Note that the IMD3 components are not 180 degree of phase with each other which leads to their partial cancellation. This phase cancellation of the IMD3 components leads to enhancement in linearity performance.

4.2.3 IMD3 Cancellation with Four Parallel FETs

For two parallel FETs circuit, it is difficult to vary the phase of the IMD3 current of the second FET to completely cancel the total IMD3 current. Therefore, the proposed technique is extended with each of the FETs further divided into two FETs of width (w/4), resulting in a total number of four FETs with same total gate periphery (w). For lower intermodulation components at the output, the IMD3 current of all the FETs, when vector summed together, must be made to cancel each other in-phase. Fig. 4-2 shows the schematic of four parallel FETs circuit with current flow.

The input current I_i is divided in two branches I_{i1} and I_{i2} which is further divided into I_{i11} , I_{i12} and I_{i21}, I_{i22}. The total output current is the complex sum of the current from each individual FET which is given as

$$I_o = I_{o1} + I_{o2} = I_{o11} + I_{o12} + I_{o21} + I_{o22} \tag{8}$$

For a given bias, each FET generates its own IMD3 current phase given by θ_{3N}. For lower intermodulation components, the IMD3 current of all the FETs, when vector summed together, must be made to cancel each other in-phase.

The derivation using four parallel FETs will not be considered here as the concept is similar, and it does not add much insight. More detail about the simulation methodology is discussed in Section 4.3 and with simulation results in Section 4.5.

Three cases can be considered: Case 1 is when all the FETs are biased with the same current, IMD3 components add in-phase and do not cancel out; Case 2a is when second FET and the fourth FET is biased in such a way to cancel out the intermod of the first and the third FET respectively; Case 2b is when second, third and fourth FETs are biased in a manner to cancel the intermod of the first FET. Case 2a and case 2b lead to the generation of out of phase IMD3 components, which when combined with in-phase, cancel at the output combiner, and the IMD3 current lowers, thereby improving the overall linearity of the amplifier. With the aid of a large-signal model as discussed in section 4.5, the FET biasing can ideally be selected in such a way that the phases of the IMD3 currents are made to cancel out the components at the output.

4.3 Simulation Methodology

Harmonic balance simulations were performed to compute the magnitude and phase of the fundamental currents and the intermodulation currents coming out of each of the FET in the circuit. A single 2.5 mm nonlinear foundry based model of FET was characterized with 50-ohm termination in the AWR microwave office. Harmonic Balance (HB) tuners were used with bias tee, as shown in Fig. 4-3 below. The bias (I_{ds}, V_{gs}) was varied from complete pinch off (0 mA/mm, -6 V) to full bias (200 mA/mm, -2.16 V). The magnitude and phase of the IMD3 current for FET was plotted for the different bias current values, as shown in Fig. 4-4(a) and Fig. 4-4(b), respectively. It can be seen from the figure that the phase of the IMD3 current varies drastically when the bias is varied from 0 mA/mm to 10 mA/mm. After that, it remains fairly constant.

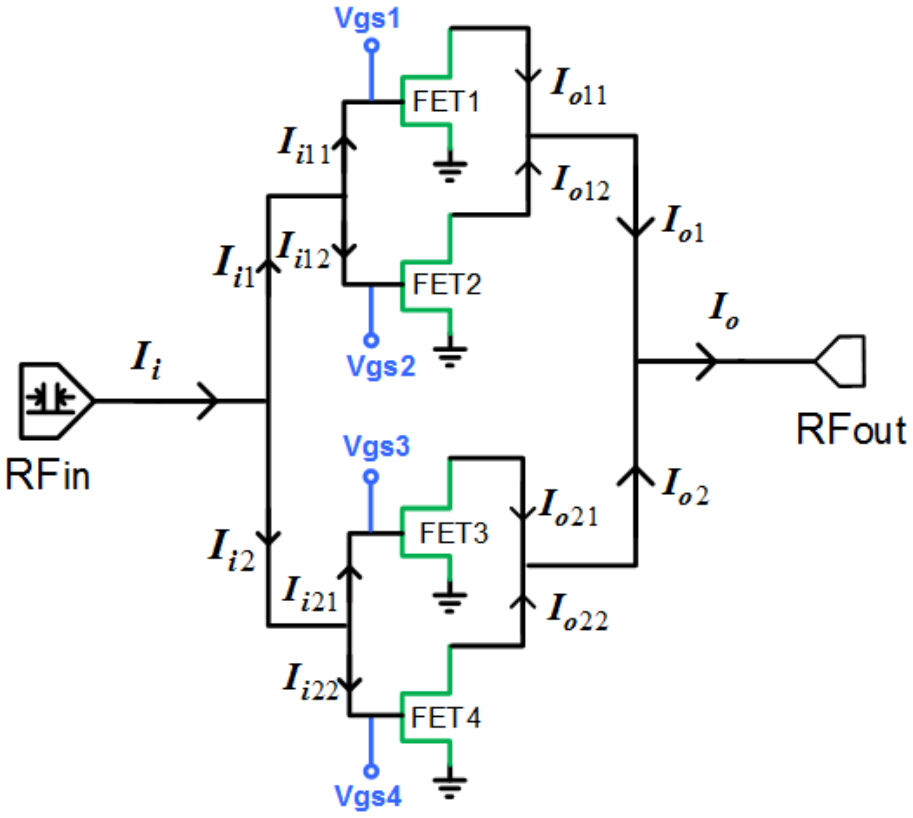


Fig. 4-2: Schematic of four parallel FETs circuit showing the direction of the current flow.

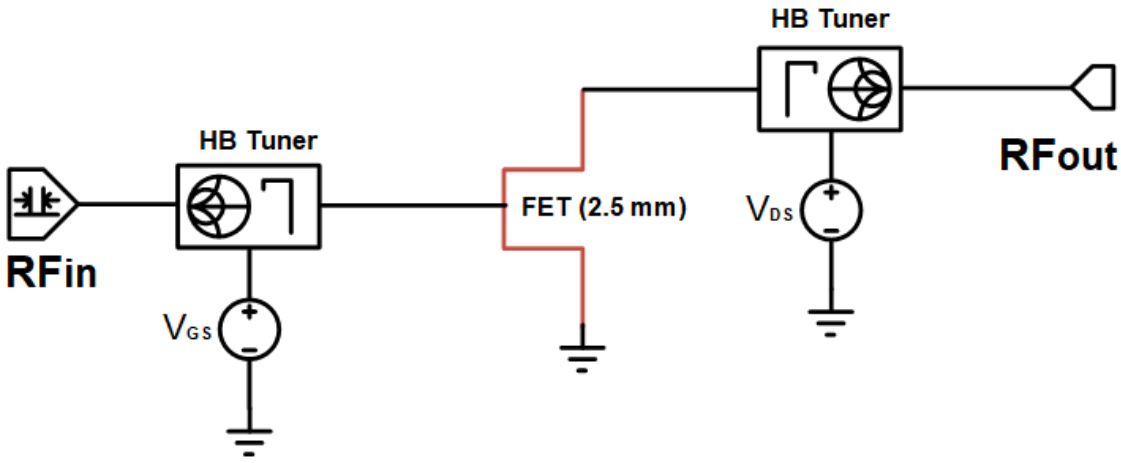
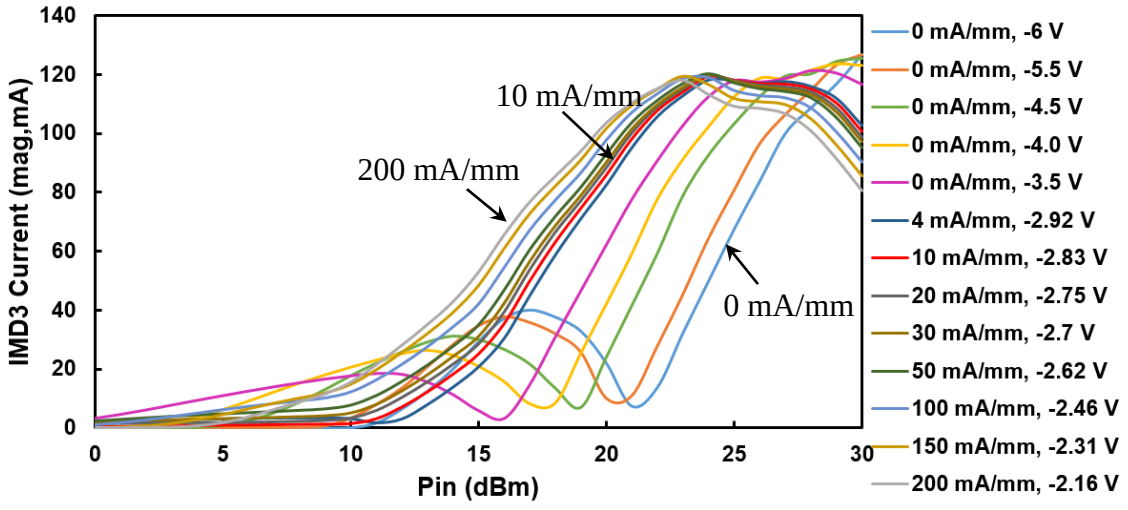
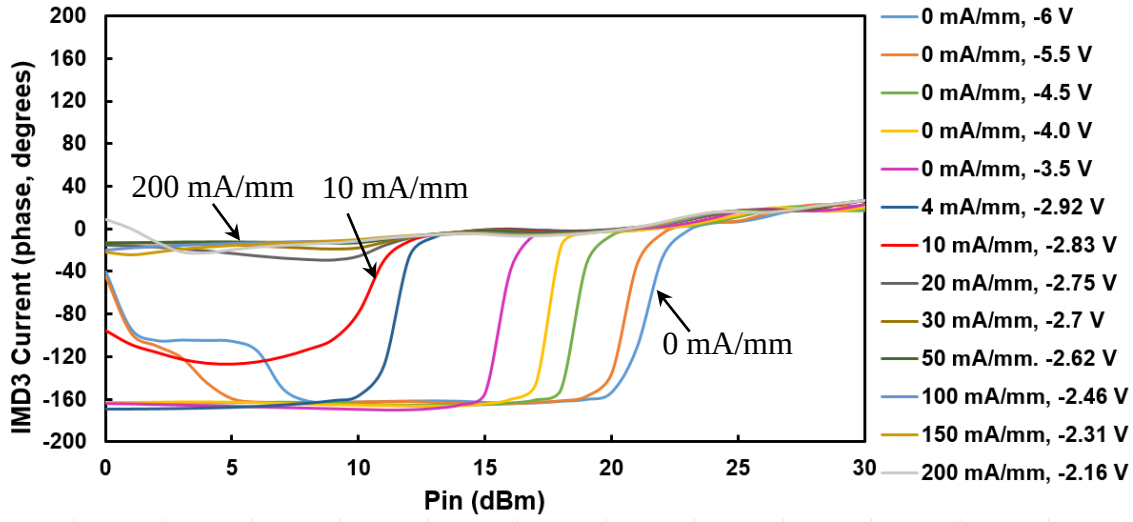


Fig. 4-3: Schematic of 2.5 mm FET terminated with 50-ohm termination using Harmonic Balance (HB) Tuners.



(a)



(b)

Fig. 4-4: (a) Plot of magnitude of IMD3 current (mA) vs. Pin (dBm). (b) Plot of phase of IMD3 current (degrees) vs. Pin (dBm) for 2.5 mm FET.

From Fig. 4-4, if two devices can be biased in such a way that the phase of IMD3 currents of one of the FETs is out of phase with that of the other FETs, then cancellation of IMD3 components can occur. Values of the bias voltages were computed from the above experiment. However, in a circuit, the conditions for cancellation will depend on the impedance matching networks and other factors as well. Therefore, a power sampler (PWRSMP) schematic element was used for simulation in AWR microwave office to see if the components are cancelling each other or not.

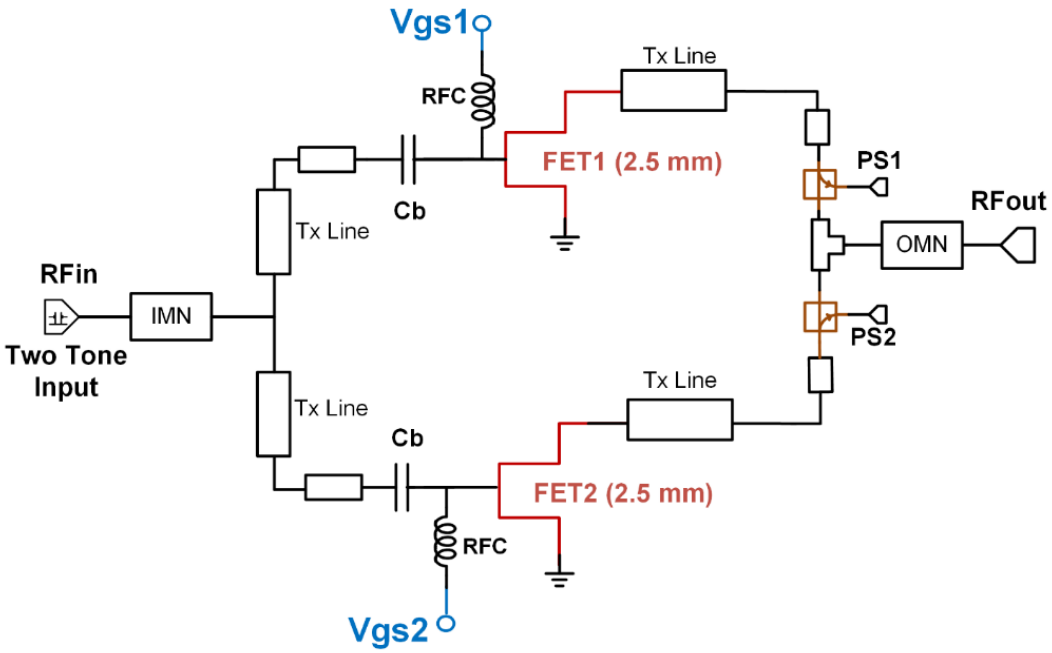
PWRSMP is an ideal frequency independent, lossless, directional coupler which can sample current, voltage, power, etc. at various points in a circuit without introducing any signal loss.
The 3 port S-matrix of the power sampler is given in equation (9) [47]:

$$S=\begin{pmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{pmatrix}=\begin{pmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{pmatrix} \quad (9)$$

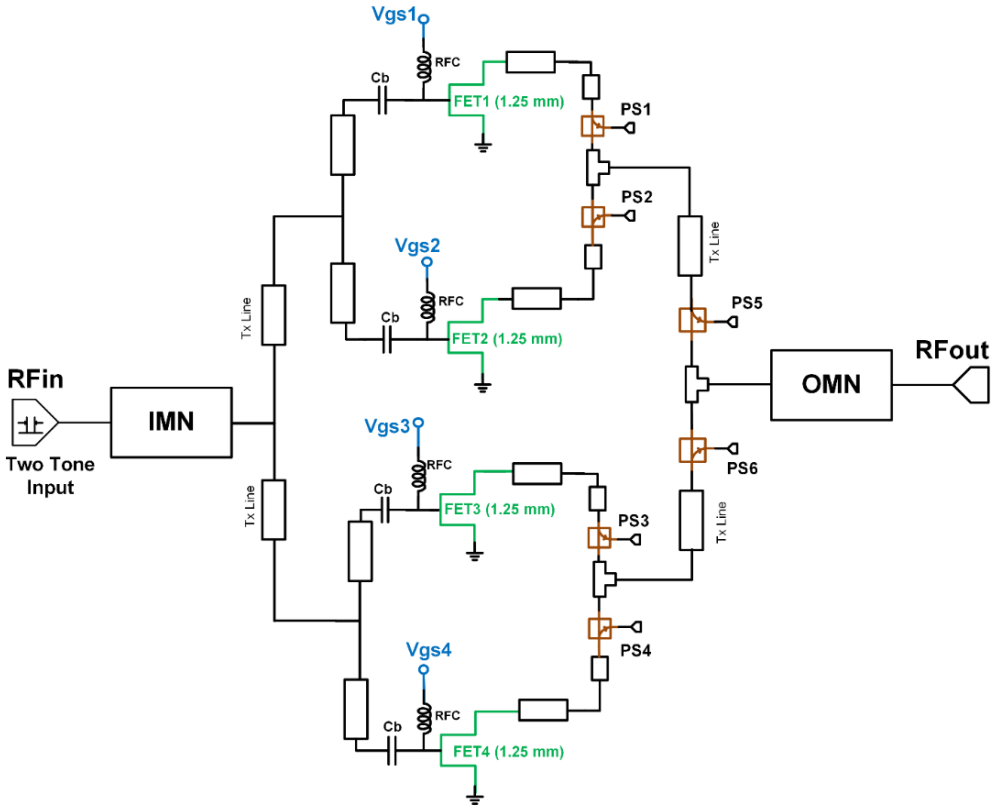
Schematics of two parallel and four parallel FETs circuit with power sampler at various nodes are as shown in Fig. 4-5(a) and Fig. 4-5(b) respectively. The input port generates two-tone signals with a frequency spacing of 5 MHz and power levels are swept from -10 dBm to 30 dBm. The intermodulation current was checked at the output of each of the FET with the power sampler. By changing the bias of each FET, the variation of the phase of the IMD3 current at the output of the FET can be seen. This is discussed further in the following sections.

4.4 Circuit Design

Three prototype amplifier circuits (total gate width = 5 mm) were designed and simulated using the foundry based nonlinear model over the frequency range of 0.8-1.0 GHz in the AWR microwave office. In the first circuit, a 5 mm (width w) GaN HEMT device was used, in the second, two parallel 2.5 mm (width w/2) GaN HEMTs were used, and in the third, four parallel 1.25 mm (width w/4) GaN HEMTs were used. Detailed schematic diagrams of three amplifiers are shown in Fig. 4-6. Because of the same overall gate periphery (5 mm), the circuits were made with similar input and output loading conditions. The output load was matched to the best power point according to the load pull results. The parasitic effects of the various device packages were taken into account for matching the output network. Series resistors were used at the input for the stabilization. Blocking capacitors (Cb = 1000 pF) were used to isolate the gate bias voltages of each of the FET from the other FET). Rogers 4350 substrate material was used for the design of the transmission lines. Fig. 4-7 show the simulated plot of the S-parameters vs. frequency. Fig. 4-8 show simulated plot of Output power (Pout), gain and PAE vs. Input Power (Pin) for the three circuits. The solid lines refer to a single 1 x 5 mm circuit and dashed and dotted lines refer to 2 x 2.5 mm and 4 x 1.25 mm circuit respectively. From the simulation of the three circuits, it can be seen that the performance is similar in the frequency band of interest (0.8-1.0 GHz).



(a)



(b)

Fig. 4-5: (a) Schematic of two parallel FETs circuit with power samplers PS1 and PS2 at the output of the two FETs. (b) Schematic of four parallel FETs circuit with power samplers at output of each FET and at the combination of two FETs. C_b is the blocking capacitor and RFC is RF choke.

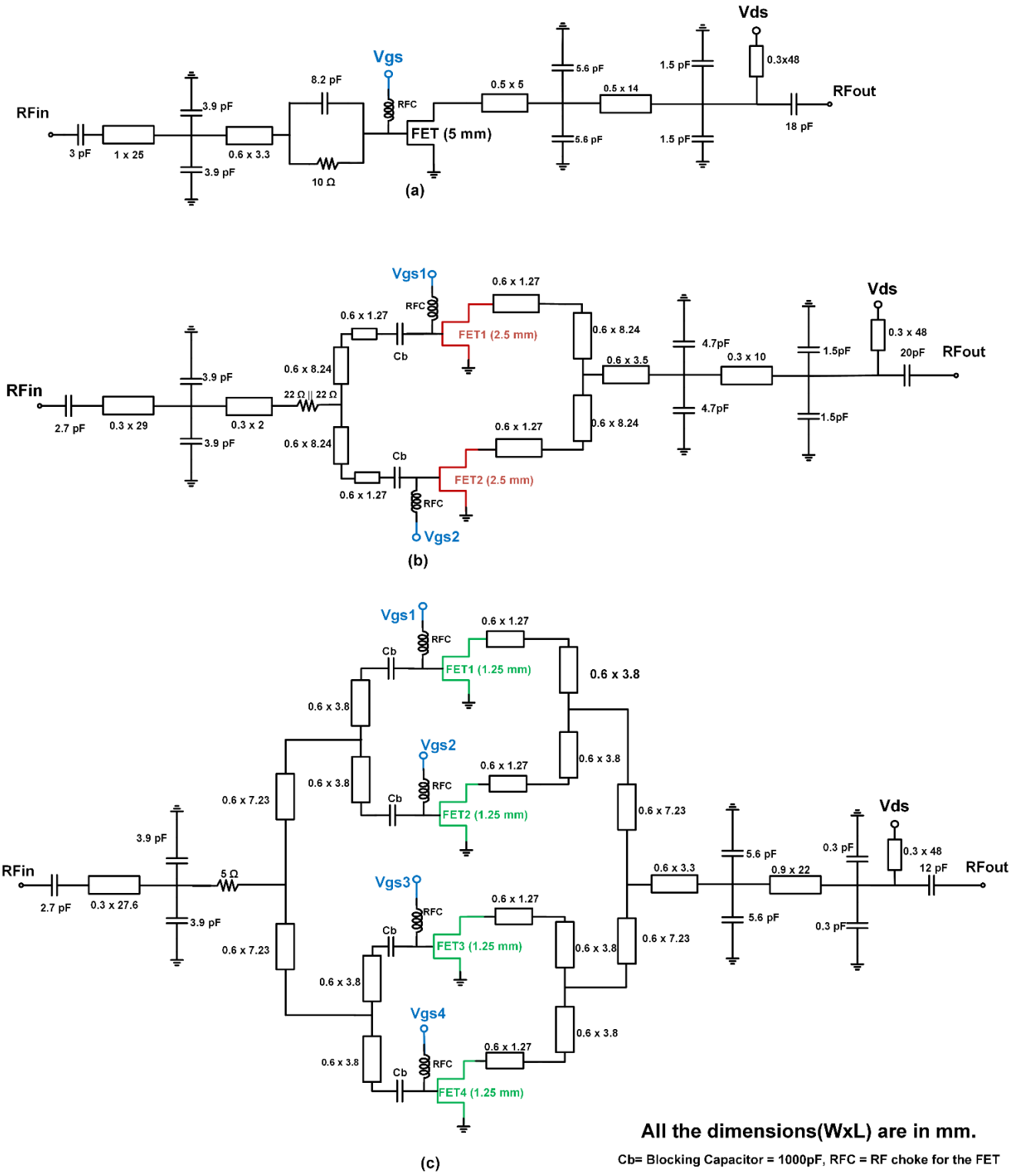


Fig. 4-6: Schematic of the three amplifier circuits (a) with a single FET of size 1 x 5 mm (width w), (b) with two parallel FETs of size 2 x 2.5 mm (width w/2) each, (c) with four parallel FETs of size 4 x 1.25 mm (width w/4) each.

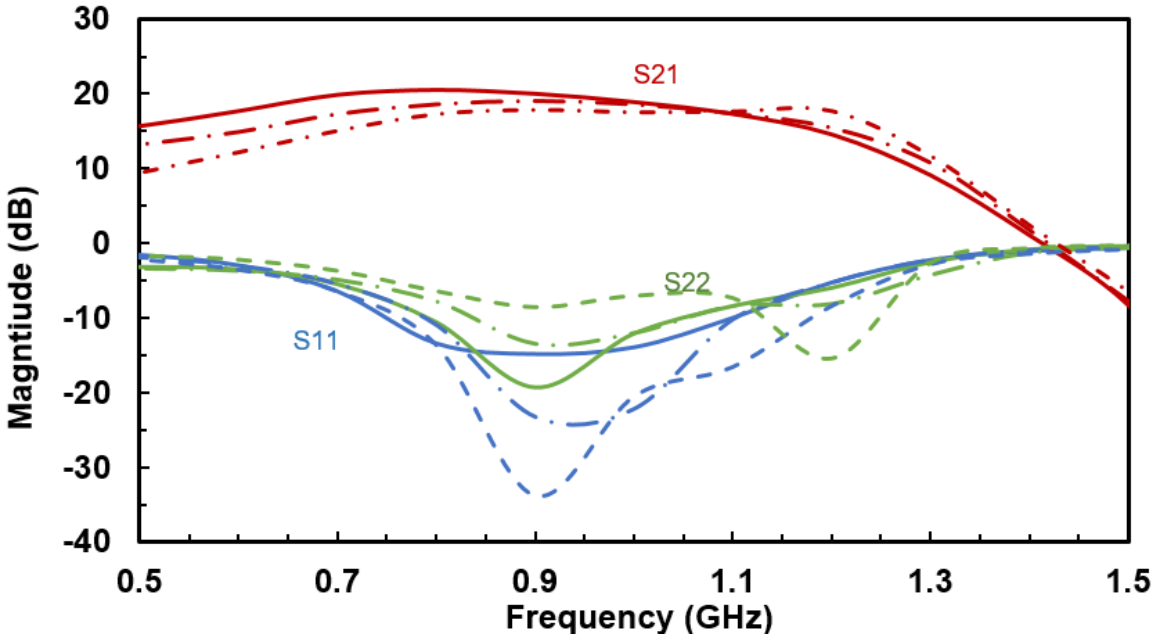


Fig. 4-7: Simulated plot of small signal S-parameters w.r.t frequency for the three circuits (1 x 5 mm, 2 x 2.5 mm and 4 x 1.25 mm).

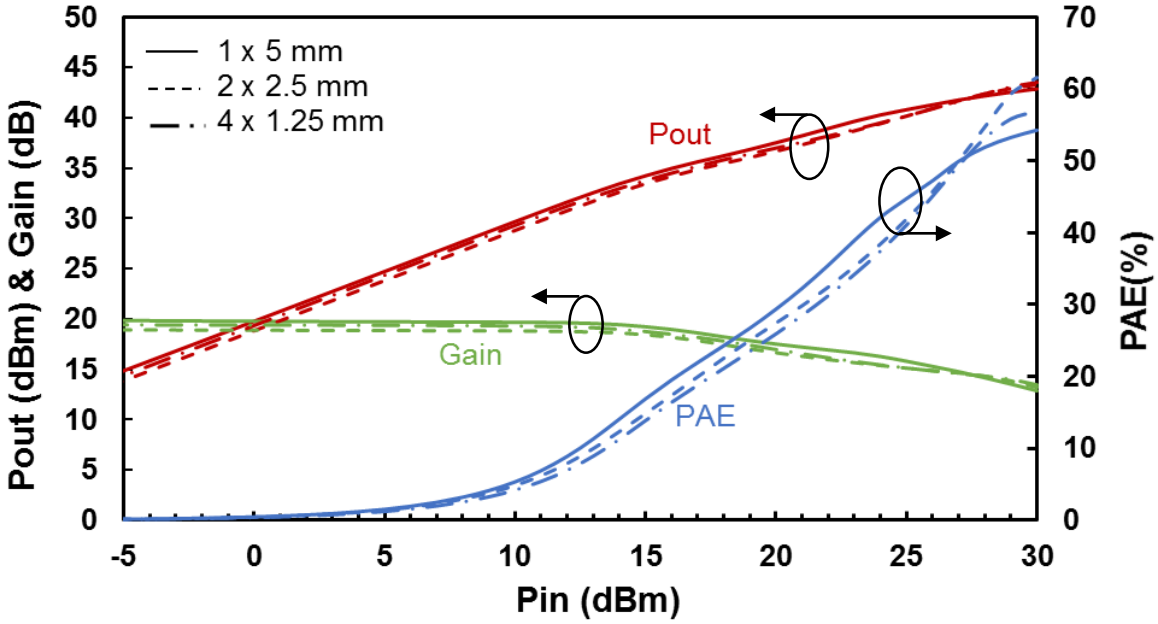


Fig. 4-8: Simulated plot of Pout, Gain and PAE w.r.t Pin of the three circuits (1 x 5 mm, 2 x 2.5 mm, 4 x 1.25 mm).

From the simulation results in Fig. 4-8, the output power obtained is 43 dBm, PAE is 55%, small signal gain about 17-20 dB for all the three circuits which are in the frequency range of 0.8-1.0 GHz.

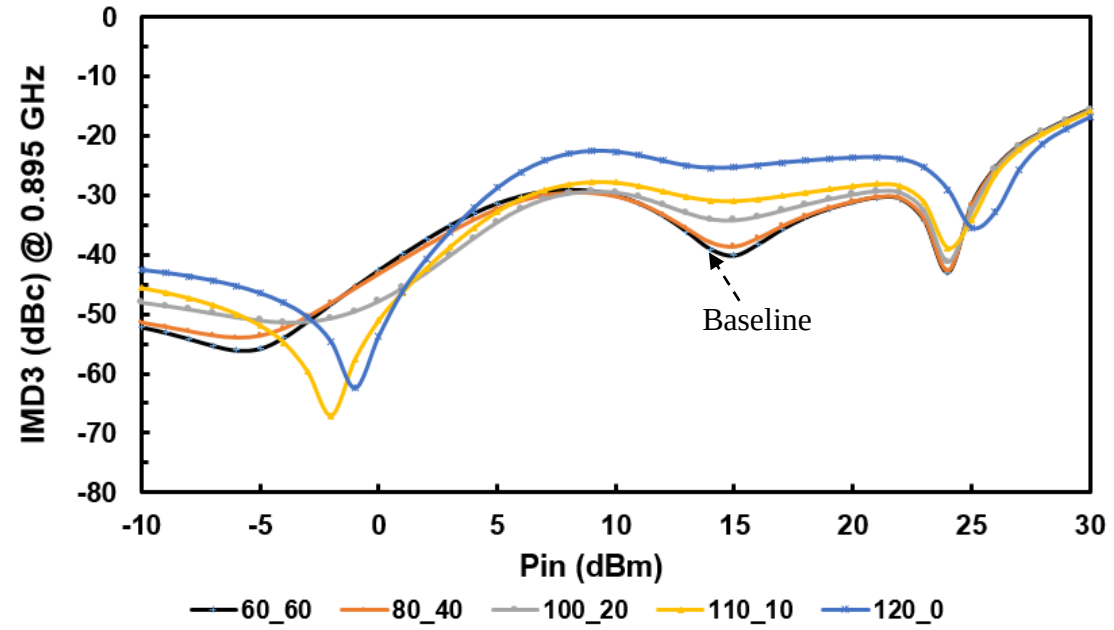
4.5 Non-linearity Cancellation Simulation Results

4.5.1 Simulation of Two Parallel FETs Circuit (2 x 2.5 mm)

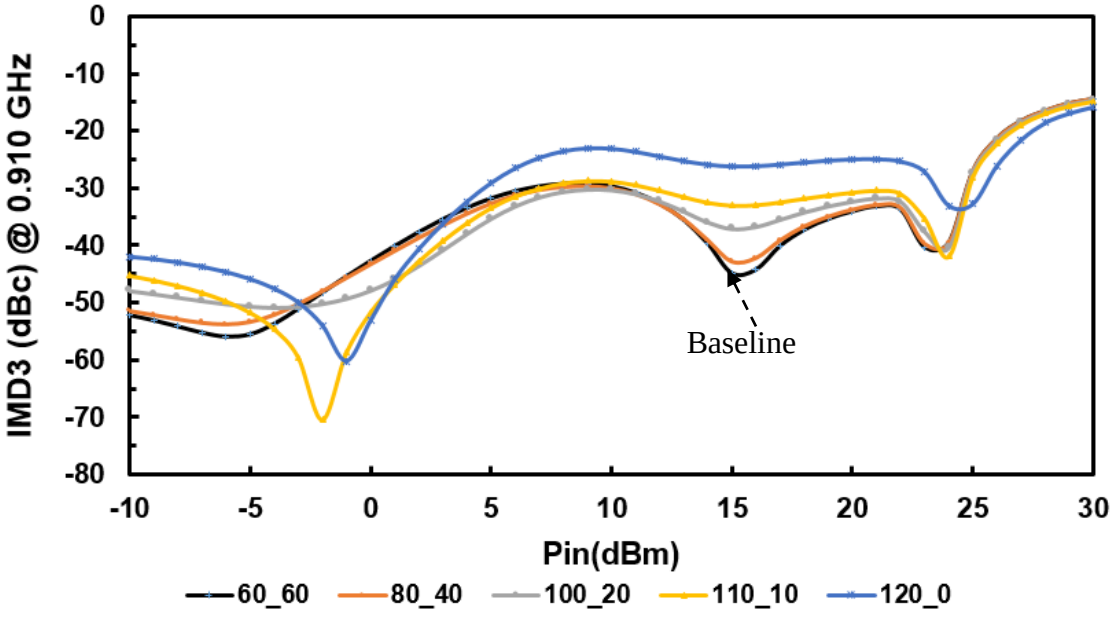
A two-tone signal at the center frequency of 900 MHz was applied to the two parallel FETs circuits at the bias current level of 60 mA/mm which is 150 mA bias for the 2.5 mm FET device. The total current was 300 mA for two parallel FETs. IMD3 vs. Pin was plotted at both the lower (Fig. 4-9(a)) and higher intermod levels (Fig. 4-9(b)). All current values in the plot are given as mA/mm. In the plot, the black line curve depicts the case (baseline) when both the devices being biased at 60 mA/mm (150 mA) (referred to as 60_60). Then, a gradient bias is applied, i.e., in one of the FETs, the bias current is increased while in the other, the current is reduced so that the net bias current remains the same. The total sum of current in both the FETs is kept at 60 mA/mm (which is 300 mA for 5 mm). It is observed that by giving the gradient bias, an improvement in linearity occurs between the power levels from -5 dBm to 0 dBm for this circuit. The maximum improvement is seen when one FET is biased at 110 mA/mm (class AB mode) and another at 10 mA/mm (deep Class AB mode) (110_10). If we further increase the current spacing, i.e., bias one FET at 120 mA/mm and another at 0 mA/mm (120_0), we do not see as much as an improvement as with the case of 110_10. There is no improvement seen at a bias of 80_40.

Fig. 4-10(i) shows the magnitude and the phase of the IMD3 currents plotted at the outputs of each of the two parallel FETs (FET1: blue and FET2: green) for different bias conditions.

The dashed lines (H) show the current at the higher intermodulation frequency (0.910 GHz) and the solid lines (L) show the current at lower intermodulation frequency (0.895 GHz). When both the FETs are biased in the same manner (60 mA/mm each), the IMD3 currents of two FETs are the same, the phase difference between the IMD3 currents of the two FETs is zero and they combine at the output, increasing the total magnitude. As the bias between the FETs is varied, the magnitude and phase of IMD3 current from the FETs start to change w.r.t each other. This is shown in Fig. 4-11(a,b,c,d). At the output, two currents vectorally add to each other. The shift in the phases can result in-phase cancellation and reduction in IMD at the output. In the simulation results, the solid line shows the simulation at frequency 0.895 GHz (lower intermod), and the dashed line shows the simulation at 0.910 GHz (higher intermod).



(a)



(b)

Fig. 4-9: Simulated plot of IMD3 vs. Pin at total bias of 60 mA/mm for 2 x 2.5 mm circuit (a) at frequency 0.895 GHz (lower intermod) (b) at frequency 0.910 GHz (higher intermod).

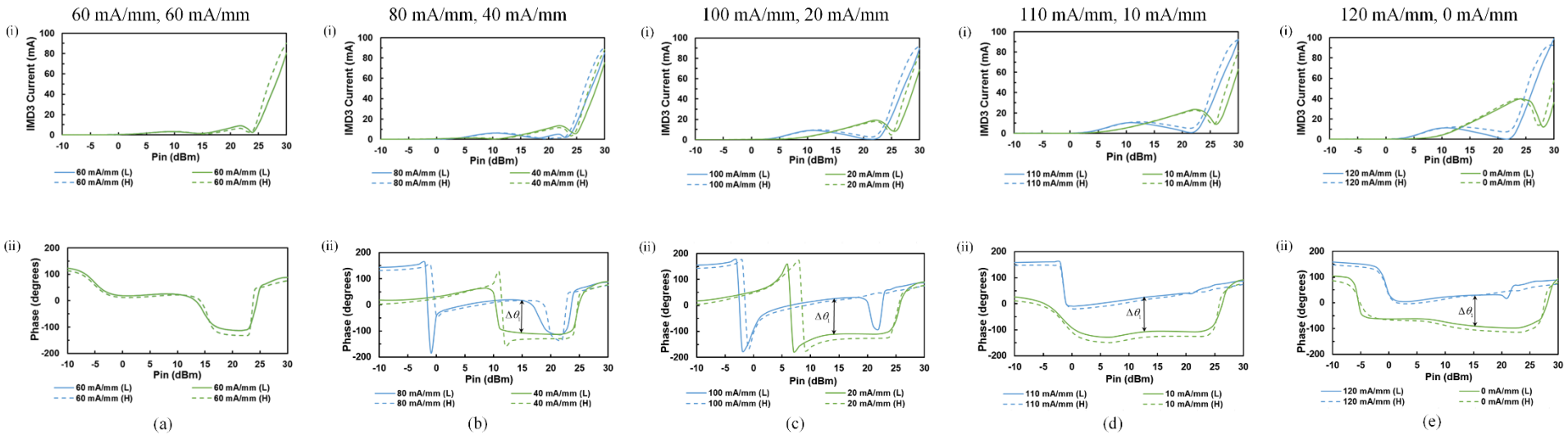


Fig. 4-10: Plot of (i) magnitude (ii) phase of IMD3 current for two parallel FETs circuit for different cases of bias conditions for two FETs (a) 60 mA/mm, 60 mA/mm (60_60) (b) 80 mA/mm, 40 mA/mm (80_40) (c) 90 mA/mm, 30 mA/mm (90_30) (d) 100 mA/mm, 20 mA/mm (100_20) (e) 120 mA/mm, 0 mA/mm (120_0). The plots are done at both the intermod levels: solid ones are at lower intermod levels (0.895 GHz) and the dotted ones are at higher intermod levels (0.910 GHz).

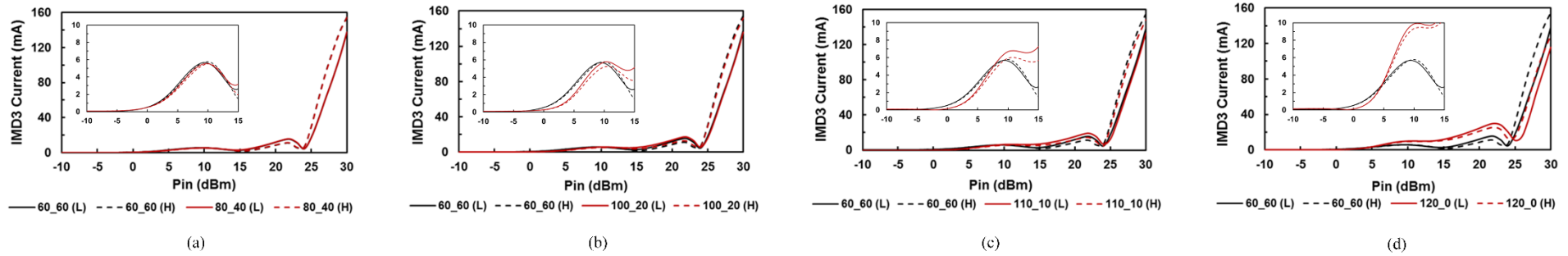


Fig. 4-11 : Comparison of plot of the IMD3 current at baseline in comparison with other bias conditions. (a) Comparison of bias condition 60_60 with 80_40. (b) Comparison of bias condition of 60_60 with 100_20. (c) Comparison of bias condition of 60_60 with 110_10. (d) Comparison of bias condition of 60_60 with 120_0. Subplot: zoomed-in view until the input power level of 15 dBm and bias current of 10 mA.

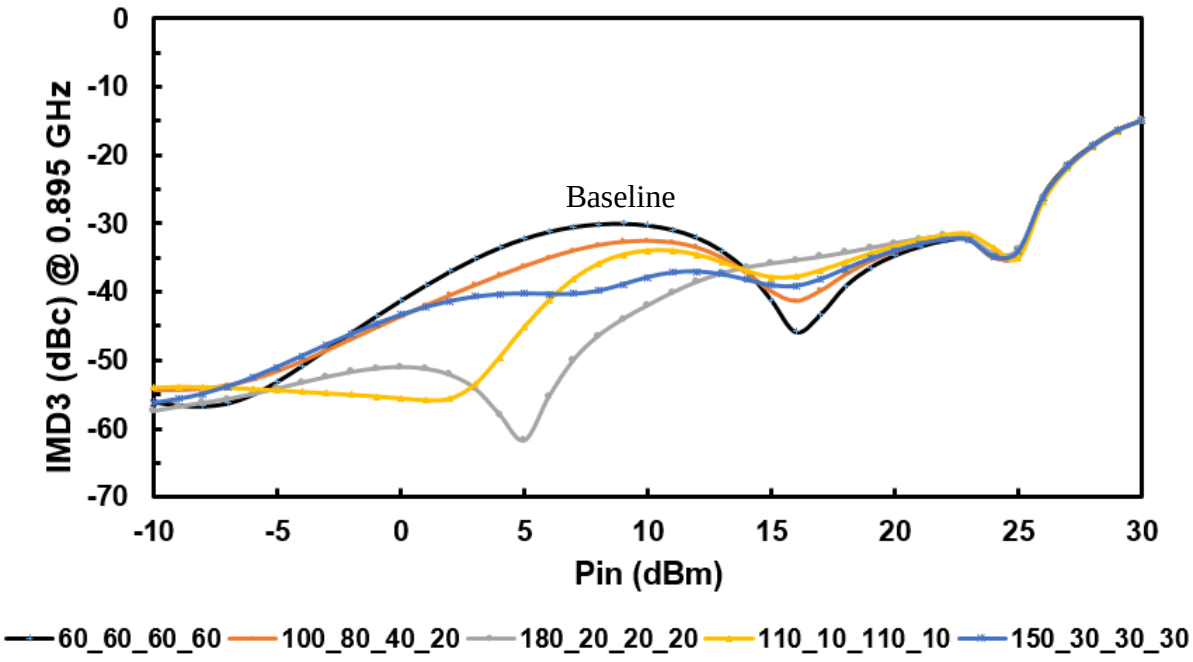
The phase difference in the IMD3 current is shown by $\Delta\theta_1$ given by the following expression.

$$\Delta\theta_1 = \left|\theta_{31} - \theta_{32}\right| \tag{10}$$

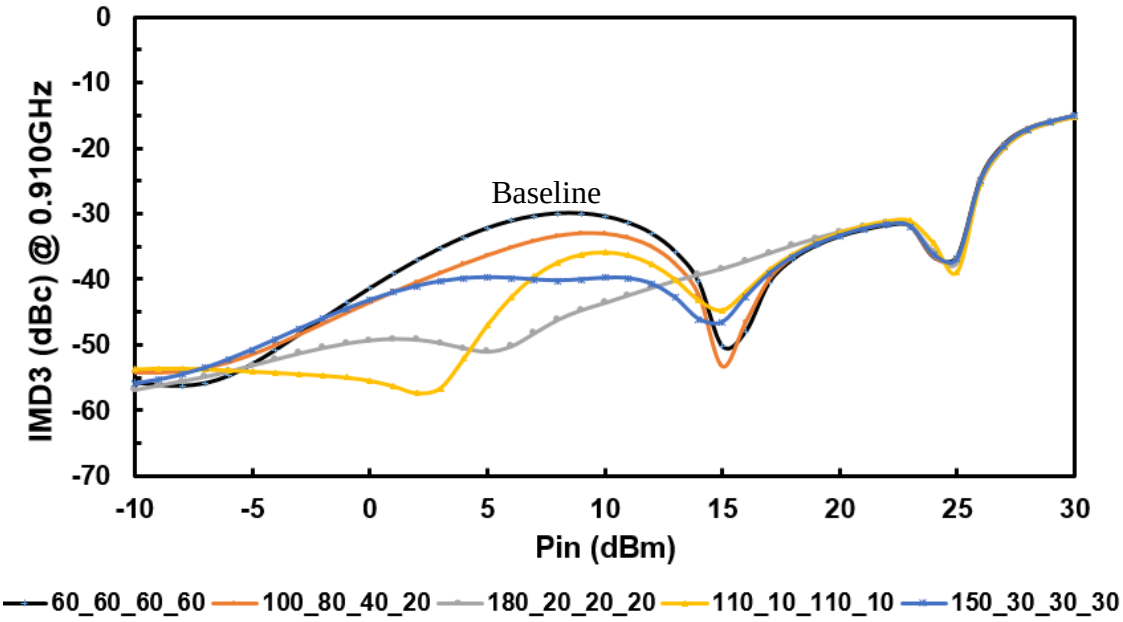
From Fig. 4.1, θ_{31} is the phase of the IMD3 component of the first parallel FET and θ_{32} is the phase of the IMD3 component of the second parallel FET. The difference in-phase $(\Delta\theta_1)$ leads to cancellation of the IMD3 components at the output and improvement in IMD3 performance. Fig. 4-11 compares the magnitude of the IMD3 current with different bias condition (red) compared to the baseline condition (black) at the output of the amplifier w.r.t input power (Pin). Fig. 4-11(a) does the comparison of the bias condition of 60_60 with the bias condition of 80_40. The phase of the IMD3 components are similar; hence, the IMD3 current of both the FETs do not cancel out with the other. However, in Fig. 4-11(b) and Fig. 4-11(c) the total IMD3 current at the output shown in red is lower than the output current of the baseline. This is until the input power (Pin) of 8 and 10 dBm, respectively. After that, it increases in magnitude. However, for the bias conditions of 120_0, it can be seen that the magnitude of the red curve is less than the black curve until the power level of 3 dBm after that it increases in magnitude showing the effect of the non-linearity in the simulation. As seen in Fig. 4-11(a,b), the IMD3 for bias condition 100_20 is lower than the IMD3 for bias condition 60_60 until Pin is 10 dBm. Similarly, the IMD3 for bias condition 110_10 is better than baseline 60_60 in the power range of -5 to 0 dBm. This result is so because of the phase cancellation of the net IMD3 current leads to the lowering of the total magnitude of IMD3 at the output.

4.5.2 Simulation of Four Parallel FETs Circuit (4 x 1.25 mm)

Large-signal simulations were then performed for four parallel FETs circuit (4 x 1.25 mm), varying the bias of each FET independently. The total bias current was kept at 60 mA/mm (300 mA). Fig. 4-12 shows simulated plots of the IMD3 vs. input power (Pin) for various bias conditions. The black curve represents a condition when all the four FETs (size = 1.25 mm each) are biased at baseline 60 mA/mm (60_60_60_60) (case 1 as discussed in section 4.2.3). The case of 110_10_110_10 refers to when FET1 and FET3 are biased at 110 mA/mm, and FET2 and FET4 are biased at 10 mA/mm (case 2a). The case 180_20_20_20 refers when first FET is biased at 180 mA/mm and all other FETs are biased at 20 mA/mm (case 2b). By applying variable bias current values, an improvement in linearity is seen.



(a)



(b)

Fig. 4-12: Simulated plot of IMD3 (dBc) vs. Pin (dBm) at different bias values for four parallel FETs circuit (4 x 1.25 mm) at frequency (a) 0.895 GHz, (b) 0.910 GHz.

At the input power of 5 dBm, the IMD3 improves up to 20 - 25 dBc at the condition 110_10_110_10 (yellow curve) and 180_20_20_20 (grey curve) compared to the baseline curve

(60_60_60_60) and up to 15 dBc at Pin of 10 dBm. It may be noted that in some cases, there is more improvement in linearity in one sideband compared to the other sideband (for example, it can be seen from Fig. 4-12 that the bias condition of 180_20_20_20 (gray curve) is more pronounced at the lower sideband Fig. 4-12(a) compared to the upper sideband Fig. 4-12(b). This is so because as seen in chapter 1, IMD3 is the ratio of the fundamental signal to the sideband. In some cases, the one sideband tends to be lower than the other sideband. This results in more pronounced curve.

Fig. 4-13(i) shows the magnitude and Fig. 4-13(ii) shows the phase plot of the IMD3 current vs. Input power (Pin) for FET1 (blue) and FET2 (green) for different bias conditions. Fig. 4-14 shows the magnitude and the phase plot of the IMD3 current vs. Pin for FET3 (blue) and FET4 (green). The phase difference in the IMD3 currents of the two FETs is represented by variable $\Delta\theta_1$.

For the baseline condition, 60_60_60_60, when all the FETs are biased with the same current, which is 60 mA/mm, there is no phase difference in the IMD3 current in the two FETs. For the bias condition of 100_80_40_20, there is a slight phase difference between the currents of FET1 and FET2, as shown in Fig. 4-13(b) and FET3 and FET4, as shown in Fig. 4-14(b), respectively.

For the bias condition of 110_10_110_10, there is a significant phase difference in the IMD3 current of the FETs. First two FETs exhibit the same difference as the third and fourth. Similarly, this fact can be seen in the case of 150_30_30_30.

If the FETs have different bias current values, the phase of the IMD3 current can vary by a considerable amount. This case is apparent for the condition 110_10_110_10, i.e., when the first FET is biased at 110 mA/mm and the second FET is biased at 10 mA/mm, where the difference in-phases can be seen. Similarly, for the bias condition of 150_30_30_30, i.e., when the first FET is biased at 150 mA/mm and the other FETs are biased at 30 mA/mm, the phase difference is apparent. This leads to the phase cancellation of the IMD3 components.

Fig. 4-15 depicts the magnitude and phase plot of the sum of the IMD3 current from two branches FET1 + FET2 (pink) and FET3 + FET4 (purple). Fig. 4-16 shows the plot of the IMD3 current at the output of the amplifier (red) for each of the bias conditions and its comparison with the baseline case: 60_60_60_60 (shown in black). It can be seen in bias conditions, when FETs are biased differently (when one is class AB and others in deep Class AB), the net IMD3 current at the output is less compared when the FETs are biased in the baseline case.

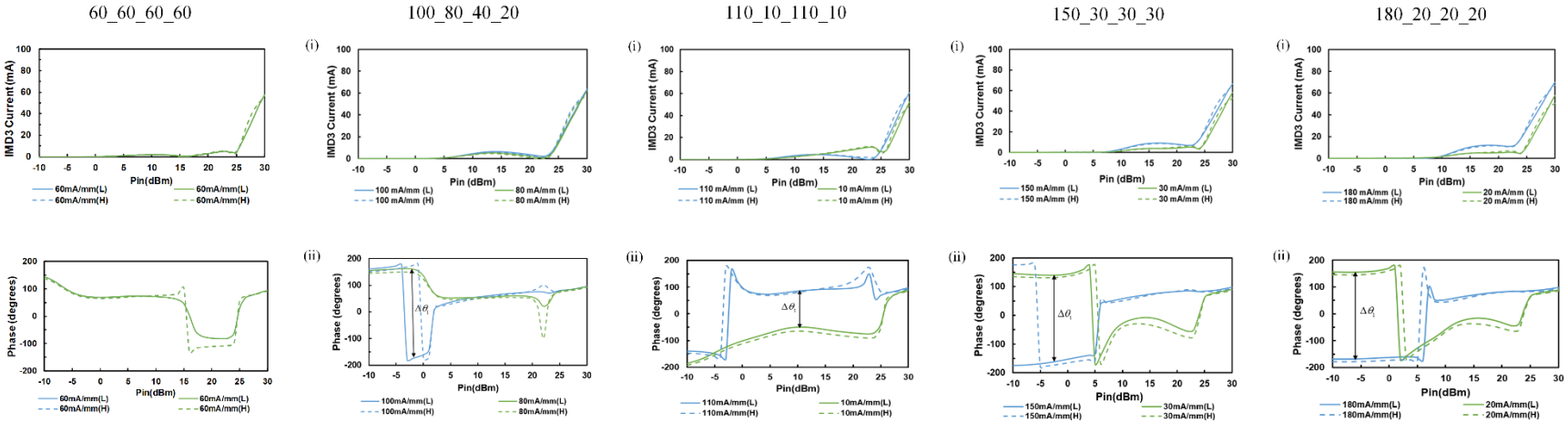


Fig. 4-13: Plot of magnitude and phase of the IMD3 current for four parallel FETs circuit (4 x 1.25 mm) for FET1 and FET2 at different bias conditions (a) 60,60,60,60 mA/mm (60_60_60_60) (b) 100,80,40,20 mA/mm (100_80_40_20) (c) 110,10,110,10 mA/mm (110_10_110_10) (d) 150,30,30,30 mA/mm (150_30_30_30) (e) 180,20,20,20 mA/mm (180_20_20_20).

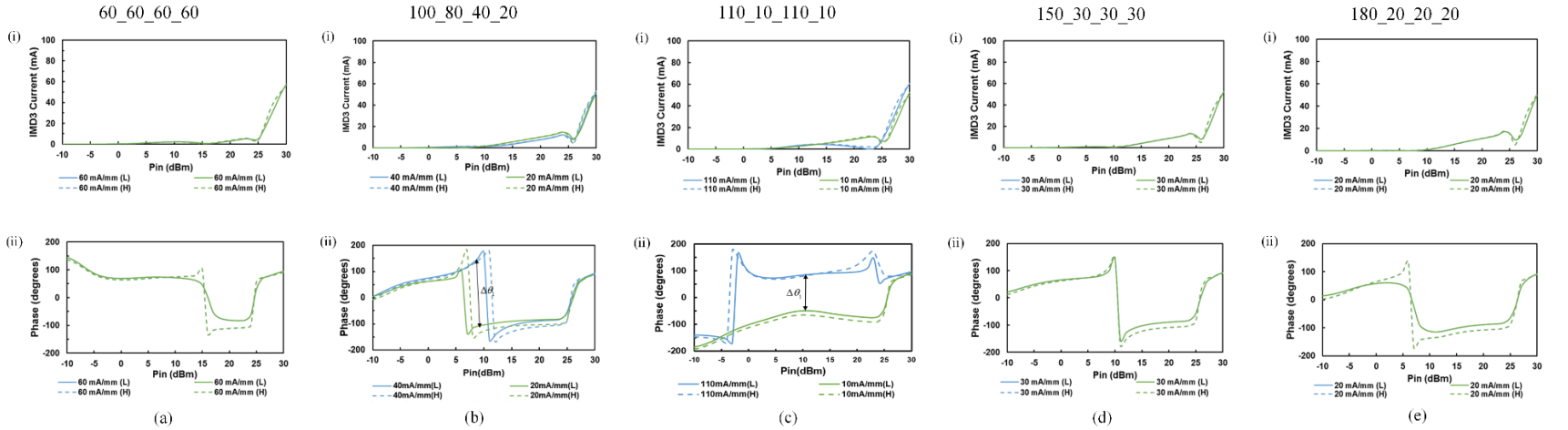


Fig. 4-14: Plot of magnitude and phase of the IMD3 current for four parallel FETs circuit (4 x 1.25 mm) for FET3 and FET4 at different bias conditions (a) 60,60,60,60 mA/mm (60_60_60_60) (b) 100,80,40,20 mA/mm (100_80_40_20) (c) 110,10,110,10 mA/mm (110_10_110_10) (d) 150,30,30,30 mA/mm (150_30_30_30) (e) 180,20,20,20 mA/mm (180_20_20_20).

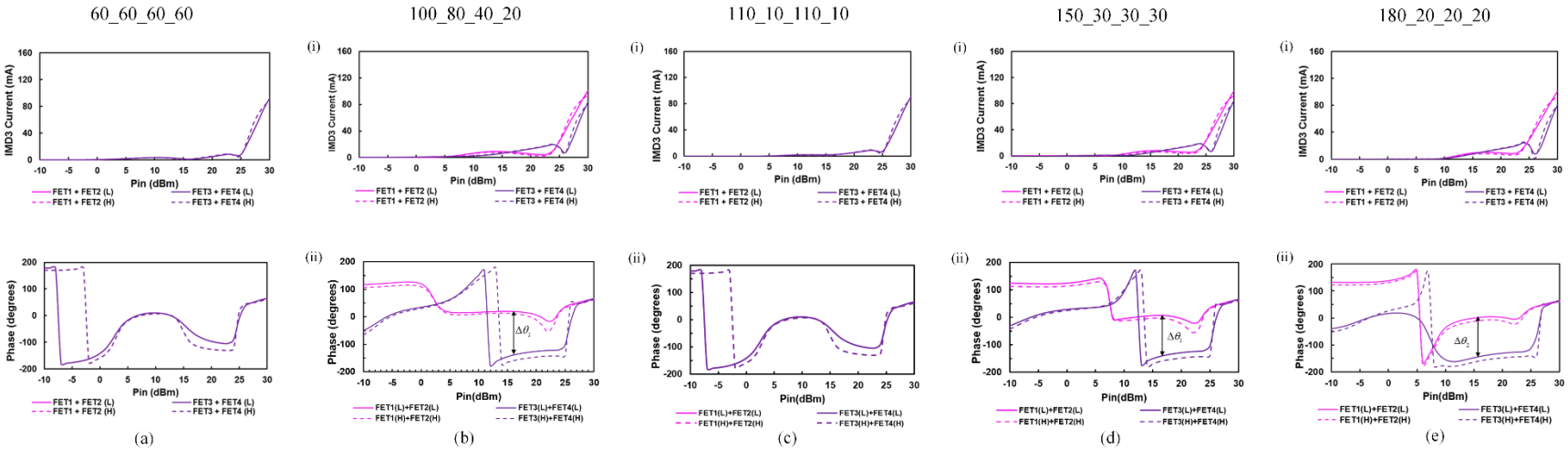


Fig. 4-15: Plot of (i) magnitude and (ii) phase of sum of the IMD3 current from FET1 + FET2 (magenta) and FET3 + FET4 (purple) for the different bias conditions: (a) 60,60,60,60 mA/mm (60_60_60_60) (b) 100,80,40,20 mA/mm (100_80_40_20) (c) 110,10,110,10 mA/mm (110_10_110_10) (d) 150,30,30,30 mA/mm (150_30_30_30) (e) 180,20,20,20 mA/mm (180_20_20_20).

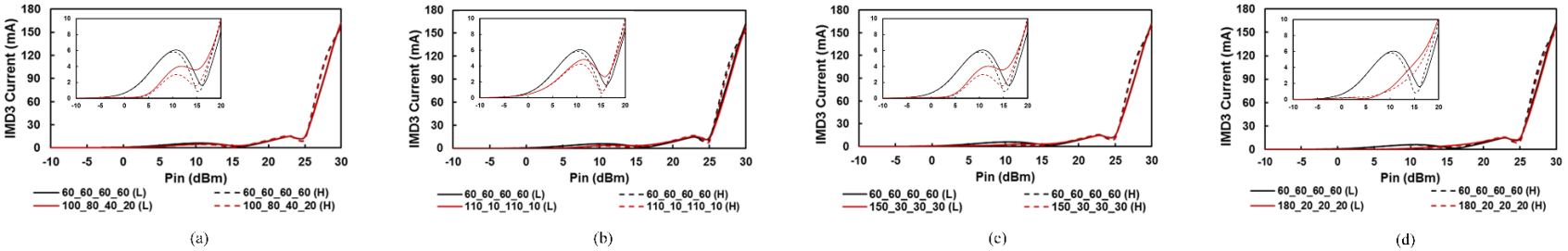


Fig. 4-16: Plot of the IMD3 current for the bias condition of 60_60_60_60 (black) in comparison with the other plots: (a) Comparison of 60_60_60_60 with bias condition of 100_80_40_20. (b) Comparison of 60_60_60_60 with bias condition of 110_10_110_10. (c) Comparison of 60_60_60_60 with 150_30_30_30 (d) Comparison of 60_60_60_60 with 180_20_20_20. Subplot : zoomed-in plot until Pin = 20 dBm.

This is due to the phase cancellation of the IMD3 components which results in lowering the magnitude of the IMD3 current. This plot explains the improvement of IMD3 found in Fig. 4-12. The phase difference is shown by $\Delta\theta_2$ for the case of the four parallel FETs circuit. This phase difference can be expressed as

$$\Delta\theta_2 = \left\| \theta_{31} - \theta_{32} \right| - \left| \theta_{33} - \theta_{34} \right\| \tag{11}$$

i.e. the phase difference of the first two parallel FETs (FET1+FET2) combined with phase difference between the third and the fourth parallel FETs (FET3 + FET4).

In Fig. 4-16(a,b,c,d), in zoomed-in plot, it can be seen that the red curve (bias variation) is lower than the black curve (baseline) until power level of 15 dBm after which, it increases in magnitude. This lower magnitude of current leads to the improvement in IMD3. It should be noted that for this technique to work, one of the sub FETs should be biased in AB and the other in deep AB. If all the FETs are in Class AB or deep Class AB, then this technique will not work.

Hence, if we compare Fig. 4-9 with two parallel FETs circuit (2 x 2.5 mm circuit) and Fig. 4-12 with four parallel FETs circuit (4 x 1.25 mm circuit), respectively, we see more improvement in linearity over more extensive power range with four parallel FETs circuit than two parallel FETs circuit. With four parallel FETs, there is a higher degree of freedom by varying the current bias values to cancel the IMD3 components with the two in parallel FETs circuit. With two parallel FETs circuit, the IMD3 cancellation is narrowband and is seen at very low power values. However, with the four parallel FETs circuit, the IMD3 cancellation can be seen both at the lower and middle power levels.

4.5.3 Comparison of Improvement in Linearity for Different Bias Values

The proposed technique was explored for five different bias values as given below. The total bias current for a circuit of 5 mm gate periphery is given in the parenthesis.

Case 1: 40 mA/mm (200 mA)

Case 2: 60 mA/mm (300 mA)

Case 3: 80 mA/mm (400 mA)

Case 4: 100 mA/mm (500 mA)

Case 5: 120 mA/mm (600 mA)

For total current values higher than 120 mA/mm (600 mA) or lower than 40 mA/mm (200 mA), it becomes difficult to achieve the phase cancellation by changing the bias values of the individual parallel FETs. Hence, they were not explored for cases other than mentioned above.

From Fig. 4-17 to Fig. 4-21 the plot of IMD3 (dBc) vs. Input Power (Pin) for the 1 x 5 mm circuit is shown in orange color, the plot for the 2 x 2.5 mm circuit is shown in green, and for the 4 x 1.25 mm circuit is shown in yellow. The solid line curve is when all the FETs in the circuit are biased with the same bias current, and the dashed line curve is when the bias current is varied for each individual FET in the circuit. Note that the bias currents are mentioned in mA/mm and their values are given in the parenthesis in the legend.

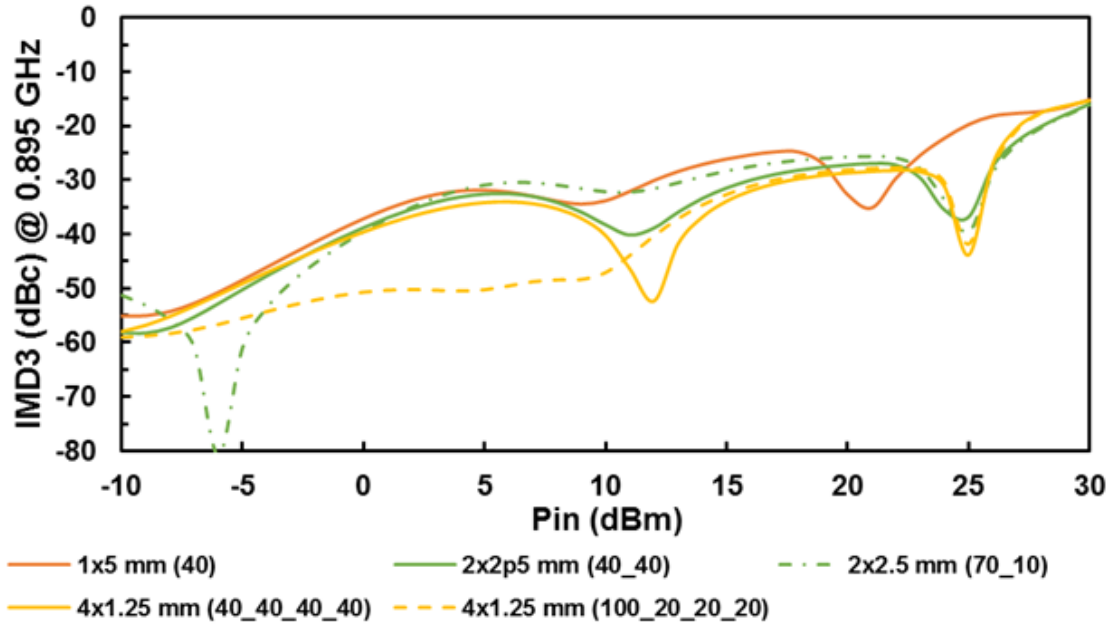
Case 1: The total bias current is 40 mA/mm (= 200 mA for 5 mm FET) as shown in Fig. 4-17.

For example, legend entry of 1 x 5 mm (40) refers to the first circuit containing a 5 mm FET biased at 40 mA/mm, which is a 200 mA total current for the 5 mm FET. Similarly, 2 x 2.5 mm (40_40) refers to each of the 2.5 mm FETs being biased at 40 mA/mm. The total current of 200 mA gets divided into 100 mA for two parallel FETs when biased with the same bias current. The dashed curve (70_10) refers to the case when the current is divided unequally into two parallel FETs, i.e., first FET is biased at 70 mA/mm (175 mA) and second FET is biased at 10 mA/mm (25 mA). Therefore, the total current is 200 mA. Similarly, legend entry of 4 x 1.25 mm (40_40_40_40) refers to 4 x 1.25 mm circuit where each FET is biased at 50 mA (40 mA/mm for 1.25 mm FET) each. 4 x 1.25 mm (100_20_20_20) refers to the first FET being biased at 100 mA/mm (125 mA for 1.25 mm FET) and the other FETs 20 mA/mm (25 mA for 1.25 mm FET). Following observations are made:

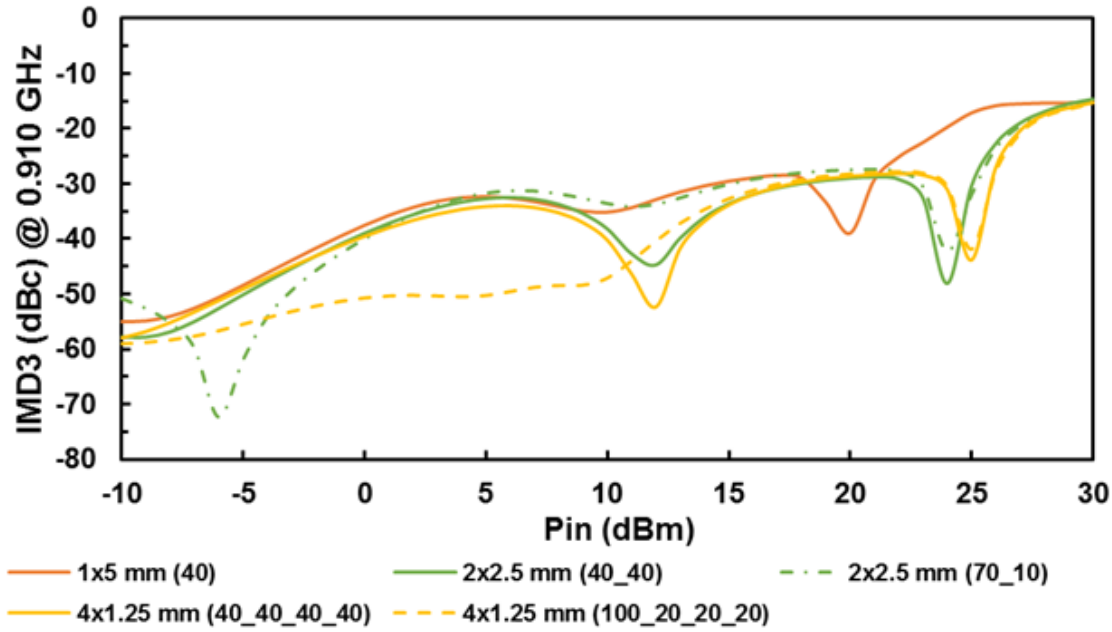
- The 2 x 2.5 mm circuit achieves improvement in the linearity up to 20 dBm at a very narrow range of power level (typically between -5 dBm to 0 dBm).
- The 4 x 1.25 mm circuit sees more improvement in linearity from low power to the mid-range power level (0 - 15 dBm). This is attributed to the fact that more phase cancellation is achieved with four parallel FETs. Hence, in order to get better linearity, it is useful to divide a large FET into multiple parallel smaller FETs.

Case 2: The total bias current is 60 mA/mm (= 300 mA for 5 mm FET).

Fig. 4-18(a,b) shows the plot of IMD3 vs. Pin when the net bias current is 60 mA/mm.

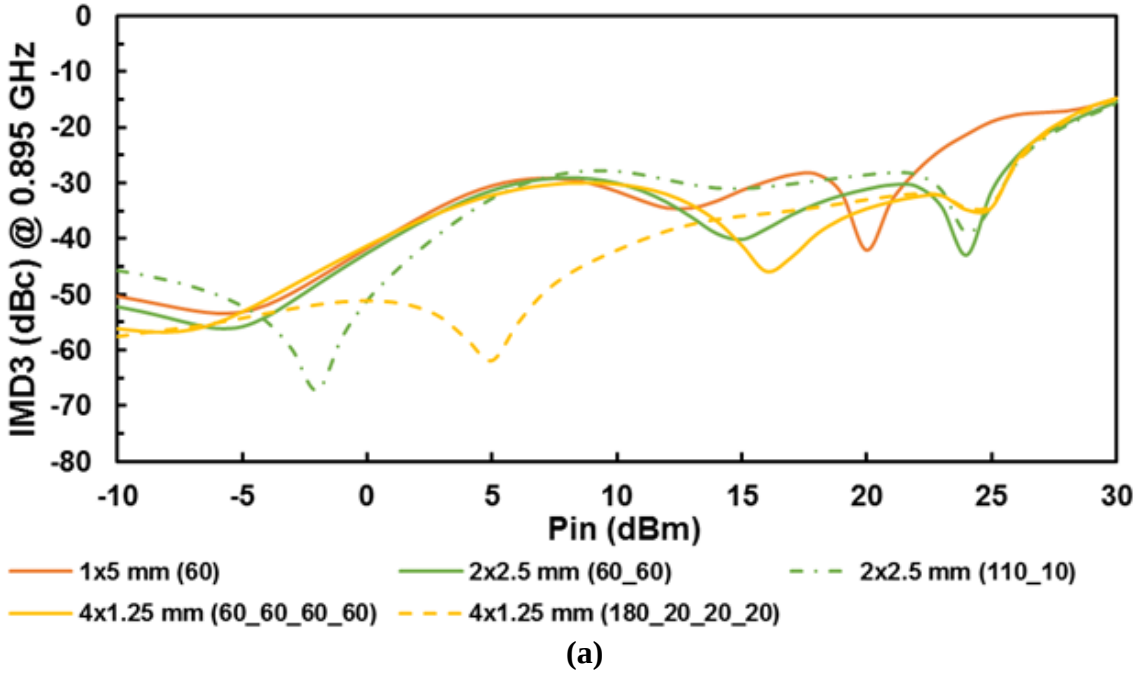


(a)

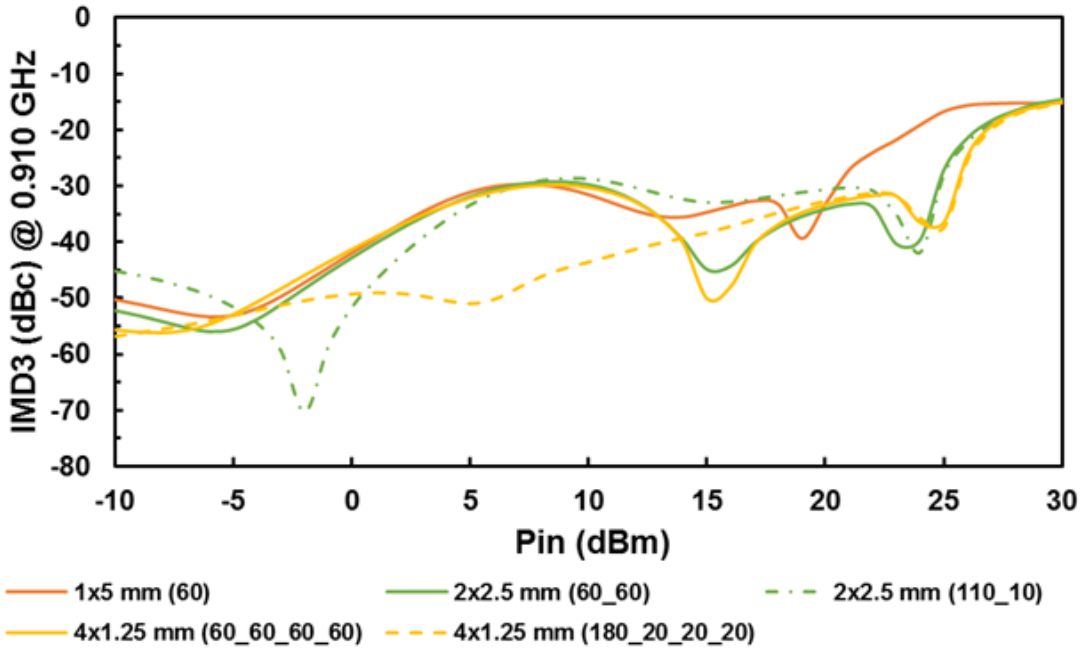


(b)

Fig. 4-17: Case 1: Simulated plot of IMD3 vs. Pin for three circuits: 1 x 5 mm circuit, 2 x 2.5 mm circuit and 4 x 1.25 mm circuit at (a) 0.895 GHz and (b) 0.910 GHz at a total bias current of 40 mA/mm (200 mA for 5 mm). Note: The solid line(s) represents the condition when the FET(s) are biased with the same bias current and dashed represent when the bias current is varied in FET(s). The sum total is kept the same (200 mA in this case).



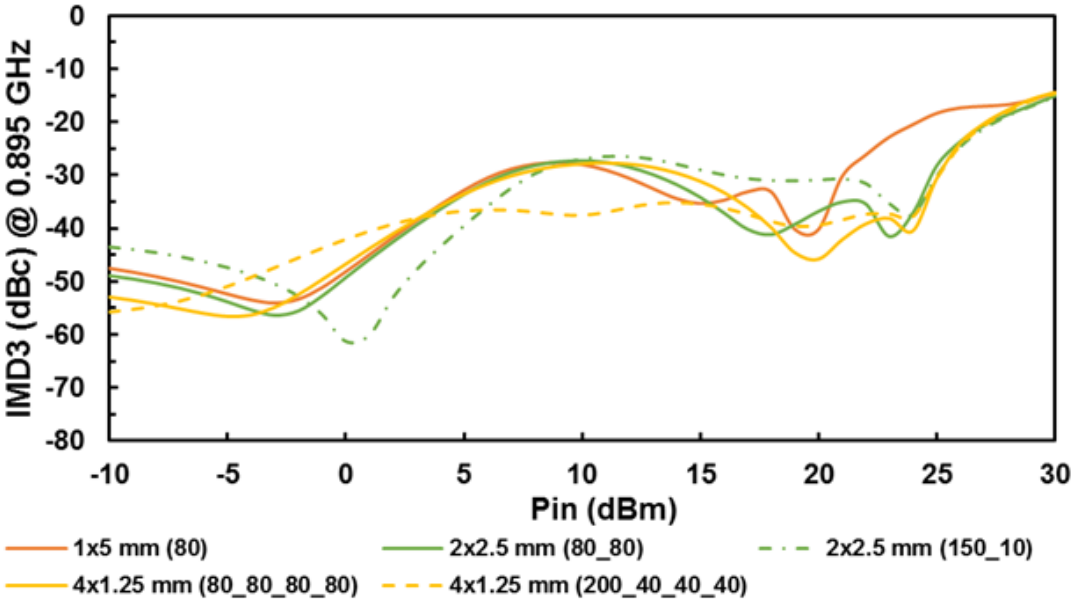
(a)



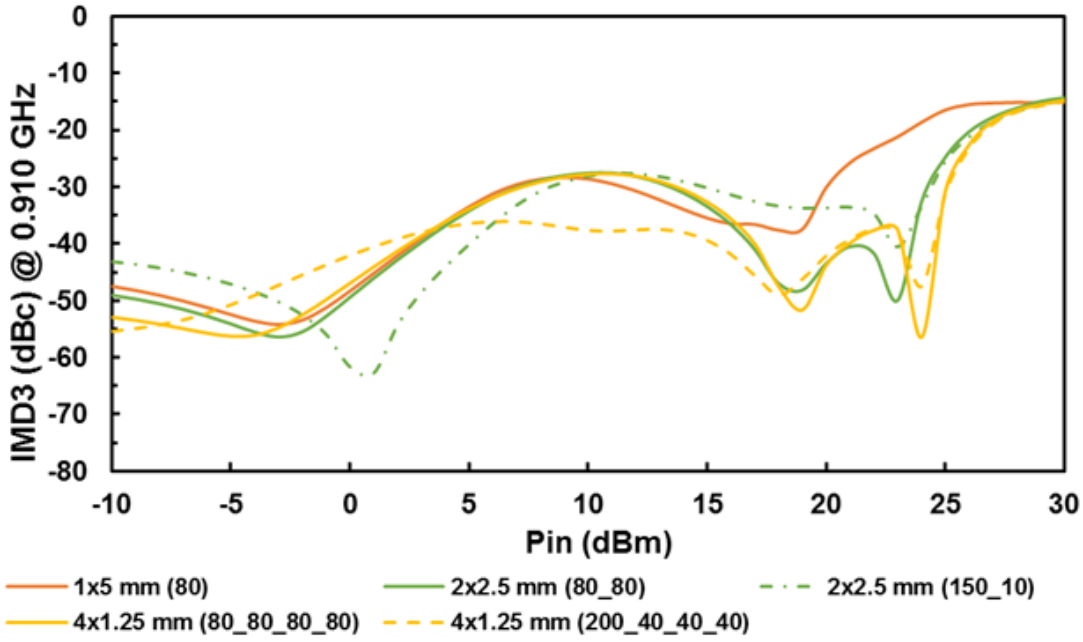
(b)

Fig. 4-18: Case 2: Simulated plot of IMD3 vs. Pin for the three circuits: 1 x 5 mm circuit, 2 x 2.5 mm circuit and 4 x 1.25 mm circuit at (a) 0.895 GHz and (b) 0.910 GHz at total bias current of 60 mA/mm (300 mA for 5 mm).

In case 2, it is also seen that by varying the bias of the 4 x 1.25 mm FET circuit, the improvement in linearity is about 20-30 dBc which is much higher than varying the bias of 2 x 2.5 mm circuit (narrowband improvement).



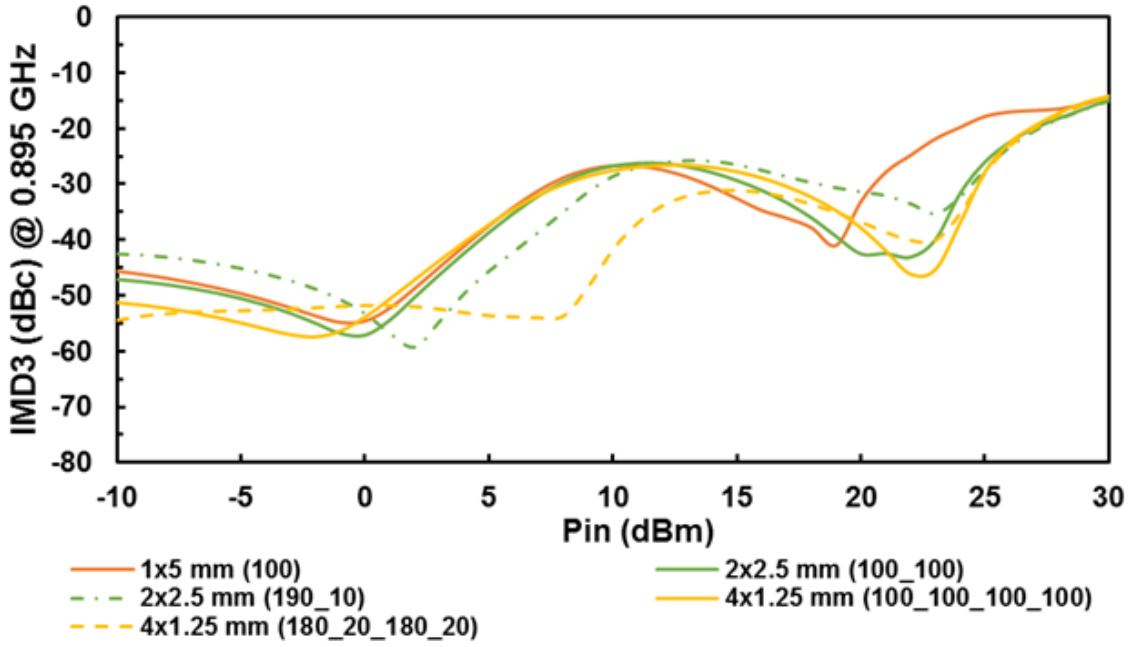
(a)



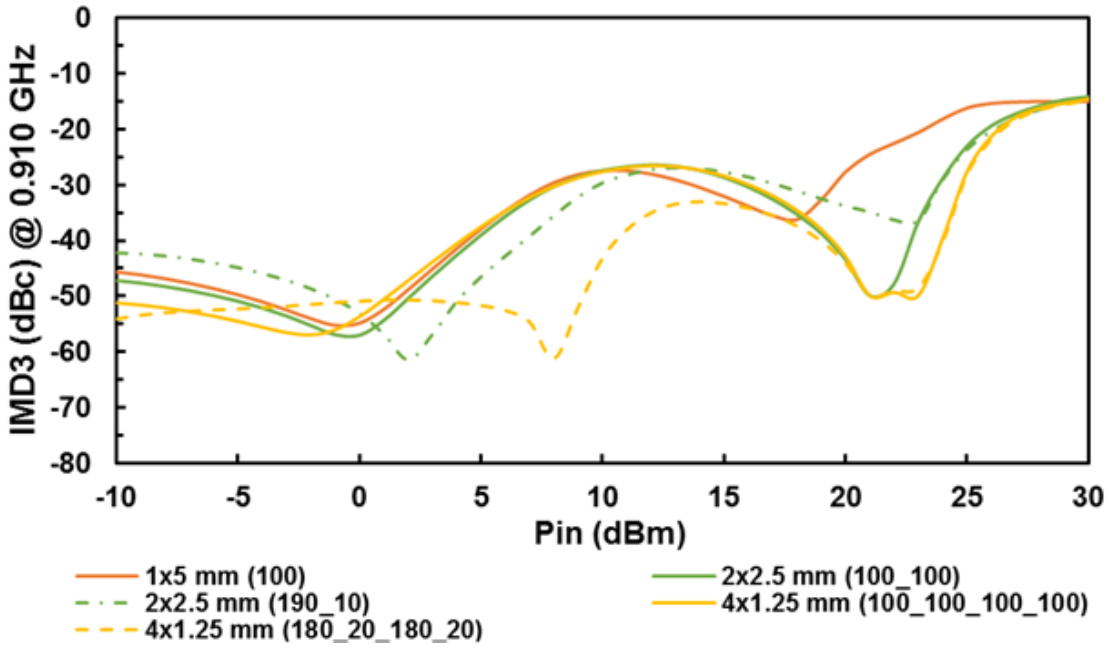
(b)

Fig. 4-19: Case 3: Simulated plot of IMD3 vs. Pin for the three circuits: 1 x 5 mm circuit, 2 x 2.5 mm circuit and 4 x 1.25 mm circuit at (a) 0.895 GHz and (b) 0.910 GHz at a total bias current of 80 mA/mm (400 mA for 5 mm).

Similarly, for **cases 3, 4, and 5**, by applying the different bias values for 4 x 1.25 mm circuit, improvement can be seen. This is illustrated in Fig. 4-19, Fig. 4-20 and Fig. 4-21 for the total bias currents of 80 mA/mm, 100 mA/mm and 120 mA/mm respectively.

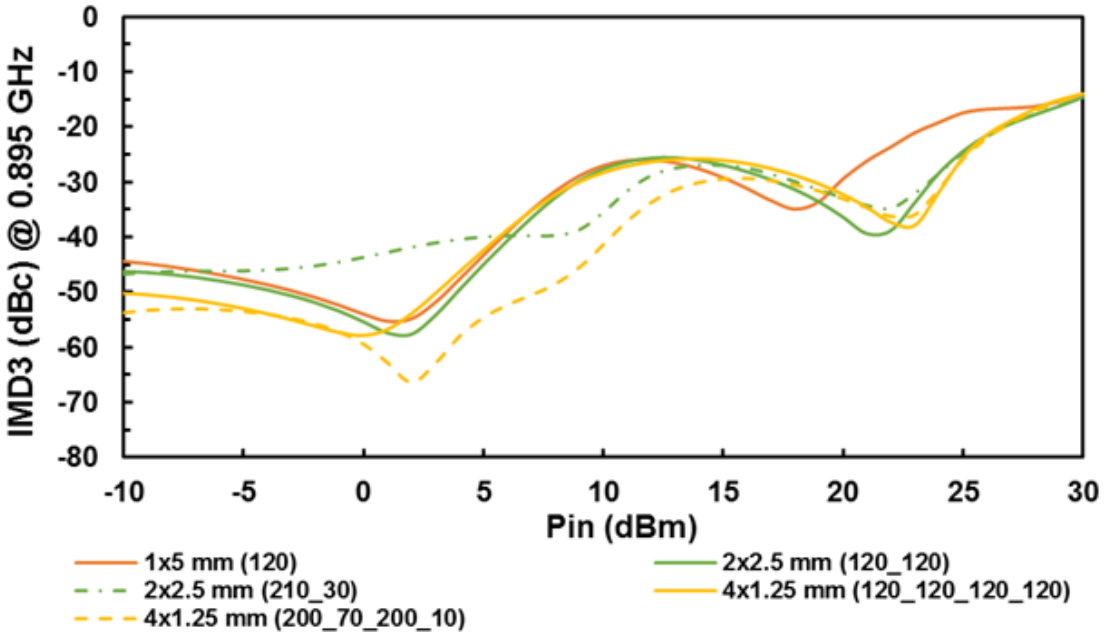


(a)

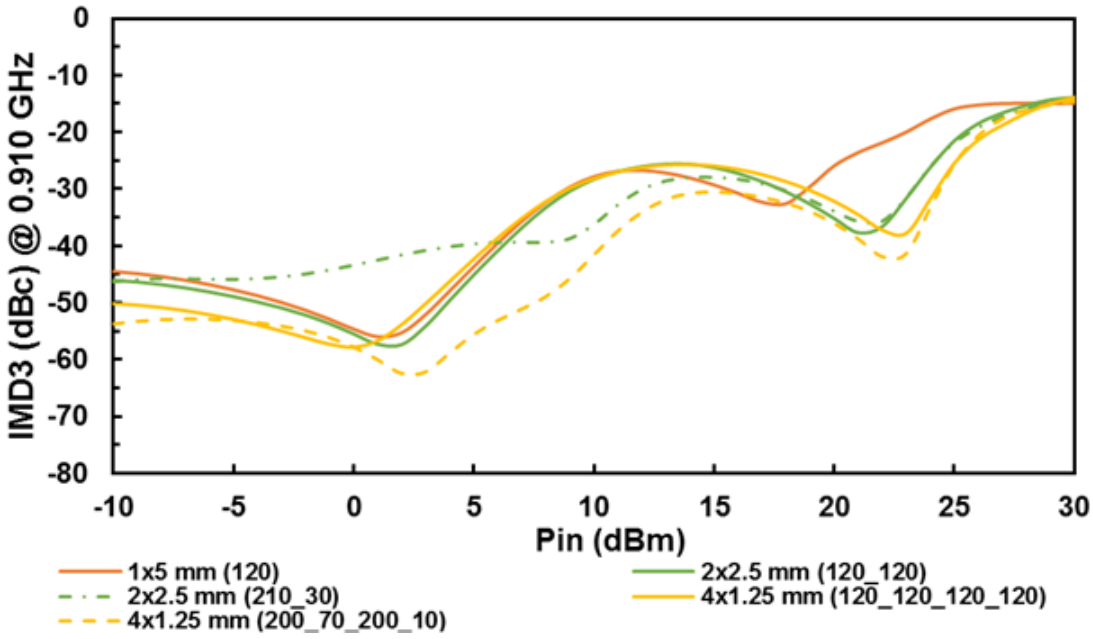


(b)

Fig. 4-20: Case 4: Simulated plot of IMD3 vs. Pin for the three circuits: 1 x 5 mm circuit, 2 x 2.5 mm circuit and 4 x 1.25 mm circuit at (a) 0.895 GHz and (b) 0.910 GHz at a total bias current of 100 mA/mm (500 mA for 5 mm).



(a)



(b)

Fig. 4-21: Case 5: Simulated plot of IMD3 vs. Pin for the three circuits: 1 x 5 mm circuit, 2 x 2.5 mm circuit and 4 x 1.25 mm circuit at (a) 0.895 GHz and (b) 0.910 GHz at a total bias current of 120 mA/mm (600 mA for 5 mm).

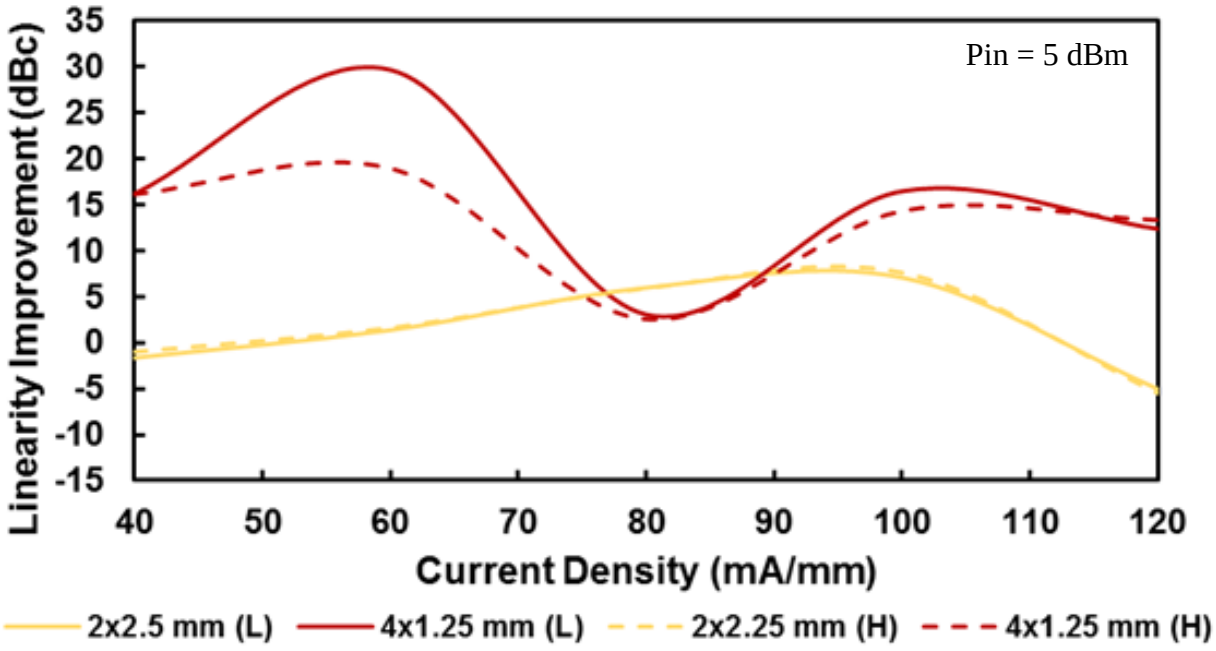
4.5.4 Summary of Improvement in Linearity for Different Bias Values

The plots in section 4.5.3 are summarized in Fig. 4-22. A comparison is made between the two circuits: using two parallel and four parallel FETs (2 x 2.5 mm and 4 x 1.25 mm) for linearity performance improvement. This exploration was done for both the higher (solid) and the lower (dashed) intermod levels and at input power of 5 dBm (Fig. 4-22(a) and input power of 15 dBm (Fig. 4-22(b)). It can be seen from Fig. 4-22(a) that the improvement by using two parallel FETs (2 x 2.5 mm, (yellow)) ranges between 0 - 5 dBc. The improvement in linearity obtained by changing the bias values for 4 x 1.25 mm is more than 20 dBc for the bias current range between 40 - 60 mA/mm and up to 15 dBc for the bias current range of 110 – 120 mA/mm. For higher power levels (Fig. 4-22(b), it can be seen that the linearity improvement by two parallel FETs is negligible and the linearity improvement by the four parallel FETs is between 0 - 5 dBc. Phase cancellation is more easily achieved with four parallel FETs than with two parallel FETs due to the additional degrees of freedom.

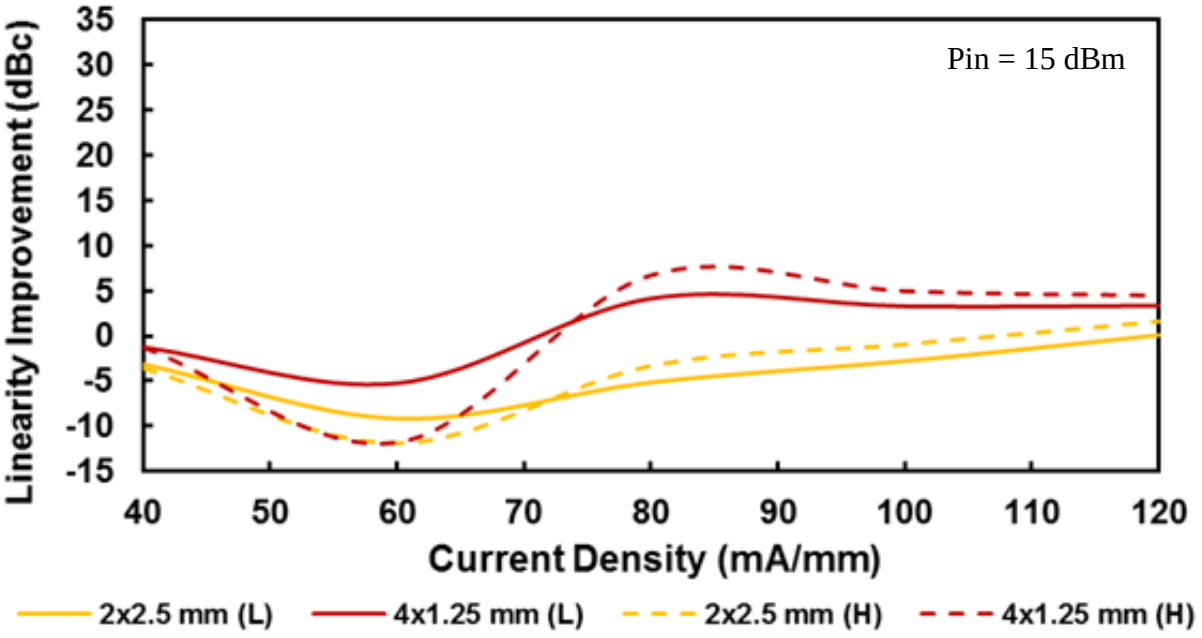
Improvement in linearization by leveraging IMD sweet spots has been discussed in the literature for CMOS-based power amplifiers [48]–[52]. On the other hand, the technique of using multiple parallel FETs and biasing them separately presented here is similar to feedforward linearization. The parallel (FETs) which generate IMD3 components out of phase compared with the first FET. These lead to the cancellation at the output and improvement in linearity.

4.6 Measurement Results

Fig. 4-23 shows the picture of three prototype assembled circuits. IMD3 vs. Pin was measured for 4 x 1.25 mm FET circuit using a two-tone signal with 5 MHz spacing at the center frequency of 0.9 GHz. The IMD3 was measured with power sweeps up to P2 dB compression point, i.e., when the output power of the amplifier with two-tone input signal deviates by 2 dB from the ideal linear characteristic. The IMD3 vs. Pin is plotted in Fig. 4-24(a) for the lower intermod (0.895 GHz) and Fig. 4-24(b) for the higher intermod (0.910 GHz), respectively. It was found that IMD3 improves by 20 dBc in the input power range of 15 dBm – 17 dBm with bias condition 180_20_20_20 (grey curve) and at 6 dBm with bias condition of 110_10_110_10 (yellow curve) compared with the baseline condition of 60_60_60_60 (black). The bias condition of 150_30_30_30 also shows improvement by about 10 dBm in the mid-power region of 15 – 17 dBm.



(a)



(b)

Fig. 4-22: Improvement in linearity for the different bias values (mA/mm) for 4 x 1.25 mm and 2 x 2.5 mm circuit for the power levels of (a) 5 dBm and (b) 15 dBm.

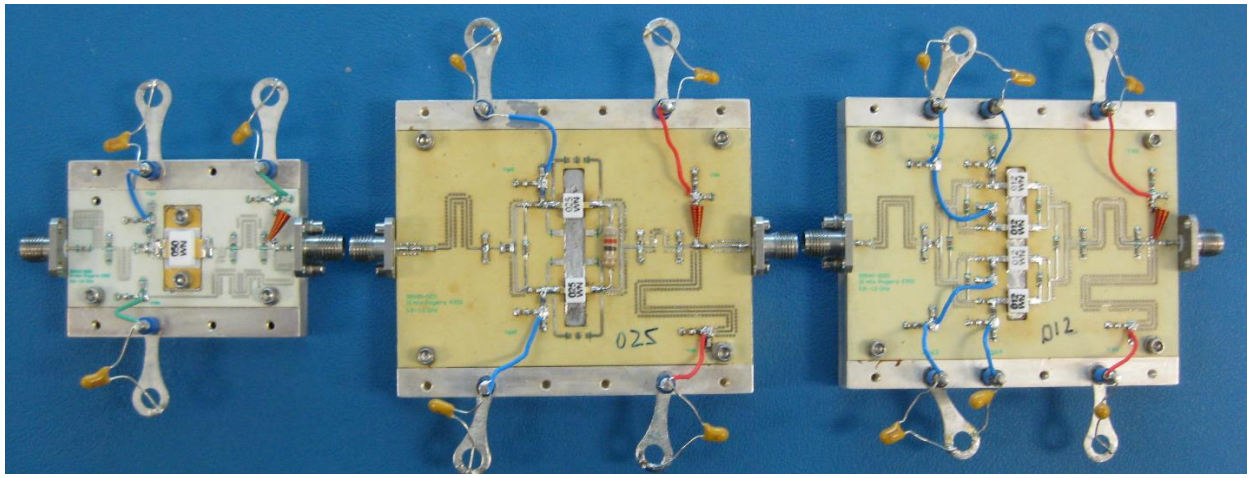
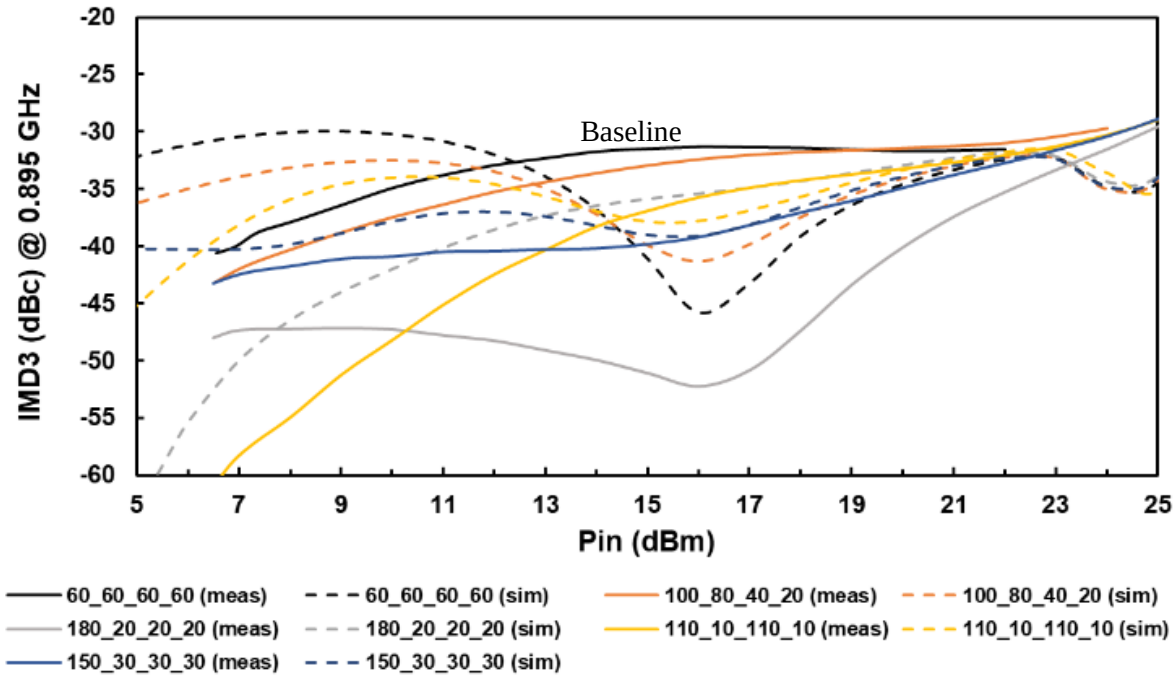
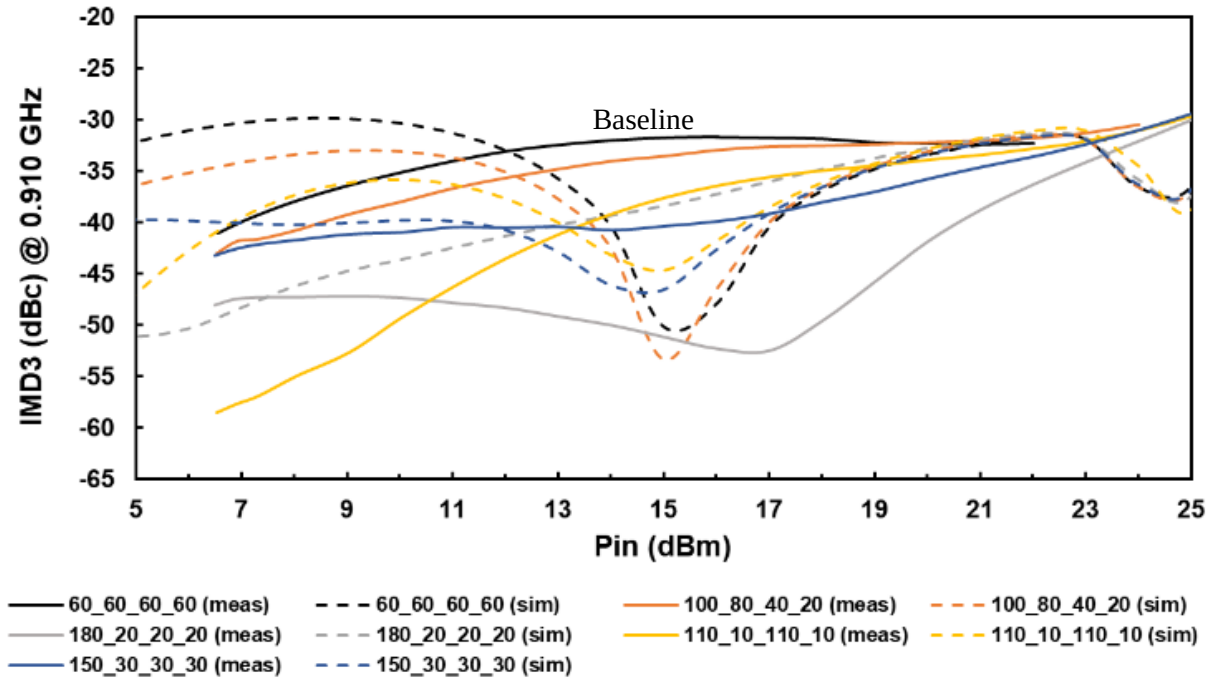


Fig. 4-23: Picture of three prototype assembled circuits using a single FET (size 5 mm), two parallel FETs (size 2.5 mm each), four parallel FETs (size 1.25 mm each) on PCB mounted on test fixtures.



(a)



(b)

Fig. 4-24: Comparison of measured and simulated IMD3 (dBc) vs. Pin (dBm) at different bias values for 4 x 1.25 mm circuit at frequency (a) 0.895 GHz (b) 0.910 GHz.

Because of the lack of accurate foundry PDK models for large-signal operation, the measured results (solid) do not match well with the simulated results (dashed). Improving the large-signal device modeling to achieve better agreement with the measured results was beyond the scope of this work. However, the results show a similar trend which is by varying the bias values, the improvements in IMD3, and hence in linearity can be obtained.

4.6.1 Measurement Results Summary

Fig. 4-25 shows the comparison of the measured vs. simulated results for linearity performance improvement at Pin = 5 dBm for both 2 x 2.5 mm circuit and 4 x 1.25 mm circuit. For simulated results, ‘sim’ keyword is mentioned in the legend. Both measured and simulated results match at the lower power levels. However, these results deviate from each other at higher power levels, as shown in Fig. 4-26. This drives the need for the development of better nonlinear models for this GaN FET technology. Nonetheless, linearity improvement of up to 25 dB is seen at both lower and higher input power levels.

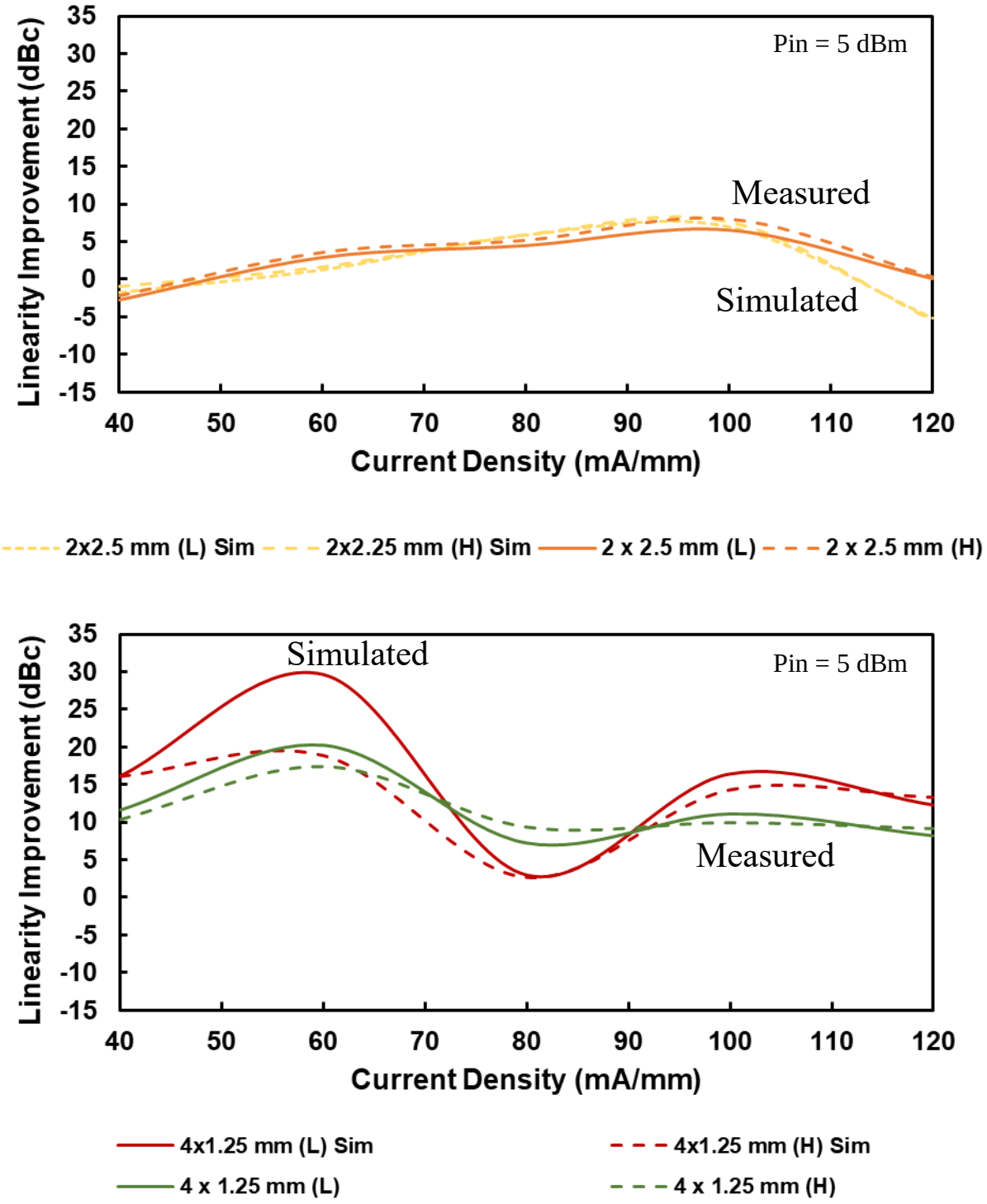
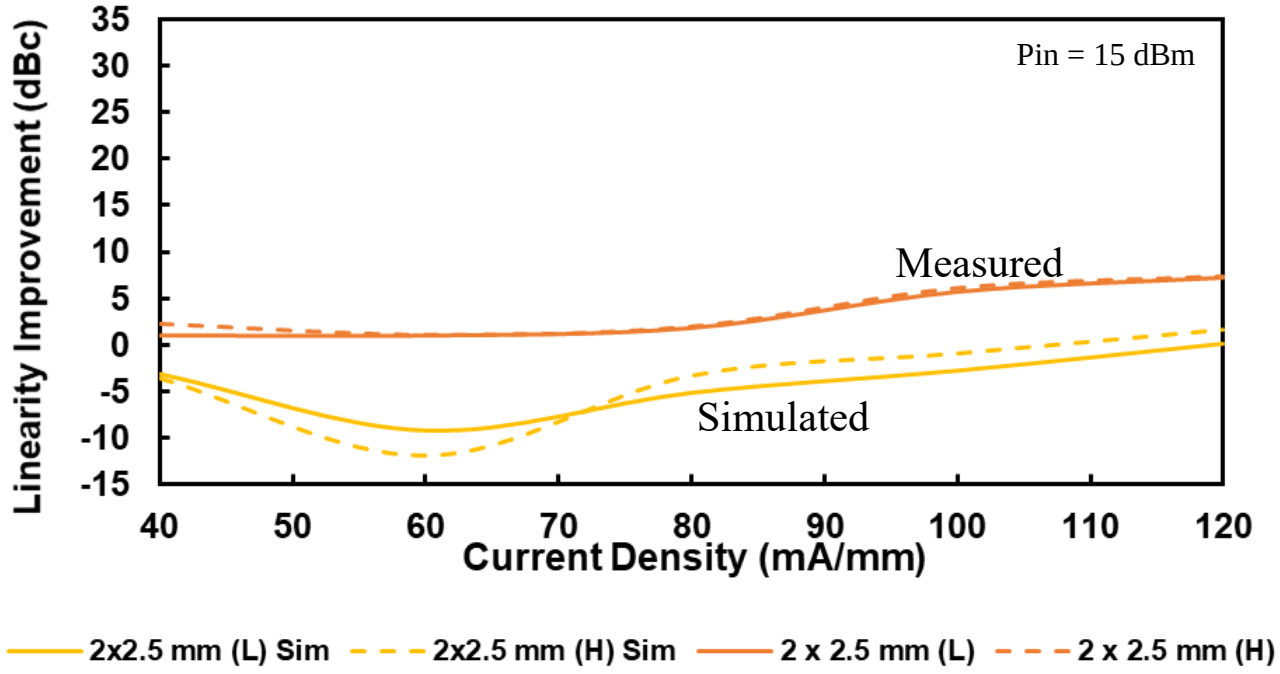


Fig. 4-25 : Comparison of measured and simulated results for linearity improvement for various current densities at Pin = 5 dBm (a) for 2 x 2.5 mm circuit, (b) for 4 x 1.25 mm circuit.



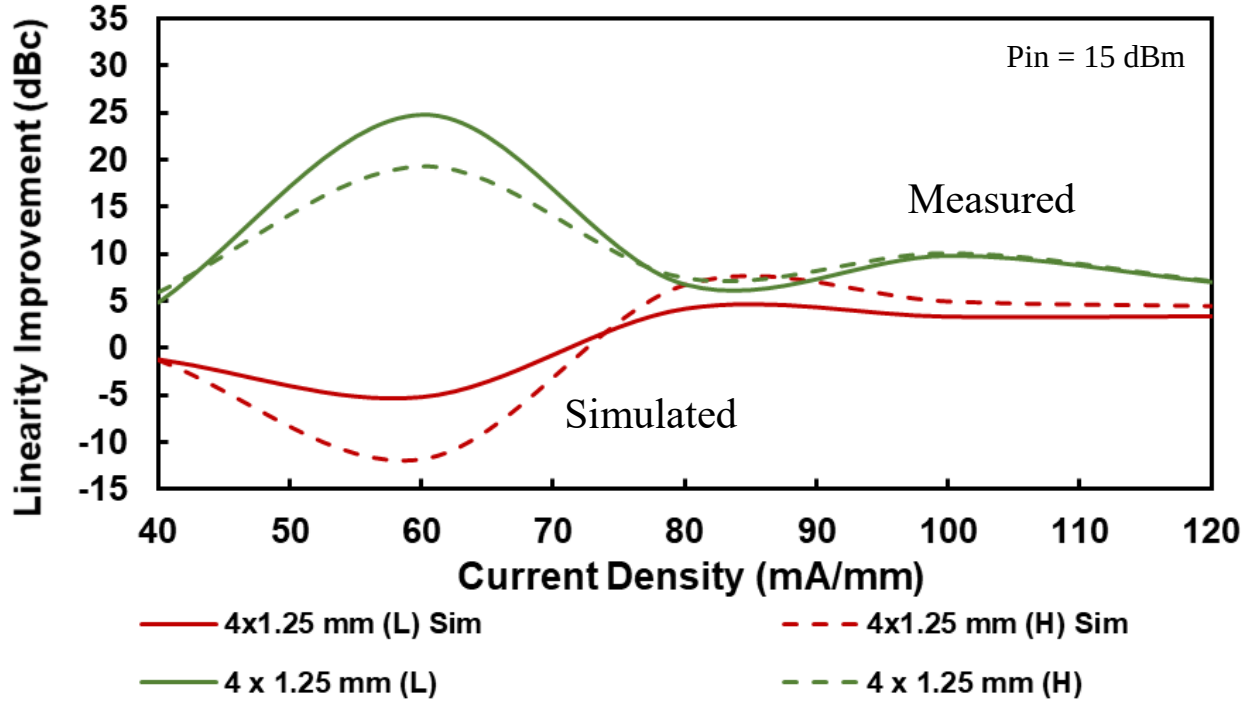


Fig. 4-26 : Comparison of measured and simulated results for linearity improvement for various current densities at Pin =15 dBm (a) for 2 x 2.5 mm circuit, (b) for 4 x 1.25 mm circuit.

Table 4-1 provides a comparison of the work with various PA linearized with other state-of-the-art analog techniques [31], [50]–[52], [54]–[59]. The measurement results show improvement by 20 dBc for 0.9 GHz for GaN HEMT circuit using multi gates devices for four parallel FETs. The proposed technique using a hybrid implementation gives higher output power compared with MMIC's. These measurements demonstrate that dividing a single FET into four parallel FETs can lead to a higher improvement in linearity comparable to similar analog circuit-level techniques for linearization.

Table 4-1: Summary of performance and comparison with state-of-the-art linearization techniques.

Ref	**Technology**	**Freq (GHz)**	**Pout (dBm)**	**Max IMD3 improv. (dBc)**	**Method**
[31]	CMOS	0.9	-4.7	6 @ 0.9 GHz	gm linearization
[50]	CMOS	3.7-8.8	19	1 - 11 @ 5 GHz	Multi-gated technique with capacitance compensation
[51]	GaN HEMT	1.9	23	4 @ 1.9 GHz	Diode predistortion
[52]	LDMOS	2.14	40	6 - 18 @ 2.14 GHz	Analog predistortion
[54]	GaN HEMT	0.8-1.0	40	4 @ 0.9 GHz	gm linearization
[55]	GaN HEMT	8 - 10	15 - 25	4 @ 10 GHz	Capacitance compensation
[56]	GaN HEMT	2.4	35	10 @ 2.4 GHz	Analog predistortion
[57]	CMOS	2.4	19.5	11 @ 2.4 GHz	Modified derivative superposition
[58]	HBT	0.88	33.5	10 @ 0.88 GHz	Phase cancellation
[59]	CMOS	5.8	19	6 - 12 @ 5.8 GHz	Analog post linearization
This work	GaN HEMT	0.8 - 1.0	43	20 @ 0.9 GHz	Phase cancellation with Parallel combined FETs

4.7 Summary

In this chapter, it has been demonstrated using large-signal simulations that if a large FET is divided into multiple smaller FETs, such that the total gate periphery is kept the same, high linearity performance can be achieved by optimizing the biases of the individual FETs to generate IMD3 phase cancellation. The phasor IMD3 currents can be observed in simulation with the help of the ideal power sampler element. When one of the FETs is biased in Class AB, and the other FET is biased in deep Class AB mode, cancellation occurs between the IMD3 components leading to improvement in IMD3. Through this method, an improvement in linearity is seen by 20 dBc at the lower power levels and by up to 15 dBc at medium power levels. This has been demonstrated with the help of measurement results for four parallel FETs circuit. IMD3 improvement is seen by about 20 dBc at Pin = 15 dBm and 5 dBm for total bias current of 60 mA/mm for four parallel FETs. Dividing a large FET into four smaller FETs gives a higher degree of freedom and better improvement in linearity. This technique finds practical use in high dynamic range RF amplifier circuits. This method of biasing parallel FETs is simpler, straightforward, and low cost to implement. No additional circuitry is needed.

Chapter 5

Design of a Linearized X-Band GaN Power Amplifier MMIC Using Multiple Parallel FETs

5.1 Introduction and Motivation

The technique of improving the linearity of GaN amplifier using multiple independently biased parallel FETs has been demonstrated in the previous chapters using hybrid circuits. This chapter investigates the implementation of this technique at higher frequencies using a MMIC (Monolithic Microwave Integrated Circuit) design approach. In a MMIC design, all the circuit elements (active and passive) are realized in an integrated form on the same semiconductor substrate [60]. Fig. 5-1 shows an example of GaN MMIC PA [61]. A MMIC implementation of the power amplifier (PA) has the following advantages compared to the hybrid implementation [62].

1. Easier assembly and testing
2. Light weight
3. Smaller Foot Print
4. Broadband performance
5. Circuit design flexibility
6. Higher frequency implementation
7. High volume manufacturing capability
8. Improved reproducibility
9. Improved reliability
10. Radiation hardness

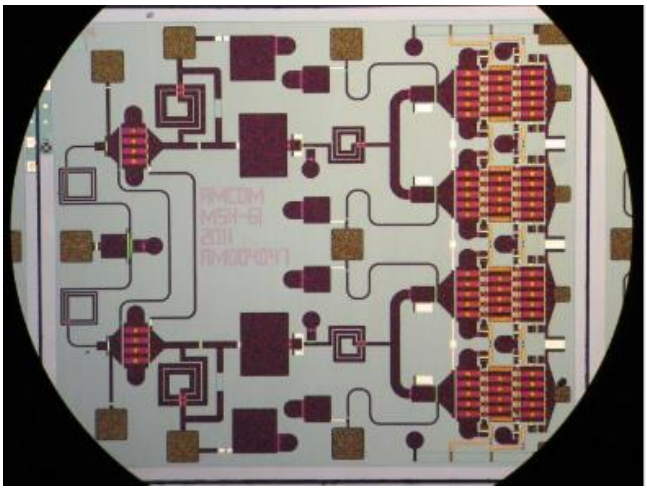


Fig. 5-1: Picture of a GaN MMIC PA as illustrated in [61].

However, MMIC design has longer development time and can incur higher engineering costs. Post manufacture tweaking in the design in order to obtain optimum performance is not possible.

This chapter presents the design and simulation of an X-Band GaN power amplifier MMIC employing the parallel gate technique over the frequency range of 8-10 GHz. In this design, a single FET is divided into four parallel FETs such that the total gate periphery remains the same. Fig. 5.1 shows the block diagram of a single GaN amplifier with gate width W and second amplifier consisting of four parallel FETs each of gate width W/4. The gate bias of each of the parallel FETs is isolated using blocking capacitors C_b. The output of the amplifier is matched to the impedance for the maximum output power from the FET, and the input is matched for the best input return loss and maximum gain [63]. The bias of each of the FETs can be varied to improve linearity performance.

In this MMIC design study, the width W is chosen to be 1 mm, and MMICs with a single FET of size 1 mm (8 x 125 um) and four parallel FETs of size 0.25 um (2 x125 um) are compared. 8 x 125 um FET refers to a device with eight fingers with a unit gate width 125 um. Similarly, 2 x125 um FET refers to a device with two fingers with a unit gate width of 125um. The PDK cells from the foundry are used for the design. There are two types of FET cells in the foundry library: ISV (Individual Source Via) and OSV (Outside Source Via). FETs with ISV structure have individual vias next to each source compared to the OSV structure which has vias at the end of the FET. Fig. 5-3 shows the layout of (a) 2 x 125 um FET (b) 8 x 125 um FET with OSV structure and (c) 8 x 125 um FET with ISV structure. For 2 x 125 um FET, both OSV and ISV configurations are same.

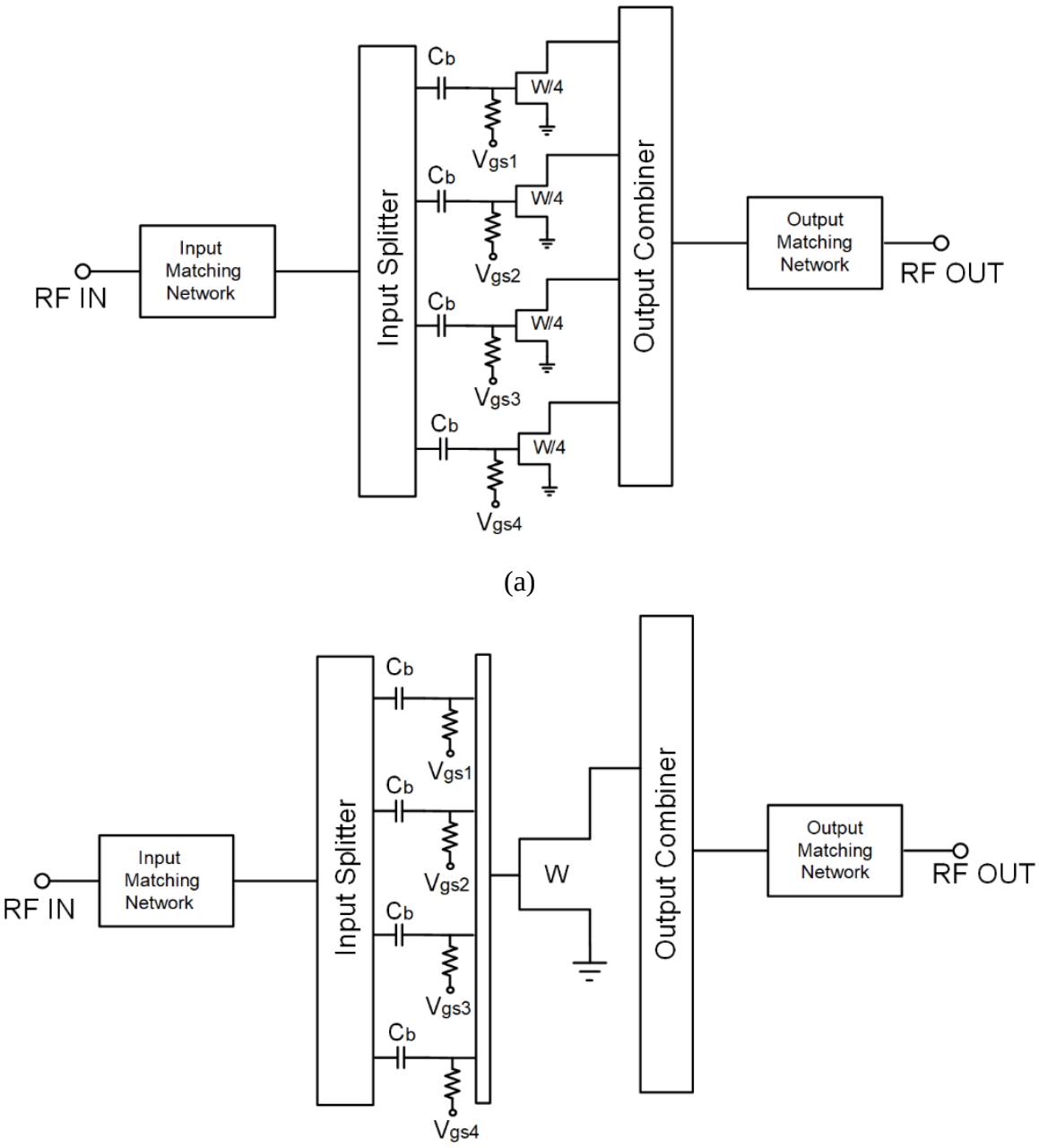


Fig. 5-2: Block Diagram of GaN MMIC PA with (a) a single FET of width W and (b) four parallel FETs of width W/4.

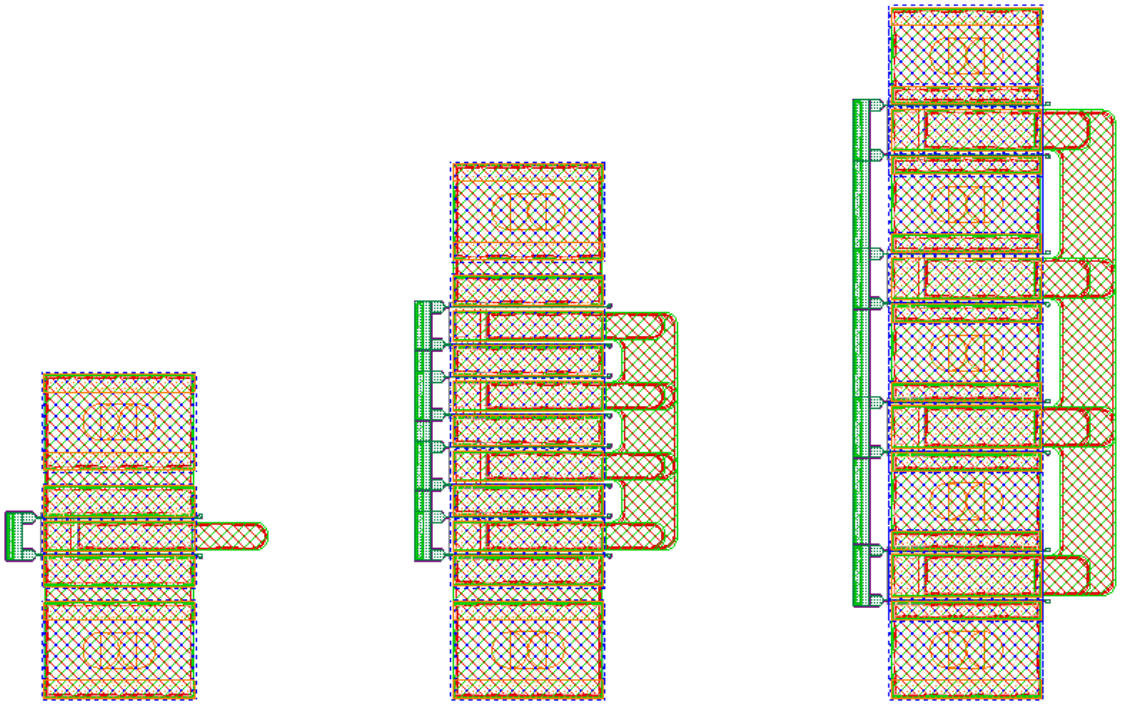


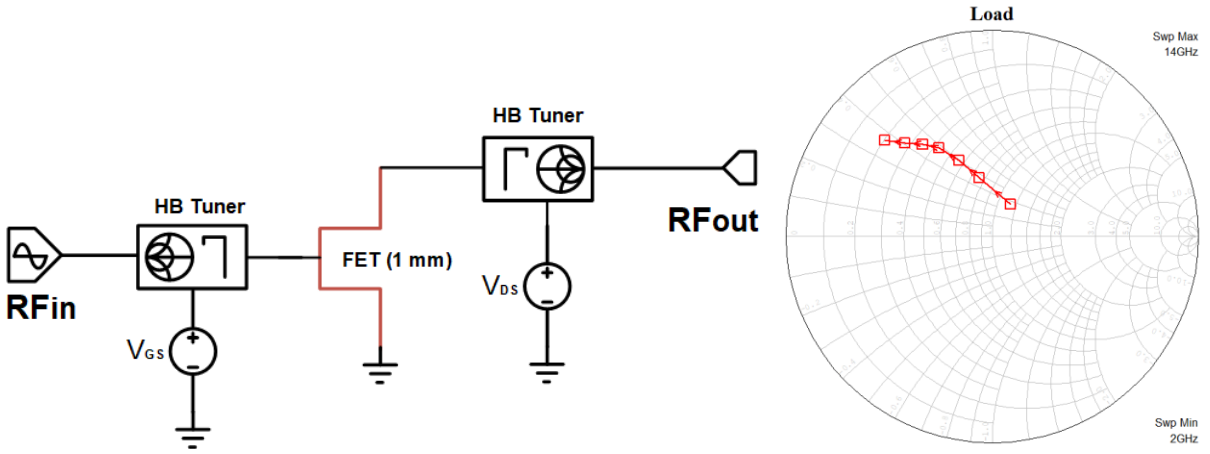
Fig. 5-3: Layout of (a) 2 x 125 um FET (b) 8 x 125 um FET (OSV structure) (c) 8 x 125um FET (ISV structure).

Considering Fig. 5-3, the ISV structure of 8 x 125 FET is chosen to ensure similarity of layout with four parallel independently biased 2 x 125 um FETs.

5.2 Design of GaN Amplifier MMIC Circuit

5.2.1 Load Pull Simulations

A nonlinear foundry based model of the GaN FET of size 1 mm (8 x 125 um) was characterized in AWR microwave office. Harmonic Balance lossless tuners with bias tee (HB tuner) were used to provide different impedances at the output of the FET. Load Pull simulations were done over the frequency range of 2-14 GHz (Fig. 5-4(a)) and the optimum load for best power was computed (Fig. 5-4(b)). This load impedance was used for designing the output matching networks of the two circuits (a) using a single 8 x 125 um FET (b) using four parallel 2 x 125 um FETs. The output network was conjugate matched with the load impedance for obtaining best power. The input network was matched for best input return loss and best gain by placing these as optimizer goals in AWR microwave office software.



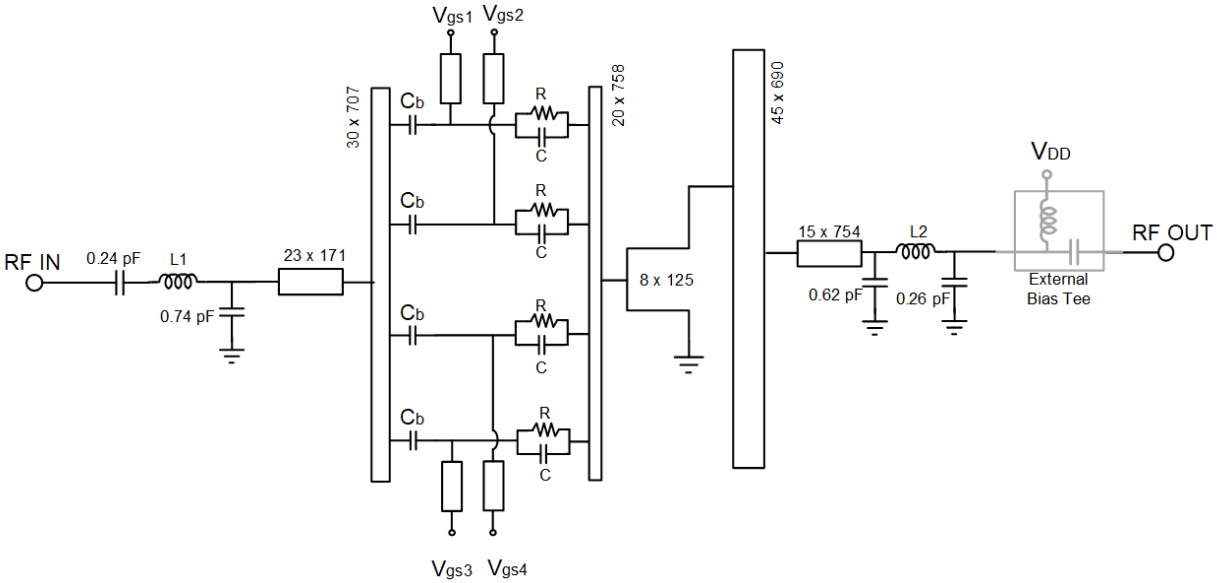
(a) (b)

Fig. 5-4: (a) Load Pull Simulation for 8 x 125 um (1 mm) FET in AWR Microwave office (b) Plot of simulated optimum load impedance on Smith chart for 8 x 125 um FET.

Fig. 5-5 shows the schematic diagram of the two MMIC circuits, one using a single 8 x 125 um FET (Fig. 5-5(a)), and the other using four parallel 2 x 125 um FETs (Fig. 5-5(b)). The input and output matching networks of the two circuits were kept similar to demonstrate improvement in linearity performance by dividing a large single FET in multiple parallel FETs. In Fig. 5-5(a), all the gate bias (V_{gs1} to V_{gs4}) are tied to the same gate voltage. However, in Fig. 5-5(b), all the gates were are at different voltages. Blocking capacitors C_b (0.42 pF) are used to isolate the gate bias voltages for each gate. Resistor parallel to capacitor (R || C, 15 ohm || 0.71 pF) is added to the input matching network for stability purposes. The drain bias is provided externally to the amplifier circuits using an external bias tee. Hence, no blocking capacitor is used in the output network. Input and Output Networks were EM simulated to give optimum performance, as discussed in the EM simulation section.

5.2.2 Layout of the Amplifier Circuits

Fig. 5-6 shows the layout of the amplifier circuits containing (a) a single 8 x 125 um FET (1 x 1 mm circuit) and (b) four parallel 2 x 125 um FET(s) (4 x 0.25 mm circuit). The inset shows the crossover of Metal 1 (green) with an Air-Bridge (red) to ensure that there is no cross-connection between the gate biases of parallel FETs. Four Vgs pads of size 200 x 200 um are used for external probing/bonding to the package. GSG pads of size 150 um x 150 um and pitch 150 um are used for the RF input and output. The cross-sectional area of both MMIC designs is 3.5 x 2 mm^2. The layout meets the design rule specifications set by the foundry service.



(a)

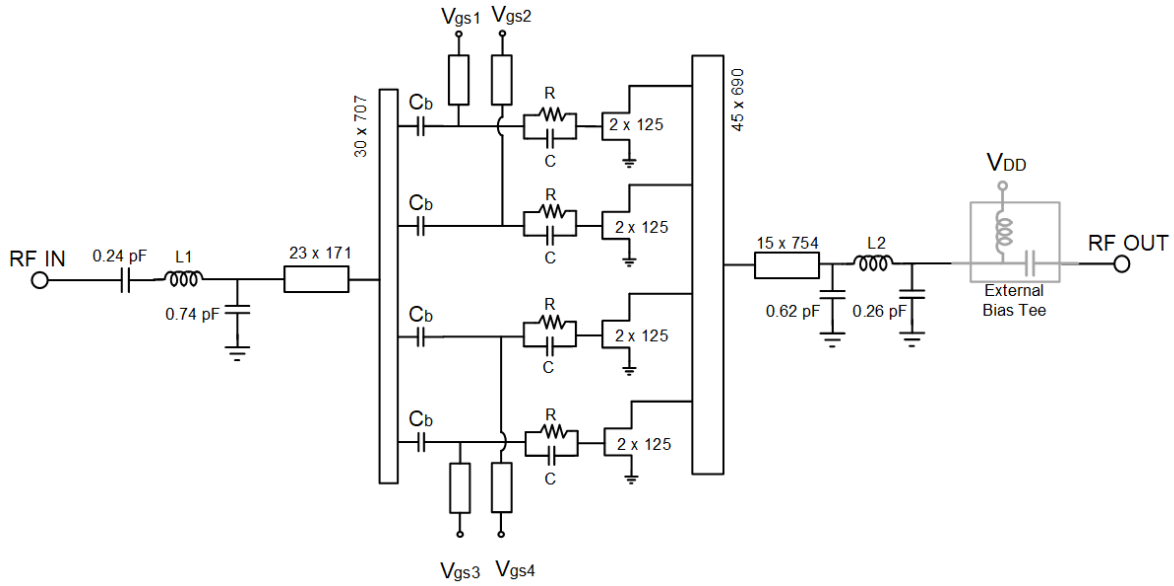
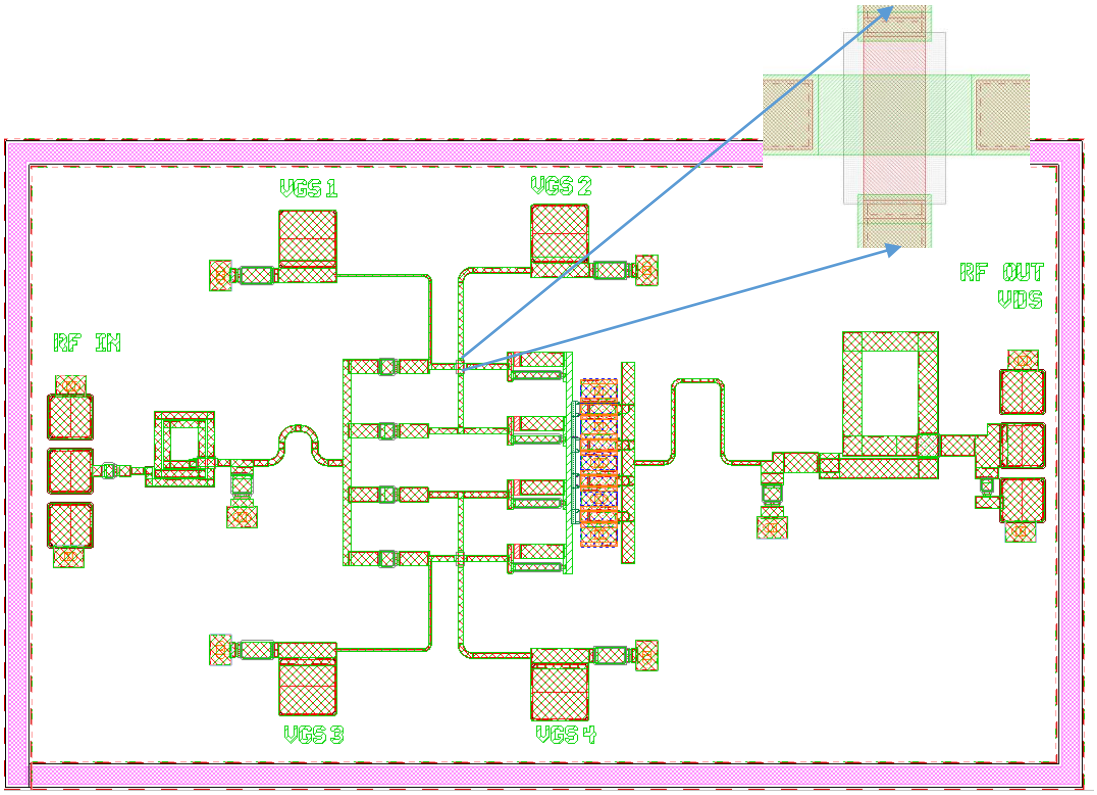
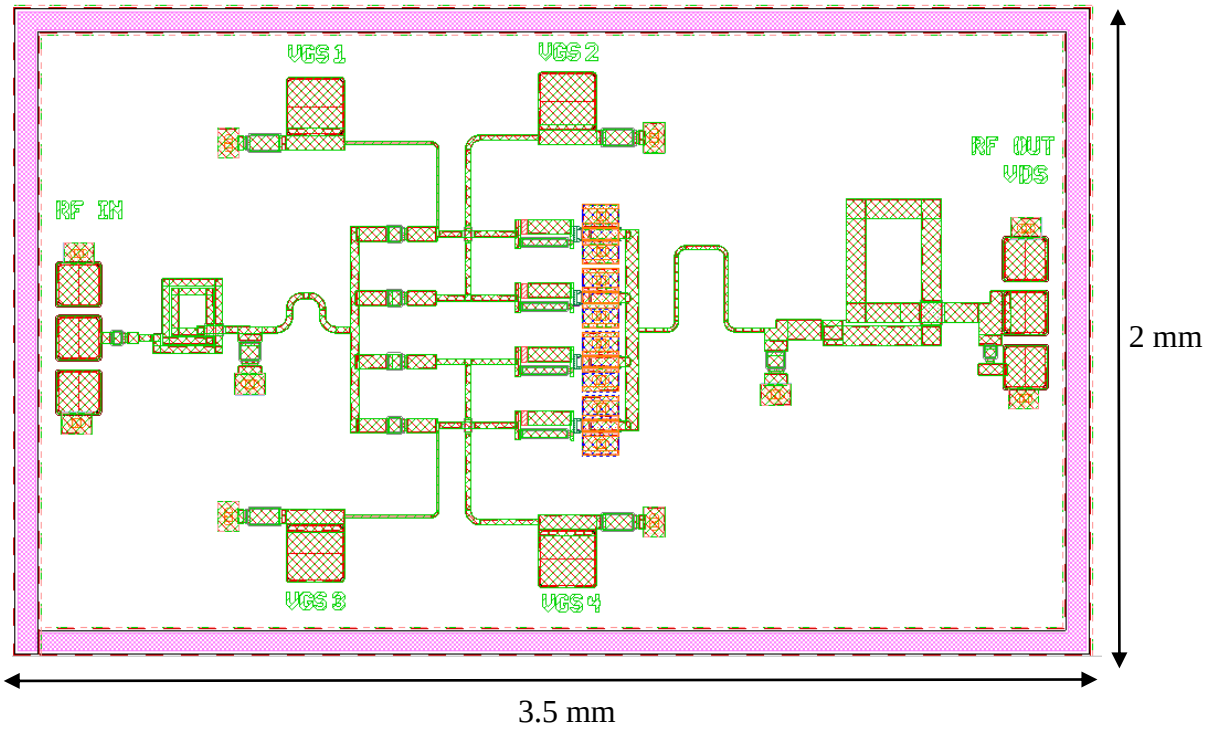


Fig. 5-5: Schematic of X-Band GaN MMIC PAs (a (b) single 8 x 125 FET (b) with four parallel 2 x 125 FETs. Note: all the dimensions (W x L) of the microstrip lines are given in um.



(a)



(b)

Fig. 5-6: Layout of X-Band GaN power amplifier MMIC containing (a) single 8 x 125 FET (1 x 1 mm circuit) (b) four parallel 2 x 125 FETs (4 x 0.25 mm circuit). The inset shows the crossover of the Metal 1 (green) and Air-Bridge (red) in order to separate the gate bias lines. Cross sectional area of MMIC designs is 3.5 x 2 mm^2.

It can be seen from Fig. 5-6 that the input and output matching networks are kept similar to each other for the two MMICs. The first circuit contains an extra transmission line before the input of the FET. This is done in order to tie all the gate bias together. This introduction of transmission line does not cause much difference in S-parameters or Output power of the two circuits as can be seen from graphs in Fig. 5-7, and Fig. 5-8, respectively. Fig. 5-7 shows simulated S-parameter performance of the two amplifier circuits. The solid curves refer to the amplifier circuit containing a single 1 mm (8 x 125 um) FET and the dashed curves refer to the amplifier circuit containing four parallel 0.25 mm (2 x 125 um) FETs. The amplifiers achieve about 15 dB of small-signal gain with input return loss of –15 dB and output return loss of –10 dB in the design frequency of 8-10 GHz. Fig. 5-8 shows simulated plot of power, gain and PAE for the two amplifier circuits at bias current of 150 mA/mm (150 mA for 1 mm gate periphery) at 28 V. As shown in the figure, both the amplifiers show similar performance and achieve output power (Pout) of 36 dBm, gain of 15 dB and PAE of 42%.

5.2.3 EM Circuit Simulations

Electromagnetic simulations of circuits were done using the Microwave Office AXIEM, a 3D Planar EM Analysis Software. The stack up or multi-layer substrate definition for GaN process was provided by the foundry. EM simulation helps to compute the accurate response of the circuit by specifying the exact spacing between the transmission lines as seen in the layout in Fig. 5-6. It is not possible to define spacing when using PDK components library components in the schematic: only length and width of the microstrip lines can be specified.

5.2.3.1 EM Simulation of the Inductor

Fig. 5-9(a) shows the schematic of the inductor used for the input in an EM simulation environment. Quality factor is used to measure the quality of inductors. Higher the Q, more closely the inductor approaches the behavior of ideal inductor. The Quality factor (Q) of the inductor is given by

$$Q = \frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} = \frac{\omega L}{R} \qquad (1)$$

From the simulation results as shown in Fig. 5-9(b), the inductor has a Q factor of 30 with inductance of 1.4 nH in the design frequency range of 8-10 GHz.

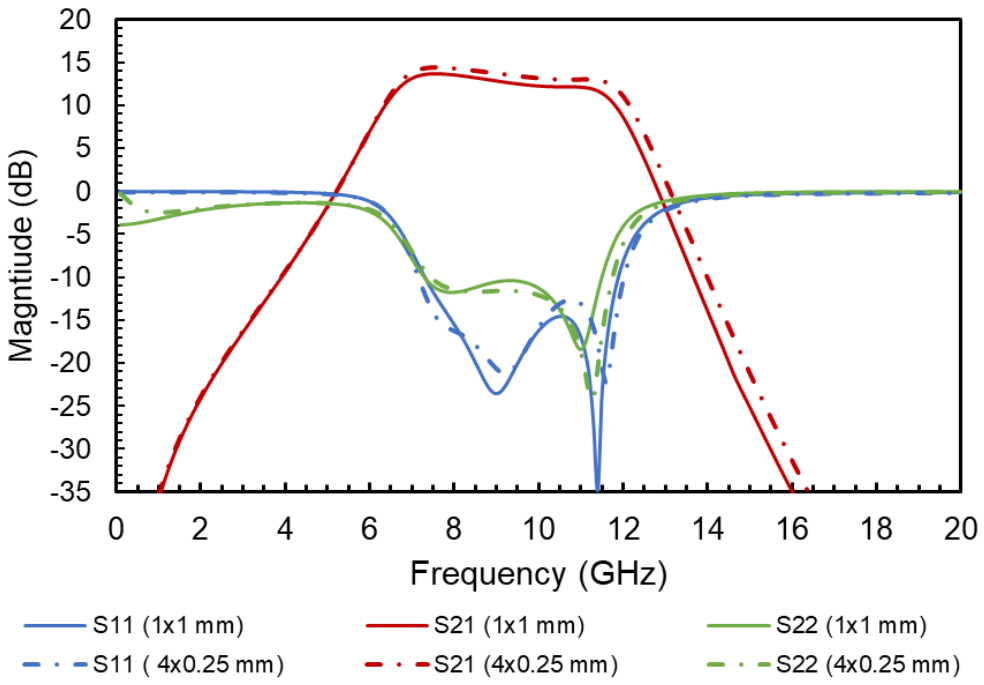


Fig. 5-7: Simulated S parameters for 1 x 1 mm and 4 x 0.25 mm amplifier circuits.

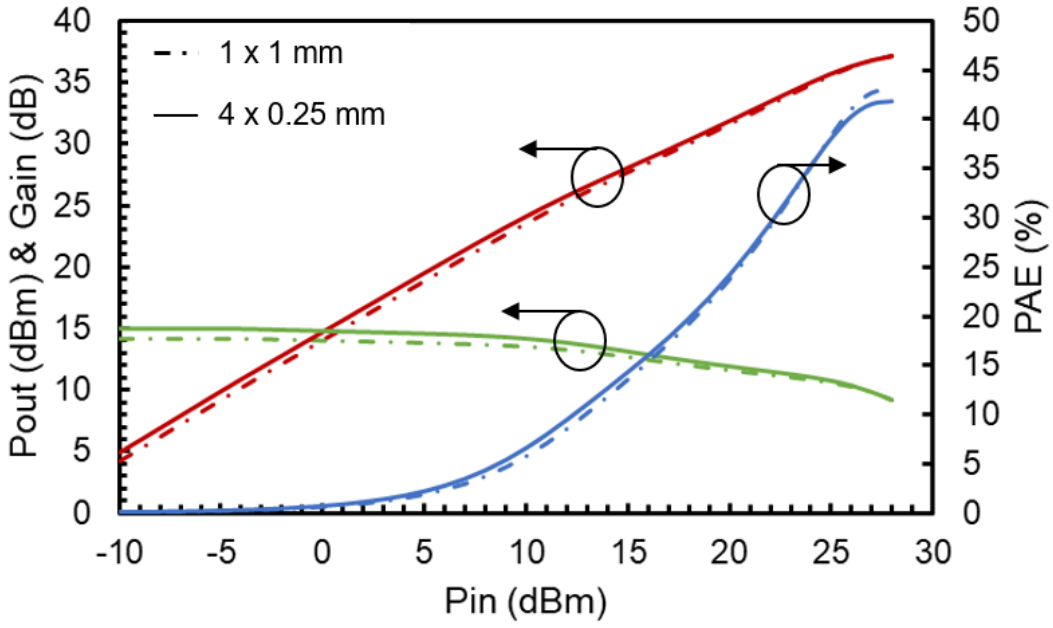
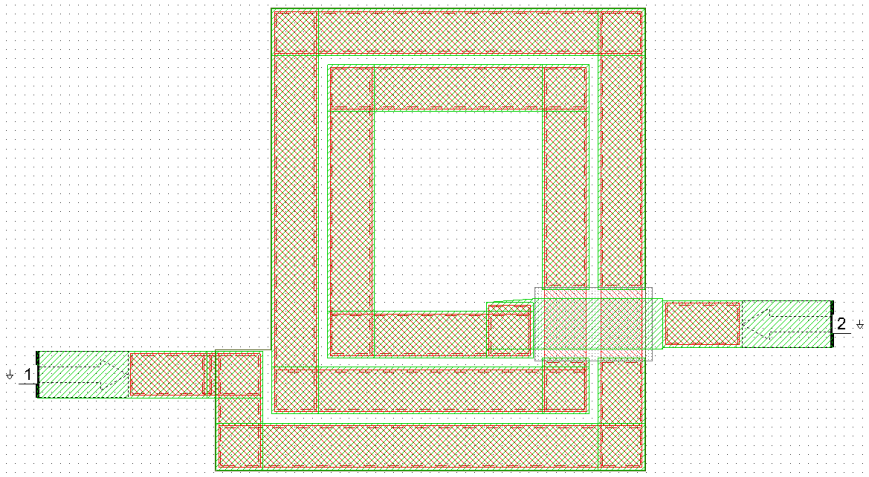
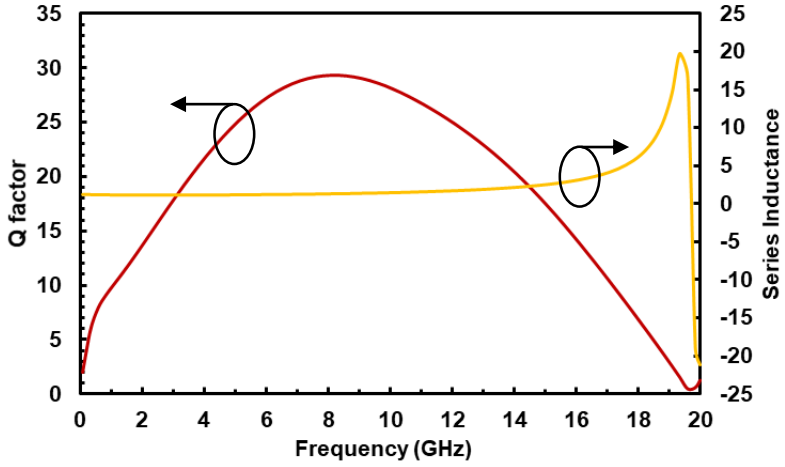


Fig. 5-8: Simulated plot of Output Power (Pout), Gain and PAE w.r.t input power (Pin) for 1 x 1 mm and 4 x 0.25 mm amplifier circuits.



(a)



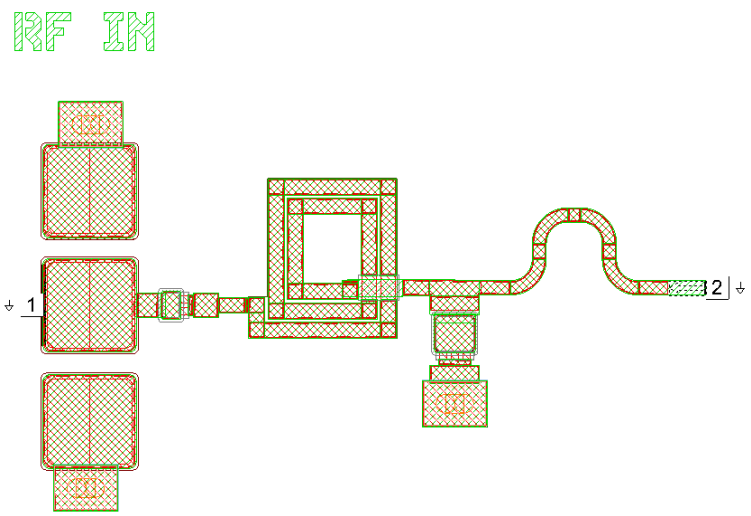
(b)

Fig. 5-9: (a) Schematic of the input inductor used for EM Simulation, (b) Plot of the Q factor and the effective series inductance from the simulation results.

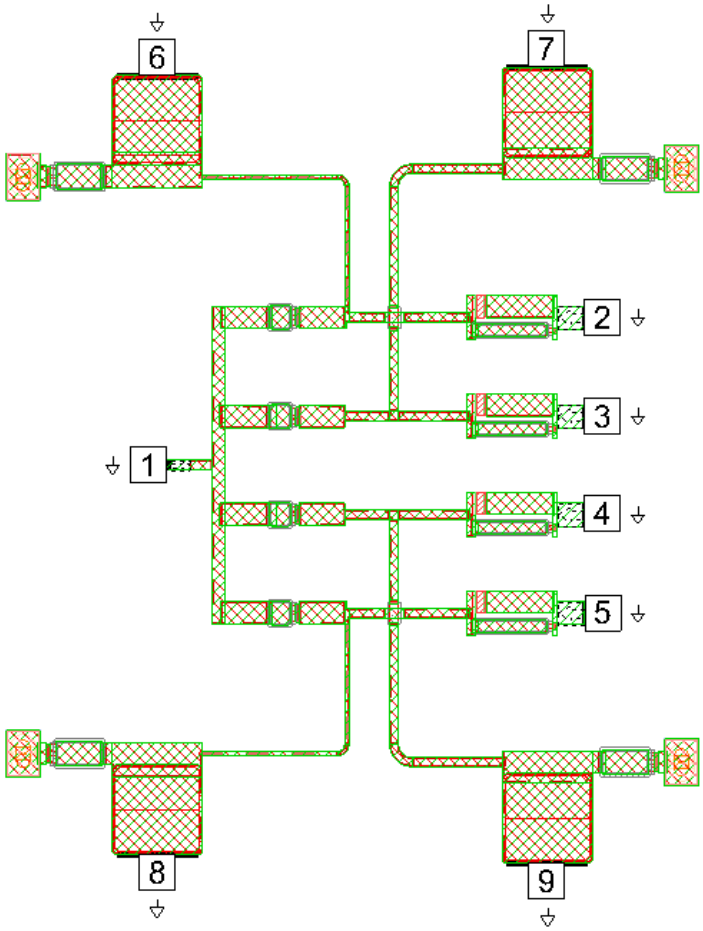
5.2.3.2 EM Simulation of the Input Matching Network

EM-based simulation for the amplifier was done by simulating the input and the output matching networks separately and combining their simulated S parameters.

Fig. 5-10 shows the division of the input network circuit in two parts: Part 1 and Part 2. In the second part, ports 2 to 5 are the inputs of the parallel FETs. Ports 6 and 9 are the gate bias of FET's. The results of the EM Simulation of the input circuit was combined in two parts and input return loss (S11) was plotted. Fig. 5-11 shows the comparison of the S-parameter with EM simulation and using PDK components in the schematic. The results match well with each other.



(a)



(b)

Fig. 5-10: Schematic of the EM simulation of the input matching network in two parts : (a) Part 1 (b) Part 2.

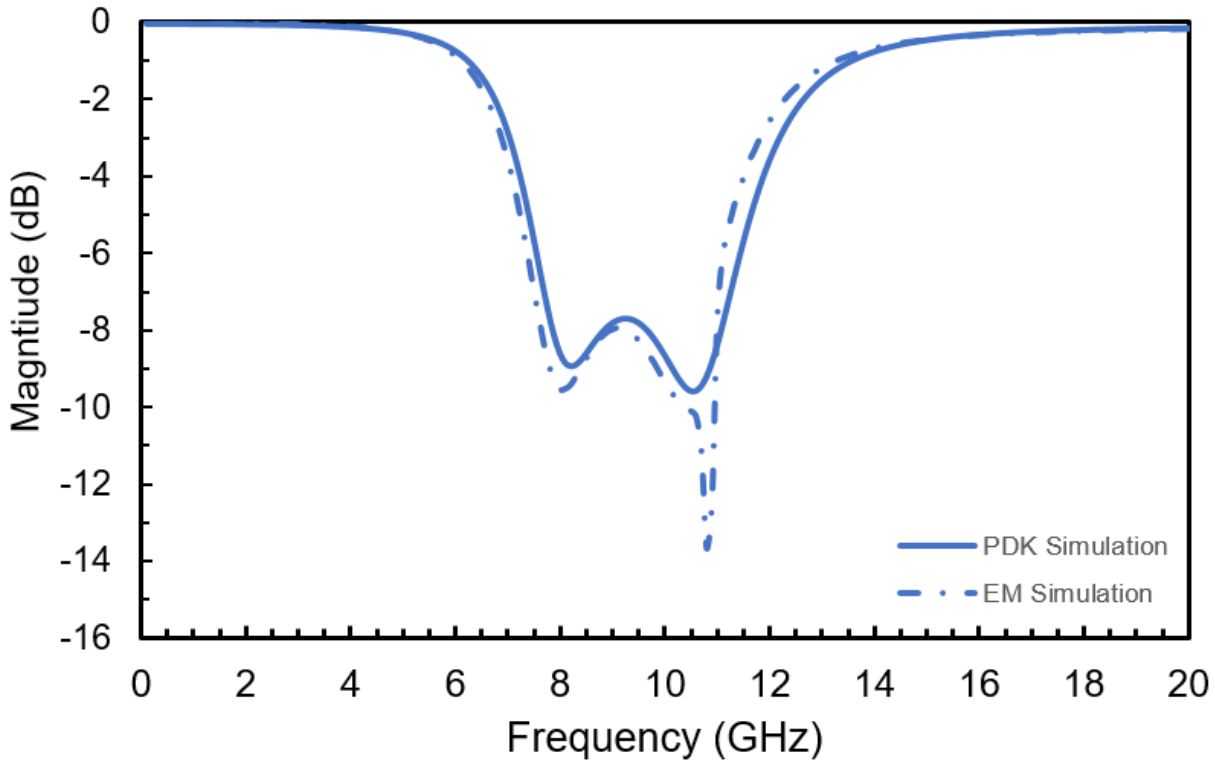


Fig. 5-11: Comparison of EM simulation with PDK simulation results for the input matching network (s11).

5.2.3.3: EM Simulation of the Output Matching Network

Fig. 5-12 shows the schematic of the output network for EM simulation. The first four ports are the output from a single large FET (8 x 125 um) or from four parallel FETs (2 x 125 um each).

Fig. 5-13 shows the EM simulation results of the output circuit. The solid lines refer to the simulation results obtained using PDK components and dashed are the EM simulations.

Fig. 5-14 shows the EM simulation of the amplifier circuit compared with the simulation done using PDK library components. The S-parameters are reasonably matched in the frequency range from 8-10 GHz.

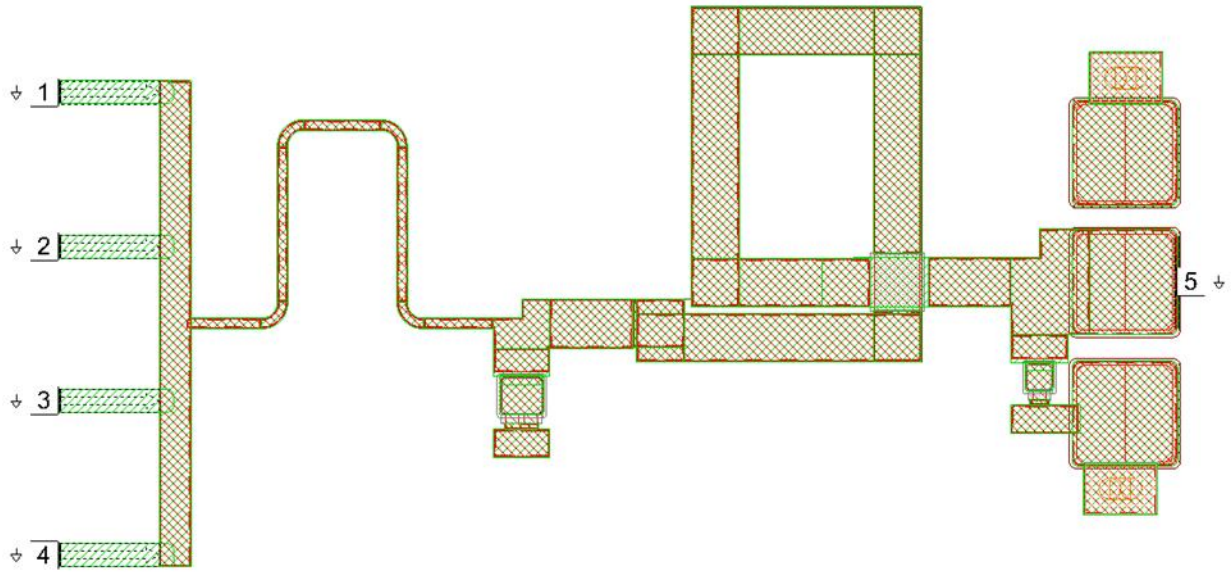


Fig. 5-12: Schematic of EM simulation of the output matching network.

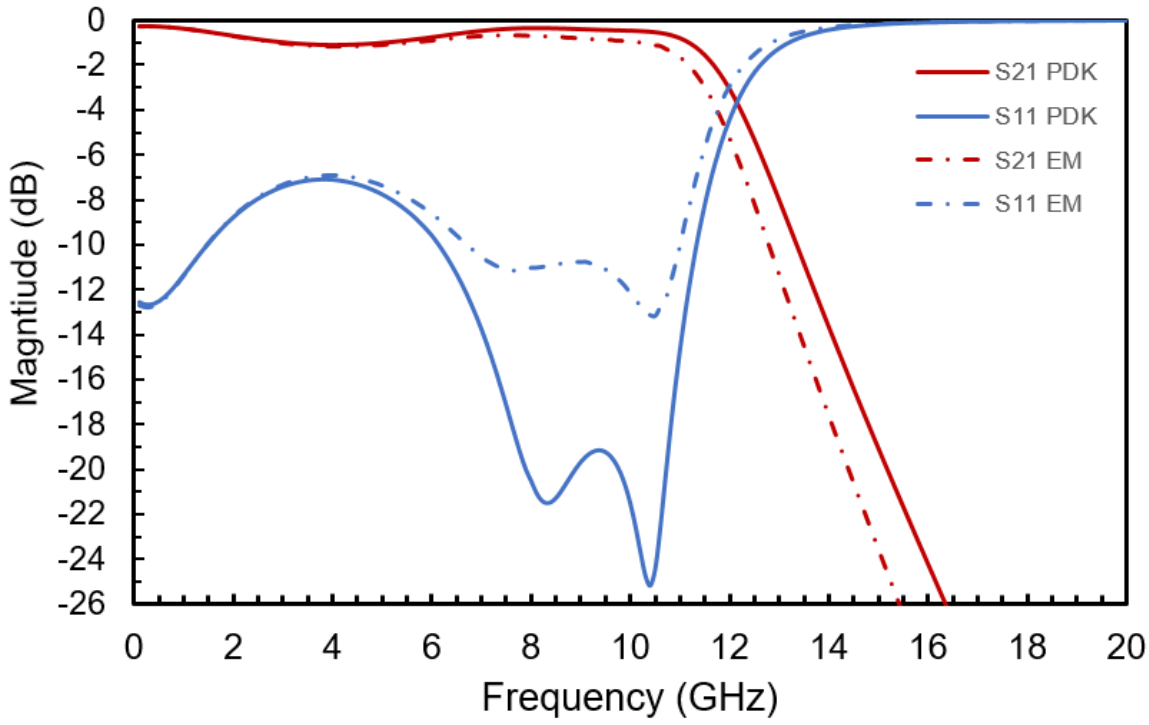


Fig. 5-13: Comparison of EM simulation with PDK simulation results for the output matching network.

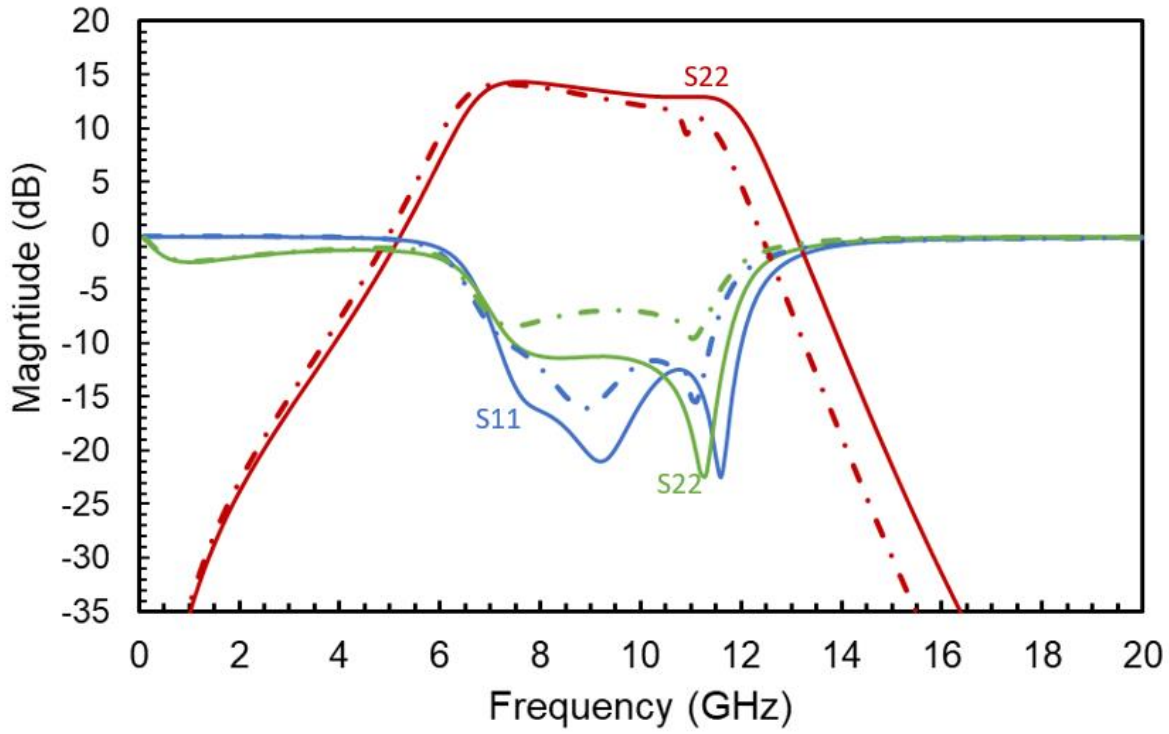
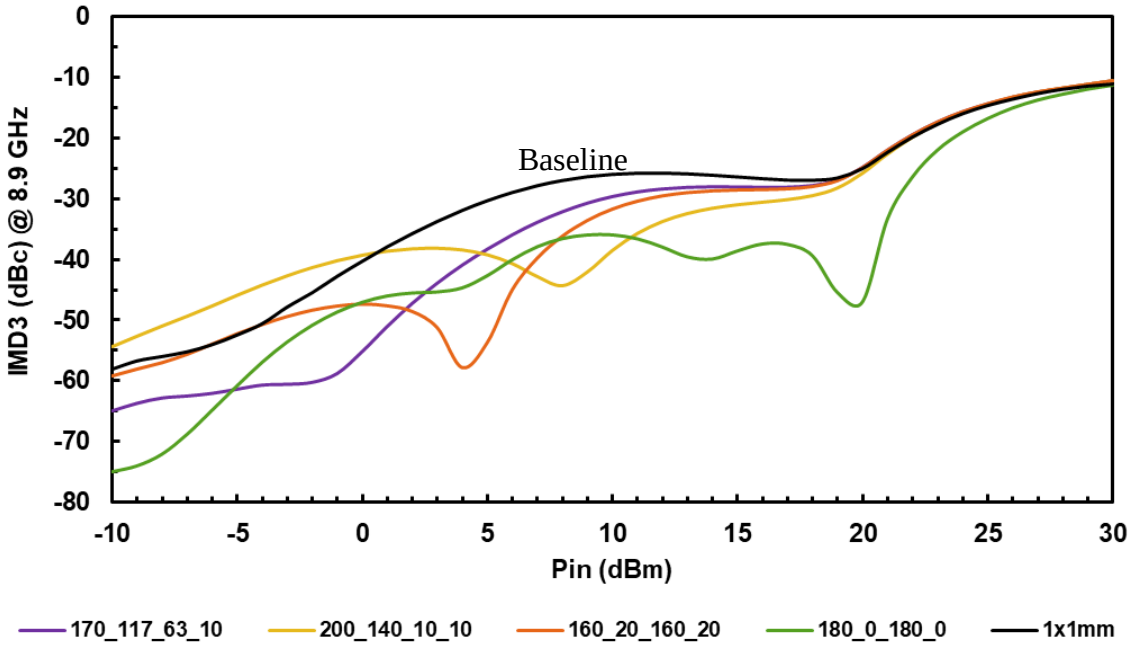


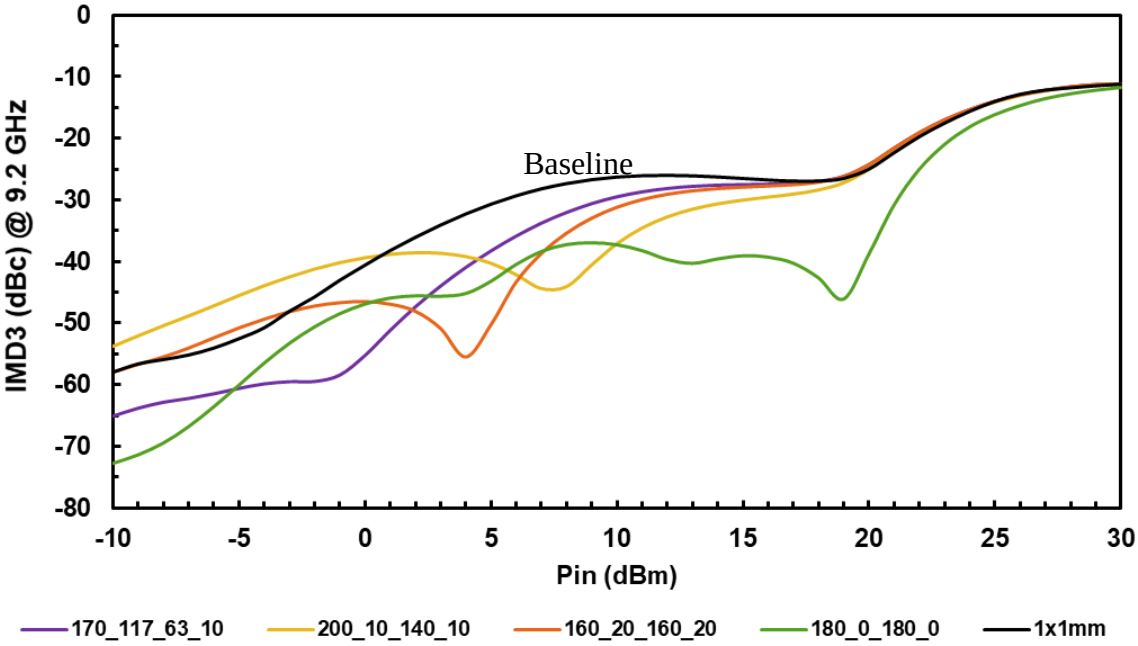
Fig. 5-14: Plot and comparison of the EM simulation with simulated S-parameter of the amplifier circuit. The dashed S-parameters are obtained with EM simulation.

5.3 Linearity Simulation Results

Large-signal harmonic balance simulations were performed for the four parallel FETs circuit (4 x 0.25 mm), varying the bias of each FET independently, and compared with the baseline simulations for the single FET circuit (8 x 125 um). A two-tone signal with spacing 100 MHz at the center frequencies of 8, 9 and 10 GHz, respectively, was applied to the amplifier circuits at the bias current levels of 90 mA/mm, which is 90 mA for a device of size 1 mm. Intermodulation distortion (IMD3) vs. Input power (Pin) was plotted for both lower and upper intermod levels at 9 GHz frequency shown in Fig. 5-15(a) and Fig. 5-15(b), respectively. In the plots, the black curve depicts the baseline case which shows the IMD3 performance of a single FET (1 x 1 mm) biased at 90 mA/mm. Different gradient bias currents were applied to the second amplifier containing four parallel FETs. Current in one of the four parallel FET(s) is increased while in others it is reduced such that the total bias current (90 mA/mm) remains the same.



(a)



(b)

Fig. 5-15: Simulated plot of IMD3 (dBc) vs. Pin (dBm) at the total bias current of 90 mA/mm for 4 x 0.25 mm circuit and 1 x 1 mm circuit (baseline case) (a) at lower intermodulation frequency (8.9 GHz) (b) at the higher intermodulation frequency (9.2 GHz).

In Fig. 5-15, the current in the legend is referred to as mA/mm. Legend entry of 170_117_63_10 refers to the bias condition for the amplifier circuit with four parallel FETs when the first FET is biased at 170 mA/mm, second at 117 mA/mm, third at 63 mA/mm and fourth at 10 mA/mm. An approximately 10 dB improvement in IMD3 is seen at a lower input power range of about -5 dBm for the bias value of 180_0_180_0; and a 20 dB improvement in IMD3 is seen at an input power level of 5 dBm for the bias value of 160_20_160_20, and about 20 – 30 dB improvement is seen for the bias value of 180_0_180_0 at about 20 dBm input power.

The reason for these improvements is attributed to phase cancellation of the IMD3 components which occurs when one device is biased in Class AB and other in deep Class AB mode, as seen with the hybrid circuit demonstrations. This phenomenon is discussed extensively in chapter 4.

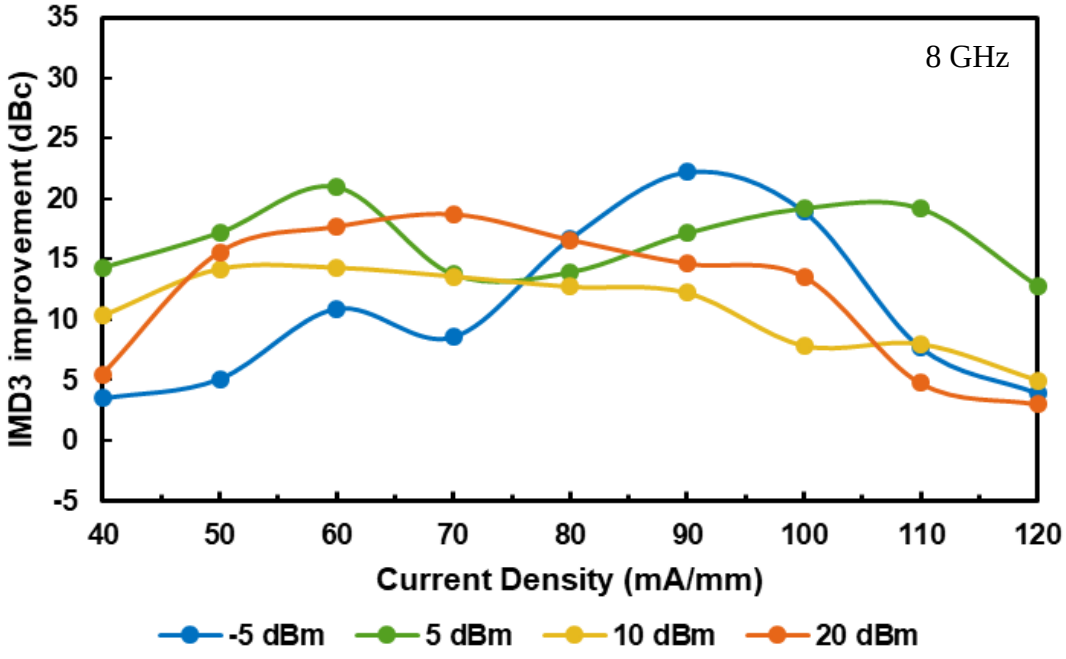
5.3.1 Summary of Improvement in Linearization

The proposed technique was explored for the current bias values from 40 mA/mm to 120 mA/mm. For the bias higher than 120 mA/mm or lower than 40 mA/mm, it becomes difficult to achieve phase cancellation by varying the bias current. Hence, this technique was not explored for the current values above 120 mA/mm and lower than 40 mA/mm.

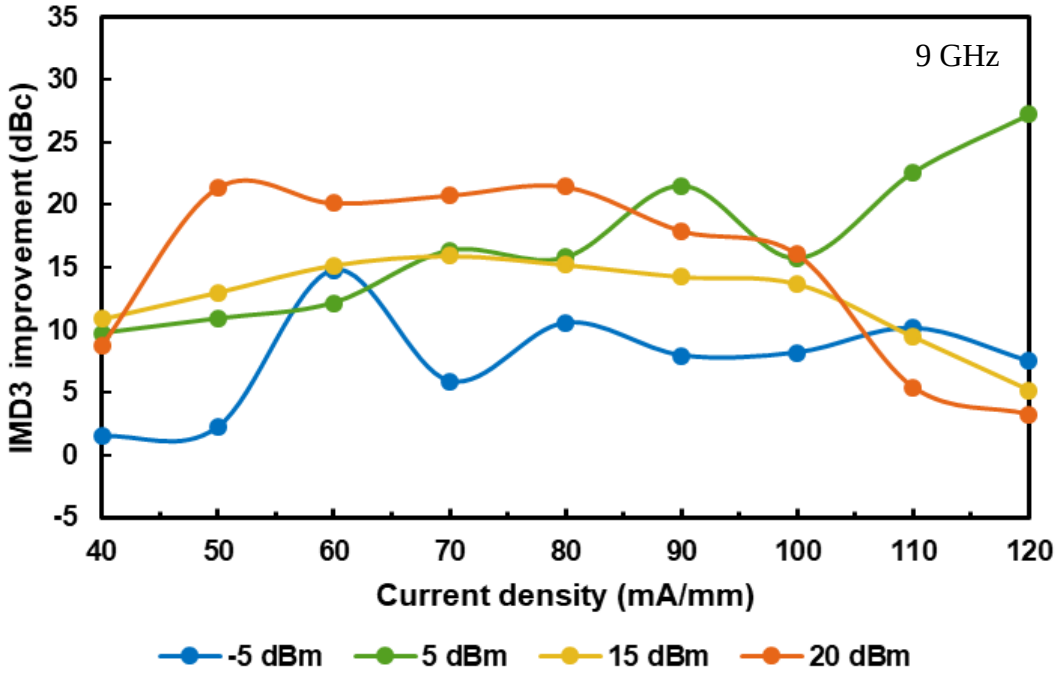
The results are summarized at the different frequencies from 8-10 GHz for different input power (Pin) levels of -5 dBm to 20 dBm in Fig. 5-16. The overall improvement in linearity is plotted by taking the average of linearity improvement achieved by the upper and lower intermods. Various currents achieve improvement at different input power levels as shown in the legend. It is found that it is easier to achieve the improvement at medium level current densities than at high and low current densities. By varying the bias of the FETs of the amplifier circuit, the maximum improvement in IMD3 up to 25 dBc can be seen.

5.3.2 Comparison Table

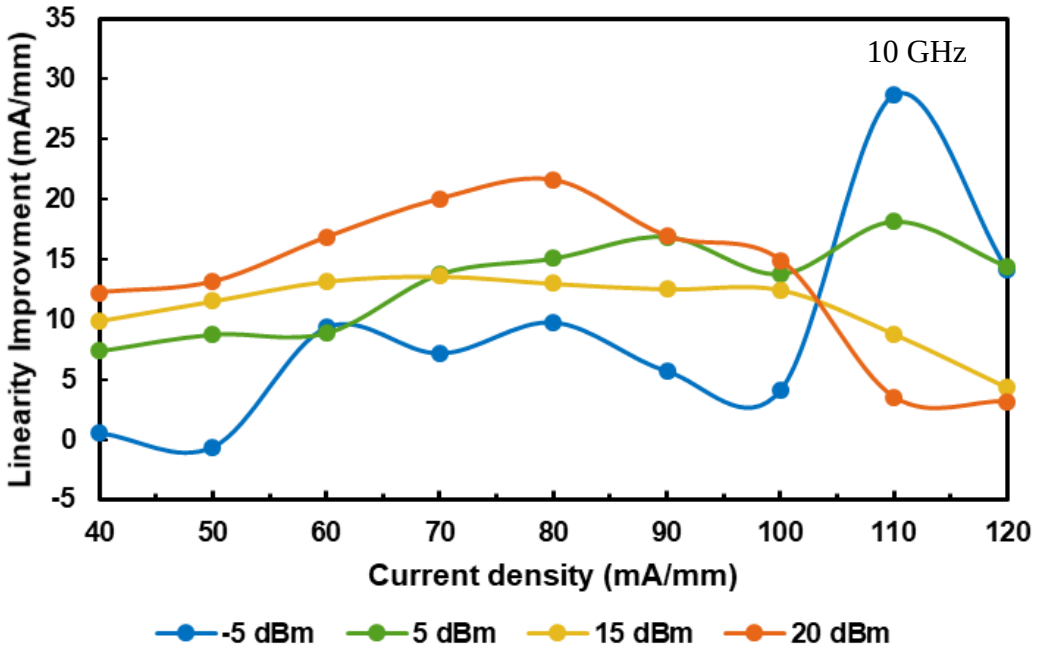
Table 5.1 provides a comparison of this work with the current state of the art PAs with similar analog linearization techniques. The simulation results show improvement by 25 – 30 dBc in linearity in the frequency range of 8-10 GHz. This technique of linearization through phase cancellation of IMD3 components using parallel FETs achieves high linearity over much broader frequency range compared with other techniques.


8 GHz
IMD3 improvement (dBc)
35
30
25
20
15
10
5
0
-5
40
50
60
70
80
90
100
110
120
Current Density (mA/mm)
-5 dBm
5 dBm
10 dBm
20 dBm

(a)


9 GHz
IMD3 improvement (dBc)
35
30
25
20
15
10
5
0
-5
40
50
60
70
80
90
100
110
120
Current density (mA/mm)
-5 dBm
5 dBm
15 dBm
20 dBm

(b)



(c)

Fig. 5-16: Simulated plot of linearity improvement vs. current density for different input power levels at the frequencies of (a) 8 GHz (b) 9 GHz (c) 10 GHz.

Table 5-1: Summary of performance and comparison of X-band GaN PAs with state-of-the-art linearization techniques in X-Band.

Ref	**Technology**	**Freq (GHz)**	**Pout (dBm)**	**Max IMD3 improvement (dBc)**	**Method of improvement**
[55]	GaN HEMT	8-10	15 - 25	4 @ 10 GHz	Capacitance Compensation
[64]	GaN HEMT	7.9-8.4	40	10.7	Predistortion
[65]	TWT	8.35-8.6	46.5	10	Predistortion
[66]	TWT	9.5	31	25.6	Feedforward and Predistortion
[67]	GaAs FET	7.5-8.5	50	10	Predistortion
This Work (sim.)	GaN HEMT	8-10	36	25-30	Phase cancellation in parallel FETs

5.4 Summary

It has been demonstrated that if a large FET is divided in four smaller FETs such that each FET is bias optimized, improvements in linearity performance can be achieved. To further study this approach, two GaN HEMT power amplifier MMICS were designed in the frequency range of 8-10 GHz in AWR microwave office software. The first amplifier consists of a single 8 x 125 um FET (1 x 1 mm) while the second amplifier consists of four parallel 2 x 125 um FETs (4 x 0.25 mm) giving the same total gate width periphery. Simulations results show the output power is achieved around 36 dBm with 15 dB gain and 42% PAE.

Simulation results show IMD3 improvement from 25-30 dBc is possible in the frequency range of 8-10 GHz by application of various gate current bias combinations. Compared with other similar linearization techniques, the proposed technique achieves better linearization over a broader range of frequencies. To the best of the authors' knowledge, this would be the first application of the mitigated transistors in the X-Band region. Future work consists of fabrication of the GaN MMIC's and measurement of the fabricated MMIC for linearity by application of various optimized bias conditions.

Chapter 6

Contributions and Future Work

6.1 Contributions

The main contribution of this work has been the demonstration of linearity enhancement of GaN amplifier circuits by using multiple independently biased parallel FETs. Linearity improvements have been demonstrated in both GaN PA and GaN LNA circuits. It has been found that when one of the FETs has been biased in Class AB and other in deep Class AB/Class B, an improvement of 15-20 dBc in the linearity was seen. The concept of using multiple parallel FETs for improving the linearity has been demonstrated for the first time for the GaN FETs, and a computer-aided design methodology has been developed to facilitate the design of such circuits.

In Chapter 2, simulation analysis was done in Matlab for flattening the g_m" characteristic of parallel FETs. A minimization function was defined to compute g_m" in the operating region. Percentage improvement of 62% and 92% in the minimization function with two and four parallel FETs was obtained respectively. This technique was then demonstrated experimentally in an amplifier design using two parallel FETs over the frequency range of 0.8-1.0 GHz. An improvement in linearity of about 4 dBc was achieved [54].

In Chapter 3, the technique of using multiple parallel FETs and biasing them individually was demonstrated for an S-Band LNA. The OIP3 obtained was > 50dBm by biasing the FETs individually and the Noise Figure (NF) obtained was about 2 dB. The experimental results showed up to 9.5 dBm improvement in OIP3 with the application of variable bias voltage. The NF remained constant with the change of the bias [68].

In Chapter 4, a detailed large-signal simulation methodology using commercial microwave CAD software was presented based on splitting a large device into multiple smaller parallel FETs. By varying the bias currents of each FET, the magnitude and phase of IMD3 component changes. Three types of prototype hybrid power amplifier circuits were designed and simulated in GaN Technology over the frequency range of 0.8-1.0 GHz: (a) a single 5 mm FET (1 x 5 mm); (b) two parallel 2.5 mm FETs (2 x 2.5 mm); and (c) four parallel 1.25 mm FETs (4 x 1.25 mm). The phase of the IMD3 components was checked using the power sampler component of the AWR microwave office. It was observed with the aid of large-signal simulations that the IMD3 currents of parallel FETs can be phase cancelled if they are biased appropriately. IMD3 improvement up to 20 dBc is achieved with four parallel FETs compared to a large single FET circuit and confirmed with measurements. IMD3 improvement is seen by about 20 dBc at Pin = 15 dBm and 5 dBm for total bias current of 60 mA/mm for four parallel FETs. Dividing a large FET into four smaller FETs gives a higher degree of freedom and better improvement in linearity. This technique finds practical use in high dynamic range RF amplifier circuits [69].

In Chapter 5, to demonstrate this technique for the MMIC's, X-Band GAN MMICs were designed in the frequency range of 8-10 GHz. The first MMIC was designed using a single 8 x 125 um FET and the second MMIC was designed using four parallel 2 x 125 um FETs making the total gate periphery to be 1 mm. Simulation results show an improvement in IMD3 by varying the bias of the parallel FETs by 25-30 dBc. This circuit achieves linearization over the broader range of frequencies (8-10 GHz) compared with the other state of the art MMICs.

6.2 Future Research Directions

6.2.1 MMIC fabrication and Testing for Linearity Improvement

Firstly, the two GaN MMIC circuits (a) using single 1 mm FET (8 x 125 um), (b) four parallel 0.25 um FETs (4 x 0.25 um) proposed in chapter 5 designed in the frequency range of 8-10 GHz will be fabricated in a foundry.

Extensive testing by giving different gate bias for improving linearity for two circuits will be performed. A lab set up for performing two-tone linearity test for IMD3 measurement is shown in Fig. 6-1. The MMIC PAs will be measured by mounting it on a PCB. In the test setup, two RF signal generators will be used to generate two-tone signals at the various frequencies from 8-10 GHz. Driver amplifiers will be used to increase the power level of RF signals. The Input power meter will check the amplitude of the input signal. Attenuators are used before the power meters as protection to stay within the dynamic range of the equipment [22], [70]. The two-tone signal will be fed to the input of the power amplifier MMIC, which is biased appropriately with DC power supply. The output power meter will measure the magnitude of the output signal and spectrum analyzer measure IMD3 and IMD5. A computer program can be used to compute Input Power (Pin), Output Power (Pout), Power Added Efficiency (PAE) and the IMD3 (third-order) and IMD5 (fifth-order) intermodulation distortion components.

Two sets of measurements will be performed (a) for the GaN MMIC PA using a single 8 x 125 um FET (b) for the GaN MMIC PA using four parallel 2 x 125 um FET by variation of the bias values. Optimum bias leading to the linearity improvement will be selected. Comparison of the simulated and measured results to state-of-the-art MMICs will be made.

6.2.2 Linearization Measurements with Complex Digitally Modulated Signals

The fabricated PA MMICs will also be characterized for linearity using complex digitally modulated signals. The PA would be tested using the various modulation schemes such as QAM, 8-PSK, 16-QAM, 64-QAM, and 128-QAM. While testing using the modulated signals, the linearity of the PA should be characterized for both in-band and out of band performance. EVM (Error Vector Magnitude) and ACPR (Adjacent Channel Power Ratio) tests would be done for characterizing the in-band and out-band linearity respectively [71].

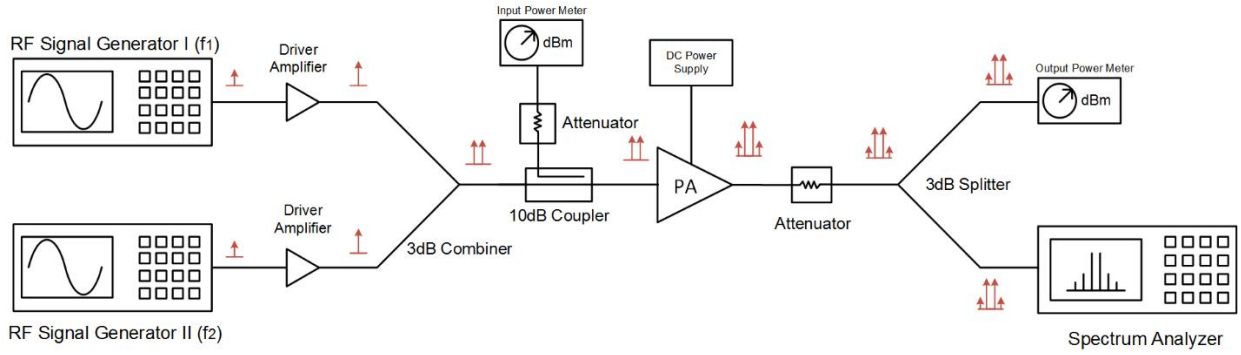


Fig. 6-1: Lab measurement set up for performing two-tone measurements.

6.2.2.1 EVM Measurement

The Error Vector Magnitude (EVM) is used to test the linearity of the amplifier when driven by a modulated signal. It is a measure of a signal waveform distortion due to amplitude and phase distortions that occur within amplifiers, as discussed in chapter 1. Fig. 6-2 shows a typical setup for measuring EVM.

A Vector Signal Generator is used to generate an I and Q baseband envelopes. These envelopes are modulated with a carrier frequency using an RF modulator. The signal generated would have all the constellation points at the ideal location. This signal would be passed from the DUT (Device Under Test). This signal would then be analyzed to calculate the deviation between the constellation from the ideal location [22], [62], [72].

6.2.2.2 ACPR Measurement

ACPR (Adjacent Channel Power Ratio) measurement is used to evaluate the linearity of the amplifier when driven by a modulated signal. Typically, the input signal to the amplifier has spectral components that are only contained in the intended channel. The nonlinearity of the amplifier causes a spectral spreading out of the intended channel to the adjacent channels [72]. This measurement is analogous to IM3/IM5 measurements [62]. ACPR is discussed in detail in chapter 1.

There are two methods to do ACPR measurement: Resolution Bandwidth (RBW) and Integration Bandwidth (IBW). Fig. 6-5 shows a typical ACPR measurement set up using the RBW filter.

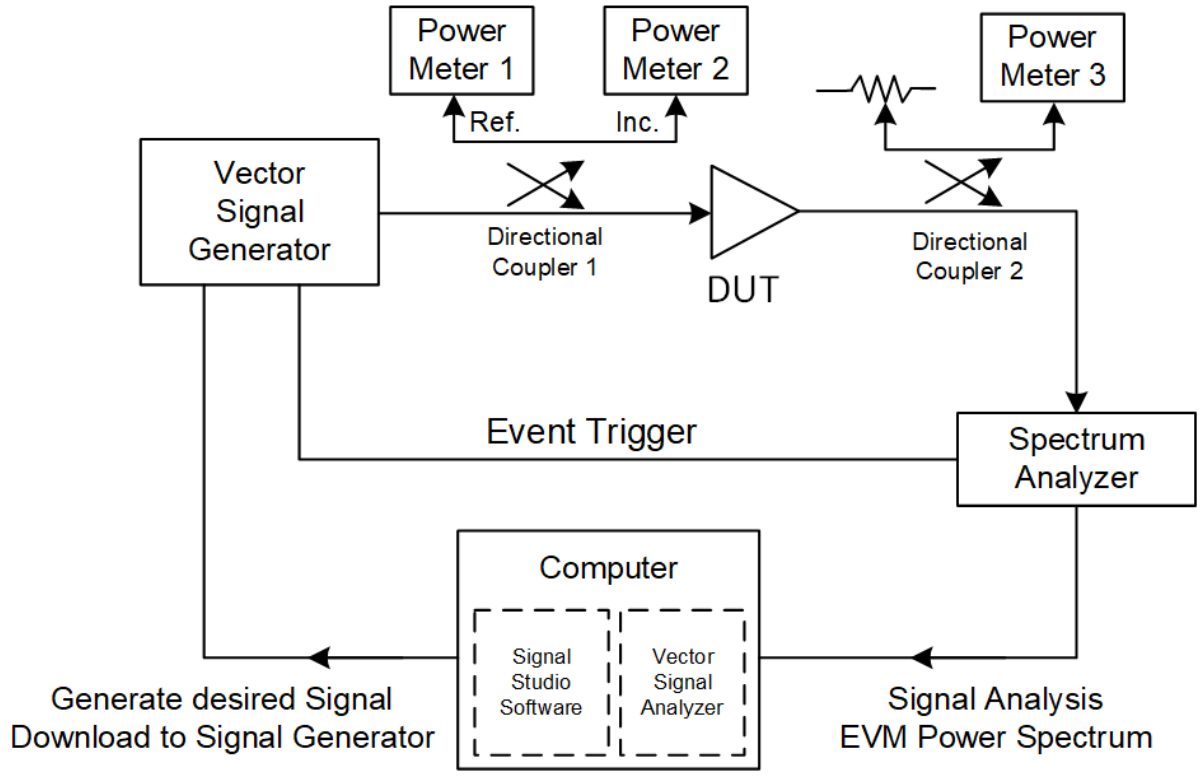


Fig. 6-2: Typical EVM measurement set up as illustrated in [62].

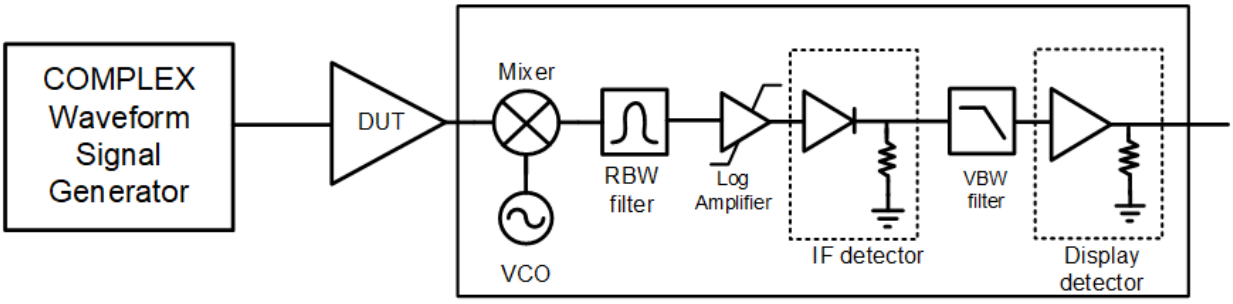


Fig. 6-3: Typical ACPR Measurement set up as illustrated in [62].

6.2.3 Nonlinear Device Modeling

In the previous chapters, discrepancies between the simulated and the measured results are observed. These discrepancies are attributed to inaccuracies in the large-signal models provided by the foundry. Hence, one direction for future work can be the development of more accurate nonlinear GaN device models for CAD.

An electrical model of the transistor is represented by equivalent circuit or mathematical equations which predict the behavior under predetermined set of conditions [62].

The Nonlinear models can be of the following three types

- Physics based models
- Compact Models
- Behavioral Models

6.2.3.1 Physics / Electromagnetic Theory Based Models

Physics-based models are linked with the doping profile and physical geometry of the device. Such models consist of two parts: extrinsic and intrinsic. The extrinsic part deals with the external pads and parasitics, while the intrinsic part deals with the active channel. The intrinsic part is obtained by solving device equations with approximate boundary and bias conditions. These models are quite complex and have lengthy extraction times [62], [73]–[75].

6.2.3.2 Compact or Measurement Based Models

Compact models are also known as analytical models. They are based on an equivalent circuit representation of the transistor. These models are obtained by fitting model simulations to the measurements: Small-signal S-parameters, Large-signal S-parameters, I-V Curve, Noise measurements, etc. Most popular compact models include Angelov, Curtice and EEHEMT[62], [76]–[78].

Nonlinear modeling steps can be summarized [79] in Fig. 6-6. A test station consisting of wafer probe station, VNA (Vector Network Analyzer) is used to acquire characteristics (DC, S-parameter) for co-efficient extraction of model parameters. Then an appropriate model is selected, and various parameters are extracted using commercial CAD software such as Keysight ADS, IC-CAP, NI AWR, etc.

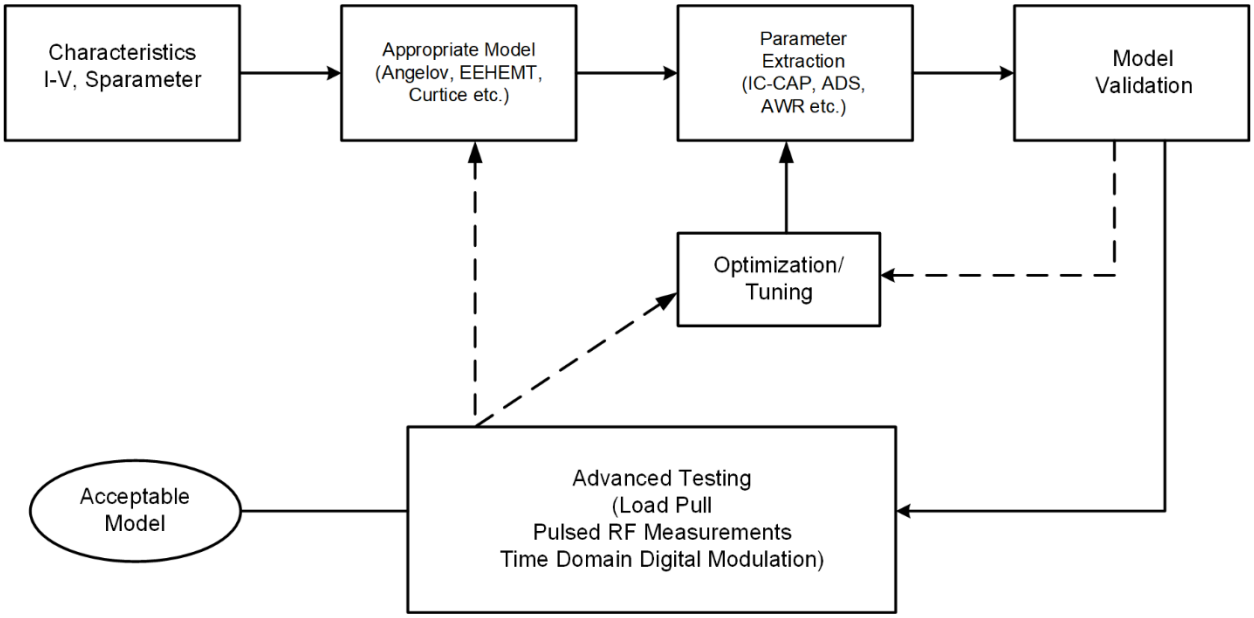


Fig. 6-4: Nonlinear modeling steps as illustrated in [79].

The model obtained is then simulated by using various input parameters and the results compared with the measurements done. The model parameters are then re-optimized to fit the measurement results. Advanced testing is also done to include load-pull and pulsed RF measurements. This process is repeated until an acceptable model is obtained.

6.2.3.3 Behavioral Models

Behavioral modeling is accomplished by relating the input and the output signals without resorting to circuit-level analysis. Behavioral modeling is typically performed by fitting the measured data to parameters of an algorithm [80].

Neural Networks are typically used for nonlinear modeling due to their flexibility. These models are abstract in nature, and the device is a black box with no physical information about the inner core device itself [81]–[83].

Selection of the model

Physics-based models are quite complex, and behavioral models do not give any knowledge of the device because of their inherent abstract nature. However, both of the models serve their purpose. We propose to develop a compact model for characterization of linearity as the model parameters are easier to extract and take a reasonable amount of time while giving details of the device.

Bibliography

[1] B. Razavi, *RF Microelectronics*, 2 edition. Upper Saddle River, NJ: Prentice Hall Communications Engineering and Emerging Technological Series, 2011.

[2] "Underlining the Meaning of Linearity," *Microwaves & Radio Frequency*, 11-Apr-2017. [Online]. Available: https://www.mwrf.com/components/underlining-meaning-linearity. [Accessed: 07-Sep-2019].

[3] L. Cho, C. Ting, C. Chen, C. Yau, and C. Hsu, "When UUDN meets 5G waveforms: New challenge of signal linearity?," in *2017 International Conference on Applied System Innovation (ICASI)*, 2017, pp. 770–773.

[4] A. F. Demir, M. Elkourdi, M. Ibrahim, and H. Arslan, "Waveform Design for 5G and Beyond," *ArXiv190205999 Eess*, pp. 51–76, Sep. 2018.

[5] T. Boles, "GaN-on-Silicon – Present capabilities and future directions," presented at the 8th International Conference On Low Dimensional Structures and Devices (LDSD 2016), Mayan Riviera, Mexico, 2018, p. 020001.

[6] A. Katz and M. Franco, "GaN Comes of Age," *IEEE Microw. Mag.*, vol. 11, no. 7, pp. S24–S34, Dec. 2010.

[7] U. K. Mishra, P. Parikh, and Yi-Feng Wu, "AlGaN/GaN HEMTs-an overview of device operation and applications," *Proc. IEEE*, vol. 90, no. 6, pp. 1022–1031, Jun. 2002.

[8] T. N. T. Do *et al.*, "7–13 GHz MMIC GaN HEMT Voltage-Controlled-Oscillators (VCOs) for satellite applications," in *2017 12th European Microwave Integrated Circuits Conference (EuMIC)*, 2017, pp. 220–223.

[9] K. Osawa, H. Yoshikoshi, A. Nitta, T. Tanaka, E. Mitani, and T. Satoh, "Over 74% efficiency, L-band 200W GaN-HEMT for space applications," in *2016 46th European Microwave Conference (EuMC)*, 2016, pp. 397–400.

[10] T. Satoh, K. Osawa, and A. Nitta, "GaN HEMT for Space Applications," in *2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2018, pp. 136–139.

[11] Y. Kobayashi, A. Tomiki, and S. Kawasaki, “Annual Deep-Space Flight Operation Verification of X-Band GaN SSPA,” *IEEE Trans. Aerosp. Electron. Syst.*, vol. 55, no. 2, pp. 930–938, Apr. 2019.

[12] S. Nakajima, “GaN HEMTs for 5G Base Station Applications,” in *2018 IEEE International Electron Devices Meeting (IEDM)*, 2018, pp. 14.2.1-14.2.4.

[13] J. Liu *et al.*, “GaN-Based Blue Laser Diodes With 2.2 W of Light Output Power Under Continuous-Wave Operation,” *IEEE Photonics Technol. Lett.*, vol. 29, no. 24, pp. 2203–2206, Dec. 2017.

[14] H. Sarnago, O. Lucia, and J. M. Burdío, “High frequency electroporation for biomedical applications using GaN gate injection transistors,” in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 698–702.

[15] D. Marti, S. Tirelli, A. R. Alt, J. Roberts, and C. R. Bolognesi, “150-GHz Cutoff Frequencies and 2-W/mm Output Power at 40 GHz in a Millimeter-Wave AlGaN/GaN HEMT Technology on Silicon,” *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1372–1374, Oct. 2012.

[16] J. S. Moon *et al.*, “Gate-recessed AlGaN-GaN HEMTs for high-performance millimeter-wave applications,” *IEEE Electron Device Lett.*, vol. 26, no. 6, pp. 348–350, Jun. 2005.

[17] K. Makiyama *et al.*, “S5-H7: GaN-HEMT technology for high power millimeter-wave amplifier,” in *2014 Lester Eastman Conference on High Performance Devices (LEC)*, 2014, pp. 1–4.

[18] K. Boutros, R. Chu, and B. Hughes, “Recent advances in GaN power electronics,” in *Proceedings of the IEEE 2013 Custom Integrated Circuits Conference*, 2013, pp. 1–4.

[19] M. Guacci, M. Tatic, D. Bortis, J. W. Kolar, Y. Kinoshita, and H. Ishida, “Novel Three-Phase Two-Third-Modulated Buck-Boost Current Source Inverter System Employing Dual-Gate Monolithic Bidirectional GaN e-FETs,” in *2019 IEEE 10th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2019, pp. 674–683.

[20] S. Nagai *et al.*, “A compact GaN Bi-directional switching diode with a GaN Bi-directional power switch and an Isolated gate driver,” in *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2016, pp. 183–186.

[21] P. B. Kenington, *High Linearity RF Amplifier Design*, 1st ed. Norwood, MA, USA: Artech House, Inc., 2000.

[22] K. A. Fayed, “The Design of Linearized Power Amplifier for Wireless Communications,” M.S. thesis, Virginia Tech, Falls Chruch, VA, 2009.

[23] W. Kester, “Confused About Amplifier Distortion Specs? | Analog Dialgoue,” vol. 27, pp. 27–29, 01-Nov-1993.

[24] Z. El-Khatib, L. MacEachern, and S. A. Mahmoud, *Distributed CMOS Bidirectional Amplifiers: Broadbanding and Linearization Techniques*. New York: Springer-Verlag, 2012.

[25] I. Khalil, “Intermodulation distortion in GaN HEMT,” M.Sc. Eng., Ferdinand-Braun-Institut, Berlin, Germany, 2009.

[26] S.-G. Kang, I.-K. Lee, and K.-S. Yoo, “Analysis and design of feedforward power amplifier,” in *1997 IEEE MTT-S International Microwave Symposium Digest*, 1997, vol. 3, pp. 1519–1522 vol.3.

[27] K. J. Parsons, R. J. Wilkinson, and P. B. Kenington, “A highly-efficient linear amplifier for satellite and cellular applications,” in *Proceedings of GLOBECOM ’95*, 1995, vol. 1, pp. 203–207 vol.1.

[28] A. K. Ezzeddine, H. L. A. Hung, and H. C. Huang, “An MMAC C-band FET feedback power amplifier,” *IEEE Trans. Microw. Theory Tech.*, vol. 38, no. 4, pp. 350–357, Apr. 1990.

[29] K. Yamauchi, K. Mori, M. Nakayama, Y. Itoh, Y. Mitsui, and O. Ishida, “A novel series diode linearizer for mobile radio power amplifiers,” in *Microwave Symposium Digest, 1996., IEEE MTT-S International*, 1996, vol. 2, pp. 831–834 vol.2.

[30] K. Yamauchi, H. Noto, S. Ishizaka, Y. Hamamatsu, M. Nakayama, and Y. Isota, “Series anti-parallel diode linearizer for class-B power amplifiers with a gain expansion,” in *Microwave Conference, 2006. APMC 2006. Asia-Pacific*, 2006, pp. 883–886.

[31] B. Kim, J.-S. Ko, and K. Lee, “A new linearization technique for MOSFET RF amplifier using multiple gated transistors,” *IEEE Microw. Guid. Wave Lett.*, vol. 10, no. 9, pp. 371–373, Sep. 2000.

[32] B. Kim, J.-S. Ko, and K. Lee, “Highly linear CMOS RF MMIC amplifier using multiple gated transistors and its Volterra series analysis,” in *Microwave Symposium Digest, 2001 IEEE MTT-S International*, 2001, vol. 1, pp. 515–518.

[33] T. W. Kim, B. Kim, I. Nam, B. Ko, and K. Lee, “A low-power highly linear cascoded multiple-gated transistor CMOS RF amplifier with 10 dB IP3 improvement (Revised),” *IEEE Microw. Wirel. Compon. Lett.*, vol. 13, no. 9, pp. 420–422, Sep. 2003.

[34] C. J. Trantanella and P. Blount, “Low Noise GaN Amplifiers with Inherent Overdrive Protection,” *Microw. J. Int. Ed Dedham*, vol. 58, no. 5, p. 78,80,82,84,86,88, May 2015.

[35] S. Colangeli, A. Bentini, W. Ciccognani, E. Limiti, and A. Nanni, “GaN-Based Robust Low-Noise Amplifiers,” *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3238–3248, Oct. 2013.

[36] F. Schwierz and J. J. Liou, “Semiconductor devices for RF applications: evolution and current status,” *Microelectron. Reliab.*, vol. 41, no. 2, pp. 145–168, Feb. 2001.

[37] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, “GaN-Based RF Power Devices and Amplifiers,” *Proc. IEEE*, vol. 96, no. 2, pp. 287–305, Feb. 2008.

[38] A. Chini *et al.*, “Power and linearity characteristics of field-plated recessed-gate AlGaN-GaN HEMTs,” *IEEE Electron Device Lett.*, vol. 25, no. 5, pp. 229–231, May 2004.

[39] “Microwaves101 | Cascade Analysis.” [Online]. Available: https://www.microwaves101.com/encyclopedias/cascade-analysis. [Accessed: 23-Sep-2019].

[40] K. W. Kobayashi, “An 8-W 250-MHz to 3-GHz Decade-Bandwidth Low-Noise GaN MMIC Feedback Amplifier With > +51-dBm OIP3,” *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2316–2326, Oct. 2012.

[41] S. Cha *et al.*, “Wideband AlGaN/GaN HEMT low noise amplifier for highly survivable receiver electronics,” in *2004 IEEE MTT-S International Microwave Symposium Digest (IEEE Cat. No.04CH37535)*, 2004, vol. 2, pp. 829-831 Vol.2.

[42] S. E. Shih *et al.*, “Broadband GaN Dual-Gate HEMT Low Noise Amplifier,” in *2007 IEEE Compound Semiconductor Integrated Circuits Symposium*, 2007, pp. 1–4.

[43] J. Zhang, H. Zirath, and V. Fusco, “Linearity improvement using a modified derivative superposition method in cascaded stages amplifier,” *IET Microw. Antennas Amp Propag.*, vol. 6, no. 8, pp. 922–928, Jun. 2012.

[44] E. E. Eid and F. M. Ghannouchi, “Adaptive nulling loop control for 1.7-GHz feedforward linearization systems,” *IEEE Trans. Microw. Theory Tech.*, vol. 45, no. 1, pp. 83–86, Jan. 1997.

[45] P. B. Kenington and D. W. Bennett, “Linear distortion correction using a feedforward system,” *IEEE Trans. Veh. Technol.*, vol. 45, no. 1, pp. 74–81, Feb. 1996.

[46] R. R. Carney and M. A. Komara, “Multi-carrier high power amplifier using digital pre-distortion,” US5937011 A, 10-Aug-1999.

[47] *Microwave Office Element Catalog*, vol. 14.03. El Segundo, CA: NI AWR Design Environment, 2019.

[48] B. Toole, C. Plett, and M. Cloutier, “RF circuit implications of moderate inversion enhanced linear region in MOSFETs,” *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 51, no. 2, pp. 319–328, Feb. 2004.

[49] P. E. de Falco, J. Birchall, and L. Smith, “Hitting the Sweet Spot: A Single-Ended Power Amplifier Exploiting Class AB Sweet Spots and Optimized Third Harmonic Termination,” *IEEE Microw. Mag.*, vol. 18, no. 1, pp. 63–70, Jan. 2017.

[50] C. Lu, A.-V. H. Pham, M. Shaw, and C. Saint, “Linearization of CMOS Broadband Power Amplifiers Through Combined Multigated Transistors and Capacitance Compensation,” *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 11, pp. 2320–2328, Nov. 2007.

[51] A. Ando, Y. Takayama, T. Yoshida, R. Ishikawa, and K. Honjo, “A high-efficiency class-F GaN HEMT power amplifier with a diode predistortion linearizer,” in *Microwave Conference, 2008. APMC 2008. Asia-Pacific*, 2008, pp. 1–4.

[52] Y.-S. Lee, M.-W. Lee, and Y.-H. Jeong, “Analog predistortion power amplifiers using IMD sweet spots for WCDMA applications,” *Microw. Opt. Technol. Lett.*, vol. 49, no. 11, pp. 2838–2841, Nov. 2007.

[53] Y.-H. Chen, K. Y. Kao, C.-Y. Chao, and K. Y. Lin, “A 24 GHz CMOS power amplifier with successive IM2 feed-forward IMD3 cancellation,” in *2015 IEEE MTT-S International Microwave Symposium*, 2015, pp. 1–4.

[54] K. Saini, S. Raman, A. K. Ezzeddine, and H. C. Huang, “Linearity enhancement for GaN HEMT amplifier using parallel transistors with independent gate bias control,” in *2016 IEEE 17th Annual Wireless and Microwave Technology Conference (WAMICON)*, 2016, pp. 1–3.

[55] V. Paidi, S. Heikman, A. Chini, U. K. Mishra, M. J. W. Rodwell, and S. I. Long, “High linearity GaN HEMT power amplifier with pre-linearization gate diode,” in *Proceedings. IEEE Lester Eastman Conference on High Performance Devices, 2004.*, 2004, pp. 223–228.

[56] Q. Cai, W. Che, and K. Ma, “A linear GaN power amplifier using novel transistor based analog predistortion method,” in *2016 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP)*, 2016, pp. 1–4.

[57] T. Joo, B. Koo, and S. Hong, “A WLAN RF CMOS PA With Large-Signal MGTR Method,” *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 3, pp. 1272–1279, Mar. 2013.

[58] S. Baek *et al.*, “A Linear InGaP/GaAs HBT Power Amplifier Using Parallel-Combined Transistors With IMD3 Cancellation,” *IEEE Microw. Wirel. Compon. Lett.*, vol. 26, no. 11, pp. 921–923, Nov. 2016.

[59] Q. Liu, S. Jiangtao, Y. Shu, K. Horie, N. Itoh, and T. Yoshimasu, “A high efficiency and high linearity power amplifier utilizing post-linearization technique for 5.8 GHz DSRC applications,” in *2011 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications*, 2011, pp. 45–48.

[60] A. Raffo and G. Crupi, *Microwave Wireless Communications | ScienceDirect*. Elsevier Ltd, 2016.

[61] A. Ezzeddine, H. A. Hung, E. Viveiros, and H. Huang, “High-power GaN MMIC PA Over 40–4000MHz,” in *2013 IEEE MTT-S International Microwave Symposium Digest (MTT)*, 2013, pp. 1–4.

[62] I. J. Bahl, *Fundamentals of RF and Microwave Transistor Amplifiers*. New Jersey: Wiley, 2009.

[63] “AN136 Amplifier design example - using Power FET AM036MX-QG-R,” Jan-2011. [Online]. Available: http://www.amcomusa.com/documents/applications/transapps/AN136.pdf. [Accessed: 29-Jul-2019].

[64] X. Xie, Z. Zhong, and Y. Guo, “X-band predistortion linearized GaN HPA for broadband satellite communications,” in *2014 IEEE International Conference on Communication Systems*, 2014, pp. 433–436.

[65] X. Hu, G. Wang, Z. Wang, and J. Luo, “Predistortion Linearization of an X-Band TWTA for Communications Applications,” *IEEE Trans. Electron Devices*, vol. 58, no. 6, pp. 1768–1774, Jun. 2011.

[66] Ji Han Joo, Min Ho Son, Yong Dug Lee, and Jin Joo Choi, “Feedforward and predistortion linearizers on an X-band helix-TWT,” in *Fifth IEEE International Vacuum Electronics Conference (IEEE Cat. No.04EX786)*, 2004, pp. 174–175.

[67] Y. Chung, B. C. Deckman, and M. P. DeLisio, “Linearization of a Spatially-Combined X-Band 100-W GaAs FET Power Amplifier System with Predistortion Linearizer,” in *2012 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2012, pp. 1–4.

[68] K. Saini, A. Ezzeddine, W. Joudeh, H. Huang, and S. Raman, “S-band GaN LNA with OIP3>50dBm using parallel independently biased gates,” in *2018 IEEE 19th Wireless and Microwave Technology Conference (WAMICON)*, 2018, pp. 1–4.

[69] K. Saini, A. Ezzeddine, W. Joudeh, H. Huang, and S. Raman, “Computer-aided design methodology for Linearity enchancement of multi-watt GaN HEMT amplifiers using multiple parallel devices,” *Int. J. RF Microw. Comput.-Aided Eng.*, Accepted.

[70] “FAQ: Where are attenuators used?” [Online]. Available: https://www.connectortips.com/faq-where-are-attenuators-used/. [Accessed: 20-Aug-2019].

[71] S. Y. Mortazavi, “Millimeter-Wave Harmonically-Tuned Silicon Power Amplifiers for High Efficiency,” Ph.D. Dissertation, Virginia Tech, Blacksburg VA, 2016.

[72] W. Y. Refai, “A Linear RF Power Amplifier with High Efficiency for Wireless Handsets,” Ph.D. Dissertation, Virginia Tech, Blacksburg VA, 2014.

[73] S. Vitanov *et al.*, “Physics-Based Modeling of GaN HEMTs,” *IEEE Trans. Electron Devices*, vol. 59, no. 3, pp. 685–693, Mar. 2012.

[74] U. Radhakrishna, L. Wei, D. Lee, T. Palacios, and D. Antoniadis, “Physics-based GaN HEMT transport and charge model: Experimental verification and performance projection,” in *2012 International Electron Devices Meeting*, 2012, pp. 13.6.1-13.6.4.

[75] S. Khandelwal, N. Goyal, and T. A. Fjeldly, “A Physics-Based Analytical Model for 2DEG Charge Density in AlGaN/GaN HEMT Devices,” *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3622–3625, Oct. 2011.

[76] I. Angelov, H. Zirath, and N. Rosman, “A new empirical nonlinear model for HEMT and MESFET devices,” *Microw. Theory Tech. IEEE Trans. On*, vol. 40, no. 12, pp. 2258–2266, Dec. 1992.

[77] W. R. Curtice, “A MESFET Model for Use in the Design of GaAs Integrated Circuits,” *Microw. Theory Tech. IEEE Trans. On*, vol. 28, no. 5, pp. 448–456, May 1980.

[78] Y. H. Chang and J. J. Chang, “Analysis of an EEHEMT Model for InP pHEMTs,” in *2007 IEEE Conference on Electron Devices and Solid-State Circuits*, 2007, pp. 237–240.

[79] L. Dunleavy, C. Baylis, W. Curtice, and R. Connick, “Modeling GaN: Powerful but Challenging,” *IEEE Microw. Mag.*, vol. 11, no. 6, pp. 82–96, Oct. 2010.

[80] K. Vryssas and A. Samelis, “Behavioral modeling of nonlinear radio-frequency power amplifiers,” in *2005 Asia-Pacific Microwave Conference Proceedings*, 2005, vol. 1.

[81] D. E. Root and J. Wood, *ARTECH HOUSE USA : Fundamentals of Nonlinear Behavioral Modeling for RF and Microwave Design*. Artech House, Inc., 2005.

[82] A. Jarndal, "Genetic algorithm-based neural-network modeling approach applied to AlGaN/GaN devices," *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 23, no. 2, pp. 149–156, 2013.

[83] A. Raffo, G. Bosi, V. Vadalà, and G. Vannini, "Behavioral Modeling of GaN FETs: A Load-Line Approach," *IEEE Trans. Microw. Theory Tech.*, vol. 62, no. 1, pp. 73–82, Jan. 2014.

Appendix A

The power series expansion of output voltage from an amplifier is given by the following equation

$$V_{out} = a_1 V_{in} + a_2 V_{in}^{\ 2} + a_3 V_{in}^{\ 3} + \ldots\ldots\ldots\ldots\ldots \quad (1)$$

Two-tone input signal is given by

$$V_{in} = V\left(\cos\omega_1 t + \cos\omega_2 t\right) \quad (2)$$

On substituting equation (2) in equation (1)

$$V_{out} = a_1 V\left(\cos\omega_1 t + \cos\omega_2 t\right) + a_2 V^2(\cos\omega_1 t + \cos\omega_2 t)^2 + a_3 V^3(\cos\omega_1 t + \cos\omega_2 t)^3 + \ldots\ldots\ldots \quad (3)$$

Simplifying the above equation,

$$V_{out} = A + B + C \quad (4)$$

where each of the terms are given by the following expression:

$$A = a_1 V(\cos\omega_1 t + \cos\omega_2 t) \quad (5)$$

$$B = a_2 V^2(\cos\omega_1 t + \cos\omega_2 t)^2 \quad (6)$$

$$C = a_3 V^3(\cos\omega_1 t + \cos\omega_2 t)^3 \quad (7)$$

Solving for B,

$$B = a_2 V^2(\cos^2\omega_1 t + \cos^2\omega_2 t + 2\cos\omega_1 t\cos\omega_2 t) \quad (8)$$

On application of the formulas, $\cos^2 x = \frac{1}{2}(1+\cos 2x)$ and

$\cos x.\cos y = \frac{1}{2}(\cos(x+y)+\cos(x-y))$ in equation (8)

$$B = a_2 V^2\left(\frac{1}{2}\left(1+\cos 2\omega_1 t\right)+\frac{1}{2}\left(1+\cos 2\omega_2 t\right)+2\left(\frac{1}{2}\left(\cos\left(\omega_1 t+\omega_2 t\right)+\cos\left(\omega_1 t-\omega_2 t\right)\right)\right)\right) \quad (9)$$

$$B = a_2 V^2\left(1+\frac{1}{2}\left(\cos 2\omega_1 t+\cos 2\omega_2 t\right)+\cos\left(\omega_1 t+\omega_2 t\right)+\cos\left(\omega_1 t-\omega_2 t\right)\right) \quad (10)$$

$$B = a_2 V^2 + \frac{a_2 V^2}{2}\left(\cos 2\omega_1 t+\cos 2\omega_2 t\right)+a_2 V^2\left(\cos\left(\omega_1 t+\omega_2 t\right)+\cos\left(\omega_1 t-\omega_2 t\right)\right) \quad (11)$$

Solving for the term C,

$$C = a_3 V^3(\cos\omega_1 t + \cos\omega_2 t)^3 \quad (12)$$

Applying the formulas, $(x+y)^3 = x^3 + y^3 + 3x^2y + 3xy^2$, $\cos^2 x = \frac{1}{2}(1+\cos 2x)$,

$\cos^3 x = \frac{1}{4}(3\cos x + \cos 3x)$

and $\cos x.\cos y = \frac{1}{2}(\cos(x+y) + \cos(x-y))$, following expression(s) can be obtained.

$$C = a_3 V^3 \left(\cos^3 \omega_1 t + \cos^3 \omega_2 t + 3\cos^2 \omega_1 t \cos \omega_2 t + 3\cos \omega_1 t \cos^2 \omega_2 t\right) \tag{13}$$

$$C = a_3 V^3 \left(\frac{9}{4}\cos \omega_1 t + \frac{1}{4}\cos 3\omega_1 t + \frac{9}{4}\cos \omega_2 t + \frac{1}{4}\cos 3\omega_2 t + \frac{3}{2}\cos 2\omega_1 t \cos \omega_2 t + \frac{3}{2}\cos \omega_1 t \cos 2\omega_2 t\right) \tag{14}$$

$$C = \frac{9}{4}a_3 V^3 (\cos \omega_1 t + \cos \omega_2 t) + \frac{1}{4}a_3 V^3 (\cos 3\omega_1 t + \cos 3\omega_2 t) + \frac{3}{4}a_3 V^3 (\cos(2\omega_2 t - \omega_1 t) + \cos(2\omega_1 t - \omega_2 t)) + \frac{3}{4}a_3 V^3 (\cos(\omega_1 t + 2\omega_2 t) + \cos(2\omega_1 t + \omega_2 t)) \tag{15}$$

$$C = \frac{9}{4}a_3 V_p{}^3 (\cos \omega_1 t + \cos \omega_2 t) + \frac{1}{4}a_3 V_p{}^3 (\cos 3\omega_1 t + \cos 3\omega_2 t) + \frac{3}{4}a_3 V_p{}^3 \{\cos(2\omega_2 t - \omega_1 t) + \cos(2\omega_1 t - \omega_2 t)\} + \frac{3}{4}a_3 V_p{}^3 \{\cos(\omega_1 t + 2\omega_2 t) + \cos(2\omega_1 t + \omega_2 t)\} \tag{16}$$

On substituting the above expressions in $V_{out} = A + B + C$, the following expression is obtained

$$V_{out} = a_1 V(\cos \omega_1 t + \cos \omega_2 t) + a_2 V^2 + \frac{a_2 V^2}{2}(\cos 2\omega_1 t + \cos 2\omega_2 t) + a_2 V^2 (\cos(\omega_1 + \omega_2)t + \cos(\omega_1 - \omega_2)t) + \frac{9a_3 V^3}{4}(\cos \omega_1 t + \cos \omega_2 t) + \frac{a_3 V^3}{4}(\cos 3\omega_1 t + \cos 3\omega_2 t) + \frac{3a_3 V^3}{4}(\cos(2\omega_1 + \omega_2)t + \cos(\omega_1 + 2\omega_2)t) + \frac{3a_3 V^3}{4}(\cos(\omega_1 - 2\omega_2)t + \cos(2\omega_1 - \omega_2)t) \tag{17}$$

The above equation can be simplified in the equation below

$$V_{out} = a_2V^2 + \left(a_1V + \frac{9a_3V^3}{4} \right)(\cos\omega_1 t + \cos\omega_2 t) + \frac{a_2V^2}{2}\left(\cos 2\omega_1 t + \cos 2\omega_2 t\right) + a_2V^2\left(\cos(\omega_1+\omega_2)t + \cos(\omega_1-\omega_2)t\right)$$
$$+ \frac{a_3V^3}{4}\left(\cos 3\omega_1 t + \cos 3\omega_2 t\right) + \frac{3a_3V^3}{4}\left(\cos\left(2\omega_1+\omega_2\right)t + \cos\left(\omega_1+2\omega_2\right)t\right) + \frac{3a_3V^3}{4}\left(\cos\left(\omega_1-2\omega_2\right)t + \cos\left(2\omega_1-\omega_2\right)t\right)$$

(18)

The above equation has the following sub parts:

- DC Term : a_2V^2 (19)
- The first order term at frequency ω_1 and ω_2 is given by

$$\left(a_1V + \frac{9a_3V^3}{4} \right)(\cos\omega_1 t + \cos\omega_2 t) \quad (20)$$

- Second-order Terms $(\omega_1+\omega_2, \omega_2 - \omega_1)$ is given by :

$$a_2V^2\left(\cos(\omega_1+\omega_2)t + \cos(\omega_1-\omega_2)t\right) \quad (21)$$

- Third-order Terms $(2\omega_2 - \omega_1, 2\omega_1 - \omega_2, 2\omega_2+\omega_1, 2\omega_1+\omega_2)$ are given by

$$\frac{3a_3V^3}{4}\left(\cos\left(2\omega_1+\omega_2\right)t + \cos\left(\omega_1+2\omega_2\right)t\right) + \frac{3a_3V^3}{4}\left(\cos\left(\omega_1-2\omega_2\right)t + \cos\left(2\omega_1-\omega_2\right)t\right) \quad (22)$$

- Second-order harmonics $(2\omega_1, 2\omega_2)$ are given by

$$\frac{a_2V^2}{2}\left(\cos 2\omega_1 t + \cos 2\omega_2 t\right) \quad (23)$$

- Third-order harmonics $(3\omega_1, 3\omega_2)$ are given by

$$\frac{a_3V^3}{4}\left(\cos 3\omega_1 t + \cos 3\omega_2 t\right) \quad (24)$$

Appendix B

Matlab code

```
clear all; close all; clc;
M = csvread('I_V_characteristics.csv');
Vds = M(:,1); % defining Vds
Vgs = M(1,:);
Vds = Vds(2:end); % Removing the first element i.e. NaN
Vgs = Vgs (2:end);
Ids = M(2:end,2:end); % defining Ids from the matrix. Ids is in A.

% Calculation of gm, gm' and gm" functions using gradient function. _ni used for all the values which are non interpolated.
gm_ni = gradient(Ids,0.25,0.2); % calculation of the gm using the gradient
gm_ni_p = gradient(gm_ni,0.25,0.2); % calculation of the first derivative of gm. p means single prime.
gm_ni_dp = gradient(gm_ni_p,0.25,0.2); % calculation of the second derivative of gm. dp means double prime.

% Interpolation of the gm, gm' and gm"
% Extension of Vgs
Vgs_finer = Vgs(1):0.01:Vgs(end); % done to increase the number of points of Vgs. Vgs_finer is the new Vgs with more points.

for i = 1:1:length(Vds)
   gm_i(i,:) =  interp1(Vgs,gm_ni(i,:),Vgs_finer,'pchip'); % gm_i referes to the interpolated gm (using the PCHIP interpolation).
   gm_i_p(i,:)= interp1(Vgs,gm_ni_p(i,:),Vgs_finer,'pchip'); % interpolation of gm prime
   gm_i_dp(i,:)= interp1(Vgs,gm_ni_dp(i,:),Vgs_finer,'pchip'); % interpolation of gm prime
end
```

```
% Calculation of Error Function without shifting.
gm_i_dpSumAll2Tx = gm_i_dp*2; % Two transistors without shifting.
gm_i_dpSumAll3Tx = gm_i_dp*3; % Three transistors without shifting.
gm_i_dpSumAll4Tx = gm_i_dp*4; % a matrix is added four times with itself to find the minimum.
error_iSumAll1TxSmallRange = rms(gm_i_dp(141,151:451));
error_iSumAll2TxSmallRange = rms(gm_i_dpSumAll2Tx(141,151:451));
error_iSumAll3TxSmallRange = rms(gm_i_dpSumAll3Tx(141,151:451));
error_iSumAll4TxSmallRange = rms(gm_i_dpSumAll4Tx(141,151:451)); % from range -4 to -1V Vgs).

%% Subroutine for column. Shifting the matrix (2Tx)
% Suffix Local for the local calculation.

columnShiftValues2Tx = -175:1:175;
columnShift2TxLocal = 98;
[gm_i_dp_2TxOrgLocal,
gm_i_dp2TxShiftLocal,gm_i_dp_2TxLocal]=ShiftAndAdd_gm_dp4(gm_i_dp,
gm_i_dp,Vgs_finer,columnShift2TxLocal);
Error2Tx_shiftedLocal = rms(gm_i_dp_2TxLocal(141,151:451));

figure(101), plot(Vgs_finer,gm_i_dp_2TxOrgLocal(141,:),'--r','linewidth',2);  hold on; grid on;
plot(Vgs_finer,gm_i_dp2TxShiftLocal(141,:),'--g','linewidth',2);
plot(Vgs_finer,gm_i_dp_2TxLocal(141,:),'b','linewidth',2);
plot(Vgs_finer,gm_i_dpSumAll2Tx(141,:),'^c','linewidth',1); hold off;
legend('Orginal gm'' (Single Tx)','Shifted gm'' (Single Tx)','Sum of 2 gm''(with shifting)',' Sum of 2 gm''(w/o Shifting)'); title('gm'' plot for 2 tranistors (-4V to -1V) using local minima','Fontsize', 16);
set(gca, 'FontSize', 14, 'FontName','Arial','FontWeight','bold'); axis([-5.5 0.5 -1.5 1.5]);
xlabel('Vgs (V)','Fontsize',14); ylabel('gm'' (A/V^3)','Fontsize',14);
```

```
columnShift2Tx = 96;
[gm_i_dp_2TxOrg, gm_i_dp2TxShift,gm_i_dp_2Tx]=ShiftAndAdd_gm_dp4(gm_i_dp,
gm_i_dp,Vgs_finer,columnShift2Tx);
Error2Tx_shifted = rms(gm_i_dp_2Tx(141,151:451));

figure(102), plot(Vgs_finer,gm_i_dp_2TxOrg(141,:),'--r','linewidth',2);  hold on; grid on;
plot(Vgs_finer,gm_i_dp2TxShift(141,:),'--g','linewidth',2);
plot(Vgs_finer,gm_i_dp_2Tx(141,:),'b','linewidth',2);
plot(Vgs_finer,gm_i_dpSumAll2Tx(141,:),'^c','linewidth',1); hold off;
legend('Orginal gm'' (Single Tx)','Shifted gm'' (Single Tx)','Sum of 2 gm''(with shifting)',' Sum of
2 gm''(w/o Shifting)'); title('gm'' plot for 2 tranistors (-4V to -1V) using Absolute
minima','Fontsize', 16);
set(gca, 'FontSize', 14, 'FontName','Arial','FontWeight','bold'); axis([-5.5 0.5 -1.5 1.5]);
xlabel('Vgs (V)','Fontsize',14); ylabel('gm'' (A/V^3)','Fontsize',14);

figure(103),
plot(Vgs_finer,gm_i_dp_2TxLocal(141,:),'-b','linewidth',2); hold on;
plot(Vgs_finer,gm_i_dp_2Tx(141,:),'* m','linewidth',2); hold off; grid on;
xlabel('Vgs (V)','Fontsize',14); ylabel('gm'' (A/V^3)','Fontsize',14);
legend('Sum 2Tx (local Minima)', 'Sum 2Tx (Absolute Minima)'); title('gm'' plot for 2 tranistors (-
4V to -1V)','Fontsize', 16);

figure(104),
plot(Vgs_finer,gm_i_dp_2TxLocal(141,:),'-b','linewidth',2); hold on;
plot(Vgs_finer,gm_i_dp_2Tx(141,:),'* m','linewidth',2);
plot(Vgs_finer,gm_i_dpSumAll2Tx(141,:),'^c','linewidth',1);hold off; grid on;
xlabel('Vgs (V)','Fontsize',14); ylabel('gm'' (A/V^3)','Fontsize',14);
set(gca, 'FontSize', 14, 'FontName','Arial','FontWeight','bold'); axis([-5.5 0.5 -1.5 1.5]);
legend('Sum 2Tx (local Minima)', 'Sum 2Tx (Absolute Minima)', 'Sum w/o shifting'); title('gm''
plot for 2 tranistors (-4V to -1V)','Fontsize', 16);
```

```
%% column shift for adding the third transistor to the sum of the two. (3Tx)
% Error Computation (Best of second + gm_dp for third) (whole range).

columnShiftValues3Tx = -175:1:175;
columnShift3TxLocal = -96;

% Function to find sum of original and shifted matrix
[gm_i_dp_3TxOrgLocal, gm_i_dp_3TxShiftLocal,
gm_i_dp_3TxLocal]=ShiftAndAdd_gm_dp4(gm_i_dp_2TxLocal,
gm_i_dp,Vgs_finer,columnShift3TxLocal);
Error3Tx_shiftedLocal = rms(gm_i_dp_3TxLocal(141,151:451));

% Plot the shifted arrays
figure(201), plot(Vgs_finer,gm_i_dp_3TxOrgLocal(141,:),'--r','linewidth',2); hold on; grid on;
plot(Vgs_finer,gm_i_dp_3TxShiftLocal(141,:),'--g','linewidth',2);
plot(Vgs_finer,gm_i_dp_3TxLocal(141,:),'b','linewidth',2);
plot(Vgs_finer,gm_i_dpSumAll3Tx(141,:),'^c','linewidth',1); hold off;
legend('Sum of 2 gm'' (With Shifting)','Shifted gm'' (Single Tx)','Sum of 3 gm'' (With Shifting)','
Sum of 3 gm'' (W/o Shifting)');
title('gm'' plot for 3 transistors(-4V to -1V) using local minima','Fontsize',16);
xlabel('Vgs (V)','Fontsize',14); ylabel('gm'' (A/V^3)','Fontsize',14); axis([-5.5 0.5 -1.5 1.5]);
set(gca, 'FontSize', 14, 'FontName','Arial','FontWeight','bold');

columnShift3TxAbs = -93;
[gm_i_dp_3TxOrg, gm_i_dp_3TxShift, gm_i_dp_3Tx]=ShiftAndAdd_gm_dp4(gm_i_dp_2Tx,
gm_i_dp,Vgs_finer,columnShift3TxAbs);
Error3Tx_shifted = rms(gm_i_dp_3Tx(141,151:451));

figure(202), plot(Vgs_finer,gm_i_dp_3TxOrg(141,:),'--r','linewidth',2);  hold on; grid on;
plot(Vgs_finer,gm_i_dp_3TxShift(141,:),'--g','linewidth',2);
plot(Vgs_finer,gm_i_dp_3Tx(141,:),'b','linewidth',2);
```

```
plot(Vgs_finer,gm_i_dpSumAll3Tx(141,:),'^c','linewidth',1); hold off;
legend('Orginal gm'' (Single Tx)','Shifted gm'' (Single Tx)','Sum of 2 gm''(with shifting)',' Sum of 2 gm''(w/o Shifting)'); title('gm'' plot for 2 tranistors (-4V to -1V) using Absolute minima','Fontsize', 16);
set(gca, 'FontSize', 14, 'FontName','Arial','FontWeight','bold'); axis([-5.5 0.5 -1.5 1.5]);
xlabel('Vgs (V)','Fontsize',14); ylabel('gm'' (A/V^3)','Fontsize',14);

figure(203),
plot(Vgs_finer,gm_i_dp_3TxLocal(141,:),'-b','linewidth',2); hold on;
plot(Vgs_finer,gm_i_dp_3Tx(141,:),'*m','linewidth',2); hold off; grid on;
xlabel('Vgs (V)','Fontsize',14); ylabel('gm'' (A/V^3)','Fontsize',14);
legend('Sum 3Tx (local Minima)', 'Sum 3Tx (Absolute Minima)'); title('gm'' plot for 3 transistors (-4V to -1V)','Fontsize', 16);

figure(204),
plot(Vgs_finer,gm_i_dp_3TxLocal(141,:),'-b','linewidth',2); hold on;
plot(Vgs_finer,gm_i_dp_3Tx(141,:),'* m','linewidth',2);
plot(Vgs_finer,gm_i_dpSumAll3Tx(141,:),'^c','linewidth',1);hold off; grid on;
xlabel('Vgs (V)','Fontsize',14); ylabel('gm'' (A/V^3)','Fontsize',14);
set(gca, 'FontSize', 14, 'FontName','Arial','FontWeight','bold'); axis([-5.5 0.5 -1.5 1.5]);
legend('Sum 3Tx (local Minima)', 'Sum 3Tx (Absolute Minima)', 'Sum w/o shifting'); title('gm'' plot for 3 tranistors (-4V to -1V)','Fontsize', 16);

%% column shift for adding the third transistor to the sum of the two. (4Tx)
% Error Computation(Best of three + gm_dp for 4th)

columnShiftValues4TxLocal = -200:1:175;
columnShift4TxLocal = -190;
[gm_i_dp_4TxOrgLocal, gm_i_dp_4TxShiftLocal,
gm_i_dp_4TxLocal]=ShiftAndAdd_gm_dp4(gm_i_dp_3TxLocal,
gm_i_dp,Vgs_finer,columnShift4TxLocal);
```

```
Error4Tx_shiftedLocal = rms(gm_i_dp_4TxLocal(141,151:451));


% Plot the shifted arrays
figure(301), plot(Vgs_finer,gm_i_dp_4TxOrgLocal(141,:),'--r','linewidth',2); hold on; grid on;
 plot(Vgs_finer,gm_i_dp_4TxShiftLocal(141,:),'--g','linewidth',2);
plot(Vgs_finer,gm_i_dp_4TxLocal(141,:),'b','linewidth',2);
plot(Vgs_finer,gm_i_dpSumAll4Tx(141,:),'^c','linewidth',1); hold off;
legend('Sum of 3 gm" (With Shifting)','Shifted gm" (single Tx)','Sum of 4 gm" (With Shifting)','
Sum of 4 gm" (W/o Shifting) ');
title('gm" plot for 4 transistors(-4V to -1V) using local minima','Fontsize',16);
xlabel('Vgs (V)','Fontsize',14); ylabel('gm" (A/V^3)','Fontsize',14); axis([-5.5 0.5 -1.5 1.5]);
set(gca, 'FontSize', 14, 'FontName','Arial','FontWeight','bold');


columnShiftValues4Tx = -225:1:175;
columnShift4Tx = -187;
[gm_i_dp_4TxOrg,  gm_i_dp_4TxShift,  gm_i_dp_4Tx]=ShiftAndAdd_gm_dp4(gm_i_dp_3Tx,
gm_i_dp,Vgs_finer,columnShift4Tx);
Error4Tx_shifted = rms(gm_i_dp_4Tx(141,151:451));


% Plot the shifted arrays
figure(302), plot(Vgs_finer,gm_i_dp_4TxOrg(141,:),'--r','linewidth',2); hold on; grid on;
 plot(Vgs_finer,gm_i_dp_4TxShift(141,:),'--g','linewidth',2);
plot(Vgs_finer,gm_i_dp_4Tx(141,:),'b','linewidth',2);
plot(Vgs_finer,gm_i_dpSumAll4Tx(141,:),'^c','linewidth',1); hold off;
legend('Sum of 3 gm" (With Shifting)','Shifted gm" (single Tx)','Sum of 4 gm" (With Shifting)','
Sum of 4 gm" (W/o Shifting)');
title('gm" plot for 4 transistors(-4V to -1V) using absolute minima','Fontsize',16);
xlabel('Vgs (V)','Fontsize',14); ylabel('gm" (A/V^3)','Fontsize',14); axis([-5.5 0.5 -1.5 1.5]);
```

```
set(gca, 'FontSize', 14, 'FontName','Arial','FontWeight','bold');

figure(303),
plot(Vgs_finer,gm_i_dp_4TxLocal(141,:),'-b','linewidth',2); hold on;
plot(Vgs_finer,gm_i_dp_4Tx(141,:),'*m','linewidth',2); hold off; grid on;
xlabel('Vgs (V)','Fontsize',14); ylabel('gm'' (A/V^3)','Fontsize',14);
legend('Sum 4Tx (local Minima)', 'Sum 4Tx (Absolute Minima)'); title('gm'' plot for 4 tranistors (-
4V to -1V)','Fontsize', 16);

figure(304),
plot(Vgs_finer,gm_i_dp_4TxLocal(141,:),'-b','linewidth',2); hold on;
plot(Vgs_finer,gm_i_dp_4Tx(141,:),'* m','linewidth',2);
plot(Vgs_finer,gm_i_dpSumAll4Tx(141,:),'^c','linewidth',1);hold off; grid on;
xlabel('Vgs (V)','Fontsize',14); ylabel('gm'' (A/V^3)','Fontsize',14);
set(gca, 'FontSize', 14, 'FontName','Arial','FontWeight','bold'); axis([-5.5 0.5 -1.5 1.5]);
legend('Sum 4Tx (local Minima)', 'Sum 4Tx (Absolute Minima)', 'Sum w/o shifting'); title('gm''
plot for 4 tranistors (-4V to -1V)','Fontsize', 16);

figure(305),
plot(Vgs_finer,gm_i_dp(141,:),'--r','linewidth',2.5);  hold on;
plot(Vgs_finer,gm_i_dp_2Tx(141,:),'xb','linewidth',1.0);
plot(Vgs_finer,gm_i_dp_3Tx(141,:),'^m','linewidth',1.0);
plot(Vgs_finer,gm_i_dp_4Tx(141,:),'k','linewidth',2.5); hold off;
xlabel('V_{gs} (V)','Fontsize',26,'FontWeight','bold'); ylabel('g_{m}''
(A/V^3)','Fontsize',26,'FontWeight','bold');
set(gca, 'FontSize', 24, 'FontName','Arial','FontWeight','bold');
legend('g_{m}'' single Tx','g_{m}'' two parallel Tx','g_{m}'' three parallel Tx','g_{m}'' four
parallel Tx');
axis([-5.2 -0.5 -0.4 0.32]);
grid on;
```

```
fig305 = figure(305);
plot(Vgs_finer,gm_i_dp(141,:),'--r','linewidth',2.5);  hold on;
plot(Vgs_finer,gm_i_dp_2Tx(141,:),'-xm','linewidth',2.5);
plot(Vgs_finer,gm_i_dp_3Tx(141,:),'-.g','linewidth',2.5);
plot(Vgs_finer,gm_i_dp_4Tx(141,:),'k','linewidth',2.5);
plot(Vgs_finer,gm_i_dpSumAll2Tx(141,:),'^c','linewidth',2.5); hold off;
xlabel('V_{gs} (V)','Fontsize',15,'FontWeight','bold'); ylabel('g_{m}"
(A/V^3)','Fontsize',15,'FontWeight','bold');
set(gca, 'FontSize', 15, 'FontName','Arial','FontWeight','bold');
legend('g_{m}" (0.5mm Tx A)','g_{m}" (A+B)','g_{m}" (A+B+C)','g_{m}"
(A+B+C+D)','g_{m}" (2mm device)','location','southwest');

axis([-5.2 -0.5 -0.8 0.6]);

figure(401),
plot(Vgs_finer,gm_i_dp(141,:),'-.b','linewidth',2); hold on; grid on;
plot(Vgs_finer,gm_i_dp_2TxLocal(141,:),'-.r','linewidth',2);
plot(Vgs_finer,gm_i_dp_3TxLocal(141,:),'-.g','linewidth',2);
plot(Vgs_finer,gm_i_dp_4TxLocal(141,:),'-.m','linewidth',2);
plot(Vgs_finer,gm_i_dpSumAll4Tx(141,:),'^c','linewidth',1);hold off; grid on;
legend('gm" (Single Tx)','gm" (2nd Tx sum)','gm" (3rd Tx sum)',' gm"(4th Tx sum)','gm"(Sum of
4tx w/o shifting)');
title('gm" plot for 4 transistors(-4V to -1V) using local minima','Fontsize',16);
xlabel('Vgs (V)','Fontsize',14); ylabel('gm" (A/V^3)','Fontsize',14); axis([-5.5 0.5 -1.5 1.5]);
set(gca, 'FontSize', 14, 'FontName','Arial','FontWeight','bold');

figure(402),
plot(Vgs_finer,gm_i_dp(141,:),'-.b','linewidth',2); hold on; grid on;
plot(Vgs_finer,gm_i_dp2TxShiftLocal(141,:),'-.r','linewidth',2);
plot(Vgs_finer,gm_i_dp_3TxShiftLocal(141,:),'-.g','linewidth',2);
plot(Vgs_finer,gm_i_dp_4TxShiftLocal(141,:),'-.m','linewidth',2);
```

```
plot(Vgs_finer,gm_i_dp_4TxLocal(141,:),'-.k','linewidth',2);
plot(Vgs_finer,gm_i_dpSumAll4Tx(141,:),'^c','linewidth',1);hold off; grid on;
legend('gm'' (Single Tx)','gm'' (2nd Tx)','gm'' (3rd Tx)',' gm''(4th Tx)','Sum of gm'','gm''(Sum of 4tx W/O shifting)');
title('gm'' plot for 4 transistors(-4V to -1V) using local minima','Fontsize',16);
xlabel('Vgs (V)','Fontsize',14); ylabel('gm'' (A/V^3)','Fontsize',14); axis([-5.5 0.5 -1.5 1.5]);
set(gca, 'FontSize', 14, 'FontName','Arial','FontWeight','bold');

figure(403),  % global minima
plot(Vgs_finer,gm_i_dp(141,:),'-.b','linewidth',2.5); hold on; grid on;
plot(Vgs_finer,gm_i_dp2TxShift(141,:),'-.r','linewidth',2.5);
plot(Vgs_finer,gm_i_dp_3TxShift(141,:),'-.g','linewidth',2.5);
plot(Vgs_finer,gm_i_dp_4TxShift(141,:),'-.m','linewidth',2.5);
hold off; grid on;
legend('gm'' (Single Tx)','gm'' (2nd Tx)','gm'' (3rd Tx)',' gm''(4th Tx)','Sum of gm'','gm''(Sum of 4tx W/O shifting)');
title('gm'' plot for 4 transistors(-4V to -1V) using global minima','Fontsize',22,'FontWeight','bold');
xlabel('Vgs (V)','Fontsize',22); ylabel('gm'' (A/V^3)','Fontsize',22); axis([-5.5 0.5 -1.5 1.5]);
set(gca, 'FontSize', 20, 'FontName','Arial','FontWeight','bold');
```

Appendix C

Taylor Series expansion of the output current from the Nth parallel FET of a non-linear amplifier is given by

$$I_{oN} = a_{1N} I_{iN} + a_{2N} I_{iN}{}^{2} + a_{3N} I_{iN}{}^{3} + \ldots\ldots\ldots\ldots\ldots \quad (1)$$

where I_{oN} is the output current and I_{iN} is the input current of the Nth parallel FET of amplifier circuit.

In this anaylsis , it is assumed that Taylor Series co-efficients have the complex amplitude given by:

$$\begin{aligned} a_{1N} &= A_{1N}(\cos\theta_{1N} + j\sin\theta_{1N}) = A_{1N} e^{j\theta_{1N}} \\ a_{2N} &= A_{2N}(\cos\theta_{2N} + j\sin\theta_{2N}) = A_{2N} e^{j\theta_{2N}} \\ a_{3N} &= A_{3N}(\cos\theta_{3N} + j\sin\theta_{3N}) = A_{3N} e^{j\theta_{3N}} \end{aligned} \quad (2)$$

The magnitude A_{xN} and phase θ_{xN} of these quantities depends on the bias conditions of each individual parallel FETs where x is a number .

Assuming that the two-tone excitation signal with amplitude I_N is applied at the circuit, the input current I_{iN} through each of the parallel FET can be expressed as

$$I_{iN} = I_N \left(\cos(\omega_1 t + \phi_1) + \cos(\omega_2 t + \phi_2)\right) \quad (3)$$

ϕ_1 and ϕ_2 are the phases of the two input signals at frequencies ω_1 and ω_2 respectively.

The input current from equation (3) can be modified as follows:

Using the Euler's identity,

$$\begin{aligned} \cos(\omega_1 t + \phi_1) &= \frac{1}{2}\left(e^{j(\omega_1 t + \phi_1)} + e^{-j(\omega_1 t + \phi_1)}\right) \\ \cos(\omega_2 t + \phi_2) &= \frac{1}{2}\left(e^{j(\omega_2 t + \phi_2)} + e^{-j(\omega_2 t + \phi_2)}\right) \end{aligned} \quad (4)$$

And substituting,

$$\begin{aligned} \kappa_1 &= \omega_1 t + \phi_1 \\ \kappa_2 &= \omega_2 t + \phi_2 \\ \cos(\kappa_1) &= \frac{1}{2}\left(e^{j\kappa_1} + e^{-j\kappa_1}\right) \\ \cos(\kappa_2) &= \frac{1}{2}\left(e^{j\kappa_2} + e^{-j\kappa_2}\right) \end{aligned} \quad (5)$$

Using the above equations, the input signal can be written as

$$I_{iN} = I_N\left(\cos(\kappa_1) + \cos\left(\kappa_2\right)\right) \tag{6}$$

So on substituting, the input signal can be written as

$$I_{iN} = \frac{I_N}{2}\left(e^{j\kappa_1} + e^{-j\kappa_1} + e^{j\kappa_2} + e^{-j\kappa_2}\right) \tag{7}$$

On substituting (7), (2) in (1) and solving for I_{oN}, we get the following result

$$\begin{aligned} I_{oN} &= A_{1N}e^{j\theta_{1N}}\left\{\frac{I_N}{2}\left(e^{j\kappa_1} + e^{-j\kappa_1} + e^{j\kappa_2} + e^{-j\kappa_2}\right)\right\} + A_{2N}e^{j\theta_{2N}}\left\{\frac{I_N}{2}\left(e^{j\kappa_1} + e^{-j\kappa_1} + e^{j\kappa_2} + e^{-j\kappa_2}\right)\right\}^2 \\ &+ A_{3N}e^{j\theta_{3N}}\left\{\frac{I_N}{2}\left(e^{j\kappa_1} + e^{-j\kappa_1} + e^{j\kappa_2} + e^{-j\kappa_2}\right)\right\}^3 + \text{.....} \end{aligned} \tag{8}$$

This term can be simplified into three parts as

$$I_{oN} = \alpha + \beta + \gamma \tag{9}$$

where each of the parts is as given below

$$\begin{aligned} \alpha &= A_{1N}e^{j\theta_{1N}}\left\{\frac{I_N}{2}\left(e^{j\kappa_1} + e^{-j\kappa_1} + e^{j\kappa_2} + e^{-j\kappa_2}\right)\right\} \\ \beta &= A_{2N}e^{j\theta_{2N}}\left\{\frac{I_N}{2}\left(e^{j\kappa_1} + e^{-j\kappa_1} + e^{j\kappa_2} + e^{-j\kappa_2}\right)\right\}^2 \\ \gamma &= A_{3N}e^{j\theta_{3N}}\left\{\frac{I_N}{2}\left(e^{j\kappa_1} + e^{-j\kappa_1} + e^{j\kappa_2} + e^{-j\kappa_2}\right)\right\}^3 \end{aligned} \tag{10}$$

Solving for α, the following expression is obtained:

$$\begin{aligned} \alpha &= A_{1N}e^{j\theta_{1N}}\left\{\frac{I_N}{2}\left(e^{j\kappa_1} + e^{-j\kappa_1} + e^{j\kappa_2} + e^{-j\kappa_2}\right)\right\} \\ \alpha &= \frac{A_{1N}I_N}{2}\left\{e^{j\kappa_1 + j\theta_{1N}} + e^{-j\kappa_1 + j\theta_{1N}} + e^{j\kappa_2 + j\theta_{1N}} + e^{-j\kappa_2 + j\theta_{1N}}\right\} \end{aligned} \tag{11}$$

On substituting the values of $\kappa_1 = \omega_1 t + \phi_1$ and $\kappa_2 = \omega_2 t + \phi_2$ in (11), α can be written as

$$\alpha = \frac{A_{1N}I_N}{2}\left\{e^{j(\omega_1 t + \phi_1 + \theta_{1N})} + e^{-j(\omega_1 t + \phi_1 - \theta_{1N})} + e^{j(\omega_2 t + \phi_2 + \theta_{1N})} + e^{-j(\omega_2 t + \phi_2 - \theta_{1N})}\right\} \tag{12}$$

Solving for β

$$\beta = A_{2N}e^{j\theta_{2N}}\left\{\frac{I_N}{2}\left(e^{j\kappa_1} + e^{-j\kappa_1} + e^{j\kappa_2} + e^{-j\kappa_2}\right)\right\}^2 \tag{13}$$

On applying the expansion formula given by

$$\begin{aligned}&(a+b+c+d)^2 = a^2+b^2+c^2+d^2+2ab+2bc+2cd+2ad+2ac+2bd\\&a=e^{j\kappa_1}, b=e^{-j\kappa_1}, c=e^{j\kappa_2}, d=e^{-j\kappa_2}\end{aligned} \tag{14}$$

β can be written as

$$\beta = A_{2N}e^{j\theta_{2N}}\left(\frac{I_N}{2}\right)^2\left(e^{j2\kappa_1}+e^{-j2\kappa_1}+e^{j2\kappa_2}+e^{-j2\kappa_2}+2+2e^{(-j\kappa_1+j\kappa_2)}+2+2e^{(j\kappa_1-j\kappa_2)}+2e^{(j\kappa_1+j\kappa_2)}+2e^{-(j\kappa_1+j\kappa_2)}\right) \tag{15}$$

$$\beta = A_{2N}\left(\frac{I_N}{2}\right)^2\begin{pmatrix}e^{j(2\kappa_1+\theta_{2N})}+e^{-j(2\kappa_1-\theta_{2N})}+e^{j(2\kappa_2+\theta_{2N})}+e^{-j(2\kappa_2-\theta_{2N})}+4e^{j\theta_{2N}}+2e^{j(-\kappa_1+\kappa_2+\theta_{2N})}\\+2e^{j(\kappa_1-\kappa_2+\theta_{2N})}+2e^{j(\kappa_1+\kappa_2+\theta_{2N})}+2e^{-j(\kappa_1+\kappa_2-\theta_{2N})}\end{pmatrix} \tag{16}$$

On substituting the values of $\kappa_1 = \omega_1 t+\phi_1$ and $\kappa_2 = \omega_2 t+\phi_2$ in (16), following expression is obtained:

$$\beta = \frac{A_{2N}{I_N}^2}{4}\begin{pmatrix}e^{j(2\omega_1 t+2\phi_1+\theta_{2N})}+e^{-j(2\omega_1 t+2\phi_1-\theta_{2N})}+e^{j(2\omega_2 t+2\phi_2+\theta_{2N})}+e^{-j(2\omega_2 t+2\phi_2-\theta_{2N})}+2e^{-j(\omega_1 t-\omega_2 t+\phi_1-\phi_2-\theta_{2N})}+\\2e^{j(\omega_1 t-\omega_2 t+\phi_1-\phi_2+\theta_{2N})}+2e^{j(\omega_1 t+\omega_2 t+\phi_1+\phi_2+\theta_{2N})}+2e^{-j(\omega_1 t+\omega_2 t+\phi_1+\phi_2-\theta_{2N})}+4e^{j\theta_{2N}}\end{pmatrix} \tag{17}$$

Solving for γ

$$\gamma = A_{3N}e^{j\theta_{3N}}\left(\frac{I_N}{2}\right)^3\left(e^{j\kappa_1}+e^{-j\kappa_1}+e^{j\kappa_2}+e^{-j\kappa_2}\right)^3 \tag{18}$$

By applying the expansion formula,

$$\begin{aligned}&(a+b+c+d)^3 = a^3+b^3+c^3+d^3+3a^2b+3ab^2+3cd^2+3c^2d+3a^2c+3b^2c+3a^2d+\\&3b^2d+3ac^2+3ad^2+3bc^2+3bd^2+6abc+6abd+6acd+6bcd\\&a=e^{j\kappa_1}, b=e^{-j\kappa_1}, c=e^{j\kappa_2}, d=e^{-j\kappa_2}\end{aligned} \tag{19}$$

$$\gamma = A_{3N}e^{j\theta_{3N}}\left(\frac{I_N}{2}\right)^3\begin{pmatrix}e^{j3\kappa_1}+e^{-j3\kappa_1}+e^{j3\kappa_2}+e^{-j3\kappa_2}+3e^{j\kappa_1}+3e^{-j\kappa_1}+3e^{-j\kappa_2}+3e^{j\kappa_2}+3e^{j(2\kappa_1+\kappa_2)}+\\3e^{j(-2\kappa_1+\kappa_2)}+3e^{j(2\kappa_1-\kappa_2)}+3e^{-j(2\kappa_1+\kappa_2)}+3e^{j(\kappa_1+2\kappa_2)}+3e^{j(\kappa_1-2\kappa_2)}+3e^{j(-\kappa_1+2\kappa_2)}\\+3e^{-j(\kappa_1+2\kappa_2)}+6e^{j\kappa_2}+6e^{-j\kappa_2}+6e^{j\kappa_1}+6e^{-j\kappa_1}\end{pmatrix} \tag{20}$$

$$\gamma = A_{3N}\left(\frac{I_N}{2}\right)^3 \begin{pmatrix} e^{j(3\kappa_1+\theta_{3N})} + e^{j(-3\kappa_1+\theta_{3N})} + e^{j(3\kappa_2+\theta_{3N})} + e^{j(-3\kappa_2+\theta_{3N})} + 3e^{j(\kappa_1+\theta_{3N})} + 3e^{j(-\kappa_1+\theta_{3N})} \\ +3e^{j(-\kappa_2+\theta_{3N})} + 3e^{j(\kappa_2+\theta_{3N})} + 3e^{j(2\kappa_1+\kappa_2+\theta_{3N})} + 3e^{j(-2\kappa_1+\kappa_2+\theta_{3N})} + 3e^{j(2\kappa_1-\kappa_2+\theta_{3N})} \\ +3e^{j(-2\kappa_1-\kappa_2+\theta_{3N})} + 3e^{j(\kappa_1+2\kappa_2+\theta_{3N})} + 3e^{j(\kappa_1-2\kappa_2+\theta_{3N})} + 3e^{j(-\kappa_1+2\kappa_2+\theta_{3N})} + \\ 3e^{j(-\kappa_1-2\kappa_2+\theta_{3N})} + 6e^{j(\kappa_2+\theta_{3N})} + 6e^{j(-\kappa_2+\theta_{3N})} + 6e^{j(\kappa_1+\theta_{3N})} + 6e^{j(-\kappa_1+\theta_{3N})} \end{pmatrix} \tag{21}$$

On substituting the values of κ_1 and κ_2 given by $\kappa_1 = \omega_1 t + \phi_1$ and $\kappa_2 = \omega_2 t + \phi_2$, in equation (21), the following expression is obtained:

$$\gamma = A_{3N}\left(\frac{I_N}{2}\right)^3 \begin{pmatrix} e^{j(3\omega_1 t+3\phi_1+\theta_{3N})} + e^{j(-3\omega_1 t-3\phi_1+\theta_{3N})} + e^{j(3\omega_2 t+3\phi_2+\theta_{3N})} + e^{j(-3\omega_2 t-3\phi_2+\theta_{3N})} + 3e^{j(\omega_1 t+\phi_1+\theta_{3N})} \\ +3e^{j(-\omega_1 t-\phi_1+\theta_{3N})} + 3e^{j(-\omega_2 t-\phi_2+\theta_{3N})} + 3e^{j(\omega_2 t+\phi_2+\theta_{3N})} + 3e^{j(2\omega_1 t+2\phi_1+\omega_2 t+\phi_2+\theta_{3N})} \\ +3e^{j(-2\omega_1 t-2\phi_1+\omega_2 t+\phi_2+\theta_{3N})} + 3e^{j(2\omega_1 t+2\phi_1-\omega_2 t-\phi_2+\theta_{3N})} + 3e^{j(-2\omega_1 t-2\phi_1-\omega_2 t-\phi_2+\theta_{3N})} \\ +3e^{j(\omega_1 t+\phi_1+2\omega_2 t+2\phi_2+\theta_{3N})} + 3e^{j(\omega_1 t+\phi_1-2\omega_2 t-2\phi_2+\theta_{3N})} + 3e^{j(-\omega_1 t-\phi_1+2\omega_2 t+2\phi_2+\theta_{3N})} \\ +3e^{j(-\omega_1 t-\phi_1-2\omega_2 t-2\phi_2+\theta_{3N})} + 6e^{j(\omega_2 t+\phi_2+\theta_{3N})} + 6e^{j(-\omega_2 t-\phi_2+\theta_{3N})} \\ +6e^{j(\omega_1 t+\phi_1+\theta_{3N})} + 6e^{j(-\omega_1 t-\phi_1+\theta_{3N})} \end{pmatrix} \tag{22}$$

$$\gamma = A_{3N}\left(\frac{I_N}{2}\right)^3 \begin{pmatrix} e^{j(3\omega_1 t+3\phi_1+\theta_{3N})} + e^{-j(3\omega_1 t+3\phi_1-\theta_{3N})} + e^{j(3\omega_2 t+3\phi_2+\theta_{3N})} + e^{-j(3\omega_2 t+3\phi_2-\theta_3)} + 3e^{j(\omega_1 t+\phi_1+\theta_{3N})} \\ +3e^{-j(\omega_1 t+\phi_1-\theta_{3N})} + 3e^{-j(\omega_2 t+\phi_2-\theta_{3N})} + 3e^{j(\omega_2 t+\phi_2+\theta_{3N})} + 3e^{j(2\omega_1 t+\omega_2 t+2\phi_1+\phi_2+\theta_{3N})} \\ +3e^{j(-2\omega_1 t+\omega_2 t-2\phi_1+\phi_2+\theta_{3N})} + 3e^{j(2\omega_1 t+2\phi_1-\omega_2 t-\phi_2+\theta_{3N})} + 3e^{j(-2\omega_1 t-2\phi_1-\omega_2 t-\phi_2+\theta_{3N})} \\ +3e^{j(\omega_1 t+\phi_1+2\omega_2 t+2\phi_2+\theta_{3N})} + 3e^{j(\omega_1 t+\phi_1-2\omega_2 t-2\phi_2+\theta_{3N})} + 3e^{j(-\omega_1 t-\phi_1+2\omega_2 t+2\phi_2+\theta_{3N})} \\ +3e^{j(-\omega_1 t-\phi_1-2\omega_2 t-2\phi_2+\theta_{3N})} + 6e^{j(\omega_2 t+\phi_2+\theta_{3N})} + 6e^{j(-\omega_2 t-\phi_2+\theta_{3N})} + 6e^{j(\omega_1 t+\phi_1+\theta_{3N})} + 6e^{j(-\omega_1 t-\phi_1+\theta_{3N})} \end{pmatrix} \tag{23}$$

$$\gamma = \frac{A_{3N} I_N}{8}^3 \begin{pmatrix} e^{j(3\omega_1 t+3\phi_1+\theta_{3N})} + e^{-j(3\omega_1 t+3\phi_1-\theta_{3N})} + e^{j(3\omega_2 t+3\phi_2+\theta_{3N})} + e^{-j(3\omega_2 t+3\phi_2-\theta_{3N})} + 9e^{j(\omega_2 t+\phi_2+\theta_{3N})} \\ +9e^{-j(\omega_2 t+\phi_2-\theta_{3N})} + 9e^{j(\omega_1 t+\phi_1+\theta_{3N})} + 9e^{-j(\omega_1 t+\phi_1-\theta_{3N})} + 3e^{j(2\omega_1 t+\omega_2 t+2\phi_1+\phi_2+\theta_{3N})} \\ +3e^{-j(2\omega_1 t+\omega_2 t+2\phi_1+\phi_2-\theta_{3N})} + 3e^{j(2\omega_1 t-\omega_2 t+2\phi_1-\phi_2+\theta_{3N})} + 3e^{-j(2\omega_1 t-\omega_2 t+2\phi_1-\phi_2-\theta_{3N})} \\ +3e^{j(\omega_1 t-2\omega_2 t+\phi_1-2\phi_2+\theta_{3N})} + 3e^{-j(\omega_1 t-2\omega_2 t+\phi_1-2\phi_2-\theta_{3N})} + 3e^{j(\omega_1 t+2\omega_2 t+\phi_1+2\phi_2+\theta_{3N})} + 3e^{-j(\omega_1 t+2\omega_2 t+\phi_1+2\phi_2-\theta_{3N})} \end{pmatrix} \tag{24}$$

On combining all the above terms and placing in the equation $I_{oN} = \alpha + \beta + \gamma$

$$I_{oN}=\frac{A_{1N}I_N}{2}\left(e^{j(\omega_1t+\phi_1+\theta_{1N})}+e^{-j(\omega_1t+\phi_1-\theta_{1N})}+e^{j(\omega_2t+\phi_2+\theta_{1N})}+e^{-j(\omega_2t+\phi_2-\theta_{1N})}\right)+$$
$$\frac{A_{2N}I_N{}^2}{4}\left(\begin{array}{l}e^{j(2\omega_1t+2\phi_1+\theta_{2N})}+e^{-j(2\omega_1t+2\phi_1-\theta_{2N})}+e^{j(2\omega_2t+2\phi_2+\theta_{2N})}+e^{-j(2\omega_2t+2\phi_2-\theta_{2N})}+2e^{-j(\omega_1t-\omega_2t+\phi_1-\phi_2-\theta_{2N})}+\\2e^{j(\omega_1t-\omega_2t+\phi_1-\phi_2+\theta_{2N})}+2e^{j(\omega_1t+\omega_2t+\phi_1+\phi_2+\theta_{2N})}+2e^{-j(\omega_1t+\omega_2t+\phi_1+\phi_2-\theta_{2N})}+4e^{j\theta_{2N}}\end{array}\right)+$$
$$\frac{A_{3N}I_N{}^3}{8}\left(\begin{array}{l}e^{j(3\omega_1t+3\phi_1+\theta_{3N})}+e^{-j(3\omega_1t+3\phi_1-\theta_{3N})}+e^{j(3\omega_2t+3\phi_2+\theta_{3N})}+e^{-j(3\omega_2t+3\phi_2-\theta_{3N})}+9e^{j(\omega_2t+\phi_2+\theta_{3N})}\\+9e^{-j(\omega_2t+\phi_2-\theta_{3N})}+9e^{j(\omega_1t+\phi_1+\theta_{3N})}+9e^{-j(\omega_1t+\phi_1-\theta_{3N})}+3e^{j(2\omega_1t+\omega_2t+2\phi_1+\phi_2+\theta_{3N})}+\\3e^{-j(2\omega_1t+\omega_2t+2\phi_1+\phi_2-\theta_{3N})}+3e^{j(2\omega_1t-\omega_2t+2\phi_1-\phi_2+\theta_{3N})}+3e^{-j(2\omega_1t-\omega_2t+2\phi_1-\phi_2-\theta_{3N})}\\+3e^{j(\omega_1t-2\omega_2t+\phi_1-2\phi_2+\theta_{3N})}+3e^{-j(\omega_1t-2\omega_2t+\phi_1-2\phi_2-\theta_{3N})}+3e^{j(\omega_1t+2\omega_2t+\phi_1+2\phi_2+\theta_{3N})}+3e^{-j(\omega_1t+2\omega_2t+\phi_1+2\phi_2-\theta_{3N})}\end{array}\right)$$

(25)

On simplifying we get the following expression,

$$I_{oN}=A_{2N}I_N{}^2e^{j\theta_{2N}}+\frac{A_{1N}I_N}{2}\left(e^{j(\omega_1t+\phi_1+\theta_{1N})}+e^{-j(\omega_1t+\phi_1-\theta_{1N})}+e^{j(\omega_2t+\phi_2+\theta_{1N})}+e^{-j(\omega_2t+\phi_2-\theta_{1N})}\right)+$$
$$\frac{9A_{3N}I_N{}^3}{8}\left(e^{j(\omega_2t+\phi_2+\theta_{3N})}+e^{-j(\omega_2t+\phi_2-\theta_{3N})}+e^{j(\omega_1t+\phi_1+\theta_{3N})}+e^{-j(\omega_1t+\phi_1-\theta_{3N})}\right)+$$
$$\frac{A_{2N}I_N{}^2}{4}\left(\begin{array}{l}e^{j(2\omega_1t+2\phi_1+\theta_{2N})}+e^{-j(2\omega_1t+2\phi_1-\theta_{2N})}+e^{j(2\omega_2t+2\phi_2+\theta_{2N})}+e^{-j(2\omega_2t+2\phi_2-\theta_{2N})}+2e^{-j(\omega_1t-\omega_2t+\phi_1-\phi_2-\theta_{2N})}+\\2e^{j(\omega_1t-\omega_2t+\phi_1-\phi_2+\theta_{2N})}+2e^{j(\omega_1t+\omega_2t+\phi_1+\phi_2+\theta_{2N})}+2e^{-j(\omega_1t+\omega_2t+\phi_1+\phi_2-\theta_{2N})}\end{array}\right)+$$
$$\frac{A_{3N}I_N{}^3}{8}\left(\begin{array}{l}e^{j(3\omega_1t+3\phi_1+\theta_{3N})}+e^{-j(3\omega_1t+3\phi_1-\theta_{3N})}+e^{j(3\omega_2t+3\phi_2+\theta_{3N})}+e^{-j(3\omega_2t+3\phi_2-\theta_{3N})}+\\3e^{j(2\omega_1t+\omega_2t+2\phi_1+\phi_2+\theta_{3N})}+3e^{-j(2\omega_1t+\omega_2t+2\phi_1+\phi_2-\theta_{3N})}+3e^{j(2\omega_1t-\omega_2t+2\phi_1-\phi_2+\theta_{3N})}+3e^{-j(2\omega_1t-\omega_2t+2\phi_1-\phi_2-\theta_{3N})}+\\3e^{j(\omega_1t-2\omega_2t+\phi_1-2\phi_2+\theta_{3N})}+3e^{-j(\omega_1t-2\omega_2t+\phi_1-2\phi_2-\theta_{3N})}+3e^{j(\omega_1t+2\omega_2t+\phi_1+2\phi_2+\theta_{3N})}+3e^{-j(\omega_1t+2\omega_2t+\phi_1+2\phi_2-\theta_{3N})}\end{array}\right)$$

(26)

The above equation has the following sub parts:

DC Term: $A_{2N}I_N{}^2e^{j\theta_{2N}}$ (27)

The first-order term is given by

$$\frac{A_{1N}I_N}{2}\left(e^{j(\omega_1t+\phi_1+\theta_{1N})}+e^{-j(\omega_1t+\phi_1-\theta_{1N})}+e^{j(\omega_2t+\phi_2+\theta_{1N})}+e^{-j(\omega_2t+\phi_2-\theta_{1N})}\right)+$$
$$\frac{9A_{3N}I_N{}^3}{8}\left(e^{j(\omega_1t+\phi_1+\theta_{3N})}+e^{-j(\omega_1t+\phi_1-\theta_{3N})}+e^{j(\omega_2t+\phi_2+\theta_{3N})}+e^{-j(\omega_2t+\phi_2-\theta_{3N})}\right) \quad (28)$$

The second order terms are given by

$$\frac{A_{2N}{I_N}^2}{4}\begin{pmatrix} e^{j(2\omega_1 t+2\phi_1+\theta_{2N})}+e^{-j(2\omega_1 t+2\phi_1-\theta_{2N})}+e^{j(2\omega_2 t+2\phi_2+\theta_{2N})}+e^{-j(2\omega_2 t+2\phi_2-\theta_{2N})}+2e^{-j(\omega_1 t-\omega_2 t+\phi_1-\phi_2-\theta_{2N})}+ \\ 2e^{j(\omega_1 t-\omega_2 t+\phi_1-\phi_2+\theta_{2N})}+2e^{j(\omega_1 t+\omega_2 t+\phi_1+\phi_2+\theta_{2N})}+2e^{-j(\omega_1 t+\omega_2 t+\phi_1+\phi_2-\theta_{2N})} \end{pmatrix}$$

(29)

And the third-order term is given by

$$\frac{A_{3N}{I_N}^3}{8}\begin{pmatrix} e^{j(3\omega_1 t+3\phi_1+\theta_{3N})}+e^{-j(3\omega_1 t+3\phi_1-\theta_{3N})}+e^{j(3\omega_2 t+3\phi_2+\theta_{3N})}+e^{-j(3\omega_2 t+3\phi_2-\theta_{3N})}+ \\ 3e^{j(2\omega_1 t+\omega_2 t+2\phi_1+\phi_2+\theta_{3N})}+3e^{-j(2\omega_1 t+\omega_2 t+2\phi_1+\phi_2-\theta_{3N})}+3e^{j(2\omega_1 t-\omega_2 t+2\phi_1-\phi_2+\theta_{3N})}+3e^{-j(2\omega_1 t-\omega_2 t+2\phi_1-\phi_2-\theta_{3N})}+ \\ 3e^{j(\omega_1 t-2\omega_2 t+\phi_1-2\phi_2+\theta_{3N})}+3e^{-j(\omega_1 t-2\omega_2 t+\phi_1-2\phi_2-\theta_{3N})}+3e^{j(\omega_1 t+2\omega_2 t+\phi_1+2\phi_2+\theta_{3N})}+3e^{-j(\omega_1 t+2\omega_2 t+\phi_1+2\phi_2-\theta_{3N})} \end{pmatrix}$$

(30)

The IMD3 Components of the FET are given by

$$\frac{3A_{3N}{I_N}^3}{8}\begin{pmatrix} e^{j(2\omega_1 t+\omega_2 t+2\phi_1+\phi_2+\theta_{3N})}+e^{-j(2\omega_1 t+\omega_2 t+2\phi_1+\phi_2-\theta_{3N})}+e^{j(2\omega_1 t-\omega_2 t+2\phi_1-\phi_2+\theta_{3N})}+e^{-j(2\omega_1 t-\omega_2 t+2\phi_1-\phi_2-\theta_{3N})}+ \\ e^{j(\omega_1 t-2\omega_2 t+\phi_1-2\phi_2+\theta_{3N})}+e^{-j(\omega_1 t-2\omega_2 t+\phi_1-2\phi_2-\theta_{3N})}+e^{j(\omega_1 t+2\omega_2 t+\phi_1+2\phi_2+\theta_{3N})}+e^{-j(\omega_1 t+2\omega_2 t+\phi_1+2\phi_2-\theta_{3N})} \end{pmatrix}$$

(31)