Impact of Inert-electrode on the Performance and Electro-thermal Reliability of ReRAM Memory Array

Mohammad Shah Al-Mamun

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Marius K. Orlowski, Chair
Louis J. Guido
Ahmad Safaai-Jazi
Xiaoting Jia
Gary R. Pickrell

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ABSTRACT

While the scaling of conventional memories based on floating gate MOSFETs is getting increasingly difficult, novel type of non-volatile memories, such as resistive switching memories, have lately found increased attention by both industry and academia. Resistive switching memory (ReRAM) is being considered one of the prime candidates for next-generation non-volatile memory due to relatively high switching speed, superior scalability, low power consumption, good retention and simplicity of its structure which does not require the expensive real estate structure of the silicon substrate. Furthermore, integration of ReRAM directly into a CMOS low-k/Cu interconnect module would not only reduce latency in connectivity constrained devices, but also would reduce chip's footprint by stacking memory layers on top of the logic circuits. One good candidate is the well-behaved $Cu/TaOx/Pt$ resistive switching device. However, since platinum (Pt) acting as the inert electrode is not an economic choice for industrial production, a Back End of Line (BEOL)-compatible replacement of Pt is highly desirable. A systematic investigation has been conducted and metals such as Ru, Rh and Ir are found to be the best potential candidates to supplant Pt. The device properties of Ru, Rh and Ir based resistive switching devices have been explored in this work. However, the challenges of implementing ReRAM cell into BEOL of CMOS encompass not only the choice of materials of a CBRAM cell proper, but also the way the cell is embedded within BEOL. In case of the inert electrode, the metal interfacing the solid electrolyte (e.g. TaOx) has to be supplanted

by a glue layer, and heat transport layer, leading to an engineering task of a composite electrode beyond the requirements of low miscibility with, and low surface diffusivity of the inert electrode with respect of the active metal atoms released by the active electrode (here Cu). The metal of the active electrode (Cu, Ag, Ni) is required to allow for a copious redox reaction but simultaneously preventing reactions with the dielectric. Finally, for the solid electrolyte, a dielectric with a moderate level of defects is preferred which may be controlled, for example by the deposition processes modulating the stoichiometry of the material.

This research study begins with exploration of several devices derived from the benchmark device Cu/TaOx/Pt and manufacturing those in Micron nanofabrication and characterization laboratory at Virginia Tech with the latter device used as a benchmark for performance assessment. Electric characterization of the manufactured Cu/TaOx/Ru devices has shown some notable differences between them due to the different formation, shape and rupture of the conductive filament. The inferior switching properties of the Ru device have been attributed to the substantially degraded inertness properties of the Ru electrode as a stopping barrier for Cu as compared to the Pt electrode. To study this degradation effect further, two nominally identical devices however differently embedded on the Si wafer have been fabricated. The electric behavior of the two devices are found to be markedly different and is attributed to the difference in high local temperatures in the device during the switching that cause species interlayer diffusion and trigger undesired chemical reactions. Thus, the embedment of the device has a foremost impact on the intrinsic device performance. To investigate the impact of inert electrode on the endurance of ReRAM memory cells, baseline device Cu/TaOx/Pt/Ti is compared with six devices

manufactured with different inert electrode constructions: Pt/Cr, Rh/Cr, Rh/Ti, Rh/Al$_2$O$_3$, Ir/Ti, and Ir/Cr, while the Cu electrode and the TaO$_x$ dielectric are identical. Although the glue layers Ti, Cr or Al$_2$O$_3$ are not an inherent part of the device proper, they have a tangible impact on the device endurance as well. It is experimentally demonstrated that inert electrodes with high thermal conductivities have superior endurance properties over an electrode with low thermal conductivity and the heat conductivity of inert electrode has a substantial impact on ReRAM cell performance. Since reset operation is a thermally driven process, frequent switching of resistive memory cell leads to a local accumulation of Joules heat, especially when the switching rate is faster than the heat removal rate.

This investigation of local heating effects led to the exploration of non-local heat transfer within a memory array. In a crossbar arranged ReRAM cell array, heat generated in one device spreads via common electrode metal lines to the neighboring cells causing their performance degradation constituting non-local heat transfer mechanism leading to performance deterioration of neighboring cells. In addition to the electrical characterization of devices affected by the remote heat transfer, novel cell array architectures have been proposed and investigated with the goal to significantly mitigate the cell-to-cell thermal crosstalk. One of the possible mitigation measures would be modified cell erasure algorithm.

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GENERAL AUDIENCE ABSTRACT

Emerging memory technologies are being intensively investigated for extending Moore's scaling law in the next decade. The resistive random-access memory (ReRAM) is one of the most propitious contenders to replace the current ubiquitous FLASH memory. ReRAM shows unique nanoionics based filamentary switching mechanism. Compared to the current nonvolatile memory based on floating gate MOSFET transistor, the advantages of ReRAM include superior scalability, low power consumption, high OFF-/ON-state resistance ratio, excellent endurance, and long retention of the logic bit states. Besides the nonvolatile memory applications, resistive switching devices implement the function of a memristor which is the fourth basic electrical component and can be used for neuromorphic computing.

A ReRAM device is in essence a metal-insulator-metal structure. One of the metal electrodes is called the active electrode and provides the building material for the filamentary connection between the electrodes. An important requirement of the second electrode, called the inert electrode, is to be immiscible with the metal atoms of the active electrode and to exhibit a minimum of susceptibility to structural changes and chemical reactions. This research presents a thorough investigation of the role and properties of the inert electrode and offers guideline for the optimal selection of the inert electrode in a commercially viable product. It has been found out that one important property of the inert electrode is its heat conductivity and also the way the inert electrode is embedded on a

substrate. Consequently, the concept of the inert electrode has been replaced by the concept of engineered inert electrode module which evolved from a single metal layer to a multilayer stack displaying glue layers, high thermal conductivity layers dissipating the heat quickly, and diffusion stop layers eliminating unwanted chemical reactions.

The investigation of the electro-thermal effects led to the discovery of the cell-to-cell thermal cross talk within the memory array which can seriously affect the performance of cells impacted by the remote heat transfer. When a memory cell is switched repeatedly a considerable amount of heat is dissipated in the cell and the heat may spread to neighboring cells that share the same metal lines. This heat transfer causes degradation of electrical performance of the neighboring cells. A method has been developed to characterize quantitatively how the electrical performance is affected by the thermal cross-talk impacting the electric performance of neighboring cells. Several novel mitigation strategies of new memory array architectures have been proposed and investigated.

To my parents, wife and daughter

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Table of Contents

x

Table of Figures

xvi

List of Tables

Chapter 1: Motivation and Background

1.1   Introduction

Since the very beginning of mankind, people have been very interested about history and desperately desired to preserve knowledge ad information using numerous medium and transfer it to the upcoming future generations. Memory is the object which is used to store that information and prevent it from obliteration over a time span that can range several million years. From early
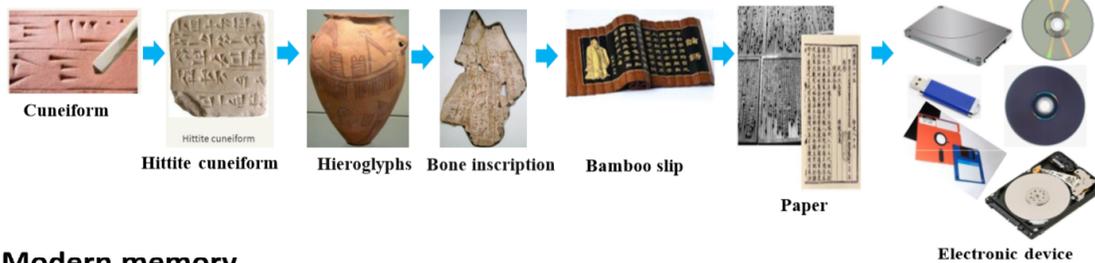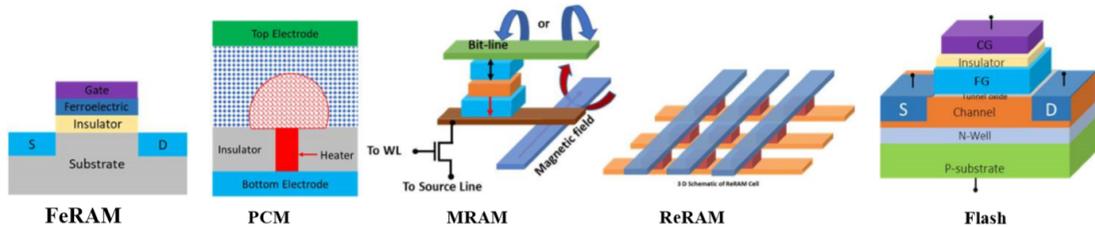
Fig. 1.1: *a) Evolution of memory; b) Emerging modern memory [1-12]*

ancient to modern high-tech days, humankind have come a long way for the emergence of storage system, which is probably one of the most significant landmarks achieved in the history of human civilization. Around 3500-3000 BCE, the first ever writing system named cuneiform was developed by Sumerians of Mesopotamia [1]. The word 'cuneiform' comes from Latin 'wedge' and corresponds to the wedge style writing pattern. This wedge-like pictogram was generated by pressing a stylus against the soft clay which is then sun-dried [1]. To use more characters the

cuneiform was simplified in the third millennium and consisted of both "consonantal alphabetic and syllabic signs" [1]. Then over the years 'Phoenician Alphabet' supplanted that. Characters are then used in the 'pictorial writing' system which is widely known as Egyptian Hieroglyphs [1]. Hieroglyphs came from Greek origin 'hiero' (mean holy) and 'glypho' (means writing). In the ancient Egyptian time it was believed that these are 'the God's word'. Then over the duration of human history, the storing media has advanced from cuneiform, knots, hieroglyphs, slates, carved bones, painted rocks, bronze inscription etc. to modern era selectron tube, punch cards, magnetic

Fig. 1.2: Emerging applications of memory technologies [15-17]

drum memory, magnetic tape, DECtape, Hard Disk Drive (HDD), laser disk, floppy disk, Compact Disk (CD), Digital Versatile Disc (DVD), Blu-ray Disc (BD), Solid State Drive (SSD) etc. [13-14]. Figure 1.1 summarizes the historical evolution of memory along with several key emerging memory technologies.

The semiconductor-based memory has been significantly flourishing over the last few years due to ever-increasing demand for data storage. The current trend of "portable electronics" demands extremely high density, low power and ultra-fast memory solutions. The current trend of
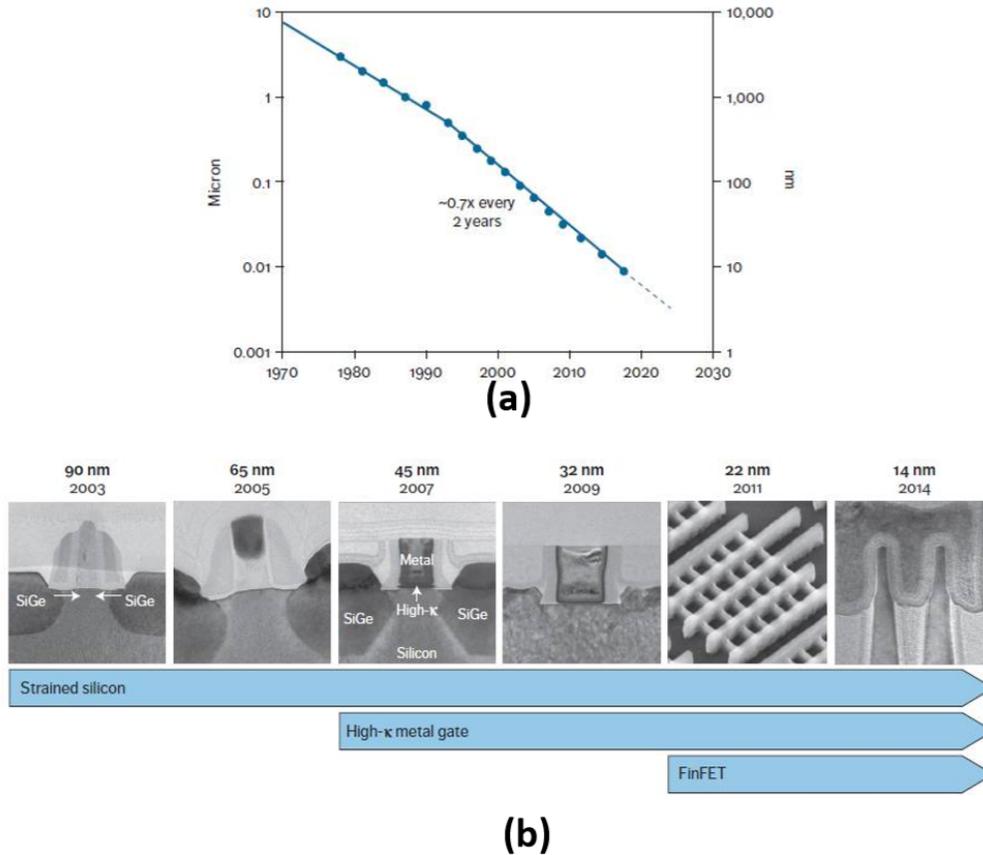
Fig. 1.3: *a) Minimum feature size scaling trend for Intel logic transistors; b) Several generations of Intel transistors.* Reprinted with permission from [18], copyright IEEE (2017)

Artificial Intelligence (AI), Autonomous Vehicle, Internet of Things (IOT) etc. have brought the innovative memory technology into the center of attention with unprecedented demand that is ever predicted. Figure 1.2 summarizes some of the key applications of modern emerging memory technologies. The current state of the art memories is rapidly reaching their physical limitation of scaling and thus will create a prevailing technological challenge for future advancement at the

current faster rate. Figure 1.3 (a) and (b) illustrates the logic transistor scaling trend as well as several generations of intel transistors respectively. Besides, in the current system architecture the memory and logic circuitry are placed in separate locations and long interconnection lines connect them. Therefore, the chip footprint is larger and there is inherently long interconnect delay between Memory and Logic [19]. So, the performance of the processor becomes increasingly limited by
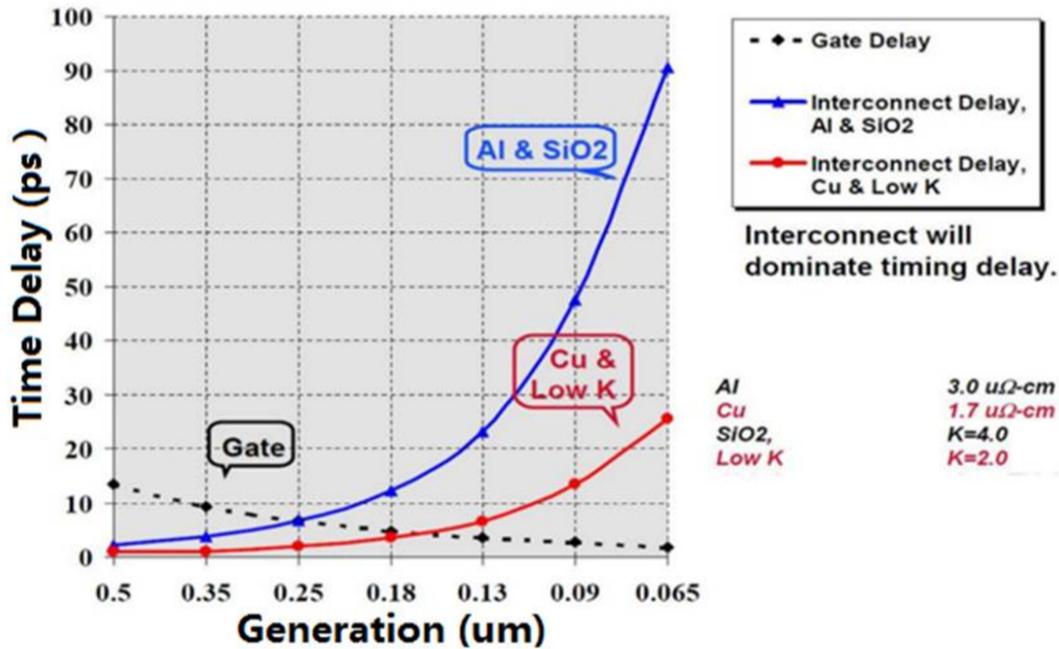
Fig. 1.4: Interconnect vs. Gate delay trend with technology scaling. Reprinted with permission from [19], copyright IEEE (1997)

the access-time delay and higher power consumption of the memory subsystem. Figure 1.4 shows the Interconnect vs. Gate delay trend with the technology scaling. Therefore, to ensure continuous advancement of speed and reduction of power consumption by several orders of magnitude a completely different and revolutionary fundamental change in the memory subsystem need to be adapted.

Recently there has been remarkable research and advancement efforts to develop plethora of innovative techniques to meet the demand for digital-era memory system. Numerous novel memory architecture with new materials have been proposed for the continuation of the next generation of memory growth. Among the various emerging memory technologies, Resistive Switching Memory or ReRAM is one of the most promising candidates in this regard. ReRAM technology can potentially solve this issue by vertically integrating memory above the logic into the 'Backend' of CMOS. A schematic diagram illustrating the future ReRAM device integration into the CMOS BEOL is shown in Fig. 1.5. Due to its excellent scaling capability, ultra-fast
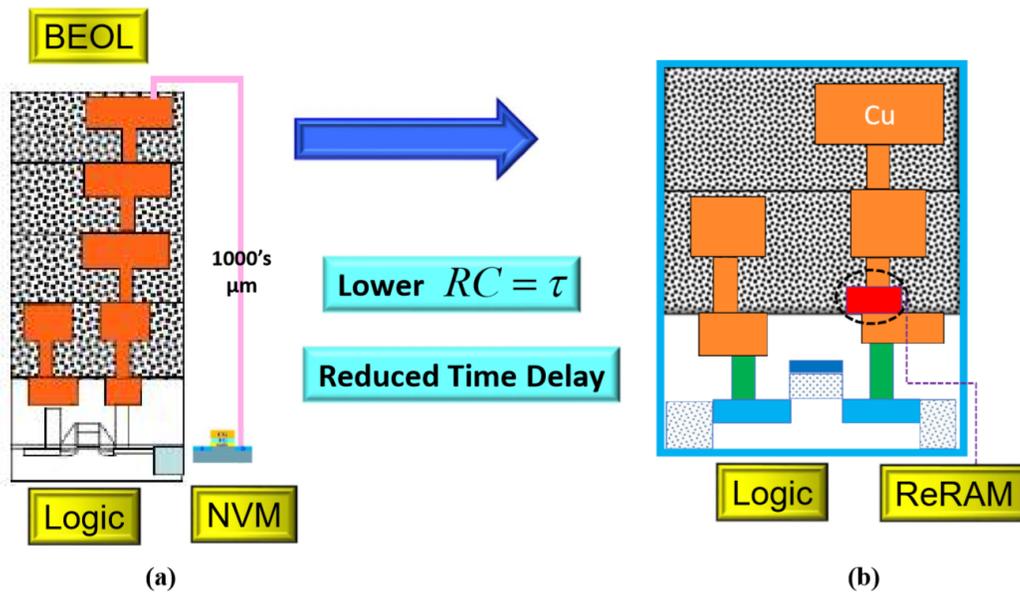
Fig. 1.5: Integration of ReRAM into CMOS BEOL would potentially reduce latency between logic-

switching ability compared to conventional memories and superior CMOS compatibility, ReRAM could an ideal choice for next generation of high-density memory integration. The investigation

and root cause analysis of performance, endurance and reliability issues of ReRAM cell and several potential solutions to remarkedly improve the functionality of ReRAM through experimental demonstration is the objective of this dissertation.

1.2 Memory Technologies

Semiconductor memories can be classified into two main groups:

i. Volatile memory

ii. Non-Volatile memory

Volatile memory is the type of memory which loses its stored content when the power supply is turned OFF. DRAM and SRAM are volatile memory. Non-volatile memory on the other hand can preserve its stored content even when the power supply is turned OFF. Flash memory (NAND,
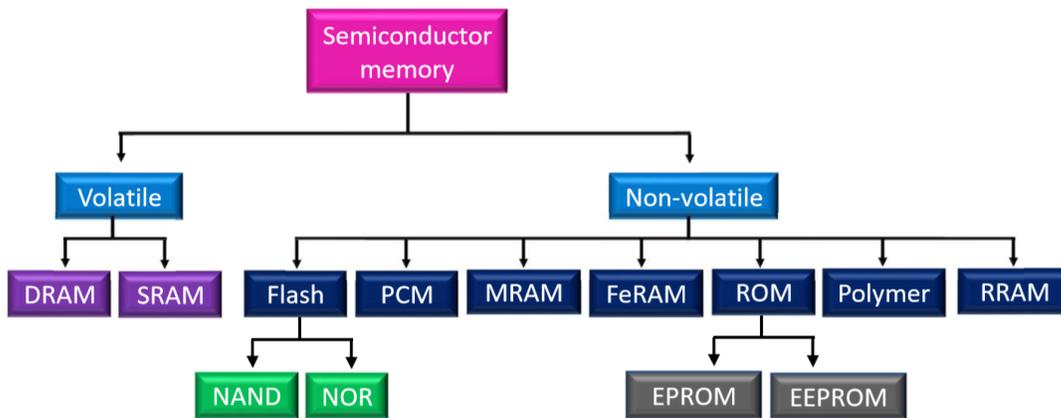
Fig. 1.6: *Classification of semiconductor memories [20]*

NOR), PCM, FeRAM, RRAM etc. are non-volatile memory. The classification of commonly known semiconductor memories is shown using Fig 1.6.

6

Again, depending on read/write capability semiconductor memory can be divided into the following two types:

i. RAM (Random-Access Memory)

ii. ROM (Read-Only Memory)

Random-Access Memories (RAM) are volatile in nature where for both read and write operations can be conducted at a faster rate and data can be accessed at individual bit-level. However, Read-Only Memories (ROM) are high-density, non-volatile memory which are generally written once and then read for many times. The write operation of ROM cells require unusually high electrical voltage and their erase operation is very cumbersome as they require the memory chips to be physically removed from the circuit and expose to ultra-violet (UV) ray. This type of memories is usually preferred for read-only applications. Based-on nature of power requirement the non-volatile memories can be classified as two types: -

i. SRAM (Static Random-Access Memory)

ii. DRAM (Dynamic Random-Access Memory)

Static Random-Access Memories can preserve data as long as the power supply is applied to the memory cells. On the other hand, Dynamic Random-Access Memory cells must be periodically refreshed (periodically re-write data content) to retain its memory content. DRAM consumes more power than SRAM. Several key memory technologies along with their principle of operation are described here.

1.2.1 SRAM (Static Random-Access Memory)

SRAM is static random-access memory which can store information as long as it is connected to the power supply. This type of memory does not require periodic refreshment to

retain its stored information like DRAM. SRAM is very fast, immune to noise, have low leakage current and consumes less power at low-frequency operation compared to DRAM. It does not have any capacitor to charge or discharge like DRAM and therefore SRAM is much faster than DRAM. But, its memory density is low due to larger cell area and power consumption is comparable to DRAM when running at relatively higher frequency. SRAM is primarily used for cache memory Among the various types of SRAM, six transistor SRAM (6Ts) is the most commonly used due to its higher capacity and better robustness characteristics [21]. Its one-bit SRAM memory cell is a latch circuit with two CMOS inverters consists of four transistors (T_2, T_3, T_4, T_5) and is connected in a cross-coupled back-to-back way, the output of one inverter is connected to the input of the other inverter. The remaining two transistors are called as access or pass transistors. The data stored in the latch circuit can be accessed through the access transistors (T_3 and T_6) connected with the bit lines (BLs). The access transistor can be turned ON or OFF by applying voltage to its gate electrode through word lines (WLs). Memory bits are stored within these 2 cross-couple inverters and depending on the state of the latch, the stored memory can be interpreted as "logic 0" or "logic 1". The schematic connection of 6T SRAM is shown in Fig. 1.7. The operating characteristics of SRAM cell can be divided as: write operation, read operation and data retention with power supply ON. During the write operation the existing information within the SRAM cell is modified according to the desired information to be stored. In the read operation, the stored information in the cell is accessed through the BLs without any modification to the existing stored bit. The write and read operations of SRAM are illustrated in detail below [21].

1.2.1.1 Write operation

The write operation of SRAM can primarily consist of any of the following situations:

i.   **Scenario 1:** 'Logic 0' needs to be stored in memory cell when 'logic 1' is already stored

ii. **Scenario 2:** 'Logic 1' needs to be stored in memory cell when 'logic 0' is already stored

SRAM write operation for both scenarios are illustrated below:

Scenario 1:

There are two bit-lines (BL_1 and BL_2) in SRAM memory cell and can be seen in Fig 1.7. They are pre-charged to opposite voltage level during the onset of write operation of SRAM cell,
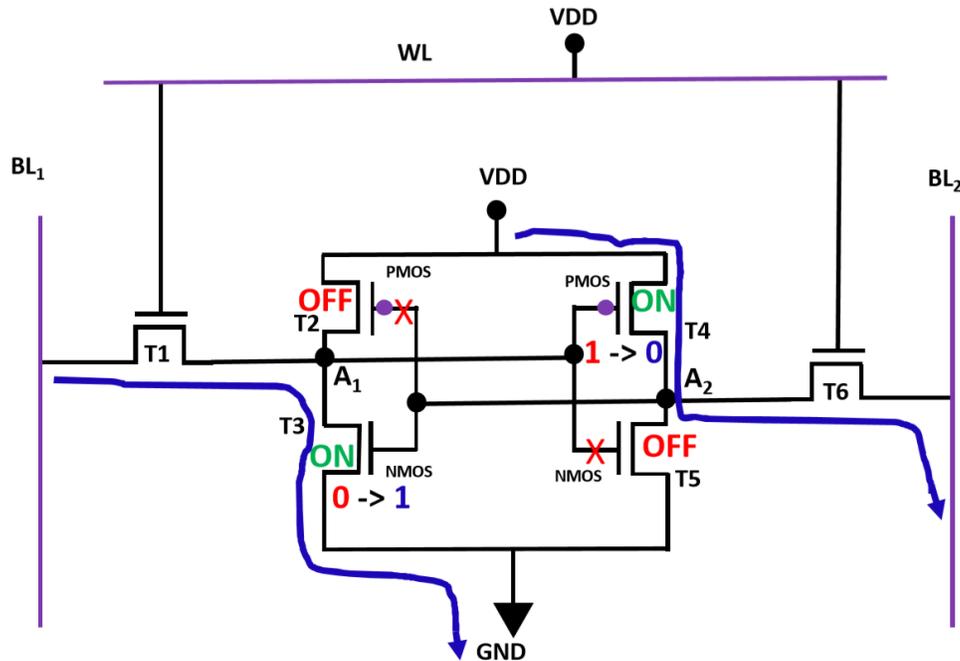
Fig. 1.7*: Write operation for bit '1' from initially stored bit '0' at node A_1 (similarly storing bit '0' from initially stored bit '1' at node A_2) and corresponding current path and voltage at node A_1 and A_2 in a SRAM cell [21]*

V_{DD} and GND. For example, '1' needs to be written at node A_1 of SRAM cell, but it is already loaded with '0'. So, BL_1 is pre-charged to V_{DD} while BL_2 is pre-charged to GND. Then the word line (or word lines) of the cells to be written are selected and V_{DD} is applied. This turns ON the pass transistor of the corresponding cells. Since '0' already exists in the memory cell, node A_1 has

'0' and node 'A$_2$' has '1'. Let's consider '0' corresponds to GND and '1' corresponds to voltage V$_{DD}$. So, transistor T$_3$ and T$_4$ is ON while transistor T$_2$ and T$_5$ is OFF. Now, current flows through path BL$_1$-T$_1$-A$_1$-T$_3$ and path V$_{DD}$-T$_4$-A$_2$-T$_6$-BL$_2$ and is shown in Fig. 1.7. As a consequence, voltage at A$_1$ increases and voltage at node A$_2$ decreases. This process continues until the reduction of voltage at node A$_2$ reaches to the point to turn ON transistor T$_2$ and turn OFF transistor T$_3$ as
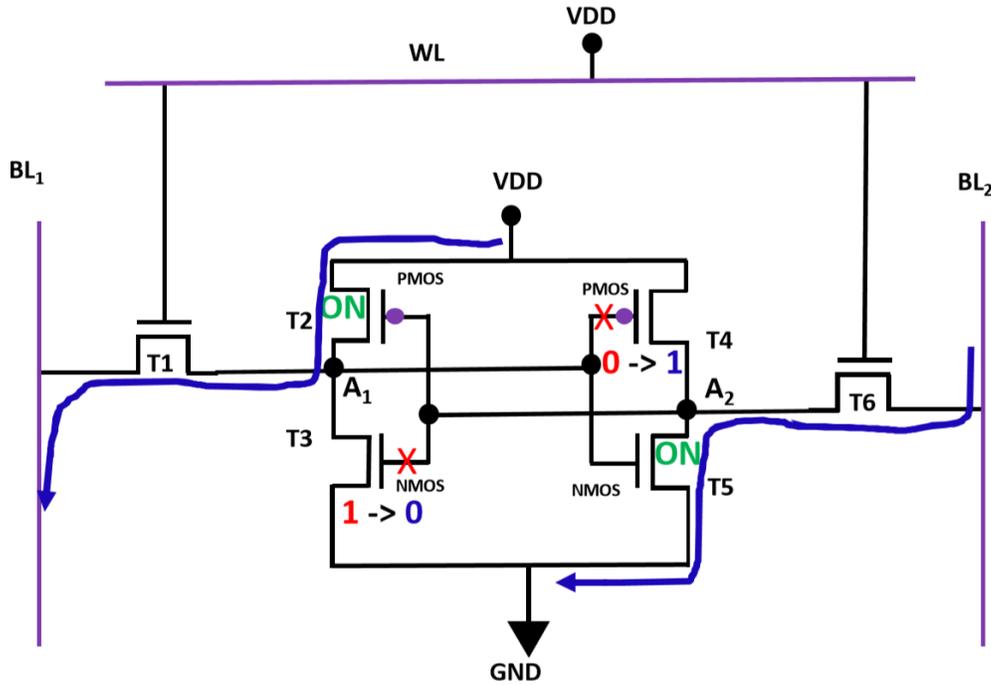
Fig. 1.8: *Write operation for bit '0' from initially stored bit '1' at node A$_1$ (similarly storing bit '1' from initially stored bit '0' at node A$_2$) and corresponding current path and voltage at node A$_1$ and A$_2$ in a SRAM cell [21]*

well as voltage increment of node A$_1$ reaches to the point to turn OFF T$_4$ and turn ON T$_5$. At this point voltage at node A$_1$ and A$_2$ are high (V$_{DD}$) and low (GND) respectively which correspond to 'logic 1' and 'logic 0' respectively. It can be noticed that the memory bit at node A$_1$ and A$_2$ are modified from initial bit '0' to '1' (for A$_1$) and bit '1' to '0' (for A$_2$) respectively.

Scenario 2:

Now let's consider bit '1' and bit '0' is initially stored at node A_1 and A_2 respectively and bit '0' and bit '1' needs to be stored at node A_1 and A_2 respectively. Bit lines BL_1 and BL_2 are pre-charged to GND and V_{DD} respectively and pass transistors are turned ON through corresponding WLs by applying appropriate voltages. Transistor T_2 and T_5 are ON, while T_3 and T_4 are OFF. So, current flows through path V_{DD}-T_2-A_1-T_1 and path BL_2-T_6-A_2-T_5 and is shown in Fig. 1.8. This causes voltage at node A_1 to decease and A_2 to increase till the reduced voltage level at A_1 turns ON T_4 and turns OFF T_5 as well as increased voltage level at A_2 turns OFF T_2 and turns ON T_3. Therefore bit '0' and bit '1' are stored at node A_1 and A_2 respectively by altering initially stored bit '1' and '0' respectively.

1.2.1.2   Read operation

READ operation is the retrieving of stored information within the memory cell. Unlike DRAM, SRAM read operation is non-destructive which means the stored bit is read without flipping or modifying its content. Let's consider the situation when 'bit 0' is stored at node A_1 and needs to be read. The process starts with pre-charging both the bit lines to same voltage level V_{DD} (unlike write operation which required two bit-lines to be pre-charged to opposite voltage levels). Pass transistors corresponding to the cells to be read are turned ON by applying appropriate voltage through the WLs. Since 'bit 0' is stored in the memory cell (consequently bit 1 is stored at node A_2), voltage at node A_1 and A_2 are GND and V_{DD} respectively. So, Transistors T_2 and T_5 are OFF while T_3 and T_4 are ON. After turning ON pass transistors, current flows through path BL_1-T_1-A_1-T_3 by discharging bit-line BL_1. However, no voltage-drop exist across pass transistor T_6 and as a result no current flows through T6 (bit-line BL_2 has pre-charged voltage V_{DD} and voltage at node

11

A_2 is also V_{DD}). Due to discharging of BL_1, its voltage can reduce from V_{DD} to $V_{DD}-\Delta V$. On the other hand, BL_2 voltage is unchanged as it does not discharge. Therefore, by sensing the voltage difference between bit-lines BL_1 ($V_{DD}-\Delta V$) and BL_2 (V_{DD}), the stored information (bit 0 at node A_1 in this case) can be detected. Figure 1.9 shows reading operation for stored 'bit 0' at node A_1
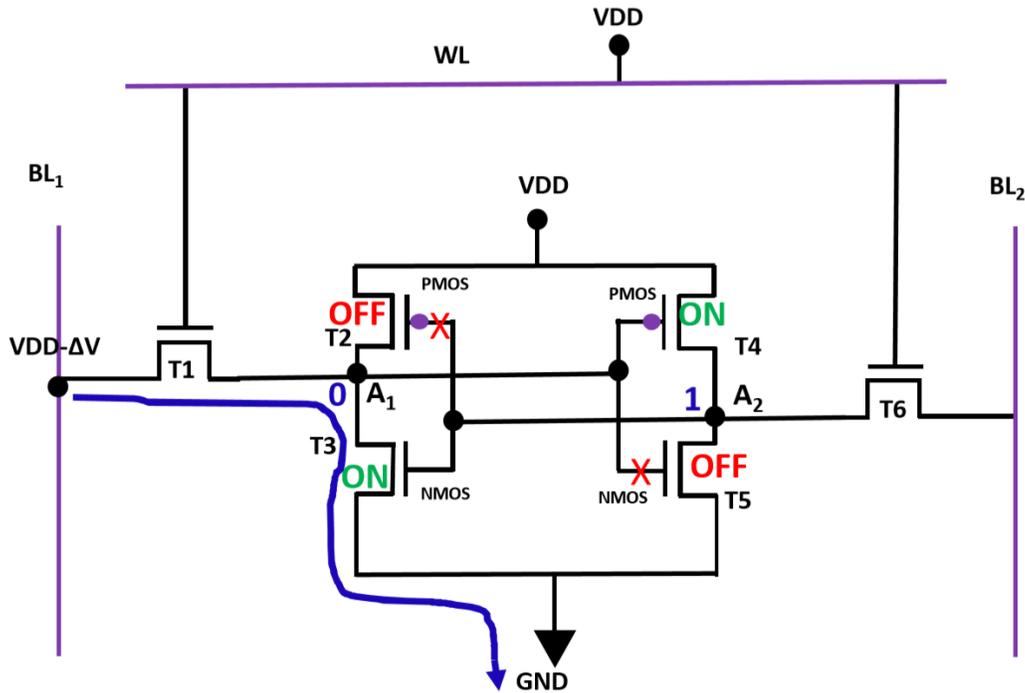
Fig. 1.9: *READ operation of stored bit '0' at node A_1 and corresponding current path and voltage levels at various nodes in a SRAM cell [21]*

schematically.

Similarly, to read the stored 'bit 1' at node A_1, both bit-lines are pre-charged to V_{DD} and corresponding pass transistors are ON through WLs. Since 'bit 1' is stored at node A_1, voltage at node A_1 and A_2 are V_{DD} and GND respectively. Therefore, transistors T_2 and T_5 are ON, while T_3 and T_4 are OFF. Right after pass transistors are tuned ON, current flows through path BL_2-T_6-A_2-T_5. But there is no potential drop across pass transistor T1 and hence no current flows through it.

So BL_2 discharges from V_{DD} to $V_{DD}-\Delta V$ while BL_1 remains unchanged. Now the voltage difference between bit-lines are having opposite polarity compared to the previous case (when bit 0 is stored at node A_1) which can be sensed to read the stored information (bit 1 at node A_1). Figure 1.10 shows read operation for 'bit 1' at node A_1.

However, during discharging of BL_1 for reading 'bit 0' at node A_1 (BL_2 for reading 'bit 1'
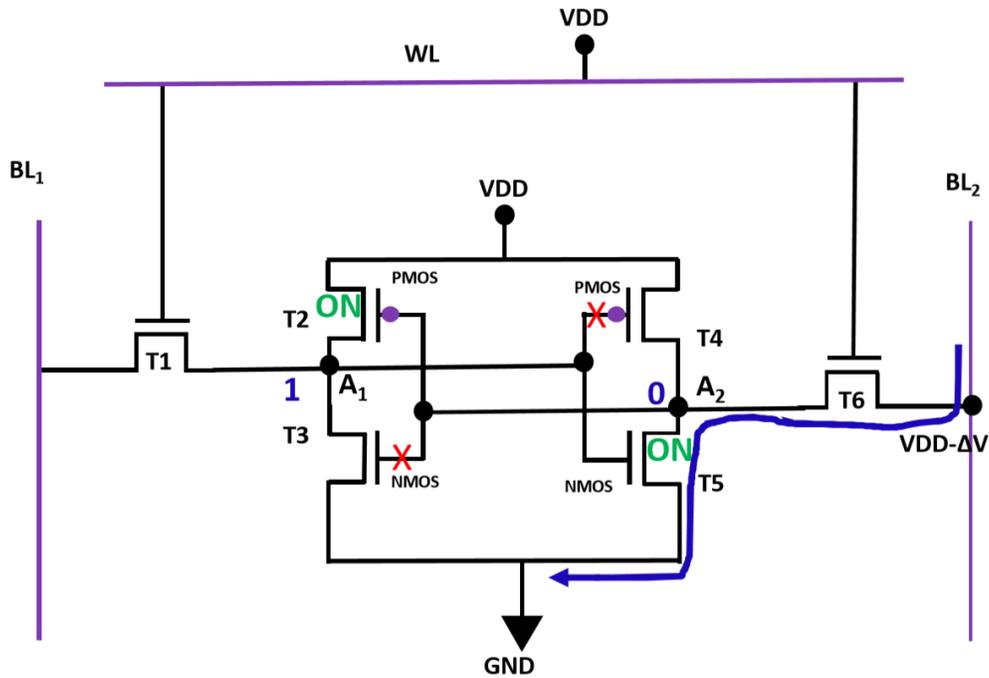
Fig. 1.10: *READ operation of stored bit '1' at node A_1 and corresponding current path and voltage levels at various nodes in a SRAM cell [21]*

at node A_1) voltage at node A_1 can be increased by a smaller amount (node A_2 for reading 'bit 1') unless T_3 is capable of carrying more current than pass transistor T_1 (T_5 than pass transistor T_6). If this happenes, it would reverse the stored bit information by turning ON T_5 and turning OFF T_4 (turning ON T_3 and turning OFF T_2 for Fig. 1.10) and would create read operation stability issues. This stability can be ensured by ensuring a strong cell ratio or beta ratio ($\beta =$

$\frac{T_3}{T_1}$ $in\ figure\ 1.9\ or\ \beta = \frac{T_5}{T_6}$ $in\ figure\ 1.10.$) [21]. Here T_1 and T_6 are pass transistors. For similar transistor technology, both T_3 and T_4 have identical mobility and therefore this beta ratio translates into physical dimension of the corresponding transistors [21]. Although SRAMs are very fast, they are volatile. Due to large number of transistors required per memory cell of SRAM, it is difficult to realize high density memory system with SRAM. It is therefore used where highly reliable and extremely fast memory is required, such as in cache memory.

1.2.2 DRAM (Dynamic Random-Access Memory)

DRAM is the dynamic random-access memory which can store data temporarily and is a widely popular type of random-memory access memory (RAM) used in computer micro-processor. Its memory is volatile in nature and the data is lost if it is not periodically re-written or refreshed. DRAM technology has significantly evolved over the past few decades and its major
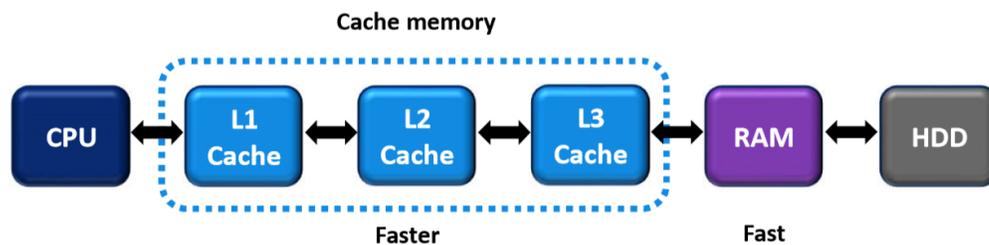
Fig. 1.11: *Process flow schematic for memory components connected in computer architecture*

technological advances lead to a broader range of applications, such as servers, cell phones, global positioning systems, tablets, desktop computers, digital cameras, smart TVs, routers etc. Figure 1.11 shows the types of memories used within the computer architecture. Here, RAM is used as a main memory. Since SRAM is much faster than DRAM, it is used as a cache memory. Hard Disk

Drive (HDD) has mechanical moving components within it and DRAM is much faster than HDD. It is both cheaper and much denser than SRAM, but slower compared to SRAM.

A single DRAM cell usually stores 1 bit of information and contains one transistor and one capacitor. The memory is stored in the form of charging state of the capacitor. By detecting the state of the capacitor (charged or discharged), the stored bit (1 or 0) can be identified. The capacitor is usually accessed through a transistor connected to it and that transistor is commonly termed as pass transistor. The gate and drain/source end of the pass transistor is connected to word line (WL) and bit line (BL) respectively. To read or write a stored bit, the pass transistor is turned on. In ideal
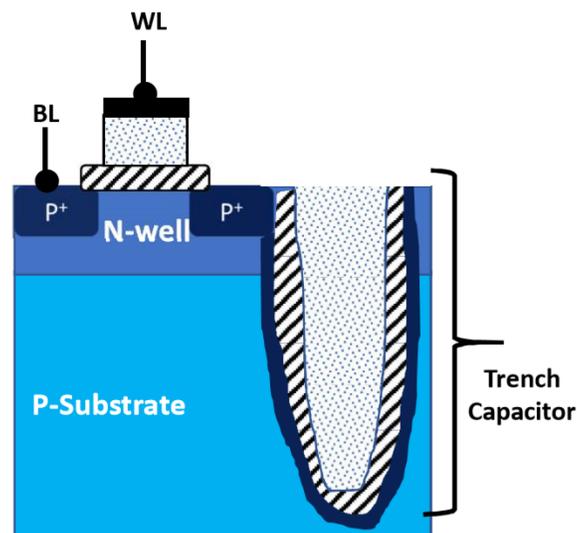
Fig. 1.12: *Schematic cross section of a DRAM memory cell [22]*

case, when the pass transistor is off the capacitor should keep its existing charge if it is pre-charged. However, in reality the capacitor gradually loses its stored charge through leaking mechanism due to pass transistor's sub-threshold current. Therefore, even if the capacitor is pre-charged it will spontaneously lose its charge. So, for a pre-charged capacitor the charged state can only be maintained if it is periodically recharged to that state. This is the reason why DRAM is volatile

15

and need to be refreshed periodically. The schematic cross section of a DRAM cell is shown in Fig. 1.12. The read and write operations of a DRAM cell is illustrated below.

1.2.2.1 Write operation

The write operation starts with selecting the appropriate cells to write. The corresponding bit lines are pre-charged to a pre-defined voltage level. Then the pass transistor is turned on by supplying voltage to word line (WL). Now, the capacitor has a continuous connection path to bit line (BL) and can be charged to the pre-charged bit line voltage level. The writing speed of a
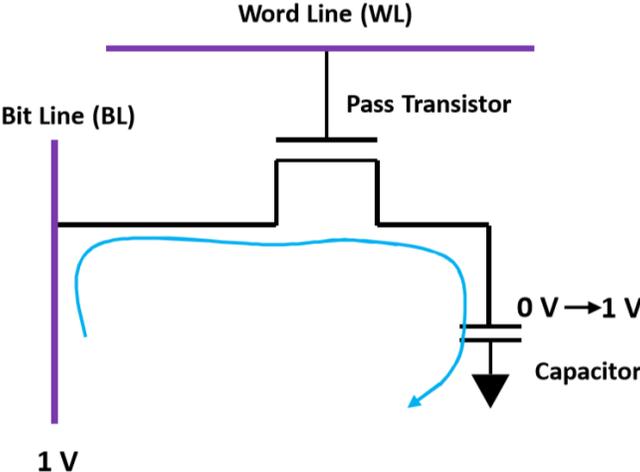
Fig. 1.13: *Write operation schematic of a DRAM memory cell*

DRAM cell depends on how quickly the capacitor can be charged. A schematic of write operation and capacitor charging path is shown in Fig. 1.13.

1.2.2.2 Read operation

The purpose of read operation is to find the charging state of the capacitor; whether it is charged or discharged. At first the pass transistor is turned on by applying appropriate voltage to

WL. The existing voltage state of the capacitor is then available to the bit lines. The voltage is then sensed through a sense amplifier. But, during this reading process the capacitor actually loses its charge as it discharges through this path. Therefore, this reading process is destructive. After every reading cycle the capacitor needs to be refreshed to restore the capacitor to its original charge state to retain its memory status. This process is relatively slow since it would take some time to fully charge the BLs to the charging state of the capacitor. To make this process faster, the capacitor can be pre-charged to some finite voltage level. For example, if the capacitor is charged to 2V and the BLs are pre-charged to 1V it would take less time to charge the BLs from 1V to 2V compared to its charging duration from 0V to 2V. Now, the increasing (if capacitor is in charged state) or decreasing (if capacitor is in discharged state) trend can be sensed and the signal can be
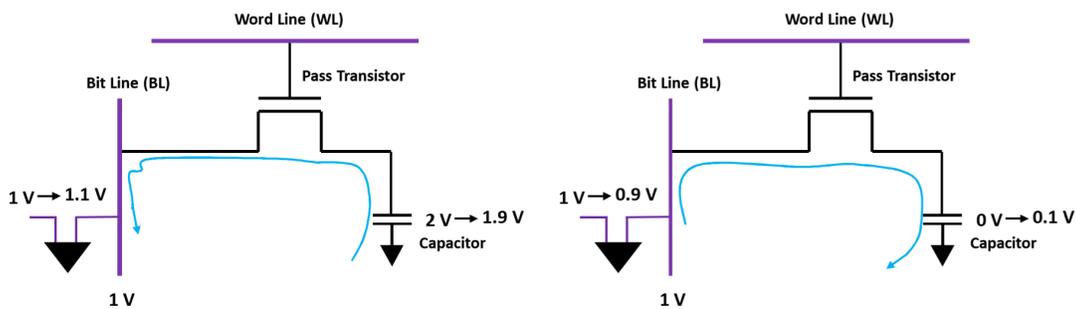
Fig. 1.14: Read-operation schematic of a DRAM memory cell: a) increasing trend when capacitor was in charged state; b) decreasing trend when capacitor was in discharged state

amplified by sense amplifier. By adopting this reading strategy, the read operation can be made even faster and can therefore significantly reduce the read-time for dynamic random-access memory. The read process is schematically illustrated in Fig. 1.14.

In summary, DRAMs are volatile, and their read operation is destructive. This memory system also requires periodic refresh (re-write memory content) at every few milliseconds. DRAM

therefore consumes high power. However, DRAM is a promising solution for very high -density

and high capacity memory system. Both volatile memory (SRAM & DRAM) are compared

Table 1.1: Comparison: SRAM vs. DRAM [23]

Feature	SRAM	DRAM
Density	Low	High
No of transistor in unit cell	6	1
Application	Cache memory	RAM
Cost/bit	Expensive	Cheaper than SRAM
Speed	Very fast	Fast

in Table 1.1.

1.2.3 MRAM (Dynamic Random-Access Memory)

MRAM is the Magnetoresistive Random-Access Memory which stores data in the form of

stable magnetic charges in contrast to the electrical charges used in conventional technologies like

DRAM and SRAM. MRAM is based on the phenomenon that application of magnetic field

changes the resistance of magnetoresistive materials. These magnetic storage memory cells have

two components- one element has switchable magnetic polarity and the other one has fixed

magnetic polarity and are usually placed on top of each other with a thin tunnel barrier layer

separating them. During the write or erase operations a current is flown through the Word-Line

and a magnetic field is induced in the respective cell. As a result, the magnetic moments in the two

magnetic storage elements can be either parallel or anti-parallel to each other depending on the

direction of the applied current. According to magnetic tunnel effect [24], for the parallel arrangement electrons can tunnel through the barrier layer and therefore changes the cell resistance to low level in the so called 'ON' state. On the other hand, if the magnetic moments are anti-parallel to each other the cell resistance will be high in the so called 'OFF' state. In this solid-state non-volatile memory, data can be stored by programming the magnetoresistive materials to a certain stable magnetic state. Various magnetic states can be easily identified by significant differences in their corresponding resistance levels. During the read operation a small amount of current is flown to measure the device resistance and by comparing the distinct resistance levels the corresponding magnetic state is determined accordingly. MRAM has several advantages such as absence of any magnetic polarization leaking effect, non-destructive read operation, free from any wear-out mechanism during magnetic state modification etc. [25]. IBM first innovated MRAM in 1970s [26] and this technology is expected to supplant DRAM soon.

A standard MRAM cell consists of a transistor and a megnetoresistive component and depending on the device resistance level the stored data can be classified as either '0' or '1'. MRAM design usually includes several layers or components such as [25]: i) free layer (FL), which is the information storage layer made up with ferromagnetic material ii) reference layer (RL), which is a magnetically anisotropic layer to avoid any accidental magnetization and therefore serving as a stable yet magnetization reference during the read or write operation within the free layer and iii) tunnel layer (TB), which is a thin insulating layer (~1 nm) of non-magnetic material. Spin-polarized current can tunnel through the barrier layer and can switch the magnetic state of free layer. Reference layer is designed with very high magnetic anisotropy to avoid any accidental switching. Free layer is engineered as uniaxial by patterning the layer with a longer shape in one direction called as easy axis. The shorter one would constitute hard axis. Easy axis

Could be either in-plane or perpendicular to the plane, but the latter one is more stable during memory operation and is generally preferred. Typically, MgO [27] and CoFeB are used as tunnel layer (TB) and storage layer [28] respectively.

In the earliest type of MRAM technology, magnetic fields were used to write data. Toggle MRAM is an example of that class of MRAM [29], [30]. In this type of memory, magnetic field can modify the magnetization of free-layer without any potential wear-out effect [25]. It has very high write endurance. The next generation of MRAM employs spin transfer torque to write information through either in-plane or perpendicular-plane magnetization [25]. The state-of-the-art 256 Mb STT MRAM is already in the market [31]. For the third generation of MRAM several phenomena are being extensively researched: spin Hall effect (SHE), voltage-controlled anisotropy (VCA), voltage-controlled magnetism [32-35], spin orbit torque (SOT) [36-40] etc. There are various challenges for these technologies such as [25], SHE does not work well for perpendicular magnetization, SOT switching requires further enhanced level of effect, VCA does not work independently rather it needs to be used with another technology, some technologies are not suitable for high-density memory as it requires more terminals in its architecture etc. Two major types of MRAMs-Magnetic Tunnel Junction (MTJ) RAM and (STT) MRAM are discussed here.

1.2.3.1 Conventional MRAM

It is well known from Biot-Savart law that current carrying conductor induces magnetic field in the vicinity of the conducting wire and the direction of magnetic field can be illustrated using the right-hand rule. A standard MRAM cell is selected using bit-lines (BLs) and word-lines (WLs) which are located above and below the Magnetic Tunnel Junction device (MTJ) as shown

in Fig. 1.15. Magnetic Tunnel Junction (MTJ) device is based on a quantum mechanical phenomenon called tunnel magnetoresistance. The basic architecture of this device usually contains a non-magnetic insulating layer sandwiched between two ferromagnetic layers and a separation transistor connected with it. The insulating layer is very thin (its thickness is on the order of ~1 nm). This layer is also called as tunnel barrier layer (TB). Electron can quantum mechanically tunnel through the very thin tunnel barrier and hence MTJ can behave like a virtual resistor whose resistivity depends on the tunnel barrier thickness as well as the relative magnetization direction of the corresponding ferromagnetic layers [41]. In ferromagnetic material the number of unpaired electrons with up-spin and down-spin are unequal and therefore it can lead to spin polarization. So unlike normal metal, ferromagnetic metal has net magnetization which can be calculated considering spin dependent density of states at fermi energy. Electron with a certain spin (up or down) can only occupy a state with similar type of spin. Therefore, when the magnetization of FL and RL are aligned as parallel, large number of majority carriers (electrons) can tunnel through the barrier. As a consequence, the resistance will be low. On the contrary, anti-parallel magnetization will significantly reduce the tunneling of both majority and minority carriers and therefore the resistance will be higher. Different magnetic state has different resistance level which can be expressed by TMR ratio as:

$$TMR\ ratio = \frac{R_{anti-parallel} - R_{parallel}}{R_{parallel}}$$

Here $R_{anti-parallel}$ and $R_{parallel}$ are MTJ device resistance when magnetization of reference and free layer are anti-parallel and parallel respectively. So, parallel/anti-parallel magnetic state is linked to low/high resistance and therefore can be used to store memory bit '0' or '1'.

Figure 1.15 shows the cross section of a standard tunnel device [25]. For the simplest case

(Fig. 1.15 (a)) the coupling between the two magnetic layer (FL and RL) depends on the thickness of insulating layer separating them [41]. The FL is usually designed to be magnetically less rigid but responsive to exerted magnetic fields. But, this structure suffers from unwanted magnetic interaction between FL and RL. An engineered SAF (synthetic anti-ferromagnetic) structure provides critical magnetic properties such as inflexible magnetic system, steady magnetic path,
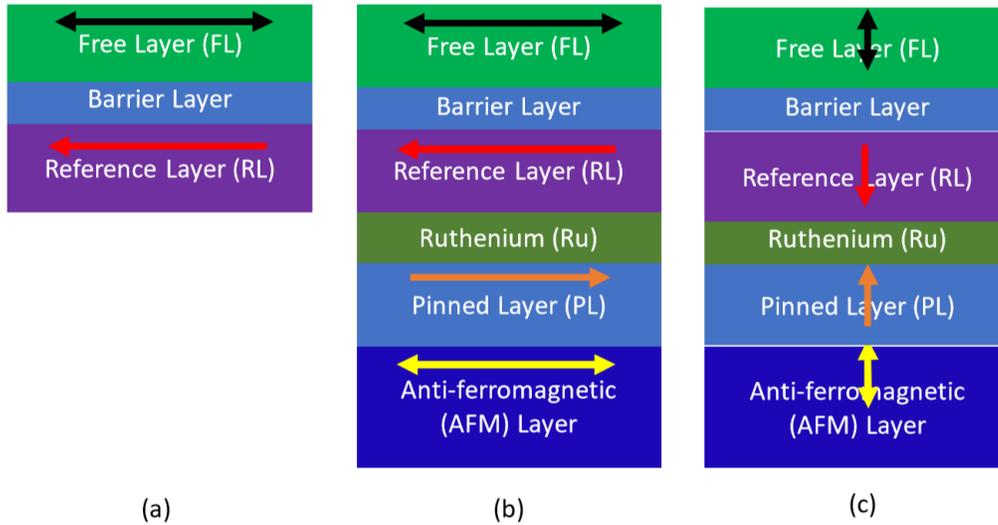
Fig. 1.15: *Cross section of Magnetic Tunnel Junction for a) simplest device design; b) in-plane device with RL pinned by AFM PL layer; c) perpendicular-plane device with RL pinned by AFM PL layer.* Reprinted with permission from [11], Copyright Materials Today (2017)

nullifying FL-RL coupling etc. by antiferromagnetically (AFM) coupling ferromagnetic layers and is a widely accepted popular solution to this problem. SAF structure can provide magnetization to in plane or perpendicular to the plane and is shown in Fig. 1.15 (b) and Fig. 1.15 (c) respectively. It can be observed that the pinned layer (PL) of SAF is directly connected to underneath AFM, whereas the reference layer (RL) of SAF is on top of ruthenium metal layer and is in contact with barrier layer (TB). Since the magnetic moment of SAF layer is less susceptible to external field and it is capable to ensure balanced magnetic moment between the layers by providing adjusted

22

dipolar field as required, AFM structure provides strong magnetic reference [25]. Again, ferromagnetic materials have asymmetric band structure and therefore once electron tunnels through the barrier it would be spin polarized [25].

Figure 1.16 (a) shows device schematic of field-controlled MRAM memory cell. To write data into a cell, current is passed through both WL and BL at the same time. As a result, WL current generates magnetic field (H_w) along easy axis and BL current generates magnetic field (H_b) in a direction transverse to the easy axis. There are two magnetic fields simultaneously
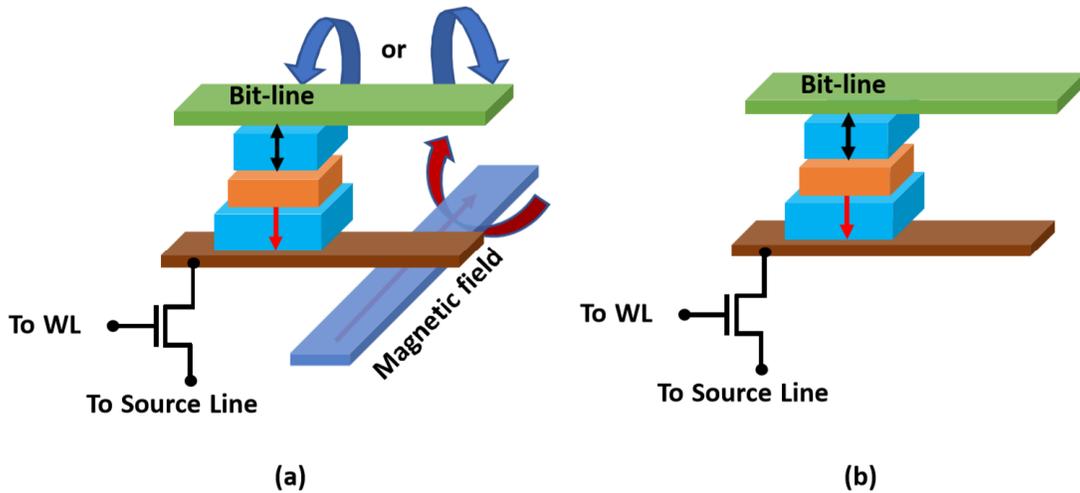
Fig. 1.16: *Device architecture schematic of a) field-controlled MRAM; b) Spin-Transfer-Torque MRAM (STT-MRAM) [11]*

generated in this process and they stay perpendicular to each other. If H_k is single domain magnetic anisotropy, then the minimum field required for field-controlled switching operation can be expressed using Stoner–Wohlfarth switching mechanism as [11]:

$$H_w + H_b = H_k^{2/3} \qquad (1)$$

When both the magnetic field (H_w, H_b) are present and collectedly exceed the minimum threshold field satisfying eq. (1) the switching operation is occurred. Since, this process requires both magnetic-field to be present, data is written only within the targeted cell and the probability of any spontaneous writing in any unwanted neighbor cell is eliminated.

Recent improvements for this device include quality enhancement for tunnel barrier layer, narrower distribution of resistance values between bit-to-bit storage in MTJ device, reduction of stray field etc. [42].

1.2.3.2 STT MRAM

A standard STT-MRAM is consist of a transistor, a tunnel junction, a word-line (WL), a bit-line (BL), and a source-line (SL) [43]. The switching operation in the Spin Transfer Torque (STT) MRAM is accomplished through passing a current through the device and it does not require application of any external magnetic field. This process encompasses selectively transporting majority carrier (electron) and transferring spin angular momentum torque through the polarized
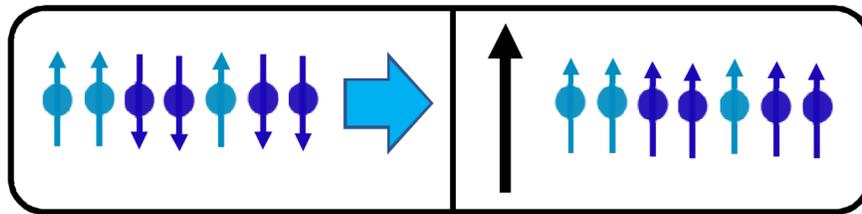
Fig. 1.17: Electrons pass through a magnetization layer get polarized and electron spins are aligned with magnetization direction of that layer [59]

electron spin in accordance with conservation of momentum. Typical electric current generally contains equal number of spin-up and spin-down electrons and are unpolarized. When electric

24

current is passed through a magnetic layer, majority of the electron spin are adjusted in accordance with the magnetization direction of that layer, the electrons get polarized. This is illustrated using Fig. 1.17. Here, the magnetic layer acts as a spin-filter. Cross section of a typical STT MRAM is shown in Fig. 1.16 (b).

When magnetization need to be modified from anti-parallel to parallel state, current is flown from FL to PL (hence electrons from PL to FL) and is shown in Fig. 1.18. If PL electron gets polarized, major number of electrons spin get converted into up-spin according to Fig. 1.18. Now, the polarized majority electrons can pass through to the FL while minority electrons are
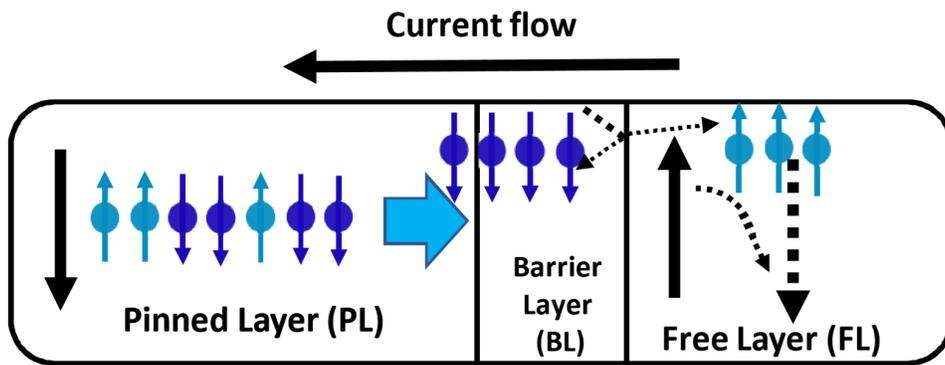
Fig. 1.18: Electron is flown from PL to FL to modify the magnetization from anti-parallel to parallel state using torque in STT-MRAM [11]

scattered. After reaching the free layer (FL), due to conservation of momentum the large number of majority-carrier electrons exert a torque on the magnetization direction of that layer [11, 25]. As a result, the magnetization of the free layer changes from anti-parallel to parallel direction. Again, to change the magnetization from parallel to anti-parallel state, current direction is reversed. In that case current is flown from PL to FL and hence electrons flow from FL to PL and is shown in Fig. 1.19. In this case the electrons with similar spin is transported through the interface, but the different spin electrons are reflected to the free layer. Now due to conservation of momentum,

spin-angular momentum transfer resulted between magnetization layer of free layer and the reflected electrons [11]. As a result, its magnetization direction changes and magnetization changes from parallel to anti-parallel.

It can be noted that only the magnetization direction of the free layer (FL) can be modified
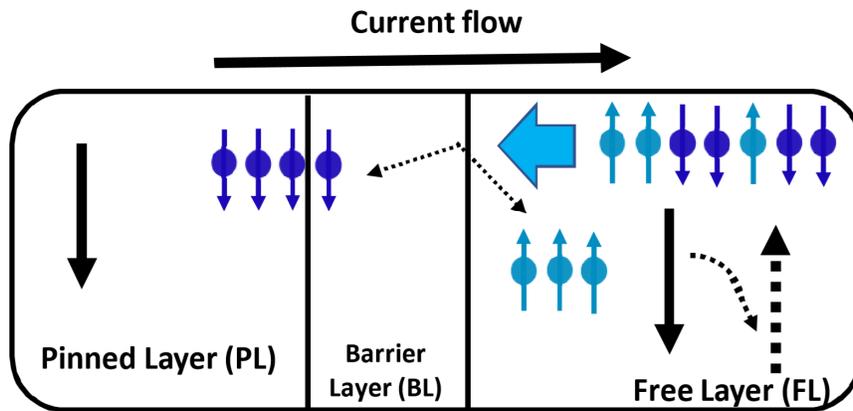
Current flow

Fig. 1.19: *Electron is flown from FL to PL to modify the magnetization from parallel to anti-parallel state using torque in STT-MRAM [11]*

and it happens only when enough level of toque is being generated. If the current level is not high enough, the magnetization direction change may come back to initial state [11]. However, too high current level can significantly increase power consumption. Therefore, spin-polarized current modifies the magnetization of the storage layer during write operation and the ensuing difference in resistance levels are sensed during the read operation. STT-MRAM and conventional MRAM has identical read operation, but their write mechanism is different.

1.2.3.3   Device Reliability & Challenges

There are manifold of challenges in MRAM technology. The field induced MRAM is stable up to an operating temperature of only 120^0 C. After that some of its key parameters such

as bit-to-bit resistance distribution and data retention lifetime etc. are severely compromised [1, 25]. It is becoming increasingly difficult to precisely control device features on the order of ~10 nm as well as maintaining a very narrow distribution of the device dimension. Wide range of materials (magnetic material, non-magnetic material, insulator etc.) constituting this type of memory device makes this requirement even more challenging [25]. Again, processing high aspect ratio features to realize high-density memory device is getting more and more difficult. Shadowing effect is becoming a common everyday problem. However, carefully designed process flows and engineered etching process combining physical bombardment and reactive etching such as RIE (reactive ion etching) can significantly alleviate these complications. STT MRAM also suffers from several reliability issues such as large power consumption due to requirement of high level of write current, thermal fluctuation induced magnetization direction reversal of free layer, barrier layer degradation induced by long duration of current pulses, alteration of magnetization state caused by extended reading time etc. [11].

1.2.4 FeRAM (Ferroelectric Random-Access Memory)

FeRAM is non-volatile Ferroelectric Random-Access Memory. When an external bias is applied across a ferroelectric material it will polarize, but upon removal of that field a hysteresis is exhibited in its polarization vs. electric field characteristics. This polarization features (P-E hysteresis) of a ferroelectric material can be used to switch between two distinct ferroelectric state of the capacitor dielectric and therefore store information accordingly. During read operation, the ferroelectric state of the capacitor is sensed. Since read operation is destructive in nature, every read process is followed by a complimentary writing bit to each read-cell. Recently, FeRAM has captivated substantial interest as future memory technology due to its numerous technological

advantages such as lowest level of power consumption, faster like DRAM, smaller cell size, relatively faster read/write operation, low voltage/power operation, faster cell accessibility etc. [44-46]. FeRAM is widely used in various applications such as IC (integrated circuit) card, mobile applications, RF (radio frequency) tag etc. [44-45]. Generally, PZT (Lead Zirconate Titanate) or SBT ($SrBi_2Ta_2O_9$) based ferroelectric materials are used for FeRAM applications [44]. FeRAM can be categorized into the following two types:

   i. Capacitor based FeRAM

   ii. FET based FeRAM

A ferroelectric unit cell inherently displays spontaneous polarization even without application of any electric field. The electric field however can modify the polarization direction within the ferroelectric film. This phenomenon can be used to store data and through polarization reversal current the stored information can be read or retrieved [45]. A characteristic P-E (polarization vs. electric field) plot of a ferroelectric materials is shown in Fig. 1.20. The magnitude of polarization at zero electric field (E=0) is called remanent polarization ($P_r : E = 0$). There is a minimum amount of field required to nullify the polarization and that field is called coercive field ($E_{coercive}$). Both P_r and $E_{coercive}$ are shown in Fig. 1.20. To counteract depolarizing field certain region of a ferroelectric material polarizes to form a domain. Switching from one polarization state to the other is enabled by dynamic evolution and dwindling of domains. When the applied electric field is high enough ($E_{applied} \gg E_{coercive}$), domains with a certain direction of orientation starts to nucleate, then proceeds with forward and sideway growth and finally completes the domain with a new

polarization state [47]. To switch to the other state, high enough voltage with opposite polarity can be applied and hence the polarization state will be reversed. Each of these polarization states can be used as a memory 'bit 0' or 'bit 1'. The device structure and operating principle of both capacitor-based FeRAM and FET-based FeRAM are described below [45].
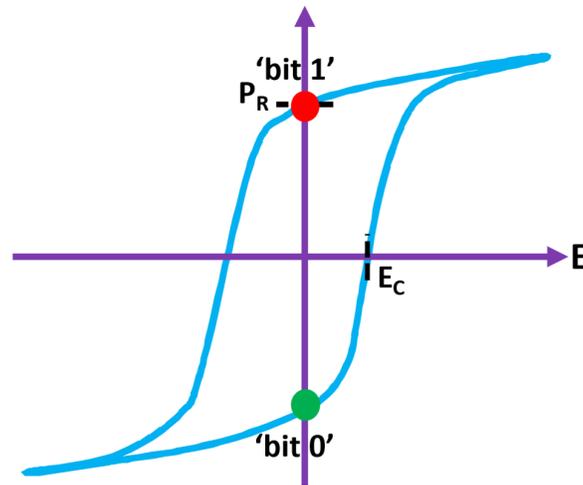
Fig. 1.20*: Schematic P-E hysteresis loop for a ferromagnetic thin film [45]*

1.2.4.1   Capacitor based FeRAM

Among the various types of capacitor based FeRAM, 1T1C cells are discussed here. The architecture of this cell contains one transistor and one capacitor per cell. The cross section of a planar type cell structure and its electrical schematic is shown in Fig. 1.21. The capacitor is stacked on top of a field oxide. At first, FET is fabricated with an isolation field oxide. Then inter-layer oxide (SiO_2) is blanket deposited followed by chemical-mechanical polishing (CMP) to planarize its surface. A thin adhesive layer (Ti) is deposited before depositing bottom electrode (Pt). Then

ferroelectric film and top electrode (Pt) are successively deposited. Etching is then conducted with
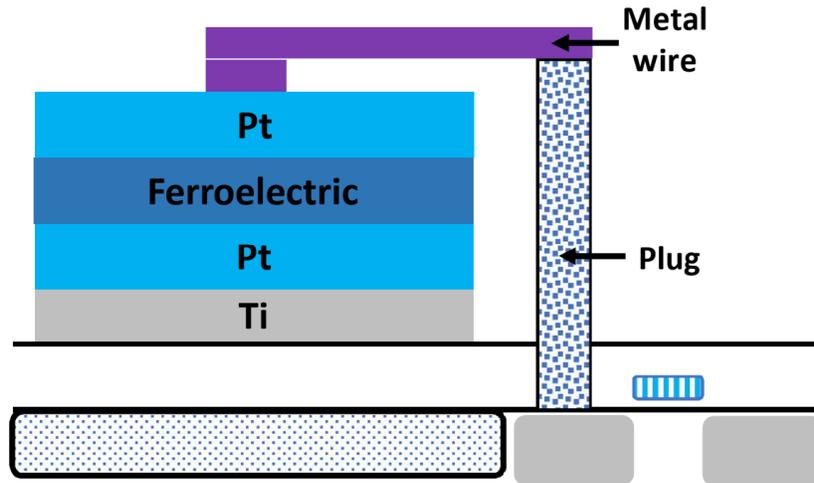
Fig. 1.21*: Cross section schematic of a planar capacitor FeRAM cell film [45]*

mask to create opening to connect the top electrode of capacitor with the drain of FET through Al wiring.

1.2.4.1.1 Write Operation

To write 'bit 1', both bit-line (BL) and pulse-line (PL) are supplied with High voltage (V_{DD}) and word-line with voltage $V_{DD}+V_t$, where Vt is the threshold voltage of the transistor. Now to change the polarization direction, PL is reduced to 0 V while BL at voltage V_{DD}. This modifies the polarization direction of ferroelectric film. Finally, both BL and WL are reduced to 0V.

Again, to write 'bit 0' BL is kept grounded (0 V) while voltage V_{DD} and $V_{DD}+V_t$ is applied to PL and WL respectively. To change the polarization direction, PL is reduced to 0V while

$V_{DD}+V_t$ voltage is kept at WL. The polarization direction of ferroelectric film is changed towards upward direction. Finally, WL is reduced to 0V. The schematic timing diagram of writing operation is shown in Fig. 1.22.

Some of the desired characteristics of this type of FeRAM is large magnitude of P_r (to ensure high polarization reversal current/area), low dielectric constant (to achieve low displacement current and hence enhanced detection of polarization reversal current), low $E_{coercive}$ (for ease of switching), low degradation of ferroelectric material etc. [45].

1.2.4.1.2 Read Operation

To enable read operation a sense amplifies is connected between BL and a reference
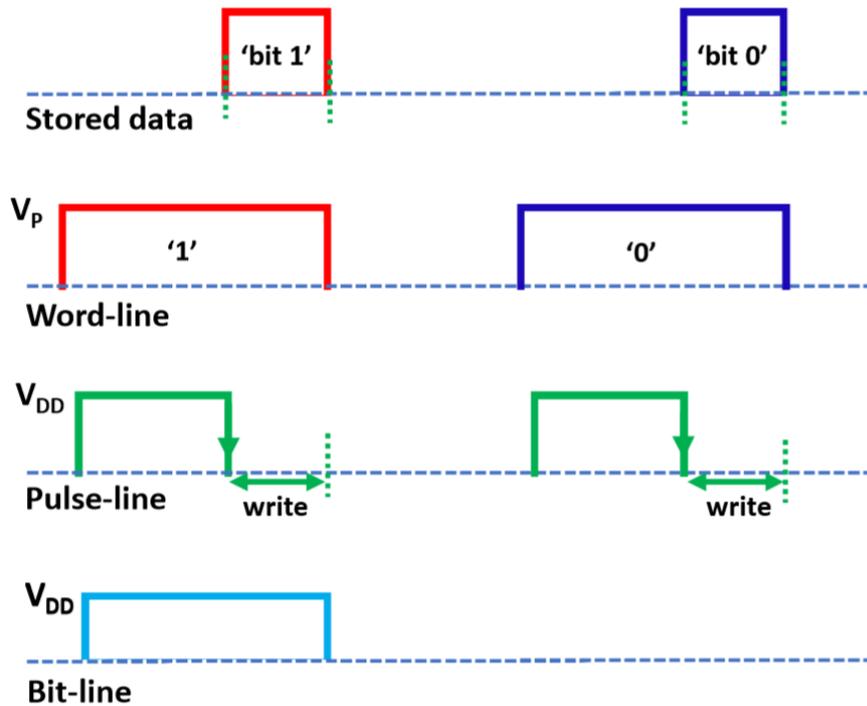
Fig. 1.22: Schematic timing diagram for 'write' operation[45]

voltage which is usually kept between the voltage correspond to 'bit 0' and 'bit 1'. Now PL voltage is increased to V_{DD}. For stored information 'bit 1', the ferroelectric material's polarization direction will be inverted, and BL voltage will increase. Sense amplifier amplifies the difference and BL voltage increases to V_{DD}. Then PL voltage is reduced to 0V and polarization direction changes to initial direction again. This read operation is destructive and therefore a re-write operation right after every read is required to bring the data to original state [45]. Extra write operation can make this process relatively slower.

1.2.4.2   FET based FeRAM

Among the various FET based FeRAM, 1T type is discussed here. This structure contains one ferroelectric gate FET and therefore scalable as well as has potential for future high-density integration. Unlike capacitor type FeRAM, read operation of this type of FeRAM is non-destructive. The cross section and circuit schematic of FeFET memory cell is shown in Fig. 1.23. It can be seen that ferroelectric material is used in placed of gate dielectric. Its principle of operation uses the fact that gate voltage can modify the polarization state of ferroelectric material
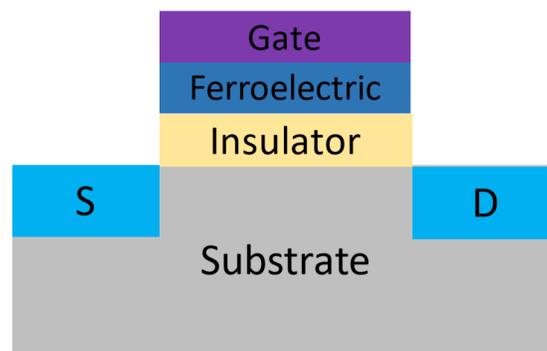
Fig. 1.23: Cross section schematic of a FET-based FeRAM cell[47]

which in turn can manipulate the conductivity of channel located between drain and source terminal. By applying a small drain voltage (without affecting the polarization of ferroelectric material), the level of drain current can be sensed (correspond to high or low channel conductivity) and can be used to classify memory information 'bit 0' or 'bit 1'. When a sufficiently high voltage ($V_{Gate} > V_{coercive}$) is applied to the gate, the polarization of ferroelectric material is aligned accordingly and accumulates positive charge in ferroelectric layer [47]. To compensate this positive charge, negative charges are gathered (for p-type substrate) at the interface of ferroelectric/semiconductor. Therefore, drain-source are connected through this highly conducting channel. This can be one state of memory. Similarly, to switch the memory cell to the other state negative voltage is applied to the gate and the ferroelectric material gets negative charges. As a result, electrons are depleted from the channel and source-drain get disconnected. This results with a highly resistive channel and can be treated as other state of the memory.

Ferroelectric film is desired to be inert with substrate as well as with buffer layer for FET type FeRAM. There have been several successful development activities which significantly advance FeRAM reliability. This includes quality improvement for ferroelectric thin film, lessening H_2 infiltration by depositing passivation film, optimization of conductive oxide to reduce polarization fatigue, development of optimized process condition for ferroelectric film etc. [45]. However, several major technological challenges are still present to realize high density or 3D FeRAM. Minimizing process temperature, improvement of barrier layer stability and reduction of inter-diffusion among elements constituting of FET, diminishing voltage dependent drifting of P-E hysteresis loop with increased number of switching cycles, retaining polarization with increased number of switching cycles, reliable performance at wide range of operating temperatures etc. are some of the key problems to mention [44-45].

1.2.5 PCM (Phase Change Memory)

PCM is a non-volatile Phase Change Memory technology. This type of memory is mainly based on chalcogenide materials such as GeSbTe alloys (also known as GST) with pseudo binary composition of GeTe and Sb_2Te_3. PCM or PCRAM memory uses the fact that there is substantial electrical resistance contrast between the two distinct phase of a material- crystalline state vs.
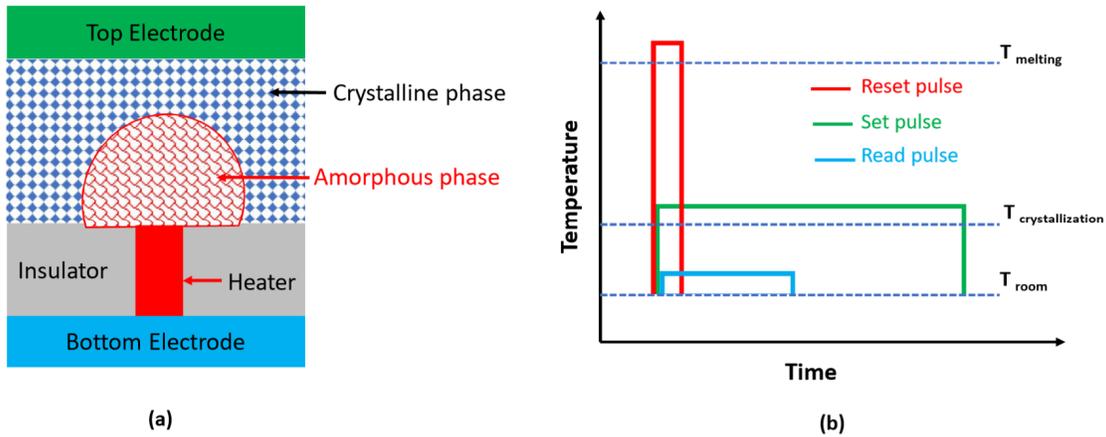
Fig. 1.24: *a) Cross section schematic of a PCM memory cell; b) Timing diagram schematic of SET, RESET and READ operation in a PCM cell.* Reprinted with permission from [9], copyright IEEE (2010)

amorphous state. In amorphous state, the atoms have periodic structure locally, but that periodic arrangement is absent for long-range order and therefore the material has very high resistance. On the contrary, the atoms are perfectly periodically arranged for long-range order in the crystalline phase and the material therefore has very low resistance. This low or high value of resistance can be used as two distinct states of memory in PCM.

1.2.5.1 Write and Erase Operation

The as-fabricated PCM material is crystalline and hence have low resistance due to BEOL processing temperature [48]. Now if a large intensity of current pulse is applied to this crystalline

34

material for a short duration, a selected material region (programming area) is melt and then if it is quenched quickly there will be a highly resistive amorphous material in the PCM cell [48-49]. This high intensity short duration current pulse is called reset pulse. Now the newly created amorphous area is in series with remaining as-fabricated crystalline material of the PCM cell located between top (TE) and bottom electrode (BE). Since, the electrical resistance of amorphous material is several orders of magnitude higher than that of crystalline material, resistance of PCM cell is effectually determined by the amorphous region. Now, to convert the PCM material from amorphous to crystalline phase the programming area needs to be locally annealed with a temperature between crystallization and annealing temperature through a moderate intensity long duration (longer than crystallization time) current pulse [48]. This medium intensity long duration pulse is called set pulse. Again, since amorphous material has very high resistance, application of a medium level of voltage will lead to a very small amount of current flowing through it. This low level of current is insufficient to generate joule heating for subsequent melting and re-crystallization of the material from existing amorphous phase. However, when amorphous material experiences a field across it which is higher than a threshold value ($V > V_t$), it activates a privileged electronic change which leads to a relatively lower resistance (resistance comparable to crystalline phase) in the amorphous material compared to its initial amorphous phase. This phenomenon is called threshold (V_t) switching. Threshold switching is the most critical factor for the set process. This low resistance can now trigger significantly large amount of current through the amorphous material and enough amount of heat is dissipated to crystallize the material [49].

1.2.5.2 Read Operation

To read the programmed state of the PCM cell, a small amount of electrical current is flown across the cell by applying a small voltage across it and the corresponding resistance of the PCM cell is measured. The current should must be low enough not to affect the existing crystallinity status in the PCM cell programming terrain. The cross-section schematic of a PCM cell as well as various current pulses for read/write operation is shown in Fig. 1.24 (a) and Fig. 1.24 (b) respectively.

1.2.5.3 Challenges

As the PCM cells are scaled down, the atomic properties of surface or interface atoms becomes more critical and the device characteristics are also significantly altered. There are numerous properties of PCM cells which are size-dependent such as; melting temperature (melting temperature decreases for thinner film) [48, 50], crystallization temperature (crystallization temperature usually increases for thinner film, although interface material property can also change with increase or decrease of temperature too) [48, 51, 52], crystallization time (based on interface characteristics it can either increase or decrease) [52], electrical resistances (resistance usually increases for thinner film) [53] etc. PCM memory technology is already used in re-writable optical data storage and non-volatile memory applications [49]. But, this technology also has several limitations such as; high power consumption specially during the reset operation, thermal cross-talk between neighbor cells are imminent with further scaling which can severely compromise its reliability. The exact amount of power consumption also depends on the properties of various materials integrated in the device structure such as -thermal conductivity, resistivity etc. [48]. Although the scaled PCM cells still exhibit its phase change properties, it is quickly reaching the

36

technological scaling limit when the PCM materials will no longer be stable in any of its phases [48].

Therefore, PCM cells are a great promise for future memory technology, but to realize its full potential several issues need to be addressed such as; threshold switching mechanism, trap properties, reliable multi-bit operation, reduced power consumption, quicker switching speed, enhanced reliability, reduced foot-print for memory selector etc. [48].

1.2.6   Flash Memory

Flash Memory is a non-volatile semiconductor memory technology where the programming (writing) and erasing operation of data can be conducted electronically. It is an upgraded version of EPROM and EEPROM. The term 'flash' originated from the fact that in flash technology a large amount of memory cells (or data) can be simultaneously erased, which is usually called as 'block erase'. However, in EEPROM data is usually erased on a byte level. Flash memory on the other hand use larger block sizes during the erase operation. As a result, erase operation is much faster in flash memory compared to EEPROM technology. Flash memory also offers faster access like DRAM, but it is slower than SRAM and ROM [54]. Intel first introduced NOR flash in 1988 and Toshiba demonstrated world's first NAND flash technology in 1989 [55]. There are two main categories of flash memory:

i.   NOR flash

ii. NAND flash

In flash technology, information is stored in the floating gate transistor (or double gate transistor) based memory cell which is arranged in array pattern. Floating gate transistor is similar to any normal MOSFET except that it has two gates-control gate (CG) and floating gate (FG).

CG is the top control gate which is accessible from outside and is available for application of electrical bias when necessary. FG however is buried within insulation oxide, electrically inaccessible and is located between CG and MOSFET channel. Due to the device architecture the FG acts like an 'electron trap' and whenever any electron is placed in FG, it will usually remain
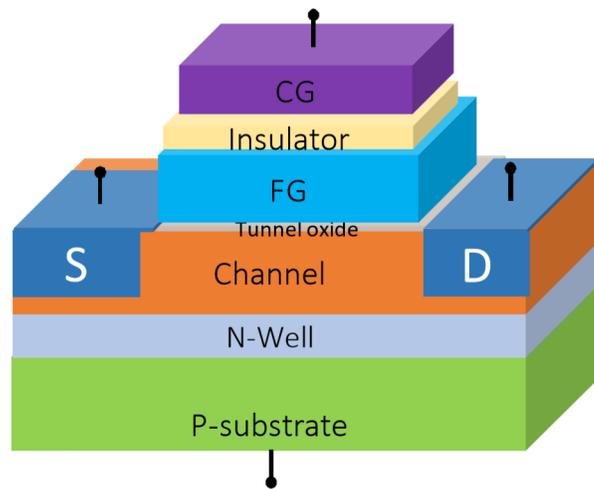
Fig. 1.25: Cross-section of a double gate Flash memory cell [54]

there for very long duration. Since CG is the only accessible gate, voltage is applied to CG to create an electric field. If that electric field is high enough, it can create electron inversion layer (for NMOS) and forms a continuous channel between source and drain. The minimum voltage necessary to create this channel is called threshold voltage (V_t). But, when electrons are trapped in FG, its negative charge will partially screen out the electric field from CG and therefore the magnitude of electric field required to create the channel will increase. In other words, the threshold voltage (V_t) will increase. Figure 1.25 shows the 3D schematic of a standard flash memory cell, which is also called as floating gate transistor. Each memory cell can store one bit or multiple bits of information and is called as single-level cell (SLC) or multi-level cell

respectively. For MLC cell, several levels of electrical charges can be stockpiled in the isolated floating gate of the double gate transistor and therefore stored bits per cell is increased consequently.

There can be two possible states of FG in floating gate transistor -either electrons are stored at FG or there are no electrons present there. The corresponding threshold voltage will be HIGH ($V_{t\text{-HIGH}}$) or LOW ($V_{t\text{-LOW}}$) respectively. By detecting the conductivity state of the channel (whether channel is insulating or conducting) the stored information in the memory cell can be categorized. Normally erased state (when no electrons at FG) is denoted as 'logic 1' and programmed state (when electrons are transported and trapped in FG) is designated as 'logic 0'. For MLC cell, multiple levels of electron density can be present at FG, which would affect the amount of current flowing through the channel. Therefore, by sensing the current level the corresponding multi-bit information can be extracted. Usually in flash memory one voltage supply with relatively small magnitude is present and using charge pump circuitry located within the memory chip the other required high voltages can be created.

1.2.6.1   NOR Flash Memory

In NOR flash memory, one end of each cell (floating gate transistor) is connected to ground and the other end to bit-line (BL). The word-lines (WL) of the transistor are connected to control gate (CG). Since cells are connected in parallel to BL, read and program operation can be conducted on cell level. Figure 1.26 (a) shows the schematic of cell-to-cell connection array of a NOR flash memory using the device architecture shown in Fig. 1.25. This technology was primarily designed for random-access read operation with technological advancement to make it competitive with contemporary memories-EPROM and EEPROM. Therefore, its write operation

is not optimized, and it is relatively slower. The parallel connection architecture of NOR flash consumes large area since every two cells requires one metal connection with source/drain diffusion area. The memory density is therefore low. NOR memory is used for machine code
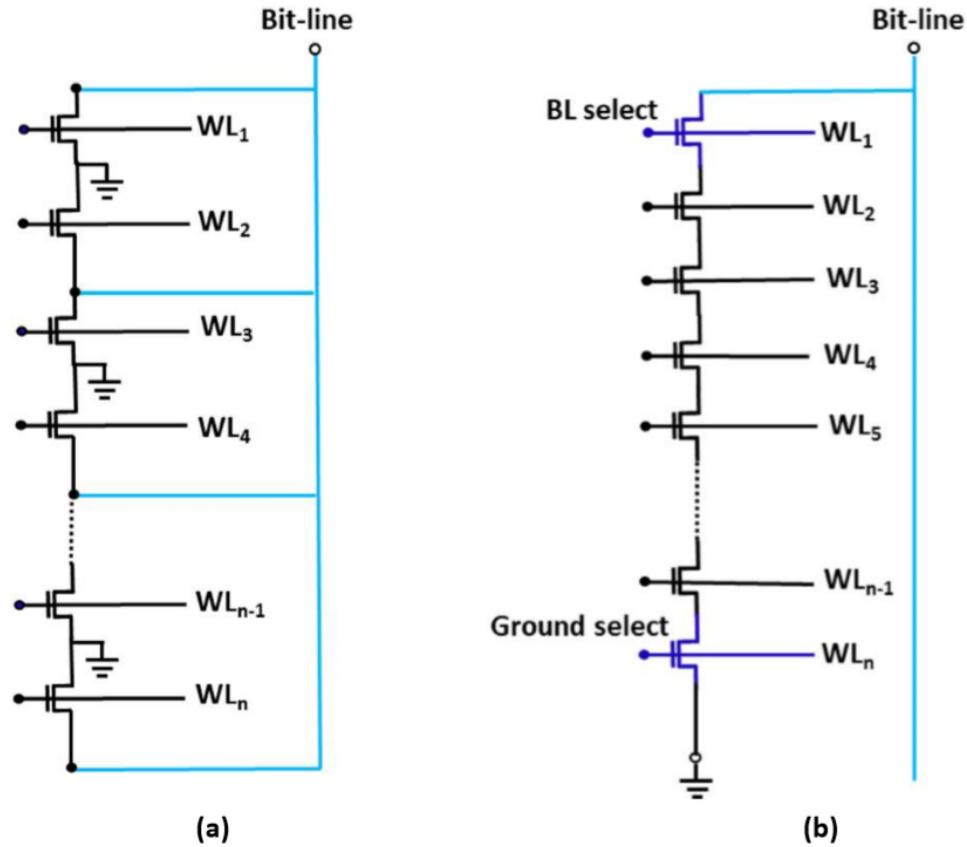
Fig. 1.26: schematic of cell-to-cell connection of a) NOR flash memory; b) NAND flash memory [54]

execution, cell phones, digital camera, medical electronics, audio player etc. [54].

When voltage is applied to one of the WLs (V = HIGH) that transistor is turned ON, output BL is then connected to ground (GND) and the output therefore goes to LOW. So, for any HIGH input (voltage at WL) the output goes to low (BL becomes grounded). This behavior resembles with 'NOR gate' and so this type of memory cell array arrangement is called as NOR.

1.2.6.1.1   Program Operation

The programming or writing operation is the process of transporting electrons from substrate (for NMOS) and trapping at floating gate (FG). NOR flash cell programming is done
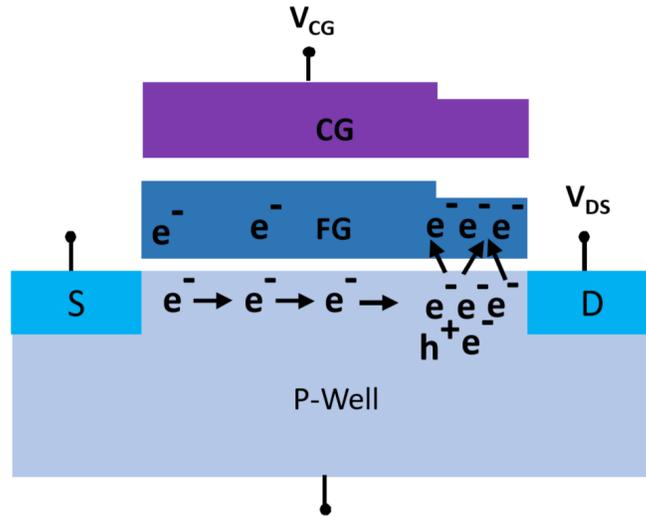
Fig. 1.27*: Program (write) operation in a NOR flash cell using Channel Hot-electron Injection (CHE)[54]*

through Channel Hot Electron mechanism (CHE). By applying large voltage between source and drain, a large electric field can be created along the lateral direction of channel. So, electrons moving along the channel will gain high energy. If there are some lucky electrons which do not undergo that many scatterings throughout this travel, they might gain high enough energy (> 3.1 eV) to overcome the energy barrier present at the tunnel oxide interface. Majority of these highly energetic hot electrons are generated closer to the drain end where depletion region is present and electric field is maximum. Now, if a high positive voltage is applied at control gate (CG) it will create strong electric field transverse direction to the channel and can inject hot electrons from the channel which can cross the oxide layer, reach floating gate and eventually getting trapped there

[20, 54]. The memory cell is now written with 'logic 0'. As more and more electrons are stored at FG, the gate potential gradually reduces and finally the process stops. This process however is not ideal and there are lot of collisions happening within the channel which creates both electrons and holes. The holes and electrons are collected into substrate and drain respectively and constituting substrate and drain current respectively. This Channel Hot Electron induced programming operation consumes large power. Modern NOR flash devices are usually programmed on byte level. Figure 1.27 schematically demonstrates the programming operation in a NOR flash memory cell.

1.2.6.1.2 Erase Operation

During erase operation, the stored electrons are removed from the FG. Both NOR and
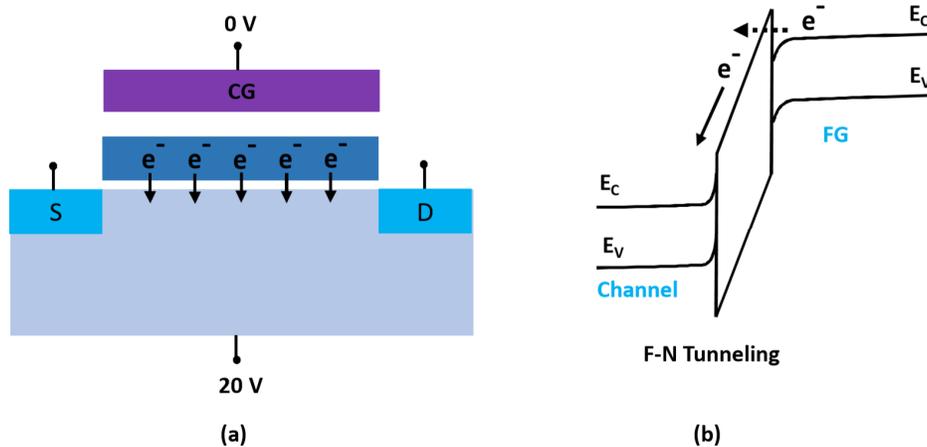
Fig. 1.28: *Erase operation in a NOR flash cell using Fowler-Nordheim tunneling a) Device-level schematic; b) Band diagram [20]*

NAND uses Fowler-Nordheim tunneling erasing mechanism. By applying high voltage between

control gate (CG) and source, high electric field can be created across tunnel oxide. As a result, through Fowler-Nordheim tunneling electrons are removed from floating gate (FG). In first generation NOR flash, voltage was applied to source terminal only with CG grounded. But this can potentially create breakdown at source/ substrate junction. By splitting the bias between gate and source terminal this problem can be mitigated. But at source/substrate junction there still could be large amount of leakage current due to band-to-band tunneling. Then a new device architecture is adopted by introducing a p-well. By applying bias to this well, electron can be extracted from the entire channel [54]. Erase operation of a NOR flash cell level is schematically shown in Fig. 1.28. After successful erase operation, electrons are removed from FG.

1.2.6.1.3   Read Operation

NOR flash cells can be randomly accessed during read operation. To read the memory state
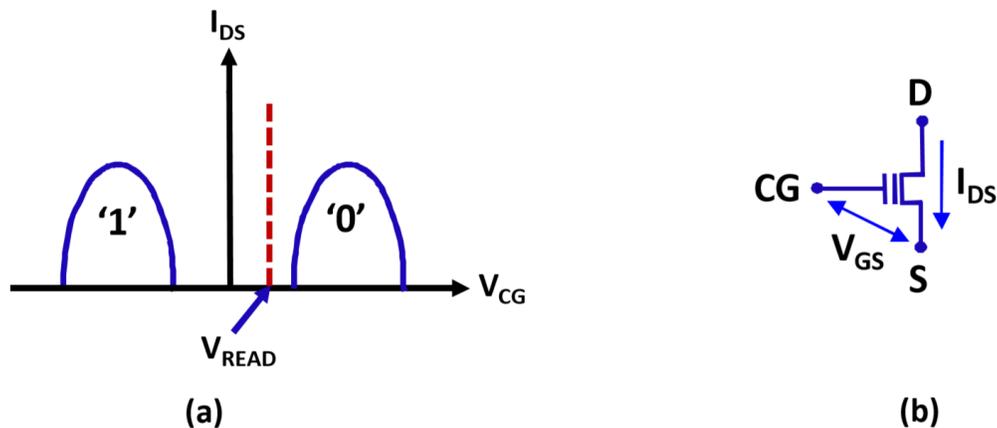
Fig. 1.29: *READ operation in a NOR flash a) Schematic current-voltage characteristics; b) transistors level circuit schematic [54]*

of a cell, its current is compared with an identical reference cell through sense amplifier circuitry. The cell with erased state (no electrons at FG) will have lower threshold voltage (V_t) than the

programmed cell (electrons trapped at FG). So, for the same voltage applied to gate (through WL) and with a smaller drain-source bias, erased cell will conduct much larger current through the channel than that of the programmed cell. If the reference cell characteristics is positioned between those two states, then by comparing with the reference cell the stored information can be retrieved. Figure 1.29 (a) and (b) illustrates the read operation through I_{DS}-V_{GS} characteristics and transistor-level circuit schematic respectively.

1.2.6.2   NAND Flash Memory

NAND memory cells are also based on floating gate transistor (also called as double gate transistor). However, several cells (16, 32 or 64 cells) are connected in series configuration and form a group [54]. One end of that series is connected to source line through an SSL transistor (source select transistor) and the other end is connected to even bit-lines (BLe) or odd bit-lines (BL$_o$) through another DSL transistor (drain select transistor). The gate of all transistors is connected to several word-lines (WLs). When all transistors are turned ON by applying voltage (V>V$_t$) to their gates through corresponding WLs, the BL gets connected to ground and the output becomes 0 V (LOW). So, for this configuration, when all inputs are HIGH (V>Vt at gates) the output becomes LOW (0V) which resembles with NAND logic. This series connected configuration saves space by eradicating several metal contacts in source/drain diffusion area (compared to one contact for every two cells in NOR flash). NAND flash technology therefore provides increased chip density and hence delivers lower cost per bit. Figure 1.25 and 1.26 (b) show the schematic of device level architecture and cell-to-cell connection array of a NAND flash memory. NAND memory is used in solid-state drive, USB drive, memory card etc. [20].

1.2.6.2.1   Program Operation

Programming is transporting of electrons from the substrate and storing it at FG. Unlike NOR, programming of NAND flash uses Fowler-Nordheim Tunneling phenomenon. High electric field is created by applying bias between CG and substrate. By flipping the bias polarity erase
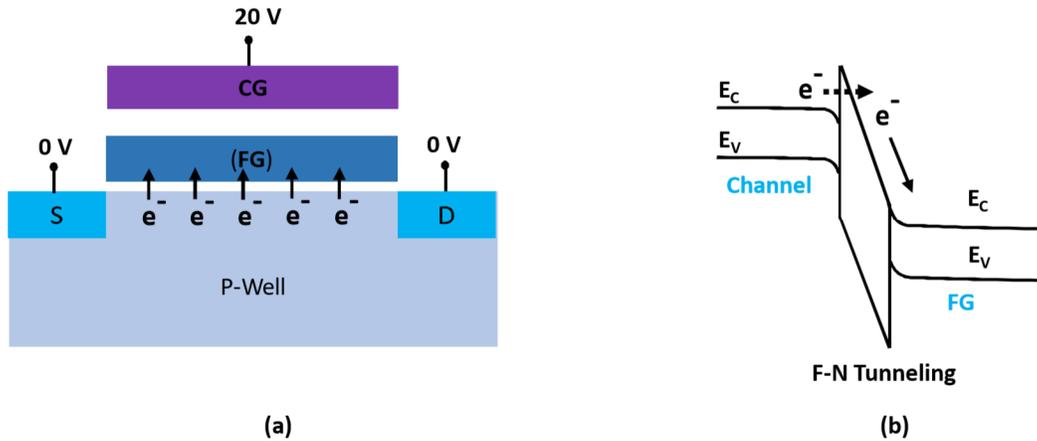
Fig. 1.30: Program operation in a NAND flash using Fowler-Nordheim Tunneling: a) Device-level schematic; b) Band diagram [54]

operation is conducted.

At first the DSL (drain select transistor) of the cell to be programmed is turned ON by applying voltage to its gate. The other pass transistors in that strings (cells in that string that are not to be programmed) are tuned ON by applying a voltage (8~10 V) higher than threshold voltage in their gates through corresponding bit-lines (BLs). The SSL (source select transistor) gate is grounded. Now BL is grounded and high voltage (~20 V) is applied to the gate of the cell to be programmed through respective WL. So, target cell has high voltage at its gate, 0V at drain and its source is floated [54, 56]. The high electric field across tunnel oxide leads to electron tunnel from substrate and accumulation at FG. High electric field (high voltage) will improve the program performance by injecting more electrons into FG but at the expense of oxide degradation. By

scaling oxide thickness and reducing bias voltage this problem can be alleviated up to the point when other degradation effects such as stress induced leakage current start affecting the device degradation.

Due to cell to cell geometry and process variations, drain modulation etc. there is a distribution of threshold voltages among cells. To ensure a reliable operation of memory cells, these distribution needs to be well-controlled and preferably very narrow specially for multi-bit
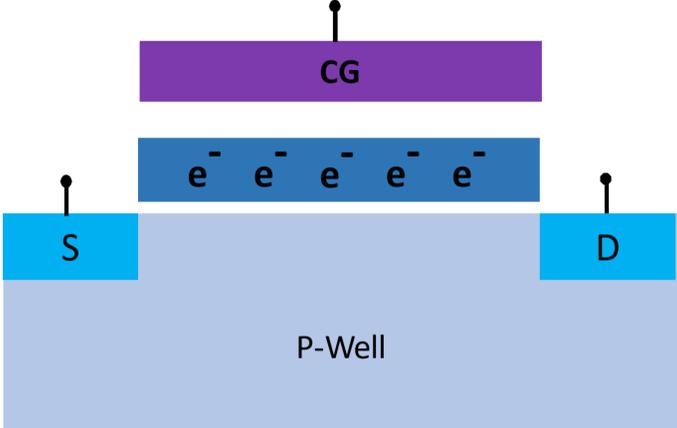
Fig. 1.31: NAND flash memory cell after successful programming operation [54]

memory cells. To ensure a tighter distribution of threshold voltage, program & verify algorithm is usually adopted. In this strategy the program operation is followed by an additional relatively longer read step where it is checked whether the cells have reached the target threshold voltage or not [20, 54]. Then another program pulse is applied to only those cells which did not meet the threshold requirement. The process stops when all cells meet target threshold, or the maximum number of attempts are reached. Figure 1.30 (a) shows device level schematic of a NAND Flash cell during programming operation and the corresponding band-diagram is shown in Fig. 1.30 (b). A device-level schematic after successful program operation is also illustrated by Fig. 1.31.

During programming of NAND cell, there is a probability that other cells connected to the same word-lines (WL) get unintentionally programmed. To avoid this accidental programming of the cells connected to same WL, they are electrically floated. Due to capacitive coupling between CG (control gate) and channel, the channel as well as the source/drain of those respective cells are
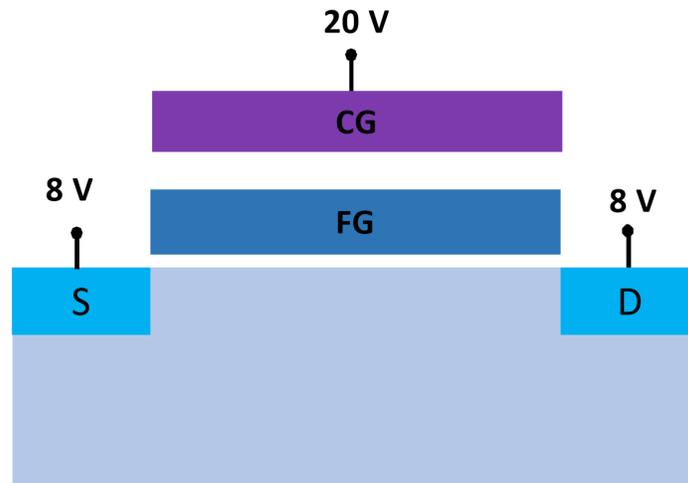
Fig. 1.32: 'Program inhibit' operation of NAND flash memory [54]

boosted up to 6~8 V. As a result, the electric field across the tunnel oxide is significantly reduced and will not be high enough to program those cells. This is known as 'program inhibit'. A device schematic with applied electrical bias to its various terminals for the 'program inhibit' operation is shown in Fig. 1.32.

1.2.6.2.2 Erase Operation

During erase operation, the stored electrons are removed from the FG using Fowler-Nordheim tunneling. Like erasing of NOR flash cell, Fowler-Nordheim Tunneling phenomenon is also used for erasing of NAND flash cell and is shown in Fig. 1.28 (a) and (b). This process is also

similar to programming of NAND flash cell except the bias polarity is reversed. Large bias is applied between CG and substrate (substrate is positive biased and gate/WL of select blocks are grounded) and this high electric high causes electrons stored at FG to tunnel through the oxide layer and reach substrate. NAND flash cells are erased as one block at a time where all block share same well. Therefore, to inhibit unselected blocks from erasing WLs of unselected blocks are floated through a process known as erase inhibit.

1.2.6.2.2   Read Operation

To read a NAND flash cell its gate is biased with small voltage V_{READ} ($V_{READ}<V_t$). A voltage higher (V_{PASS}) than cell threshold voltage is applied to the gates of other transistors in that
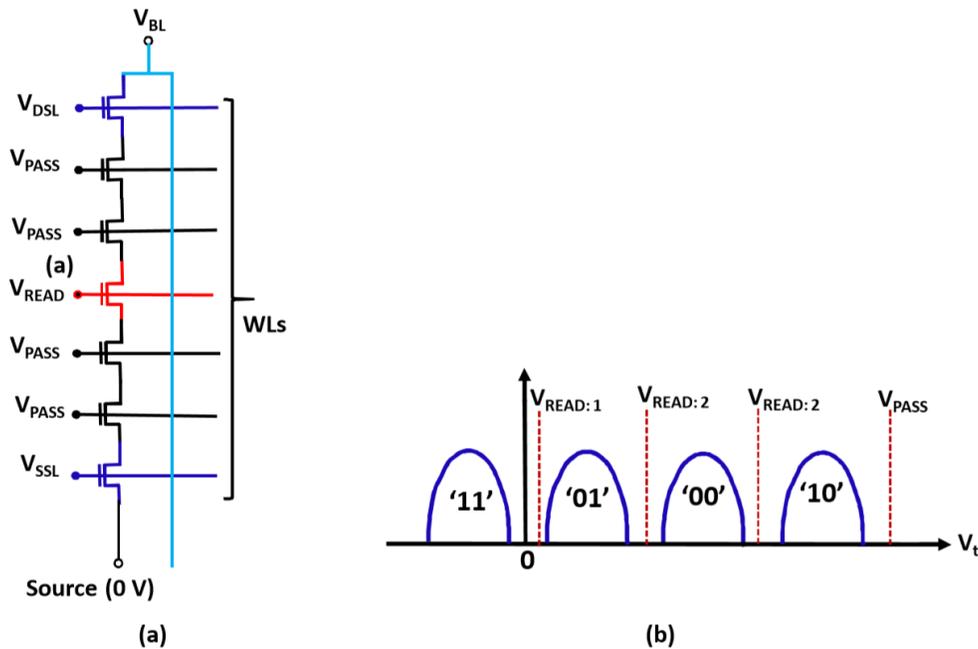
Fig. 1.33*: READ operation in a NAND flash memory: a) Cell-to-cell connection array schematic; b) Schematic current-voltage characteristics for an MLC cell [54]*

48

voltage. By applying a relatively high voltage to its gate (~4V) it is ensured that both types of pass transistors are turned ON and form a continuous channel. The selected BLs are pre-charged and then floated. Since all these cells are connected in series, if the cell to be read are already programmed then BL will not be discharged. On the other hand, when the cells to be read are erased, BL will be discharged. By sensing the BL voltage after a certain period, the memory status group. An erased cell has normal threshold voltage whereas a programmed cell has high threshold of the target cell can be identified. NAND cells are usually read on page level. Figure 1.33 (a) and (b) shows Cell-to-cell connection array schematic and current-voltage characteristics for an MLC (multi-level cell) NAND memory cell respectively.

1.2.6.2.3   Challenges

The latest state-of-the art NAND device is vertical NAND (V-NAND) where the cells are stacked vertically, and the charge trap layer is surrounded by cylindrically shaped geometrical architecture [20]. V-NAND is a promising solution to realize high density memory technology. In NAND flash, cells can be randomly accessed for reading, but random-access operation is not possible for re-writing or erasing process [54]. The reliability of this memory also deteriorates beyond a finite number of switching cycles (also called as program-erase cycles or P-E cycles). Latest NAND memory chips can go through as many as 10^6 P-E cycles [55]. Wear leveling technique can further improve the integrity of chip by dynamically counting and mapping the P-E cycles of each cell and spread the successive write operations to different sectors accordingly [54]. Authentication of write operation and remapping data to other blocks in case of unsuccessful write operation could be another useful approach. Again, repeated read operation can deteriorate the integrity of nearby cells in the same block and those cells can potentially become programmed

over time [54, 56]. This is called read-disturb. By keeping track of the number of read operation in each block through flash controller and dynamically coping those data into new blocks once the read threshold (maximum number of read operation) is exceeded can significantly alleviate this problem [54]. Again, due to series connected architecture the signal intensity received by sense amplifier during read operation is weak. This can decrease the speed of read operation. Therefore, NAND flash memory may not be the best choice for high speed random-access applications. But it is a very good choice for low power, scalable, high density and low cost per bit memory solutions.

1.2.7 ROM

ROM is Read-Only Memory. These types of memories are primarily used for reading operation. Their write operation is either cumbersome or too slow and therefore not considered for writing operation. Among the various types of ROM technologies- PROM, EPROM and EEPROM are discussed here.

1.2.7.1 PROM

PROM is Programable Read Only Memory where data can be written only one time. Information is usually stored as fuse or anti-fuse in this digital irreversible memory technology [57]. This non-volatile technology is usually a factory-made blank memory. It can be programmed or burned later using a tool named PROM programmer. Once programmed the written content is permanent and usually not erasable. PROM is used in microcontrollers, RFID (radio-frequency identification), HDMI (high-definition multimedia interface) etc. [58].

1.2.7.2   EPROM

EPROM is Erasable Programable Read-only Memory. This non-volatile memory is based on Floating Gate Avalanche MOS (Metal-Oxide-Semiconductor) transistor.   The transistor contains two gates-control gate (CG) and floating gate (FG). Control gate is accessible for electrical connection and bias voltage can be applied to the CG, whereas the FG is electrically isolated and is usually buried inside an oxide layer and is similar to the device discussed in Fig. 1.25 for flash memory. The schematic of an EPROM memory array is shown in Fig. 1.34. It can be observed that memory cell is positioned at each intersection of world-line (WL) and bit-line (BL). Each WL is connected to FG of several transistors. On the other hand, voltage source V_{DD} is connected to Drain end of several transistors along its direction as it goes vertically and finally is connected to the output through an inverter. Each transistor can be selected through corresponding WL and BL. For example, if the transistor is ON it will pull down the BL and the input of the inverter will be low (0). As a result, the output of the inverter will be High (1). Similarly, when the transistor is OFF the output of the inverter will be low (0). The program read, and erase operation of EPROM memory cell is described below [59-61].

1.2.7.2.1   Program Operation

All EPROM cells need to be completely erased before it is ready to program. Channel Hot Electron Injection (CHE) is used to program an EPROM memory cell where electrons can tunnel through the tunnel layer due to high electric field and eventually get trapped in the FG. The process is similar to the one illustrated using Fig. 1.27 in flash memory. Very high voltage (~ 25 V) is applied to the WL which is connected to the CG. As a result, the corresponding cell is ON. Again

, BL of that cell is also supplied with small voltage (~ 5V) which is also the drain of that transistor. So, a continuous channel is formed underneath the gate and a current will flow from Drain to Source terminal (electron will flow from source to the drain end). Besides, high gate voltage (~ 25 V) applied at CG will create a very strong electric field and will act along vertical direction with
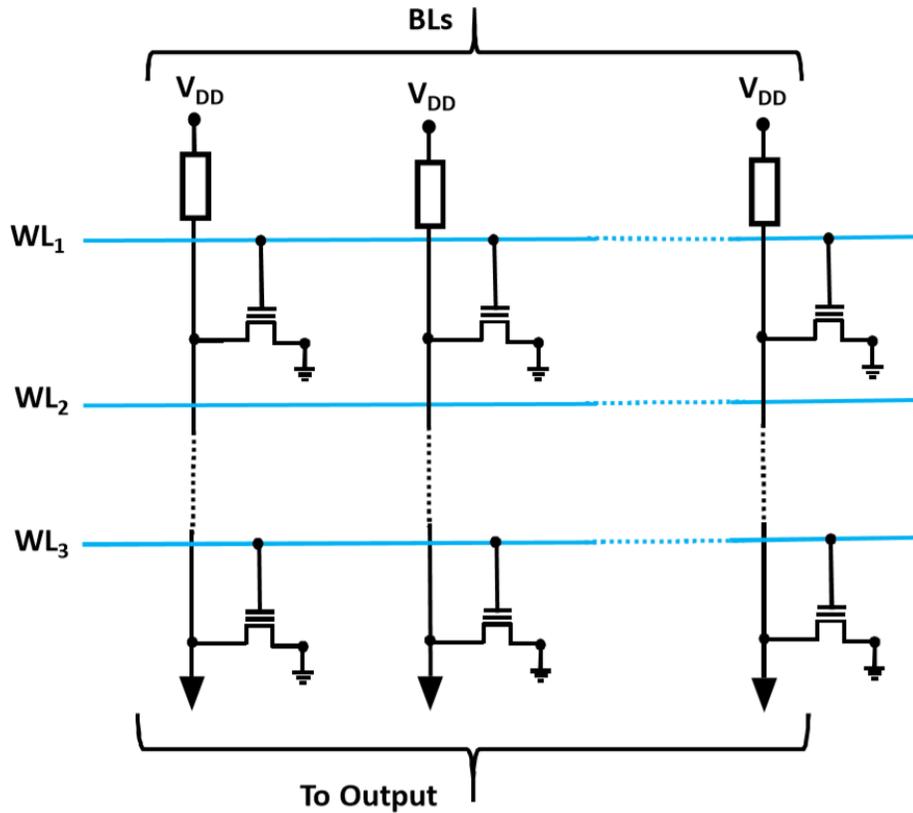
Fig. 1.34: *Schematic of EPROM memory cell array cell [59]*

respect to the channel. As a result, some of the electrons moving from source to drain can gain enough energy and overcome the energy barrier present at Si/SiO_2 interface and eventually can be implanted into the floating gate (FG) [62]. The cell is thus programmed. The information written into the memory cell through this process is 'bit 0'. The trapped electron can stay in FG for several years.

52

1.2.7.2.2   Read Operation

If a cell is programmed (electrons are implanted into the FG), more voltage is required at CG to invert and create a channel. In other words, the threshold voltage (V_t) of that transistor is increased. So, if a moderate read voltage to CG (V_{READ}) will not be enough to invert and create a channel. The transistor will remain in the OFF state and very negligible current will flow within the channel with V_{DS} applied to drain. By sensing the low (or negligible) level of current, the cell can be identified as programmed ('bit 0' is stored in the memory).

On the other hand, if the cell is not programmed (no electron is present in FG) the channel can be created just by applying normal threshold voltage (V_t) at CG. In this case with V_{DS} applied to drain terminal, a large amount of current will be flown in the channel. By sensing the current level, the cell can be recognized with stored information 'bit 1'.

1.2.7.2.3   Erase Operation

To erase the memory content written into the cell, the entire memory chip is exposed with UV (Ultraviolet) ray. Usually there is a quartz window on top of the memory cell to facilitate UV exposure as needed. During normal operation this quartz window is opaquely covered to prevent it from spontaneously erasing the memory cell over long time. Upon exposure, the electrons implanted in FG acquire very high energy and can overcome the energy barrier at SiO_2/Si interface and eventually can move into Si substrate or part of them can even get into CG. This causes the threshold voltage (Vt) of the transistor to decrease to the normal V_t level. However, erasing operation takes long time (~ 30 minutes) before the memory can be ready for re-program operation. Besides, for the UV exposure the memory chip needs to be taken out of the circuit. Once erase

operation is completed, it can be re-inserted into the electrical circuit. It is not possible to erase part of the memory within that chip, only the entire memory content of that chip is erasable. Due to the cumbersomeness of erasing process, it is rarely erased and is primarily used as read-only memory.

1.2.7.3   EEPROM

EEPROM is Electrically Erasable Programable Read-only Memory. This non-volatile memory is electrically erasable and is based on Floating Gate Tunneling Oxide MOS (Metal-Oxide-Semiconductor) transistor and is like the one discussed in Fig. 1.25 in flash memory. It is also called as double-E-PROM or E-E-PROM. The schematic of EEPROM memory array is shown in Fig. 1.35. Each EEPROM memory cell contains two transistors- one double gate transistor as discussed in EPROM and one usual transistor called access transistor. However, over drain area the oxide thickness is very small (< 100 Å). So, if a very high voltage is applied at CG electrons from drain end can easily tunnel through the thin oxides and reach floating gate (FG). Since the oxide thickness is very low, this process can be very fast. Since the additional select transistor is connected to the drain of the double gate transistor, the voltage available at BL reaches drain end only when the corresponding select transistor is ON. Again, there are additional WLs to turn ON the select transistor. The desired cell can be easily be selected and programming can be done at the bit-level. During the erase operation select transistor also ensures that only the target cell is erased, and unwanted neighbor cells are not affected by that operation. It can be noted that in EEPROM electron reaches FG by tunneling the thin oxide barrier, whereas in EPROM electron

is implanted into FG through high electric field induced implantation. The program, read and erase operation of EEPROM memory cell is described below [59-61].

1.2.7.3.1   Program Operation:

During the program operation electrons are tunneled through the thin tunnel layer and are trapped into FG using Fowler-Nordheim tunneling as discussed in Fig. 1.30. The select transistor of that target cell is turned on by applying voltage to the corresponding word line (WL). Low voltage (0 V) is applied to the BL and through access transistor it reaches the drain end of the
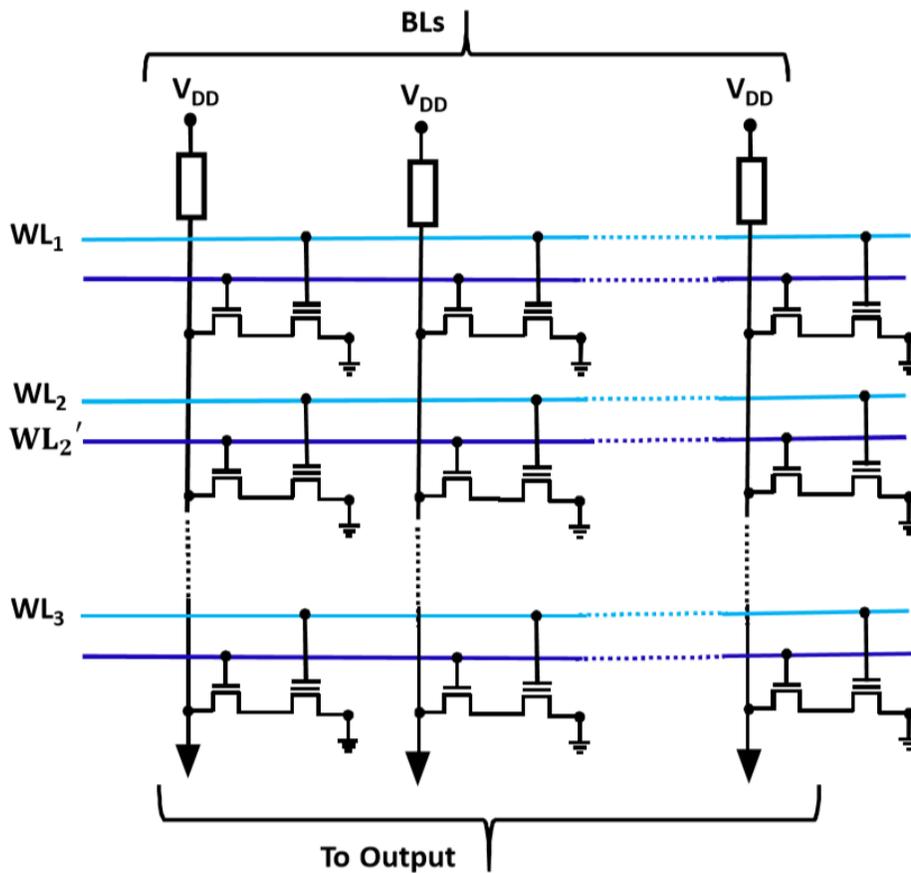
Fig. 1.35*: Schematic of EEPROM memory cell array [59]*

target cell. Since $V_{DS} = 0$ V is only applied to the target cell (by turning ON that corresponding select transistor only), all other cells are floating and not affected. Now, high voltage between CG and drain end of target cell leads to very high electric field. As a result, electrons can easily tunnel through the thin oxide layer at the drain end and reach FG. The cell is then programmed and 'bit 0' is stored in that memory cell.

1.2.7.3.2   Read Operation:

The read operation is very similar to the read operation in EPROM. Programmed (written) cell has increased threshold voltage and the inverted channel is not created by applying read voltage (V_{READ}) at CG. Therefore, with V_{DS} applied to drain the channel current is negligibly small and cell can be identified as programmed. On the other hand, non-programmed cell has normal threshold voltage (V_t) and inverted channel can be easily created by applying V_{READ} at CG. Application of V_{DS} at drain end will result large amount of current flowing into the channel and the cell thus can be recognized as non-programmed cell ('bit 1').

1.2.7.3.3   Erase Operation:

The erase operation is conducted using Fowler-Nordheim tunneling where stored electrons at FG are removed through tunneling as discussed in Fig. 1.28. Low voltage (0 V) is applied to the gate (CG) of the cell to be erased. The corresponding access transistor is turned ON through respective WL. High voltage (25 V) is applied to the drain end through BL. The high electric field created between CG/drain will cause electrons stored in FG to tunnel into drain end and the cell will be erased. Without presence of any access transistor all cells sharing the same BL will have high electric field between their CG/drain and hence all cells might be erased. Therefore, with

access transistor it is possible to conduct erase operation on the bit-level and one cell is erasable at one time.

Since EEPROM uses two (2) transistors per memory cell its density is lower. But, the memory cell is electrically erasable, and it doesn't require to take the chip out of the electrical circuit. The short duration, high voltage required for write/erase operation are usually generated through charge pumping circuit. Like other types of ROM (Read-only Memory), EEPROM is not as fast as RAM (Random-Access Memory). Due to being very similar, EEPROM is sometimes also called as Flash EEPROM. The major difference of EEPROM with Flash memory is that in EEPROM data can be programmed (written) or erased as one-bit at a time (one cell at a time), whereas flash memory can be erased in blocks (each block contains several cells). Therefore, erase operation in flash memory is much faster than in EEPROM. The write time in EEPROM is ~ 10 μs but its read operation is much faster ~ 10 ns [62].

1.2.7   Polymer memory

Polymer based memories have recently attracted ever-growing interest as a promising novel non-volatile memory [20]. In a standard polymer memory, an organic layer containing nanoparticles, molecules etc. are inserted between two metal electrodes. This type of memories has numerous advantages such as simple device architecture, 3D stacking capability, superior scalability, low-cost, high device density, simple fabrication process, free read/write capability etc. [20, 63, 64].

The data storage mechanism is entirely different in polymer-based memory compared to traditional electronic memories. The conductivity of the organic polymer material can be tuned by

applying suitable electric bias. The 'LOW' and 'HIGH' conductivity state of the organic layer can be used as two different memory states and information can be stored accordingly. The device fabrication process starts with patterning and depositing the bottom electrode layer. The organic later is then mixed with all desired constituting elements in a solvent and sol-gel spin coated on top of the deposited bottom electrode materials. After evaporation of the solvent by hot-furnace treatment, depending on the organic layer material viscosity and spin-speed a thin organic film with thickness of 10-200 nm can be obtained. Finally, the patterned top electrodes are deposited.
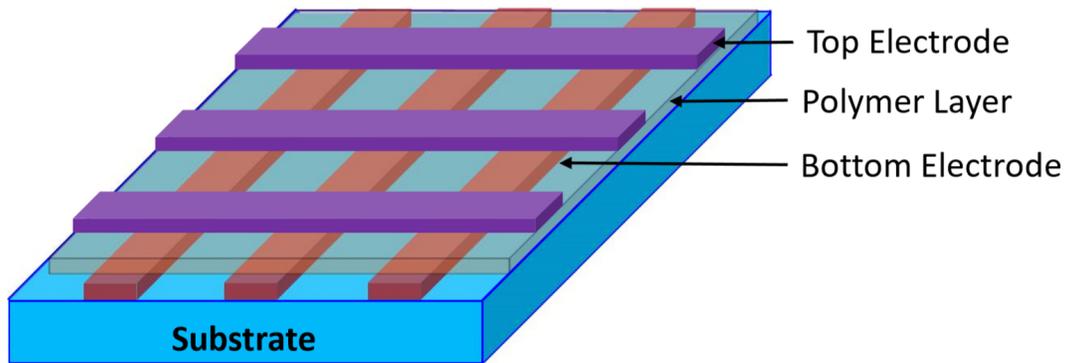
Fig. 1.36: Cross-section schematic of a polymer memory device

Since most polymer materials and constitute of long polymer chains, they are potentially integrate-able with recent state of the art high density 3D technologies [65]. A 3D schematic of polymer-based memory device is described in Fig. 1.36.

1.2.8 Resistive Random-Access Memory (ReRAM)

Resistive Random-Access Memory (ReRAM) have attracted substantial interest due to its inherent characteristic advantages such non-volatility, non-destructive readout, low-power operation, high-density, superior scalability, simple device structure, easy fabrication process,

faster switching capability, small feature size, high density integration, excellent compatibility with state-of-the-art CMOS technology etc. [66-71]. A perfect memory technology would have characteristics such as high density and high capacity, low-power consumption, long retention, high endurance, superior scalability, small feature size, high resistance ratio, tighter distribution of device parameters, high device yields, compatibility and integrate-ability with existing CMOS technology etc. [66]. Although no current memory technology possesses all those fascinating characteristics altogether, Resistive Random-Access Memory (ReRAM) has numerous technological advantages and is considered as one of the most promising candidates for non-volatile memory.

1.2.8.1   Device Architecture:

The research and development effort for resistive memory device started dated back to 1960's [72]. But this technology has been attracting significant interest due to ever increasing demand from data storage industry since 1990 [73, 74]. Resistive Memory cell (also known as
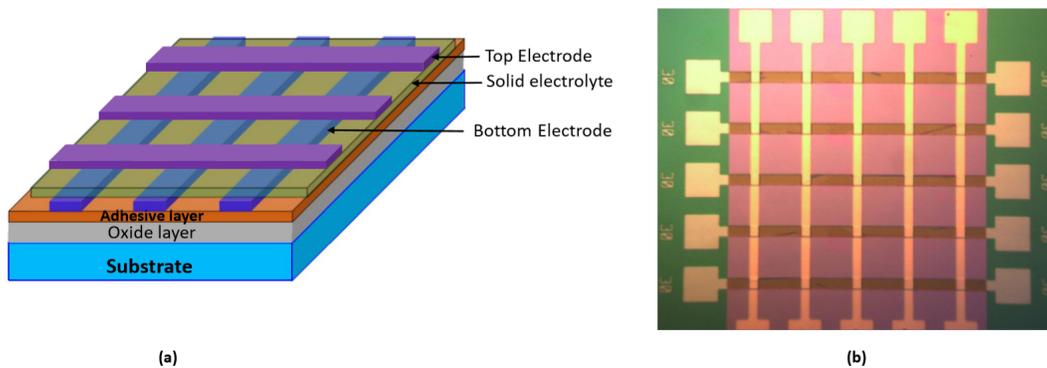
Fig. 1.37: *ReRAM memory device: a) 3D device schematic; b) Optical micrograph of a fabricated 30 X 30 μm memory cell array*

ReRAM) is a two terminal device where a thin metal oxide film is sandwiched between two metal electrodes in a Metal-Insulator-Metal (M-I-M) architecture and therefore forms an electrochemical cell. The top electrode is also called as active electrode or TE and the bottom electrode is named as inert electrode or BE. The insulator film is usually a metal oxide and sometimes is also referred as solid electrolyte. The oxide layer is conductive for ions but impermeable for electrons. The active electrode consists of metals such as Cu, Ag, Ni which can readily generate metal ions and are capable of drifting through the solid electrolyte. The bottom electrode such as Pt, W is inert, capable of stopping the ions and ideally no metal ions can penetrate through it. Metal oxide layers should be selected such that ions can be transported through it with high mobility and Cu_2S, SiO_2, TaO_x, GeS, Ta_2O_5, WO_3, AgGeSe etc. are usually used as solid electrolyte [75]. The typical ReRAM cells are arranged in a crossbar array architecture where the top and bottom electrode are running perpendicular to each other and a ReRAM memory cell is located at each intersection between TE and BE. Since the operation of this device is based on ionic migration, it is also called as nanoionics device [76]. The 3D device schematic of a standard ReRAM memory cell array along with the optical micrograph of the fabricated ReRAM array is shown in Fig. 1.37.

1.2.8.2   Memristor

In 1971 Leon Chua proposed the forth electrical element 'memory resistor' (also called as memristor) in addition to the existing three elements: resistor, capacitor and inductor [77]. He also mentioned that all resistive switching memory devices are memristors irrespective of their corresponding mechanisms [78]. The charge q and magnetic flux φ can be expressed by the following basic relations:

$$q(t) = \int_{-\infty}^{t} i(\tau) d\tau \qquad (1)$$

$$\varphi(t) = \int_{-\infty}^{t} v(\tau) d\tau \qquad (2)$$

Here i is electric current and v is voltage. But flux and charge can also be expressed as a function

of charge and flux respectively:

$$\varphi = \varphi^\wedge(q) \qquad (3)$$

$$q = q^\wedge(\varphi) \qquad (4)$$

Now the voltage v and current i can be expressed as:

$$v = \frac{d\varphi}{dt} = \frac{d\varphi^\wedge(q)}{dq} * \frac{dq}{dt} = R(q) * i \qquad (5)$$

$$i = \frac{dq}{dt} = \frac{dq^\wedge(q)}{d\varphi} * \frac{d\varphi}{dt} = G(\varphi) * v \qquad (6)$$

Here

$$R(q) = \frac{dq^\wedge(q)}{d\varphi} \qquad (7)$$

$$\text{and, } G(\varphi) = \frac{dq^\wedge(q)}{d\varphi} \qquad (8)$$

$R(q)$ and $G(\varphi)$ are called memristance and memductance respectively. Using Ohm's law and
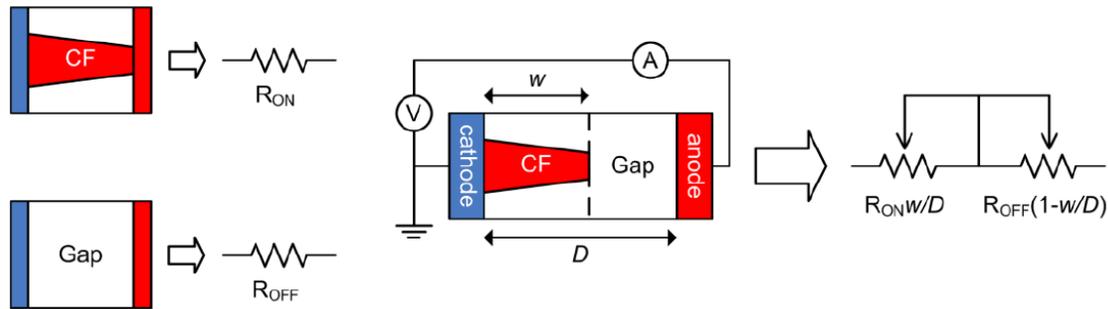
Fig. 1.38: *Equivalent circuit diagram of conductive filament based variable resistor memristor.* Reprinted

with permission from [79], copyright Springer Nature (2008)

using eq'n (5) and eq'n (7) it can be stated that, $v = i * R(q)$. But at time $t = t_0$, the memristance [R(q)] depends on the entire history of $i(t)$ from $t = -\infty$ to $t = t_0$. Similarly using eq'n (6) and eq'n (8) it can be written that $i = v * G(\varphi)$. But $G(\varphi)$ (memductance) at time $t = t_0$ depends on the entire history of $v(t)$ from $t = -\infty$ to $t = t_0$.

Therefore, the input and output of the memristor is coupled in a unique way. The present state of the memristor not only depends on itself, but also on the external applied bias as well as on the history of previous states of the device. A traditional ReRAM device can be considered as series connected high resistance and low resistance segment where the boundary between the two regions
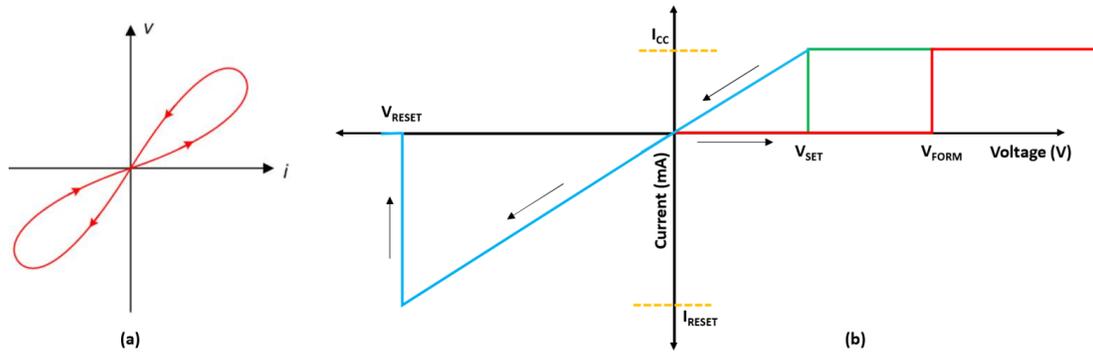
Fig. 1.39: *Signature of memristors: a) Pinched hysteresis loop schematic; b) Current-voltage characteristics schematic with key parameters*

can be tuned through externally applied electrical bias [79]. A schematic of memristor model is shown in Fig. 1.38.

In actual ReRAM device this moving boundary is the migration of metallic ions in the ion conductive solid electrolyte layer triggered by externally applied voltage. A current-voltage characteristic of memristor device with pinched hysteresis loop is shown in Fig. 1.39.

1.2.8.3   ReRAM Performance Parameters

Resistive random-access memory technology uses numerous terminologies. Some of the key terms used in this dissertation are introduced here:

FORMING Operation

RRAM is a metal-insulator-metal (M-I-M) structure with a solid electrolyte sandwiched between the two electrodes- top electrode (TE) and bottom electrode (BE). By applying high enough electrical stress through appropriate bias to the electrode, redox reaction can be triggered at electrode/solid electrolyte interface [80]. As a result, ions can migrate into solid-electrolyte through diffusion phenomena and start piling up on the other electrode. Over time it keeps growing and eventually they connect the top and bottom electrode together through either conducting filament or oxygen vacancy filament [79]. Forming is the process to create this filament for the very first time connecting the TE and BE together. The voltage at which the filament formation is completed is called as Forming voltage. FORMING is the highest voltage in ReRAM operation since the entire filament needs to be built for the very first time. FORMING operation leads to a soft-breakdown and the FORMING voltage is usually termed as V_{FORM} which increases proportionately with the thickness of solid electrolyte (or dielectric) layer.

RESET Operation

RESET is the partial rupturing or breaking of the filament connecting TE and BE together. This is primarily a thermal dissolution process due to joule's heating. For a standard conical-shaped filament geometry the maximum filament resistance is located at the narrowest region of the filament, which is also called as tip. During RESET process maximum amount of joule's heat

is produced in that region. Besides, the lowest number of atoms are also present at the tip. Therefore, during RESET process joules heating generates highly elevated temperature at the filament tip, thermally diffuse out few atoms present there and causes partial dissolution or rupturing of the filament. This process is called RESET. The voltage at which the filament rupture is completed is called as RESET voltage and is usually expressed as V_{RESET}.

SET Operation

SET is the process of rebuilding the filament to connect TE and BE together after the filament has been ruptured at least once. The voltage at which the rebuilding of filament is completed is called SET voltage and is expressed as V_{SET}. Since during RESET the filament is only partially ruptured, to rebuild the filament a smaller voltage is required compared to voltage required to build the filament for the very first time. Hence $V_{SET} < V_{FORM}$.

Compliance current (I_{CC})

This is the limiting current applied to the ReRAM cell from external circuitry during FORMING or SET operation so that as soon as the filament is formed the maximum amount of current flowing through the cell can be controlled lest the device being permanently damaged. The excess current is routed to the bypass circuitry. This limiting current is called as compliance current and is denoted as I_{CC}. This current limiting capability allows the device operation at lower current level. Therefore, the redox reaction at RESET process as well as conduction area can be well regulated. A wide range of I_{CC} is used (nA to mA) during FORMING or SET operation depending on the requirement of the filament geometry. For a fixed voltage ramp rate, higher the I_{CC} lower is the filament resistance since the filament becomes thicker by accumulating more atoms within its

filament, specially at the filament tip. But, since RESET is a thermally driven rupturing process the current is usually not limited during this process. Typical RESET current is mA to 0.1A.

Ramp Rate (rr)

Ramp rate or sweep rate ($\Delta v / \Delta t$) is the rate by which the DC voltage is applied to ReRAM

| (a) | (b) |
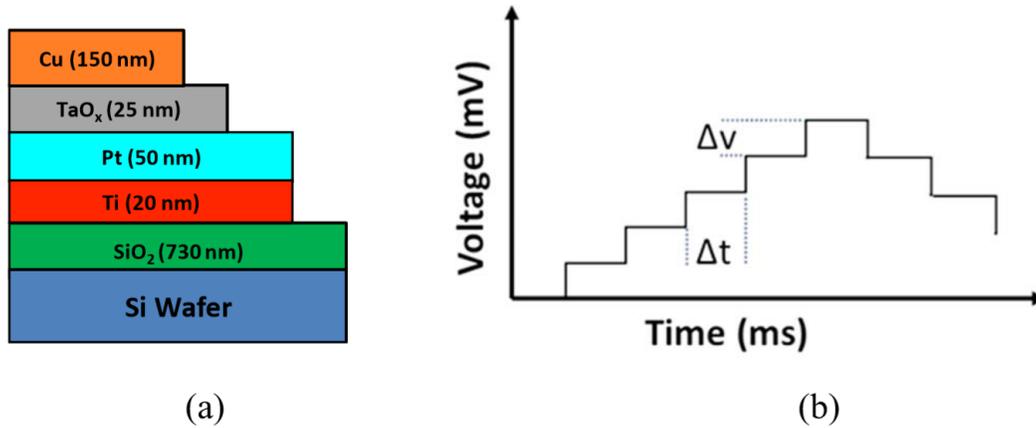
Fig. 1.40*: Schematic diagram of a) Standard ReRAM cell; b) illustration of voltage sweep mode*

cell. In other words, it is the rate of applied voltage change over time. Keithley 4200 SCS semiconductor characterization system which is used in this work for ReRAM device characterization has a 50 milli-seconds per step built-in interval time. So, during testing when ReRAM cells are stressed with DC voltage the user can choose the voltage per step and hence can control the ramp rate applied to the device accordingly. Figure 1.40 shows a cross section schematic of Cu/TaO$_x$/Pt device and illustrates the operation of voltage sweep mode. Voltage is applied to top electrode (Cu) and bottom electrode (Pt) is grounded. For example, by selecting a voltage stress rate of 0.06 v/step, the corresponding applied voltage is 1.2 v/sec

$$[0.06 \left(\frac{V}{step}\right) X \frac{1}{50*10^{-3}\left(\frac{sec}{step}\right)} = 1.2 \frac{V}{sec}].$$

R$_{OFF}$/R$_{ON}$ Ratio

After successful FORMING or SET process, a continuous filament connects TE and BE and the resistance of the filament at this condition is called as ON resistance (R$_{on}$). Since filament connects TE and BE together, the resistance is low. This resistance also depends on the limiting current (I$_{CC}$) imposed during filament building process. On the other hand, after successful RESET operation the filament is partially broken and there is no continuous connection between TE and BE. Hence, the filament resistance becomes high and is denoted as OFF resistance (R$_{OFF}$). R$_{OFF}$/R$_{ON}$ ratio is the ratio between these two resistances and is desired to be very high ($\sim 10^5$) for reliable operation of ReRAM device [81]. Very large R$_{OFF}$/R$_{on}$ ratio is also essential to realize multi-bits per cell memory storage system and would increase the memory density accordingly. The resistance ratio needs to be at least greater than ten (R$_{OFF}$/R$_{on}$ >10) to successfully distinguish between two memory states [82].

Retention Time

Retention is the intrinsic characteristics of a memory cell to retain its existing memory content. It is the length of time the memory cell can keep its memory unchanged after a successful programming (writing) or erasing operation. According to datasheet, commercial memory products can retain its memory content for several ($\sim$10 years) years.

Endurance

Endurance is the maximum number of times the memory cells can undergo successful SET/RESET operation (also called switching cycles) before the two memory states becomes indistinguishable due to electrical fatigue. Every time a cell is switched (SET/RESET), it incurs some permanent damage or degradation to the cell. Over time as the number of switching cycles

increase, there will be a critical number of cycles beyond which the device memory status after SET or RESET process is no longer separable. The device then reaches its endurance limit.

Unipolar vs. Bipolar Operation

According to the polarity of operating electrical bias, ReRAM can be classified into two types - 'unipolar' and 'bipolar'. In unipolar ReRAM cell the dominant switching mechanism is Joules heating and therefore the switching operation is independent of applied bias polarity. So V_{SET} and V_{RESET} can have the same polarity – both can be positive, or both can be negative.
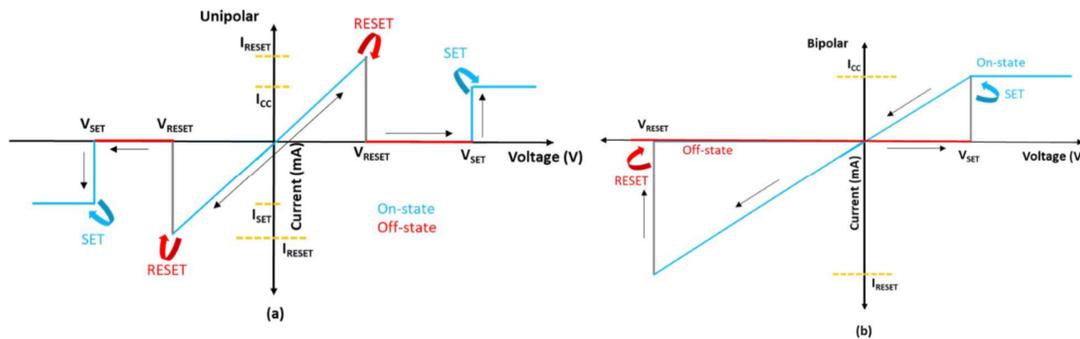
Fig. 1.41: *Schematic current-voltage characteristics of a ReRAM cell for: a) Unipolar switching; b) Bipolar switching.*

Unipolar operation usually requires high RESET current (I_{RESET}) than that of bipolar case.

Bipolar operation of ReRAM cell is the case when voltage with opposite polarity needs to be applied for successful SET and RESET operation. In bipolar case the dominant switching mechanism is redox reaction followed by electrochemical migration [83]. Since Joules heating supportively with electric field accelerates the bipolar switching operation, the switching operation therefore depends on the polarity of the applied electrical bias - polarity of V_{SET} and V_{RESET} are

67

either positive and negative or negative and positive respectively. The unipolar and bipolar switching operation is illustrated using Fig. 1.41.

1.2.8.4 I_{CC} vs. R_{on} Relationship

If R_{ON}/R_{OFF} resistance ratio in RRAM memory cell is sufficiently high ($>>10^3$), multiple bits of data can be stored in a single memory cell. One critical parameter for controlling filament resistance is limiting current (I_{CC}). By applying different levels of I_{CC}, various magnitudes of low resistance state (LRS) of filament can be achieved and this characteristic dependence can be mathematically expressed as [1]:

$$R_{on} = \frac{A}{I_{cc}^{\ n}} \qquad\qquad (9)$$
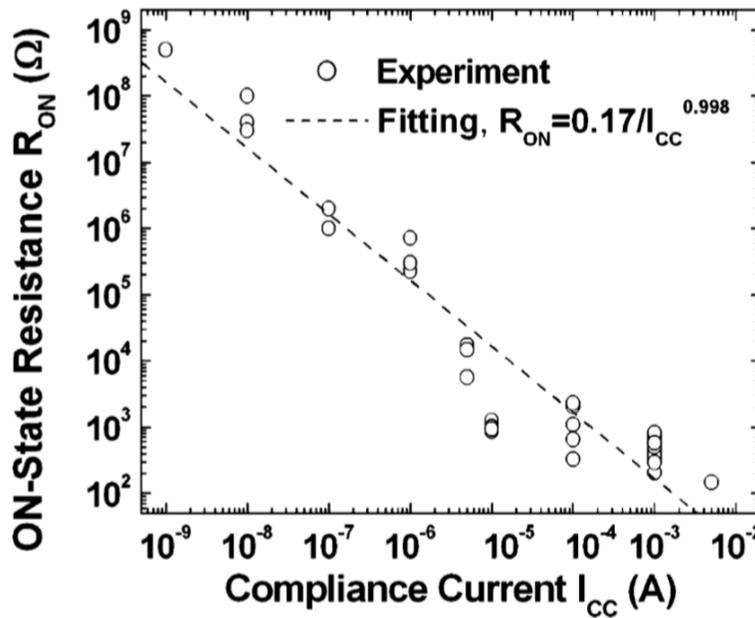
Fig. 1.42*: I_{CC}-R_{ON} relationship in Cu/TaOX/Pt ReRAM memory cell.* Reprinted with permission from [84], Copyright (c) 2013, The Japan Society of Applied Physics

68

Here, A is the minimum voltage required to SET a ReRAM cell and is independent of switching mechanism. Its unit is voltage. n is a fitting parameter with a value closer to 1 ($n \cong 1$). Figure 1.42 shows the I_{CC}-R_{ON} relationship for Cu/TaO$_x$/Pt device. In this case, by fitting the experimental data it was found that n= 0.998 and A=0.17 V [84]. For low resistance (LRS) value larger than 12.9 KΩ (R_{on}> 12.9 KΩ, the gap between growing filament and electrode are very small. Electrons tunnel through this gap and hence lead to non-ohmic I-V characteristics [85]. For R_{ON}< 12.9 KΩ, the nanofilament grows radially and the ohmic behavior of I_{CC}-R_{ON} characteristics can be explained with proposed model [86].

1.2.8.5 Ramp Rate (rr) Dependence of V_{SET}

During characterization of a ReRAM cell, usually a DC bias is applied to it with a predetermined fixed ramp rate. When this applied voltage is smaller than FORMING or SET voltage ($V_{APPLIED}$< V_{FORM} or $V_{APPLIED}$<V_{SET}), very low level of current flows through the cell. As

(a)

(b)
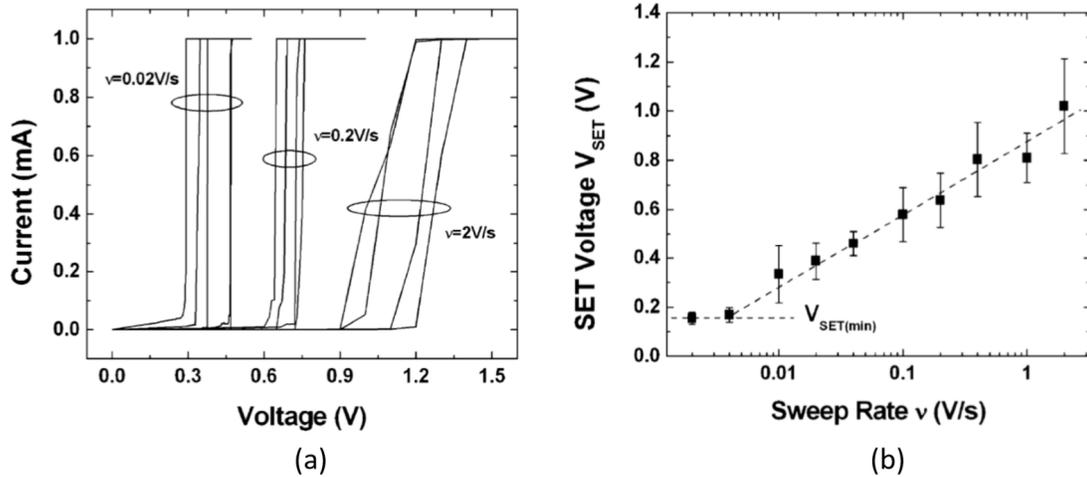
Fig. 1.43: a) Current-voltage characteristics of Cu/TaOx/Pt device with ramp rate= 0.02, 0.2 and 2 v/s; b) Dependence of V_{SET} on voltage sweep rate. Reprinted with permission from [84], Copyright (c) 2013, The Japan Society of Applied Physics

69

soon as the voltage reaches V_{SET}, the current suddenly increases and reaches the compliance current level (I_{CC}). To investigate the impact of sweep rate on filament characteristics the sweep rate of the applied DC bias was varied with three orders of magnitude and filament resistance was found to be independent of sweep rate [84]. This phenomenon is illustrated in Fig. 1.43 where the sweep rate is varied from 0.01 to 2 v/s. This was an expected outcome for constant compliance current level (I_{CC}) according to equation (1). In the first phase, before the I_{CC} limit is reached filament growth continues, and its resistance keep reducing due to the applied voltage V_{CF} across the filament which can be expressed as, $V_{CF} = I_{CC} * R_{CF}$. In the next phase I_{CC} limit is reached, but R_{CF} continues to drop due to filament growth along the radial direction. There is a minimum voltage below which cations cannot nucleate and filament growth cannot continue anymore. The reduction of resistance come to an end and results with a constant filament resistance [84]. Although V_{SET} changes with sweep rate (low sweep rate results with low V_{SET} and vice versa), $V_{SET\,(min)}$ is the lowest SET voltage for a small sweep rate which can be expressed as:

$$V_{CF} = I_{CC} * R_{CF} = V_{SET(min)}$$

Although reduction of sweep rate reduces V_{SET}, the time to complete SET operation increases with reducing sweep rate [84] and can be shown mathematically by the following relationship [87]:

$$t_{SET} = \frac{V_{SET}}{\nu} \cong \frac{lin\,\nu}{\nu} \qquad (10)$$

1.2.8.6 Quantized Conductance in RRAM Cell

If the switching duration is longer and sweep rate is slow enough, the transition region near V_{SET} can be investigated in detail. For a sweep rate of 0.002 V/s and $V_{SET} = 0.16$ V, the conductance was found to change with integer multiples of quantum unit G_0 from the I-V characteristics of

Cu/TaO$_x$/Pt device [88]. For this device the conductance changes from $1 * G_0$ to $2* G_0$ and $4* G_0$, where $G_0 = \frac{2*e^2}{h} = 77.5\ \mu S = 12.91\ K\Omega^{-1}$; here h is Plank's constant and e is electron change [88]. The mechanism of this quantum conductance phenomena was hypothesized due to tunneling of electron from single to multiple atoms during current-voltage sweep operation [89-94]. Fig. 1.44 shows the I-V characteristics of Cu/TaO$_x$/Pt device with quantum conductance phenomena until the voltage is closer to V$_{SET}$. At that point the rate of change of current is too fast to observe any distinctive quantized levels [84].

Quantized conductance was also observed in ReRAM cell with graphene nanoplatelets suspended into P3HT polymer (3-hexylthiophene) at room temperature and zero magnetic field [95]. It was observed that from HRS (100 KΩ) to LRS (5 KΩ) the conductance changes with
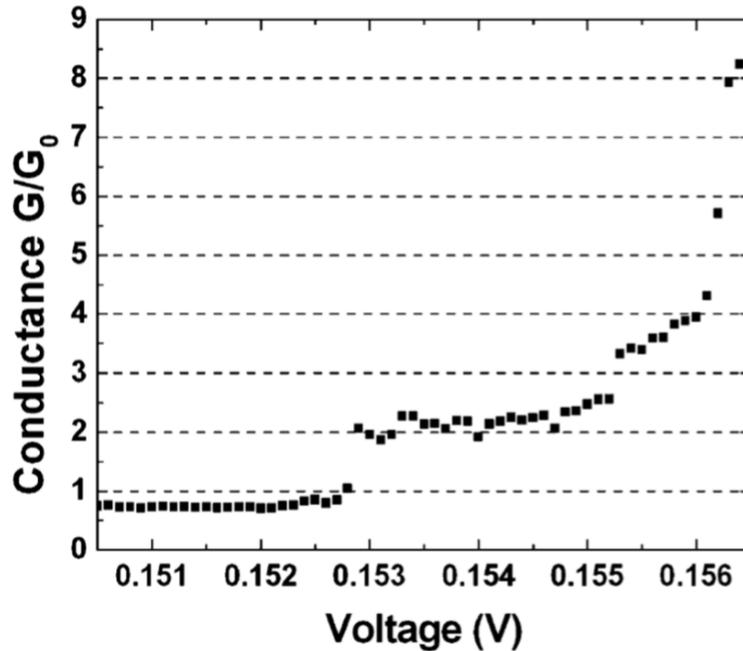
Fig. 1.44: *Quantum conductance observed in current-voltage characteristics of Cu/TaOx/Pt device for V<V$_{SET}$ where voltage sweep rate=0.002 v/s, G$_0$ = 2e^2/h* ,Reprinted with permission from [84], Copyright (c) 2013, The Japan Society of Applied Physics

multiple discrete quantized levels (multiples of G_0) without any flat plateaus. The energy consumed during these quantized levels are calculated to be much higher than thermal energy (κT) and therefore any dominating thermal contribution is eliminated [95]. Figure 1.19 illustrates the quantum conductance observed during SET operation of graphene suspended P3HT polymer based ReRAM cell at room temperature and zero magnetic field.
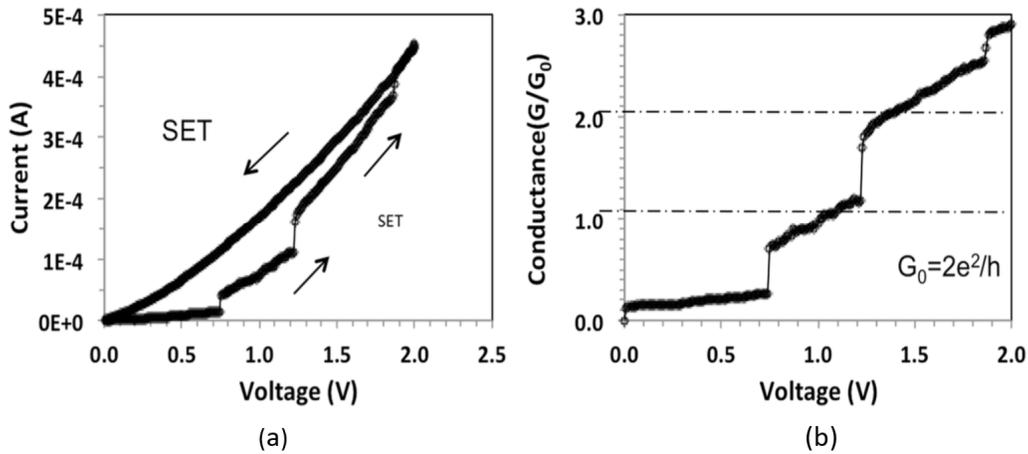
Fig. 1.45: *a) Current-voltage characteristics of Au/GNP/P3HT/Cu device; b) Conductance vs. voltage characteristics.* Reprinted with permision from [88], Copyright, Nanoscale Research Letters (2016)

1.2.8.7 Fundamental of ReRAM Memory Cell

Depending on the presence or absence of continuous conductive filament (metallic conductive filament or vacancy filament) between the top and bottom electrode, the resistance of a ReRAM cell between the two electrodes can be either LOW or HIGH respectively which is usually termed as Low Resistance State (LRS) or High Resistance State (HRS) respectively. When the device resistance is HIGH the memory cell is OFF (no continuous filament exists between TE and BE), the memory state is '0'. On the other hand, when the two electrodes are connected the device resistance is LOW, the memory cell is ON, and the memory state is '1'. The corresponding

72

device resistance is referred as R_{ON} which can be precisely controlled through a limiting current I_{CC} (also known as compliance current) by using the I_{CC}-R_{ON} relationship. By applying appropriate bias, the device resistance can be changed from HRS to LRS in a process called SET operation. The written memory content (LRS state) is preserved until an appropriate electrical stress changes the memory state from LRS to HRS in a process named as RESET or erase operation. During both SET and RESET process a minimum voltage (called as threshold voltage) needs to be applied to toggle the device resistance between LRS and HRS and the corresponding voltages are called as SET voltage (V_{SET}) and RESET voltage (V_{RESET}) respectively. Since the filament connects the top and bottom electrode through a conductive filament bridge it is also called as Conductive Bridge RAM or CBRAM. To form a conductive bridge in a fresh cell, a relatively higher voltage (called $V_{FORMING}$) is to be applied during the electroforming process since the entire filament needs to be established. Since RESET process only partially ruptures the filament, for the subsequent filament formation smaller voltage (V_{SET}) is required. Hence V_{SET} is usually smaller than $V_{FORMING}$.

1.2.8.7.1   Switching Operation of ReRAM Cell

The switching mechanism in nanostructure ReRAM cell is primarily due to electrochemical reaction at the top electrode/metal oxide interface due to electron transfer between them through a process known as redox (reduction-oxidation) reaction. Without any external applied bias, the oxidation current and reduction current balances each other resulting with zero net current. However, with an applied electrical stress one component will dominate and therefore either oxidation or reduction reaction is usually observed at one time at the electrode/electrolyte interface.

In ReRAM, the device resistance is independent of cell size and therefore localized filamentary switching mechanism is proposed. According to the widely accepted switching mechanism, the ReRAM cells can be classified into the following two types: -

i.   Anion-type ReRAM

ii. Cation-type ReRAM

The switching operation of anion-type is dominated by migration of negatively charged oxygen ions towards the TE (active electrode) and thereby formation of vacancy filament (V_o). In cation-type, the prevalent mechanism is redox reaction and formation of metallic conductive filament is due to migration of positively charged metal ions from the TE (active electrode) through the meal oxide (solid electrolyte) towards the BE (inert electrode).

i.   Anion-type ReRAM

When negative bias is applied to the TE of ReRAM cell redox reaction occurs at the electrode/electrolyte interface according to the following equation (11):

$$Cu \rightarrow Cu^+ + e^- \qquad (11)$$
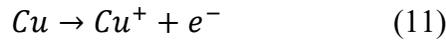
Since negative bias is applied to the TE, electrons are efficiently injected into the oxide (electrolyte) while Cu^+ ions are retracted back to TE. These injected electrons can negatively charge the oxygen present in the metal oxide. As the O^{2-} ions migrate from top electrode toward the bottom electrode under the applied electric field, they leave a charge neutral oxygen vacancy (V_o) in that lattice position in accordance with the reactions shown in eq'n (12):

$$TaO_X + 2*e^- \rightarrow TaO_X^{-1} + O^{2-} \rightarrow TaO_X V_o + O^{2-} \quad (12)$$
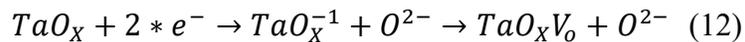
Again, oxygen vacancies have Fermi level very close to the conduction band ($E_F \cong E_C$) and therefore more vacancies will form under the previously created one. As this process continues the

vacancy filament (V_o) will continue to extend into the oxide, which in turn lead to ever-increasing electric field between the end of vacancy filament (V_o CF) and BE. Due to this self-accelerating growth process the vacancy filament will eventually connect the TE and BE together and can serve as a moving channel for electrons. The resistance of vacancy filament thus changes from HRS to LRS in the so-called SET process. The growth process for the vacancy filament is illustrated in Fig. 1.46. Singly charged oxygen ion is very unstable in metal oxide and therefore will not contribute vacancy according to equation (1). During the RESET operation, oxygen ions recombine with vacancy and the device resistance changes from LRS to HRS. This type of switching mechanism is demonstrated using SiO_2 as well as metal oxides such as WO_x [97, 98], HfO_x [99-104], TaO_x [105], AlO_x [106, 107] etc.

Again, the electrons generated according to eq. (1) can hop within the bulk metal oxide
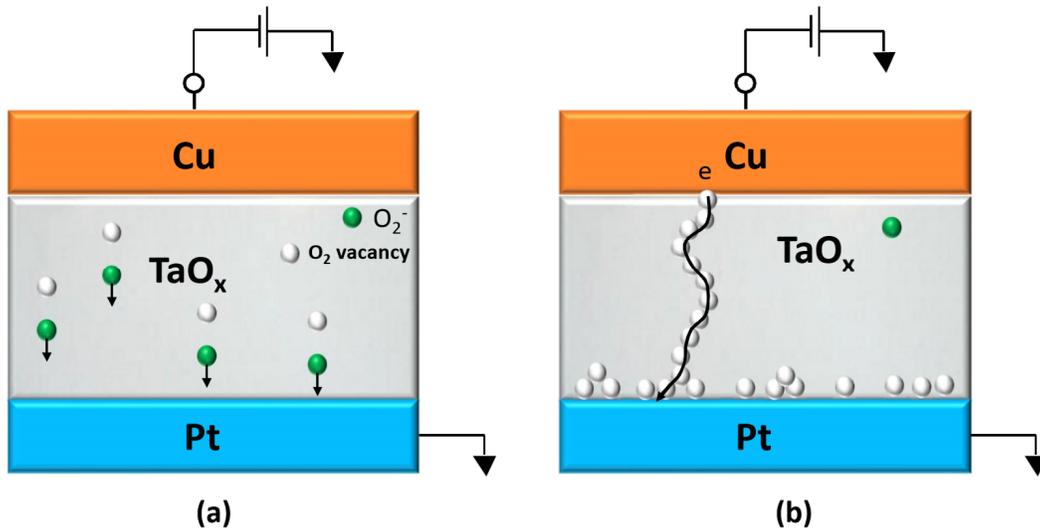
Fig. 1.46: *a) Generation of oxygen vacancy; b) Formation of conductive path [96]*

(electrolyte) and generate vacancy which accumulates over time and after reaching above a certain threshold it can provide 'conductive percolative path' between the TE and BE [96]. However, this

process is more relevant to dielectric breakdown of oxide, more stochastic in nature and does not contain any self-accelerating phenomena. It is therefore not an efficient process for conductive vacancy filament [V_o CF] formation.

ii. Cation-type ReRAM

This switching operation is governed by redox reaction and transportation of metal ions into the oxide. When positive voltage is applied to the TE, it triggers electrochemical reaction and oxidizes the electrode to create metal ions according to eq'n (13). The generated metal ions are very mobile and can be moved within the ion conductive electrolyte by applying electric field. Therefore, the electrons are retracted back to electrode whereas the Cu^+ ions are injected into the oxide layer (electrolyte) and are drifted towards the BE. When Cu^+ ions reach BE (inert electrode),
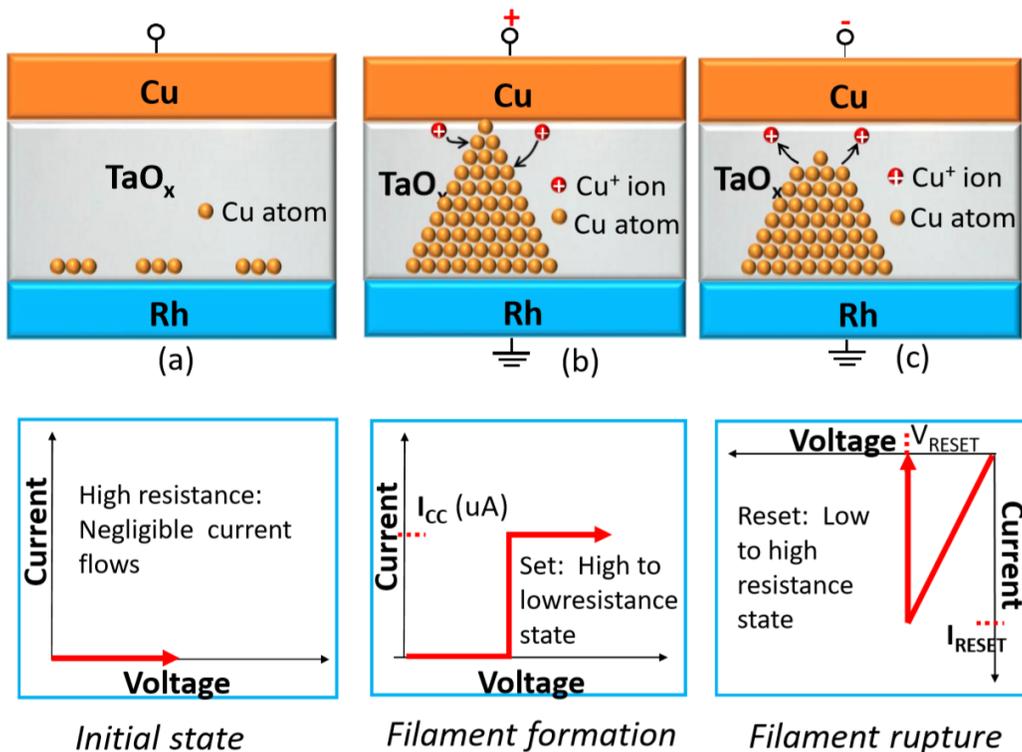
Fig. 1.47: *a) Initial High Resistance State (HRS); b) Formation of filament during SET operation; c) Rupturing of filament during RESET operation*

76

they are reduced and converted back to metal atoms in accordance with the reduction reaction

shown in eq'n (13):

$$Cu^+ + e^- \rightarrow Cu \qquad (13)$$
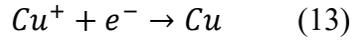
As this process continues the accumulated Cu atoms nucleate, stack on top of each other and the

filament grows in a zigzag pattern and continue to extend into the oxide. The electric field between

the end of filament and TE increases further. The extended filament thus grows at an ever-

accelerated rate until the TE and BE are connected through the nanoscale conductive metallic

filament (CF). The device resistance then changes from HRS to LRS in a so-called SET operation.

This metallic nanofilament will be preserved until sufficient energy is provided to remove some

of its atoms. If the bias voltage is reversed (negative voltage is applied to the TE instead) Joules

heating is triggered at the location of highest resistance of the filament (at the tip of the filament)

and electrochemical dissolution can partially rupture the filament and the filament resistance

changes from LRS to HRS. This process is known as RESET operation. Figure 1.47 illustrates this

switching operation in detail. This type of ReRAM is CMOS compatible, has very high R_{ON}/R_{OFF}

ratio, low operating voltage, multi-bit per cell capability and can potentially replace SRAM by

1T2R architecture [83, 108].

1.2.8.8   Other common mechanisms for switching operation

Among the other mechanisms space-charge constrained conduction (SCLC), charging-

discharging of trap, Pool-Frenkel emission, Schottky emission etc. are also commonly popular

[66]. SCLC mechanism is dominated by defects where small-voltage region has ohmic

characteristics (I $\propto$ V) and square law ($I \propto V^2$) relationship for voltage higher than trap-filled

voltage [66]. In trap charging-discharging case, it follows either negative differential resistance (NDR) or I-V characteristics with a N-shape behavior [109, 110]. Thermionically emitted electrons over applied electric field induced reduced barrier is the basis of Schottky emission mechanism. According to Pool-Frenkel mechanism the trapped electrons can be moved into the conduction band through electric field excitation [66].

1.2.8.9   State of the art ReRAM technologies

The performance of ReRAM memory cell is reliant on characteristics of both TE and BE [111, 112]. Different electrode materials can have varied work functions, dissimilar level of barrier height at electrode/solid-electrolyte interface and can even form different type of contacts-ohmic vs. Schottky [66]. Depending of the level of voltage drop across electrode/solid-electrolyte interface (low voltage-drop for ohmic contact or small Schottky barrier height, high voltage-drop for large Schottky barrier height), the effective applied electric field may or may not be able to successfully trigger the switching operation in the memory cell [113, 114]. Although, typically FORMING operation is followed by subsequent SET operation and requires larger voltage ($V_{FORMING} > V_{SET}$) FORMING-less switching operation is recently demonstrated with Au (TE)/ZrO_2/Al (BE) structure and is attributed to the deoxidizing characteristics of Al [66]. It was hypothesized that O^{2-} ions generated from ZrO_2 reacts with Al and creates large number of oxygen vacancies for subsequent formation of conductive filament. It was also reported that ease of electrochemical reactions and metal ion migrations into the solid electrolyte is the key factor for an excellent switching characteristic [111]. Doped oxides have been demonstrated to significantly improve endurance, retention time and switching time and is attributed to creation of homogeneously distributed electron traps. [111, 115, 116]. Via-hole structure is also a prevalent

approach to realize tighter distribution of switching voltage for potential eradication of sidewall and corner effects in the fabricated device geometry [117]. Oxygen ion conductive buffer layer such as Ti or TiO_X between TE and electrolyte can absorb oxygen atoms or modulate barrier height at the interface and improves the switching characteristics further [118, 119]. The one transistor ReRAM or 1T1R device architecture provides smaller reset current (I_{RESET}) and therefore leads to uniform switching characteristics [119] and has great potential to emerge as future functional memory by replacing currently popular flash memory [120, 121].

Reversable and non-volatile ReRAM cells with real world applications was first demonstrated in 2002 [122, 123]. 64-bit perovskite -oxide based ReRAM cells were reported by Zhuang et al. [124]. Samsung Advanced Institute of Technology successfully demonstrated low power operation (<3V, 2mA) of ReRAM cells based on binary transition-metal-oxide with switching cycles> 10^6, reading cycles>10^{12} in 2004 [125]. CuO_x based Sub-mA ReRAM cells were also reported [126]. TaO_x based ReRAM cells with excellent switching (>10^9 cycles) and retention (10 years at 85º C) characteristics were demonstrated in 2008 [127]. 1-kbit memory array with HfO_x based highly scaled 30nm memory cell was reported in 2009 [128]. Recently 64 Mbit ReRAM operation was also successfully demonstrated [129].

Resistive switching memory device holds a great promise and is a very good candidate for next generation of future memory technology. With the recent trend of IOT (internet of things), artificial intelligence (AI), autonomous driving, real-time processing, emerging neuro-inspired computing etc. and endurance, degradation and physical and technological scaling limitations of other memory technologies the significance and potential of ReRAM technology is even more pronounced. It can also potentially fill the latency gap between Flash technology and DRAM. Although recently there has also been significant progress in ReRAM technology, there

are still a lot of challenges and difficulties which need to be addressed. Enhancing the speed of write/erase operation, tightening the distribution of device parameters from cell to cell, improving endurance and retention, precisely controlling the homogeneity at electrode/electrolyte interface (for oxygen mobility), oxidation control of electrodes etc. are some of the greatest challenges which need to be addressed properly to make ReRAM technology competitive enough to supplant its rivals [130, 131]. A comprehensive understanding of device operating mechanisms is yet to achieve. However, recent discovery of novel device architecture and innovation work is expected to achieve a significant technological breakthrough in ReRAM based non-volatile technology and is expected to have future successful memory solution based on ReRAM technology very soon.

1.3   Comparison of memory technologies

ReRAM is highly scalable, compatible and integrate-able with CMOS technology and are faster than PCM with simple two terminal device architecture [132]. It is capable of storing multi-bits per cell by switching between several distinct resistance states. ReRAM is a very promising high-density future memory systems since its crossbar architecture does not requires any access transistors. However, it requires relatively high power for the write operation and the device operation parameters can vary from cell-to-cell. ReRAM can have revolutionary versatile applications in areas such as personal computer, data center, automotive, medical, military and can potentially replace Hard Disk Drives, flash memories, random-access memories etc. [133].

FeRAM combines the non-volatile memory characteristics with faster read and write time of DRAM. FeRAM is faster than flash memory and has high endurance, but the read operation is destructive. Therefore, every read operation is followed by a write cycle. FeRAM has potential

application in small consumer electronics such as smart card, security chip, hand-held phone, power-meter, personal digital assistants (PDAs) etc. and is expected to replace SRAM and EEPROM for various applications [20].

MRAM is a non-volatile memory and combines the advantage of high density of DRAM and faster operational speed of SRAM. MRAM consumes less power and is relatively faster than existing memory technologies. But MRAM is very expensive and suffers from cell-to-cell crosstalk due to penetration of magnetic field into the neighboring cells [20].

The read operation speed in PCM is comparable with flash technology, while the write operation is much faster. PCM technology allows rewrite operation without requiring any pre-erase and therefore sometimes called as perfect RAM. However, erase operation require high

Table 1.2: Comparison of memory technologies [14]

Feature	PCM	MRAM	FeRAM	STT-RRAM	RRAM	NAND	NOR
Cell Size	small	Large	Large	small	small	small	small
Storage mechanism)	amorphous /crystalline material phase	Magnetization of ferromagnetic material	polarization of ferroelectric material	torque through spin polarized current	Low/High resistance for Cu/O_2^- vacancy filamnent	electron tunnel in/out of FG	electron tunnel in/out of FG
Read time (ns)	20-50	3-20	20-80	2-20	1-20	10^4	<80
Write time (ns)	20	3-20	50	2-20	10-30	1ms/sector	1 s/sector
Endurance	10^{12}	>10^{15}	10^{12}	>10^{16}	10^{13}	10^7	10^6
Density	High	Low	Low	High	High	High	Low

density of supply current. PCM is a promising technology for future high-density, high-speed, low-cost, non-volatile memory solutions [20].

The parallel connection of cells to bit-line architecture in NOR flash facilitates cell level access for read or program operations at the expense of larger footprint. Its write and erase operations are slower but read operations are relatively faster compared to NAND [134]. NOR flash technology has both random-access and byte-level write capability and is ideal for small volume of code storage and execution applications [20]. On the other hand, series connected cells in NAND flash technology saves chip-footprint and is therefore preferred for high density, large

Table 1.3: Advantages and shortcomings of some key memory technologies [14, 20]

Types of Memory	Advantages	Shortcomings
PCM (Phase Change memory)	• Faster read • High scalability • High density	• Expensive • Poor scalability
MRAM (Magnetic random-access memory)	• Faster read, write • High endurance • Low power consumption • High density	• Poor scalability • Lager power consumption • Low density
FeRAM (Ferroelectric random-access memory)	• High endurance • Low power consumption • Faster write	• Low density • Expensive • Low capacity
RRAM (Resistive random-access memory)	• High density • High scalability • Low cost	• Large write power • Low endurance • Cell-to-Cell variability
NAND Flash	• Faster write and erase operation • High density large data storage	• No random access capability • Slow read operation
NOR Flash	• Byte-level write capability • Random access to data (byte)	• Slow write and erase operation

storage and lower cost per bit memory solutions. NAND has smaller erase block with no random-access capability and its erase and write operations are slightly faster than NOR. Application for NAND flash includes MP3 player, USB drive, memory card, digital camera, storage of large

audio/video files etc. [135-138]. Various memory technologies are compared using Table 1.2 and Table 1.3.

1.4   Organization of this thesis

The objective of this research work is to systematically investigate and explore the impact of inert electrode on the endurance, reliability and performance of the ReRAM memory cell or array, examine the crucial cell degradation mechanisms, investigate how the memory operations in a cell can affect the performance of the cells in that vicinity and find the potential solutions to alleviate this problem, if not completely eliminate and significantly improve the performance of ReRAM memory cell arranged in a crossbar array architecture. All the cell degradation phenomena and proposed solutions have been investigated experimentally.

Chapter 1 sets the foundation of this dissertation and describe the essential theories, fundamental physics, key operation mechanism etc. The basic operating principles of major conventional memories as well as emerging memory technologies including ReRAM are illustrated in a comprehensive manner.

Chapter 2 describes the Resistive Switching Memory devices (ReRAM) in detail. It includes challenges to implement ReRAM devices in existing CMOS technology, choice of materials for top electrode, solid electrolyte and bottom electrode with underlying physics and material characteristics. The device fabrication, characterization and performance analysis of standard $Cu/TaO_x/Pt$ has been conducted in detail, which serves as a benchmark for the devices later described in this dissertation. Finally, the instability of ReRAM cells during the read operation was investigated in detail and some possible mechanism is hypothesized.

Chapter 3 presents step-by-step detailed fabrication process flow for all the devices fabricated for this dissertation. All the ReRAM devices are fabricated in a crossbar array architecture using Virginia Tech nanofabrication & characterization laboratory. A brief introduction of all relevant processing technologies has also been included.

Chapter 4 investigates $Cu/TaO_x/Ru$ ReRAM memory cells in detail. Its device fabrication, characterization methodology, switching characteristics, device embedment issues etc. has been analyzed comprehensively and possible device degradation mechanism and filament geometry has been proposed. This is followed by XRD analysis of several thin material stacks to experimentally demonstrate the key reactions involved and compounds formed during the device operation. Some key generated compounds responsible for device failure have been identified and supported with numerous research work related to those compounds. Some potential solutions have also been experimentally demonstrated to significantly improve the device performance in this regard.

Chapter 5 introduces an important property of the bottom electrode-heat conductivity and experimentally demonstrates how critical this property is for reliable and enhanced device performance. Several device structure and test methodologies has been presented to extrapolate the device parameters affected by this effect and device operation mechanism has been proposed in terms of filament flux.

Chapter 6 introduces a novel effect "cell-to-cell thermal crosstalk" and experimentally demonstrates how this effect can significantly impact the performance of memory cells arranged in a crossbar array architecture. New device parameters have been proposed to measure this degradation effect. This is followed by proposed solutions to significantly alleviate this issue. Several device structures incorporating potential solutions have been experimentally demonstrated and the proposed solutions have been validated experimentally.

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Chapter 2: Resistive Random-Access Memory (ReRAM)

2.1   Introduction

While the scaling of conventional memories such as volatile dynamic random-access memory (DRAM) and nonvolatile flash technologies is getting increasingly difficult, novel types of non-volatile memories, such as resistive-switching memories have lately been of attention to both industry and academia [1-9]. Resistive switching memory is being considered for next-generation non-volatile memory due to its relatively high switching speed, superior scalability, low power consumption, good retention and simple structure [10-12]. These two-terminal devices have figure eight-like pinched current–voltage (I–V) hysteresis and operate by changing resistance from high resistance (HRS) state (OFF-state) to low resistance (LRS) state (ON-state) in response to applied voltage or current due to the formation and rupture of a conductive filament. In particular, Conductive Bridging Random Access Memory (CBRAM), also referred as Programmable Metallization Cell (PMC), is a promising candidate for resistive memory device due to its highly scalable and low-cost technology [13]. Currently, the interconnect RC scaling methods have reached their limits and there is an urgent need for alternative ways to reduce or remove the latency constraints in CMOS low-k/Cu interconnect. One method is building CBRAM directly into a low-k/Cu interconnects to reduce the latency in connectivity constrained computational devices and the chip's footprint by stacking memory on top of logic circuits [14-16]. This is possible since the Cu metal lines and low-k/Cu interconnect already prefigure a potential RS device, and the cross-bar architecture of a typical two-terminal RS device array is essentially the same as a CMOS metal interconnect system. Thus, the interconnect information

95

bottleneck could be untied and morphed into several system architectures using the same basic universal hardware platform.

A CBRAM device consists of an insulating/solid-state electrolyte layer sandwiched between an oxidizable active anode and an inert cathode. Different dielectric and semiconductor materials have been investigated as solid electrolytes in CBRAM cells, such as GeSe, GeS_2, WO_3, ZnO_2, Al_2O_3, Ta_2O_5 or TaO_x [17-20]. The active metal can be any oxidizing metal like Cu, Ni or Ag which has a high activation energy, thus yielding ions readily [21-23]. The inert metal material is usually Pt, Ir or W, which are the stopping barriers of Cu, Ni and Ag cations. Under application of a positive bias to the active electrode, Cu^+ or Ag^+ ions are generated and migrate through the solid electrolyte. These ions accumulate at the inert electrode. The accumulated atoms nucleate and grow to form a nanoscale metallic conductive filament (CF) connecting both electrodes, so-called FORMING and SET processes. Under reverse bias the filament is electrochemically dissolved, and the cell is switched back to the HRS, so-called RESET process. The ON/OFF ratio of CBRAM is usually significantly higher than 10^3 [24] and potentially allows multilevel switching operation in a single memory cell to store multiple bits of data [25].

One strong candidate for non-volatile memories is the well-behaved and well-characterized $Cu/TaO_x/Pt$ resistive switching device due to excellent unipolar and bipolar switching characteristics, device performance, retention and reliability [26]. This device can be operated as a memory cell with copper (Cu) or oxygen vacancy (V_o) conductive filaments. This Pt based ReRAM memory cell is considered as a benchmark device in this work and a detailed analysis of its fabrication, characterization, testing and performance investigation is included in this chapter.

2.2   Challenges to Implement Resistive Memory Cells in the CMOS BEOL

There are manifold challenges of implementing resistive switching memory cell into back-end-of-line of CMOS [27]. The challenges include not only the choice of materials of a stand-alone CBRAM cell, but also the way the cell is embedded in BEOL [28]. In case of the inert electrode, a composite electrode is required with appropriate glue layer, heat transport layer, and inert metal proper with sufficient thermal conductivity, low miscibility with, and low surface diffusivity of the active metal atoms. The active metal is required not only to allow for a copious redox reaction but also to simultaneously prevent reactions with the dielectric. A dielectric is preferred with a moderate level of defects which may be controlled by deposition processes. Finally, the choice of the materials is gated by the material and process compatibility with BEOL, as well as by the dynamics of resistive switching operations, including Joules heat during SET and RESET operations.

The integration challenge of implementing a well-behaved memory cell array into backend CMOS can be illustrated broadly by the likely consequences of an attempt to integrate a stand-alone resistive switching cell that has been carefully engineered to satisfy all the non-volatile memory array requirements and specifications. When seeking to embed such an optimized memory array into the back-end CMOS, it would, most likely, turn out that, either the memory cell materials are incompatible with BEOL materials and/or manufacturing processes, or it would lead to prohibitively high manufacturing costs, or, even when cost-effective and material- and process-compatible, the embedded memory array would display dramatically degraded electric behavior or fail altogether. In the following section, the challenges as well as design considerations of a highly reliable and best possible ReRAM memory cell along with each of its key layers is discussed in detail incorporating data obtained from recent experiments conducted in this work.

2.2.1   Choice of Active Electrode Metal

The reaction leading to the supply of metallic cations is the redox reaction (1). In case of Cu which is characterized by an ionization energy of 7.7 eV there is a copious production of Cu^+ ions and electrons. Experiments with metals with higher ionization energies such as Pt in $Pt/TaO_x/Pt$ devices have shown much lower injection levels of electrons and therefore much higher forming voltages for oxygen vacancy filaments which are driven by the reaction (2). The ionization energy is only indicative for the efficiency of the reaction (1) since the reaction takes place at the interface to the dielectric. The $Ta/TaO_x/Pt$ devices have shown [29] clearly that although Ta's ionization energy, 7.55 eV is slightly lower than that of Cu, 7.72 eV, the redox reaction Ta $\longleftrightarrow$ Ta^+ + e- is significantly less efficient than for Cu. The reason for the low Ta oxidation reaction is that in oxygen deficient, i.e. Ta rich TaO_x with $x \approx 2$ is less favorable than for Cu. However, Ta^+ electromigration in TaO_x appears to occur at a faster rate than that of Cu. Metals with low ionization energies, such as Ti (6.83 eV), are also ill-suited as candidates for the active electrode. Analysis of $Ti/TaO_x/Pt$ and $Cu/TaO_x/Ti$ devices has shown that Ti^+ ion undergoes a rapid reaction with oxygen of TaO_x leading to a formation of a conductive TiO_{2-x} layer. Thus, the Ti oxidation reaction is fast, but Ti^+ are immediately consumed in Ti silicide reaction. In fact, neither Ti filaments nor presence of free Ti^+ ions in TaO_x could be deduced [29].   It appears that Cu has a moderate ionization efficiency which, on the one hand, precludes a chemical reaction with the dielectric and, on another hand, provides a large supply of electrons and Cu^+ at the Cu-TaO_x interface. Ti (6.8 eV) has a lower ionization energy than Cu (7.7 eV) which leads to a strong reactivity with an oxide dielectric. As a consequence, neither electrons nor Ti^+ ions are being provided. Thus, Cu (7.7 eV), Ag (7.6 eV), and Ni (7.6 eV) with moderate and very similar ionization rates appear to be the optimal cations for resistive switching. In fact, these are the three

metals for which metallic filament formation has been reported. The inert Pt electrode has a very high ionization potential (9.0 eV) which precludes an efficient redox reaction and hence the difficulty to form V_o filaments than in $Cu/TaO_x/Pt$ devices. Also, the stopping power of the Ti electrode for Cu ions is significantly lower than that of Pt, while the stopping power for Ta is not as good as that of Pt but still significantly larger than that of Ti.

From the cross-comparisons between the various devices a consistent picture emerges of mechanisms responsible for the formation of the filaments and their properties. Following mechanisms are responsible for the filament formation and the characteristics of its hypothesized geometric shape: (i) moderate efficiency of the redox reaction (1); not too low to provide enough metal cations and electrons, but not too high to undergo reaction with the matrix of the solid electrolyte. (ii) Metal oxidation is responsible for the efficiency of electron injection. This is important when the conductive filament is a defect filament such as oxygen vacancy. (iii) Sufficiently high diffusivity of cations in the solid electrolyte. (iv) High cation stopping power at the inert electrode (dissolution of cations in the counter-electrode). (v) Low interface diffusivity of neutralized cations along the inert electrode/solid electrolyte interface.

2.2.2   Choice of Solid Electrolyte

In most cases, it is desirable that the solid electrolyte should exhibit a moderate level of defectivity. Point defects such as oxygen vacancies or even extended defects such as nano-pores are conducive to ion electromigration. When comparing, for example, oxygen deficient TaO_x with stoichiometric Ta_2O_5 layers with higher density than TaO_x films, $Pt/TaO_x/Pt$ and $Ti/TaO_x/Pt$ devices showed consistently superior performance with their counterparts with Ta_2O_5 [29]. Similar observations have been made elsewhere in literature. According to Brumbach et al. [30] x=2 in

TaO$_x$ is the most favorable stoichiometry for resistive switching. SiO$_2$ dielectrics deposited with PVD and showing much higher defectivity than thermally grown oxides deployed in Cu/SiO$_2$/Pt devices allow only for a reliable resistive switching of Cu filaments for layers thinner than 35 nm but do not allow for dielectric defect (oxygen vacancy) filament formation [31]. However, SiCOH films which are significantly less dense than SiO$_2$ are a good candidate for resistive switching applications with forming, setting and resetting voltages well below 1V [29]. This holds also true for porous SiCOH dielectrics with porosity up to 25% [32]. However, the forming voltage for porous SiCOH appears to increase with porosity [32].

2.2.3   Choice of Inert Electrode Metal

A highly reliable and best performing ReRAM cell design requires a more thorough review of the properties of the inert metal electrode. The foremost property of the inert electrode is to be immiscible with the metal of the active electrode, in this case Cu. The desired immiscibility should hold not only at room temperature but also at elevated temperatures up to 900^0 C. When Cu ions arrive at the inert electrode it is desirable that they are stopped at the dielectric/inert electrode interface. Only when they stick to the surface of the inert electrode and agglomerate, they can build back efficiently a metallic dendrite which upon reaching the active electrode forms the conductive filament. The property of the immiscibility is often (but not always) related to the ionization energy of the elemental metal. It is seen from Table 2.1 that the metal of the inert electrode of this reference device, Pt, has a high ionization energy of 8.96 eV. Ir has similar ionization energy (8.97 eV) but first results of a Cu/TaO$_x$/Ir devices have shown poor electric performance compared with corresponding Cu/TaO$_x$/Pt device. While the relation between ionization energy and miscibility is

not fully understood, since the miscibility by its very nature involves not only the properties of the inert metal electrode but also of the active metal, the high ionization energy is nevertheless highly desirable not only in order to preclude reactions with the dielectric but also to prevent the redox reaction (1) and triggering subsequent reaction involving copiously generated electrons similar to

Table 2.1: Thermal Conductivity and Ionization Energy of Elemental Metals

Metal	Therm. Cond. W/(m·K)	Ionization Energy eV
Ag	406	7.58
Al	205	5.99
Au	315	9.23
Co	100	7.88
Cr	94	6.77
Cu	385	7.72
Ir	147	8.97
Ni	90	7.64
Pd	72	8.34
Pt	72	8.96
Rh	150	7.46
Ru	117	7.36
Ta	54	7.55
Ti	22	6.83
W	165	7.86

reaction (2) which may introduce unwanted charged defects into the dielectric.

Further required property of the inert electrode is a low surface diffusivity of active metal atoms on its surface. This is an independent characteristic of the immiscibility property. A high surface diffusivity of active metal atoms on the surface of the inert electrode would lead to weakening of the base of the filament leading to higher forming and set voltages, and likely to

cylindrical shape of the filament which are difficult to rupture. All data so far indicates that Cu surface diffusivity at Pt interfaces is low.

Another required property of the inert electrode is that the conductor stays amorphous also at elevated local temperatures as high as 900^0 C. If the inert electrode metal forms crystalline grains, the grain boundaries at the surface would allow active metal atom diffusion into the inert electrode preventing thus orderly formation of a rupturable filament.

Finally, the inert electrode should be immune to reactions with elements in the subjacent layers on the wafer. The inert electrode is separated only by a thin glue layer such as Ti from underlying passivation layers. Elements such as Si may diffuse through the glue layer and form silicides as hypothesized in the case of the Ru devices and is discussed later chapter 4.

2.3 Device Embedment issue

It was surprisingly found that the electric and RS behavior of identical devices but on different substrate layers is markedly different [27, 28]. Apparently, different embedment of nominally identical RS devices has a key impact on the intrinsic device performance. During resistive switching the local temperatures at the filament both during the form/set and in the reset operations can exceed 700^0 C [33] i.e. far higher than the maximum temperature to which the CMOS backend may be usually exposed when the underlying processor is in operation. This temperature is estimated to be around 120° C. At such high temperature the bottom electrode material (BE) can change its crystallinity from amorphous to polycrystalline or crystalline, which can significantly compromise its diffusion barrier property to underlying Si and can lead to start of silicidation which might later cause diffusion barrier failure for Cu. The crystallinity phase of

BE metal also depends on the deposition method and the subsequent 'accidental', i.e. related to the RS switching behavior, local anneals.

Again, electric performance of nominally identical devices depended sensitively on the glue layer. The impact of the glue layer showed up most dramatically in the stability of the filaments formed at low I_{CC} values. The difference in the electric performance is attributed to the difference in the Joules heat generated in the Cu CF during operation of the cell between V_{SET} and end-voltage of the ramp and during the reset operation. Device embedment issue is discussed in detail in chapter 4.

2.4 Reference CBRAM Device: Cu/TaO$_x$/Pt

Cu/TaO$_x$/Pt based devices have proven to be one of the more popular types of CBRAM
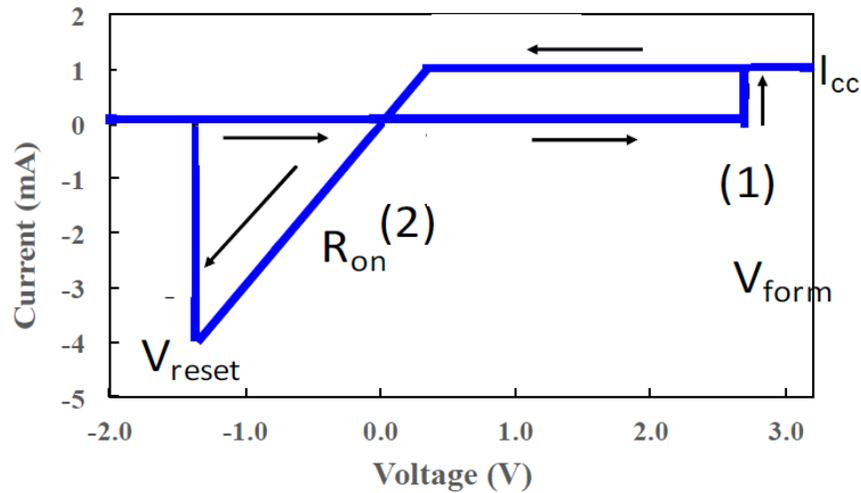
Fig. 2.1: *Standard resistive switching characterization. The quantities being monitored are: R_{OFF}, V_{SET}, R_{ON}, V_{RESET}, and I_{RESET}.*

devices due to numerous reports of excellent unipolar and bipolar switching characteristics, device

performance, retention, reliability, endurance, and yield [34-39]. Commercialization of non-volatile memory products based on RS devices derived from a Cu/TaO$_x$/Pt cell has also been recently reported [40]. Additionally, Cu/TaO$_x$/Pt RS devices offer the potential to co-integrate CMOS logic and RS memory into a single product via fabrication of the devices directly into the Cu metal interconnect wiring.

A single Cu/TaO$_x$/Pt switch relies on electrochemical formation and rupture of a conductive filament (CF) bridging the dielectric between the active Cu and inert Pt electrode. In this measurement, the bottom electrode is grounded, and the bias voltage is applied to the top electrode. When active electrode is supplied with a positive voltage, Cu cations dissolve in the solid electrolyte and electro-migrate through it. As a result, Cu cations are electrochemically reduced on the Pt cathode. As more Cu atoms aggregate at the TaO$_x$/Pt interface, the current will remain substantially zero until a critical voltage V_{SET} is reached (1), at which a nanoscale conductive filament forms a conductive path connecting the Cu and Pt electrodes, and the cell switches from a high resistive state (HRS) characterized by R_{OFF} (1–900 MΩ) to a low resistive state (LRS) characterized by R_{on} (70–6000 Ω), yielding a ratio of $R_{OFF}/R_{ON} \approx 10^3-10^7$. Table 2.2 gives the range of forming voltages, V_{FORM}, and LRS (R_{ON}) of CFs for different Cu/TaO$_x$/Pt devices under I_{CC} = 10 µA and voltage sweep rate rr = 2 V/s. When negative voltage sweep is applied across the device, ohmic behavior is detected until it reaches a negative voltage V_{RESET}. At this point, the CF is ruptured and the current collapses to a very trivial value.

Sweep rate is defined as the rate of change of voltage with time. The devices are stressed with a linear ramp voltage having a natural interval time of 50 µs per step size. The range of V_{FORM} for Pt devices is 4.1 V – 5.2 V. Cu/TaO$_x$/Pt device can be switched between the HRS and LRS

based on the formation and rupture of two types of nanofilaments in the same device: Cu and oxygen vacancy conductive bridges based on the polarity of switching voltage.

It is generally assumed that for low I_{CC} values the Cu CF assumes a truncated cone-shaped filament with a narrow constriction as shown in Fig. 2.2(a). Such filament can be easily ruptured since sufficiently high current will generate a high local temperature close to the tip of the filament which leads to Cu atom out-diffusion there and a formation of a gap in the filament close to the

Table 2.2: Typical forming voltages and on-resistances of Cu/TaOx/Pt devices.

Cu/TaO$_x$/Pt	V_{FORM} (V)	R_{ON} (Ω)
Sample 1	5.2 V	1.40E+04
Sample 2	4.7 V	1.23E+04
Sample 3	4.1 V	1.35E+04
Sample 4	5.1 V	1.58E+04
Sample 5	4.5 V	1.14E+04

Cu interface as shown in Fig. 2.2(a). The maximum temperatures reported [33] are in the range of 700^0 C-900^0 C. For large I_{CC} currents the CF assumes a more cylindrical shape, and the location of maximum temperature moves to a position half way between the two electrodes as seen in Fig. 2.2 (b). Cylinder-shaped CFs are difficult to rupture since the local temperature is significantly lower than in the case of cone-shaped CF and often lead to a permanent un-resettable ON-state. For the subsequent discussion it is important to note that, the local temperature of the conductive filament may be more than 700^0 C when the current (independent of its polarity) flowing through the filament is in the range of mA. When, after the cell is set to the ON-state, the voltage is swept back, ohmic behavior is observed (2) (see Fig. 2.1) until a negative voltage V_{RESET} = -1.4 V is reached when the cell switches abruptly (3) from LRS to HRS state. The rupture of the CF is

triggered by a critical current $I_{RESET} = V_{RESET}/R_{ON}$.

When a negative voltage is applied to the Cu electrode of a RS device in the OFF-state while the Pt electrode is grounded, the formation of a conductive filament can be observed and has been ascribed to oxygen vacancies (V_o). In general, $V_{FORM}(V_o)$ is larger than $V_{FORM}(Cu)$ for Cu CF. Under negative bias voltages, the migration of Cu^+ ions in electrolyte is suppressed. Therefore,

(a)   (b)
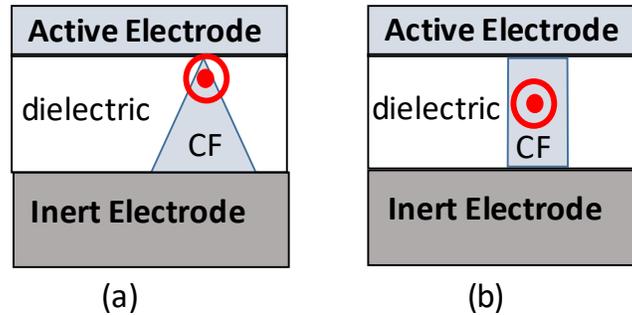
Fig. 2.2: Two cases of geometric shapes of a conductive filament (CF). The concentric red circles indicate the position of the maximum temperature at high cell currents. The location of maximum temperature is indicative of the location of the gap in the ruptured filament. (a) a cone-shaped filament with distinct constriction at the apex usually formed at lower I_{CC} values and characterized by high ON-resistance, R_{ON} and easy to rupture. (b) a cylindrically shaped filament formed usually at higher I_{CC} currents with low R_{ON} and difficult, if not, impossible to rupture.

the Cu filament cannot form a conductive path between electrodes. The filament is attributed to an oxygen vacancy filament according to following reactions. First, electro-reduction reaction (1) occurs at the $Cu-TaO_x$ interface:

$$Cu \longleftrightarrow Cu^+ + e\text{- (Reduction-Oxidation)} \qquad (1)$$
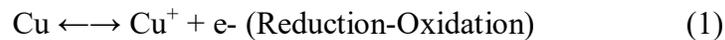
Under negative bias to the Cu electrode reaction (1) provides electrons which at negative bias will be injected into the dielectric while the positive Cu^+ ions will be returned to the Cu

electrode. The injected electrons may charge and dislodge the negative oxygen ion from the metal oxide matrix leaving behind a neutral oxygen vacancy V_o according to the reaction:

$$TaO_x + 2e^- \rightarrow TaO_{x-1} + O^{2-} = TaO_xV_o + O^{2-} \qquad (2)$$

Vacancies (V_o) created this way lead to formation of oxygen vacancy filaments which are discussed in more detail elsewhere [41]. In summary, although $Cu/TaO_x/Pt$ device shows very promising resistive switching behavior and uses Cu as the active electrode rendering it compatible with modern back-end metallization, its use of Pt eliminates it from realistic deployment in CMOS technology.

2.4.1   Device Fabrication

$Cu/TaO_x/Pt$ resistive device has been fabricated in a crossbar array on a thermally oxidized

(a)   (b)
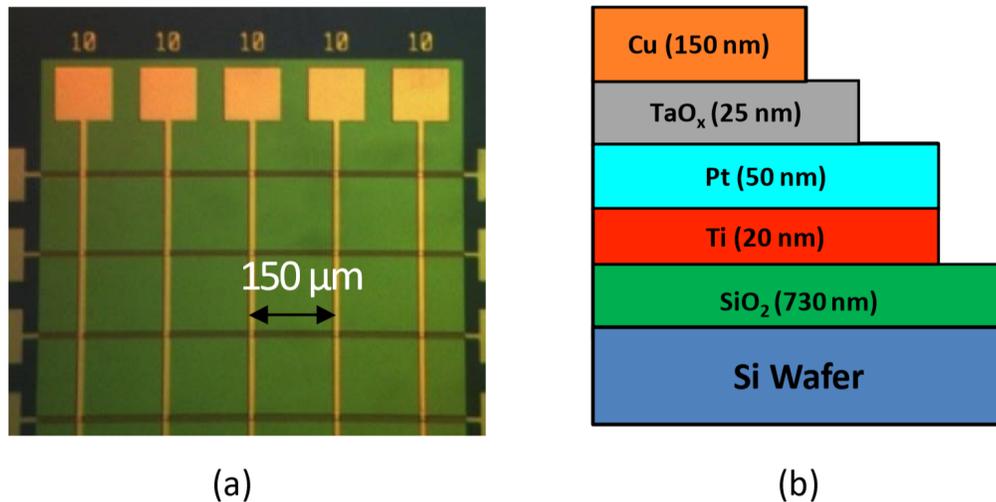
Fig. 2.3: *a) Optical micrograph of the crossbar architecture; b) Device cross-section of Cu/TaOₓ/Pt resistive switching device.*

Si wafer. The metal electrodes and solid electrolyte were deposited by e-beam evaporation and

patterned by the liftoff technology. The oxygen-deficient tantalum oxide TaO_x layer was deposited by evaporating the Ta_2O_5 pellets without oxygen injection into the evaporation chamber. Deposition of sub-stoichiometric Ta_2O_x ($x < 5$) layer is a critical process in order to produce the required oxygen vacancies in these RS devices [42]. A thin Ti layer was deposited between Pt and SiO_2 to improve the adhesion. Fig. 2.3(a) shows the optical micrograph of the crossbar architecture of resistive $Cu/TaO_x/Pt$ device. The Cu top electrodes run perpendicularly to the Pt bottom electrodes and one resistive switch cell locates at each cross point since it has a blanket layer of dielectric in between. The width of the metal lines varies from 5 μm to 25 μm. Fig. 2.3(b) shows the cross-section view of $Cu/TaO_x/Pt$ resistive switching devices with layer thickness specified. All four layers (Cu, TaO_x, Pt, Ti) have been deposited by e-beam PVD in a Kurt Lesker PVD-250 chamber, with the thicknesses 150 nm, 25 nm, 50 nm and 20 nm respectively.

2.4.2   Characterization Methodology

All devices have been subjected to the standard resistive switching characterization as shown in Fig. 2.1. The voltage is being ramped with a ramp rate rr starting at 0 V on the positive (or negative) bias axis while the current is being monitored. At a critical voltage V_{SET}, the current increases very rapidly indicating that the device became highly conductive. Usually, lest the device be damaged, a compliance current I_{CC} is applied to limit the current flowing through the device. The level of I_{CC} determines in many instances the nature of the filament and the value of the on-state resistance, R_{ON}. When the voltage is being ramped down, the device displays an ohmic behavior of the on-state and characterized by R_{ON}. When the current at negative bias reaches a critical current I_{RESET} at V_{RESET}, the conductive state is ruptured, and the device reverts to the off-state characterized by a high resistance, called off-state resistance, R_{OFF}.

2.4.3   Switching Characteristics of Cu/TaO$_x$/Pt Device

I-V characteristics of resistive Cu/TaO$_x$/Pt devices were measured by a Keithley 4200-SCS (Semiconductor Characterization System). A characteristic I-V switching cycle of the Pt device is shown in Fig. 2.4. When the cell is set to an ON-state for the very first time, one speaks of forming operation, characterized by the forming voltage, V$_{FORM}$. The V$_{FORM}$ is always larger than V$_{SET}$,
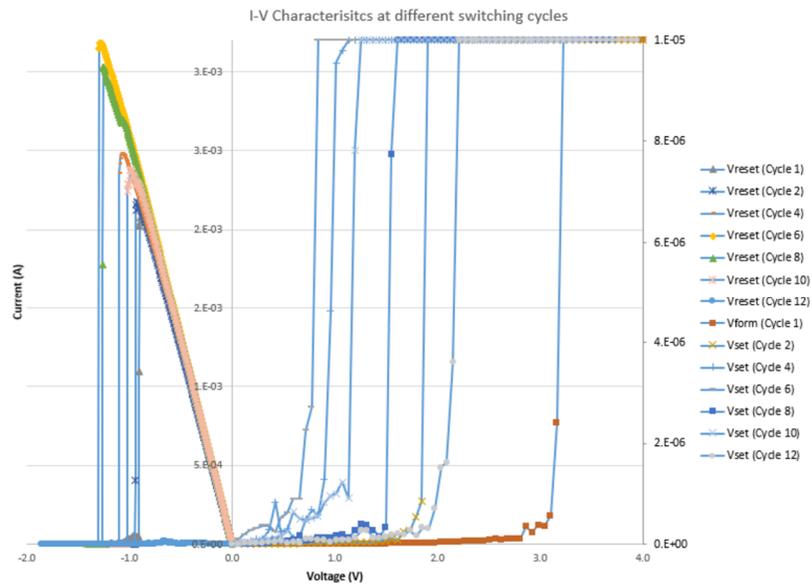
Fig. 2.4: *Even cycles of a typical first 12 set and reset switching cycles of a Cu/TaO$_X$/Pt device. Note the different vertical current linear scales for set and reset operation.*

since the Cu filament has to be formed in its entirety and not partially whereas fraction of the filament has been merely ruptured but not totally undone for the subsequent set operations. For Cu/TaO$_x$/Pt devices, it was found that V$_{FORM}$ distribution with a mean V$_{FORM, m}$=4.6 V and a standard deviation of σ=0.6 V, the V$_{SET}$ distribution with a mean, V$_{SET, m}$=2.8 V, and standard deviation, σ=0.78 V. The rupture of the CF is triggered mainly by Joules heating at a critical

current $I_{RESET} = V_{RESET}/R_{ON}$. The V_{RESET} distribution of the Cu/TaO$_x$/Pt devices is characterized by $V_{RESET, m}$=-0.9 V and σ=0.5 V.

In most instances, a compliance current I_{CC} is imposed, lest the devices be damaged during the set operation. No I_{CC} current limitation is applied during the reset operation. R_{on} of the LRS state depends on I_{CC} via the relation (3), where the exponent n for cation filaments is very close to unity.

$$Ron = \frac{A}{I_{cc}{}^n} \tag{3}$$

The R_{on}–I_{CC} relation in eq. (3) has been reported to be valid for numerous
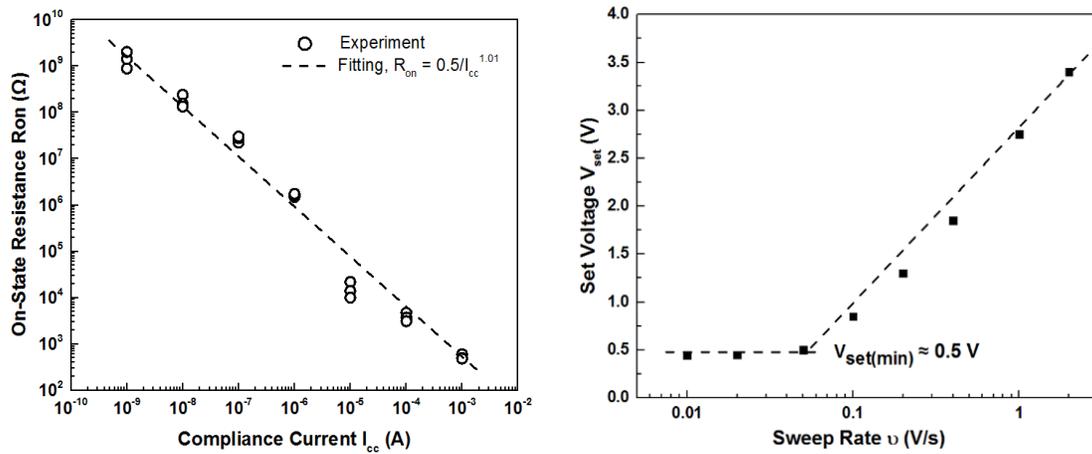
Fig. 2.5: (a) Dependence of on-resistance Ron on compliance current Icc for Cu/TaOx/Pt device @ rr =0.2 V/s; (b) Dependence of SET voltage on voltage sweep rate for the Cu/TaOx/Pt device (Ron @ Icc = 100 μA).

anode/electrolyte/cathode material systems [43-50] with n≈1. In [50] it has been shown that the constant A in eq'n (3) is universally correlated to the minimum SET voltage for all metallic conductive filaments reported so far. It is known [51] that the compliance current enforced externally by Keithley 4200-SCS leads to a transient overshoot current especially during the very fast last phase of filament formation, as Keithley circuitry is unable to respond instantly to large

current changes. In this work, where different devices are compared with one another, the effect of current overshoot should be the same for all devices, and thus the relative comparisons should still be valid.

From the R_{ON} vs I_{CC} plot shown in Fig. 2.5(a), the constant A=0.5 V and the exponent n = 1.01 are obtained by curve fitting. Here, the voltage sweep rate rr = 0.2 V/s has been used for the set operation. In Fig. 2.5(b) V_{SET} is plotted as a function of the sweep rate. It is seen that the minimum V_{SET} at low sweep rates corresponds to the constant A as predicted by the theory [50]. The slope of the plot was found out to be the minimum possible value of SET voltage. Fig. 2.6(a) shows the dependence of the forming voltage and on-resistance on three different voltage sweep rates of 0.1 V/s, 0.2 V/s and 2V/s. It can be seen that not only does the forming voltage increase
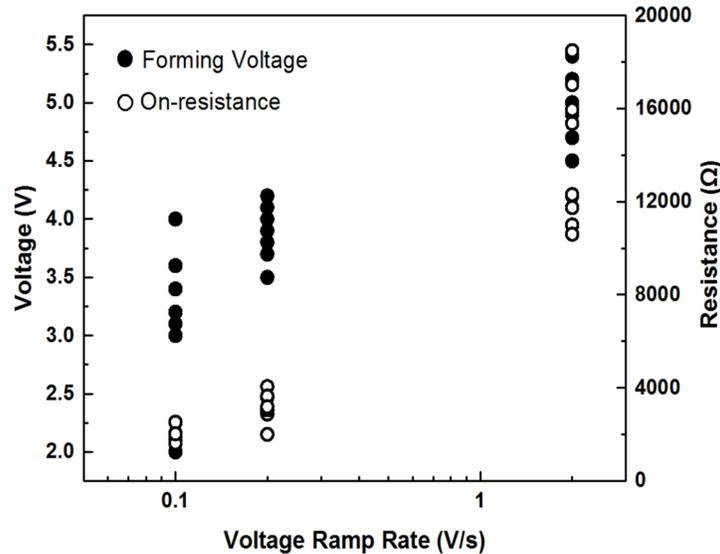
Fig. 2.6: Dependence of forming voltage V_{FORM} and on-resistance R_{ON} on voltage sweep rate @ I_{CC} = 100 μA.

with increasing ramp rate, but also the on-resistance increases with increasing ramp rate. The dispersion of R_{ON} is significantly higher at high ramp rate compared to the one at low ramp rate.

111

According to eq'n (3) R_{ON} can be tuned by imposing different levels of the compliance current I_{CC} and voltage sweep rate. When the voltage sweep rate increases from 0.2 V/s to 2V/s, the constant A value of relation (3) increases from 0.5 V to 1.01 V.

Fig. 2.7 depicts the dependence of R_{ON} on voltage sweep rate under different levels of compliance current (5µA, 100µA and 1mA). The range of voltage ramp rate is 0.1 V/s to 2 V/s. It can be seen that R_{ON} is larger at lower I_{CC}, in agreement with eq'n (3). Under low compliance current (5µA and 100µA), R_{ON} increases with increasing voltage sweep rate. However, in the case of high compliance current, R_{ON} becomes independent with voltage ramp rate, indicating ohmic behavior of a robust and stable conductive filament.

Since filament rupturing is chiefly a thermal phenomenon, the heat conductivity of the inert
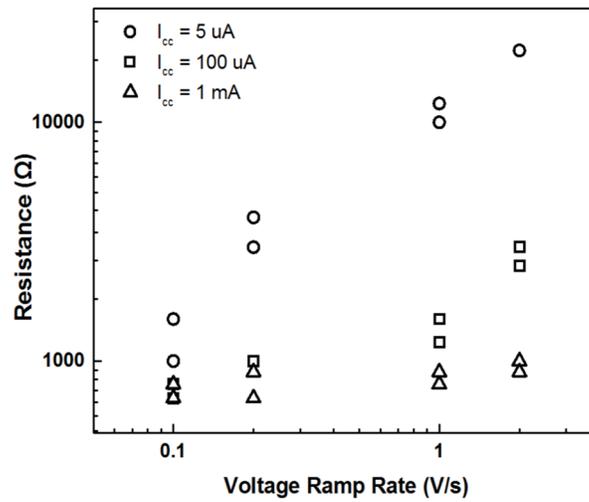
Fig. 2.7*: Dependence of on-resistance R_{ON} on voltage sweep rate rr @ I_{CC} = 5 µA, 100 µA and 1mA.*

electrode plays a significant role in determining the maximum temperature of the filament.

During the heating of a resistive cell A, the reset operation results in rupturing of the CF at a reset current $I_{RESET}=V_{RESET}/R_{ON}$ of typically a few of mA. Hence, most of the Joules heat Q_{JH} is deposited according to eq'n (4)

$$Q_{JH} = \int_0^{t_{res}} \frac{V^2(t)}{R_{on}} \, dt \ = \int_0^{(V_{res}/rr)} \frac{rr^2 * t^2}{R_{on}} dt \ = \ \frac{V_{res}^3 * I_{cc}}{3 * rr * A} \ dt \qquad (4)$$

where V_{RES} is the reset voltage, $t_{RESET} = V_{RESET}/rr$ is the reset time, the low reset ramp rate rr=0.1V/s is to maximize the heating during the reset [52, 53]. Depending on chosen values for I_{CC} and rr, Q_{JH} can be varied from 3 to 60 µJ.

With respect to the geometrical shape of the filament, the cells with large R_{ON} are associated with a truncated cone with a sharp constriction of the top (see Fig. 2.8(a)), where the bulk of the R_{ON} resistance is concentrated at the tip of the cone. Filaments with a sharp constriction
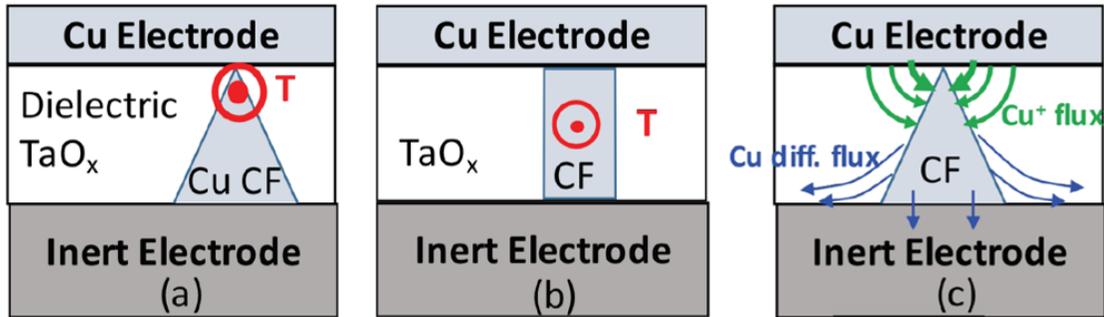
Fig. 2.8: *(a) location of the highest temperature due to the Joules heating during reset operation. (b) cylinder-like shape of the filament with maximum temperature in midway between the electrodes. (c) Cu conductive filament with a sharp constriction at the Cu electrode interface with Cu constructive (Cu⁺ ion electromigration) and destructive (Cu out-diffusion) fluxes responsible for the shape of the CF.*

at the top of the cone are easy to rupture since the maximum Joules heating is deposited at the tip and leads there to a high local temperature which, in turn, leads to Cu out diffusion and formation of a gap in the filament which completes the rupture of the filament and restores the HRS state. In contrast, the shape of Cu filament with a small R_{ON} approaches that of a cylinder (Fig. 2.8(b)) and the temperature hot spot moves to the center (i.e. midway between the electrode interfaces) of the filament where it is much more difficult to reach high temperature and cause out-diffusion of a

larger number of Cu atoms to form a gap. Experimentally, it is found consistently that filament rupturing is more difficult with decreasing R_{ON} resistance.

In the set operation there are two fluxes responsible for the formation of the filament as shown in Fig. 2.8(c). At the tip of the filament there is a large voltage drop which creates high electric field between the filament tip and the Cu electrode, which allows for further transport of Cu^+ ions from the Cu electrode to the filament even after establishing the initial connection between the Cu filament and the Cu electrode. The role of I_{CC} is to limit the resulting voltage drop and thus set a limit on the electric field driving the Cu^+ ion transport. When sufficient number of Cu atoms are deposited at the tip, the resistance of the filament sinks, reducing the electric field at the tip and bringing the formation of the filament to a halt at a given I_{CC}. When I_{CC} is increased, then the electric field at the tip increases proportionally triggering additional arrival of Cu^+ ions until the resistance of the filament drops sufficiently to reduce the electric field and thus to halt further Cu^+ ion transport. The second flux is the Cu atom diffusion flux weakening the base of the filament and leads to an increased R_{ON} resistance. The diffusion effect can be gradual in so far as any weakening of the filament leads to increased R_{ON} resistance which, in turn, may trigger the compensating Cu^+ electromigration flux.

The Cu diffusion flux is impacted by the thermal conductivity of the inert electrode. For the otherwise same conditions, the inert electrode with high heat conductivity will be able to remove the heat at a higher rate than an electrode with low heat conductivity. The larger heat removal rate will result in lower attainable maximum temperature. Hence, a cell with inert electrode of low heat conductivity is bound to display enhanced Cu diffusion. The high temperature in the filament during the reset will trigger Cu diffusion near the base of the filament partly into the dielectric, partly along the TaO_x/inert electrode interface, and partly into the inert

114

electrode if the inertness of the electrode is not perfect. The overall result of those diffusion components is the weakening of the base of the cone and a transformation of the shape of the filament from a sharply cone-shaped into a more cylinder-shape filament as shown in Fig. 2.8(b). Once the shape of the filament is sufficiently close to a cylinder-like shape the respective filament will be very difficult to be ruptured and the number of switching cycles comes to a halt.

Fig. 2.9 illustrates the SET voltage's dependence on ambient temperature and the RESET voltage's near independence on the ambient temperature. V_{SET} and V_{RESET} of five different cells are plotted when the ambient temperature is 20 °C, subsequently increases to 85 °C and reduces back to 20 °C. It can be seen that the SET voltage at 85 °C is reduced by ~ 0.8V compared with
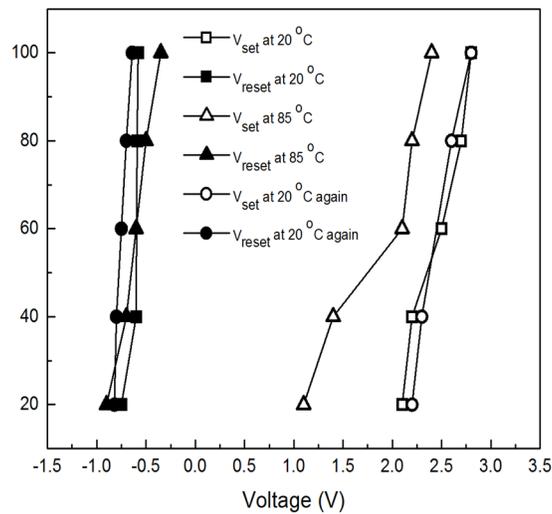
Fig. 2.9: *Dependence of set voltage V_{SET} and reset voltage V_{RESET} on ambient temperature of 20 °C and 85 °C.*

the set voltages at room temperature. The reduction of V_{SET} with increasing temperature can be explained by three different mechanisms in TaO_x. (1) The ionization rate of Cu, the rate for Cu ionizes to Cu ion ($Cu \rightarrow Cu^+ + e^-$), increases with increasing temperature. (2) The mobility of Cu ions in TaO_x increases with increasing temperature. (3) The nucleation of Cu ions or the speed of

115

forming the cluster of Cu at the interface of Pt electrode may also accelerate with increasing temperature, as all of those reactions are governed by Arrhenius law. It is found that the RESET voltage is independent of temperature. The local temperature leading to rupturing of the filament has been reported [54] to be around 900^0 C and therefore slight change of ambient temperature has little impact on the high local temperature responsible for the partial dissolution of the filament.

The metallic Cu filaments are well characterized by their temperature coefficient of resistance (TCR). For Cu filaments with R_{ON}=1 kΩ, the TCR(Cu)=0.003 K^{-1} (which is close to the TCR of bulk Cu of 0.0039 K^{-1}. In Fig. 2.10 (a) and (b) the TCR measurement for a fragile filament (R_{ON}=11.2 KΩ) formed at I_{CC}=10 μA and for a robust filament (R_{ON}=250 Ω) formed at I_{CC}=10
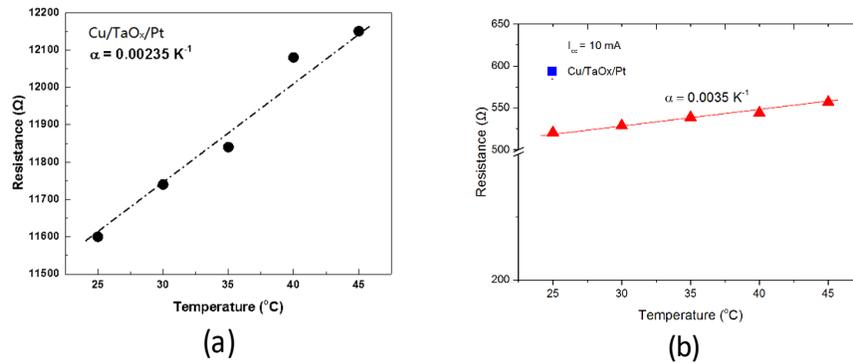
Fig. 2.10: On-resistance, R_{ON}, of the Cu filament of Cu/TaOx/Pt and Cu/TaOx/Ru for set operation at different I_{CC} levels: (a) Cu CF for Pt devices @ I_{CC} = 10 μA; (b) Cu CF for Ru devices @ I_{CC} = 10 μA; (c) Cu CF for Pt and Ru devices @ I_{CC} = 10 mA.

mA. For a fragile Cu filament, the TCR=0.00235K^{-1} and for the robust filament TCR=0.00362 K^{-1}. The Cu bulk values have been verified on the Cu lines with following dimensions: thickness 150 nm, width 1 μm – 35 μm, and length 150 μm. The measurement of the TCR of the copper lines yielded consistently TCR values of 0.0388 K^{-1} - 0.00396 K^{-1}, in good agreement with the TCR value of the TCR for bulk Cu of 0.0039 K^{-1}. This is in agreement with a study of the electric properties of free-standing Cu nanowires reported in [55]. Y. Zhao et al [55] reported that TCR for

Cu nanowires decreases with decreasing of the diameter: at 230 nm TCR=0.0038 K^{-1}, at 100 nm TCR=0.0033 K^{-1} and at 50 nm TCR=0.0028K^{-1}. Also A. Bid et al [56] reported TCR values between 0.004 K^{-1} and 0.0025 K^{-1} for Cu nanowires with diameters between 200 nm and 15 nm respectively. The metallic nature of the filament has also been deduced by Xiao et al [57] using ab initio atomic calculations attributed the main contribution to the conductive path is from Cu-Cu metallic bonds. As seen from Fig. 2.10 the TCR increases with decreasing R_{ON} resistance.

2.4.4 Cu Filament Geometry in Cu/TaOx/Pt

The Cu filament for Pt device has been assumed to have a shape of a truncated cone see Fig. 2.11(a), with the top radius, a, much smaller than the bottom radius, b. For low I_{CC} a $\ll$ b, but for high I_{CC} b $\approx$ a, and the truncated cone becomes a cylinder. The shape of the filament for various

$$R_{on} = \frac{\rho \cdot h}{\pi \cdot a \cdot b}$$
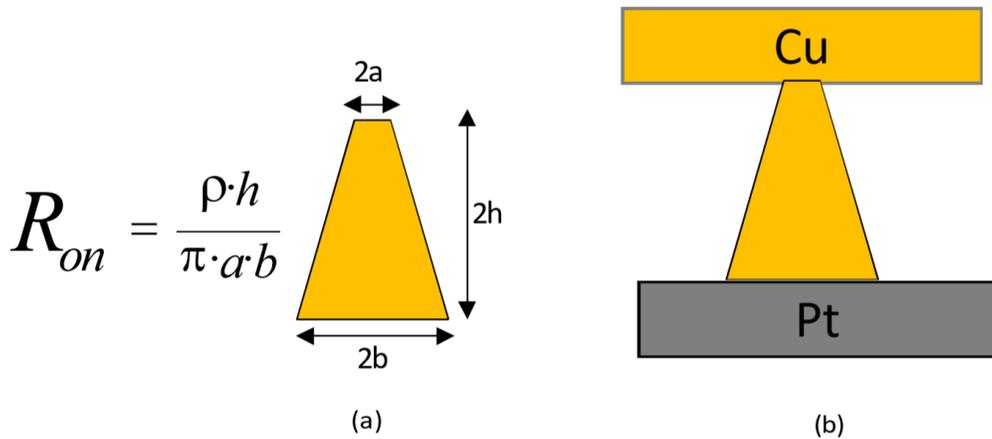
Fig. 2.11: *a) Geometric model of a truncated cone for conductive filament with the formula for on-state resistance, R_{ON}; b) Hypothesized geometrical shape of Cu conductive filament structures for Cu/TaOx/Pt device*

ReRAM memory devices are discussed in detail in section 2.4.5. For a sharply truncated cone the bulk majority of the resistance resides in the tip of the cone. This is also the locus of the Joules heat deposition according to $\int_0^{V_{reset}/rr} \frac{rr^2 \times t^2}{R_{on}} dt$ [58]. Therefore, during the reset operation the tip of the cone becomes hot causing the diffusion of Cu atoms and thus rupturing the filament. Based on equation given in Fig. 2.11(a), Cu filaments for the Pt device was constructed as: b_{Pt} = 3 nm and a_{Pt} = 0.5nm of the Cu CF in Pt devices. The length of Cu CF h, which is also thickness of solid electrolyte, is 25 nm. The resistivity of copper filament is assumed to be 300×10^{-6} $\Omega \cdot$ cm [33]. Based on equation in Fig. 2.11(a), the resistance of Cu CFs for Pt device is 15,923 Ω, which is almost the same values shown in Table 2.2. However, a cylindrically shaped Cu filament is much more difficult to rupture and therefore causes a significantly degraded number of switching of cycles. Ru devices demonstrate a more cylindrical filament shape and is discussed in detail in chapter 4.

2.4.5 Conductive Filament Geometry in ReRAM Device

The filament growth mechanism usually involves the following three dynamic processes:

i.   dissolution of active electrode metal at the top electrode/dielectric interface

ii. electromigration of the generated cations (metal ions) through the dielectric

iii. reduction of the transported cations and recrystallization of filaments

The electromigration of cation occurs within the dielectric layer and is dependent on the properties of the dielectric material. There have been numerous investigations to explore the growth dynamics and shape of the conductive filament in ReRAM device through numerous techniques such as in-situ or ex-situ Transmission Electron Microscopy (TEM), TEM imaging, morphological

and compositional analysis of filaments, Scanning Electron Microscopy (SEM), Scanning Transmission Electron Microscopy (STEM), Scanning Probe Microscopy based 3D probing etc. [59-67]. Through TEM image analysis of an already formed filament, the filament geometry has been confirmed as conical or nearly cylindrical shape and the dimension ranging from 5-20 nm near the filament tip (narrowest region) and 30-70 nm at the base of the filament (widest region of the filament) depending on the applied compliance current [59]. Energy-Dispersive X-ray Spectroscopy (EDX) confirms the filament is of metallic in nature and consists of atoms from active electrode metal [59, 60]. This is consistent with ECM theory [68]. During filament formation usually one dominant filament is formed. There are also many incomplete filaments exist in the electrolyte which can form dendrite like structure with branches. For relatively thicker solid electrolyte layer, the dominant filaments are found to be more like dendrite structure instead of well-known cone-shaped filaments and the branches point towards the active electrode. The presence of single complete filament supports the well accepted hypothesis of self-limiting mechanism of filament formation. Once a filament growth process is completed electrodes are shorted by the filament, the electric field between active and inert electrode drops and hence any further filament growth process is suppressed [69]. The formation and dissolution of filament occurs at the thinnest region of the filament where the filament resistance is highest. Therefore, the filament geometry as well as the electrolyte/electrode interface at the thinnest region of the filament is very crucial for reliable programming and erasing of ReRAM cells. After rupturing the filament during RESET operation, only a small portion of the filament is dissolved, and substantial amount of filament materials are still preserved in the solid electrolyte layer which facilitates restoration of the complete filament during subsequent SET operation. This is confirmed by TEM image analysis and is consistent with $V_{SET} < V_{FORMING}$. [59]. Therefore, the device resistance at the

OFF state never reaches the initial device resistance, meaning that the initial R_{OFF} is larger than the subsequent R_{OFF}. The residual metallic filaments lead to OFF-state leakage current and the magnitude of this leakage current increases with the switching cycle. This will deteriorate the
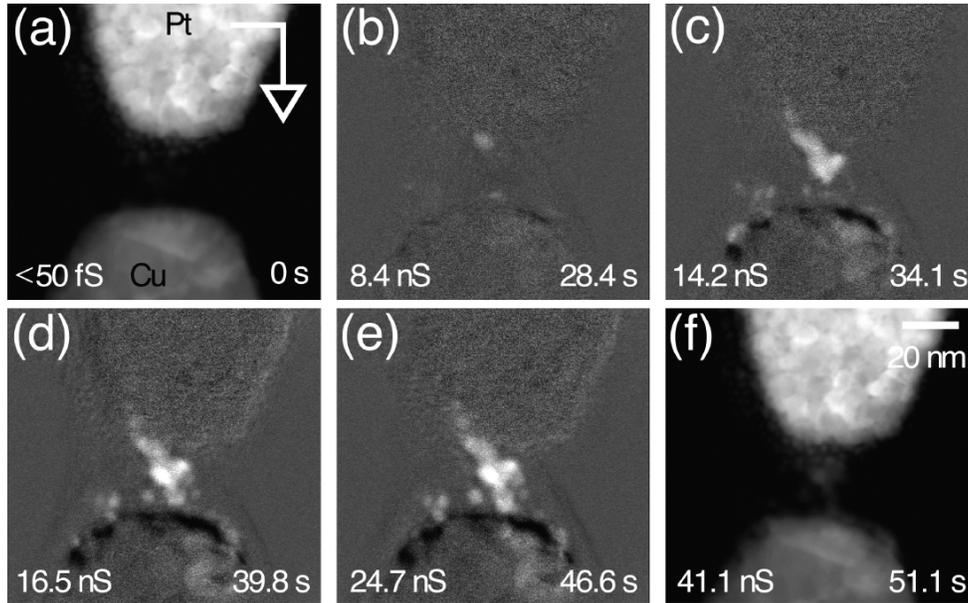
Fig. 2.12: STEM image of Inverted-cone shaped filament growth a) before and; (b-f) after filament formation in Cu/Al₂O₃/Pt device. Reprinted with permission from [71], Copyright American Chemical Society (2015)

device reliability over the operation time of ReRAM cell [70].

In general, depending on the kinetics the conductive filament growth modes can be categorized into four different regimes [65]: -

  i.   both ion mobility and redox rates are high

  ii. ion mobility is high, but redox rates are low

  iii. ion mobility is low, but redox rates are high

  iv. both ion mobility and redox rate are low

When the cation mobility is very high, majority of ions can successfully electromigrate across the dielectric layer very quickly and will reach the inert electrode. In this case the probability of cations agglomeration or nucleation within the dielectric layer is very low. Again, the high oxidation-reduction rate will ensure that the rate of cation dissolve rate at top electrode/dielectric interface as well as cation reduction rate at dielectric/inert-electrode interface is very high. So large supply of cations reaching the inert electrode will be reduced there and the filament will grow from inert electrode towards the active electrode (top electrode) [65]. This will result an inverted-cone shaped conductive filament [72, 73] where the wider base of the filament is at the inert electrode
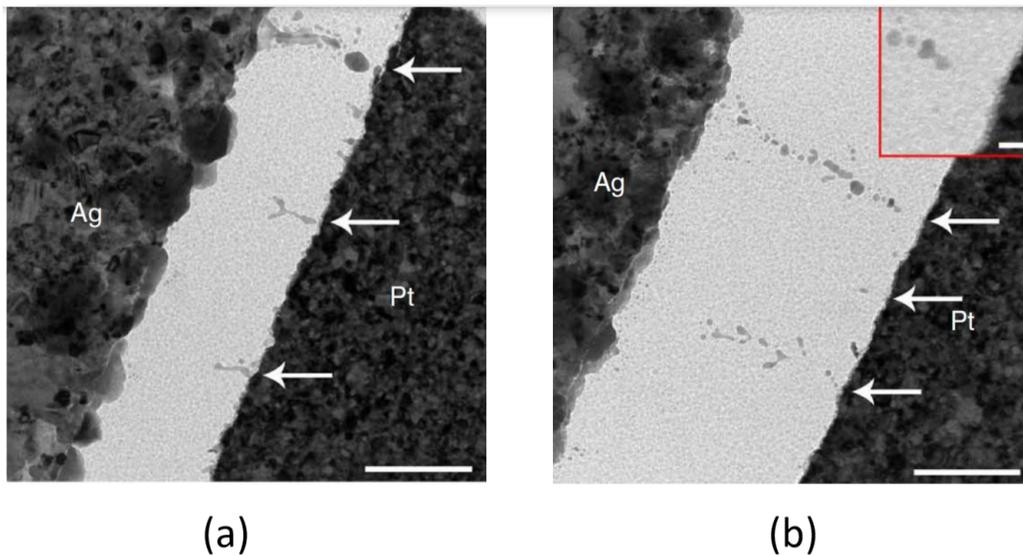
Fig. 2.13: *TEM image of Ag/SiO2/Pt device after: (a) FORMING and (b) RESET operation.* Reprinted with permission from [59], copyright Nature Communications (2012)

[61] etc. Figure 2.12 shows the SEM image of inverted-cone shaped filament growth before and after filament formation for $Cu/Al_2O_3/Pt$ device [61]. Chalcogenides material such as GeS_x, $GeSe_x$ etc. usually shows this reverse-cone shaped filament [71,76].

121

In the case when ion mobility is high, but redox rates are low the rate-limiting factor is the reduction or crystallization process since the cation supply is limited. But the highly mobile cations will reach inert electrode and nucleate. But due to limited supply of cations the reduction of cations primarily occurs at the edges where the electric field is maximum. As a result, branched shaped conductive filament pointing towards active electrode is formed [59, 65]. Limited cation supply is the pre-requisite for this dendrite shaped filament which is also seen for devices with thicker dielectric layer [59]. Figure 2.13 shows the dendrite-shaped filament for Ag/SiO_2/Pt device during FORMING (a) and RESET (b) operation where high defect density of SiO_2 dielectric leads to high

(a)   (b)
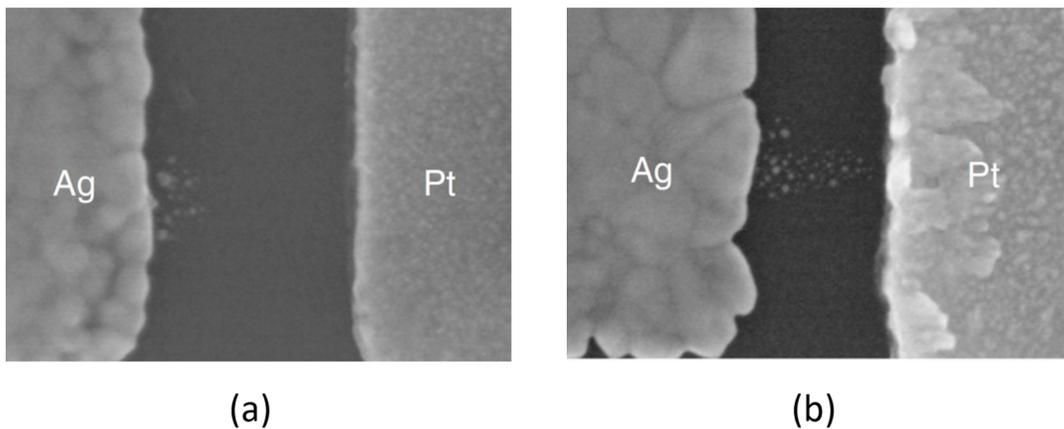
Fig. 2.14: *SEM image of filament formation in Ag/a-Si/Pt device with different programming current by applying voltage: (a) 22V; (b) 26V.* Reprinted with permission from [59], copyright Nature Communications (2012)

mobility of cations.

If the material system has low cation mobility but high redox rate, there is large number of nucleation within the dielectric and this cause a gap between the nuclei and active electrode. After some time, the nuclei and active electrode are connected, and the filament growth continues until they reach inert electrode [65].

122

When both ion mobility and redox rate are low, the cations move very slowly within the dielectric and the rate limiting process is the cation electromigration rate. As a result, the cations can be reduced within the dielectric nearer to the active electrode by seizing electrons injected from the inert electrode. Considering the electroneutrality condition, there will be large number of
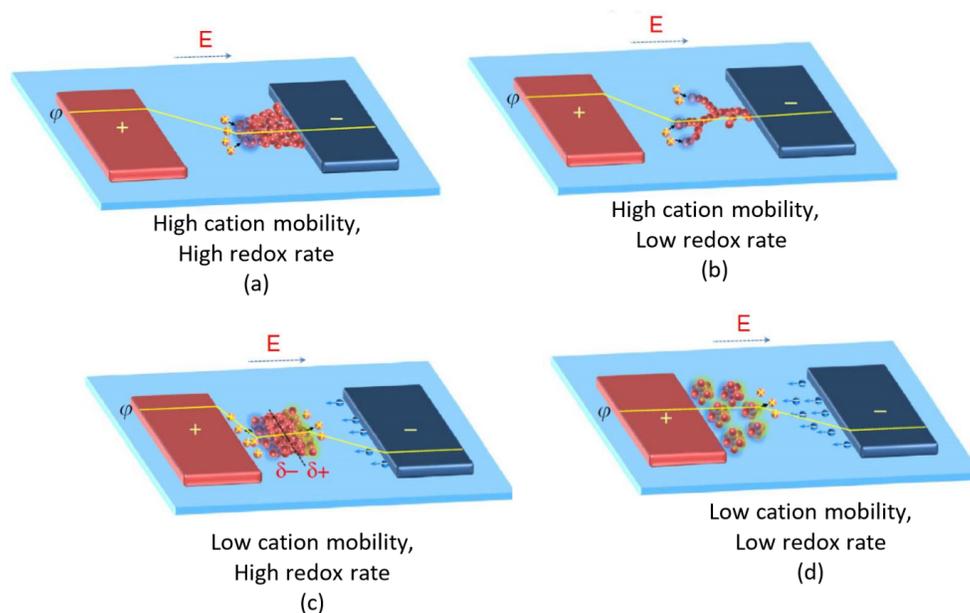
Fig. 2.15: *Kinetics of conductive filament growth when: (a) both cation mobility and redox rates are high; (b) cations mobility is high, but redox rates are low; (c) ion mobility is low, but redox rates are high; (d) both ion mobility and redox rates are low.* Reprinted with permission from [65], Copyright Nature Communications (2014)

electrons injected from the cathode and the probability of cation reduction or chance of reduction through nucleation within the dielectric after satisfying nucleation conditions before reaching the inert electrode by this process is very high. The reduced cations can then continue to pile and form clusters. Later the cluster can split and move further and then again merge later. This process of split and merge can continue to repeat until the filament reaches the inert electrode and creates

a conically-shaped filament [65]. In this case the filament starts at active electrode and gradually grows towards the inert electrode and the material system has very low conductivity of cations. Figure 2.14 shows SEM image of filament formation in Ag/a-Si/Pt device with different programming current.

In summary, the cation mobility and dielectric layer defect density regulates the electromigration rate in the dielectric and determines the direction along which the filament will grow. The redox reaction rate on the other hand regulates cation generation and supply rate as well

(a)   (b)   (c)
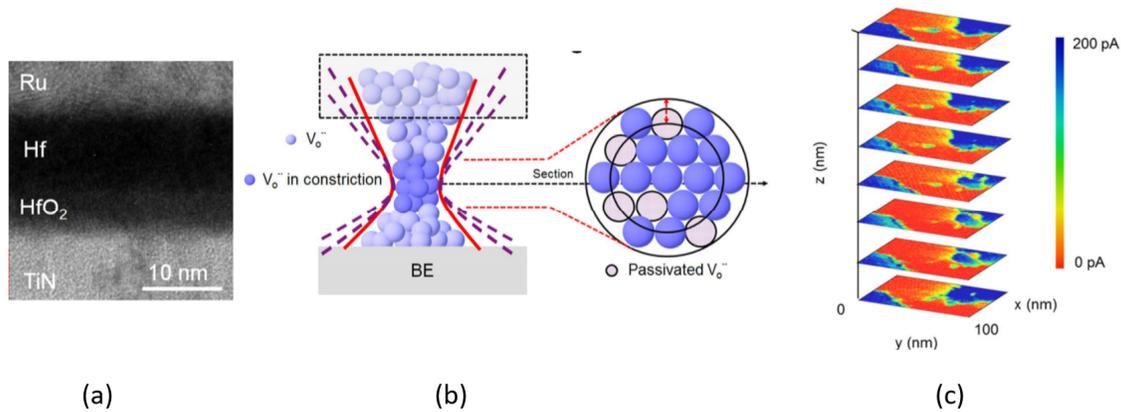
Fig. 2.16: *(a) HR TEM image of device cross-section; (b) schematic of conductive filament; (c) stacked layer in C-AFM tomography.* Reprinted with permission from [77], Copyright American Chemical Society (2015)

as the geometrical shape of the conductive filament. Figure 2.15 schematically shows the filament formation for all these four conditions discussed above.

Umberto et al. conducted high resolution conductive AFM microscopy (C-AFM) on Ru-Hf/HfO$_2$/TiN bilayer structure and through controllably removing materials demonstrated 2D conductivity mapping at various heights for oxide conductive filament [77]. Figure 2.16 (a), (b) and (c) shows HR TEM image of device cross-section, schematic of 3D conductive filament and

stacked layer in C-AFM tomography respectively. The filament is demonstrated to be of hourglass shape. In this device structure, Ru is used for electrical contact and Hf provides vacancy as HfO_2 cannot provide enough concentration of vacancy (V_o).

2.5   Investigated Materials for ReRAM Bottom electrode

The elemental metals investigated in this work for potential bottom electrodes are Ta, Os, W, Ir, Rh, Co, Ru with Pt for the benchmark device. Close-by elements in the periodic table with identical group or period locations usually have comparable electronic configuration with analogous physical and chemical characteristics. The periodic table locations of all the investigated materials are shown in Fig. 2.17.

Fig. 2.17: Potential bottom electrode materials investigated in this work [78]

Several key properties of these elements which potentially can affect the performance in resistive switching operation are also summarized in Fig. 2.18. All the eight elements listed here have

negligible solubility with Cu even at 700^0 C. So, the metal ions (Cu^+ ions) arriving at the bottom electrode is stopped, agglomerate and can continue building metallic dendrite and form conductive filament. The desirable high ionization energy of those elements precludes any potential reaction with the solid electrolyte as well as prevents any redox reactions. The low surface diffusivity

Metal	Pt	Ta	OS	W	Ir	Rh	Co	Ru
Melting Point (°C)	1768	3017	3033	3422	2446	1964	1495	2334
Boiling Point (°C)	3825	5458	5012	5555	4428	3695	2870	4150
Ionization Energy (eV)	8.96	7.55	8.44	7.87	8.97	7.46	7.88	7.36
Work Function (eV)	6.35	4.22	4.83	4.55	5.6	4.98	5	4.8
Bulk Resistivity (10^{-8} Ω.m)	10.6	13.5	8.12	5.6	4.7	4.38	5.6	7.1
Surface Energy (eV)	0.98	0.86	1.6	1.71	1.36	1.09	0.94	1.28
Cost ($/gm)	50	2.8	14.3	1.2	25	29.60	0.21	1.3
Availability	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes
Solubility with Cu till 700^0 C	Trivial	Trivial	Trivial	Trivial	Trivial	Trivial	Trivial	Trivial

☐ Unsuitable   ☐ May affect performance

Fig. 2.18: Crucial material parameters for potential bottom electrodes to obtain superior ReRAM device performance [79-84]

ensures that the top electrode metals after reaching the bottom electrode would not move too far away to weaken the filament base. As a result, the formation of cylindrical geometry shaped filament is avoided (which are difficult to rupture) and the device can be operated with lower voltages (lower $V_{FORMING}$ and V_{SET}). Pt is expensive ($50/gm), incompatible with CMOS and therefore, is only considered as benchmark device for comparison of device performances. Elements like Ta, OS and W have very high melting point and is not ideal for e-Beam evaporation

with good quality thin film. Therefore, devices with bottom electrode consists of Ir, Rh, Co, Ru are investigated in this work.

2.6   Instability of High Resistance Conductive filaments in ReRAM cells During the READ Operation

The mechanism of resistive switching random access memory (ReRAM) has been attributed to formation and rupture of conductive filaments assumed to consist of metal precipitates such as (Cu, Ag, Ni) or oxygen vacancies in metal oxides such as TaO_x [85]. In these filamentary ReRAM memory cells, the resistance of the on-state, R_{ON}, is determined by the limiting current, often called compliance current, I_{CC}, by the relation $R_{ON} \sim A/I_{CC}^n$ [64], where A is a constant and the exponent n in many ReRAM cells is close to unity. Because the on-resistance, R_{ON}, of the conductive filament (CF) is determined by the level of the applied compliance current, a realization of a multi bit memory cell appears feasible. Also because of low power requirements for memory array operation the level of the compliance current, I_{CC}, equivalent to the height and width of the voltage pulse in commercial memory operation, should be as low as practicable. However, interestingly it was found that at low I_{CC} (< 50 µA), the resulting R_{ON} is operationally undefined. This means that the actual value of R_{ON} depends sensitively on the details of the reading operation itself. The R_{ON} can increase or decrease depending on the read voltage polarity, the read voltage starting point and the read voltage ramp rate. In contrast, a set operation performed at a high I_{CC} levels leads to a stable R_{ON} with low resistance independent of the reading conditions. However, the filament formed at low I_{CC}, is very fragile and subject to reconstruction during the read operation. Therefore, the read operation does not merely "read" the actual R_{ON} value, but acts as

another modifying set operation, substantially changing the R_{ON} value and would/could lead to erroneous R_{ON} readings. Those changes in R_{ON} values provide a good insight into microscopic ionic mechanisms responsible for the resistance changes and reaction as well as transport times involved.

2.6.1 Device Manufacturing

Several ReRAM devices have been fabricated in this work, including $Cu/TaO_x/Pt$ device which is generally used here as a benchmark device and is discussed in detail in this chapter. However, $Cu/TaO_x/Rh$ device is used to investigate the instability of conductive filaments in ReRAM cells during the READ Operation. The benchmark device $Cu/TaO_x/Pt$ is expected to yield
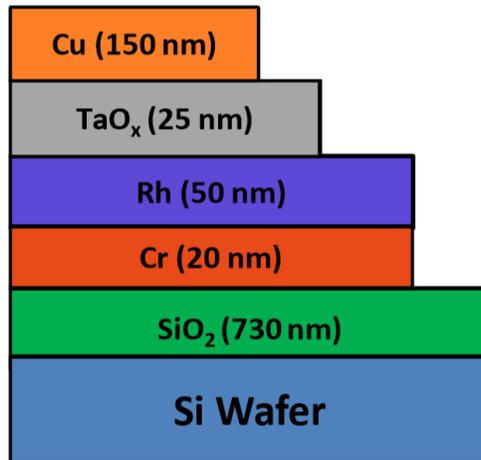
Fig. 2.19: *Device cross-section of Cu/TaOx/Rh resistive switching device.*

similar results. $Cu/TaO_x/Rh$ device has been fabricated in a crossbar array on a thermally oxidized Si wafer. The metal electrodes and solid electrolyte were deposited by e-beam evaporation and patterned by the lift-off technology. The oxygen-deficient tantalum oxide (TaO_x) layer was deposited by evaporating the Ta_2O_5 pellets without oxygen injection into the evaporation chamber.

A thin Cr layer was deposited between Rh bottom electrode and SiO_2 to improve the adhesion of Rh layer with SiO_2. The Cu top electrodes run perpendicularly to the Rh bottom electrodes and one resistive switch cell is located at each cross point with a blanket TaO_x layer of dielectric in between. The width of the metal lines varies from 1 μm to 35 μm. The Cu, TaO_x, Rh layers have been deposited by e-beam evaporation in a Kurt Lesker PVD-250 chamber, with the thicknesses 150 nm, 25 nm, 50 nm, respectively. More details on the manufacturing and characterization of the $Cu/TaO_x/Rh$ device are discussed in chapter 4 [86]. Fig. 2.19 shows the cross section of a Rhodium (Rh) devices with thickness of different layers specified.

2.6.2   Device Characterization and Discussion

The $Cu/TaO_x/Rh$ device is set by ramping the voltage at a constant ramp rate rr while limiting the current flowing through the device to a compliance current I_{CC}. Since for sufficiently high ramp rate (≥2V/s), the R_{ON} is related to I_{CC} by the relation $R_{on}=A/I_{CC}^n$ [64], for I_{CC}=500 μA it can be calculated that R_{ON}=1 kΩ. To investigate the resistance value obtained through the read measurements the following tests were conducted:

i.   Test 1: V_{SWEEP} from 0V to 0.1V, with and without I_{CC} = 5 μA

ii. Test 2: V_{SWEEP} from 0.1V to -0.1V with and without I_{CC} =5 μA

iii. Test 3: V_{SWEEP} from 0V to -4.0V with no I_{CC} imposed

iv. Test 4: V_{SWEEP} from -0.1V to 0.1V with and without I_{CC} = 5 μA

For R_{ON} formed at I_{CC}=500 μA, all tests return the same value of R_{ON} (set)=1 kΩ, independent of the voltage ramp rate rr. The above reading tests yield, however, different R_{ON} values for highly resistive filaments formed at low I_{CC} currents. Here the discussion of these effects

is started by forming a filament at I_{CC}=5 µA, which according to the relation calibrated to the device should give R_{ON} (set)=A/I_{CC}^n ≈100 kΩ. The actual experimental results and relevant observations are discussed in detail below:

2.6.2.1   Experimental Results of Reading Test 1

When performing the four reading tests specified above without imposition of I_{CC}, it was found that in all voltage intervals the same value of R_{ON}=0.45 kΩ independent of the voltage sweep ramp rate. This R_{ON} value is much smaller than the R_{ON} (set) = 100 kΩ. The R_{ON}=0.45 kΩ would correspond to on-resistance set at I_{CC}>500 µA. Hence the suspicion that the reading operations without imposition of I_{CC} have reconstructed the filament at already very small voltages. In the following the on-state set at I_{CC}=5 µA has been subjected to the four tests with I_{CC}=5 µA applied to tests 1, 2, and 4. Performing Test 1 (0.0V → 0.1V) the obtained $R_{ON}^+(1)$ (denoting reading of R_{ON} at positive voltage for Test 1), it is seen that $R_{ON}^+(1)$ values are a strong function of the ramp rate rr and are shown in Fig. 2.20(a). It can be seen that the R_{ON} values decrease strongly with decreasing ramp rate. Only at a high ramp rate rr=10 V/s, it is found that R_{ON}=100 kΩ≈ R_{ON} set) which can be identified with the R_{ON} reached after the set operation R_{ON} (set). It is expected that in this test the maximum current is 0.1V/100 kΩ=1 µA which is still less than the applied I_{CC}=5 µA used at the set operation and during the test. But it turns out that the cell current is reaching I_{CC}=5 µA at about 0.03-0.06V. Thus, the maximum voltage to which the filament is exposed is much less than the maximum voltage applied. The observed decrease of the measured R_{ON} with low rr, may be explained as follows. Assuming a truncated cone shape of the Cu filament, the bulk of the resistance R_{ON} resides at the tip of the cone. Consequently, when current flows through the

130

CF, a large voltage drop occurs at the tip generating there a large electric field whose maximum for Test 1 can be estimated to be $E_{max} \approx 0.1V/0.3nm = 3 \times 10^6$ V/cm, where 0.3 nm is the size of a Cu atom. This electric field is, indeed, close to the critical electric field estimated to be responsible
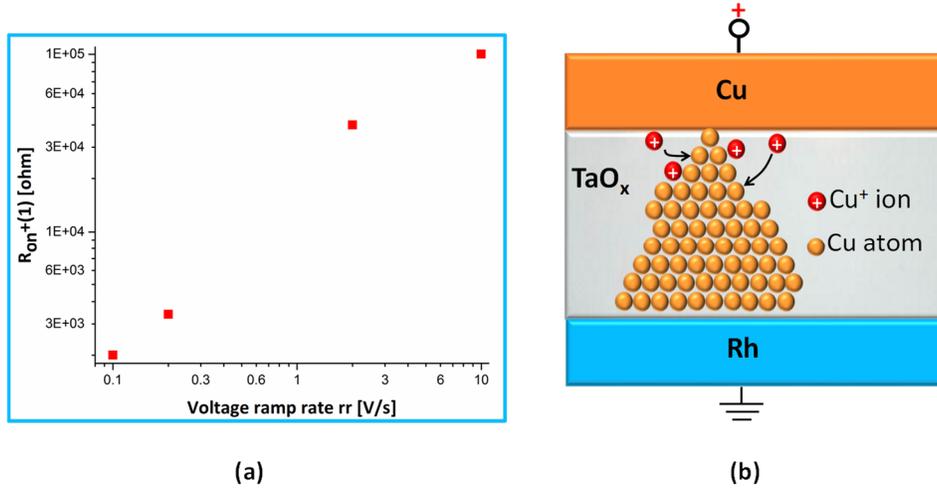
Fig. 2.20: *a) Reading of the CF resistance during Test 1 as a function of the voltage ramp rate rr. b) strengthening of the original tip of the filament by additional Cu^+ ions.*

for Cu drift transport in SiO_2 based dielectrics [87, 88]. For a slow ramp rate at positive bias there is plenty of time for Cu^+, created in the reaction at the Cu/TaO_x interface: $Cu \rightarrow Cu^+ + e^-$, to drift to the tip of the filament and to thicken the tip by additional Cu atoms, leading to a significant decrease of the R_{ON} resistance, which is shown in Fig. 2.20(b). The lower the ramp rate the larger is the Cu^+ drift to the tip of the cone, and consequently leading to a lower R_{ON} value. In contrast, at high ramp rate of rr=10V/s, the time is too short for the Cu^+ transport to add new Cu atoms to the filament and hence the R_{ON} remains unchanged. The device is now subjected to Test 2, ramping the voltage from 0.1V to -0.1 using I_{CC}=5 μA.

2.6.2.2   Experimental Results of Reading Test 2

For Test 2 one observes a clear change of slope at the origin, i.e. at 0V. The slope at positive voltage is denoted by $R_{ON}^+(2)$ and the slope at negative bias by $R_{ON}^-(2)$. It can be observed that $R_{ON}^+(2) \geq R_{ON}^+(1)$ and $R_{ON}^+(2) \geq R_{ON}^-(2)$. The ratio $R_{ON}^+(2)/R_{ON}^+(1)$ as a function of the ramp rate is shown in Fig. 2.21(a) and the ratio $R_{ON}^+(2) \geq R_{ON}^-(2)$ is shown in Fig. 2.21(b). It can be seen that this ratio is larger than 1 for low ramp rates rr and is equal 1 for rr=10V/s. For this high ramp rate all the resistances are the same, i.e. $R_{ON}^+(1) = R_{ON}^+(2) = R_{ON}^-(2) = R_{ON}$ (set) $= 100$ kΩ. First, a hypothesis is proposed for the observed inequality $R_{ON}^+(2) \geq R_{ON}^+(1)$, indicating a weakening of the CF during the sweep from 0.1V to 0.0V. During the ramp down of the voltage from 0.1V to 0.0.V in Test 2, it is expected not to have any additional transport of Cu^+ to the tip of the cone since the filament has seen already this bias at the end of Test 1. On these grounds, any lowering of $R_{ON}^+(2)$ compared with $R_{ON}^+(1)$ should be excluded. Experimentally this is confirmed and observed that $R_{ON}^+(2)$ actually increases, indicating a weakening of the filament. One way to explain this is to notice that the Cu atoms located on the surface of the truncated cone may undergo the same reaction $Cu \rightarrow Cu^+ + e-$ as at the Cu/TaO_x interface, see Fig. 2.22(a). The ratio of Cu surface atoms to volume Cu atoms is the largest at the tip of the cone. In absence of the $Cu^+ \rightarrow$ $TaV_oO_{x-1}+O^2$. It is known that TaO_x devices under a negative bias applied to Cu electrode form conductive filaments whose building blocks are oxygen vacancies [89]. The highest field is again Cu filament and reduce its resistance as depicted schematically in Fig. 2.22(b). This effect is another manifestation of a hybrid $Cu-V_o$ filament discussed in [90]: the CF consists now of Cu transport from the Cu/TaO_x interface, the positive field at the tip displaces the Cu^+ ions close to the tip of the cone deeper in the bulk of TaO_x layer, leading to a weakening of the filament and therefore to an increase of R_{ON} resistance. The smaller the ramp rate, the more time is given for

the process to proceed, leading to a larger increase in resistance. Eventually, this process will be opposed by the countervailing effect: the weakening of the tip would generate a larger voltage drop at the tip leading to a Cu^+ transport from the Cu/TaO_x interface. However, since the voltage is ramped down there is little time for this effect to come into play.

(a)

(b)
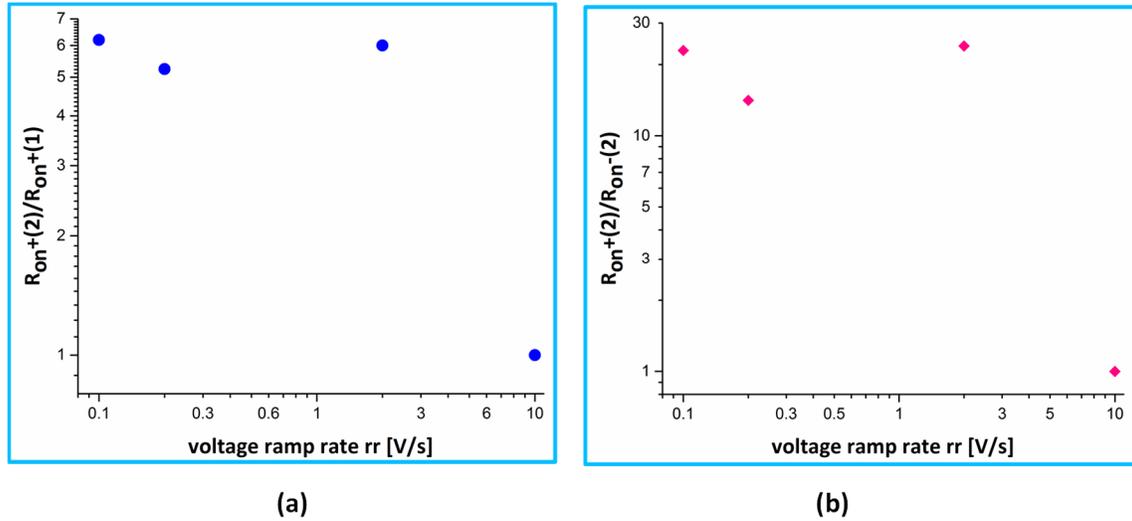
Fig. 2.21: *a) The ratio of resistances $R_{ON}^+(2)/R_{ON}^+(1)$ as a function of ramp rate rr. b) the ratio of on-resistance reading at positive, $R_{ON}^+(2)$, and negative bias, $R_{ON}^-(2)$, as a function of the ramp rate rr.*

Second, a hypothetical explanation is proposed for the ratio $R_{ON}^+(2)/R_{ON}^-(2) \geq 1$ being larger than unity, as shown in Fig. 2.21(a). This ratio is larger than 10 for all ramp rates except for rr=10V/s where the two values are the same. $R_{ON}^-(2)$ is the resistance measured at the negative bias from 0V to -0.1V. As soon as the sweep enters the negative bias range, there is a chance [89] to form oxygen vacancies V_o in TaO_x according to two reactions: (i) $Cu \rightarrow Cu^+ + e-$ which under a negative bias leads to injection of electrons into TaO_x and triggering the reaction (ii) TaO_x+2e^- at the tip of the cone and at negative bias oxygen vacancies will agglomerate around the tip of the

atoms and oxygen vacancies V_o. At a fast ramp rate, such as rr=10V/s, the time to form vacancies and to agglomerate them around the tip of Cu filament is too short to be effective. At lower ramp rate of 2V/s and below, there is enough time for vacancies to agglomerate and to reduce the overall
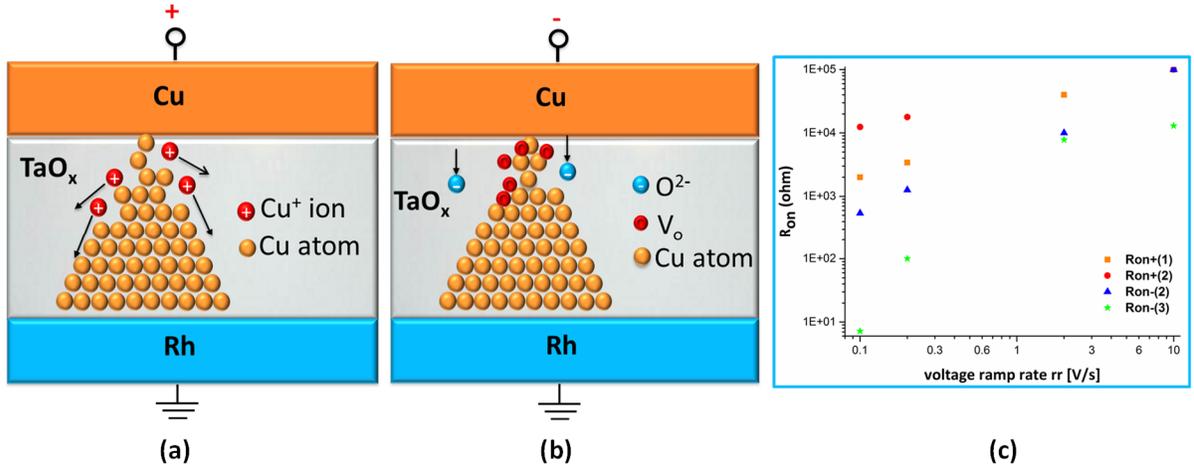
Fig. 2.22: *(a) under positive bias weakening of the Cu CF by dislodging Cu^+ ions from the surface of the filament. (b) under negative bias strengthening of the Cu CF by agglomeration of vacancies at the tip of CF. (c) readings of on-resistance at negative and positive bias for the reading tests 1, 2, and 3. $R_{ON}^+(1)$, $R_{ON}^+(2)$, $R_{ON}^-(2)$ at rr=10V/s have the same value of 100 $k\Omega$.*

resistance of the filament. The agglomeration of vacancies around the tip may also prevent removal of Cu^+ from the surface of the filament. Removal of Cu atoms by itself would weaken the filament and lead to a higher resistance.

2.6.2.3   Experimental Results of Reading Test 3

In the R_{ON} read measurement of Test 3, the R_{ON} resistance is probed at negative bias in the from 0 V to -4V at various voltage ramp rates. The resistance at negative voltages is denoted by $R_{ON}^-(3)$. It is observed that $R_{ON}^-(3)$ is consistently smaller than $R_{ON}^-(2)$. Test 2 ended at -0.1V and showed a significantly higher resistance value. The question arises why a new Test 3 performed at

negative bias starting at 0V produces a substantially lower resistance $R_{ON}^-(3)$. The results for $R_{ON}^+(1)$, $R_{ON}^+(2)$, $R_{ON}^-(2)$, and $R_{ON}^-(3)$ are shown in Fig. 2.22(c). The differences between the R_{ON} readings may be understood in terms of the different equilibrium conditions for electrons, Cu ions, oxygen vacancies, and oxygen ions. In Test 2, 0V is reached in passing during the sweep from 0.1V to -0.1V. In particular, during the 0.1V to 0.0V segment of the sweep all electrons in TaO_x are swept to the Cu electrode and TaO_x is mostly depleted of them. In case of Test 3, the sweep starts at 0V when there was an ample time to establish an equilibrium concentration of electrons including the electrons stemming from the reaction $Cu \rightarrow Cu^+ + e\text{-}$. Thus, for Test 3 there are much more electrons at 0V than for Test 2. When the bias becomes negative, those electrons are injected into TaO_x and induce formation of oxygen ions, O^{2-}, which in high electric fields around the tip of the filament are displaced and leave oxygen vacancies, V_o, behind. These vacancies agglomerate at the tip and lower the resistance $R_{ON}^-(3)$. A decrease of the voltage ramp rate allows more time for the process to occur, and therefore $R_{ON}^-(3)$ decreases with decreasing rr, as seen in Fig. 2.22(c).

2.6.2.4 Experimental Results of Reading Test 4

Finally, in Test 4 the sweep begins at a negative voltage of -0.1V and ends at 0.1V, i.e. it sweeps the same voltage interval but in an opposite direction as Test 2. Again, a change of slope at the origin can be observed: the R_{ON} resistance at negative bias is denoted by $R_{ON}^-(4)$ and at positive bias by $R_{ON}^+(4)$. Now the R_{ON} resistance readings between the Test 2 and Test 4 is compared. The relation for R_{ON}^+ and R_{ON}^- reverses for rr=0.2V/s: at low ramp rates such as rr=0.2V/s, for Test 2 $R_{ON}^+(2)>R_{ON}^-(2)$, whereas for Test 4 it is observed that $R_{ON}^+(4) < R_{ON}^-(4)$. However, for a fast ramp rate of rr=10V/s it is found that all the resistances $R_{ON}^+(2)$, $R_{ON}^-(2)$,

$R_{ON}^+(4)$, and $R_{ON}^-(4)$ are the same and equal to R_{ON} (set). There might be two reasons possibly responsible for the inequality $R_{ON}^-(4) > R_{ON}^+(4)$. At the negative bias, Cu atoms at the cone surface of the filament are ionized, dislodged, and moved by the electric field towards the Cu electrode, thus weakening the filament. This occurs at the beginning of the sweep at formally at -0.1V, but due to the imposition of I_{CC} effectively at -0.06V, when the electric field at the tip of CF is the highest. As soon as the sweep enters positive bias, the Cu^+ are moved back to the filament surface, thus strengthening the filament and lowering its resistance.

2.6.3   Summary

It is experimentally demonstrated that conductive filaments of resistive switching memory cells formed at low I_{CC} levels are very unstable and subject to reconstruction during read operations even at small voltages. The result of a R_{ON} reading depends on several details of the read operation: the starting voltage of the voltage sweep, polarity of the applied bias, and the voltage ramp rate. Thus, highly resistive filaments appear to be unsuited for memory applications as the read operation would not be able to differentiate between conductive on-states characterized by different on-state resistance, provided that the resistance of the filament is sufficiently high: 10 kΩ and larger. On the other hand, this intrinsic instability of highly resistive filaments provides a very sensitive probe into the microscopic mechanisms responsible for the filament formation, which involves the formation and transport of Cu atoms and ions, oxygen ions, and oxygen vacancies, as well as non-equilibrium conditions for electrons in the TaO_x and at the Cu/TaO_x as well as Cu CF/TaO_x interfaces. At negative bias, oxygen vacancies agglomerate around the tip of the original Cu filament, forming a composite $Cu-V_o$ filament, and effectively lowering its resistance. Most likely, useful information such as the efficiency of the redox reaction $Cu \longleftrightarrow Cu^+ + e\text{-}$ and reaction

responsible for formation of vacancies, i.e. $TaO_x + 2e^- \leftrightarrow TaV_oO_{x-1} + O^{2-}$ etc., may also be possible to extract.

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Chapter 3: Fabrication of Resistive Random-Access Memory (ReRAM) cells

3.1   Introduction

All the Resistive Switching Memory devices (ReRAM) described in this work were
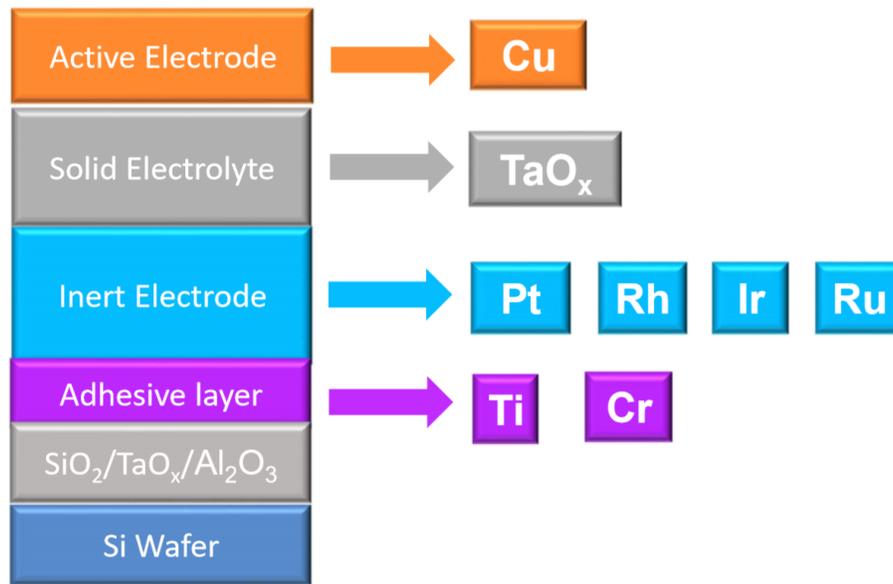
Fig. 3.1*: Cross-section schematic of ReRAM memory cell (inorganic) with different materials used for various layers*

fabricated at nanofabrication and characterization laboratory at Virginia Tech. The two terminal ReRAM devices have Metal-Insulator-Metal architecture and are arranged in a crossbar array. These ReRAM devices are processed on a thermally oxidized 4-inch diameter silicon wafer. The fabricated ReRAM devices can be categorized into the following two types:

i.   Inorganic devices

ii.   Organic (polymer) devices

In inorganic devices the solid electrolyte (oxide layer) was oxygen deficient TaO_x, whereas in polymer devices an organic polymer layer is used instead of TaO_x.
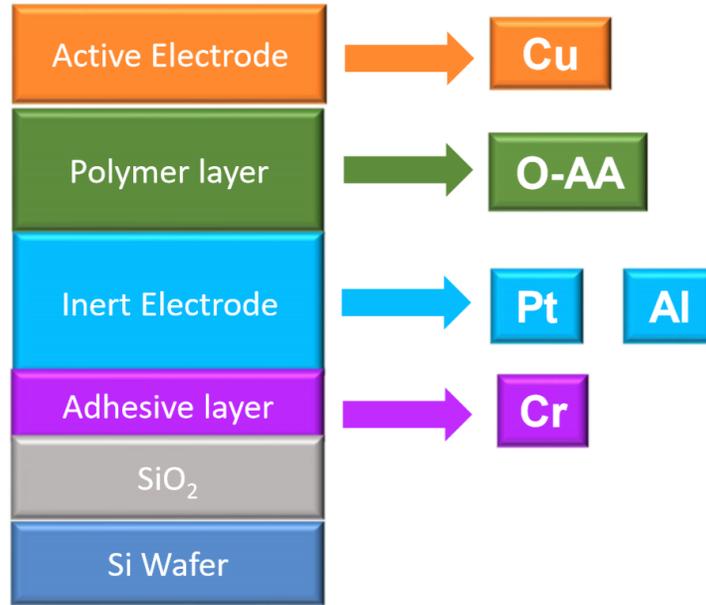
Fig. 3.2: *Cross-section schematic of ReRAM memory cell (organic) with different layers and corresponding materials used in this work*

3.2 Materials Selected for ReRAM Device

There are numerous potential materials which are being investigated for inorganic ReRAM devices. For top electrode Ag, Ni, Cu are some of the common choices. In case of solid electrolyte SiO_2, HfO_2, Ta_2O_5, TaO_x, WO_x etc. are used and are discussed in chapter 1. For bottom electrode Ta, W, Pt etc. have been explored by several researchers. In this work Cu is used as top electrode, oxygen deficient TaO_x as solid electrolyte and Pt, Rh, Ir, Ru as inert electrode and have been explored for resistive switching. Besides Ti, Cr has also been investigated as a thin adhesive layer. All the materials explored in this work for inorganic ReRAM device are summarized in Fig. 3.1. For organic or polymer ReRAM devices Cu is used as top electrode, O-AA (organic Anthranilic

146

acid) instead of solid electrolyte as dielectric layer and Al, Pt are used as bottom electrode. For
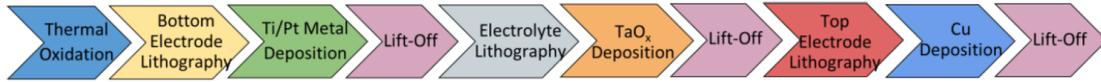
Fig. 3.3: *Fabrication process flow for ReRAM memory cell*

adhesion purpose, thin Cr layer is used. Figure 3.2 lists all the materials explored in this work for

organic ReRAM devices.

3.3   Step-By-Step Fabrication Process Flow

The complete process flow for fabrication of ReRAM memory cell is summarized in Fig.

3.3. Both inorganic ReRAM devices as well as polymer switching layer based organic ReRAM

devices are fabricated in this work. In the following some major processing steps are discussed in

detail:

i.   Cleaning

ii.   Thermal Oxidation

iii. Photolithography

iv.   Physical Vapor Deposition

v.   Liftoff

etc. for fabrication of inorganic ReRAM devices and

vi.   Polymer deposition and fabrication of organic memory devices

3.3.1   Wafer Cleaning

Cleaning is one of the most important process in the semiconductor fabrication process
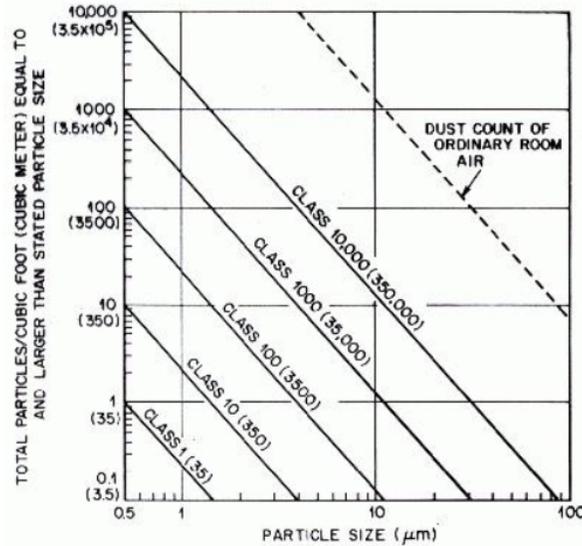
Fig. 3.4: *Various cleanroom classifications with particle sizes vs. particles/ft³ [1]*

flow. Any unwanted contamination can result degradation of device performance, poor device reliability and even complete failure of the device. Therefore, it is extremely important to precisely control the density and size of particulates or contaminants present in the device as well as within the fabrication environment. To avoid contaminants, dust, aerial particles etc. and to ensure a controlled temperature, pressure, humidity, lighting etc. the photolithography process is rather conducted in a controlled cleanroom atmosphere. Depending on the density of airborne particles there could be various classifications of cleanroom: class 10, class 100, class 1000, class 10000 etc. For example, a class 100 cleanroom is an environment where a 0.5 um or larger sized particle density is smaller than 100 counts/ft³. Various particle sizes and the corresponding cleanroom classifications are summarized in Fig. 3.4.

148

Cleaning procedure can be divided into two types- dry cleaning and wet cleaning. In dry cleaning, gas phase chemical reaction with contaminants create volatile compounds and thus cleans the wafer surface. However, in wet cleaning solvent/acid/base creates a solvable compound by reacting with contaminants. There are two major standard cleaning procedures developed by W. Kern are often widely used. In this procedure, cleaning is conducted through H_2O_2 and various oxide, acid/base solution followed by subsequent deionized water (DI) rinses. There are two standard procedures: RCA1 and RCA2 which removes the organic and metal ion contaminants

- N_2 blow dry
- Soak into acetone & ultrasonicate
- Soak into Isopropyl alcohol (IPA) & ultrasonicate
- Rinse using deionized (DI) water
- N_2 blow dry
- Soak into aqua regia
- Rinse using deionized (DI) water
- Soak into buffered hydrofluoric acid (BHF)
- N_2 blow dry
- Dehydration bake (10 minutes @ 115 °C)
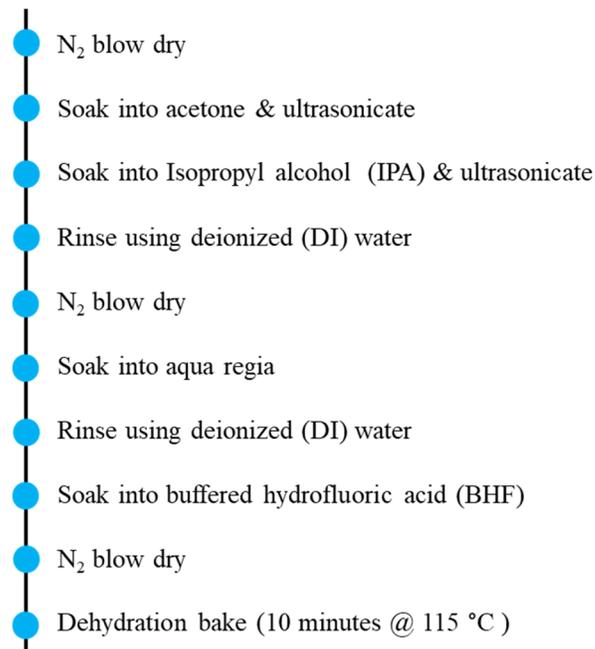
Fig. 3.5*: Wafer cleaning procedure followed in this work*

respectively. The solution for RCA 1 clean can be prepared using the following steps [2]:

i.   Ammonium and deionized water are mixed (NH_3: DI water = 1:5)

ii.   The above solution is heated to the boiling point

iii.   1 part of H_2O_2 is added into the as prepared solution

In RCA 1 clean, the wafer is submerged into the prepared solution and the organic contaminants

are removed. Again, for RCA 2 clean the solution preparation steps are [2]:

i.   HCl and deionized water are mixed (HCl: DI water = 1:6)

ii.   the solution is then heated to the boiling point

iii.   1 part of H_2O_2 is added into the solution

By immersing the wafer into the RCA 2 solution, metal ion contaminants are eliminated.

Wafer Cleaning Process Used in ReRAM device

During ReRAM device fabrication, wet cleaning procedure is used. The wafer is first blow-dried using nitrogen to remove any dust particles. Then it is cleaned using wet chemical cleaning

Fig. 3.6: a) Chemical fume hood; b) Ultrasonicator

process using solvents. Acetone, Isopropyl alcohol (isopropanol or 2-propanolisopropyl or IPA) are used as solvents. Every clean process is followed by rinsing into Deionized water and N_2 blow dry. The step-by step wafer cleaning procedure is illustrated using Fig. 3.5. The entire cleaning procedure with ultrasonication is conducted in a wet bench in VT cleanroom facility.

Figure 3.6 shows the ultrasonicator used in this work and the chemical fume hood where the wafer cleaning procedure is conducted.

3.3.2   Thermal Oxidation

One of the major advantages of silicon-based technology is that silicon can easily form high quality oxide through a process called oxidation. Oxidation of silicon is a method where a nearly uniform SiO$_2$ thin film (few nm to 2-3 µm) is obtained with low or acceptable levels of defect density. Oxides are typically used as an insulator in both active region of device as well as field region. This method is usually conducted at relatively high temperatures (900-1150^0 C) either using molecular oxygen as oxidant (dry oxidation) or oxygen with H$_2$O steam (wet oxidation). It is also called thermal oxidation. Typically, the reactions involved in the oxidation process are [3]:

$$Si_{(solid)} + O_{2(gas)} \rightarrow SiO_{2\ (solid)} \qquad\qquad (1)$$

or,

$$Si_{(solid)} + 2H_2O_{(steam)} \rightarrow SiO_{2\ (solid)} + 2H_{2\ (gas)} \qquad (2)$$
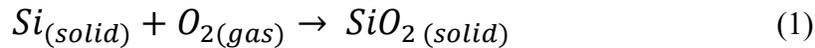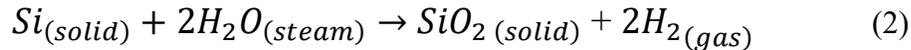
In the above reactions, silicon atoms are supplied by the Si substrate, O_2 are the dry oxygen supplied as a gas source for dry oxidation process and H_2O are the steam supplied along with oxygen gas during the wet oxidation process.

The density of oxide is low for wet oxidation process, but it provides higher oxidation (oxide growth) rate. On the contrary, dry oxidation provides high quality (dense) oxide at the cost of lower oxidation rate. During the thermal oxidation process 44% of silicon is consumed from the substrate [3]. Silicon oxidation can readily happen even at room temperature and can form a very thin (15^0 - 20^0 A) low quality oxide, usually called as native oxide. Since this native oxide can passivate the surface at room temperature, it prevents further oxidation at room temperature. It is a common practice to strip this native oxide by dipping Si wafer into HF (Hydrofluoric acid) or

BHF solution (Buffered Hydrofluoric Acid) as part of the wafer cleaning procedure before the beginning of thermal oxidation process. By controlling the furnace temperature, oxidation duration and gas flow rate into the oxidation chamber, the oxide thickness can be precisely controlled. It is possible to process multiple wafers at the same time through batch processing by loading several wafers into a wafer boat. Although thermal oxidation can provide high quality oxides, the usage of this process is limited to few early stages of processing due to potential contamination of furnace, inability of some potential materials used in later process steps to endure such high temperature etc.

The thickness of oxide greater than 300^0 A can be accurately predicted by Deal-Grove model [4]. When Si atom and oxygen molecule come together and react, it forms SiO_2. As discussed before, 2-2.5 nm oxide can form even at room temperature. But once some thin layer of SiO_2 is formed, to continue further growth either oxygen molecules need to travel through that already existing oxide layer and reach Si surface or Si atoms need to pass through that oxide layer to encounter oxygen at wafer surface through a process called diffusion and then react. However, the diffusivity of oxygen in SiO_2 is several orders of magnitude higher than that of Si. Therefore, oxygen diffusion into oxide is dominant and chemical reaction happens only at Si/SiO_2 interface. This Si/SiO_2 interface always stays inside and never meets atmosphere and therefore it is reasonably free from impurities. Thus, thermal oxidation provides high quality, low defect density silicon dioxide.

The thermal energy at room temperature is very low for both silicon and oxygen molecule. Therefore, none of them could diffuse through the thin native oxide (15^0 - 20^0 A) layer present at room temperature. Thus, the oxidation process terminates quickly, and the native oxide cannot get thicker anymore. To ensure an incessant reaction, thermal energy (heat) needs to be supplied to

the Si wafer in an oxidizing environment. The entire gas phase oxidation process can be comprising of the following three series steps: i) transportation of gas phase oxidant to the wafer surface (F_1), ii) diffusion of the species across the oxide layer (F_2), and iii) the oxidation reaction (F_3). The entire oxidation process is demonstrated in detail in Fig. 3.7 in terms of four components C_g, C_s, C_o, C_I, which are oxygen concentration in the atmospheric gas far away from the wafer, oxygen concentration in the stagnant layer at the wafer surface, oxygen concentration in the oxide of the wafer surface and oxygen concentration at Si/SiO$_2$ interface into the oxide respectively. The term flux (F) can be defined as the number of oxygen molecules passing through an area per unit time. It is also called as oxygen flux. It can be approximated that only gas flow is not enough to transport oxygen molecule from bulk of the atmospheric gas into the oxide region. Therefore, Fick's first law can be used to define its diffusion through this region as [6]:

$$F_1 \approx D_1 * \frac{C_g - C_s}{t_{stag}} \tag{3}$$

Where D_1 is the diffusion coefficient between atmosphere and stagnant gas layer and t_{stag} is the thickness of stagnant gas layer. This can again be rewritten using mass transfer coefficient as:

$$F_1 = F_{gas} = h_g * (C_g - C_s) \tag{4}$$

The other two fluxes can also be expressed as [3]:

$$F_2 \approx D_2 * \frac{C_0 - C_i}{t_{oxide}} \tag{5}$$

$$F_3 \approx K_s * C_I \tag{6}$$

Where F_2 is molecular oxygen diffusion flux through the oxide due to concentration gradient between ambient (oxygen source) and reacting surface and t_{oxide} is the oxide layer thickness. Now it can be safely assumed that oxygen concentration linearly varies in the growing oxide film.
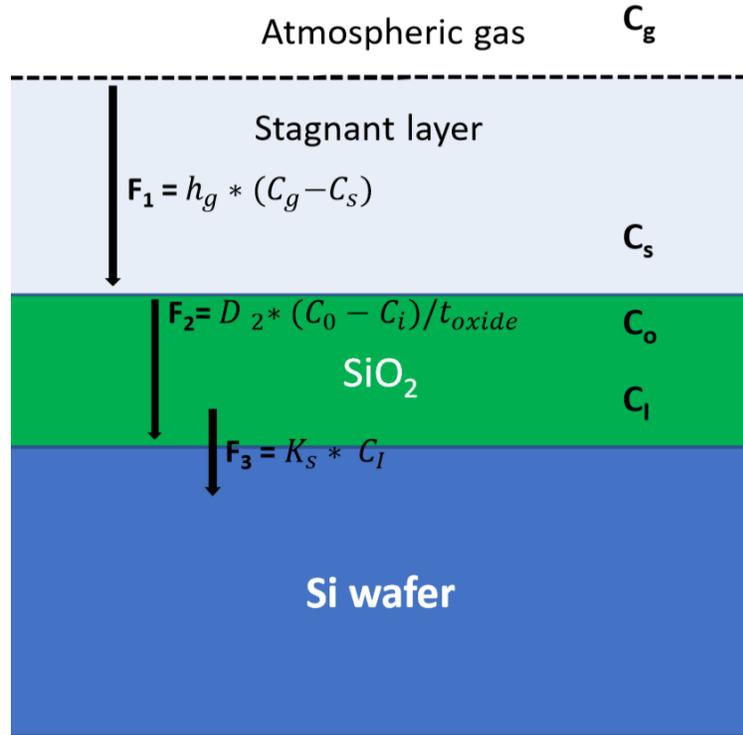
Fig. 3.7: *Schematic diagram containing all the fluxes in silicon oxidation process [5]*

The flux F_3 is due to oxygen reaction at reacting surface where there is copious supply of silicon to react and form SiO₂ and it is controlled by reaction kinetics. In equilibrium all fluxes must balance:

$$F_1 = F_2 = F_3 \qquad (7)$$

So, the oxide thickness can be expressed by a differential eq'n (8) as [6]:

$$t_{oxide}^2 + A * t_{oxide} = B * (t + \tau) \qquad (8)$$

Where,
$$A = 2 * D \left(\frac{1}{K_s} + \frac{1}{h}\right)$$

$$B = \frac{2*D*H*p_g}{N_1}$$

$$\tau = \frac{t_0^2 + A * t_0}{B}$$

Here, initial oxide thickness is t_0. Since oxidation is usually carried out at atmospheric pressure, $K_s \ll h$ and growth rate is therefore independent of mas transfer coefficient or furnace geometry.
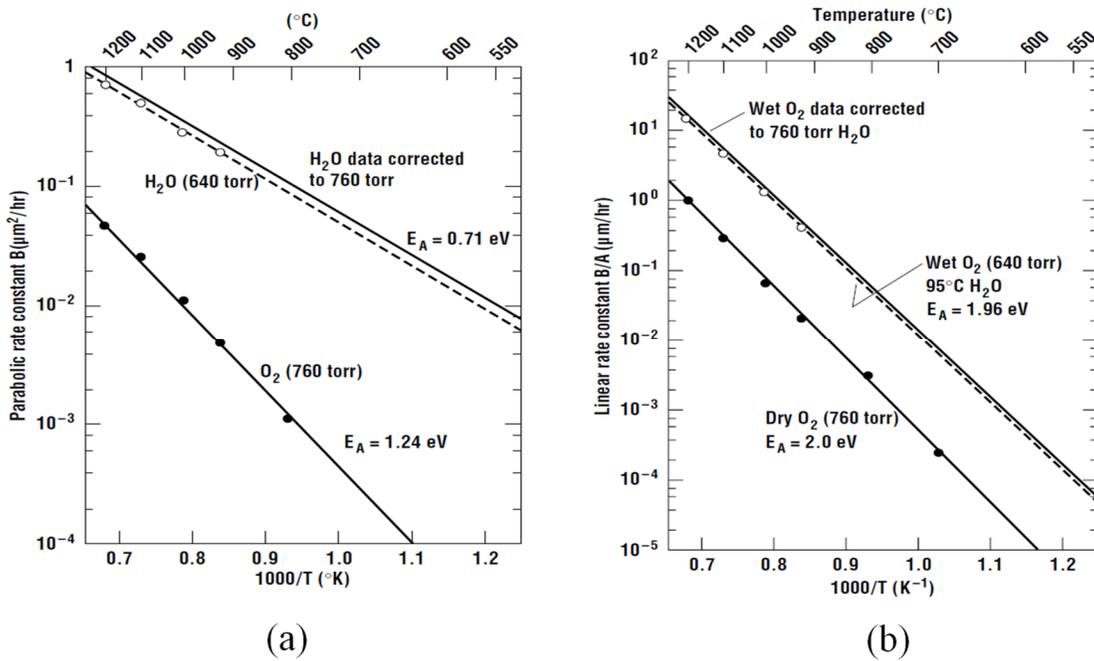
Fig. 3.8: *Arrhenius plot of a) parabolic rate constant (B); b) linear rate constant (B/A) for both dry and wet oxidation*. Reprinted with permission from [6], Copyright 2008, Oxford University Press, Inc.

Both A and B coefficients are proportional to diffusivity and follows Arrhenius function too [6].

For a considerably thick oxide film, the linear thickness term in eq'n (8) can be neglected and, $t_{oxide}^2 = B * (t + \tau)$ (9)

On the contrary, when the oxide film is very thin, the quadratic term in eq'n (8) can be ignored and so,

$$t_{oxide} = \frac{B}{A} * (t + \tau) \qquad (10)$$

Here, B is parabolic rate coefficient and B/A is called as linear rate coefficient in accordance with the simplified assumption shown in eq. (9) and eq. (10) respectively. Figure 3.8(a) and Fig. 3.8(b) shows parabolic and linear rate coefficient respectively and some typical values of those parameters are summarized for standard process conditions in Table 3.1.

From the perspective of micro/nanoelectronics fabrication process, amorphous form of SiO_2 is preferred and this form of silicon dioxide is also called as fused silica. Its short-range

Table 3.1: *Oxidation coefficients for silicon.* Reprinted with permission from [6], Copyright 2008, Oxford University Press, Inc.

Temperature (°C)	Dry			Wet (640 torr)	
	A (μm)	B (μm^2/hr)	τ (hr)	A (μm)	B (μm^2/hr)
800	0.370	0.0011	9	—	—
920	0.235	0.0049	1.4	0.50	0.203
1000	0.165	0.0117	0.37	0.226	0.287
1100	0.090	0.027	0.076	0.11	0.510
1200	0.040	0.045	0.027	0.05	0.720

atomic orientation contains four oxygen atoms at the corners and one at the center of the polyhedron structure. The orientation of silicon substrate can also affect the thermal oxidation rate through adapting linear oxidation rate constant for surface reaction rate limited process. For example, oxidation rate of (111) surface is 1.7 times faster than that of a (100) surface. This is usually attributed to the low density of silicon bonds at (100) surface than that at (111) surface [5].

Thermal Oxidation Process Used in ReRAM Device

The oxidation process can be divided into two parts-dry oxidation and wet oxidation. Figure 3.9 shows a schematic oxidation furnace and its various important parts. The oxidation furnace system used in this work along with the wafer load tray is shown in Fig. 3.10. During dry oxidation high purity O_2 is flown into the chamber, whereas for wet oxidation steam is added with
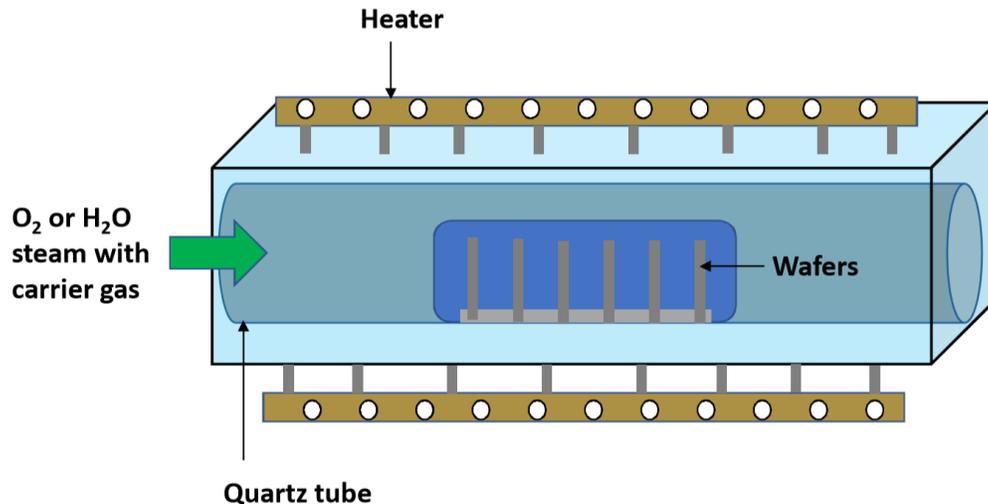
Fig. 3.9: *Oxidation-furnace schematic diagram*

O_2 at the desired chamber temperature. Dry oxidation process is slow but provides high -quality and dense oxide. On the contrary, wet oxidation provides less dense oxide but with a faster oxidation rate. For the ReRAM device, thick isolation oxide is required to avoid unwanted current flow between the memory arrays which are fabricated on top of that oxide. Therefore, thicker wet oxide is sandwiched between two thin dry oxide layers. The oxidation process therefore consists of short duration (~10 minutes) dry oxidation, followed by long duration wet oxidation (~2 hours) and short duration dry oxidation (~10 minutes) processes.

The wafers are first cleaned using wet chemical cleaning process discussed above. The oxidation furnace is then set at 650^0 C temperature and high purity N_2 is purged into the chamber

at the rate of 1L/min. Once the chamber reaches the set temperature, cleaned Si wafer is then placed onto a quartz boat and loaded into chamber. The chamber temperature is then set at desired

(a)   (b)   (c)
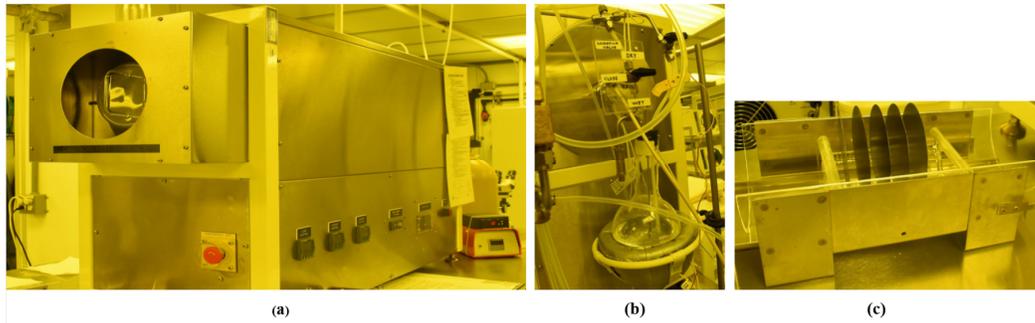
Fig. 3.10: a) Oxidation-furnace; b) O$_2$ & N$_2$ flow valve with steam boiler; c) Quartz tray loaded with wafer (from oxidation process used in this work)

oxidation temperature of 1050^0 C. The boiler assembly loaded with a distilled water filled beaker

- Set chamber temperature $=650^0$ C and N$_2$ flow rate $=$1L/min

- Place wafer on quartz tray and load into chamber

- Set steam boiler temperature $=95\sim97^0$ C & chamber temperate$=$ 1050^0 C

- Close N$_2$ valve and open O$_2$ valve with flow rate$=$ 0.7 L/min

- Time the Dry oxidation process for desired thickness

- Open steam flow valve for desired duration of wet oxidation

- Close steam flow valve and run dry oxidation for desired thickness

- Close O$_2$ flow valve, turn off steam boiler, set N$_2$ flow rate$=$ 1L/min

- Set chamber temperate to ambient temperature and wait for it to cool down

- Take quartz tray loaded with wafer out of chamber

- Turn off N2 flow

Fig. 3.11: Thermal oxidation process flow used in this work

is then set at 95-97^{0}C so that O_2 flow can be passed through a bubbler containing steam and O_2 with steam can be supplied into the furnace during wet oxidation. There is a thermocouple set up within the furnace to monitor chamber temperature. Once the chamber reaches oxidation temperature, N_2 flow valve is closed and O_2 is supplied into the chamber with a rate of 0.7L/min. This starts dry oxidation process. This process is continued for a predetermined amount of time for the desired dry oxide thickness. During the wet oxidation the steam valve is opened for certain duration. Finally, the steam flow valve is closed for the final dry oxidation process. Once the oxidation process is completed, O_2 flow valve is closed, N_2 purge valve is opened and the chamber temperature is ramped down to room temperature. When the chamber reaches ambient temperature the quartz boat containing water is taken out of the furnace. The entire oxidation process is summarized in Fig. 3.11.

3.3.3 Photolithography

The word "lithography" comes from the Greek origin "lithos (stone)" and "graphein" (write). Lithography is a printing method where a shape form master pattern is transferred onto the substrate or wafer. In integrated circuit (IC) industry, the term "photolithography" is widely used instead of "lithography" where a sequence of multiple complex pattern is consecutively transferred. There has been significant research and development effort in photolithography which is enabling to realize ceaselessly smaller and smaller features.

3.3.3.1 Spin-coating Photoresist

Photoresist is a light sensitive organic (polymer) material whose solubility can be modulated (soluble or insoluble to developer solution) upon exposure to controlled doses of

ultraviolet radiation. Photoresist contains three components: solvent, resist polymer and sensitizer. Solvent enables pouring and spreading of resist on the wafer surface, resist polymer changes its structure through crosslinking with molecules upon exposure to UV light and, sensitizer controls the photochemical reaction.

Photoresist can be either positive type or negative type. In positive tone resist, the UV
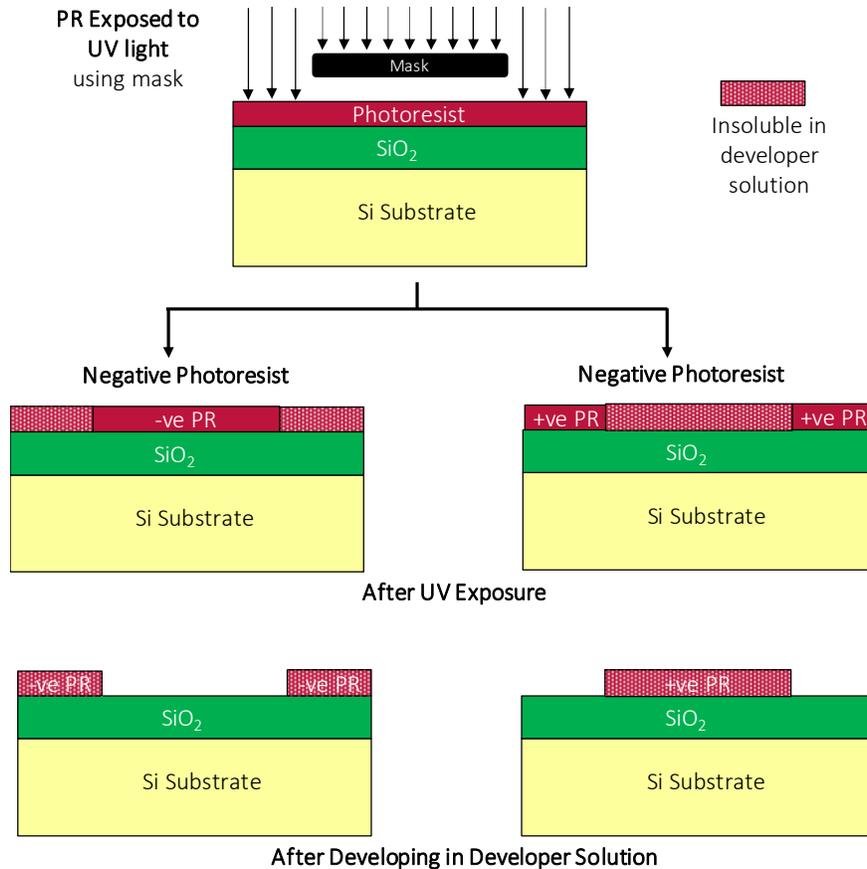
Fig. 3.12: *Negative vs. positive photoresist: UV exposure, development and pattern transfer*

exposure deteriorates the strength of the main or side polymer chains in the exposed area during the photochemical reaction and therefore those regions are developed faster than the unexposed areas and are washed out after development. On the contrary, in the UV exposed areas negative tone photoresist strengthens its bonds with main or side chain through crosslinking and unexposed

160

areas are thus dissolved instead. Figure 3.12 shows the process flow for both positive as well as negative photoresist.

Spin-coating is one of the most important steps for pattern transfer procedure as it controls the potential defect density that can be transferred to the subsequent process to follow. The excellence of this process determines the quality of reproducible feature size or line widths. Once

Spin-coat HMDS (Hexamethyldisiloxane) on wafer
  i. 15 sec @ 500 rpm
  ii. 45 sec @ 3000 rpm

Pre-bake: 1 minute @ 110 ^{0}C

Spin-coat photoresist AZ 5214
  i. 15 sec @ 500 rpm
  ii. 45 sec@ 1500 rpm
  iii. 15 sec @ 500 rpm

Soft-bake: 1 minute @ 110 ^{0}C

UV exposure (I or h-line) for a dose ~ 90 mJ/cm^2

Post exposure bake: 90 sec@ 110 ^{0}C

Flood exposure: > 200 mJ/cm^2

Develop: MF 319 @ 1min
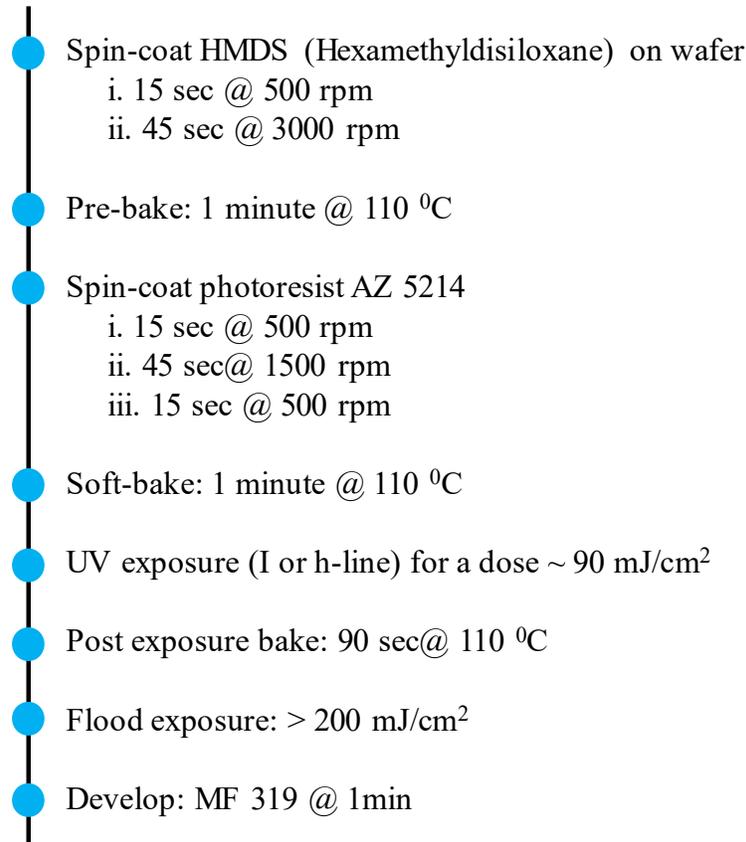
Fig. 3.13: Thermal oxidation process flow used in this work

the wafer is cleaned, it is then locked in a wafer platen assembly of a spinner through a controllable vacuum clamp. The next step is wafer priming. Some photoresist may not adhere well enough to the silicon wafer which is usually coated with a thin native oxide. To ensure better adhesion, the photo-process must be conducted in a controlled temperature and humidity (~40% RH)

environment and the surface need to be hydrophobic. Therefore, once the wafer cleaning procedure is successfully completed it is annealed to remove any unwanted water remaining on the wafer surface. Besides adhesion promoter such as Hexamethyldisiloxane (HMDS) can also provide excellent adhesion to the photoresist. Its functional cluster can easily react and form bond with oxide followed by strong adhesion to the resist. The next step is spin-coating a UV sensitive thin polymer layer on the wafer. Depending on the desired thickness of organic polymer film, the wafer is spun at a predetermined high speed and uniform thin coating is achieved. The viscosity of the resist polymer and spun speed determines the PR film thickness. The photoresist vendor often provides a datasheet or spin speed vs. film thickness plot for reference. The film thickness (T) can be expressed by the following empirical relationship as [2]:

$$T = \frac{k * C^{\beta} * \eta^{\gamma}}{\omega^{a}} \quad (11)$$

Here k is a calibration constant, C is the resist polymer concentration, η is viscosity of the selected polymer and ω is the spin-speed (rpm). The amount of photoresist to be spun on each wafer should be an educated guesstimate: too miniscule amount would create areas not covered by photoresist and too much resist would lead to ridges at the edge. Edge bed removal can alleviate this problem to some extent. The spun photoresist film contains some solvent with it (10%~15%) and is usually followed by a soft-bake (90^{0}~110^{0} C) step for few minutes. It is also called as pre-bake. This pre-bake step serves as the adhesion promoter as well as improves the process/device yield. AZ 5214 E image reversal high resolution photoresist is used for this work and photoresist with thickness~ 2 µm is usually achieved. The process recipe is shown in Fig. 3.13.

3.3.3.2　　Mask Alignment & UV Exposure

Mask is the master template used to recurrently produce the prototype pattern onto the polymer coated substrate. It is usually made of quartz and are optically flat. Ultraviolet (UV) light can pass through glass and quartz but is impervious to metal design written onto the quartz. Electron-beam lithography is used to print this high-resolution metallic design pattern (chrome) on the mask. Depending on the nature of contact between mask and substrate, optical exposure apparatuses can be categorized as: contact printing, projection printing and proximity printing. In case of contact mask system chrome-side of mask comes in contact with the underneath polymer coated wafer and theoretically minimizes the diffraction effects. However, neither wafer nor mask is perfectly flat. By applying few atmospheric pressure (~0.05 to 0.3 atm) the contact between mask and wafer is significantly improved and the surface nonuniformity effect is dramatically reduced. The wafer can also be aligned with respect to mask by exploring the available features such as, movement along x and y direction, few degrees of rotation (theta movement). High intensity mercury arc lamp can expose the wafer with controlled amount of dose as required. This system is inexpensive and can print features as small as 0.5 μm [7]. This hard contact system is limited by the amount of defect generation over time on both wafer as well as on mask. Since wafer and mask are in close contact, the printed resolution is also affected by the degree of light scattering by the thin film polymer spun-coated on the wafer.

Proximity printing is a non-contact printing where the space between mask and wafer (10-100 μm) is precisely controlled by N_2 flow. This technique is free from generation of any contact related defects, but at the expense of reduced resolution. If g (~0 to 15 μm) is the gap between mask and wafer, the minimum feature size that can be resolved using this technique can be expressed as [7]:

$$W_{min} = \sqrt{k * \lambda * g} \qquad (12)$$

Here the value of constant k depends on photoresist process.

Projection printing is the upgraded version of contact printing which can provide superior resolution with no contact related defect generation and is the most preferred technology. There are two different types of lenses used in this system: condenser and projector [7]. Condenser either collimates or focuses the light on the projector after passing through the mask and projector refocuses that on the wafer. Again, since light coming from condenser lens side can be diffracted by the mask placed on its way, to successfully reimage the pattern and project on the wafer optical systems in place should be capable of collecting several orders of diffracted light (at least 2~3 diffraction order). The numerical aperture of that optical system can be expressed as:

$$NA = n * \sin \theta \qquad (13)$$

Here θ is the half angle of acceptance and n is index of refraction of the medium. However, the resolution of this system is affected by imperfections such as distortion, aberration, separation of mask-lens etc. [7]. For a well-designed optical system, the limit can be expressed by Rayleigh criterion as [7]:

$$W_{min} \cong k * \frac{\lambda}{NA} \qquad (14)$$

Here k is a system dependent constant and varies between 0.4 to 0.8.

Shorter wavelengths are used to print smaller features, but at the expense of increased complexity of the exposure system with more optics to be added into the system. This will make the system more expensive and will absorb further energy, specially at shorter wavelengths. One potential solution could be deployment of highly sensitive photoresist as it likely compensates for the energy loss. Modern state of the art systems can print image as small as size of the wavelength

used and further improvements can be achieved with resolution enhancement technique (RET).

After the wafers are coated with polymer (photoresist), these are then loaded into the mask aligner and exposure system so that the wafer can be precisely oriented with the respective alignment geometry marked on the mask. The wafer is then exposed with required dose (J/cm^2) of
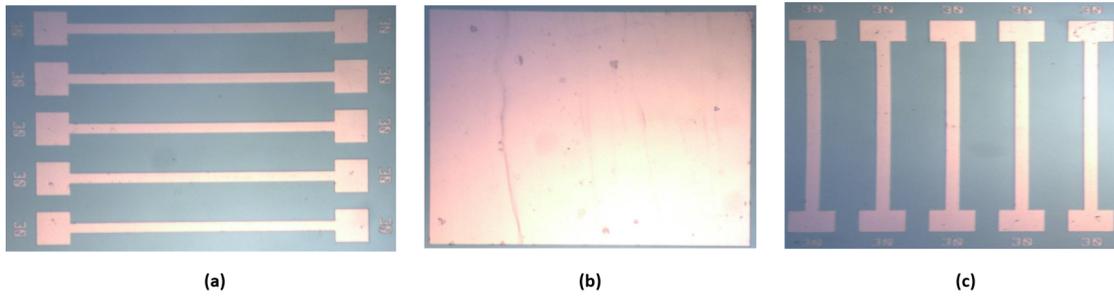
Fig. 3.14: *Quartz photomask for patterning: a) Bottom electrode; b) Solid electrolyte; c) Top electrode*

UV lamp to replicate a perfect duplication of the mask image onto the resist. The dose (J/cm^2) is source light intensity (W/cm^2) multiplied by the duration of exposure (seconds): $\frac{J}{cm^2} = \frac{W}{cm^2} * sec$
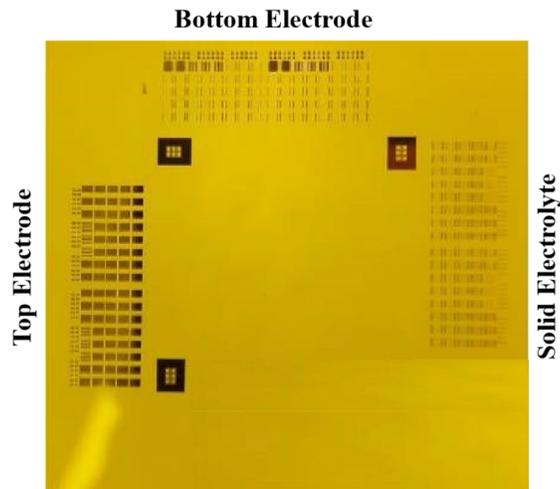
Fig. 3.15: *Complete mask used in this work for: top electrode, solid electrolyte and bottom electrode*

In photolithography, depending on the available optics the source light can be of a wide range

165

of wavelengths: EUV (extreme ultraviolet) to UV (near ultraviolet) with wavelength of 10-14 nm to 350-500 nm respectively. Near UV system is the most commonly used one and usually comprises of i-line (365 nm) or g-line (435 nm) with mercury lamp as the source.

Three different quartz photomasks are used for the ReRAM device fabrication in this work. One mask for the top electrode, one for the solid electrolyte layer and one mask for the bottom electrode layer. Every mask-set has its own alignment mark to facilitate alignment with the subsequent process steps. Each ReRAM cell is located at the intersection of top and bottom electrode where its size is ranged from 1 µm to 35 µm and there are 100 devices at each size. The top and bottom electrode layers are arranged in a crossbar array arrangement. Figure 3.14 shows the masks for top electrode, solid electrolyte and bottom electrode for crossbar array organized 30x30 µm ReRAM cells. The entire photomask is also shown in Fig. 3.15. The spin-coating

(a)   (b)
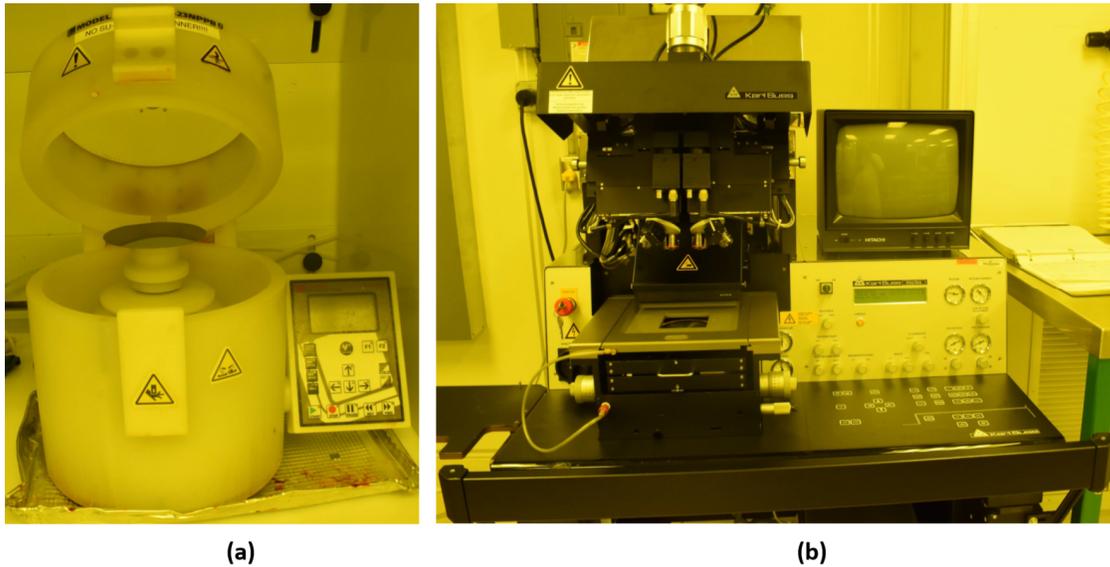
Fig. 3.16: *a) Spin-coating system; b) Karl-SUSS MA6 mask alignment system used in this work*

system and mask alignment tool used in this work are shown in Fig. 3.16.

166

3.3.3.3 Post-exposure Bake (PEB)

The next step is post-exposure baking (PEB) such as flood exposure, post-baking which either initiates new chemical reaction or terminates the already started one as needed and determined by the selection of wavelength, photoresist and the governing chemistry. PEB is very crucial for image reversal photoresist. The post-bake temperature is usually somewhat higher than pre-bake temperature. But, this temperature needs to be carefully selected since with the presence of catalyst the reaction is accelerated with temperature. This step also affects the outcome of the next development process.

3.3.2.4 Development

The final stage of lithography is the development where photoresist is selectively removed upon dissolving into developer solution. It results a transferred pattern as designed and required by the subsequent steps to follow. Development can be two types: wet development and dry development [2]. Usually in wet development, wafers are immersed into developer solution at a certain temperature for a specific time period. If the sample wetting is a challenge, surfactant can be used to make it uniform. For an extremely quick development process, buffers solution can provide an extended development time for better duration control. However, when negative photoresist encounters organic solvent it can bulge, and its adhesion property can also be comprised. Vapor based dry development process can be a potential solution to this problem which is recently preferred for high resolution features.

MF-319 developer is used for the image reversal photoresist AZ 5214 E-IR in this work. The development time is approximately 60-70 seconds and require some agitation during the development process. The wafer is then deionized water rinsed and N_2 blow dried. After successful

development, reversed image of the mask is transferred to the substrate. Dektak surface profiler is used to verify the thickness of the photoresist and is found to be approximately ~ 2 µm.

Before the sample is moved out for the next process step, it is preferably post baked or hard baked at somewhat higher temperature and extended duration compared to the pre-bake process. This is especially true for negative photoresist which usually swells after development steps. By removing the excess solvents from the resist, it also improves resist quality as well as significantly improves the adhesion.

3.3.4   Physical Vapor Deposition

E-beam evaporation (electron-beam), a physical vapor deposition technique is used in this work to deposit thin film by evaporating and physically transferring materials from crucibles (material holder) onto the substrate which is usually located on top of the crucible without involving any chemical reaction. As the method implies, the materials to be deposited need to be heated. Crucible heating systems can be of three types: resistive, inductive and electron-beam [8]. In resistive evaporation system, charge loaded into crucible is being resistively heated. Since both filament wire and evaporation materials are equally heated, evaporation and outgassing of wire can be a challenging problem. For inductive heating system, RF powered wire is wrapped around the loaded crucible and induced eddy current heats the crucible. Water-cooled system can be deployed to keep the temperature within the desired limit. However, there is a potential risk to contaminate evaporation materials with crucible whenever high melting temperature materials need to be deposited. E-beam heating system comes with the solution, where only evaporation materials are heated but the crucible is being cooled down. In the e-beam evaporation system, typically there is an electron gun which can provide high density of beam depending on supplied

current level which can be directionally controlled by a strong magnetic field and can eventually lead the beam to be incident onto the evaporation source materials. The beam can also be rastered across the evaporation material region within the crucible to control the amount of material to be
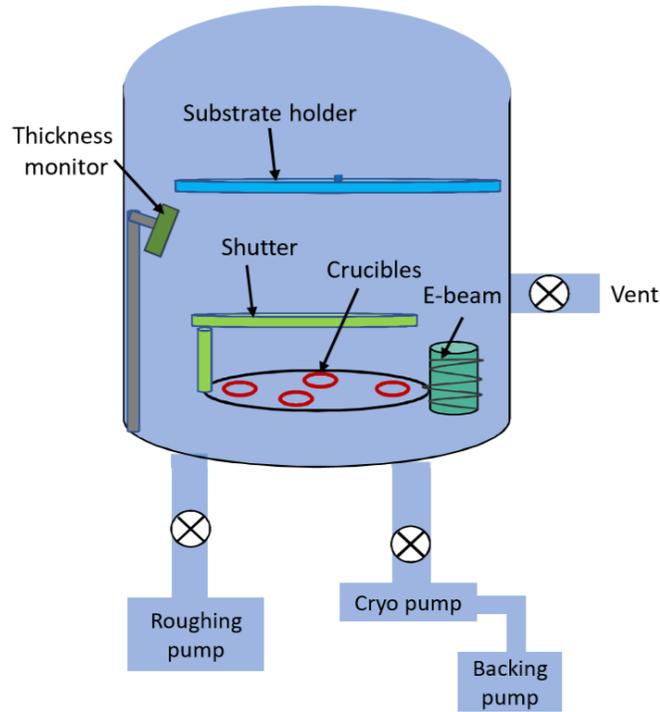
Fig. 3.17: A simple E-beam evaporation chamber schematic

heated to be deposited. However, this technique also has some challenges such as potential radiation induced damage, hot-electron induced contamination etc. Although state of the art micro/nanofabrication technologies use sputtering for metal deposition, evaporation is still used in research and development works.

A 3D schematic of an evaporation system is shown in Fig. 3.17. Usually there are multiple crucible positions in the chamber to load several evaporation materials and deposit multiple thin films in a single vacuum. The chamber can be pumped down to pressure, $P \leq 10^{-6}$ torr through a combination of roughing pump and a diffusion or cryopump. The pumping down process starts

with roughing pump. When chamber pressure reaches on the order of 10^{-3} torr the cryopump takes over, which can trap gas molecules on its surface to further reduce the pressure. Over time, the cryopump gets saturated with trapped molecules and therefore the chamber needs to be periodically regenerated (heating and purging with N_2 gas) to maintain the pumping capacity of the cryopump. At low chamber pressure ($\sim 10^{-6}$ torr), the mean free path of the molecules gets sufficiently higher. Therefore, as the evaporation materials is heated through e-beams, it can yield vapor, which can travel in a straight line up to the substrate located on top of the source materials by adopting a spherical geometry. As the evaporated source materials strike the substrate it gets physically deposited on the substrate without going through any chemical reaction. Hence the process is called as physical vapor deposition (PVD).

Although at low chamber pressure the evaporated materials can travel relatively straight vertical path, only a fraction of materials evaporated into the crucible actually accumulate onto the wafer surface located on top. This is because a fraction of angle seen from crucible is subtended by the wafer and some materials are lost. The evaporated material deposition rate can be defined as the rate of mass accumulation at wafer surface/area and can be expressed as [8]:

$$R_{deposition} = \sqrt{\frac{M}{2*\pi*K*\rho^2}} * \frac{P_e}{\sqrt{T}} * \frac{A}{4*\pi*r^2} \qquad (15)$$

The deposition rate is dependent on evaporation source materials, deposition temperature and chamber geometry. Although arranging wafers in a planetary fashion (hemispherical cage) can provide nearly uniform deposition rate across various wafers processed at the same time, there will still exist some minor variability due to flat geometrical shape of the wafer [8].

There are several parameters that can be controlled by the user during the deposition process using Kurt J Lesker PVD 250, such as:

i.   Lateral/longitudinal amplitude of beam sweep (it controls evaporation area)

ii. Level of current supplied (it controls beam density and deposition rate)

The deposition rate as well as the film thickness is usually monitored through a microbalance quartz crystal, which changes its resonant frequency as more and more materials are being deposited during the film deposition process. Material parameter such as density of evaporation source, and geometrical parameters such as tooling factor, Z-ratio etc. are also
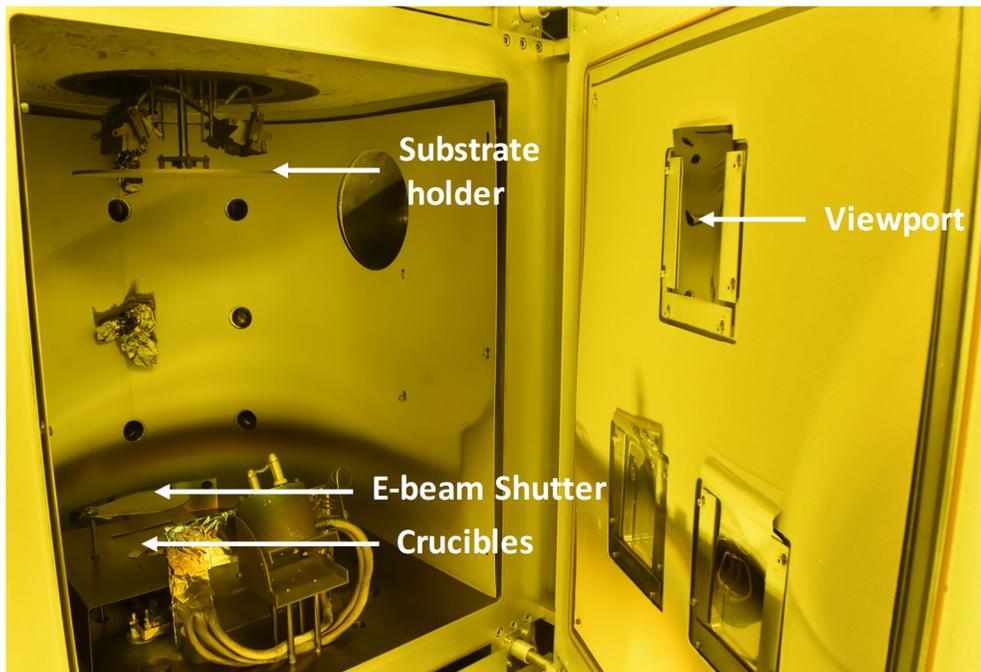
Fig. 3.18: A KJL PVD 250 E-beam evaporation system used in this work for thin film deposition

evaluated during this measurement process. After several runs there would be a situation when there are too many materials deposited onto the crystal and its resonant frequency has shifted by several percent. Then it is time to replace this relatively inexpensive crystal and ensure accurate deposition rate measurement through sharp change of resonance with a new crystal.

Kurt J. Lesker (PVD 250) e-beam evaporation tool is used in this work and is shown in Fig. 3.18 along with its various parts. The voltage is kept fixed at 7.5 KV and the current level is usually ramped up/down. The process starts with venting (injecting N_2 into the chamber) the chamber and bringing the chamber pressure to atmospheric level (760 mTorr). The sample is then attached with the substrate holder through high temperature adhesion tape and placed into the sample holder position located towards the upper side of the chamber. Evaporation material usually comes in the form of pellets and is loaded into the preconditioned crucibles and placed into the crucible holder situated towards the lower portion of the chamber. There are pockets for up to four crucibles to be loaded without breaking the vacuum in Kurt J. Lesker PVD 250 tool.

The chamber is then pumped initially through a roughing pump (from atmospheric level to $\sim 10^{-3}$ torr pressure) and later through cryopump down to ultra-low chamber pressure ($\sim 10^{-6}$ torr). Then the respective evaporation material source pocket is selected and corresponding parameters (density, z-ratio, tooling factor) are loaded into the crystal oscillator software interface system. The current is then slowly increased through a control knob and the crucible is then continuously monitored through an access window. The beam sweep function and longitudinal/lateral amplitude parameter can be tuned to control the desired area of crucibles to be heated through the e-beam. At this point the source shutter is opened, and the evaporating materials are let to be physically struck deposited onto the substrate on the upper portion of the chamber. The initial deposition rate is kept very low (~0.3 Å/s) by selecting relatively low current specially for the first few nm of film deposition as well as for deposition of adhesion layer. After deposition of 10-15nm film the deposition rate can be increased a bit specially for thicker film by increasing the current. The exact amount of current varies from material to material and usually large currents are required to evaporate high melting temperature materials. The deposition rate as well as the current film

thickness is continuously monitored. Once the desired film thickness is achieved the source shutter is closed and the current is gradually reduced to zero. Special care needs to be taken for low thermal conductivity evaporation sources and the current reduction rate needs to be slowed down accordingly to avoid unwanted thermal shock and crack of the materials/crucibles. There should

Table 3.2: E-beam deposition parameters for various thin films

Material	Cu	TaO$_x$	Pt	Ti	Cr	Ru	Rh	Ir	SiO$_2$
Thickness (Å)	1500	250	500	200	200	500	500	500	50
Melting temperature (^{0}C)	1085	1872	1768	1,668	1,907	2,334	1,964	2,466	1,710
Chamber base pressure (Torr)	2x10^{-6}	2x10^{-6}	1x10^{-6}	1.9x10^{-6}	9.2x10^{-6}	1x10^{-6}	1x10^{-6}	1x10^{-6}	0.5x10^{-5}
E-beam current (mA)	120	60	190	95	15	254	146	125	18
E-Beam deposition rate (Å/s)	0.7	0.5	0.5	0.4	0.3	0.3	0.3	0.4	0.5
Density (g/cm^3)	8.93	8.2	21.45	4.5	7.21	12.36	12.4	22.4	2.65
Tooling factor	140	140	140	140	140	140	140	140	140
Z-ratio	0.437	0.3	0.245	0.628	0.305	0.182	0.21	0.129	1

be few minutes of wait time to let the crucible cool down. Then the next crucible can be selected, and the process is repeated. Once the deposition of all desired materials is done, the chamber is vented and the sample as well as the crucibles loaded with materials are taken out. The chamber is then pumped down again and is usually kept under vacuum. To achieve a high deposition rate, the current can be set to high level, but it can compromise the quality and morphology of the deposited film. The best practice is to deposit at very low deposition rate as possible (through relatively low current level) with ultra-low chamber pressure ($\sim 10^{-7}$ mTorr).

Several thin films such as Cu, TaO$_x$, Pt, Ti, Cr, Ru, Rh, Ir and SiO$_2$ are deposited using e-beam evaporation in this work. The e-beam process parameters for all those thin films are summarized in Table 3.2.

3.3.5 Liftoff

Lift off is a technique to remove photoresist along with the materials deposited on top of that, while keeping the materials placed directly onto the wafer through the openings of photoresist defined by pattern transfer as designed. This is a material removal process from the selected area without employing sophisticated process such as dry etching, ion milling etc.

The lift off process starts with a desired thickness of photoresist spinning and patterning.
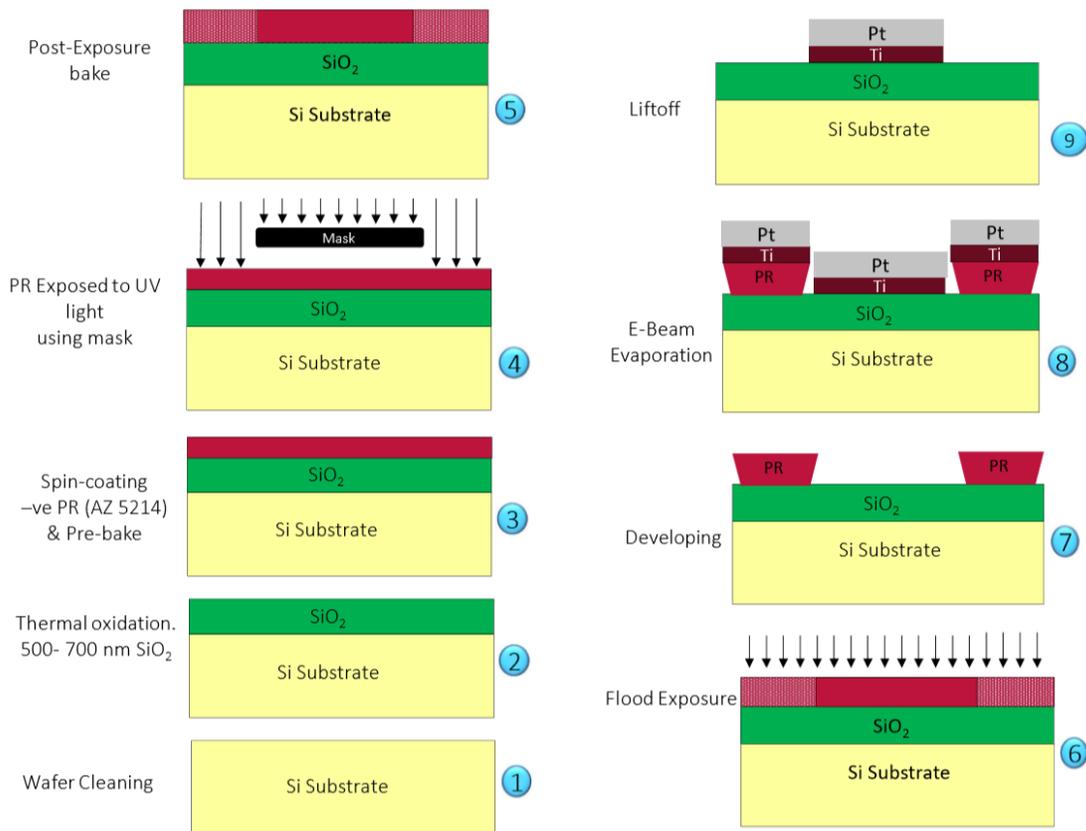
Fig. 3.19*: Complete process flow for fabrication of Cu/TaOx/Pt ReRAM memory cell*

Usually image reversal photoresist is a preferred pattern transfer material for subsequent lift off process due to its worthwhile undercut profile, which makes the lift off process much easier compared to other types of resists. Then a thin metal layer is deposited through a process which

characteristically offers advantageous poor step coverage specially with slight to almost no coating into the sidewall. Evaporation is a perfect choice for this no-isotropic deposition profile. The wafer is then submerged into a photoresist dissolving solution, such as acetone (CH_3-CO-CH_3). The undercut resist profile creates some opening and allows acetone to attack from the sideways. As the photoresist is dissolving into acetone, the metals deposited on top of photoresist lifts off the substrate in few minutes while the metals deposited directly on top of the substrate stays in place. Since there is no etching involved in this patterned metal transfer process, it is free from any etch related damage to the substrate. The patterned lines are also free from undercut and have infinite selectivity as well [9]. However, the lift off technology is limited to one metallization layer at a time and sputtering technique would not work with it. The lifted off materials can float within the solution and can potentially stick onto the wafer. It can also suffer from low yield issues. Lift off process is primarily suited for research and development.

Figure 3.19 shows step-by-step process flow to illustrate the entire fabrication process
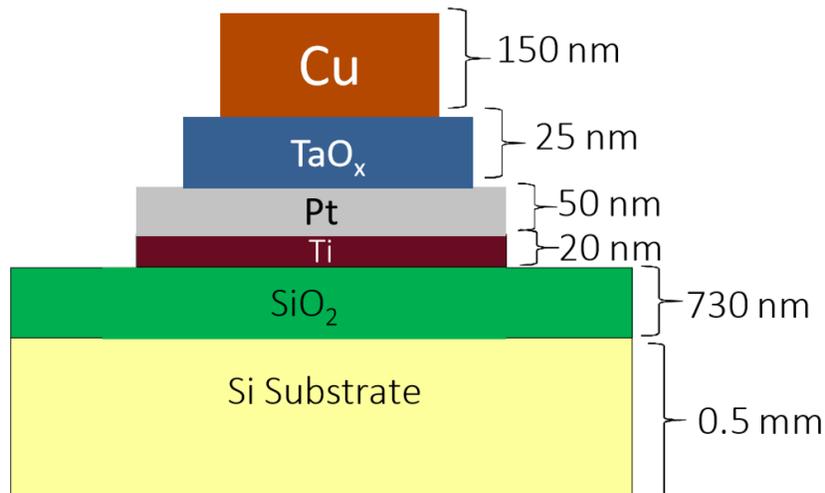
Fig. 3.20: Cross-section of a completed Cu/TaOx/Pt ReRAM memory cell with layer thickness specified

flow. The device cross section of a completed Cu/TaO$_x$/Pt device along with the thickness of various layers are shown in Fig. 3.20.

3.4. Fabrication of Polymer Memory Device

Wearable or bendable electronics is an emerging field which can be used in clothes, tents, watches, and even army suits. To ensure durability of these devices, these need to be flexible. By replacing the solid electrolyte layer in conventional ReRAM cell by switchable organic polymer material quasi-flexible memory device can be realized. The fabrication procedure of this quasi-flexible memory device is discussed here.

Like traditional ReRAM memory cell, bottom electrode is patterned and BE material is deposited using e-beam evaporation and photolithography on top of oxidized silicon substrate. The polymer layer is then spin-deposited. However, shadow mask is used to deposit top electrode material by avoiding liftoff technology.

○ 0.178 gm AA+ 3ml DMF+ 0.1 M HCL **A**

○ 0.08 M solution of ANI; $C_{AA}/C_{ANI}=5$ **B**   Definition of solutions A, B. and C

○ Prepare 50 ml solution of 0.1 M APS & 0.1 M HCL **C**

○ Mix solution A, B &C to get 0.013 mol/L AA
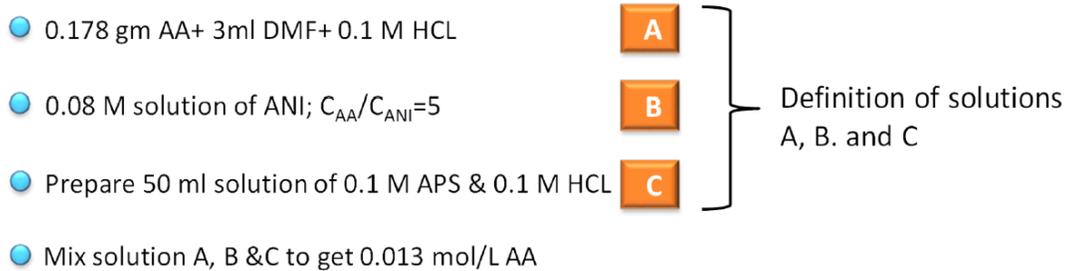
Fig. 3.21: *Summarized process flow for preparation of O-AA polymer solution [10].*

3.4.1   Organic Polymer

There have been a variety of organic polymers that have been explored by several researchers.   Each polymer had its own advantages and disadvantages. However, organic-anthranilic acid (O-AA) is used for this case due to its low-cost and superior device performance. O-AA based devices exhibit low switching voltages, high ON/OFF current ratios, and stable ON and OFF states in ambient condition without any device degradation even up to one year [10].

O-AA was prepared [10] by first mixing 3mL of DMF with 48.87 mL of HCl. This was then combined with 0.178g of AA. 3.3254 mL of ANI was then added to this mixture. A combination 10 mL of APS and 50 mL HCl was then added to the mixture to produce O-AA. Filter paper was then used to filter out any impurities in the solution. The filtered solution was then used

Table 3.3: amount of chemical used for O-AA solution

Reagents	Amount
AA (Anthranilic acid)	0.178 gm
ANI (Aniline)	3.245 mL
APS (Ammonium persulphate)	10 mL
DMF (N,N-Dimethylformamide)	3 mL
HCL	46.873 mL

as spin-coated polymer layer for the fabricated ReRAM device. The polymer preparation steps are summarized in Fig. 3.21. The amount of chemical used for the polymer preparation is also listed in Table 3.3.

3.4.2   Shadow Mask

A physical mask is first drawn using AutoCAD and then printed. This mask is then used to create a shadow mask consist of flexible and transparent plastic material. The electrode sizes are on the order of 10's of mm for visual convenience. Some alignment marks are also imprinted so that top electrode layer is properly aligned with bottom electrode and they are perpendicular to each other. Figure 3.22(a) and (b) shows the AutoCAD design for the shadow mask and the as-prepared shadow mask respectively.

Four devices have been fabricated where Cu/TaOx/Pt serves as the bench device. Then

(a)   (b)
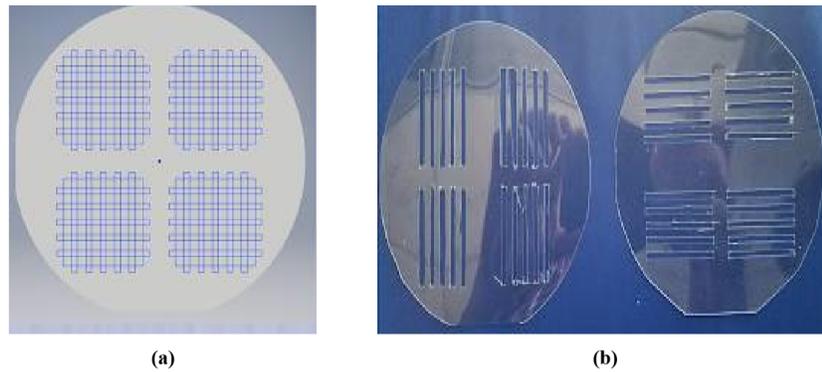
Fig. 3.22: *a) Designed mask using AutoCAD; b) As-prepared shadow mask*

(a)   (b)   (c)   (d)
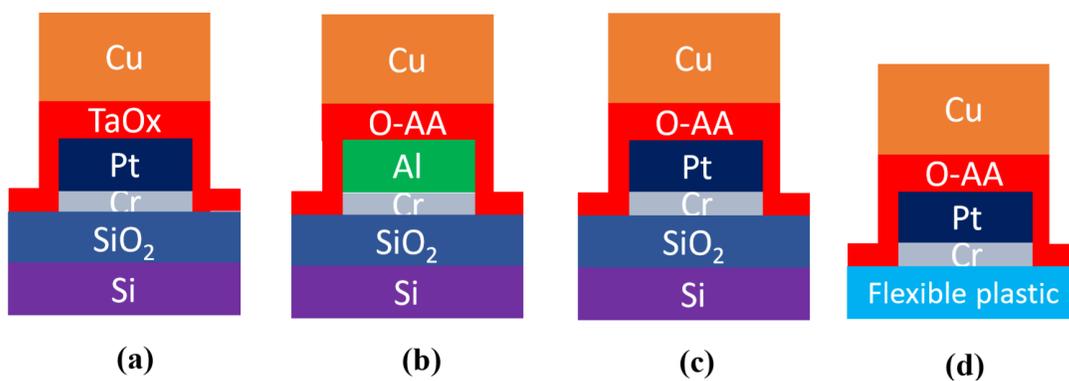
Fig. 3.23: *Cross section of fabricated devices: a) Cu/TaOx/Pt on Si; b) Cu/O-AA/Pt on Si; c) Cu/O-AA/Pt on Si; d) Cu/O-AA/Pt on Flexible plastic substrate*

178

gradually replacing one layer at a time the quasi-flexible ReRAM device are fabricated. The cross-section of the fabricated devices is shown in Fig. 3.23. The thickness of various layers is summarized in Table 3.4.

Table 3.4: Thickness of various layer of the fabricated devices shown in Fig. 2.22

Material	SiO_2	Cr	Al	Pt	O-AA	P3HT (PGN)	Cu
Thickness (nm)	750	20	50	50	600, 1200	700	150

3.5   Fabricated Inorganic ReRAM Devices

Several devices have been fabricated in this work with Cu/TaOx/Pt/Ti as the benchmark
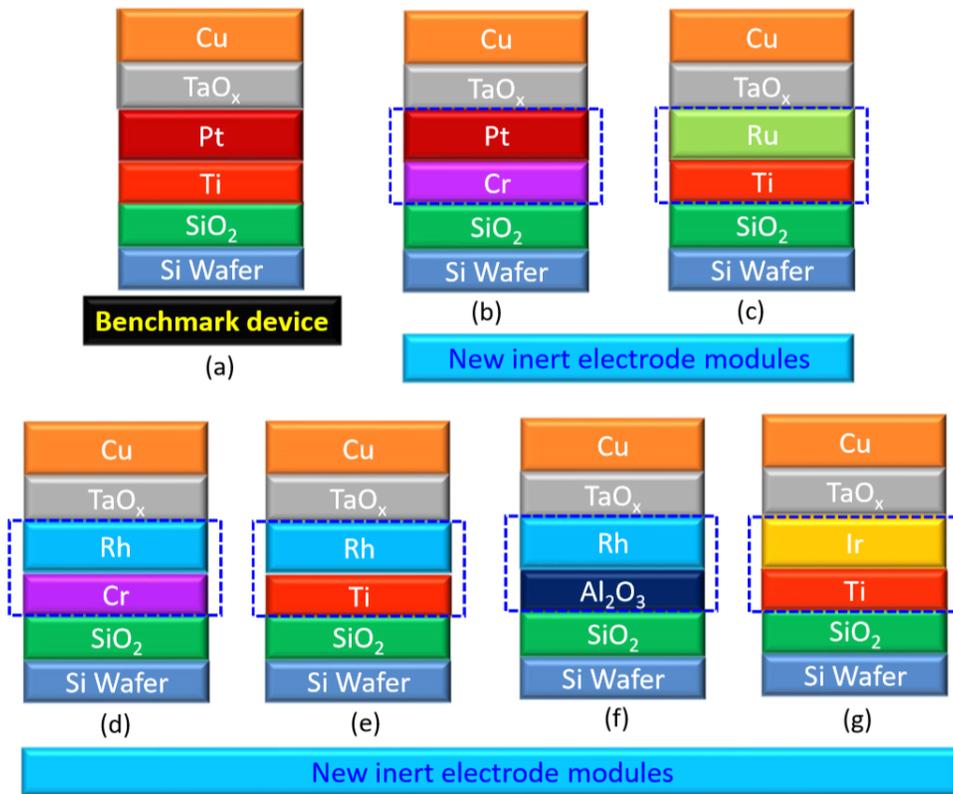
Fig. 3.24: *Cross section of fabricated devices: a) Cu/TaOₓ/Pt/Ti; b) Cu/TaOₓ/Pt/Cr; c) Cu/TaOₓ/Ru/Ti; d) Cu/TaOₓ/Rh/Cr; e) Cu/TaOₓ/Rh/Ti; f) Cu/TaOₓ/Rh/Al₂O₃; g) Cu/TaOₓ/Ir/Ti*

device for performance analysis and comparison of device performance. Then $Cu/TaO_x/Ru/Ti$,

$Cu/TaO_x/Rh/Ti$ and $Cu/TaO_x/Ir/Ti$ devices are fabricated. Later, adhesive layer Ti is replaced

with Cr and devices such as $Cu/TaO_x/Pt/Cr$, $Cu/TaO_x/Rh/Cr$ as well as $Cu/TaO_x/Rh/Al_2O_3$ are

 fabricated. The cross-section of all fabricated devices is shown in Fig. 3.24. All the devices are

on oxidized silicon wafer.

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Chapter 4: Investigation of Cu/TaO$_x$/Ru based ReRAM memory cell

4.1   Introduction

The resistive switching (RS) device has lately been of great attention to both industry and academia as a potential replacement for volatile dynamic random-access memory (DRAM) and nonvolatile flash technologies that are nearing the end of their dimensional scaling roadmaps [1-9]. These two-terminal devices have figure eight-like pinched current–voltage (I–V) hysteresis switching between a high resistance R$_{OFF}$ (OFF state) to a low resistance R$_{ON}$ (ON-state) with memristive characteristics [2, 3]. Conductive Bridging Random Access Memory (CBRAM), also referred as Programmable Metallization Cell (PMC), is a promising candidate for a resistive memory device due to its highly scalable and low-cost technology [10]. CBRAM memory is being extensively explored as a promising contender for a resistive memory device [11]. Building nonvolatile memory (NVM) directly into a CMOS low-k/ Cu interconnect module would reduce latency in connectivity constrained devices and reduce chip's footprint by stacking memory on top of the logic circuits [12]. Large-scale integration of metal-oxide filamentary memory with a selector device based on 1T1R architecture has been reported [13,14]. Low-k dielectrics and Cu metal lines prefigure a potential ReRAM cell, and the cross-bar architecture of a typical two-terminal RS device array is essentially the same as a CMOS metal interconnect system. Thus, the interconnect information bottleneck could be untied and morphed into several system architectures using the same device platform.

One strong candidate for non-volatile memories is the well-behaved and well characterized $Cu/TaO_x/Pt$ resistive switching device due to excellent unipolar and bipolar switching characteristics, device performance, retention, reliability [15]. This device can be operated as a memory cell with copper (Cu) or oxygen vacancy (V_o) conductive filaments. However, since platinum (Pt) is not an economic choice for industrial production and has been not used in back-end-of-line (BEOL), a BEOL-compatible replacement of Pt is highly desirable. A good candidate for a replacement of Pt is ruthenium (Ru) which has been already deployed in the CMOS BEOL supplanting Ta or TaN as the liner material [16, 17]. Ru is ca. 45 times less expensive than Pt, and has similar properties as Pt.

Pt and Ru are both transition metals with almost identical outer shell structure: Ru has one electron in the fifth orbital and 15 electrons in the fourth orbital, while the larger Pt atom has one electron in the sixth orbital and 17 electrons in the fifth orbital. Ru has a relatively large work function of 4.7 eV compared with 5.1-5.9 eV for Pt. The melting temperature of Ru, $T_m(Ru) = 2334^o\,C$, is lower than that of Ta, $T_m(Ta) = 3017^o\,C$, and Ru has an electrical resistivity half that of Ta, Ru: ρ_{bulk}=7.1 $\mu\Omega.cm$ vs Ta: $\rho_{bulk} = 13.5$ $\mu\Omega.cm$, while Cu resistivity is still lower, at ρ_{bulk} =1.7 $\mu\Omega.cm$. In addition, the Ru-Cu phase diagram shows negligible solid solubility between the two elements, even at $900^o\,C$, rendering Ru an excellent inert electrode for Cu ions. [18]. Moreover, Ru is ca. 45 times less expensive than Pt, and has similar properties as Pt. Based on these considerations, a $Cu/TaO_x/Ru$ device appears promising.

The first part of this chapter discusses in detail the similarities and differences between the $Cu/TaO_x/Ru$ and $Cu/TaO_x/Pt$ devices using the latter one as a bench-mark for the Ru device performance assessment. The electric characterization of both devices has shown many similarities and some notable differences. Compared with $Cu/TaO_x/Pt$ device, $Cu/TaO_x/Ru$ device shows less

reliable set and reset switching characteristics due to the different formation, shape and rupture of the conductive filament.

4.2   Device Fabrication

The ReRAM devices based on crossbar array architecture are fabricated on a thermally oxidized Si substrate with a SiO_2 thickness of 730 nm. Both metal electrodes and oxide (solid electrolyte) were deposited by electron beam evaporation and patterned by lift-off technology. A thin Ti layer of 20 nm was used between Ru and SiO_2 to improve the adhesion of the Ru layer. The thickness of TaO_x was 25 nm. The width of metal lines varies between 5μm and 35μm
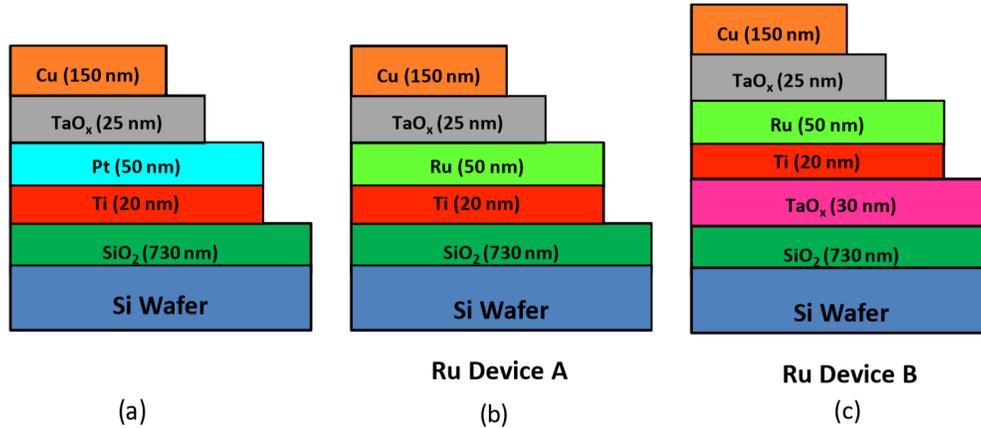
Fig. 4.1: *Device cross-section of a (a) Cu/TaOx/Pt resistive switching device; (b) Cu/TaOx/Ru resistive switching device A; (c) Cu/TaOx/Ru resistive switching device B (with TaO_x diffusion barrier layer)with layer thickness specified*

resulting in rectangular areas of the device in the range of (5 to 35) x (5 to 35) μm^2. The distance between the metal lines is 150 μm. All metal layers (Cu, Ru, Ti) were deposited by Physical Vapor Deposition (PVD) in a Kurt Lesker e-beam PVD-250 chamber. I–V characteristics were measured by a Keithley 4200-SCS at room temperature. The oxygen-deficient TaO_x (x≈1.9) was deposited also in the PVD-250 chamber by evaporating Ta_2O_5 pellets without O_2 injection into the

evaporation chamber. Figure. 4.1(a), 4.1(b) and 4.1(c) show the cross-section view of $Cu/TaO_x/Pt$, $Cu/TaO_x/Ru$ device A and $Cu/TaO_x/Ru$ device B resistive switching devices, respectively, with layer thicknesses specified. Moreover, nominally identical Ru devices have been embedded on two different substrates: while Ru device A is manufactured on $Ti(20nm)/SiO_2(730nm)/Si$, i.e the same substrate used for the Pt device, the Ru device B is defined on the $Ti(20nm)/TaO_x(30nm)/SiO_2(730nm)/Si$ substrate as shown in Fig. 4.1(b) and 4.1(c) respectively. Here, the additional 30 nm thick TaO_x layer, deposited by e-beam PVD, has been inserted between SiO_2 and Ti layers, i.e. outside of the device proper. Although, the additional TaO_x layer outside of the cell proper should not, in principle, impact the cell's electrical properties, it is found that it has a major impact on them, indicating that the embedment of the resistive cell is an important factor in the cell's overall performance [19].

4.3   Characterization Methodology

Both $Cu/TaO_x/Pt$ and $Cu/TaO_x/Ru$ devices have been subjected to the standard resistive switching characterization described in more detail in [20]. The voltage is being ramped starting at 0 V on the positive (or negative) bias axis while the current is being monitored. At a critical voltage V_{SET}, the current increases very rapidly indicating that the device became highly conductive. Usually, lest the device be damaged, a compliance current I_{cc} is applied to limit the current flowing through the device. The level of I_{CC} determines in many instances the nature of the filament and the value of the on-state resistance, R_{ON}, via the relation $R_{ON} \sim 1/I_{CC}^n$ [20]. Then the voltage is ramped down, the device displays an ohmic behavior of the on-state and characterized by R_{ON}. When the current at negative bias reaches a critical current I_{RESET} at V_{RESET}, the conductive state is ruptured and the device reverts to the off-state characterized by a high, off-

state resistance, R_{OFF}. I-V characteristics of resistive Cu/TaO$_x$/Pt devices were measured by a Keithley 4200-SCS (Semiconductor Characterization System). In our measurements, the bottom electrode is grounded and the bias voltage is applied to the top Cu electrode. When positive voltage with appropriate magnitude is applied to the top electrode, Cu cations are generated at top-electrode/solid elctrolyte interface, dissolve in the oxide layer and can migrate through the solid electrolyte. When these cations reach inert electrode (bottom electrode), they are electrochemically reduced on the Ru cathode. As more and more Cu atoms aggregate over time at the TaO$_x$/Ru or TaO$_x$/Pt interface, a nanoscale filament forms a conductive path between two electrodes.

4.4 Switching Characteristics of Cu/TaO$_x$/Ru Device

The Cu/TaO$_x$/Ru devices have been characterized in the same way as the Cu/TaO$_x$/Pt devices and is discussed in detail in chapter 2. Table 4.1 gives the range of Form voltages and LRS (R_{ON}) of CFs for different Cu/TaO$_x$/Ru devices under I_{CC} = 10 μA and voltage sweep rate rr = 2 V/s. The following distributions are found: for V_{FORM} a mean $V_{FORM, m}$ = 7.3 V and a standard deviation of σ = 0.7V, for V_{SET} a mean $V_{SET, m}$ = 4.4 V, and standard deviation, σ = 0.9 V.

Table 4.1: Typical Form voltage and On-resistance of Cu/TaO$_x$/Ru devices

Device	V_{form} (V)	R_{on} (Ω)
Sample 1	7.6	15,432
Sample 2	7.5	12,050
Sample 3	6.9	13,260
Sample 4	7.8	10,868
Sample 5	7.2	11,845

Compared with Pt devices, Ru devices have significantly higher forming voltage (by 2.0 - 2.5V) while the on-resistance is very similar and appears to be controlled only by the compliance current. The rupturing of the CF is triggered mainly by Joules heating at a critical current $I_{RESET} = V_{RESET}/R_{ON}$. The V_{RESET} distribution of the Cu/TaO$_x$/Ru devices is characterized by $V_{RESET, m}$=-3.4 V and $\sigma = 0.7$ V. Thus, all the critical voltages of the Ru devices are considerably higher than of Pt devices: $\Delta V_{FORM} = 2.7$ V, ΔV_{SET}=1.6 V and $\Delta V_{RESET} = 2.5$ V. For V_{FORM} and V_{SET}, part of the difference can be explained by the difference of work function between Pt and Ru of 1.65 eV, which agrees remarkably well with the differential for set voltages, $\Delta V_{SET} = 1.6$V. In the set operation, only the gap in the ruptured filament has to be closed to restore the filament. The built-in field in case of Pt electrode is the work function difference between Pt and Cu divided by the thickness of the TaO$_x$ dielectric, which in case of Pt devices comes to a quite high field of 6.8×10^5 V/cm. This field favors Cu$^+$ ion transport toward the Pt electrode. The corresponding built-in field in case of Ru devices is 6×10^4 V/cm, i.e. one order of magnitude lower than for the Pt device. The field responsible for the formation of the Cu filament in its final stages has been estimated to be $(1-2) \times 10^6$ V/cm [21]. The calculation of the effective fields at V_{SET} for Pt and Ru including the built-in potential, are, indeed, in this range and approximately the same:

$$\frac{[\frac{\Delta\phi(Pt, Cu)}{q} + Vset, m(Pt)]V}{25nm} \approx \frac{[\frac{\Delta\phi(Ru, Cu)}{q} + Vset, m(Ru)]V}{25nm} \approx 1.8 \times 10^6 V/cm$$

Which is in excellent agreement with [21]. The higher delta in V_{FORM} for both devices of 1.1 V in excess of 1.6V of the work function difference could be explained by lower nucleation rate of Cu on Ru than on Pt. This would also indicate that there is higher surface diffusion of Cu on Ru than on Pt. The difference between V_{RESET} voltages of 2.5 V cannot be explained by the work function

difference between Pt and Ru, as the main mechanism of the dissolution of the conducting filament is the Cu atom out-diffusion at high temperatures near the filament constriction. The higher reset voltage for Ru devices is discussed in more detail below which appears to be tied to the issue of Ru inertness and integrity. The high built-in field for the Pt device has been verified experimentally in the following way. The Pt and Ru devices are set under three different I_{CC} conditions of 10, 50, and 100 µA and subsequently the devices are reset. During the reset the ruptured gap in the filament is estimated to be ~ 5-7 nm. This means that the built-in field in the gap would be for Pt devices 1.65V/7nm=2.4 ×10^6 V/cm and for Ru devices 0.1V/7nm=1.4×10^5 V/cm. Therefore, the built-in
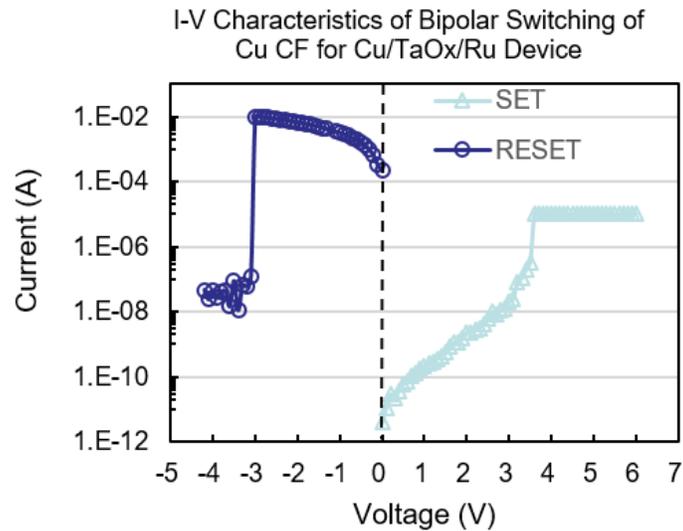
Fig. 4.2: The bipolar switching of set and reset operation for a Cu/TaO$_X$/Ru device on a logarithmic current scale with V_{SET} = 3.8V and V_{RESET} = -3.1V.

field for Ru devices is more than one order of magnitude lower than for the Pt device. The built-in field for Pt device is high enough to spontaneously set the device. Indeed, experimentally we

observe a spontaneous setting on a large fraction of devices after a wait time of 48 h (i.e. when the device is at 300K) that initially has been set at I_{CC}=10 µA and occasionally for those set at

I_{CC}=50μA. No spontaneous setting of the devices has been observed for I_{CC}=100 μA. Not a single instance of spontaneous setting of the devices has been observed for the Ru devices tested at the same conditions. Spontaneous set operations have been also observed during consecutive switching cycles of a Pt device. During the repeated switching cycle test it was observed that after a 5th reset operation, the device was ON spontaneously, after a time of the order of tens of seconds. Here, the spontaneous formation capability of the CF has been augmented by the elevated local temperatures in the cell caused by the Joules heat dissipation leading to higher rate of Cu ionization and higher Cu^+ ion electromigration mobility. This is another confirmation of the impact of work function difference between the active and inert electrode.

In Figure 4.2, a typical set and reset bipolar operation for Cu CF in Cu/TaO$_x$/Ru device is shown. The V_{SET} = 3.5 V at I_{CC} = 10 uA and V_{RESET} = -3 V. The bipolar switching cycles have been repeated on Cu/TaO$_x$/Ru devices. We observe that most of Cu/TaO$_x$/Ru devices is becoming not resettable after few set-reset operations. The failure of the Ru devices after a few switching cycles is likely to be related to the geometrical shape of the Cu filament.

As in the case of Pt devices, R_{ON} for Ru devices also depends on the compliance current, I_{CC}. On a double logarithmic scale, it can be seen that R_{ON} also decreases linearly with increasing I_{CC} conforming to the eq. (1) below:

$$Ron = \frac{A}{I_{cc}{}^n} \qquad\qquad (1)$$

As is shown in Fig. 4.3(a), the extracted parameters are A = 0.61 V and n = 1.08. The condition for the set operation is: voltage sweep rate rr = 0.2 V/s. It can be concluded that Cu/TaO$_x$/Ru devices have slightly higher constant A value than Cu/TaO$_x$/Pt device when the set operation is

the same (rr = 0.2 V/s). As shown elsewhere [22] with the exponent of I_{CC} in the denominator being close to 1, the constant A of 0.5 V (for Pt device) and 0.61 V (for Ru device) can be interpreted as the lowest possible V_{SET} voltages under which the Pt device and Ru device, respectively, can be set at a given voltage ramp rate. Lowest value for the constant A can be reached as a limiting case for very slow voltage ramp rates. The difference in the minimum set voltage extracted from R_{ON} - I_{CC} characteristics confirms that the V_{SET} voltage for Ru devices is higher than for Cu device.

Previous work has shown [23] that Cu and vacancy conductive filaments can be
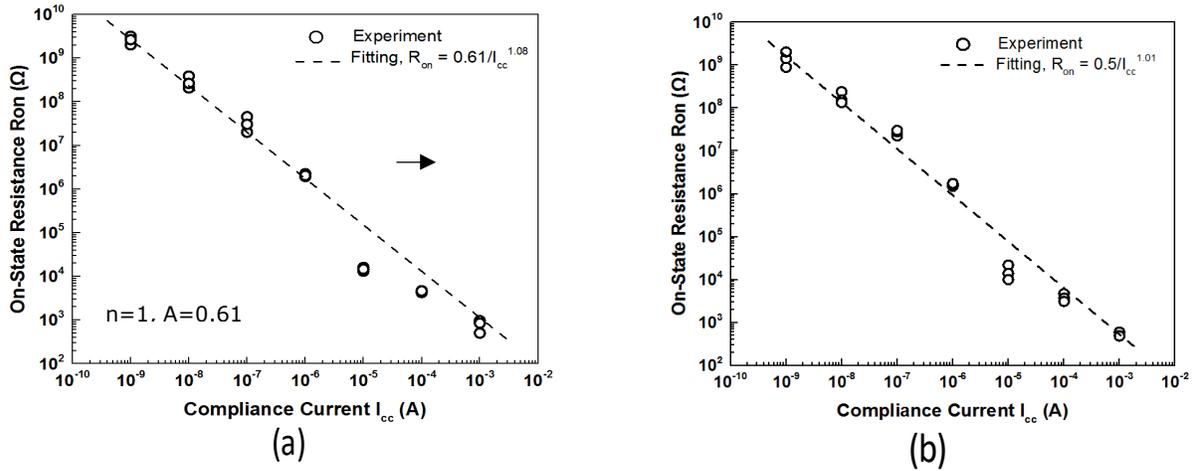
Fig. 4.3: *Dependence of on-resistance, R_{ON}, on compliance current, I_{CC}, for the (a) Cu/TaO$_X$/Ru device @ rr =0.2 V/s; (b) Cu/TaO$_X$/Pt device @ rr =0.2 V/s.*

distinguished by their temperature coefficient of resistance (TCR) or α as defined by

$$R(T) = R(T_0) \times [1 + \alpha(T - T_0)] \qquad (2)$$

Since in Pt and Ru devices the filament is made of Cu atoms similar temperature coefficients of resistance is expected. Here the TCR from resistance measurements of the on-state is extracted as

190

a function of temperature and is also shown in Fig. 4.4(a) and 4.4(b). It is found that TCR (Ru-device) = 0.00236 K^{-1} and TCR(Pt-device) = 0.00235 K^{-1} for almost the same values of $R_{ON} \approx 15$ kΩ, at the same set conditions I_{CC}=10 μA. Within the accuracy of this measurement these values
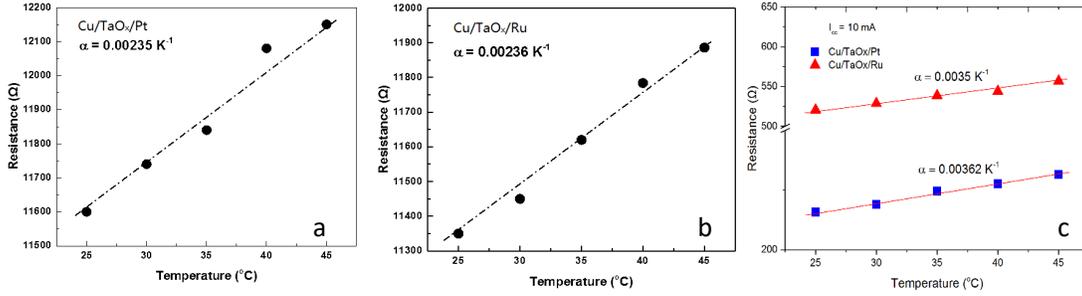
Fig. 4.4: *On-resistance, R_{ON}, of the Cu filament of Cu/TaO$_X$/Pt and Cu/TaO$_X$/Ru for set operation at different I_{CC} levels: (a) Cu CF for Pt devices @ I_{CC} = 10 μA; (b) Cu CF for Ru devices @ I_{CC} = 10 μA; (c) Cu CF for Pt and Ru devices @ I_{CC} = 10 mA. The extracted temperature resistance α coefficient is indicated.*

are identical. The same measurements have been repeated for a different set conditions at three orders of magnitude higher I_{CC}, I_{CC}=10mA. For I_{CC}=10mA, much lower R_{ON} for the filaments 510 Ω for Ru and 230 Ω for the Pt device is obtained. It has been observed that for both devices TCR increases with decreasing R_{ON} reaching a value of 0.0035 K^{-1} at R_{ON}= 300 Ω as seen in Fig. 4.4(c). These values are typical of strong Cu filaments (for comparison the TCR of bulk Cu is 0.0039-0.004 K^{-1}). Therefore, it can be concluded that under a positive voltage stress applied to the Cu electrode, Cu conductive filaments are formed in both devices. Moreover, these values are consistent with TCR values of Cu CFs observed in many other devices.

To summarize the characterization of Ru devices one can state that with the proviso that all critical threshold voltages, V_{FORM}, V_{SET}, and V_{RESET} are higher than for Pt devices which can be partly understood in terms of work function difference between Pt and Ru, Pt and Ru devices behave very similarly. There are, however, two major differences: (i) V_{RESET} is much higher in Ru

than in Pt devices, and (ii) the maximum number of set-reset cycles for Ru is substantially lower than for Pt devices, particularly when the devices are set at I_{CC}>100µA, i.e. for low R_{ON}. These two issues are discussed in detail in the subsequent sections.

4.5   Limited Switching Cycles of Cu/TaO$_x$/Ru Devices

The major drawback of the Ru device is that while Pt devices can be switched repeatedly back and forth, Ru device are becoming non-resettable after several set-reset operations and sometimes even after the first set operation when the set operation is performed at high I_{CC}. In some cases, it was even difficult to reset a weak Cu filament in a Ru device formed at I_{CC} as low as 5 µA. The failure of the Ru devices to switch after several switching cycles is likely to be related to the geometrical shape of the Cu filament.

It is known that even in Pt devices, it is difficult and sometimes impossible to reset the cell if the cell has been set at high I_{CC}. This phenomenon may be explained by different geometrical shape of the filament. For low I_{CC} the shape of the CF can be approximated by a truncated cone as shown in Fig. 4.5(a) where the bulk of the CF's resistance resides in the tip of the cone. This is also the locus of the Joules heat deposition according to $\int_0^{V_{reset}/rr} \frac{rr^2 \times t^2}{R_{ON}} dt$ [24]. Since during the reset the power dissipated in the filament is equal to $I_{RESET}^2 \times R_{ON}$, the highest temperature is reached in the constriction at the tip of the cone, where the rupturing of the filament is easy, as shown in Fig. 4.5(a). At high I_{CC} (as seen in Fig. 4.3, R_{ON} vs I_{CC}) the R_{ON} decreases sharply by adding Cu atoms to the upper section of the cone. Therefore, the shape of the filament becomes more and more cylindrical as shown in Fig. 4.5(b). In this case, the maximum temperature, in absence of any pronounced constriction, is reached in the middle section of the cylinder, where the

192

low resistance filament is relatively strong. Hence, rupturing of the CF becomes difficult or impossible.

The cylindrical shape of the CF may be also obtained if the base of the cone in contact with Ru electrode is eroded, see Fig. 4.6(a). As the bottom base of the CF is reduced while new Cu^+ ions are added from the top during the set operation, the shape of the filament will tend to become
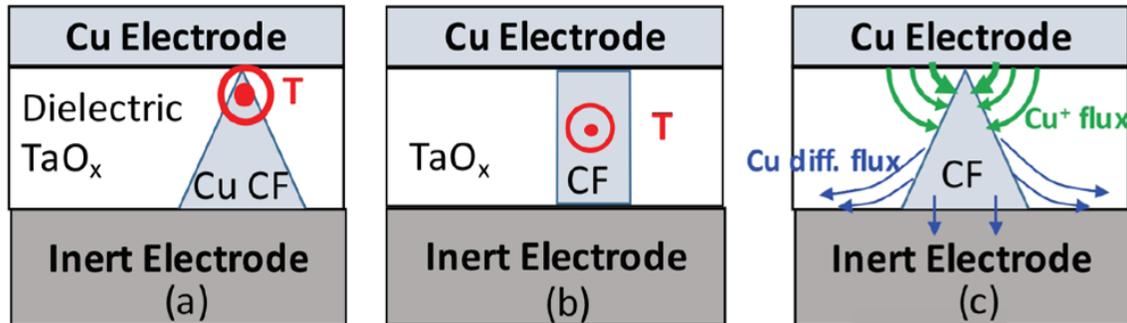
Fig. 4.5: *(a) Location of the highest temperature due to the Joules heating during reset operation. (b) cylinder-like shape of the filament with maximum temperature in midway between the electrodes. (c) Cu conductive filament with a sharp constriction at the Cu electrode interface with Cu constructive (Cu^+ ion electromigration) and destructive (Cu out-diffusion) fluxes responsible for the shape of the CF.*

cylindrical. There are several possible mechanisms for the erosion of the base of the cone: (i) Cu surface diffusion along the Ru interface to which has been alluded before in the context of the much larger V_{FORM} for Ru than for Pt devices, (ii) crystallization of Ru and out-diffusion of Cu along the Ru grain boundaries, (iii) Cu and Ru chemical reaction with oxygen and/or with Si.

Ru surfaces, which contributes to the excellent electroplating properties of Cu on Ru. Ru has a fairly high surface energy of 1.28 eV when compared with the surface energy of Cu (0.69 eV) and of Pt (0.98 eV) [25, 26]. Based on these reported values the wetting and also Cu adatom diffusion on Ru is expected to be significantly higher than on Pt surfaces. The higher interfacial diffusion of Cu on Ru than on Pt surfaces is likely to be responsible for lateral Cu transport at the

bottom of the filament as shown in Fig. 4.6 (a). The lateral Cu diffusion could create a broad base of the filament and might also be responsible for the shape of the filament to adopt a more cylindrical form.

To keep the R_{ON} constant, the loss of Cu atoms at the base of the cone has to be

$$R_{on} = \frac{\rho \cdot h}{\pi \cdot a \cdot b}$$

(a)   (b)
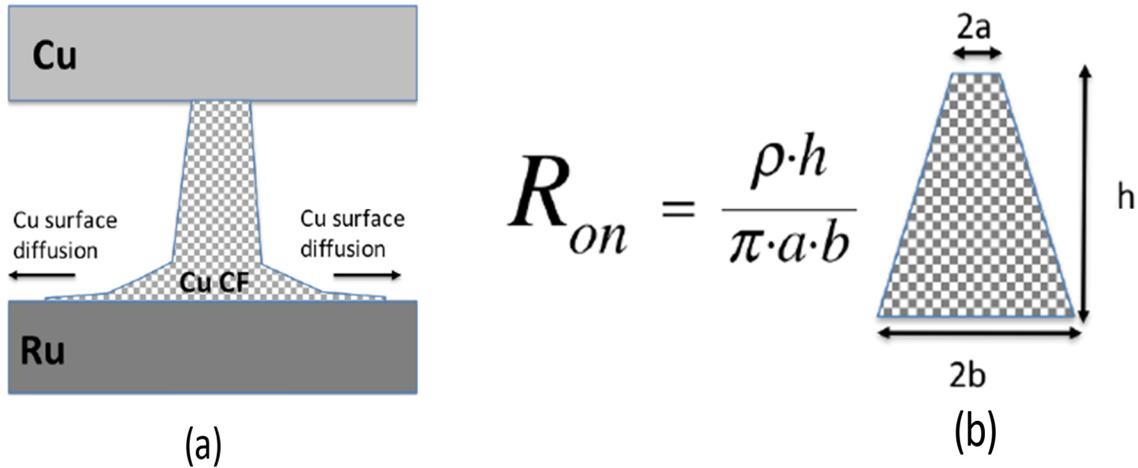
Fig. 4.6: (a) Hypothesized geometrical shape of Cu conductive filament structures for Cu/TaO$_X$/Ru device with a degraded base at the TaO$_X$/Ru interface, (b) Truncated cone shape of a conductive filament with the equation (eq'n (2)) for on-state resistance, R_{on} for a truncated cone geometry.

compensated by additional flux of Cu$^+$ ions explaining the need for higher forming voltages in Ru devices in excess of the work function difference of 1.6 V. Whereas, with a nearly perfect stopping power, the shape of the filament in the Pt device can be assumed to be conical with more or less sharp tip at the Cu electrode, the shape of the Cu filament in the Ru device is more cylinder-like especially if the Ru device is undergoing several set-reset switching cycles. These mechanisms appear to be very similar to the properties of Cu/TaO$_x$/Ta devices observed in [27].

The on-resistance of a conically shaped resistor is given by:

$$R = \rho \frac{h}{\pi a b}$$

(3)

194

where h is height, a is the radius of the truncated cone base at the top, b the radius of the base at the bottom, and ρ is the specific resistivity of the filament, see Fig. 4.6(b). To demonstrate the difference between the hypothesized shapes for the Cu CF for the Pt and Ru device, two cone shapes have been constructed with the same overall CF resistance, R_{ON}: the following parameters for the Pt device is assumed $b_{Pt} = 3$ nm and $a_{Pt} = 0.5$nm and for Ru device $b_{Ru} = 1.76$ nm and $a_{Ru} = 0.85$ nm, for a common height h=25 nm. Based on eq'n [3], the resistances of Cu CFs for Ru and Pt devices are 15,966 Ω and 15,923 Ω respectively, which are almost the same values shown in Fig. 4.3(a) and Fig. 4.3(b) when the devices are set at $I_{CC} = 10$ μA. Here, the resistivity of copper filament has been assumed to be $\rho=300\times10^{-6}$ Ω·cm [28].

4.6   Impact of Embedment of Cu/TaOx/Ru on its Device Performance

In [29, 30] the electric performances of Cu/TaO$_x$/Ru and Cu/TaO$_x$/Pt devices have been compared. It was found that the performance of the Ru device is far inferior to that of the Pt device. The result was surprising as both Pt and Ru are known to be excellent diffusion barriers for Cu in CMOS backend applications. The poor resistive switching (RS) properties of the Ru device have been imputed to the greatly degraded inertness properties of the Ru electrode as a stopping barrier for Cu drift-diffusion. The degraded inertness of the Ru electrode, in turn, can be attributed hypothetically to several factors, discussed below. The electric performance of two nominally identical Cu/TaO$_x$/Ru devices however differently embedded on the Si wafer as shown in Fig. 4.1(b) and 4.1(c) has been compared in detail in the next section. The surprising finding is that the electric and RS behavior of the two identical devices but on different substrate layers is markedly different. Apparently, different embedment of nominally identical RS devices has a major impact on the intrinsic device performance. In [30] three possible reasons for this disparity

195

have been identified. First, the layers of Ti and Ru involved are very thin (10 nm and 50 nm). Second, during resistive switching the local temperatures at the filament both during the form/set and in the reset operations can exceed 600° C [28] i.e. far higher than the maximum temperature to which the CMOS backend may be usually exposed when the underlying processor is in operation. This temperature is estimated to be around 120° C. Indeed, up to 120° C and a little too high above, amorphous Ru appears to remain an excellent diffusion barrier for Cu. The third reason is the crystallinity phase of Ru thin layers depends on the deposition method and the subsequent 'accidental', i.e. related to the RS switching behavior, local anneals.

In [29] it was found that the Ru device(A) can be switched a limited number of times at a high compliance current I_{CC} (~ 0.5 mA) while the device (B) at such I_{CC} levels shows either volatile filament formation or when a filament forms, it cannot be reset. Conversely, at I_{CC} of $\sim$ 5mA Ru device (B) shows fairly good RS behavior, while Ru device (A) shows mostly volatile behavior. The I_{CC} level is not the only critical parameter. The other important parameter is the applied ramp rate rr during the voltage sweep. Both parameters determine the thermal budget during the set and reset operations and are thus responsible for: 1) chemical reactions taking place between the thin metal and dielectric layers and chemical compounds that result from it. 2) impacting Cu surface diffusion on the Ru electrode and Cu penetration through the Ru electrode which appears to include compounds such as Ru_2Si_3 and Cu_3Si in case of Ru device A. The purpose of inserting TaO_x layer between SiO_2 and Ti is to prevent possible silicidation reactions. Indeed, there are many reports in the literature on a number of issues related to Ru: a) thin Ru amorphous films crystallize into a polycrystalline phase at about 550° C [31]; b) observation of a strong diffusive penetration of Cu through the Ru layer was observed at 475° C [32]; c) Ru silicide formation at 350° C [33]; d) Cu silicide is formed at 200° C [34].

Because of the chemical reactions triggered by the local high temperatures caused by RS switching behavior, the Ru devices show different properties over the stable Pt devices. In contrast to Pt devices, the voltage ramp rate has a major impact on the resistance of the on-state, R_{ON}, in the Ru devices: lower ramp rate leads to a higher R_{ON} values because the forming filament is exposed for a longer time to elevated temperatures and suffers from Cu out-diffusion. The observation that R_{ON} in Ru device (A) is significantly higher than in the Ru device (B) at the same I_{CC} and rr values, demonstrates that Ru in Ru device (B) has superior inertness properties over the Ru device (A). In summary, there are several factors that can affect Cu agglomeration on Ru: 1) Cu penetration into Ru electrode either to intrinsic miscibility of Cu in Ru at elevated temperatures, or diffusion of Cu into grain boundaries in case of poly-crystallinity of the Ru electrode, or Cu diffusion into Ru_xSi_y silicide, or finally Cu absorption into Cu_xSi_y silicide. 2) larger Cu surface diffusion at the Ru interface than at the Pt device.

Another issue came to the fore when identical devices $Cu/TaO_x/Pt$ and $Cu/TaO_x/Ir$ have been implemented with different glue layers as shown in Fig. 4.7. In case (a) of Fig. 4.7, a Ti glue layer has been used, and a Cr layer in case (b). It was found that the electric performance of nominally identical devices depended sensitively on the glue layer. The impact of the glue layer showed up most dramatically in the stability of the filaments formed at low I_{CC} values. While devices manufactured with Ti glue layer showed volatile behavior, meaning that the filament dissolved spontaneously after the device have been set and unpowered, devices manufactured with Cr glue layers showed non-volatile, stable behavior. The difference in the electric performance is attributed to the difference in the Joules heat generated in the Cu CF during operation of the cell between V_{SET} and end-voltage of the ramp and during the reset operation. The heat conductivity

197

of Ti [22 W/(m.K)] is much smaller than of Cr [94 W/(m.K)] as shown in Table 2.1 in chapter 2. Therefore, in case of Ti the local temperature of the filament may be higher than in case of Cr glue layer and also the heat may linger for a longer time in case of Ti than in case of Cr. It is seen that thermal conductivity of Cr is more than 4 times larger than that of Ti. The case of Pt on Ti is particularly disadvantageous since the thermal conductivity of Pt is 72 W/(m.K) and of Ti 22
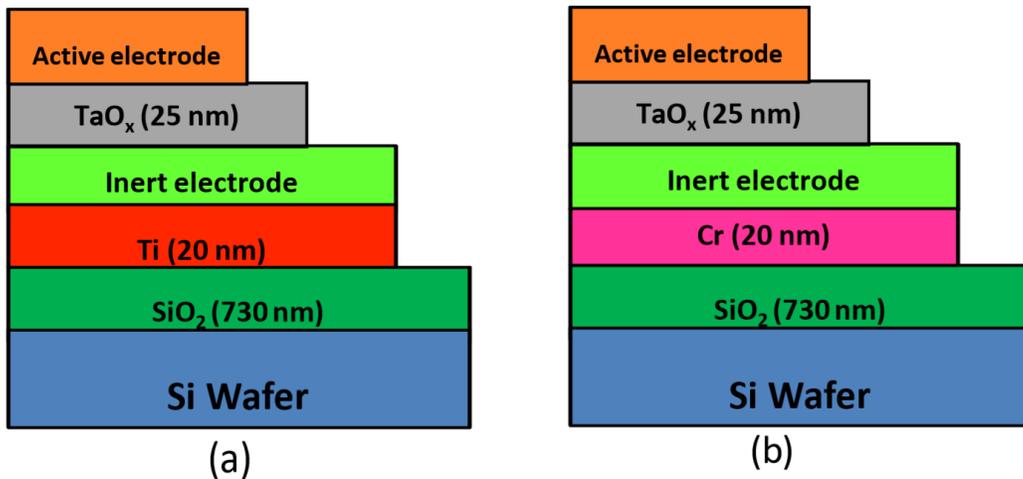
Fig. 4.7: Identical devices with two choices for inert electrode, Pt and Ir, with different glue layers: (a) Ti 20 nm, and (b) Cr 20 nm. The otherwise identical devices of (a) and (b) display different electric performance.

W/(m.K). The Joules heat generated in the filament cannot be easily dissipated and lingers therefore for some time around the hot spot in the filament. The thermal conductivity of Cu is excellent but the contact area between the cone-shaped filament at the tip of the filament is very small compared with the large contact area of the base of the cone with the inert electrode (see Fig. 4.5). A combination of Rh with 150 W/(m.K) with Cr 94 W/(m.K) in terms of heat conduction looks particularly promising. Therefore, for Rh/Cr composite inert electrode, heat dissipation should be much higher than in the case of Pt/Ti. Indeed, first tentative results indicate that such a

device (Cu/TaO$_x$/Rh/Cr) shows excellent resistive switching characteristics [35]. Another attractive candidate for a composite inert electrode from the thermal point of view, would be Au/Cr electrode which is however prohibitively expensive must be eliminated from further considerations.

4.7   Ru Devices Integrated on two Different Substrates

To study the relative degradation of Cu/TaO$_x$/Ru vs Cu/TaO$_x$/Pt devices, two nominally identical Cu/TaO$_x$/Ru devices however embedded differently on the Si wafer have been manufactured. While the substrate for Ru device A is the same as for the Pt device, i.e. Ti(20nm)/SiO$_2$(730nm)/Si, the Ru device B is manufactured on the layer stack Ti(20nm)/TaO$_x$(30nm)/SiO$_2$(730nm)/Si. Thus, Ru device B has an additional TaO$_x$-30nm layer
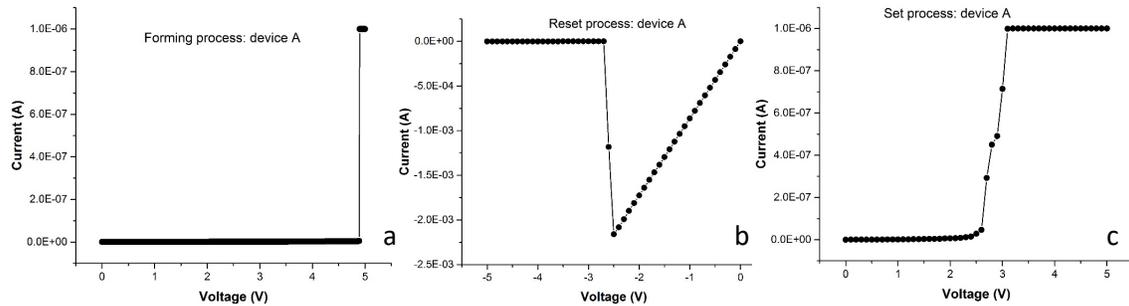
Fig. 4.8: *Switching operation of Ru device A with the same substrate as the benchmark Pt device @ I$_{CC}$= 1μA, rr= 2V/s: a) forming operation with V$_{FORM}$= 4.9V b) reset operation with V$_{RESET}$=-2.5V, c) set operation with V$_{SET}$=3.1V.*

inserted between SiO$_2$ and Ti layers. The electrical characterization of the two Ru devices, A and B, has been guided by the hypothesis that the difference in electric performance between the two devices is caused by effects stemming from larger or smaller exposure to the Joules heating dissipated in the device. Therefore, the form/set operations have been performed at low and high

I_{CC} currents, i.e. I_{CC}=1 µA, 5 µA, 10 µA, and 50 µA. Clearly, once the filament is formed exposure to Joules heating effects at 50 µA should be larger than at 1 µA. To control the heating effects further, also during the reset operation, the reset voltage ramp rate, rr, has been varied between 0.2V/s and 2V/s. In the reset operation the currents flowing through the cell are large; on the order of a few mA. Therefore, low ramp rate implies larger heating because of longer duration of exposure to high currents flowing through the cell, before the cell is ruptured at a reset current, I_{RESET}. Thus, most heating would occur for I_{CC}=50 µA and rr=0.2V and least heating for I_{CC}=1 µA and rr=2.0 V/s.

In general, it is found that the Ru device B with the additional TaO_x layer inserted between SiO_2 and Ti shows much better performance than the Ru device A (i.e. without that TaO_x layer) at all test conditions. However, the degree of improved switching properties of Ru cell B over cell A
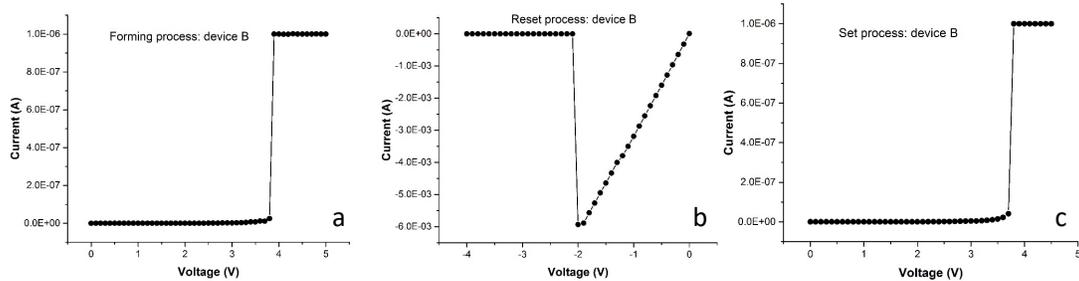
Fig. 4.9: *Switching operation of Ru device B with the modified substrate with TaO_X inserted between Ti and SiO_2 @ Icc= 1 µA, rr= 2V/s: a) forming operation with V_{FORM}= 3.95 V b) reset operation with V_{RESET}= -2.1 V, c) set operation with V_{SET} = 3.8V.*

varies with the levels of applied compliance current and ramp rate. The highest improvement is found for I_{CC}=50 uA and rr=0.2V/s, and almost no difference in performance between the two devices can be observed for the condition I_{CC}=1 uA and rr=2.0V/s. A typical successful forming,

reset, and set I-V characteristics for device B are shown in Fig. 4.9. No I-V characteristics of comparable quality can be shown for the device A; its best behavior is shown in Fig. 4.8.

It is found that at I_{CC}= 50 μA and rr=0.2V/s the Ru device A does not display resistive switching behavior at all. The device A cannot be reset after the filament has been formed the very first time. However, when the reset ramp rate is increased fivefold to rr=1V/s – thus reducing the Joules heat - the device A can be neither set or, if the set operation is eventually successful, the device cannot be reset, i.e. the resistive switching cell has been permanently damaged. During the set operation, even if successful, no sharp set transition can be observed but rather a gradual transition to the conductive state characteristic for a dielectric breakdown. In contrast, device B with the additional TaO_x layer at the bottom shows some resistive switching behavior for a few cycles. Sharp formation and set characteristics are observed with V_{SET} between 2.6 V and 4.0 V, however the subsequent reset attempts have proved unsuccessful. The frequency of devices B displaying resistive switching behavior is quite low at about 1% of the devices B tested. It can be concluded that high heating effects are detrimental to both devices. But, while device B displays some (if small) degree of resisting switching behavior, device A does not display it at all.

Keeping the reset ramp rate at 2.0V/s but now reducing the I_{CC} current from 50 μA to 1 μA, it is observed that resistive switching behavior for both devices with the frequency of the Ru devices B twice as high as for the Ru devices A.

The switching behavior improves when I_{CC} is kept at 50 μA and the ramp rate is increased from 0.2V/s to 2.0V/s for both devices. Now both devices show some resistive switching behavior, however, again, the frequency of resistive switching is at least three times higher for the device B than for device A. Clearly, reduced thermal budget due to the faster voltage ramp rate improves resistive switching behavior of both devices. Table 4.2 shows comparison of the V_{FORM}, V_{SET} and

V_{RESET} for both devices. It can be seen that V_{FORM} for device A is higher $4.6V<V_{FORM}(A)<5.0V$

than V_{FORM}, for device B $2.9\ V<V_{FORM}(B)<4.5V$. A similar observation applies to V_{SET}. This

Table 4.2: Comparison of threshold voltages and R_{ON} for Ru devices A and B, both set at $I_{CC}=50$ µA and rr=2.0V/s.

Device	V_{form} (V)	V_{reset} (V)	V_{set} (V)	R_{on} (KΩ)
A (Ti/SiO_2)	$4.6 - 5.0$	$1.7 - 3.6$	$2.8 - 4.5$	$13 - 42.0$
B $(Ti/TaO_x/SiO_2)$	$2.9 - 4.5$	$1.5 - 3.3$	$2.5 - 3.6$	$10 - 20.0$

observation could be explained by the assumption that Cu loss of the filament for device A is

higher than for device B. It can also be seen that the reset and R_{ON} values for devices A and B are

comparable. This indicates that once a Cu filament is established the dynamics of the creation of

a gap in the filament during the reset operation are the same.

Table 4.3 shows the values for the same quantities as in Table 4.2 but now for $I_{CC}=1$ uA

and rr=2.0V/s. Comparing Table 4.2 and Table 4.3, the same trends described above in Table 4.2

can be found. The frequency of the devices B tested that display resistive switching behavior is

now very high at 100%, while the frequency for the devices A tested showing resistive switching

behavior is about 2% for the same switching conditions. Manifestly, the least amount of heating

produces best resistive switching behavior for device B.

Device A and B are measured which are set at very high $I_{CC}=0.5$ mA at which a robust

filament with a low R_{ON} is being formed. We find the same trends as found at lower I_{CC} current

levels. Interestingly, for rr=2.0V/s the frequency of resistive switching is about the same at 60%

for both devices. However, when rr is lowered rr from 2.0V/s to 0.2V/s, i.e. allow for more Joules

heating, the frequency of device A drops to 17% while the frequency of devices B stays constant at 60%. Thus again, Ru device B is much less sensitive to dissipated Joules heating than the Ru device A.

Finally, two I-V characteristics of both devices at the same stress conditions with very low I_{CC} are compared: I_{CC}=1 μA and rr=2V/s. The first measurement was taken on a fresh device. The

Table 4.3: Comparison of threshold voltages and R_{ON} for Ru devices A and B, both set at I_{CC}=1 μA and rr=2.0V/s.

Device	V_{form} (V)	V_{reset} (V)	V_{set} (V)	R_{on} (KΩ)
A (Ti/SiO$_2$)	4.9	2.6	1.6 − 3.4	3.0 − 4.0
B (Ti/TaO$_x$/SiO$_2$)	3.8 − 4.2	1.5 − 3.5	2.8 − 3.0	2.0 − 16.0

second measurement was taken on a fresh device that has experienced resistive switching at I_{CC}=50 μA and rr=2V/s, prior to the measurement at I_{CC}= 1 μA. Thus, in the second case the device has experienced considerable "pre-heating" at I_{CC}= 50 μA. Both devices A and B perform worse after they have been "preheated" at I_{CC}=50 μA. While in the case of device B some of the devices exhibit resistive switching, there was almost no resistive switching for the device A. This means that at the operation at I_{CC}=50 μA, some irreversible changes must have taken place. On the other hand, the same experiment with "pre-heating" at 1 μA did not affect the subsequent resistive switching of both devices.

4.8 Discussion of Possible Causes for High Sensitivity of the Ru Device A to Joules Heating

There is a sizeable circumstantial evidence from the extant literature pointing to a possible cause of the degraded behavior of Ru device A vs Ru device B. During the forming and set operations a substantial local heating of the filament takes place. The maximum temperature has been estimated to be between 600°C and 1000°C [36, 37-39]. Regner and Malen [40] have argued that because of the nm dimensions of the filament the thermal transport is non-diffusive and the
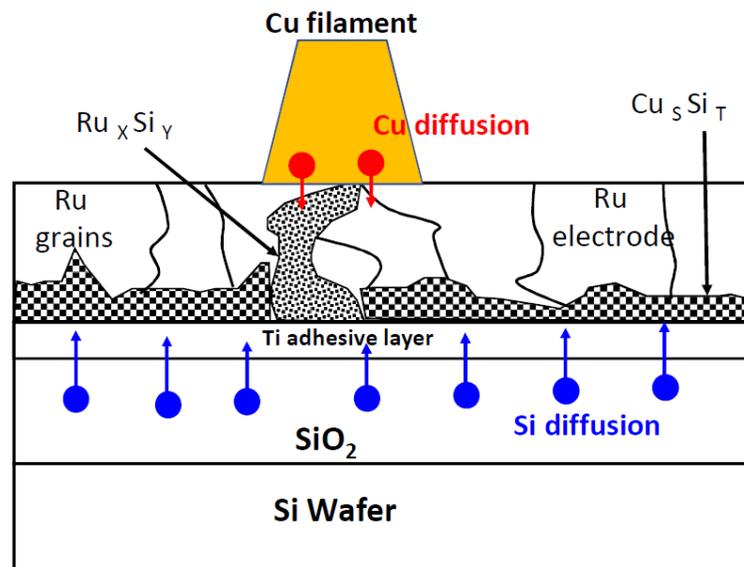
Fig. 4.10: *Possible mechanisms of the hypothesized degradation of the Ru electrode. Elevated local temperatures in the immediate vicinity of the filament may cause Si diffusion into Ru, possibly along Ru grain boundaries and lead to Ru_XSi_Y reactions. Cu may use the Ru grain boundaries as diffusion paths and undergo a silicidation reaction.*

differential Fourier equation of heat transport is grossly inadequate. The solution of the more adequate Boltzmann transport equation leads to much higher temperature estimates [40], as high as 1000° C. Our hypothesis is that such high temperatures even at relatively short times of

microseconds up to seconds can activate Si diffusion from the SiO_2 layer through the thin Ti layer into Ru layer, possibly accompanied by a TiO_x reaction. The Ru layer, in turn, can undergo, at such high temperature, local crystallization creating grain boundaries along which Si may readily diffuse [41]. Thus, Si that may reach at the Ru/Ti interface, may induce Ru silicide reaction to Ru_xSi_y and/or it can travel along the Ru grain boundaries and trigger Cu silicide reaction and form Cu_sSi_t at the forming base of the Cu filament at the Ru/TaO_x interface [42]. Both silicides are known to be poor diffusion barriers for Cu atoms [42]. The possible degradation mechanisms of the Ru electrode are shown conceptually in Fig. 4.10. Those degradation mechanisms may also explain the low frequency of resistive switching behavior for the Ru device A when compared with the Ru device B. For both devices, the worse performance is found when the base of the Cu filament overlaps with a possible Ru grain boundary. In this case, the Cu atoms can be drained out of the filament through Cu diffusion along the grain boundary. The best-case scenario for resistive switching is when the Cu filament does not overlap significantly or at all with a grain boundary. In that case the resistive switching behavior in both devices should be comparable. The non-overlap case may be responsible for the few instances when good resistive switching behavior can be observed for device A. In case of device A, the silicide reactions lead to inclusions of Ru_xSi_y and Cu_sSi_t most likely along the grain boundaries and, hence, such inclusions widen the area at the Ru surface where Cu can easily diffuse into the electrode. Therefore, device A suffers from Cu in-diffusion more than device B. Both Ru and Cu silicide reactions, compromise the inertness of the Ru electrode and lead of Cu loss into Ru electrode. The motivation of inserting TaO_x layer between Ti and SiO_2 layer in device B, was to stop or at least reduce the Si diffusion into the Ru electrode. The experimental results seem to confirm it showing that in case of device B the degradation of the Ru electrode due to silicide reactions has been reduced but perchance not completely

suppressed. The TaO_x layer of only 30 nm deposited by PVD is known to form tantalum oxide with lower density and higher porosity than the stoichiometric Ta_2O_5 deposited by ALD. Thus, the inserted 30 nm TaO_x layer may be not a perfect diffusion barrier for Si, either. Although a direct evidence for such reactions in our devices is lacking since their verification at the location of nanometer sized filament is very difficult to ascertain, several circumstantial evidences found in the literature for similar cases are discussed now.

The first inertness issue is Si diffusion and possible silicidation reactions. In [43] it has been shown for the layer stack of $Si/SiO_2/Ru$ that Si is the dominant diffusion species due to its high diffusivity and capability to dissolve interstitially in Ru [44, 45]. It has been observed that at a temperature $\sim600^\circ$ C Ru_xSi_y interlayer silicide at the Ru/SiO_2 interface begins to grow [46]. As a result, the dense Ru film is progressively being converted into less-dense Ru_2Si_3 leading to increased thickness of the silicided Ru layer. The presence of Ru_2Si_3 interlayer has been directly confirmed in [47, 48]. Our case is similar, except that an intervening layer of Ti is inserted between SiO_2 and Ru. But since the Ti layer is very thin (15 nm), it does not constitute most likely an effective barrier to Si diffusion. Therefore, it can be suspected that the ruthenium silicidation takes place in our devices as well.

Second issue to be addressed is the crystallinity of the Ru electrode. It has also been found that the as-deposited thin Ru films (~5 nm) tend to be amorphous, whereas relatively thicker Ru films (>20 nm) are polycrystalline in nature with vertical columnar microstructures with respect to Si substrate [46]. The size of Ru grains increases with temperature. The columnar Ru grain structure implies that there are many direct diffusion grain boundary paths for Cu between the top and bottom surface of the Ru layer.

Third issue is the adhesion of Cu atoms to Ru interface. It is known that Cu has a low wetting angle on Ru (43º) [49] and high affinity to Ru surface [50]. Therefore, Cu adheres strongly to Ru surface even at high temperatures as high as 600º C [51]. These findings argue strongly against significant Cu surface diffusion on Ru surface. However, at 475º C and above Cu starts diffusing through the energetically favorable inter-grain boundaries of Ru columnar microstructure.

These three reliability issues may conspire to cause substantial degradation of the inertness properties of the Ru electrode and trigger enhanced Cu diffusion through the degraded Ru electrode. The existing Ru_2Si_3 may accelerate the Cu diffusion even further [33, 52]. At 550^0 C, Cu can completely diffuse through a 20 nm Ru film, penetrate into the Si substrate, and form Cu_3Si by interacting with the substrate and eventually completely nullifies the barrier functionality of the remaining Ru layer [33, 53]. The Cu_3Si is found to be morphologically inverted pyramid-shaped rectangular crystallites with orientation perpendicular to the substrate [54, 55]. Such isolated crystals form a rough surface and induce a permanent damage to the Cu metallization in CMOS BEOL. Similar damage is most likely being done to the Cu filaments in our devices. Although, ideally both Ru and Cu are relatively inert on thermally stable SiO_2 even at high temperatures, the direct reaction with Si causes barrier failure at the same temperature for both Si and SiO_2 substrate [56]. Thus, the temperature at which Ru_2Si_3 forms may be the key triggering factor for the degradation of the inertness properties of Ru [57].

Given the degradation mechanisms described above, some mitigation strategies may be considered. One is a deposition of a thicker Ru electrode (presently at 50 nm). However, because of the columnar grain structure thicker Ru layer is not likely to be of much help. The other approach would be to limit the temperature of filament rupturing. This is difficult to achieve since the

rupturing temperature appears to be an intrinsic property of the device. The formation of Ru_2Si_3 requires higher temperature than formation of Cu_3Si [57], but it can be reached readily during a filament formation or filament rupture. Indeed, it has been shown that the barrier functionality of Ru film fails completely at ~700° C irrespective of the Ru layer thickness [57].

In conclusion, applying above observations to the circumstances encountered in our devices, it is plausible to argue that the insertion of the TaO_x layer between SiO_2 and Ti leads to a suppression of Si diffusion which leads, in turn, to a suppression of Ru and Cu silicide reactions. Since Ti is known to be an aggressive oxygen getter, the TiO_x at the interface of SiO_2 frees up Si atoms that can then readily diffuse into the Ru layer. The insertion of TaO_x layer between Ti and SiO_2 acts as an effective Si diffusion barrier.

4.9   XRD Studies of Embedment Layer Systems for Ru devices A and B

Extensive XRD studies of various layer combinations shown in Fig. 4.11 representative of the Ru devices A and B have been performed. The cross-sections of Ru devices A and B are shown Fig. 4.1(b) and 4.1(c) i.e. $Cu(25nm)/Ru(50nm)/Ti(40nm)/SiO_2(611nm)/Si$ for device A (the same substrate as for the Pt device) and, $Cu(25nm)/Ru(50nm)/Ti(40nm)/TaO_x(27nm)/SiO_2(611nm)/Si$ for Ru device B. In order to extract the significant XRD signals, the following auxiliary samples have also been manufactured: 1) Si (Si wafer with native oxide), 2) $SiO_2(611nm)/Si$, 3) $Ti(20nm)/Si$, 4) $TaO_x(27nm)/Si$, 5) $Ru(50nm)/Si$, 6) $Cu(25nm)/Si$, 7) $Cu(25nm)/SiO_2(611nm)/Si$, 8) $Ru(50nm)/SiO_2(611nm)/Si$, 9) $TaO_x(27nm)/SiO_2(611nm)/Si$, 10) $Ti(40nm)/SiO_2(611nm)/Si$ 11) $Ti(20nm)/TaO_x(27nm)/SiO_2(611nm)/Si$, and 12) $Ru(50nm)/Ti(40nm)/SiO_2(611nm)/Si$. These layer combinations are auxiliary samples and serve the purpose to track the XRD peaks with a single layer added to the previous layer stack and so help subtract background signals in order to

extract the relevant signals pertinent to Ru devices. The XRD measurements have been performed on all the aforementioned samples shown in Fig. 4.11. XRD studies were conducted for three annealing conditions: i) unannealed, i.e. @ 300K, ii) annealed at 600° C for 10 min, and iii) annealed at 900° C for 30 min. While an extensive study of this XRD study will be published
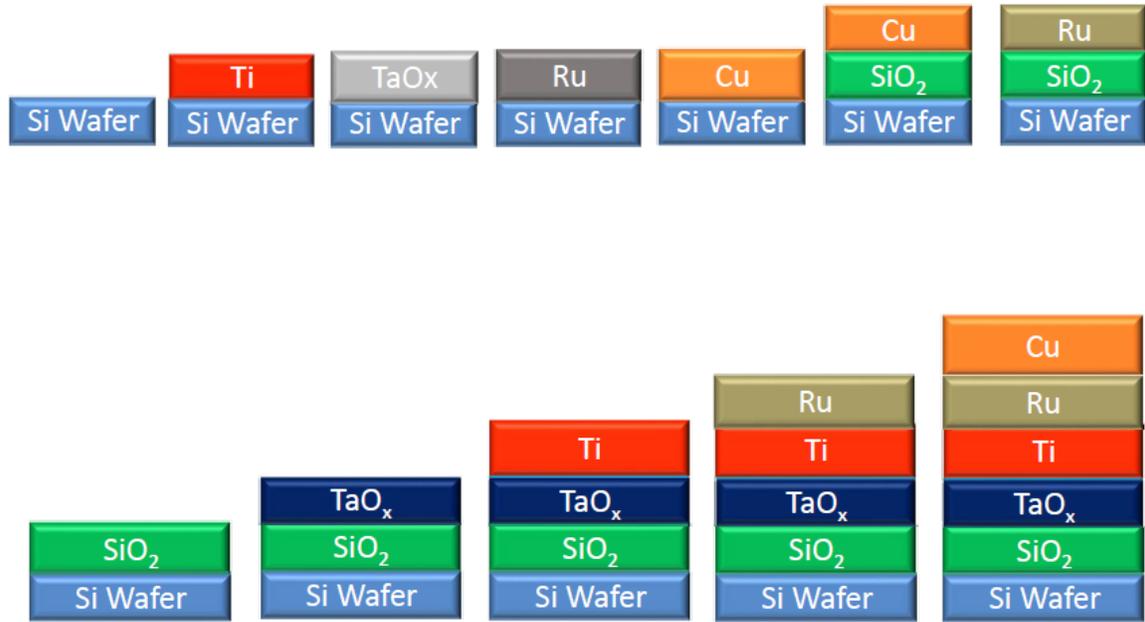
Fig. 4.11: *Cross-section schematic of as-prepared auxiliary samples to systematically investigate X-ray powder diffraction*

elsewhere [58], the results relevant to Ru devices A and B are summarized below. Ru crystallization peaks are observed at 42.15° of the XRD spectra on all samples containing a Ru layer at room temperature as well as for samples annealed at 600^0 C. Besides, Ruthenium silicidation peak (Ru_3Si_2) at 41.7° appears in both Ru/Si and Ru/SiO$_2$/Si samples annealed at 600^0 C. This silicidation peak is absent at room temperature. This is in agreement with XRD studies of similar layer systems reported in [57]. XRD signals for samples of Ru/SiO$_2$/Si at 300K, Ru/Si after an RTP anneal at 600° C for 10 min, and for Ru/SiO$_2$/Si after an anneal at 600° C for 10 min

are shown in Fig. 4.12. It is seen from Fig. 4.13 that the Ru silicidation peak at 41.7º is also present in both Ru/Si and Ru/SiO$_2$/Si samples after annealing at 900^{0}C for 30 minutes. However, insertion of an additional Titanium (Ti) layer reduces the silicidation peak intensity at 41.7º as seen in Ru/Ti/SiO$_2$/Si sample after annealing at 900^0 C for 30 minutes. This ruthenium silicidation
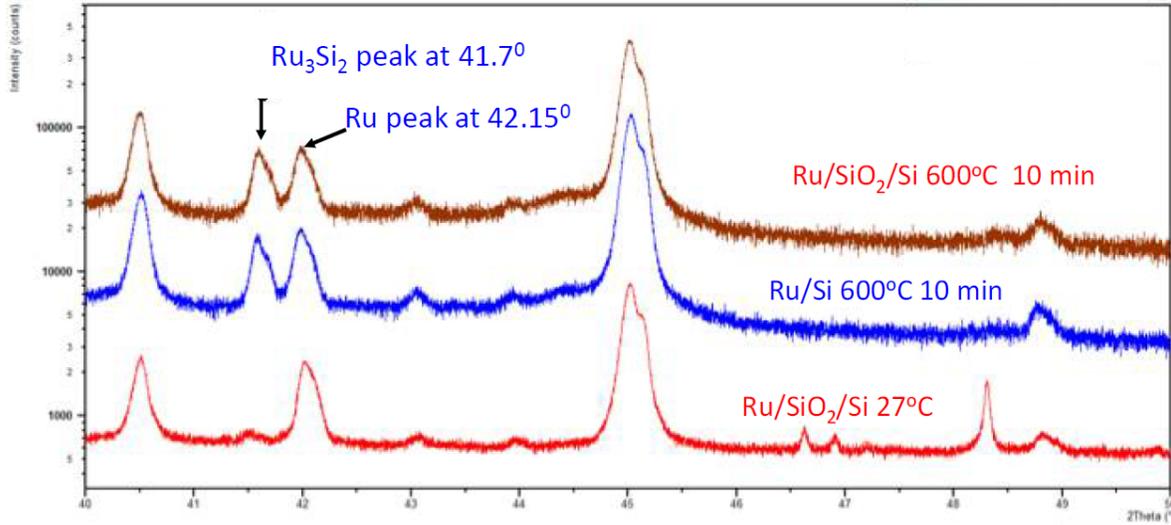
Fig. 4.12: *XRD spectra of three-layer structures: Ru/SiO$_2$/Si as deposited, Ru/Si and Ru/SiO$_2$/Si after a 600^0 C 10 min anneal. The Ru silicidation peak has been observed in layer structures with a Ru layer only after a 600^0 C anneal. The peak disappears after an anneal at 900^0 C for 30 min.*

(Ru$_3$Si$_2$) peak at 41.7º is further suppressed by insertion of an additional 30nm TaO$_x$ layer between titanium and SiO$_2$ layer and can be seen in Ru/Ti/TaO$_x$/SiO$_2$/Si sample after annealing at 900^0 C for 30 minutes. So, TaO$_x$ layer inserted between SiO$_2$ and Ti acts as a Si diffusion barrier, and hence suppresses the Ru silicidation reaction. No XRD peaks related to copper silicide reaction is observed. The lack of a clear Cu$_3$Si signal may not necessarily eliminate this reaction altogether, but points, at least, to scarcity of the compound which could be formed along the Ru grain boundaries. The XRD study confirms that the inertness of the Ru electrode is impaired by Ru silicidation at temperatures around 600º C and beyond. The XRD study corroborates not only the

210

difference in electrical performance between Pt and Ru device but also among the Ru devices embedded on different substrates.
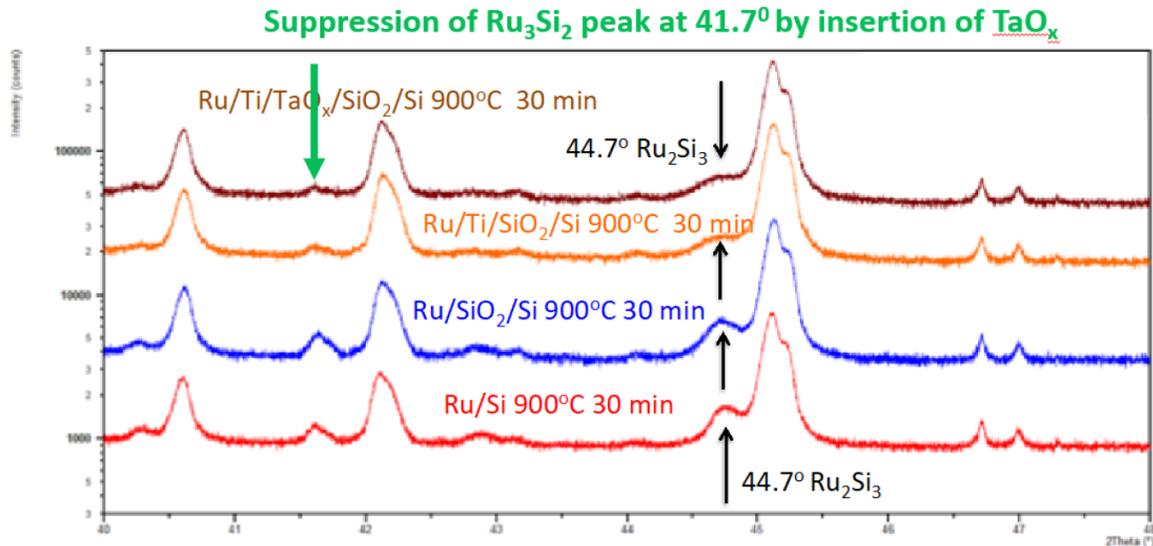
Fig. 4.13: *XRD spectra of four-layer structures annealed at 900^0 C for 30 min: Ru/Si, Ru/SiO₂/Si, Ru/Ti/SiO₂/Si and Ru/Ti/TaOX/SiO₂/Si. On all structures a Ru crystallization peak can be observed at 42.15^0, and Ti layer suppresses the ruthenium silication peak at 41.7^0. This peak is further suppressed by additional TaOx layer*

The anneal of the XRD samples at 600°C and 900°C is intended to mimic the likely local temperatures in the memory cells that are likely to occur during the switching operations.

4.10   Summary

Cu/TaOx/Ru devices compared to Cu/TaOx/Pt devices have higher forming, set, and reset voltages which can be partly attributed to the work function difference between Pt and Ru of 1.6 eV and partly to the impaired integrity properties of Ru vs Pt inert electrode. The performance deterioration of Ru devices is particularly conspicuous when the cell is exposed to high Joules heat dissipation. At low Joules heat dissipation, the switching performance of both Ru and Pt devices

is comparable. The Joules heat dissipation affects also the maximum switching cycles in both devices, with Pt devices, in many cases being unlimited, and in case of Ru, in extreme case of high Joules heat, limited to only one cycle. The integrity of the inert electrode appears to have a major impact on the Cu diffusional fluxes which in turn, determine the geometrical shape of the Cu conductive filament. The Pt electrode with its excellent stopping power produces conical CF with a sharp constriction near the Cu electrode interface, whereas in case of Ru electrode, the loss of Cu ions at the base of the Cu filament leads to a more cylindrical shape of the filament which causes more difficult to rupture in a reset operation. However, Pt with its highest work functions among the metals, induces high built-in electric field in the device which may reach critical fields in the ruptured filament's gap leading to spontaneous set operation, as demonstrated experimentally.

It has also been demonstrated that the electrical switching properties of the nominally the same resistive switching device $Cu/TaO_x/Ru$, however embedded differently on the wafer ($Cu/TaO_x/Ru/Ti/SiO_2/Si$ vs. $Cu/TaO_x/Ru/Ti/TaO_x/SiO_2/Si$), differ substantially. This is the result of chemical and structural interactions of the device proper with its immediate environment which is induced by the nanometer dimension of the layers involved and significant heat deposition during the switching of the resistive switching cell. This finding points to the broader and critical impact of the device's embedment on its structural, material integrity, and, eventually, its electrical reliability. In the particular case of this investigation, the significant degradation of the integrity of Ru electrode can be attributed to Ru grain crystallization and to ruthenium silicidation, which has been confirmed by extensive XRD studies. The insertion of a TaO_x layer between the SiO_2 and Ti layer led to a slight suppression of the Ru crystallization and silicidation reaction and thus to an

improved electrical performance of the Ru device on the $Ti/TaO_x/SiO_2/Si$ substrate as compared

to the Ru device manufactured on the $Ti/SiO_2/Si$ substrate.

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Chapter 5: Impact of the Heat Conductivity of the Inert Electrode on ReRAM Performance and Endurance

5.1 Introduction

The resistive switching (RS) device has lately been of great attention to both industry and academia as a potential replacement for volatile dynamic random-access memory (DRAM) and nonvolatile flash technologies that are nearing the end of their dimensional scaling roadmaps [1-9]. These two-terminal devices exhibit figure eight-like pinched current–voltage (I–V) hysteresis switching between a high resistance OFF state (R_{OFF}) and a low resistance ON-state (R_{ON}) with memristive characteristics [2,3]. Resistive switching memory (ReRAM) is classified in subcategories of nanomechanical, magnetoresistive, electrochemical, valence change, thermochemical, and phase change memory [7]. The focus of this work is on the electrochemical and valance change filamentary (also called conductive bridge or CBRAM) memory. In particular, Conductive Bridging Random Access Memory (CBRAM), also referred as Programmable Metallization Cell (PMC), is a promising candidate for a resistive memory device due to its highly scalable and low-cost technology [10]. CBRAM memory is being extensively explored as a promising candidate for a resistive memory device [11]. Both types of resistive switching memory have the potential to reduce latency in connectivity constrained computational devices by building resistive switching (RS) memory directly into a CMOS low-k/Cu interconnect to bring memory and logic closer together [12]. Large-scale integration of metal-oxide filamentary memory with a selector device based on 1T1R architecture has been reported [13,14]. Low-k dielectrics and Cu metal lines prefigure a potential ReRAM cell, and the cross-bar architecture of a typical two-

terminal RS device array is essentially the same as a CMOS metal interconnect system. Thus, the interconnect information bottleneck could be untied and morphed into several system architectures using the same device platform.

In general, a CBRAM device consists of an active anode, an insulating oxide layer, and an inert cathode. In some CBRAM devices, the anode materials are of Cu, Ag or Ni, which can dissolve, in the insulating layer [15-17]. The insulating layer is a solid-state electrolyte, such as SiO_2, GeS_2, Al_2O_3, Ta_2O_5, or TaO_x. The inert metal material is usually Pt, Ir or W, which are the stopping barriers of Cu and Ag cations. When a positive voltage is applied to the active electrode, cations such as Cu or Ag migrate through the solid electrolyte and move towards the inert cathode (Pt or W). The Cu or Ag cations are electrochemically reduced and deposited on the cathode to form a nanoscale conductive filament (CF) in so-called FORM and SET processes. Under reverse bias, the filament is electrochemically dissolved, and the cell is switched back to the HRS; so-called RESET process. The ON/OFF ratio of CBRAM is usually significantly higher than 10^3 [18] and allows also multilevel switching in a single memory cell [19].

To date, $Cu/TaO_x/Pt$ based devices have proven to be one of the more popular types of CBRAM devices due to numerous reports of excellent unipolar and bipolar switching characteristics, device performance, retention, reliability, endurance, and yield [8, 9, 20-23]. Commercialization of non-volatile memory products based on RS devices derived from a $Cu/TaO_x/Pt$ cell has also been recently reported [24]. However, Pt is generally considered to be incompatible with CMOS process flow [25]. Hence, for cost reasons and ease of manufacturing, it is desirable to replace the inert Pt electrode with another metal used in or with Cu interconnects such as Ti, Ta, W or Ru [26]. The former two are commonly used in metal interconnects as adhesion and Cu diffusion barriers while W is used as the wiring for lower metal layer local

interconnections. Several derivative TaO_x based RS devices employing Ti, Ta, and W as electrodes have been previously reported [27-37].

Endurance is the cyclability of a memory device and is one of the most important parameters for non-volatile memory devices. A very high endurance memory device can be programmed (written) and erased for large number of times and has wide range of applications with frequent read/write capability characteristics. The device endurance however, depends mostly on the property of bottom electrode or inert electrode of ReRAM memory cell. In this chapter the impact of inert electrode on the endurance of ReRAM memory cell during repeated set and reset switching is investigated in detail. During the switching, a considerable current flow can occur (usually limited by compliance current lest the device be damaged) leading to the heating of the conductive filament (CF). This is especially the case during the reset operation where the rupturing process is chiefly a thermal dissolution effect. $Cu/TaO_x/Pt/Ti$ device is used as the baseline device and is compared with six devices manufactured with different inert electrode constructions: Pt/Cr, Rh/Cr, Rh/Ti, Rh/Al_2O_3, Ir/Ti, and Ir/Cr, while the Cu electrode and the TaO_x dielectric are identical. Although the glue layers Ti, Cr or Al_2O_3 are not an inherent part of the device proper, they have a tangible impact on the device endurance as well. It is consistently found that inert electrodes with high thermal conductivities have superior endurance properties over an electrode with low thermal conductivity. Specifically, Rh (150/Cr (94) (numbers represent the heat conductivity in units of W/(m·K)) is not only superior to Pt (72)/Ti (20) but also to Rh (150)/Ti (20) device. The impact of heat conductivity of the inert electrode on the endurance is therefore explained by the deformation of the Cu filament due to Cu fluxes during the switching cycles.

5.2   Switching Operation and Heating in ReRAM Cell

In the set operation there are two fluxes responsible for the formation of filament as shown in Fig. 5.1(c). At the tip of the filament there is a large voltage drop which creates high electric field between the filament tip and the Cu electrode, which allows for further transport of Cu^+ ions from the Cu electrode to the filament even after establishing the initial connection between the Cu filament and the Cu electrode. The role of I_{CC} is to limit the resulting voltage drop
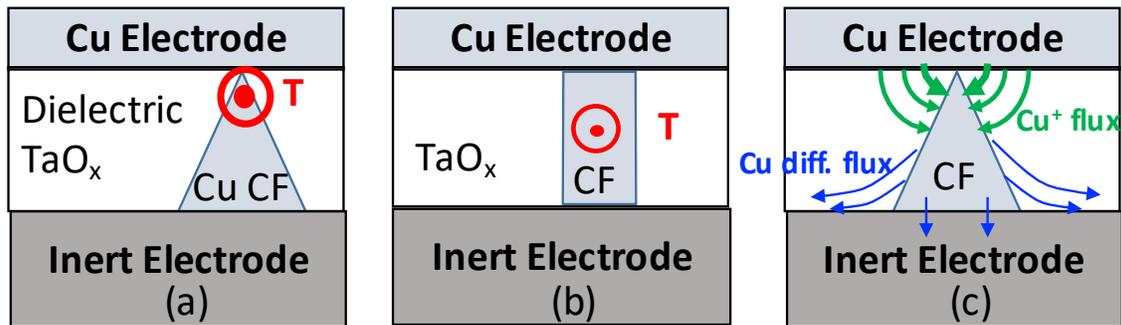
Fig. 5.1: (a) Cu CF with a sharp constriction and max. temperature at the tip. (b) Cu CF of cylinder-like shape with maximum temperature between the electrodes. (c) Constructive Cu^+ migration flux and destructive Cu diffusion flux.

and thus, set a limit on the electric field driving the Cu^+ ion transport. When sufficient number of Cu atoms are deposited at the tip, the resistance of the filament sinks, reducing the electric field at the tip and bringing the formation of the filament to a halt at a given I_{CC}. When I_{CC} is increased, then the electric field at the tip increases proportionally triggering additional arrival of Cu^+ ions until the resistance of the filament drops sufficiently to reduce the electric field and thus to halt further Cu^+ ion transport. The second flux is the Cu atom diffusion flux weakening the base of the filament and leads to an increased R_{ON} resistance. The diffusion effect can be gradual in so far as

any weakening of the filament leads to increased R_{ON} resistance which, in turn, may trigger the compensating Cu^+ electromigration flux.

The Cu diffusion flux is impacted by the thermal conductivity of the inert electrode. For the otherwise same conditions, the inert electrode with high heat conductivity will be able to remove the heat at a higher rate than an electrode with low heat conductivity. The larger heat

Fig. 5.2: Hypothesized mechanism of Joule's heat balance.

removal rate will result in lower attainable maximum temperature. Hence, a cell with inert electrode of low heat conductivity is bound to display enhanced Cu diffusion. The high temperature in the filament during the reset will trigger Cu diffusion near the base of the filament partly into the dielectric, partly along the TaO_x/inert electrode interface, and partly into the inert electrode if the inertness of the electrode is not perfect. The overall result of those diffusion components is the weakening of the base of the cone and a transformation of the shape of the filament from a sharply cone-shaped (Fig. 5.1(a)) into a more cylinder-shape filament as shown in Fig. 5.1(b). Once the shape of the filament is sufficiently close to a cylinder-like shape the

respective filament will be very difficult to be ruptured and the number of switching cycles comes to a halt.

The RESET operation is the dominant heat generation process. The temperature of CF is determined by the Joules heating and by the rate of heat removal, i.e. by the thermal conductivity of the surrounding materials. The Joules heat for a linear voltage ramp V(t)=rr×t is given by [38]

$$W_j = \frac{rr^2 * t_{res}^3}{3 * R_{ON}} \qquad (1)$$

where t_{RESET} is the time when the filament ruptures at V_{RESET}=rr×t_{RESET} (12). The heat removal

Table 5.1: Thermal Conductivity of Elemental Metals

Metal	Therm. Cond. W/(m·K)
Ag	406
Al	205
Au	315
Co	100
Cr	94
Cu	385
Ir	147
Ni	90
Pd	72
Pt	72
Rh	150
Ru	117
Ta	54
Ti	22
W	165

depends mainly on the heat conductivity of the inert metal with which the cone-shaped filament forms a broad base (Fig. 5.1(a)). When a device is repeatedly set and reset, and the heat removal

225

rate is slower than the switching speed, then the heat around CF can accumulate over time and lead to substantial Cu diffusion effects (Fig. 5.1(c)) which degrade the properties of the filament. To assess the thermal effects, we have manufactured otherwise identical memory cells with Pt/Ti, Pt/Cr, Rh/Cr, Rh/Ti, Rh/Al$_2$O$_3$, Ir/Ti, and Ir/Cr as inert electrode. The heat conductivities of the metals vary considerably from 20 W/(m·K) for Ti to 385 W/(m·K) for Cu. The thermal conductivity of several elemental metals is listed in Table 2.1.

5.3   Thermal Conductivity

According to thermodynamics, whenever there is a temperature gradient between an object and its surrounding medium an energy is transferred through the object's boundary. This energy is called heat. Heat is transported from the direction of high temperature towards the low temperature in accordance with second law of thermodynamics. There are three distinct modes of heat transport- conduction, convection, and radiation. In conduction mode of heat transfer, energy is transferred from one molecule to the next molecules without involving any displacement of particles. Usually conduction is the preferred heat transfer mechanism in solids.

The heat transfer through conduction mechanism is generally expressed by Fourier's law named by French scientist J.B.J. Fourier [39]. Let's consider a flat metal plate of thickness t and surface area A. Temperatures at two opposite points in the surfaces A, B are T_A and T_B respectively, where $T_A > T_B$. According to Fourier's law, the rate of heat flow (Q) can be expressed as [39]:

$$Q \propto A * \frac{T_A - T_B}{t} \qquad (1)$$

$$\text{So, } Q = k * \frac{T_A - T_B}{t} \qquad (2)$$

226

$$\text{and, } k = \frac{Q}{\frac{T_A - T_B}{t}} \tag{3}$$

Here, A is surface area, $(T_A - T_B)$ is the temperature gradient and k is proportionality constant known as thermal conductivity. In differential form, the heat transfer rate can be written as:

$$Q = (k * A) \lim_{x \to 0} \frac{T(L) - T(L + \Delta l)}{\Delta l} \tag{4}$$

$$\text{or, } Q = -(k * A) * \frac{dT}{dl} \tag{5}$$

Eq'n (5) is called one-dimensional heat conduction of Fourier's law. Thermal conductivity is the
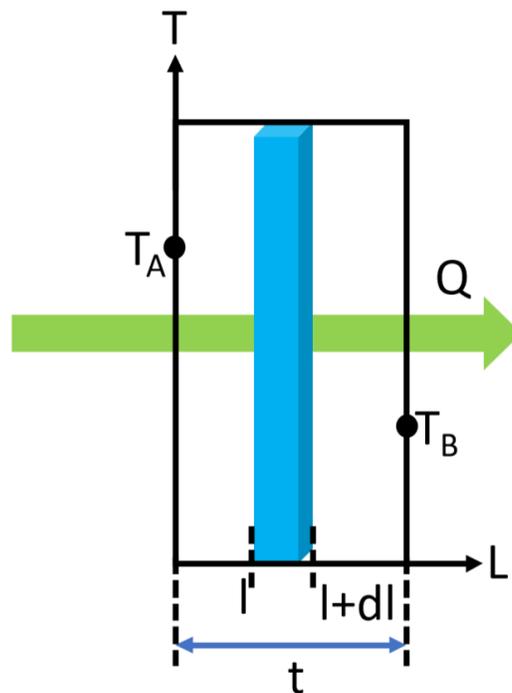
Fig. 5.3: *Heat conduction through a one-dimensional large plane wall*

intrinsic property of a material and is the ability to transport heat. Eq'n (5) can also be written as

$$\frac{dQ}{dA} = -(k) * \nabla T \tag{6}$$

where ∇ is the Laplacian differential-operator.

227

In solid materials, heat can be transported via electrons, holes, phonons, EM (electromagnetic waves) waves or other form of excitations etc. [40]. The total thermal conductivity of a material can expressed as the sum of thermal conductivities from all the excitation components:

$$k = \int_{i=1}^{n} k_i$$

Here n is the total number of excitation sources contributing to the overall thermal conductivity. The overall thermal conductivity of metals or solids consists of contribution from two independent components and can be expressed as [40]:

$$k = k_{electron} + k_{phonon}$$

Here $k_{electron}$ and k_{phonon} are the contributions from electronic thermal conductivity and phonon thermal conductivity respectively. Metals are solids with often having the crystalline structure, but they can also be amorphous. According to the band structure of metals, conduction and valance band overlaps and hence there are numerous mobile electrons. So, electrons are the leading heat transporter in pure metals. In impure metals or alloys there are significant contributions of thermal conductivity from phonon components. In insulators lattice vibration or phonons convey most of the heat. The thermal conductivity of a metal and its electrical conductivity is related through the Wiedemann-Franz law as [40]:

$$\frac{k}{\sigma} \equiv k * \rho = L * T$$

Here, σ is electrical conductivity, T is temperature in kelvin and L is the Lorentz number and it relates thermal conductivity with electrical conductivity for a pure metal.

Different materials have dissimilar crystal dimensions (for crystalline materials) or grain sizes (for polycrystalline materials), diverse density of defects or dislocations, distinct magnitude of carrier concentration, lattice forces etc. Therefore, thermal conductivities vary considerably from material to material. However, the magnitude of thermal conductivity gives a qualitative measure about the defect density or deviation from the ideal crystalline structure.

5.4 Device Fabrication

All devices Cu/TaO$_x$/IE, with various construction of the inert electrode IE=Pt/Ti, Pt/Cr, Rh/Cr, Rh/Ti, Rh/Al$_2$O$_3$, Ir/Ti, and Ir/Cr have been fabricated in a crossbar array on a thermally oxidized Si wafer. The metal electrodes and solid electrolyte were deposited by e-beam

(a)   (b)
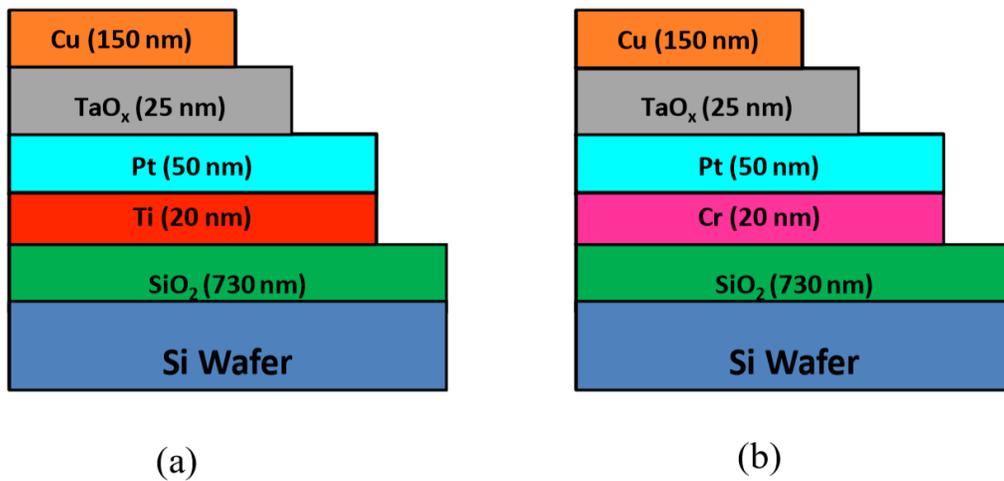
Fig. 5.4: *Cross-section of Cu/TaO$_X$/Pt resistive switching device with (a) Pt/Ti; (b) Pt/Cr inert-electrode module.*

evaporation and patterned by the liftoff technology. The oxygen-deficient tantalum oxide (TaO$_x$) layer was deposited by evaporating the Ta$_2$O$_5$ pellets without oxygen injection into the evaporation chamber. Our standard procedure was to use a thin layer of Ti as a glue layer for the inert metals

Pt, Rh, and Ir, as they have poor adhesion properties with SiO₂. However, Ti has a very low heat conductivity of 20 W/(m·K). It turned out that Cr is an equally good adhesion layer however with significantly higher heat conductivity of 94 W/(m·K). The Cu top electrodes run perpendicularly to the IE bottom electrodes and one resistive switch cell is located at each cross point with a blanket
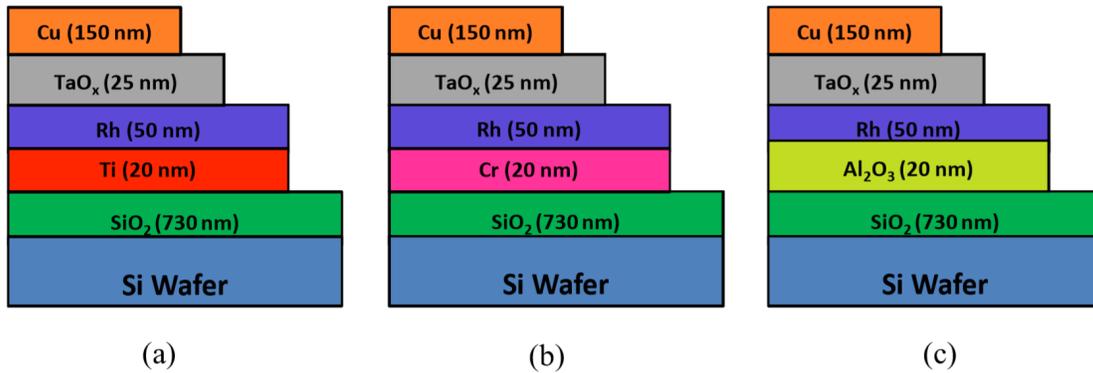
Fig. 5.5: *Cross-section of Cu/TaOₓ/Rh resistive switching device with (a) Rh/Ti; (b) Rh/Cr; (c) Rh/Al₂O₃ inert-electrode module.*

TaOₓ layer of dielectric in between. The width of the metal lines varies from 5 μm to 35 μm. The Cu, TaOₓ, Pt, Rh, Ir, Ti, Cr layers have been deposited by e-beam PVD in a Kurt Lesker PVD-250
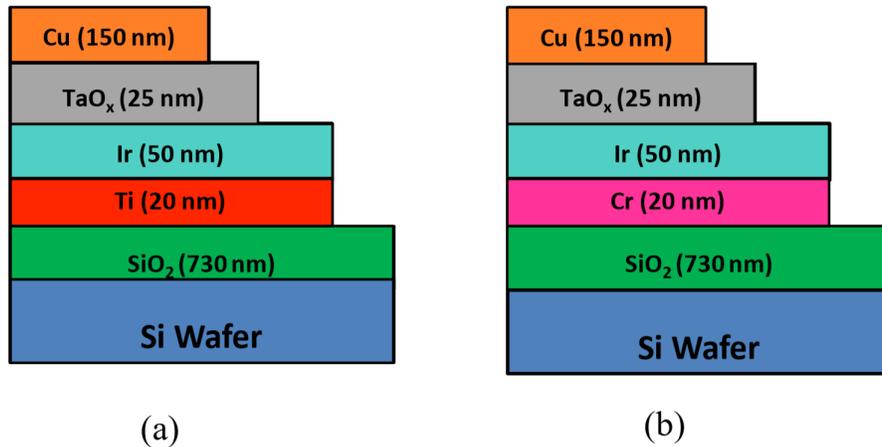
Fig. 5.6: *Cross-section of Cu/TaOₓ/Ir resistive switching device with (a) Ir/Ti; (b) Ir/Cr inert-electrode module.*

chamber, with the thicknesses 150 nm for Cu, 25 nm for TaO_x, 50 nm for Pt, Rh, Cr, and 20 nm

for Ti, Cr, whereas 20 nm Al_2O_3 was deposited using Savannah 100 thermal ALD. Al_2O_3 turned

out to be a decent adhesion layer, albeit not as good as Ti and Cr, with a low heat conductivity of

12 W/(m·K). Thus, the heat conductivity of the inert metal is varied between 150 for Rh to

72 W/(m·K) for Pt, and the heat conductivity of the adhesion layer is varied between 94 for

Cr to 12 W/(m·K) for Al_2O_3. Figure 5.4(a) and (b) shows cross-section of $Cu/TaO_x/Pt$ devices on

Ti and Cr adhesive layer respectively. Again, the cross-section of $Cu/TaO_x/Rh$ devices on adhesive

layer Ti, Cr and Al_2O_3 are shown in Fig 5.5(a), (b) and (c) respectively. Finally, the fabricated

device cross-section of $Cu/TaO_x/Ir$ on glue or adhesive layer Ti and Cr are shown in Fig. 5.6(a)

and (b) respectively.

5.5   Device Characterization

All the devices have been characterized by monitoring the forming voltage, V_{FORM}, when

CF is being formed the very first time, the reset voltage, V_{RESET}, the set voltage, V_{SET}, the

maximum number of switching cycles resulting from repeated set and reset operations, and the

resistance of the filament R_{ON}, when the cell is in the low resistance state. The following four set

Icc (μA)	rr (Volt/sec)	Joules heat
5	2	Lowest
5	0.2	Low
50	2	Moderate
50	0.2	Highest

Fig. 5.7: I_{CC} *vs. voltage sweep rate and generation of corresponding Joules heat*

conditions have been applied: the compliance current is I_{CC}=5 µA or 50 µA and the voltage ramp rate rr=0.2V/s or 2.0V/s. The resulting four testing conditions allowed us to control the Joules heat generated in the Cu filament during the set operation. The highest Joules heat is generated when I_{CC} is high (50 µA) and the rr (0.2V/s) low, and the lowest Joules heat is being generated when when I_{CC} is low (5 µA) and the rr (2.0V/s) high. The reset condition has been kept at I_{CC}=0.1 A and rr=0.2V/s.

5.6   Analysis of the Experimental Results

We find that the range of the distributions of the critical switching voltages for V_{FORM}, V_{SET}, and V_{RESET}, for all devices largely overlap indicating that all devices behave very comparably. For all the devices, we found V_{FORM} to be in the interval (2V, 6V), V_{SET} in (1V, 5V), and V_{RESET} in (-3.5V, -0.5V). In case of V_{RESET}, we find a slight non-uniformity with Pt/Ti devices tending to reset, occasionally, at higher values up to -4V. The electrical characterization shows, however, clear differences between the devices in the endurance behavior and finer details manifesting itself in the variation of the Cu filament resistance R_{ON}. The endurance test was performed by setting and resetting the device manually on the Keithley 4200-SCS station repeatedly, maximally up to 100 times. In many cases, the devices failed to switch after some number of switching cycles significantly less than 100 times. The result of these tests provides the following ranking starting with the highest number of cycles: 1) Rh/Cr, 2) Rh/Ti, 3) Pt/Cr, 4) Pt/Ti, 5) Rh/Al$_2$O$_3$, 6) Ir/Ti. The device Ir/Cr could not be reliably tested as many cells did not work properly due to some misprocessing issue. The largest number of switching cycles is found for the Rh/Cr device and the smallest number of switching cycles is found for Rh/Al$_2$O$_3$ device. We

explain the different number of switching cycles by the degradation of the geometrical shape of the Cu filament. It is known that R_{ON} can be controlled by the level of I_{CC} during the set operation. All our devices follow the relation $R_{ON}=C/I_{CC}^{n}$ where the exponent n is close to unity. In Table 5.2 the constants C and the exponents n for the individual devices are listed. According to the above relation, the R_{ON} resistance is large for low I_{CC} and small for large I_{CC}. With respect to the geometrical shape of the filament, we associate the cells with large R_{ON} with a truncated cone with a sharp constriction of the top (see Fig. 5.1(a)), where the bulk of the R_{ON} resistance is concentrated at the tip of the cone. Filaments with a sharp constriction at the top of the cone are easy to rupture since the maximum Joules heating is deposited at the tip and leads there to a high local temperature which, in turn, leads to Cu out diffusion and formation of a gap in the filament which completes

Table 5.2: Coefficients C and n for the relation $R_{ON}=C/I_{CC}^{n}$ for various device types. All set operations have been performed at voltage ramp rate rr=2V/s.

Device	C	n
Rh/Cr	0.12	1.05
Rh/Ti	0.17	1.05
Rh/Al$_2$O$_3$	0.10	1.0
Pt/Cr	0.18	0.98
Pt/Ti	0.09	1.03

the rupture of the filament and restores the HRS state. In contrast, the shape of Cu filament with a small R_{ON} approaches that of a cylinder (Fig. 5.1(b)) and the temperature hot spot moves to the center (i.e. midway between the electrode interfaces) of the filament where it is much more difficult to reach high temperature and cause out-diffusion of a larger number of Cu atoms to form

a gap. Experimentally, we find consistently that filament rupturing is more difficult with decreasing R_{ON} resistance.

Since filament rupturing is chiefly a thermal phenomenon, the heat conductivity of the inert electrode plays a significant role in determining the maximum temperature of the filament. For the otherwise same conditions, the inert electrode with high heat conductivity will be able to remove heat at a higher rate than an electrode with low heat conductivity. The larger heat removal rate will result in lower maximum temperature. Hence, a cell with inert electrode of low heat conductivity is bound to suffer from enhanced Cu diffusion. The high temperature in the filament during the reset will trigger Cu diffusion near the base of the filament partly into the dielectric, partly along the TaO_x/inert electrode interface, and partly into the inert electrode if the inertness of the electrode is not perfect. The overall result of those diffusion paths is the weakening of the base of the cone and a transformation of the shape of the filament from a sharply cone-shaped into a more cylinder-shape filament as shown in Fig. 5.1(b). Once the shape of the filament is sufficiently close to a cylinder-like shape the respective filament will be very difficult to be ruptured and the number of switching cycles comes to a halt.

When looking at the heat conductivities in units of W/(m·K) of the inert electrode construction considered in this study, arranged from highest to lowest effective conductivity, the following sequence arises: Rh(150)/Cr(94)) Rh(150)/Ti(20), , Ir(147)/Cr(94), Ir(147)/Ti(20), Rh(150)/Al$_2$O$_3$(12), Pt(72)/Cr(94), Pt(72)/Ti(20), Ir(147)/Cr(94). Comparing this ranking with the endurance ranking given above, a strong correlation between them can be observed. The highest number of repeated switching cycles are observed for Rh/Cr electrode which also has the highest heat conductivity. It should be kept in mind that the effective heat conductivity is dominated by

the heat conductivity of the inert metal because of its thickness of around 50 nm-55 nm compared with the thickness of the glue layer of approximately 15 nm – 20 nm. Nevertheless, the comparison between the inert electrodes Rh/Cr and Rh/Ti or Rh/Al$_2$O$_3$ as well as between Pt/Cr and Pt/Ti shows that slightly better switching behavior is found for Rh/Cr than for Rh/Ti or Rh/Al$_2$O$_3$ and

Rh/Cr	Rh/Ti	Pt/Cr	Pt/Ti	Rh/Al$_2$O$_3$	Ir/Ti
1	2	3	4	5	6
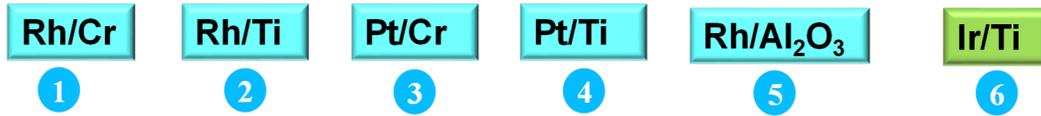
Fig. 5.8: Device ranking according to the maximum number switching cycles from the test

for Pt/Cr than for Pt/Ti demonstrating that even slight differences in the effective heat conductivity are reflected in the number of switching cycles. The results for Ir/Cr and Ir/Ti electrodes are less clear and could be influenced by the inertness properties of Ir such as formation of grains and grain boundaries providing additional channels for Cu diffusion, or miscibility of Cu with Ir, or possibly even some compound chemical reactions.

To study the heating effects for different inert electrode constructions during the set operation we have monitored the R$_{ON}$ resistance as a function of the set conditions. In the set operation there are two fluxes responsible for the formation of the filament as shown in Fig. 5.1(c) at the tip of the filament there is a large voltage drop which creates high electric field between the filament tip and the Cu electrode, which allows for further transport of Cu$^+$ ions from the Cu electrode to the filament even after establishing the initial connection between the Cu filament and the Cu electrode. The role of I$_{CC}$ is to limit the resulting voltage drop and thus set a limit on the electric field driving the Cu$^+$ ion transport. When sufficient number of Cu atoms is deposited at the tip, the resistance of the filament sinks, reducing the electric field at the tip and bringing the formation of the filament to a halt at a given I$_{CC}$. If the I$_{CC}$ is increased, then the electric field at

235

the tip increases proportionally triggering additional arrival of Cu^+ ions until the resistance of the filament drops sufficiently to halt further Cu^+ ion transport. The second flux is the Cu atom diffusion flux that weakens the base of the filament and leads to increased R_{ON} resistance. The diffusion effect can be subtle in so far as any weakening of the filament leads to increased R_{ON} resistance which, in turn, may trigger the compensating Cu^+ electromigration flux.

Our first comparison between R_{ON} values for various memory cells is done between the set

Table 5.3: R_{ON} at I_{CC}=5 µA for two voltage ramp rates (rr) and for different devices

Icc= 5 µA		
Device	rr = 2 v/s	rr = 0.2 v/s
Rh/Cr	20 kΩ	2.5 kΩ
Rh/Ti	22 kΩ	2.3 kΩ
Rh/Al$_2$O$_3$	30 kΩ	2.3 kΩ
Pt/Cr	20 kΩ	2.1 kΩ
Pt/Ti	20 kΩ	2.1 kΩ
Ir/Ti	20 kΩ	2.1 kΩ

conditions with high voltage ramp rate rr=2V/s and low voltage ramp rate rr=0.2V/s at the same low I_{CC}= 5 µA. In this case the Joules heating due to low I_{CC} is negligible. However, the duration of the set conditions at rr=0.2V/s is ten times longer than for rr=2V/s. Hence more Cu^+ ions can be transported to the tip of the filament at the same electric fields. Indeed, we find for a rr=2V/s that R_{ON} is typically 20 kΩ or larger while R_{ON} at rr=0.2V/s is considerably smaller, typically between 2.1 kΩ and 2.5 kΩ. The Table 5.3 shows the results for the different devices. Overall, for all the devices tested at I_{CC}=5µA, R_{ON} at rr=2V/s is roughly one order of magnitude higher than at rr=0.2V/s. The same tests are repeated at higher compliance current, I_{CC}=50 µA. At rr=2V/s we obtain for R_{ON} a 10 times lower R_{ON} than at I_{CC}=5µA, confirming the relation $R_{ON}=C/I_{CC}^n$,

quantified in Table 5.2. With higher heating, one can expect more losses due Cu diffusion. Indeed, R_{ON} values at 0.2V/s are lower than at 2V/s but now only by a factor of 2-4, instead of 10 as in the case of I_{CC}=5 µA. The results are summarized in Table 5.4. In one case of Ir/Ti and Rh/Al$_2$O$_3$, the R_{ON} value between rr=2V/s and rr=0.2/s does not change. To demonstrate the Cu diffusion flux

Table 5.4: R_{ON} at I_{CC}=50 µA for two voltage ramp rates (rr) and for different devices

Icc= 50 µA		
Device	rr = 2 v/s	rr = 0.2 v/s
Rh/Cr	2 kΩ	500 Ω
Rh/Ti	2 kΩ	225-750 Ω
Rh/Al$_2$O$_3$	2 kΩ	2 kΩ
Pt/Cr	2 kΩ	331-1 kΩ
Pt/Ti	2 kΩ	230-1 kΩ
Ir/Ti	2 kΩ	2 kΩ

effects, we have set the devices also at I_{CC}=100 µA and rr=2V/s, 0.2V/s, and 0.002V/s. For all devices we obtain stable R_{ON} at 2V/s and very unstable R_{ON} at 0.002V/s. For example, for the Pt/Ti device, R_{ON} at I_{CC}=100 µA and 2V/s is 1kΩ, at 0.2V/s 220-232 Ω, and at 0.002V/s, 158 Ω – 11 kΩ. The great range of R_{ON} values at 0.002V/s is a reflection of the instability resulting from the competition between the constructive Cu^+ migration flux and the destructive Cu diffusion flux (see Fig. 5.1(c)).

5.7   Conclusion:

Switching cycles are impacted by the effective heat conductivity of inert electrode module. Inert electrode stack with low heat conductivity cannot remove heat at a faster rate, causes higher local maximum temperature, high temperature triggers enhanced Cu diffusion near the filament

base into dielectric, along TaOx/inert electrode interface and into inert-electrode (if imperfect) and therefore, weaken filament base and covers the filament from sharply cone shaped into cylindrical shape, which is difficult to rupture, and the switching cycles stops. The heat conductivity of the glue layer also plays a role, if secondary. Devices with adhesive material which have high thermal conductivity such as Cr [94 W/(m.K)] is expected to have better endurance than devices with adhesive layer Ti [20W/(m.K)] for the same inert electrode. The device endurance ranking listed in this work through limited set and reset operations of the investigated inert electrode materials closely follows the ranking of effective thermal conductivity of the inert electrode module. Ir/Ti, Ir/Cr electrode results are less clear and could be affected by inertness properties of Ir (miscibility of Cu with Ir, Cu diffusion through formation of grain boundaries, compound formation etc.). For high frequency switching cells, Rh electrode (highest heat conductivity) shows best long-term performance and endurance. The root cause of the different endurances of the cells is the effective Joules heating deposited in the Cu filament. Therefore, electrode with high thermal conductivity leads to a superior resistive switching behavior over an electrode with low heat conductivity.

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Chapter 6

PART-1: Thermal Cross-Talk Between Cell-to-Cell

6.1   Introduction

Resistive Random-Access Memory (ReRAM) is one of the prime candidates to replace current floating gate technology because of their excellent scaling potential, low power consumption, high switching speed, and good retention and endurance properties [1]. A two-terminal resistive memory cell, such as $Cu/TaO_x/Pt$, can be switched between low resistive state (LRS) and high resistive state (HRS) by application of high enough voltage or current. ReRAM cells lie at the intersection of perpendicular metal electrode lines forming a crossbar array as shown in Fig. 6.1(a). Repeated switching of a cell leads to an accumulation of deposition of Joules heat in the device. Here it is demonstrated that this Joules heat is transported along the electrode metal lines affecting the neighboring cells and causing the deterioration of their electrical properties [2]. Also, cells with no common metal lines with the heated cell are less liable to be degraded.

When a memory cell is switched repeatedly a considerable amount of heat is deposited in the cell that may spread to neighboring cells which share the same metal lines. This thermal cross-talk causes degradation of electrical performance of the neighboring cells. It is found that even neighboring cells without common metal lines with the heated cells suffer from electrical degradation when intermediate cells are set into a conductive state. The inter-cell thermal cross-talk poses a serious electro-thermal reliability problem for the operation of a memory crossbar array, especially at a much more tighter pitch than our manufactured samples in Virginia Tech cleanroom facility.

243

6.2   Device Fabrication and Characterization

The Cu/TaO$_x$/Pt/Ti resistive ReRAM cell arrays (Fig. 6.1(a)) have been fabricated in a crossbar array on a thermally oxidized Si wafer [3] with a SiO$_2$ layer 650 nm thick. Cu (150 nm),

(a)   (b)
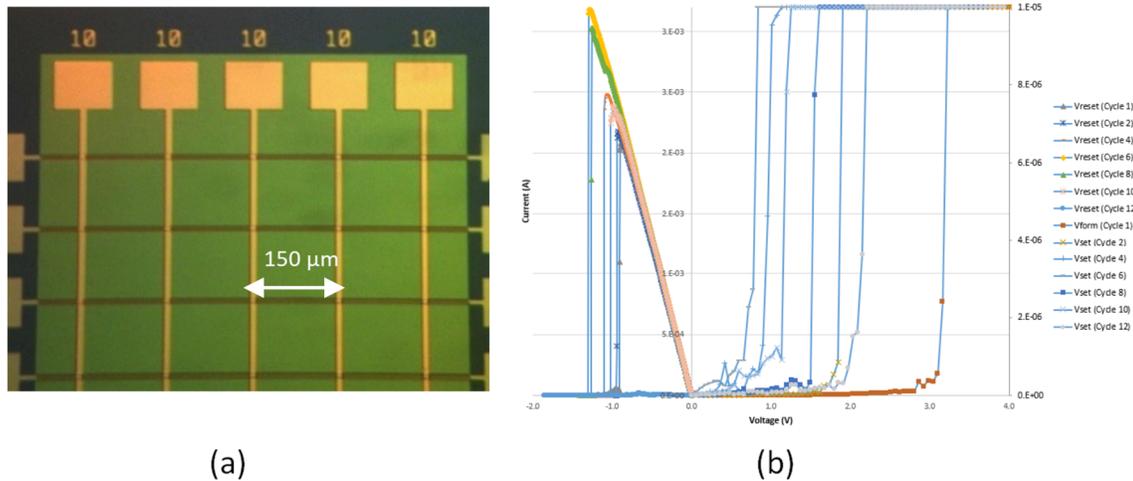
Fig. 6.1: *(a) Cu/TaO$_X$/Pt are located at the intersections of Cu and Pt lines forming a crossbar array (b) even number of repeated switching set and reset even cycles of a 15 μm×10 μm cell*

Pt (50nm), Ti (20nm) layers have been deposited by e-beam PVD. The Pt electrode lines are patterned with lift-off technique with photoresist thickness of 2 μm to make sure that the side walls are sloped gently thus avoiding any corner field effects. The oxygen-deficient TaO$_x$ of 25 nm was deposited in blanket fashion by evaporating TaO$_x$ pellets without O$_2$ injection into the PVD evaporation chamber. The thickness of the TaO$_x$ on the sloped sidewalls of Pt line is 98% of the planar thickness as confirmed by Ta$_2$O$_5$ atomic layer cells manufactured with Ta$_2$O$_5$ deposition by atomic layer deposition (ALD) [3]. The width of the metal lines varies between 1 μm and 35 μm. The neighboring line pitch is between (150+1) = 151 μm and (150+35) = 185 μm. The detailed description of memory cells used in this investigation can be found in [4, 5]. The electrical characterization was performed at room temperature on a probe station equipped with Keithley

4200-SCS. Before a measurement is taken the two grounded needles are placed on the cell contacts for at least 20 s to fully discharge the cell capacitor. Then the voltage of the Cu electrode starting at 0V is ramped at a ramp rate (rr). During the set operation, a compliance current (I_{CC}) of 5 μA to 1 mA has been imposed without an off-chip resistance lest the device be damaged. A Cu conductive filament (CF) is established at a critical positive voltage V_{SET} and the conductive path is ruptured at a negative critical voltage V_{RESET}. A typical I-V characteristics for the set and reset operations are shown in Fig. 6.1(b).

6.3 Test Methodology

We have noticed that the electrical switching of a fresh cell A has been degraded when the direct neighbor of cell A, a cell B has been heated by repeated set-reset cycles. This degradation
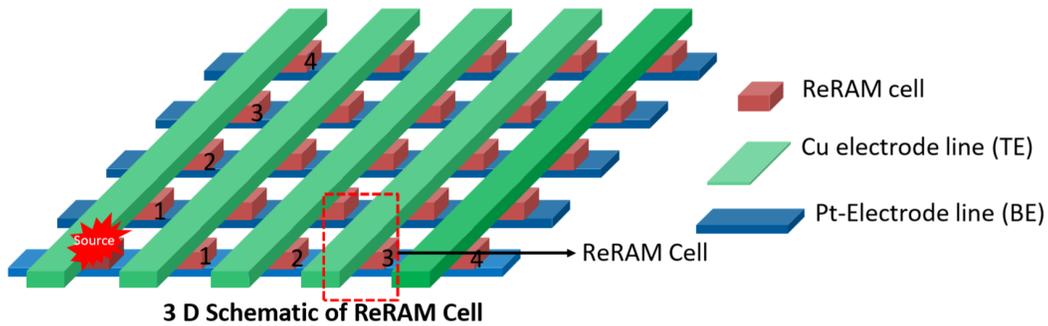
Fig. 6.2: 3D schematic of ReRAM cell arranged in a crossbar array

of electrical properties disappears when the cell was tested again after 10, 15, 20 minutes or a longer time period. We assume that the degradation subsided after times smaller than 10 min. We estimate that the cooling-off time lies between 1.5-5.0 minutes. Electrical tests between various Pt

and Cu line proved that there are no sneak paths between the heated and the probed cell [6]. We

hypothesize that the degradation of cell A is due to inter-cell thermal cross-talk which subsides

$$D\% = 1 - \frac{\text{MAX for probed cell affected by remote heating}}{\text{MAX of a fresh cell} = 15}$$
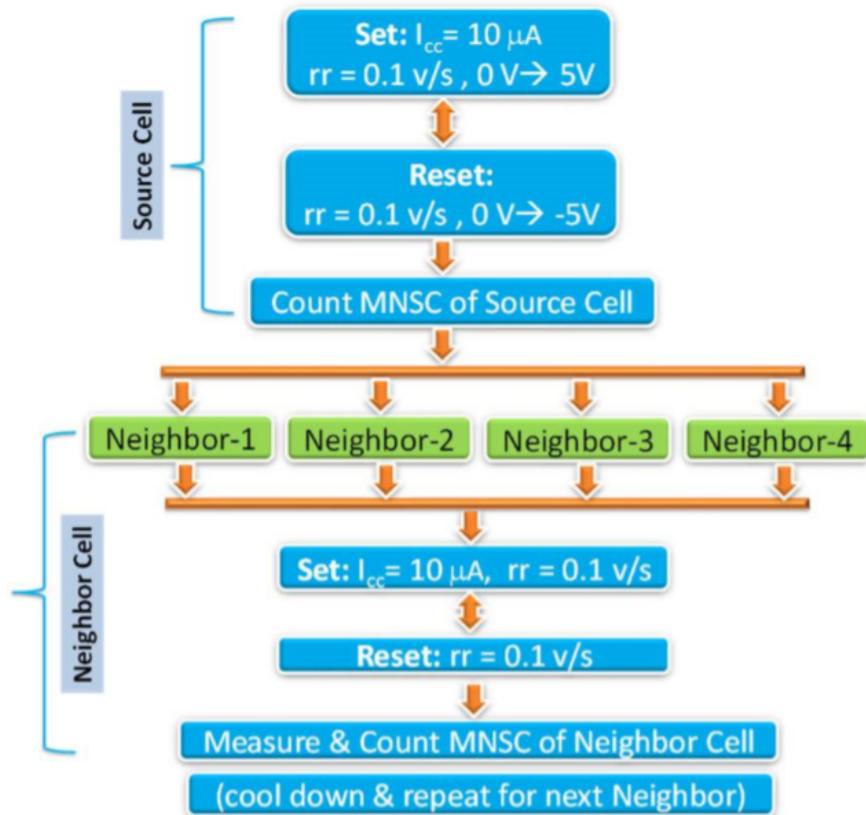
Fig. 6.3: *Process flow for measurement of thermal-crosstalk between ReRAM cells*

within a few minutes.

In order to quantify the thermal cross-talk, we create a "marginal" memory cell as a probe

into the thermal transfer phenomena. By "marginal" we mean a device that is set at a I_{cc} of only

10 μA and rr=1.1V/s. When the cell is set at such conditions the cell is very volatile and undergoes a spontaneous reset in more than 90% of cases of tested devices. The marginality of the device is further demonstrated by subjecting the device to a set operation at I_{CC} = 3-5 μA with the result that the device cannot be set in a permanent LRS state. Despite several set operations such cell remains in an off-state. On the other hand, when we set the same device at I_{CC} = 8-10 μA, the LRS state is stable although only for a very small number of switching cycles, typically 11-14, when the cell becomes volatile. Such set operation at I_{CC}=10 μA has been applied to ~ 100 cells with a mean of 12.7 maximum cycles and standard deviation σ = 1.3. A low rr = 0.1V/s has been applied during the reset operation to allow for a long heating time. For a low rr, the current lingers for a long time and hence low rr maximizes heat dissipation. When the maximum number of switching cycles (Max) is reached the device is driven to highly unstable performance. This can be contrasted with a device set at I_{CC} = 40-100 μA when the cell can be switched repeatedly more than hundred of times. Hence, a cell set at I_{CC}=10 μA is our "canary in the coal mine" and the number Max is our metric to quantify the degree of the thermal cross-talk. The Max number of switching cycles is defined by the onset of cells volatility. In our experimental setup the time between heating the cell B and characterization of cell B is about 50s - the time required to replace the needles on the probe station.

When testing in such a way, the 1st, 2nd, 3rd, and 4th neighboring cell, we find that 1st neighbor suffers most yielding Max of 0-3 switching cycles while the 3rd and 4th neighbor are degraded only slightly showing Max of 11-14 compared with a mean of ~13 for a fresh or thermally unaffected cell. At this point it is instructive to estimate the heat dissipated in the cell during a single reset operation, characterized by a reset current $I_{RESET}=V_{RESET}/R_{ON}$. Here R_{ON} is the

resistance of the LRS state. The reset current is typically $1mA < I_{RESET} < 6mA$. For a cell to which a constant voltage ramp rate is applied the Joules heat Q can be calculated by eq'n (1)

$$Q = \int_0^{t_{res}} \frac{V^2(t)}{R_{on}} dt = \int_0^{V_{res}/rr} \frac{rr^2 \times t^2}{R_{on}} dt = \frac{V_{res}^3 \times I_{cc}}{3 \times rr \times K} \qquad (1)$$

Here the reset time at an applied voltage ramp rate rr is $t_{RESET} = V_{RESET}/rr$ [7,8]. In eq'n (1), the well known relation between R_{ON} and I_{CC}, $R_{ON} = K/I_{CC}^n$, has been used [9] that R_{ON}, with $K \approx 0.3V$ and $n \approx 1$ for our memory cells. For Q according to eq'n (1) one obtains $\sim$ 3-5 µJ [8]. The advantage of the above equation is that the heat dissipated in the device is described in terms of experimentally measurable parameters, namely, the compliance current I_{CC}, the voltage ramp rate rr, and the reset voltage V_{RESET}. Of course, when the cell is switched on and off repeatedly and in a quick succession, the total heat deposited in the cell will be $Q_{tot} = Max \times Q \times f$, where f is a dimensionless, positive number smaller than 1 accounting for the outflow of heat out of the device between the switching events.

6.4   Test Results and Cell Degradation

Maximum number of switching cycles (MAX) of a marginal device serves as our metric to quantify the parasitic heat transfer and cell performance degradation. After heating a device, four neighboring cells along the electrode line (Fig. 6.2) are being characterized one at a time. we define degradation (D%) as:

$$D\% = 1 - \frac{\text{MAX for probed cell affected by remote heating}}{\text{MAX of a fresh cell} = 15}$$

248

Several thermal models exist in the literature describing the temperature distribution in ReRAM cells. Mickel et al [10] established a geometrically equivalent circuit to describe the heat flow through a conductive filament, yielding temperature distribution of the memory cell. The critical temperature responsible for the rupturing of a filament is calculated to be ~1225° K. In another work, Mickel et al [11] proposed a set of constitutive equations describing the evolution of the heat transport. Based on this work, the temperature responsible for the rupturing of the filament is ~1500° K. Sun et also found that the peak temperature of the filament is somewhere between 600° C and 900° C [12]. Thus there is a consensus that the local temperature of the filament is very high and this temperature can only increase further when the cell is switched on and off equentially and frequently. For a cell switched frequently, this temperature due to $Q_{tot}>Q$ can only increase.

We turn, for a moment, our attention to the formation of the conductive state at a low I_{CC}. Since at a low I_{CC} a weak filament is highly resistive with a constriction at the tip of the truncated cone shaped filament, the area of contact formed with the Cu electrode is smaller than the area of contact with the Pt electrode (see Fig. 6.5(a)). Hence, one would expect a more efficient heat transport from the filament to the Pt line rather than to the Cu line. Hence, based on this argument one would expect cells neighboring the heated cell and disposed along the Pt line should experience a larger heat transfer than the neighbors disposed along the Cu line. We now look at the impact of heat transfer along the Pt and Cu electrodes and compare the results in Table 6.1.

6.4.1   Degradation of Cells Disposed along the Pt Electrode

The neighbor cells located on the Pt electrode line are characterized, one by one, immediately (i.e. within 45-55 sec) after heating of the heated cell marked by a red dot after the

device heating. The metric for degradation is established customarily by degradation defined in this context as D = (Max of an unheated cell - Max for sample cell affected by thermal cross-talk) /(Max of an unheated cell). The mean of Max for an unheated cell has been found to be 12.7 set-
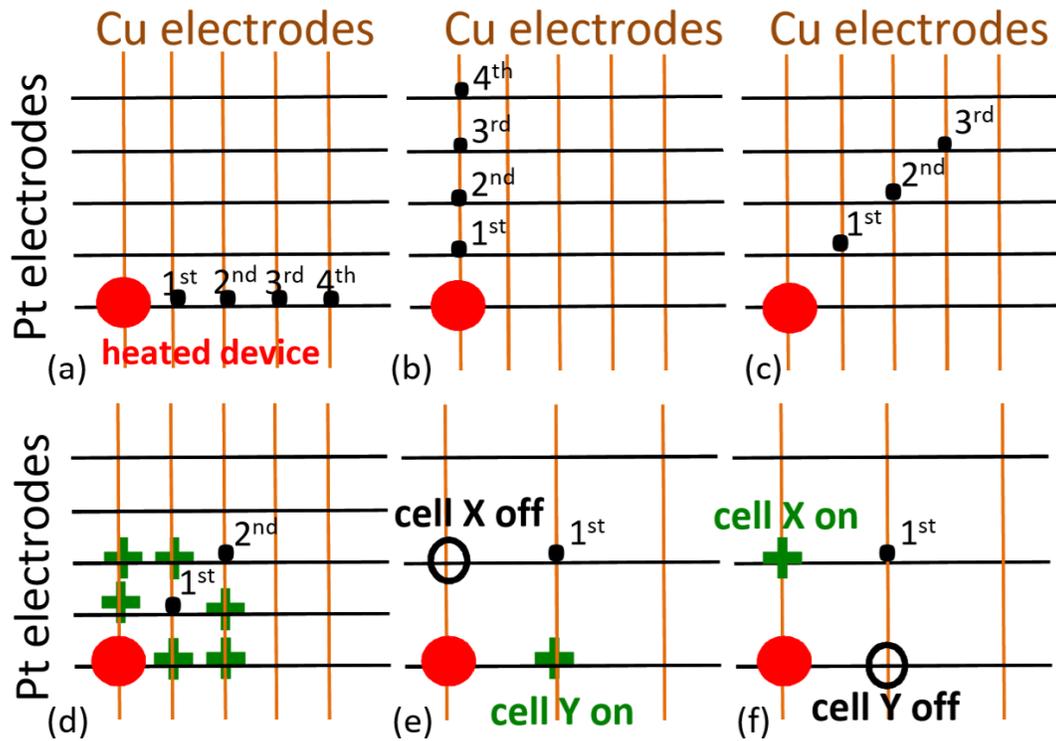
Fig. 6.4: *Location of neighbor cells relative to the heated cell marked by a red dot. Initially the cells are set in an Off-state. (a) heat transport from the heated cell to its neighbors located on the Pt electrode. (b) heat transport to its neighbors on the Cu electrode. (c) heat transport to its neighbors located diagonally with respect to the heated cell. (d) heat transport to its neighbors on diagonal locations with intermediate cells (marked by green crosses) in the ON-state. (e) thermal path from the heated cell to 1st cell via the cell Y. (f) thermal path from the heated cell to 1st cell via the cell X*

reset cycles. The cell degradation results for cells disposed along the Pt electrode are shown in Table 6.1 based on 66 devices being measured. It can be seen that for the nearest neighbors the degradation is about 67%. In contrast, the degradation of the 4th device located on the Pt electrode

is much smaller, D = 13%. The results could be explained by the heat transfer over a distance of n × 150 μm where n=1, 2, 3, 4, corresponding to the 1st, 2nd, 3rd, 4th neighboring cell. Since the memory array has been manufactured on a Si wafer with a grown field oxide of 650 nm thickness, it is reasonable to assume that the main heat transfer is effected mainly via the metal lines.

The switching behavior of a cell B is impacted whenever a neighboring cell A went through a repeated switching cycles. This means, quite surprisingly, that the thermal cross-talk is effective over distances of multiple of 150 μm. At the same time, this means that the electrode lines cannot be assumed to be effective heat sinks even for devices subject to no electrical stress. The heat transport over such large distances is further supported by the experimental dependence of the effect on the width of the metal lines. For wider Pt line (35 μm) the next neighbor is degraded much less (Max = 6) than for a narrow Pt line (10 μm) cell, Max=3, as the heat is dissipated faster along the wider 35 μm Pt line.

6.4.2   Degradation of Cells Located along the Cu Electrode

The neighbor cells of the heated memory cell disposed now along the Cu electrode (Fig. 6.4(b)) are characterized analogously. The degradation results are summarized in Table 6.1 (Cu electrode) based on 53 tested cells. The degradation in terms of Max for cells located on the Cu line is significantly larger than of those cells disposed on the Pt electrode. It can be observed that for the Cu line, the distant neighboring cells are more severely degraded than those for the Pt electrode. Comparison of the 4th cell on the Pt electrode with the 4th cell on the Cu electrode shows that the degradation of is 5 fold larger for the Cu electrode. This appears to be consistent with the much better heat conductivity of Cu (385 W/(mK) and 150 nm thick) lines than Pt (72 W/(m.K)

and 50 nm thick) lines, but is at odds with the assumptions of much larger contact area of the Cu CF with the Pt than with the Cu electrode, as discussed before. Also here we find the same line width dependence as for Pt lines. The next neighbor is degraded much less for a wide Cu line of 35 µm than for a narrower Cu line of 5 or 10 µm.

6.4.3   Degradation of neighboring cells with neither Pt nor Cu Electrodes in Common Lines with the Heated Cell

Fig. 6.4(c) shows four neighbor cells of the heated device but not sharing any of the Pt and Cu electrodes with it. The cells in Fig. 6.4(c) are electrically characterized for two different

Table 6.1: Degradation D of the neighbor cells of the heated device

# Neighbor	Neighbor Cell to the Heated Cell Along Pt Metal Line				Neighbor Cell to the Heated Cell Along Cu Metal Line			
	1st	2nd	3rd	4th	1st	2nd	3rd	4th
D%	67	53	40	13	80	75	70	67

conditions: 1) the cells between the hot cell and the tested cell are in a non-conductive state, and 2) the intermediate cells are preset to a conductive state at I_{CC}=100 µA shown in Fig. 6.4(d) by the green crosses. The I_{CC}=100 µA ensures that a low resistance Cu filament is formed with R_{ON} typically between 450 Ω and 550 Ω. Such a low resistance, robust filament is assumed to provide a path of high thermal conductivity between Pt and Cu electrode.

In the first case, as could be expected, we find no degradation of maximum switching cycles Max for any of the diagonal neighbors of the heated device. This can be explained by the absence of any continuous thermal path between the devices. When, however, the cells marked by green crosses are preset in a conductive, i.e. LRS, state (see Fig. 6.4(d)), the targeted neighboring cell is found to be degraded considerably. A degradation of D = 19% is found for the 1st diagonal

neighbor. The product of degradation $0.67 \times 0.80 = 0.53$ (see Table 6.1) being larger than 0.19 indicates that the Cu filament despite its nanometer cross-section but, apparently by virtue of its small length of 25 nm, provides an efficient conduit for the heat transport. We conclude that the thermal cross-talk along the Cu electrode is circa 15 fold more efficient than along the Pt electrode. It is known that the heat transport is proportional to the temperature gradient, to the wire cross-section, to the thermal conductivity of the material, and inversely proportional to the length of the wire. The higher heat transport over the Cu line would indicate that the high conductivity of the Cu line more than compensates for the small contact area between the filament and the Cu electrode. The cross-section of the filament, assumed to be of cylindrical shape, is estimated to be about 15 nm. When the thermal conductivity of the Cu filament is assumed to be roughly half of the thermal conductivity of bulk Cu, ie. around 190 W/m.K then one could conclude that the heat transport via Cu filament 25 nm long is comparable with the heat transport along the Pt electrode over a distance of ~150 μm, assuming similar contact areas with the Cu and Pt electrodes.

It should be noted that in case of the 1st diagonal device as shown in Fig. 6.4(d) there exist two thermal conduction paths between the heated cell and the 1st diagonal cell. Evaluation of the electrical degradation of the 1st diagonal cell with intermediate cells partly in LRS and partly in HRS states as shown in Fig. 6.4(e) and Fig. 6.4(f) reveal that the two individual paths contribute differently to the degradation of the probed diagonal devices. The path first along the Cu and then along the Pt electrode (Fig. 6.4(f)) causes a more severe degradation of the 1st diagonal cell than the conductive path first along Pt and then along the Cu electrode as shown in Fig. 6.4(e). In case of Fig. 6.4(e), the degradation of the 1st diagonal cell is 7%; and in case of Fig. 6.4(f)) the degradation of the 1st diagonal device is 11%. This can be compared to the degradation of the 2nd cells along Cu and Pt line, which are 75% and 53%, showing that the thermal connection by dint

of Cu filament poses a heat transfer bottleneck. It shows also that the two paths contribute constructively and additively to the overall degradation of (7%+11%) ≈ 19%. Testing the degradation of the neighbor cells as a function of the width of the metal lines, which in our case vary between 5 μm and 35 μm, we find that for a Cu line of 35 μm it takes less time to reach the 4th neighbor than for a narrow Cu line of 5 or 10 μm.

6.5   Revised Shape of Cu Filament

According to well known truncated shaped cone theory (Fig. 6.5a), bottom electrode (Pt) line has a broad base contact with filament than Cu line and is expected to transfer heat more efficiently. However, measured degradation results indicate that heat transfer from cell to cell is 15× more efficient (thickness x heat conductivity) over Cu than over Pt line.

A more plausible explanation of the more predominant heat transport over the Cu line can be achieved assuming a revised shape of the Cu CF. Rather than a truncated cone shape Fig. 6.5(c), an hourglass shape is hypothesized for the Cu CF with a constriction, the locus of the highest temperature during the reset operation, shifted deeper into the TaO_x. A modified shape of the filament is shown in Fig. 6.5 (b) and (c). For low I_{CC} the hourglass shape has a large base with Pt electrode and a small base with the Cu electrode (Fig. 6.5(b)). As the I_{cc} increases the base with Cu grows while the base with Pt stays more or less constant (Fig. 6.5(c)) and the constriction of

the filament will thicken and the contact area will increase compared with filament formed at a lower I_{CC} [Fig. 6.5(b)]. The hourglass-shaped filament would be more consistent with our data as
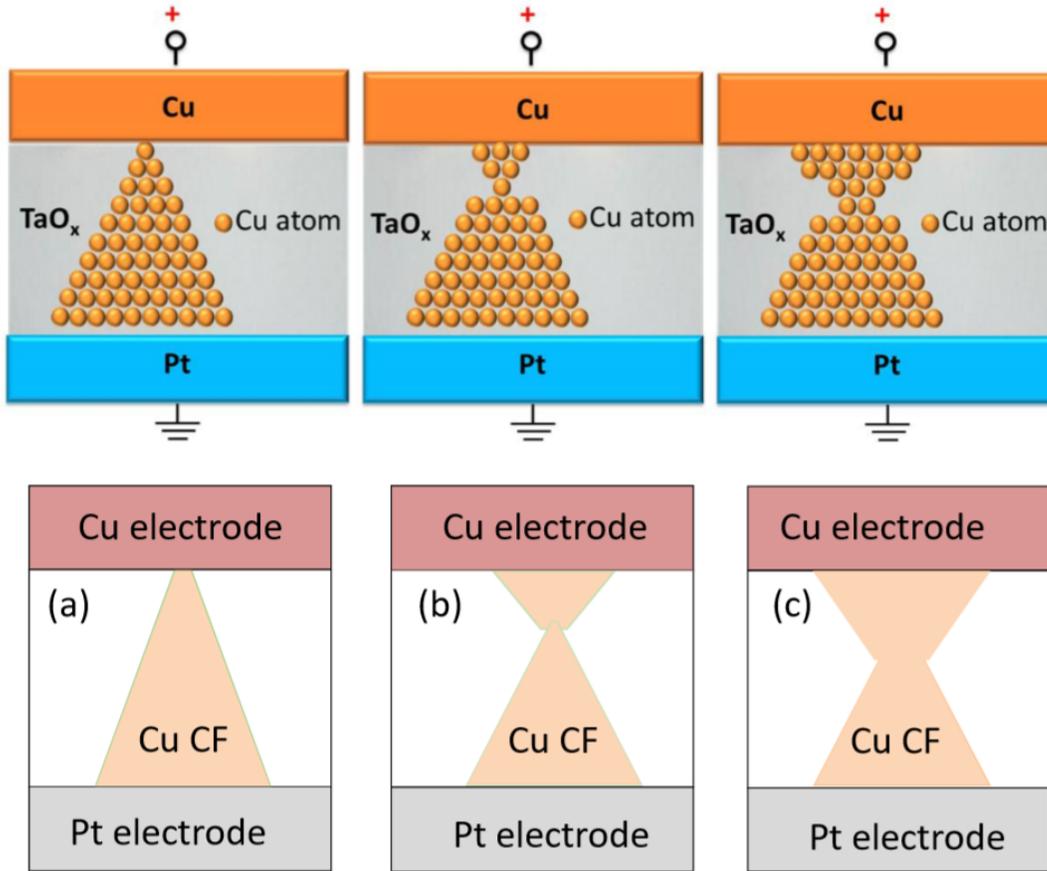
Fig. 6.5: *Different geometrical shapes approximating the actual form of a Cu filament: (a) conventionally assumed shape of a truncated cone. (b) an hourglass-shaped filament formed at low I_{CC}. (c) an hourglass-shaped filament formed at high I_{CC}*

it provides now a larger contact area with the Cu electrode and would thus explain the large heat transport from the filament along the Cu electrode line to the neighboring cells along the Cu electrode.

6.6   Potential Solutions for Cell-to-Cell Thermal Degradation Problem

In this work it is experimentally demonstrated that during repeated consequtive set/reset (or switching) operation, the heat dissipation can spread along the electrode lines and affect the performace of the neighboring cells. This degradation of the neighboring cells is more severe along
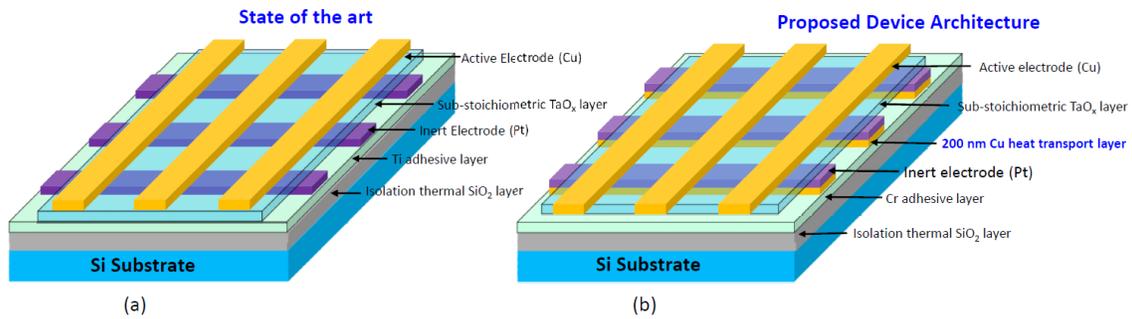
Fig. 6.6: *Cross-section schematic of ReRAM devices with different layers specified for a)Pt inert-elctrode based state of the art device; b) Engineered inert-electrode module based proposed novel device*

the copper (Cu) electrode line than along the platinum (Pt) electrode line. One observes that cells nearest to the heating source cell (cell subject to repeated switching operation) are affected most and this degradation effect gradually degrades as we go far away from the source cell.

One possible solution to this problem is to provide a faster heat dissipation where heat can be transported much more quickly along the electrode lines. Faster heat dissipation would mean that the neighboring cells are exposed for a shorter time to the transient heat and to lower peak temperatures and hence suffer less degradation. This can be achieved through an engineered inert-eletrode module with a thick (200 nm or more) copper heat transport layer which can act as a heat sink. Figure 6.6(b) shows the cross section schematic of this enginerred inert-electrode module along with its various layers specified. The proposed device structure has been fabricated and characterized. It is found that 200 nm Cu heat transport layer leads to a much higher maximum

number of switching cycles for all the neighbor cells along the Cu eletrode lines as well as for

neighbor cells along the Pt electrode lines. In other words, all the neighbor cells are found to be

unaffected by source cell heating effect and therefore exhibit the same number of switching

Table 6.2: R_{ON} of preset filament set at I_{CC}=100 μA before and after heating the source cell with I_{CC}=10 μA, rr=2 v/s for 13 switching cycles

Source cell			neighbor cell RON (ohm)			
			along Pt electrode		along Cu electrode	
			before heating	after heating	before heating	after heating
rr (v/s)	Icc (uA)	1st neighbor	500	500	500	500
		2nd neighbor	500	500	500	500
2	10	3rd neighbor	500	500	500	500
		4th neighbor	500	500	500	500

cycles as that of a fresh cell. This observation indicates that for commercial memory arrays with

much smaller pitch than in our memory crossbar arrays the heat accumulated in a heated device

will linger for a long time, posing thus serious problem for commercial memory arrays with a

Table 6.3: R_{ON} of preset filament set at I_{CC}=100 μA before and after heating the source cell with I_{CC}=10 μA, rr=0.1 v/s for 13 switching cycles

Source cell			neighbor cell RON (ohm)			
			along Pt electrode		along Cu electrode	
			before heating	after heating	before heating	after heating
rr (v/s)	Icc (uA)	1st neighbor	500	3.00E+05	500	1.30E+07
		2nd neighbor	500	5.00E+05	500	5.00E+06
0.1	10	3rd neighbor	500	5.00E+05	500	8.40E+06
		4th neighbor	500	5.00E+05	500	1.30E+06

line pitch of a few to tens of nanometer. However, it can be noted that in this methodology to

characterize the degradation, there is an inherently 30-45 sec time delay between heating the source

cell and then moving the probes and start testing the neighbor cells. Although the thermal

degradation of the neighbor cells appear to be virtually eliminated by incorporating the additional

Cu heat transport layer, some heat might still be dissipated along the electrode lines and affect the neighbors within that small time interval used to switch the probing needles on the probe station.

To further investigate the thermal degradation effect in detail, a preset filament with an $I_{CC}= 100\mu A$ is formed at the first neighbor cell along one electrode line and its R_{ON} value is recorded. Then the source cell is switched back and forth for 13 cycles (with $I_{CC}=10~\mu A$ and rr= 2V/s and 0.1 v/s for set and reset process respectively) and immediately after heating the R_{ON} value of the preset filament of the first neighbor cell is verified. If there is no thermal degradation, the R_{ON} value of the preset filament will be unchanged. This process is repeated for all the four

Proposed Best-Possible Device Architecture
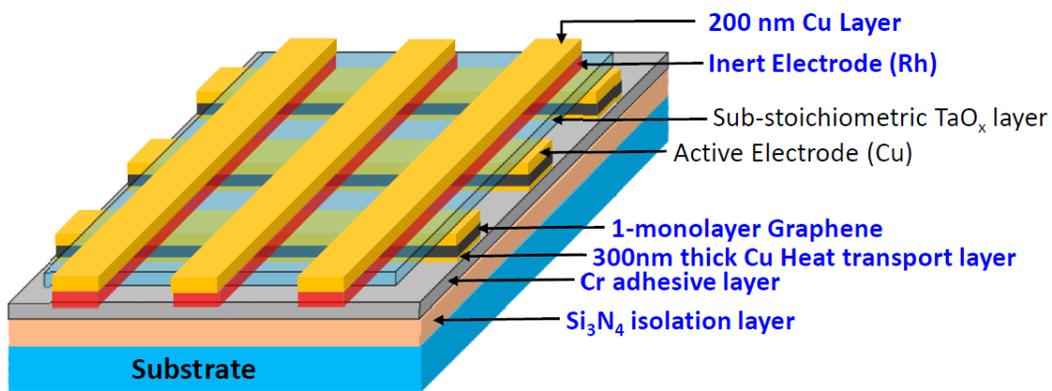
Fig. 6.7: *Cross-section schematic of engineered inter-electrode module based proposed best possible ReRAM device architecture*

neighbors along Pt electrode as well as along Cu electrode line. The test results are summarized in Table 6.2. It can be seen that the preset filament is unaffected by the heat generated during 13 switching cycles of source cell (until it becomes temporarily volatile) with ramp rate rr= 2v/s. However, if more heat is generated by switching the source cell with a ramp rate, rr=0.1 v/s (instead of 2 v/s), the R_{ON} value of the preset filament set at $I_{CC}=100$ uA is changed. Again, this degradation

is more severe as we go closer to the source cell and the degradation diminishes as we move far away from the source cell. Table 6.3 shows the thermal degradation for the source cell switched with a ramp rate rr=0.1 v/s.

However, the best possible ReRAM device solution would be incorporating an engineered inert-electrode module with an extremely high thermal conductive layer such as graphene monolayer (thermal conductivity, 3000-5000 W/m.k). Figure 6.7 shows the schematic cross section of the posposed device architecture which is expected to provide the best possible

Table 6.4: Dimension of various layers for benchmark device as well as engineered inert-electrode modeule based proposed novel device

Benchmark Device			Improved Device			
Material	Thickness (nm)	Thermal Conductivity (W/m.k)	Material	Thickness (nm)	Thermal Conductivity (W/m.k)	Purpose
Cu	100	385	Cu	200	385	Top Electrode
TaOx	25	4	TaOx	25	4	Dielectric
Pt	50	72	Rh	50	150	Bottom Electrode
Ti	20	20	Cr	20	94	Adhesive Layer
			Graphene	1-monolayer	3000-5000	Heat Transport Layer
SiO_2	750	1.4	Si_3N_4	750	43	Isolation Layer

endurance and relaibility of ReRAM cell array. A list of all materials and thickness of its various layers along with its thermal properties for both Pt based benchmark device as well as for proposed novel device structure have been listed in Table 6.4.

6.7   Summary of the Observtions

This observation indicates that for commercial memory arrays with much smaller pitch than in our memory crossbar arrays the heat accumulated in a heated device will linger for a long

time, posing thus are serious problem for commercial memory arrays with a line pitch of a few to tens of nanometer.

In terms of thermal conductivity of the electrode material, this creates a dilemma as to the suitable choice of the electrode material: an electrode material of high thermal conductivity would induce a quicker heat dissipation of the heated device and allow a quicker return to the undegraded switching behavior than an electrode material characterized by low thermal conductivity. However, in the case of higher thermal conductivity material, the more distant cells in the crossbar array would be affected more than in the case of low thermal conductivity electrode material. The optimum choice of the thermal properties of the electrodes should be gated by the way the memory array is being programmed and more importantly how it is being erased, since most heat is dissipated during the reset operation.

In terms of thermal modeling of the heat dissipation in resistive memory cells, the results shown here indicate that the electrodes of the ReRAM cell cannot be treated as perfect heat sinks. These results indicate that the local temperature of the metal lines may exceed considerably the ambient room temperature assumed frequently in some thermal models. The perfect sink property of the electrode has been assumed on the grounds that the electrode lines are much more massive than a Cu filament in a cell. Our results show that this assumption is incorrect.

6.8   Conclusions

It is experimentally found that the heat deposited in a cell stressed by frequent switching is transported to the neighboring cells causing their serious degradation in terms of electrical performance. Since the degradation of the cell performance occurs only when a cell nearby undergoes repeated switching cycles, its observed degradation, in absence of other discoverable

factors, has been attributed to the impact of the heated cell in which heat is being dissipated over ~13 switching cycles.

The neighbor cells disposed along one of the electrode common with the heated device degrade most with neighbor cells located along the Cu electrode degrading much more than the cells located along the Pt electrode. Cells with no electrode lines in common with the heated cell experience electrical degradation in terms of maximum switching cycles only in the case when an continuous thermal path is provided between the probed neighbor and the heated cells. This occurs when the intermediate cells along the Cu and Pt line shared with the heated device (as in the electrical sneak path problem) are set into an LRS state. Thus the electrical sneak path problems has its analogue in thermal transport. It has been also shown that electrical performance of a memory cell can be used as a probe into heat transfer phenomena.

PART-2: Neuromorphic Semi-Organic Devices on Flexible Substrates

Memristor devices hold the promise of a realization of neuro-inspired computing with neuromorphic functionality implemented on truly neuromorphic hardware. Due to the advantages of good scalability, flexibility, low cost, ease of processing, 3D stacking capability, and large capacity for data storage, polymer-based memristors on flexible substrates look highly attractive, e.g. as wearable electronics. In this work the progress of realization of such devices are demonstrated starting with a benchmark, inorganic memristor manufactured on Si substrate which are well-characterized [13]. Such filamentary and phase-transition memristors on Si have been

successfully modeled [14] according to Chua's theory [15] in terms of electric flux ϕ and total charge q only (q= q(ϕ)), independent of any specific current or voltage driving input.

Here manufacturing and characterization of such semi-organic devices starting with a well characterized Metal-Insulator-Metal structure (Cu/TaO$_x$/Pt/on Si) manufactured on a Si substrate and step by step replacing the switching layer (TaO$_x$) and the substrate by organic polymers are illustrated. The four derivative devices manufactured are: Cu/O-AA/Al/on Si, Cu/O-AA/Pt/on Si,

Material	SiO$_2$	Cr	Al/Pt	OAA	Cu	Au	P3HT (PGN)
Thickness (nm)	750	210	50	50	150	60	650
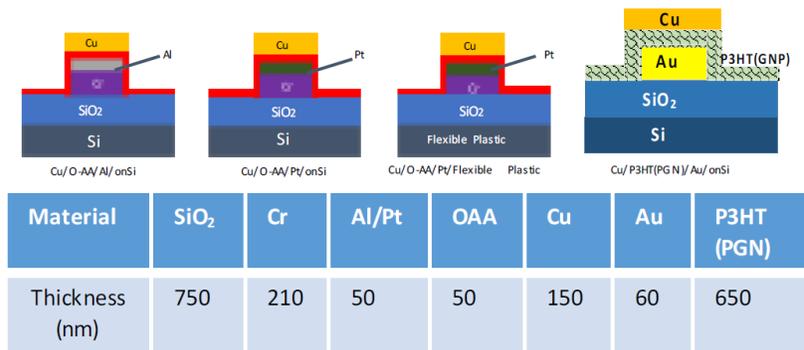
Fig. 6.8: Cross-sections of four semi-organic devices derived form the inorganic Cu/TaOx/Pt device. All devices have an organic active switching layer. One of such devices has been manufactured successfully on a flexible substrate. The last device has organic switching layer of P3HT polymer with suspended graphene

Cu/O-AA/Pt/Flex, and Cu/P3HT(GNP)/Au/on Si whose cross-sections are shown in Fig. 6.8. Here O-AA stands for polymer o-anthranilic acid, Flex for flexible substrate, P3HT for 3-hexylthiophene polymer, GNP for graphene nanoplatelets powder suspended in P3HT. It is found that: a) conductivity of O-AA increases with increasing concentration of anthranilic acid, b) concentration of graphene nanoplatelets in P3HT modifies conduction properties of the active switching layer from insulator to metallic conductivity. Those technology parameters may help tune the neuromorphic properties of the respective devices.

All derivative semi-organic devices display characteristic current-voltage pinched

262

hysteretic loop under periodic voltage excitation, very similar to the benchmark device Cu/TaOx/Pt/on Si, demonstrating that the replacement of inorganic by organic materials has successfully preserved the basic memristive properties. Fig. 6.9 (a) shows a general I-V characteristic for all devices with the threshold voltages, V_{SET}, and V_{RESET}. Fig. 6.9 (b) shows I-V for Cu/O-AA/Al/on Si and Cu/O-AA/Pt/on Si. Fig. 6.9 (c) shows the same I-V for Cu/O-
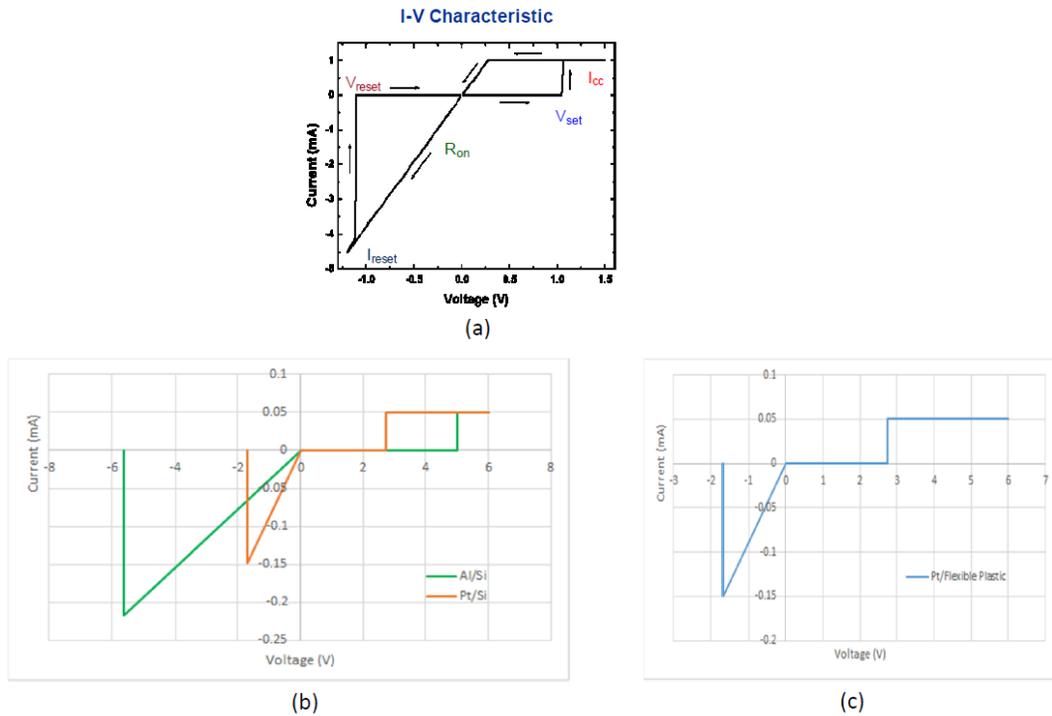
Fig. 6.9: *a) General I-V characteristics for the devices in this work with switching threshold voltages V_{set} and V_{reset} for Cu/TaOx/Pt device; b) I-V characteristics for devices with polymer switching layer O-AA on Si substrate: Cu/O-AA/Al/on Si and Cu/O-AA/Pt/on Si; c) I-V characteristic for Cu/O-AA/Pt/Flex device with polymer switching layer O-AA and flexible polymer substrate*

AA/Pt/Flex. In case of the P3HT device, in addition, to the I-V hysteresis, Fig. 6.10 (a), quantized conductance is observed at no magnetic field and at 300K with integer multiples of $G_o = 2e^2/h$ (=12.91 kΩ^{-1}), and in some devices with partially quantized, $(n/7) \times G_o$ as shown in Fig. 6.10 (b)

[16].

(a)   (b)
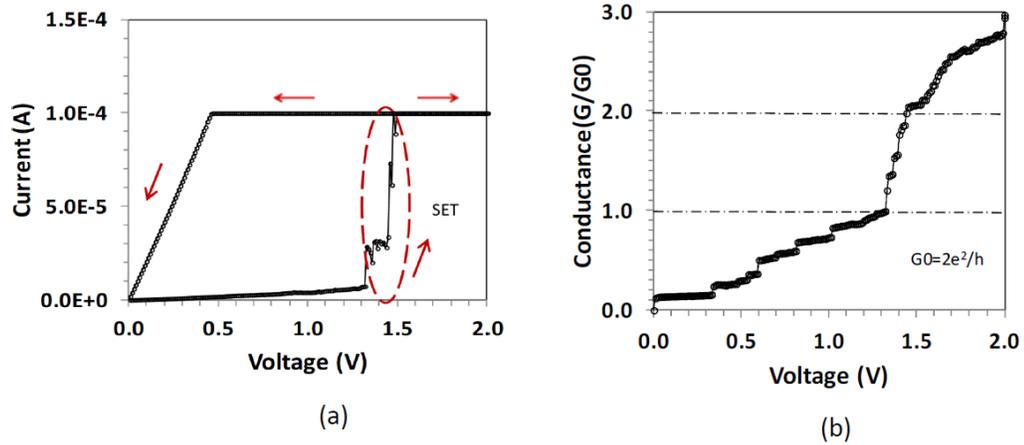
Fig. 6.10: *a) I-V characteristics of a Cu/P3HT(PGN)/Cu/on Si withP3HT polymer doped with graphene*

nanoplatelets (GNP conc.: 0.1 mg/ml) with a Icc = 0.1 mA; b) Conductance of the set operation as function

of voltage for the device Cu/P3HT(PGN)/Cu/on Si. Integer and partial quantization of the conductance is

observed. Reprinted with permision from [16], Copyright, Nanoscale Research Letters (2016)

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Chapter 7: Conclusion and Future Remarks

The main focus of this research is to explore the inert electrode, inert electrode/solid-electrolyte interface and the inert-electrode module (inert -electrode, adhesive layer and thermal oxide) on the performance, reliability and endurance of ReRAM memory cell or array arrangement. By exploring several materials the best potential candidates for inert-electrode are short listed and investigated in the view of material analysis as well as electrical characterization of the ReRAM device. The root-cause analysis have been conducted to find the atomistic reasons that might limiting the device performance. Several solutions have been proposed and experimentally verfied by fabricating ReRAM device in accordance with the proposed solution. The significance improvement of the device performance and mitigation of the limiting cases has also been improved. In the future, more investigations can be pursued in the following areas:-

i.   Verically stacked multilayer 3D ReRAM is the promising future of ReRAM technology. The cell-to-cell degradation need to be investigated for 3D ReRAM and novel device architecture as well as new materials and processes need to be explored to realize high density 3D memory solutions

ii.   Further research is required to investigate the diffusion of cations in different composition of solid electrolyte and the subsequent impact of filament shape- conical or inverted-conical shape. The narrowest region of the tip and the corresponding electrode/solid electrolyte interface is one of the factor affecting device performance and reliability

iii. Comprehesnive TCAD modeling and simulations need to be conducted to see the impact of defect levels in the solid-electrolyte and the corresponding impact on filament geometry, thermal transport and cell-to-cell thermal degradation. However, accurate models need to

be developed and validated first to properly incoprporate the physical mechanism occuring in the ReRAM cells during SET and RESET operations. Novel solutions can also be explored using simulation tools which can significantly minimize experimental time and expense. The optimized and properly modeled device can then be fabricated and the proposed novel architecture can be experimnetally verified in an economic and fast possible way.

iv. Novel cell management algorithm can be devleped considering the cell-to-cell thermal crosstalk effect demonstarted for the first time experimentally in this research specially for the RESET operation. This will significantly alleviate cell-to-cell thermal degradation effect and will improve the device performance and reliability by several orders of magnitude.

List of Publications

This dissertation contains the following publications

[1]   H. An, **M. Al-Mamun**, M. Orlowski and Y. Yi, "Robust Deep Reservoir Computing with Reliable Memristor Design with Heat Dissipation Enhancement Feature", IEEE Transactions on IEEE Nanotechnology, Oct. 2019 (submitted)

[2]   **M. Al-Mamun,** S. W. King and M. Orlowski "Heat Transfer Proximity Effects in Resistive Memory Crossbar Arrays", AVS 66th International Symposium & Exhibition, Oct. (2019).

[3]   **M. Al-Mamun** and M. Orlowski, Parasitic Cell-to-Cell Heat Transfer in ReRAM Arrays and Thermally Induced Memory Cell Performance Degradation, (manuscript in preparation for ECS Journal of Solid-State Science and Technology)

[4]   **M. Al-Mamun** and M. Orlowski, "Thermal and Chemical Integrity of Ru Electrode in Cu/TaOx/Ru ReRAM Memory Cell", Journal of Solid-State Science and Technology, Oct. (2019) (under review)

[5]   **M. Al-Mamun** and M. Orlowski, "Performance Degradation Due to Nonlocal Heating Effects in Resistive ReRAM Memory Arrays". MRS Advances, 1-8.265, (2019).

[6]   **M. Al-Mamun** and M. Orlowski, "Performance Degradation due to Nonlocal Heating Effects in Resistive ReRAM Memory Arrays", *MRS Spring Meeting and Exhibit*, April 22-26, Phoenix, Arizona, (2019).

[7]   **M. Al-Mamun**, M. Altaf, A. Edrees, and M. Orlowski, "Neuromorphic Semi-Organic Devices on Flexible Substrates", *Workshop on Innovative Nanoscale Devices and Systems*, Hawaii Nov. (2018).

[8]   **M. Al-Mamun**, S. W. King, S.R. Meda and M. Orlowski "Impact of the Heat Conductivity of the Inert Electrode on ReRAM Performance and Endurance", *ECS Trans*. Vol. 85, issue 8, 207-212, (2018).

[9]   H. An, **M. Al-Mamun**, M. Orlowski and Yang Yi "Learning Accuracy Analysis of Memristor-based Nonlinear Computing Module on Long Short-term Memory", *International Conference on Neuromorphic Systems (ICONS)*, July 23 - 26, 2018

[10]   **M. Al-Mamun** and M. Orlowski, "Instability of high resistance conductive filaments in RRAM cells during the READ operation", *MRS Spring meeting and exhibit*, April 2-6, , Phoenix, Arizona, (2018).

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