Impact of Device Parametric Tolerances on Current Sharing Behavior of a SiC Half-Bridge Power Module

Grace R. Watt

Thesis submitted to the faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

Master of Science
In
Electrical Engineering

Rolando Burgos, Chair
Khai D. Ngo
Guo-Quan Lu
Christina M. DiMarino

December 9, 2019
Blacksburg, Virginia

Keywords: SiC MOSFET, power module packaging, flexible PCB, current sharing, symmetrical direct bonded copper (DBC) layout, diode-less module, multi-chip module, device parametric tolerances, package parasitics, vertical GaN
Copyright 2019, Grace R. Watt

Impact of Device Parametric Tolerances on Current Sharing Behavior of a SiC Half-Bridge Power Module

Grace R. Watt

This paper describes the design, fabrication, and testing of a 1.2 kV, 6.5 mΩ, half-bridge, SiC MOSFET power module to evaluate the impact of parametric device tolerances on electrical and thermal performance. Paralleling power devices increases current handling capability for the same bus voltage. However, inherent parametric differences among dies leads to unbalanced current sharing causing overstress and overheating. In this design, a symmetrical DBC layout is utilized to balance parasitic inductances in the current pathways of paralleled dies to isolate the impact of parametric tolerances. In addition, the paper investigates the benefits of flexible PCB in place of wire bonds for the gate loop interconnection to reduce and minimize the gate loop inductance. The balanced modules have dies with similar threshold voltages while the unbalanced modules have dies with unbalanced threshold voltages to force unbalanced current sharing. The modules were placed into a clamped inductive DPT and a continuous, boost converter. Rogowski coils looped under the wire bonds of the bottom switch dies to observe current behavior. Four modules performed continuously for least 10 minutes at 200 V, 37.6 A input, at 30 kHz with 50% duty cycle. The modules could not perform for multiple minutes at 250 V with 47.7 A (23 A/die). The energy loss differential for a ~17% difference in threshold voltage ranged from 4.52% (~10 μJ) to -30.9% (~30 μJ). The energy loss differential for a~0.5% difference in V_{th} ranged from -2.26% (~8 μJ) to 5.66% (~10 μJ). The loss differential was dependent on whether current unbalance due to on-state resistance compensated current unbalance due to threshold voltage. While device parametric tolerances are inherent, if the higher threshold voltage devices can be paired with devices that have higher on-state resistance, the overall loss differential may perform similarly to well-matched dies. Lastly, the most consistently performing unbalanced module with 17.7% difference in V_{th} had 119.9 μJ more energy loss and was 22.2°C hotter during continuous testing than the most consistently performing balanced module with 0.6% difference in V_{th}.

Impact of Device Parametric Tolerances on Current Sharing Behavior of a SiC Half-Bridge Power Module

Grace R. Watt

GENERAL AUDIENCE ABSTRACT

This paper describes the design, construction, and testing of advanced power devices for use in electric vehicles. Power devices are necessary to supply electricity to different parts of the vehicle; for example, energy is stored in a battery as direct current (DC) power, but the motor requires alternating current (AC) power. Therefore, power electronics can alter the energy to be delivered as DC or AC. In order to carry more power, multiple devices can be used together just as 10 people can carry more weight than 1 person. However, because the devices are not perfect, there can be slight differences in the performance of one device to another. One device may have to carry more current than another device which could cause failure earlier than intended. In this research project, multiple power devices were placed into a package, or "module." In a control module, the devices were selected with similar properties to one another. In an experimental module, the devices were selected with properties very different from one another. It was determined that the when the devices were 17.7% difference, there was 119.9 μJ more energy loss and it was 22.2°C hotter than when the difference was only 0.6%. However, the severity of the difference was dependent on how multiple device characteristics interacted with one another. It may be possible to compensate some of the impact of device differences in one characteristic with opposing differences in another device characteristic.

Acknowledgements

I would firstly like to acknowledge the financial support provided by the U.S. Department of Energy Advanced Manufacturing Office through the Wide Bandgap Generation (WBGen) Fellowship at the Center for Power Electronics Systems (CPES) at Virginia Tech (http://www.eng.vt.edu/WBGen).

The team at General Motors, specifically Marko Jaksic and Mehrdad Teimor, were incredibly supportive and knowledgeable throughout my project. I want to acknowledge the support of General Motors and the Department of Energy, Office of Energy Efficiency and Renewable Energy (EERE), under award number DE-EE0007285, Highly Integrated Wide Bandgap Power Module for Next Generation Plug-in Vehicles.

Thank you to Dr. Rolando Burgos for his guidance in my research and navigating graduate studies. I was always grateful for the perspective he has gained from extensive experience on various power electronics projects which honed the questions I asked in research and the directions I took. Thank you to Dr. Lu and his students, Chao Ding, Langbing Lui, and Shengchang Lu. They provided invaluable expertise and recommendations for use of the sintering paste and other materials in my module. Thank you for Dr. Christina DiMarino for her expertise on packaging. It is exciting to see packaging research growing at CPES and I look forward to the contributions her team will enable. Thank you for Dr. Ngo for his research questions and guidance while I was a student at CPES. He took the time to care about my research and my life, even sharing peppers with me and offering bitter melon which I could not handle.

Significant gratitude goes to Slavko Mocevic, Amy Romero, and Joe Kozak who mentored me in my research and in graduate life. Slavko spent many hours with me going over my test setups and results and discussing theory. While I might have appreciated some sugar-coated feedback at times, his honesty and willingness to ask the difficult questions was invaluable. When I could not 100% understand my setup, normally something would break as he warned. When he reminded me of the progress I was making, I gained the confidence I needed to keep going. Thank you to Joe for all our complex conversations related to work culture, friends and relationships, religion,

or other topics in which we both enjoyed going deeper. Joe cares deeply for people and I was immensely grateful for his willingness to do the work to make graduate life increasingly better.

I cannot say enough about Emma Raszmann and how critical her friendship is to me as both a researcher and young professional. She provided patience and a lack of judgment with me that was necessary when I had doubts and questions in the research, duh. She also spent hours with me discussing life and the joys and grief it brought us whether over a drink at Cabo Fish Taco or coffee or soccer. I am thrilled for wherever her path will lead.

Special thanks to Shengchang for his willingness to enjoy Disneyland and go back for fireworks! Thanks to David Nam and Tianyu Zhao who were part of the "packaging team," as we lamented the challenges of packaging that others did not understand. We also enjoyed fun times together in our packaging team gathering complete with karaoke and delicious food.

I also want to thank many friends from CPES including Shuo, Bo, Tianyu, Sizhan, Bo Wen, Jianghui and Ye, David, Josh, Lee, John, Michael, Cong and Jiewen, Ibrahim and Danny, Daniel, Vladamir, even Chris and too many others to name.

Thank you to Genesis Alvarez who was a roommate and friend beginning during recruitment weekend and through graduation. We shared so many important moments both when school and life were so difficult and when we were having breakthroughs. I will miss our movie nights and talks and cooking and crying and laughing. We really did so much together whether it was talking about faith or playing soccer, you were dear to me. Also thank you to Sherin Abraham who joined Gen and I in our 2nd year. She ended up being such a great addition to the apartment with her laughter, energy, and conversation. She has a kind and strong heart and she is going to go far! I feel like I learned so much about life from Sherin and am excited for where God takes her.

I must acknowledge Gravitate and BCF for their role in my life while at Blacksburg. Each Thursday was a highlight of my week; laughing and digging in deep into scripture, sharing a meal and checking in on everyone, and having a community that cared deeply and understood me deeply. Christine and Russell also went above and beyond in their care for me and I will, beautifully, never be able to repay them. Thank you to Angela and Meredith for weekly meetings and all the ladies for the joy you gave me which I really cannot express.

Thank you to Na, Trish, Marianne, Audri, Yan, Teresa, David, and Linda who care so genuinely and thoroughly for us. These people brought joy to me whenever I was upstairs or when we had meals together. I would have gone barefoot at my wedding without Trish. Na, Elianne, and Annabelle as well as Dad and Grandma were like a family away from home even though we were only friends for half the time I was there. You invited me into your home and lives, and I know God has amazing plans for your family.

To LAIGSA and SHPE, especially the executive board for LAIGSA, you all were friends and co-workers in a community that was dear to me. I learned so much from working with you about how to run an organization and care for graduate students. Whether we were setting up for salsa, the holiday party, or many of our tailgates, I found our time together to be a refuge. The soccer teams mattered to me and I felt so incredibly honored to join our team.

Lastly, and perhaps most important, I must thank Jesus and my family and dearest friends. Without you, I would have curled up into a permanent cry ball the first semester. While it was difficult, the lessons I learned and love that carried me through have changed my life. I hope you can know how much your support means. Kyle, I love you and you are a patient, patient boyfriend, fiancé, and now husband.

Contents

Chapter 1 Introduction 1

1.1 Electric Vehicles 1

1.2 Power Electronics for Electric Vehicles 4

1.2.1 Semiconductors 4

1.2.2 Wide Band Gap Power Semiconductor Devices 6

1.2.3 Quasistatic Behavior of MOSFETs 8

1.2.4 Dynamic Behavior of MOSFETs 11

1.3 Multi-Chip Power Module Packaging 21

1.4 Research Motivations and Objectives 23

1.4.1 Device Parametric Tolerances 25

1.4.2 Package Parasitics 29

1.4.3 Objective 33

Chapter 2 Design of a Balanced Power Module for Automotive Applications 36

2.1 Introduction 36

2.2 Survey of Power Module Packaging Techniques and Limitations 36

2.3 Module Design 38

2.3.1 Symmetrical/Balanced DBC Pattern and Current Sharing Simulation 38

2.3.2 Die Placement based on Threshold Voltage 40

2.3.3 Flexible PCB for Gate Connection 46

2.3.4 Use of the Body Diode in SiC MOSFET 50

Chapter 3 Power Module Fabrication 52

3.1 Package Material Selection 52

3.1.1 Substrate Selection 53

3.1.2 Attachment Selection 53

3.1.3 Housing and Encapsulant Selection 55

3.2 Module Fabrication 55

3.2.1 Substrate Patterning and Cutting 55

3.2.2 Attachment Material Heat Profiles 57
3.2.3 Die Attachment 58
3.2.4 Die Interconnection 61
3.2.5 Flexible PCB Attachment 64
3.2.6 Power Terminals 70
3.2.7 Thermal Management 73
3.2.8 Housing and Encapsulant 75
3.2.9 Summary of Fabricated Module Yield 80
Chapter 4 Power Module Characterization 82
4.1 Static Characterization 82
4.1.1 Introduction 82
4.1.2 Static Results 83
4.2 Dynamic Characterization 87
4.2.1 Introduction 87
4.2.2 Gate Driver Design 89
4.2.3 Desaturation Circuit for Overcurrent Protection 91
4.2.4 Tuning the Desaturation Circuit 95
4.2.5 Capacitor Bank 98
4.2.6 Low Voltage Switching Test Results 100
4.2.7 600 V Switching Test Results 103
Chapter 5 Power Module Thermal Testing 113
5.1 Introduction 113
5.1.1 Heat Removal and Thermal Resistance Estimation 114
5.1.2 Junction Temperature Estimation 117
5.2 Continuous Test Setup 123
5.3 Continuous Test Results 125
5.4 Continuous Thermal Test Results 135
Chapter 6 Conclusion 143

Appendix A Evaluation of an Automated Modeling Tool Applied to New 600 V, 2 A Vertical Gallium Nitride (GaN) Transistors 148

Bibliography 166

List of Figures

Figure 1-1. Passenger electric car stock globally from Fig. 1.1 of Global EV Outlook 2019 [7] 2

Figure 1-2. Outlook for EV growth from EV30@30 Scenario Fig. 2 Global EV Outlook [7].. 2

Figure 1-3. Influence of charging option on customer purchase of EVs [2] 3

Figure 1-4. Block diagram of an electric vehicle powertrain [2] 3

Figure 1-5. Energy bandgaps of different types of materials 5

Figure 1-6. Material properties comparison of Si, SiC, and GaN 7

Figure 1-7. Device capacitance definitions 9

Figure 1-8. Step-by-step walkthrough of the gate charge plot 10

Figure 1-9. Ideal turn-on and turn-off waveforms for a MOSFET [18] 12

Figure 1-10. Impact of input capacitance on turn-on delay 14

Figure 1-11. Rise of the drain current as the transistor turns on 15

Figure. 1-12. Miller plateau as the transistor turns on 16

Figure. 1-13. Final behavior as the transistor turns on 17

Figure. 1-14. Turn-off delay as the gate source bias drops 18

Figure. 1-15. Miller plateau as the transistor turns off 19

Figure. 1-16. Fall of the drain current as the transistor turns off 20

Figure 1-17. Final reduction of gate-source bias as transistor turns off 21

Figure 1-18. Functions of a power module package with an example of a commerical power module (CREE CAS120M12BM2) 22

Figure 1-19. A power module package and chip are analogous to the human body and brain [30, 31] 22

Figure 1-20. Increased current carrying capacity with paralleled dies 24

Figure 1-21. Device parametric tolerances can lead to unbalanced current sharing 25

Figure 1-22. Package parasitics can lead to unbalanced current sharing 25

Figure 1-23. Simulation of static and dynamic unbalanced current sharing 25

Figure 1-24. Impact of unbalanced threshold voltages on a) turn-on and b) turn-off behavior of discrete SiC MOSFETs [20] 26

Figure 1-25. Impact of unbalanced on-state resistance on a) turn-on, b) turn-off, and c) on-state behavior of discrete SiC MOSFETs [20] 27

Figure 1-26. Thermal impact of unbalanced current sharing in discrete SiC MOSFET devices 28

Figure 1-27. a) Multi-chip half-bride power module with assymetrical pathway impedance for paralleled dies where $L_{C4} > L_{C3} > L_{C2} > L_{C1}$ and b) Improved current sharing after adjusting the wire bonds [34] 30

Figure 1-28. Impact of switching loop stray inductance mismatch on a) turn-on and b) turn-off behavior of discrete SiC MOSFETs [20] 31

Figure 1-29. Impact of common source stray inductance mismatch on a) turn-on and b) turn-off behavior of discrete SiC MOSFETs [20] 31

Figure 1-30. Addition of auxiliary source connection reduced dynamic current imbalance from a) to c) during turn-on and from b) to d) during turn-off [20] 32

Figure 1-31. Thermal comparison of a module with unbalanced and balanced parasitic inductances [37] 33

Figure 1-32. Symmetrical DBC layout with DC- trace wraparound 34

Figure 1-33. Fabricated 1.2 kV, 6.5 mΩ SiC half-bridge power module 35

Figure 2-1. Symmetrical DBC layout for symmetrical parasitic inductance in the current pathway 39

Figure 2-2. Dies in Position C and D in parallel act as the bottom side switching device 39

Figure 2-3. Simulation of the current sharing characteristics for a symmetrical and non-symmetrical design 40

Figure 2-4. 3-terminal test fixture for characterizing bare die 41

Figure 2-5. Threshold voltages of bare dies measured with the Keysight B1505a curve tracer 41

Figure 2-6. Die selection for a balanced power module (4) based on threshold voltages 42

Figure 2-7. Die selection for a balanced power module (6) based on threshold voltages 43

Figure 2-8. Die selection for a unbalanced power module (8) based on threshold voltages 43

Figure 2-9. Die selection for a unbalanced power module (9) based on threshold voltages 44

Figure 2-10. On-state resistance measurements of a subset of the CREE dies; high resistance due to the wires and pins of the test fixture 45

Figure 2-11. Resistances of bare die across multiple tests repeated with the same parameters 45

Figure 2-12. With a shared source inductance, gate and power loops are coupled and Lgs is large 46

Figure 2-13. Voltage surge in V_{ds} and gate inductance can cause gate ringing which may lead to unintentional turn on and turn off [55] 46

Figure 2-14. Connection of flexible PCB to die and substrate... 47

Figure 2-15. Overlap of kelvin source and gate planes reduces loop inductance 47

Figure 2-16. Comparison of flexible PCB and wire bond inductances simulated in Ansys Q3D 48

Figure 2-17. Adding kelvin source connection decouples the gate and power loops and reduces Lgs.. 48

Figure 2-18. Wire bond failure mechanisms [58] 49

Figure 2-19. a) Top view of the flexible PCB from Altium designer, b) bottom view of the fabricated flexible PCB, and c) substrate with dies displaying connection points for flexible PCB 50

Figure 3-1. Elements of a package 53

Figure 3-2. Partially etched DBC pattern with ferric chloride etching machine...................... 56

Figure 3-3. Patterned substrate after etching of unwanted metal using a Kapton tape mask... 56

Figure 3-4. Undesirable bend in bottom device wires b. new design (white) vs old design (red) c. New vs old substrate pattern 57

Figure 3-5. Heat profile for Kyocera nanosilver paste sintered under P=0............................. 58

Figure 3-6. Heat profile for Sn96.3/Ag3.7 [69, 70] 58

Figure 3-7. Heat profile for Sn63/Pb37 [71] 58

Figure 3-8. Laser-cut Kapton mask placed on DBC substrate... 59

Figure 3-9. Sinter paste printed into Kapton mask... 59

Figure 3-10. Dies are placed onto printed sinter paste squares and Kapton mask is removed 60

Figure 3-11. Substrate placed onto programmable hotplate.. 60

Figure 3-12. Die shear test with the Nordson DAGE 4000 Multipurpose Bondtester........... 61

Figure 3-13. Sheared die with bottom side coated in cured nanosilver sinter paste 61

Figure 3-14. tpt HB30 Heavy Wire Bonder 62

Figure 3-15. 8 cascaded wire bonds per die 63

Figure 3-16. Wire bonds tall enough to fit Rogowski coil loops underneath 63

Figure 3-17. Microscopic view of the pull test 64

Figure 3-18. Destructive wire pull test results 64

Figure 3-19. Connections with sinter method 65

Figure 3-20. Microscopic image of sinter paste not adhering to aluminum surface of die...... 65

Figure 3-21. Die with nickel:gold topcoat and space around the gate terminal....................... 66

Figure 3-22. a) Laser-cut Kapton mask dimensions, b) size perspective against tweezers, and c) only 1.13 mm between gate and source of the die.. 67

Figure 3-23. Microscopic image of a) solder masks placed onto dies, b) filled with solder paste, and c) masks removed with double-sided Kapton tape placed on substrate below flexible PCB 67

Figure 3-24. Microscopic image of a) flexible PCB secured onto die and substrate and b) tweezers used to carefully align flexible PCB pads onto the source and gate of the parallel dies 68

Figure 3-25. Microscopic image of a) flexible PCB flap pulled upward by elastic force and b) shifted flap away from the source and gate pads of the die.. 69

Figure 3-26. Fixture for use during curing of the flexible PCB connection 69

Figure 3-27. Microscopic images of screws flush against the flexible PCB flaps.................. 70

Figure 3-28. Original design of power terminals to interface with vias on the capacitor bank board 71

Figure 3-29. a. New design of power terminals with screw connections; b. the power terminals sit flush against the capacitor bank board c. which required updates including adding screw holes and extending the board 72

Figure 3-30. Updated design (Altium) of the capacitor bank replacing the via connection with screws 72

Figure 3-31. a) Final design of the power terminals b) which interface with the capacitor bank using screws 72

Figure 3-32. Solder preform sits between the baseplate and the DBC 73

Figure 3-33. Baseplate attachment process for the two test samples and x-ray image of the sample 74

Figure 3-34. C-SAM image of the voids in the solder attachment to the baseplate 74

Figure 3-35. Processing for attaching the baseplate to the power module with cured layer displayed 75

Figure 3-36. Approximate dimensions of housing to rest on the baseplate and edge of the substrate 76

Figure 3-37. Duratron U1000 PEI material and housing machined by Virginia Tech 76

Figure 3-38. Attachment of housing with generic sealant 77

Figure 3-39. a. Two parts of encapsulant are mixed producing bubbles b-c. Bubbles are removed using a vacuum d. Encapsulant is poured into the module producing bubbles e. Bubbles are removed f. Encapsulant is cured at 70°C for 4 hours 78

Figure 3-40. a. Rogowksi coil coated in Kapton tape for protection against scratching b. Rogwoski coil looping through plastic tubing and under bottom switch wire bonds.................. 79

Figure 3-41. Module 9 alternative encapsulation technique for black surface IR camera compatibility 80

Figure 4-1. Static characterization test configuration using the Agilent B1505A curve tracer 83

Figure 4-2. Static characterization test set up using the Agilent B1505A curve tracer 83

Figure 4-3. Breakdown voltage with threshold of either 1.5 kV or 100 µA leakage current; top switch is red, bottom switch is blue 84

Figure 4-4. Transfer characteristics with 10 V applied across V_{ds}; top switch is red, bottom switch is blue.. 84

Figure 4-5. On-state resistance with 15 V applied across $V_{gs;}$ top switch is red, bottom switch is blue... 85

Figure 4-6. Output characteristics with a 7, 9, 11, 13, and 15 V applied to V_{gs}; top switch is red, bottom switch is blue 86

Figure 4-7. Double pulse test setup with die current monitoring.. 88

Figure 4-8. Rogowski coil interface with module 89

Figure 4-9. Gate driver with top and bottom switch circuitry designed to be thin for the placement of the Rogowski coils 89

Figure 4-10. Pins of the flexible PCB interface with vias on the board.................................. 90

Figure 4-11. Gate driver board layout 91

Figure 4-12. Simplified schematic of the driving circuit 91

Figure 4-13. Example schematic of a desaturation circuit 92

Figure 4-14. Desaturation circuit behavior during device ON and OFF states 93

Figure 4-15. Desaturation circuit behavior during device switching 94

Figure 4-16. Desaturation circuit behavior during a short circuit event................................. 94

Figure 4-17. Desaturation circuit for this gate driver after tuning 95

Figure 4-18. Tuning desaturation response time with blanking capacitor 96

Figure 4-19. Tuning the diode voltages and desaturation threshold voltage........................... 97

Figure 4-20. Validating desaturation threshold voltage 97

Figure 4-21. Approximate current for the desaturation threshold voltage based on the output curves for the dies[83] 98

Figure 4-22. Power module screws into capacitor bank board with screw for load inductor connection 99

Figure 4-23. Test set up with Rogowski coils through the wire bonds of the bottom side die of a partially fabricated module 99

Figure 4-24. Test set up for dynamic characterization of module.. 100

Figure 4-25. Static current sharing for unbalanced and balanced modules........................... 101

Figure 4-26. Balanced module (4) turn on and turn off behavior 102

Figure 4-27. Unbalanced module (2) turn on and turn off behavior 103

Figure 4-28. 600 V DPT results for balanced modules 4 and 6 103

Figure 4-29. 600 V DPT results for unbalanced modules 8 and 9 104

Figure 4-30. 600 V DPT turn-on results for balanced modules 4 and 6 104

Figure 4-31. 600 V DPT turn-off results for balanced modules 4 and 6............................... 105

Figure 4-32. 600 V DPT turn-on results for unbalanced modules 8 and 9 106

Figure 4-33. 600 V DPT turn-off results for unbalanced modules 8 and 9 107

Figure 4-34. Simulation of unbalanced Rg in paralleled dies 108

Figure 4-35. Simulation of unbalanced Cds in paralleled dies.. 109

Figure 4-36. Simulation of unbalanced Lgs in paralleled dies.. 109

Figure 4-37. Simulation of unbalanced Lds in paralleled dies.. 110

Figure 4-38. 600 V DPT switching energy for balanced modules 4 and 6 with percent differences 111

Figure 4-39. 600 V DPT switching energy for unbalanced modules 8 and 9 with percent differences 112

Figure 5-1. Equivalent thermal resistances for each layer from junction to ambient assuming lumped capacity 114

Figure 5-2. 0° and 45° heat spreading throughout the module.. 116

Figure 5-3. Calculating the approximate area for the 45° heat spreading case 116

Figure 5-4. Estimating switching power loss for various frequencies based on switching energy loss for balanced module 6 118

Figure 5-5. Estimating switching power loss for various frequencies based on switching energy loss for unbalanced module 8 119

Figure 5-6. Estimating conduction power loss for various rms drain currents for balanced module 6 and unbalanced module 8.. 120

Figure 5-7. Estimating total power loss for various operating points for balanced module 6 and unbalanced module 8 121

Figure 5-8. Estimating junction temperature for various operating points for balanced module 6 and unbalanced module 8 ... 122

Figure 5-9. Fully fabricated module with heat sink and black liquid tape covering the face of the baseplate ... 123

Figure 5-10. Continuous, boost, test setup with equipment indicated ... 124

Figure 5-11. Continuous, boost, test setup with some equipment shown ... 125

Figure 5-12. Closer image of the continuous, boost, test setup with busbar connection ... 125

Figure 5-13. Continuous test results for balanced 6 and unbalanced module 8 at 250 V, 47.7 A input ... 126

Figure 5-14. Continuous test results for balanced modules 4 and 6 at 200 V, 37.7 A input .. 126

Figure 5-15. Continuous test results for unbalanced modules 8 and 9 at 200 V, 37.7 A input ... 127

Figure 5-16. Continuous test turn-on results for balanced modules 4 and 6 at 200 V, 37.7 A input ... 128

Figure 5-17. Continuous test turn-off results for balanced modules 4 and 6 at 200 V, 37.7 A input ... 128

Figure 5-18. Continuous static results for balanced modules 4 and 6 at 200 V, 37.7 A input 129

Figure 5-19. Continuous test turn-on results for unbalanced modules 8 and 9 at 200 V, 37.7 A input ... 129

Figure 5-20. Continuous test turn-off results for unbalanced modules 8 and 9 at 200 V, 37.7 A input, 400 V, 18.85 A output ... 130

Figure 5-21. Continuous static results for unbalanced modules 8 and 9 at 200 V, 37.7 A input 130

Figure 5-22. Total energy loss for all continuously tested modules 133

Figure 5-23. Energy loss for all continuously tested modules 133

Figure 5-24. Thermal test setup for continuous test of modules 136

Figure 5-25. After ~5 minutes, the module reached thermal equilibrium 137

Figure 5-26. Thermal image of modules 4, 6, 8, and 9 at 200 V, 37.7 A input, 400 V, 18.85 A output 138

Figure 5-27. Comparison of module 4, 6, 8, and 9 temperature for 200 V, 37.7 A input, 400 V, 18.85 A output 138

Figure 5-28. On-state resistance for modules 4, 6, 8, and 9 across switching current 139

Figure 5-29. Thermal image of modules 4, 6, 8, and 9 at 150 V, 28.3 A input, 300 V, 14.15 A 139

Figure 5-30. Thermal image of modules 4, 6, 8, and 9 at 250 V, 47.7 A input, 400 V, 18.85 A output NOT NECESSARILY AT THERMAL EQILIBRIUM 140

Figure 5-31. Module 6 after experiencing thermal runaway after 2-3 minutes at 250 V, 47.7 A input, 500 V, 23.86 A output 140

Figure 5-32. Thermal setup and image of module 9 from the side angle run at low power 141

Figure 5-33. Thermal setup and image of module 9 from the front angle run at low power 141

Figure 5-34. Thermal performance of paralleled die a high-temperature, high-frequency continuous test 142

Figure A-1. Approximate Vertical Trench MOSFET Structure 149

Figure A-2. *Power MOSFET Tool* User Interface with static characteristic curves 151

Figure A-3. Saber *Power MOSFET Tool* Subcircuit Model 151

Figure A-4. Device capacitance definitions 152

Figure A-5. Double-pulse test schematic 153

Figure A-6. Saber® (blue) overlaid on experimental (gray) SiC transfer characteristics comparison measured with a drain-source voltage of 1 V at 25°C... 155

Figure A-7. Saber® (blue) overlaid on experimental (gray) SiC output characteristics comparison measured at various gate-source voltages at 25°C 155

Figure A-8. Saber® (blue) overlaid on experimental (gray) SiC on-state resistance comparison measured with a gate-source voltage of 20 V at 25°C.. 155

Figure A-9. Saber® (color) overlaid on experimental (dash) SiC capacitance curve comparison at 25°C 156

Figure A-10. Saber® (blue) overlaid on experimental (gray) SiC gate charge curve comparison at 25°C 156

Figure A-11. Saber® (blue) overlaid on experimental (gray) Monolith SiC turn-on waveforms at a drain-source voltage of 600 V, a 20 A load current, and 3.01 Ω gate resistance at 25°C.... 157

Figure A-12. Saber® (blue) overlaid on experimental (gray) Monolith SiC turn-off at a drain-source voltage of 600 V, a 20 A load current, and 3.01 Ω gate resistance at 25°C.................... 157

Figure A-13. Saber® (blue) overlaid on experimental (gray) Vertical GaN transfer characteristics comparison measured with a drain-source voltage of 10 V at 25°C.................. 158

Figure A-14. Saber® (blue) overlaid on experimental (gray) Vertical GaN output characteristics comparison measured at various gate-source voltages at 25°C 158

Figure A-15. Saber® (blue) overlaid on experimental (gray) Vertical GaN Rds (on) characteristics comparison measured with a gate-source voltage of 10 V at 25°C 159

Figure A-16. Saber® (color) overlaid on experimental (dash) Vertical GaN capacitance curve comparison at 25°C 160

Figure A-17. Saber® Vertical GaN gate charge model curve at 25°C 160

Figure A-18. Saber® double pulse test set up with optimized parasitic elements 161

Figure A-19. Saber® (blue) overlaid on experimental (gray) GaN turn-on waveforms with optimized parasitic circuit elements at a drain-source voltage of 400 V, a 1 A load current, and 2.5 Ω gate resistance at 25°C 162

Figure A-20. Saber® (blue) overlaid on experimental (gray) GaN turn-off waveforms with optimized parasitic circuit elements at a drain-source voltage of 400 V, a 1 A load current, and 2.5 Ω gate resistance at 25°C 163

Chapter 1 **Introduction**

1.1 Electric Vehicles

The demand for electrical vehicles (EVs), whether pure electric (no engine) or hybrid (HEV), is driven by a desire to reduce the impact of car emissions on the environment, lower operating costs, increase fuel efficiency, and improve overall performance [1-5]. In December 2018, nearly 50,000 EV were sold in the US which pushed the estimated total number of EVs to over 350k in 2018 alone. This followed a trend in monthly sales gain demonstrating that EVs are increasingly popular. As of July 2019, the total sales worldwide in 2019 alone were over 1 million [6]. According to the 2019 Global EV Outlook, the 2018 global EV stock which includes battery electric vehicles and plug-in electric vehicles was over 5 million and they estimate that the total stock will continue increasing to over 250 million by 2030 (Figure 1-1-Figure 1-2). An increasing demand for EVs encourages improvement in the operating systems particular to EVs to increase the margin of benefit over conventional vehicles.

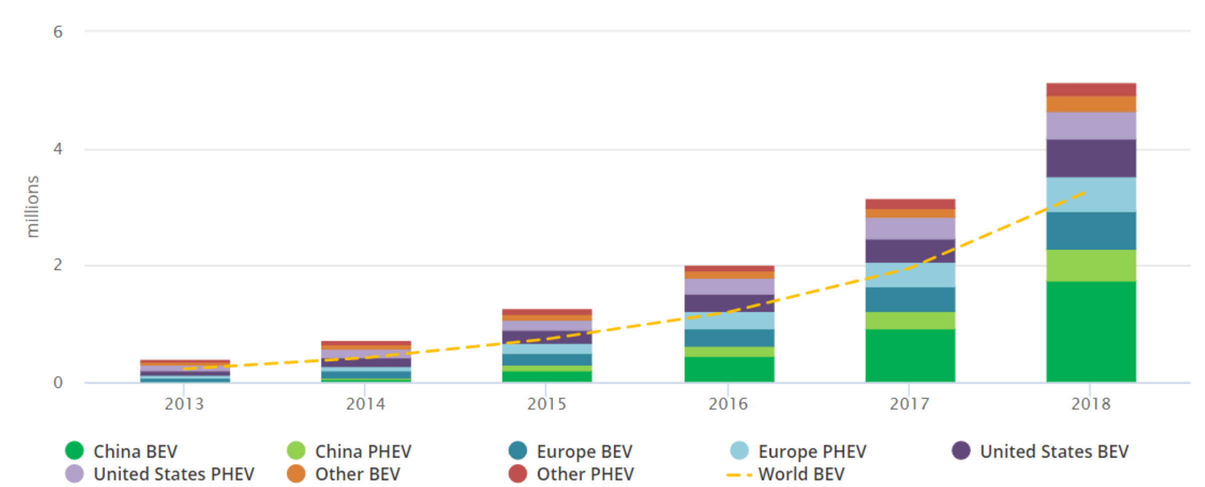


Figure 1-1. Passenger electric car stock globally from Fig. 1.1 of Global EV Outlook 2019 [7]

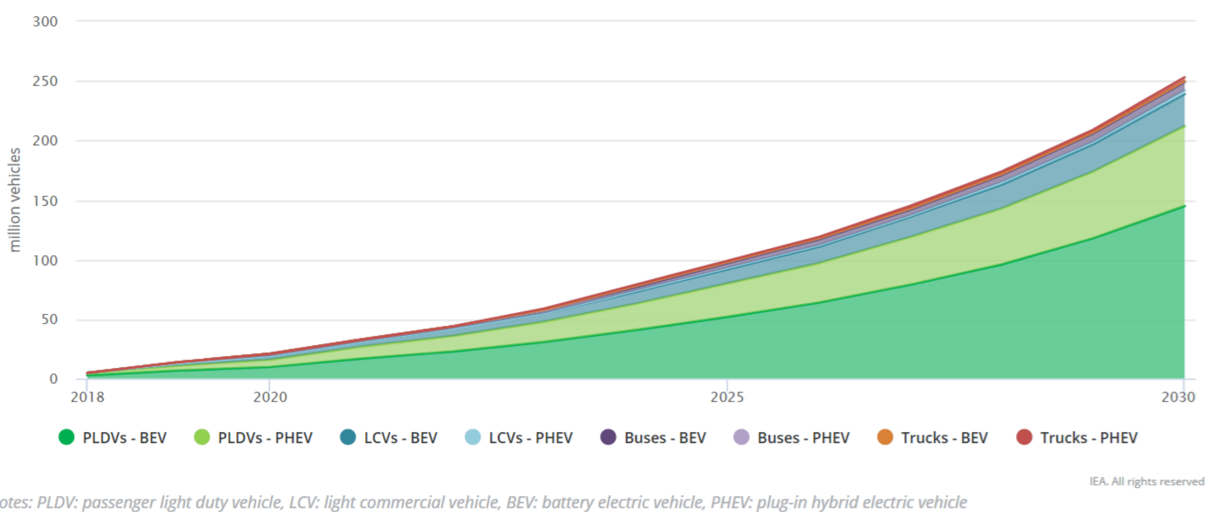


Figure 1-2. Outlook for EV growth from EV30@30 Scenario Fig. 2 Global EV Outlook [7]

One downside of EVs compared to conventional vehicles is their range which may be anywhere from tens of miles to over two hundred on a single charge [8]. Another downside is the time is takes to charge compared to filling a tank of gas; forty five minutes at a Level 3 public station and 3-9 hours at home [8]. Therefore, barriers to electric vehicle adoption involve the efficiency and speed of storing and utilizing the energy.

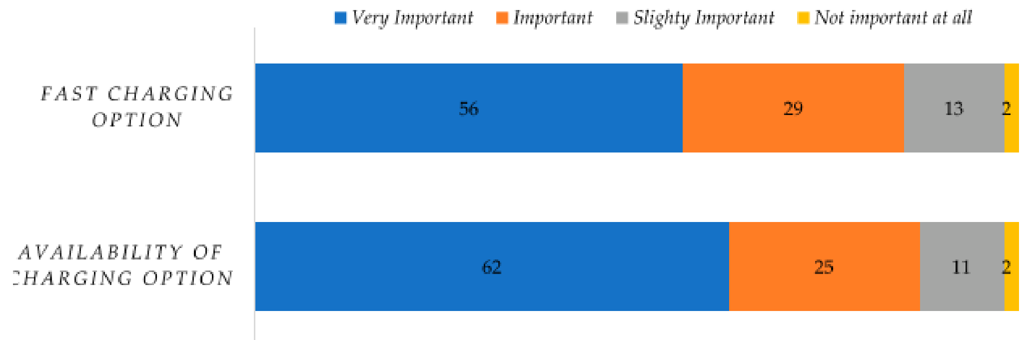


Figure 1-3. Influence of charging option on customer purchase of EVs [2]

When choosing a vehicle, customers often want reliability, driving range, safety, comfort, and high road performance [9, 10] (Figure 1-3). These performance goals are highly dependent on the powertrain and more advanced technology is necessary to increase the benefit of EVs and HEVs [2, 5] (Figure 1-4).

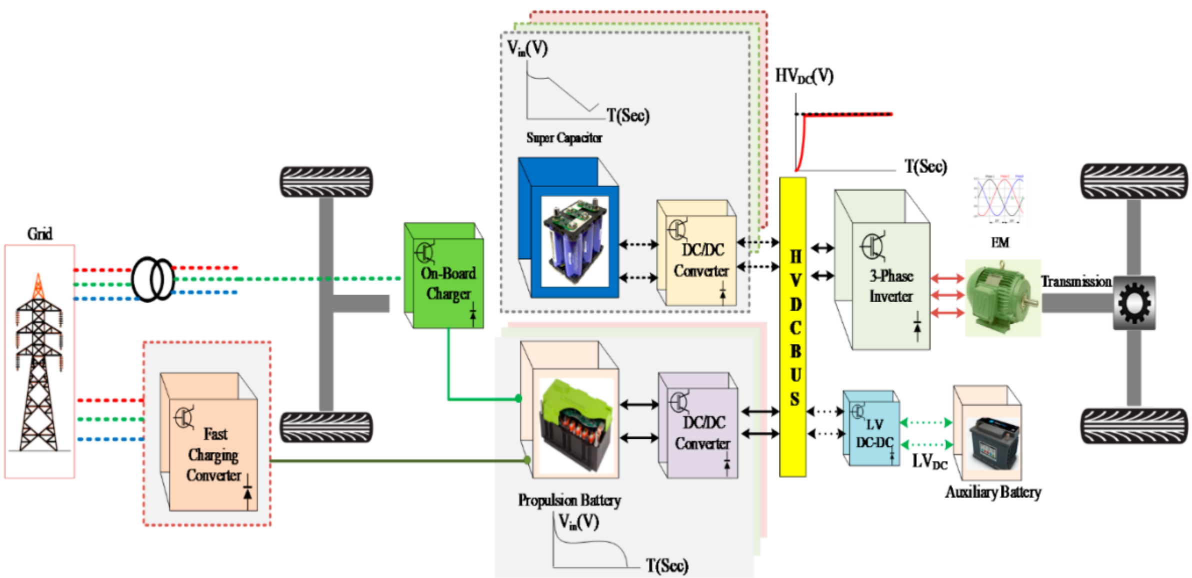


Figure 1-4. Block diagram of an electric vehicle powertrain [2]

Specifically, an efficient and lightweight drivetrain, which works in conjunction with the engine to move the wheels, can increase the desirability of an EV [10, 11]. A benefit of using an electrified

drivetrain is that electric vehicles can convert 67% of electrical power to the wheels while conventional vehicles can only convert 15% of the gasoline to the wheels [12]. A critical element of the technology that allows for improved efficiency and use of electricity to drive the motor, are called power electronics [9].

1.2 Power Electronics for Electric Vehicles

Power electronics is the study of systems that process and control the flow of electric power using electronic circuits [13-15]. The system will process a power input of a specific form and magnitude and output power to meet design specifications. One type of power electronics system is called a converter, which increases or decreases the magnitude of direct current (DC) power. Another common type is an inverter which changes DC power to alternating current (AC) power.

Parts of an EV require different magnitudes and forms of power. For example, energy is stored as direct current (DC) power in batteries while the motor requires alternating current (AC) power to run. Vehicles include low voltage, high voltage as well as primary and auxiliary battery packs and therefore, DC-DC converters are required to step up and step down power while traction inverters in an electrified drive-train ensure the DC power is changed to the appropriately rated AC power necessary for running the motor [2, 4, 5, 10, 16]. The traction inverter can also capture energy from regenerative braking to charge the battery; another function that increases the efficiency of EVs [2, 4, 9].

1.2.1 Semiconductors

A key component of inverters and converters are semiconductors which have values of electric conductivity in between that of insulators and conductors. Insulators prevent the flow the electric charges; while conductors allow electric charges flow freely (Figure 1-5).

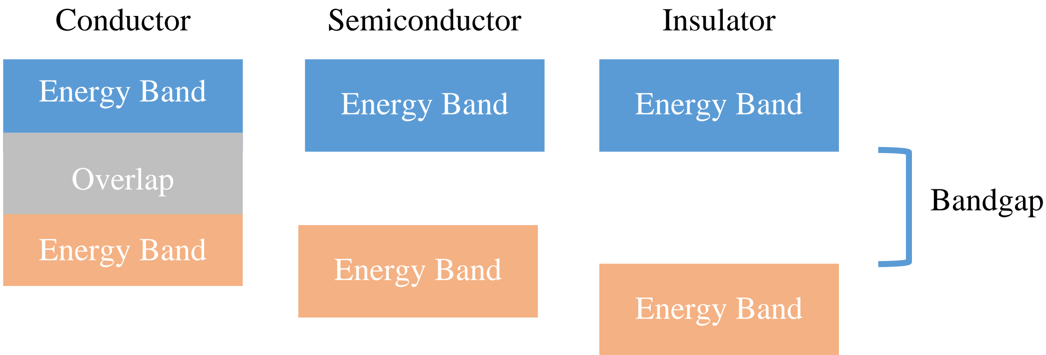


Figure 1-5. Energy bandgaps of different types of materials

Electrons are confined to energy bands and cannot exist in the space between the energy bands. In conductors, the energy bands overlap, and thus, there is no space or band gap within the material where electrons cannot travel. Insulators, on the other hand, have such a wide gap between energy bands that no electron has enough energy to cross and move freely between bands. In semiconductors, the band gap is narrow enough that, given enough energy, an electron could jump from one energy band to the next. Therefore, semiconductors are useful in certain applications because they can behave as either conductors or insulators depending on how much energy the engineer provides. In particular, the semiconductors can act like switches which conduct for a time, then stop conducting for a time. Depending on how these are designed, switches can redirect the flow of current. This is a necessary step for realizing a primary goal of power electronics: controlling the outgoing energy form [17].

The switches involved in this research are called metal-oxide-semiconductor field effect transistors (MOSFETs), which fall under a subcategory of switches primarily used in power

applications. MOSFETs work like a water pipe with a door; energy is required to open the door to control how much water flows through the pipe, the constraints of which are determined by the properties of the MOSFET. Specifically, MOSFETs and similar power devices are made from different semiconductor materials which could include silicon (Si), silicon carbide (SiC), and gallium nitride (GaN). The most utilized semiconductor switches in industry are currently made with silicon (Si IGBTs). SiC and GaN have a wider band gap and are becoming more popular.

1.2.2 Wide Band Gap Power Semiconductor Devices

Si transistors are conventionally the semiconductor material used in power electronic systems. Both Si MOSFETs and Si (insulated-gate bipolar transistors) IGBTs are useful for various applications. For example, Si IGBTs can handle high voltage (5 kV) and current (1 kA) but with limited frequency (100 kHz) while Si MOSFETs can perform in the MHz range but high on-state resistance increases conduction losses with higher blocking voltages limiting applications to below 600V [18]. Semiconductors that have a wide electric gap between the conduction and valence band, commonly referred to as wide band gap (WBG) devices, can potentially perform more quickly and efficiently at higher temperatures, frequencies, and power than silicon (Si) [19]. One reason is that the unipolar structure of SiC MOSFETs removes the tail current which contribute to higher switching losses and lower frequency in Si IGBTs [20]. The material property comparison of Si, SiC, and GaN help explain the higher performance of the WBG semiconductors (Table 1 and Figure 1-6) [21-25].

Table 1. Material Properties for Si, SiC, and GaN

Parameter	Si	4H-SiC	2H-GaN

Bandgap Energy, E_g (eV)	1.12	3.26	3.44
Relative Permittivity/Dielectric constant, ε_s	11.8	10	9.5
Critical Electric Field, E_c (MV/cm)	0.3	2.0	3.0
Electron saturated drift velocity, V_{sat} (10^7 cm/s)	1.0	2.0	3.0
Thermal Conductivity (W/cm^3 K)	1.5	4.9	1.3
Intrinsic Carrier Density, n_i (cm^{-3})	1.5x10^{10}	8.2x10^{-9}	1.0x10^{-10}
Electron Mobility (cm^2/V-sec)	1450	900	2000

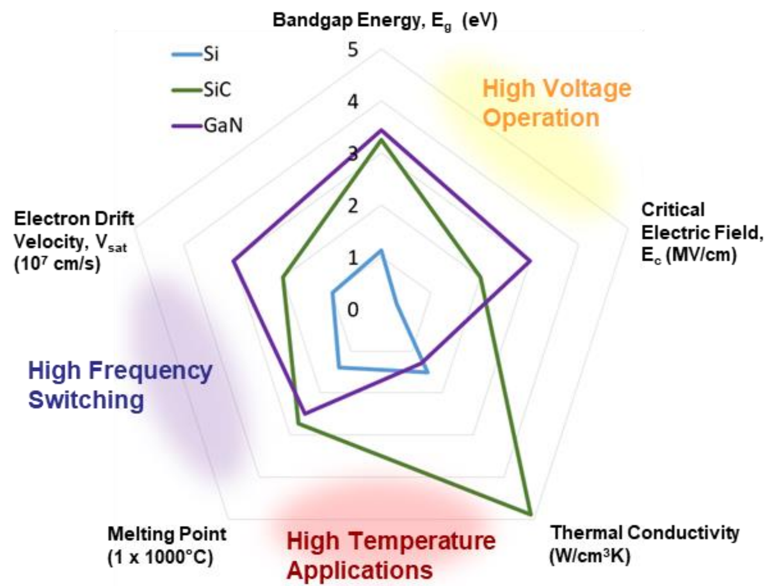


Figure 1-6. Material properties comparison of Si, SiC, and GaN

A wider band gap means that the semiconductor requires more energy to jump an electron from the valence to the conduction band which is defined by the critical electric field. The higher critical electric field of SiC and GaN allow for higher blocking voltages. This means that the devices can be thinner with higher doped drift layers which lowers the on-state resistance [18, 26]. In addition, when the temperature increases, electrons gain energy and require less to the make the jump. Therefore, with higher temperatures, the likelihood of electrons unintentionally jumping to the

conduction band increases which limits the operating temperature. With a wider band gap, the operating temperature can be higher without unintentionally exciting electrons to the conduction band. Thermal conductivity describes the ability of a material to transfer heat so SiC and GaN are better at dissipating heat. Combined with a higher melting point, wide band gap materials can perform at higher temperatures than Si. The disadvantages of GaN compared to SiC include the poorer thermal conductivity which makes SiC better suited for high temperature applications. Lastly, both SiC and GaN have higher electron drift velocity than Si; GaN has the highest value qualifying it as the most suitable material for higher switching frequency operation [26, 27].

1.2.3 Quasistatic Behavior of MOSFETs

The behavior of MOSFETs is often presented in a few different plots which include: a) output curves, the drain current, I_d, as the drain-source voltage, V_{ds}, increases for various gate-source voltages, V_{gs} , b) transfer curve, the drain current, I_d, as the device turns on with increasing gate-source for a given drain-source voltage, V_{ds}, c) capacitance values (Figure 1-7) with increasing drain-source voltage, V_{ds} , and d) the gate voltage, V_{gs} , as the gate charge increases.

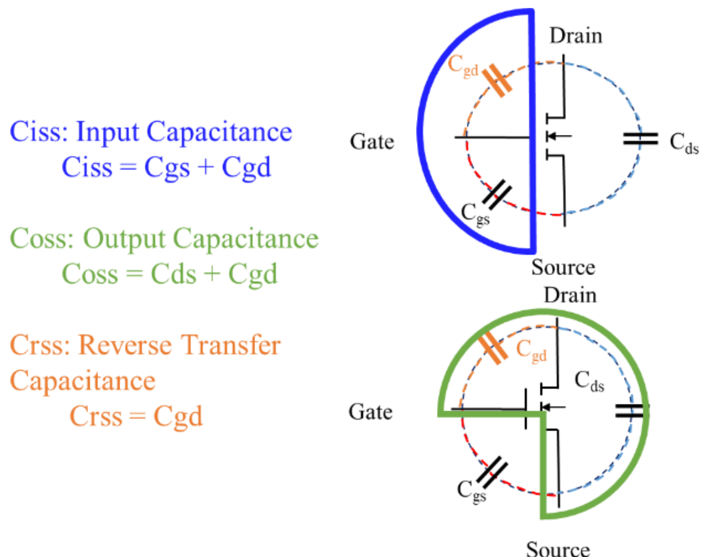


Figure 1-7. Device capacitance definitions

In fact, the behavior observed in the output, I_d vs. V_{ds}, and transfer, I_d vs. V_{gs}, characteristic curves and the capacitance curves of a transistor relate to one another as presented in Figure 1-7; the segments of the gate-charge plot (Figure 1-8d) allow for validation of a transistor's static behavior presented in a datasheet or in a model. Understanding the relationship among the behavioral curves increases the likelihood of an accurate model and can occasionally draw attention to inconsistencies in datasheets or models [28].

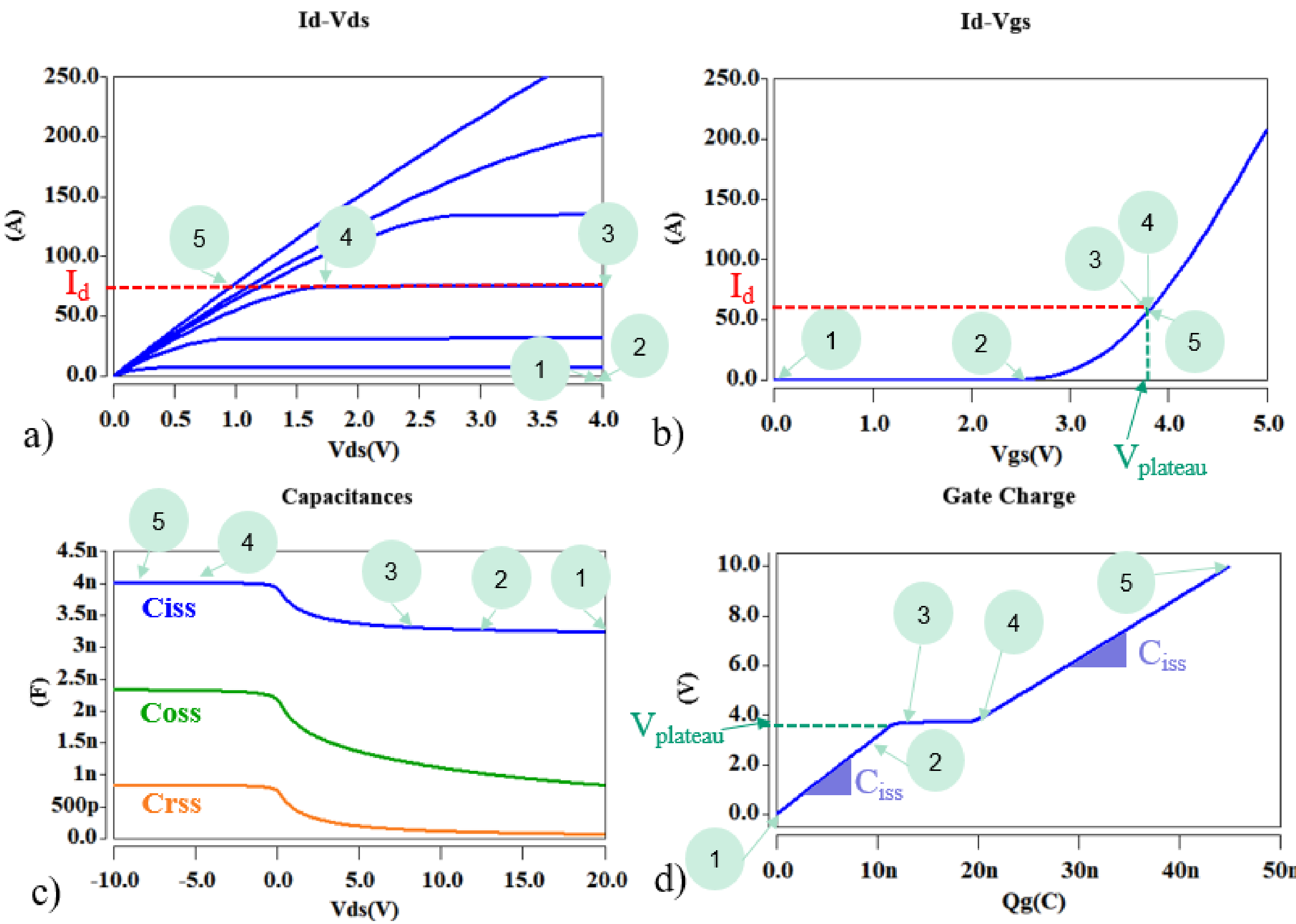


Figure 1-8. Step-by-step walkthrough of the gate charge plot

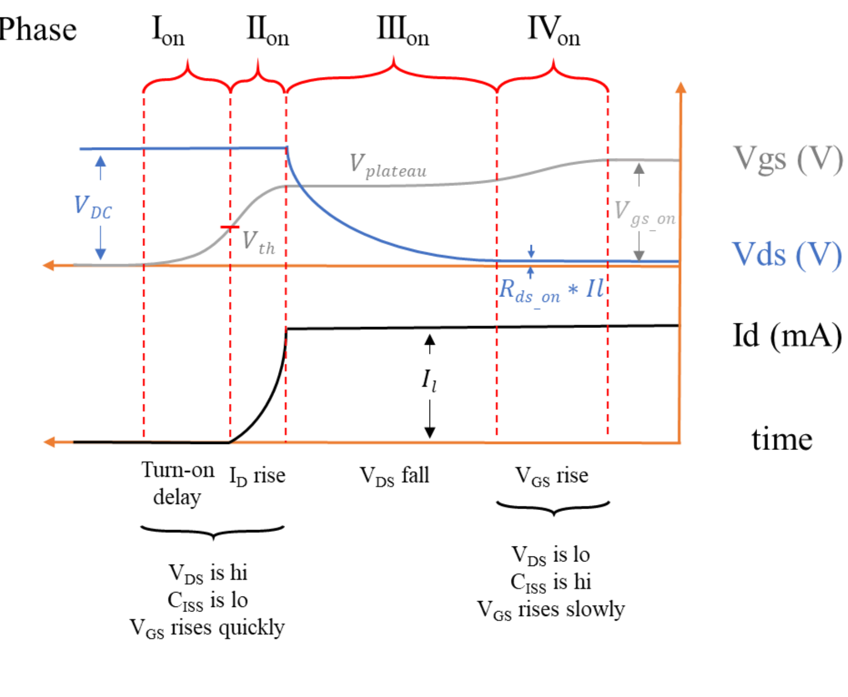
During turn-on operation, from points 1 to 2, the gate voltage, V_{gs}, rises (d) until the device starts to conduct the load current (b) which implies that the bias across the drain and source, V_{ds}, is high and constant (a). The rise rate is determined by the low input capacitance characteristic of high V_{ds} (c). At the end of this segment, from points 2 to 3, the device turns on and begins to conduct current (b). During the second segment, from points 3 to 4, the saturation of the drain current in the Id-V_{ds} view leads to a clamping of V_{gs}, at the Miller plateau (d). The drain current remains constant as V_{ds} drops (a). The difference in slope between the saturation region and quasi-linear at the knee point (a) is less pronounced in SiC than Si due to low transconductance [29]. In

the last segment, from points 4 to 5, the rise of $V_{gs,}$ is less steep than in the low charge region (d) because it now depends on the high input capacitance characteristic at low V_{ds} (c). The device is now fully on, conducting the full load current.

Important notes regarding device behavior and the gate charge plot include the fact that only the capacitances seen by the gate, C_{gd} and C_{gs}, impact the gate charge plot; it is not impacted by the drain source capacitance, C_{ds}, nor the gate resistance (Figure 1-7). The height of the Miller plateau must match the magnitude of V_{gs} required to sustain the load current while the width is determined by the charge under the C_{iss} curve from V_{ds} to the bias remaining between drain and source once the device has entered the quasi-linear region. The Miller plateau is flat if the saturation region is flat in the output curves. Reasons for a slanted Miller plateau include a rise in junction temperature during the measurement, or channel length modulation that makes the output saturation region non-flat. A more in-depth discussion of the gate-charge plots, characteristics of the Miller plateau, and identifying inconsistencies in datasheets is available in [28].

1.2.4 Dynamic Behavior of MOSFETs

The switching waveforms include but are not limited to the turn-on and turn-off delay, the rise and fall times, and reverse-recovery behavior of the diode. The switching speeds depend on the parasitic capacitance and inductance values [18]. Figure 1-9 presents ideal waveforms for turn-on and turn-off behavior of MOSFETs. This plot does not demonstrate ringing and overshoots that can occur from parasitic impedances.



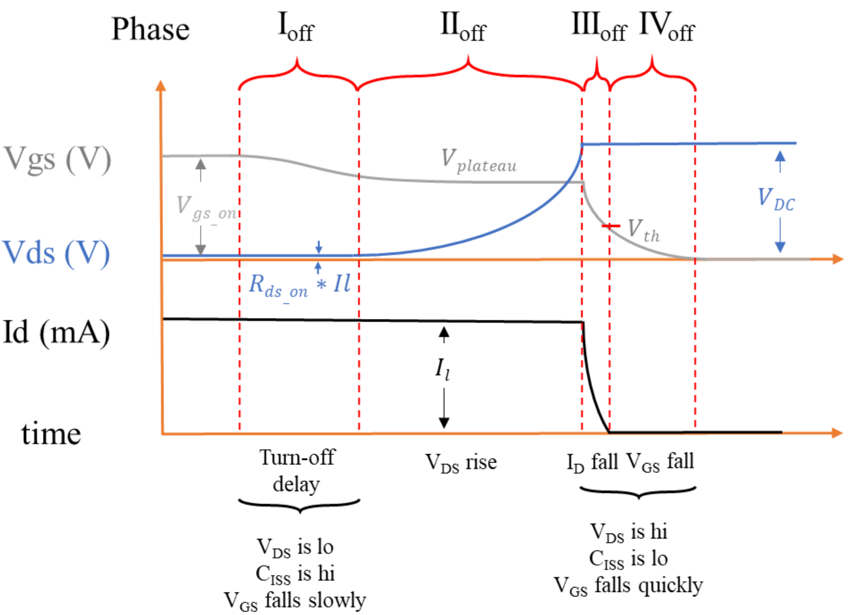


Figure 1-9. Ideal turn-on and turn-off waveforms for a MOSFET [18]

(a) Phase I_{on}: Turn-On Delay

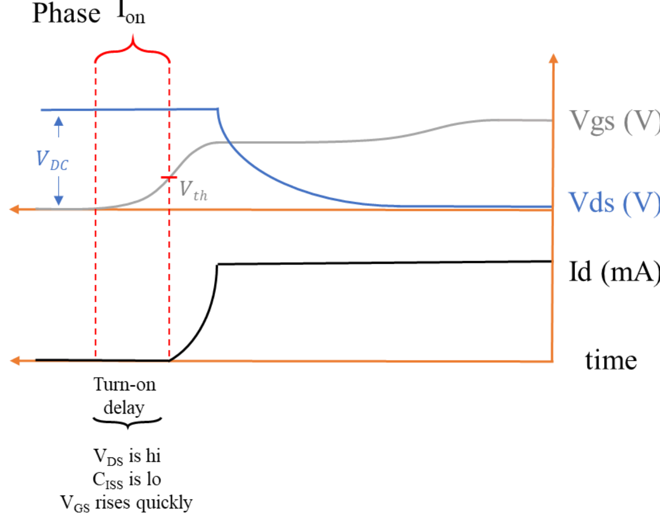
Specifically, the turn-on delay occurs as the input capacitance charges and V_{gs}, starts to rise with the goal of surpassing the threshold voltage, V_{th}, thus creating a channel for current to flow from the drain to the source, I_d (Figure 1-10). V_{gs} is defined in relation to its on-state bias magnitude (3). Until I_d can flow, the bias between V_{ds}, remains high at the bus voltage, V_{dc} (1). The turn-on delay time, td_{on} ,is proportional to the magnitude of C_{iss}, and the gate resistance, R_g (4) [18].

$$V_{ds} = V_{dc} \tag{1}$$

$$I_d = 0 \tag{2}$$

$$V_{gs} = Vgs_{on}\left[1 - e^{\left(-\frac{t}{R_g C_{iss}}\right)}\right] \tag{3}$$

$$td_{on} = R_g C_{iss} \ln\left[\frac{Vgs_{on}}{(Vgs_{on}\text{-}V_{th})}\right] \tag{4}$$



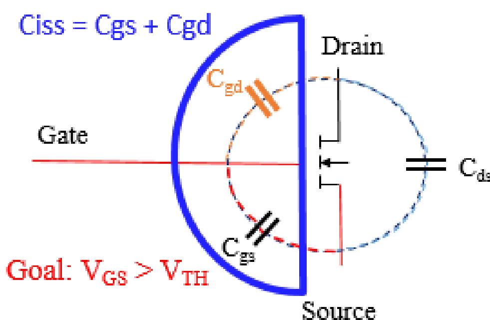


Figure 1-10. Impact of input capacitance on turn-on delay

(b) Phase II_{on}: Drain Current Rise

The goal for phase II of the turn-on process is a transfer of current from the freewheeling diode to the MOSFET. I_d rises in proportion to the transconductance, g_{fs}, and V_{gs} (6). V_{gs} begins to flatten after surpassing V_{th} (Figure 1-11.) at the Miller plateau or $V_{plateau;}$ the gate current is directed towards charging C_{gd}, a process which impacts the rise time of the current, t_{ir} (8).

$$V_{ds} = V_{dc} \qquad (5)$$

$$I_d = g_{fs}(V_{gs,}V_{ds}) * V_{gs} \qquad (6)$$

$$V_{gs} = Vgs_{on}\left[1 - e^{\left(-\frac{t}{R_g C_{iss}}\right)}\right] \quad (7)$$

$$t_{ir} = R_g C_{iss} \ln\left[\frac{Vgs_{on}\text{-}V_{th}}{Vgs_{on}\text{-}V_{\text{plateau}}}\right] \quad (8)$$

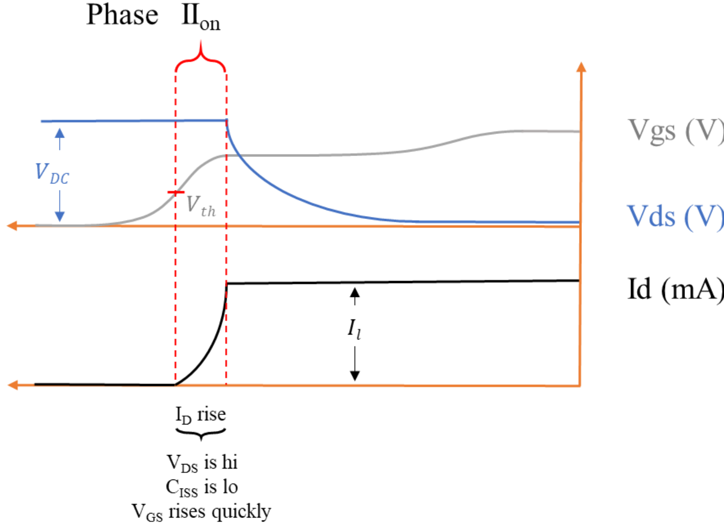


Figure 1-11. Rise of the drain current as the transistor turns on

(c) Phase III$_{on}$: Drain Source Voltage Fall and Miller Plateau

In phase III, the freewheeling diode stops conducting and starts blocking voltage and thus, V_{ds} drops to its on-state value, Vgs_{on}, consisting of the on-state resistance, Rds_{on}, and the load current, I_L (11). V_{gs} hits the Miller plateau as C_{gd} charges with I_d deviating away from C_{gs} (Figure. 1-12). The rate (9) and time (12) for V_{ds} to fall is dependent on C_{gd}. Additionally, a reverse recovery overshoot is common in the falling V_{ds} waveform steadying out to the on-state value.

$$\frac{dV_{ds}}{dt} = \frac{Vgs_{on}\text{-}V_{\text{plateau}}}{R_g C_{GD}} \quad (9)$$

$$I_d = I_L \quad (10)$$

$$V_{gs} = V_{\text{plateau}} = \frac{I_L}{g_{fs}} \tag{11}$$

$$t_{vf} = \frac{Q_{GD} R_g}{(Vgs_{on} \text{-} V_{\text{plateau}})} \tag{12}$$

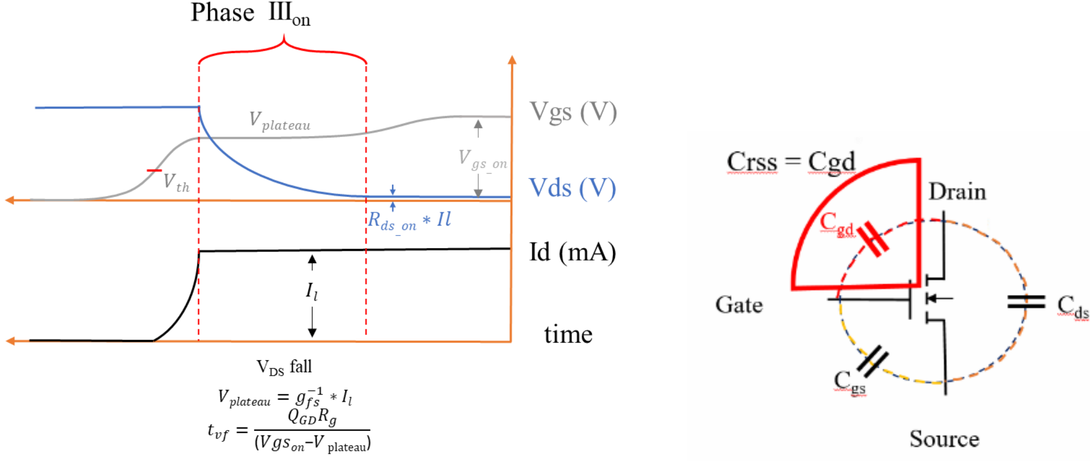


Figure. 1-12. Miller plateau as the transistor turns on

(d) Phase IV$_{on}$: Increase Bias from Gate to Source

In the last phase of the turn-on process, V_{gs} increases to its on-state value and I_d is equivalent to I_L (14). V_{ds} is small, but not zero (typically < 5V), due to the on-state resistance which allows a small amount of leakage current to flow (13) (Figure. 1-13). C_{iss} is high because of the low V_{ds} (Figure 1-8c).

$$V_{ds} = Rds_{on} * I_L \tag{13}$$

$$I_d = I_L \tag{14}$$

$$t = R_g C_{iss} \tag{15}$$

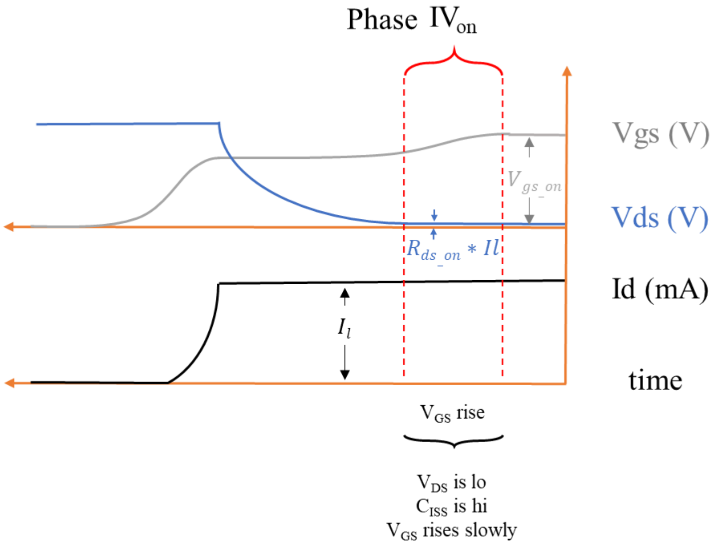


Figure. 1-13. Final behavior as the transistor turns on

(e) Phase I_{off}: Turn-Off Delay

The first step of the turn off process is reducing the applied V_{gs} to zero. V_{gs} then starts to drop back to the Miller plateau (18) (Figure. 1-14).The time delay until turn-off, td_{off}, is proportional to C_{iss} (19). V_{ds} and I_d remain at their on-state magnitudes (16, 17).

$$V_{ds} = Rds_{on} * I_L \quad (16)$$

$$I_d = I_L \quad (17)$$

$$V_{gs} = Vgs_{on}\ e^{(-\frac{t}{R_g C_{iss}})} \quad (18)$$

$$td_{off} = R_g C_{iss} \ln\left[\frac{Vgs_{on}}{V_{\text{plateau}}}\right] \quad (19)$$

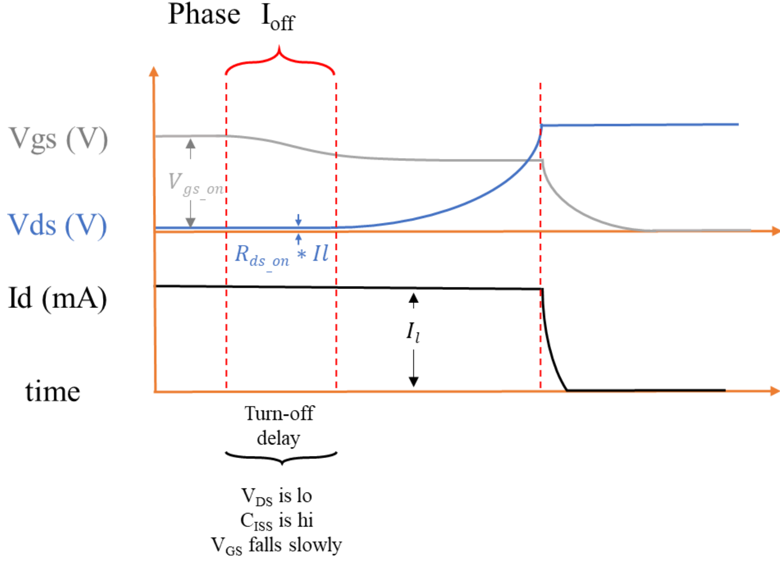


Figure. 1-14. Turn-off delay as the gate source bias drops

(f) Phase II_{off}: Bias between the drain and source increases

As V_{gs} steadies at the Miller plateau (22), V_{ds} begins to increase (Figure. 1-15) at a rate inversely proportional to the gate resistance and reverse transfer capacitance (20) whereas the time for the voltage fall, t_{vr}, has the opposite proportionality (23). I_d remains at I_L (21) although the freewheeling diode begins to pull current from the MOSFET channel.

$$\frac{dV_{ds}}{dt} = \frac{V_{\text{plateau}}}{R_g C_{GD}} \tag{20}$$

$$I_d = I_L \tag{21}$$

$$V_{gs} = V_{\text{plateau}} = \frac{I_L}{g_{fs}} \tag{22}$$

$$t_{vr} = \frac{Q_{GD} R_g}{V_{\text{plateau}}} \tag{23}$$

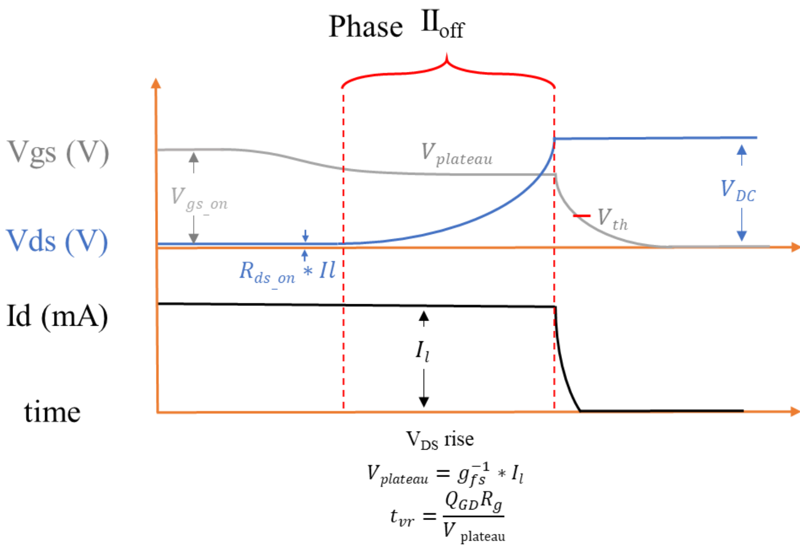


Figure. 1-15. Miller plateau as the transistor turns off

(g) Phase III_{off}: Drain current falls

After the transistor leaves the saturation region, I_d fully transfers to the freewheeling diode. V_{gs} continues to decrease until it reaches V_{th} (26). This is a result of the discharging C_{iss} and thus the time for the current to fall, t_{ir}, is dependent on C_{iss} (27) and the magnitude is proportional to the transconductance and V_{gs} (25). Lastly, V_{ds} remains clamped to the bus voltage (24) (Figure. 1-16).

$$V_{ds} = V_{dc} \tag{24}$$

$$I_d = g_{fs}(V_{gs,}V_{ds}) * V_{gs} \tag{25}$$

$$V_{gs} = V_{\text{plateau}}\, e^{\left(-\frac{t}{R_g C_{iss}}\right)} \tag{26}$$

$$t_{ir} = R_g C_{iss} \ln\left[\frac{V_{\text{plateau}}}{Vth}\right] \tag{27}$$

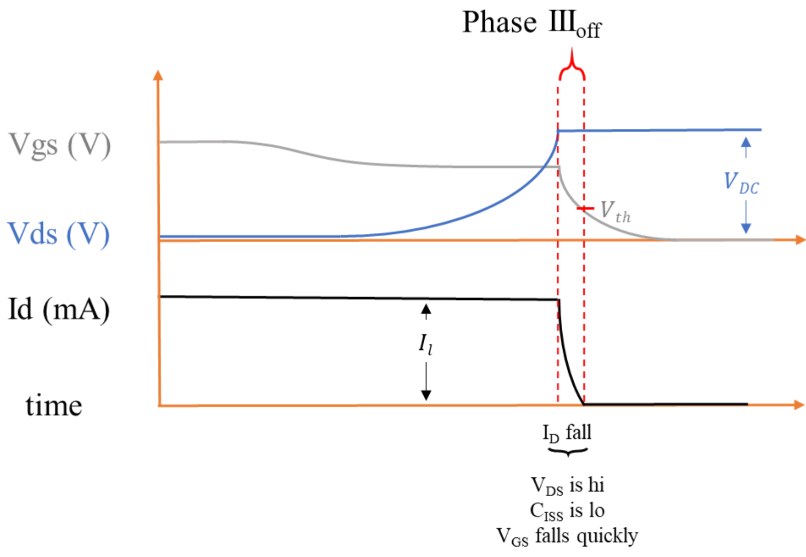


Figure. 1-16. Fall of the drain current as the transistor turns off

(h) Phase IV_{off}: Gate source bias falls, transistor off

As V_{gs} falls to zero, C_{iss} fully discharges. The load current is now fully transferred to the freewheeling diode and the transistor drain current is zero (29). V_{ds} remains high at the bus voltage magnitude (28) (Figure 1-17).

$$V_{ds} = V_{dc} \tag{28}$$

$$I_d = 0 \tag{29}$$

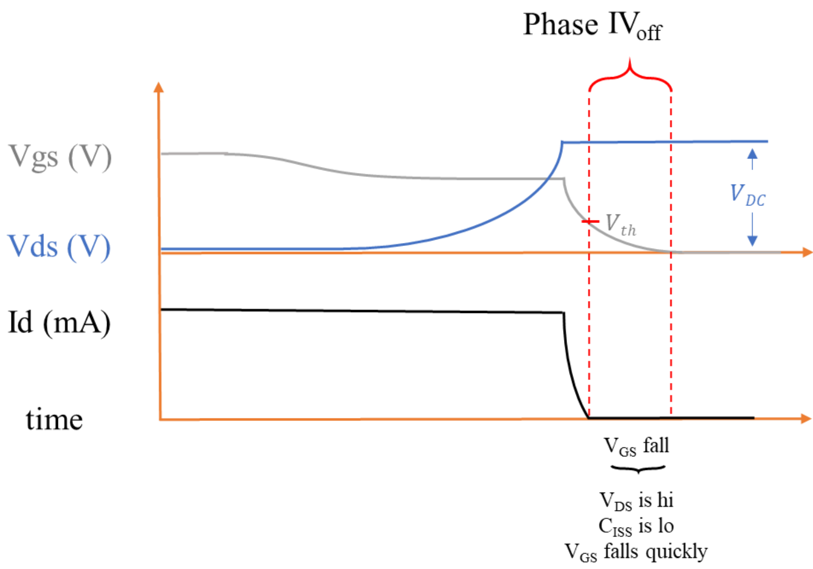


Figure 1-17. Final reduction of gate-source bias as transistor turns off

1.3 Multi-Chip Power Module Packaging

Power modules provide a support structure around semiconductor chips so that they can perform reliably over time. Without a module, the chip could suffer from electrical, thermal, or mechanical breakdown. In addition, chips require interconnections in order to integrate the chip into the rest of the system. Therefore, packages provide protection for the semiconductors while also providing power and signal distribution according to the application of the chip (Figure 1-18). For further understanding, compare a brain to the chip and the human body and nervous system to the power module; the brain is powerful but could not function without the body and nervous system which protect the brain and connect it to the rest of the body systems (Figure 1-19) [30]. The brain's purpose can be executed in various applications because it is protected and interconnected.

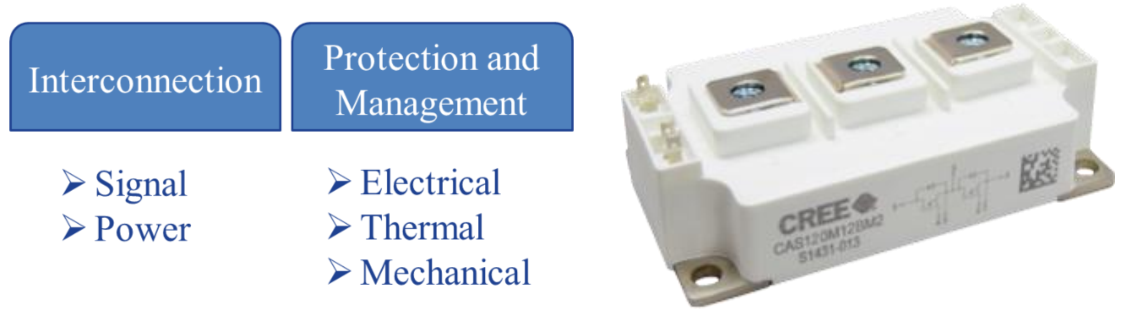


Figure 1-18. Functions of a power module package with an example of a commerical power module (CREE CAS120M12BM2)

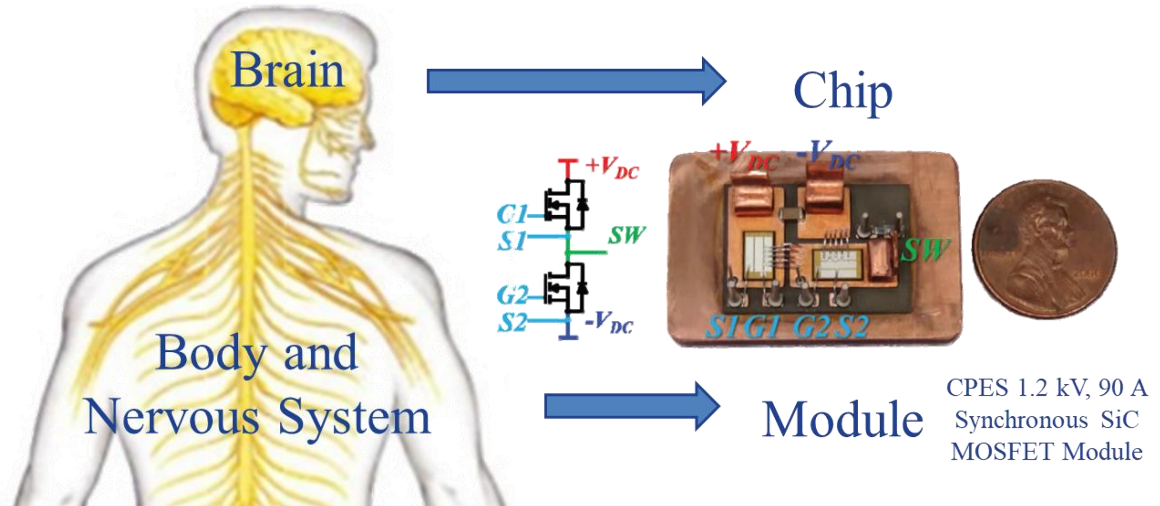


Figure 1-19. A power module package and chip are analogous to the human body and brain [30, 31]

Packaging and integration are essential to meeting the aggressive size, weight, efficiency, power, and cost requirements for 21st-century electronic energy systems. While packages exist for Si and often WBG devices are placed into these packages, they are not optimized to take advantage of the benefits of SiC and GaN. In general, power devices are one of, if not the most expensive and critical element of many circuits. While they could be utilized in their bare die form, they are often packaged in modules which are specially designed to protect them and the surrounding elements of the circuit. The application of this research is electric vehicles where compact systems

are necessary to regulate hundreds or thousands of volts while minimizing additional weight added to the moving vehicle.

Another benefit of packaging devices is that higher power modules can be designed while managing thermal performance; simply using a larger die would increase power capacity but with considerably poorer thermal performance and inefficiency across the die. Electric vehicles have high ambient temperature surrounding the power electronics demanding devices that can perform well at high temperatures. In addition, thermal management systems cannot be too bulky or heavy as the car must be lightweight to travel. Therefore, this research is intended to study and improve the design of power modules to be used in electric vehicles.

1.4 Research Motivations and Objectives

High current SiC MOSFET power modules are becoming global solutions in load harsh power electronics systems such as renewable energy generation, automotive and rail-traction applications [32]. Paralleling dies in multi-chip modules or paralleling discrete SiC MOSFETs increases the current rating of power modules while also allowing for high power with fewer die (Figure 1-20); paralleling die can also reduce conduction losses by ensuring the devices operate in the linear region [20, 26, 33, 34].

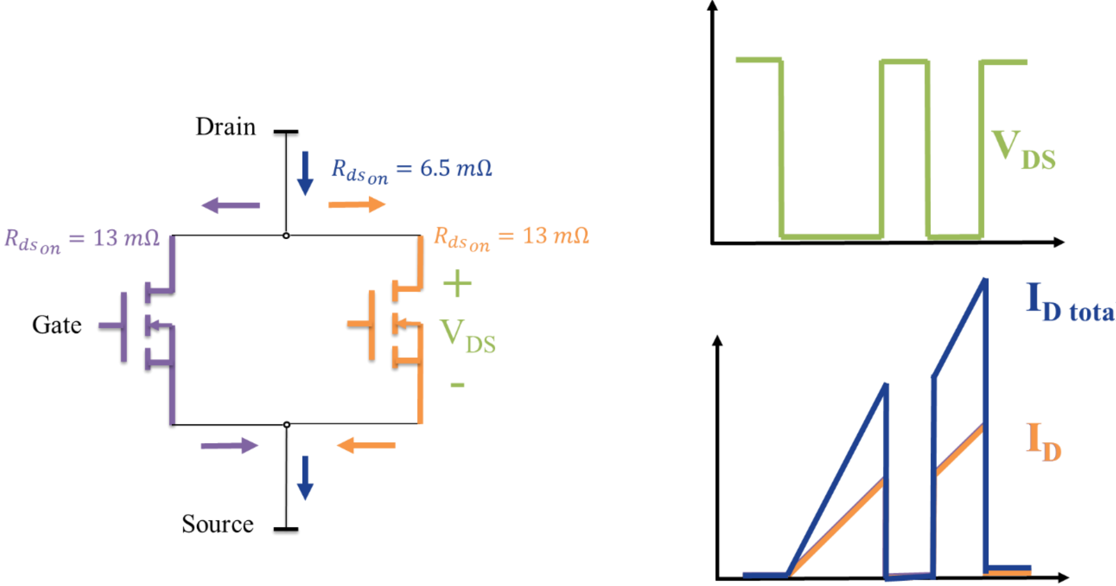
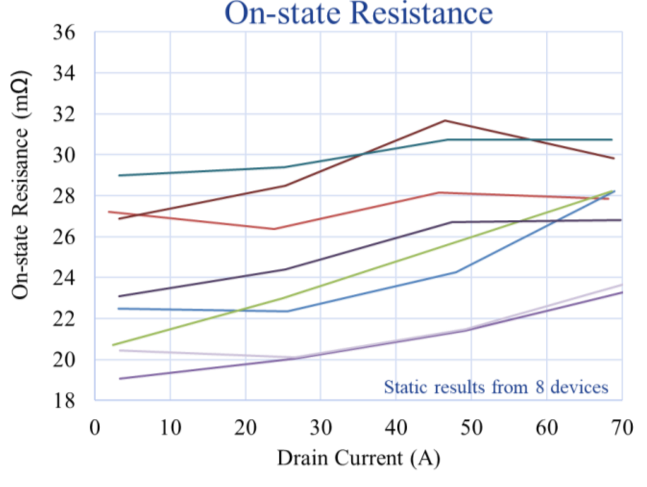


Figure 1-20. Increased current carrying capacity with paralleled dies

However, variations in the device parametrics can lead to unbalanced current sharing of the paralleled dies (Figure 1-21-Figure 1-23). In addition, differences in the impedance of the current pathways can also lead to mismatched current overshoots and ringing as well as mismatched rates of increase during static, on-state current sharing (Figure 1-22-Figure 1-23) [20, 35]. Improving performance of paralleled die include but are not limited to adjusting the length of the wire bonds, active gate driver control, and use of auxiliary source connection [20].



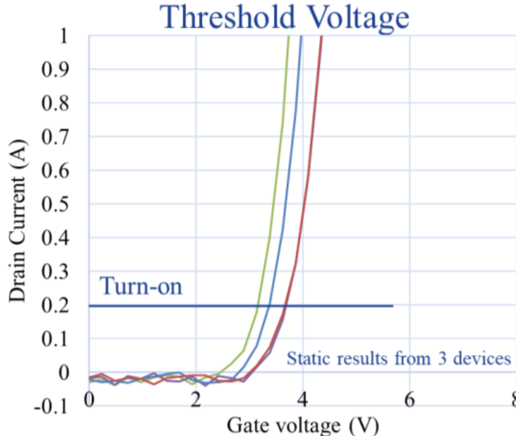


Figure 1-21. Device parametric tolerances can lead to unbalanced current sharing

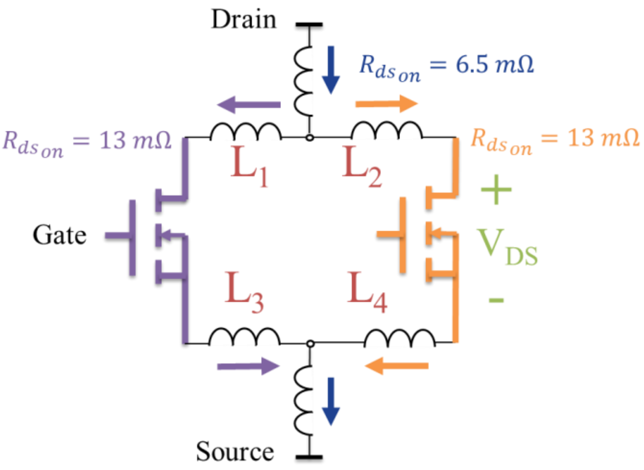


Figure 1-22. Package parasitics can lead to unbalanced current sharing

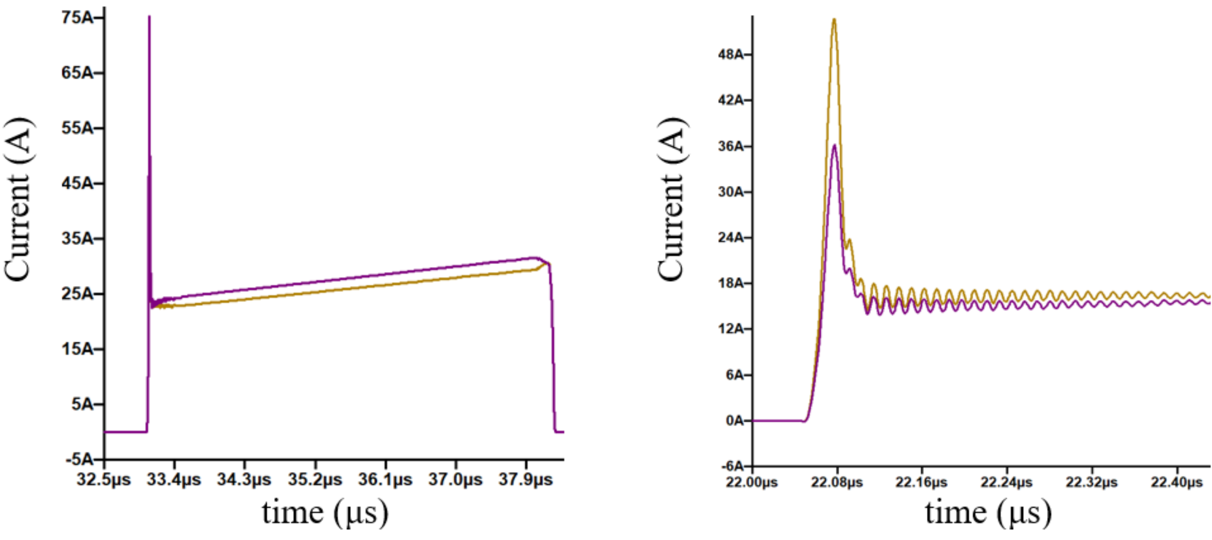


Figure 1-23. Simulation of static and dynamic unbalanced current sharing

1.4.1 Device Parametric Tolerances

The threshold voltage of MOSFETs results from nonidealities in the interface or oxide; due to developing manufacturing techniques of SiC, variations occur in the threshold voltages of these

devices [20]. Mismatch in the threshold voltages of paralleled dies causes them to turn on at different times, thereby sending the majority of the current through one device momentarily [20, 34]. Threshold voltage mismatch would be apparent in the dynamic switching behavior of the devices (Figure 1-21-Figure 1-24).

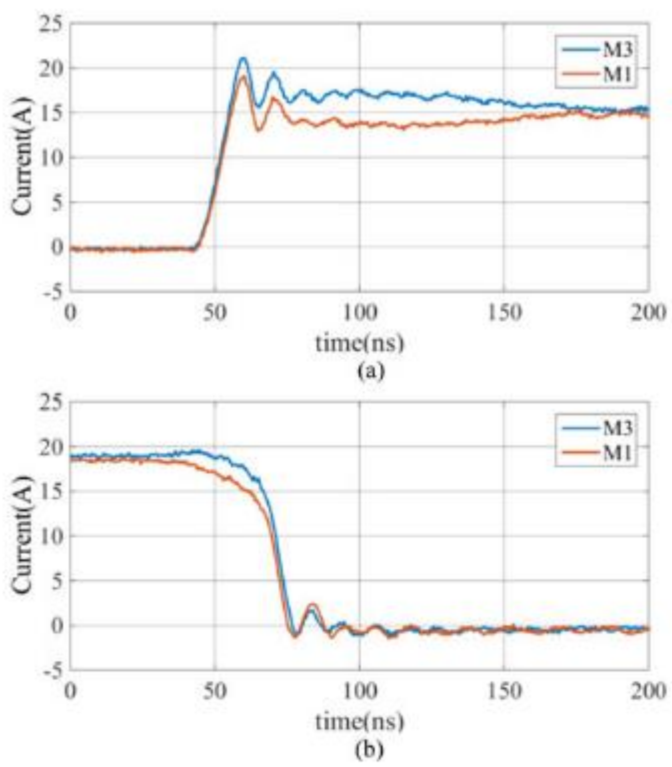


Figure 1-24. Impact of unbalanced threshold voltages on a) turn-on and b) turn-off behavior of discrete SiC MOSFETs [20]

Static current sharing is dependent on the pathway impedances composed of inductance and on-state resistance [20]. If any of the impedance parameters of the pathways are mismatched, current distribution among the dies can be unequal (Figure 1-22). Variations in on-state current sharing are typically attributable to a mismatch in on-state resistance of individual die (Figure 1-25).

On-state resistance mismatch may also contribute to unbalanced switching and conduction losses (Figure 1-25). However, the impact of this effect may be limited for devices with positive temperature coefficient [35].

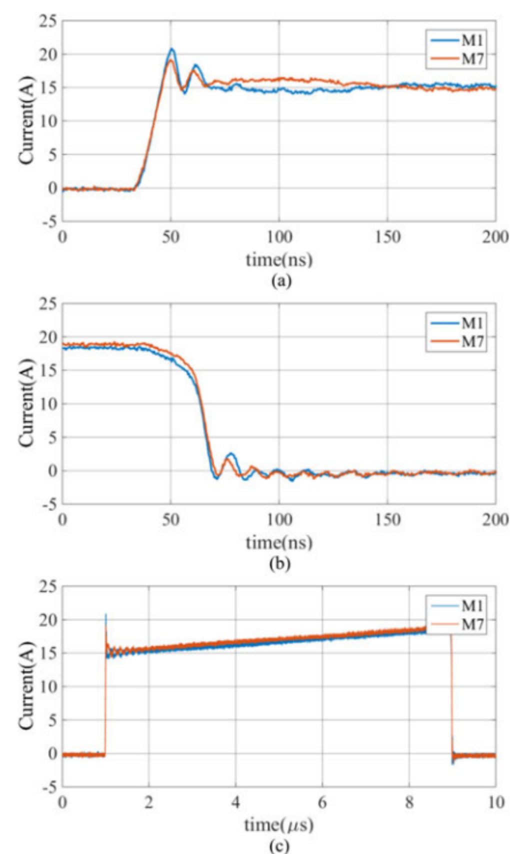


Figure 1-25. Impact of unbalanced on-state resistance on a) turn-on, b) turn-off, and c) on-state behavior of discrete SiC MOSFETs [20]

A paper evaluated the electrical and thermal impact of discrete device parametric tolerances [36]. It determined that differences in on-state resistance for paralleled devices led to the most significant unbalance in the current sharing. On the other hand, if the on-state resistances were well-matched, the threshold voltage had less of an impact on current sharing unbalance. In a boost

test with devices that were balanced in both on-state resistance and threshold voltage, one device presented higher switching losses and higher temperature (Figure 1-26). The unbalance in switching losses was attributed to a likely mismatch in parasitic inductance in the current pathway [36].

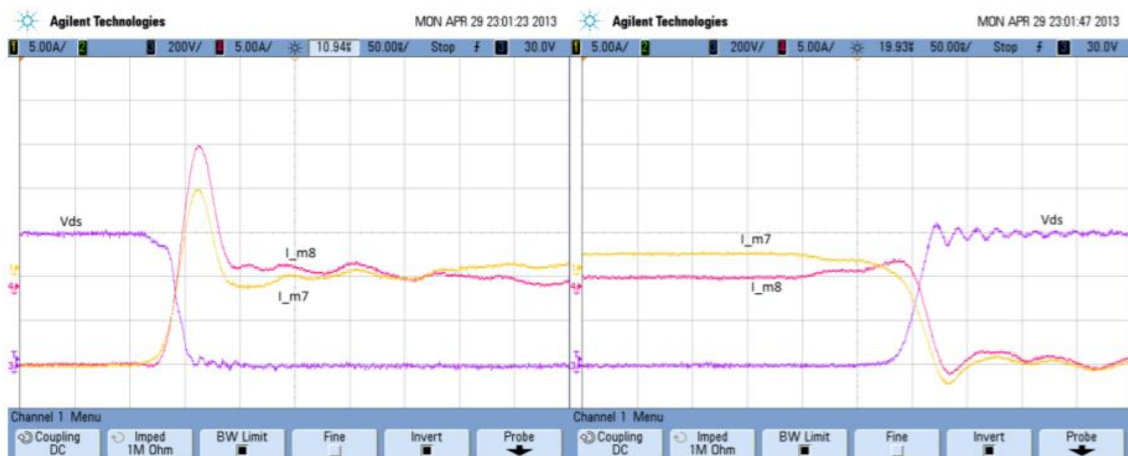


Fig. 15 : Switching transients of the dc/dc boost converter's parallel-connected MOSFETs

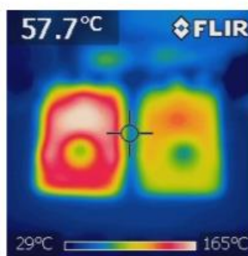


Fig. 16 : Thermal image of the parallel-connected MOSFET of the dc/dc boost converter

Figure 1-26. Thermal impact of unbalanced current sharing in discrete SiC MOSFET devices

1.4.2 Package Parasitics

When the current pathways have similar impedances, the current should increase at the same rate and experience the same overshoot. This ultimately means that neither die is experiencing more current stress than the other, which leads to improved reliability and prevents catastrophic failures. When not balanced, each die will experience different current loads especially during turn-on [34].

Mismatch of the parasitic impedances in current pathways can lead to unbalanced stress throughout modules which could contribute to poorer reliability. Often, the geometry of the DBC leads to asymmetrical pathway impedance for parallel dies as seen in Figure 1-27. While a symmetrical DBC is favorable for current sharing behavior, this is difficult to achieve with a large numbers of devices and can also poorly utilize space and may put additional constraints on the thermal management of the system [20, 35]. Another source of unbalanced static or dynamic current sharing may be electrical couplings between power and gate loops [34]. One reason for designing a module with such coupling is to create a negative feedback path for the gate loop. A method for mitigating this unbalance is offsetting the impedance of the pathway with varying lengths of wire bonds where impedance increase with the length of the wire [34]. Compensating the unbalance with wire bonds led to better dynamic current sharing (Figure 1-27b).

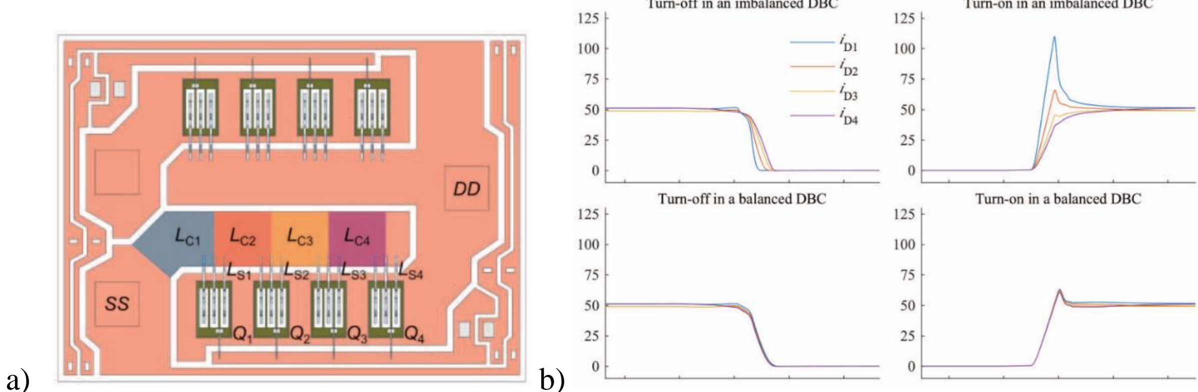


Figure 1-27. a) Multi-chip half-bride power module with assymetrical pathway impedance for paralleled dies where L_{C4}> L_{C3}> L_{C2}> L_{C1} and b) Improved current sharing after adjusting the wire bonds [34]

Both common source and switching loop stray inductance can negatively impact current sharing behavior of paralleled dies. Mismatched switching loop stray inductance may cause unbalanced current sharing during the on-state (Figure 1-28). However, the impact of pathway inductance mismatch is often less significant than on-state resistance mismatch in static current sharing [20].

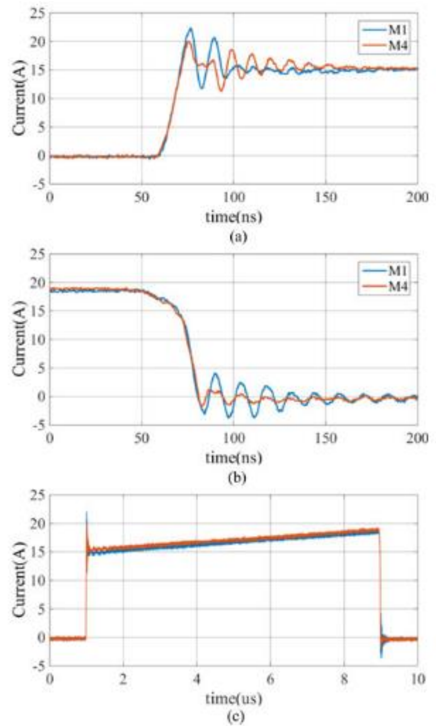


Figure 1-28. Impact of switching loop stray inductance mismatch on a) turn-on and b) turn-off behavior of discrete SiC MOSFETs [20]

Common source stray inductance has the most negative impact on dynamic current sharing compared to switching loop stray inductance (Figure 1-29). Because switching losses have a significant impact on module performance, this effect is problematic and deserves investigation and mitigation as many have done [20, 26, 34, 35]. One such solution was addition of an auxiliary source connection to reduce the impact of current coupling between the gate and power loops (Figure 1-30).

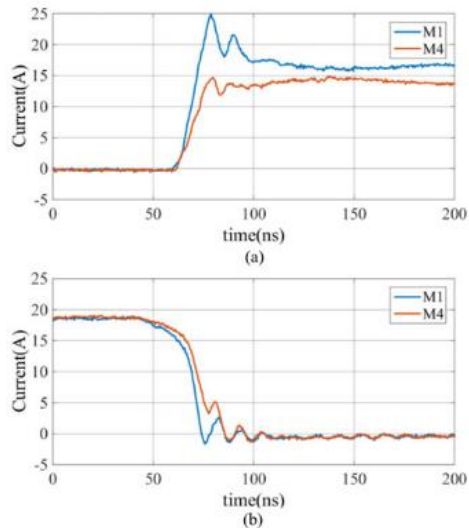


Figure 1-29. Impact of common source stray inductance mismatch on a) turn-on and b) turn-off behavior of discrete SiC MOSFETs [20]

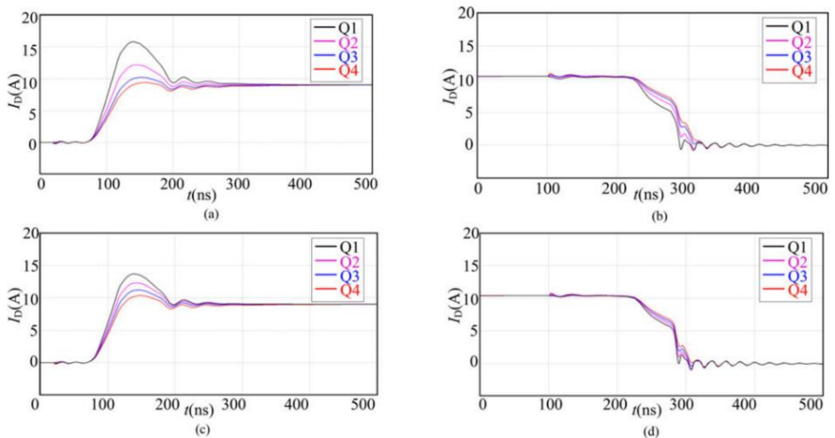


Figure 1-30. Addition of auxiliary source connection reduced dynamic current imbalance from a) to c) during turn-on and from b) to d) during turn-off [20]

Similar research evaluated the thermal impact of symmetrical parasitic inductances for a multi-chip module [37]; the research compared a conventional module to a module with symmetrical power loop inductances and found that balancing parasitic inductances helped balance heating of the paralleled chips. The method for balanced inductances utilized a set of DC terminals in parallel with those in the conventional, baseline layout. By creating balanced inductances, the new method helps mitigate large voltage overshoot and unbalanced dynamic current sharing (Figure 1-31). This paper found improved thermal performance in balancing the parasitic inductances but did not evaluate the impact of device parametric tolerances.

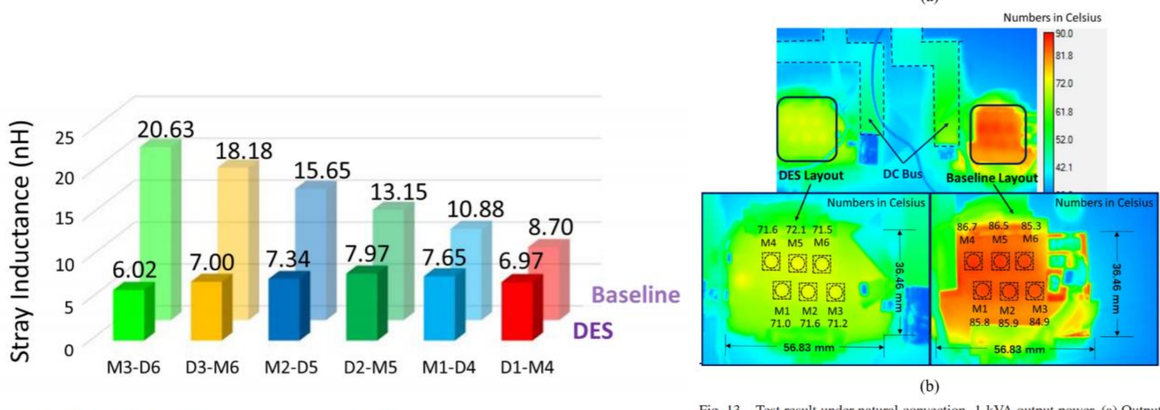


Figure 1-31. Thermal comparison of a module with unbalanced and balanced parasitic inductances [37]

1.4.3 Objective

In this thesis, the primary objective is to observe the impact of device parameter tolerances on the current sharing behavior of modules with paralleled dies. In order to mitigate the impact of package parasitics, the DBC pattern is designed symmetrically so that the impedances of the traces are similar (Figure 1-32). In practice, a perfectly symmetrical DBC is challenging for more than 2 devices and could also increase the demands of the thermal management system; however, the primary area of interest in this research is the impact of mismatched device characteristics and therefore is an acceptable design [35, 38]. The control power module has dies with similar threshold voltages to further increase the likelihood of balanced current sharing. The die in the experimental power module has die selected with dissimilar threshold voltages, forcing current through one die before the other. The on-state resistances of the bare die were too difficult to characterize without a functional probing station and therefore, this parametric difference could not be controlled.

Another method of interest to reduce the gate loop inductance is the use of flexible PCB as the gate, drain, and kelvin source interconnection [39]. Replacing classical wire bonds with flexible PCB or other planar technologies has been shown to increase power density and reduce loop inductance [40, 41]. A low gate loop inductance reduces the potential impact of parasitic resonance [42-44].

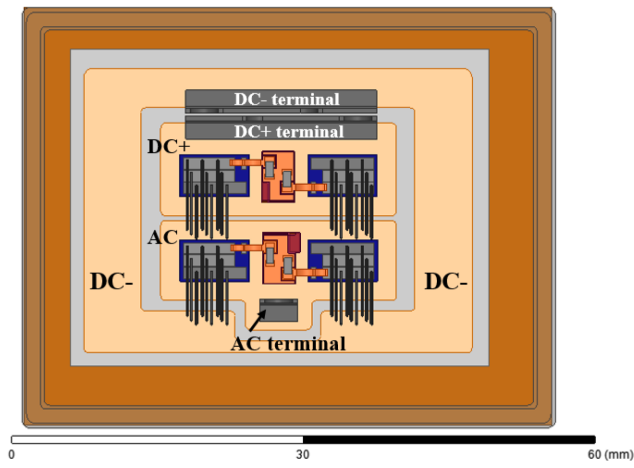


Figure 1-32. Symmetrical DBC layout with DC- trace wraparound

To obtain a compact power module, Wolfspeed's CPM3-1200-0013C, 1200 V, 13 mΩ, SiC MOSFET is used. The SiC MOSFET half-bridge power module is shown in with indicated patterned DBC and dies wire bonded and sintered to the appropriate DC+, DC- and AC pad. The developed module consists of 2 paralleled dies in each switch position. The body diodes of the SiC MOSFET dies are utilized instead of the external antiparallel diodes [33, 45]. A Rogowski coil passes through the low side wire bonds in order to observe current sharing behavior. The focus of this paper is on current sharing behavior and characterization of the power module while previous work emphasized the challenges and methods associated with the fabrication process [45].

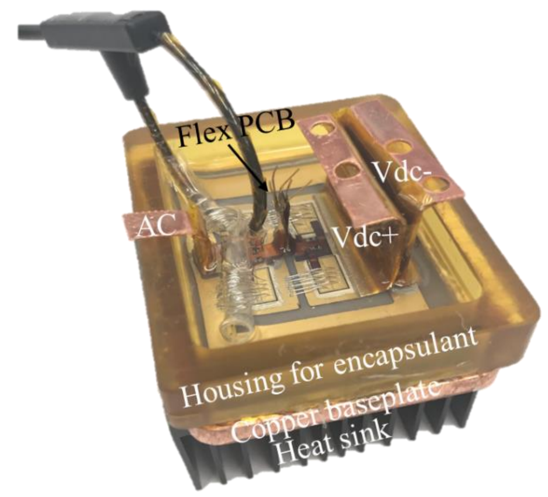


Figure 1-33. Fabricated 1.2 kV, 6.5 mΩ SiC half-bridge power module

The properties of silicon carbide (SiC) MOSFET devices such as high-power density capabilities [1], high temperature operation, and low losses [2] make them more desirable for use in power modules compared to Si IGBTs. Furthermore, lower switching times enable high switching frequency operation, reducing the passive components in the system, further improving power density [3]. With these advantages comes the need for updated packaging techniques to fully utilize these benefits.

Chapter 2 Design of a Balanced Power Module for Automotive Applications

2.1 Introduction

The design elements of interest in this research project include a symmetrical DBC layout to mitigate the impact of package parasitics on the unbalance of current sharing for paralleled dies. Paralleled dies are selected together based on measured threshold voltages in order to increase the likelihood of balanced dynamic current sharing in a control module or intentionally create unbalanced current sharing in an experimental module. The gate interconnection is made from flexible PCB as opposed to wire bonds, reducing the gate loop inductance. Lastly, the body diodes of the MOSFETs are used in placed of external anti-parallel diodes to increase power density.

2.2 Survey of Power Module Packaging Techniques and Limitations

The increased switching speed of SiC devices, higher di/dt and dv/dt, can lead to more severe unwanted overshoots and noise due to parasitic inductances and capacitances. For example, the stray inductance of the commutation loop can lead to overvoltage [39]. Multiple methods have been proposed and tested to reduce the parasitic elements of the circuit.

With classical packaging materials, direct bond ceramic (DBC) substrates and wire bond interconnections, there are multiple efforts to optimize the layout, including stacking or layering of the DBC which replaces leads and interconnections with electrical press contacts [42]. A similar method stacked the negative terminal on its own substrate onto the base substrate in order to provide a wide and parallel current return path and minimize the commutation loop area [46]. [47] utilized the bottom side of the DBC and a folded copper piece connected the DC- bus on bottom to DC+ bus on top which leads to a 3.4 nH power loop inductance. Another method integrates the DC link capacitor into the package to achieve a 7.2 nH commutation loop [43]. An International Rectifier (IR) half-bridge module implemented a common terminal which reduces the package inductance to less than 8.4 nH and is easily scalable [48]. The IR design ensured proximity of the negative and positive terminals in the symmetric pattern which increased the reliability of current sharing measurements.

Wire bondless solutions take advantage of the fact that wire bonds are a primary mode of failure in power modules. They also increase inductance and limit current carrying capacity. Therefore, [49] designed a GaN power module with the power and signal connections of the embedded chip directly attached to the DBC substrate to obtain a high frequency and high power system.

Another perspective is utilization of PCBs in place of the DBC substrate which allows for lower cost, high volume production. Active and passive components can be embedded into the module. Furthermore, decoupling capacitors can be soldered directly to or close to the die, reducing the current pathway. Finally, dies can be stacked within the PCB as another means for lowering stray inductance [50, 51].

Multiple half-bridge power modules were surveyed to compare number of top and bottom side dies, power loop inductance, whether the design included external diodes, and the presence of an external gate resistor embedded into the package [23, 32, 33, 46, 48, 49, 52, 53].

2.3 Module Design

2.3.1 Symmetrical/Balanced DBC Pattern and Current Sharing Simulation

A balanced and symmetrical DBC layout increases the likelihood of current balance in the commutation loop. When not balanced, each die will experience different current loads especially during turn-on [34]. One balancing method utilizes the split-output DBC layout, which attempts to decouple the body diode and junction capacitance to improve balance of paralleled dies [54].

The method utilized in this paper is a design with symmetrical pathways in the commutation loop (Figure 1-32). A large current return path allows for the positive and negative power terminals to be closer together, which decreases the inductance between the two. The inductance can be kept small by designing short conduction paths with enough space among dies for thermal management [33]. Designing the current pathways for balancing the current loop involved iterations of the module layout to ensure symmetrical geometry; for example, positioning the DC leads directly in the center of the DC+ and DC- substrate pads. The DC negative trace wraps around the perimeter of the module allowing the current to flow through symmetrical pathways; current will not be passed through either die more than the other as a result of asymmetrical parasitics (Figure 2-1).

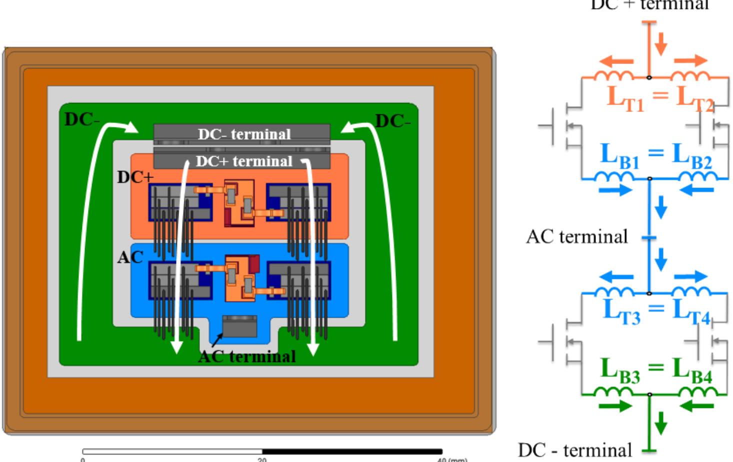


Figure 2-1. Symmetrical DBC layout for symmetrical parasitic inductance in the current pathway

In order to simulate the symmetry, the module parasitics and the flexible PCB were extracted (ANSYS Q3D) and exported into LTSpice along with an existing Wolfspeed die spice model. Figure 2-2 shows the configuration of the power module in which the two bottom positions in the half-bridge were analyzed. The current was simulated for unbalanced and balanced power loops indicating that a balanced design leads to less current and thus less thermal stress on the die in Position C (Figure 2-3).

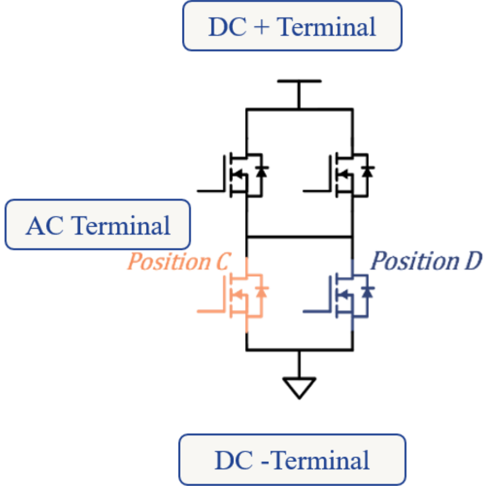


Figure 2-2. Dies in Position C and D in parallel act as the bottom side switching device

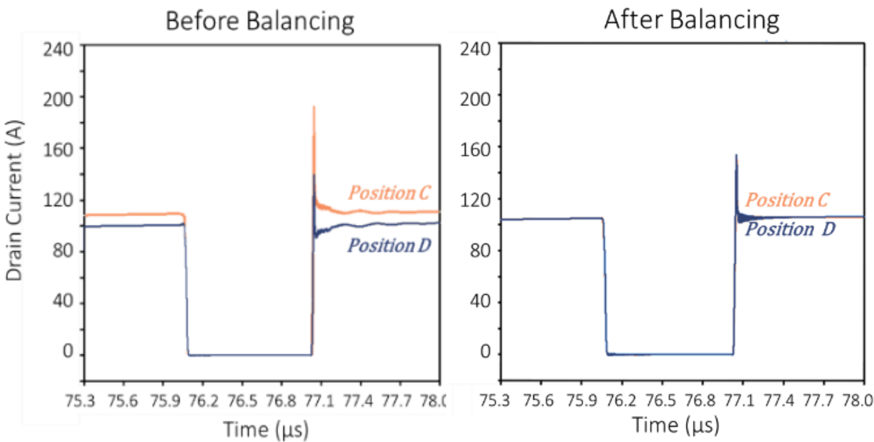


Figure 2-3. Simulation of the current sharing characteristics for a symmetrical and non-symmetrical design

2.3.2 Die Placement based on Threshold Voltage

One method of balancing the current is tuning the wire bond length to achieve equal path inductances [34]. Other options to improve unbalance are DBC layout adjustments as described above, die placement, and the bond wire geometry. Therefore, the other design feature of this paper is selection of die with similar and dissimilar static characteristics to observe the impact of balanced and unbalanced dies on current sharing behavior.

Figure 2-5 shows the threshold voltages of the dies measured using a B1505a curve tracer from Keysight. A test fixture was made so that spring-loaded pins touched the gate, source, and drain pads of the bare die. 3 terminals protruded from the fixture which could be used in the curve tracer (Figure 2-4).

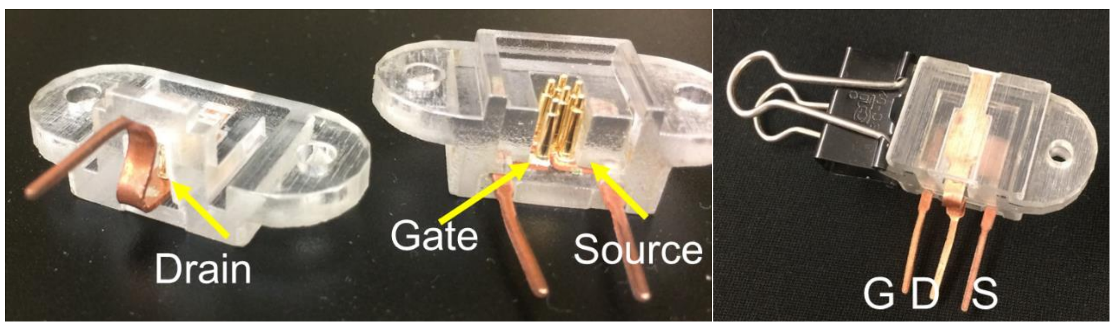


Figure 2-4. 3-terminal test fixture for characterizing bare die

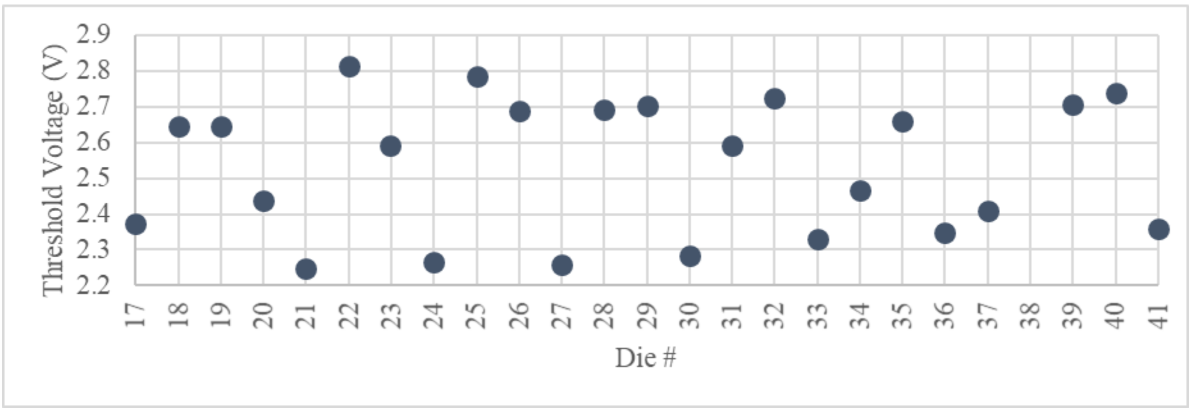


Figure 2-5. Threshold voltages of bare dies measured with the Keysight B1505a curve tracer

A total of nine modules were fabricated and will be identified by whether they are balanced or unbalanced and the number of the module. Dies were then selected with either similar or dissimilar threshold voltages accordingly for the balanced and unbalanced modules. For balanced module (4), Die 23 and 31 have similar threshold voltages and are paralleled in the top switch and Die 32 and 40 have similar threshold voltage and are paralleled in the bottom switch (Figure 2-6). The paralleled dies in each switch position turn on at the same time. For balanced module (6), Die 34 and 20 have similar threshold voltages and are paralleled in the top switch and Die 18 and 19 have similar threshold voltage and are paralleled in the bottom switch (Figure 2-7). For unbalanced module (8), Die 26 and 28 have similar threshold voltages and are paralleled in the top switch and Die 39 and 27 have dissimilar threshold voltage and are paralleled in the bottom switch (Figure

2-8). For unbalanced module (9), Die 35 and 37 have similar threshold voltages and are paralleled in the top switch and Die 24 and 29 have dissimilar threshold voltage and are paralleled in the bottom switch (Figure 2-9).

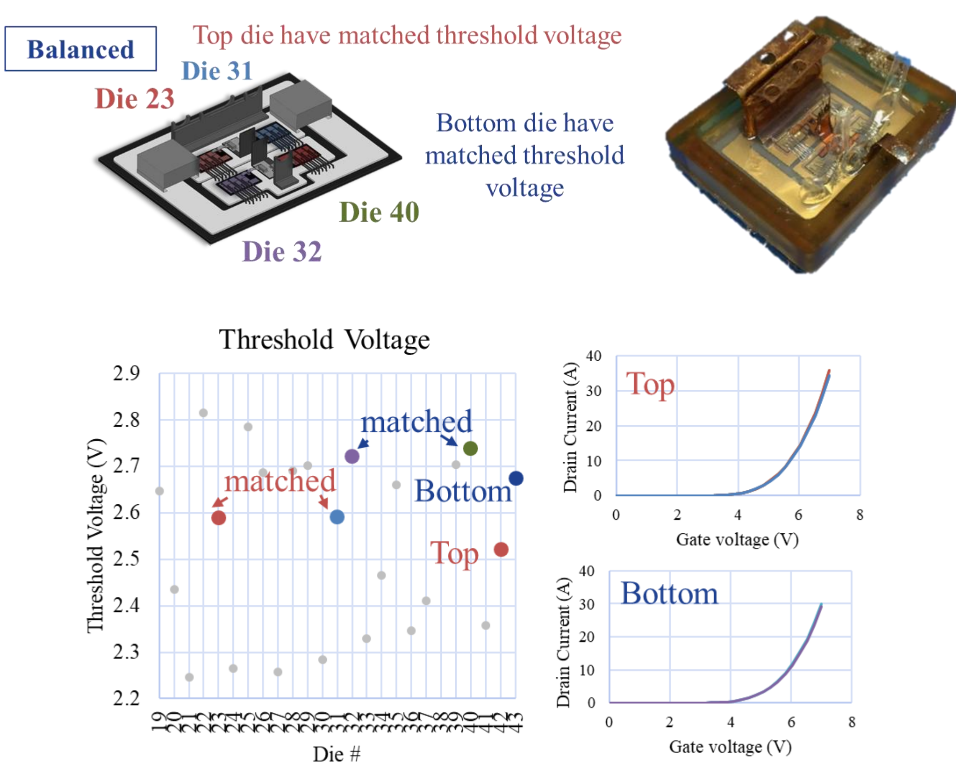
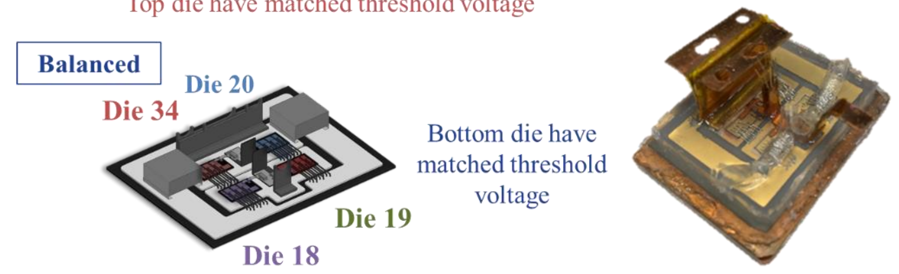


Figure 2-6. Die selection for a balanced power module (4) based on threshold voltages



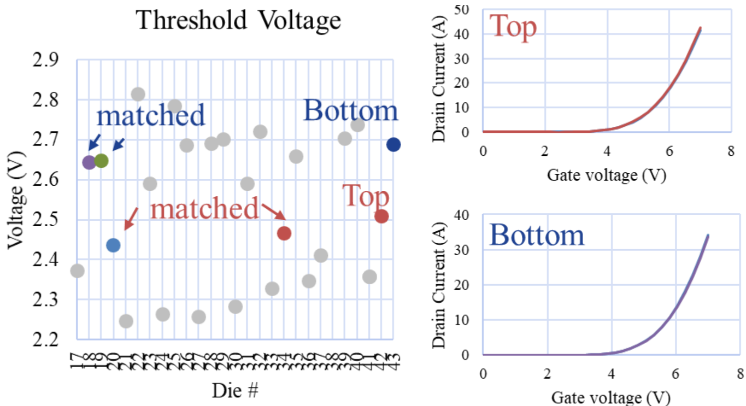


Figure 2-7. Die selection for a balanced power module (6) based on threshold voltages

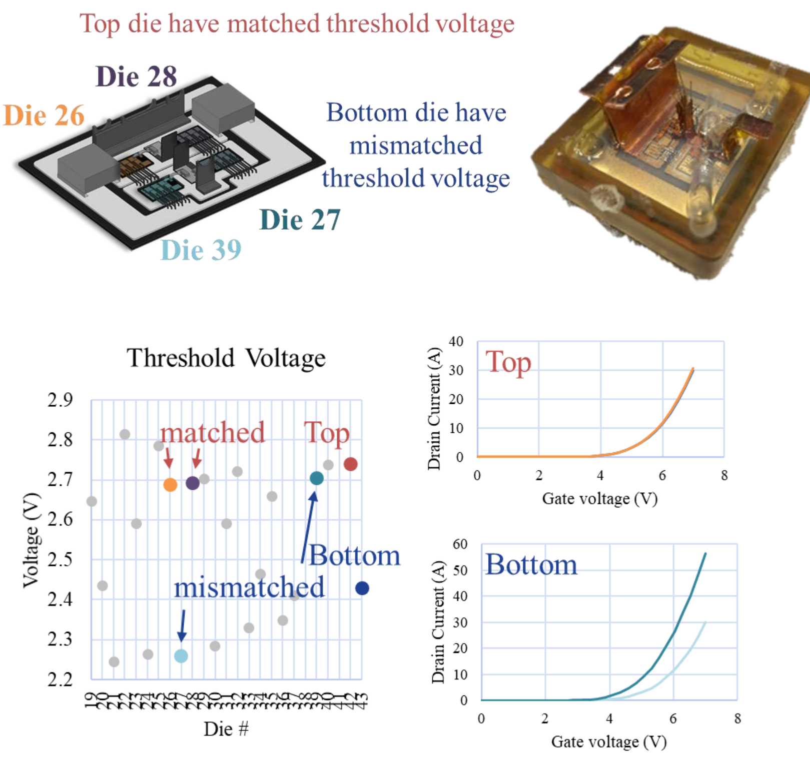


Figure 2-8. Die selection for a unbalanced power module (8) based on threshold voltages

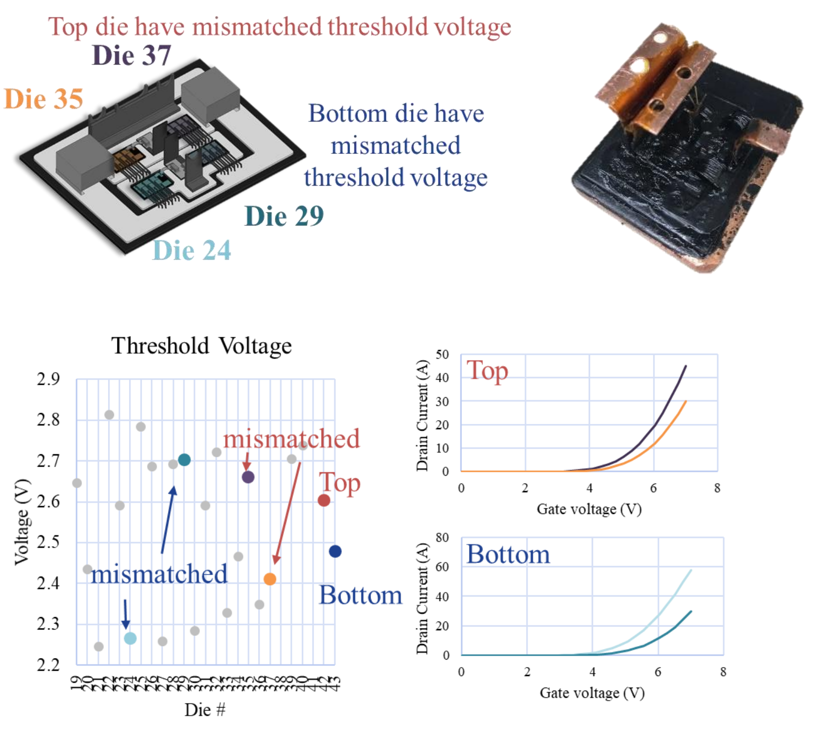


Figure 2-9. Die selection for a unbalanced power module (9) based on threshold voltages

(i) On-state resistance measurement

Ideally, the research would evaluate both the impact of dies' threshold voltage and on-state resistance. However, this requires an accurate relative measurement of the dies' characteristics so that the dies can be selected with dissimilar and similar on-state resistance measurements. Unfortunately, the bare die test fixture did not allow for accurate or precise on-state measurements. The values were in the 15-30 mΩ range instead of the expected 13 mΩ (Figure 2-10). CREE was consulted which explained that die testing is typically done on the fabricated wafer before being cut. Therefore, the source pad has much better contact than the bare die test structure we created. Accurate measurements were observable once the die was fully and properly packaged; however, that value corresponds to the paralleled dies and not each individual die. Not only were the values

too high, the relative values among dies were inconsistent so that it was not possible to determine similarities (Figure 2-11).

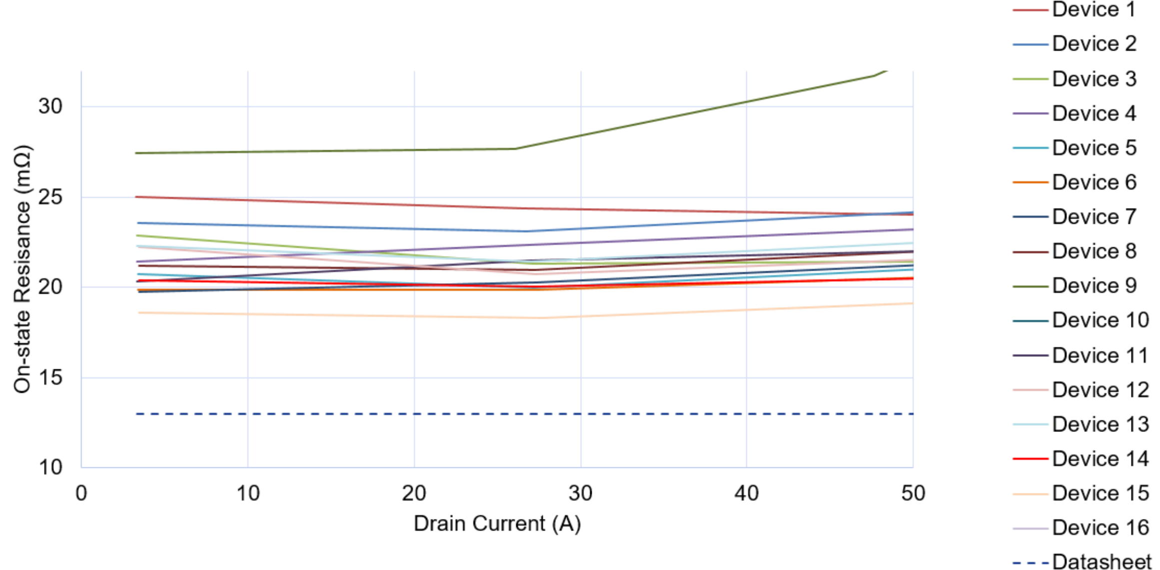


Figure 2-10. On-state resistance measurements of a subset of the CREE dies; high resistance due to the wires and pins of the test fixture

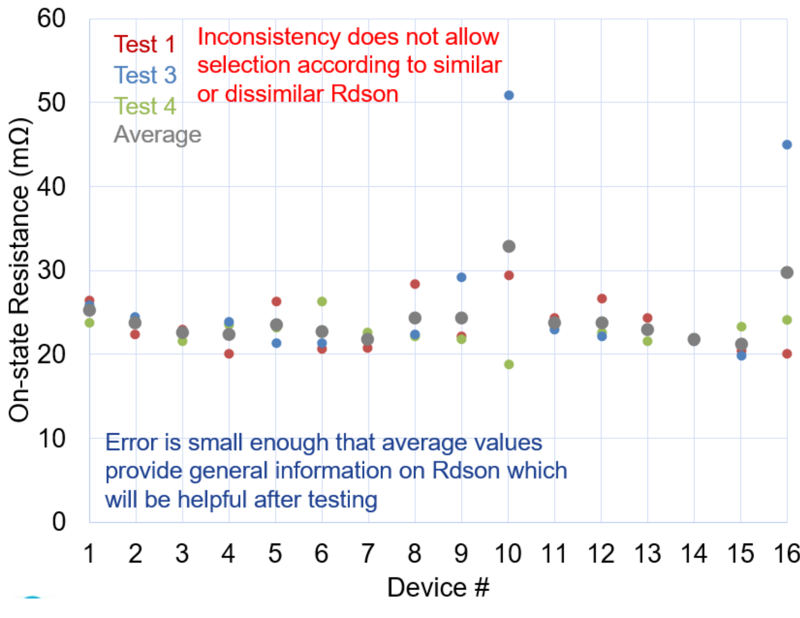


Figure 2-11. Resistances of bare die across multiple tests repeated with the same parameters

2.3.3 Flexible PCB for Gate Connection

Due to the faster switching and high dv/dt of SiC devices, the control loop is more susceptible to oscillations and noise coming from the power stage. Often the gate and power loops share parasitic inductance connected to the source of the dies, coupling the two loops. Additionally, the gate-source inductance, Lgs, is large because the current pathway and terminal often have high inductance (Figure 2-12). Noise in the power loop can be transferred to the gate loop because of the coupling and a large Lgs leads to significant gate loop noise, unintentionally turning the device on and off repeatedly which can damage the device or surrounding circuitry (Figure 2-13).

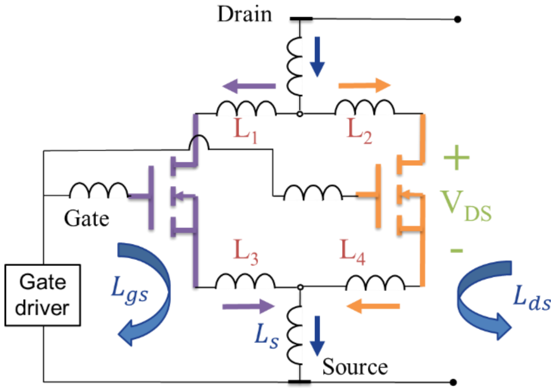


Figure 2-12. With a shared source inductance, gate and power loops are coupled and Lgs is large

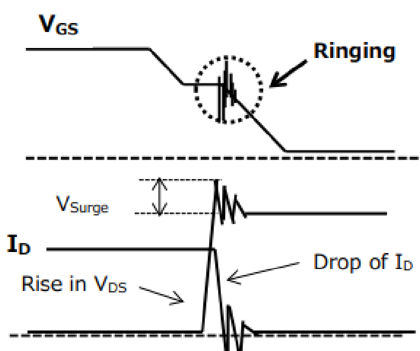


Figure 2-13. Voltage surge in V_{ds} and gate inductance can cause gate ringing which may lead to unintentional turn on and turn off [55]

Therefore, a flexible circuit is utilized for the gate loop as well as connections to the drain and source (Figure 2-14) to reduce the inductance typically more present when wire bonds connect the gate of the die to external leads. Wires have higher inductance as they are long and thin, whereas a flexible PCB in comparison, is essentially two copper planes stacked upon one another (Figure 2-15); copper planes have relatively lower inductance due to the higher ratio of area width to length and the mutual inductance of stacked copper planes also helps reduce the relative inductance (Figure 2-16) [40]. This method also decouples the gate and power loop with the use of kelvin source connections (Figure 2-17).

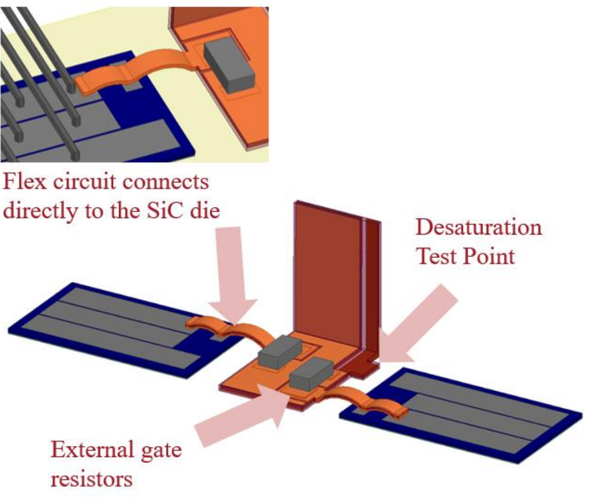


Figure 2-14. Connection of flexible PCB to die and substrate

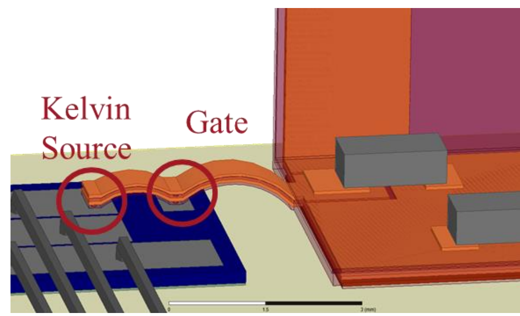


Figure 2-15. Overlap of kelvin source and gate planes reduces loop inductance

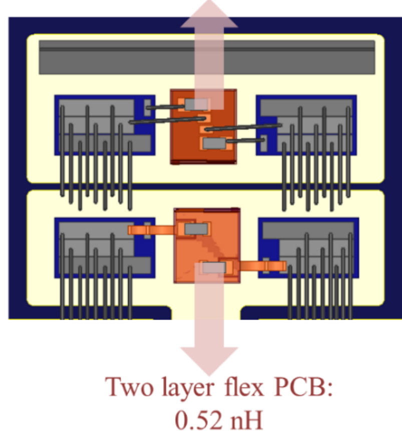


Figure 2-16. Comparison of flexible PCB and wire bond inductances simulated in Ansys Q3D

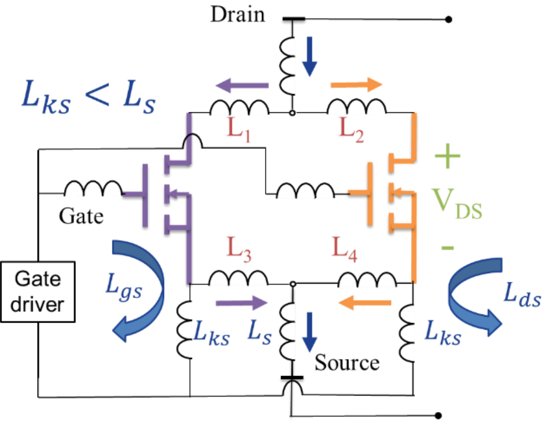


Figure 2-17. Adding kelvin source connection decouples the gate and power loops and reduces Lgs

Flexible PCB also increases contact surface with the die and subsequently improves heat distribution [40]. Modes of wire bond weakness and failure include mechanical stress and bending and thermal expansion mismatch between the wire and the die. In addition, mechanical damage can occur from the ultrasonic power or bonding force [56]. Temperature swings can eventually lead to crack failures and lift off [57]. Researchers have sought alternative methods for wire bonds which include using metal structures, ceramic, or polymeric connections; another solution is a

nickel coated die surface which demonstrated higher reliability in the nickel-aluminum contact at high temperature [56]. Implementation of flexible PCB with the use of solder attach could possibly mitigate the failure modes common to wire bonds (Figure 2-18).

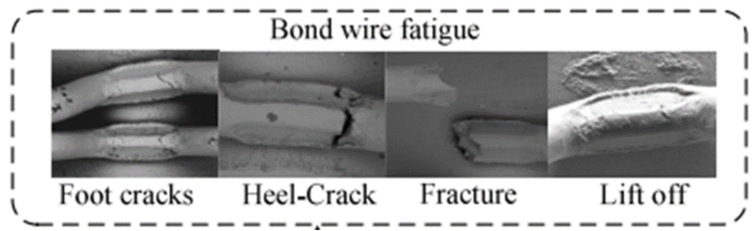


Figure 2-18. Wire bond failure mechanisms [58]

The base material of the flexible PCB is a double layer of 0.5 oz. copper separated by 25 µm polyimide. The final finish is electroless nickel immersion gold (ENIG) with a cover layer of 25 µm polyimide and 25 µm adhesive. The final copper weight after processing is around 1 oz.; details provided by Q-Flex Inc. The flexible PCB was designed so that external gate resistors could be soldered onto the top. This method takes advantage of the 3D structure so that the space above the die can be used. The flexible PCB bends upward and three wires provide external connection to the gate and kelvin source on the die and the desaturation connection on the substrate (Figure 2-19). In addition, the use of the kelvin source connection to the die may reduce current coupling [20].

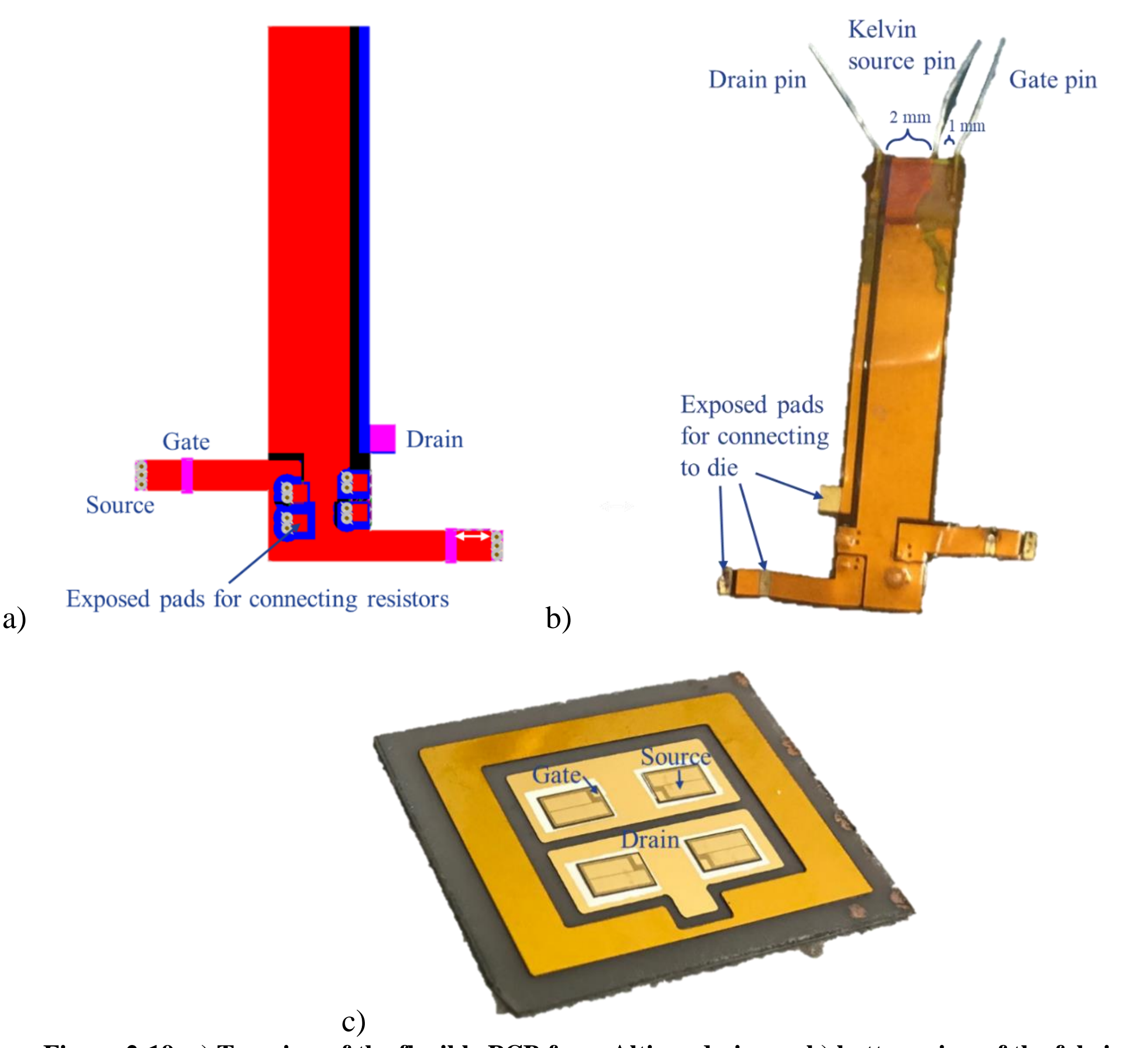


Figure 2-19. a) Top view of the flexible PCB from Altium designer, b) bottom view of the fabricated flexible PCB, and c) substrate with dies displaying connection points for flexible PCB

2.3.4 Use of the Body Diode in SiC MOSFET

Placement of the SiC MOSFETs and antiparallel diodes can improve power commutation [37, 59]. However, by using the body diode in the SiC MOSFET during dead time instead of external antiparallel diodes, even higher power density and lower cost is achievable [33]. In the case of Si MOSFET, the high reverse recovery loss negates the benefit of using the body diode [60] whereas it was found that with Wolfspeed's 1200 V, 13 mΩ SiC MOSFET, the reverse recovery of the

body diode does not contribute as much to the switching losses and the temperature does not have an effect either [61]. The stability of the body diode was verified in [62] although some research suggested forward biasing the body diode could reduce conduction current and increase leakage current [63]. Multiple studies have explored the feasibility of modules without external antiparallel diodes with promising conclusions of reverse recovery behavior in body diodes comparable to external diodes, more than twice the power density, and half the switching losses of similarly rated commercial modules [33, 60]. Therefore, for this device it is suitable and of interest to use the body diode in the SiC MOSFET for a smaller design.

Chapter 3 **Power Module Fabrication**

3.1 Package Material Selection

Table 2. PACKAGE MATERIALS

	Selected Material	***Reason***
Substrate	Au coated DBC - AlN	Solderability, ↓ CTE, ↑ k (170 W/mk)
Die attach	Kyocera nanosilver paste	Pressure less
Die	CREE CPM3-1200-0013A 1.2 kV 13 mΩ	Voltage, robust body diode, low resistance
Die interconnect	10 mil Al wire bonds (8 per die)	Manufacturability
Gate loop interconnect	Cu and Al flexible PCB (Au and Cu plating)	↓ inductance vs. wire bonds
Power terminals	21 mil Cu plates	Manufacturability
Baseplate attach	Sn63/Pb37 solder preform coated in flux	Void mitigation
Housing	Machined Duratron U1000 PEI	170 °C continuous performance
Heat sink	ATS-56005-C3-R0	Dimensions
Heat sink attach	Saint-Gobain C675	Manufacturability
Encapsulant	Nusil R-2188	High temperature capability

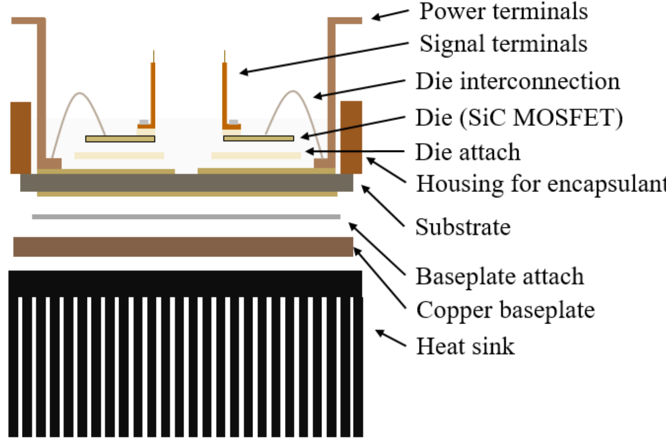


Figure 3-1. Elements of a package

3.1.1 Substrate Selection

Classical modules are built on a direct bonded copper (DBC) substrate which includes an internal ceramic insulation layer covered by top and bottom layers of copper. The ceramic of choice was aluminum nitride, AlN, and the copper was attached as direct bonded copper (DBC) as opposed to an active metal brazing (AMB) method (Table 2). The coating was electroless nickel followed by immersion gold. An AlN substrate has better thermal conductivity than alumina (Al_2O_3) and is more readily available than other substrates like silicon nitride (Si_3Ni_4) [64]. Initial tests utilized alumina but thermal cycle testing confirmed lower thermal reliability [33].

3.1.2 Attachment Selection

To attach the die to the gold coated substrate, a nanosilver sintering paste from Kyocera is used in pressure-less conditions (Table 2). Because the terminals and baseplate must be attached after the flexible circuit, using sinter paste allows for more flexibility in choosing solder pastes with compatible heat profiles. The power terminals are connected using solder paste. The copper base

plate is connected using a flux-coated solder preform to prevent voids and achieve better thermal impedance. In order to operate at high temperature with enough durability, all heat profiles should have a melting temperature above 175° (Table 3).

Table 3. Liquidis Points of Attachment Materials

Component	***Selected Material***	***Liquidis upon curing*** (°C)
Die sinter [65]	Kyocera nanosilver paste	961
Flexible PCB and Power terminals	Sn96.3/Ag3.7	221
Baseplate solder preform	Sn63/Pb36	183

Lifetime of power modules is highly dependent on the strength and reliability of the layers and materials connecting the passive and active components. Solder fatigue is a primary failure mechanism in power modules and thus, alternative technologies are desirable [32, 57]. Silver sintering technology is superior to solder technology in every way apart from cost as demonstrated by from Table 4 and is a lead free alternative [63].

Table 4. Solder and Sinter Property Comparison

Property	***unit***	***Solder layer SnAg(3.5)***	***Ag diffusion sinter layer***
Melting point	℃	221	961
Thermal conductivity	W/m/K	70	240
Electrical conductivity	MS/m	8	41
Layer thickness	µm	~90	~20
CTE	ppm/K	28	19
Tensile strength	MPa	30	55

Nanosilver sinter paste has many beneficial properties including low processing temperature, no aging at room temperature, insensitivity to strain rate, low thermal resistance, strong electrical

and dielectric properties, and a highly reactive surface [65-68]. This is result of the combined properties of polymer matrices and nanosilver fillers [65]. An alternative material for future investigation is copper sinter paste which demonstrated comparable shear strength but at a much lower cost than nanosilver sinter paste [43]. An extensive study was conducted on various silver sintering pastes and Kyocera nanosilver paste with resin reinforcing (CT2700R7S) was selected because it had high shear strength and minimum voids even when cured without pressure and in air.

3.1.3 Housing and Encapsulant Selection

Lastly, a housing structure is made from Duratron U1000 polyetherimide (PEI) from Quadrant which performs well up to 170°C. The structure secures the encapsulating material, Nusil R-2613, allowing for higher power performance.

3.2 Module Fabrication

3.2.1 Substrate Patterning and Cutting

The DBC substrate is patterned substrate with Kapton tape mask and ferric chloride etch (Figure 3-2). The Kapton tape protects gold and copper parts that form the conductive traces while exposed gold and copper on the substrate are removed using ferric chloride (Figure 3-3).

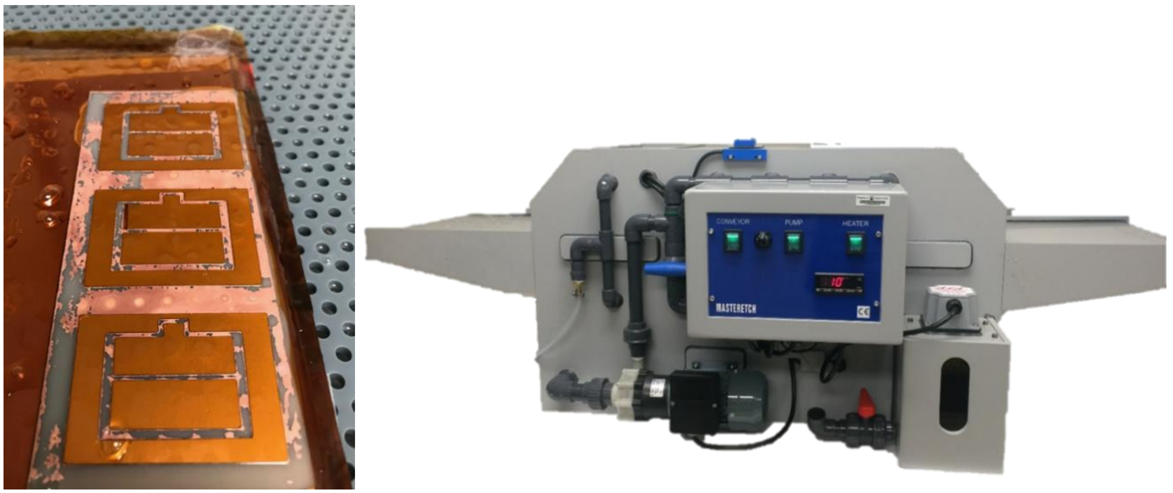


Figure 3-2. Partially etched DBC pattern with ferric chloride etching machine

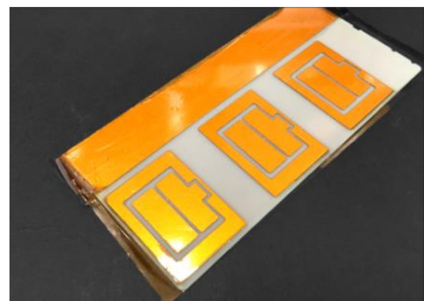


Figure 3-3. Patterned substrate after etching of unwanted metal using a Kapton tape mask

AlN ceramic is particularly tough to cut and therefore, 20-30 iterations of laser cutting are required and it is critical to make sure the laser is focused at the height of the ceramic as opposed to the height of the Kapton tape layer as before. Lastly, a modification of the DBC substrate is required to accommodate the wire bonds on the bottom switch (Figure 3-4).

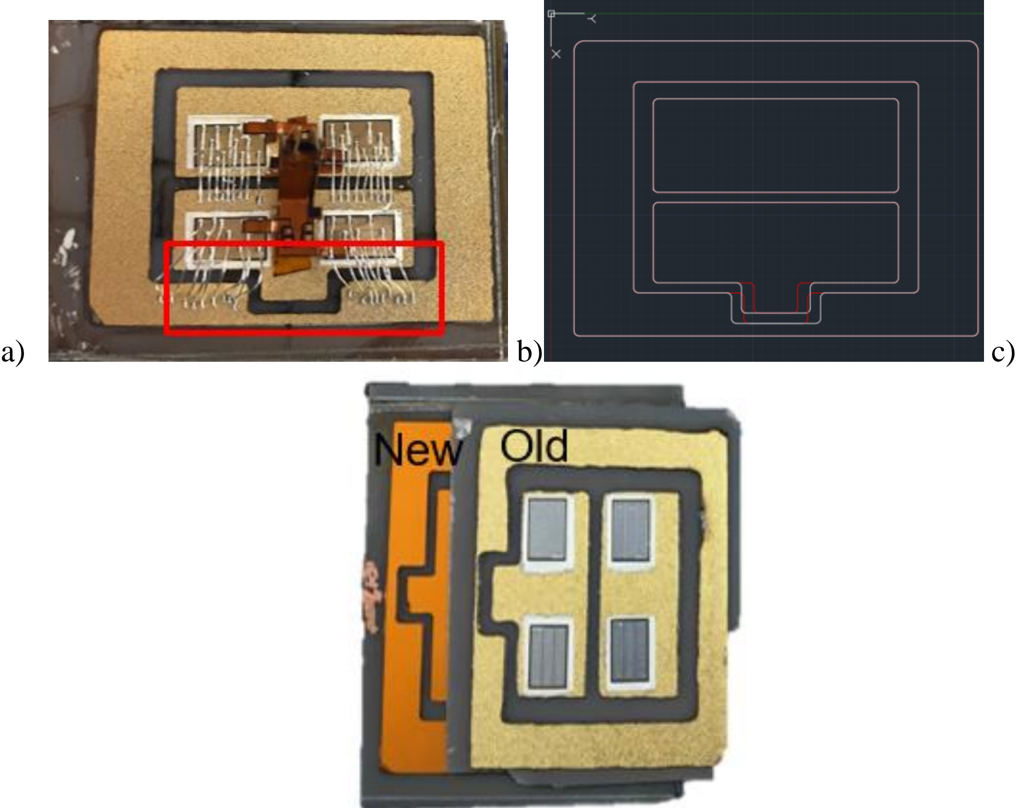


Figure 3-4. Undesirable bend in bottom device wires b. new design (white) vs old design (red) c. New vs old substrate pattern

3.2.2 Attachment Material Heat Profiles

To attach the die to the gold coated substrate, a nanosilver sintering paste from Kyocera is used in pressure-less conditions (Figure 3-5). The power terminals are connected using solder paste (Figure 3-6). The copper base plate is connected using a solder preform to prevent voids and achieve better thermal impedance (Figure 3-7). Careful attention must be paid to the order and material of the attaching pastes.

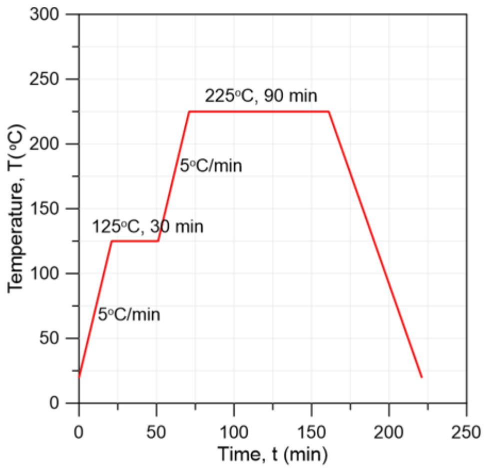


Figure 3-5. Heat profile for Kyocera nanosilver paste sintered under P=0

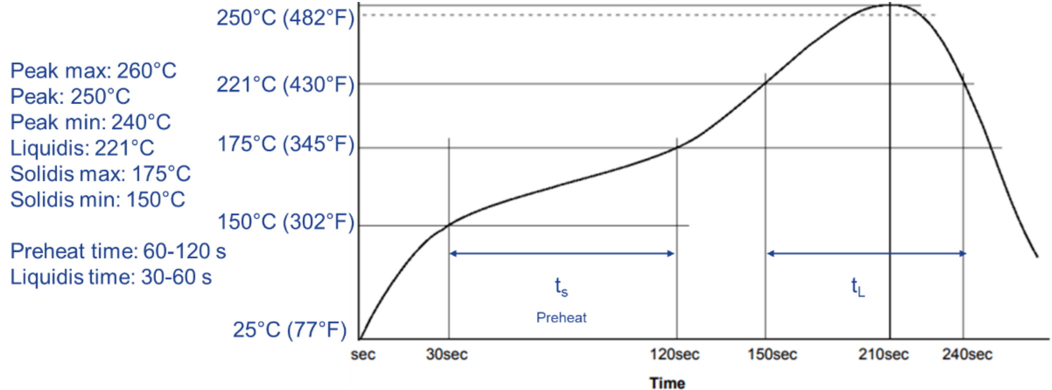


Figure 3-6. Heat profile for Sn96.3/Ag3.7 [69, 70]

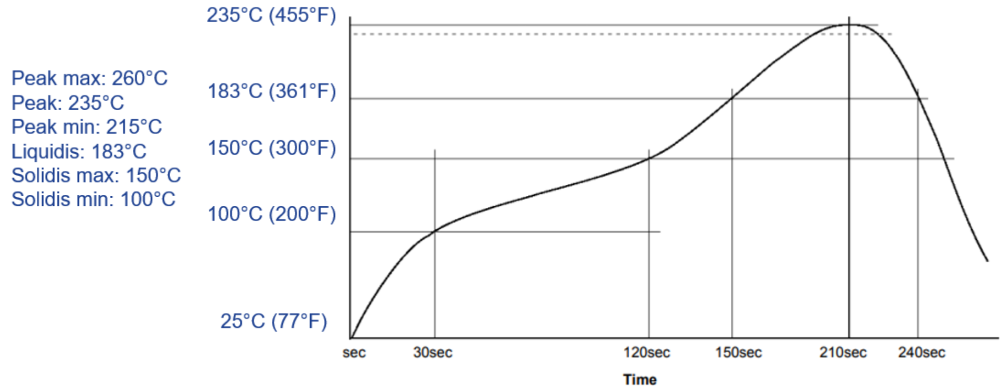


Figure 3-7. Heat profile for Sn63/Pb37 [71]

3.2.3 Die Attachment

The silver sinter paste is extruded in squares using a laser cut Kapton mask as a stencil (Figure 3-8). The printing process uses a squeegee to create a flat surface to prevent voiding (Figure 3-9). A vacuum pen is a simple but beneficial tool for picking up and placing the dies on the center of the printed squares of silver sinter paste. After the dies are placed onto the silver paste, each one should be moved slightly to ensure the paste contacts with the entire bottom side of the dies. Then, the Kapton mask is removed (Figure 3-10). Lastly, the substrate is put through a heating profile (Figure 3-5) using a programmable hot plate (Figure 3-11).

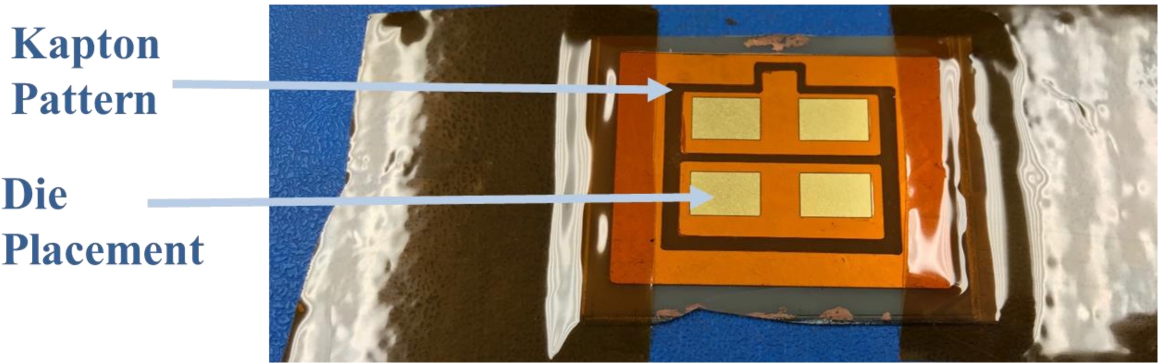


Figure 3-8. Laser-cut Kapton mask placed on DBC substrate

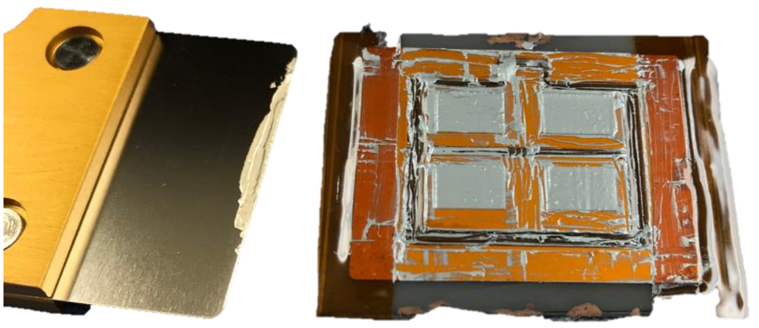


Figure 3-9. Sinter paste printed into Kapton mask

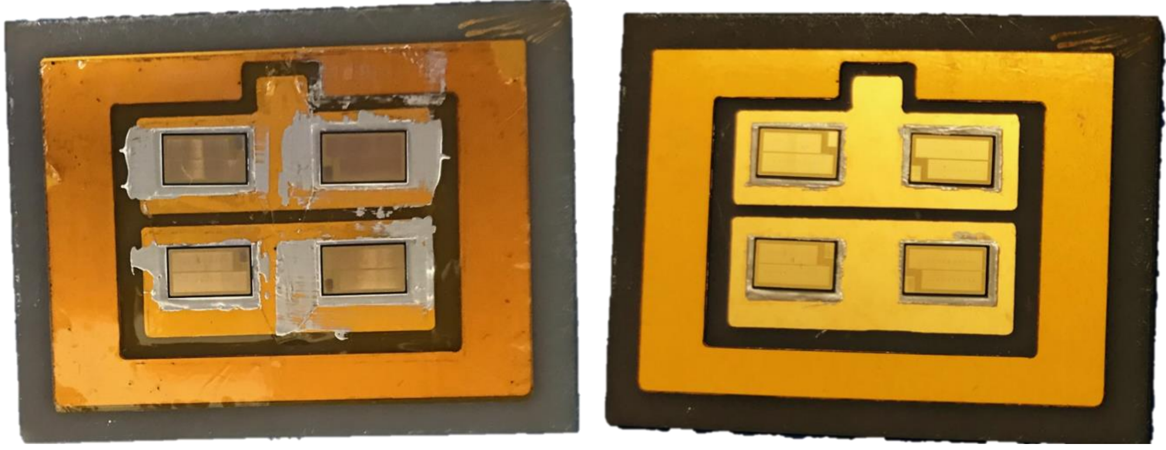


Figure 3-10. Dies are placed onto printed sinter paste squares and Kapton mask is removed

Figure 3-11. Substrate placed onto programmable hotplate

Test dies were sheared using the Nordson DAGE 4000 Multipurpose Bondtester (Figure 3-12). An ideally sheared die will have attachment material coating both the die and the substrate indicating no significant voids in the attachment joint, which was mostly the case experimentally (Figure 3-13). The shear strength should be above 5 kg according to MIL-STD-883E, 2019.5 Die Shear Strength. The test dies sheared at 69.5 kg and 40 kg, 21.6 MPa and 12.4 MPa, respectively (30). This demonstrated that the die attachment methodology and material were sufficient.

$$MPa = \frac{Force\ (kg)}{Size\ (cm^2)} * 1e^4 \left(\frac{cm^2}{m^2}\right) * g\ \left(\frac{m}{s^2}\right) * 1e^{-6} \left(\frac{MPa}{Pa}\right) \tag{30}$$

$$g = 9.80665 \frac{m}{s^2}$$

$$Pa = \frac{kg}{m * s^2}$$

$$Size\ (cm^2) = 0.725\ cm\ * 0.436\ cm = 0.3161\ cm^2$$

$$\boldsymbol{F_1 = 69.5\ kg = 21.6\ MPa}$$

$$\boldsymbol{F_2 = 40\ kg = 12.4\ MPa}$$

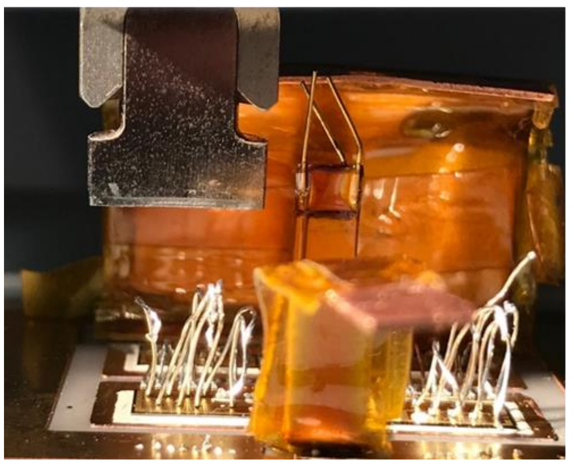
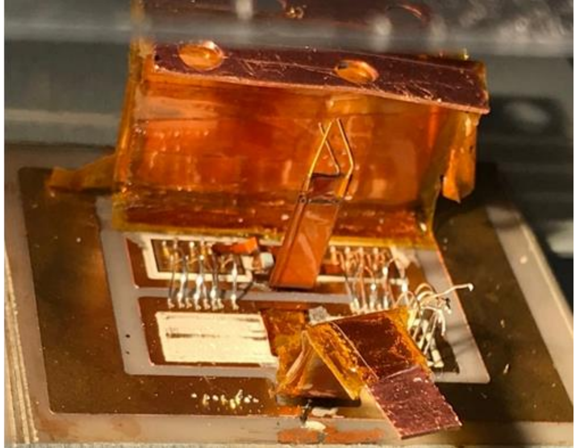



Figure 3-12. Die shear test with the Nordson DAGE 4000 Multipurpose Bondtester

Figure 3-13. Sheared die with bottom side coated in cured nanosilver sinter paste

3.2.4 Die Interconnection

The sources of the paralleled top side die are connected to the AC pad and the sources of the bottom side die are connected to the DC- pad with 10 mil Al wire bonds using the tpt HB30 heavy wire bonder (Figure 3-14).

Figure 3-14. tpt HB30 Heavy Wire Bonder

To allow for high currents to flow through the power module, eight wire bonds are needed per die (Figure 3-15). Specifically, each bond wire can carry 15 A (31) so the wire bond constraint for each die is 120 A. In addition, based on the recommendations from the wire bonder, the spacing between wire bonds should be about 1.14 mm and the pad size should be 25 mil x 40 mil.

$$I = k * d^{1.5} \tag{31}$$

d = diameter of wire-bond = .01 inch

$\kappa = \frac{\pi}{2}\sqrt{\frac{h}{p}}$ = constant based on material = 7,585

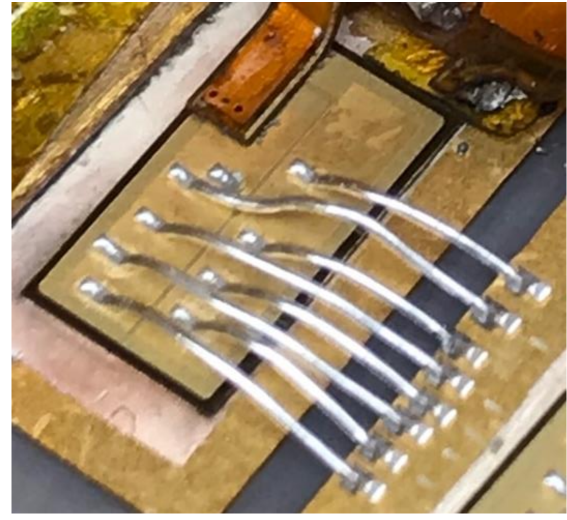


Figure 3-15. 8 cascaded wire bonds per die

Rogowski coils are used to monitor the current behavior. In order to ensure the stability of this measurement method, the wire bonds of the bottom side die are placed with arches that have a diameter slightly larger than the Rogowski coil (Figure 3-16).

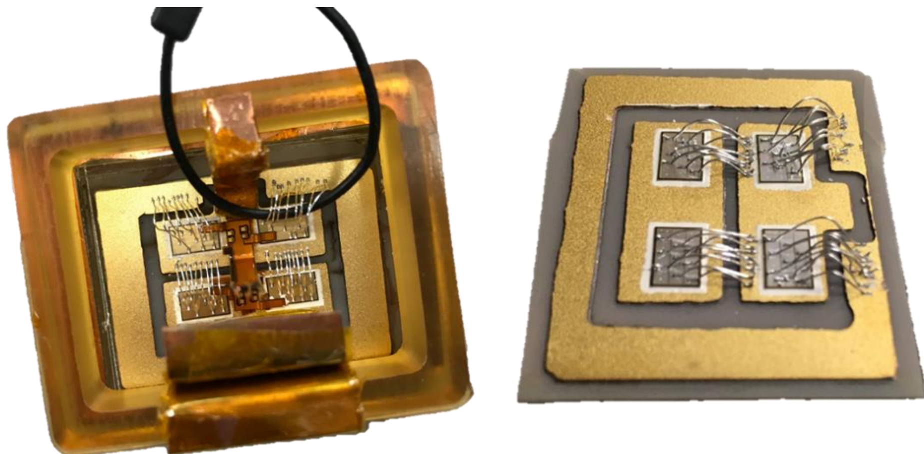


Figure 3-16. Wire bonds tall enough to fit Rogowski coil loops underneath

Lastly, a wire pull test is conducted using the Nordson DAGE 4000 Multipurpose Bondtester. According to MIL-STD-883F, 2011.7 Destructive Bond Pull Test (Figure 3-17), the minimum pull force of each bond should be above 100 g and all test bonds passed (Figure 3-18).

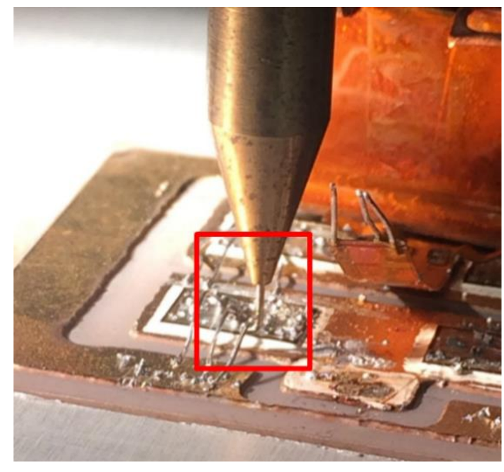


Figure 3-17. Microscopic view of the pull test

Test Detail

Test	Force	Type
1	380.71 g	Pass
2	335.35 g	Pass
3	327.10 g	Pass
4	377.15 g	Pass
5	238.72 g	Pass
6	385.64 g	Pass
7	306.55 g	Pass

Figure 3-18. Destructive wire pull test results

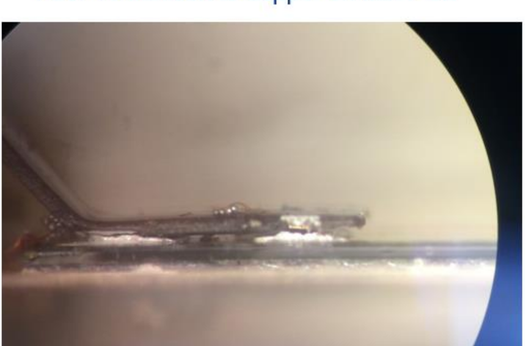
3.2.5 Flexible PCB Attachment

Attaching the flexible PCB on the bare die is challenging due to heat sensitivity of the die, incompatibility of some attachment materials to the die, and the small area available for attachment which can lead to shorting of the die terminals. Solder paste, due to the excess flux, is less viscous and placement of the paste will change during curing as the flux burns away which could create electrical shorts. Sinter paste has higher viscosity so the placement before curing and after curing is nearly unchanged; this property is beneficial because the attachment material needs to be constrained to the small pads of the die. Sinter paste was the original material choice because it

would not melt during the curing steps for the power terminals and baseplate later. However, the sinter paste has poor pull strength despite strong shear strength which led to cracking in many of the joints and repeated failure of the bonds (Figure 3-19).

Therefore, the flexible PCB is attached using the solder paste; typically, this process is not feasible because bare dies often have an aluminum topcoat compatible with aluminum wire bonds but not with nanosilver or solder paste (Figure 3-20).

Poor connection to copper on flex PCB



Strong connection to copper on flex PCB

Figure 3-19. Connections with sinter method

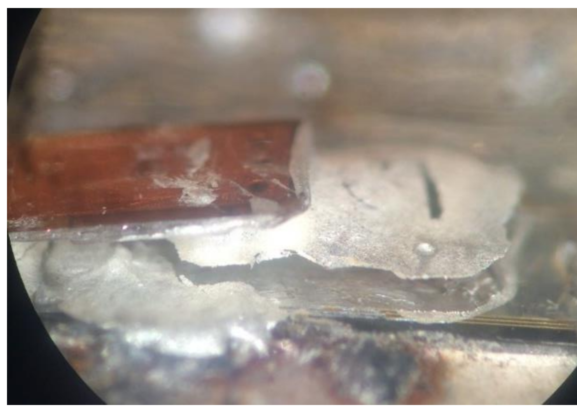


Figure 3-20. Microscopic image of sinter paste not adhering to aluminum surface of die

The dies for this module have a nickel: gold topcoat. Furthermore, additional space (0.6 mm) is added between the gate and source pads to reduce the likelihood of shorting (Figure 3-21).

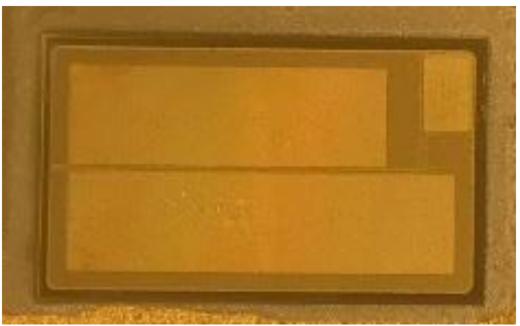
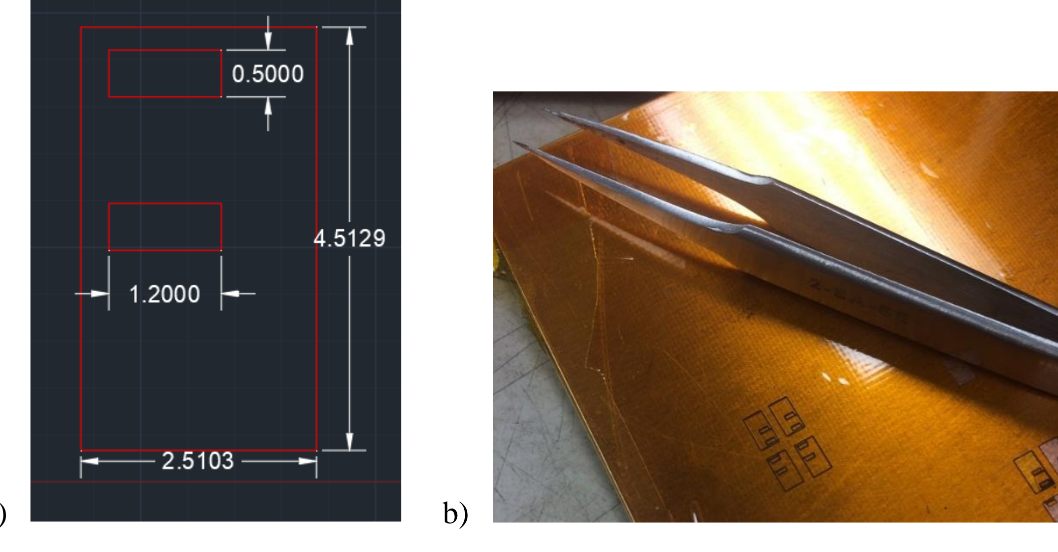


Figure 3-21. Die with nickel:gold topcoat and space around the gate terminal

Small, laser-cut Kapton masks constrain the paste to the 0.5 mm x 1.2 mm gate and source pads of the die (Figure 3-22). The size of the Kapton mask requires careful placement underneath a microscope. Once secure, the open space is filled with solder paste and the mask if removed. Lastly, a piece of double-sided Kapton tape sits underneath the position of the flexible PCB to secure it when curing (Figure 3-23). In order to align the flexible PCB over the gate and source of the dies, the gate and source wings are bent and the length is adjusted in order to fit the unique location of each die (Figure 3-24).



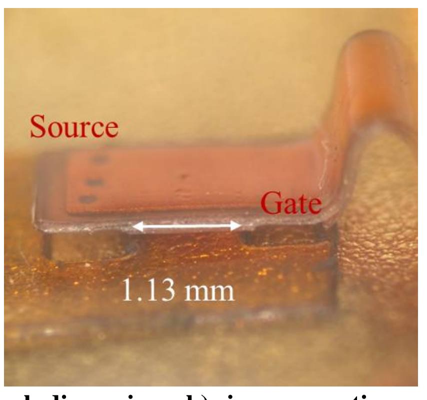
c)


Figure 3-22. a) Laser-cut Kapton mask dimensions, b) size perspective against tweezers, and c) only 1.13 mm between gate and source of the die

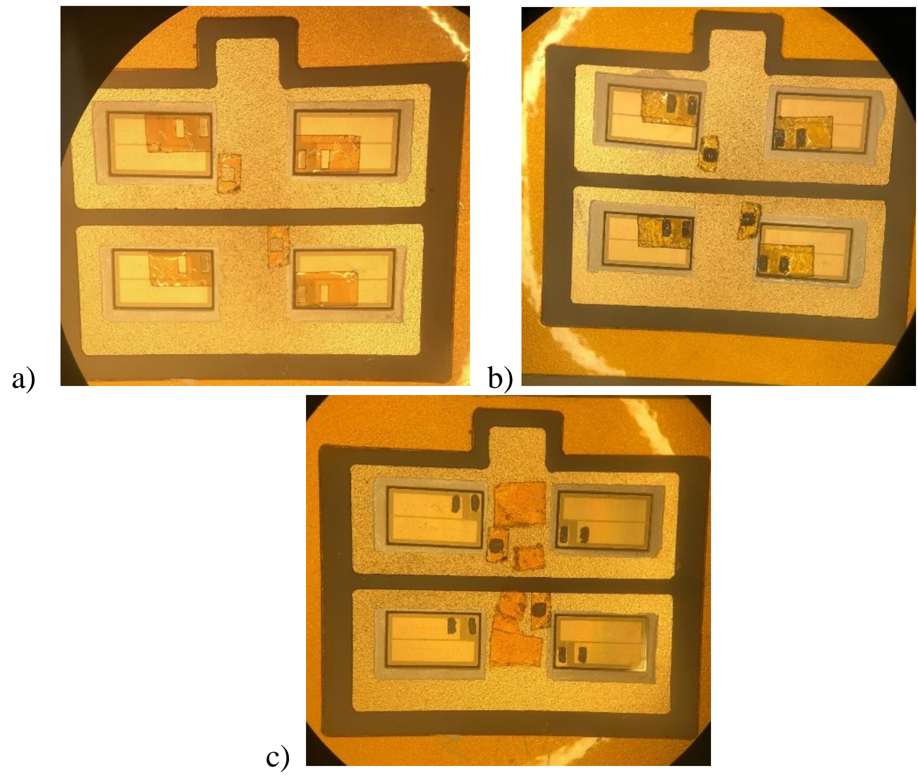


Figure 3-23. Microscopic image of a) solder masks placed onto dies, b) filled with solder paste, and c) masks removed with double-sided Kapton tape placed on substrate below flexible PCB

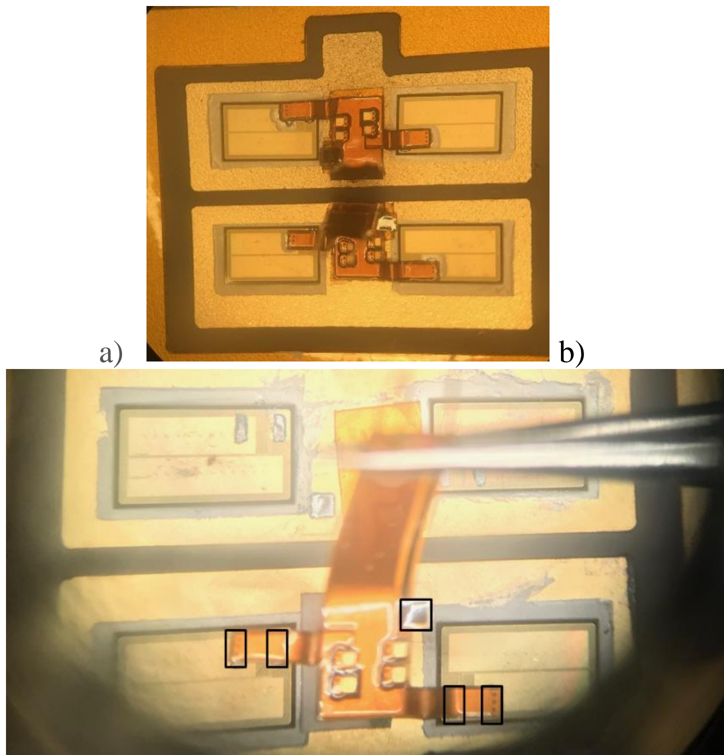
a)  b)

Figure 3-24. Microscopic image of a) flexible PCB secured onto die and substrate and b) tweezers used to carefully align flexible PCB pads onto the source and gate of the parallel dies

The flexible nature of the PCB allows for unique positioning onto the dies but also creates elasticity in the connection; without downward force, the flaps will pop up and prevent a strong connection to the dies (Figure 3-25). In addition, the flexible PCB may shift during curing which may reduce the strength of the connection or completely disconnect (Figure 3-25). Therefore, a fixture is fabricated that applies pressure to the four flexible PCB flaps above the four dies in the module (Figure 3-26).

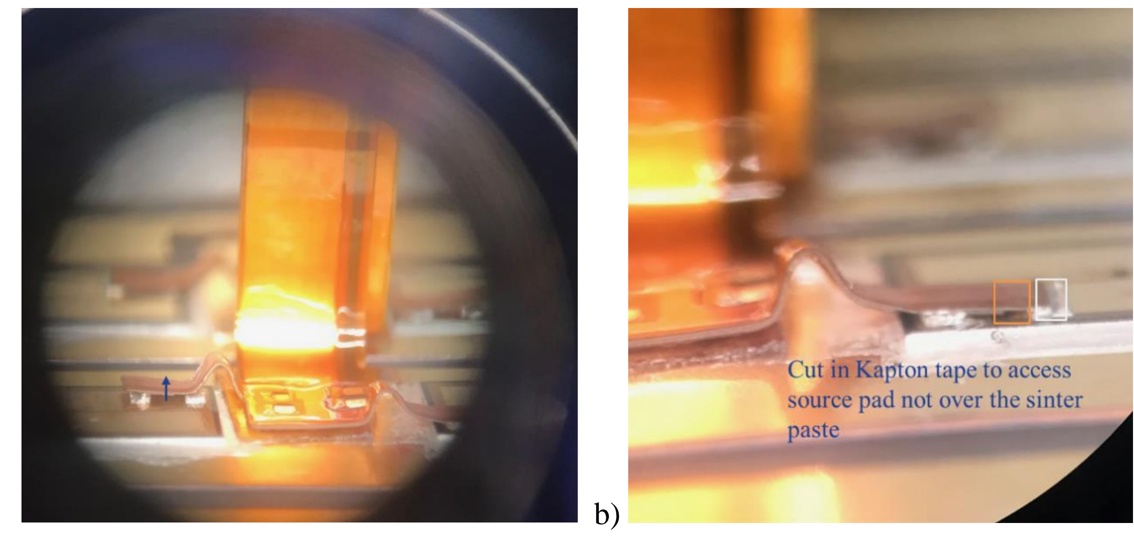


Figure 3-25. Microscopic image of a) flexible PCB flap pulled upward by elastic force and b) shifted flap away from the source and gate pads of the die

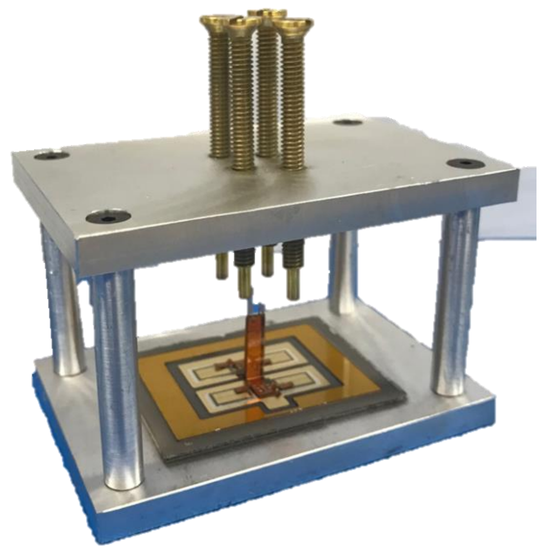


Figure 3-26. Fixture for use during curing of the flexible PCB connection

There are four screws with the correct dimensions to fit onto the flexible PCB flaps. After the flexible PCBs have been secured onto the double-sided Kapton tape and dies, the substrate is slid into the test fixture. Each screw is iteratively turned and lightly touch the flexible PCB before

tightening (Figure 3-27). It is very important to only turn the screw slightly once contact has been made; the flexible PCB should not move easily but too much pressure will damage the dies.

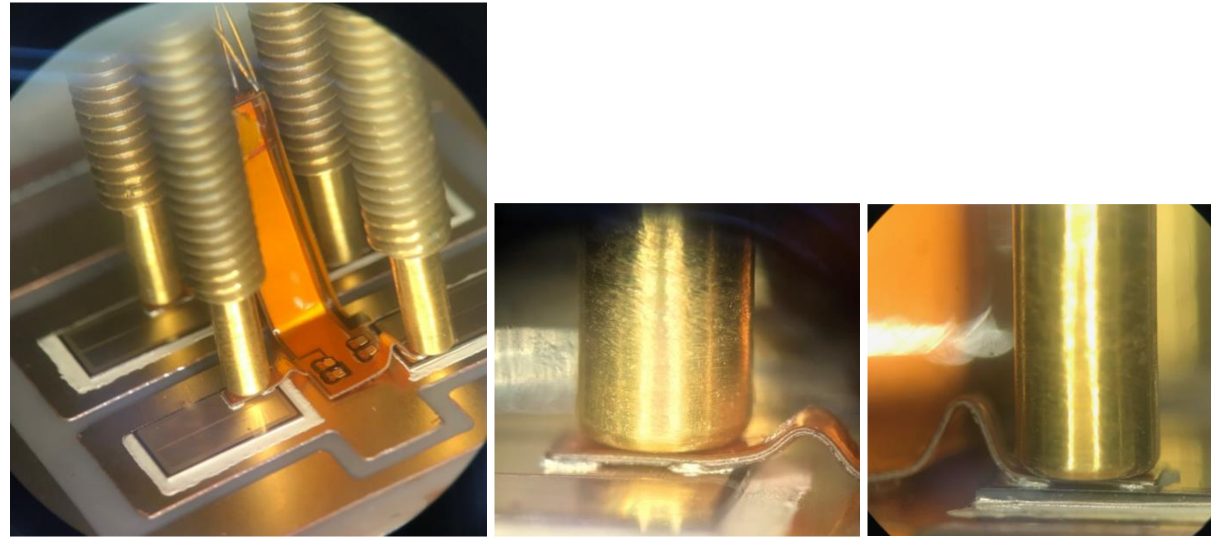


Figure 3-27. Microscopic images of screws flush against the flexible PCB flaps

3.2.6 Power Terminals

The original design for the power terminal connection was creating pins that would interface with vias on the capacitor bank board (Figure 3-28). A stronger connection is designed with screw holes on the power terminals and the capacitor bank board which requires updates to the capacitor bank PCB (Figure 3-29-Figure 3-31). A metal hole puncher is used to create screw holes on the power terminals before the terminals are bent using pliers. In the future, it is recommended to purchase power terminals because cutting and bending the terminals manually will not create a perfectly flat connection surface [72]. Fabricated busbars are affordable and fast and therefore the cost and time is not too extreme to warrant in-home fabrication. However, the final design is effective at providing power to the module. The current carrying capacity of the DC and AC terminal is estimated using a formula for PCB traces which determined that the DC terminals could

carry up to 360 A and the AC terminal could carry up to 110 A (32) [73]. The thickness of the terminals is 21 mil and the "k" value is selected based on classifying the trace as an external layer.

$$I = k\Delta T^{0.44} A^{0.725} \quad (32)$$

Using 0.55 mm (21 mil) copper planes

Where:

$$A_{DC} = 14.3\,mm^2$$

$$A_{AC} = 2.75\,mm^2$$

$$\Delta T = 50°C$$

$$k = 0.048$$

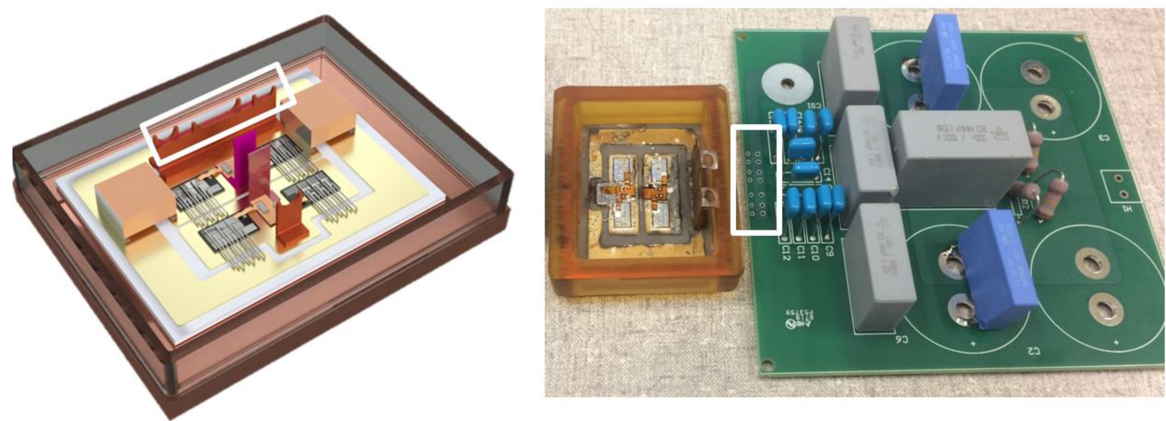
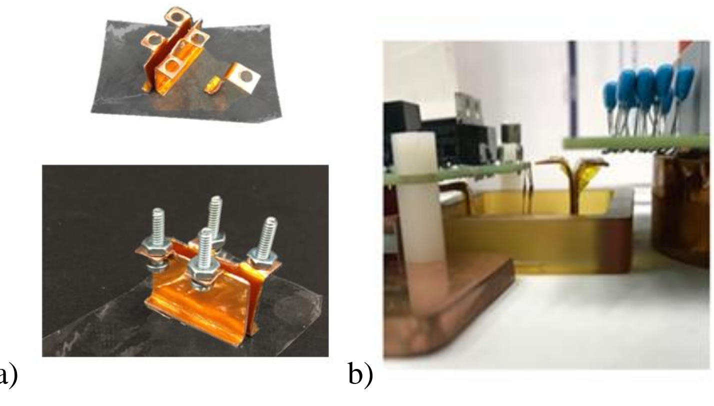
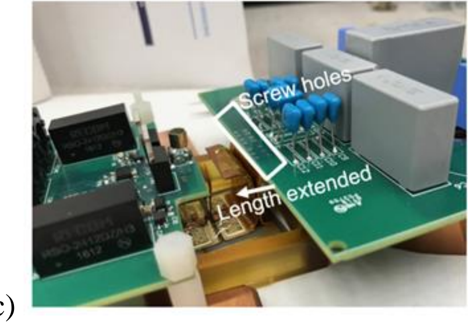


Figure 3-28. Original design of power terminals to interface with vias on the capacitor bank board



a) b)



c)

Figure 3-29. a. New design of power terminals with screw connections; b. the power terminals sit flush against the capacitor bank board c. which required updates including adding screw holes and extending the board

Inductive load connection

Screw holes for Vdc + and Vdc – power terminal connection

Figure 3-30. Updated design (Altium) of the capacitor bank replacing the via connection with screws

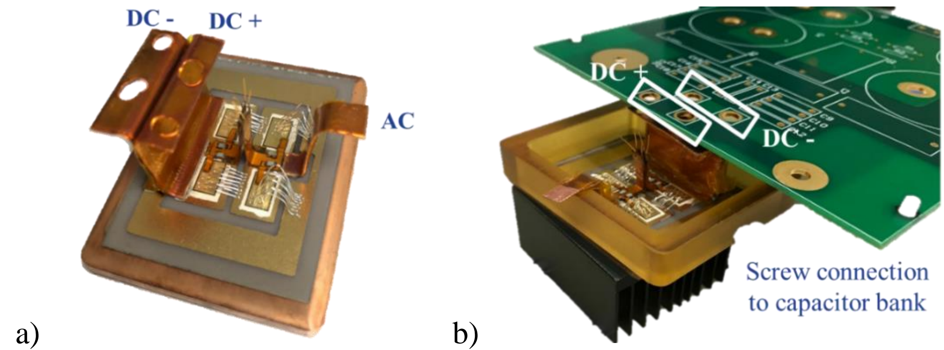


Figure 3-31. a) Final design of the power terminals b) which interface with the capacitor bank using screws

3.2.7 Thermal Management

A copper baseplate is utilized for spreading heat and a heat sink and fan are used to remove heat from the module. The copper baseplate is attached with a flux-coated Sn63/Pb37 (Figure 3-7) preform (Figure 3-32). To evaluate the effectiveness of the connection, an x-ray image was made of two samples (Figure 3-33). However, the copper was too thick to observe contrast in the solder layer. Therefore, the samples were sent to the National Renewable Energy Laboratory (NREL) in order to use a C-mode scanning acoustic microscope (C-SAM) to evaluate the voiding in the solder attachment layer (Figure 3-34). The C-SAM analysis demonstrates less than 7% voiding in both samples which is less than the 50% expected maximum for effective bonding.

Figure 3-32. Solder preform sits between the baseplate and the DBC

Figure 3-33. Baseplate attachment process for the two test samples and x-ray image of the sample

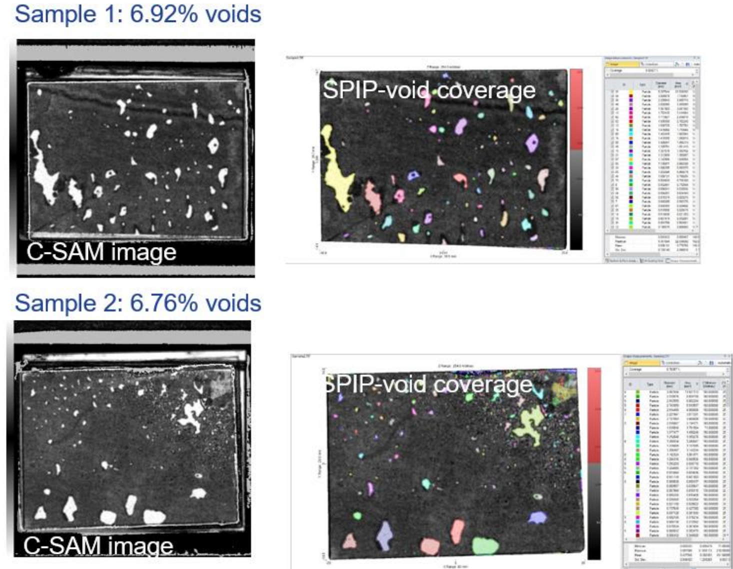


Figure 3-34. C-SAM image of the voids in the solder attachment to the baseplate

Figure 3-35 presents the process for attaching the baseplate to the power module with the last images showing the cured layer in between the baseplate and substrate. The heat sink, ATS-56005-C3-R0, includes an adhesive, high-performance thermal interface material, Saint-Gobain C675 [74]. Lastly, the fan used for cooling during the continuous testing is PF40561BX-000U-S99 which has an air flow of 31.7 CFM. Using an airflow calculator based on a 40 mm circular duct, the air velocity is calculated as 2.98 m/s which is used to estimate the thermal resistance of the heat sink [75, 76].

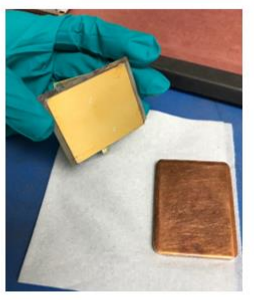
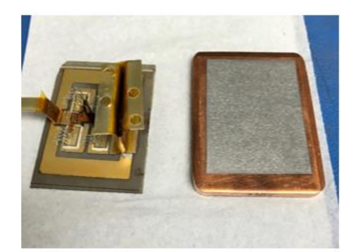



Figure 3-35. Processing for attaching the baseplate to the power module with cured layer displayed

3.2.8 Housing and Encapsulant

Housing for the power module can serve multiple purposes. If the package needs to be hermetic, impervious to moisture and gas, or functional in high-temperature environments, it may be important to pay attention to the material or manufacturing process [19, 56]. In this case, the main purpose of the housing is to hold the encapsulant in place as it cures from liquid to solid. The housing could provide more protection for the module as well. The rectangular housing rests on top of the baseplate and should be sealed around the substrate (Figure 3-36). The primary design constraints are ensuring it does not melt or become unreliable at 175°C, the approximate temperature for an automotive environment. The material of choice is donated Quadrant Duratron U1000 PEI, polyetherimide which performs in continuous use up to 170°C [77]. Randy Waldron, the Laboratory Instrument Maker with Virginia Tech Industrial and Systems Engineering machine

shop cut the material (Figure 3-37). It is attached with generic sealant from the hardware store and cures in 24 hours (Figure 3-38).

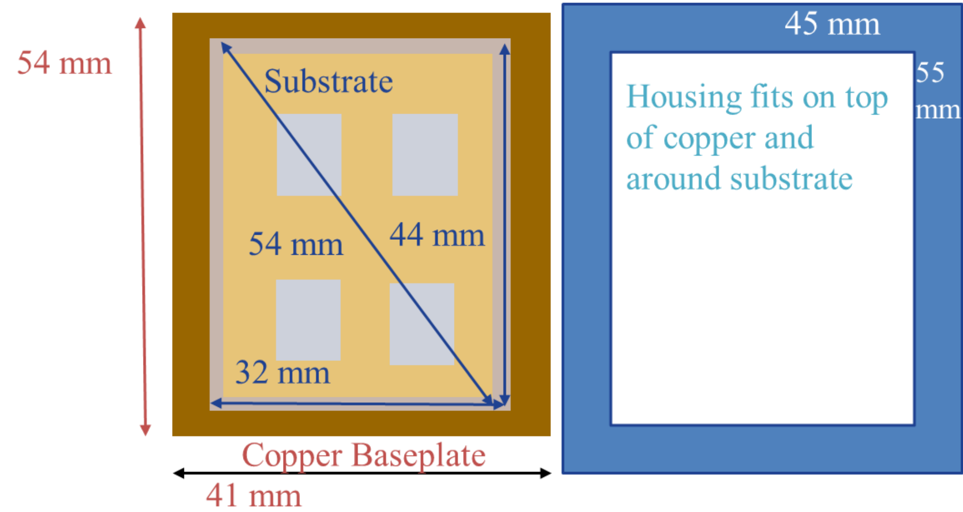


Figure 3-36. Approximate dimensions of housing to rest on the baseplate and edge of the substrate

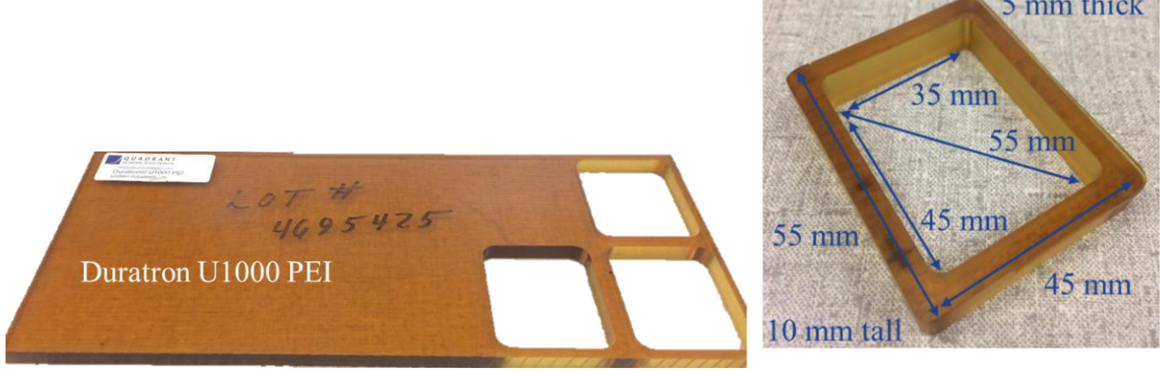


Figure 3-37. Duratron U1000 PEI material and housing machined by Virginia Tech

Figure 3-38. Attachment of housing with generic sealant

Encapsulant provides mechanical and electrical insulation for the power module [19, 56]. Nusil R-2188 is cured by mixing two parts equally. The instructions for encapsulation are described and shown below (Figure 3-39) which include two degassing stages to remove bubbles which could cause shorting and destruction of the module. In order to utilize the Rogowksi coils after encapsulating the module, plastic tubes are looped underneath the bottom switch wire bonds (Figure 3-40).

Encapsulant instructions:

1. Use gloves

2. Remove metal guard from tube
3. Remove plastic cap; use flat screwdriver or other tool to wedge it out because it may be sealed shut
4. Mix Part A and Part B equally by pushing down on the tubes
5. Stir well
6. Place in vacuum to remove air bubbles for 30 minutes minimum at room temperature
7. Pour into module, place in vacuum to remove any bubbles
8. Cure according to datasheet

Vacuum instructions:

1. Make sure top right vent knob (black with white sticker) is closed (vents the chamber)
2. Make sure vacuum knob (larger bottom right) is open (opens connection to pump)
3. Close door
4. Start the pump (under the table) by flipping the switch
5. Press against the door to improve the seal. Only need to do this for a couple of seconds and then the vacuum will hold the seal for you.
6. Once pressure gets to ~28, close the vacuum knob (closes connection to pump)
7. Turn off pump
8. Once done, open vent knob to vent the chamber (door will open automatically)
9. Reset: close the vent knob and open the vacuum knob

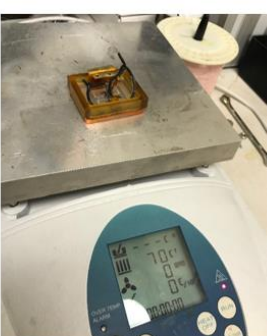


Figure 3-39. a. Two parts of encapsulant are mixed producing bubbles b-c. Bubbles are removed using a vacuum d. Encapsulant is poured into the module producing bubbles e. Bubbles are removed f. Encapsulant is cured at 70°C for 4 hours

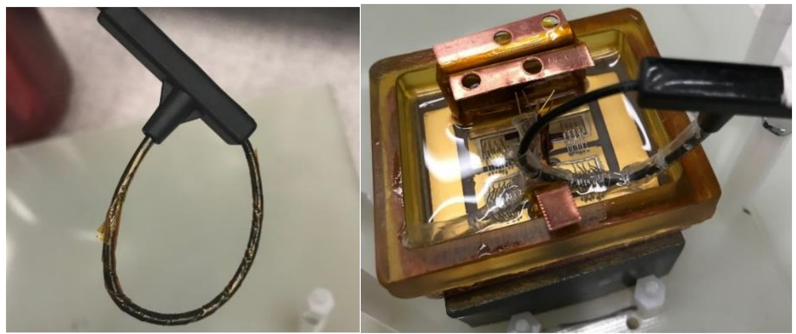


Figure 3-40. a. Rogowksi coil coated in Kapton tape for protection against scratching b. Rogwoski coil looping through plastic tubing and under bottom switch wire bonds

Module 9 was covered firstly with 2 layers of Silicone Conformal Coating (Dielectric) from MG Chemicals then 2 layers of Liquid Tape Spray from Performix (Figure 3-41). In theory, this would allow for monitoring of the temperature for individul dies because the black coating is non-reflective for the infrared camera. This method did not work well in our test setup; others have managed to achieve favorable results so we may not have used a large enough resistance to accentuate losses, had too thick of a dielectric layer, or had too much cooling from the fan [59]. In addition, the liquid tape was placed into the vaccuum as it cured but the cure time is a few minutes as opposed to many minutes or hours for Nusil R-2188 which provides time for the bubbles to come out of the liquid and then resettle flat; the bubbles in the liquid tape created craters that remained after curing.

Figure 3-41. Module 9 alternative encapsulation technique for black surface IR camera compatibility

3.2.9 Summary of Fabricated Module Yield

Nine modules were fabricated; four modules broke due to wire bond force breaking the dies, problems with the flexible PCB, and gate-source shorting. Five modules were fully fabricated and tested, two balanced and three unbalanced. One module (7) had a drain-source short on the top switch; the wire bonds were cut to disconnect the top dies and a diode was placed from DC+ to AC. Lastly, the last module (9) was not encapsulated in Nusil R-2188 silicon gel but with insulating spray in order to have a more access to the dies for thermal measurement which will be explained in the thermal testing chapter.

Module	Image	Status	Issues
1 Balanced		Broken	Pin snap G-S on flex shorted in repair attempt
3 Balanced		Broken	Wire bond force too strong
5 Unbalanced		Broken	Flex was not attached; G-S on die shorted during repair attempt
2 Unbalanced		Incomplete; Resistance on bottom die 2x	Could switch and see if one die is broken

Module	Image	Status	Issues
4 Balanced		Complete	
6 Balanced		Complete	
7 Unbalanced		Complete	Bot. switch blocks 1.2 kV Top switch 400 V BD may be due to dust?
8 Unbalanced		Complete	
9 Unbalanced		Complete	Encapsulated with clear and tape insulating spray

Chapter 4 **Power Module Characterization**

4.1 Static Characterization

4.1.1 Introduction

To test the functionality of the half-bridge, SiC power module, firstly, a static characterization is performed using the Agilent B1505A curve tracer. The modules are hooked up with the power applied to the main terminals and the sensing functionality attached to the flexible gate, kelvin source, and drain connections (Figure 4-1-Figure 4-2). Static characterization provides information about whether the devices are functioning properly and helps determine operating constraints.

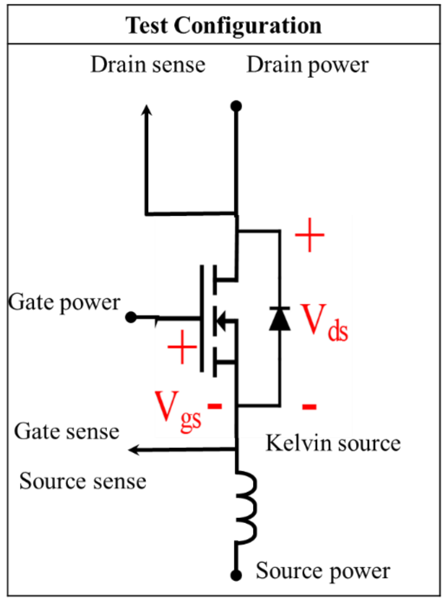


Figure 4-1. Static characterization test configuration using the Agilent B1505A curve tracer

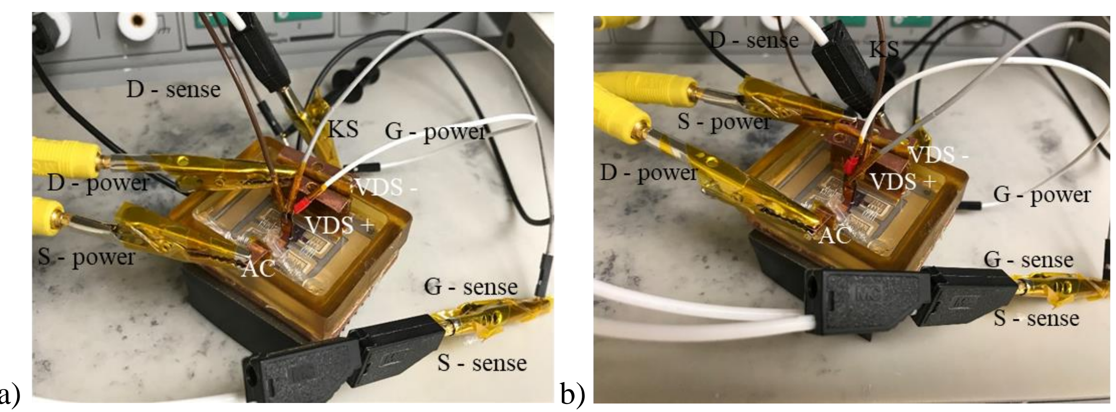


Figure 4-2. Static characterization test set up using the Agilent B1505A curve tracer

4.1.2 Static Results

Four fabricated modules are below 100 µA leakage current up to 600 V and those that are encapsulated in Nusil R-2188 reached 1.5 kV (Figure 4-3). The bottom and top side devices begins conducting current between 2.1 and 2.5 V applied across the gate and source as expected reaching 100 A between 6 and 8 V_{gs} (Figure 4-4). The on-state resistance for top and bottom switch positions is between 5.5 and 7 mΩ which is expected with two 13 mΩ die in parallel (Figure 4-5). Lastly, the output curves demonstrate 60 A conduction at less than 500 mV with the recommended 15 V_{gs} (Figure 4-6).

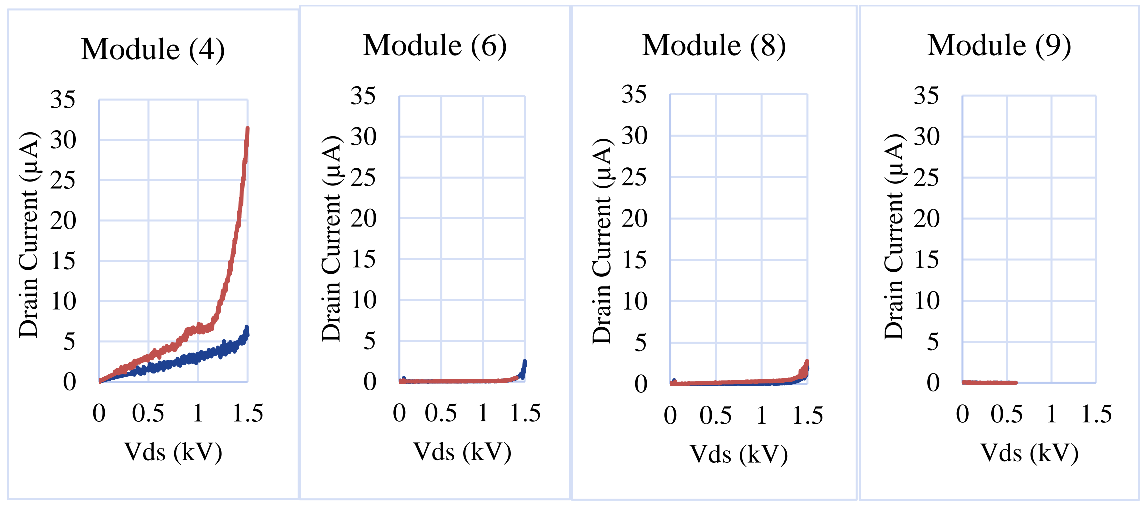


Figure 4-3. Breakdown voltage with threshold of either 1.5 kV or 100 µA leakage current; top switch is red, bottom switch is blue

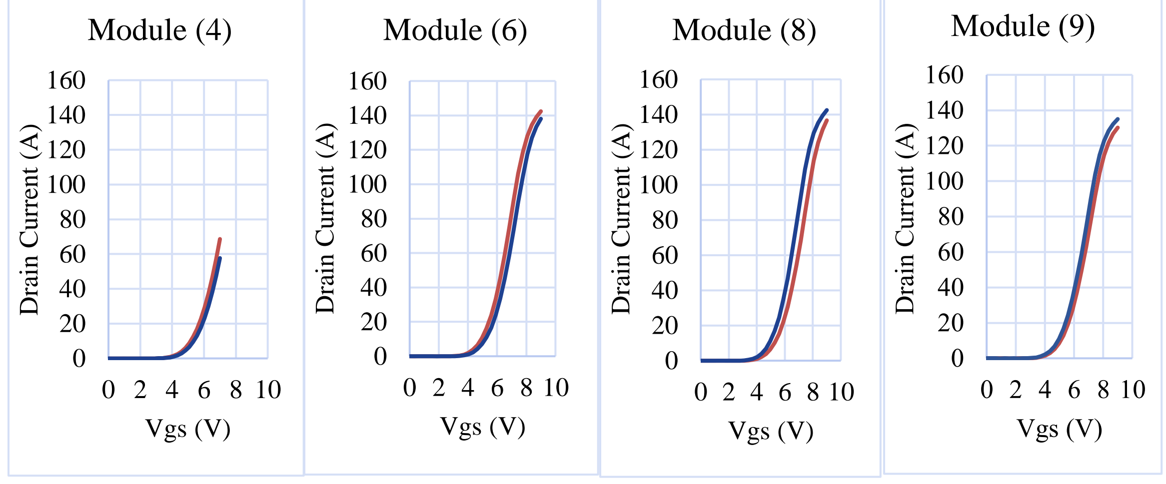


Figure 4-4. Transfer characteristics with 10 V applied across V_{ds}; top switch is red, bottom switch is blue

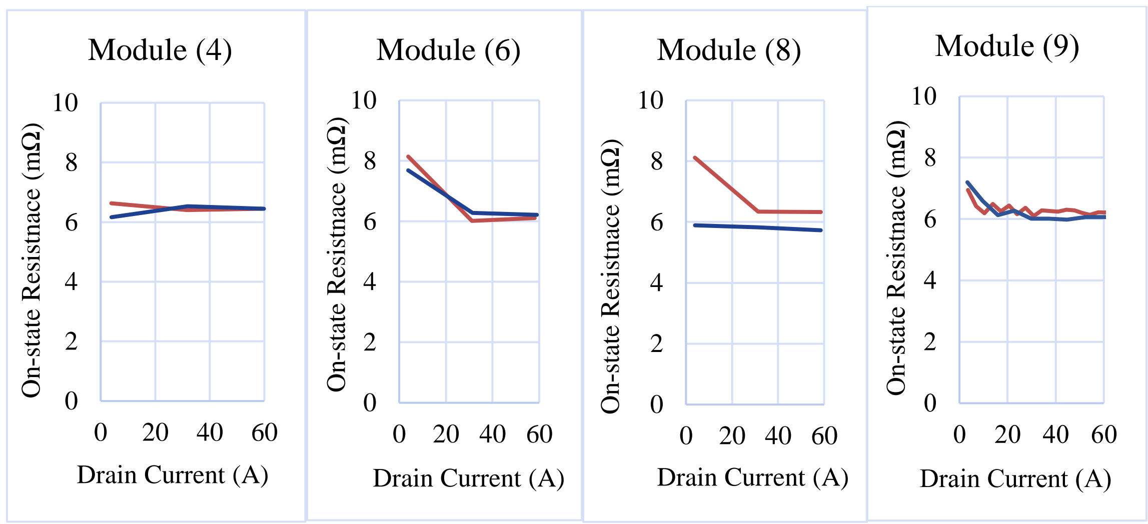


Figure 4-5. On-state resistance with 15 V applied across V_{gs}; top switch is red, bottom switch is blue

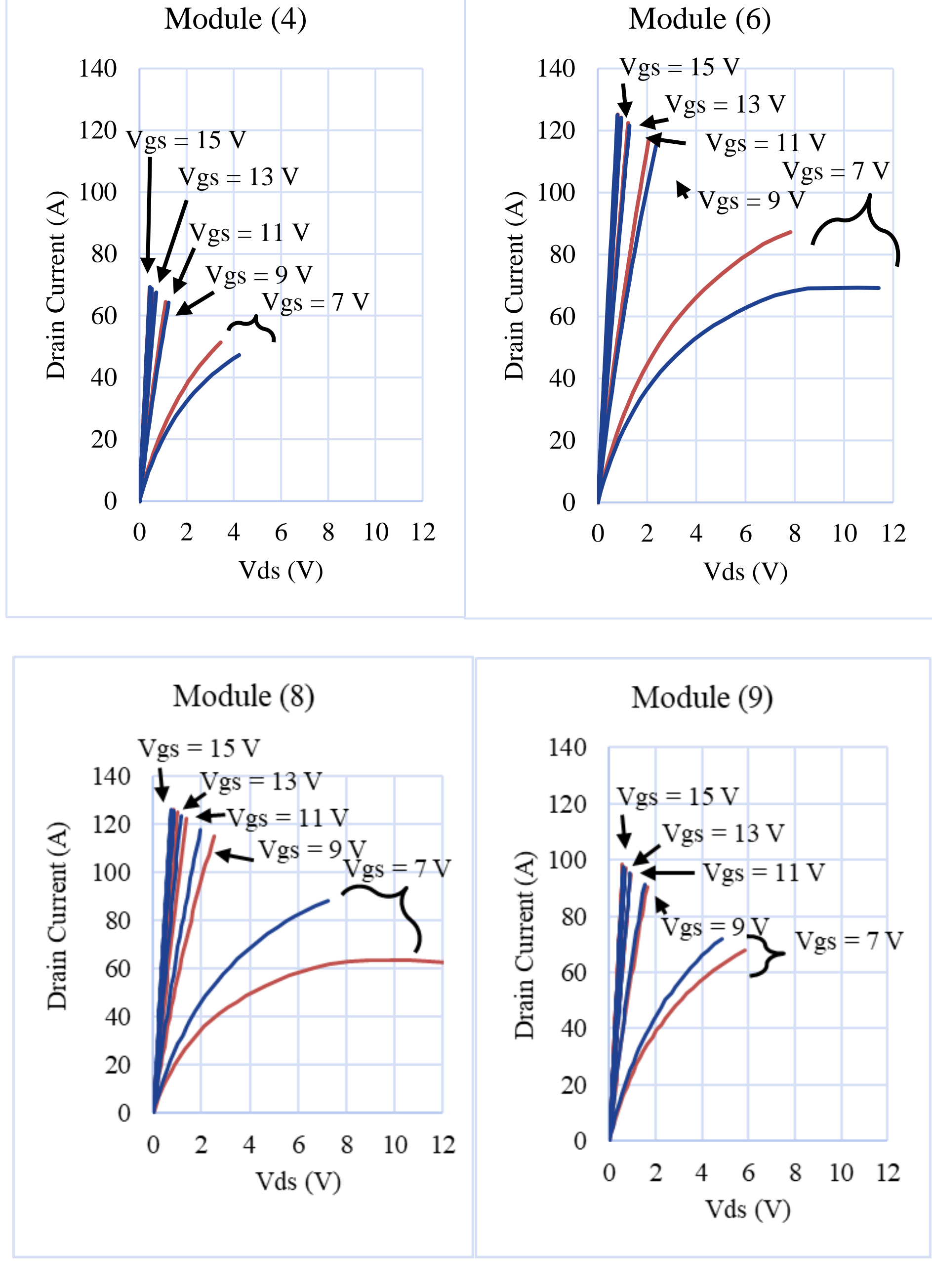


Figure 4-6. Output characteristics with a 7, 9, 11, 13, and 15 V applied to V_{gs}; top switch is red, bottom switch is blue

4.2 *Dynamic Characterization*

4.2.1 Introduction

To characterize the dynamic performance, the power module is tested under different load currents using a clamped inductive load tester (Figure 4-7). If any of the impedance parameters of the pathways are mismatched, current distribution among the dies can be unequal. In this case, the inductance for both current pathways are the same because they share the load inductance. In addition, any parasitic inductance introduced by the module will be similar due to symmetrical DBC design. Therefore, the current should increase at a similar rate due to inductance. Often, static current sharing is dominated by the on-state resistance of the dies; because the on-state resistance of the modules could not be controlled, there may be unpredictable differences in static, on-state current rise.

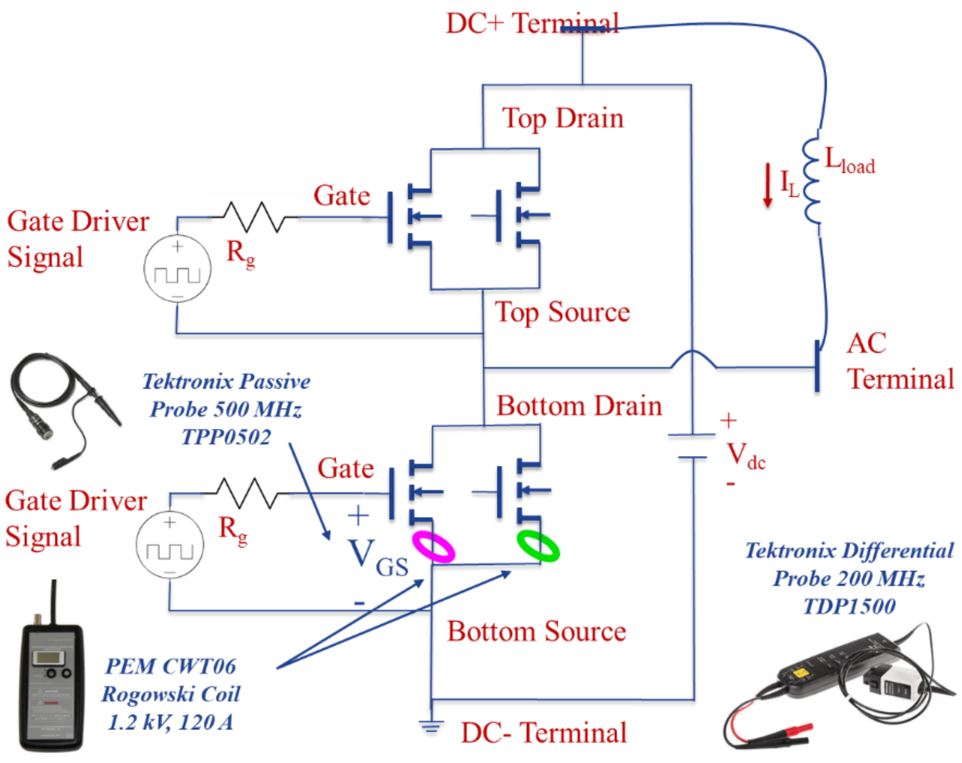


Figure 4-7. Double pulse test setup with die current monitoring

The individual die currents in the bottom switch (position C and D from Figure 2-2) for the module are monitored. These currents are measured using Rogowski coils which are looped around the wire bonds of the bottom die (Figure 4-8); the wire bonds have been attached with high loops to fit the coil (Figure 3-16). With this data, the effectiveness of the symmetrical DBC patterning and die selection can be evaluated for balancing the shared current. Therefore, the gate driver PCB must be configured in a way that allows for effective and safe use of the delicate Rogowski coil loops.

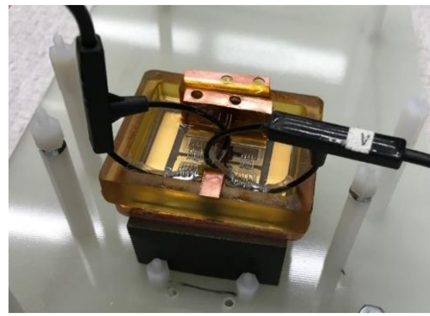


Figure 4-8. Rogowski coil interface with module

4.2.2 Gate Driver Design

The gate driver PCB has dual gate driver functionality so that the top devices and bottom devices can be switched independently (Figure 4-9). It is designed with vias that attach to the gate, kelvin source, and drain pins coming out of the flexible PCB (Figure 4-10). The thin design of the gate driver provides space for the placement of the Rogowski coils measuring individual die currents; the gate driver board sits above the pins of the flexible PCB but does not sit entirely above the wire bonds of the bottom switches (Figure 4-9).

Figure 4-9. Gate driver with top and bottom switch circuitry designed to be thin for the placement of the Rogowski coils

Figure 4-10. Pins of the flexible PCB interface with vias on the board

The gate drive layout for the bottom switch and simplified schematic are shown in Figure 4-11-Figure 4-12. The isolated ISO5851 gate driver IC is selected for benefits such as desaturation protection and low propagation delay, which are crucial for SiC MOSFET applications. The source current is only 2.5 A which could be insufficient with a driving voltage of 15 V and an approximate 2.95 Ω minimum per die. Therefore, a ZXGD3006 current booster stage is utilized to achieve 10 A max driving current. The driving circuit sits close to the gate and source to minimize inductance in the control loop [78]. Lastly, the MGJ2D241505SC power supply chip provides -5/+15 V for driving the gate and is selected for its low capacitance.

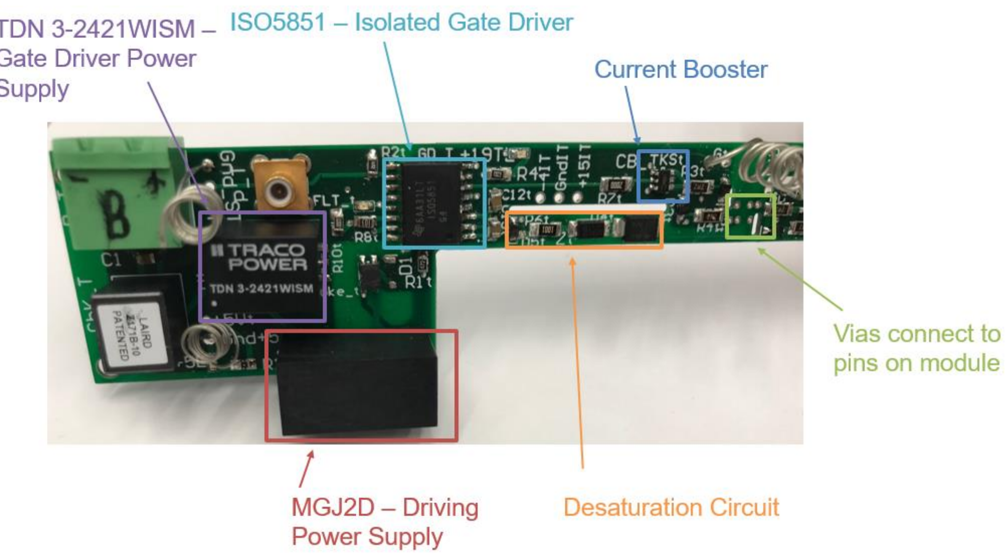


Figure 4-11. Gate driver board layout

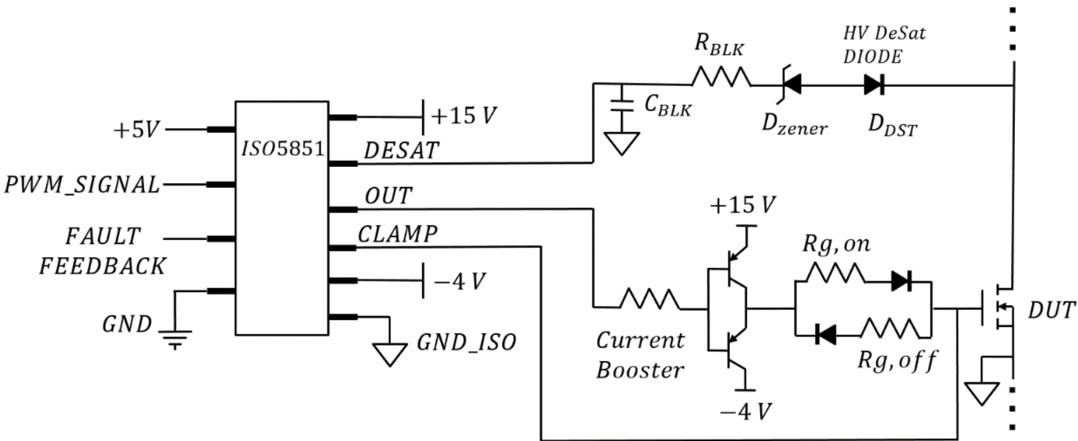


Figure 4-12. Simplified schematic of the driving circuit

4.2.3 Desaturation Circuit for Overcurrent Protection

Excessive current during a short-circuit event could damage the switch so overcurrent protection is required. One method is commonly referred to as desaturation protection in which the on-state voltage is monitored [79-82]. The protection circuit shuts off the device once a set on-state voltage is reached, which is often referred to as a “threshold” or “desaturation” voltage, $V_{ds_{threshold}}$. The threshold voltage is often set according to 2x the high temperature output characteristics of the device. For example, if the device is rated for 120 A, the on-state voltage at 2x120 A, 240 A, based on the high temperature output curve could serve as the threshold voltage.

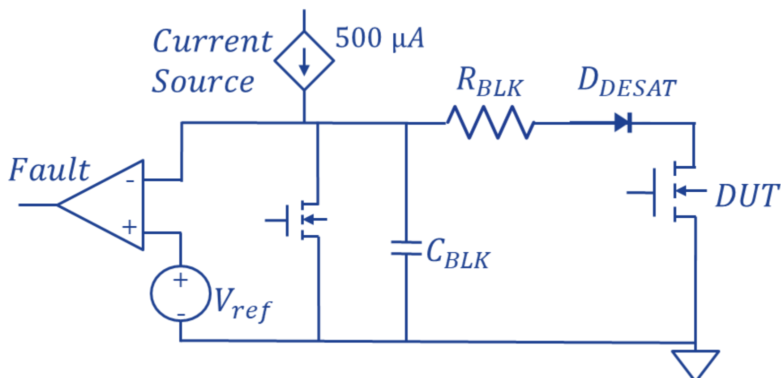


Figure 4-13. Example schematic of a desaturation circuit

Often, the protection circuit includes a reference voltage, and a comparator. A current source is attached to the top rail of the comparator which produces a current in the mA or μA range. The current source, reference voltage, and comparator are either determined by the user or are part of the internal circuitry of an integrated gate driver chip. The rest of the circuit includes either a diode sense circuitry or resistors [81]. In the case of the diode sense circuitry, a high voltage diode is in series with the device under test (DUT) which are in parallel with the comparator. The comparator compares the reference voltage, V_{ref}, which will be referred to as the "desaturation voltage," against the combined value of the forward voltage of the diode, $V_{D_{fwd}}$, in series with the DUT on-state voltage, V_{ds}. Lastly, a blanking resistor is in series with the high-voltage diode which can be used to control and limit the reverse recovery current.

During normal OFF operation, the voltage across the DUT is high and no significant current is flowing. The diode will block the voltage across the drain and source of the DUT during OFF operation (Figure 4-14). During normal ON operation, high current passes through the DUT and the on-state voltage is less than 4 V, $V_{ds_{on}}$ (33). The total voltage of the diode and the DUT is less than the desaturation threshold voltage and the diode is turned on (34). Therefore, the desaturation

current created by the current source will flow in the forward direction through the diode and the DUT without tripping the comparator (Figure 4-14).

$$V_{ds_{threshold}} > V_{ds_{on}} \qquad (33)$$

$$V_{ref} > V_{ds_{on}} + V_{D_{fwd}} + V_{R_{BLK}} \qquad (34)$$

Figure 4-14. Desaturation circuit behavior during device ON and OFF states

During switching, Vds is either rising to or falling from its value in the 100s of volts (Figure 4-15). This changing voltage, dv/dt, interacts with the capacitance of the high voltage diode, causing a small reverse recovery current (35). This current can be minimized with a low capacitance diode. The time the reverse current flows can be minimized with a fast reverse recovery response [80, 82]. During switching events, current flows backwards through the diode and the desaturation circuit can sense the high voltage of the switching DUT. Without a delay, the system would trigger the device to turn off due to safe, switching operation.

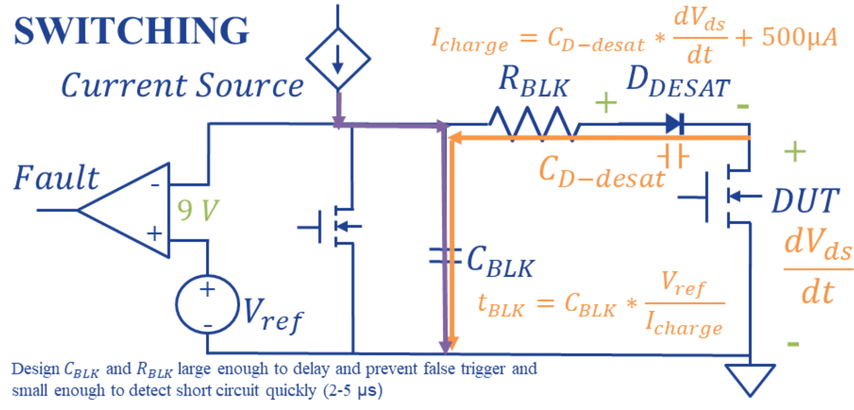


Figure 4-15. Desaturation circuit behavior during device switching

Therefore, a blanking capacitor is placed in parallel with the DUT which charges from the current provided by the current source, I_{chip} (either internal to the chip or external and selected by the user), as well as the diode's reverse recovery current, $I_{reverse}$,which together are defined as I_{charge} (36). The time it takes for the blanking capacitor to charge creates a delay as the DUT switches (37), once the DUT is off, the diode will be blocking or if the device turns on, the desaturation circuit will see a safe, low, on-state voltage.

$$I_{reverse} = C_{D-desat} * \frac{dV_{ds}}{dt} \quad (35)$$

$$I_{charge} = C_{D-desat} * \frac{dV_{ds}}{dt} + I_{chip} \quad (36)$$

$$t_{BLK} = C_{BLK} * \frac{V_{ref}}{I_{charge}} \quad (37)$$

However, during a short circuit event, the current increases drastically and the on-state voltage jumps above the normal operating value and the threshold voltage (38). The blanking capacitor will begin to charge and since the combined voltage of the diode and DUT is greater than the reference voltage (39), the device is turned off (Figure 4-16).

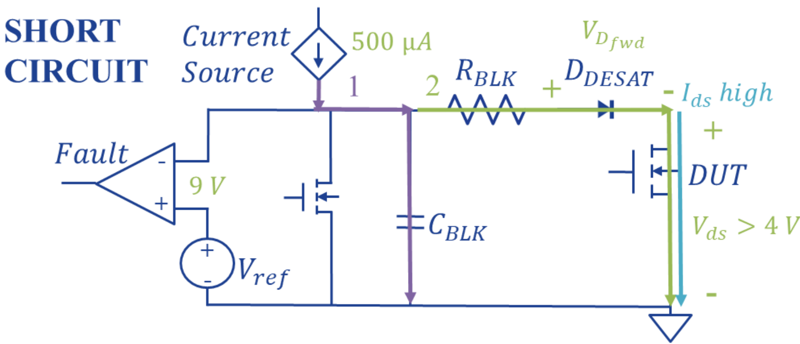


Figure 4-16. Desaturation circuit behavior during a short circuit event

$$V_{ds_{threshold}} < V_{ds_{on}} \tag{38}$$

$$V_{ref} < V_{ds_{on}} + V_{D_{fwd}} + V_{R_{BLK}} \tag{39}$$

4.2.4 Tuning the Desaturation Circuit

For this gate driver, the external desaturation (DeSat) protection circuit consists of a blanking capacitor, a blanking resistor, a Zener diode, and a high voltage blocking diode. A resistor and low-valued capacitor are used to fine tune the protection voltage level according to the operation and the DeSat protection blanking time, which has to be approximately less than 4 µs for many SiC devices [79-82]. Often, the desaturation threshold voltage is set based on the on-state drain-source voltage at elevated temperature, found using the output characteristics, for a peak turn-on current assumed to be about 2X the rated current. The desaturation circuit after tuning is presented in Figure 4-17 with a STTH212 high-voltage diode.

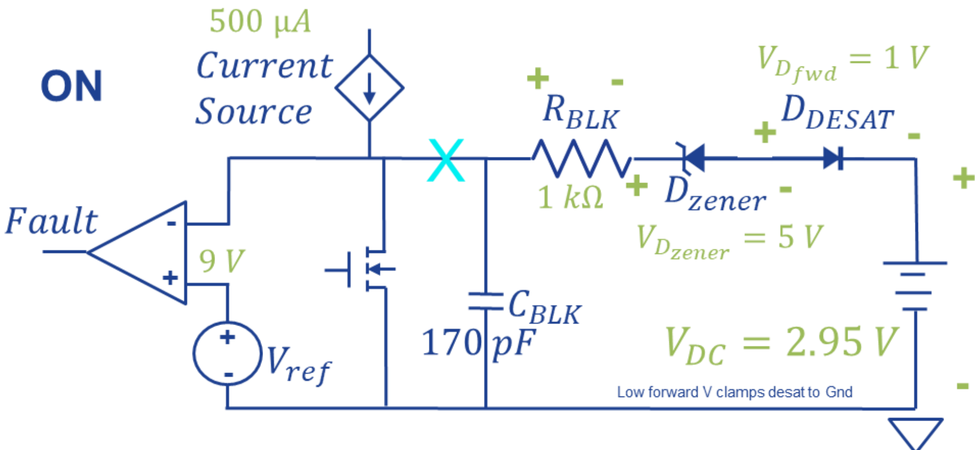


Figure 4-17. Desaturation circuit for this gate driver after tuning

The response time is tuned with the blanking resistor and capacitor because the resistor can impact the reverse recovery current and the capacitor is positively proportional to the time it will take to charge. Using a 150 pF capacitor and a 1 kΩ resistor, the blanking time was 1.9 µs (Figure

4-18). This was later considered a little too fast, so a larger capacitor is used to increase the charging time and smaller resistor was used to reduce the reverse recovery current.

$$t_{BLK} = 150\ pF * \frac{9\ V}{500\mu A + 110\mu A} = 1.9\ \mu s \qquad (37)$$

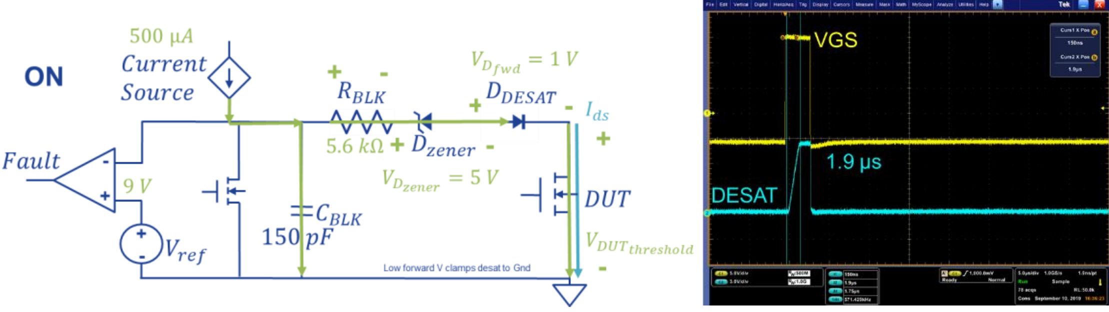


Figure 4-18. Tuning desaturation response time with blanking capacitor

To achieve the set threshold voltage, the voltage of the diode and resistance is subtracted from the reference voltage (40). In this case, the reference was 9 V and the diode voltages were approximately 6 V, so the threshold voltage would be 3 V.

$$V_{ds_{threshold}} = V_{ref} - V_{D_{fwd}} - V_{D_{zener}} - V_{R_{BLK}} \qquad (40)$$

Experimentally, the diode voltages were 5.31V and the threshold voltage was 2.95 V (the reference voltage was 8.21 V experimentally). The diode voltage was confirmed by measuring the voltage before the blanking resistor to ground after creating a short in place of the DUT (Figure 4-19).

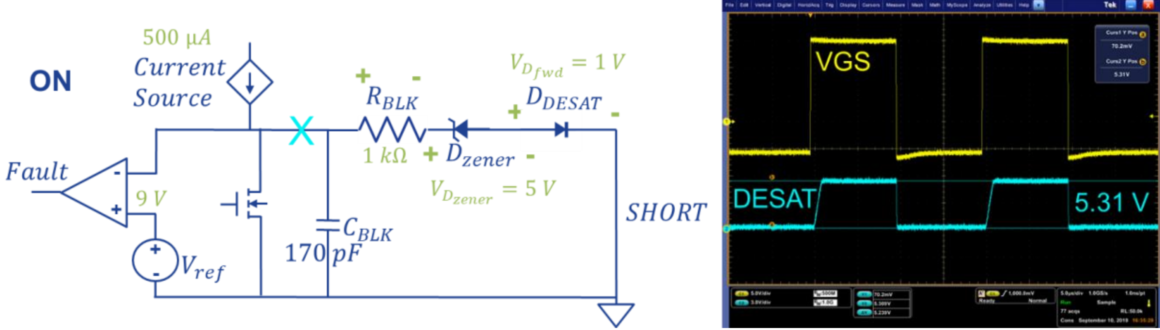


Figure 4-19. Tuning the diode voltages and desaturation threshold voltage

The experimental threshold voltage and reference voltage were determined with a voltage source in place of the DUT; the voltage was slowly raised to imitate on-state voltage until the desaturation circuit tripped (Figure 4-19-Figure 4-20). The value of the threshold voltage was tuned by increasing the value of the Zener diode and resistor. It is important to note that the Zener diode should be checked for its rated current to ensure that the voltage is large enough. The Zener diode that was initially selected had a 3.6 V rating but only in the mA range, so it did not contribute significantly in reducing the threshold voltage. According to the chosen parameters of protection and device output characteristics, the device will turn off at 210 A (2.95 V) at 25°C and 120 A (2.95 V) at 175°C (Figure 4-21).

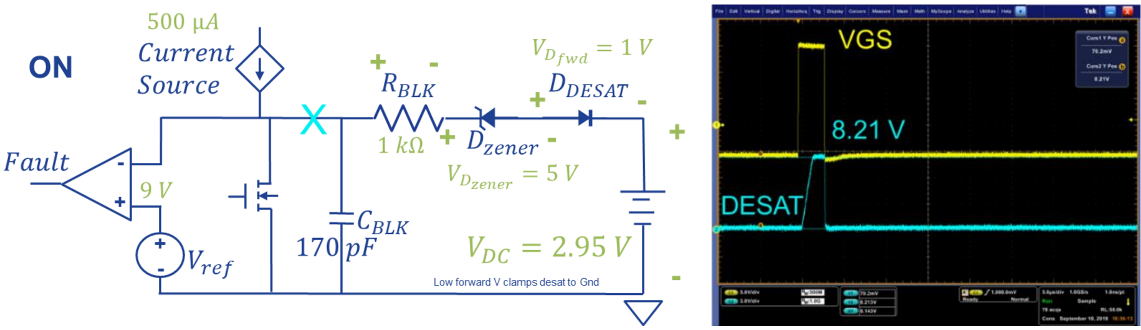


Figure 4-20. Validating desaturation threshold voltage

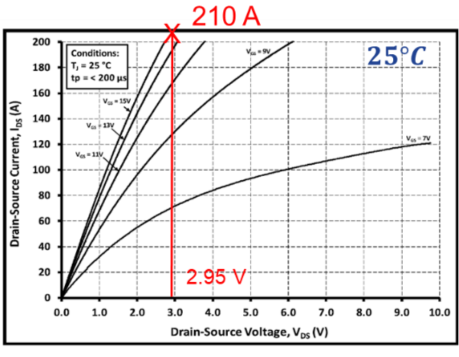


Figure 2. Output Characteristics T_J = 25 °C

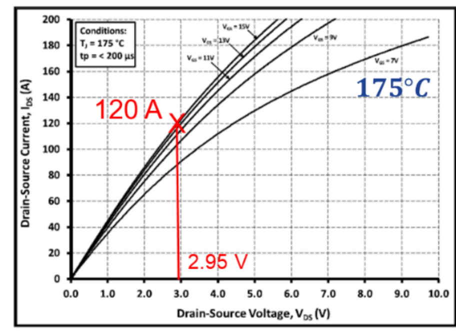


Figure 3. Output Characteristics T_J = 175 °C

Figure 4-21. Approximate current for the desaturation threshold voltage based on the output curves for the dies[83]

(a) Aside: setting the LED resistances

In normal operation, the fault pin is pulled high to the control side VCC. During a short circuit, the fault output will go low. A red indicator LED is placed in parallel with the pull-up resistor so that when the fault goes low, the light will turn on. The LED requires 20 mA to turn and thus, the resistance before the LED needs to be less than 250 Ω.

$$\mathrm{I} = 20\ \mathrm{mA} < \frac{\mathrm{V}}{\mathrm{R}}$$

$$\mathrm{R} < \frac{\mathrm{V}}{\mathrm{I}} = \frac{5\ \mathrm{V}}{20\ \mathrm{mA}} = 250\Omega$$

4.2.5 Capacitor Bank

The capacitor bank PCB connects to a 600 V-800 V power supply. The DC terminals on the module connect to the board with screws (Figure 4-22). The load inductor attaches to a screw on the board and the AC terminal of the power module. The complete test setup is shown in Figure 4-23-Figure 4-24.

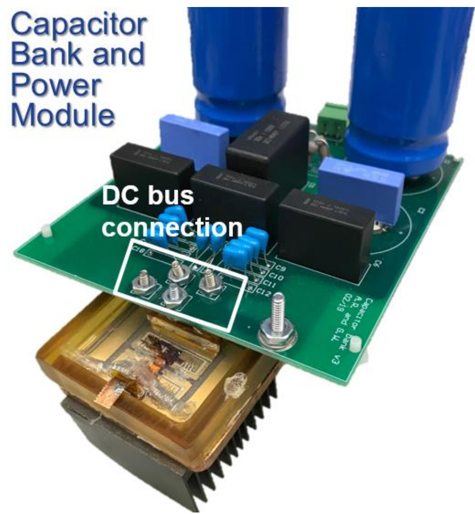


Figure 4-22. Power module screws into capacitor bank board with screw for load inductor connection

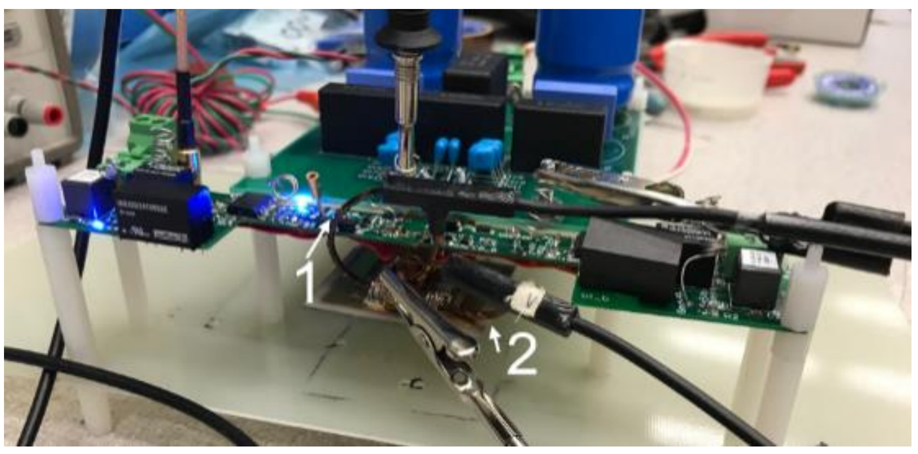


Figure 4-23. Test set up with Rogowski coils through the wire bonds of the bottom side die of a partially fabricated module

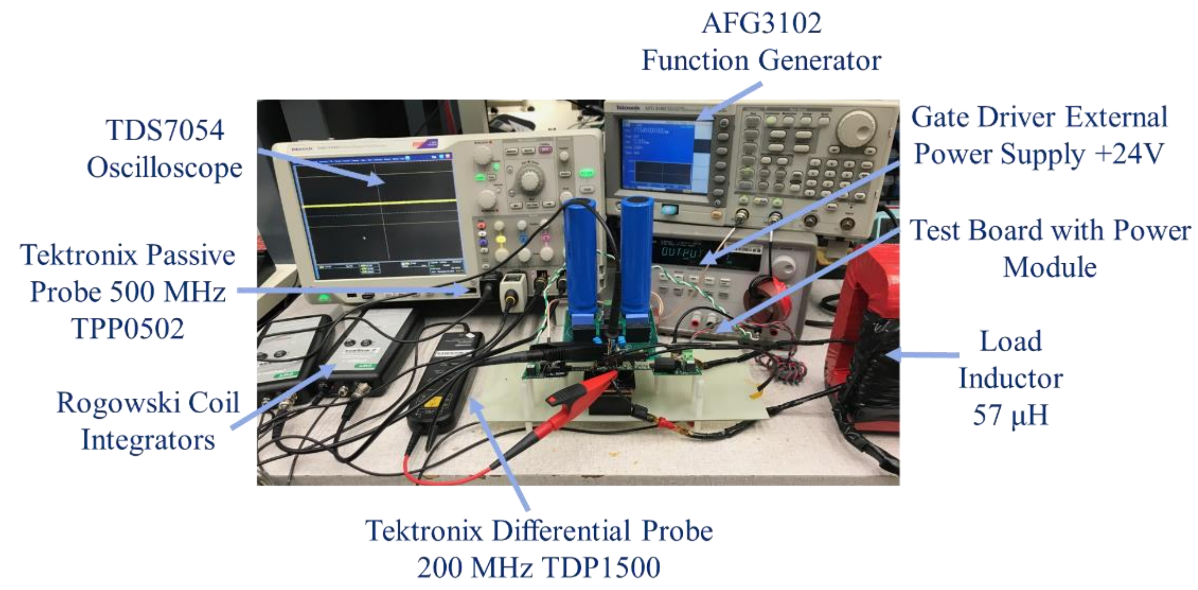


Figure 4-24. Test set up for dynamic characterization of module

4.2.6 Low Voltage Switching Test Results

Initial clamped inductive double pulse tests (DPT) are conducted with low DC bus voltage and a -5 V to 14 V driving signal. Results confirm that the both dies are successfully able to switch and conduct current. Static current sharing is dependent on the pathway impedances composed of inductance and on-state resistance.

In the results, static, on-state, current sharing is nearly equivalent (Figure 4-25). With time, slight mismatch of current through devices can be observed. This minimal and tolerable difference is a result of the mismatched current pathway impedances, which could be caused by either slight difference in inductances or on-state resistance of dies.

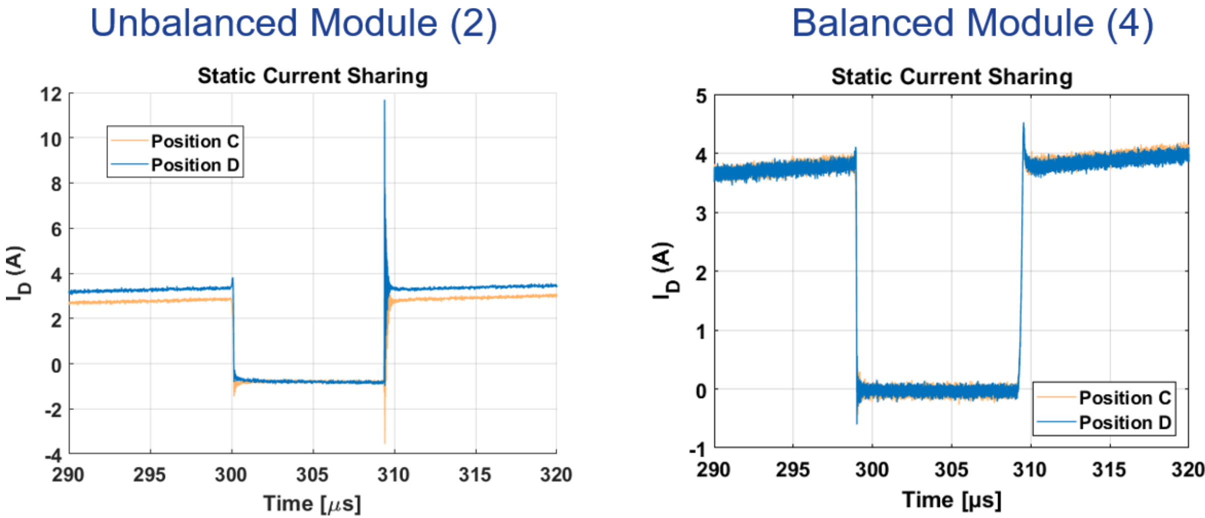


Figure 4-25. Static current sharing for unbalanced and balanced modules

Dynamic switching results are shown in Figure 4-26-Figure 4-27. During switching, the paralleled die should turn on at the same time due to similarity in their threshold voltages. Furthermore, when the pathways have similar inductance due to a symmetrical designed DBC, the current should increase at the same rate and experience the same overshoot. This ultimately means that neither die is experiencing more current stress than the other, which leads to improved reliability and prevents catastrophic failures due to die overstress.

During turn-on, the dies behave as expected, turning on at the same time, increasing at similar rates, and overshooting to the same peak value for the balanced module. During turn-off, however, the die in Position C begins to turn off before the die in Position D. This droop in current is may be attributed to the gate driving circuitry with a problem in the flexible PCB or may also be a measurement error. The fall rate and undershoot of the 2 die are similar suggesting sufficiently matched inductances. Therefore, the static current difference is most likely caused the on-state resistance difference.

Low voltage switching tests using the Rogowski coils confirm that current sharing between the dies is satisfactory for the module and test design, especially during turn-on. Furthermore, the balanced and unbalanced modules behave differently as expected with balanced and unbalanced current sharing due to the matched and mismatched threshold voltages. High-voltage tests are necessary to determine if the parasitic inductances are similar enough or if there is still enough difference to cause significantly different rise in current. High-voltage tests may also reveal or dispel problematic mismatches in overshoots.

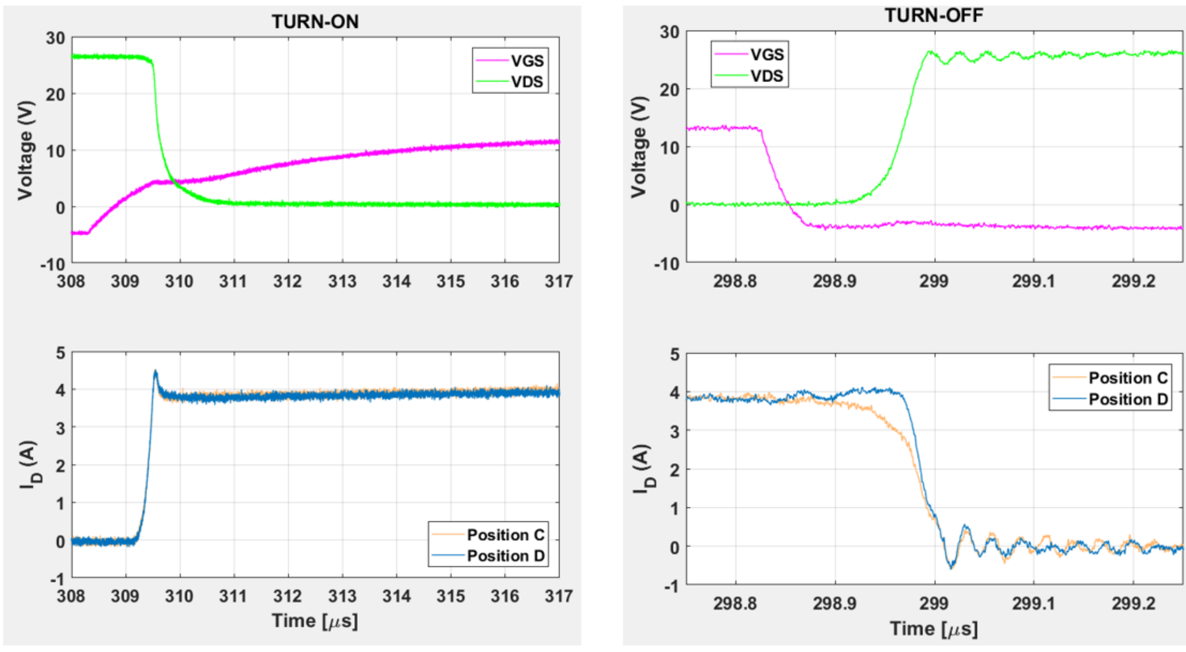


Figure 4-26. Balanced module (4) turn on and turn off behavior

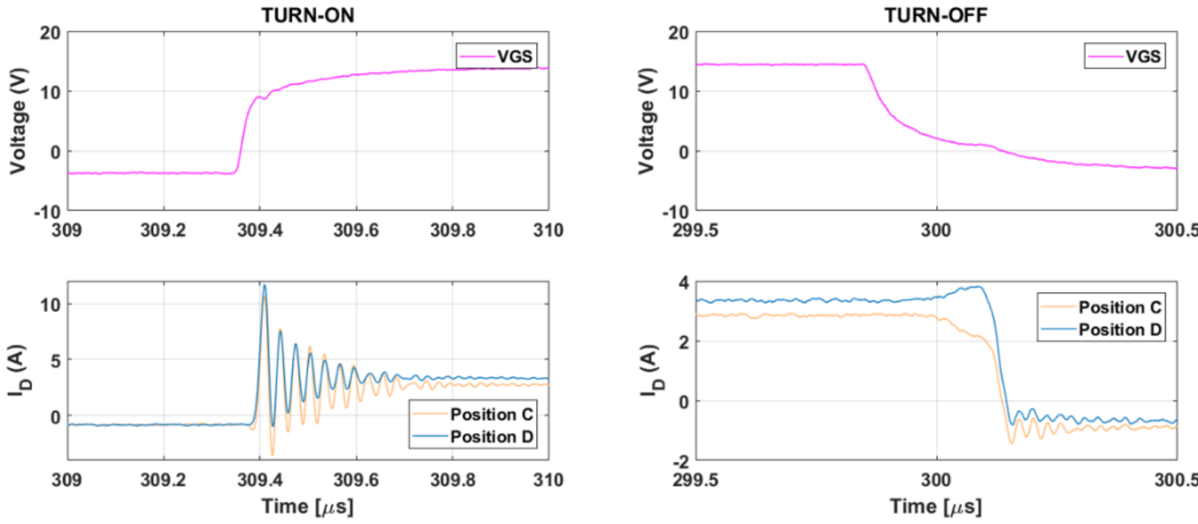


Figure 4-27. Unbalanced module (2) turn on and turn off behavior

4.2.7 600 V Switching Test Results

The modules are then tested up to 600 V (Figure 4-28-Figure 4-29). Some modules handled up to 120 A total, 60 A per die, but 100 A was sufficient as continuous tests most likely would not exceed 100 A, 50 A per die.

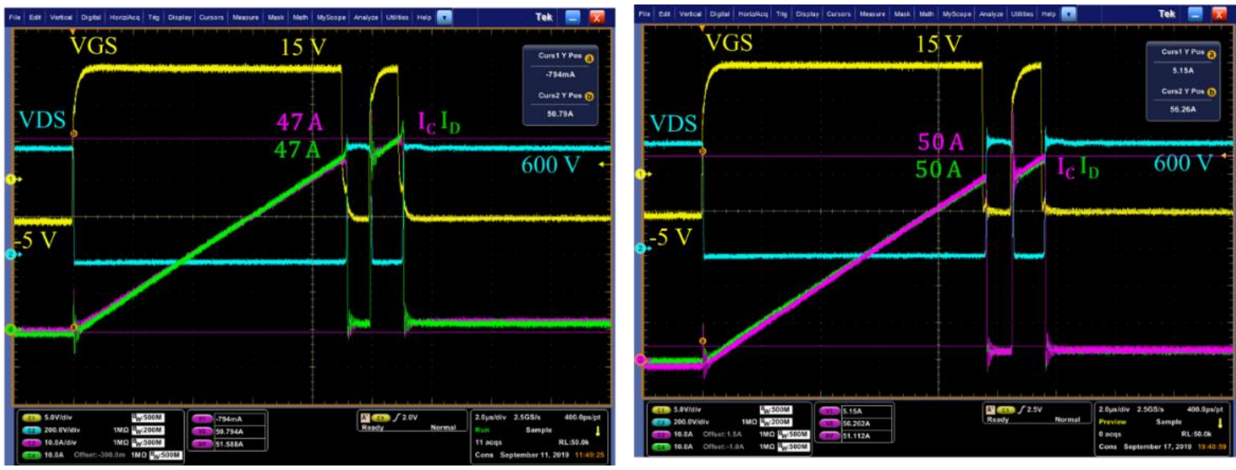


Figure 4-28. 600 V DPT results for balanced modules 4 and 6

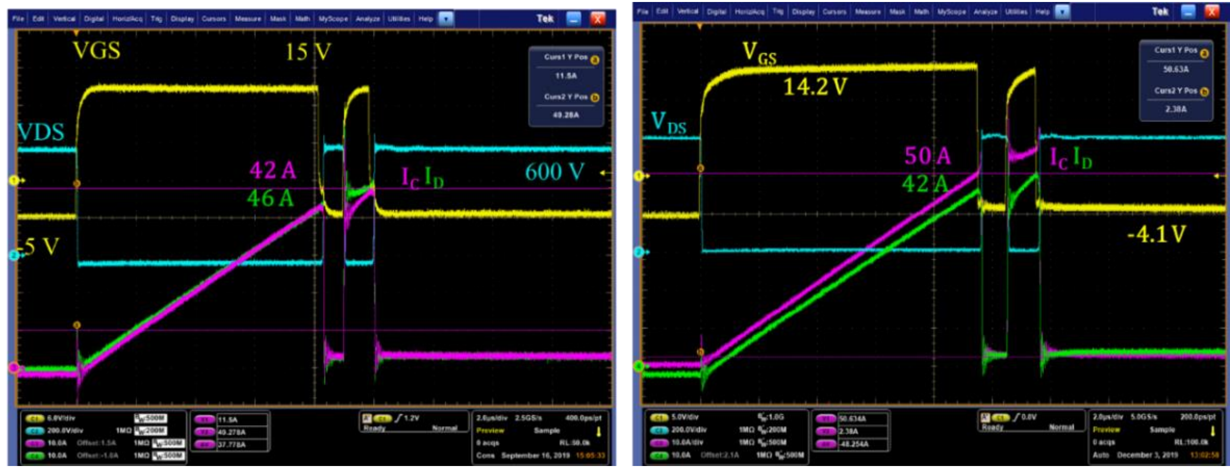


Figure 4-29. 600 V DPT results for unbalanced modules 8 and 9

The turn-on results for the balanced modules demonstrate expected dynamic sharing in both the peak current (0% difference for module 4 and 2.32% difference for module 6) and ringing of the paralleled dies (Figure 4-30-Table 5). Percent difference is calculated as the value of D subtracted from the value of C and divided by the average of the 2 values.

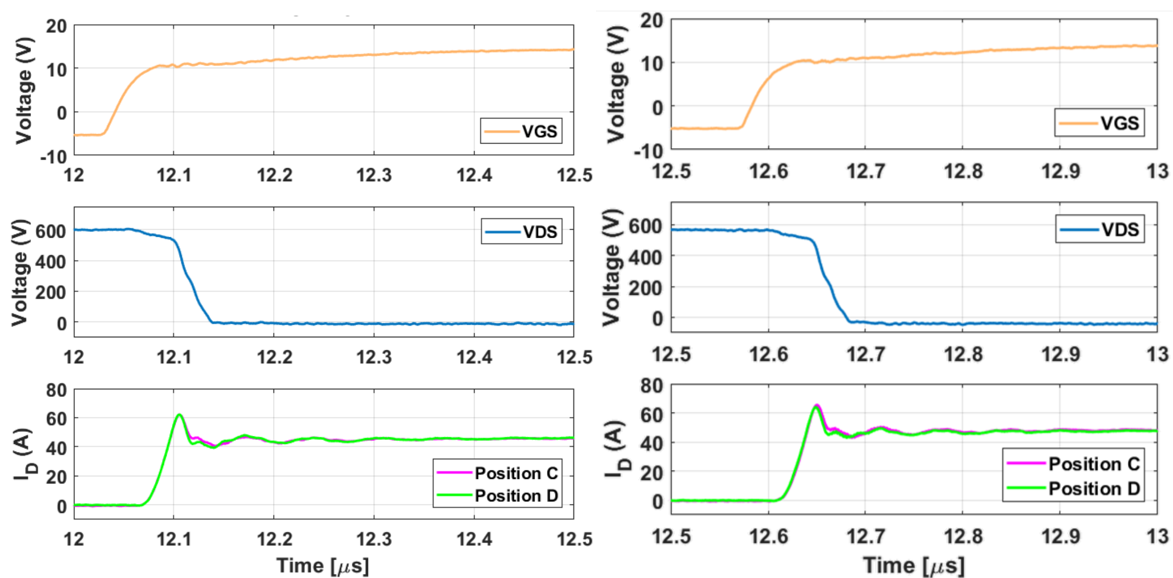


Figure 4-30. 600 V DPT turn-on results for balanced modules 4 and 6

The turn-off results for the balanced module 6 demonstrate expected dynamic sharing in both the peak current (-3.77%) and ringing of the paralleled dies (Figure 4-31-Table 6). However, in module 4, the current in die C began to drop before D so that the peak current and di/dt were significantly different. In order to theorize on the reason for this behavior, a simulation was made for unbalanced parasitic inductances, gate resistances, and capacitances in the paralleled bottom dies (Figure 4-34-Figure 4-37). The unbalanced gate resistance simulation most closely resembled the turn-off behavior of module 4 although this should then be apparent in the turn-on speed which is not the case (Figure 4-34). Because the impact of a potentially higher gate resistance in die D was not apparent during turn-on, this is likely not the case. However, if this was the source of the behavior, the fabrication method for attaching the flexible PCB may have added additional gate resistance to one die over the other.

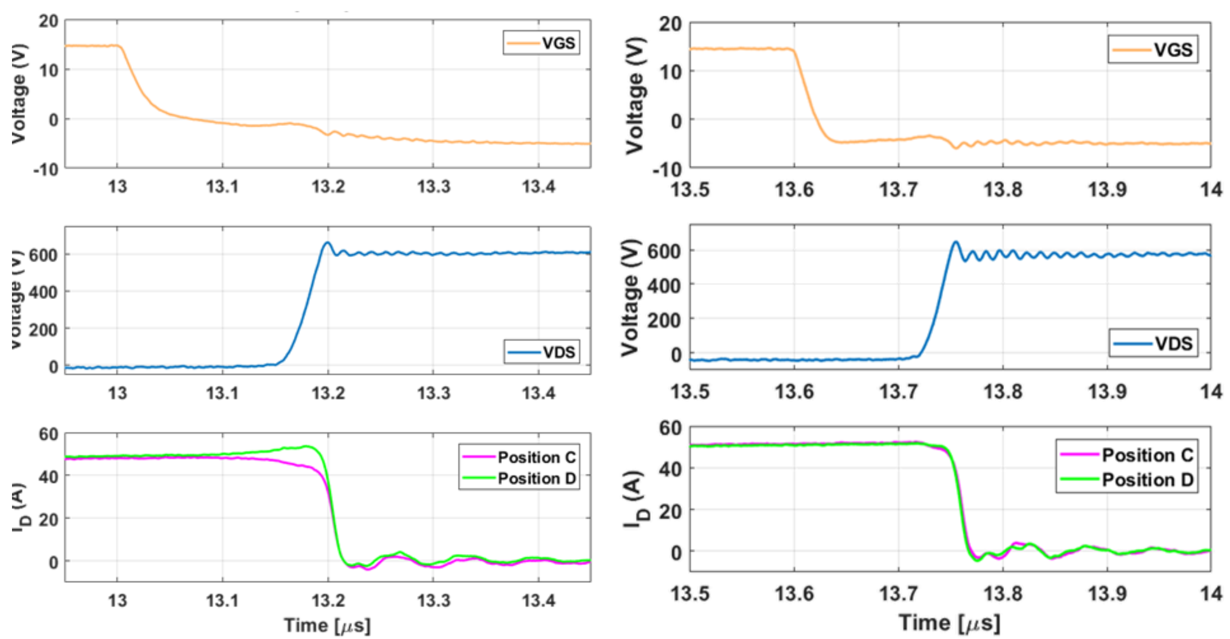


Figure 4-31. 600 V DPT turn-off results for balanced modules 4 and 6

The peak current during turn-on for the unbalanced modules is significantly different with 13.3% and 22.0% difference for modules 8 and 9, respectively (Figure 4-29-Table 5). The ringing for the unbalanced modules is similar, suggesting a balanced parasitic inductance in the current pathway.

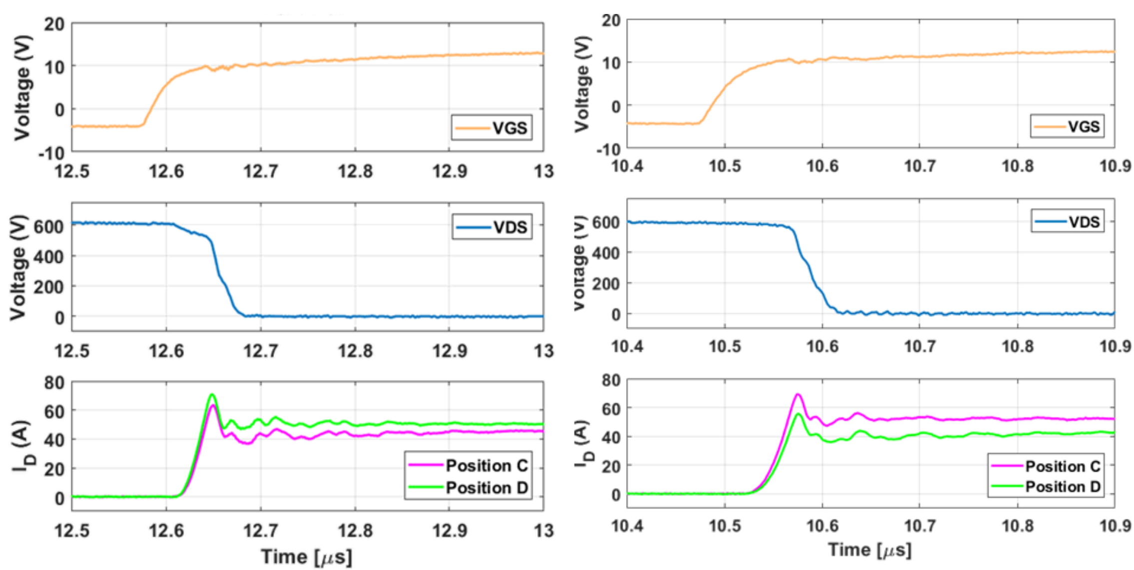


Figure 4-32. 600 V DPT turn-on results for unbalanced modules 8 and 9

In module 8, the peak current during turn-off is insignificantly different (-2.84%) and the di/dt was the least different of all modules (-10.2%) (Figure 4-33-Table 6). The peak current and di/dt for module 9 differs significantly between dies (17.8% and 22.0%) which may be attributable to both the lower threshold voltage and the lower current in Die D during static sharing.

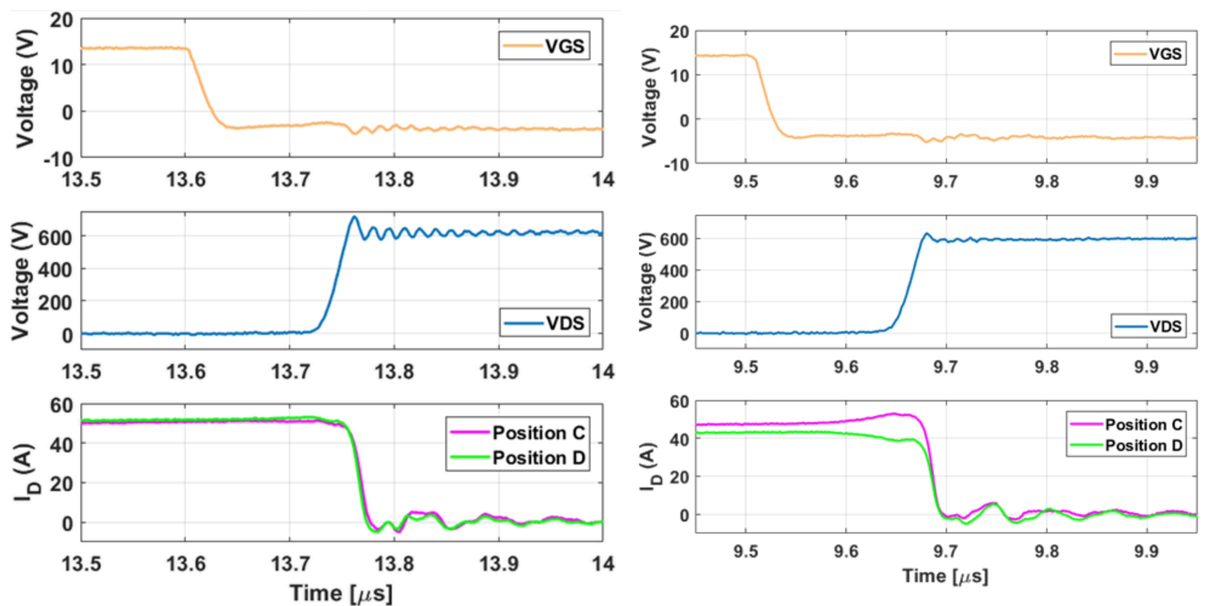


Figure 4-33. 600 V DPT turn-off results for unbalanced modules 8 and 9

Table 5. DPT turn-on result comparisons for Modules 4, 6, 8, and 9 where pink indicates a higher value for die C and grean, negative indicates a higher value for die D for percent difference

$\frac{dV}{dt}$	**14.0 V/ns (34.8 ns)**		**13.64 V/ns (35.6 ns)**		**10.6 V/ns (46.2 ns)**		**13.6 V/ns (35.4 ns)**	
$\frac{dI}{dt}$	1.83 A/ns (19.6 ns) 1.92 A/ns (19.2 ns)	-4.8% diff	1.92 A/ns (20 ns) 1.92 A/ns (20 ns)	0% diff	1.96 A/ns (19.2 ns) 2.17 A/ns (18.4 ns)	-10.2% diff	1.53 A/ns (27.2 ns) 1.28 A/ns (26.4 ns)	17.8% diff
Peak current	62.1 62.1	0% diff	65.4 63.9	2.32% diff	63.4 70.8	13.3% diff	69.2 55.5	22.0% diff

Table 6. DPT turn-off result comparisons for Modules 4, 6, 8, and 9 where pink indicates a higher value for die C and grean, negative indicates a higher value for die D for percent difference

$\frac{dV}{dt}$	16.4 V/ns (30 ns)		20.9 V/ns (23.2 ns)		21.0 V/ns (23.2 ns)		18.6 V/ns (25.8 ns)	
$\frac{dI}{dt}$	1.58 A/ns (24 ns) 2.85 A/ns (13.6 ns)	-57.3% diff	2.43 A/ns (16.8 ns) 2.78 A/ns (14.4 ns)	-13.4% diff	2.53 A/ns (15.8 ns) 2.82 A/ns (14.2 ns)	-10.8% diff	3.03 A/ns (12.4 ns) 1.61 A/ns (21.4 ns)	61.2% diff
Peak current	43.9 53.5	-19.7% diff	48.6 50.0	-3.77% diff	49.4 51.3	-2.84% diff	52.2 39.3	28.2% diff

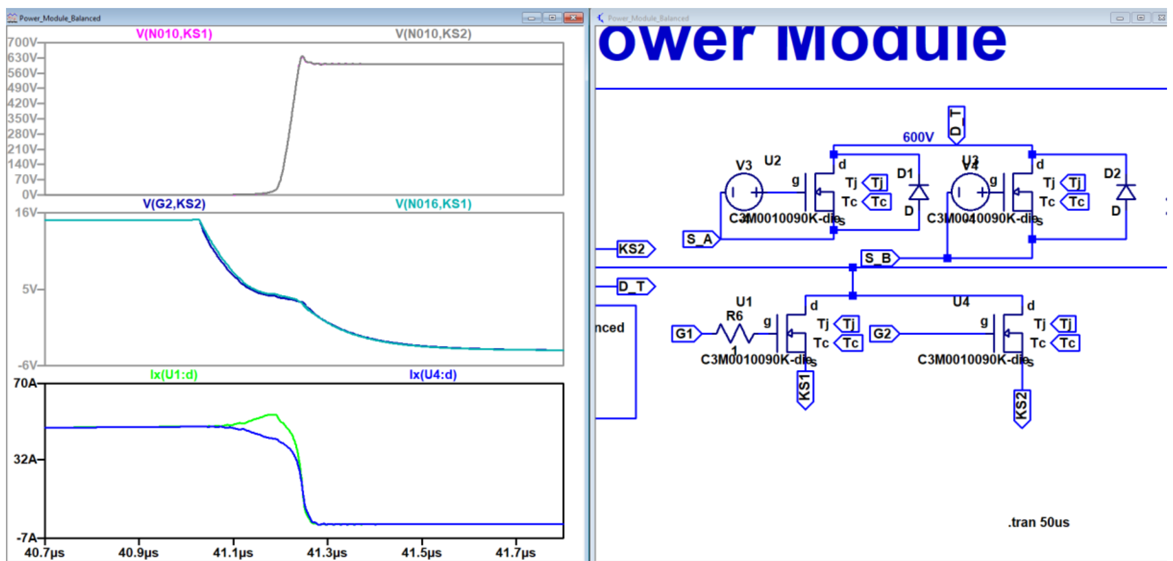


Figure 4-34. Simulation of unbalanced Rg in paralleled dies

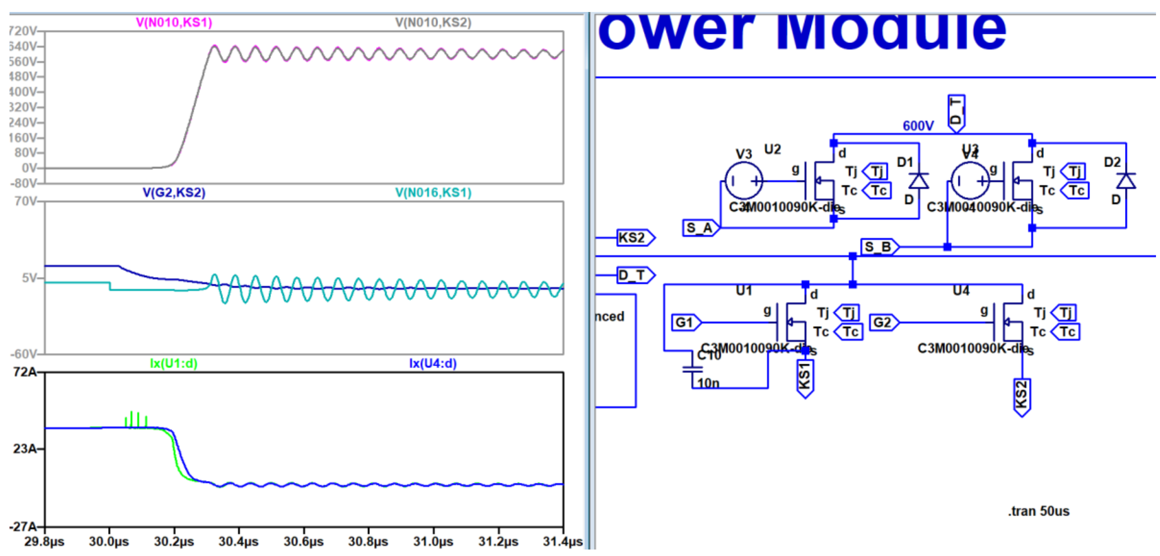


Figure 4-35. Simulation of unbalanced Cds in paralleled dies

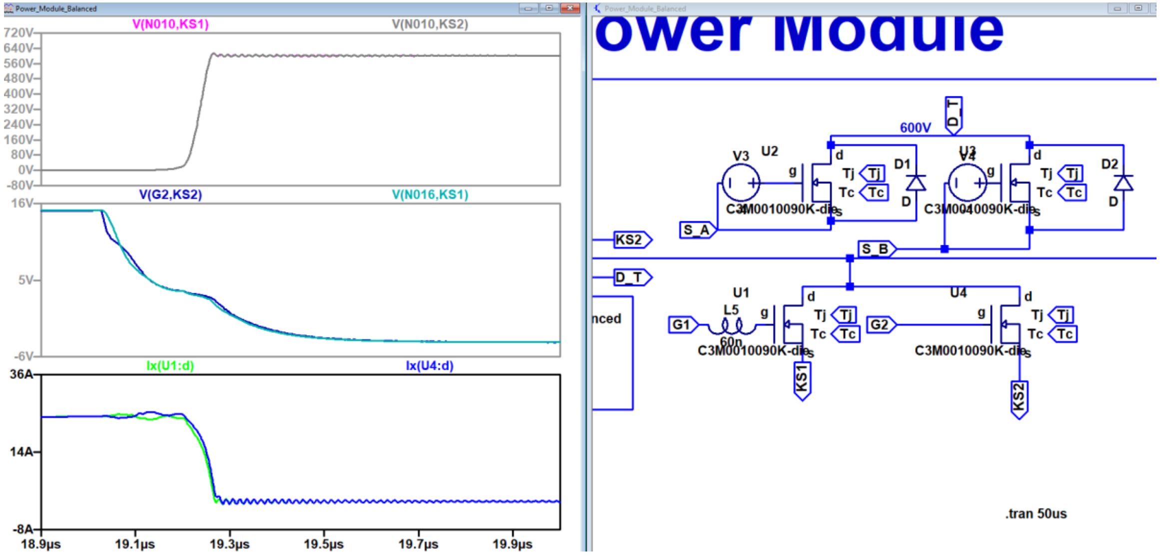


Figure 4-36. Simulation of unbalanced Lgs in paralleled dies

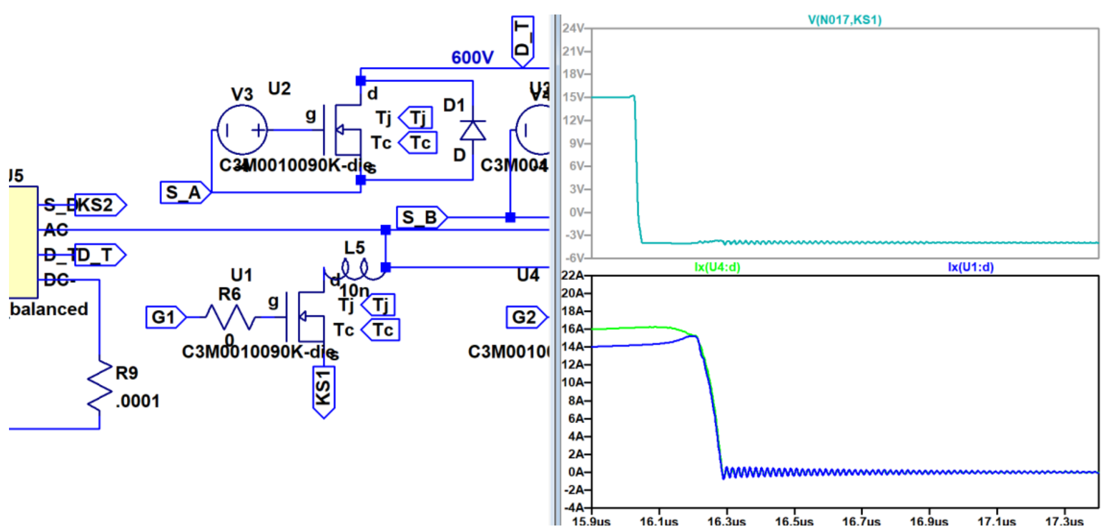


Figure 4-37. Simulation of unbalanced Lds in paralleled dies

In modules 4 and 6, the threshold voltages are balanced with percent difference below 1% (Figure 4-38). The switching energy in balanced module 6 is less than 5% different for turn-on, turn-off, and the total energy which is approximately less than a 10 µJ difference. In balanced module 4, the difference in peak current during turn-off leads to significantly lower energy loss in die D compared to die C (-15.5% or ~100µJ) (Figure 4-38). Percent difference is calculated as the value of D subtracted from the value of C and divided by the average of the 2 values.

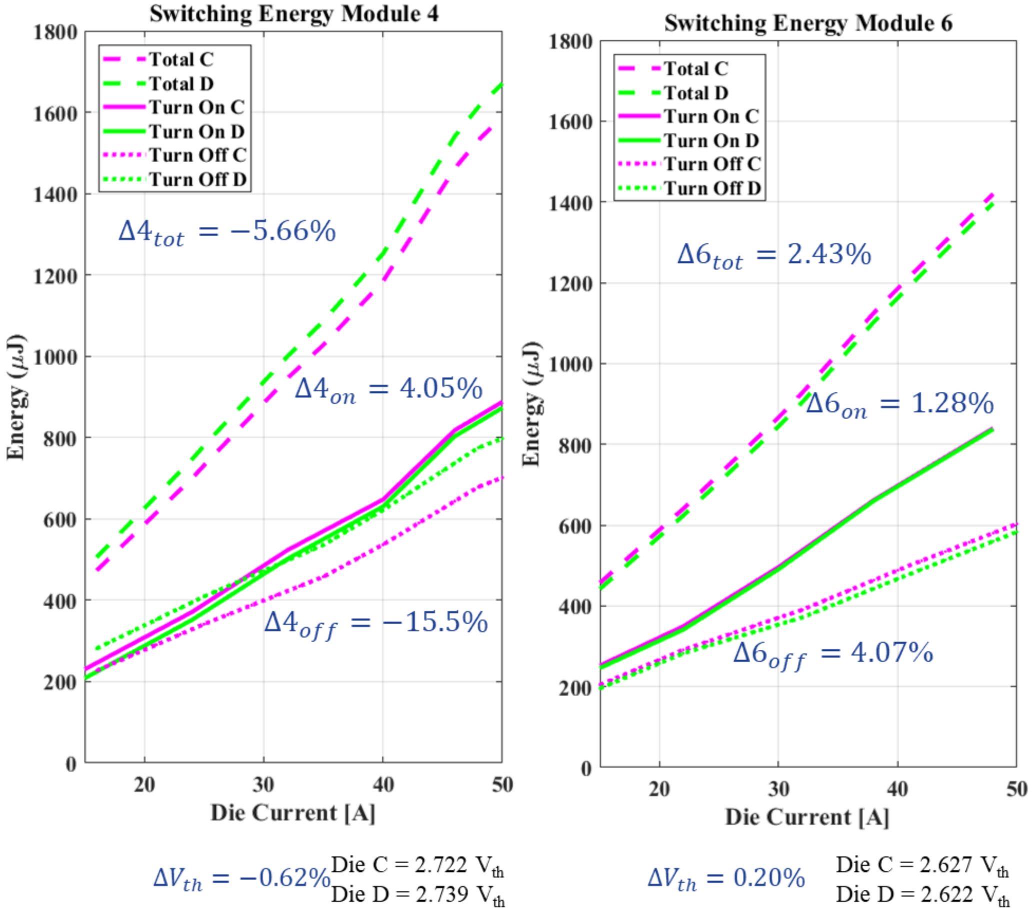


Figure 4-38. 600 V DPT switching energy for balanced modules 4 and 6 with percent differences

In modules 8 and 9, the threshold voltages are unbalanced with over 17.5% difference between the paralleled dies (Figure 4-39). It may be expected to see a significant difference in the energy loss, however, the results for these 2 similarly designed modules varied. In module 8, die D has greater turn-on energy loss (-17.4% or ~100 µJ) due the larger current peak; during turn-off, die C has a slower di/dt and therefore has higher turn-off loss (10.1% or ~50 µJ). The overall energy loss is relatively balanced with -4.52% difference or ~30 µJ. This suggests, that in some cases, if the turn-on and turn-off compensate for one another, the overall loss differential is not significant.

In the case of module 9, both the turn-on and turn-off energy are higher for die C which leads to a 27.3% difference or approximately 400 μJ difference for 40 A of die current (Figure 4-39). Module 9 has the poorest static current sharing as well as dynamic current sharing; during both dynamic and static sharing, die C carries less current. Perhaps static current sharing exacerbates energy loss differential during dynamic current sharing.

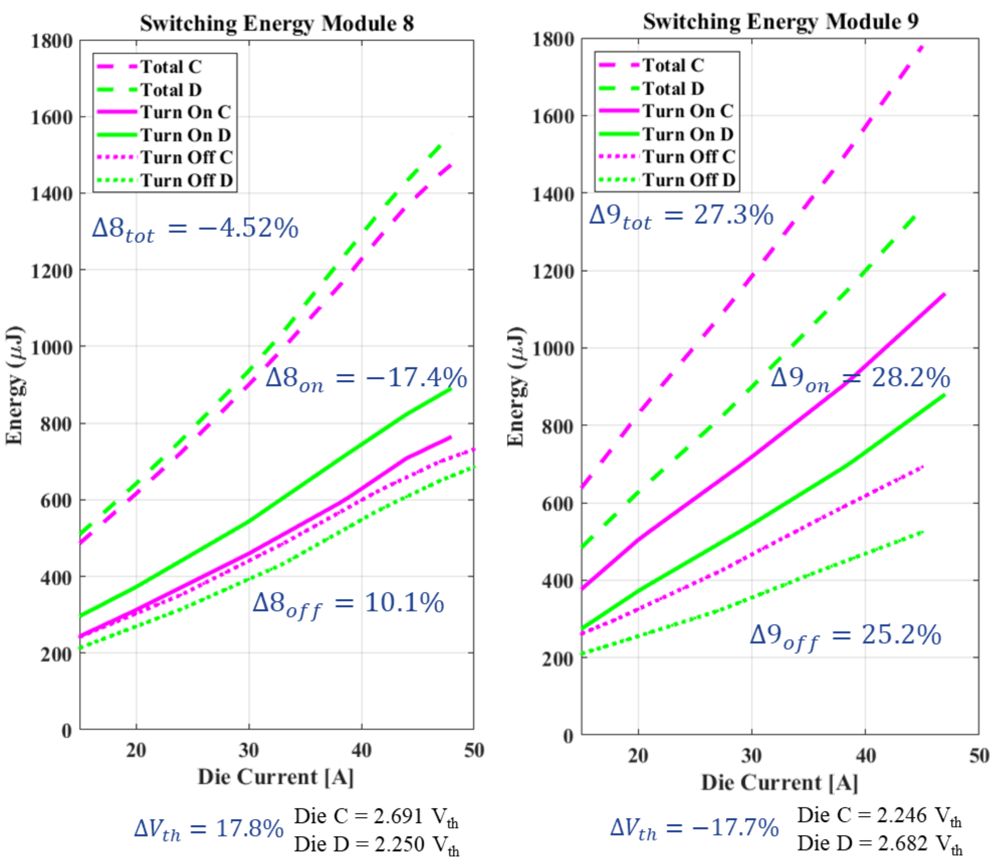


Figure 4-39. 600 V DPT switching energy for unbalanced modules 8 and 9 with percent differences

Chapter 5 **Power Module Thermal Testing**

5.1 Introduction

Power modules generate heat due to switching and conduction loss in the semiconductor devices as well as resistance in the leads and interconnections. This can cause a rise in temperature of the dies and package. A thermal management system is needed to extract the heat away from the dies; without, the heat can lead to poor reliability over time, lower efficiency, or catastrophic failure in the case of thermal runaway. The thermal performance is one of the leading constraining factors in that temperature is often the strongest contributor to package reliability [30]. Applications such as automotive modules require reliability in environments with potentially high ambient temperature. The dies in this project are rated up to 175°C operating temperature and there is expectation that SiC will be able to operate reliably in the 200-300°C range [19]. Advanced packaging is required to take advantage of the higher breakdown voltage, higher operating temperature, and ensure improved CTE mismatch for SiC over Si. Designing a thermal management system requires an understanding of how heat is generated and distributed in power modules. Device parametric tolerances are inevitable and quantifying the impact can provide

design constraints when selecting dies. In this study, we were interested in the impact of inherent device parametric tolerances on the thermal performance of the module.

5.1.1 Heat Removal and Thermal Resistance Estimation

The temperature of the dies is typically the hottest because the dies generate the most heat and is called the "junction temperature". Each subsequent layer is cooler than the dies so the heat will be transferred by conduction away from the dies. Once the heat reaches the heat sink, it can be transferred by convection, a transfer of heat from a solid to a fluid in motion, which is moving air in this case (Figure 5-1) [84]. The heat sink is designed with fins to increase the surface area for convection of heat to the surrounding air. A fan increases the air flow which has a higher heat transfer coefficient than stagnant air. Based on the material properties and geometry of each layer of the power module, the equivalent thermal resistance can be estimated.

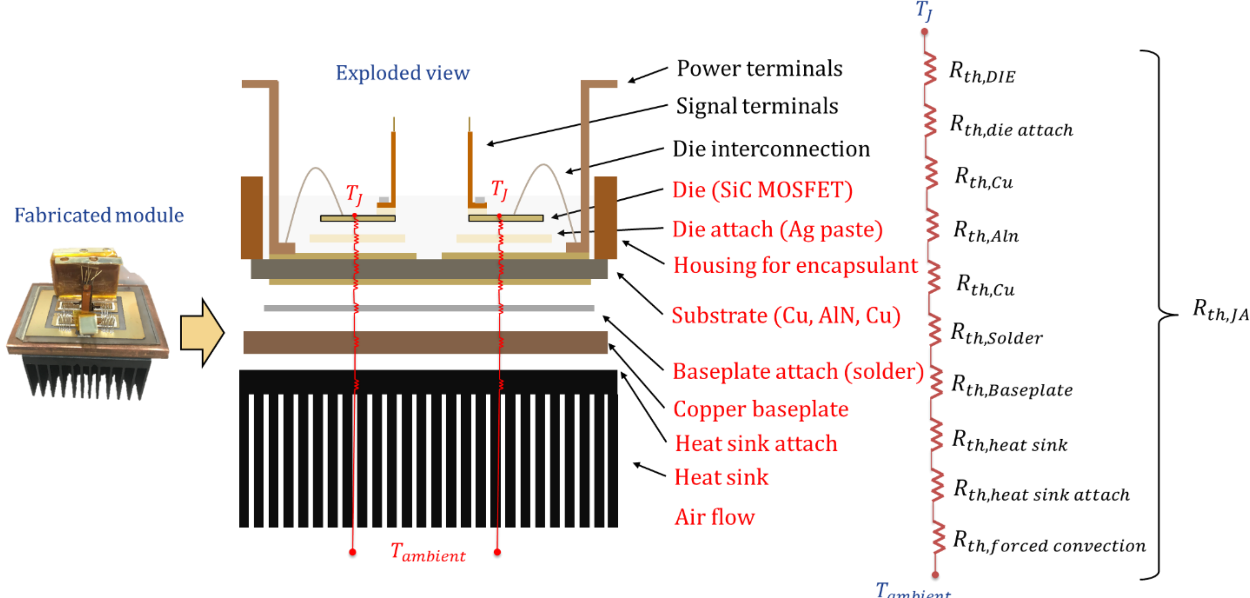


Figure 5-1. Equivalent thermal resistances for each layer from junction to ambient assuming lumped capacity

In general, the thickness, thermal conductivity, and area for each layer are necessary to calculate the thermal resistance for conduction (41) while the heat transfer coefficient and area are necessary to calculate the thermal resistance of convection (42).

$$R_{th_{cond}} = \frac{t}{\kappa * A} \quad (41)$$

$$R_{th_{conv}} = \frac{1}{h_c * A} \quad (42)$$

Thermal resistance can increase with additional layers because interfaces between layers may have voids which limit effective heat transfer; however, spreading of heat helps remove heat from the dies and each layer spreads the heat more. Layers with low thermal conductivity increase heat spreading. Often heat sinks, baseplates, and substrates can be used for heat spreading. A common rule for heat spreading angle is 45°, although more accurate calculations can lend to better thermal design and thermal performance simulation [23, 84]. In this case, both 0° and 45° heat spreading angle cases are calculated to estimate the thermal resistance of the module; however, the 0° case is utilized to estimate the worst case scenario for the junction temperature in order to run the continuous test well within a safe operating condition (Figure 5-2). In 45° case, a trapezoidal pyramid is formed with a smaller area at the top than the bottom base. In order to estimate the area for each layer, the average area is calculated with the length and width of the top area and the thickness of the layer in order to find the area of the base (Figure 5-3).

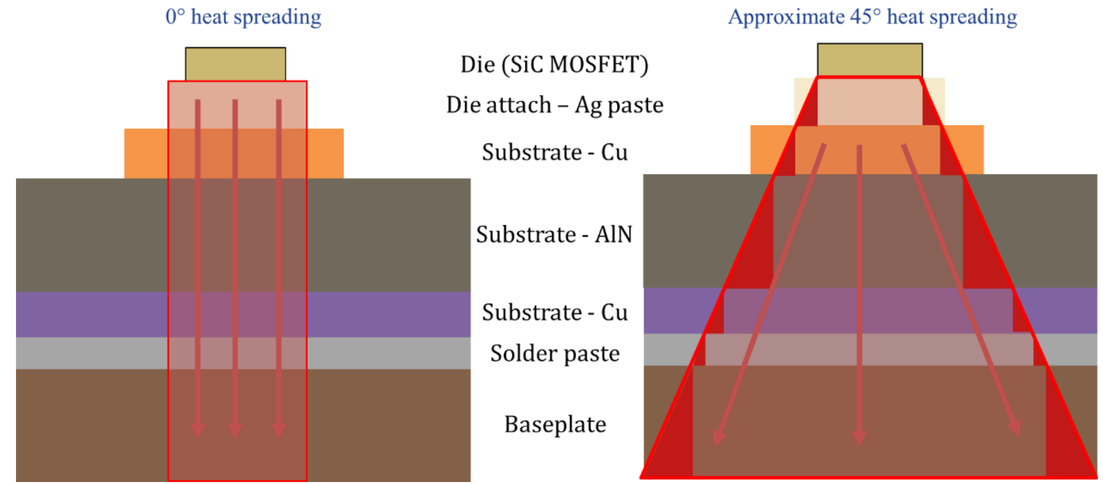


Figure 5-2. 0° and 45° heat spreading throughout the module

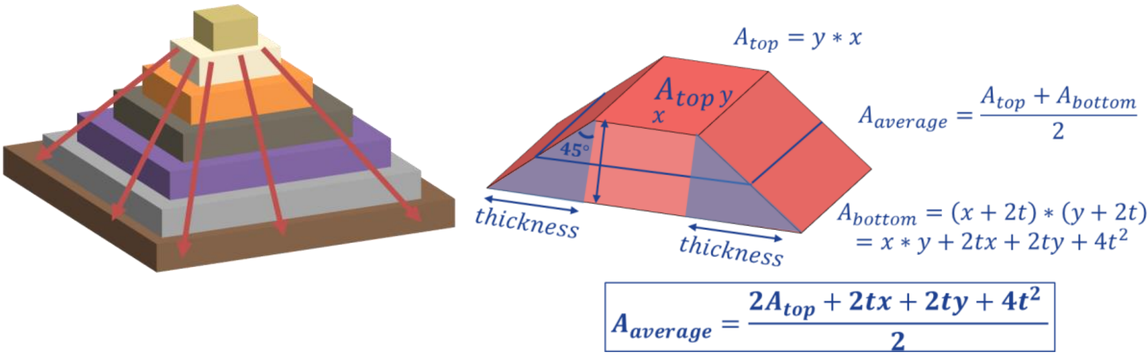


Figure 5-3. Calculating the approximate area for the 45° heat spreading case

In the 0° case, conduction through the baseplate is 0.595 K/W for a singular die (41); with 2 dies in parallel, that value is halved, 0.298 K/W. In the 45° case, conduction through the baseplate is 0.255 K/W for a singular die and 0.127 K/W for 2 dies in parallel (Table 7). The fan of choice, PF40561BX-000U-S99, has a thermal resistance dependent on the air flow passing through the fins. The airflow is determined based on the air flow value of 31.7 CFM for the fan of choice, ATS-56005-C3-R0 [74]. The values for the air velocity in m/s is converted with an air velocity calculator [75, 76]. Therefore, the thermal resistance of the heat sink and fan based on convection

is 3.597 K/W. The total module thermal resistance is approximately 3.895 K/W for the 0° case and 3.724 K/W for the 45° case after adding the thermal resistances of the heat sink, fan, and 2 paralleled dies.

Table 7. Equivalent thermal resistances for the power module for 0° and 45° heat spreading

	t (m)	$\kappa\left(\frac{W}{mK}\right)$	A (m^2) 0°	A (m^2) 45°	$R_{th}\left(\frac{K}{W}\right)$ 0°	$R_{th}\left(\frac{K}{W}\right)$ 45°
Die (SiC MOSFET)	$18 * 10^{-5}$ (180 µm)	120	$A_{die} = 4.36$ mm x 7.26 mm $= 3.17 * 10^{-5}$ m^2		0.0473	0.0473
Die attach	$5 * 10^{-5}$ m (50 µm)	240	$3.17 * 10^{-5}$	$3.22 * 10^{-5}$	0.0066	0.0065
Substrate - copper	$2 * 10^{-4}$ m (8 mil)	400	$3.17 * 10^{-5}$	$3.53 * 10^{-5}$	0.0158	0.0142
Substrate - AlN	$6.35 * 10^{-4}$ m (25 mil)	177	$3.17 * 10^{-5}$	$4.65 * 10^{-5}$	0.113	0.0771
Substrate - copper	$2 * 10^{-4}$ m (8 mil)	400	$3.17 * 10^{-5}$	$5.85 * 10^{-5}$	0.0158	0.0086
Solder paste	$1.27 * 10^{-4}$ m (5 mil)	50	$3.17 * 10^{-5}$	$6.36 * 10^{-5}$	0.0802	0.0399
Baseplate	$4 * 10^{-3}$ m	400	$3.17 * 10^{-5}$	$1.64 * 10^{-4}$	0.3159	0.0611
Heat sink					1.2 @ 3 m/s	
Forced Convection	$h_C = 24.7 \frac{W}{m^2K}$	$hc = 10.45 - v + 10\sqrt{v}$ where $v = 2.98$ m/s				

5.1.2 Junction Temperature Estimation

Knowing the thermal resistance of the package allows for estimating the junction temperature of the dies under various operating conditions. Heat is generated by switching and conduction losses in the module; power loss multiplied by thermal resistance provides a temperature value (43).

$$\Delta T = P * R_{th} \tag{43}$$

First, switching power loss is dependent on switching energy loss and frequency (44). The energy loss is multiplied by potential operating frequencies, 5 kHz, 10 kHz, 20 kHz, and 30 kHz for the balanced 6 (Figure 5-4) and unbalanced 8 (Figure 5-5) cases to estimate the power loss.

$$P_{sw} = E_{sw} * F_{sw} \tag{44}$$

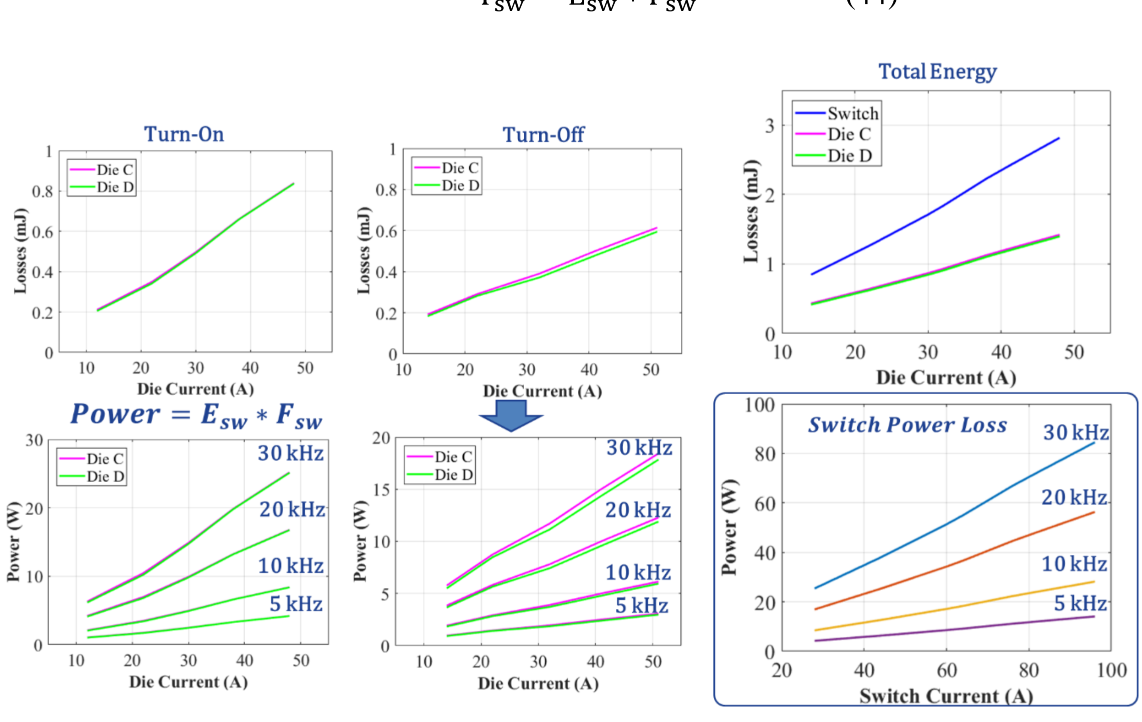


Figure 5-4. Estimating switching power loss for various frequencies based on switching energy loss for balanced module 6

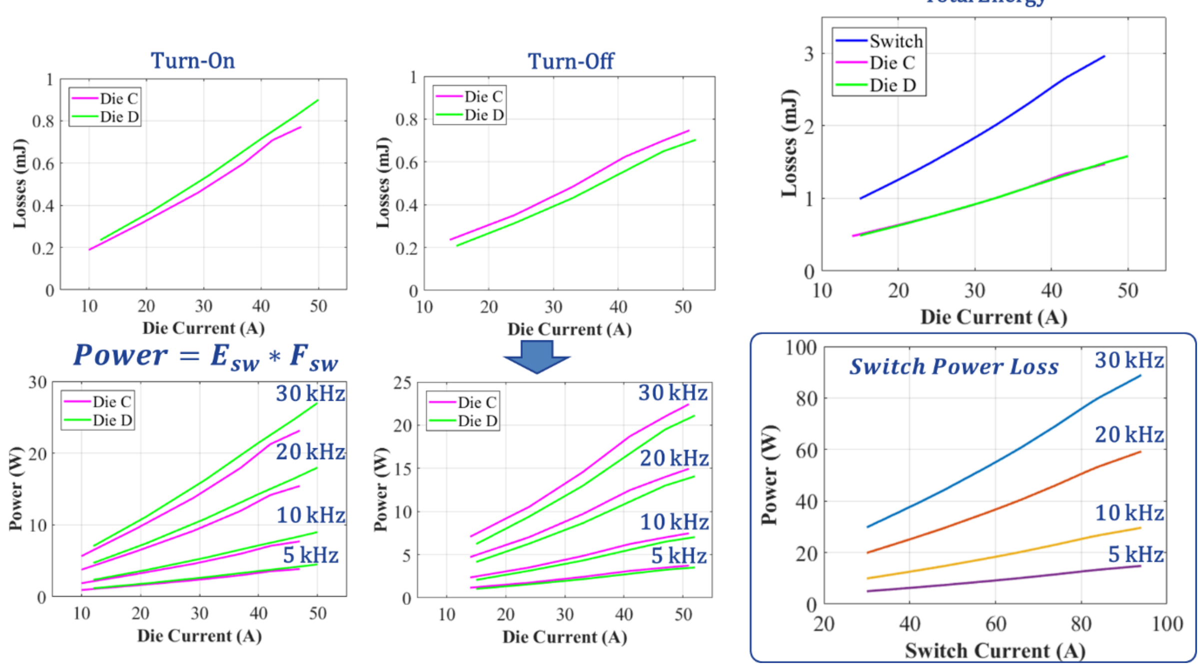


Figure 5-5. Estimating switching power loss for various frequencies based on switching energy loss for unbalanced module 8

Second, the conduction power loss is estimated based on the on-state resistance for various rms currents (45-46). On-state resistance may increase with temperature; we know the values at 25°C but the on-state resistance at 175°C had to be estimated based on the datasheet information [83]. By multiplying the on-state resistance by rms die currents, the conduction losses is estimated (Figure 5-6).

$$P_{cond} = {I_{rms}}^2 * R_{dson} \qquad (45)$$

$$I_{rms} = I_{peak} * \sqrt{D} \qquad (46)$$

Where $D = 50\%$

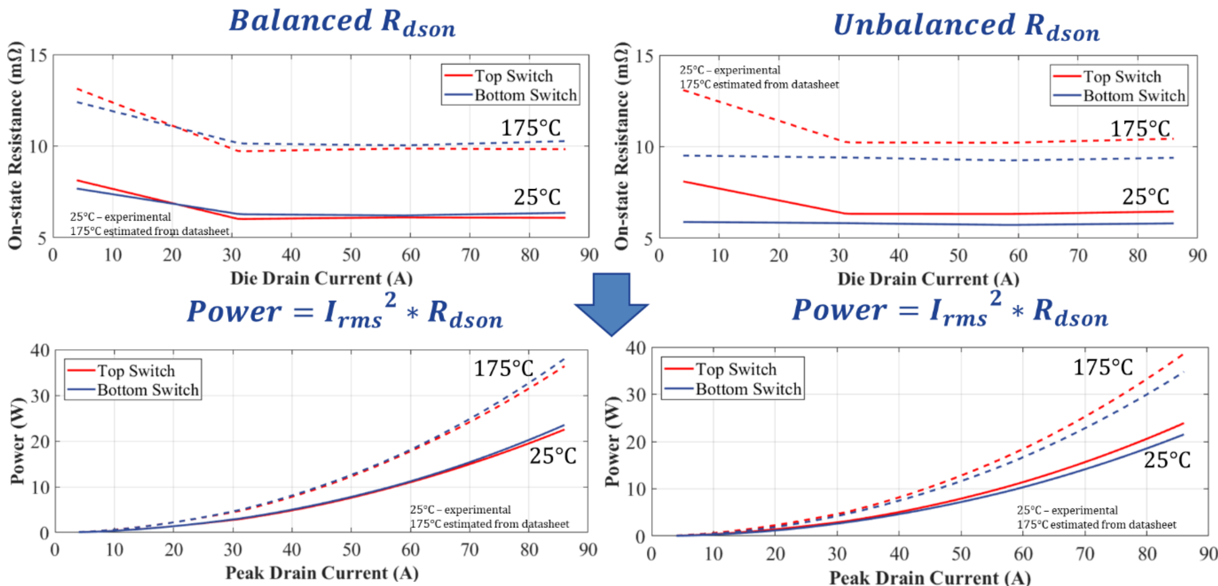


Figure 5-6. Estimating conduction power loss for various rms drain currents for balanced module 6 and unbalanced module 8

Once switching and conduction loss are estimated, they can be added together for each frequency to determine the estimated total power loss for various frequencies and currents (Figure 5-7). In this final step, the currents for each die are added together as well so that the current values are given for the entire switch; in this way, the power loss is estimated for operating the module as opposed to operating individual dies.

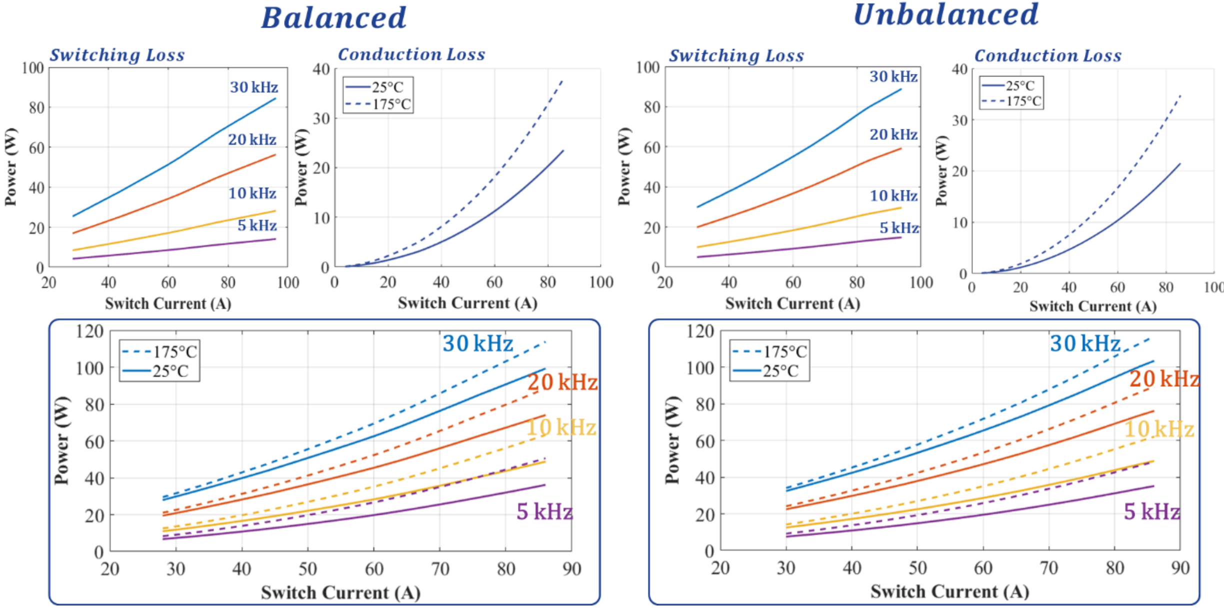


Figure 5-7. Estimating total power loss for various operating points for balanced module 6 and unbalanced module 8

Lastly, the junction temperature can be estimated from baseplate to junction for various operating conditions by multiplying the power loss and the thermal resistance from baseplate to junction. This same calculation could be done for the ambient to junction temperature change, however, the most accessible thermal measurement for these modules was the baseplate. As seen in Figure 5-9, the encapsulant is thick and reflective so thermal measurements cannot be made with the infrared camera from the top of the module. The face of the baseplate was the best place to measure temperature. An ideal location is measuring the middle of the baseplate; at this location, the heat has not spread and will be hottest. However, this is covered by the heatsink. Therefore, we chose to monitor temperature at the edge of the baseplate where the infrared camera could access. It is assumed this value is lower than the value in the baseplate to junction temperature estimate because it is the edge of the baseplate. Furthermore, the individual die temperatures cannot be measured from the edge, but the overall temperature rise for both dies may be

comparable from one module to another. This method is not an accurate measure of junction temperature but provides a consistence method for comparing baseplate temperatures which can still provide information about thermal management. Therefore, the baseplate to junction temperature estimation guided operating constraints for the continuous tests. For example, the temperature rise at 50 A and 30 kHz is 35°C; if we want to keep the junction temperature below 150°C, that may be a risky operating point if the edge of the baseplate reads 100°C.

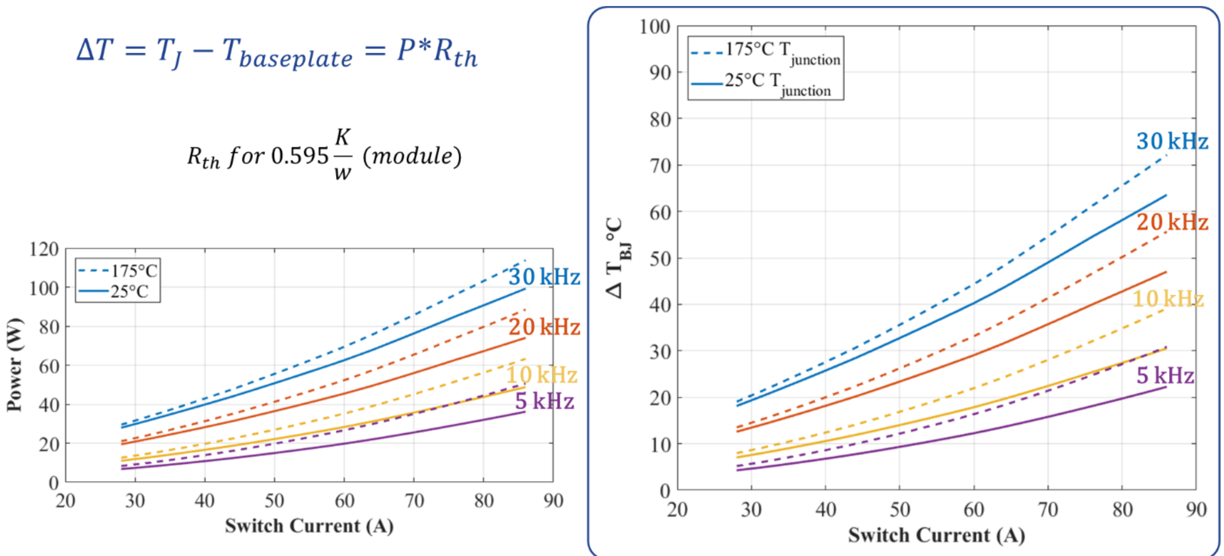


Figure 5-8. Estimating junction temperature for various operating points for balanced module 6 and unbalanced module 8

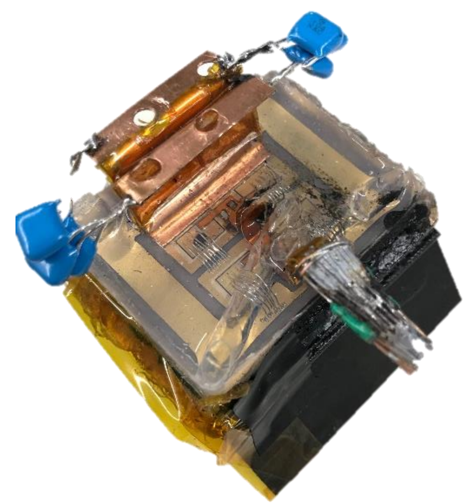


Figure 5-9. Fully fabricated module with heat sink and black liquid tape covering the face of the baseplate

5.2 Continuous Test Setup

In order to evaluate the thermal performance of the module, it is placed into a boost converter (Figure 5-10). The primary behavior of interest is the MOSFET switching of the bottom dies; therefore, a boost converter allows for hard switching of the bottom switch while the top switch is held low with only conduction of the body diode. The driving signal is an open loop system using a function generator with a 50% duty cycle, 30 kHz square wave form given to the bottom switch and a -5 V signal for the top switch to pull it low. The Magna-Power MTD1000-100/480+BD+HS+LXI can provide enough current and voltage. Two 30 kW resistors banks are connected in series to create approximately 22 Ω. A busbar is created with 2 large copper plates that come in a roll; both DC- and DC+ are drilled to fit over the terminals of the capacitor that is in parallel with the load resistor. By using large planes for the DC busbar and stacking them on one another, the inductance is reduced. The impact of the inductance is further reduced with decoupling capacitors soldered onto the terminals of the module, although the length of the leads

should be minimized more (Figure 5-9). The other end of the busbar is hole punched to interface with the screw holes of the module (Figure 5-12). A 500 μH inductor is connected to the AC terminal of the module and the DC+ cable from the power supply. Rogowski coils fit underneath the wire bonds through the plastic tubing for monitoring the current of the bottom dies. In initial testing, a large current Tektronix A6304XL 500 Amp Current Probe is used to double check the input current. Tektronix TDP1500 200 MHz Differential Probes are eventually used to monitor the input and output voltages (Figure 5-11).

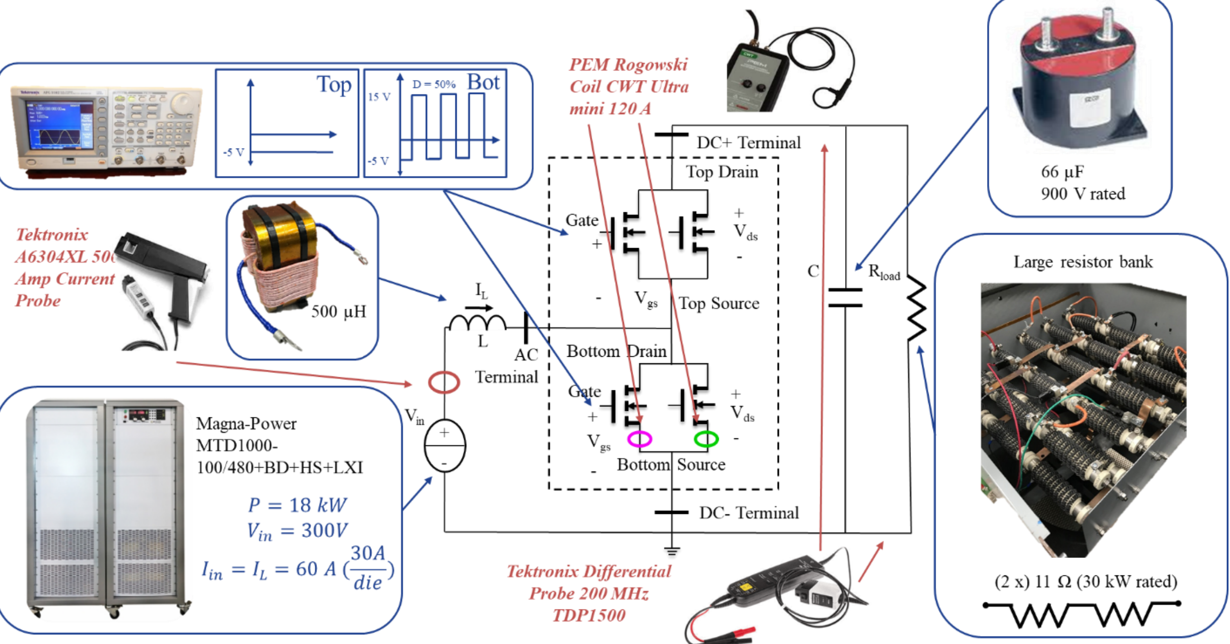


Figure 5-10. Continuous, boost, test setup with equipment indicated

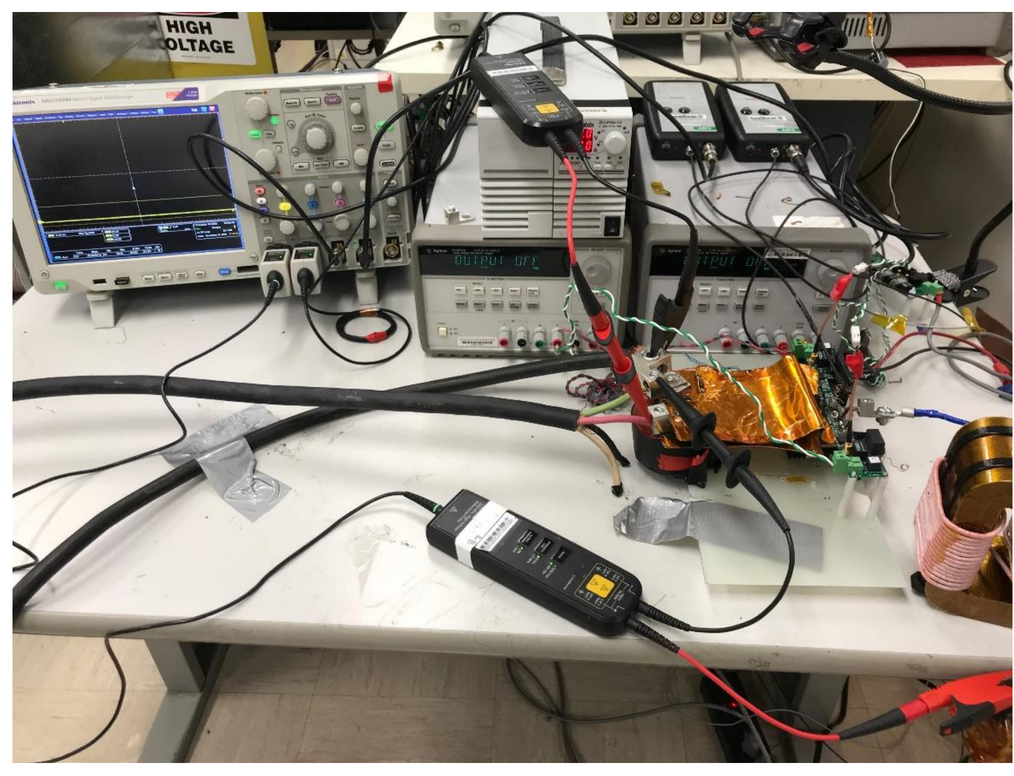


Figure 5-11. Continuous, boost, test setup with some equipment shown

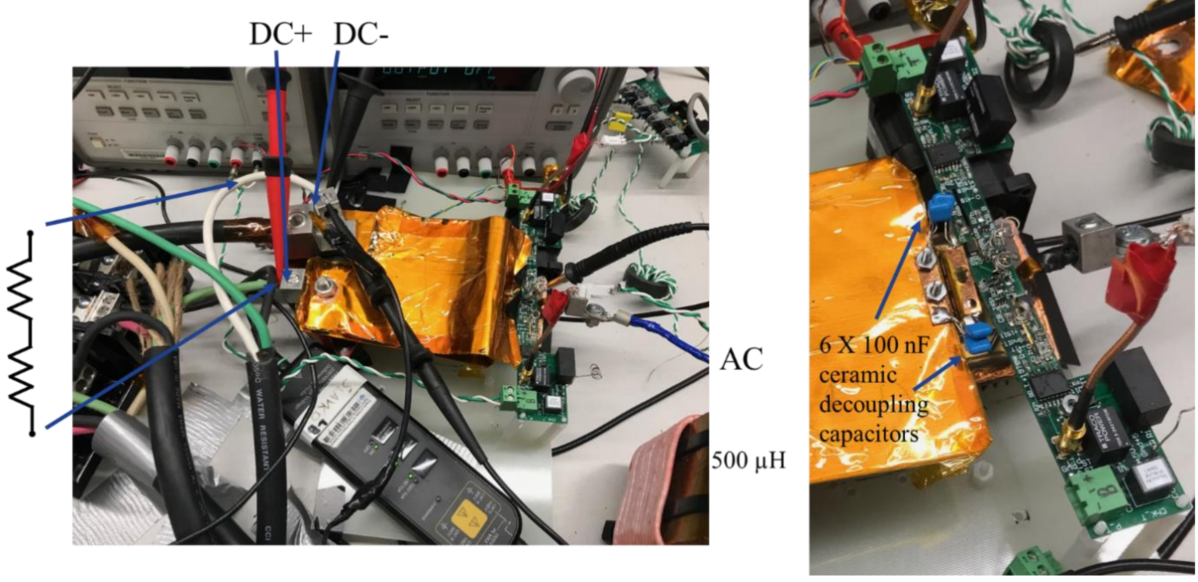


Figure 5-12. Closer image of the continuous, boost, test setup with busbar connection

5.3 Continuous Test Results

The modules were tested continuously at 30 kHz up to 250 V, 47.7 A input, however, this was not thermally stable (Figure 5-13). The modules could run continuously at 200 V, 37.7 A input for at least 10 minutes (Figure 5-14-Figure 5-15).

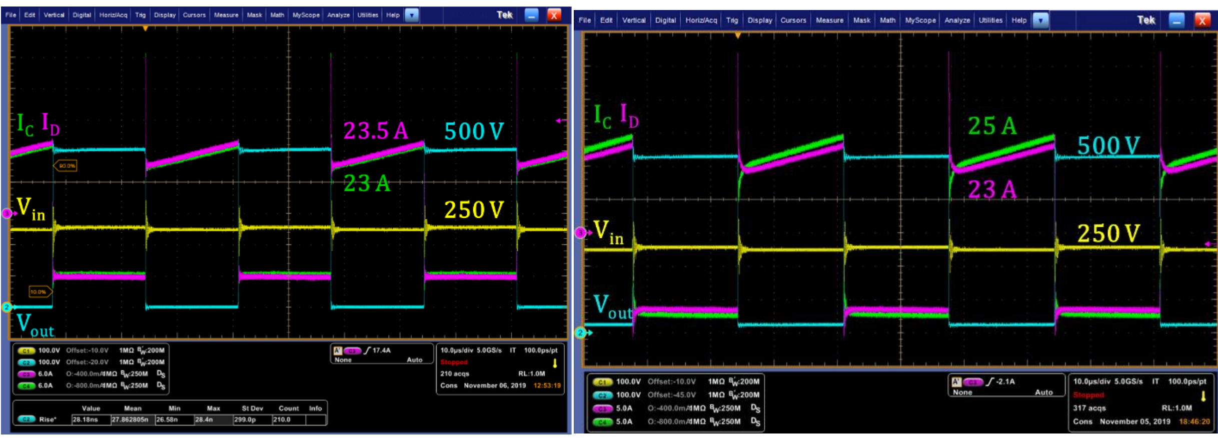


Figure 5-13. Continuous test results for balanced 6 and unbalanced module 8 at 250 V, 47.7 A input

Figure 5-14. Continuous test results for balanced modules 4 and 6 at 200 V, 37.7 A input

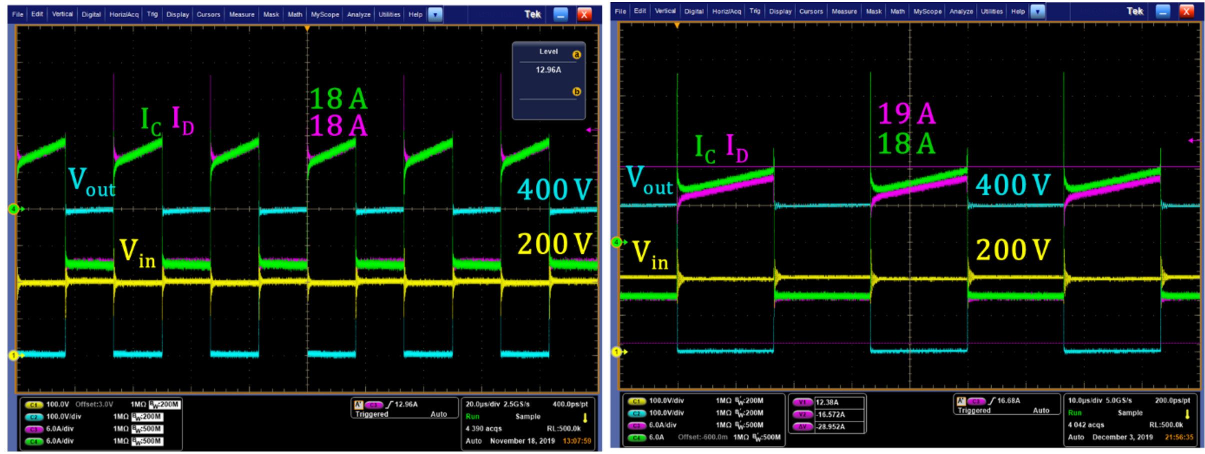


Figure 5-15. Continuous test results for unbalanced modules 8 and 9 at 200 V, 37.7 A input

The turn-on dynamic current sharing for the balanced modules is well matched in both turn-on time and peak current with less than 7% difference in di/dt and less than 2.5% difference in peak current (Figure 5-16-Table 10). The turn-on dynamic current sharing for the unbalanced modules is significantly different in both di/dt and peak current with 18.9% and -26.7% difference in peak current and 18.2% and -29.8% difference in di/dt for modules 8 and 9, respectively (Figure 5-19-Table 9). The average peak current for module 8 was less than 30 which is lower than all other modules although the static current was in an appropriate range. Later testing of module 8 presented a short circuit in the module without catastrophic failure. Because the behavior of module 8 during DPT testing was similar to the other modules, malfunction may have already occurred before the continuous test results presented here. Therefore, data from module 8 may not be reliable for continuous test comparison.

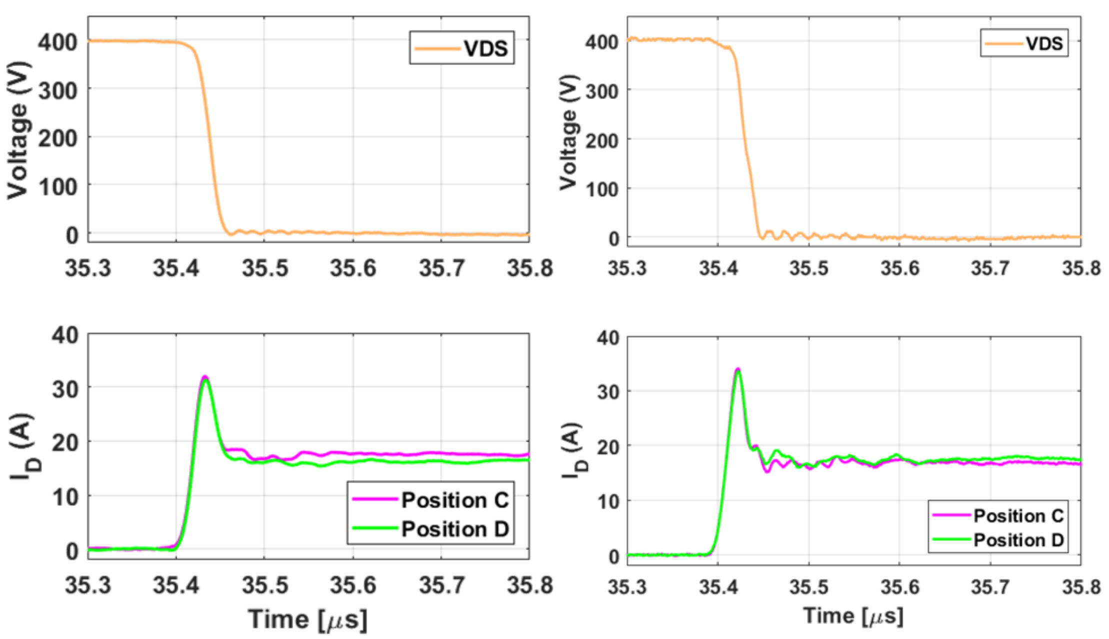


Figure 5-16. Continuous test turn-on results for balanced modules 4 and 6 at 200 V, 37.7 A input

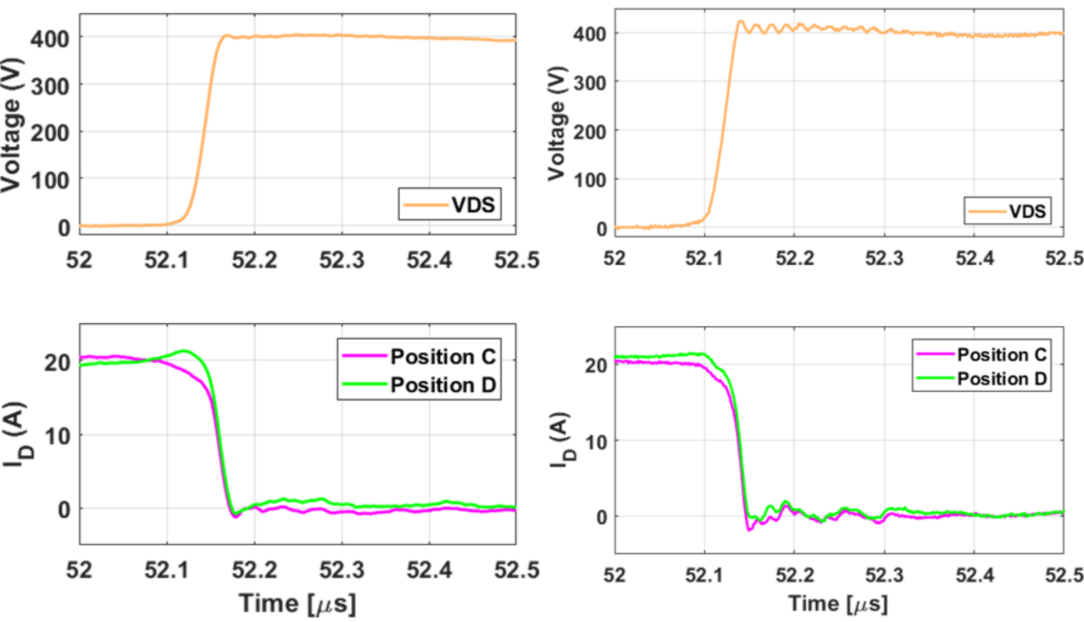


Figure 5-17. Continuous test turn-off results for balanced modules 4 and 6 at 200 V, 37.7 A input

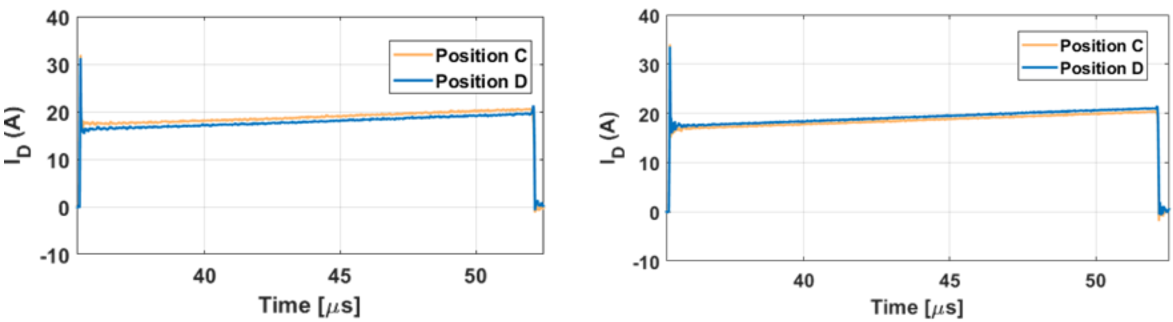


Figure 5-18. Continuous static results for balanced modules 4 and 6 at 200 V, 37.7 A input

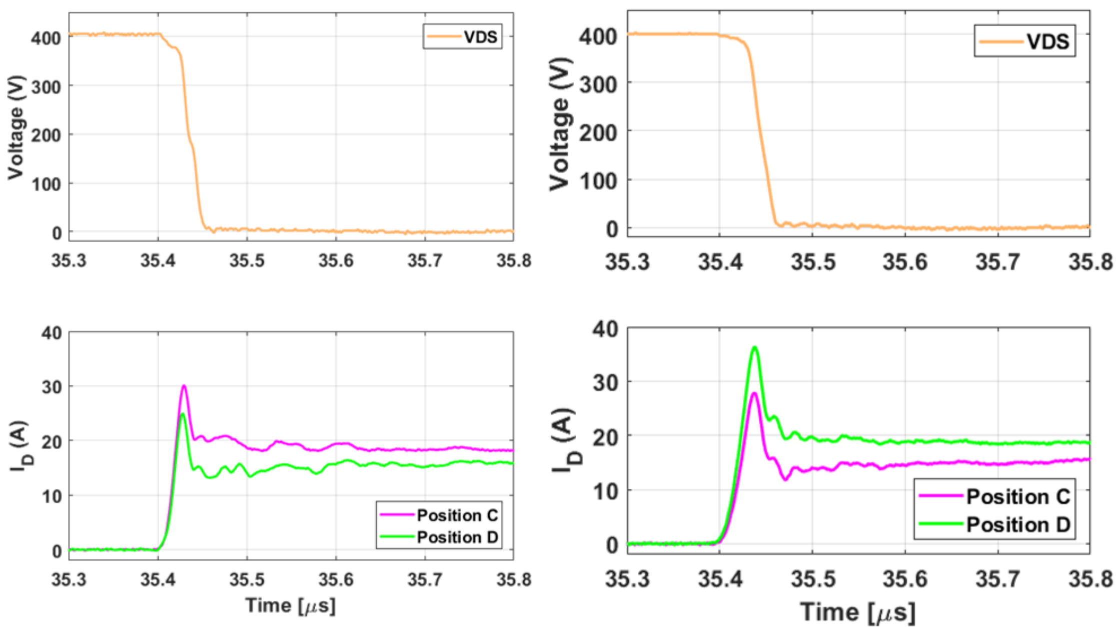


Figure 5-19. Continuous test turn-on results for unbalanced modules 8 and 9 at 200 V, 37.7 A input

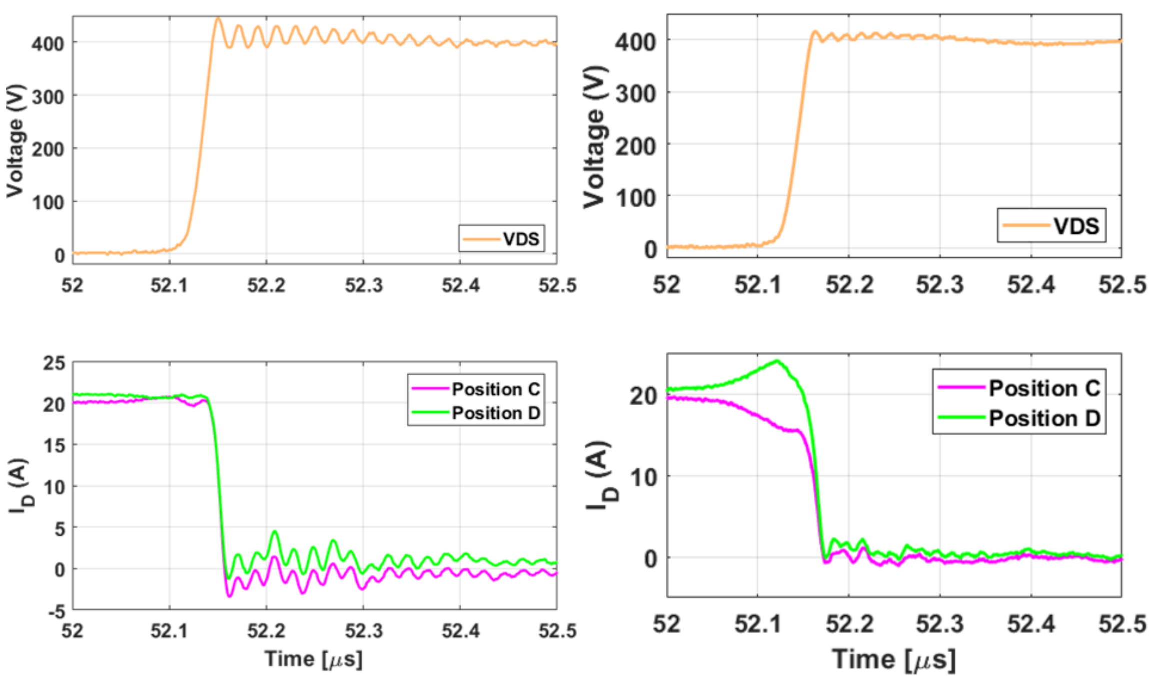


Figure 5-20. Continuous test turn-off results for unbalanced modules 8 and 9 at 200 V, 37.7 A input, 400 V, 18.85 A output

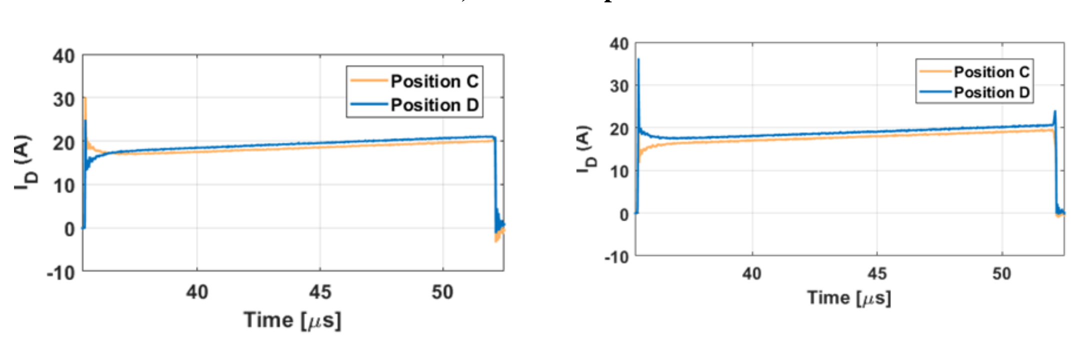


Figure 5-21. Continuous static results for unbalanced modules 8 and 9 at 200 V, 37.7 A input

Table 8. Continuous test turn-on result comparisons for Modules 4, 6, 8, and 9 where pink indicates a higher value for die C and grean, negative indicates a higher value for die D for percent difference

$\frac{dV}{dt}$	13.3 V/ns (24 ns)		14.2 V/ns (22.6 ns)		14 V/ns (23.2 ns)		12.6 V/ns (25.4 ns)	
$\frac{dI}{dt}$	1 A/ns (14 ns)	-6.76% diff	1.15 A/ns (11.6 ns)	3.54% diff	1.26 A/ns (11.6 ns)	18.2% diff	0.713 A/ns (17.4 ns)	-29.8% diff

	1.07 A/ns (12 ns)		1.11 A/ns (12.6 ns)		1.05 A/ns (12.2 ns)		0.963 A/ns (17.2 ns)	
Peak current	31.96 A 31.3 A	2.15% diff	34.0 A 33.5 A	1.47% diff	30.1 A 24.9 A	18.9% diff	27.9 A 36.4 A	-26.7% diff

Table 9. Continuous test turn-off result comparisons for Modules 4, 6, 8, and 9 where pink indicates a higher value for die C and grean, negative indicates a higher value for die D for percent difference

$\frac{dV}{dt}$	**10.7 V/ns (30 ns)**		**12.1 V/ns (26.4 ns)**		**13.7 V/ns (23.4 ns)**		**11.5 V/ns (27.8 ns)**	
$\frac{dI}{dt}$	0.371 A/ns (44 ns) 0.322 A/ns (20 ns)	14.1% diff	0.509 A/ns (31.6 ns) 0.7 A/ns (26.4 ns)	-31.6% diff	1.45 A/ns (11 ns) 1.29 A/ns (13 ns)	11.7% diff	0.214 A/ns (73 ns) 0.963 A/ns (17.2 ns)	-127% diff
Peak current	18.6 A 21.3 A	-13.3% diff	19.95 A 21.5 A	-7.62% diff	21.1 A 21.1 A	0% diff	24.1 A 16.0 A	-40.5% diff

Table 10. Continuous test static on-state result comparisons for Modules 4, 6, 8, and 9 where pink indicates a higher value for die C and grean, negative indicates a higher value for die D for percent difference

Static current	18.7 A 17.8 A	4.75% diff	18.5 A 19.3 A	-4.06% diff	18.3 A 19.4 A	-5.41% diff	17.9 A 18.9 A	-5.74% diff
Average	18.25 A		18.9 A		18.85 A		18.4 A	

Balanced module 4 and unbalanced module 9 demonstrate similar behavior as in DPT with die C turning off before die D causing an overshoot in die D. The peak currents are -13.3% and -40.5% different for modules 4 and 9, respectively. Module 4 has relatively low percent difference in di/dt at 14.1% because die C has a higher static value which offset the faster slope in die D. Module 9

has significantly higher percent difference for di/dt at -127% which results from the already lower static current in die C when it starts to turn off earlier forcing die D to carry more current momentarily.

The impact of threshold voltage alone could not ensure balanced dynamic current sharing. Minor dynamic unbalance in Module 6 where die C carries less current than D is made worse because die C also carries less current during dynamic current sharing. On the other hand, module 4 has a more significant difference in peak current but because opposite dies carry more current during the static on-state and during the switching state, the overall di/dt percent difference is relatively low. Therefore, static and dynamic behavior interact to determine the overall impact of unbalanced current sharing.

In terms of energy loss, unbalanced module 9 has the highest total loss with 855.2 µJ and unbalanced module 8 has the lowest total loss with 679 µJ (+23.0% difference) (Figure 5-23). The balanced modules, 4 and 6, have lower total energy loss than unbalanced module 9. The loss differential is smallest for the balanced modules compared to the unbalanced modules (Table 11).

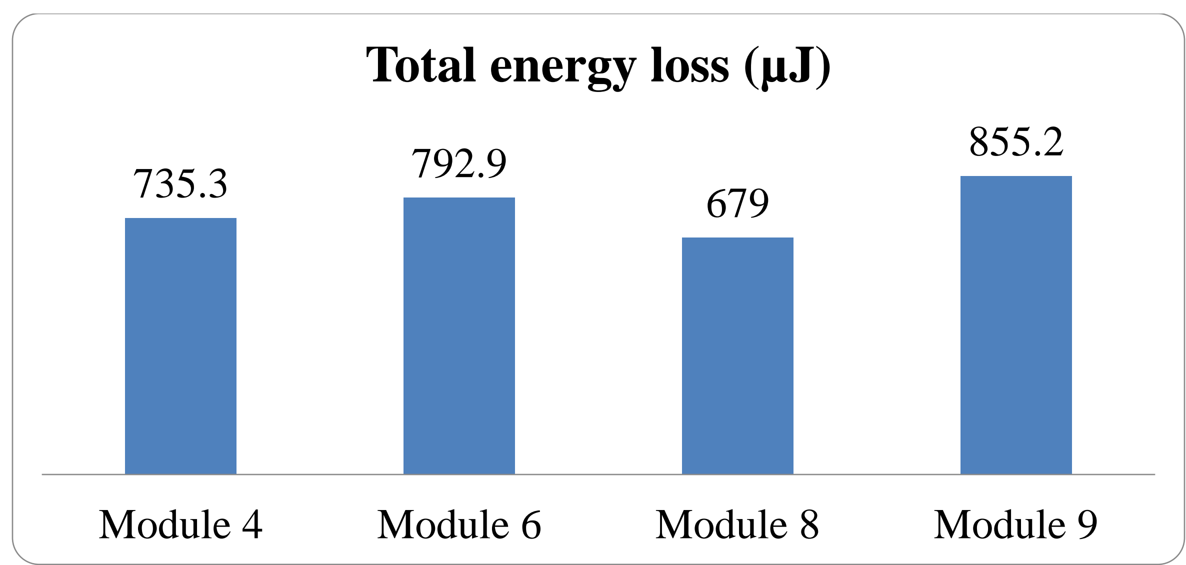


Figure 5-22. Total energy loss for all continuously tested modules

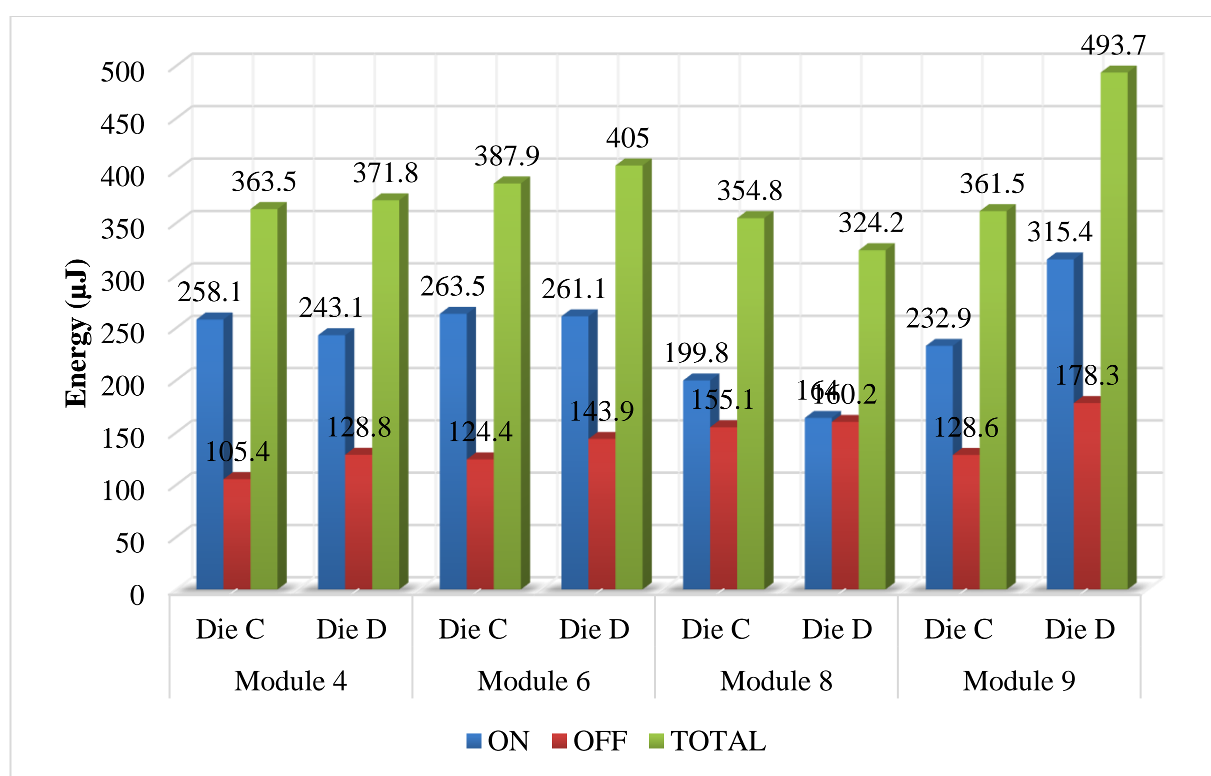


Figure 5-23. Energy loss for all continuously tested modules

Table 11. Continuous test energy loss result comparisons for Modules 4, 6, 8, and 9 where pink indicates a higher value for die C and grean, negative indicates a higher value for die D for percent difference

Turn-on	258.1	5.99% diff	263.5	0.91% diff	199.8	19.7% diff	232.9	-30.1% diff
	243.1		261.1		164		315.4	
Turn-off	105.4	-20.0% diff	124.4	-14.5% diff	155.1	-3.24% diff	128.6	-32.4% diff
	128.8		143.9		160.2		178.3	
Total	363.5	-2.26% diff	387.9	-4.31% diff	354.8	9.01% diff	361.5	-30.9% diff
	371.8		405		324.2		493.7	

Module 9 has significantly higher losses and energy differential, -30.9%, because die D carries more current during turn-on, turn-off, and the static state. Die D has the highest losses during turn-on and turn-off, -30.1% and -32.4% difference compared to die C (Figure 5-23-Table 11).

For module 8, die C has a higher overshoot but die D carries more current during the static on-state. Module 8 has lower loss differential, 9.01%, because die C has higher losses during turn on (19.7%) but die D carries more current in the static on-state (-5.41%) which offsets the turn-on losses from die C (-3.24). Again, module 8 may have had electrical damage during this test, so it cannot be determined if the overall lower loss was a result of design or due to damage that caused the low overshoots.

Comparing the balanced modules, in module 4, the offsetting effect between static and dynamic current sharing leads to lower total energy loss, 735.3 μJ, compared to module 6, 792.9 μJ (-7.34 % difference) (Figure 5-23, Figure 5-22). However, the average static current for module 4, 18.3 A, is slightly higher than the module 6, 18.9 A (-3.23 % difference) so if test conditions are different, that could account for some of the higher energy loss in module 6. However, the percent difference in average static current is -3.23% while the percent difference in loss is -7.34% which suggests any difference in test conditions does not account for all the difference.

Table 12. Summary of percent differences for Modules 4, 6, 8, and 9 where pink indicates a higher value for die C and grean, negative indicates a higher value for die D

Turn-on di/dt	-6.76% diff	3.54% diff	18.2% diff	-29.8% diff
Turn-on peak current	2.15% diff	1.47% diff	18.9% diff	-26.7% diff
Turn-off di/dt	14.1% diff	-31.6% diff	11.7% diff	-127% diff
Turn-off peak current	-13.3% diff	-7.62% diff	0% diff	-40.5% diff
Static current	4.75% diff	-4.06% diff	-5.41% diff	-5.74% diff

Sum of peak current and static current	-6.4%	-10.2%	13.49%	-72.9%
Total energy loss	-2.26%	-4.31%	9.01%	-30.9%
Vth	-0.62%	0.20%	17.8%	-17.7%

To summarize, the overall loss differential is lowest for the balanced modules as expected (Table 12). For both balanced modules, which have less than 1% difference in the threshold voltage of the paralleled dies, there is less than 5% difference total energy loss. In module 4, there is a significant difference in the turn-off loss, but this difference is compensated during turn-on and the static on-state. In the unbalanced modules, which has ~17% difference in threshold voltages, the loss differential ranges from 9.01% in module 8 to -30.9% in module 9. Unbalanced module 8 has the lowest losses overall because of the lowest overshoot during turn-on while unbalanced module 9 has the highest losses because of the large overshoot for the paralleled die with the lower threshold voltage.

To reiterate, the highest loss differential occurs (for both balanced and unbalanced cases), when one die carries more current during turn-on, turn-off, and the static state. If the dies took turns carrying more current because of either the threshold voltage mismatch, possible on-state resistance, or another source of mismatch, the losses could be offset. Therefore, while device parametric tolerances are inherent, if the higher threshold voltage devices can be paired with devices that have higher on-state resistance, the overall loss differential may perform similarly to well-matched dies.

5.4 Continuous Thermal Test Results

The thermal impact of device parametric tolerances is critical because thermal management adds density and weight to the system. Furthermore, overheating, and thermal overstress are primary limiting factors to performing at maximum current ratings of the bare dies.

To assess the thermal performance, the front baseplate face is coated with spray on electrical tape to create a black surface for the IR camera (Figure 5-26). The small thermal camera that connects directly with iPhones is held inside the test bay using a flexible tripod; a ~8ft female to female iPhone cable connects the camera inside the bay to a phone outside the bay.

The hottest spot is identified on this front face (Figure 5-26). It should be noted that this is not the hottest spot in the baseplate; nor will this spot align with the baseplate to junction temperature calculated earlier because the baseplate is hottest at the very center, underneath the dies where the heat has not spread (Figure 5-2). Therefore, this method is not intended to estimate the junction temperature accurately but to compare the overall heating of the baseplate due to balanced and unbalanced module design.

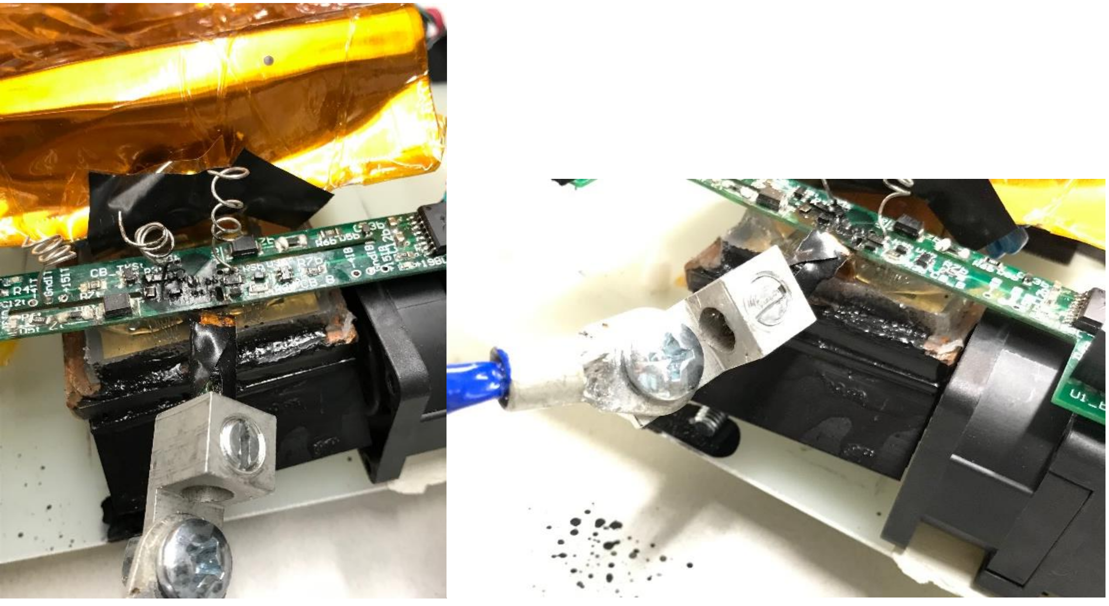


Figure 5-24. Thermal test setup for continuous test of modules

The ideal method for measuring temperature is to ensure thermal equilibrium once the temperature no longer rises. If the module experiences thermal runaway that is a different situation but at low enough power, the fan can sufficiently balance the power loss and reach thermal equilibrium. It is consistent after five minutes when the temperature is relatively flat except for cases of thermal runaway (Figure 5-25).

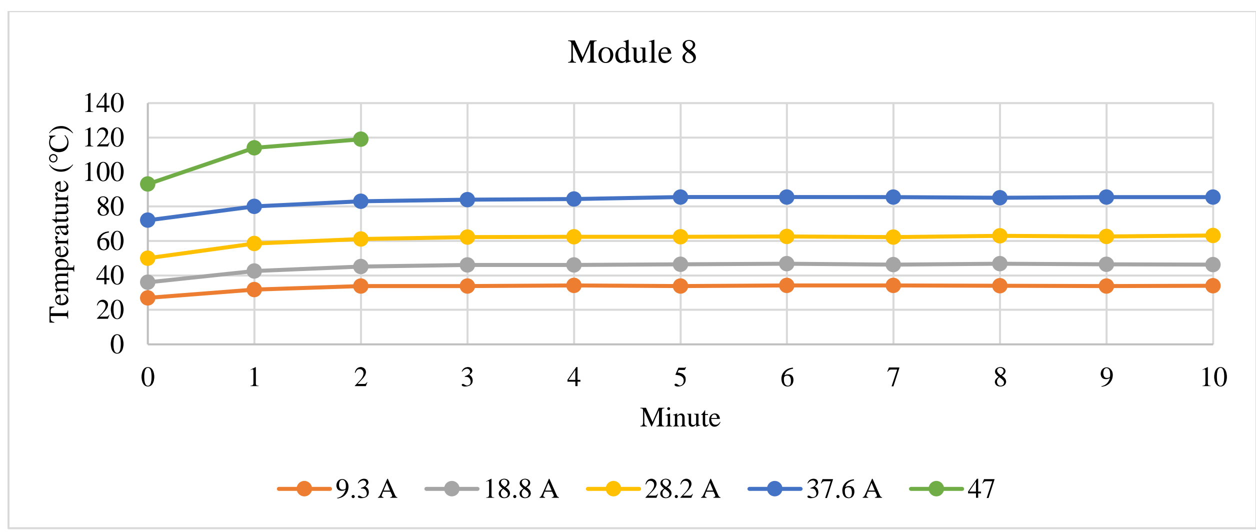


Figure 5-25. After ~5 minutes, the module reached thermal equilibrium

The temperature of the baseplate is evaluated using a spot identifier on the thermal camera. Thermal equilibrium is reached for the 200 V, 37.7 A input, 400 V, 18.85 output case although the value varies according to the spot by a few degrees as seen in the two values for module 9 (Figure 5-26). Therefore, when comparing temperatures, consider +/- 5 degree. Balanced module 6, and unbalanced modules 8, and 9 all have insignificantly different temperatures in the 91.9°C to 96.7°C range (Figure 5-27). Balanced module 4 has the lowest temperature of 70.9°C. According to the losses, module 8 should have the lowest temperature with the lowest switching losses. In addition, module 8 has the lowest on-state resistance which would contribute to lower conduction losses as well (Figure 5-28).

Figure 5-26. Thermal image of modules 4, 6, 8, and 9 at 200 V, 37.7 A input, 400 V, 18.85 A output

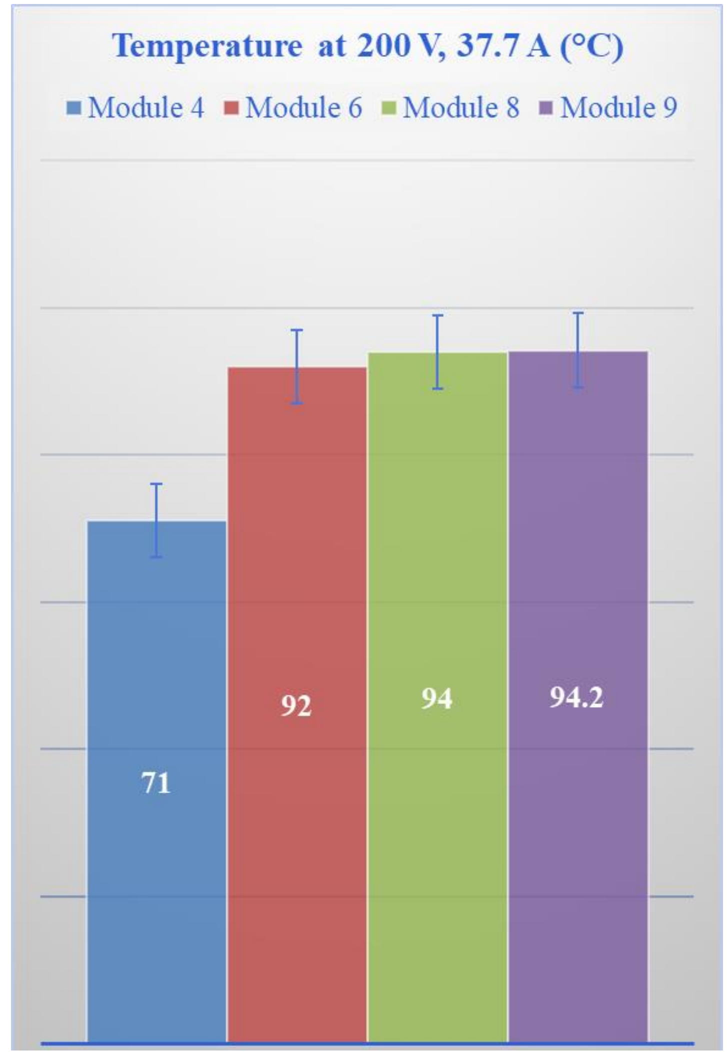


Figure 5-27. Comparison of module 4, 6, 8, and 9 temperature for 200 V, 37.7 A input, 400 V, 18.85 A output

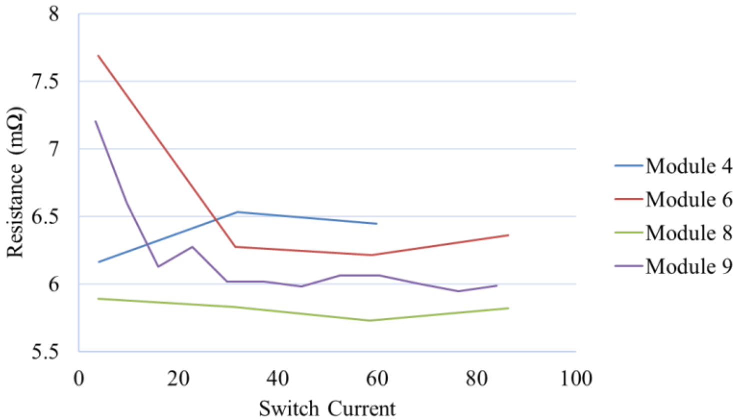


Figure 5-28. On-state resistance for modules 4, 6, 8, and 9 across switching current

Based on the thermal results at 150 V, 28.3 A, both unbalanced modules have higher temperatures than the balanced modules (Figure 5-29). Module 4 again has the lowest temperature. When a 250 V, 47.7 A input test is attempted, modules 6 and 9 reach destructive levels of temperature with module 6 blowing up (Figure 5-30-Figure 5-31). The heat sink is attached with the high-performance adhesive thermal interface material that came with the heat sink. It is very possible that this method led to excessive voids or poor attachment which led to poor thermal management. In order to determine if this were the case, an x-ray or acoustic image of the heat sink attachment for all the modules would confirm or negate the presence of excessive voids.

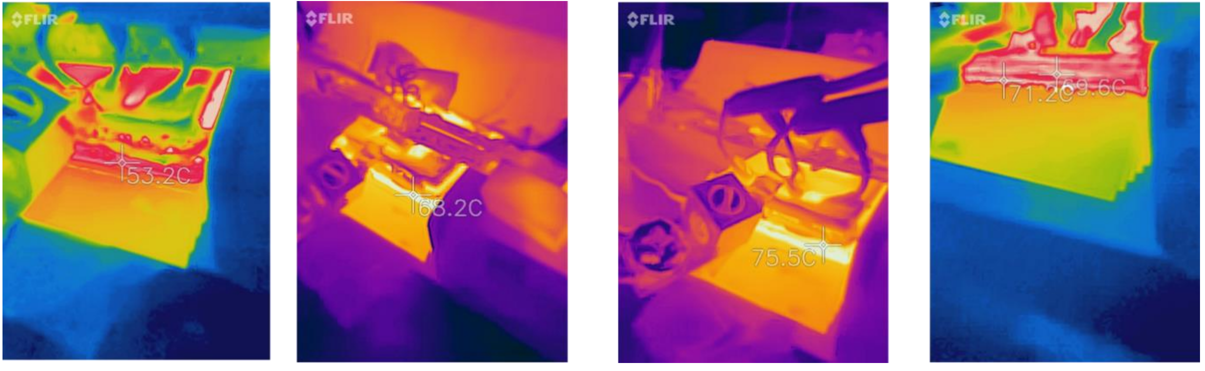


Figure 5-29. Thermal image of modules 4, 6, 8, and 9 at 150 V, 28.3 A input, 300 V, 14.15 A

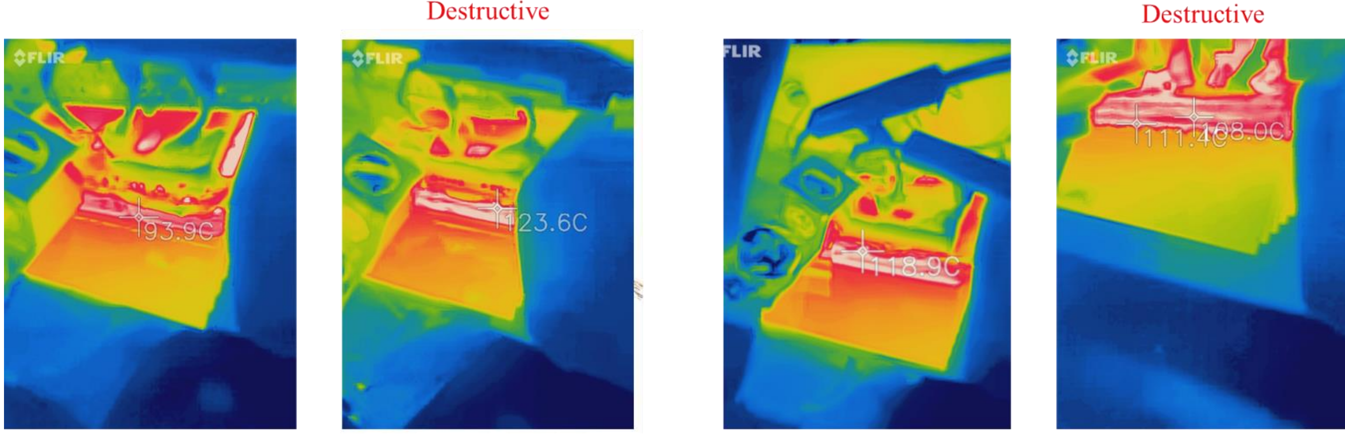


Figure 5-30. Thermal image of modules 4, 6, 8, and 9 at 250 V, 47.7 A input, 400 V, 18.85 A output NOT NECESSARILY AT THERMAL EQILIBRIUM

Figure 5-31. Module 6 after experiencing thermal runaway after 2-3 minutes at 250 V, 47.7 A input, 500 V, 23.86 A output

Ideally, the junction temperature should be measured as close to the dies as possible while still maintaining electrical insulation of the module. Therefore, module 9 is fabricated with insulating spray as opposed to thick silicon encapsulant. Specifically, it has 2 layers of Silicone Conformal Coating (Dielectric) from MG Chemicals then 2 layers of Liquid Tape Spray from Performix (Figure 3-41). In theory, this would allow for monitoring of the temperature for individul dies

because the black coating is non-reflective for the infrared camera. This method did not work well in our test setup. The heat was quickly spread across the entire insulating layer preventing distinguishing the heat generated by the dies (Figure 5-32-Figure 5-33).

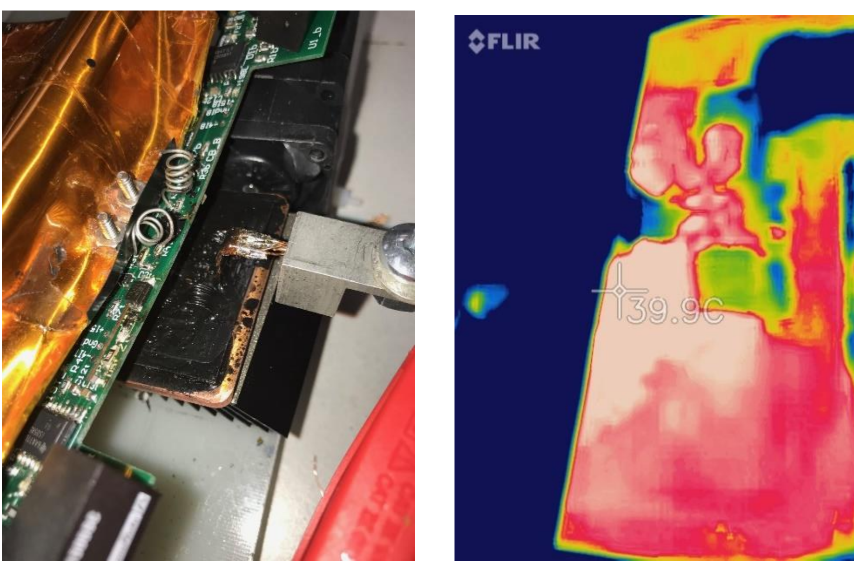


Figure 5-32. Thermal setup and image of module 9 from the side angle run at low power

Figure 5-33. Thermal setup and image of module 9 from the front angle run at low power

Others have managed to achieve favorable results with method so we may not have a large enough resistance to accentuate losses, have too thick of a dielectric layer, or have too much

cooling from the fan [59]. In addition, the liquid tape was placed into the vaccuum as it cured but the cure time is a few minutes as opposed to many minutes or hours for Nusil R-2188 which provides time for the bubbles to come out of the liquid and then resettle flat; the bubbles in the liquid tape created craters that remained after curing. In a paper with successful results, after monitoring the individual surface temperature, there was a 20°C difference which was attributed to fabrication process. The paper did not mention the impact of the parasitic inductances and parametric tolerances on the temperature. Therefore, while this paper does not contribute to understanding the thermal behavior of the modules, it does demonstrate the potential for improving thermal testing.

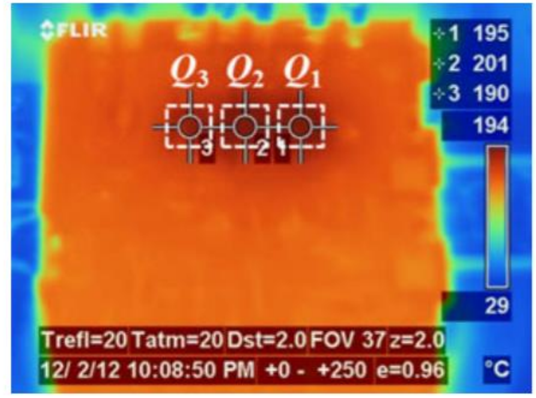


Fig. 28. Thermal map of the module at 560 V and 100 kHz.

Figure 5-34. Thermal performance of paralleled die a high-temperature, high-frequency continuous test

Chapter 6 **Conclusion**

In this paper, a power module is designed with a symmetrical DBC layout in the current pathway to create balanced parasitic inductances in order to evaluate the impact of device parametric tolerances on the electrical and thermal performance. Specifically, the paralleled dies of the half-bridge modules are selected with similar threshold voltages in the balanced module and dissimilar threshold voltages in the unbalanced module. Therefore, the dissimilar paralleled dies will turn on at different times and exhibit unbalanced current sharing. Another design feature is the use of flexible PCB in place of wire bonds for the gate loop interconnection in order to reduce and minimize the gate loop inductance.

Fabrication of the modules is completed within CPES using high-temperature materials with careful attention to the attachment of the flexible PCBs directly to the dies. Many of the fabrication methods are conventional such as ferric chloride etching of the DBC, solder attachment of the terminals and baseplate, and wire bonding of the source interconnection. However, the flexible PCB is attached to the dies' surface which requires nickel: gold topcoat, as opposed to conventional aluminum, modification of the gate and source pad dimensions, and a special fixture while the attachment solder cured. Nine modules are fabricated in total, with a yield of four fully functional modules, two balanced (modules 4 and 6) and two unbalanced (modules 8 and 9).

Static characterization presents the high current capabilities of the SiC MOSFETs which has been reported before. The results validate that the module could conduct current at an expected driving voltage with reduced resistance due to paralleling the devices.

In order to evaluate the electrical performance, the modules are placed into both a clamped inductive DPT and then a continuous, boost converter. A specialized gate driver is designed to interface with the flexible PCB and accommodate Rogowski coils that loop under the wire bonds of the die in the bottom switch position.

Dynamic switching results for the balanced modules demonstrate balanced overshoot and ringing, suggesting balanced parasitic inductances and threshold voltages. Results during the static on-state of the device suggest mismatched on-state resistances with unbalanced current rise; this unbalance during the static on-state is most likely not attributable to unbalanced parasitic inductance. In balanced module 4, there is a mismatch in the overshoot during turn-off which may be attributable to added gate resistance in the flexible PCB or another unidentified source.

Dynamic switching results for the unbalanced modules demonstrates the impact of threshold voltage mismatch on the electrical performance of the modules. In unbalanced module (8) with unbalanced static and dynamic current sharing, die d has higher turn-on loss (~100 μJ) while die C has higher turn-off loss (~20 μJ), so the overall loss differential is small (~60 μJ). In unbalanced module (9) with unbalanced dynamic current sharing and balanced static sharing, die C has higher turn-on (~200 μJ) and turn-off losses (~150 μJ), so the overall loss differential is large (~350 μJ). Therefore, the overall loss differential in unbalanced modules depends on both the static and dynamic current sharing.

To evaluate the thermal performance of each module, they are tested under continuous operation. Four modules perform for at least 10 minutes at 200 V, 37.6 A in a continuous boost converter at 30 kHz. When run at 250 V with 47.7 A (23 A/die), the modules are unable to perform reliably for multiple minutes; improved thermal management is necessary to take full advantage of the high current rating of the dies (140 A @ 25°C). The temperatures for balanced 6, unbalanced 8, and unbalanced 9 are within 2.2°C of one another while balanced module 4 was 20°C lower.

The temperature result for unbalanced 8 does not align with the fact that this module has the lowest energy loss; the module later experienced a destructive short circuit which suggests that it may have been already unreliable at the time of this test. Most likely, the continuous thermal and electrical results for module 8 are not reliable as the behavior is inconsistent with the DPT results and the continuous results for the other modules.

The elevated temperature result for balanced module 6 and ultimately, the destructive thermal runaway is not consistent with the energy losses that were in between modules 4 and 9. The heat sink attachment is an adhesive sheet as opposed to a thicker, more liquid-like thermal interface material; there may have been voids with the adhesive sheet method. X-ray or acoustic imaging of the modules could provide more information on the thermal management reliability but that is not complete yet.

Furthermore, measuring temperature at the edge of the baseplate is not ideal as the heat spreads and is cooler at the edges. In addition, this method does not allow for accurate comparisons of the individual die temperature. The last encapsulation method, using a dielectric spray that is much thinner than the silicon Nusil R-2188, allows for monitoring of temperature closer to the individual dies. However, the temperature appear nearly uniform on the top without any distinguishing areas

for the individual dies. This may be a result of poor curing of the spray with bubbles or not using a high enough gate resistance as others did with a similar method.

In conclusion, the primary research interest for this paper was the impact of device parametric tolerances on the electrical and thermal performance of multichip modules that utilize paralleled dies. A literature review presented a paper that investigated the same question but with discrete devices, not bare dies. Another paper considered the impact of parasitic inductances on the electrical and thermal behavior. This paper was able to observe bare die behavior by intentionally designing the wire bonds to be high enough to use Rogowski coils for current measurement of individual dies; this is not a conventional method and adds additional inductance so would not be used in practice. In order to evaluate the device parametric tolerances, a symmetrical DBC layout was used to ensure balanced parasitic inductances through the paralleled dies; multiple papers have considered different designs to minimize and balance parasitic inductances.

For the unbalanced modules during DPT, a ~17% difference in threshold voltage led to either a 4.52% or 27.3% difference in the overall switching loss. During continuous testing, a ~17% led to either a 9.01% or -30.9% difference. The loss differential was dependent on whether the on-state resistance unbalance compensated some current unbalance. For the balanced modules during DPT, a ~0.5% difference led to either a 5.66% or 2.43% in overall switching loss in the balanced modules while during continuous testing, there was either a -2.26% or -4.31% difference.

The highest loss differential occurred (for both balanced and unbalanced cases), when one die carried more current during turn-on, turn-off, or the static state. If the dies took turns carrying more current because of either the threshold voltage mismatch, possible on-state resistance, or another source of mismatch, the losses could be offset. Therefore, while device parametric tolerances are

inherent, if the higher threshold voltage devices can be paired with devices that have higher on-state resistance, the overall loss differential may perform similarly to well-matched dies.

Comparing balanced module 4 and unbalanced module 9, whose energy loss results are most consistent with the temperature measurements, the unbalanced module had 119.9 μJ more energy loss and was 22.2°C hotter. The unbalanced module dies had worst-case scenario differences in threshold voltage for the batch of dies we received at 17.7% (2.246 V and 2.682 V) so that the temperature difference and loss presented here could be the approximate worst-case design scenario for tolerances in threshold voltage. (The datasheet presents a range of 1.7 V to 3.5 V, a 66% difference. Further research may have to be done on more unbalanced devices to cover the full range of threshold voltage tolerance possible in commercial dies.) Balanced module 6 and unbalance module 8 demonstrated the inconsistency that can occur with developing fabrication techniques, especially related to thermal management. Further research should investigate a more accurate impact of on-state resistance and how the tolerance interacts with the threshold voltage in the electrical and thermal performance of modules. In addition, more accurate temperature measurements as well as fabricating many more modules, would contribute significantly to the research question.

Appendix A Evaluation of an Automated Modeling Tool Applied to New 600 V, 2 A Vertical Gallium Nitride (GaN) Transistors

An accurate subcircuit model allows for circuit design and simulation of switching devices. However, the characterization process is challenging with emerging devices because the physics of the devices' structure are often not fully understood, as is the case with GaN on GaN transistors [85]. The *Power MOSFET Tool* through Synopsys® Saber® utilizes output, transfer, and Rds(on) characteristic curves to predict static and dynamic behavior in various conditions. Therefore, this paper presents a subcircuit of a GaN vertical transistor developed with the *Power MOSFET Tool*. The model is compared against experimental static and dynamic results for this device as a demonstration of its efficacy [86, 87].

Vertical gallium nitride (GaN) transistors hold promise for higher power, frequency, and efficiency compared to Si and laterally configured GaN devices. [85, 86]. A lateral structure is most common in current commercial GaN devices because it utilizes well-understood Si or SiC substrates. In addition, cost and lack of familiarity with GaN substrates limits the benefit of the vertical structure. However, with maturity in GaN substrates, a vertical device would have

advantages over the more common lateral structure including better performance above 600V/100A, efficient chip utilization area, and reduced sensitivity to surface trapping [86, 88].

A lateral structure is most common in current commercial GaN devices because it utilizes well-understood Si or SiC substrates. In addition, cost and lack of familiarity with GaN substrates limits the benefit of the vertical structure. However, with maturity in GaN substrates, a vertical device would have advantages over the more common lateral structure including better performance above 600V/100A, efficient chip utilization area, and reduced sensitivity to surface trapping [86-88].

Figure A-1 provides an approximate visualization of a vertically oriented MOSFET. A full description of the vertical GaN fabrication process is available in [88]. The specific gate structure in this study is the trench MOSFET which is advantageous for its high packing density and subsequent low on-resistance [62, 89].

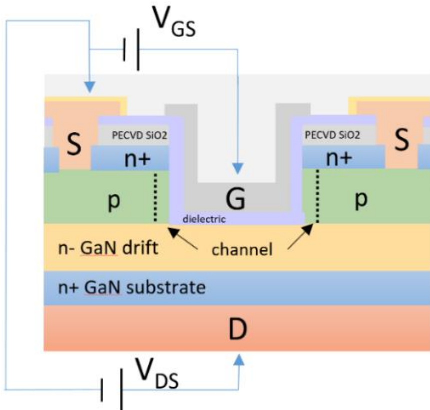


Figure A-1. Approximate Vertical Trench MOSFET Structure

As vertical GaN develops, it is helpful to have a subcircuit model because it provides access to model parameters even when the physics of the device structure are less familiar [85]. An accurate subcircuit model can allow for circuit design and simulation of the emerging device. The *Power*

MOSFET Tool through Synopsys® Saber® can estimate static and dynamic behaviors of the device given measured transfer, output, and on-state resistances curves [90]. The tool has demonstrated maturity and accuracy with SiC MOSFET devices [18, 91-93], GaN FET and other GaN-based converters [85, 94], and in modeling the physics of GaN power semiconductor devices [95]. Therefore, this paper presents a subcircuit of a GaN vertical transistor developed with the *Power MOSFET Tool.* The model is compared against the experimental static and dynamic results for this device as a demonstration of its efficacy [86].

(b) MOSFET Subcurcuit Model

The subcircuit model (Figure A-2) produced by Saber includes a MOSFET whose parameters determine the output and transfer characteristics. A body diode models the behavior of the PN junction between the drain and source, including reverse recovery effect. Parasitic capacitances, C_{gd}, C_{gs}, and C_{ds}, as defined in Figure A-4 determine the switching speeds. The lead inductances, L_d, L_g, and L_s, will contribute to the noise in the experimental switching waveforms.

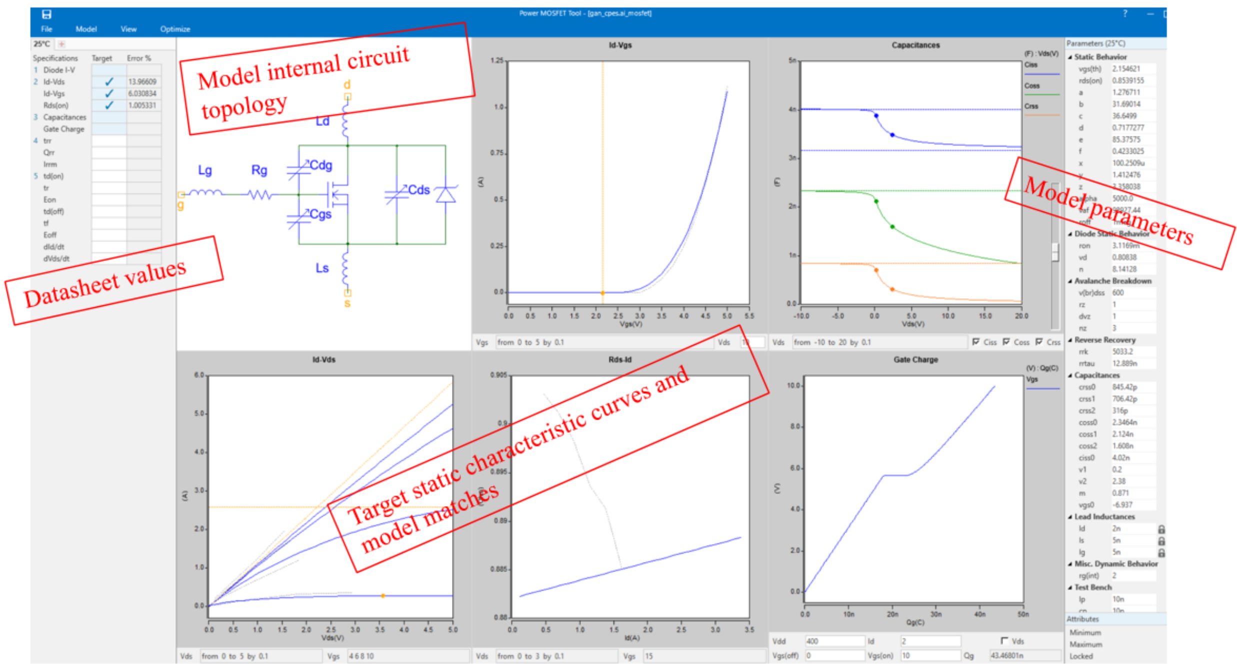


Figure A-2. ***Power MOSFET Tool*** **User Interface with static characteristic curves**

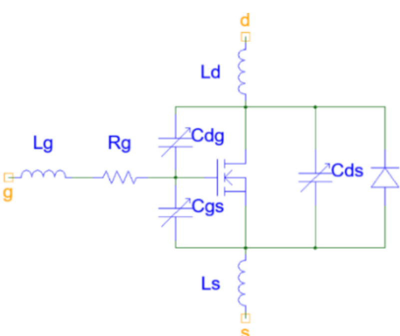


Figure A-3. Saber *Power MOSFET Tool* Subcircuit Model

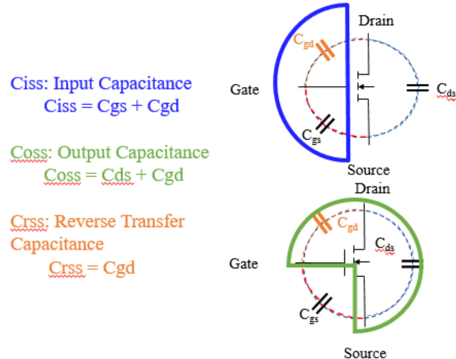


Figure A-4. Device capacitance definitions

(c) Saber Power MOSFET Tool

The user interface of the *Power MOSFET Tool* includes an internal circuit topology of the device model. Gray static curves represent target data imported from an experiment or from a datasheet and superimposed blue curves represent the model (Fig. 3). The parameters determined by the model lie on the right hand side of the interface; the experimental test bench parameters provide a means to more accurately represent the test conditions for the target data and achieve the best match. The switching test produces dynamic waveforms based on the static characteristics of the device. Therefore, in order for the model to work best and estimate the switching behavior, the user should provide output and transfer curves, resistance vs. current, and capacitance measurements [91].

(d) Characterization of Dynamic Behavior

To test the switching behavior, the subcircuit model is placed into an inductive load double-pulse test circuit simulation with lead inductances, and test bench parasitics approximating the experimental setup (Figure A-5).

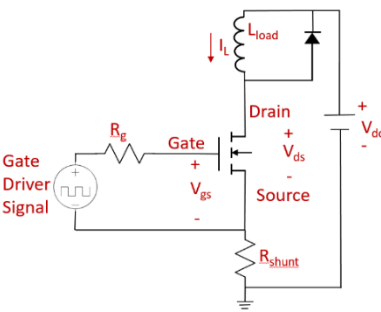


Figure A-5. Double-pulse test schematic

The specialized experimental test setup for this vertical GaN transistor is described in detail in [86]. Highlights of the switching characterization PCB included mounting of the bare die directly to the board and separation of the power and gate loop to reduce gate and power loop inductances, which were 5.5 nH and 12.8 nH respectively. This strategy is particularly important when working with the fast switching times of GaN which could lead to unwanted overshoot and ringing.

The PCB allowed for either a phase leg configuration with another GaN serving as the high-side switch or a freewheeling Schottky diode which was the configuration of choice using the Wolfspeed 600 V, 3 A SiC Schottky diode (CPW3-0600S003).

A 100 µH load inductor was designed for a 5 pF equivalent parallel capacitance (EPC). A 101 mΩ shunt resistor allowed for measurement of the current. The external gate resistance started at 10 Ω and tests were repeated at 5 Ω and 2.5 Ω, the last of which was simulated in the model. An isolated power supply, Recom Power (RSO-2415S) split into 0 V and 8 V supplying the gate driver chip, IXDN614. The bus voltage was tested up to 450 V and 2 A.

When tested at 450 V with a 2 A load current, experimental devices presented 77 V/ns turn-on and 33 V/ns turn-off switching speeds with 8.12 µJ turn-on and 3.04 µJ turn-off losses. Static

characteristics presented a threshold voltage of 3.3 V, 600 V blocking voltage at a 0 V gate bias, with an on –state resistance of 880 mΩ at a 10 V gate bias [86].

(e) SiC Static and Dynamic Modeling

Utilizing the tool for SiC provides an idea of what is possible for materials other than Si. The SiC device under testing was a Monolith/Littelfuse LSIC1MO120E0080 (80 mΩ, 1.2 kV, 20 A). Datasheet static characteristic curves served as target data with the following error as reported by the *Power MOSFET Tool* (Figure A-6-12):

Table 1: SiC Static Modeling Error

	Output	Transfer	Rds (on)	Capacitances	Gate Charge
Error %	3.15	7.92	2.21	10.6	11.3

The mismatch of the transfer curve at high V_{gs} results from the upward slope in the saturation region of the output curves that is characteristic of SiC as opposed to Si behavior with a constant drain current in the saturation region [29] (Figure A-6). The on-state resistance slope as well as Rds initial and final values match well with the experimental data. As demonstrated in past work [18, 85, 92, 94], the SiC MOSFET modeling confirms the tool can work with SiC and accurate modeling of the vertical GaN transistor may be feasible.

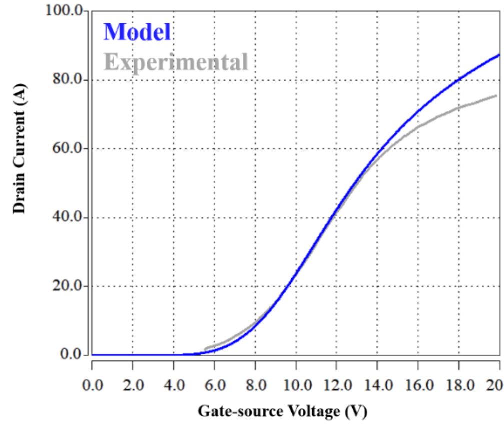


Figure A-6. Saber® (blue) overlaid on experimental (gray) SiC transfer characteristics comparison measured with a drain-source voltage of 1 V at 25°C

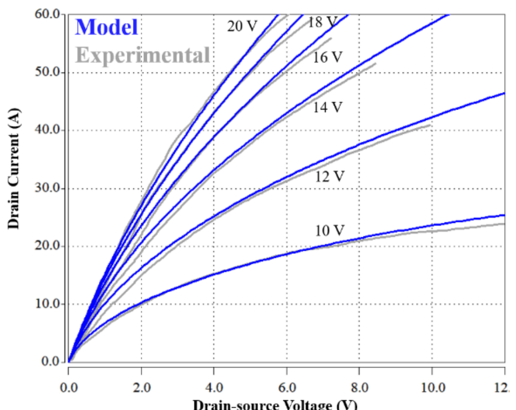


Figure A-7. Saber® (blue) overlaid on experimental (gray) SiC output characteristics comparison measured at various gate-source voltages at 25°C

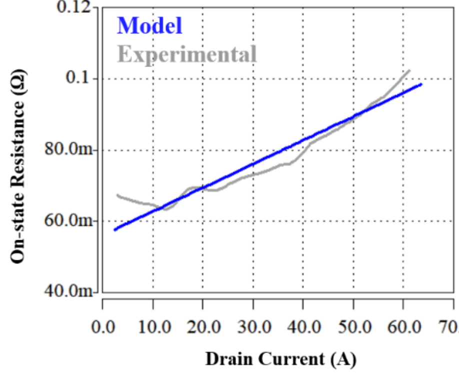


Figure A-8. Saber® (blue) overlaid on experimental (gray) SiC on-state resistance comparison measured with a gate-source voltage of 20 V at 25°C

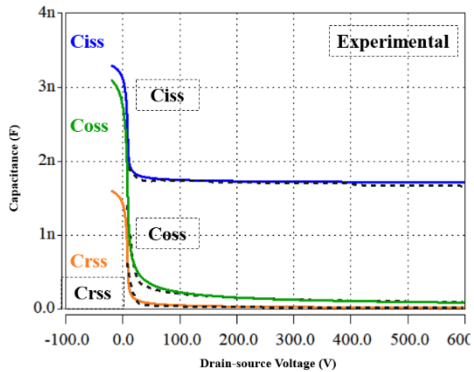


Figure A-9. Saber® (color) overlaid on experimental (dash) SiC capacitance curve comparison at 25°C

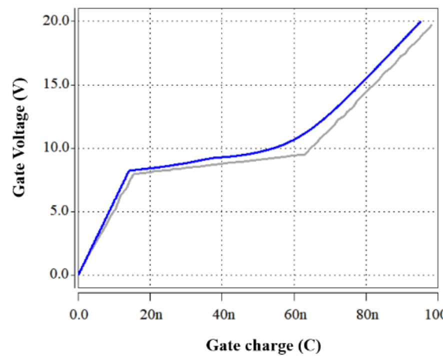


Figure A-10. Saber® (blue) overlaid on experimental (gray) SiC gate charge curve comparison at 25°C

The device was switched at 600 V bus voltage at a 20 A load current. The gate driving voltage ranged from 0 V to 20 V with a 3.01 Ω external gate resistor [96]. The freewheeling device was a Monolith MSA12D10C 1.2 kV, 10 A Schottky diode paralleled with a 1 mH load inductor. A 25.28 mΩ shunt resistor allowed for measurement of the current. When compared to the model switching waveforms, turn on and off times and rates match with insignificant error; the experimental plateau in V_{gs} appears to start a few nanoseconds before the model however, that has a negligible impact on the turn-on time and loss (Figure A-11-14). By optimizing the parasitic elements of the model test circuit, the parasitic ringing for the waveforms matched in frequency and magnitude except for a 100 V difference in the initial overshoot of V_{ds} during turn-off (Figure A-12).

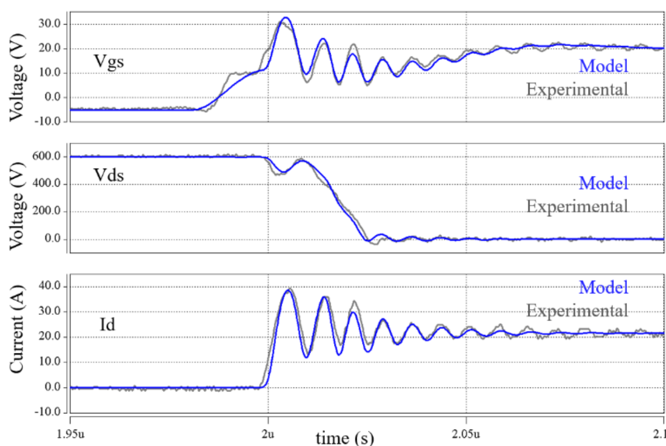


Figure A-11. Saber® (blue) overlaid on experimental (gray) Monolith SiC turn-on waveforms at a drain-source voltage of 600 V, a 20 A load current, and 3.01 Ω gate resistance at 25°C

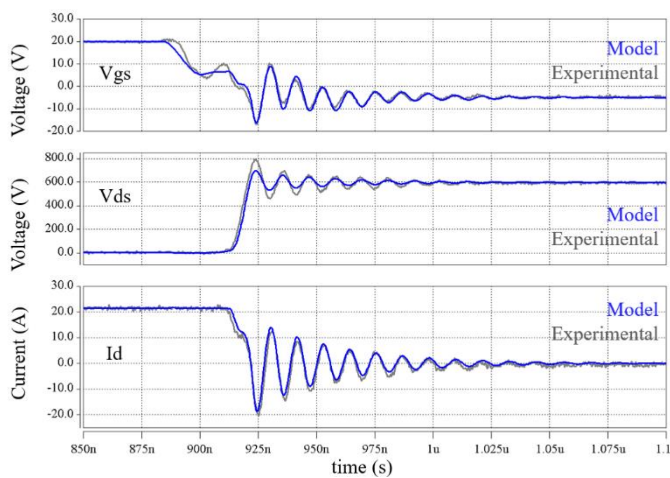


Figure A-12. Saber® (blue) overlaid on experimental (gray) Monolith SiC turn-off at a drain-source voltage of 600 V, a 20 A load current, and 3.01 Ω gate resistance at 25°C

(f) GaN Static Modeling

An initial test with the imported experimental GaN curves produced a transfer curve with 5.98% error and output curves with 9.34% error. Saber® developers suggested removing data points at or below the threshold voltage for the transfer curve, and points or curves near zero in the output curves which reduced the optimization time and the error to 6.13% and 5.41%, respectively [91].

Unfortunately, with the addition of the experimental Rds curve, the error jumped to 8.17% for the transfer curve and 8.42% for the output curves (Figure A-13-16). Furthermore, the Rds curve had a 6.02% error that equates to a value about 100 mΩ less than desired (Figure A-15). This error will not have a significant effect on the switching behavior compared to the impact of the reactive inductances, the stray inductance of the test setup and capacitance of the device.

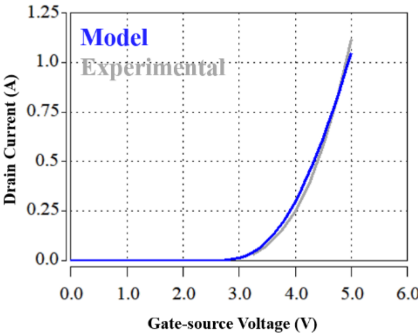


Figure A-13. Saber® (blue) overlaid on experimental (gray) Vertical GaN transfer characteristics comparison measured with a drain-source voltage of 10 V at 25°C

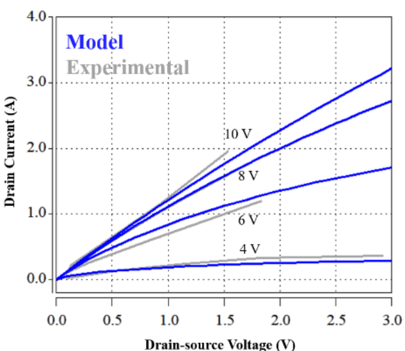


Figure A-14. Saber® (blue) overlaid on experimental (gray) Vertical GaN output characteristics comparison measured at various gate-source voltages at 25°C

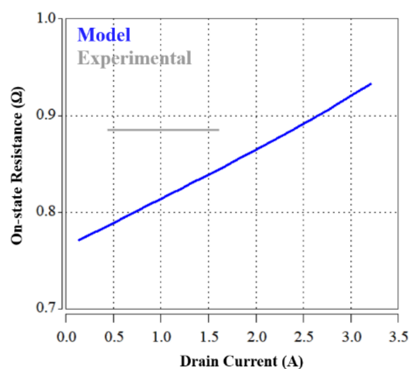


Figure A-15. Saber® (blue) overlaid on experimental (gray) Vertical GaN Rds (on) characteristics comparison measured with a gate-source voltage of 10 V at 25°C

The next step for modeling switching behavior was fitting the experimental capacitance vs. drain-source voltage curves, C-V. Saber® achieved a 17.4% error match for the input, C_{iss}, output, C_{oss}, and reverse transfer, C_{rss}, experimental capacitance curves measured between 0 and 300 V (Figure A-16). The model gate charge curve presents a plateau time, reflective of the C_{iss} value (~200 pF). C_{iss} drops at high V_{ds} as C_{gd} decreases with V_{ds}. The 17.4% mismatch in the data is most likely a result of a layout change between the transistor used for measuring static capacitance and the transistor that was switched experimentally. The study was done throughout the various stages of vertical GaN development and thus, some mismatch is not unexpected. That being said, an experimental gate charge plot would provide further perspective on the capacitance behavior across V_{ds}.

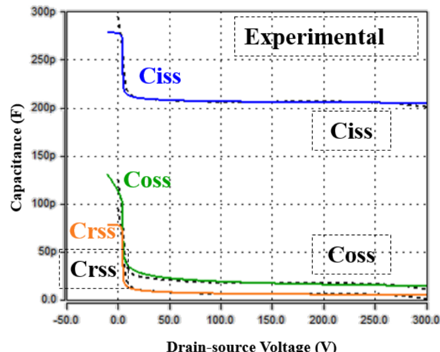


Figure A-16. Saber® (color) overlaid on experimental (dash) Vertical GaN capacitance curve comparison at 25°C

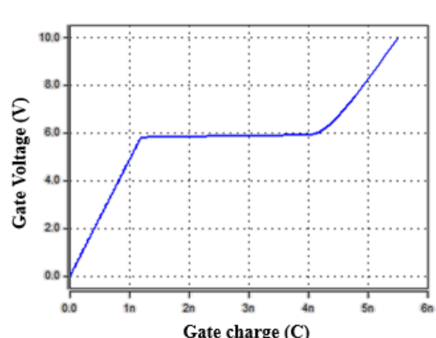


Figure A-17. Saber® Vertical GaN gate charge model curve at 25°C

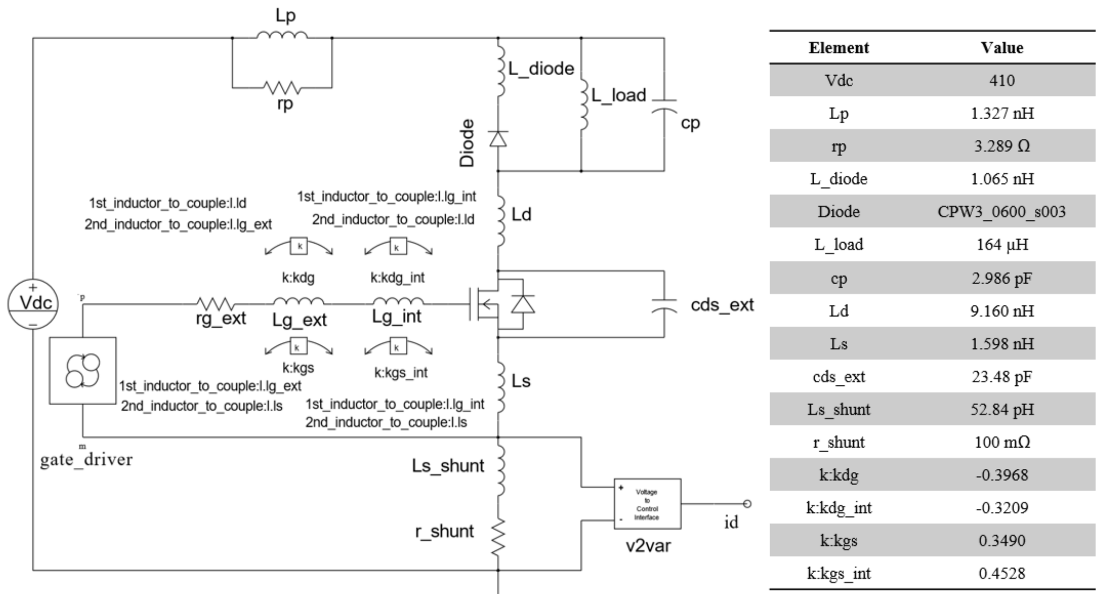
(g) GaN Dynamic Modeling

The model was simulated at 400 V with a 1 A load current and 2.5 Ω external gate resistance (Figure A-18) where the static behavior was defined according to the output, transfer, on-state resistance, capacitance, and gate charge behavior above.

The optimization of the test set up was done outside the Saber® MOSFET tool, using the generic parameter optimization function of Saber®. Minimizing the errors between simulated and measured V_{ds}, V_{gs} and I_d waveforms in the double-pulse test circuit was the target of this multi-objective optimization. Along with the capacitance parameters, parasitic elements in the circuit were also numerically optimized to fit the ringing in the switching waveforms. These parasitic

elements included stray inductances in the power and gate loop, a stray inductance in series with the free-wheeling diode, as well as a damping resistance across the stray inductance of the power loop. The MOSFET model and the external gate resistor were not touched during the optimization of the test setup. Only the parasitic elements were optimized.

An additional external capacitance (23 pF) was optimized to improve the fitting of the experimental switching waveforms. In retrospect, this extra capacitance can be attributed to the test setup or a change in the layout between the devices used for transient measurements and capacitance measurements.



Element	Value
Vdc	410
Lp	1.327 nH
rp	3.289 Ω
L_diode	1.065 nH
Diode	CPW3_0600_s003
L_load	164 μH
cp	2.986 pF
Ld	9.160 nH
Ls	1.598 nH
cds_ext	23.48 pF
Ls_shunt	52.84 pH
r_shunt	100 mΩ
k:kdg	-0.3968
k:kdg_int	-0.3209
k:kgs	0.3490
k:kgs_int	0.4528

Figure A-18. Saber® double pulse test set up with optimized parasitic elements

The experimental turn-on and turn-off time were 8.48 ns and 30.2 ns respectively when measured from 10% V_{gs} to 10% V_{gs} and 90% Vgs to 90% V_{ds}. The model switched in the same time with 1 or 2 ns error (Figure A-19-22). The two primary areas of mismatch were in the negative bias undershoot of V_{ds} during turn on and the amplitude of the ringing in Vgs during turn on (Figure A-19). The cause of the negative V_{ds} dip requires further investigation because of the bizarre nature

of the behavior; reverse recovery behavior from the top side switch was not the cause because a Schottky diode was used for freewheeling the current.

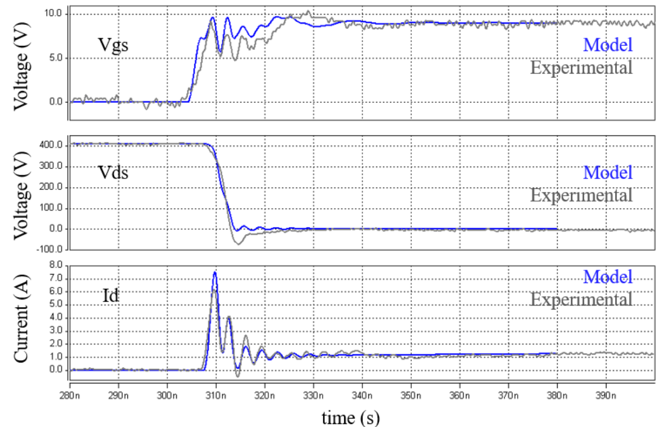


Figure A-19. Saber® (blue) overlaid on experimental (gray) GaN turn-on waveforms with optimized parasitic circuit elements at a drain-source voltage of 400 V, a 1 A load current, and 2.5 Ω gate resistance at 25°C

(h) Conclusion

With optimization of the parasitic elements, the waveforms match with an insignificant error that would not impact the switching times and loss. That being said, improvement is possible with experimental gate charge curves. Furthermore, updating the capacitance optimization models in the *Power MOSFET Tool* to match GaN device theory will also improve the model.

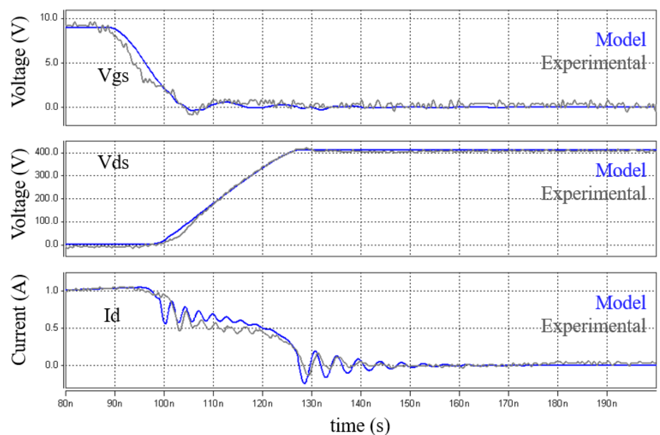


Figure A-20. Saber® (blue) overlaid on experimental (gray) GaN turn-off waveforms with optimized parasitic circuit elements at a drain-source voltage of 400 V, a 1 A load current, and 2.5 Ω gate resistance at 25°C

(i) Summary

This paper demonstrated effective models of wide bandgap devices that accurately simulated switching time and parasitic ringing. The primary investigation compared the experimental and modeled static and dynamic behavior of HRL's 600 V, 2 A vertical GaN transistor. The properties of GaN devices, and more specifically, vertically oriented GaN devices, could allow for efficient performance at high frequency and high power. The experimental turn-on and turn-off times are 8.48 ns and 30.2 ns, demonstrating the potential for high frequency applications with GaN [86]. A model allows for simulation of the device and optimization of its behavior in converters. The *Power MOSFET Tool* through Synopsys® Saber® was used to develop the model.

Firstly, a SiC example indicated that Saber® is effective at creating an accurate subcircuit model when given output, transfer, and on-state resistance curves obtained experimentally or from a datasheet. The SiC static data matched with a maximum error of 11.3% and the dynamic behavior

demonstrated minimal error such the model in a test circuit would produce accurate timing and loss.

The GaN model had a maximum error of 8.42% for output, transfer, and Rds_{on} characteristics. It switched within a couple nanoseconds of the experimental times and the parasitic ringing accurately represented the rise and fall times so the modeled loss and timing would be accurate in test simulation.

A critical methodological finding for model development was the accuracy of parasitic ringing frequency and magnitude afforded by optimizing the parasitic elements in the model circuits. Furthermore, the rates of rise and fall matched more closely with this technique.

Experimentally, the fabricated device yielded a threshold voltage of 4.8 V, 600 V blocking voltage at a 0 V gate bias, with an on-state resistance of 1.7 Ω at a 10 V gate bias [88], although other experimental static testing produced resistances closer to 1 Ω under the same conditions. The device successfully switched up to 450 V under a 2 A load current [86]. The results demonstrate potential with more research on vertical GaN transistors.

(j) Acknowledgment

The authors acknowledge the financial support provided by the U.S. Department of Energy Advanced Manufacturing Office through the Wide Bandgap Generation (WBGen) Fellowship at the Center for Power Electronics Systems (CPES) at Virginia Tech (http://www.eng.vt.edu/WBGen).

The information, data, or work presented herein was funded in part by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award Number DE-

AR000450, Strategies for Wide-Bandgap, Inexpensive Transistors for Controlling High Efficiency Systems (SWITCHES), with HRL Laboratories, LLC., managed by Dr. Isik Kizilyalli.

Monolith SiC MOSFET devices were provided under sub recipient agreement and subsequently referenced device test data in Section V, resulted in part, from work supported by the U.S. Department of Energy, Vehicle Technologies Office (VTO) under Award Number DE-EE-0007285, Highly Integrated Wide Bandgap Power Module for Next Generation Plug-in Vehicles.

Thank you to Alan Courtay and David Norris from Synopsys® for assistance and guidance with the Saber® software and the *Power MOSFET Tool*.

Bibliography

[1] DukeEnergy, "Electric Vehicles Take Charge," *Current Times,*
[2] S. Chakraborty, H.-N. Vu, M. M. Hasan, D.-D. Tran, E. M. Baghdadi, and O. Hegazy, "DC-DC Converter Topologies for Electric Vehicles, Plug-in Hybrid Electric Vehicles and Fast Charging Stations: State of the Art and Future Trends," *Energies,* vol. 12, no. 8, 2019, doi: 10.3390/en12081569.
[3] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-Up DC–DC Converters: A Comprehensive Review of Voltage-Boosting Techniques, Topologies, and Applications," *IEEE Transactions on Power Electronics,* vol. 32, no. 12, pp. 9143-9178, 2017, doi: 10.1109/TPEL.2017.2652318.
[4] J. V. M. a. H. G. Monzer Al Sakka, "DC/DC Converters for Electric Vehicles, Electric Vehicles - Modelling and Simulations, Seref Soylu," *IntechOpen,* September 12, 2011, doi: 10.5772/17048.
[5] M. Hawes, "Emerging Solutions to Hybrid & Electric Vehicle DC:DC Converter Design and Test," *Keysight Technologies, Inc. White Paper,* no. Automotive & Energy Solutions, 2017.
[6] S. Loveday, "December 2018 U.S. Plug-In EV Sales Report Card," *InsideEVs,*
[7] "Global EV Outlook " *International Energy Agency,* 2019.
[8] DukeEnergy. Electric Vehicles [Online] Available: https://www.duke-energy.com/energy-education/energy-savings-and-efficiency/electric-vehicles
[9] Danfoss. "Electric traction inverter for HEVs and EVs." https://www.danfoss.com/en-us/markets/automotive/dsp/electric-traction-inverter-hevev/#tab-overview (accessed.
[10] S. Microelectronics, "Main Inverter (Electric Traction)," 2019.
[11] I. Hofman, P. Sergeant, and A. V. d. Bossche, "Drivetrain design for an ultra light electric vehicle with high efficiency," in *2013 World Electric Vehicle Symposium and Exhibition (EVS27)*, 17-20 Nov. 2013 2013, pp. 1-6, doi: 10.1109/EVS.2013.6914766.
[12] D. Serpa, "TANK TO WHEEL EFFICIENCY," *AfterOilEV,*
[13] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*. Springer Science & Business Media, 2007.
[14] Wikibooks. "Power Electronics." https://en.wikibooks.org/wiki/Power_Electronics (accessed.

[15] Wikipedia. "Power electronics." https://en.wikipedia.org/wiki/Power_electronics (accessed.
[16] K. Nardone and T. Curatolo, "Adaptive Cell Topologies Raise the Bar for DC-DC Converter Performance in EV/HEV Applications," *Vicor Power,* 2019.
[17] C. Gable and S. Gable. "Inverters and Converters in Hybrids and EV (Electric Vehicles)." ThoughtCo. https://www.thoughtco.com/how-inverters-and-converters-work-85612 (accessed.
[18] Z. Chen, "Characterization and Modeling of High-Switching-Speed Behavior of SiC Active Devices," masters thesis 2009.
[19] C. Chen, F. Luo, and Y. Kang, "A review of SiC power module packaging: Layout, material system and integration," *CPSS Transactions on Power Electronics and Applications,* vol. 2, no. 3, pp. 170-186, 2017, doi: 10.24295/CPSSTPEA.2017.00017.
[20] Q. Haihong *et al.*, "Influences of circuit mismatch on paralleling silicon carbide MOSFETs," in *2017 12th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, 18-20 June 2017 2017, pp. 556-561, doi: 10.1109/ICIEA.2017.8282906.
[21] S. Dimitrijev, J. Han, D. Haasmann, H. A. Moghadam, and A. Aminbeidokhti, "Power-switching applications beyond silicon: The status and future prospects of SiC and GaN devices," in *2014 29th International Conference on Microelectronics Proceedings - MIEL 2014*, 12-14 May 2014 2014, pp. 43-46, doi: 10.1109/MIEL.2014.6842083.
[22] H. Wang, F. Wang, A. Q. Huang, and C. W. Tipton, "Investigation of power MOSFETs for high temperature operation," in *Fourtieth IAS Annual Meeting. Conference Record of the 2005 Industry Applications Conference, 2005.*, 2-6 Oct. 2005 2005, vol. 1, pp. 388-392 Vol. 1, doi: 10.1109/IAS.2005.1518337.
[23] Z. Chen, "Electrical Integration of SiC Power Devices for High-Power-Density Applications," Doctor of Philosophy, Electrical Engineering, Virginia Polytechnic Institute and State University, Blacksburg, Virginia, 2013.
[24] MicrosemiPPG, "Gallium Nitride (GaN) versus Silicon Carbide (SiC) In The High Frequency (RF) and Power Switching Applications," 5/11/2010.
[25] N. Kaminski and O. Hilt, "SiC and GaN devices - wide bandgap is not all the same," *IET Circuits, Devices & Systems,* vol. 8, no. 3, pp. 227-236, 2014, doi: 10.1049/iet-cds.2013.0223.
[26] Y. Cui, M. S. Chinthavali, F. Xu, and L. M. Tolbert, "Characterization and modeling of silicon carbide power devices and paralleling operation," in *2012 IEEE International Symposium on Industrial Electronics*, 28-31 May 2012 2012, pp. 228-233, doi: 10.1109/ISIE.2012.6237089.
[27] W. v. Muench and E. Pettenpaul, "Saturated electron drift velocity in 6H silicon carbide," *Journal of Applied Physics,* vol. 48, no. 11, pp. 4823-4825, 1977, doi: 10.1063/1.323506.
[28] A. Courtay. "The Gate Charge Cheat Sheet." https://www.linkedin.com/pulse/gate-charge-cheat-sheet-alan-courtay (accessed.
[29] Z. Chen, D. Boroyevich, and J. Li, "Behavioral comparison of Si and SiC power MOSFETs for high-frequency applications," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 17-21 March 2013 2013, pp. 2453-2460, doi: 10.1109/APEC.2013.6520640.
[30] R. R. Tummala, *Fundamentals of microsystems packaging*. McGraw-Hill Education, 2001.

[31] C. DiMarino, W. Zhang, N. Haryani, Q. Wang, R. Burgos, and D. Boroyevich, "A high-density, high-efficiency 1.2 kV SiC MOSFET module and gate drive circuit," in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 7-9 Nov. 2016 2016, pp. 47-52, doi: 10.1109/WiPDA.2016.7799908.

[32] Y. Wang, Y. Wu, X. Dai, S. Jones, and G. Liu, "Reliability Design for Automotive Power Modules," in *PCIM Asia 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 24-26 June 2015 2015, pp. 1-8.

[33] C. DiMarino, W. Zhang, R. Burgos, and D. Boroyevich, "Design of a high-density, diode-less 1.2 kV, 90 A SiC MOSFET half-bridge power module," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2-4 Nov. 2015 2015, pp. 210-214, doi: 10.1109/WiPDA.2015.7369278.

[34] S. Bęczkowski, A. B. Jørgensen, H. Li, C. Uhrenfeldt, X. Dai, and S. Munk-Nielsen, "Switching current imbalance mitigation in power modules with parallel connected SiC MOSFETs," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, 11-14 Sept. 2017 2017, pp. P.1-P.8, doi: 10.23919/EPE17ECCEEurope.2017.8099245.

[35] Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock, and F. Wang, "Active current balancing for parallel-connected silicon carbide MOSFETs," in *2013 IEEE Energy Conversion Congress and Exposition*, 15-19 Sept. 2013 2013, pp. 1563-1569, doi: 10.1109/ECCE.2013.6646891.

[36] D. Sadik, J. Colmenares, D. Peftitsis, J. Lim, J. Rabkowski, and H. Nee, "Experimental investigations of static and transient current sharing of parallel-connected silicon carbide MOSFETs," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2-6 Sept. 2013 2013, pp. 1-10, doi: 10.1109/EPE.2013.6634432.

[37] M. Wang, F. Luo, and L. Xu, "A Double-End Sourced Wire-Bonded Multichip SiC MOSFET Power Module With Improved Dynamic Current Sharing," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 5, no. 4, pp. 1828-1836, 2017, doi: 10.1109/JESTPE.2017.2720731.

[38] InternationalRectifier, "PARALLELING POWER MOSFETs,"

[39] G. Regnat, P. Jeannin, D. Frey, J. Ewanchuk, S. V. Mollov, and J. Ferrieux, "Optimized Power Modules for Silicon Carbide <sc>mosfet</sc>," *IEEE Transactions on Industry Applications,* vol. 54, no. 2, pp. 1634-1644, 2018, doi: 10.1109/TIA.2017.2784802.

[40] P. Beckedahl, M. Spang, and O. Tamm, "Breakthrough into the third dimension - Sintered multi layer flex for ultra low inductance power modules," in *CIPS 2014; 8th International Conference on Integrated Power Electronics Systems*, 25-27 Feb. 2014 2014, pp. 1-5.

[41] L. Stevanovic, "Packaging challenges and solutions for silicon carbide power electronic," presented at the ECTC Panel Session: Power Electronics – A Booming Market, San Diego, CA, 2012. [Online]. Available: http://www.ectc.net/files/62/3_2_Stevanovic_GE.pdf.

[42] M. Meisser, D. Hamilton, T. Blank, and P. Mawby, "Low-inductive compact SiC power modules for high-frequency operation," in *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 20-22 May 2014 2014, pp. 1-8.

[43] B. N. An *et al.*, "A highly integrated copper sintered SiC power module for fast switching operation," in *2018 International Conference on Electronics Packaging and iMAPS All Asia Conference (ICEP-IAAC)*, 17-21 April 2018 2018, pp. 375-380, doi: 10.23919/ICEP.2018.8374327.
[44] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Gate-Drive Considerations for Silicon Carbide FET-Based Half-Bridge Circuits," presented at the PCIM Europe, Nuremberg, Germany, 2013, 311-318.
[45] G. Watt, A. Romero, R. Burgos, and M. Jaksic, "Design of a Compact, Low Inductance 1200 V, 6.5 mΩ SiC Half-Bridge Power Module with Flexible PCB Gate Loop Connection," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 17-21 March 2019 2019, pp. 2786-2793, doi: 10.1109/APEC.2019.8722138.
[46] S. Kicin *et al.*, "Full SiC half-bridge module for high frequency and high temperature operation," in *2015 IEEE 65th Electronic Components and Technology Conference (ECTC)*, 26-29 May 2015 2015, pp. 950-956, doi: 10.1109/ECTC.2015.7159709.
[47] L. Zhang, P. Liu, A. Q. Huang, S. Guo, and R. Yu, "An improved SiC MOSFET-gate driver integrated power module with ultra low stray inductances," in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 30 Oct.-1 Nov. 2017 2017, pp. 342-345, doi: 10.1109/WiPDA.2017.8170570.
[48] W. Grant and J. Polack, "ELECTRONIC HALF BRIDGE MODULE," Patent Appl. 09/494,563, 2001.
[49] B. Passmore *et al.*, "A 650 V/150 A enhancement mode GaN-based half-bridge power module for high frequency power conversion systems," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 20-24 Sept. 2015 2015, pp. 4520-4524, doi: 10.1109/ECCE.2015.7310298.
[50] J. Marchesini, P. Jeannin, Y. Avenas, J. Delaine, C. Buttay, and R. Riva, "Implementation and Switching Behavior of a PCB-DBC IGBT Module Based on the Power Chip-on-Chip 3-D Concept," *IEEE Transactions on Industry Applications,* vol. 53, no. 1, pp. 362-370, 2017, doi: 10.1109/TIA.2016.2604379.
[51] G. Regnat *et al.*, "Silicon carbide power chip on chip module based on embedded die technology with paralleled dies," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 20-24 Sept. 2015 2015, pp. 4913-4919, doi: 10.1109/ECCE.2015.7310353.
[52] K. Takao, T. Shinohe, T. Yamamoto, K. Hasegawa, and M. Ishida, "1200 V-360 A SiC Power Module with Phase Leg Clustering Concept for Low Parasitic Inductance and High Speed Switching," in *CIPS 2014; 8th International Conference on Integrated Power Electronics Systems*, 25-27 Feb. 2014 2014, pp. 1-7.
[53] S. Hatsukawaa, S. Toyoshima, T. Tsuno, and Y. Mikamura, "Newly Developed Switching Analysis Method for 3.3 kV 400 A Full SiC Module," *Materials Science Forum,* vol. 858, pp. 1099-1102, 2016.
[54] H. Li, S. Munk-Nielsen, S. Bęczkowski, and X. Wang, "A Novel DBC Layout for Current Imbalance Mitigation in SiC MOSFET Multichip Power Modules," *IEEE Transactions on Power Electronics,* vol. 31, no. 12, pp. 8042-8045, 2016, doi: 10.1109/TPEL.2016.2562030.
[55] Toshiba, "Parasitic Oscillation and Ringing of Power MOSFETs,"

[56] M. Olszewski, "HIGH-TEMPERATURE HIGH-POWER PACKAGING TECHNIQUES FOR HEV TRACTION APPLICATIONS," Department of Electrical & Computer Engineering
University of Idaho, 2007. [Online]. Available: https://www.osti.gov/servlets/purl/921886
[57] U. Scheuermann, "Reliability of Planar SKiN Interconnect Technology," in *2012 7th International Conference on Integrated Power Electronics Systems (CIPS)*, 6-8 March 2012 2012, pp. 1-8.
[58] R. Zheng *et al.*, "Online Aging Parameter Extraction with Induced Voltage v_{eE} between Kelvin and Power Emitter in Turn-off Progress for IGBT Modules," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 23-27 Sept. 2018 2018, pp. 362-366, doi: 10.1109/ECCE.2018.8557554.
[59] Z. Chen, Y. Yao, D. Boroyevich, K. D. T. Ngo, P. Mattavelli, and K. Rajashekara, "A 1200-V, 60-A SiC MOSFET Multichip Phase-Leg Module for High-Temperature, High-Frequency Applications," *IEEE Transactions on Power Electronics,* vol. 29, no. 5, pp. 2307-2320, 2014, doi: 10.1109/TPEL.2013.2283245.
[60] T. Funaki, M. Matsushita, M. Sasagawa, T. Kimoto, and T. Hikihara, "A Study on SiC Devices in Synchronous Rectification of DC-DC Converter," in *APEC 07 - Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition*, 25 Feb.-1 March 2007 2007, pp. 339-344, doi: 10.1109/APEX.2007.357536.
[61] X. Hou, D. Boroyevich, and R. Burgos, "Characterization on latest-generation SiC MOSFET's body diode," in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 7-9 Nov. 2016 2016, pp. 247-252, doi: 10.1109/WiPDA.2016.7799947.
[62] B. Hull *et al.*, "Reliability and stability of SiC power mosfets and next-generation SiC MOSFETs," in *2014 IEEE Workshop on Wide Bandgap Power Devices and Applications*, 13-15 Oct. 2014 2014, pp. 139-142, doi: 10.1109/WiPDA.2014.6964641.
[63] A. Agarwal, H. Fatima, S. Haney, and S. Ryu, "A New Degradation Mechanism in High-Voltage SiC Power MOSFETs," *IEEE Electron Device Letters,* vol. 28, no. 7, pp. 587-589, 2007, doi: 10.1109/LED.2007.897861.
[64] W. W. Sheng and R. P. Colino, *Power electronic modules: design and manufacture*, 1 ed. Boca Raton: CRC Press, 2005.
[65] Y. Mei, Y. Cao, G. Chen, X. Li, G. Lu, and X. Chen, "Rapid Sintering Nanosilver Joint by Pulse Current for Power Electronics Packaging," *IEEE Transactions on Device and Materials Reliability,* vol. 13, no. 1, pp. 258-265, 2013, doi: 10.1109/TDMR.2012.2237552.
[66] K. S. Siow, *Journal of Alloys and Compounds,* vol. 514, pp. 6-19, Feb 2011.
[67] H. Yu, L. Li, and Y. Zhang, "Silver nanoparticle-based thermal interface materials with ultra-low thermal resistance for power electronics applications," *Scripta Materialia,* vol. 66, pp. 931-934, Jun 2012.
[68] P. Zhang, R. Wei, J. Zeng, M. Cai, J. Xiao, and D. Yang, "Thermal Properties of Silver Nanoparticle Sintering Bonding Paste for High-Power LED Packaging," *Journal of Nanomaterials,* vol. 2016,, no. Article ID 8681513, p. 6, 2016, doi: http://dx.doi.org/10.1155/2016/8681513.
[69] AIMsolder, "RMA258-15R

SN96.3/Ag3.7,"
[70] Kester, "Alloy Temperature Chart,"
[71] Vishay, "Recommended Soldering Profiles."
[72] https://rapidmanufacturing.com/typical-part/sheet-metal-busbars/ (accessed.
[73] "Trace Width Calculator." https://www.7pcb.com/trace-width-calculator.php (accessed.
[74] "ATS-56005-C3-R0 Datasheet." https://www.qats.com/DataSheet/HSDS_ATS-56005-C3-R0 (accessed.
[75] "Air Flow Calculator." https://www.engineering.com/calculators/airflow.htm (accessed.
[76] "PF40561BX-000U-S99 Datasheet." https://media.digikey.com/pdf/Data%20Sheets/Sunon%20PDFs/PF40561BX-000U-S99_Spec.pdf (accessed.
[77] M. C. A. Materials. "Duratron® PEI." https://www.mcam.com/na-en/products/engineering-plastics/advanced-325-425-f/duratronr-pei/ (accessed.
[78] J. Wang, Z. Shen, C. DiMarino, R. Burgos, and D. Boroyevich, "Gate driver design for 1.7kV SiC MOSFET module with Rogowski current sensor for shortcircuit protection," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 20-24 March 2016 2016, pp. 516-523, doi: 10.1109/APEC.2016.7467921.
[79] T. Instruments, "Understanding the short circuit protection for silicon carbide MOSFETs," *TI TechNotes*, vol. SLUA863A–January 2018–Revised March 2019,
[80] T. I. Incorporated, "ISO5451 High-CMTI 2.5-A and 5-A Isolated IGBT, MOSFET Gate Driver datasheet (Rev. C)," no. SLLSEO1C, 2017.
[81] P. Integrations. *SID11x2K SCALE-iDriver Family, Short-Circuit Protection*, vol. Rev. G 05/18, 2018.
[82] A. Technologies, "4.0 Amp Gate Drive Optocoupler with Integrated (VCE) Desaturation Detection, Active Miller Clamping, Fault and UVLO Status Feedback," *ACPL-337J Datasheet,* vol. AV02-4390EN, 2014.
[83] Wolfspeed. "Silicon Carbide Power MOSFET
C3M Planar MOSFET Technology
N-Channel Enhancement Mode." https://www.wolfspeed.com/power/products/sic-mosfets/cpm3-1200-0013a (accessed.
[84] A. B. Lostetter, F. Barlow, and A. Elshabini, "An overview to integrated power module design for high power electronics packaging," *Microelectronics Reliability,* vol. 40, pp. 365-379, 03/01 2000, doi: 10.1016/S0026-2714(99)00219-X.
[85] G. H. Aghdam, "Model characterization and performance evaluation of GaN FET in DC-DC POL regulators," in *2015 IEEE International Telecommunications Energy Conference (INTELEC)*, 18-22 Oct. 2015 2015, pp. 1-4, doi: 10.1109/INTLEC.2015.7572432.
[86] A. Romero *et al.*, "Static and dynamic characterization of a GaN-on-GaN 600 V, 2 a vertical transistor," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 1-5 Oct. 2017 2017, pp. 413-418, doi: 10.1109/ECCE.2017.8095812.
[87] G. Watt, A. Courtay, A. Romero, R. Burgos, R. Chu, and D. Boroyevich, "Evaluation of an Automated Modeling Tool Applied to New 600 V, 2 A Vertical GaN Transistors," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 17-21 March 2019 2019, pp. 2920-2927, doi: 10.1109/APEC.2019.8721880.

[88] R. Li, Y. Cao, M. Chen, and R. Chu, "600 V/1.7 Ohm Normally-Off GaN Vertical Trench Metal-Oxide-Semiconductor Field-Effect Transistor," *IEEE Electron Device Letters,* vol. 37, no. 11, pp. 1466-1469, 2016, doi: 10.1109/LED.2016.2614515.

[89] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. New York, NY: Springer Science, 2008.

[90] "Saber Synopsys Webpage." https://www.synopsys.com/verification/virtual-prototyping/saber.html (accessed.

[91] CPES, "CPES-APEI Final Report," 2009.

[92] J. M. Ortiz-Rodriguez, T. Duong, A. Rivera-Lopez, and A. R. Hefner, "High-Voltage, High-Frequency SiC Power MOSFETs Model Validation," in *2007 IEEE Power Electronics Specialists Conference*, 17-21 June 2007 2007, pp. 1018-1022, doi: 10.1109/PESC.2007.4342130.

[93] T. R. McNutt, A. R. Hefner, H. A. Mantooth, D. Berning, and S. H. Ryu, "Silicon Carbide Power MOSFET Model and Parameter Extraction Sequence," *IEEE Transactions on Power Electronics,* vol. 22, no. 2, pp. 353-363, 2007, doi: 10.1109/TPEL.2006.889890.

[94] B. H. R. Khanna, W. Stanchina, R. Chu, K. Boutros, and G. Reed PY, "Modeling and characterization of a 300 V GaN based boost converter with 96% efficiency at 1 MHz," *2014 IEEE Energy Conversion Congress and Exposition (ECCE),* no. SN - 2329-3721, 2014, doi: DO - 10.1109/ECCE.2014.6953380.

[95] R. M. Kotecha, "A physics-based compact device model for GaN HEMT power devices," 2016: IEEE, pp. 108-113, doi: 10.1109/WiPDA.2016.7799919.

[96] A. Marzoughi, A. Romero, R. Burgos, and D. Boroyevich, "Comparing the State-of-the-Art SiC MOSFETs: Test results reveal characteristics of four major manufacturers? 900-V and 1.2-kV SiC devices," *IEEE Power Electronics Magazine,* vol. 4, no. 2, pp. 36-45, 2017, doi: 10.1109/MPEL.2017.2692309.