The Investigation of Inorganic Co Based ReRAM Devices and Organic Cu Doped PANI-CSA Top Electrode Based ReRAM Devices

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Academic Abstract

Recently, the resistance switching random access memory (ReRAM) in several MIM systems has been studied extensively for applications to the next generation non-volatile memory (NVM) devices and memristors since the scaling of conventional memories based on floating gate MOSFETs is getting increasingly difficult. ReRAM is being considered one of the most promising candidates for next generation non-volatile memory due to its relatively high switching speed, superior scalability, low power consumption, good retention and simple fabrication method. Cu/TaO_X/Pt resistive switching device is a very good candidate due to its well performance and well characterization. However, since platinum (Pt) acting as the inert electrode is not economical efficient for industrial production, a compatible replacement of Pt is highly desirable. The device property of Co based resistive switching devices has been explored in this work. Compared with Pt devices, electric characterization of the fabricated Cu/TaO_X/Co devices exhibits very similar FORM, SET and RESET voltages for Cu conductive filaments. However, for the oxygen vacancy (V_O) filament the Co device has a significant smaller FORM, SET and RESET voltages of V_O filament, which can be partly attributed to the work function difference between Pt and Co of 1.35 V and partly to the impaired integrity properties of Co vs Pt inert electrode. The limit of SET-RESET operations is mainly due to the geometrical shape of the Cu conductive filament is more cylindered rather than Cone-like shape as well as the high Joules heat dissipation. What's more, ReRAM is also the most promising candidate for a flexible memory, as

a variety of materials can be used both inorganics, organics and even hybrid nanocomposites. Besides inorganic ReRAM device, we also fabricated an organic ReRAM device with the structure Cu doped PANI-CSA/O-AA/Al. We have manufactured ReRAM based on Cu-doped PANI-CSA polymer electrode, O-AA as the polymer solid electrolyte and Al as the bottom electrode for the first time. This polymer device shows a significantly lower forming voltage than inorganic ReRAM devices such as $Cu/TaO_X/Pt$. Our results also demonstrate that our organic ReRAM is a promising candidate for inexpensive candidate for inexpensive and environmentally friendly memory devices. We have demonstrated that the FORM operation of the polymer devices depends on the concentration of Cu^+ ions as well as the thickness of the polymer electrode.

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General Audience Abstract

Although the scaling of conventional memories such as volatile dynamic random access memory (DRAM) and non-volatile flash technology is becoming increasingly difficult, new types of non-volatile memories, such as resistive switching memories, have recently attracted the attention of both industry and academia. Resistive switching memory is considered as the next generation non-volatile memory because of its excellent scalability, high switching speed, simple structure and low power consumption. What's more, ReRAM is also a promising candidate for a flexible memory, as a variety of materials can be used both inorganics, organics and even hybrid nanocomposites. ReRAM shows unique nanoionics based filamentary switching mechanism. Besides the nonvolatile memory applications, resistive switching devices implement the formation of a memristor, which is the fourth basic electrical component and can be used for neuromorphic computing.

First, we report the device property of Co based resistive switching devices with a structure of Cu/TaO_X/Co layers. The I-V characteristics of the manufactured Cu/TaO_X/Co devices shows very similar FORM, SET and RESET voltages for Cu conductive filaments compared with Pt device. However, the Co device has a significant smaller FORM, SET and RESET voltages for oxygen vacancy (V_O) filaments, which can be partly attributed to the work function difference between Pt and Co of 13.5 eV and partly to the impaired integrity properties of Co vs Pt inert electrode. The main reason for the limit of SET-RESET operations is that high Joules heat dissipation. With

high Joules heat accumulation, the maximum switching cycles of Co devices is up to 8 times, while in the case of Pt cases, it is almost unlimited.

Secondly, we fabricated an organic ReRAM device with the structure Cu-doped PANI-CSA/O-AA/Al. Cu-doped PANI-CSA polymer electrode has been introduced for the first time as the top polymer electrode of a ReRAM device. Compared to inorganic ReRAM device, this polymer device can be operated at a significantly lower forming voltage than inorganic devices such as $Cu/TaO_X/Pt$. We have demonstrated that our organic ReRAM is a promising candidate for environmentally friendly and flexible memory devices. Our results demonstrate the FORM operation of the polymer devices depend on the concentration of Cu^+ ions as well as the thickness of the polymer top layer.

This thesis is dedicated

To my parents Bingyan Li (李炳炎) and Hanying Zhou (周含英)

To my sister Hui Li (李蕙)

To my girlfriend Chen Song (宋晨)

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Chapter1

Introduction

Since the very beginning of human beings, people desperately desired to use a variety of media to preserve knowledge and information and pass it on to the future generations. Memory is the object used to store information and prevent it from disappearing over a period of millions of years. From ancient times to modern high-tech era, humans have come a long way toward the emergence of storage system, which is probably one of the most significant milestones in the history of human civilization. In the new Stone Age, ancient human learned to record the information by painting on the interior walls and ceilings of caves (Lascaux, France).[1] After the invention of words and characteristics, ancient Egyptians and Chinese wrote words and paints on potteries and ritual bronzes to record events and stories.[2, 3] The acquisition and dissemination of knowledge and information became more convenient after the invention of paper.[4] Subsequently, after the industrial revolution, the impulse to improvement information recording and storage (population census of US government) gave birth to the first punched card data processing equipment.[5] The semiconductor memory is the newest method for human to record everything in society.[6] Overall, in human history, storage media has advanced form cuneiform, knots, hieroglyphs, slates, bronze inscription, paper *etc.* to modern era punch cards, electron tube, magnetic drum memory, magnetic tape, Hard Disk Drive (HDD), Solid State Drive

(SSD) *etc.*[7, 8] Figure. 1.1 describe the historical evolution of memory along with several key emerging memory technologies.

Figure. 1.1. Evolution of memory.

In the past few decades, semiconductor memory has flourished due to the growing demand for data storage. The current trends of portable electronics require extremely high density, ultra-fast and low power consumption memory. Current trends in Artificial Intelligence (AI), Internet of Things (IOT), Autonomous Vehicle *etc.* have made innovative memory technologies the focus of attention and their demands are unprecedented.[9-11] The current state of the art memories will create a prevailing technical challenge to future development at the current faster rate, as it is rapidly reaching their physical limitation of scaling. Figure. 1.2 (a) and (b) illustrate the scaling trend of logic transistor as well as several generations of intel transistors, respectively.[12] Besides, the memories and logic circuits are placed in separate locations in the current system architecture, where long interconnection lines connect. As a result, the chip takes up more space and there are inherently longer interconnect delays between memory and logic.[13] Therefore, processor subsystem access time delay and higher power consumption of the

memory subsystem are increasingly limiting processor performance. Figure 1.3 shows the trend of Interconnect vs Gate delay as the technology scaling. Therefore, in order to ensure continuous increases in speed and reductions in power consumption by several orders of magnitude, it is necessary to adapt to fundamental different and revolutionary changes in the memory subsystem.

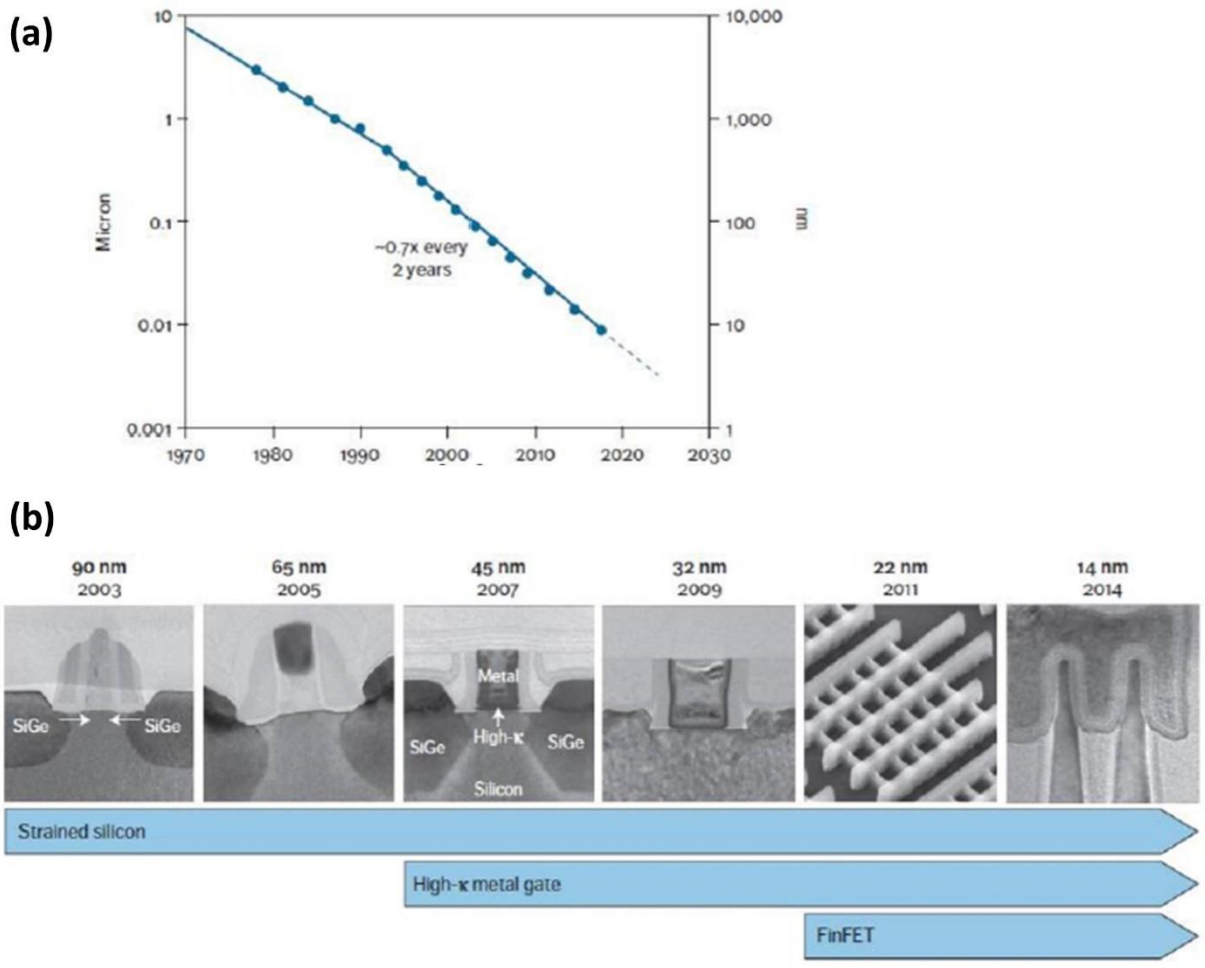

Figure. 1.2. (a) Minimum feature size scaling trend for Intel logic transistors. (b) Several generations of Intel transistors.[12] Reprinted with permission from [12], copyright IEEE (2017)

Recently, remarkable research and progress have been made to develop many innovative technologies to meet the demand for memory systems in the digital age. Many novel memory architectures with new materials have been proposed to continue the growth of the next generation memory. Resistive Switching Memory (ReRAM) is one of the most promising candidates among these various emerging memory technologies. ReRAM technology can potentially solve this problem by vertically integrating memory above the logic into the 'backend' of CMOS. Compared to conventional memory, ReRAM could be an ideal choice for next generation of high-density memory integration due to its excellent scaling capability, ultra-fast switching ability and excellent CMOS compatibility. In this thesis, we investigate and analyze root cause of performance, reliability and durability issues of ReRAM and experimentally demonstrate several possible solutions to significantly improve it functionality.

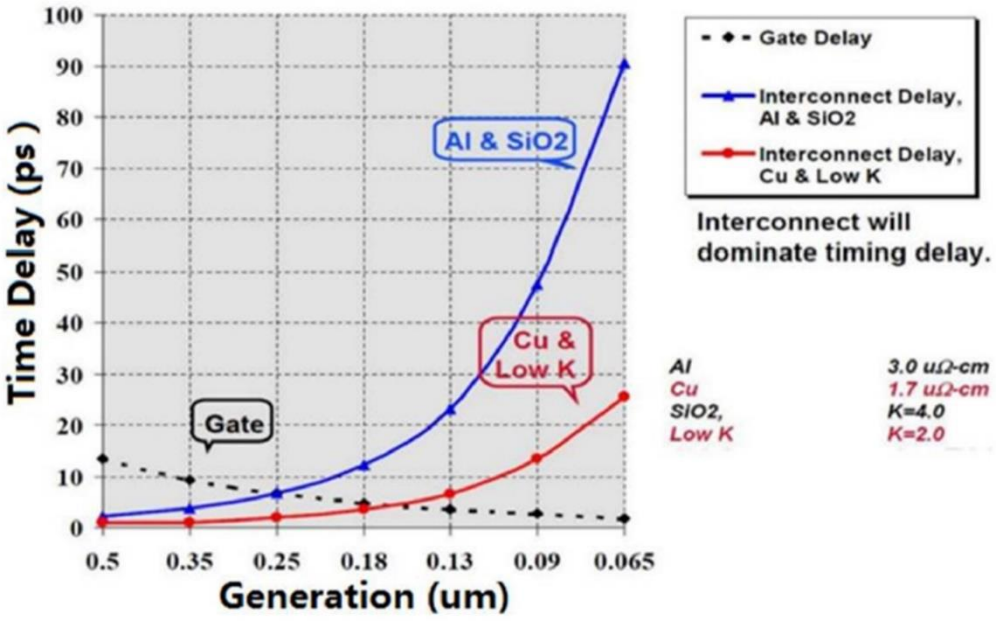

Figure. 1.3. (a) Interconnect vs Gate delay trend with technology scaling.[13] Reprinted with permission from [13], copyright IEEE (1997)

1.1 Semiconductor Memory Technology

Semiconductor memory is a digital electronic semiconductor device used for digital data storage, such as the memory used in computer and cellphone. Since the miniaturization of digital computers in 1970s to 1980s, the development of information technology increased dramatically, which has also increased the demand for semiconductor memory. Semiconductor memories can be divided into two main categories: I. Volatile memory,[14] II. Non-volatile memory.[15]

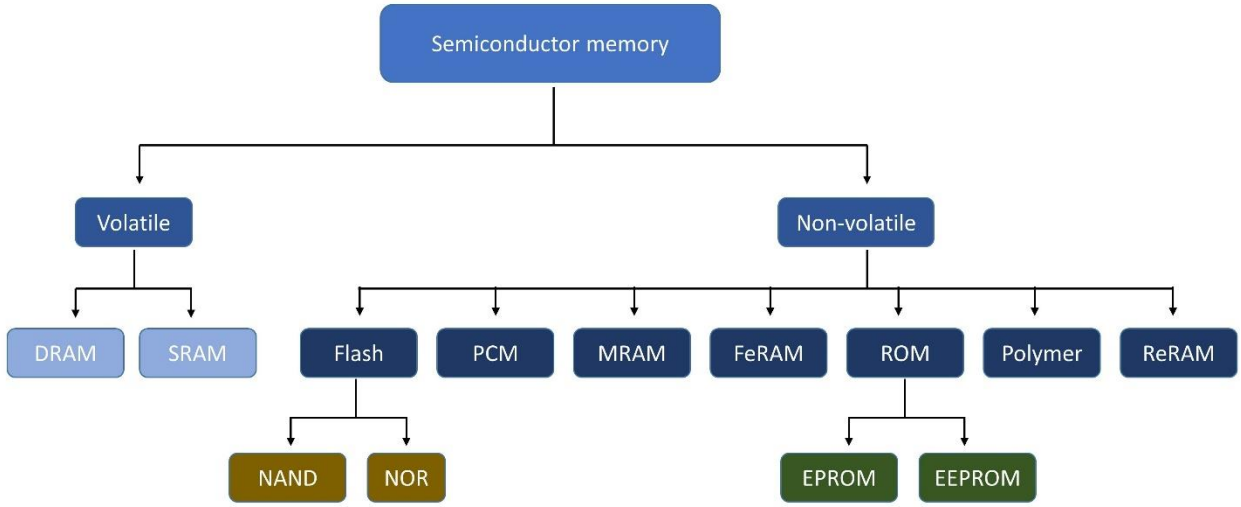

Figure. 1.4. Classification of semiconductor memories.[16]

1.1.1 Volatile Memory

Volatile memory is the type of memory that loses its stored information when the power is turned off. There are two types of volatile memory: Dynamic RAM (DRAM) and Static RAM (SRAM).[14, 17, 18] DRAM stores each bit of information in a single capacitor integrated with one

transistor in the circuit, which makes it space efficient and cheap. On the other hand, DRAM must be refreshed periodically to retain its memory content. Compared to DRAM, SRAM does not require periodic refreshes to retain its stored information and is faster. However, it still requires constant current to sustain the difference in voltage. Each bit in a SRAM chip requires a unit of six transistors, which makes it much more expensive.

1.1.2 Non-volatile Memory

In contrast, non-volatile memory is a type of computer memory that can retrieve stored information even after the power is turned off. The examples of non-volatile memory include flash memory (NAND, NOR), FeRAM, PCM and ReRAM etc.[15, 19-21]

Flash memory is a solid-state chip that maintains stored information without any external power supply. It is an upgraded version of EPROM and EEPROM. In flash memory, the information is stored in the floating gate transistor (or double gate transistor) based memory cell arranged in array pattern. Floating gate is similar to any normal MOSFET except that it has two gates-control gate (CG) and floating gate (FG). By controlling the voltage applied on CG, extra charge can be trapped in FG. Then, the charge trapped in FG can create electron inversion layer and forms a continuous channel between source and drain.

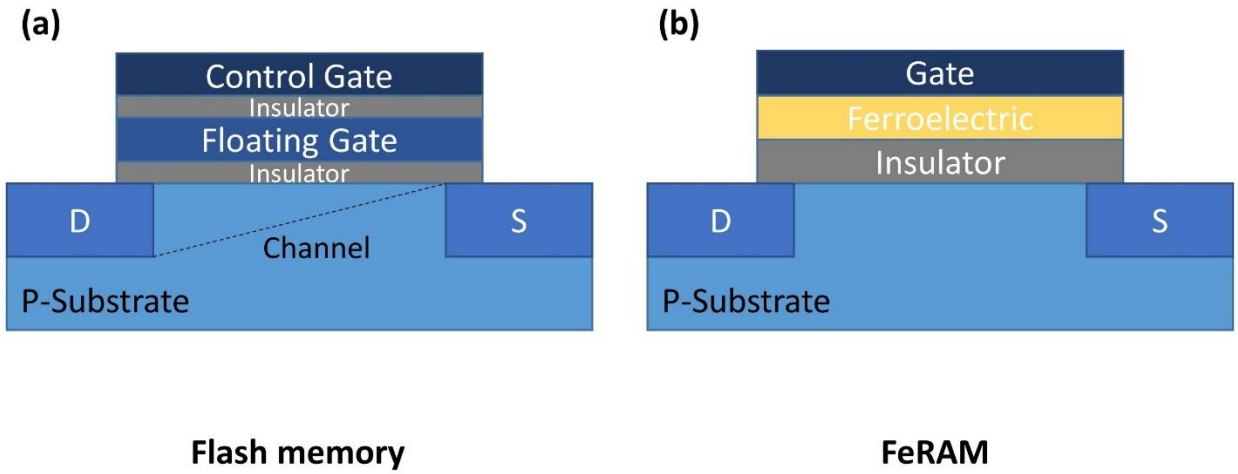

Figure. 1.5. (a) Shematic drawing of flash memory. (b) Schematic drawing of FeRAM.

FeRAM is another non-volatile Random-Access Memory. When an external bias is applied to a ferroelectric material, it will be polarized. Nevertheless, when the electric field is removed, a hysteresis phenomenon will occur between its polarization and electric field characteristics. This polarization characteristic of a ferroelectric material can used to switch between two different ferroelectric states of a capacitor dielectric and therefore store information accordingly.

1.2 Resistive Switching Memory

Resistive switching RAM (ReRAM) based on a resistive switching mechanism offers the potential for co-integration and manufacturing using standard native materials to standard BEOL interconnect.[22-26] ReRAM is a simple two terminal metal-insulator-metal (MIM) device, which is the same as a CMOS metal interconnect system with metal vias being replaced by ReRAM.[27] It is

also due to the compatibility of the materials used to make ReRAM devices with materials and processes used in CMOS backend, that the ReRAM is a prime candidate for non-volatile memory to be integrated with CMOS technology. In many cases the dielectrics such as TaO_X or SiO_2 is sandwiched between the active electrode (Cu, Ag, Ni) and inert electrode (Pt, Ti, Au, W) commonly utilized BEOL interconnects for various purposes.[28-34]

In this section, fundamentals of resistive switching RAM and the switching mechanism of memory devices based on solid electrolytes will be reviewed, following by a review of some basis concept and terminologies about ReRAM.

1.2.1 Fundamentals of Resistive Memory

Non-volatile memory technology plays a very significant role in the market of modern electronics products including computer, portable storage devices, mobile phone and so on. So far, flash memory has dominated the non-volatile memories market, with a market share of more than 90%. Several non-volatile memories based on different concepts have attracted remarkable attention from both of industry and academic fields, such as Resistive RAM (ReRAM), Magnetoresistive RAM (MRAM) and Phase change RAM (PRAM).[20, 21, 35] Compared with other prototypes, ReRAM has relatively high scalability, high switching speed, low power consumption, good retention and simple structure.[36] The device structure of ReRAM is a thin film stack consist of a metal anode, an insulator and a metal cathode, which constitute an electrochemical cell. Conductive bridge RAM (CBRAM) is one type of ReRAM with two metal electrodes made of different materials.[28] Its basic structure is shown in Figure. 1.6. The active

metal can be any oxidizing metal with a moderate ionization energy, such as Cu or Ag, and therefore easily generate Cu^+ and Ag^+ ions, respectively.[29, 30] The solid electrolyte layer allows relatively high mobility of metal ions. SiO_2, Ta_2O_5, TaO_X, $SrTiO_3$, AgGeSe and HfO_2 are available materials that can be used for solid electrolyte.[37-42] The inert metal material is usually Pt, Ir or W, which is characterized by a barrier layer that can efficient block the diffusion of Cu and Ag cations ion to the electrode material. Therefore, the operation of resistive memory depends on ions, and this type of device is also called nano-ionic device.

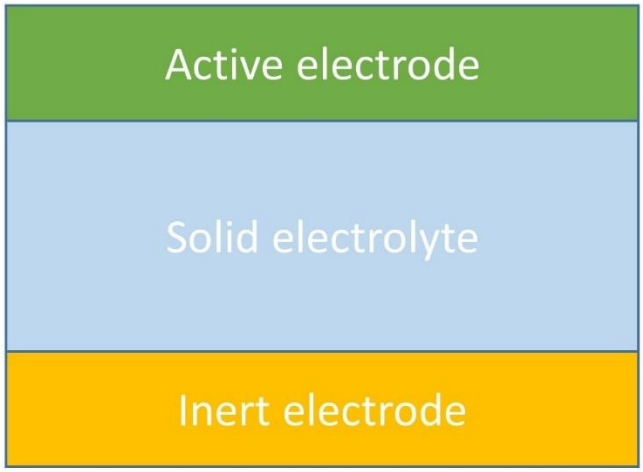

Figure. 1.6. Stack structure of a ReRAM.

Resistive switching memory is a two-terminal non-volatile electrical device that is typically operated by switching between two resistive states.[28] The device operates by applying voltage biases/pulses, which causes a change in the resistance of the material. There are two states: high resistance state (HRS) /off state and low resistance state (LRS) /on state. HRS and LRS can

be expressed as logical values of 0 and 1, respectively. R_{on} is the resistance of the corresponding device in the low resistance state, whose magnitude can be controlled by an external selection of the imposed compliance current I_{CC}. The SET process is the transition from the HRS to the LRS, while the RESET process is the transition from the LRS to the HRS. During the SET and RESET processes, there are threshold voltages, at which the resistance of the device switches more or less abruptly and are called set voltage (V_{SET}) denoting the transition from HRS to LRS, and RESET voltage (V_{RESET}) making the transition from LRS to HRS. Figure. 1.7 illustrates the current flowing through a CBRAM device during the formation, RESET and SET operation. Formation is a specific SET operation performed on a new device (*i.e.* untested device) for the first time.

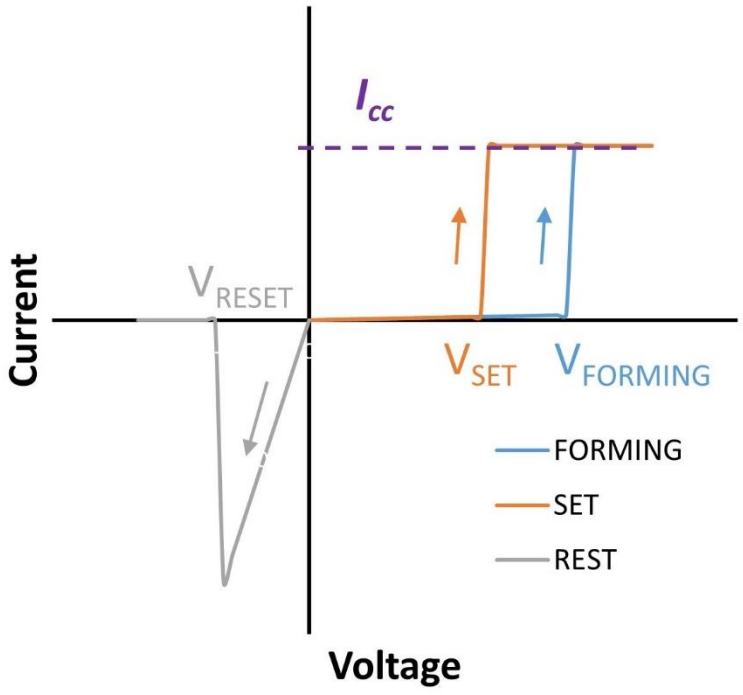

Figure. 1.7. I-V curve of the different operations: FORM, SET and RESET.

In CBRAM, the device in the HRS can be transferred to LRS by applying V_{SET}, while during RESET LRS can be set back to HRS by applying V_{RESET}. Figure. 1.8 shows the schematic diagram of ionic mechanisms of the switching process of a CBRAM device with an inert Pt electrode and an oxidizable Cu electrode. With a positive bias applied to the Cu electrode, Cu ions are ionized at the interface between Cu electrode and the dielectric, and migrate through the solid electrolyte. These ion accumulate at the inert electrode interface due to its stopping power. The accumulated ions nucleate and grow to form a nanoscale metallic conductive filament (CF) that eventually connects both electrodes. Due to a short circuit between top and bottom electrodes, the initially highly resistive cell switches to LRS. Under reverse bias, the filament is ruptured or locally dissolved by Joule heat deposited in the filament and partly by electrochemical ionization of Cu forming the filament and the cell is switched back to the HRS.

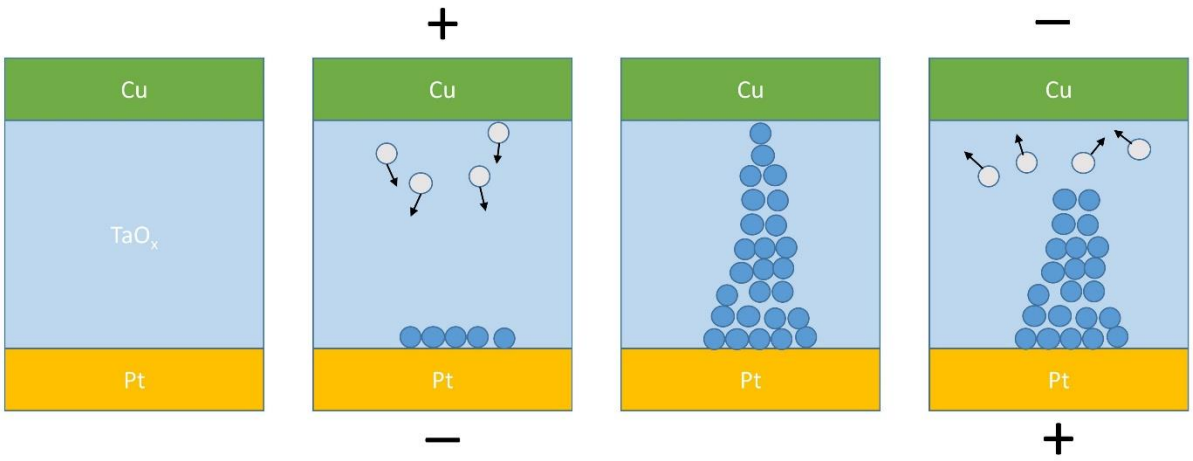

Figure. 1.8. Schematic illustration of switching process of ReRAM devices. (a) Off state. (b) Switching on. (c) On state. (d) Switching off.

According to the voltage polarity of the reset operation, there are two working modes of operation of the resistive switches, unipolar mode and bipolar mode as shown in Figure. 1.9.[39, 43] In the case of bipolar resistive switching, the polarity of the external voltage for the SET and RESET is opposite. For unipolar resistive switching, the polarity of the external voltage for the SET and RESET is the same. Due to the high current and tiny cross section of the filament, it is likely to perform a RESET operation due to high Joule heat generated in the filament. Memory cells based on Cu and Ag migration are typical bipolar resistive switches.

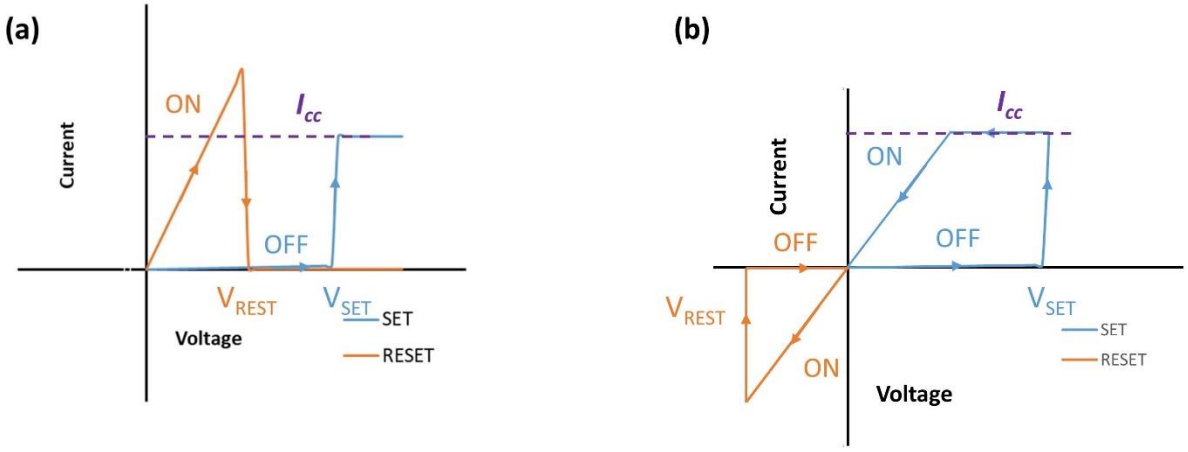

Figure. 1.9. (a) Unipolar and (b) Bipolar modes of operations.

1.2.2 Parameters for Evaluating for Memory Device Performance

In order to systematically evaluate the resistive switching performance of devices in this study, the following terminology is used to describe and compare the performance of device.

FORM Voltage

After the fabrication, the memory cells are in very high resistive state: on the order of tens to hundreds of MΩ because there are no filaments. A filament will be formed after applying a high voltage bias. At V_{FORM}, the current increases dramatically and the cell switches to LRS. Therefore, form is a phenomenon in which a conductive filament is formed in the solid electrolyte for the first time in a fresh cell. Generally, V_{FORM} depends on the thickness of the dielectric and the materials of the electrode metals and dielectric. Different polarities of form voltage can produce different conductive filaments in the solid electrolyte.

RESET Voltage

RESET is the phenomenon in which the conductive filament bridge either is ruptured due to the thermal dissolution caused by Joule heat (unipolar mode) with the help of ion migration in case of the bipolar mode. RESET switches the device from a LRS to a HRS. During the RESET, the resistance of the switch is called R_{off}.

SET Voltage

SET is the phenomenon in which the conductive filament are re-established after being ruptured at least once due to Joule heating and by electrochemical migration of ions. The SET voltage (V_{SET}) is usually lower than V_{FORM} of the device, which may be due to the existence of

partial filament established during the preceding the FORM or SET Process. SET switches the device into the LRS (also called the on state), and the corresponding device resistance is Ron.

Compliance Current

During the SET and FORM process, the external circuit applies a limiting current called compliance current (I_{CC}) to prevent permanently damage to the devices. In the case of a set operation, the normal range of I_{CC} used in study is 5 μA to 0.5 mA. A compliance current limit is not required during the reset operation. The filament may never be ruptured if a low enough compliance current is applied during the RESET operation.

Endurance

ReRAM devices can frequently switch from HRS to LRS, but each operation can cause damage to the integrity of the device called degradation. Endurance is defined as the number of SET/RESET cycles that can be tolerated before the device can no longer be switched.[44] The end of the switching cycles is marked by state in a permanent irreversible LRS state.

Retention time

Retention time shows the inherent ability of a resistive memory device to maintain its stored state after it has been programmed or erased. Regardless of the percentage of time the device turned on, the aim of retention time of all commercial products is 10 years.[45]

1.2.3 Switching Mechanism of Resistive Memory (Cu/TaO_X/Pt) Device

Cu/TaO_X/Pt resistive device is a potential candidate for non-volatile memory that can switch between HRS and LRS based on the formation and rupture of two types of conductive filament. During the SET and RESET operations, in terms of the conduction mechanism, a Cu or oxygen vacancy conductive filament (CF) forms and ruptures in the Cu/TaO_X/Pt device. Under a positive bias, the Cu active electrode is oxidized to Cu^+ ions and drifts toward the Pt electrode under the influence of a high electric field. The following reduction-oxidation reaction occurs at the interface between the Cu electrode and the TaO_X layer:

$$Cu \rightarrow Cu^+ + e^- \qquad (1)$$

The Cu^+ ions are reduced and deposited on the surface of the Pt electrode as Cu atoms. during the SET process, the Cu conductive filament (CF) grows vertically until it reaches the top Cu electrode. After the SET, the two electrodes are connected via the CF, which causes the device to switch from HRS to LRS. When a negative bias is applied to the Cu electrode of a new device, negative oxygen atoms O^- or O^{2-} may be displaced form TaO_X matrix leaving an empty space, so called oxygen vacancy. Accumulation of vacancies leads to a formation of the oxygen vacancy conductive filament can be established in TaO_X layer. The following electrode reduction reaction occurs in the TaO_X layer:

$$TaO_x + 2e^- \rightarrow TaO_x^{-1} + O^{2-} \rightarrow TaO_xV_o + O^{2-} \qquad (2)$$

Under the electric field pointing from Pt to Cu, the O^{2-} ions migrate from the Cu electrode to the Pt electrode. As a result, a conductive filament is formed by displaced O^{2-} ions, resulting in leaving vacancies V_O behind. During the SET operation, the device switches to LRS through the

oxygen vacancy conductive filament. Figure. 1.10 shows the two different types of conductive filaments inside a single Cu/TaO_X/Pt resistive device.

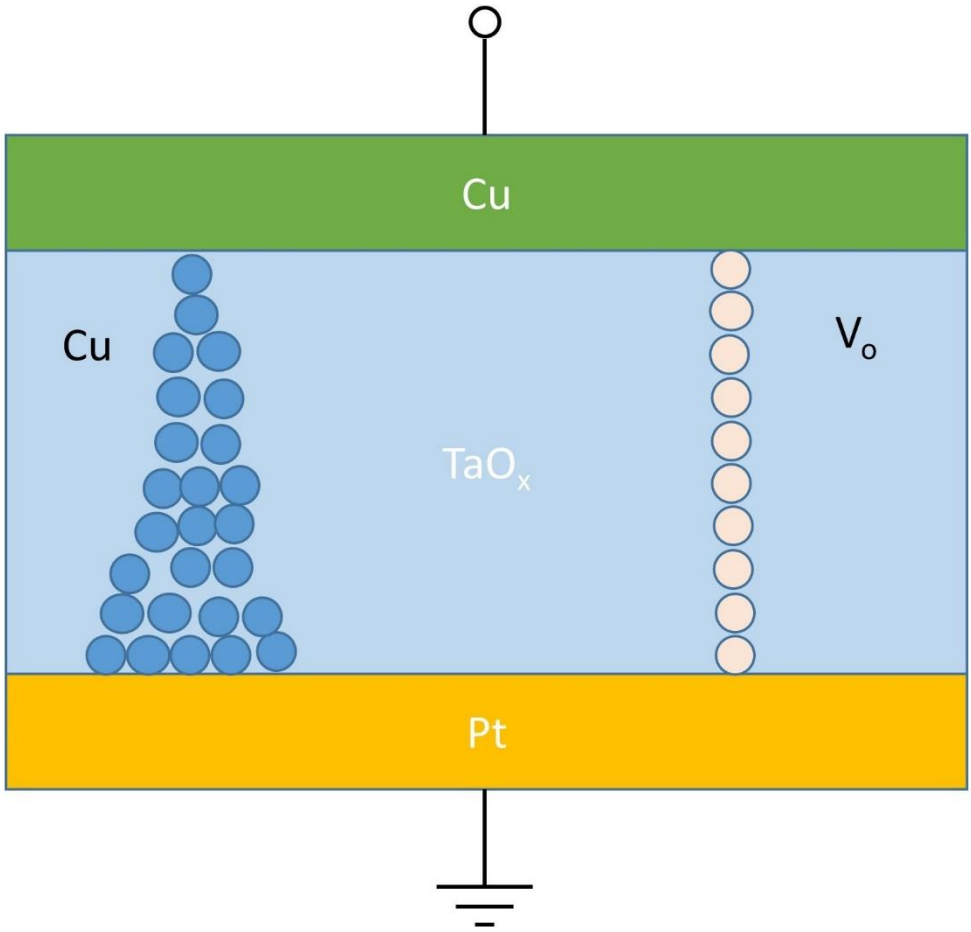

Figure. 1.10. Two different types of conductive filaments inside a Cu/TaO_X/Pt resistive device.

1.3 Polymer Memory

As a promising novel non-volatile memory, polymer based memory has recently attracted significant attention from scientists.[16] In a standard polymer memory, an organic layer

containing molecules, nanoparticles *etc.* are inserted between two metal electrodes. This type of memories has various advantages, such as simple device architecture, 3D stacking capability, low-cost, simple fabrication process, free read/write capability *etc.*[16, 46, 47]

In this thesis, we use the Cu doped polymer electrode to replace the transitional metal active electrode such as Cu electrode in the Cu/TaO_X/Pt device. Compared with traditional electronic memory, the data storage mechanism of polymer based memory is completely different. The conductivity of the organic polymer material can be adjusted by applying an appropriate electric bias. The 'LOW' and 'HIGH' resistance state of the organic layer can be used as two different memory states and information can be stored accordingly. The device fabrication process begins with patterning and depositing first the bottom electrode aluminum (Al) layer. The organic is then mixed with all required constituent elements in a solvent and spin coated on top of the deposited bottom electrode materials to form the solid electrolyte layer. After thermal annealed on a hot furnace, depending on the organic layer material viscosity and spin-speed, a thin organic film with thickness of 25 nm to 200 nm could be obtained. Finally, the Cu doped polymer electrodes are spin coated on the top. Since most polymer materials consist of long polymer chains, they have the potential to integrate with the latest high density 3D technologies.[48] A 3D schematic of polymer based memory device is described in Figure. 1.11.

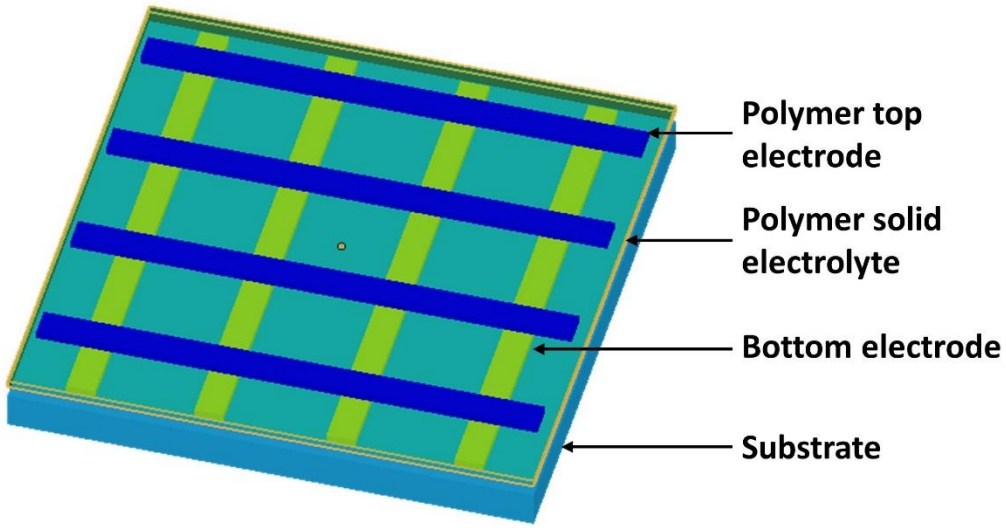

Figure. 1.11 3D schematic drawing of polymer ReRAM.

1.4 Document Organization

This chapter is followed by the fabrication and characterization chapter, in which we presents the step by step detailed fabrication process flow for the inorganic Cu/TaO_X/Co device and the organic Cu doped PANI-CSA/O-AA/Al device that we will discuss in the later part of this thesis. All the ReRAM devices are fabricated in a crossbar array architecture using Virginia Tech nanofabrication & characterization laboratory. A brief introduction of all relevant processing technologies has also been included.

In Chapter 3, we describe the first stage of the work where we discuss the fabrication and characterization of inorganic ReRAM device with a structure of Cu/TaO_X/Co. The Cu/TaO_X/Co device owns a similar FORM, SET and RESET voltages compared with the Cu/TaO_X/Pt. The same as Pt and Ru devices, the on-state resistance of the Co devices is mainly limited by the

compliance current (I_{CC}). The reliability of Co devices is limited by the joule's heat accumulated in the Cu conductive filament during the SET-RESET operations.

Chapter 4 introduces Cu doped PANI-CSA/O-AA/Al ReRAM memory cells in detail. Its device fabrication, characterization methodology, switching characteristics *etc.* has been analyzed comprehensively. The organic ReRAM device owns a relative lower FORM voltage and very limited switching cycles. The performance of this organic ReRAM device also depends on the concentration of the Cu^{+} ions as well as the thickness of the top polymer electrode.

In Chapter 5, we present a discussion of the results achieved in this thesis and an overview of future currently under way and possible directions in which the project could be expanded using different inert electrode materials and possible organic bottom electrode such as graphene.

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Chapter 2

Fabrication and Characterization of Resistive Random-Access Memory (ReRAM) cells

Although the scaling of conventional memories such as volatile dynamic random-access memory (DRAM) and non-volatile flash technology is becoming increasingly difficult, new types of non-volatile memories, such as resistive switching memories, have recently attracted the attention of both industry and academia.[1-8] Resistive switching memory is considered as the next generation non-volatile memory because of its excellent scalability, high switching speed, simple structure and low power consumption.[9, 10] These two terminal devices have figure eight like clamped current-voltage (I-V) hysteresis and work by change of resistance from high resistance (HRS) state (OFF-state) to low resistance (LRS) state (ON-state) responding to applied voltage or current due to the formation and rupture of a conductive filament. In particular, Conductive Bridging Random Access Memory (CBRAM), also known as Programmable Metallization Cell (PMC), is a potential candidate for resistive memory devices due to its highly scalable and low cost technology.[11] Currently, the interconnect RC scaling methods have reached their limits, and alternative methods are urgently needed to reduce or eliminate the latency constraints in CMOS low-k/Cu interconnect. Building CBRAM directly into a low-k/Cu interconnects is one of the promising methods that can reduce the latency in connectivity constrained computational devices and the chip's footprint by stacking memory on top of logic

circuits.[12, 13] This is possible because the Cu metal lines and low-k/Cu interconnect have been prefabricated as potential RS devices, and the cross-bar architecture of a typical two-terminal RS device array is basically the same as a CMOS metal interconnect system. Therefore, the same basic general hardware platform can be used to resolved the bottleneck of interconnect information and transform it into multiple system architectures.

CBRAM devices consist of an insulating electrolyte layer sandwiched between an inert cathode and an oxidizable active anode. Different dielectric and semiconductor materials have been studied as solid electrolytes in CBRAM cells, such as GeSe, WO_3, Al_2O_3, Ta_2O_5 or TaO_X.[14-16] The active metal can be any oxidizing metal having a high activation energy, such as Cu, Ag or Ni, and thus easily yields ions.[17-19] The inert metal materials are usually Pt, Ir or W, which are the stopping barriers for Cu, Ni and Ag cations. When a positive bias is applied to the active electrode, Cu^+ or Ag^+ ions are created and pass through the solid electrolyte. These ions accumulate at the interface between the solid electrolyte and inert electrode. The accumulated atoms nucleate and grow to form a nanoscale metallic conductive filament (CF) connecting both electrodes, so called FORM and SET processes. Under a reverse bias, the filament is mainly dissolved by Joule heat and partly by electrochemically ionization of Cu forming the filament, and the cell is switched back to the HRS, known as RESET process.

2.1 Challenges to Implement Resistive Memory Cells in the CMOS BEOL

There are various challenges in implementing resistive switching memory cells into back-end-of-line (BEOL) of CMOS.[20] The challenges include not only selecting materials for stand-alone

CBRAM cells, but also the way to embed the cells in BEOL.[21] In case of the inert electrode, a composite electrode having an appropriate adhesive layer, heat transport layer, and an appropriate inert metal is required, which has sufficient thermal conductivity, low surface diffusion, and low miscibility with the active metal atoms. The active metal is required not only to undergo a large number of redox reaction but also to prevent reactions with the dielectric at the same time. A dielectric with a moderate defects level is preferred, which can be controlled by deposition processes. Finally, the choice of the materials depends on the material and process compatibility with BEOL, and the dynamics of the resistive switching operations, including Joules heat during SET and RESET operations.

The possible consequences of attempts to integrate independent resistive switching cells that are carefully designed to satisfy the requirements and specifications of all non-volatile memory array can broadly illustrate the integration challenges of implementing a good performance memory cell array into backend CMOS. When attempting to embed such optimized memory arrays into the BOEL of CMOS, is likely to be found that either the memory cell materials are incompatible with BEOL materials or manufacturing processes, or it results in excessive manufacturing costs, or even if it is cost effective compatible with materials and processes, the embedded memory arrays would also show dramatically electrical degradation or complete failure. In the following section, we will discuss the fabrication process of inorganic ReRAM and polymer ReRAM.

2.1.1 Choice of Active Electrode Metal

The reaction leading to the supply of metallic cations is the redox reaction (1). In case of Cu, of which the ionization energy is 7.7 eV, there is copious production of Cu^+ ions and electrons. The ionization energy only indicates the efficiency of the reaction (1), because the reaction occurs at the interface to the active layer and dielectric layer. Experiments with metals with higher ionization energies, such as Pt in Pt/TaO_X/Pt devices, have shown that the level of electron injection is much lower and therefore the voltage for the formation of oxygen vacancy filaments driven by the reaction (2) is much higher. The Ta/TaO_X/Pt device clearly shows that although ionization energy of Ta is 7.55 eV, which is slightly lower than that of Cu, which is 7.72 eV, the efficiency of the redox reaction ($\mathrm{Ta} \longleftrightarrow \mathrm{Ta} + \mathrm{e}^-$) is significantly lower than that of Cu, because it is not as good as Cu, under the condition of insufficient oxygen, that is, Ta rich TaO_X with $x \approx 2$.[22] Metals with low ionization energies, such as Ti (6.83 eV), are also ill-suited as candidates for the active electrode because the Ti^+ ions are immediately consumed in TiO_X and possibly in titanium silicide reaction.[22] Therefore, Cu (7.7 eV), Ni (7.6 eV) and Ag (7.6 eV) with moderate and very similar ionization rates appear to be the best cations for resistive switching memories.[17-19] In fact, these are the three metals, for which metallic filament formation has been reported.

From the cross comparisons between the various devices, a consistent picture of mechanism of the filament formation and its characteristics is gradually emerging. Following mechanisms are responsible for the formation of filament and the characteristics of their hypothesized geometric shape: (i) Moderate efficiency of the redox reaction (1), not too high to react with the solid electrolyte, but not too low to provide sufficient metal cations and electrons. (ii)

Sufficiently high diffusion rate of cations in the solid electrolyte. (iii) High cation stopping ability at the solid electrolyte/inert electrode interface. (iv) Low interfacial diffusion rate of neutralized cations along the solid electrolyte/inert electrode interface. (v) Metal oxidation is responsible for the efficiency of electron injection, which is important when the conductive filament is a defect filament such as oxygen vacancy.

2.1.2 Choice of Solid Electrolyte

In most cases, it is desirable that the solid electrolyte should exhibit a moderate level of defects. Point defects (such as oxygen vacancies) or extended defects (such as nanopores) can facilitate ion electromigration. For example, when comparing the oxygen deficient TaO_X with stoichiometric Ta_2O_5 layers with higher density, Cu/TaO_X/Pt consistently showed better performance than the Cu-Pt devices with the Ta_2O_5 switching layer.[22] According to Brumbach *et al.,* x=2 in TaO_X is the optimal stoichiometric ratio for ReRAM.[23] Compared with thermally grown SiO_2, PVD deposited Cu/SiO_2/Pt devices show much higher defect and allow only a reliable resistive switching of Cu filaments for layers thinner than 35 nm, but not for dielectric defect (oxygen vacancy) filament formation.[24] However, SiCOH films with a density significantly lower than SiO_2 are ideal candidates for ReRAM applications with FORM, SET and RESET voltages well below 1 V.[22]

2.1.3 Choice of Inert Electrode Metal

Highly reliable and best performing ReRAM cell designs require a more thorough review of the properties of the inert metal electrode. The most important property of the inert electrode is that it is immiscible with the metal of the active electrode (Cu, in this case). The required immiscibility should be maintained not only at room temperature but also at high temperatures up to 900 ^{o}C. When Cu ions reach the inert electrode, it is desirable that they stop at the dielectric/inert electrode interface. Only when they adhere to the surface of the inert electrode and aggregate, they can effectively build a metallic dendrite that forms the conductive filament when it reaches the active Cu electrode. Immiscibility is usually (but not always) related to the ionization energy of elemental metals. As can be seen form Table. 2.1, the metal (Pt) of the inert electrode of a typical ReRAM device has a high ionization energy of 8.96 eV. Although Ir has similar ionization energy (8.97 eV), preliminary results of a Cu/TaO_X/Ir devices show poor electrical performance compared to the corresponding Cu/TaO_X/Pt device. Although the relation between ionization energy and miscibility has not been fully understood, miscibility itself involves not only the properties of the inert metal but also of the active metal.

Metal	Ag	Al	Au	Co	Cr	Cu	Ir	Ni	Pd	Pt	Rh	Ru	Ta	Ti	W
Therm. Cond. W/(m·K)	406	205	315	100	94	385	147	90	72	72	150	117	54	22	165
Ionization Energy eV	7.58	5.99	9.23	7.88	6.77	7.22	8.97	7.64	8.34	8.96	7.46	7.36	7.55	6.83	7.86

Table. 2.1. Thermal conductivity and ionization energy of elemental metals.

The inert electrode also requires the property of low surface diffusion of active metal atoms on its surface. The high surface diffusivity of active metal atoms on the surface of the inert electrode would cause the filament base become weaker, which results in a higher FORM and SET voltages, and likely forms a cylindrical filament that is difficult to rupture. All the data so far indicate that Cu surface diffusivity at the Pt electrode is low.

Another required property of an inert electrode is that the conductor remains amorphous at local high temperatures up to 900 ^{o}C. If the inert electrode metal forms crystalline grains, the grain boundaries on the surface would allow active metal atoms diffuse into the inert electrode, thereby preventing the formation of a filament that can be easily ruptured.

Finally, the inert electrode should not react with elements in the underlying layers on the wafer. The inert electrode is separated from the subjacent passivation layers only by a thin glue layer such as Ti. In the case of the Ru devices, elements such as Si may diffuse through the glue layer and form ruthenium silicide.

2.2 Fabrication of Cu/TaO_X/Co ReRAM Device

Cu/TaO_X/Co resistive switching memory devices have been fabricated at nanofabrication and characterization laboratory at Virginia Tech. The two terminal ReRAM devices have Metal-Insulator-Metal architecture and are arranged on a thermally oxidized Si wafer in the form of a crossbar array. Figure 2.1 shows the schematic drawing of the Cu/TaO_X/Co device.

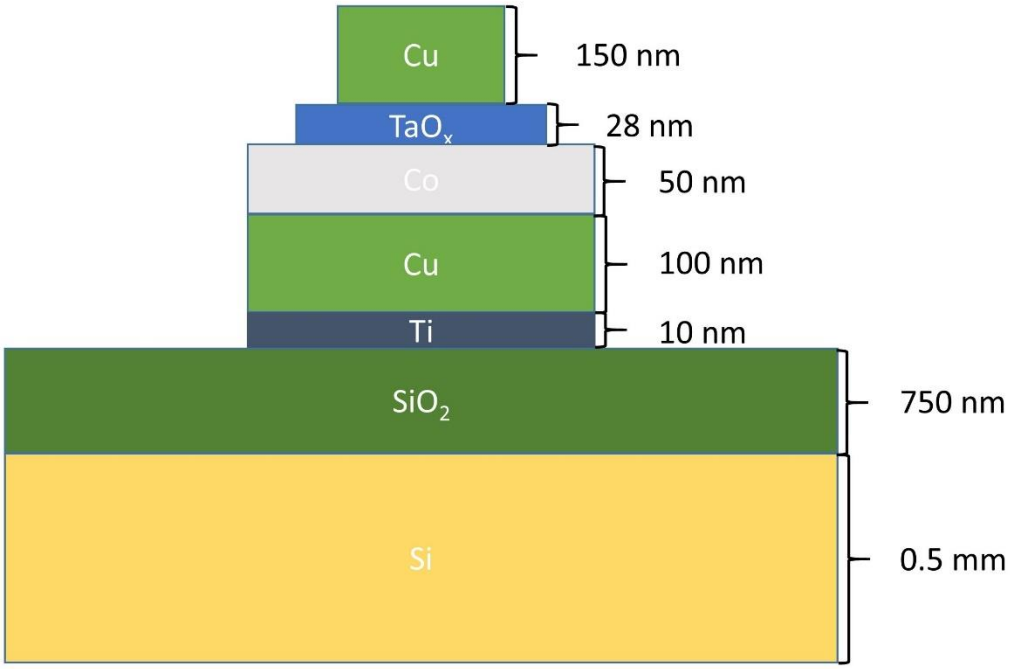

Figure. 2.1 The cross-section of a completed Cu/TaO_X/Co resistive switching device.

For ReRAM devices, various potential materials are being investigated. For top electrode, Ag, Ni, Cu have been explored by several researchers. In case of solid electrolyte SiO_2, HfO_2, Ta_2O_5, TaO_X, WO_X *etc.* are some of the common choices. For bottom electrode, Ta, W, Pt *etc.* are widely used. While in this thesis, Cu is used as the top electrode, oxygen deficient TaO_X as the solid electrolyte and Co as the inert electrode.

2.2.1 Step by Step Fabrication Process Flow

Figure. 2.2 depicts the complete process flow for fabrication of ReRAM memory cell. Some main processing steps are discussed in detail below:

I. Wafer Cleaning

II. Thermal Oxidation

III. Photolithography

IV. Physical Vapor Deposition

V. Liftoff

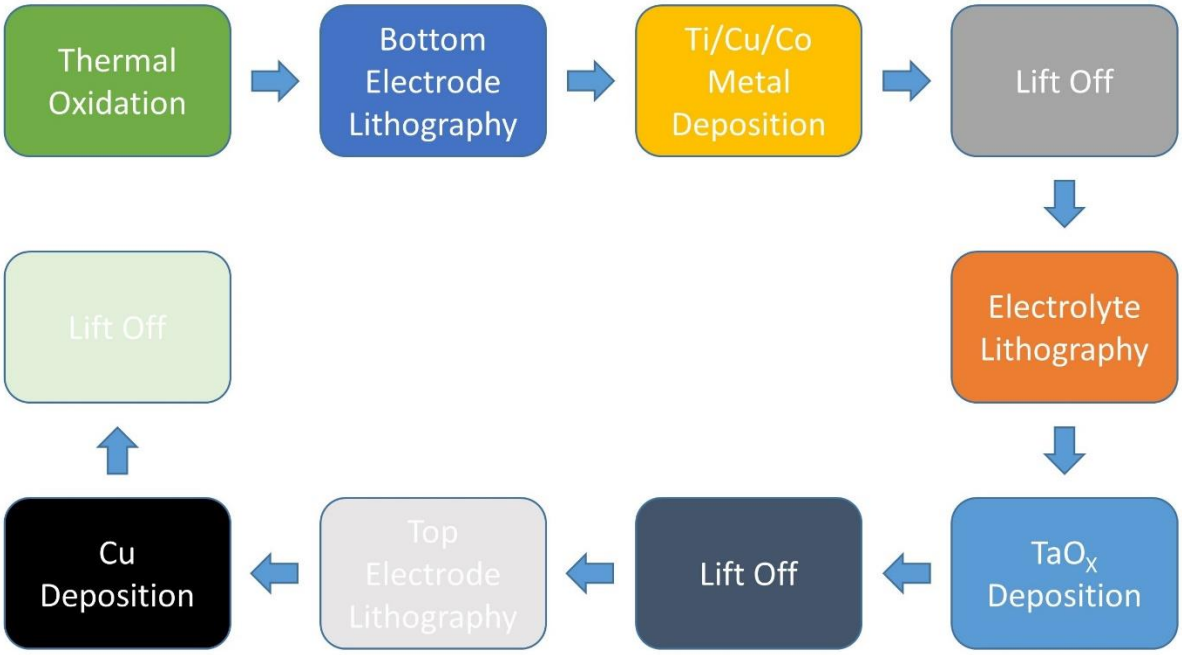

Figure. 2.2. Fabrication process flow for ReRAM memory cell.

2.2.2 Wafer Cleaning

Cleaning is the first process in the semiconductor fabrication process flow and the basis of other processes. Any undesired contamination can cause poor device performance, device reliability degradation and even complete device failure. Therefore, the precisely control of the

density and size of particles or contaminants present in the device and in the fabrication environment is extremely important. In order to avoid contaminants, dust, airl particles *etc.* and ensure controlled temperature, humidity, pressure, lighting *etc.*, the photolithography process should be performed in a controlled cleanroom.

There are two types of cleaning procedures: dry cleaning and wet cleaning. In dry cleaning, gas phase chemical reactions with contaminants create volatile compounds and thus cleans the wafer surface. However, in wet cleaning, solvent/acid/base reacts with contaminants to form a solvable compound. During ReRAM device fabrication, a wet cleaning procedure is used. The wafer is first blow dried with nitrogen (N_2) to remove any dust particles and then cleaned by a wet chemical cleaning process using solvents (Acetone and Isopropyl alcohol (IPA)). After each cleaning process, rinse with Deionized water and blow dry with N_2. The step by step wafer cleaning procedure is illustrated using Figure. 2.3. The entire cleaning process with ultrasonication is performed in the wet bench in VT cleanroom facility.

Figure. 2.3. Wafer cleaning process flow.

2.2.3 Thermal Oxidation

There are two parts in the oxidation process: dry oxidation and wet oxidation. Figure. 2.4 shows a schematic diagram of the oxidation furnace and the oxidation furnace system used in this work. During dry oxidation, high purity O_2 flows into the chamber, while for wet oxidation, steam is added with O_2 at the required chamber temperature. Dry oxidation process provides high quality and dense oxide, but it is slow. In contrast, wet oxidation provides less dense oxide

but has a faster oxidation rate. For the ReRAM devices, a thick isolation oxide is required to avoid unnecessary current flowing between the memory arrays fabricated on the oxide. Therefore, thicker wet oxide is sandwiched between thin dry oxide layers to balance the thickness requirements and time consumption. Therefore, the oxidation process includes a dry oxidation with a short duration (10 minutes), followed by wet oxidation with a long duration (2 hours) and dry oxidation with a short duration (10 minutes).

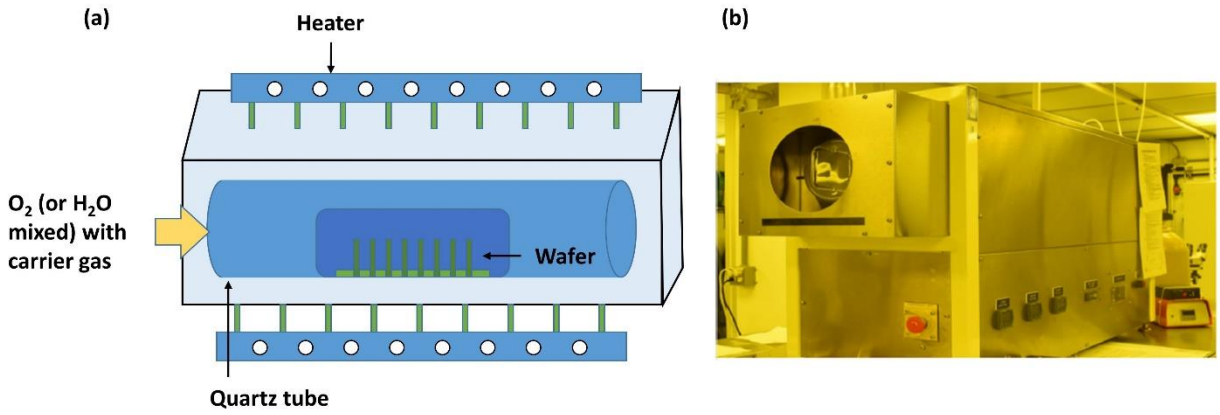

Figure. 2.4 (a) The schematic diagram of oxidation furnace. (b) The image of the oxidation furnace that used in this thesis.

The wafer is first cleaned using wet chemical cleaning process described above. The oxidation furnace is then set at temperature of 650 ^{o}C and high purity N_2 is blown into the chamber at a rate of 1 L/min. After the chamber reaches the desired temperature, the cleaned Si wafers are placed on a quartz boat and loaded into chamber. The chamber temperature is then set to desired 1050 ^{o}C oxidation temperature. Then set the temperature of the boiler assembled with the beaker filled with distilled water at 95-97 ^{o}C, so that O_2 flow can pass through the steam

bubbler and during wet oxidation process, the steamed O_2 can be supplied into the furnace. The furnace is equipped with a thermocouple to monitor the furnace temperature. Once the chamber reaches the desired oxidation temperature, the N_2 flow vale is turned off and the O_2 is supplied into the chamber with a rate of 0.7 L/min, which starts dry oxidation process. For the desired dry oxide thickness, this process is continued for a predetermined time. During the wet oxidation process, the steam valve is open for a certain period of time. Finally, the steam flow valve is closed for the final dry oxidation process. After the oxidation process is completed, the O_2 flow valve is closed, the N_2 purge valve is opened and the temperature of the chamber is reduced to room temperature. When the chamber reaches ambient temperature, the quartz boat filled with wafer is taken out of the furnace. The entire oxidation process is shown in Figure. 2.5.

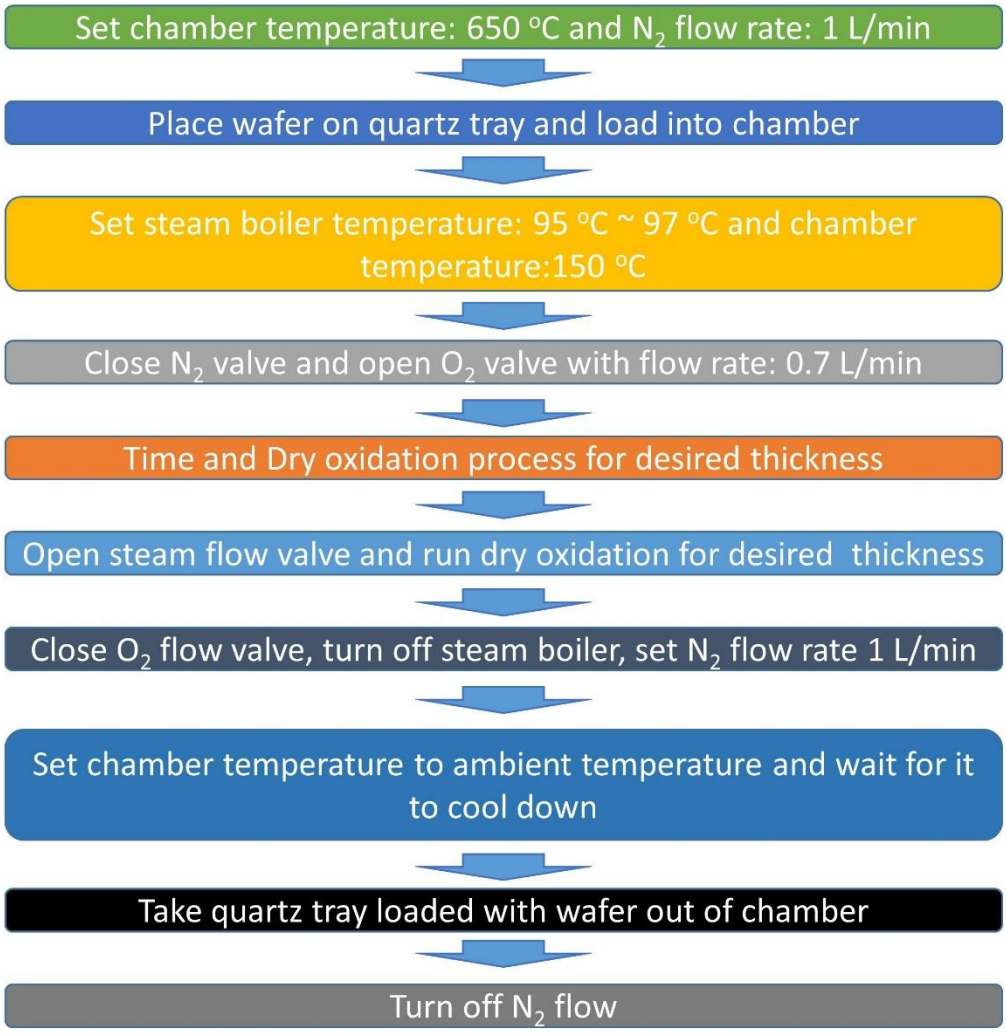

Figure. 2.5. The process flow of thermal oxidation used in this work.

2.2.4 Photolithography

Photolithography, also know as optical lithography or UV lithography, is a process used in microfabrication to pattern a portion of a thin film or the bulk of a substrate (also called a wafer). It uses light to transfer a geometric pattern from a photomask (also known as an optical

mask) to a photosensitive chemical photoresist on the substrate. The process schematic drawing is shown in Figure. 2.6.

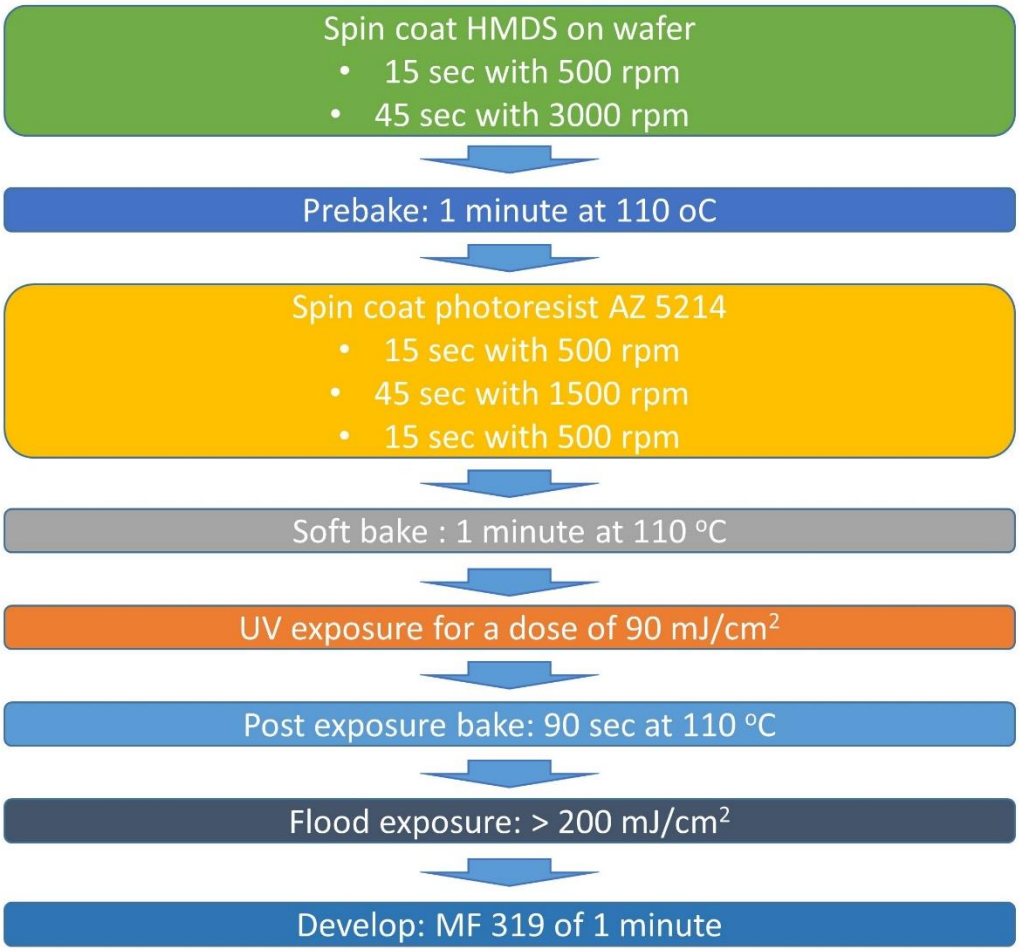

Figure. 2.6. The photolithography process flow used in this work.

Spin-coating Photoresist

Photoresist is a photosensitive organic material that can modulate its solubility after exposure to a controlled dose of ultraviolet radiation. Photoresist contains three components: solvent, resist polymer and sensitizer. The solvent enables the resist to be cast and spread on the wafer

surface, the resist polymer changes its structure by crosslinking with molecules under exposure to UV light, and the sensitizer controls the photochemical reaction.

Photoresist can be either positive type or negative type. In positive photoresist, the UV exposure reduce the strength of the main or side chains of polymer in the exposed area during the photochemical reaction, so these areas are developed faster than the unexposed areas and are washed out after development. In contrast, in a negative photoresist, the UV exposed areas strengthens its bonding with main or side chain through the crosslinking, so that unexposed regions are dissolved instead. Figure. 2.7 shows a schematic drawing of both positive and negative photoresist. The photoresist that we used in this experiment is a negative photoresist (AZ 5214).

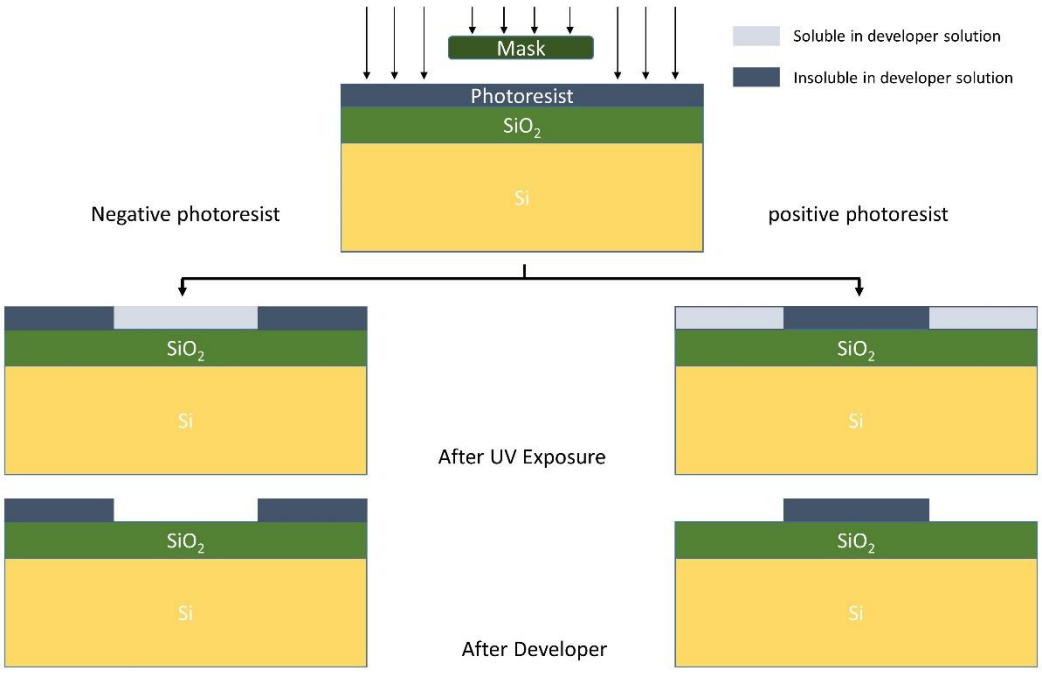

Figure. 2.7. Negative vs Positive photoresist: UV exposure. Development and pattern transfer.

Spin coating is one of the most important steps in forming a uniform photoresist layer on the wafer. Once the wafer is clean, it is locked in the wafer platen assembly of a spinner by a controlled vacuum clamp. The next step is wafer priming. Some photoresists may not adhere well to the silicon wafer that is usually coated with a thin natural oxide. To ensure better adhesion, the light treatment must be performed in a controlled temperature and humidity (40%) environment, and the surface must to be hydrophobic. Therefore, once the wafer cleaning process is successfully completed, it is annealed to remove excess moisture remaining on the wafer surface. In addition, an adhesion promoter such as Hexamethyldisiloxane (HMDS) can also provide excellent adhesion to the photoresist. Its functional clusters can easily react and form bonds with the oxide, and then adhere firmly to the resist. The next step is to spin coat a thin, UV sensitive polymer layer on the wafer. Depending on the desired thickness of organic polymer film, the wafer is spun at a desired high speed and uniform thin coating is obtained.

Mask Alignment & UV Exposure

Mask is a master template for repeated producing the prototype pattern onto the photoresist coated substrate. It is usually made of quartz and is optically flat. Ultraviolet (UV) light can pass through quartz but is cannot penetrate metal design written onto the quartz. In photolithography, depending on the available optics, the source light have a wide range of wavelengths: extreme ultraviolet (EUV) to near ultraviolet (UV) with wavelength of 10-14 nm to 350-500 nm, respectively. The near UV system is the most commonly used system and usually

consists of g-line (435 nm) or i-line (365 nm) with a mercury lamp as the source. The mask aligner is a machine that actually transfers a designed pattern to the wafer. A mask is placed over the wafer with the desired pattern on it. After the wafer is coated with photoresist, it is then loaded into the mask aligner and exposure system so that the wafer can be precisely aligned with the corresponding alignment geometry marked on the mask. Then, the wafer is exposed with the required dos (J/cm^2) of UV light to perfectly replicate a duplication of the mask image onto the photoresist.

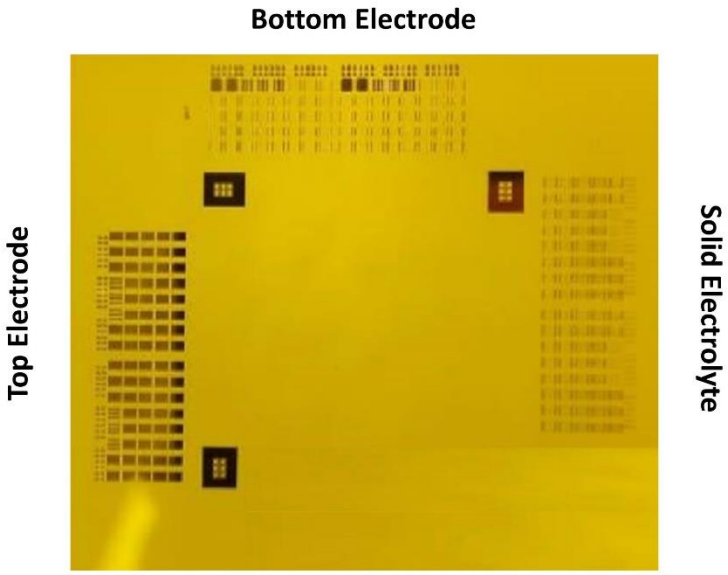

Figure. 2.8. The mask used in this thesis: top electrode, solid electrolyte and bottom electrode.

In this work, there are three different quartz photomasks used for the fabrication of ReRAM devices. One mask for the bottom electrode, one for the top electrode and one for the solid electrolyte. Each mask set has its own alignment mask to facilitate alignment with the subsequent process steps. Every ReRAM device is located at the intersection of top and bottom

electrode layers and arranged in a crossbar array. Figure. 2.8 shows the entire photomask. The spin coating system and mask alignment tool used in this work are shown in Figure. 2.9.

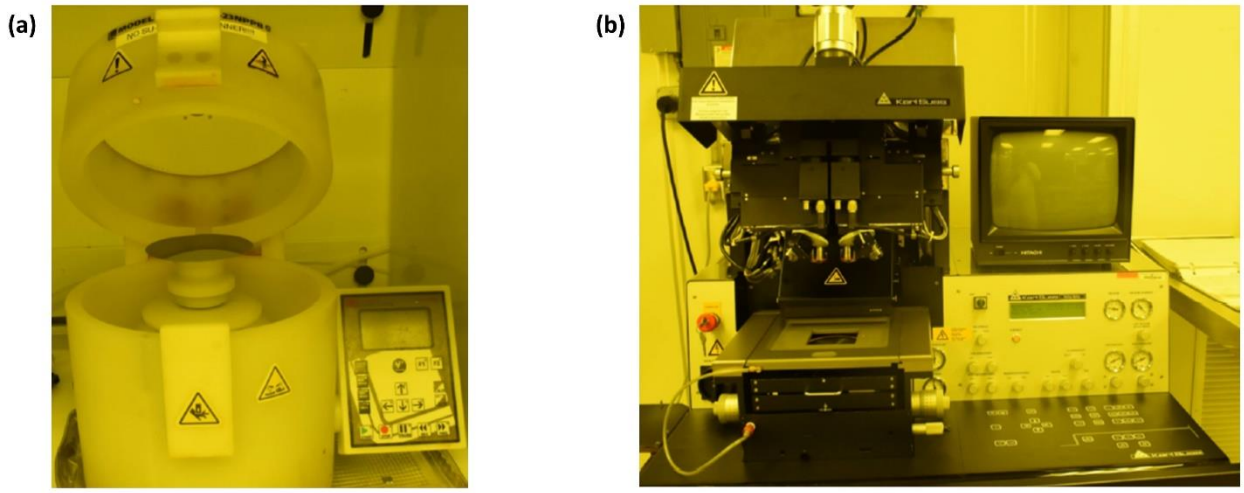

Figure. 2.9. (a) Spin coating equipment. (b) Karl-SUSS MA6 mask alignment system used in this thesis.

Post-exposure Bake (PEB)

The next step is post-exposure baking (PEB), such as flood exposure, post-baking which either start a new chemical reaction or terminates the reaction that has begun as needed and is determined by the selecting of wavelength, photoresist and controlling the chemical reaction. PEB is very crucial for image reversal photoresist. The post-baking temperature is usually slightly higher than pre-baking temperature. However, this temperature needs to be carefully selected because in the presence of catalyst, the reaction accelerates with temperature. This step also affects the results of the next development process.

Development

The final stage of photolithography is development, in which the photoresist is selectively removed after dissolving in a developer solution. It results a transferred pattern as designed and required by the subsequent steps to follow. There are two types of development: dry development and wet development. Usually in wet development, a wafer is immersed in a developer solution at a certain temperature for a specific period of time. When a negative photoresist encounters an organic solvent, it swells and its adhesive property are impaired. A vapor based dry development process may be a potential solution to this problem, which has recently been referred to as a high resolution feature.

MF-319 develop is used for the image reversal photoresist AZ 5214 E-IR in this work. The development time is about 60-70 seconds and some agitation is required during the development process. The wafer is then rinsed with deionized water and dried with N_2. After successful development, reversed image of the mask is transferred to the substrate. Dektak surface profiler is used to verify the thickness of the photoresist, and it is found that thickness is about 2 µm. Before moving the sample to the next process step, it is better to post bake or hard bake the sample at slightly higher temperature and longer duration than the prebake process. This is especially true for negative photoresist, which usually swell after development step. It also improves resist quality and significantly improve the adhesion by removing the excess solvent from the resist.

2.2.5 Physical Vapor Deposition

Physical vapor deposition (PVD) is one of the methods to create nanoscale thin films. The PVD method is achieved by physically generating vapor and then deposit the vapor on the substrate under Ultra High Vacuum (UHV) condition. In this thesis, an E-beam evaporation (PVD-250) is used to realize the deposition of top electrode, dielectric and bottom electrode. There are four crucible positions in the chamber, which can load multiple materials and deposit multiple thin films in same vacuum process. There are two vacuum pumps, a backup pump and a cryopump, which can provide a high vacuum environment with a pressure less than 10^{-6} torr. The deposition rate can be controlled by the level of current. A microbalance quatz crystal is used to monitor the deposition rate and the film thickness. As more and more materials are deposited during the film deposition process, resonant frequency is changed. During this measurement, material parameters such as density of evaporation source, and geometrical parameters (such as tooling factor, Z-ratio *etc.*) are also evaluated.

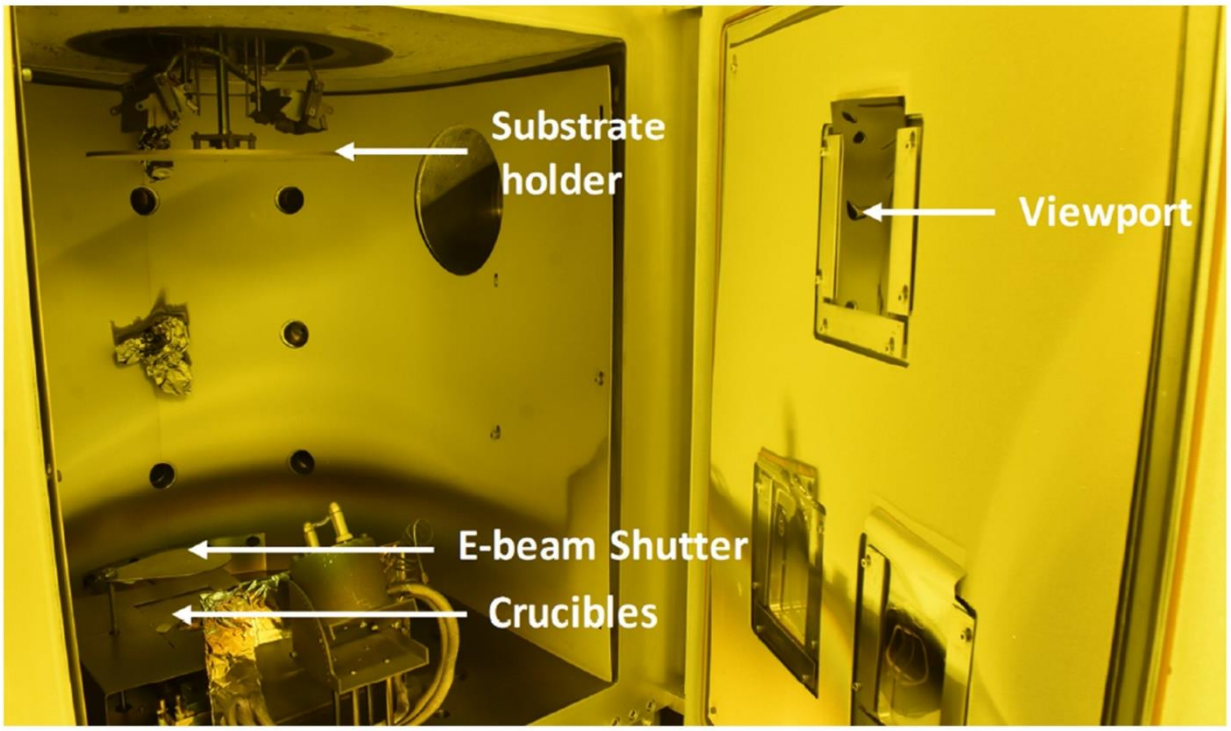

Figure. 2.10. Kurt J. Lesker PVD-250 E-beam evaporation used in this thesis for thin film deposition.

Kurt J. Lesker (PVD-250) e-beam evaporation is the PVD used in this work (Figure. 2.10). The process begins by venting the chamber (injecting N_2 into the chamber) to atmospheric level. Then, the sample is attached to the substrate holder by high temperature adhesion tape, and placed on the sample holder position located at the upper portion of the chamber. The target materials are loaded into the preprocessed crucibles and placed in the crucible holder located at the lower side of the chamber. The chamber is then pumped to a high vacuum level (10^{-6} torr) by a roughing pump and then by a cryopump. Then, select the corresponding evaporation material source and enter the corresponding parameters (density, z-ratio, tooling factor) into

the crystal oscillator software interface system to monitor the thickness. Then, gradually increase the current until the material melt, which can be continuously monitored through an access window. At this time, the source shutter is opened, and the evaporation material is physically struck on the substrate. During the deposition, the deposition rate was kept constant by adjusting the current. After reaching the desired thickness, there should be few minutes of waiting time for the crucible to cool down. The next crucible can then be selected and the process can be repeated. After all desired thicknesses are completed, the chamber is vented and the sample and the crucibles are taken out. The chamber is then pumped down again and usually under vacuum. In this thesis, some thin films such as Cu, TaO_X, Co, Ti are deposited using e-beam evaporation. Table 2.2 lists the e-beam process parameters for all these thin films.

Material	Thickness (Å)	Melting temperature (°C)	Chamber base pressure (Torr)	Current (mA)	Deposition rate (Å/s)	Density (g/cm3)	Tooling factor	Z-ratio
Cu	1500	1085	2×10^{-6}	120	0.7	8.93	140	0.437
TaO_X	280	1872	2×10^{-6}	60	0.5	8.2	140	0.3
Co	500	1495	1×10^{-6}	90	0.5	8.90	140	0.343
Ti	100	1668	1.9×10^{-6}	95	0.4	4.5	140	0.628

Table. 2.2. E-beam deposition parameters for various thin films.

2.2.6 Lift off

Lift off is a technique to remove photoresist and the materials deposited on the top of it, while keeping the materials directly on the wafer through the openings of photoresist defined by

designed pattern. This is a material removal process from the selected area without the need for complicated process such as ion milling, dry etching *etc.*

After removing from the PVD-250, the wafer is then immersed into a photoresist dissolving solution, such as acetone (CH_3-CO-CH_3). Undercutting the resist profile creates some openings and makes acetone attack from the side. When the photoresist is dissolved in acetone, the metals deposited on top of the photoresist lifts off the substrate within minutes, while the metals deposited directly on top of the substrate remain on the sample. Since no etching is involved in this patterned metal transfer process, no etching related damage is caused to the substrate. However, the lift off technology is only limited to one metallization layer at a time, and sputtering technique cannot work with it. The lifted off materials may float in the solution and may stick to the wafer. It may also experience problem with low yield. The lift off process is mainly suitable for research and development.

2.3 Fabrication of Polymer ReRAM Device

Like traditional inorganic ReRAM memory cell, the bottom electrode of the polymer device is patterned by PVD method with a shadow mask. The organic dielectric switching layer and the top conductive polymer layer are deposited by the spin coating method. The cross section of the fabricated devices with the corresponding layer thickness is shown in Figure. 2.11.

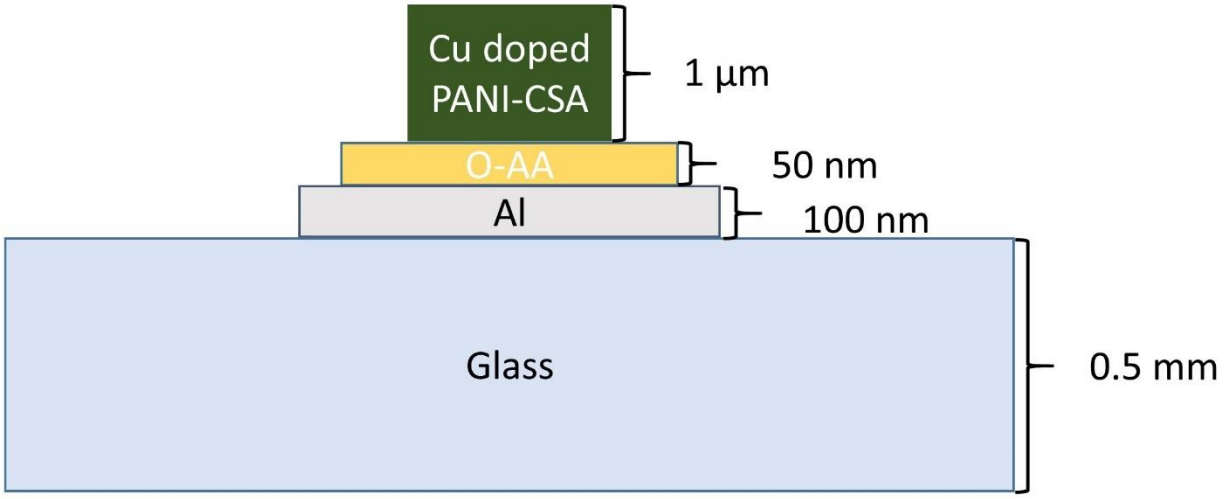

Figure. 2.11. The cross section of a Cu doped PANI-CSA/O-AA/Al device on glass.

2.3.1 Bottom Electrode

A handmade physical mask is used to create a shadow mask composed of flexible and transparent plastic material (Figure. 2.12). The electrode is about 22 mm in length and 3 mm in width. Then, glass slides are put in the PVD with the shadow mask to deposit the desired bottom electrode. The thickness of various layers is summarized in Table 2.3.

Material	Glass	Al	O-AA	Cu doped PANI-CSA
Thickness	1 mm	100 nm	50 nm	1 µm

Table. 2.3 Thickness of various layer of the fabricated devices shown in Figure 2.11.

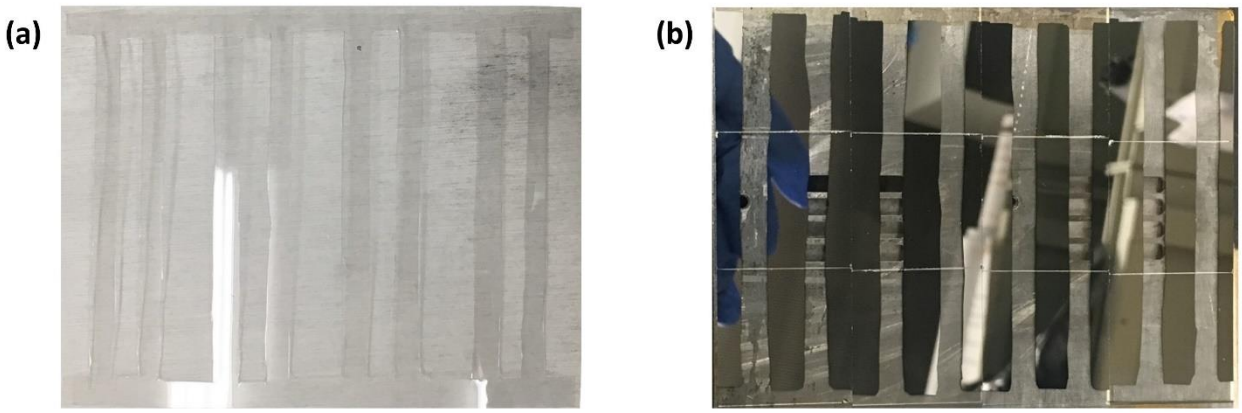

Figure. 2.12. (a) The handmade physical mask for the bottom electrode. (b) The sample that we get after PVD deposition of 100 nm Al on glasses.

2.3.2 Organic Dielectric Layer

There have been a variety of organic polymers that have been explored by several researchers. Each polymer had its own specific advantages and disadvantages for a particular application. However, organic anthranilic acid (O-AA) is used for this case due to its low-cost and superior device performance.[25, 26] Reported O-AA based devices exhibit low switching voltages, high ON/OFF current ratios, and stable ON and OFF states in ambient condition without any device degradation even up to one year.[27]

O-AA was prepared by first mixing 3 mL of DMF with 48.87 mL of HCl. This was then combined with 0.178 g of AA. 3.3254 mL of ANI was then added to this mixture. A combination of 10 mL of APS and 50 mL HCl was then added to the mixture to produce O-AA. The polymer was collected by filtration from the solution, washed with 1.2 M HCl until the filtrate became colorless and then dried under vacuum at 20 ^{o}C, till constant weigh. Then, the collected

polymer was dissolved in acetone with a concentration of 10 mg/ml. Finally, the solution is spin-coated on the bottom electrode samples to create a layer of organic dielectric with a thickness about 50 nm. The amount of chemical used for the polymer preparation is also listed in Table.2.4.

Chemical	Amount
AA (Anthranilic Acid)	0.178 mg
ANI (Aniline)	3.245 mL
APS (Ammonium Persulphate)	10 mL
DMF (N, N-Dimethylformamide)	3 mL
HCl	46.873 mL

Table. 2.4. Amount of chemical used for the preparation of O-AA.

2.3.3 Top Conductive Polymer Electrode

Polyaniline-CSA (PANI-CSA) has been one of the most studied conducting polymers during the last few decades due to its easy synthesis, low cost, environmental stability, simple doping/dedoping process, high conductivity, eminent catalyst activity and high pseudo-capacitance.[28-30] In order to improve the conductivity of the polymer and provide Cu ions for building of conductive filament (CF), we doped PANI-CSA polymer with Cu^{2+} ions by adding chemical $Cu(BF_4)_2$ to PANI polymer.[31] The PANI polymer and CSA are mixed with a mole ratio of 2:1, and then desired $Cu(BF_4)_2$ are added to the mixture with any desired weigh ratio. Finally, all the mixture is dissolved in solvent (m-cresol, acetonitrile, deionized water (DI water)) to

prepare the solution. The solution preparation required 3-4 days of stirring with an initial heating at 50 °C for 12 hours to make the solution homogenous.

	PANI concentration	More ratio (PANI:CSA)	Doped with Cu concentration	solvent	Spin coating speed	Resistance
Sample 1	10 mg/ml	1:2	6.4 mg/g	acetonitrile	1500 rpm	>99 MΩ/□
Sample 2	10 mg/ml	1:2	6.4 mg/g	DI water	1500 rpm	> 99 MΩ/□
Sample 3	6 mg/ml	1:2	6.4 mg/g	M-cresol	1000 rpm	7.2 kΩ/□

Table 2.5 The Cu-doped PANI-CSA polymer dissolved in acetonitrile, DI water and m-cresol, respectively. Resistance larger than 99 MΩ/□ means the value is out of range.

One of the most important issues of the polymer ReRAM is sufficiently high conductivity of the top polymer electrode. We first try to determine how the solvent would affect the conductivity of the Cu-doped PANI-CSA. We have chosen three materials (acetonitrile, DI water and m-cresol) as the solvent of Cu-doped PANI-CSA, and labeled these samples as 1, 2 and 3, respectively. The electric conductivities of these samples have been measured by the four probe methods, and the results are shown in Table. 2.5. Table 2.5 shows that the conductivity of Cu-doped PANI-CSA could be highly impacted by the type of solvent. Cu-doped PANI-CSA could only be highly conductive when it is dissolved in m-cresol. Our hypothesis is that the properties of the solvent could affect also the morphology of the polymer, and thereby modify the conductivity.

	solvent	Concentration(PANI)	More ratio (PANI:CSA)	Cu concentration	Spin coating speed	After 100 °C annealing 1 min	thickness	Conductivity (S/m)
Sample 4	M-cresol	6 mg/ml	1:2	0	1000 rpm	7.47 kΩ/□	70 nm	1.91 k
Sample 5	M-cresol	6 mg/ml	1:2	6.4 mg/g	1000 rpm	7.2 kΩ/□	64 nm	2.17 k
Sample 6	M-cresol	6 mg/ml	1:2	12.8 mg/g	1000 rpm	6.6 kΩ/□	86 nm	1.76 k
Sample 7	M-cresol	6 mg/ml	1:2	64 mg/g	1000 rpm	10.93 kΩ/□	84 nm	1.09 k

Table.2.6 The conductivity of Cu doped PANI-CSA changed with concentration of Cu^{+} ions.

Besides the solvent, the conductivity of the PANI-CSA material also depends on the concentration of Cu doping. We have adjusted the amount of $Cu(BF_4)_2$, while 4 samples of PANI-CSA (6 mg/ml) have been prepared. We have chosen four Cu contents of 0, 6.4 mg/g, 12.8 mg/g to 64 mg/g as a Cu doping and labeled the samples 4, 5, 6 and 7, respectively. The electric conductivity of these samples have been measured by the four probe methods, and the results are shown in Table. 2.6. The conductivity as a function of the Cu content increases first a little bit (from 0 mg/g to 6.4 mg/g) and then decreases with the increasing amount of copper content. The decrease of conductivity with the Cu contents is a little bit surprising, but could be explained by the role of the BF_4^- compound, which may act as an electron trap. In ref. [28], it has been shown that the addition of copper to the PANI polymer can substantially change the morphology and structure of the polymers, thereby modifying also other properties such as conductivity and electrocatalytic activity.[28] Our hypothesis is that the presence of BF_4^- in sufficient quantities may decrease the conductivity of the polymer by immobilizing the free electrons. From Table. 2.6, it can be seen that sample 5 (6.4 mg/g) exhibits the highest conductivity while sample 7 has the lowest conductivity.

	solvent	Concentration(PANI)	More ratio (PANI:CSA)	Cu concentration	Spin coating speed	Resistance before annealing	After 100 °C annealing 1 min	thickness
Sample 8	M-cresol	10 mg/ml	1:2	12.8 mg/g	850 rpm	Out of contact	5.80 kΩ/□	500 nm
Sample 9	M-cresol	10 mg/ml	1:2	12.8 mg/g	1000 rpm	Out of contact	5.76 kΩ/□	280nm
Sample 10	M-cresol	10 mg/ml	1:2	12.8 mg/g	1500 rpm	Out of contact	8.07 kΩ/□	200 nm

Table. 2.7 The thickness of Cu-doped PANI-CSA changed with the spin coating speed.

Another important property of the doped polymer as the top active electrode is the thickness of the electrode. We have prepared three samples spin coated with three different speed 850, 1000 and 1500 rpm and labeled the samples 8, 9 and 10, respectively. The thickness of these samples have been measured by a profilometer Dektak 150 from Veeco, and the results are shown in Table. 2.7. As we predicted, thickness will dramatically decrease with the increasing spin coating speed. Beside the spin coating speed, the concentration of the Cu-doped PANI-CSA polymer is the other determining parameter. We have prepared three samples with concentrations of PANI-CSA and labeled the samples 11, 12 and 13, respectively. Table. 2.8 shows that the thickness of the polymer electrode increase with a higher concentration of the polymer. While, the thickness does not linearly increase with the concentration. This is mainly due to not only the concentration of the polymer increase but also the viscosity of the solution change.

	solvent	Concentration (PANI)	More ratio (PANI:CSA)	Cu concentration	Spin coating speed	thickness
Sample 8	M-cresol	10 mg/ml	1:2	12.8 mg/g	1000 rpm	250 nm
Sample 9	M-cresol	15 mg/ml	1:2	12.8 mg/g	1000 rpm	500 nm
Sample 10	M-cresol	20 mg/ml	1:2	12.8 mg/g	1000 rpm	1000 nm

Table. 2.8 The thickness of Cu-doped PANI-CSA changed with the concentration of the polymer.

2.4 Characterization of ReRAM Device

I-V characteristics of resistive Cu/TaO_X/Co devices and polymer devices were measured with Keithley 4200-SCS (Semiconductor Characterization System). All devices are characterized by a standard resistive switching process. The voltage is ramped up at a ramp rate rr (usually, 0.2 V/s) from 0 V on the positive (or negative) bias axis while the current is being monitored. At the critical voltage V_{SET}, the current increases very rapidly, indicating that the device becomes highly conductive. In general, to avoid damaging the device, a compliance current I_{CC} (20 µA, 50 µA, 100 µA, 200 µA and 500 µA) should be applied to limit the current flowing through the device. In many cases, the level of I_{CC} determines the nature of the filament and the value of the on-state resistance, R_{ON}. When the voltage is being ramped down, the device displays the ohmic behavior of the ON-state and is characterized by R_{ON}. When the device is set to the ON-state for the very first time, one speaks of FORM operation, characterized by the FORM voltage, V_{FORM}. The V_{FORM} is always larger than V_{SET}, because the Cu filament must be formed completely, not partially, and a part of the filament has been merely ruptured but not completely undone for the subsequent set operations. When the negative bias current reaches

a critical current I_{RESET} at V_{RESET}, the conductive filament is ruptured, and the device reverts to the off-state characterized by a high resistance, which is called OFF-state resistance, R_{OFF}.

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Chapter3

Investigation of Cu/TaO_X/Co Based ReRAM Devices

3.1 Introduction

The Resistive Switching Random Access memory (ReRAM) devices has recently attracted significantly attention of both industry and academia due to the potential candidate for volatile dynamic random-access memory (DRAM) and nonvolatile flash technologies that are approaching their physical limits.[1-8] This two-terminal device exhibit a distinctive 'fingerprint' characterized by a pinched hysteresis of current-voltage (I-V) loop switching between a low resistance R_{on} (on-state) to a high resistance R_{off} (off-state) with memristive characteristics.[2, 3] Conductive Bridging Random Access Memory (CBRAM), also known as Programmable Metallization Cell (PMC), is one of the most promising candidates for a resistive switching memory device due to its low cost and highly scalable technology.[9, 10] Building non-volatile memory (NVM) directly into a Complementary metal-oxide-semiconductor (CMOS) low-k/Cu interconnect module would reduce latency in connectivity constrained devices and reduce chip's footprint by stacking memory on the top of the logic circuits.[11, 12] Large-scale integration of Metal-Insulator-Metal resistive memory by using CMOS process has been reported.[11, 13-15] Low-k dielectrics and Cu metal lines prefigure a potential ReRAM cell, and the cross bar architecture of a typical two terminal RS device array is essentially the same as a CMOS metal

interconnect system. Therefore, the same device platform can be used to resolve the bottleneck of interconnect information and embed it into multiple system architectures.

Due to excellent unipolar and bipolar switching characteristics, device performance, retention, reliability, a Cu/TaO_X/Pt resistive switching device with well performance and well characterization is a strong candidate for non-volatile memory.[10] This device can be used as a memory cell with conductive filaments formed by copper (Cu) or oxygen vacancy (V_O). However, a back-end-of-line (BEOL) compatible Pt alternative is highly needed because platinum (Pt) is not an economical option for industrial production and has not yet been used in the BEOL. A good candidate to replace Pt is Cobalt (Co), which has been studied in the CMOS BEOL as a possible candidate for lining material.[16-19]

Cobalt is a transition metals with the symbol Co and atomic number 27, which is between Iron and Nickel: Co atom has 2 electrons in the fourth orbital and 15 electrons in the third orbital, while Pt atom has one electron in the sixth orbital and 17 electrons in the fifth orbital. Compared with Pt's 8.96 eV, the ionization energy of Co is relatively smaller at 7.88 eV. The work function of Co is 5 eV which is lower than that of Pt of 6.3 eV. Thus the work function difference between Cu and Pt of $\Delta\phi$ = 1.6 eV is much larger than the work function difference between Cu and Co of 0.3 eV. This difference between the work function differences indicates a lower build-in electric field in the Co device than in the Pt device. On this ground alone, one would expect higher forming voltages for the Cu filament and lower forming voltages for the vacancy oxygen (V_O) filaments for the Co device. The melting temperature of Co, T_m(Co) = 1495 ^oC, is lower than that of Pt, T_m(Pt) = 1768.3 ^oC, and the electrical resistivity of Co is almost 2/3 of Pt, Co: ρ_{Co} = 62.4 nΩ·m vs Pt: ρ_{Pt} = 105 nΩ·m, while Cu has a lower resistivity, ρ_{Cu} = 16.8 nΩ·m.

In addition, the thermal conductivity of Co is 100 W/(m·K) much higher than that of Pt (72 W/(m·K)), which may improve device endurance. Moreover, Co is much cheaper than Pt, and has similar properties as Pt, which makes a Cu/TaO_X/Co device more promising.

3.2 Device Fabrication

The ReRAM devices based on crossbar array architecture are fabricated on a thermally oxidized silicon (Si) substrate with a SiO_2 thickness about 730 nm. Both metal electrodes and insulator (solid electrolyte) were patterned by photolithography technology and then deposited by electron beam evaporation. A 10 nm thin titanium (Ti) layer was deposited between SiO_2 and Cu to improve the adhesion of the Cu layer, which provide a heat sink for the device to improve the thermal endurance of the device. Above the Cu layer, a 50 nm thickness of Co layer is deposited as the inert electrode. The thickness of solid electrolyte (TaO_X) was 28 nm. A layer of Cu with a thickness of 150 nm is deposited on the top of the solid electrolyte as the active electrode. The width of the metal lines varies between 5 µm, 10 µm, 15 µm, 20 µm, 25 µm, 30 µm, and 35 µm resulting in rectangular areas of the device in the range of 25 to 1225 μm^2. The gap between the nearest metal lines is 150 µm. All metal layers (Cu, Co, Ti) were deposited by Physical Vapor Deposition (PVD) method in a Kurt J. Lesker e-beam PVD-250 chamber. The oxygen deficient TaO_X ($x \approx 1.9$) was deposited also in the PVD-250 chamber by evaporating Ta_2O_5 pellets without O_2 injection into the evaporation chamber. I-V characteristics were measured by a Keithley 4200-SCS (Semiconductor Characterization System). Figure. 3.1 shows the cross-section view of Cu/TaO_X/Co resistive switching device with layer thicknesses specified.

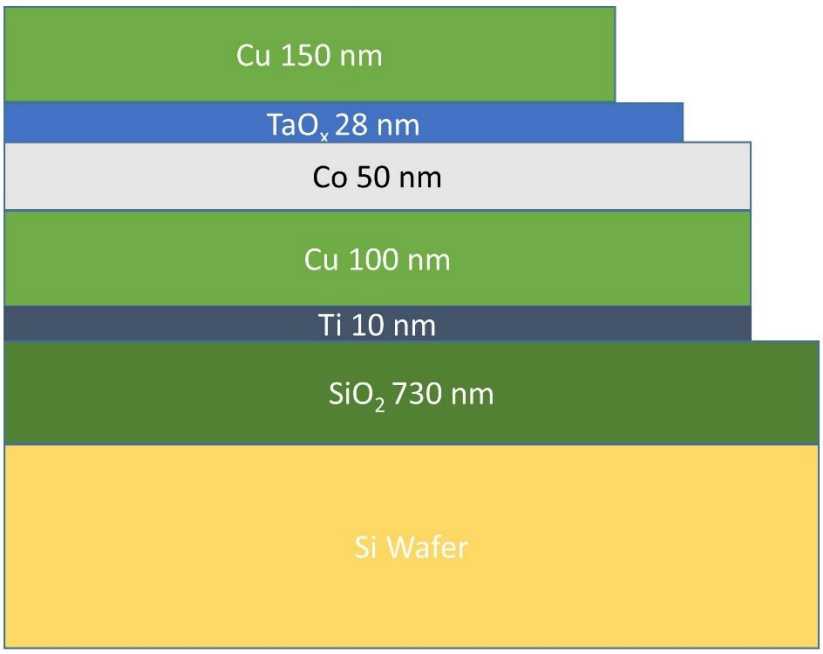

Figure. 3.1 Cross-section view of Cu/TaO_X/Co resistive switching device with layer thicknesses specified.

3.3 Characterization Methodology

The Cu/TaO_X/Co devices have been characterized by an established methodology of ReRAM devices in Dr. Orlowski's group.[12] A positive voltage is applied to the top electrode starting at 0 V at a voltage ramp rate (rr=2 V/s), while the current through the device is being monitored. When the voltage reaches a critical threshold voltage V_{FORM} (or V_{SET}), the current increases very precipitously, showing that the device is transitioned from highly resistive to the highly conductive state. In general, to avoid a permanent damage to the device, a compliance current I_{CC} is applied to limit the current flowing through the device. Then, the voltage ramp is reversed and the device shows ohmic behavior in the on-state characterized by resistance R_{ON}. When the

voltage sweep is in the negative bias and reaches a critical threshold voltage V_{RESET} at a critical current I_{RESET}, the low resistance filament is ruptured, and the device reverts from the low resistance on-state to the off-state characterized by a high resistance, R_{OFF}. I-V characteristics of resistive Cu/TaO_X/Co devices were measured by a Keithley 4200-SCS (Semiconductor Characterization System). In our measurements, the bias voltage is applied to the top Cu electrode while the bottom Co electrode is grounded. When a positive voltage is applied to the top electrode, Cu^+ cations are generated at top electrode/Solid electrolyte interface, are dissolved in the oxide layer, and can migrate in the electric field through the solid electrolyte. When Cu^+ cations reach inert electrode (bottom electrode), they are electrochemically reduced on the Co cathode. As more and more Cu atoms accumulate on the TaO_X/Co interface over time, a nanoscale filament forms a conductive path between two electrodes.

3.4 Switching Characteristics of Cu/TaO_X/Co Devices

The Cu/TaO_X/Co devices have been electrically characterized in standard characterization method. Table 3.1 give the statistics mean values for critical threshold voltages of the Cu/TaO_X/Co devices. During the voltage sweeps a ramp rate of rr=2 V/s has been used. From our data, we can obtain a mean V_{FORM} = 4.71 V for the forming voltage, when the filament is being formed for the first time, with a standard deviation σ = 2.20 V and a mean of V_{SET} = 2.67 V for the subsequent setting of the device with a standard deviation σ = 1.68 V.

Positive Bias	V_{FORM}	V_{SET}	V_{REEST}
Average (V)	4.71	2.67	-0.97
Standard Deviation	2.20	1.68	0.60

Table. 3.1 Statistics data of V_{FORM}, V_{SET} and V_{RESET} of Co devices with a positive bias.

Compared with typical Pt device, Co devices have a slightly higher forming voltage V_{FORM} (Co) = 4.71 V vs V_{FORM} (Pt) = 4.5 V. However, the distribution of the forming voltages for Pt devices is much tighter with σ = 0.7 V whereas the distribution of V_{FORM} for Co devices is σ = 2.2 V. Likewise, the on-state resistance, R_{ON} in Co devices also appears to be controlled by the I_{CC}. via the relation $\mathrm{R_{ON}} = \mathrm{A/I_{CC}}^{\mathrm{n}}$ as in the Pt devices. The conductive filament (CF) is ruptured when high enough critical current I_{RESET} is flowing through the filament due to the Joules heating at the threshold voltage V_{RESET}. The Cu/TaO_X/Co devices has a mean of V_{RESET} = -0.97 V with a standard deviation σ = 0.60 V. Thus, all the critical voltage parameters of the Co devices are only slightly different with the Pt devices (V_{FORM} = 4.7 V, V_{SET} = 2.8 V, V_{RESET} = -0.9V).[20] During the forming operation, the electric field causes migration of Cu^+ cations that have been created at the Cu/solid electrolyte interface in the so called redox reaction

$$\mathrm{Cu} \longleftrightarrow \mathrm{Cu^+} + \mathrm{e^-}$$

and transports the Cu^+ cation toward the inert Co/Pt electrode. This electric field is a superposition of an applied electric field and a build in electric field, which is the difference between work function of the active and the inert electrode divided by the thickness of solid electrolyte. Previous study shows that the fields responsible for Cu filament formation are

around a few of 10^6 V/cm at room temperature.[21] In the Co case, $\mathrm{E(Co)} = \frac{\Delta\phi(\mathrm{Co,Cu})+\mathrm{V_{FORM}(Co)}}{28\ \mathrm{nm}} \approx 1.8 \times 10^6\ \mathrm{V/cm}$, while for Pt devices, $\mathrm{E(Pt)} = \frac{\Delta\phi(\mathrm{Pt,Cu})+\mathrm{V_{FORM}(Pt)}}{25\ \mathrm{nm}} \approx 2.5 \times 10^6\ \mathrm{V/cm}$, both of which are satisfied with the requirement for electric field. The lower effective electric field of Co devices is explained by the lower work function difference between Cu on Co than that between Cu and Pt. The effective electrical field depends also on the roughness of the metals. Our results on V_{FORM} for both devices lead us to hypothesize that the Co surface roughness may be higher than the roughness of Pt surface, which is equivalent to the reduction of the effective thickness of the TaO_X layer.[20]

Negative Bias	V_{FORM}	V_{SET}	V_{REEST}
Average (V)	-2.17	-1.49	0.788
Standard Deviation	1.12	0.73	0.32

Table. 3.2. Statistics data of V_{FORM}, V_{SET} and V_{RESET} of Co devices with a negative bias.

Figure 3.2 shows a typical FORM, SET and RESET bipolar operation for Cu conductive filament in (CF) Cu/TaO_X/Co device with positive bias. The V_{FORM} = 5.3 V and V_{SET} = 1.8 V at I_{CC} = 100 µA and V_{RESET} = -0.89 V. The bipolar switching cycles have been repeated on Cu/TaO_X/Co devices, while most devices are becoming not resettable after few set-reset operations with maximum cycles of 10. After a few switching cycles, the failure of the Co devices may be related to the geometry of the Cu filament.

A conductive filament can be also formed when a negative voltage bias is applied to the copper electrode. It is known form literature[22, 23] that in this case the filament formed in TaO_X consists

of metal oxide defects, so called oxygen vacancies, V_O. Subsequently, we report on the characterization of Co devices with V_O filament.

Applying a negative voltage to the Co device, we obtain a mean V_{FORM} = -2.17 V with a standard deviation σ = 1.12 V, a mean V_{SET} = -1.49 V with a standard deviation σ = 0.73 V and average V_{RESET} = 0.79 V with a standard deviation σ = 0.32 V. All the critical voltage parameters of the Co devices are considerably lower than the Pt devices (V_{FORM} = -4 V, V_{SET} = -2 V). The significant difference of V_{FORM} and V_{SET} ((ΔV_{FORM} = 1.83 V, ΔV_{SET} = 0.5 V) between Co device and Pt device can be partially explained by the work function difference (ΔV_{WF} =1.35 V) between Co (5.0 V) and Pt (6.35). In case of Pt devices, the high work function difference between Cu and Pt establishes a field, which is opposed to V_O formation. In case of Co, this built-in field is close to zero and therefore the forming and reset voltages are significantly smaller.

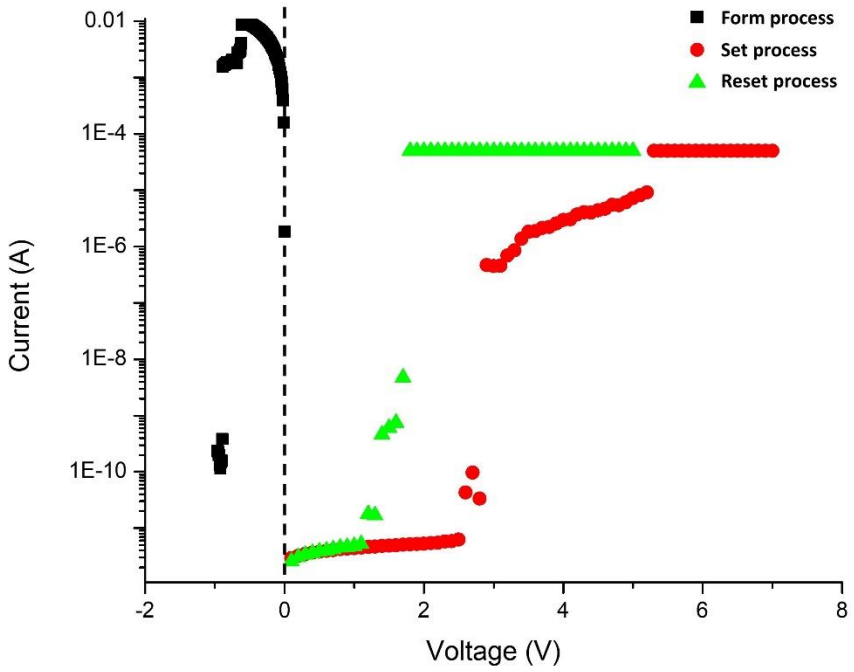

Figure. 3.2. The bipolar switching of FORM, SET and RESET operation with positive bias for a Cu/TaO$_X$/Co device on a logarithmic current scale with V_{FORM} = 5.3 V, V_{SET} = 1.8 V and V_{RESET} = -0.89 V.

Figure 3.3 shows a typical FORM, SET and RESET bipolar operation for Cu conductive filament in (CF) Cu/TaO$_X$/Co device with negative bias. The V_{FORM} = -2.8 V and V_{SET} = -0.9 V at I_{CC} = 100 µA and V_{RESET} = 0.36 V.

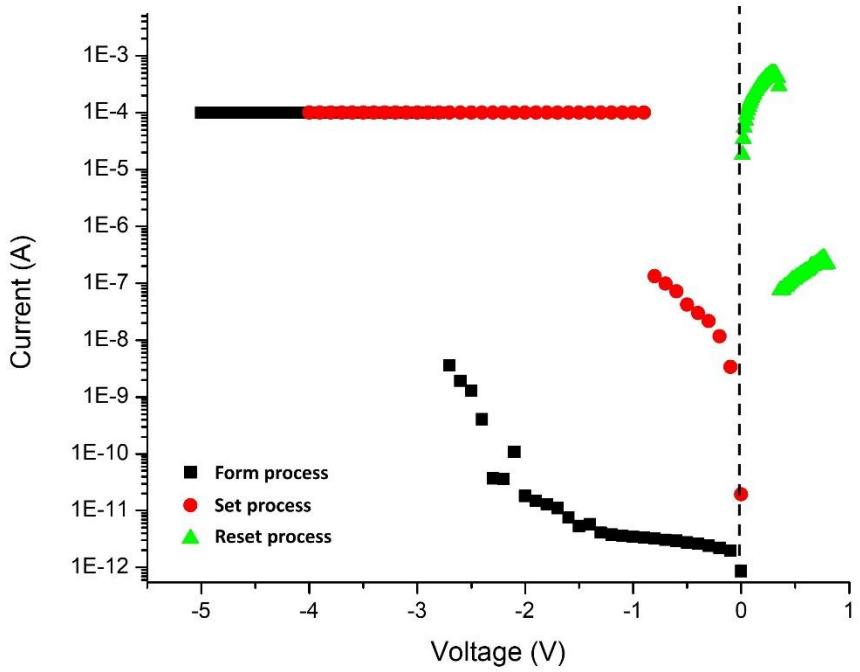

Figure. 3.3 The bipolar switching of FORM, SET and RESET operation with negative bias for a Cu/TaO$_X$/Co device on a logarithmic current scale with V_{FORM} = -2.8 V, V_{SET} = -0.9 V and V_{RESET} = 0.36 V.

Like Pt devices, R_{ON} for Co devices also depends on the compliance current (I_{CC}). It can be seen from Figure. 3.4 (a) that on a double logarithmic scale, R_{ON} also decreases linearly with the increase I_{CC} that satisfies the following equation. (1):

$$R_{ON} = \frac{A}{I_{cc}{}^{n}} \qquad (1)$$

As shown in Figure. 3.4 (a), the extracted parameter A is 0.13 V and exponent parameter n = 0.98 are obtained by curve fitting for the Cu filament. The voltage sweep rate rr = 2 V/s is used during the set operation. The value of A (Cu filament) of 0.13 V, which is slightly smaller than Pt

device (A = 0.17 V) under the same condition, can be interpreted as the lowest possible V_{SET} voltage, required to switch the memory form off-state to on-state, can be extracted using small voltage sweep rates.[22, 24]

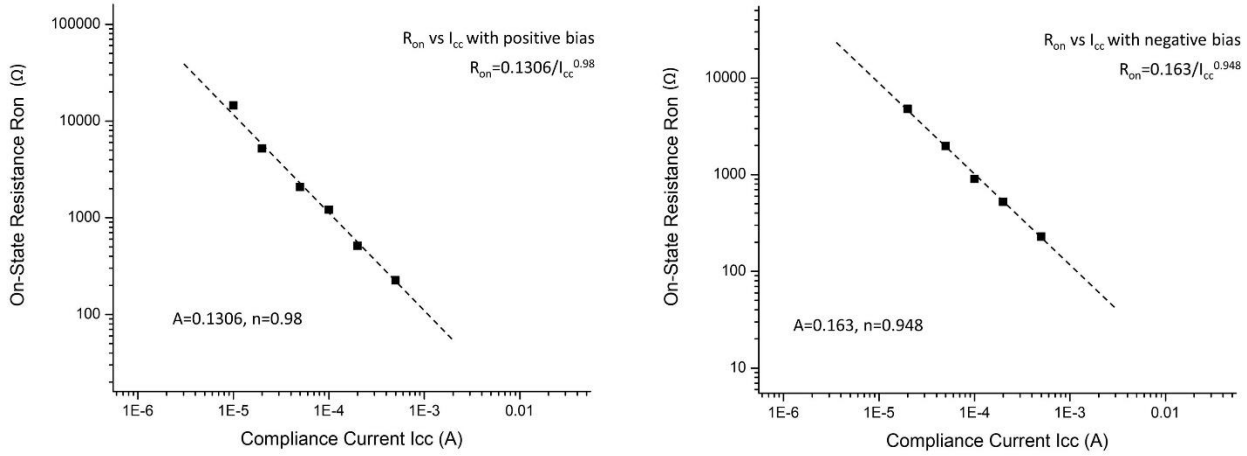

Figure. 3.4 (a) Dependence of on-resistance, R_{ON}, on compliance current, I_{CC}, for Cu conductive filament (CF) in the Cu/TaO_X/Co device, with a parameter A = 0.13 V and n = 0.98. (b) Dependence of on-resistance, R_{ON}, on compliance current, I_{CC}, for oxygen vacancy (V_O) conductive filament (CF) in the Cu/TaO_X/Co device, with a parameter A = 0.16 V and n = 0.95.

The extracted parameter A is 0.16 V and exponent parameter n = 0.95 for oxygen vacancy (V_O) CF, as shown in Figure. 3. 4 (b). The voltage sweep rate rr = 2 V/s is used during the set operation. The parameter A for oxygen vacancy (V_O) CFs is 0.16 slightly larger than that of Cu CFs. In contrast to metallic Cu CFs, where the exponent n for various devices is found universally to be 1, we find the n= 0.95 for oxygen vacancy (V_O) CFs.

3.5 Limited Switching Cycles of Cu/TaO_X/Co Devices

Compared with Pt devices that can be switched repeated back and forth, the major drawback of the Co device is that it is non-resettable after several set-reset cycles (maximum 10) and sometime even after first one or two set operation when the set process is operated at high I_{CC}. Another phenomenon shared with Pt devices, it is very difficult to set the device at low I_{CC} (smaller than 10 μA), which is similar with Pt and Ru devices. Figure. 3.5 shows the trend of average cycles with the increasing of I_{CC}. The failure of Co devices after several switching cycles is likely to be related to the geometrical shape of the Cu filament. The altered shape of the filament is attributed to the reduced stopping power of Co with respect to Cu diffusion compared with the stopping power of Pt. Reduced stopping power means Cu loss into the Co electrode which results in a reduced base of the filament with the inert electrode which drives the geometry of the filament to a cylindrical shape. Because of the reduced topping power in Co device, not all Cu^+ ions are stopped sharply at the Co interface but some may migrate into the Co electrode.

During the set and reset operations, a substantial local heating of the filament takes place. The maximum temperature has been estimated to been 600 ^oC and 1000 ^oC.[25-28] Regner and Malen have argued that because of the nm dimensions of the filament the thermal transport is non-diffusive and the differential Fourier equation of heat transport is grossly inadequate. The solution of the more adequate Boltzmann transport equation leads to much higher temperature with estimates as high as 1000 ^oC. Our hypothesis is that such high temperature even at relatively short times of microseconds up to seconds can lead to the formation of an alloy of Cu_XCo_{1-X}.[29] According to the Co-Cu diagram, the stoichiometric ratio x in Cu_XCo_{1-X} can be

as high as 0.1 at temperature of 1000 ^{o}C.[30-33] The high temperature makes the Cu atoms at the bottom of Cu filament easily migrate into the Co layer. Besides, the Co layer, in turn, can undergo, at such high temperature, local crystallization creating grains and grain boundaries, which pathways for the diffusion of Cu atoms.[34, 35] At the same time, the loss of Cu at the base of the Cu filament, leads to a different geometry of the filament. Whereas with a nearly perfect shopping power, the shape of the filament in the Pt device can be assumed to be conical with more or less sharp tip at the Cu electrode, the shape of the Cu filament in the Co device may be hypothesized as more cylinder-like. It is known that filaments without pronounced constriction are more difficult to rupture by Joule heat, which explains the limited switching cycles of the Co device.[20]

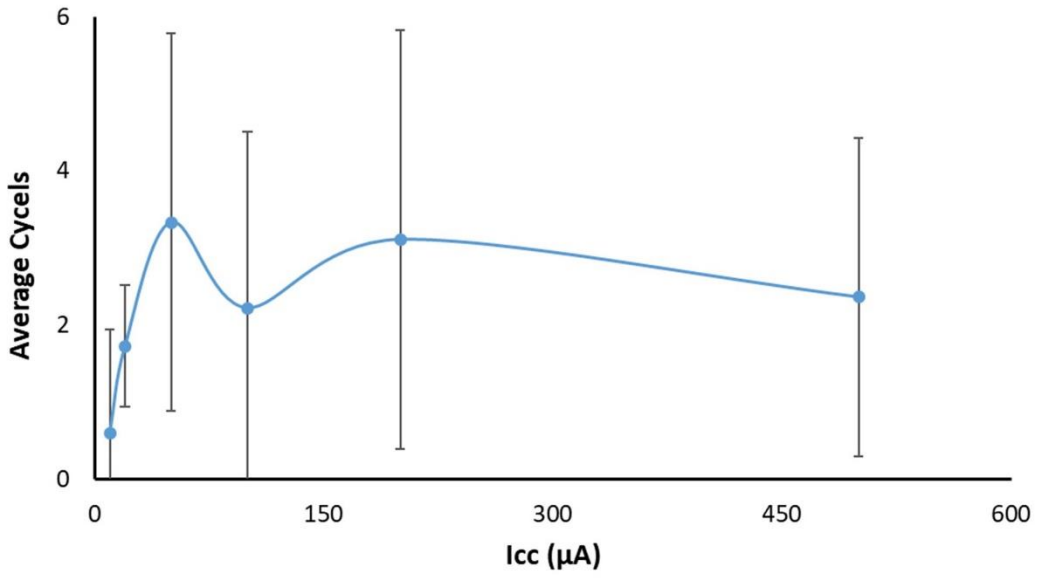

Figure. 3.5 The average cycles of the Co device change with the increasing of I_{CC}. The error bar is the standard deviation of the cycles.

When compared to the R_{ON} of Pt devices, the R_{ON} of Co devices are lower for the same I_{CC}. Since during the reset process the power dissipated in the filament is equal to $I_{RESET}{}^2 \times R_{ON}$, the highest temperature is reached in the constriction at the top of the cone, where the rupture of the filament happens, as shown in Figure. 3.6(a). At High I_{CC} (as shown in Figure. 3.3, Ron vs I_{CC}) the Ron decreases sharply by adding Cu atoms to the upper section of the cone. Therefore, the sharp of the filament becomes more and more cylindrical as shown in Figure.3.6(c). In this case, the maximum temperature, in absence of any pronounced constriction, is reached in the middle section of the cylinder, where the low resistance is relatively strong. Hence, rupturing of the filament becomes difficult.

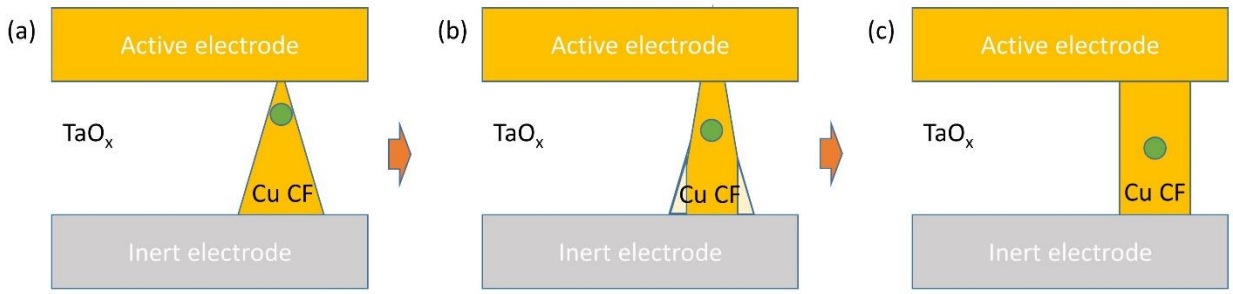

Figure. 3.6 Location of the highest temperature due to the Joules heating during reset operation. (a) Cone-like shape of the filament with maximum temperature at the top of the filament. (b) The middle stage of the geometrical change from cone-like shape to cylinder-like shape of the filament with maximum temperature. (c) cylinder-like shape of the filament with maximum temperature in the middle of the filament.

3.6 Retention Degradation Study of Cu/TaO_X/Co Devices

The retention is another drawback of the Cu/TaO_X/Co devices. The retention properties of this type of device has been characterized at room temperature as shown Figure. 3.8 a and b (1 means on-state characterized by R_{ON}, 0 means off-state, characterized R_{OFF}). The characterization has been done at a sweep rate rr = 2 V/s from 0V to 5 V and the current has been monitored during the set operation with a time separation of 10 minutes, 30 minutes, 1 hours, 2 hours, 12 hours, 24 hours and 48 hours. Figure 3.8.a shows the on-state of a Cu CF based Cu/TaO_X/Co device with a retention time up to two hours. While, the on-state of a V_O based Cu/TaO_X/Co device owns a higher retention time up to 12 hours, which is similar to a Pt device. Thus, the retention of the V_O filament is much higher than of the Cu filament.

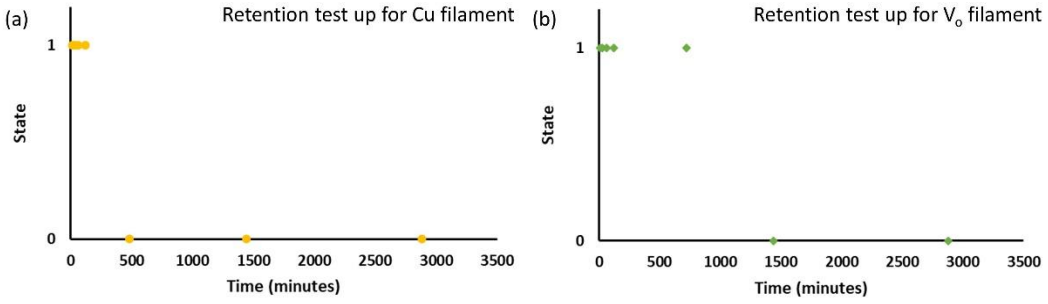

Figure. 3.7 (a) The retention test of Cu filament at room temperature. (b) The retention test of V_O filament at room temperature.

The lower retention time of Cu filament of Co device compared to the Ru and Pt device is mainly due to the after several operation cycles, the heat accumulated in the Cu filament makes the Cu atoms migrate into the Co layer. Besides, the chemical degradation of Cu also

remove the Cu atoms from the Cu filament. The loss of Cu atoms makes the Cu filament thinner and thinner until the filament ruptured.

3.7 Conclusion

Compared to Cu/TaO_X/Pt devices, Cu/TaO_X/Co device exhibits very similar form, set and reset voltages for the Cu filament. However, for the V_O filament the Co device has a significant smaller form, set and reset voltages of V_O filament, which can be partly attributed to the work function difference between Pt and Co of 1.35 V and partly to the impaired integrity properties of Co vs Pt inert electrode. As in the case of Pt and Ru devices, the on-state resistance of the Co devices is limited by the compliance current (I_{CC}) and conforms to the equation (1). The performance deterioration of Co devices is particularly conspicuous when the cell is exposed to high Joules heat dissipation. With high Joules heat accumulation, the maximum switching cycles of Co devices is up to 8 times, while in the case of Pt cases, it is almost unlimited. The properties of Co electrode appears to have a major impact on the Cu diffusional fluxes, which in turn, determine the geometrical shape of the Cu conductive filament. The Pt electrode with its excellent stopping power and amorphous structure produces a conical CF with a sharp constriction near the Cu electrode interface, whereas in case of Co electrode, the loss Cu ions at the base of the Cu filament may lead to a more cylindrical shape of the filament which is more difficult to be ruptured in a reset operation.

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Chapter 4

Investigation of Polymer based ReRAM devices

4.1 Introduction

A successful development of flexible electronics require new types of flexible volatile or nonvolatile memories with novel organic materials.[1-3] Among the new types of novel memory including FeRAM, MRAM, PCM and ReRAM,[4-6] resistive switching random access memory (ReRAM) is the most promising candidate for a flexible memory, as a variety of materials can be used both inorganic, organic and even hybrid nanocomposites.[7-16] Organic material-based ReRAM is emerging non-volatile memory with miscellaneous advantages, such as flexibility, printability, transparency, compatibility with various substrates, and variable form processing capabilities.[16-21]

Recently, various organic materials including polymers have been used in non-volatile memory elements having resistive behavior.[22-24] Among them, polymer solid electrolytes have shown a great promise as constitutive materials for the inorganic electrolytes of ReRAM devices because polymers are flexible, biocompatible and inexpensive as well as environmentally friendly.[25] Poly o-anthranilic acid (O-AA), polymethylmethacrylate (PMMA) and Poly(N-vinylcarbazole) (PVK) are the most well studied polymer solid electrolyte in the literature.[26-31] However, much of the previous research has focused almost exclusively on the solid electrolyte layer (called also the

switching layer) of the ReRAM device, and only a handful of articles have addressed the possibility of replacing the active and inert metallic electrode by such an organic layer.

In this work, we report the first organic ReRAM based on Cu-doped organic material, here: PANI-CSA, as the top electrode, and O-AA as the polymer solid electrolyte as the switching layer. The PANI-CSA is most widely investigated and used conductive polymer electrode for the potential conductive electrode application of molecular sensing, optical electronics and flexible electronics due to environmental stability, ease preparation, low cost and relative high conductivity.[32-34] The Cu doping of the polymer electrode improves not only the conductivity of the electrode but also provides Cu^{+} ions as building blocks for the formation of Cu filament in the ReRAM devices.[35-37] O-AA has been employed as the switching layer due to its water solubility and easy synthesis method.[26, 38, 39] For the bottom electrode, we choose Aluminum (Al) due to its low melting temperature, high conductivity and affordability. The ReRAM device, which has been manufactured with Cu-doped PANI-CSA/O-AA/Al as the top active electrode, exhibits bipolar memory I-V characteristics. By controlling of the concentration of Cu and the thickness of the top electrode, our results demonstrate that the switching behavior of the polymer ReRAM device is enabled by the availability of Cu^{+} ions provided by the top electrode.

4.2 Device Fabrication

Like traditional ReRAM memory cell, the bottom electrode is deposited by the e-beam PVD method and patterned with a shadow mask. On the other hand, the organic dielectric O-AA

layer and the top conductive polymer layer are deposited using the spin coating method. The cross section of the fabricated devices is shown in Figure. 4.1.

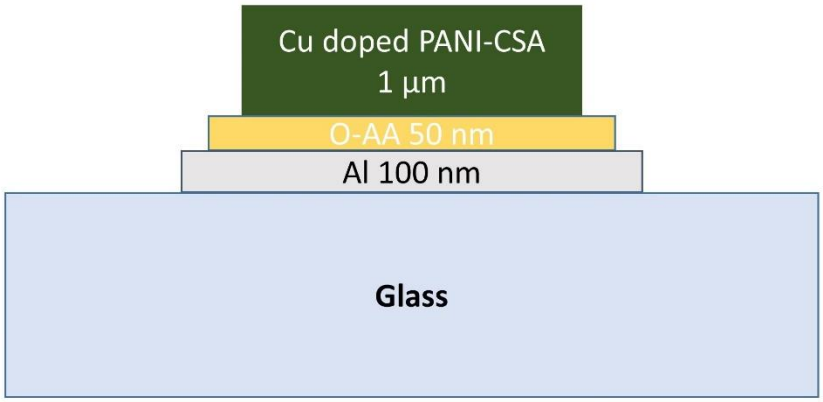

Figure. 4.1. Cross-section of polymer ReRAM device with structure of Cu-doped PANI-CSA/ O-AA/Al/Glass with the thickness of the respective layers indicated.

Deposition of the bottom electrode: A handmade physical mask is used to create a shadow mask composed of flexible and transparent plastic material. The electrode is about 22 mm in length and 3 mm in width. Then, glass slides are put in the e-beam PVD with the shadow mask to deposit the aluminum with thickness of 100 nm.

Polymer Solid Electrolyte: O-AA was prepared by first mixing 3 mL of DMF with 48.87 mL of HCl. This was then combined with 0.178 g of AA. 3.3254 mL of ANI was then added to this mixture.[38] A combination of 10 mL of APS and 50 mL HCl was then added to the mixture to produce O-AA. The polymer was collected by filtration from the solution, washed with 1.2 M HCl until the filtrate became colorless and then dried under vacuum at 20 ^{o}C, till constant

weigh.[39]39 Then, the collected polymer was dissolved in acetone with a concentration of 10 mg/ml. Finally, the solution is spin coated on the bottom electrode samples with a resolution of 1000 rpm for 60 s to create a layer of organic dielectric with a thickness about 50 nm. After getting the desired polymer solid electrolyte, the sample is then annealed at 100 ^{o}C for 60 s.

Top Electrode: The polyaniline (PANI) polymer and camphorsulfonic acid (CSA) are mixed with a mole ratio of 2:1, and then desired $Cu(BF_4)_2$ are added to the mixture with a desired weigh ratio of 6.4 mg/g.[32] Finally, all the mixture is dissolved in m-cresol to prepare a solution. The solution needs to be stirred for 3-4 days, and heated at 50 ^{o}C for 12 hours to make the solution homogenous. A thin film of Cu doped PANI-CSA was deposited on the top the sample using spin coating at a speed of 1000 rpm to create a top electrode with a thickness of 1 µm. The film was soft baked at 100 ^{o}C for 1 minute. Finally, we use the m-cresol to remove part of the top polymer electrode to explore the bottom electrode.

4.3 Device Characterization

The Cu-doped PANI-CSA/O-AA/Al devices have been characterized by an established methodology of ReRAM devices in Dr. Orlowski's group. A positive voltage is applied to the top electrode starting at 0 V at a voltage ramp rate of rr=2 V/s, while the current through the device is being monitored. When the voltage reaches a critical threshold voltage V_{FORM} (or V_{SET}), the current increases very precipitously, showing that the device is transitioned from highly resistive to a highly conductive state. In general, to avoid a permanent damage to the device, a

compliance current I_{CC} is applied to limit the current flowing through the device. Then, the voltage ramp is reversed and the device shows ohmic behavior in the on-state characterized by a resistance R_{ON}. When the device voltage sweep is in the negative bias and reaches a critical threshold voltage V_{RESET} at a critical current I_{RESET}, the low resistance filament is ruptured, and the device reverts from the low resistance on state to the off-state characterized by a high resistance, R_{OFF}. I-V characteristics of polymer devices were measured by a Keithley 4200-SCS (Semiconductor Characterization System). In our measurements, the bias voltage is applied to the top Cu-doped PANI-CSA electrode while the bottom Al electrode is grounded. Refer here to the schematic figure of the set and reset from chapter 3.

4.4 Results and Discussion

One of the most important issues of the polymer ReRAM is sufficiently high conductivity of the top polymer electrode. In order to investigate how the conductivity of the PANI-CSA material depends on the concentration of Cu, we have adjusted the amount of $Cu(BF_4)_2$, while 4 samples of PANI-CSA (6 mg/ml) have been prepared. We have chosen four Cu contents of 0, 6.4 mg/g, 12.8 mg/g to 64 mg/g as a Cu doping and labeled the samples 1, 2, 3 and 4, respectively. The electric conductivity of these samples has been measured by the four probe methods, and the results are shown in Table. 4.1. The conductivity as a function of the Cu content increases first a little bit (from 0 mg/g to 6.4 mg/g) and then decreases with the increasing amount of copper content. The decrease of conductivity with the Cu contents is a little bit surprising, but could be explained by the role of the BF_4^- compound, which may act as an electron trap. In ref. [37], it

has been shown that the addition of copper to the PANI polymer can substantially change the morphology and structure of the polymers, thereby modifying also other properties such as conductivity and electrocatalytic activity.[37] Our hypothesis is that the presence of BF_4^- in sufficient quantities may decrease the conductivity of the polymer by immobilizing the free electrons. From Table. 4.1, it can be seen that sample 2 (6.4 mg/g) exhibits the highest conductivity while sample 4 has the lowest conductivity. Therefore, for further manufacturing, we have prepared two polymers electrodes with copper content of 6.4 mg/g and 12.8 mg/g and the doping of 64 mg/g has been not further pursued.

	solvent	Concentration(PANI)	More ratio (PANI:CSA)	Cu concentration	Spin coating speed	After 100 °C annealing 1 min	thickness	Conductivity (S/m)
sample1	M-cresol	6 mg/ml	1:2	0	1000 rpm	7.47 kΩ/□	70 nm	1.91 k
sample2	M-cresol	6 mg/ml	1:2	6.4 mg/g	1000 rpm	7.2 kΩ/□	64 nm	2.17 k
sample3	M-cresol	6 mg/ml	1:2	12.8 mg/g	1000 rpm	6.6 kΩ/□	86 nm	1.76 k
sample4	M-cresol	6 mg/ml	1:2	64 mg/g	1000 rpm	10.93 kΩ/□	84 nm	1.09 k

Table.4.1 The conductivity of Cu doped PANI-CSA changed with concentration of Cu^+ ions.

After the polymer device have been manufactured, it has been characterized electrically using standard characterization methods. After having tested several devices, we obtain a mean value of the forming voltage of V_{FORM} = 2.94 V, a mean value for the set voltage of V_{SET} = 2.74 V and a mean reset voltage of V_{RESET} = -1.01 V. Compared to inorganic ReRAM devices, such as Cu/TaO_X/Pt, we observed that the forming voltage is quite low (compared with 5 V for Cu/TaO_X/Pt and 7 V for Cu/TaO_X/Ru with a significantly thinner dielectric [TaO_X thickness of 25 nm]).[40] The significant smaller forming voltage is likely due to the high diffusivity of Cu in the O-

AA layer. The work function difference cannot account for the low values of V_{FORM} as the work function between Cu-doped PANI-CSA and Al is almost zero and thus much smaller than the work function difference between Cu and Pt of 1.6 eV, which establishes a built-in electric field in support of Cu filament formation.[41]

Figure 4.2 shows a typical FORM, SET and RESET bipolar operation for Cu conductive filament in Cu-doped PANI-CSA/O-AA/Al device with positive bias. The V_{FORM} = 3.1 V and V_{SET} = 1.4 V at I_{CC} = 100 µA and V_{RESET} = -0.89 V. The bipolar switching cycles have been repeated on polymer devices, while most devices are becoming not resettable after few set-reset cycles with maximum cycles up to three. Our hypothesis for the limited endurance of the polymer devices after a few switching cycles is that the top polymer electrode (PANI-CSA) and the polymer solid electrolyte (O-AA) are both based on the chemical aniline. During the set-reset operation, the electric field may help the merge of PANI-CSA layer and O-AA layer expedited by the deposited Joule heat, which creates an unresettable permanent Cu filament-polymer matrix melted connection in the device.

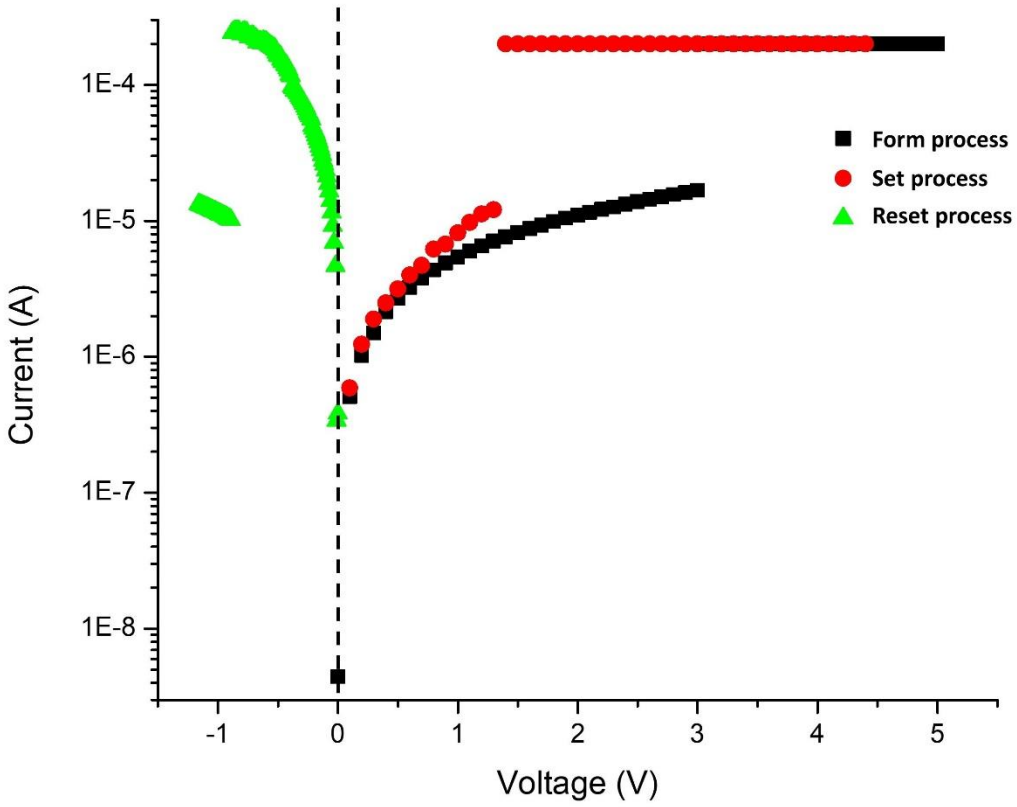

Figure. 4. 2. The bipolar switching of FORM, SET and RESET operation with positive bias for a polymer device on a logarithmic current scale with V_{FORM} = 3.1 V, V_{SET} = 1.4 V and V_{RESET} = -0.89 V.

We find that, like inorganic devices (e.g. Cu/TaO_X/Pt), R_{ON} for polymer devices depends on the magnitude of the compliance current (I_{CC}). It can be seen from Figure. 4.3 that on a double logarithmic scale, R_{ON} also decreases linearly with the increase I_{CC} and satisfies the following equation. (1):

$$R_{ON} = \frac{A}{I_{cc}{}^{n}} \qquad (1)$$

As shown in Figure. 4.3, the extracted parameter A is 0.286 V and exponent parameter n = 0.919 are obtained by curve fitting. The voltage sweep rate rr = 2 V/s is used during the set operation. The value of the constant A (Cu filament) of 0.286 V, which is slightly smaller than inorganic device (A almost equals 0.1) under the same condition, can be interpreted as the lowest possible V_{SET} voltage, required to switch the memory form off-state to on-state, which can be extracted using small voltage sweep rates.

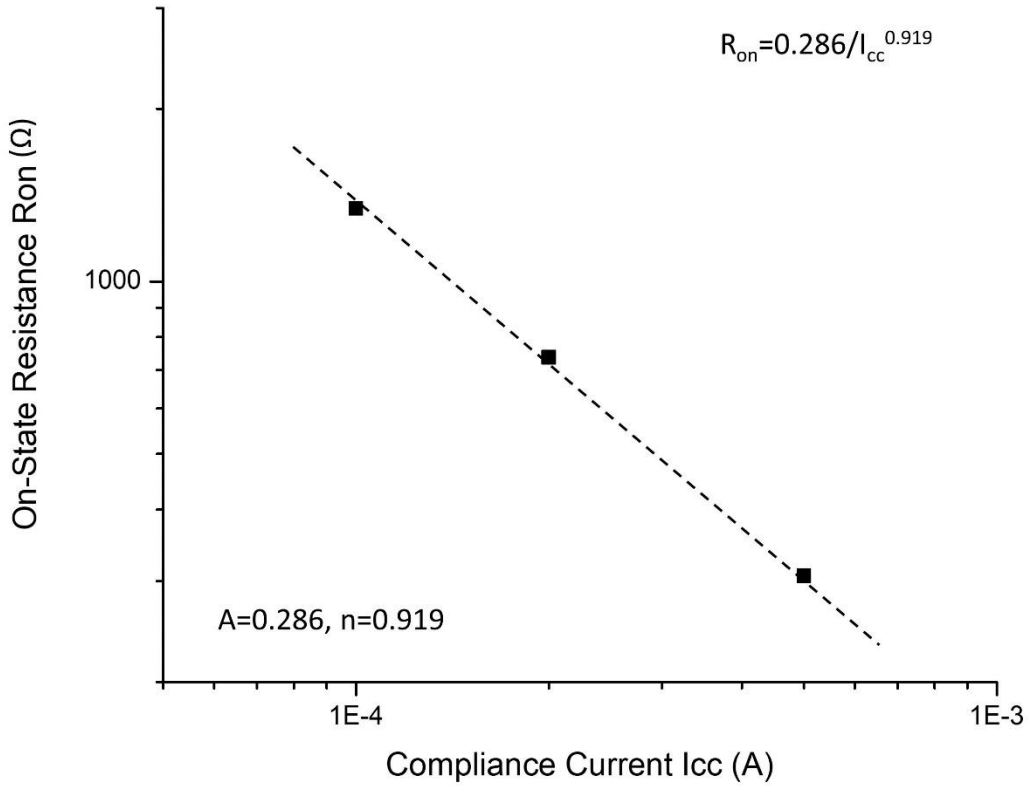

Figure. 4.3 Dependence of on-resistance, R_{ON}, on compliance current, I_{CC}, for Cu conductive filament (CF) in the polymer device, with a parameter A = 0.286 V and n = 0.919.

In order to investigate how the concentration of Cu^+ ions in the polymer electrode may influence the switching behavior of the polymer devices, we have prepared three devices with three different concentrations of Cu^+ ions from 0, 6.4 mg/g to 12.8 mg/g with the same thickness of 1 µm. Figure. 4.4 shows that the polymer device exhibits resistive switching only when the concentration of Cu^+ ions is non zero (*i.e.* for non-zero Cu contents). Apparently, the Cu doping provides the Cu^+ ions needed as building blocks for the formation of the Cu filament in the organic solid electrolyte O-AA. In Figure. 4. 4, it can be seen that for undoped polymer electrode no sharp transition from highly resistive to a low resistive state can be observed. It can be also seen that for the higher Cu concentration corresponding to 12.8 mg/g, the V_{FORM} (12.8 mg/g) = 3.0 V is slightly smaller than for the Cu concentration for 6.4 mg/g V_{FORM} (6.4 mg/g) = 3.2 V. This may be explained by the larger supply of Cu^+ ions in case of 12.8 mg/g than for 6.4 mg/g for the formation of the Cu filament.

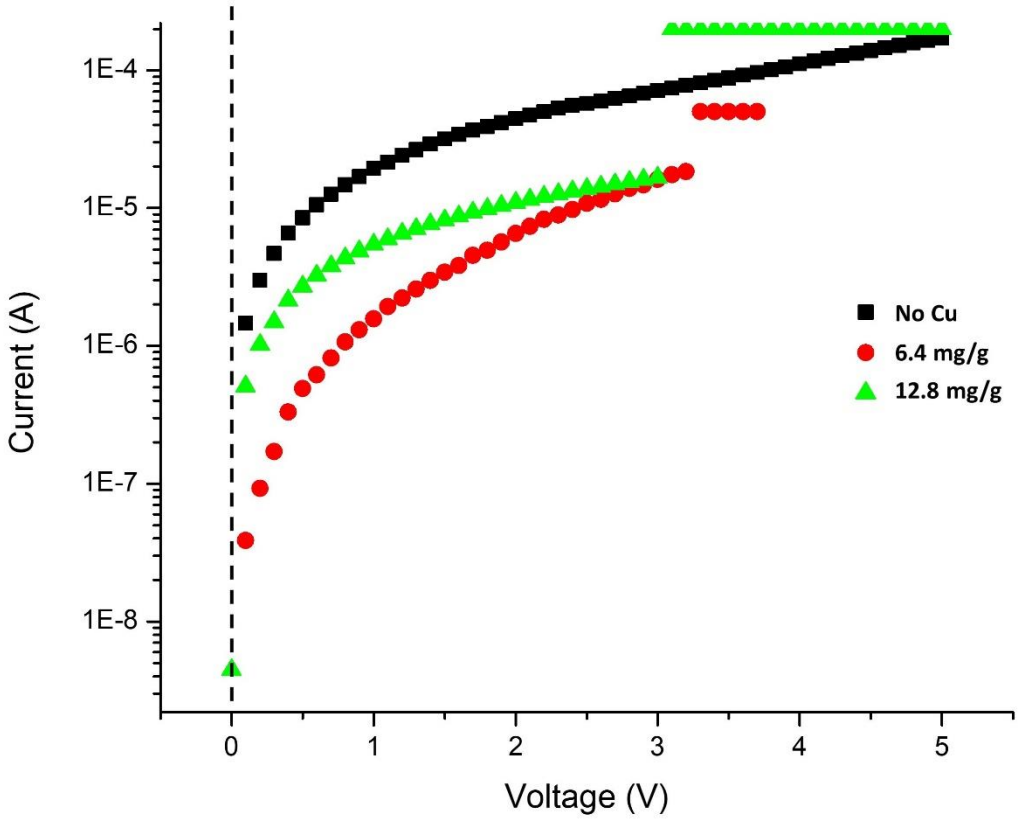

Figure. 4.4 The FORM operation of polymer devices with different concentration of Cu^+ ions. Black: Without doping Cu^+ ions. Red: Doped with 6.4 mg/g Cu^+ ions. Green: Doped with 12.8 mg/g Cu^+ ions.

Furthermore, the thickness of the top polymer electrode layer also have an influence on the FORM operation of the conductive filament in the polymer solid electrolyte. Figure. 4. 5 shows the dependence of the FORM operation of the polymer devices on the thickness of the top polymer electrode layer. Three thickness have been selected: 250 nm, 500 nm and 1000 nm with the Cu concentration of 6.4 mg/g. As can be seen from Figure. 4. 5, the forming operation can be observed only for an electrode of 1000 nm thickness, with a forming voltage $V_{form} \cong$

2.8 V. Apparently, the thick top electrode has a sufficient supply of copper to establish a Cu filament across the O-AA layer. Together with our hypothesis started before that the Cu diffusion appears to be fast across O-AA layer, this indicates that in our organic ReRAM devices the formation of the Cu filament is supply-limited and not transport-limited.

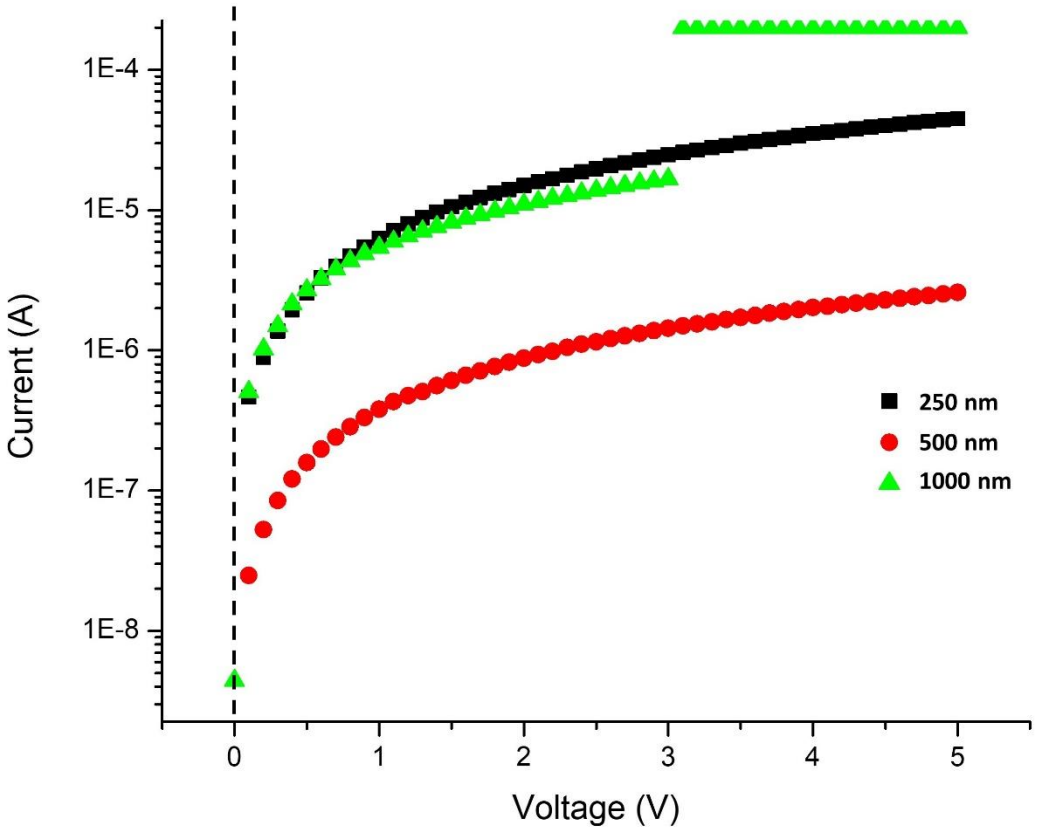

Figure. 4.5 The FORM operation of polymer devices with different thickness of top polymer electrode. Black: Thickness of 250 nm. Red: Thickness of 500 nm. Green: Thickness of 1000 nm. A sharp transition can be observed only with the electrode thickness of 1000 nm.

4.5 Conclusion

Cu-doped PANI-CSA polymer electrode has been introduced for the first time as top polymer electrode of a ReRAM device. We have manufactured ReRAM based on PANI-CSA and O-AA, which operate at significantly lower forming voltage than inorganic devices such as Cu/TaO_X/Pt. Our results demonstrate that our organic ReRAM is a promising candidate for inexpensive and environmentally friendly memory devices. We have demonstrated that R_{ON} for polymer devices obey the same relation with the compliance current (I_{CC}) as its much more researched inorganic counterparts. We have demonstrated that the FORM operation of polymer devices depends on the concentration of Cu^+ ions in the PANI-CSA electrode. The polymer device can be operated with sufficiently high concentration of Cu^+ ions (in our case 6.4 mg/g, but possibly lower). Finally, the thickness of the top polymer electrode layer has also an impact on the forming voltage of the conductive filament in the polymer solid electrolyte. The FORM operation can be only observed when minimum thickness of polymer electrode is sufficiently large (larger than 500 nm and smaller than 1000 nm).

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Chapter 5

Conclusion and Future Work

In this work we have manufactured and electrically characterized ReRAM memory devices with inorganic and organic materials. The novelty of the inorganic devices is that we have for the first time manufactured and Cu/TaO_X device with cobalt as an inert electrode. Because of prevalent use of cobalt in CMOS technology such a device is of great interest for co-integration of non-volatile memory within the CMOS metallization architecture. The novelty of the organic device is that we have demonstrated that an organic PANI-CSA polymer doped with Cu can serve successfully as the active electrode and provide Cu^+ as building blocks for the conductive filament between the electrodes.

5.1 Resistive Memory Device Based on Co Electrode

In first part of our investigation, we fabricated resistive switching memory (ReRAM) with a Co as a bottom electrode and characterized the device electrically. We have found very similar switching behavior as for the well-characterized Cu/TaO_X/Pt device. The form, set and reset voltages for the Co device are very close the corresponding values for the Pt device.

	V_{FORM} (V)	V_{SET} (V)	V_{REEST} (V)
Co devices	4.71	2.67	-0.97
Pt devices	4.7	2.8	-0.9

Table. 5.1 The mean values of FORM SET and RESET voltages of Co devices and Pt devices.

Also the relation between the R_{on} resistance and the compliance current I_{CC},

$$R_{on}=A/I_{CC}^{n} \qquad (1)$$

imposed during the form and set operations looks very similar with similar values for the constant A and the exponent n.

However, in terms of endurance with respect to the number of sequential switching cycles, the Co device is far inferior to the Pt device. Whereas, the Pt device can be switched virtually infinitely frequently the maximum number of switching cycles in the Co device is limited to 10 at the same switching condtions.

This performance deterioration of Co devices is particularly severe when the cell is exposed to high Joules heat dissipation. This indicates that the Co has degraded inertness properties compared with the Pt device. The diminished inertness of the Co layer leads likely to Cu loss into the C o layer either via a Co-Cu alloy compound formation, or by Cu diffusion along the Co grain boundaries, or to excessive surface diffusion of Cu along the Co surface, or by a combination of those three mechanisms. This Cu loss from the filament at the TaO_X/Co interface drives the shape of the nanofilament from a conical shape to a cylindrical shape which are known to be difficult to rupture.

5.2 Organic Resistive Memory Device

In the second part of the present work, we have manufactured Cu doped PANI-CSA polymer electrode as the top polymer electrode of ReRAM. For the dielectric switching layer also an

organic material, O-AA, has been used, while the bottom electrode was a conventional Al electrode. Our electric characterization has demonstrated that such a device constitutes a functioning resistive switching cell with surprisingly low V_{FORM} voltage of only V_{FORM} =2.9 V. This feature makes the device particularly attractive for low voltage and low power applications. Thus, this device is a promising candidate for inexpensive and environmentally friendly memory array. The device was extensively characterized and it has been shown that the relation (1) holds also for the organic device with n of about 0.92 and constant A of 0.29 V. We have also shown that optimum doping of the top electrode is 6.4 mg/g and that the dopings of 12.8 mg/g and 64mg/g lead to degraded conductivity of the electrode. The reason for this is not entirely clear. We have also shown also that the thickness of organic active electrode has to be 1000 nm or larger and that thicknesses of 250 nm and 500 nm render the device inoperable. The reason for this is most likely that the activation of Cu to a Cu+ ion in the doped polymer is quite limited. Hence, to provide a sufficient supply of Cu+ ions the thickness of the electrode has to exceed a minimum thickness that is larger than 500 nm and smaller than 1000 nm. The down side of the device is that it can be switched on and off only a few times.

5.3 Future Work

For the inorganic device further research should aim at a deeper understanding of the poor intertness properties of the Co electrode. This could be addressed by providing more efficient metal layers as heat sink of the device to reduce the maximum temperature that the device may experience. Another avenue would be to try different glue and adhesion layers that would

retard grain crystallization of Co at elevated temperatures that the device may experience during the switching cycles.

For the organic device. The next step in this project is the development of an organic bottom electrode to replace the present Al electrode. With an organic bottom electrode a fully organic memory would have been achieved. Other avenue of research would be to look for alternatives to the Cu doping of top electrode. Cu could be replaced by Ni or Ag leading hopefully to improved endurance of the switching capability. One could also add extra layer of layer between the bottom electrode and the adhesion layer to provide an efficient heat path to remove the accumulated heat in the conductive filament from the device. In addition, for the organic device, one should explore new top polymer electrode and polymer solid electrolyte, such as PMMA and PVK. One possible promising candidate for the bottom electrode would be graphene which has been already used in Dr. Orlowski's group as a heat sink for the inorganic devices such as Cu/TaO_X/Pt but not yet in organic devices.