High Frequency Bi-directional DC/DC Converter with Integrated Magnetics for Battery Charger Application

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Abstract

Due to the concerns regarding increasing fuel cost and air pollution, plug-in electric vehicles (PEVs) are drawing more and more attention. PEVs have a rechargeable battery that can be restored to full charge by plugging to an external electrical source. However, the commercialization of the PEV is impeded by the demands of a lightweight, compact, yet efficient on-board charger system. Since the state-of-the-art Level 2 on-board charger products are largely silicon (Si)-based, they operate at less than 100 kHz switching frequency, resulting in a low power density at 3-12 W/in^3, as well as an efficiency no more than 92 - 94%

Advanced power semiconductor devices have consistently proven to be a major force in pushing the progressive development of power conversion technology. The emerging wide bandgap (WBG) material based power semiconductor devices are considered as game changing devices which can exceed the limit of Si and be used to pursue groundbreaking high frequency, high efficiency, and high power density power conversion.

Using wide bandgap devices, a novel two-stage on-board charger system architecture is proposed at first. The first stage, employing an interleaved bridgeless totem-pole AC/DC in critical conduction mode (CRM) to realize zero voltage switching (ZVS), is operated at over 300 kHz. A bi-directional CLLC resonant converter operating at 500 kHz is chosen for the second stage. Instead of using the conventional fixed 400 V DC-link voltage, a variable DC-link voltage concept is proposed to improve the efficiency within the entire battery voltage range. 1.2 kV SiC devices are adopted for the AC/DC stage and the primary

side of DC/DC stage while 650 V GaN devices are used for the secondary side of the DC/DC stage. In addition, a two-stage combined control strategy is adopted to eliminate the double line frequency ripple generated by the AC/DC stage.

The much higher operating frequency of wide bandgap devices also provides us the opportunity to use PCB winding based magnetics due to the reduced voltage-second. Compared with conventional litz-wire based transformer. The manufacture process is greatly simplified and the parasitic is much easier to control. In addition, the resonant inductors are integrated into the PCB transformer so that the total number of magnetic components is reduced. A transformer loss model based on finite element analysis is built and used to optimize the transformer loss and volume to get the best performance under high frequency operation.

Due to the larger inter-winding capacitor of PCB winding transformer, common mode noise becomes a severe issue. A symmetrical resonant converter structure as well as a symmetrical transformer structure is proposed. By utilizing the two transformer cells, the common mode current is cancelled within the transformers and the total system common mode noise can be suppressed.

In order to charge the battery faster, the single-phase on-board charger concept is extended to a higher power level. By using the three-phase interleaved CLLC resonant converter, the charging power is pushed to 12.5 kW. In addition, the integrated PCB winding transformer in single phase is also extended to the three phase. Due to the interleaving between each phase, further integration is achieved and the transformer size is further reduced.

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General Audience Abstract

Plug-in electric vehicles (PEVs) are drawing more and more attention due to the advantages of energy saving, low CO_2 emission and cost effective in the long run. The power source of PEVs is a high voltage DC rechargeable battery that can be restored to full charge by plugging to an external electrical source, during which the battery charger plays an essential role by converting the grid AC voltage to the required battery DC voltage.

Silicon based power semiconductor devices have been dominating the market over the past several decades and achieved numerous outstanding performances. As they almost reach their theatrical limit, the progress to purse the high-efficiency, high-density and high-reliability power conversion also slows down. On this avenue, the emerging wide bandgap (WBG) material based power semiconductor devices are envisioned as the game changer: they can help increase the switching frequency by a factor of ten compared with their silicon counterparts while keeping the same efficiency, resulting in a small size, lightweight yet high efficiency power converter.

With WBG devices, magnetics benefit the most from the high switching frequency. Higher switching speed means less energy to store during one switching cycle. Consequently, the size of the magnetic component can be greatly reduced. In addition, the reduced number of turns provides the opportunity to adopt print circuit board as windings. Compared with the conventional litz-wire based magnetics, planar magnetics not only can effectively reduce the converter size, but also offer improved reliability through automated manufacturing process with repeatable parasitics.

This dissertation is dedicated to address the key high-frequency oriented challenges of adopting WBG devices (including both SiC and GaN) and integrated PCB winding magnetics in the battery charger applications.

First, a novel two-stage on-board charger system architecture is proposed. The first stage employs an interleaved bridgeless totem-pole AC/DC with zero voltage switching, and a bi-directional CLLC resonant converter is chosen for the second stage.

Second, a PCB winding based transformer with integrated resonant inductors is designed, so that the total number of magnetic components is reduced and the manufacturability is greatly improved. A transformer loss model based on finite element analysis is built and employed to optimize the transformer loss and volume to get the best performance under high frequency operations.

In addition, a symmetrical resonant converter structure as well as a symmetrical transformer structure is proposed to solve the common noise issue brought by the large parasitic capacitance in PCB winding magnetics. By utilizing the two transformer cells, the common mode current is cancelled within the transformers, and the total system common mode noise can be suppressed.

Finally, the single-phase on-board charger concept is extended to a higher power level to charge the battery faster. By utilizing the three-phase interleaved CLLC resonant converter as DC/DC stage, the charging power is pushed to 12.5 kW. In addition, the integrated PCB winding magnetic in single phase is also extended to the three phase. Due to the interleaving between the three phase, further integration is achieved and the transformer size is further reduced.

To My Parents:

Jianping Cai and Jianguo Li

To My Wife

Jie Wang

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Chapter 1 **Introduction**

1.1 **Overview of electric vehicle charging**

The advancement of transportation has significantly changed the lifestyles in the past decades. While bringing enormous convenience to social activities, transportation has also consumed a large amount of energy. Currently, petroleum almost exclusively fuels the United States (US) transportation system, creating a major challenge: it represents a significant fraction of total greenhouse gas (GHG) emissions both globally and in the US — light-duty vehicles (LDVs) are responsible for 17.5% of carbon dioxide (CO2) emissions in the US [1, 2].

According to the report by Electric Power Research Institute and the Natural Resources Defense Council (Fig. 1.1) [3], the GHG emission of conventional vehicles is 3 times higher than the plug in hybrid electric vehicles (PHEV) when renewable energy is used to generate the electric power. Even if the energy is from coal, the emission reduction is still around 40%. Therefore, moving from conventional vehicles to electric vehicles (including both PHEV and PEV) is the trend to save the energy and the environment.

The difference between PEV and PHEV is that the powertrain is driven by a battery pack only or by a combination of battery pack and gasoline. The first type of powertrain consumes pure electric energy. Therefore, when the battery pack charge level drops to a certain level, the vehicle cannot be driven. The PHEV, on the other hand, can switch between the conventional internal combustion engine system and an electric propulsion system. As a result, there is no need to worry about the driving range.

Both PEV and PHEV need an on-board charger to converter AC grid power to DC to charge the high voltage battery inside the vehicle. The charger can be plugged into the household electric socket for home charging or plugged into a designated charging post for faster charging. As a result, a highly efficient but compact battery charger is very critical in the PEV or PHEV's electric systems.

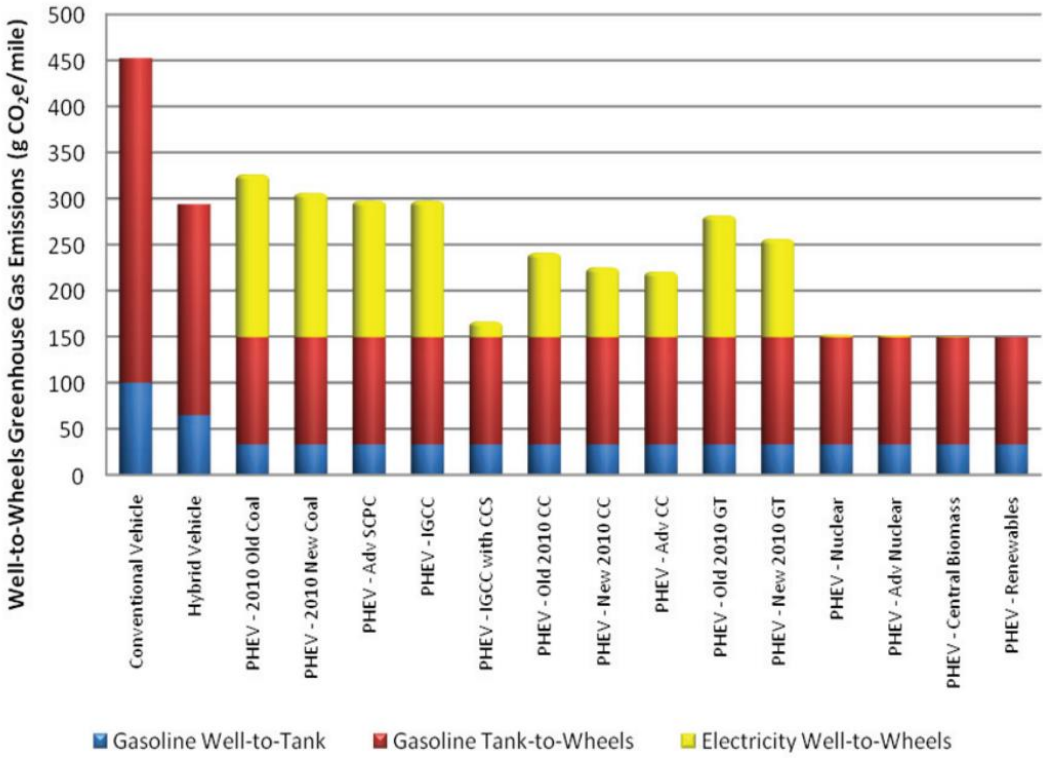

Fig. 1.1. Year 2010 comparison of PHEV 20 GHG emissions (12,000miles driven per year)

1.2 Battery charging system for Electric Vehicle

There are two types of EV charging systems, either conductive or inductive. The conductive charging uses a hard-wired connection between the AC grid power and EV while the inductive charging uses magnetic coupling between two coils to transfer energy from AC grid to the on-board battery.

For conductive charging, the charging systems can be categorized by the power levels, as shown in Table 1.1 [4].

Table 1.1. Different Level of Charging.

Charging Level	Setting	Supply Power
AC Level 1	Residential/parking lot 5mi/h @ 1.7 kW	120 VAC/16 A
AC Level 2 (minimum)	Residential/Commercial 10mi/h @ 3.4 kW	208/240 VAC/16A
AC Level 2 (maximum)	Residential/Commercial 60mi/h @ 19.2 kW	208/240 VAC/100A
DC Level 1	Commercial 120mi/h @ 40 kW	208 VAC/480 VAC (Three Phase)

DC Level 2	Commercial 300mi/h @ 100 kW	208 VAC/480 VAC (Three Phase)

The Level 1 charger is an on-board charger and is usually used in residential household with 120 VAC outlets. Its maximum power is 1.9 kW and can supply around 5 miles of driving per hour. The Level 2 charger utilizes 208 VAC or 240 VAC voltage, which is also available in most U. S households, and the maximum charging power can reach 19.2 kW depending on the ability of the circuit. With the maximum power, it can provide 120 miles of driving per hour.

Aside from AC charging, there is also DC charging. DC charging uses off-board charger instead of the on-board charger due to its much larger power level. It is usually deployed in commercial charging stations. The off-board charger converts the AC power to DC power and charge the battery directly. The power level can be 40 kW for DC level 1 charging and up to 100 kW for DC level 2 charging.

1.3 Bi-directional operation requirement

Nowadays, there are higher requirements for on-board charger systems. Not only it should supply power from the AC grid to the on-board battery, it should also have the ability to utilize the power inside the battery to support AC-grid or some standalone loads with discharging mode operation.

There are two typical applications for the discharging mode [5]. One is for the future smart grid. In the future, the households will have multiple power sources, such as solar power and wind power. In order to take advantage of these renewable power, energy storage is needed, and battery inside the EV can serve such a role. It can be charged when there is more energy generated by these renewable power sources (such as during the day) and discharged when there is not enough energy generated (during the night). In addition, it can be used to even support the grid when there is a power outage. The other application is for off-site workers. Sometimes they need to finish their job off-site where there are no power outlets, and the on-board battery can be a very good power source for the tools, like electric drills and electric cutting machines.

1.4 Overview of wide bandgap (WBG) power devices

Recent emerging wide bandgap power devices, including both gallium nitride (GaN) transistors and silicon carbide (SiC) transistors, are very promising candidates for high frequency power conversion techniques. Due to the advantages of the materials, the WBG power devices have larger band gap, higher electron mobility and higher electron velocity [6, 7]. Thus, better figure of merits can be projected for GaN transistors and SiC transistors than the state-of-the-art Si transistors, which allows WBG devices to switch with much faster transition speed and lower switching loss. By using WBG devices in a circuit design, the switching frequency can be pushed to more than 10 times higher compared with their Si counterparts while the whole system achieves similar or even higher efficiency. Therefore, it is able to achieve high frequency, high efficiency and high power density power conversion at the same time.

Table 1.2. Material properties of Si, SiC and GaN [8].

Parameter	Si	SiC	GaN
E_g (eV)	1.12	3.2	3.4
Critical Field E_{crit} (MV/cm)	0.3	3.5	3.3
Electron Mobility um ($cm^2/(V \cdot s)$)	1500	650	990-2000
Permittivity ε_r	11.8	9.7	9

Both SiC devices and GaN devices are classified as WBG devices because of the significantly higher band gap energy E_g compared with Si devices. The band gap of a semiconductor material reflects the strength of the chemical bonds between atoms in the lattice. High band gap energy means an electron requires more energy to jump from one site to another. Based on this, power semiconductor devices made of high band gap energy material usually have lower leakage current and higher operating temperature.

For the critical electric field, it is also related to the chemical bonds of the material. Generally speaking, the stronger bonds, the higher critical field. Eq. (1.1) shows the relationship between breakdown voltage, drift region width, and critical field.

$$V_{BR} = \frac{1}{2} w_{drift} \cdot E_{crit} \quad (1.1)$$

According to this equation, the breakdown voltage is proportional to the width of the drift region and the critical field. So for a given breakdown voltage, both SiC and GaN devices have around ten times smaller drift region compared to Si devices.The on state resistance can be derived as Eq. (1.2), in which μ_n is the mobility of electrons [6].

$$R_{on} = \frac{4V_{BR}^2}{\varepsilon_0 \varepsilon_r \mu_n E_{crit}^3} \quad (1.2)$$

In Fig. 1.2 [7, 9], the x-axis is the breakdown voltage while the y-axis is the specific on-resistance. The three solid lines are theoretical limit for Si, SiC and GaN based on material properties. Si technology has become very mature over last three decades so that the state-of-the-art Si MOSFETs are close to their theoretical limit. Recent Si based Super Junction MOSFET even outperforms Si's limitation. Therefore, there is still some margin that the performance of Si device can be continually improved in future.

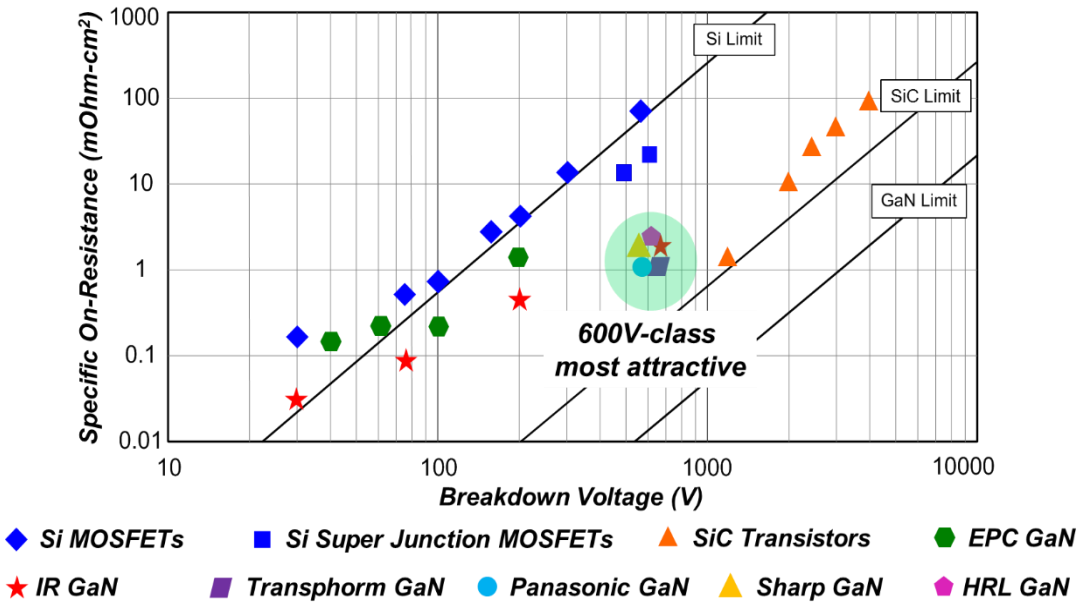

Fig. 1.2. Specific on-resistance vs. breakdown voltage for Si, SiC and GaN

For GaN and SiC, they have much better theoretical limit compared with their Si counterparts and with the continuous development, they can approach their limit just like Si and achieve better and better performance.

1.5 Literature review and challenges in EV charging

The commercialization of the PEV is impeded by the demands of a lightweight, compact, yet efficient on-board charger system. Since the state-of-the-art Level 2 on-board charger products are largely Si-based, they operate at less than 100 kHz switching frequency, resulting in low power density as well as low efficiency. In [10], a two-stage on-board charger is built using Si devise with switching frequency around 80 kHz. The full load efficiency is 94% and the power density is only 9 W/in^3. In [11, 12] a similar 3.3 kW on-board charger is built with 93.6% overall efficiency and around 9.9 W/in^3 power density. In [13], a 3.3 kW bi-directional on-board charger is built using Si devise. 10 W/in^3 power density and over 94.5% efficiency is achieved. Another on-board charging using Si device is proposed in [14]. It has bi-directional operation capability and a full load efficiency around 93.5%. In the 2012 Nissan LEAF, a 6.6 kW on-board charger is installed. However, the power density is only 10.8 W/in^3 and the efficiency is around 90% - 92% [15].

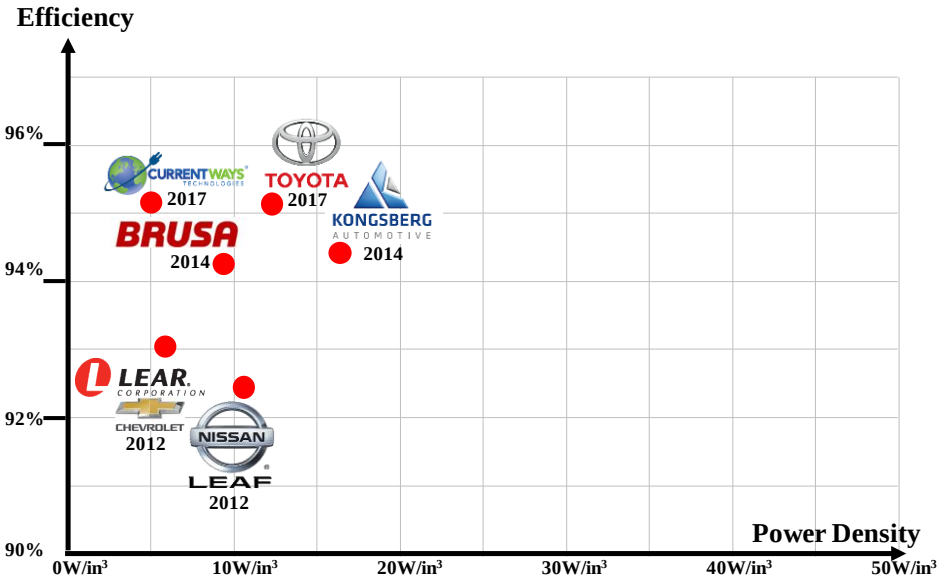

Fig. 1.3. Commercial on-board charger product benchmarking.

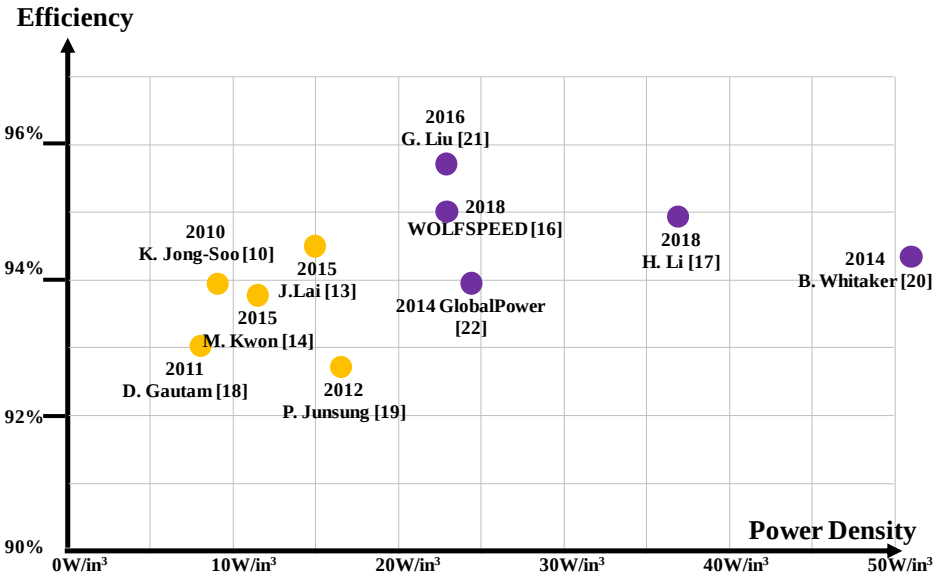

Fig. 1.4. On-board charger benchmarking in research area (Yellow: Si based, Purple: WBG based) [10, 13, 14, 16-22]

All the above commercial products or research products using Si device have low power density and low efficiency (summarized in Fig. 1.3 and Fig. 1.4). Compared with Si device, the absence of reverse recovery charge in WBG device enables bi-directional operation with a single converter. In addition, WBG device has a much better figure of merit than its Si counterpart. For a given on-resistance and breakdown voltage, WBG device requires a much smaller die size, which can translate into smaller gate charge and junction capacitance. Both of these characteristics are able to shorten the current and voltage transition

interval and thus reduce the switching loss. Therefore, by moving to WBG devices, the system switching frequency is increased to 100 kHz – 300 kHz and around 95% efficiency is achieved (shown in Fig. 1.4).

However, despite the aforementioned advantages of WBG devices, challenges remain in their application in the on-board charger system. The first challenge is the bi-directional operation. In [20], a very compact 3.3 kW on-board charger prototype is developed using SiC modules with phase shift full bridge as the second stage. The power density is greatly improved compared with its Si counterparts due to relatively high operating frequency but the efficiency is still in the range of 94%-95%. In addition, it has no reverse power flow capability. In [23], a 7.2 kW on-board charger is proposed using parallel GaN devices with folding circuit as the first stage. Although it is very efficient, it can only handle unity power factor in the discharging mode. Also, it requires additional active filter circuit to handle the double line frequency ripple.

The second challenge is to achieve zero voltage switching (ZVS) under all conditions. For high frequency operations, even WBG devices require a soft switching technique due to the relatively large turn on loss [24, 25]. However, for the AC/DC stage, the conventional continuous conduction mode (CCM) operation is hard switching based [21, 26], generating considerable amount of turn on related loss. In comparison, critical conduction mode (CRM) operation (or boundary mode operation) can achieve ZVS without any additional cost and gains its popularity in low power applications, like 1 kW server power supply [27, 28].

For the isolated DC/DC stage, the dual active bridge DC/DC converter can only achieve ZVS under heavy load [29], and the control becomes very complex when ZVS is desired under light load condition [30]. The LLC resonant converter [31], on the other hand, can achieve ZVS under any load conditions, and hence is widely used in off-line applications such as server [32-34] and telecom power supplies. However, due to its asymmetrical resonant tank, the reverse power flow needs additional handling, considering there is no gain boost capability [26].

The third challenge is to maintain high efficiency over the entire charging cycle. For applications like battery chargers, the output voltage can vary widely with different states of charge of the battery, hindering the optimization of the converter. This is especially true for resonant converters, of which the switching frequency must deviate a lot from the resonant frequency in order to achieve the wide output voltage range. In [21], even with advanced control to reduce the switching frequency range, the efficiency of DC/DC stage drops up to 3% when the battery voltage is very low/high.

The fourth challenge is high power density magnetics with good manufacturability. Litz-wire based transformers and inductors are known to be complicated. Intensive labor work is needed during their manufacture process [35]. PCB winding magnetics, on the other hand, are much more suitable for mass production. However, their requirement is much more stringent. They are never realized in a 6.6 kW power level due to the difficulty to reduce the AC winding loss under high frequency operations. In addition, magnetic integration is more complicated for PCB winding transformer because of the limitation of winding structure and sensitive AC winding loss. Additional inductors will compromise the entire system power density.

The last challenge is common mode (CM) noise. Due to the adoption of WBG devices, the dv/dt of switch node voltage is increased significantly. Together with the large inter-winding capacitance of PCB winding magnetics, CM noise can be a very severe issue. Larger CM filter is needed to pass the EMI requirement, which decreases the system efficiency and density.

1.6 Proposed dissertation outline

Although these challenges exist in both Si device and WBG device based applications, the superior performance of WBG devices gives us the opportunity to have a better solution, as the proposed two-stage on-board charger structure in this paper.

The proposed dissertation outline is:

In chapter 2, a novel two-stage on-board charger structure is proposed. The first stage is a bridgeless totem pole AC/DC converter working at CRM so that soft switching can be achieved for all the fast switches. The second stage is a CLLC resonant converter. Similar with the well-known LLC converter, it can achieve soft switching under all conditions. In addition, due to the symmetrical resonant tank, it is more suitable for bi-directional operation. Variable DC-link voltage is adopted so that the DC/DC stage can always work at its optimized point, providing best efficiency for the entire battery voltage. With soft switching technique, the switching frequency of AC/DC stage and DC/DC stage is pushed to 300 kHz and 500 kHz respectively.

In chapter 3, a novel integrated PCB winding transformer structure is proposed. Using matrix transformer concept, two UI core based transformer is integrated into one UI core, resulting smaller footprint core loss. In addition, by changing the UI core structure to an EI core structure, leakage inductance of the new transformer can be controlled by changing the cross section area of the center leg. Therefore, it can serve as resonant inductor. In addition, the leakage flux is confined inside the core instead of flowing through the air, avoiding additional eddy current or EMI issues.

In chapter 4, regarding to the inter-winding capacitance issue of PCB winding transformer, a new symmetrical resonant converter and symmetrical transformer structure is proposed to cancel out the CM noise. This method is not sensitive to PCB winding layout and switching frequency of the converter and have over 20 dB reduction for the CM noise.

In chapter 5, the on-board charger concept is extended to a higher power level. A three-phase interleaved CLLC converter is designed to provide 12.5 kW power. Device evaluation is performed to find the best suitable device. Based on the single-phase integrated PCB winding magnetic, a three-phase integrated magnetic is proposed. Due to the interleave between the three phases, further integration can be done and an even smaller footprint is achieved.

Chapter 6 gives the summary of this dissertation.

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Chapter 2 **Novel Two-Stage Structure and Control for Bi-Directional On-Board Charger**

There are two different types of on-board charger, one is single-stage AC to DC conversion [1-9] (as shown in Fig. 2.1) and the other one is two-stage AC to DC and DC to DC (as shown in Fig. 2.2)

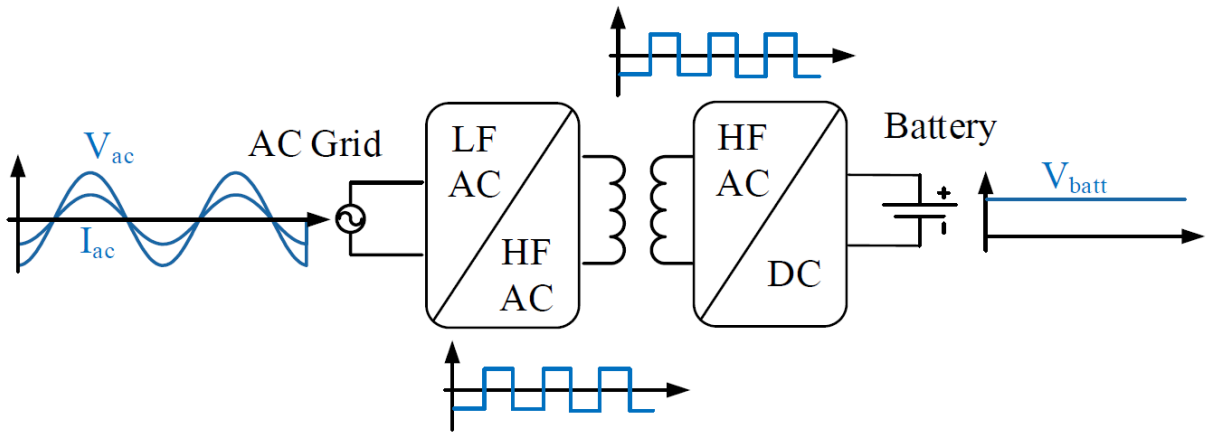


Fig. 2.1. Single-stage AC to DC conversion for on-board charger system.

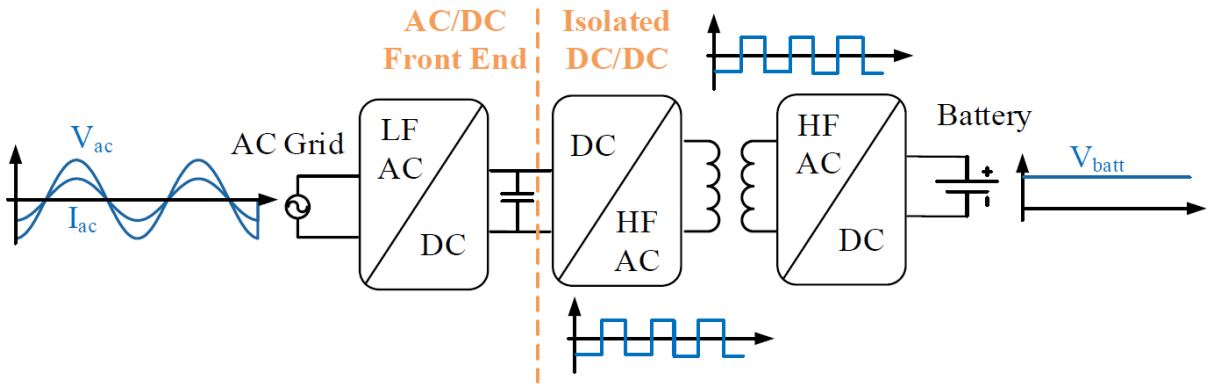


Fig. 2.2. Two-stage AC to DC and DC to DC conversion for on-board charger system.

Although the single-stage solution seems to be simpler and more appealing, it has several drawbacks [10].

1. It is difficult to achieve soft switching for the AC side switches. Individual control of the switches that comprise the four-quadrant switch is needed in order to achieve zero voltage switching (ZVS). Therefore, very complicated driving circuits are required.

2. It is very difficult to optimize the converter under wide operating conditions. For on-board charger application, the input voltage has very wide range (from 85 VAC to 265 VAC) and the output voltage also has a very larger range (from 250 VDC to 450 VDC). To cover such large operating range, the optimization of the converter becomes very difficult and the overall efficiency of the system is not good.

3. It is difficult to control the double line frequency ripple. Because of the power factor correction, there is double line frequency power flowing into the converter. However, the desired output current and voltage are all constant, which means there has to be an energy storage unit in the converter to absorb the double line frequency power, which can be very challenging for single-stage solution.

For the two-stage structure, the first stage is usually a non-isolated AC/DC converter performing power factor correction. The second stage is a DC/DC converter providing voltage regulation and isolation capability.

For AC/DC stage, it has been reviewed in [11, 12], and the topologies that are suitable for on-board charger is reviewed in [13-15]. Among these topologies, the bridgeless totem pole PFC shows great potential due to its simplicity, less number of components and the ability to achieve soft switching when working at critical conduction mode (CRM) [16, 17]. Its structure is shown in Fig. 2.3.

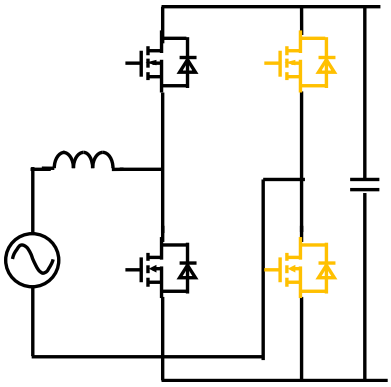


Fig. 2.3. Bridgeless totem-pole PFC

For the DC/DC converter, it has been reviewed in [18, 19]. There are basically two types of DC/DC converter, pulse width modulation (PWM) type converter and resonant type converter.

Dual active bridge (DAB) (as shown in Fig. 2.4) is a very popular PWM type converter when it comes to bi-directional operation. It can achieve soft switching for both primary and secondary side devices with a fixed switching frequency. [20-23]. The operating waveform of DAB is shown in Fig. 2.5.

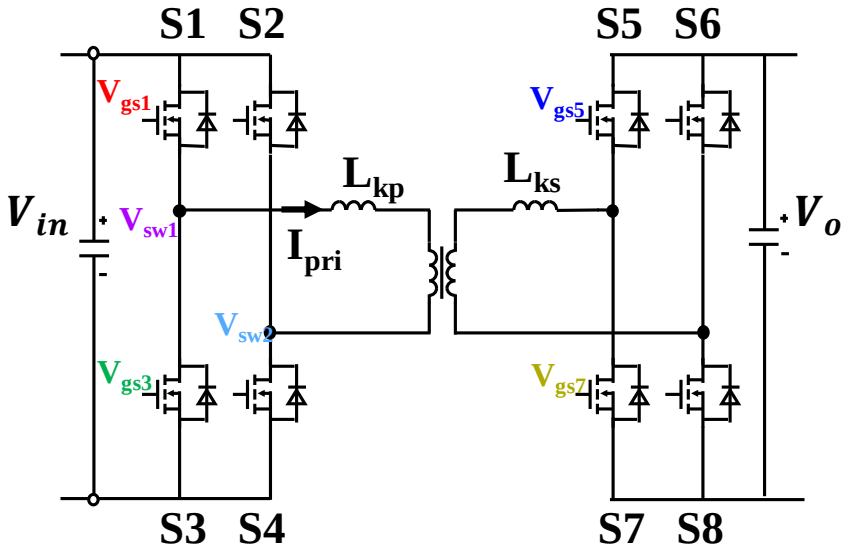


Fig. 2.4. Dual active bridge converter

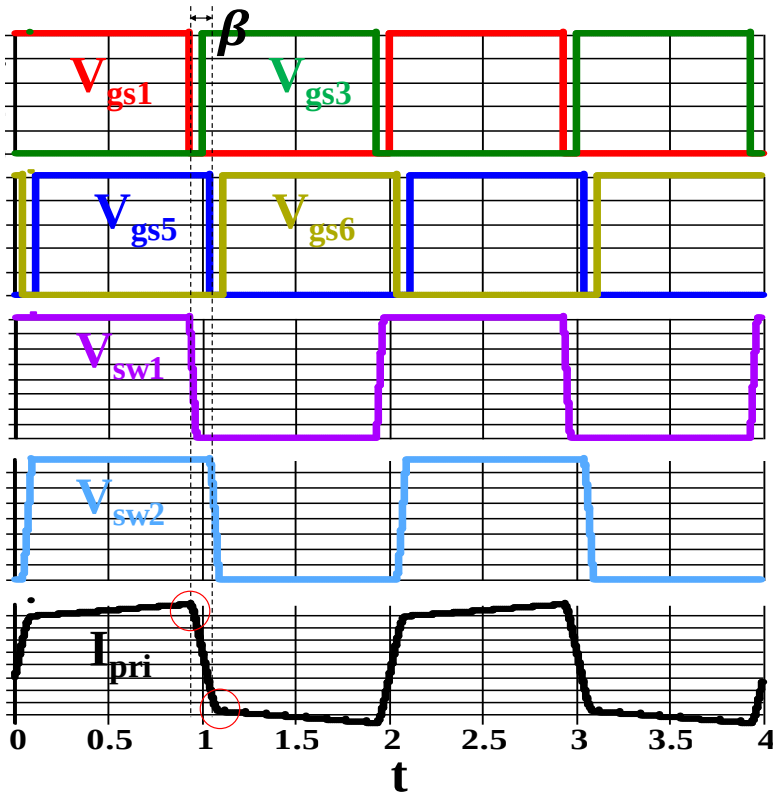


Fig. 2.5. Waveform of DAB.

However, there are some issues with the DAB converter.

1. The devices are turning off at peak current. As a result, large turn off loss is generated. This may not be a big issue under low switching frequency, but when it comes to high switching frequency, this large turn off loss will significantly affect the total system efficiency.

2. ZVS is not guaranteed at light load conduction. Soft switching is achieved utilizing the energy stored in the leakage inductance of the transformer. However, under light load condition, the energy in the leakage inductance is not enough anymore, and soft switching is lost. With high frequency operation, this will also result in low efficiency [24, 25].

For resonant type converter, CLLC converter is a very good candidate for bi-directional operation [26-28]. It has the following benefits.

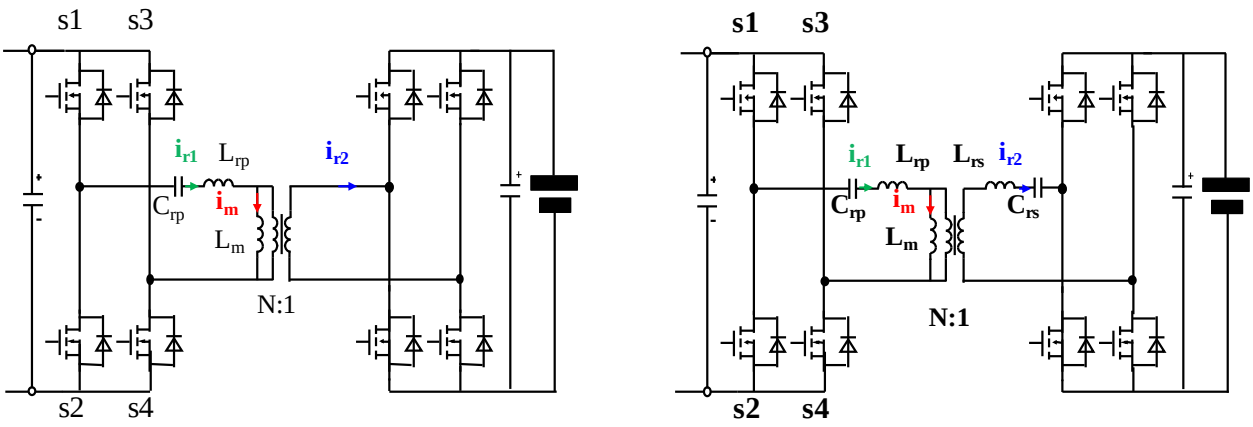
1. Soft switching is achieved under any load conditions. Similar with the popular LLC resonant converter, CLLC converter utilizes the magnetizing inductance to help achieve soft switching. It is not related to load conditions.

2. Turn off current is the peak of magnetizing current instead of peak resonant current. This greatly helps to reduce the turn off because of the much smaller turn off current, making it very suitable for high frequency operation.

However, it does have one drawback, which is the large RMS current. Because of the resonance, the current in the resonant tank is a sinusoidal waveform, which under the same output current, will have larger RMS value compared with the square current waveform in the DAB converter, resulting larger conduction loss.

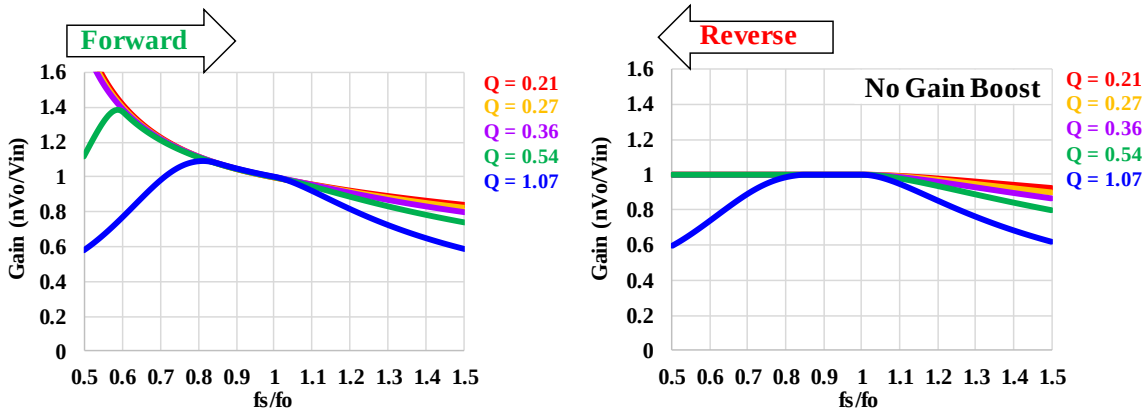
2.1 Analysis of CLLC bi-directional resonant converter

Fig. 2.6 shows both the popular LLC resonant converter and CLLC resonant converter featuring symmetrical resonant tank. For LLC converter, its forward and reverse gain curve are shown in Fig. 2.7. It is clear that under forward operation, it has both gain boost and decrease capability. But under reverse operation, it can only decrease gain. This asymmetry makes the design of bi-directional operation very difficult. However, for CLLC resonant converter, due to its symmetrical resonant tank, its gain curves for both forward and reverse power flow are very similar, as shown in Fig. 2.8, providing both gain boost and decrease capability.



(a) LLC converter (b) CLLC converter

Fig. 2.6. (a) LLC resonant converter and (b) CLLC resonant converter.



(a) Forward (b) Reverse

Fig. 2.7. LLC converter gain curve.

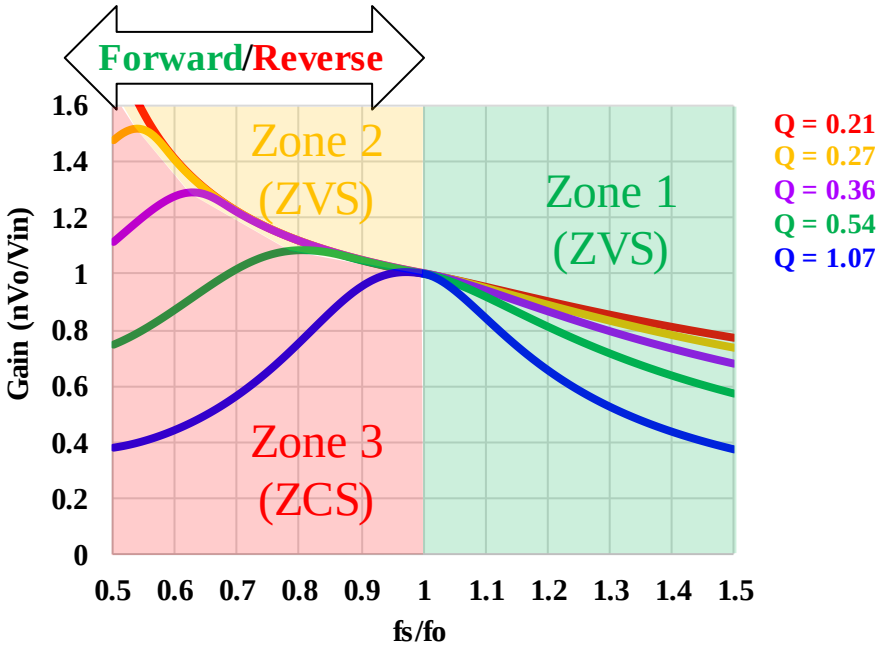


Fig. 2.8. CLLC converter forward and reverse gain curve.

Fig. 2.9 shows the working waveform of CLLC at resonant frequency. At this condition, minimum circulating energy is utilized to help primary switch achieve ZVS.

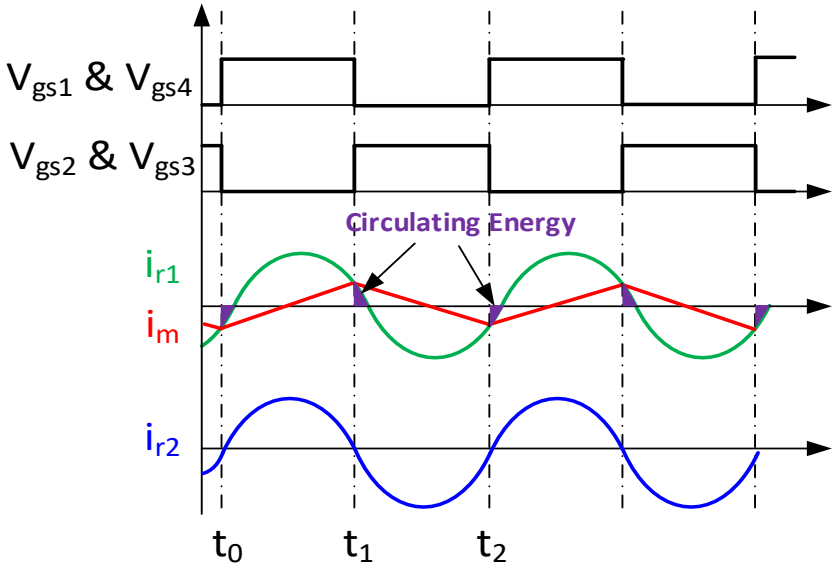


Fig. 2.9. Working waveform of CLLC @$f_s = f_o$.

Fig. 2.10 shows the working waveform when switching frequency is larger than resonant frequency (zone 1 in Fig. 2.8). At this condition, the gain of the converter is less than unity and the circulating current

is larger compared with f_s=f_o case, resulting in larger conduction loss. In addition, the turn off current is larger, which generates larger turn off loss.

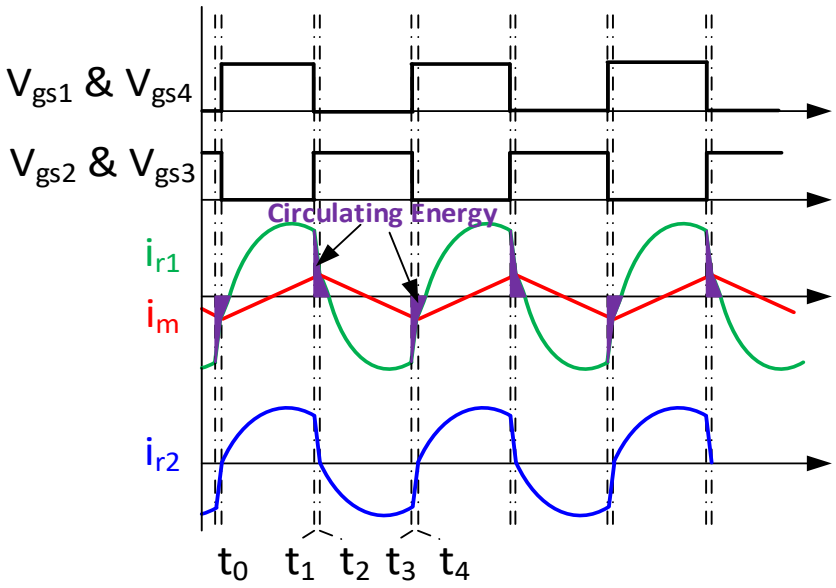


Fig. 2.10. Working waveform of CLLC @ $f_s > f_o$ (zone 1).

Fig. 2.11 shows the working waveform when switching frequency is smaller than resonant frequency with relatively light load (zone 2 in Fig. 2.8). The gain of the converter is larger than one at this condition, but there is certain period during which no energy is transferred from input to output. This results in larger RMS current and therefore larger conduction loss.

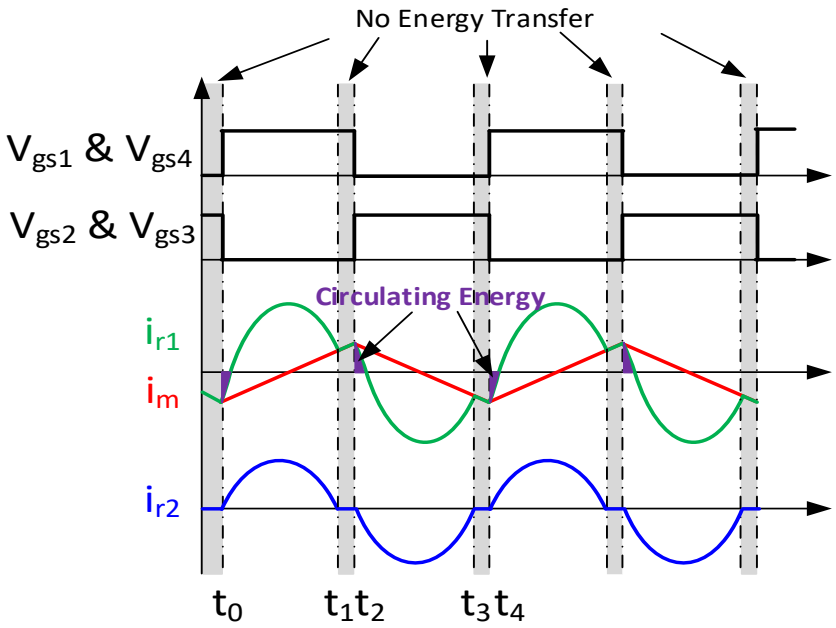


Fig. 2.11. Working waveform of CLLC @ $f_s < f_o$ (zone 2).

Fig. 2.12 shows the working waveform when switching frequency is smaller than resonant frequency with relatively heavy load (zone 3 in Fig. 2.8). At this condition, zero current switching (ZCS) is achieved instead of ZVS for primary switches, resulting in very large switching loss. Usually the resonant converter is purposely designed so this condition is always avoided.

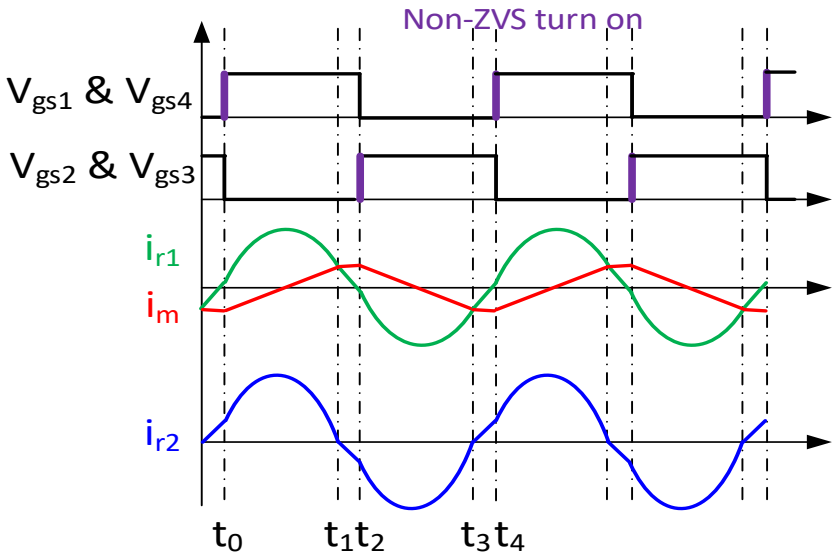


Fig. 2.12. Working waveform of CLLC @ $f_s < f_o$ (zone 3).

With the illustrated working principle above, it is clear that for CLLC converter, gain regulation is realized by changing switching frequency, and the best efficiency is achieved when switching frequency equals to resonant frequency, at which condition the gain is unity.

Due to the symmetrical resonant tank, the reverse working principle is the same.

2.2 Comparison between LLC and CLLC

For the CLLC converter shown in Fig. 2.6 (b), if we have,

$$L_{rp} = N^2 L_{rs} \tag{2.1}$$

$$N^2 C_{rp} = C_{rs} \tag{2.2}$$

Then the CLLC resonant converter has a symmetrical resonant tank. As a result, the gain curve for CLLC is the same for forward power flow and reverse power flow.

However, CLLC also has some drawbacks in order to achieve the bi-directional power flow.

(1) Reduced peak gain

If we define the quality factor (Q) of LLC converter and CLLC converter as below,

$$Q_{LLC} = \frac{\sqrt{\frac{L_{rp}}{C_{rp}}}}{N^2 R_o} \tag{2.3}$$

$$Q_{CLLC} = \frac{\sqrt{\frac{2L_{rp}}{C_{rp/2}}}}{N^2 R_o} \tag{2.4}$$

Where R_o is the output resistance.

Then under the same Q value, LLC converter always has larger peak gain compared with CLLC, as show in Fig. 2.13.

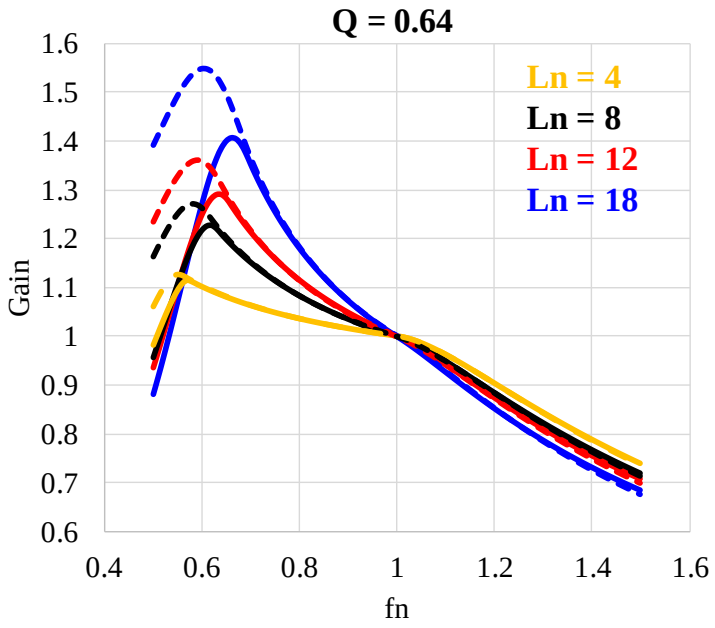


Fig. 2.13. Gain curve comparison between LLC (dash line) and CLLC (solid line).

Here f_n is defined as the normalized switching frequency.

$$f_n = \frac{f_s}{f_o} \tag{2.5}$$

From this figure, it is very clear that LLC has high peak gain than CLLC.

(2) Gain slop of LLC and CLLC are the same under same L_n and same Q

If we define,

$$L_n = \frac{L_m}{L_{rp}} \tag{2.6}$$

From Fig. 2.13, we can also find out that under the same Q and L_n, even though CLLC has smaller peak gain compared with LLC, it has the same gain curve slop compared with LLC converter. This means that with certain gain range requirement, CLLC converter always has the same frequency range with LLC converter if peak gain requirement is satisfied.

(3) L_n determines gain slop when switching frequency is smaller than resonant frequency while Q and L_n both determine gain slop when switching frequency is larger than resonant frequency.

From Eq. (2.3) and Eq. (2.4), we can find out that for LLC and CLLC converter, Q value is different even under the same load condition.

With the same output resistance R_o,

$$Q_{LLC} = \frac{1}{2} Q_{CLLC} \tag{2.7}$$

Therefore, under the same load condition, the gain curve for LLC and CLLC are actually different, as shown in Fig. 2.14,

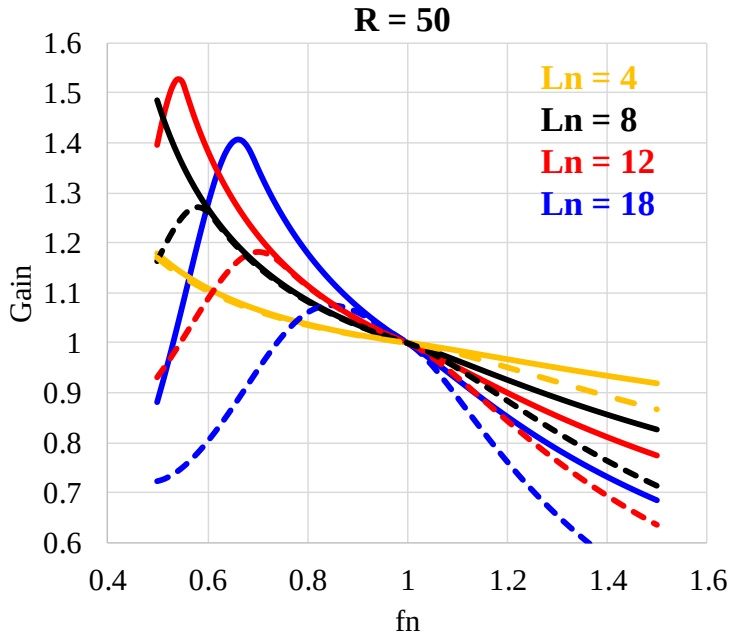


Fig. 2.14. Gain curve comparison between LLC (dash line) and CLLC (solid line).

It is clear that under the same load condition, CLLC has less peak gain. In addition, the gain slop between CLLC and LLC is the same when switching frequency is smaller than resonant frequency. However, when switching frequency is higher than resonant frequency, CLLC has steeper gain compared with LLC under the same load condition.

2.3 Proposed novel variable DC-link voltage structure

From section II, it has been demonstrated that resonant converter can only achieve best efficiency when switching frequency equals to resonant frequency. Other than that the efficiency drops. Due to this limitation, the wide output voltage range for battery charger application becomes a significant challenge.

Fig. 2.15 shows the conventional two-stage on-board battery charger structure using 650 V GaN devices. Due to the current rating of available GaN devices, four-phase interleaved structure is adopted for the bridgeless totem pole PFC and two modules are in parallel for CLLC resonant converter to handle the large power.

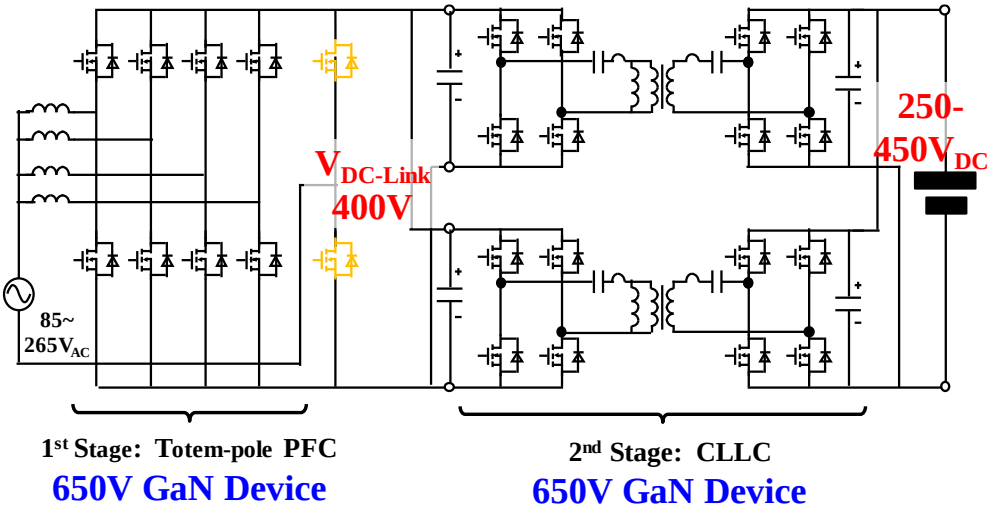


Fig. 2.15. Conventional two-stage on-board charger with fixed DC-link voltage.

Since the DC-link voltage is fixed at 400 V, with 250 V-450 V battery voltage range, the input and output voltage relation of DC/DC stage is shown in Fig. 2.16, as well as the switching frequency range.

Due to wide battery voltage range, the switching frequency range of CLLC converter is very wide, from 0.65f_o to 1.4f_o. A thorough loss analysis is performed for this fixed DC-link voltage structure using GS66516T from GaN Systems. The resonant frequency of DC/DC stage is set at 500 kHz. Conduction loss is calculated using on resistance provided by the datasheet and switching loss is calculated based on double pulse testing results.

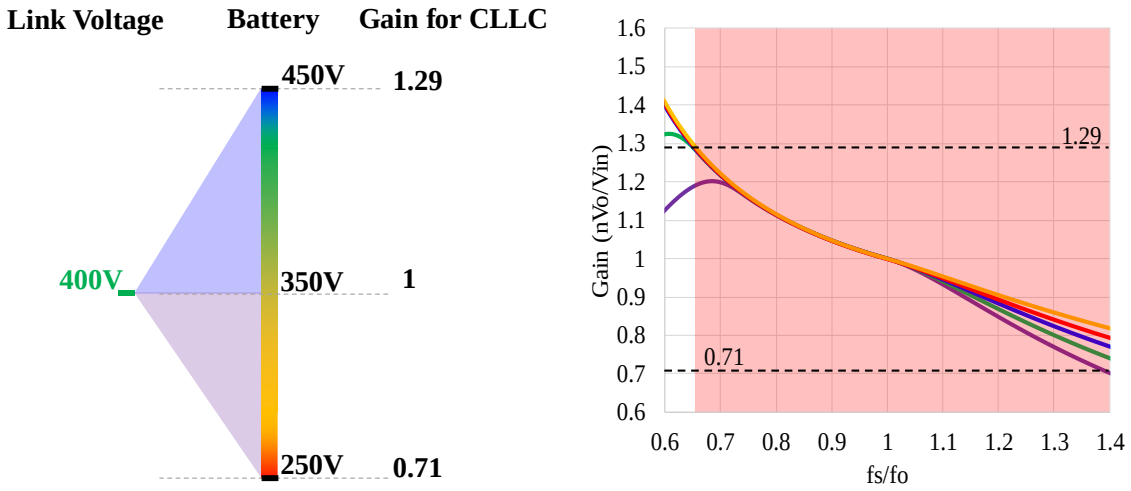
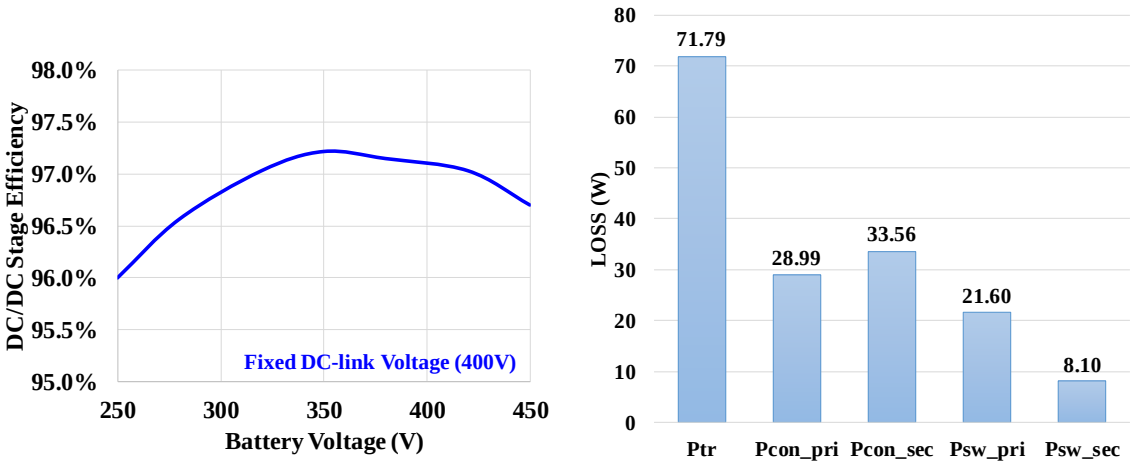


Fig. 2.16. Gain and switching frequency range for fixed DC-link voltage (400 V).

The calculation result verifies our analysis that the highest efficiency is achieved when gain is unity (switching frequency equals to resonant frequency). From 350 V battery voltage to 250 V battery voltage, the charging efficiency drops over 1%.

It should be noted that the evaluation is based on a pre-defined charging profile. When battery voltage is between 250 V-300 V, 22 A constant current charging is used and when battery voltage is between 300 V-450 V, 6.6 kW constant power charging is use.



(a) Efficiency evaluation (b) Loss breakdown @ 350V battery voltage

Fig. 2.17. DC/DC stage evaluation for fixed DC-link voltage (400 V).

Loss breakdown at 350 V battery voltage is provided including transformer loss, device conduction loss and switching loss for both primary side and secondary side.

In order to improve efficiency at different battery voltage, we can reduce the required CLLC gain range by allowing the DC-link voltage to vary. Due to power factor correction requirement and device voltage rating limitation, the maximum DC-link voltage variation is 400 V-450 V when 650 V GaN devices are used. With this range, the input and output relation for DC/DC stage is shown in Fig. 2.18.

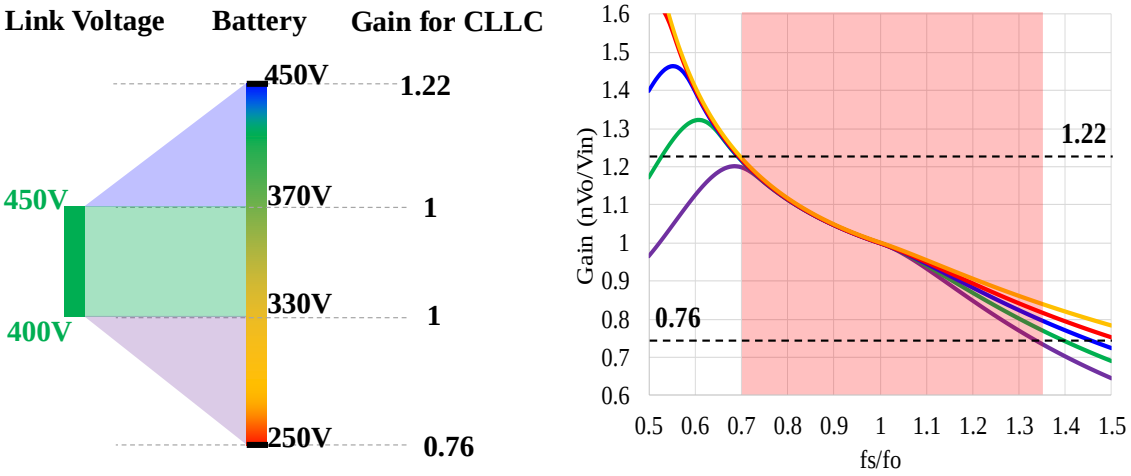


Fig. 2.18. Gain and switching frequency range for variable DC-link voltage (400 V - 450 V).

From Fig. 2.18, we can see that within 330 V-370 V battery voltage range, the gain requirement for DC/DC stage is just unity if DC-link voltage follows battery voltage. From gain curve, we can also find that the switching frequency range reduces to $0.7f_o$-$1.37f_o$, which is smaller than fixed DC-link voltage structure. Efficiency evaluation is also performed and the result is shown in Fig. 2.22. With reduced switching frequency range, DC/DC stage efficiency is improved. It should be noted that the slightly different efficiency at resonant frequency is caused by different turns ratio (1.14:1 for fixed DC-link voltage and 1.21:1 for variable DC-link voltage).

Although efficiency is improved, the improvement is very limited. In order to further reduce switching frequency range, a new two-stage structure is proposed, as shown in Fig. 2.19.

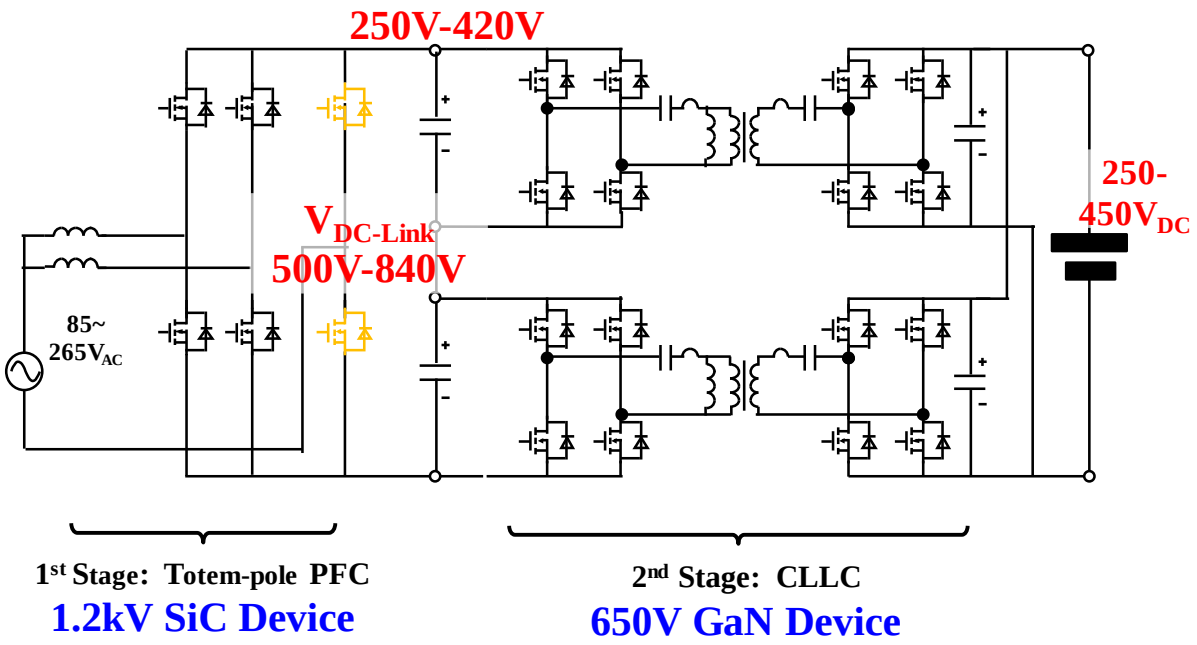


Fig. 2.19. Variable DC-link voltage structure using split capacitors.

To further increase the DC-link voltage variation range, 1.2 kV SiC devices are used in AC/DC stage. Using this configuration, DC-link voltage range can be extended to 500 V-840 V, and the input and output voltage relation of DC/DC stage is shown in Fig. 2.20. Here, the lower voltage limit is determined by the lowest battery voltage and the upper voltage limit is determined by device rating. Considering DC-link voltage ripple and drain source voltage ringing of the device, it is safe and necessary to clamp the DC-link voltage at 840 V.

By changing DC-link voltage from 500 V to 840 V, the gain range of DC/DC stage is greatly reduced to only 1 - 1.07, and the switching frequency range is also reduced significantly, to only $0.9f_o$ - f_o. We can see that almost within the entire battery voltage range, the gain requirement for DC/DC stage is just unity, which means the switching frequency of the converter can stay at resonant frequency most of the time, providing best efficiency.

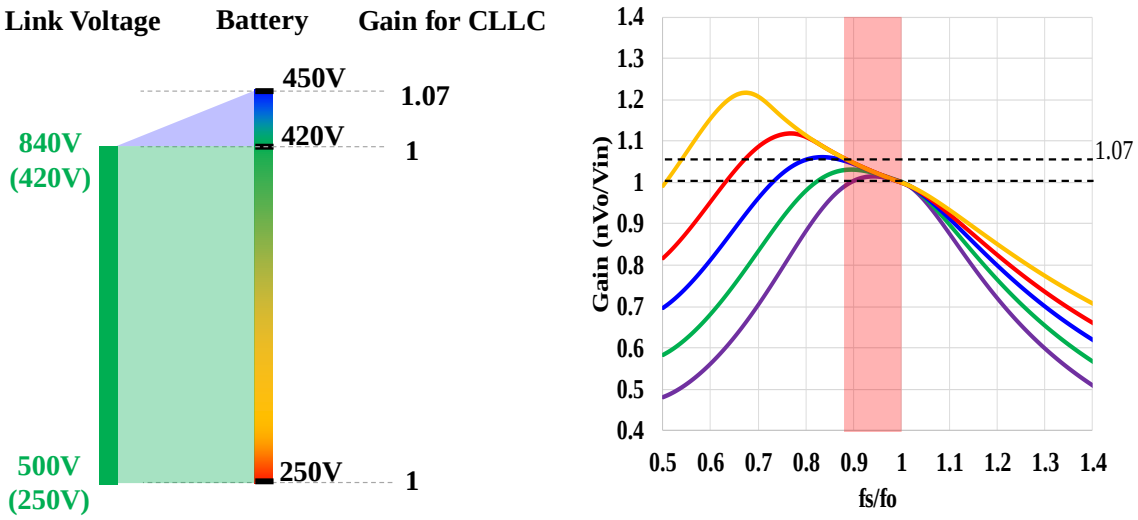


Fig. 2.20. Gain and switching frequency range for variable DC-link voltage (500V - 840V).

Loss analysis using SiC device from GE and GS66516T from GaN Systems is also performed for this structure and the result is shown in Fig. 2.22. It shows that the efficiency of variable DC-link voltage (500 V – 840 V) is even worse than the fixed DC-link voltage structure under certain conditions. This is because the two modules of the DC/DC stage are in fact in series on primary side. Under low DC-link voltage, the current is higher, and the series configuration brings significant conduction loss and compromises the system efficiency.

To solve this problem, another two-stage structure with variable DC-link voltage is proposed, as shown in Fig. 2.21. In this structure, the primary side devices of DC/DC stage are also changed to 1.2 kV SiC devices. Therefore, no series connection is required and the conduction loss can be reduced. For the secondary side of DC/DC stage, still 650 V GaN devices are adopted and two sets of output are used in parallel to handle the large output current.

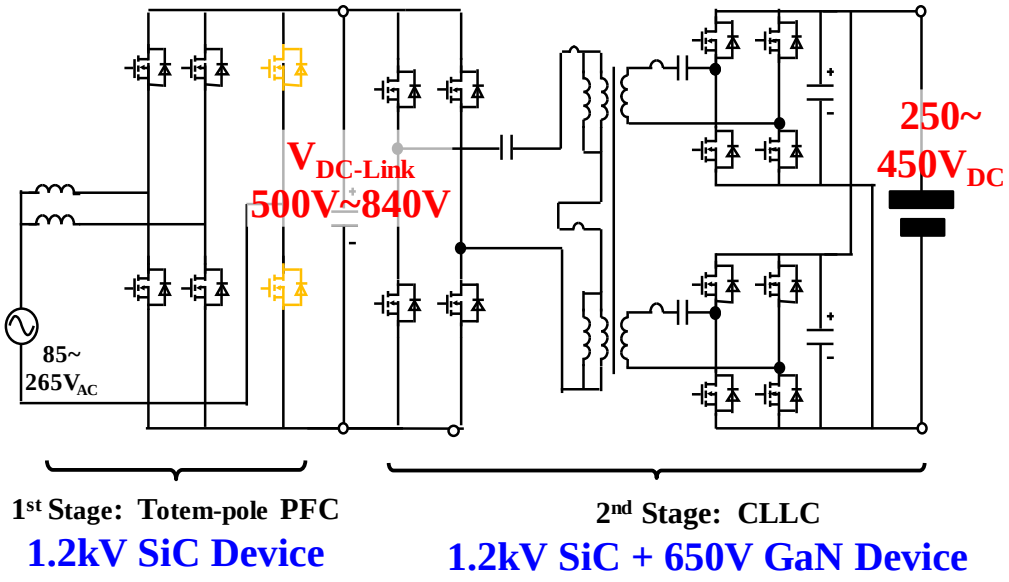


Fig. 2.21. Variable DC-link voltage structure without split capacitors.

Following the same procedure, efficiency of this structure is analyzed and the result is shown in Fig. 2.22. It can be seen that by reducing gain range of DC/DC stage with the last proposed structure, the efficiency curve becomes much flatter, indicating very high efficiency over the entire battery voltage range.

What's more, the proposed structure also brings significant benefit to the transformer design. With large gain range (conventional fixed DC-link structure), large resonant inductors are required for resonant converter to realize good gain regulation capability. But with the proposed variable DC-link structure, due to the very small gain range requirement, the required resonant inductors become much smaller, which can help to lower down the inductor loss and also gives us the opportunity to integrate them into transformer.

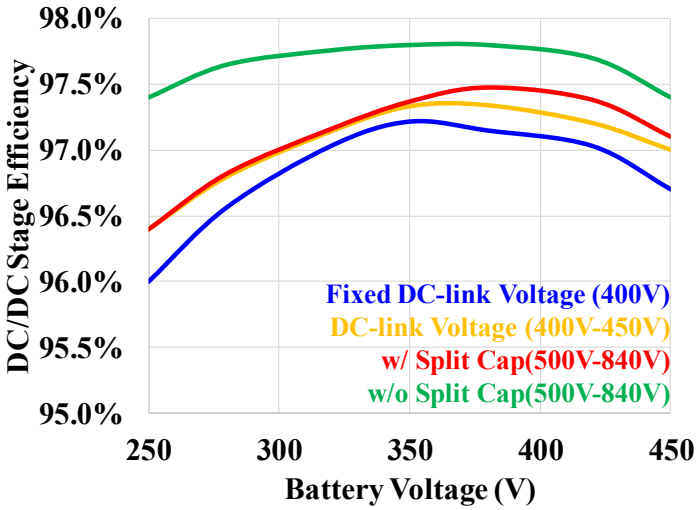


Fig. 2.22. DC/DC stage evaluation and comparison.

Detailed loss breakdown comparison under 350 V battery voltage for the DC/DC stage is shown in Fig. 2.23.

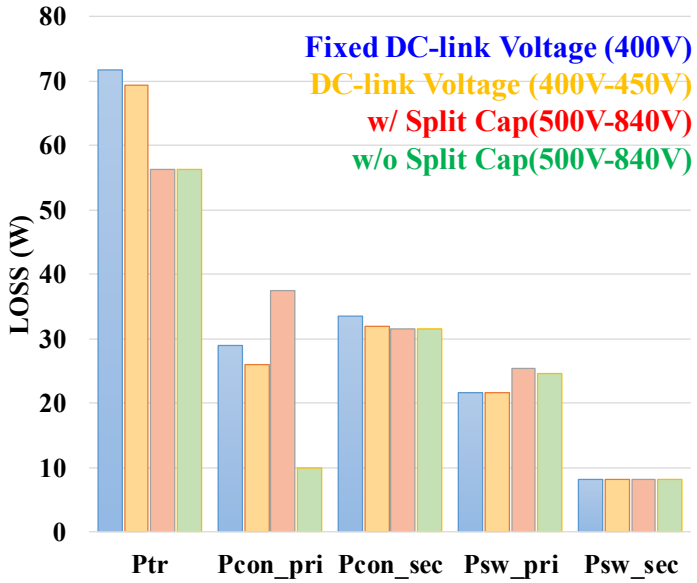


Fig. 2.23. Loss break down of the four candidates @350V.

Due to the variable DC-link voltage, DC/DC stage gains benefits for reduced frequency range. However, the burden shifted to AC/DC stage, as shown in Fig. 2.24. First stage efficiency is compromised because of the high turn off voltage. It should be noted here that because of the large turn off current and turn off loss, the minimum switching frequency of AC/DC stage is decreased from 500 kHz for GaN version to 300 kHz for SiC version.

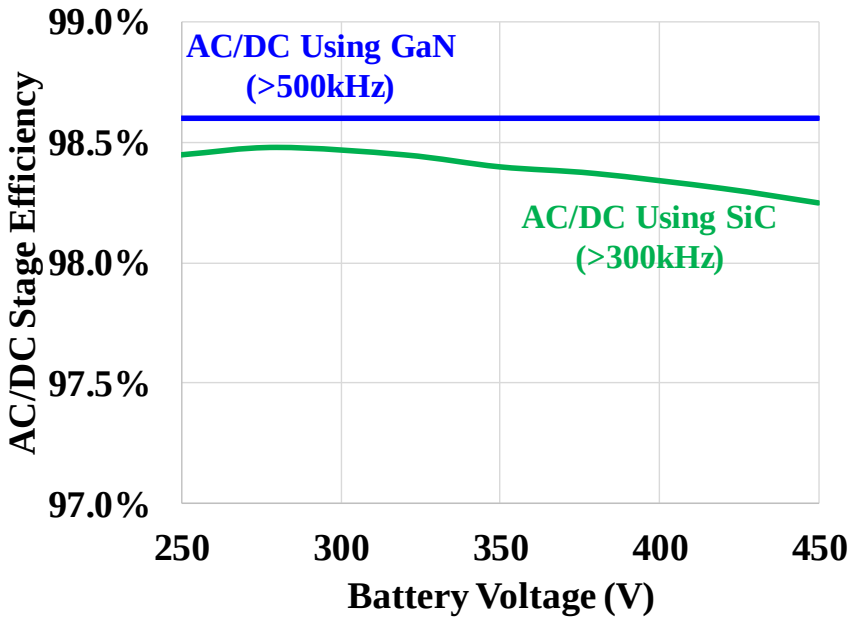


Fig. 2.24. AC/DC stage efficiency evaluation and comparison.

If two-stage efficiency is compared, as shown in Fig. 2.25, it can be seen that the last proposed candidate has not only the best peak efficiency, but also a very flat efficiency curve. 1.5% efficiency is improved at low battery voltage compared with conventional fixed DC-link structure. Therefore, we chose the last candidate as our final design.

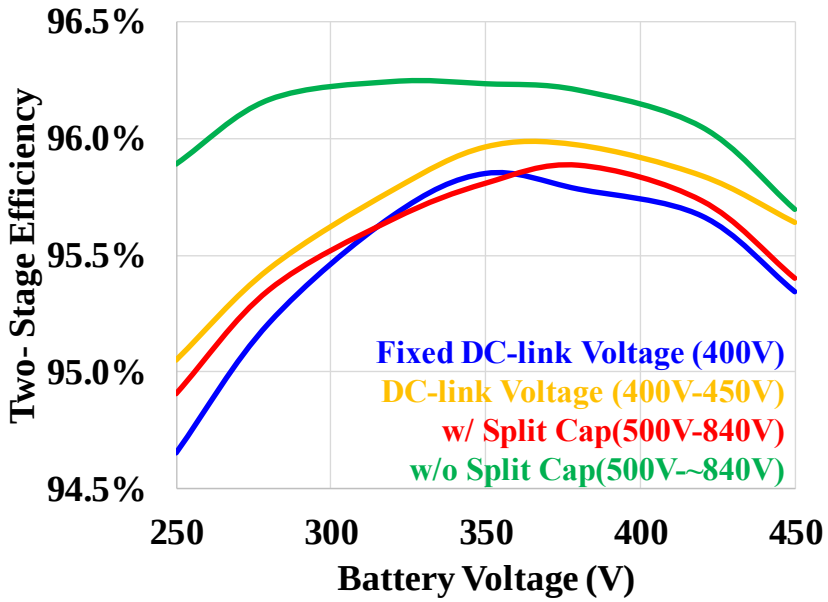
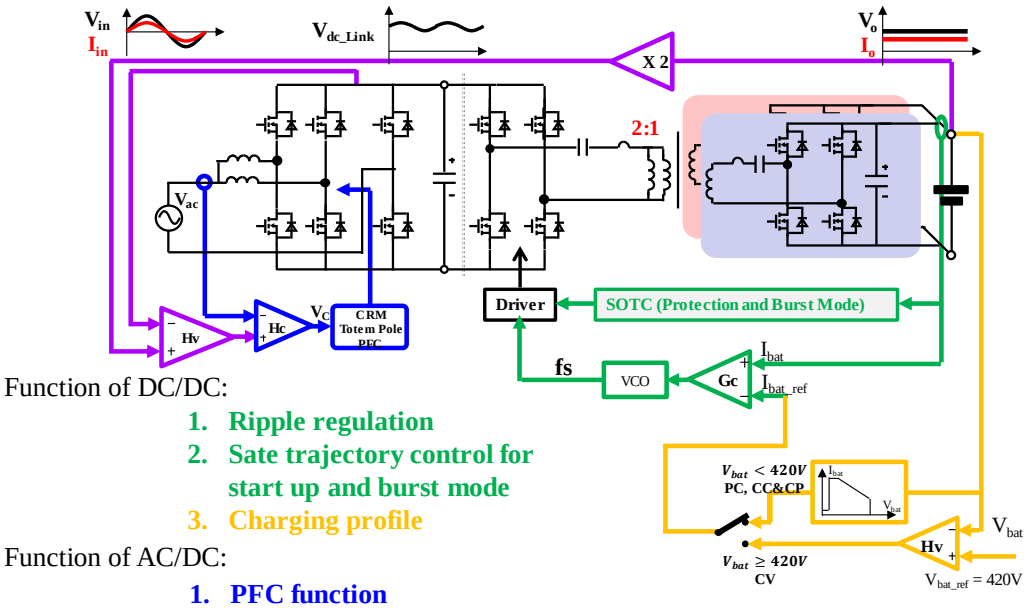


Fig. 2.25. Two-stage efficiency evaluation and comparison.

2.4 Two-stage combined control strategy for both charging and discharging mode.

From previous analysis, the benefit of the proposed variable DC-link structure is to keep the switching frequency of the DC/DC stage at resonant frequency so that high efficiency can be maintained over the entire battery voltage range. This DC transformer (DCX) concept has been proved to be very efficient [29]. However, in applications like battery charger, this concept has the problem of very large output current ripple [30]. Due to PFC function of AC/DC stage, there is second order harmonic voltage ripple on the DC-link. Although this ripple can be kept small (5%) by using large amount of DC-link capacitors, the output current ripple still can be significant because of the very small internal resistance of the battery if DCX concept is adopted. Usually this large charging current ripple is not acceptable by the battery because it compromises the lifetime. Also, the large amount of DC-link capacitors lower down the power density of the whole system and increases the weight of the converter significantly.

In order to solve this problem, a two-stage combined control strategy is proposed, as shown in Fig. 2.26.



Function of DC/DC:

1. **Ripple regulation**
2. **Sate trajectory control for start up and burst mode**
3. **Charging profile**

Function of AC/DC:

1. **PFC function**
2. **CRM operation**
3. **DC-link voltage regulation**

Fig. 2.26. Proposed control strategy for charging mode operation.

In this control structure, there are four control loops. 1) The blue loop of the AC/DC stage is to maintain CRM operation and also power factor correction [31]. 2) The purple loop is to make sure the DC-link voltage follows battery voltage so that the switching frequency of the DC/DC stage can always stay around resonant frequency. 3) Instead of using DCX concept, a minor control is introduced as the green loop shows, eliminating double line frequency ripple in the output current. Simplified optimal trajectory control [32] is utilized for fast transient and soft start up. 4) Last, pre-defined charging profile needs to be followed, including pre-charge, constant current (CC) charge, constant power (CP) charge and constant voltage (CV) charge, as shown in Fig. 2.27.

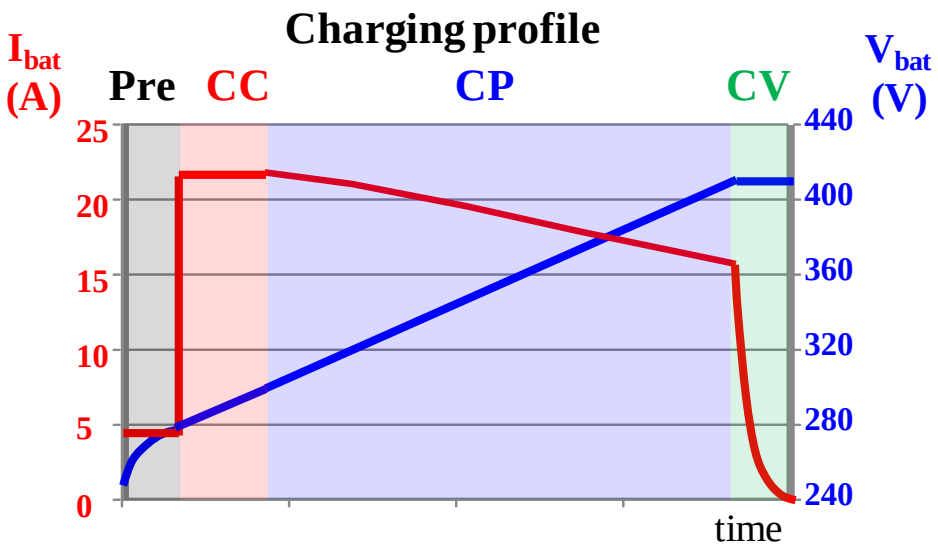


Fig. 2.27. Charging profile for the proposed on-board charger.

The structure of the control is very simple but the concept is new. By using this control strategy, on one hand, the average DC-link voltage always tracks twice of the battery voltage so that the gain for second stage is kept around unity. On the other hand, the current loop of DC/DC stage can make sure there is no second order line frequency ripple past from DC-link to battery.

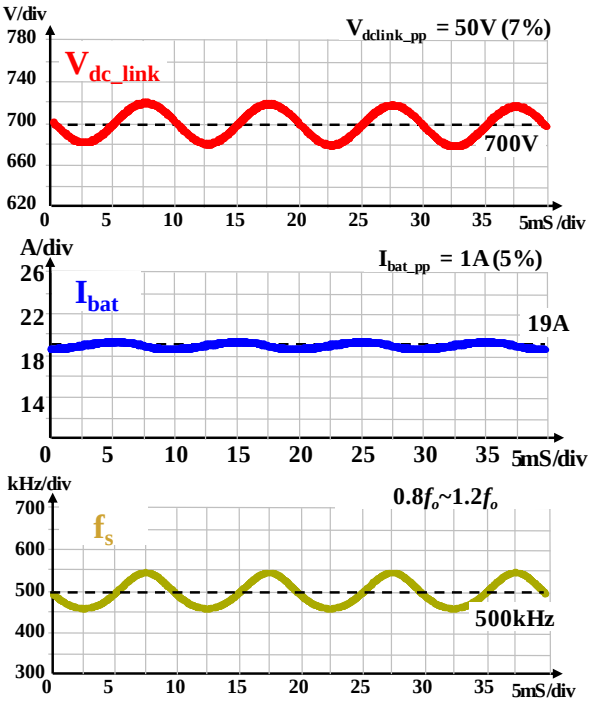
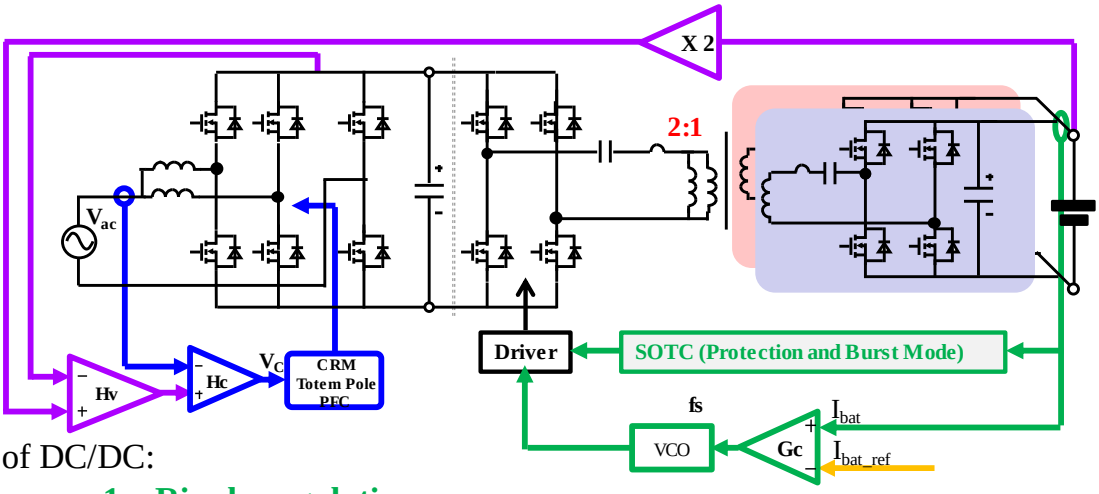


Fig. 2.28. Simulation results of the proposed control for charging mode

Simulation results of the proposed control strategy are shown in Fig. 2.28. With 7% DC-link ripple, the charging current ripple is only 5%. And if we take a look at the switching frequency, we can see that it is varying around resonant frequency. By doing this, the second stage can be very efficient at different battery voltage while still prevent the second order line frequency ripple from passing to the battery.

The same control concept can also be adopted in discharging mode, as shown in Fig. 2.29.

For discharging operation, there are two different modes, grid-tied mode and standalone mode. For grid-tied application, control strategy is almost the same with charging mode due to the inherent bi-directional operation characteristic of both AC/DC stage and DC/DC stage. For standalone application, where AC side is connected to a standalone load, the AC/DC stage needs to control the output AC voltage. Therefore, the DC-link voltage control lies on the DC/DC stage, as shown in the yellow loop in Fig. 2.29 (b). Other control loops are the same with grid-tied application.



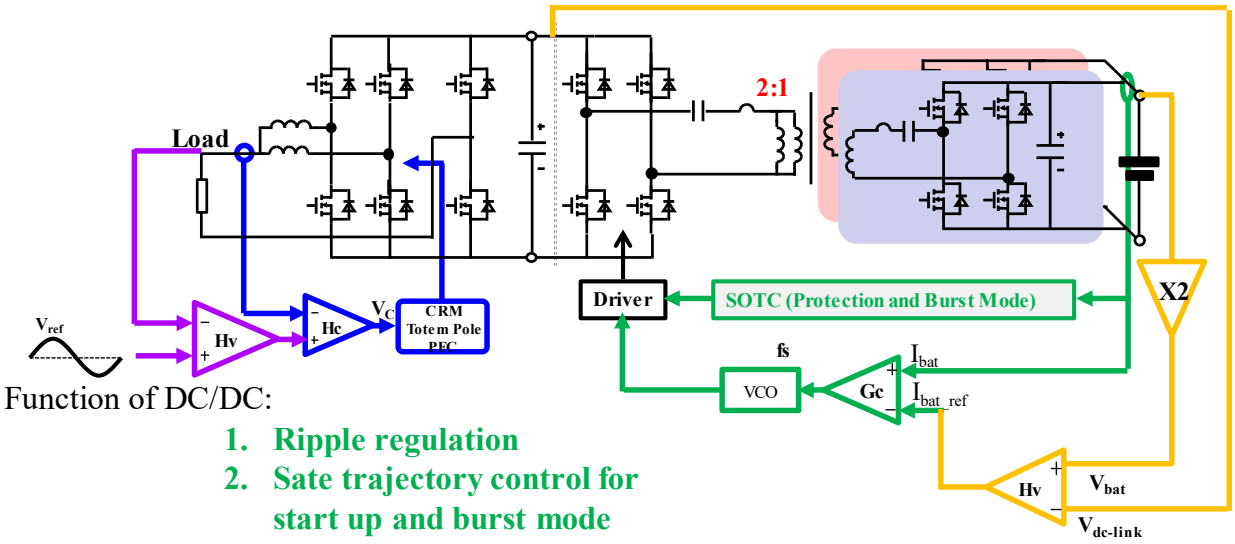
Function of DC/DC:

1. **Ripple regulation**
2. **Sate trajectory control for start up and burst mode**
3. **Discharging power**

Function of AC/DC:

1. **PFC function**
2. **CRM operation**
3. **DC-link voltage regulation**

(a) grid-tied operation



Function of DC/DC:

1. **Ripple regulation**
2. **Sate trajectory control for start up and burst mode**
3. **DC-link voltage regulation**

Function of AC/DC:

1. **PFC function**
2. **CRM operation**
3. **AC voltage regulation**

(b) Standalone operation

Fig. 2.29. Control strategy for discharging mode.

2.5 DC-link capacitor selection and design

The proposed variable DC-link structure can help to achieve very good efficiency over the entire battery voltage range. However, the increasing of DC-link voltage also brings some drawbacks, one of which is large DC-link capacitor size.

Usually there are two kinds of capacitors that can be used as the DC-link capacitors. One is film capacitor and one is aluminum electrolytic capacitor.

Film capacitor has very long lifetime even under high temperature conditions. It can handle larger ripple current compared with the aluminum electrolytic capacitor due to the much smaller dissipation factor. Moreover, film capacitor has much higher voltage rating. It is common to find film capacitors with over kV voltage rating (Table 2.1). However, for aluminum electrolytic capacitor, the lifetime is much shorter,

especially when the temperature rise is significant. In addition, the most commonly used voltage rating for aluminum electrolytic capacitors is below 500V, as shown in Table 2.2.

Table 2.1. Typical specifications for film capacitors.

Brand	Vdc (V)	Capacitance (uF)	Capacitance Density (uF/in^3)	Lifetime @80ºC (hour)
EPCOS	450	480	18 (4.5 @ 900V)	>200,000
VISHAY	500	100	17 (4.25@1000V)	>200,000
EPCOS	920	200	7.6	>200,000
VISHAY	1000	20	6.1	>200,000

Table 2.2. Typical specifications for aluminum electrolytic capacitors.

Brand	Vdc (V)	Capacitance (uF)	Capacitance Density (uF/in^3)	Lifetime @80ºC (hour)
TDK	450	560	86.7 (21.7 @ 900V)	>45,000
TDK	450	470	80.1 (20.0@900V)	>45,000
KEMET	500	560	40.7(10.2@1000V)	>45,000

Due to the lower cost, in the products some still prefer to use aluminum electrolytic capacitors. Also, the high capacitance density means the whole system volume and weight can be greatly reduced. However, the most challenging part for using aluminum electrolytic capacitors is to achieve the required lifetime, which is closely related to the ambient temperature and the ripple current.

2.5.1 **Ripple current calculation**

The input current and voltage waveform of the AC/DC stage is shown in Fig. 2.30. Due to the power factor correction (PFC) function, the total input power has double line frequency ripple.

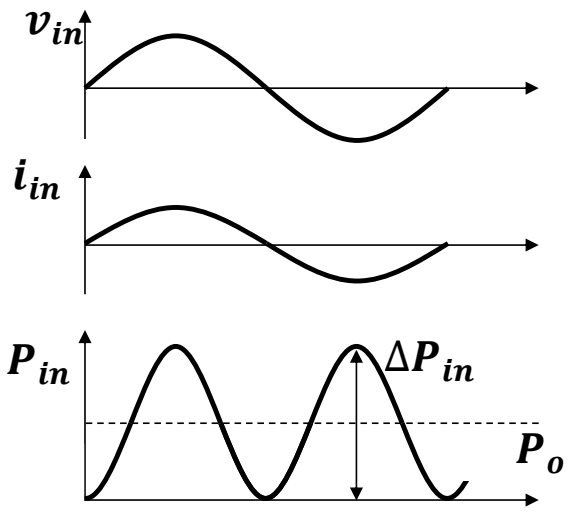


Fig. 2.30. Input voltage and current waveform and the resulted input power.

$v_{in} = V_{in}\sin(2\pi ft)$

$i_{in} = I_{in}\sin(2\pi ft)$

$$P_{in} = v_{in}i_{in} = \frac{V_{in}I_{in}}{2}[1 - \cos(4\pi ft)] \quad (2.8)$$

(2.9)

However, the output current has constant value since its DC current and DC voltage. As a result, all the double line frequency power needs to be absorbed by the DC-link capacitors.

$$P_{2f} = \frac{V_{in}I_{in}}{2}\cos(4\pi ft) \quad (2.10)$$

The voltage across the DC-link capacitors and the current flowing through them are shown in Fig. 2.31.

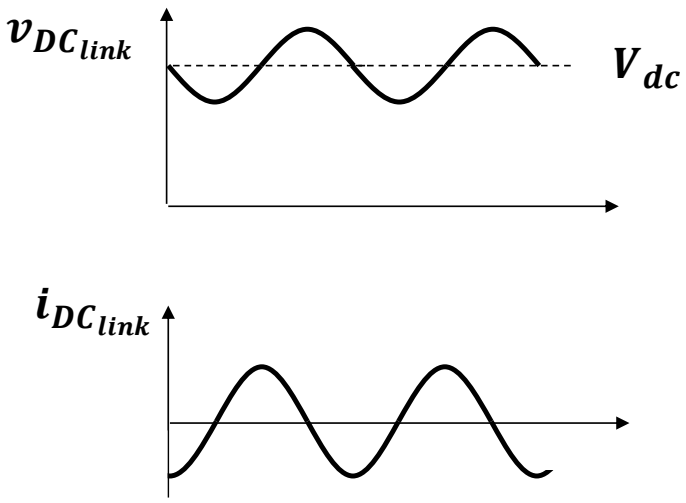


Fig. 2.31. Voltage across the DC-link capacitors and the current flowing through them.

If we assume the ripple voltage is much smaller than the average voltage on the DC-link, the power absorbed by the DC-link capacitor can be expressed as,

$$P_{2f} = \frac{V_{in}I_{in}}{2}\cos(4\pi ft) \approx V_{dc}i_{DC_{link}} \tag{2.11}$$

Then, the current flowing through the capacitors can be expressed as,

$$i_{DC_{link}} = \frac{V_{in}I_{in}}{2V_{dc}}\cos(4\pi ft) \tag{2.12}$$

Therefore, the RMS value of ripple current is,

$$i_{DC_{link-RMS}} = \frac{V_{in}I_{in}}{2\sqrt{2}V_{dc}} \tag{2.13}$$

For conventional fixed DC-link voltage structure, the DC-link voltage is always a constant value, that is, 400 V. However, for the proposed variable DC-link structure, the DC-link voltage is varying between 500 V and 840 V. The ripple current RMS value for the conventional fixed DC-link voltage and the proposed variable DC-link voltage structure can be calculated, as shown in Fig. 2.32. It should be noted for simplicity, pre-charge and CV charging mode is ignored. Instead, only CC and CP charging mode are used before and after 300 V battery voltage respectively.

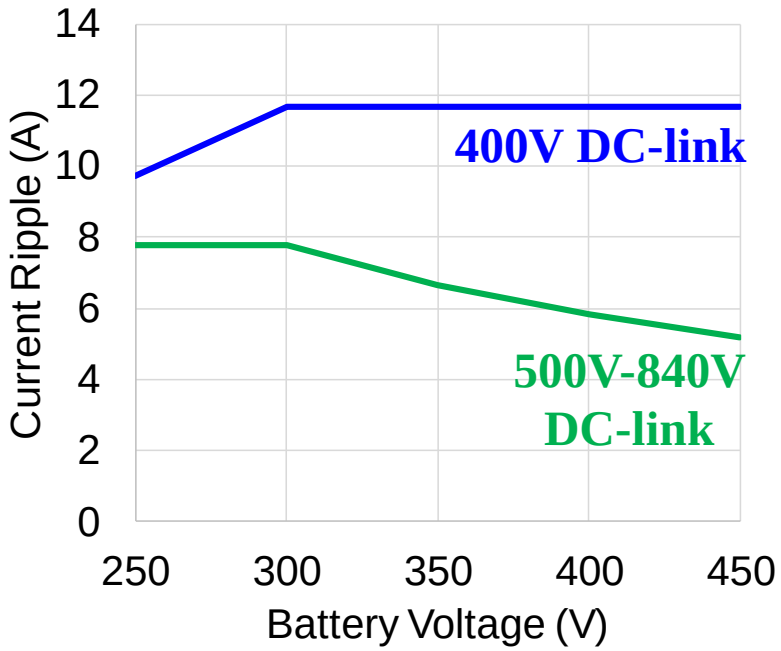


Fig. 2.32. Ripple current RMS value with different DC-link voltage.

2.5.2 Capacitor size comparison

The lifetime of aluminum electrolytic capacitor is affected by the ambient temperature, its voltage stress and current stress.

From Fig. 2.32, we can see that for conventional fixed DC-link voltage structure, the current stress is higher than the proposed variable DC-link structure, mainly because its DC-link voltage is lower.

If we took an average value, the ripple current RMS value for conventional fixed DC-link voltage structure compared with that in the proposed variable DC-link structure is,

$$\frac{\overline{\iota_{fixed}}}{\iota_{variable}} = \frac{5}{3} \tag{2.14}$$

To have the same amount ripple current flowing through each capacitor, the number of capacitors in parallel should have the ratio of,

$$\frac{N_{pallel-fixed}}{N_{pallel-variable}} = \frac{5}{3} \tag{2.15}$$

However, due to the voltage stress, for the proposed variable DC-link structure, we need two 450 V aluminum electrolytic capacitors in series to handle the high voltage, so the number of capacitors needed for both cases has the following ratio,

$$\frac{N_{fixed}}{N_{variable}} = \frac{5}{6} \approx 83\% \tag{2.16}$$

From Eq. (2.16) we can see that in order to achieve the same amount of lifetime, with the proposed variable DC-link voltage structure, we need around 18% more aluminum electrolytic capacitors to handle the current ripple.

However, it should be noted that the above calculation is only based on same ripple current (same lifetime of electrolytic capacitor). At this number of capacitor ratio, the DC-link capacitance ratio is,

$$\frac{C_{fixed}}{C_{variable}} = \frac{5}{6/4} = \frac{10}{3} \tag{2.17}$$

The DC-link voltage ripple (peak-to-peak) percentage is shown in Fig. 2.33. It is clear that even though for both case, the lifetime of electrolytic capacitor is the same, the DC-link voltage ripple is much smaller for the fixed voltage case.

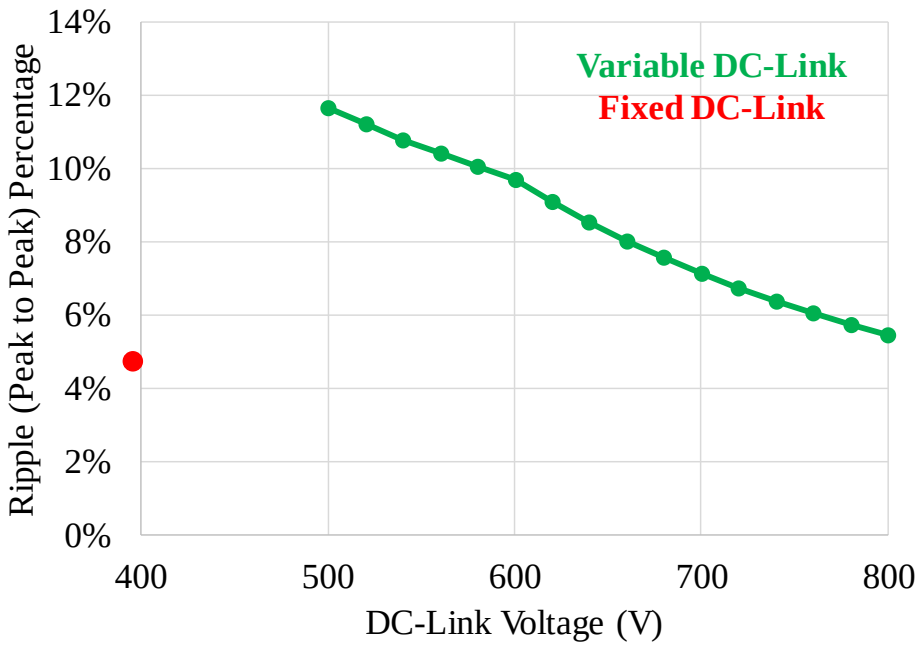


Fig. 2.33. DC-link voltage ripple (peak to peak) percentage comparison.

2.5.3 DC-link capacitor value selection

With the proposed system architecture, the DC/DC stage is only responsible for regulating the double line frequency ripple while the average output voltage is regulated by the AC/DC stage. From above analysis, we can see that in order to reduce the DC-link capacitor size, larger DC-link voltage ripple is generated, which increases the regulation burden of the DC/DC stage due to the larger switching frequency variation. This will also increase the total system loss of the CLLC converter because of the deviation from optimal working condition.

According to Eq. (2.13), the DC-link voltage ripple can be calculated as,

$$\Delta v_{DC_{link}} = i_{DC_{link}} \times \frac{1}{4\pi f C_{DC_{link}}} = \frac{V_{in} I_{in}}{2 V_{dc} \pi f C_{DC_{link}}} \cos(4\pi f t) \tag{2.18}$$

Fig. 2.34 shows the DC-link capacitance impact on DC-link voltage ripple according to Eq. (2.18)

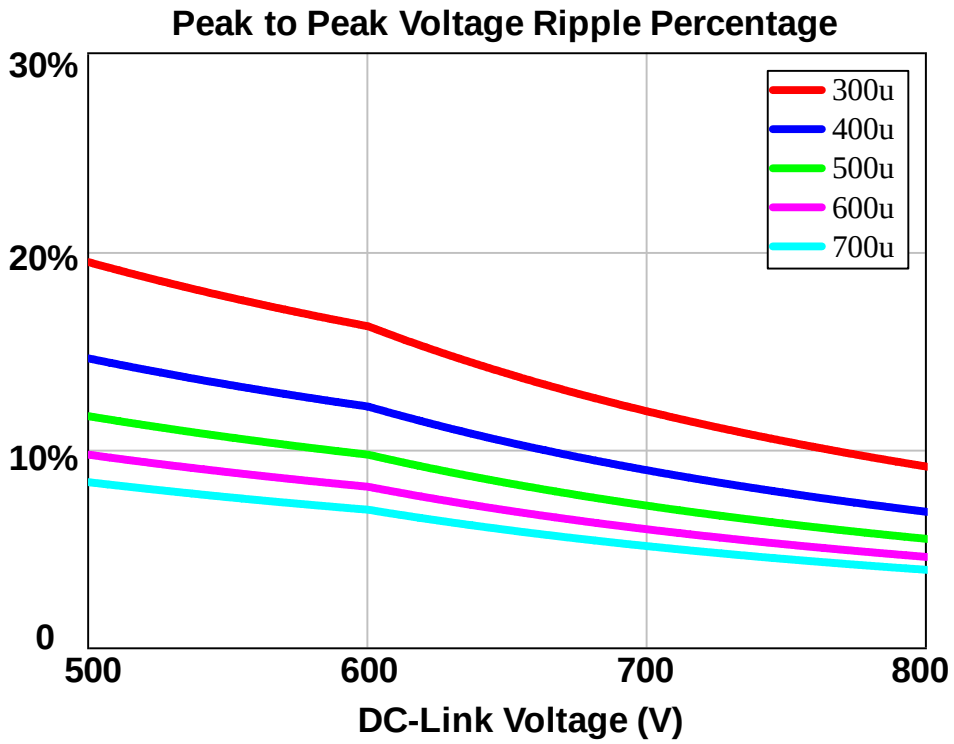


Fig. 2.34. DC-link capacitance impact on DC-link voltage ripple.

It is clear that with the increasing of DC-link capacitance, the ripple voltage becomes smaller. In addition, higher DC-link voltage also means smaller voltage ripple since more power can be stored with the same amount of ripple.

However, there is certain limitation for the maximum and minimum DC-link voltage. Firstly, the device voltage rating is limited. Even though 1.2 kV SiC device is used, the maximum voltage it can handle should be below 900 V considering high current turn off generated ringing. Secondly, the requirement of power factor correction needs to be considered. The maximum RMS value for AC input voltage is 265 V, which is corresponding to 375 V peak input voltage. Under this condition, the minimum DC-link voltage required for power factor correction is above 375 V. If maximum and minimum duty cycle is taken into consideration, the minimum DC-link voltage should be above 390 V.

Fig. 2.35 shows the maximum and minimum DC-link voltage according to different DC-link capacitance. It is clear that to meet the above two requirements, the minimum capacitance value we can use is 200 uF.

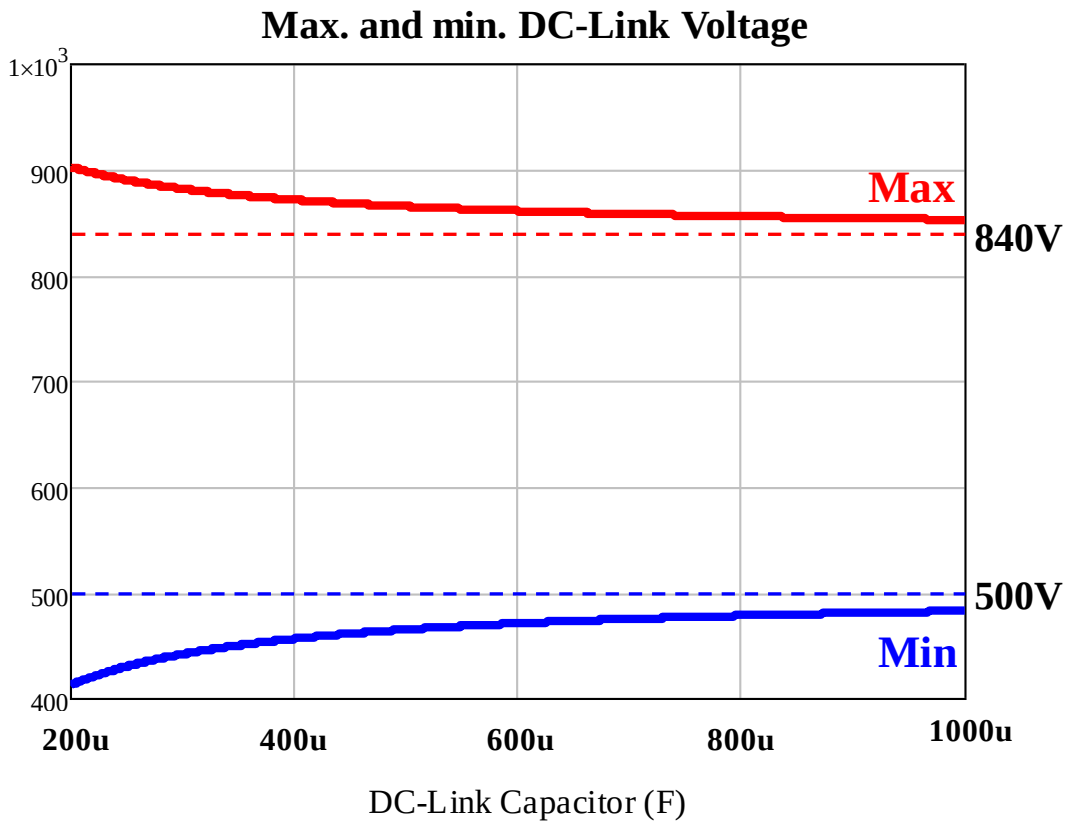


Fig. 2.35. Maximum and minimum DC-link voltage with different DC-link capacitance.

A simulation is conducted in order to get the switching frequency range with different DC-link voltage ripple, and the results are shown in Fig. 2.36.

From this figure, we can see that the larger voltage ripple results in larger switching frequency range. For minimum switching frequency, the worst case is 200 uF DC-link capacitance and 500 V DC-link voltage (corresponding to 250 V battery voltage), and the minimum switching frequency is around 260 kHz ($0.5f_o$). For maximum switching frequency, the worst case is 200 uF DC-link capacitance and 800V DC-link voltage, where the maximum switching frequency reaches over 1 MHz ($> 2f_o$). It should be noted that the switching frequency range is simulated followed by the previously proposed charging profile.

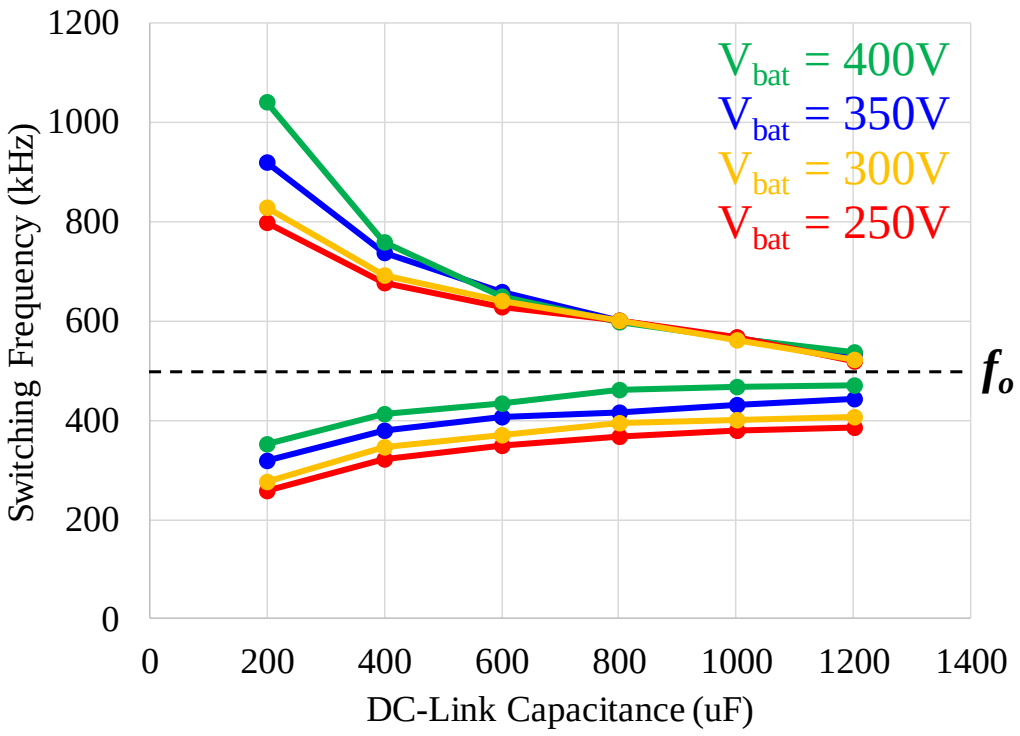


Fig. 2.36. Switching frequency range under different DC-link capacitance.

According to the analysis in Chapter 2, the large switching frequency range can increase the total system loss. Therefore, a loss model is built to analyze the impact of wide switching frequency range (double line frequency).

(1) Device loss

Circuit simulation using SIMPLIS can generate the RMS current flowing through each device as well as the turn off current of the primary side device.

Therefore, the total device loss will be the summary of channel conduction loss, dead time third quadrant reverse conduction loss and the turn off loss.

$$P_{device} = P_{cond} + P_{3rd} + P_{sw} \tag{2.19}$$

(2) Winding loss

A circuit model (as shown in Fig. 2.37) can be built to get the winding loss with different input and output current [33].

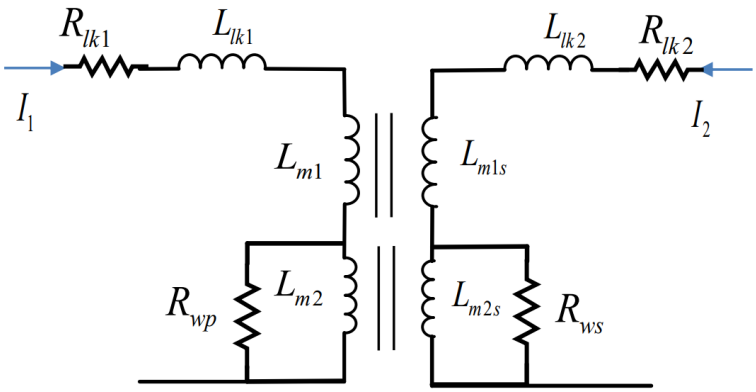


Fig. 2.37. Equivalent circuit for transformer winding loss model.

In this model, R_{lk} represents the winding loss caused by the DC resistance on each side, and the R_w represents the winding loss caused by the mutual coupling between the primary and secondary. The values for R_{wp} and R_{ws} are calculated in order to include the open-circuit loss and the phase shift impact in the simulation.

The parameters in the equivalent circuit for transformer winding loss can be extracted from finite element analysis (FEA).

In FEA, the 2-by-2 impedance matrix of the designed transformer is,

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} R_{11} + j\omega L_{11} & R_{12} + j\omega L_{12} \\ R_{21} + j\omega L_{21} & R_{22} + j\omega L_{22} \end{bmatrix} =$$

$$\begin{bmatrix} 56.7m\Omega + j\omega \times 19.25uH & 39.96m\Omega + j\omega \times 17.85uH \\ 39.96m\Omega + j\omega \times 17.85uH & 56.7m\Omega + j\omega \times 19.25uH \end{bmatrix} \quad (2.20)$$

With this impedance matrix, we can calculate the parameters in the winding loss model, as shown Table 2.3. Due to the symmetry between primary side and secondary side, we also have symmetrical parameters.

Table 2.3. Parameter value in the winding loss model.

Parameter	Value
L_{k1}, L_{k2}	1.4 uH
R_{k1}, R_{k2}	16.74 mΩ
L_{m1}	17.85 uH
L_{m2}	10.74 uH
R_{wp}, R_{ws}	80 mΩ

With these parameters, the transformer winding loss can be simulated under different primary and secondary side current.

(3) Core loss

In [34], an Equivalent Elliptical Loop (EEL) method is proposed to calculate core loss under arbitrary current input. Actually, the core loss is calculated according to the flux density and its changing rate.

$$P_v(t) = |K| \cdot \left|\frac{dB}{dt}\right|^{\alpha} \tag{2.21}$$

Where

$$K = \pm \frac{1}{C_{\alpha\beta}} C_m |B_m \cos(\theta)|^{\beta-\alpha} \tag{2.22}$$

$$C_{\alpha\beta} = (2\pi)^{\alpha} \frac{2}{\pi} \int_0^{\frac{\pi}{2}} \cos^{\beta} \theta \, d\theta \tag{2.23}$$

Here, α, β and C_m is the same as in Steinmetz Equation.

With the above calculation, we can get the relationship between DC-link capacitance and the system loss, as shown in Fig. 2.38.

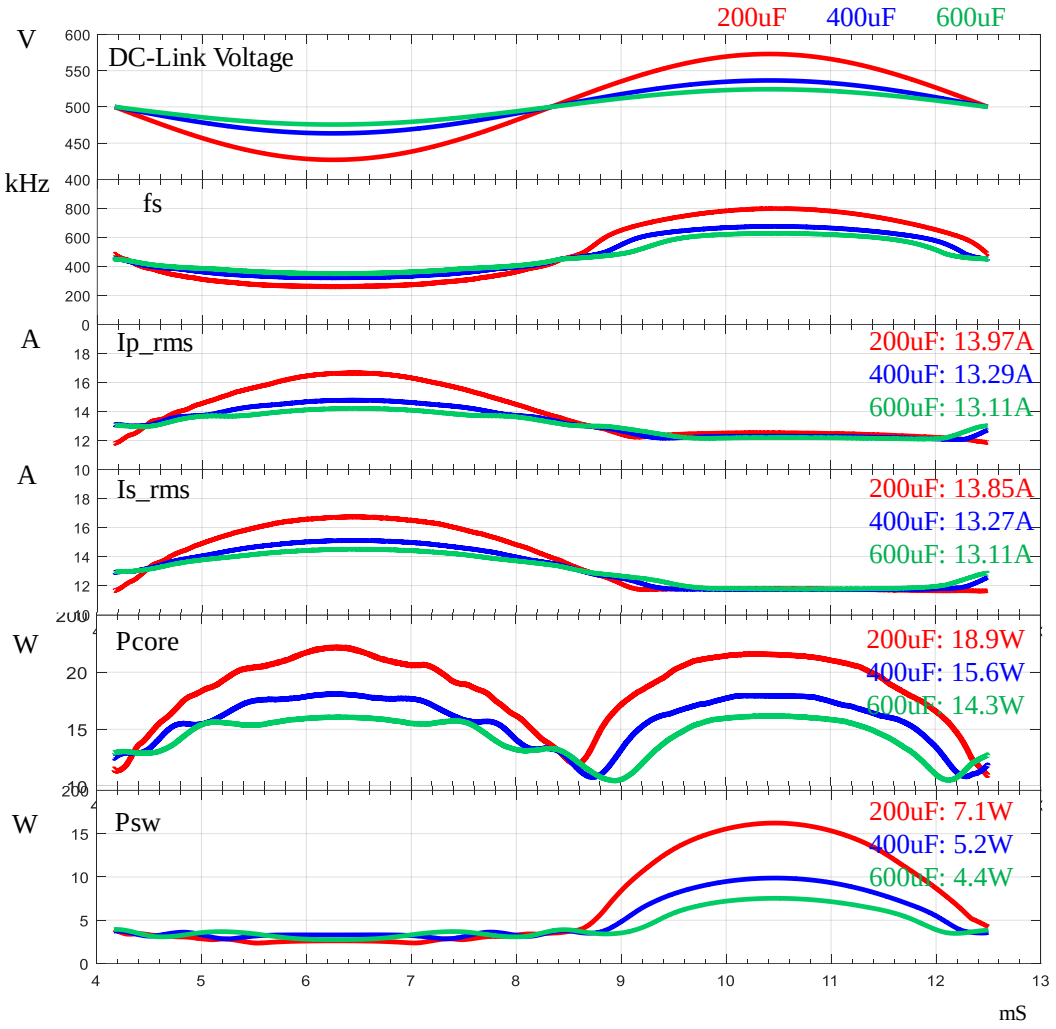


Fig. 2.38. Calculation results for half line cycle. (From top to bottom: DC-link voltage, switching frequency, primary side RMS current, secondary side RMS current, core loss and switching loss).

From this figure, it is clear that DC-link voltage is changing in half line cycle and the corresponding switching frequency is also changing to make sure the output voltage (current) is constant.

When DC-link voltage is lower than twice of the output voltage, switching frequency is smaller than resonant frequency. During this time, the RMS current of primary side and secondary side increases, and the lower DC-link voltage, the lower switching frequency, the higher RMS current. However, when the DC-link voltage is higher than twice of the output voltage, the switching frequency is higher than resonant frequency. During this period, the RMS current of primary side and secondary side stays the same.

Core loss is also increasing when switching frequency deviates from resonant frequency. When switching frequency is lower than resonant frequency, the voltage-second on the core is increasing, which increases the core loss. When switching frequency is higher than resonant frequency, the *dB*/*dt* inside the core becomes larger, which also increases the core loss.

As for the switching loss, when switching frequency is lower than resonant frequency, the turn off current is always magnetizing current, which almost does not change during this period. However, when the switching frequency is higher than resonant frequency, the turn off current becomes much higher, which increases the turn off loss.

The total system efficiency according to different DC-link voltage and DC-link capacitance is shown in Fig. 2.39. We can see that 500 V DC-link voltage is the worst case, where the efficiency drops when smaller DC-link capacitor is used. 600 uF is the best tradeoff between efficiency and the footprint. DC-link capacitance larger than this value will not bring benefit to the efficiency while DC-link capacitance smaller than this value will cause obvious efficiency drop.

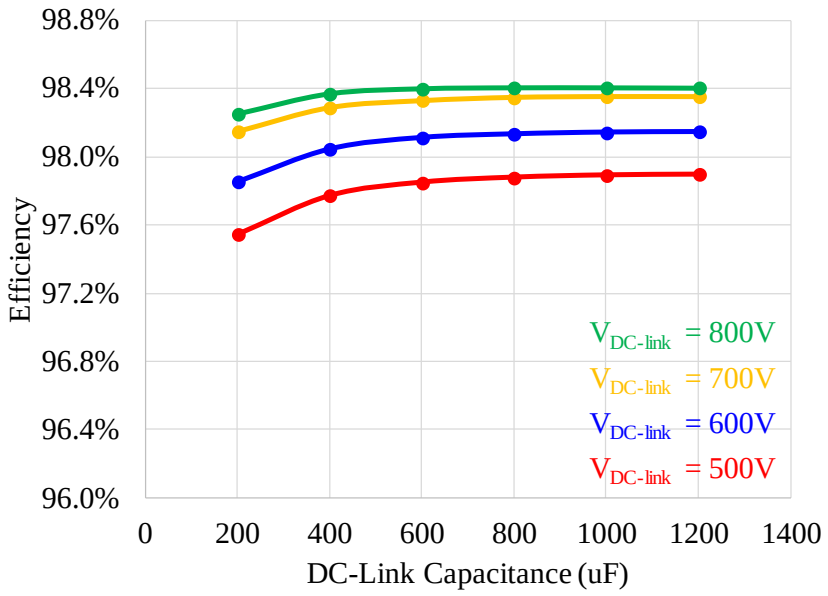


Fig. 2.39. System efficiency according to different DC-link voltage and DC-link capacitance.

2.5.4 **Lifetime consideration**

(1) Electrolytic capacitor

Another very important factor that needs to be take into consideration is the DC-link capacitor lifetime. From Table 2.1 and Table 2.2, we can find out that compared with film capacitor, electrolytic capacitor has much larger capacitance density, which means for the same amount of capacitance, the footprint of electrolytic capacitor is much smaller than that of the film capacitor. However, it should be also noted that the lift time of electrolytic capacitor is much shorter compared with the film capacitor.

The most important two factors that impact the lift time of electrolytic capacitor is the ambient temperature and the current ripple (loss).

According to previous analysis, the current ripple flowing through the DC-link capacitor is

$$i_{DC_{link-RMS}} = \frac{V_{in} I_{in}}{2\sqrt{2} V_{dc}} \tag{2.24}$$

If capacitor from TDK with part No. B43644E5127M0*# is used (120 uF, 450 V, 25 mm x 25 mm), the relationship between lifetime and DC-link capacitance is shown in Fig. 2.40 [35].

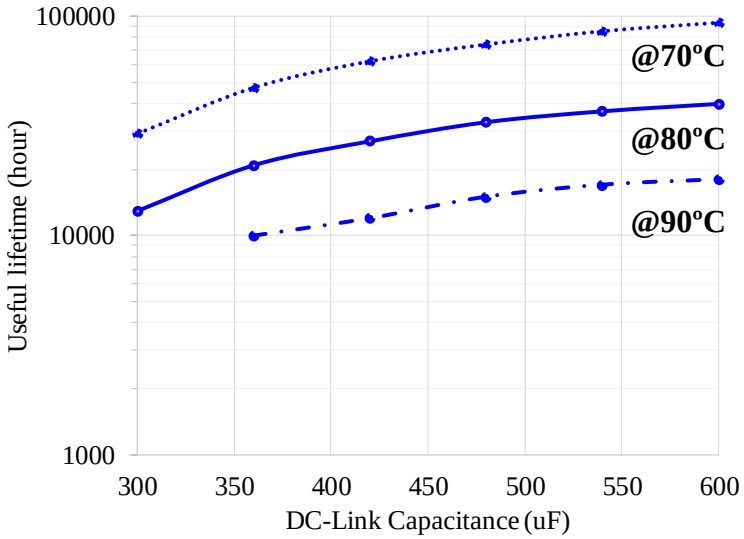


Fig. 2.40. Relationship between lifetime and DC-link capacitance for electrolytic capacitor.

In this figure, the lifetime is calculated based on 70ºC (dotted line), 80ºC (solid line) and 90ºC (dash-dotted) ambient temperature. It is very clear that temperature has a very strong impact of the lifetime. In fact, with 80º ambient temperature, the lifetime of electrolytic capacitor is always less than 50,000 hours.

Fig. 2.41 shows the relationship between DC-link capacitance and total system power density. It is obvious that the larger value capacitance we use the lower power density we can achieve.

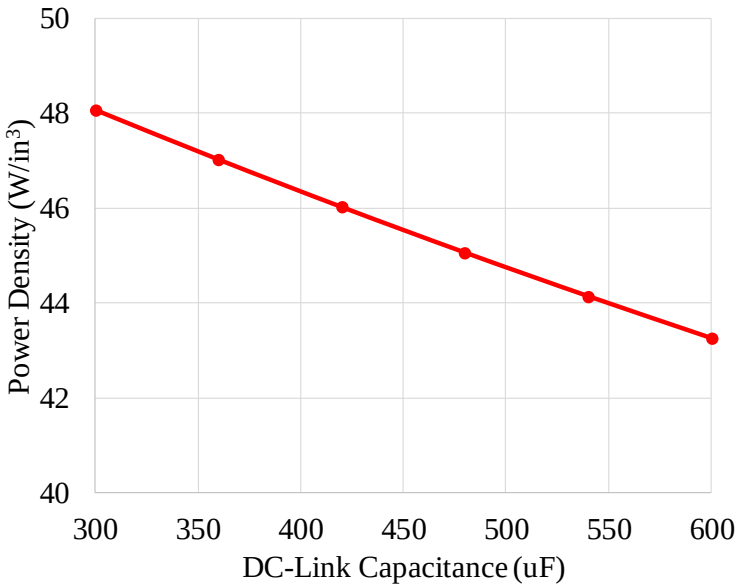


Fig. 2.41. Power density with different value of DC-link capacitance using electrolytic capacitor.

(2) Film capacitor

Compared with electrolytic capacitor, film capacitor can handle much larger current ripple and higher voltage. However, the drawback is the low capacitance density.

Table 2.1 shows the typical film capacitor from different companies. We can see that it is very common to find film capacitor to handle 1 kV DC-link voltage; therefore, there is no need to put capacitors in series. However, the capacitance density of film capacitor is around 10 uF/in^3. Compared with Electrolytic capacitor, which has a density value of 20 uF/in^3, it is still much smaller.

The lifetime of film capacitor is not significantly related to the temperature and current ripple. In fact, the voltage stress on the capacitor has more impact, as shown in Fig. 2.42 [36].

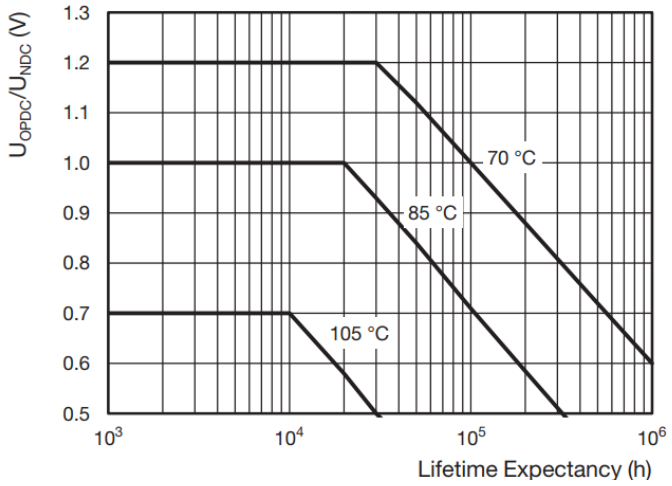


Fig. 2.42. Lifetime expectancy of film capacitor (from VISHAY).

With Fig. 2.42, we can calculate the lifetime expectancy of film capacitor according to different DC-link capacitance, as shown in Fig. 2.43.

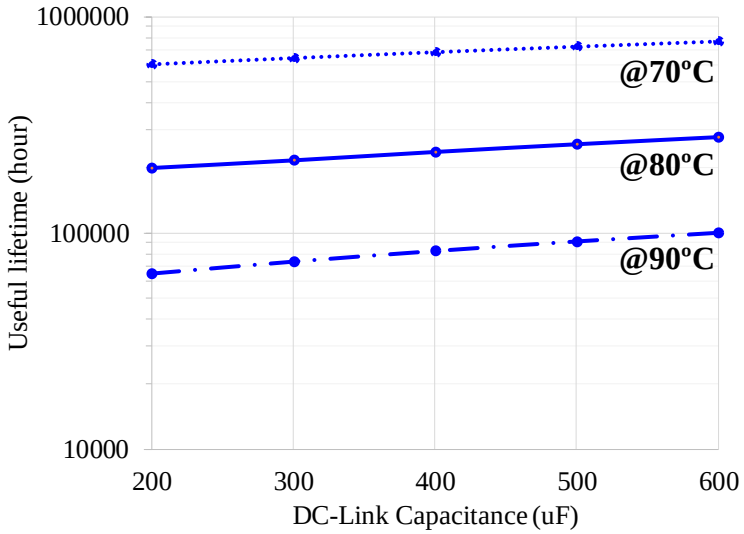


Fig. 2.43. Relationship between lifetime and DC-link capacitance for film capacitor.

From Fig. 2.43, we can see that film capacitor has much longer lifetime. Even under 90ºC ambient temperature, the lifetime of film capacitor can achieve over 60,000 hours.

The relationship between power density and DC-link capacitance for film capacitor is shown in Fig. 2.44.

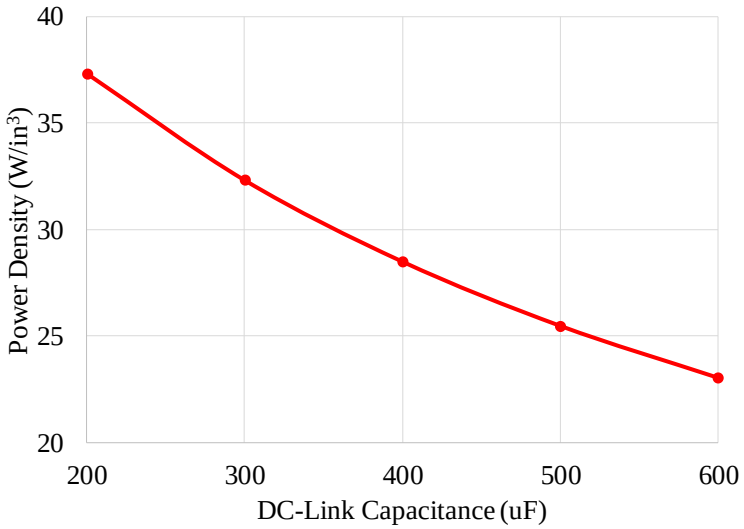


Fig. 2.44. Relationship between power density and DC-link capacitance for film capacitor.

If we compare film capacitor with electrolytic capacitor from power density and lifetime point of view, we have Fig. 2.45.

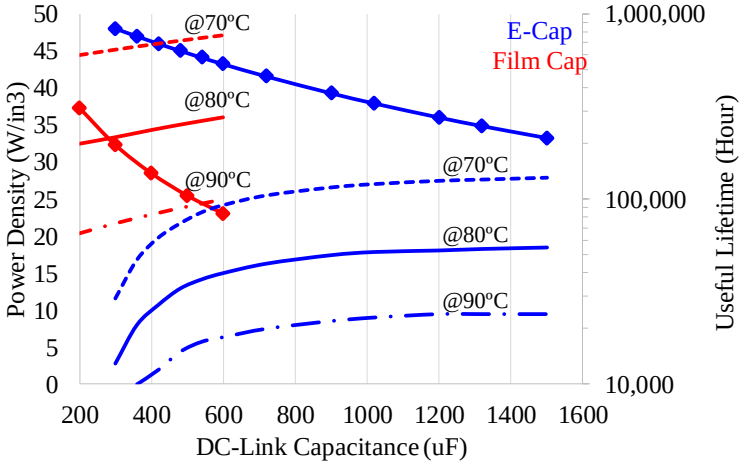


Fig. 2.45. Comparison between electrolytic capacitor and film capacitor for lifetime (line) and power density (line with marker).

From this comparison, we can see that power density of film capacitor is worse than electrolytic capacitor even the capacitance of electrolytic capacitor is five times larger (1000 uF compared with 200 uF). However, from lifetime point of view, under high ambient temperature, the lifetime of electrolytic capacitor is decreasing very quickly and even with very large capacitance, the lifetime is still less than

50,000 hours. For film capacitor, lifetime is not an issue since with 200 uF capacitance and under 90ºC ambient temperature, the lifetime is still larger than 60,000 hours.

From the above analysis, it is clear that when the ambient temperature is high and a long lifetime (> 50,000 hours) is required, film capacitor is a better choice because we can use smaller capacitance and achieve higher power density. However, if the ambient temperature is low and the lifetime requirement is not high, then electrolytic capacitor is more beneficial from power density and efficiency point view due to the much higher capacitance density.

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Chapter 3 **PCB Winding Magnetic with Integrated Resonant Inductors**

With the adoption of wide bandgap devices, the switching frequency of power converters increases to hundreds of kHz. One of the benefits of high frequency operation is the significant reduction of the voltage-second across the transformer. With similar flux density inside the magnetic core, the required number of turns becomes much less, making it possible to use single printed circuit board (PCB) (no separated daughter boards) as transformer windings. For example, in [1], a 6-layer PCB winding coupled inductor for 1.2 kW totem-pole PFC is built. In [2], a 65 W adapter also uses 6-layer PCB to build the flyback transformer. In [3], another 65 W adapter is proposed using two-stage structure. Both the AC/DC and the DC/DC stage use PCB winding magnetics. In [4, 5], a 48 V- 12 V bus converter is designed. Multi-layer PCB is adopted to achieve high power density and high density. In [6], a PCB winding based voltage regulator module is proposed with output current of 140A. In [7-9], a 4-layer/6-layer PCB winding transformer is used for a 400 V-12 V 1 kW DC/DC converter.

Another benefit of high switching frequency operation is the reduced inductance value. With smaller inductance, it is much easier to integrate it into the transformer, reducing the number of magnetic components and their size and volume.

However, there are also challenges come with the high switching frequency and PCB winding magnetics. One of them is the high AC winding loss. Due to skin effect and proximity effect, the AC loss of PCB winding can be overwhelming. A lot of work has been done in this area to calculate and reduce AC loss of PCB winding [10-12]. Interleave is the best solution since it cancels the magnetic field between windings and therefore greatly reduces the AC related loss. However, this configuration also results in very small leakage inductance [13].

The small leakage inductance poses another challenge. For some applications, certain leakage inductance is required to achieve magnetic integration. With such small and uncontrolled leakage inductance, it becomes very difficult. Several methods have been proposed to calculate and control the leakage inductance of transformer. Some of them utilize magnetic shunt to serve as additional magnetic path so that leakage inductance is purposely increased [14, 15]. However, the manufacture of this kind of transformer is complicated and almost impossible to be done automatically with PCB winding. In addition, the core loss of low permeability material is usually much higher, lowering down the efficiency of the transformer. Some propose to purposely separate primary winding and secondary winding so that the desired leakage inductance can be achieved [16]. But with this method, not only the AC winding loss increases due to the compromised interleave structure, but also all the leakage flux is flowing in the air, causing additional eddy current loss and EMI issue. In addition, the realization of such structure using PCB winding is very difficult.

The last challenge is the optimization of PCB winding transformer. Dowell's 1D model [10-12] is widely used for AC winding loss calculation of planar transformers. It is simple and accurate with the assumption that flux is only distributed in one direction. This assumption usually holds for ideal PCB winding transformer where magnetizing current is very small and can be ignored. However, for LLC or CLLC type resonant converter, magnetizing current is utilized to help primary switch achieve zero voltage switching (ZVS). Usually this current is not small enough to be ignored, especially for high power applications, where the junction capacitance of device is much larger, requiring higher magnetizing current. In addition, the fringing effect brought by flux around air gap also has significant impact on winding loss, compromising the accuracy of Dowell's 1D model.

3.1 Matrix transformer with winding interleave

With wide bandgap devices, switching frequency of power electronics converters can be pushed to several hundred kHz, which helps to reduce the voltage-second across the transformer and therefore reduce the required number of turns. This provides us the opportunity to implement windings using PCB.

Compared with litz-wire based magnetics, PCB winding magnetics are more sensitive to high frequency AC winding loss. Due to the limitation of PCB copper layer thickness, the skin effect can have a huge impact on the total winding loss when the frequency becomes very high. In addition, there is no twist between each layer, leading to very prominent proximity effect. AC winding loss of PCB winding transformer can be calculated by the following equation [17] if 1D model is considered .

$$\frac{R_{AC}}{R_{DC}} = \frac{\varepsilon}{2}\left[\frac{\sinh\varepsilon+\sin\varepsilon}{\cosh\varepsilon-\cos\varepsilon} + (2m-1)^2\frac{\sinh\varepsilon-\sin\varepsilon}{\cosh\varepsilon+\cos\varepsilon}\right] \quad (3.1)$$

Where R_{dc} is the DC resistance of the winding. ε is an effective thickness of the skin depth, which is defined as h/δ . h is the thickness of the conductor and δ is the skin depth at the given frequency. m represents a winding portion and defined as,

$$m = \frac{F(h)}{F(h)-F(0)} \quad (3.2)$$

Where *F(h)* and *F(0) are* the magneto motive forces (MMFs) at the surfaces of the layer.

The impact of *m* on AC resistance is shown in Fig. 3.1

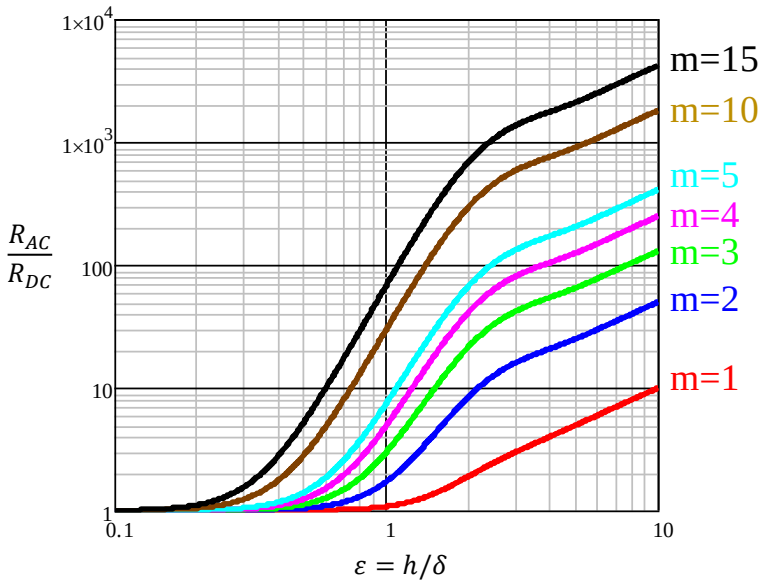


Fig. 3.1. Impact of *m* on AC resistance.

From this figure, it is found that with larger *m*, the increasing of AC resistance also becomes larger. Even when the copper thickness equals to the skin depth ($\varepsilon = 1$), the AC resistance is over 10 times of DC resistance when *m* is larger than 5. Therefore, in order to reduce AC winding loss, *m* has to be kept small.

The best way to reduce *m* value is to interleave primary and secondary windings, which is shown in Fig. 3.2. In this figure, red rectangles represent primary windings while blue rectangles represent secondary windings. The resulted MMF is also shown on the right side. From this figure, with fully interleaved structure, *m* value for each winding is only 1. With $\varepsilon = 1$, AC resistance is around 8.6% larger than DC resistance.

For PCB winding transformer in high power applications, multi-turn per layer is not recommended since it makes multi-layer structure almost impossible with the complicated winding to winding connections. And the reduced winding width results in too much conduction loss. Therefore, if a 6:6 turns ratio PCB winding transformer is adopted in a conventional EI core structure, 12-layer PCB is needed to implement all the windings. Fig. 3.2 shows the cross section view of this EI core transformer.

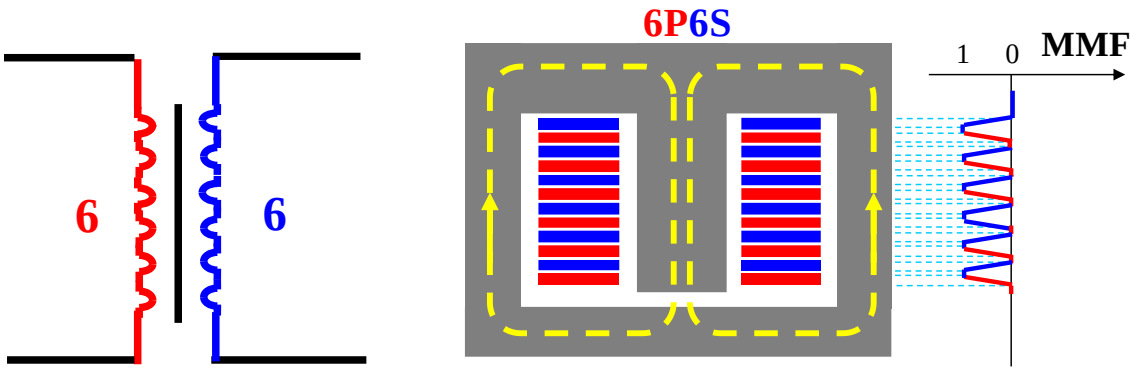


Fig. 3.2. Cross section view of conventional PCB winding transformer using EI core structure with 12-layer board.

However, 12-layer board is too much in practical application due to its high cost, especially in high power applications where the board is much larger. Daughter board is one way to lower down the cost. However, the connections between PCBs are difficult and complicated. Also, it compromises the simplicity of the system and has additional manufacture process involved.

To reduce the number of PCB layers while keep the same number of turns, we can split the single EI core transformer into two UI core transformers, as shown in Fig. 3.3. Both the primary windings and secondary windings are connected in series to achieve 6:6 turn ratio. Due to the series connection, current in each layer for both transformers are the same, so is the flux (yellow line) flowing within each core.

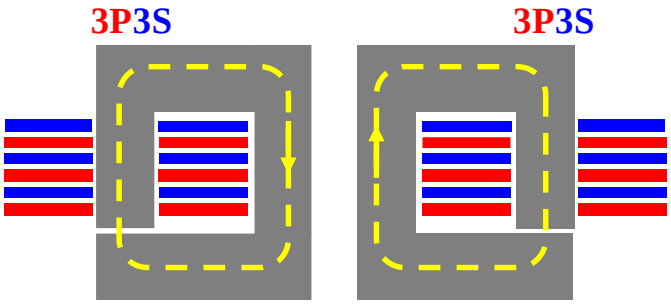
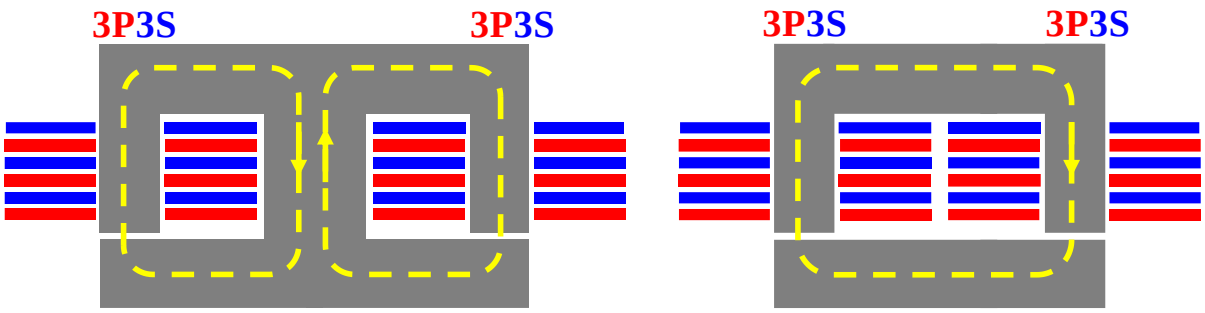


Fig. 3.3. UI core transformer with reduced number of layers.

By using this method, the required number of PCB layers is reduced by half. However, the drawbacks are larger footprint, increased number of cores and higher core loss.

In [7, 8, 18], a matrix transformer concept is proposed. By integrating the two UI core transformers together as shown in Fig. 3.4 (a), with purposely-arranged flux direction, the center post flux from two parts of the windings is in reverse direction and cancelled out. As a result, one single UI core with 6-layer PCB (Fig. 3.4 (b)) can achieve the same number of turns and the total footprint is reduced.



(a) Integrated transformer (b) Reduced footprint with flux cancellation

Fig. 3.4. Integrated matrix transformer with flux cancellation.

3.2 Proposed transformer structure with controllable leakage inductance

For converters like LLC [19], CLLC [20] or dual active bridge [21], apart from the transformer, there are also inductors in series with it. Especially for the bi-directional converters like CLLC or dual active bridge, inductors are required on both side of the transformer. However, there is no good way to build inductors using PCB due to the lack of interleaving [1]. With high frequency operation, the skin effect and proximity effect will generate significant amount of eddy current loss. As a result, litz-wire based discrete inductors are usually used even though it compromises the manufacturability and increases the complexity of the system by introducing additional magnetic components.

Magnetic integration is a good way to simplify the system by using the leakage inductance of the transformer as the additional inductors. However, it requires certain leakage inductance value according to the design of the converter. For example, if good regulation for resonant converter is desired or large zero voltage switching (ZVS) range for dual active bridge is needed, a large inductor value is required.

Although the matrix transformer structure provides a very good solution to achieve higher number of turns with less number of layers, its leakage inductance is not controllable and is quite small due to the interleaving between the primary windings and secondary windings. 2D finite element analysis (FEA) using ANSYS Electronics Desktop shows that the resulted leakage inductance is only around 100 nH (Fig. 3.5), which is too small to achieve magnetic integration.

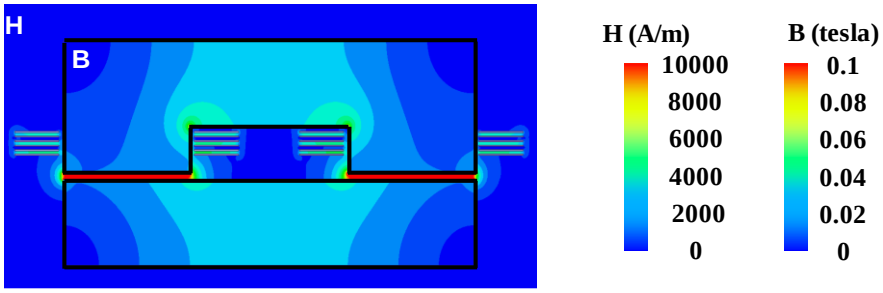


Fig. 3.5. 2D FEA simulation result of the fully interleaved transformer structure.

When interleave is not used, as shown in Fig. 3.7, more leakage inductance can be generated, which is around 2 uH. But at this time, AC winding loss increases significantly since there's no interleaving between primary windings and secondary windings and the MMF becomes very high. Winding loss simulation results are shown in Fig. 3.7 for both interleaved winding structure (Fig. 3.7 (a)) and non-interleaved winding structure (Fig. 3.7 (b)). We can see that without interleaving, current crowding becomes very severe and winding loss increases over 8 times

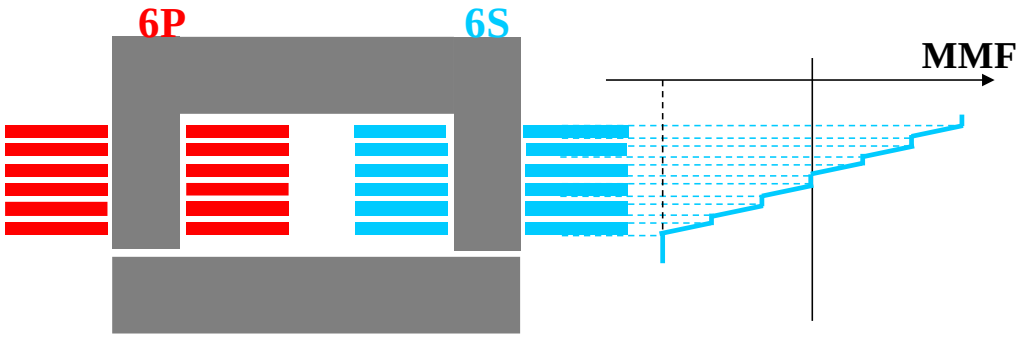
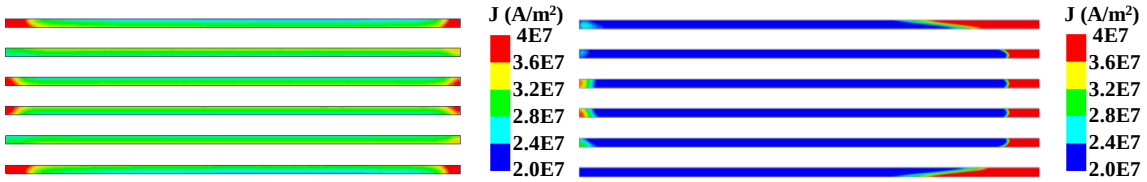


Fig. 3.6. Winding structure with no interleave.



(a) (b)

Fig. 3.7. Current distribution comparison between (a) interleaved winding and (b) non-interleaved winding.

Several methods have been proposed to introduce additional leakage inductance. Such as increasing the distance between primary windings and secondary windings or adding additional low permeability materials as magnetic shunt. However, both of them sacrifice winding interleave and the transformer structures are quite complicated. Therefore, neither of these methods are suitable for PCB winding magnetics.

In order to increase the leakage inductance, we need to create flux that is not coupled between primary windings and secondary windings. Therefore, instead of using evenly distributed windings as shown in Fig. 3.3, we can use two UI core transformer with turns ratio of 2:4 and 4:2 respectively, as shown.in Fig. 3.8.

It is clear that for each transformer, the primary windings and secondary windings are perfectly coupled and the leakage inductance of each transformer is very small. If we ignore the reluctance of the magnetic core and only consider the reluctance of the air gap, the self-inductance and mutual-inductance matrices for the two transformers can be written as,

$$\begin{bmatrix} v_{p1} \\ v_{s1} \end{bmatrix} = \begin{bmatrix} \frac{4}{R_g} & \frac{8}{R_g} \\ \frac{8}{R_g} & \frac{16}{R_g} \end{bmatrix} \begin{bmatrix} \frac{di_{p1}}{dt} \\ \frac{di_{s1}}{dt} \end{bmatrix} \tag{3.3}$$

$$\begin{bmatrix} v_{p2} \\ v_{s2} \end{bmatrix} = \begin{bmatrix} \frac{16}{R_g} & \frac{8}{R_g} \\ \frac{8}{R_g} & \frac{4}{R_g} \end{bmatrix} \begin{bmatrix} \frac{di_{p2}}{dt} \\ \frac{di_{s2}}{dt} \end{bmatrix} \tag{3.4}$$

Where R_g is the reluctance of the air gap.

$$R_g = \frac{l_g}{\mu_r \mu_0 A_e} \tag{3.5}$$

A_e and l_g are the area and length of the air gap respectively.

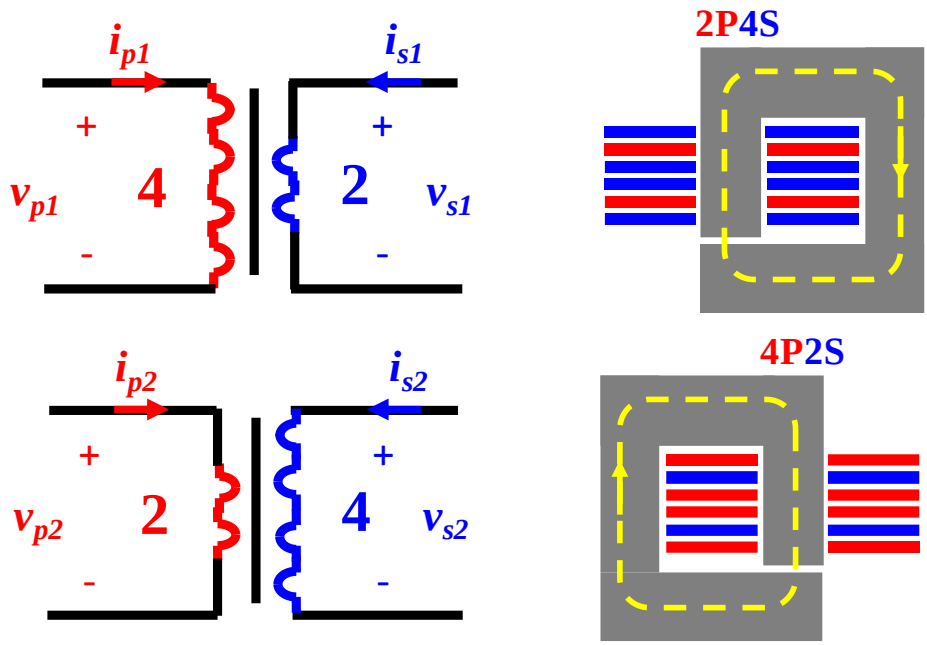


Fig. 3.8. Transformer with unbalanced winding distribution.

If we connect the two transformers in a way that primary windings are all in series and secondary windings are all in series, as shown in Fig. 3.9, due to the symmetry, we have

$$i_p = i_{p1} = i_{p2}$$

$$i_s = i_{s1} = i_{s2} \tag{3.6}$$

The resulted self-inductance and mutual-inductance matrix is,

$$\begin{bmatrix} v_p \\ v_s \end{bmatrix} = \begin{bmatrix} \frac{20}{R_g} & \frac{16}{R_g} \\ \frac{16}{R_g} & \frac{20}{R_g} \end{bmatrix} \begin{bmatrix} \frac{di_p}{dt} \\ \frac{di_s}{dt} \end{bmatrix} \tag{3.7}$$

From this matrix, we can easily calculate the magnetizing inductance and leakage inductance of both sides,

$$L_m = \frac{16}{R_g}$$

$$L_{kp} = L_{ks} = \frac{4}{R_g} \tag{3.8}$$

And the turns ratio is 1:1.

It is clear that by connecting the two UI core transformers, the resulted transformer has a built-in leakage inductance. However, the ratio between magnetizing inductance and leakage inductance is four for the given 6-layer transformer example.

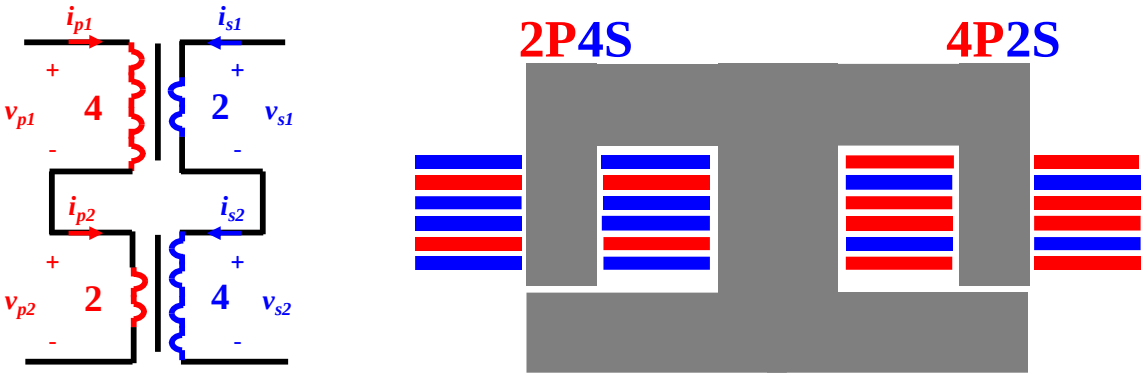


Fig. 3.9. Two transformers connected in series to have a built-in leakage inductance.

In order to control the magnetizing inductance and leakage inductance separately, another air gap is introduced, which is located at the center post, as shown in Fig. 3.10.

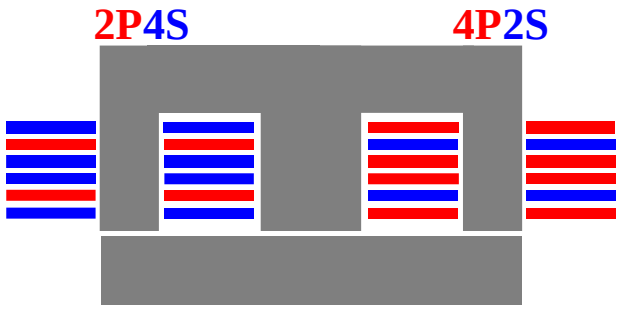


Fig. 3.10. Matrix transformer with unbalanced winding distribution and air gap in center post.

With this structure, by modifying the reluctance of the outer post and center post air gaps, we can control the magnetizing inductance and leakage inductance of the transformer. In addition, most of the interleaving between the primary windings and secondary windings is kept, meaning that low AC winding

loss can still be achieved, which is very important for PCB winding magnetics with high frequency operation.

3.3 Reluctance model of the proposed magnetic structure

Based on this transformer structure, a reluctance model is built, as shown in Fig. 3.11. We made two assumptions to simplify the model without losing accuracy. 1) The permeability of the core is much larger than 1 (permeability of the air). 2) Leakage flux in the air is very small and can be ignored. With the above two assumptions, only the reluctance of the air gap needs to be taken into consideration, which are R_{g1} and R_{g2} for outer post and center post respectively.

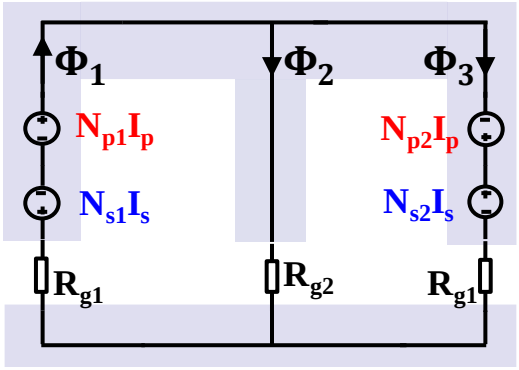


Fig. 3.11. Reluctance model of the proposed transformer structure.

With the reluctance model, the flux inside each core post can be calculated by,

$$\Phi_1 = \frac{(N_{p1}R_{g1}+N_{p1}R_{g2}+N_{p2}R_{g2})i_p-(N_{s1}R_{g1}+N_{s1}R_{g2}+N_{s2}R_{g2})i_s}{R_{g1}(R_{g1}+2R_{g2})} \quad (3.9)$$

$$\Phi_2 = \frac{(N_{p1}-N_{p2})i_p+(N_{s2}-N_{s1})i_s}{R_{g1}+2R_{g2}} \quad (3.10)$$

$$\Phi_3 = \frac{(N_{p1}R_{g2}+N_{p2}R_{g1}+N_{p2}R_{g2})i_p-(N_{s1}R_{g2}+N_{s2}R_{g1}+N_{s2}R_{g2})i_s}{R_{g1}(R_{g1}+2R_{g2})} \quad (3.11)$$

The direction of the flux in each post is also shown in Fig. 3.11.

From these equations, we can see that the flux in each core post is determined by the air gap reluctance R_{g1}, R_{g2}, primary current, secondary current and winding arrangement on the two outer post. With non-ideal transformer (considering magnetizing current), the flux distribution between left core post and right core post are not the same.

For transformer structure shown in Fig. 3.10, we have $N_{p1} = 4$, $N_{s1} = 2$, $N_{p2} = 2$, $N_{s2} = 4$;

Using the reluctance model, we can calculate the flux in each core post.

$$\Phi_1 = \frac{2(2R_{g1}i_p+3R_{g2}i_p-R_{g1}i_s-3R_{g2}i_s)}{R_{g1}(R_{g1}+2R_{g2})} \tag{3.12}$$

$$\Phi_2 = \frac{2(i_p+i_s)}{R_{g1}+2R_{g2}} \tag{3.13}$$

$$\Phi_3 = \frac{2(R_{g1}i_p+3R_{g2}i_p-2R_{g1}i_s-3R_{g2}i_s)}{R_{g1}(R_{g1}+2R_{g2})} \tag{3.14}$$

Where,

$$R_{g1} = \frac{l_{g1}}{\mu_r\mu_0 A_1} \tag{3.15}$$

$$R_{g2} = \frac{l_{g2}}{\mu_r\mu_0 A_2} \tag{3.16}$$

A_1, A_2 and l_{g1}, l_{g2} are the area and length of the outer post and center post air gap respectively.

If transformer T-model is used, as shown in Fig. 3.12, magnetizing inductance and leakage inductance can be calculated by the following equations.

$$L_m = \frac{N_{s1}\Phi_1|_{i_s=0}+N_{s2}\Phi_3|_{i_s=0}}{i_p} = \frac{18}{R_{g1}} - \frac{2}{R_{g1}+2R_{g2}} \tag{3.17}$$

$$L_{kp} = L_{ks} = \frac{N_{p1}\Phi_1|_{i_s=0}+N_{p2}\Phi_3|_{i_s=0}}{i_p} - \frac{N_{s1}\Phi_1|_{i_s=0}+N_{s2}\Phi_3|_{i_s=0}}{i_p} = \frac{4}{R_{g1}+2R_{g2}} \tag{3.18}$$

Due to the symmetry of the primary side and secondary side, leakage inductance on both sides is the same, and the turns ratio *N* is 1.

For a desired magnetizing inductance and leakage inductance, we can calculate the required air gap reluctance by the following equations,

$$R_{g1} = \frac{36}{2L_m + L_{kp}} \tag{3.19}$$

$$R_{g2} = \frac{2}{L_{kp}} - \frac{18}{2L_m + L_{kp}} \tag{3.20}$$

Together with Eq. (3.17) and Eq. (3.18), we can calculate the required air gap length for different magnetizing and leakage inductance.

$$l_{g1} = A_1 R_{g1} \mu_r \mu_0 = \frac{36 A_1 \mu_r \mu_0}{L_{kp} + 2L_m} \tag{3.21}$$

$$l_{g2} = A_2 R_{g2} \mu_r \mu_0 = A_2 \mu_r \mu_0 \left(\frac{2}{L_{kp}} - \frac{18}{2L_m + L_{kp}} \right) \tag{3.22}$$

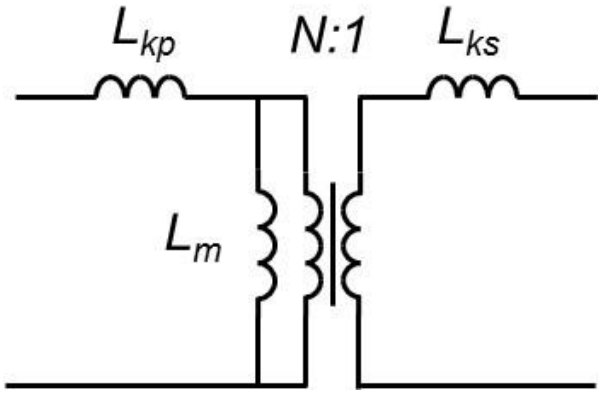


Fig. 3.12. T-model of transformer.

It is clear that with the proposed EI core structure, both magnetizing and leakage inductance can be controlled by adjusting the reluctance of the air gap.

In fact, changing air gap length is not the only way. The center post air gap reluctance can also be controlled by the cross section area, as shown in Eq.(3.16). As a result, we can use uniform air gap length among the three core posts and change the cross section area of center post to achieve the desired leakage inductance,

$$l_{g1} = l_{g2} = l_g = A_1 R_{g1} \mu_r \mu_0 = \frac{36 A_1 \mu_r \mu_0}{L_{kp}+2L_m} \tag{3.23}$$

$$A_2 = \frac{l_g}{\mu_r \mu_0 R_{g2}} = \frac{l_g}{\mu_r \mu_0 \left(\frac{2}{L_{kp}} - \frac{18}{2L_m+L_{kp}}\right)} \tag{3.24}$$

Using 2D FEA simulation, we are able to verify the reluctance model.

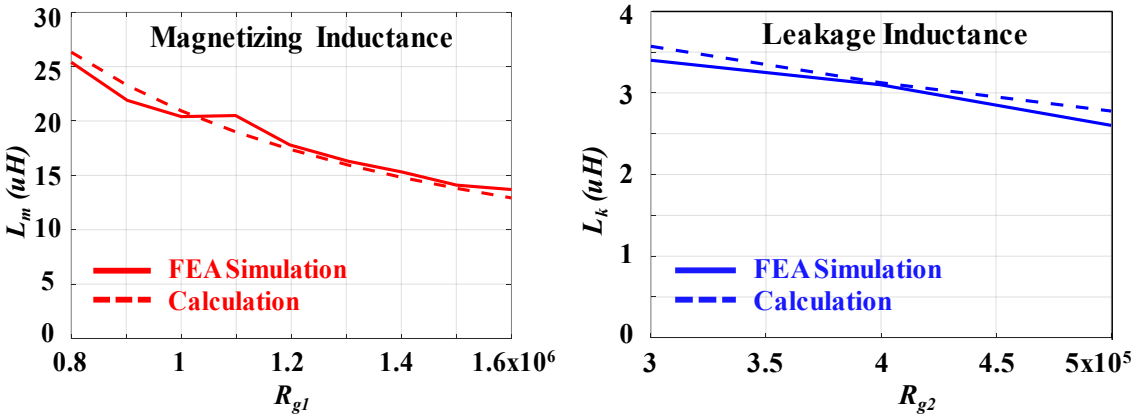


Fig. 3.13. Verification of the reluctance model.

With the proposed EI core transformer structure, we can separately control the magnetizing inductance and leakage inductance by using different combinations of R_{g1} and R_{g2}. However, there are still limitations regarding to how much leakage inductance we can achieve.

Eq.(3.25) gives the generalized calculation of magnetizing inductance and leakage inductance for a 1:1 transformer.

$$L_m = \frac{N^2}{2R_{g1}} - \frac{(2N_1-N)^2}{2R_{g1}+4R_{g2}}$$

$$L_k = \frac{(2N_1-N)^2}{R_{g1}+2R_{g2}} \tag{3.25}$$

Where N is the total number primary windings and N_1 is the number of primary windings on the left post ($N_1 \leq \frac{N}{2}$).

From this equation, we can get the ratio between magnetizing inductance and leakage inductance L_n.

$$L_n = \frac{L_m}{L_k} = \frac{N^2}{(2N_1 - N)^2 \frac{R_{g1}}{R_{g2}}} + \frac{2N_1(N-N_1)}{(2N_1-N)^2} \tag{3.26}$$

The minimum ratio between magnetizing inductance and leakage inductance is achieved when R_{g2} = 0, and it is the case shown in Fig. 3.9.

$$\min(L_n) = \frac{2N_1(N-N_1)}{(2N_1-N)^2} \tag{3.27}$$

In fact, L_n is a very important factor in resonant converters. It determines the peak gain of the converter and also the switching frequency range for a certain input and output voltage range.

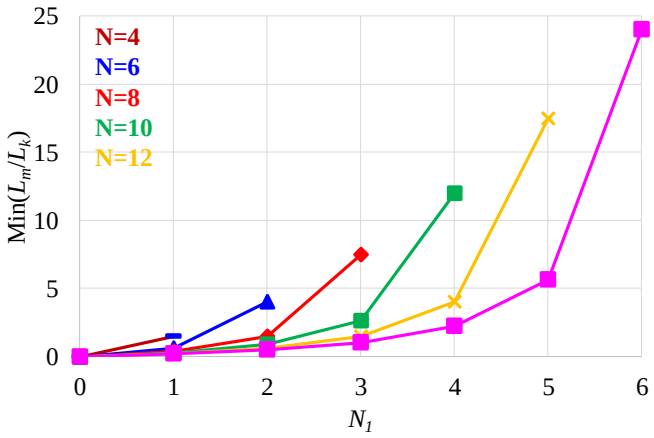


Fig. 3.14. Minimum ratio between magnetizing inductance and leakage inductance.

Fig. 3.14 shows the minimum L_n with different N and N_1. From this figure, we can find out that with more unbalancing in the winding distribution (smaller N_1), we can achieve smaller minimum L_n (larger leakage inductance with the same magnetizing inductance). However, it also means that we have less interleave between primary and secondary windings, resulting in larger AC winding loss. Therefore, for design purpose, we should choose larger N_1 as long as the minimum L_n satisfies our requirement. Then we

can adjust the reluctance of outer post and center post to achieve the desired magnetizing inductance and leakage inductance.

The benefits of the proposed EI core transformer structure is obvious. The leakage flux is controlled by the reluctance of the center post air gap. If the center post air gap reluctance is large, less leakage flux will flow through it, resulting in smaller leakage inductance. If the center post air gap reluctance is small, more leakage flux will flow through it, resulting in large leakage inductance. In addition, compared with conventional transformer, the leakage flux in the proposed magnetic structure is confined within the core instead of in the air. The confined flux can help with radiated EMI and reduce eddy current loss in the surrounding metals.

2D FEA is conducted to get the flux distribution of the proposed transformer structure, and the result is shown in Fig. 3.15. From this figure, we can see that large amount of flux is flowing through the center post, and most of it is leakage flux.

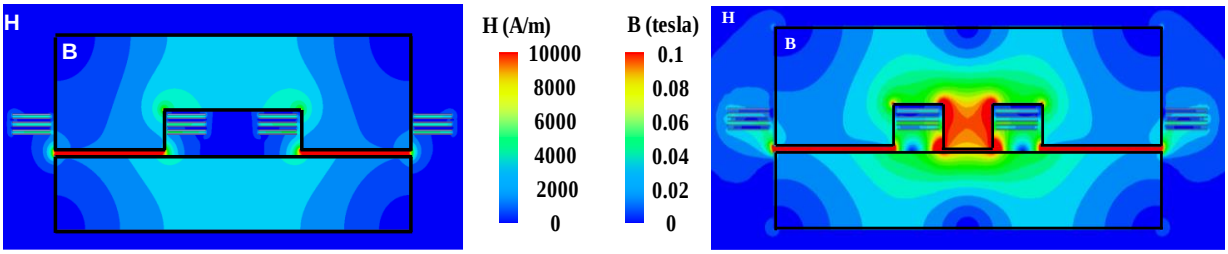


Fig. 3.15. Flux distribution comparison between (a) fully interleaved structure and (b) the proposed magnetic structure.

From this comparison, we can also find out that very strong flux is concentrated in the center post of the core for the proposed magnetic structure while the flux in the air is very weak. The averaged magnetic flux in the air is 540 A/m for the fully interleaved structure and 1200 A/m for the proposed magnetic structure. The leakage inductance increases 14 times (104 nH to 1.5 uH) while the flux in the air increases one time.

3.4 Transformer loss model

In order to get a proper transformer design, loss model is usually needed, including both core loss and winding loss. Dowell's 1D model [10-12] has been widely used to calculate the AC winding loss of planar transformers. However, one important assumption for an accurate 1D model is that magnetic field is distributed evenly in horizontal direction (parallel with winding) and the vertical direction (perpendicular to winding) flux distribution can be ignored. For an ideal transformer (assuming 1:1 turns ratio for simplicity), of which the primary side current is the same with the secondary side current, this usually holds, as shown in Fig. 3.16. But in practical, several factors can compromise this assumption.

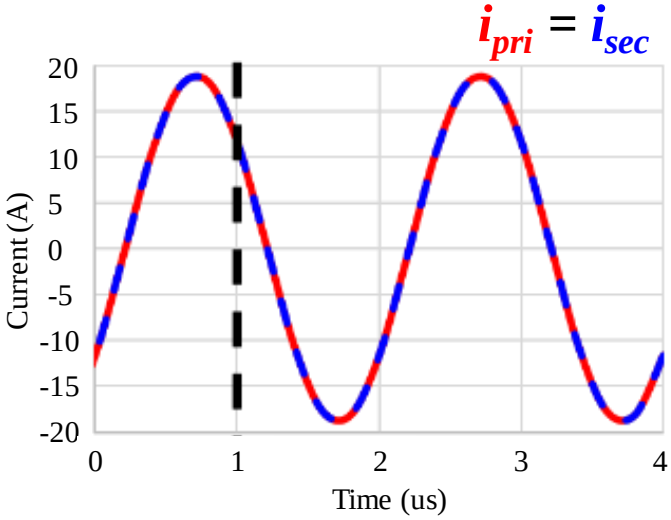
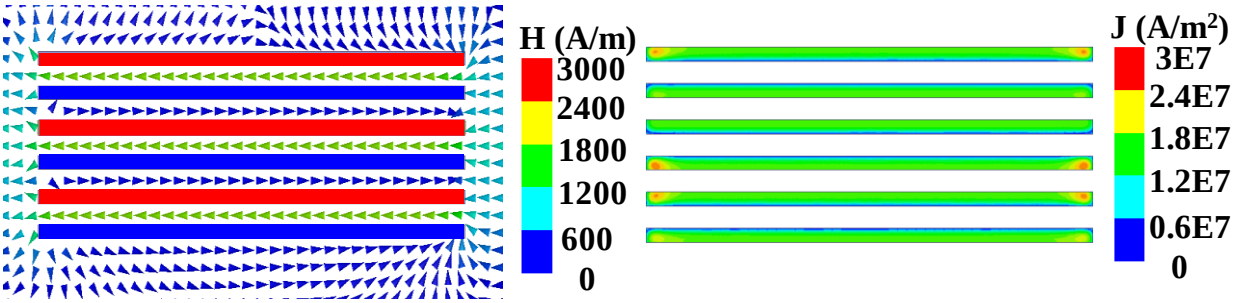


Fig. 3.16. Primary and secondary side current waveform of ideal transformer.



(a) (b)

Fig. 3.17. (a) Magnetic field and (a) current distribution of ideal transformer @ 1 us (in Fig. 3.16).

For LLC or CLLC type resonant converter, magnetizing current is utilized to realize soft switching of the primary side switches. As a result, the primary side current and secondary side current cannot be considered the same, as shown in Fig. 3.18. The resulted magnetic field distribution and current distribution

are shown in Fig. 3.19. It is clear that when magnetizing current is not ignored, magnetic field is not horizontal anymore and a large portion of vertical magnetic field appears. The assumption of Dowell's equation does not hold under this condition. Neither is the 1D model.

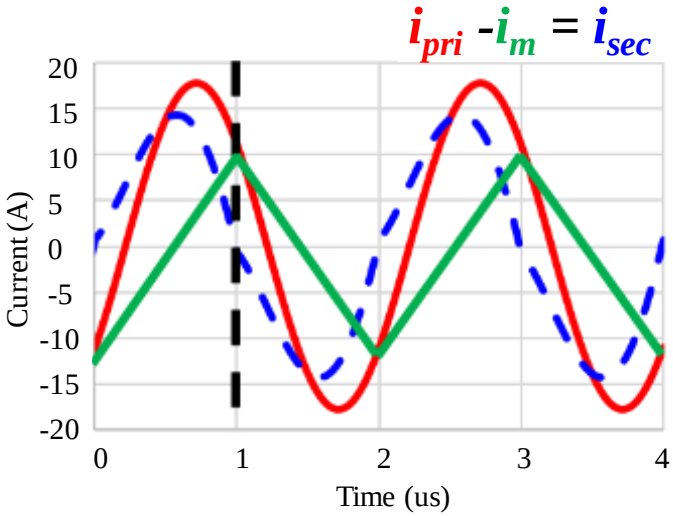
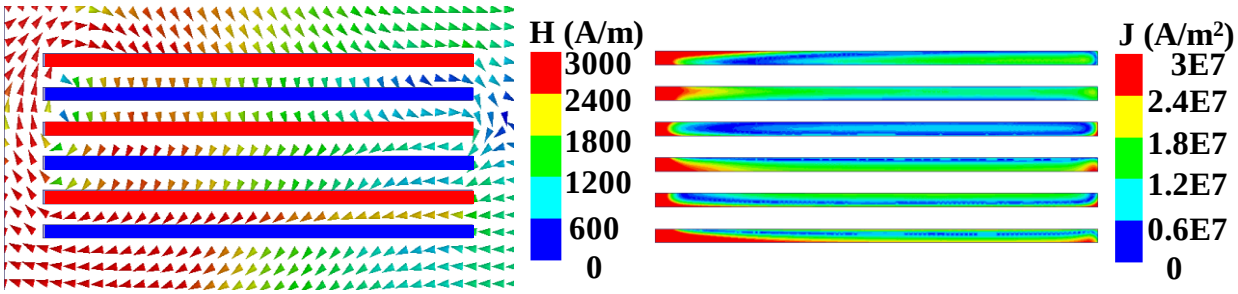


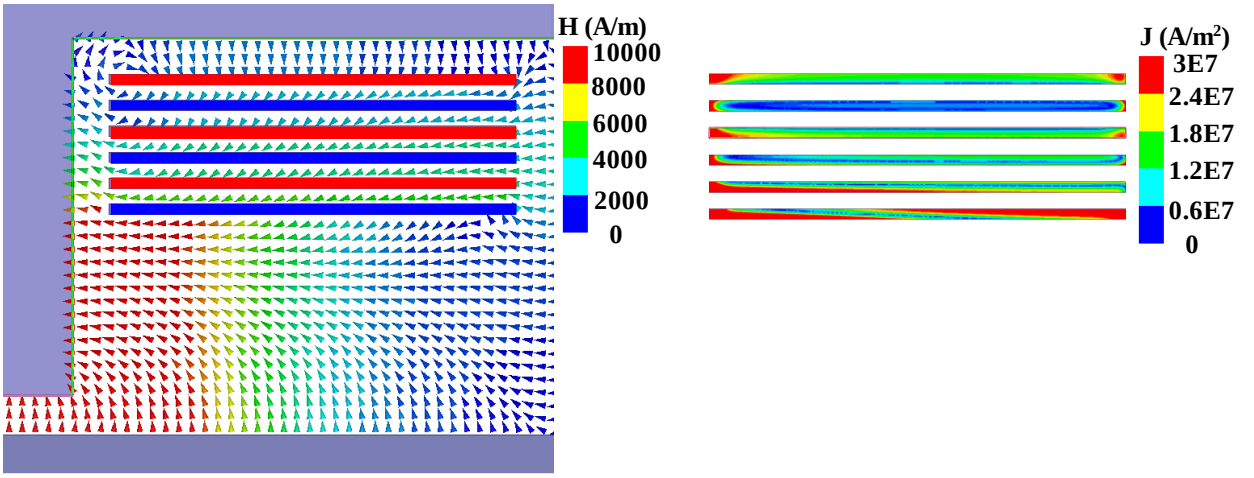
Fig. 3.18. Current waveform of non-ideal transformer.



(a) (b)

Fig. 3.19. (a) Magnetic field and (a) current distribution of non-ideal transformer @ 1 μs (in Fig. 3.18).

Another factor that has impact on winding loss is the air gap. In order to get the required magnetizing current, certain magnetizing inductance is needed, which means air gap needs to be inserted. The magnetic flux around air gap radiates and has significant impact on the distribution of magnetic flux, as shown in Fig. 3.20. Although windings can be positioned far from the air gap, the impact still exists and further comprises the assumption of Dowell's 1D model.



(a) (b)

Fig. 3.20. Fringing flux impact on (a) magnetic field and (a) current distribution @ 1 us (in Fig. 3.18).

From above analysis, we can see that both magnetizing current and air gap have impact on the magnetic flux distribution around the windings. 2D FEA simulation is built to quantify the impact of magnetizing current and fringing effect, and the results are shown in Fig. 3.21.

Total winding loss is simulated with different winding width. Without the impact of magnetizing current and fringing effect of the air gap, the calculation results are very accurate compared with FEA simulation. However, if the two impacts are taken into consideration, the loss of the winding increases as much as 50%. It should be noted that in all the simulations, windings are placed far away (5 times of air gap length) from the air gap to minimize the fringing effect.

This result is based on perfect interleave winding structure. For non-perfect interleave winding structure, the difference between calculation and FEA simulation can be even larger.

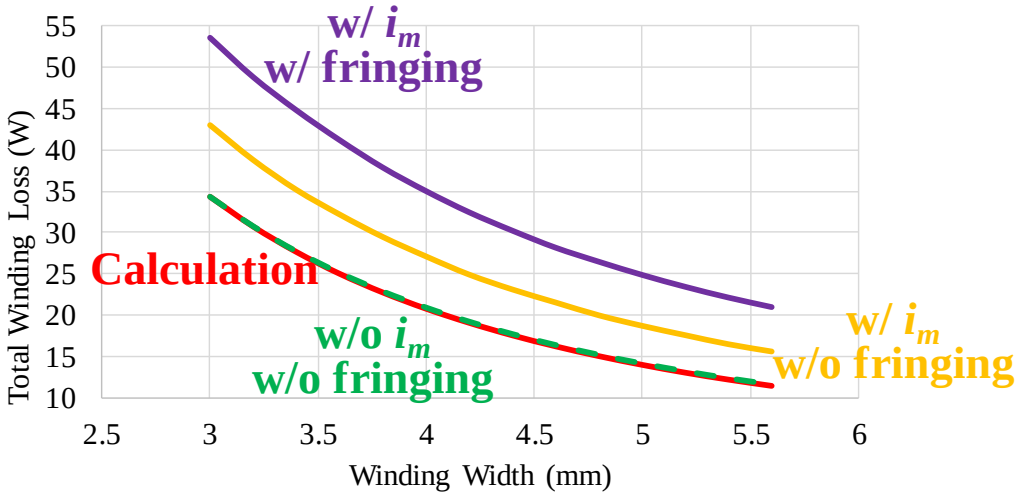


Fig. 3.21. 2D FEA simulation results.

According to the above analysis, in order to take into account the impact of magnetizing current and fringing effect of the air gap, 2D FEA simulation is used to get the accurate winding loss.

From the model, it is easy to identify that the total winding loss is related to the following transformer parameters,

$$P_{winding} = P_{winding}(a, b, b_c, c) \tag{3.28}$$

Where

a is the core post length; *b* and b_c are the outer and center post width respectively; *c* is winding width; *d* is the clearance between winding and core, which is 0.5 mm as constant. All the parameters related to the transformer dimension are marked in Fig. 3.22.

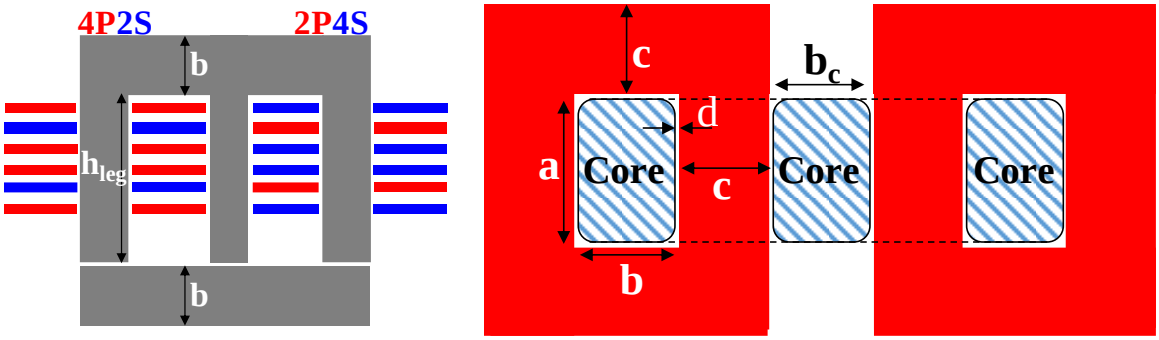


Fig. 3.22. EI core structure with marked dimensions.

It should be noted here that h_{leg} is the outer core post height. For a given 2.4 mm 6-layer board, h_{leg} is selected as 6.2 mm to avoid fringing flux brought by air gap. The distance between winding and air gap is 5 times of the air gap length.

Transformer core loss can be calculated by Steinmetz Equation.

For a given EI core structure, as shown in Fig. 3.22, according to Eq.(3.12) – Eq.(3.14), flux density inside the core can be calculated as,

$$B_1\left(i_p, i_s, a, b, R_{g1}, R_{g2}\right) = \frac{\Phi_1}{ab} = \frac{2\left(2R_{g1}i_p + 3R_{g2}i_p - R_{g1}i_s - 3R_{g2}i_s\right)}{R_{g1}\left(R_{g1}+2R_{g2}\right)}\frac{1}{ab} \tag{3.29}$$

$$B_2\left(i_p, i_s, a, b_C, R_{g1}, R_{g2}\right) = \frac{\Phi_2}{ab_c} = \frac{2\left(i_p+i_s\right)}{R_{g1}+2R_{g2}}\frac{1}{ab_c} \tag{3.30}$$

$$B_3\left(i_p, i_s, a, b, R_{g1}, R_{g2}\right) = \frac{\Phi_3}{ab} = \frac{2\left(R_{g1}i_p + 3R_{g2}i_p - 2R_{g1}i_s - 3R_{g2}i_s\right)}{R_{g1}\left(R_{g1}+2R_{g2}\right)}\frac{1}{ab} \tag{3.31}$$

If we apply Eq.(3.19) – Eq.(3.20), then we have,

$$B_1\left(i_p, i_s, a, b, L_{kp}, L_m\right) = \frac{2\left[\frac{72}{L_{kp}+2L_m}i_p + \frac{3\left(4L_m-16L_{kp}\right)}{L_{kp}\left(L_{kp}+2L_m\right)}i_p - \frac{36}{L_{kp}+2L_m}i_s - \frac{3\left(4L_m-16L_{kp}\right)}{L_{kp}\left(L_{kp}+2L_m\right)}i_s\right]}{\frac{36}{L_{kp}+2L_m}\left[\frac{36}{L_{kp}+2L_m} + \frac{8\left(L_m-4L_{kp}\right)}{L_{kp}\left(L_{kp}+2L_m\right)}\right]}\frac{1}{ab} \tag{3.32}$$

$$B_2\left(i_p, i_s, a, b_c, L_{kp}, L_m\right) = \frac{2\left(i_p+i_s\right)}{\frac{36}{L_{kp}+2L_m} + \frac{8\left(L_m-4L_{kp}\right)}{L_{kp}\left(L_{kp}+2L_m\right)}}\frac{1}{ab_c} \tag{3.33}$$

$$B_3\left(i_p, i_s, a, b, L_{kp}, L_m\right) = \frac{2\left[\frac{36}{L_{kp}+2L_m} + \frac{3\left(4L_m-16L_{kp}\right)}{L_{kp}\left(L_{kp}+2L_m\right)}i_p - \frac{72}{L_{kp}+2L_m}i_s - \frac{3\left(4L_m-16L_{kp}\right)}{L_{kp}\left(L_{kp}+2L_m\right)}i_s\right]}{\frac{36}{L_{kp}+2L_m}\left[\frac{36}{L_{kp}+2L_m} + \frac{8\left(L_m-4L_{kp}\right)}{L_{kp}\left(L_{kp}+2L_m\right)}\right]}\frac{1}{ab} \tag{3.34}$$

With the given working condition, i_p and i_s is considered as known variables. Therefore, the core loss density can be calculated using Steinmetz Equation [22],

$$P_{v1}(a, b, L_{kp}, L_m) = k f_s^{\alpha} B_{m1}(a, b, L_{kp}, L_m)^{\beta} (Ct_2 T^2 - Ct_1 T + Ct) \quad (3.35)$$

$$P_{v2}(a, b_c, L_{kp}, L_m) = k f_s^{\alpha} B_{m2}(a, b, L_{kp}, L_m)^{\beta} (Ct_2 T^2 - Ct_1 T + Ct) \quad (3.36)$$

$$P_{v3}(a, b, L_{kp}, L_m) = k f_s^{\alpha} B_{m3}(a, b, L_{kp}, L_m)^{\beta} (Ct_2 T^2 - Ct_1 T + Ct) \quad (3.37)$$

Where B_{mk} (k = 1, 2, 3) is the maximum flux density in each post; f_s is the switching frequency; T is the working temperature. k, α, β, Ct_2, Ct_1 *and* Ct are constant with certain material.

With core loss density, we can calculate the transformer core loss,

$$P_{core}(a, b, b_c, c, L_{kp}, L_m) = P_{v1} Vol_1 + P_{v2} Vol_2 + P_{v1} Vol_2 \quad (3.38)$$

The expression of Vol_1, Vol_2, and Vol_3 are shown below,

$$Vol_1(a, b, c) = Vol_3(a, b, c) = abh_{leg} + 2ab\left(2d + b + c + \frac{b_c}{2}\right) \quad (3.39)$$

$$Vol_2(a, b_c, c) = ab_c h_{leg} \quad (3.40)$$

Here, in order to simplify the problem, it is assumed that flux is evenly distributed within the core.

According to Eq. (3.38), core loss is related to the transformer dimension parameters, a, b, b_c and c as well as the leakage inductance and magnetizing inductance, L_{kp} and L_m.

With both winding loss and core loss, the total transformer loss can be calculated as,

$$P_{tr}(a, b, b_c, c, L_{kp}, L_m) = P_{winding}(a, b, b_c, c) + P_{core}(a, b, b_c, c, L_{kp}, L_m) \quad (3.41)$$

And the transformer footprint is,

$$Tr_{ft}(a, b, b_c, c) = (a + 2c + 2d)(2b + 4c + 6d + b_c) \quad (3.42)$$

For a usual transformer design, core loss density and footprint should be design parameters. Therefore, we can changing the depending parameters by substitute Eq.(3.35), Eq.(3.36) and Eq.(3.42) into Eq.(3.41),

$$P_{tr} = P_{tr}(a, b, b_c, c, L_{kp}, L_m) = P_{tr}(a, Tr_{ft}, P_{v1}, P_{v2}, L_{kp}, L_m) \quad (3.43)$$

Where P_{v1} and P_{v2} are the core loss density of outer post and center post respectively.

By changing the depending parameters, the total transformer loss is related to a, Tr_{ft}, which are transformer dimensions, and P_{v1}, P_{v2}, L_{kp}, L_m, which are design parameters. Here, Tr_{ft} is the transformer footprint; P_{v1} and P_{v2} are core loss density of outer post and center post respectively.

From this equation, we can find out that for a transformer design, there are six parameters that need to be determined, which all have impact on the transformer loss and volume.

3.5 Optimization based on the 6.6 kW CLLC converter

Based on the previous proposed two-stage 6.6 kW on-board charger architecture, a split core transformer structure is adopted, as shown in Fig. 3.23. For each core, the turn ratio is 6:6, and the primary side of the two transformers are connected in series so a total 12:6:6 turns ratio is achieved. By using the proposed integrated transformer structure, the leakage inductance and magnetizing inductance can both be controlled.

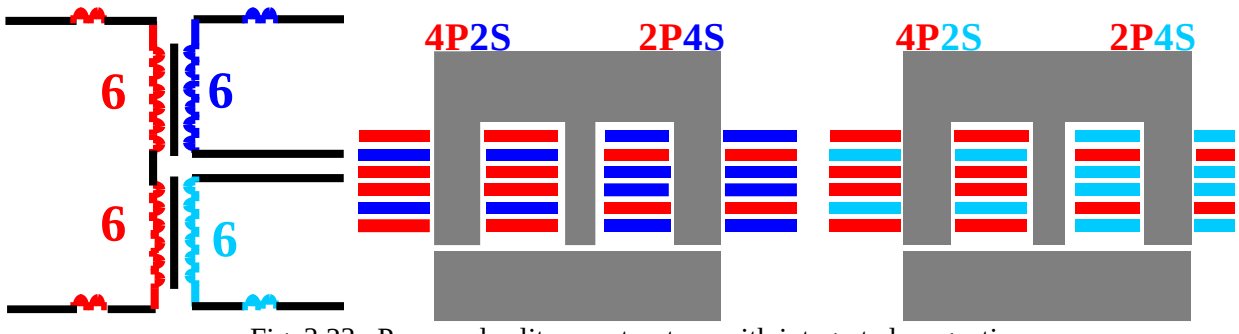


Fig. 3.23. Proposed split core structure with integrated magnetics.

Fig. 3.24 shows the core loss density comparison between several core material candidates, which are suitable for high frequency operation. 3F36 from Ferroxcube is selected due to its lowest core loss density at 500 kHz frequency.

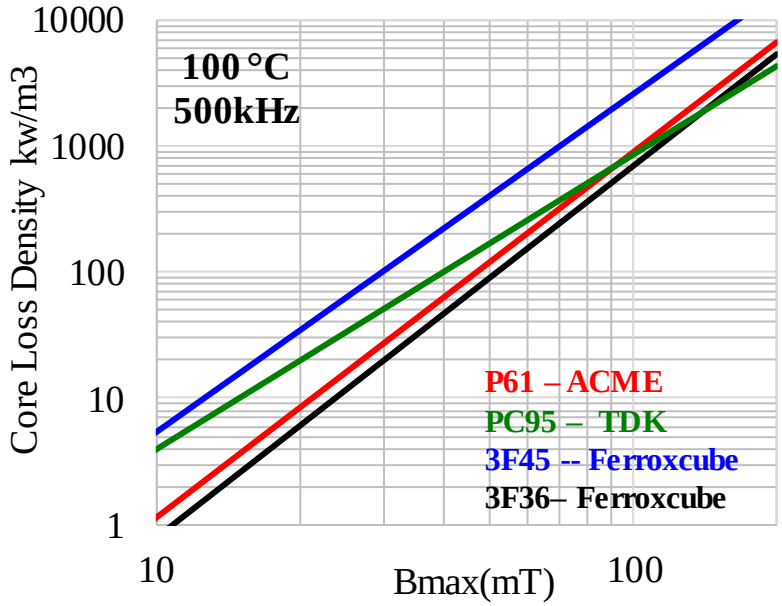


Fig. 3.24. Core loss density comparison between different materials.

For 3F36, their values are show in Table 3.1 [23].

Table 3.1. Core loss density related constant for 3F36

Parameter	Value	Parameter	Value
α	2.7199	Ct_2	8.926e-5
β	2.1952	Ct_1	1.172e-2
k	1.12e-7	Ct	1.282

With core loss density, we can calculate the transformer core loss according to Eq.(3.38)

Here, the total transformer loss is related to six parameters. a and Tr_{ft} are system dimension parameters. P_{v1}, P_{v2}, L_{kp} and L_m are system design parameters.

First, magnetizing inductance can be given according to the requirement of ZVS realization [24].

$$L_m \leq \frac{T_s t_{dead}}{8C_j} \tag{3.44}$$

Where t_{dead} is the dead time to achieve ZVS; C_j is the total equivalent junction capacitance; T_s is the switching period.

It should be noted that C_j consists of primary and secondary side devices' junction capacitors and PCB winding parasitic capacitor,

$$C_j = C_{oss\_pri} + C_{oss\_sec} + C_{pcb} \tag{3.45}$$

For 500 kHz operation, we can select t_{dead} = 100 ns, which is around 5% of the total switching period. Then L_m value is determined, to be 36 μH.

If we give 500 kW/m^3 core loss density for center post, 300 kW/m^3 core loss density for outer post, and 5000 mm^2 as transformer footprint, we can draw the 3D optimization figure with a and L_n as parameters and the results are shown in Fig. 3.26.

In this figure, L_n is an important parameter that represents the regulation capability of the resonant converter,

$$L_n = \frac{L_m}{L_k} \tag{3.46}$$

From this figure, it can be seen that larger L_n (smaller leakage inductance) results in smaller transformer loss. However, larger L_n also means the regulation capability of the resonant converter is weaker, therefore the switching frequency range for the required gain is larger. Considering 10% ripple on DC-link, then the switching frequency range for different L_n is shown in Fig. 3.25. Larger frequency range means larger loss. The device loss can be calculated through Eq. (3.47). The relationship between L_n and device related loss are shown in Fig. 3.26 (a).

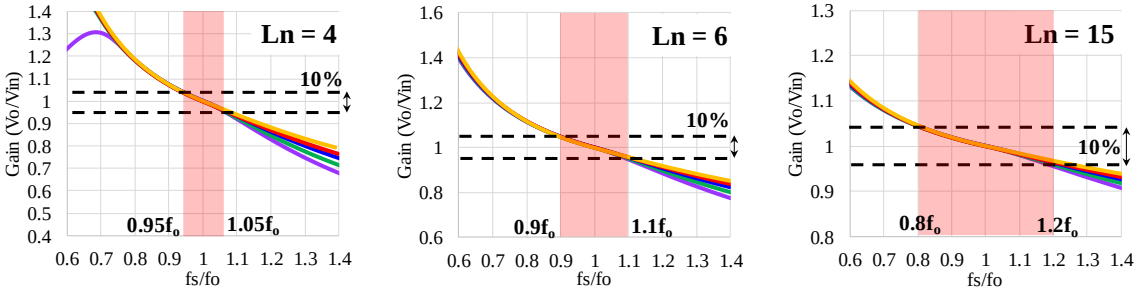
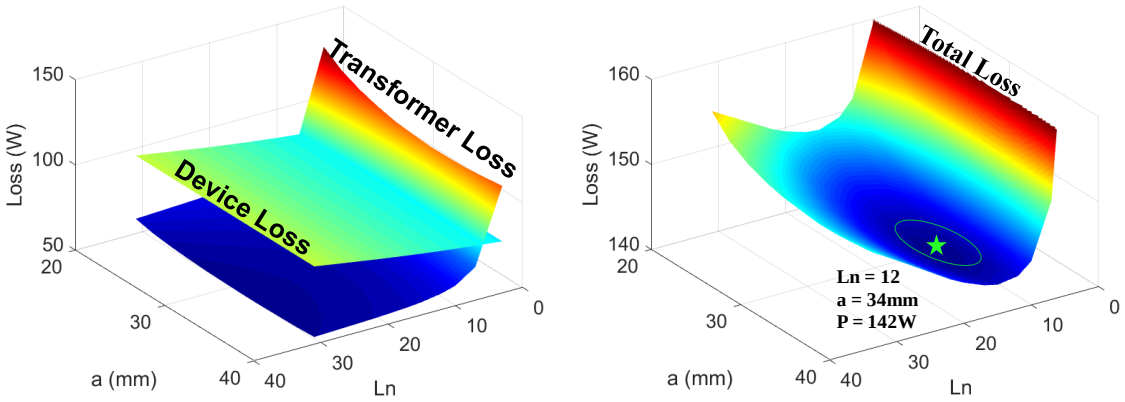


Fig. 3.25. Switching frequency range with different L_n.

$$P_{device}(L_m, L_k) = I_{pri}^2 R_{on-pri} + I_{sec}^2 R_{on-sec} + P_{sw} + P_{dr} \quad (3.47)$$

By combining device loss and transformer loss together, we can have the total system loss, as shown in Fig. 3.26 (b).



(a) (b)

Fig. 3.26. 3D Optimization results for (a) transformer loss and device loss and (b) total loss.

From Fig. 3.26 (b), we can find the lowest loss point, which is around 142 W. At this time, the ratio between magnetizing and leakage inductance is around 12.

By repeating the same optimization steps with different footprint and core loss density, we can have the loss surface, as shown in Fig. 3.27.

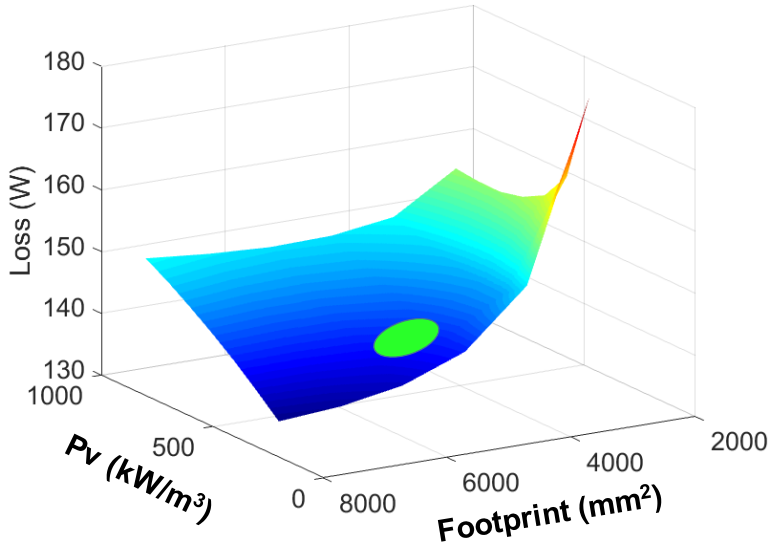


Fig. 3.27. Total loss according to different core loss density and footprint.

From this figure, we can see that the total loss is reducing with the increasing of transformer footprint. However, after certain point, the reduction becomes very limited. Therefore, the final selection is based on the best tradeoff between total loss and transformer footprint.

$$footprint = 5000 \text{ mm}^2,\ P_v = 300 \text{ kW/m}^3,\ Loss = \ 142 \text{ W}$$

In comparison, litz-wire based transformer and inductors (discrete magnetics) are designed. The results are shown in Table 3.2. The primary side inductor uses ER core with 80 mm^2 cross section area and secondary side inductors use ER core with 50 mm^2 cross section area. The transformer is also ER core based with 325 mm^2 cross section area. AWG48/2000 litz-wires are used for both inductors and transformer.

From the comparison, we can see that with similar volume, the proposed integrated PCB winding transformer has about 8% larger loss compared with litz-wire based magnetics. However, with PCB magnetics, we also gain the benefits of manufacture automation and good parasitic control, both of which are impossible for litz-wire magnetics.

Table 3.2. Comparison between the proposed integrated PCB magnetic and litz-wire magnetics

	Proposed PCB magnetic	Litz-wire magnetics

L_m	18 uH	18 uH
L_{kp}	1.5 uH (integrated)	1.5 uH
L_{ks}	1.5 uH (integrated)	1.5 uH
Inductor Winding Loss	-	4.1 W
Inductor Core Loss	-	4.3 W
Transformer Winding Loss	35.4 W	28.7 W
Transformer Core Loss	24.1 W	18 W
Total Loss	59.5 W	55.1 W
Volume	135,000 mm^3	140,000 mm^3

In addition, compared with the PCB winding matrix transformer structure, the proposed integrated magnetic has around 15% - 17% loss increase due to the non-perfect interleave winding structure and additional leakage flux inside the core. However, additional inductor loss is saved.

3.6 Experimental verification

Hardware prototype (as shown in Fig. 3.28) based on the proposed split core transformer with controllable leakage inductance using 6-layer 3 Oz PCB is built to verify previous analysis.

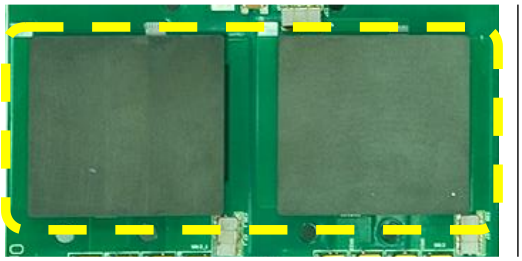


Fig. 3.28. Hardware prototype based on the proposed transformer structure.

Different methods are used to test the magnetizing inductance and leakage inductance of the transformer. Also, since the two transformers are the same, only one is tested.

(1) Secondary side is open

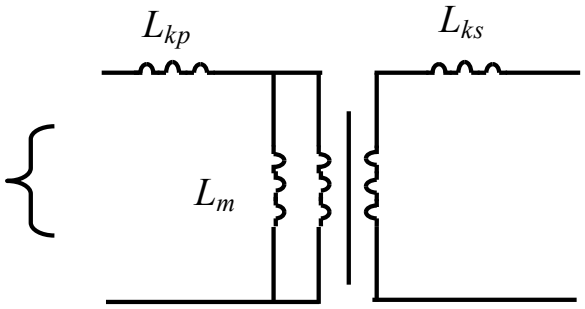


Fig. 3.29. Testing method one with secondary side open.

Using this method, the tested inductance on primary side terminal is the primary side self-inductance, which is also the sum of primary side leakage inductance and magnetizing inductance.

$$L_1 = L_p = L_{kp} + L_m \tag{3.48}$$

(2) Secondary side is short

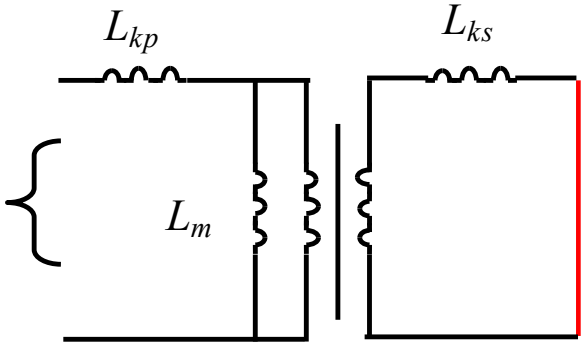


Fig. 3.30. Testing method two with secondary side short.

Using this method, the tested inductance on primary side terminal is the sum of primary side leakage inductance and magnetizing inductance in parallel with secondary side leakage inductance.

$$L_2 = L_{kp} + L_m // L_{ks} \tag{3.49}$$

(3) Primary side and secondary side is in series.

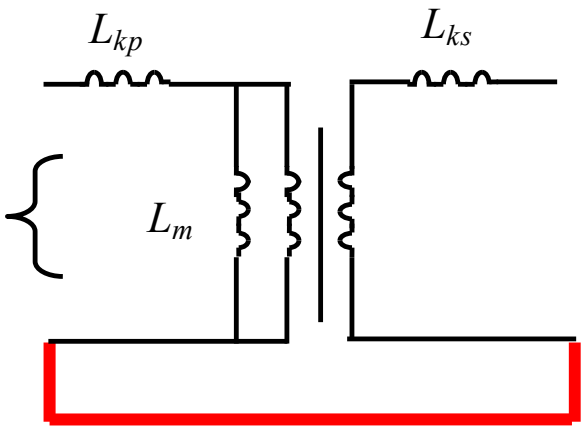


Fig. 3.31. Testing method three with primary side and secondary side in series.

Since the primary side and secondary side are the same, the magnetizing flux is fully cancelled using this method. Therefore, the tested inductance on primary side terminal is the sum of primary side leakage inductance and secondary side leakage inductance.

$$L_3 = L_{kp} + L_{ks} \tag{3.50}$$

The tested results are shown in Table 3.3.

Table 3.3. Testing results of the proposed transformer

	Testing Results
L_1	19.5 uH
L_2	2.9 uH
L_3	2.95 uH

With some calculation, we can get the tested magnetizing inductance and leakage inductance, as shown in Table 3.4.

Table 3.4. Testing results of the proposed transformer

	Calculation Results	Testing Results
L_m	18 uH	18 uH
L_k	1.2 uH	1.49 uH
L_n	15	12.1

The leakage inductance is larger than the calculation result because the leakage in the air and the termination effect are not included in the calculation. Other than that, the testing results show a very good match with the calculation results.

3.7 Switching frequency impact

Previously, 500 kHz switching frequency is arbitrarily selected as the working frequency of the CLLC converter. However, different switching frequency needs to be evaluated to get the optimized working condition for the transformer.

Based on the same optimization procedure, we can get the lowest transformer loss under different footprint and different switching frequency with L_n = 12, as shown in Fig. 3.32.

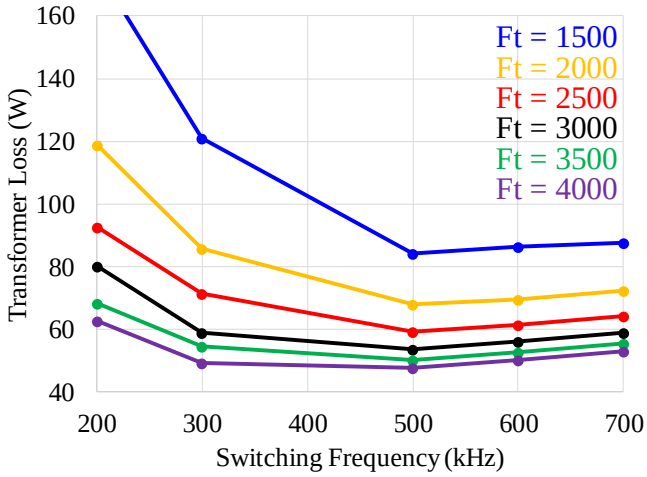


Fig. 3.32. Total transformer loss at different footprint and different frequency with L_n = 12.

It is clear that with smaller footprint, high switching frequency is preferred due to the reduced cross section area. When footprint is increasing, the optimal switching frequency also moves to lower value.

However, for the total system loss, device related loss needs to be considered. The device related loss according to different switching frequency when L_n = 12 is shown in Fig. 3.33.

If we add the transformer loss and device related loss together, we can get the total system loss, as shown in Fig. 3.34.

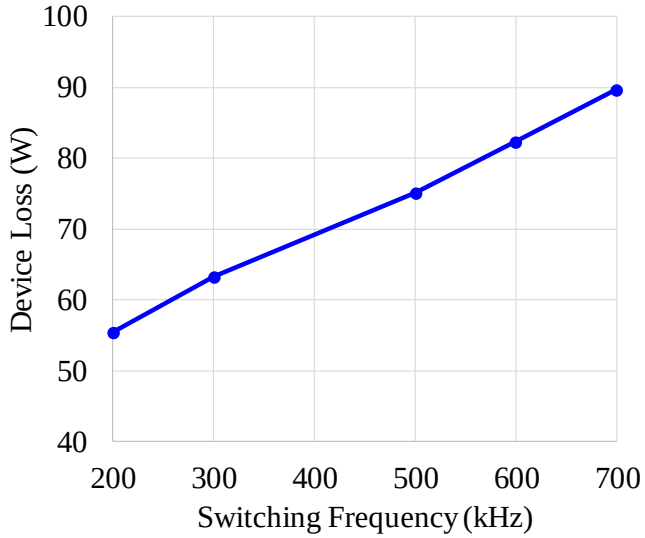


Fig. 3.33. Device related loss according to different switching frequency.

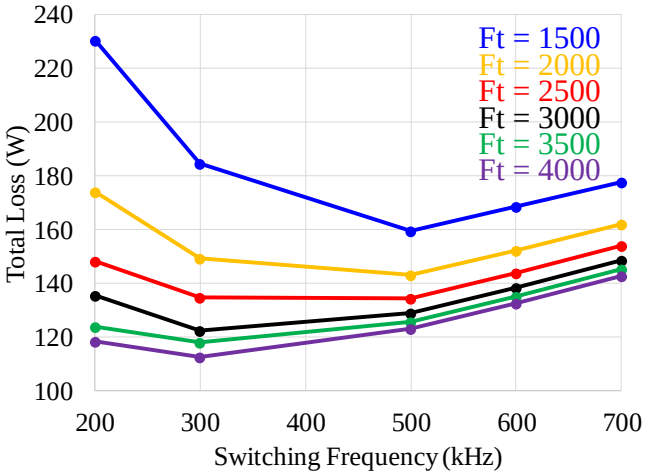


Fig. 3.34. Total system loss at different footprint and different frequency with L_n = 12.

From Fig. 3.34, we can see that at with 2500 mm^2 footprint, 300 kHz – 500 kHz switching frequency has almost the same loss due to the tradeoff between device loss and transformer loss. With footprint larger than 2500 mm^2, lower switching frequency has better efficiency and with footprint smaller than 2500 mm^2, higher switching frequency will be a better choice.

The tradeoff between transformer footprint and the total system loss can be seen in Fig. 3.35. It is clear that with high switching frequency, the transformer footprint can be reduced but in the meantime, the total loss is increased. The best tradeoff zone is in the range of 400kHz – 500 kHz.

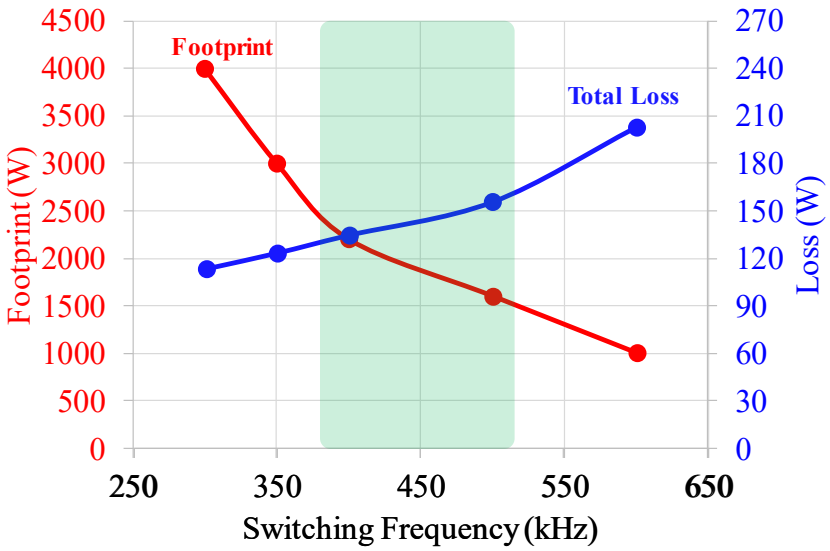


Fig. 3.35. Tradeoff between footprint (red solid line) and total system loss (blue dotted line) with different switching frequency.

3.8 Hardware testing results

A 6.6 kW on-board charger prototype is built, as shown in Fig. 3.36. Totem-pole AC/DC working at critical conduction mode is adopted to realize soft switching for all the fast switches. Two phases are interleaved together to reduce the total input current ripple, and the minimum switching frequency for each phase is 300 kHz. For the second stage, a CLLC resonant converter working at 500 kHz is used. A PCB winding based integrated transformer is designed and used to reduce the total footprint of the magnetics and help simplify the manufacture process. 1.2 kV SiC devices from GE is used as the fast switches for AC/DC stage and primary side switch of the DC/DC stage while 650 V GaN devices from GaN Systems are selected as the secondary side devices for the DC/DC stage.

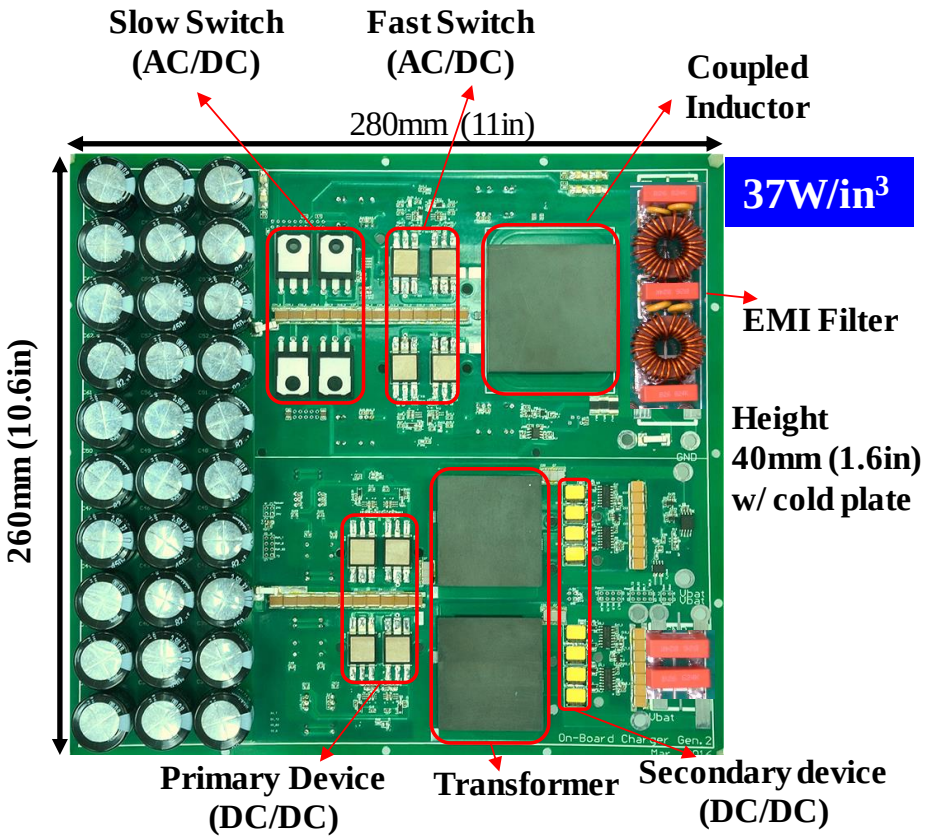
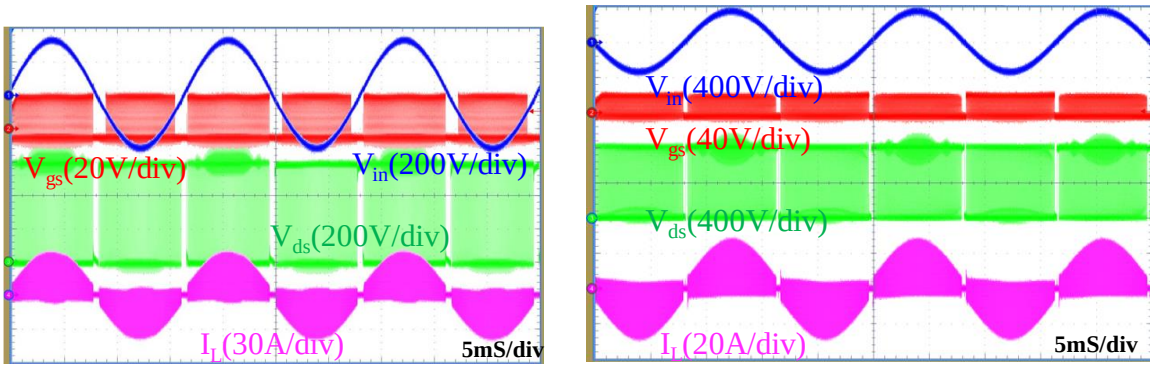


Fig. 3.36. Prototype of the 6.6 kW on-board charger.

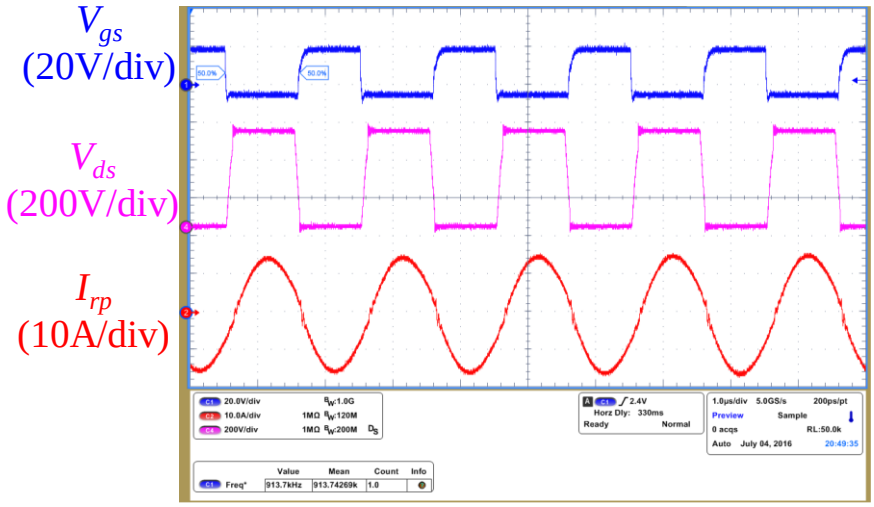
The testing waveforms of the AC/DC stage for charging and discharging modes with 400 V battery voltage and full load are shown in Fig. 3.37, where V_{in} is the input AC voltage; V_{gs} and V_{ds} are the gate source and drain source voltages of the SiC device; and I_L is the one phase inductor current. 0.99 power factor and 2.3% total harmonic distortion (THD) is achieved.



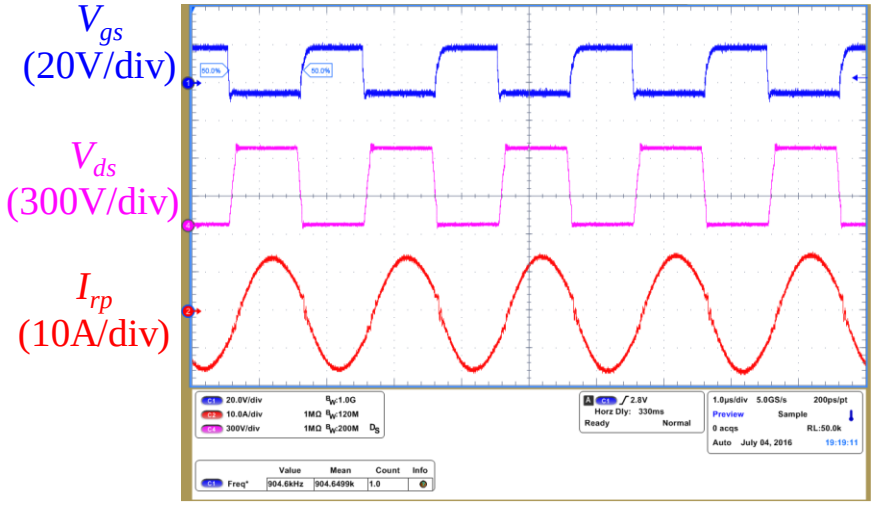
(a) Charging mode (b) Discharging mode

Fig. 3.37. Working waveforms of AC/DC stage with 400 V battery voltage and full load.

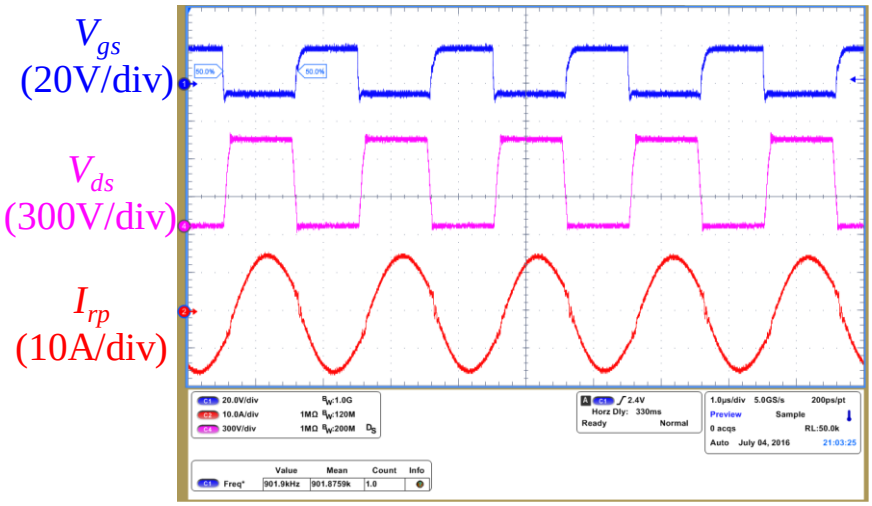
The charging and discharging waveforms of the DC/DC stage are shown in Fig. 3.38 (a) – (d) and Fig. 3.38 (e) – (h) respectively. In Fig. 3.38 (a) – (d), V_{gs} and V_{ds} are the gate source voltage and drain source voltage of primary device (SiC device) respectively, and I_{rp} is the primary-side resonant current. In Fig. 3.38 (e) – (h), V_{gs} and V_{ds} are the gate source voltage and the drain source voltage of the secondary device (GaN device, which is now the active device in the discharging mode), and I_{rs} is the secondary-side resonant current.



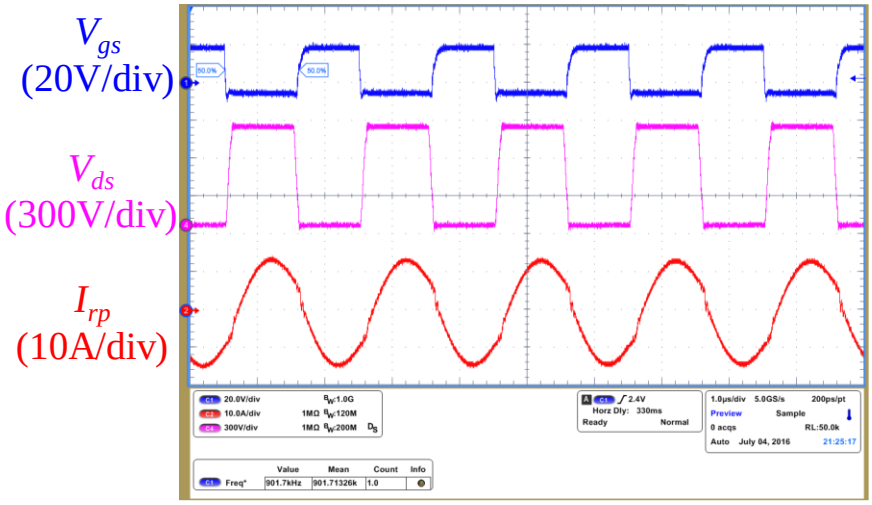
(a) charging mode @ 250 V battery voltage



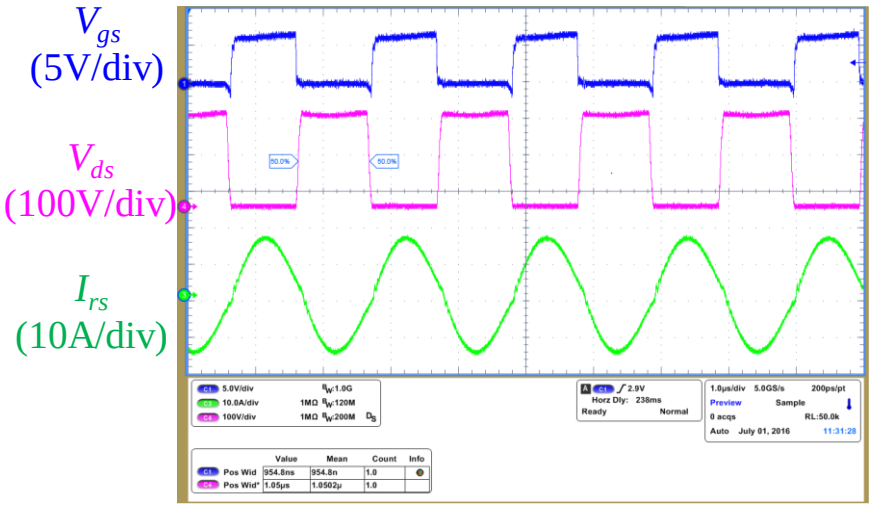
(b) charging mode @ 300 V battery voltage.



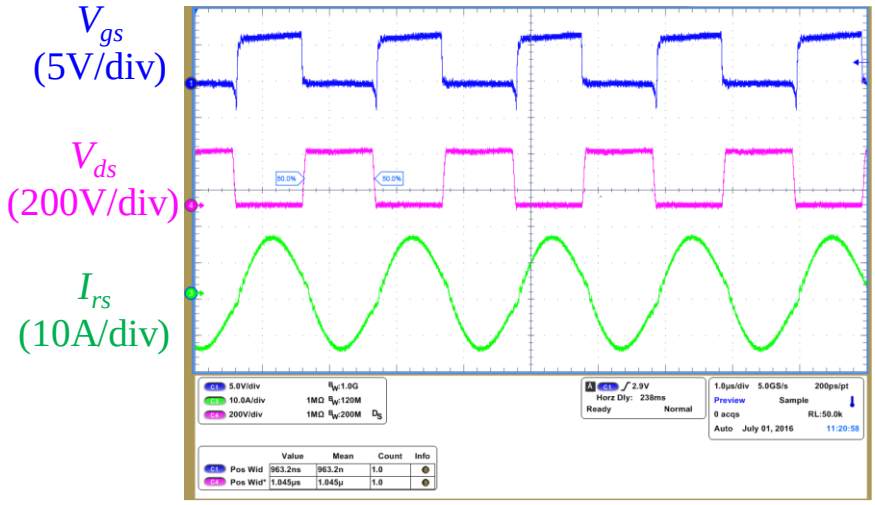
(c) charging mode @ 350 V battery voltage.



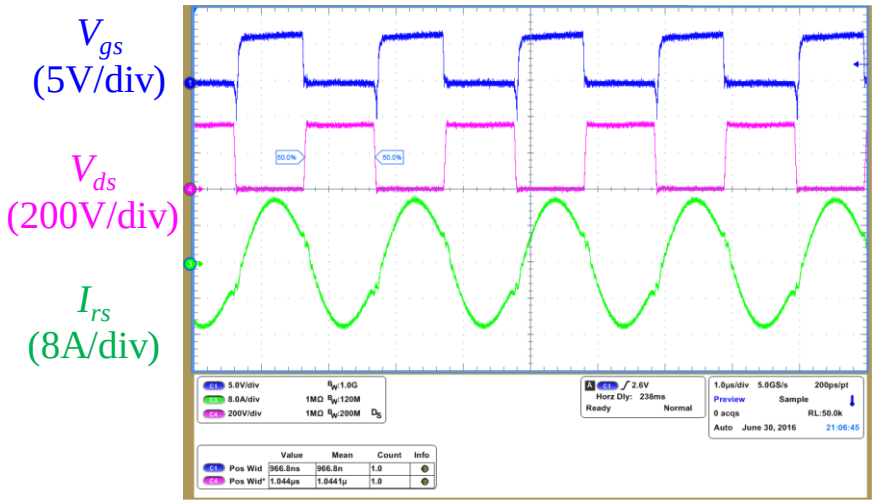
(d) charging mode @ 400 V battery voltage.



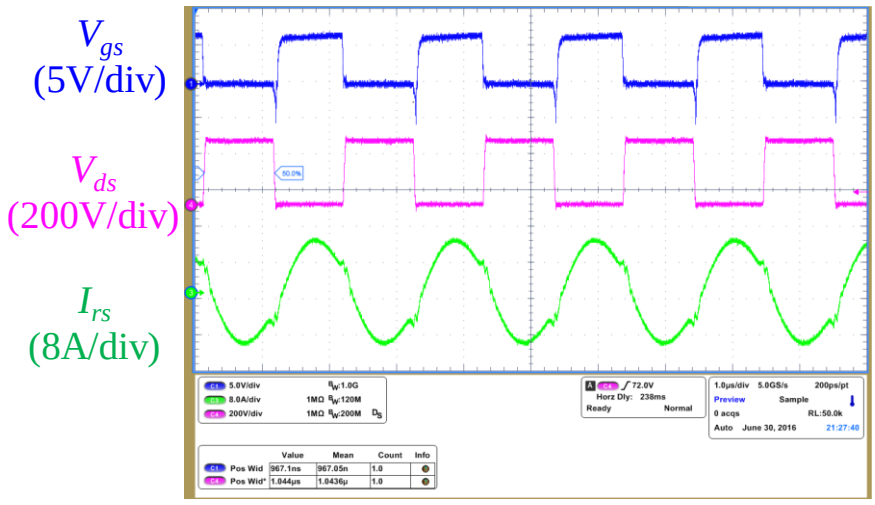
(e) discharging mode @ 250 V battery voltage.



(f) discharging mode @ 300 V battery voltage.



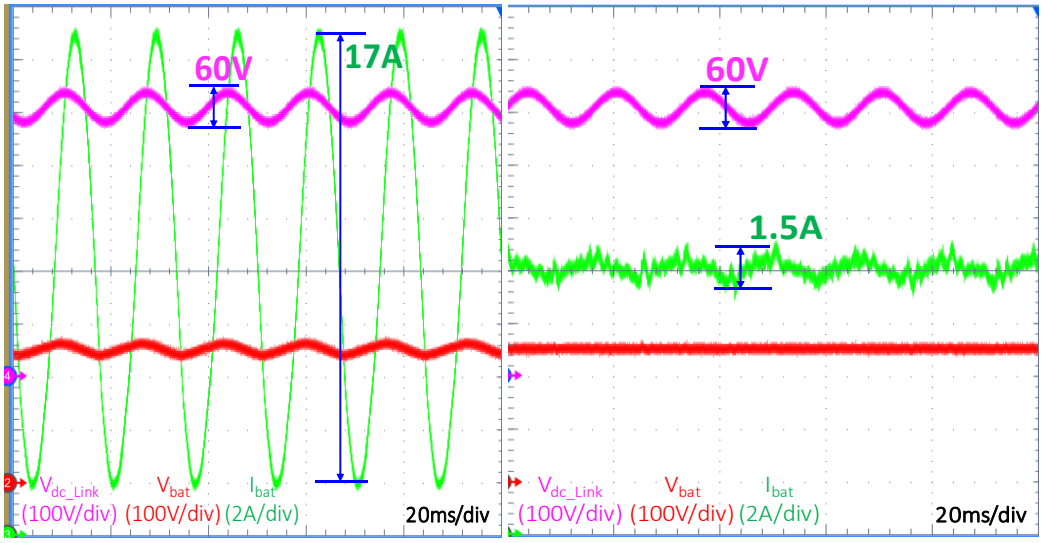
(g) discharging mode @ 350 V battery voltage.



(h) discharging mode @ 400 V battery voltage.

Fig. 3.38. Working waveforms of DC/DC stage with different battery voltage and full load.

Closed-loop operation is also verified with the prototype, and the results are shown in Fig. 3.39. The worst case for the DC-link voltage ripple is 250 V battery voltage. Under this condition, the peak-to-peak ripple is around 60 V. An electronic load under constant voltage mode is used to simulate the battery. With a 60 V DC-link voltage ripple, the output current ripple is over 17 A for DCX (fixed switching frequency) operation, and it can be suppressed to 1.5 A if the DC/DC stage current-loop control is introduced. Instead of a fixed switching frequency, the switching frequency varies between 400 kHz to 600 kHz.



(a) (b)

Fig. 3.39. (a) Open-loop (DCX) and (b) closed-loop operation results.

The tested efficiency of the charging mode is shown in Fig. 3.40. With 240 V AC input, the two-stage total efficiency is over 96% for the entire battery voltage range, which verifies our evaluation and demonstrates the superior performance of the proposed two-stage structure. It should be noted that the testing is based on litz-wire inductor. The coupled inductor version is still under testing. Compared with the state-of-the-art Si-based low-frequency design, 2% peak efficiency improvement is achieved, and more improvement can be observed under low and high battery voltages. As a result, during an entire charging cycle, 50% loss can be saved by using the proposed high efficiency charger.

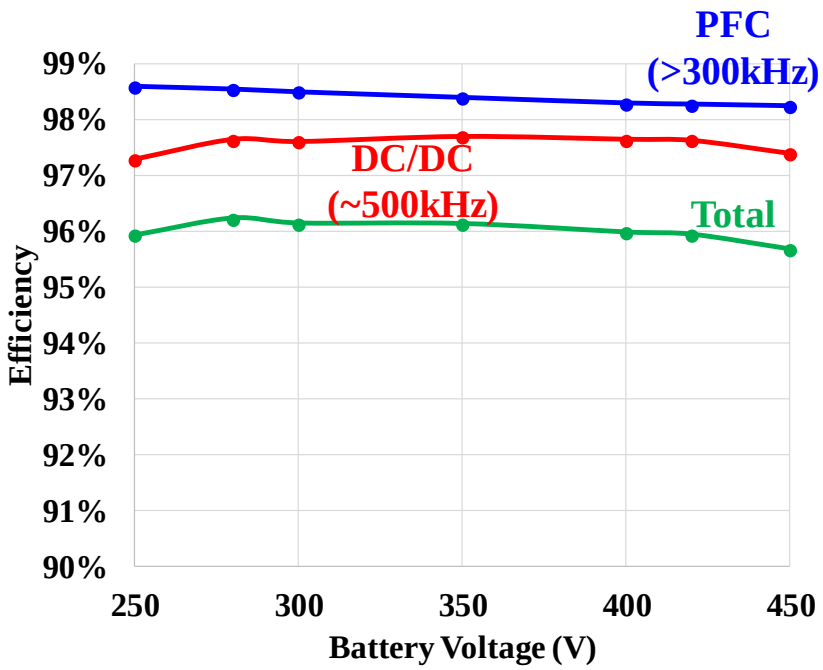
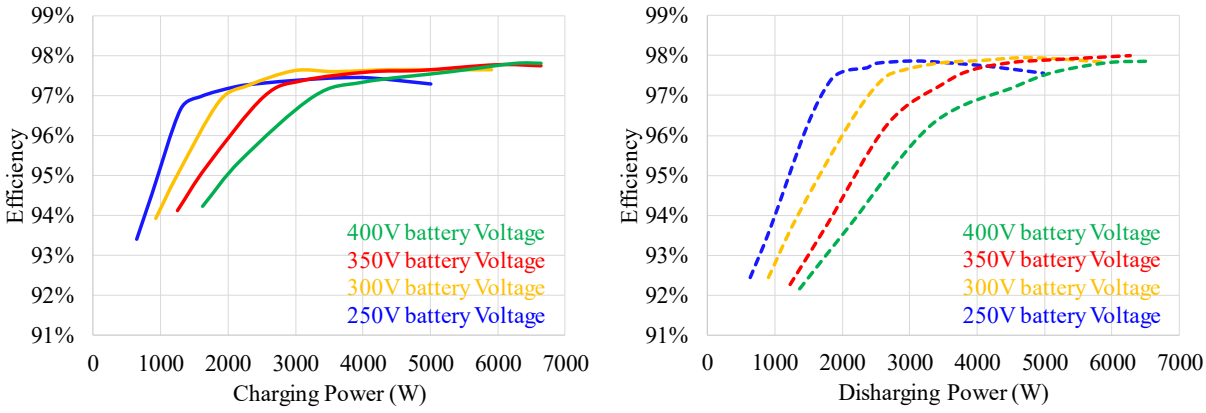


Fig. 3.40. Efficiency curves with different battery voltages under full load during charging mode.

Also, due to the symmetrical structure of both AC/DC stage and DC/DC stage, the discharging mode efficiency is very close to charging mode, as shown in Fig. 3.41.



(a) Charging mode (b) Discharging mode

Fig. 3.41. Two-stage efficiency with different load condition for (a) charging mode and (b) discharging mode.

The detailed loss breakdown at 350 V battery voltage and full load is shown in Fig. 3.42. The red bars show AC/DC stage loss and the blue bars show DC/DC stage loss.

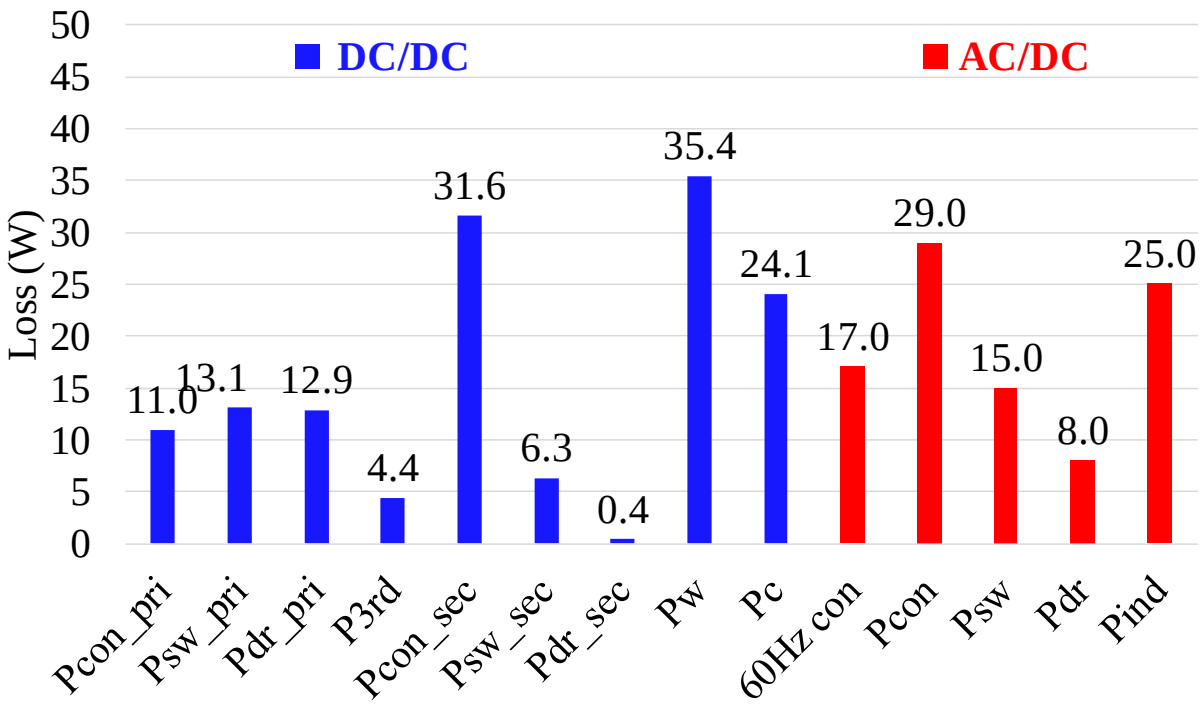


Fig. 3.42. System loss breakdown at 350 V battery voltage and 6.6 kW full power in charging mode.

Due to the limitation of available SiC device, the selected device is not the best choice because of the very small conduction loss but relatively large switching loss (turn off loss and driving loss). Further optimization can be done if more suitable devices are available.

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Chapter 4 A Symmetrical Transformer and Resonant Converter Structure to Reduce Common Mode Noise

The newly emerged wide bandgap (WBG) devices, including both silicon carbide (SiC) and gallium nitride (GaN), provide much better figure of merit compared with silicon (Si) devices [1]. With given on resistance and breakdown voltage, the required die size for WBG device is greatly reduced, providing much smaller gate charge and junction capacitor. This helps the device to achieve faster turn on/off, shorten the current/voltage transition interval and significantly reduce the switching loss. However, the fast turn on/off also brings high *dv*/*dt* at the switch node, causing severe common mode (CM) noise issue. Compared with PWM converter, resonant converter has the ability to achieve zero voltage switching (ZVS) for all the switches, and it is widely used in applications like server power supply [2-4], telecom power supply [5] and on-board charger for electric vehicles [6, 7]. ZVS can totally eliminate the large turn on loss and greatly improve the system efficiency [8-10], especially under high switching frequency (hundreds of kHz or even MHz). It also helps to slow down the fast *dv*/*dt* at turn on instant. However, the turn off *dv*/*dt* may get worse due to the larger turn off current.

One benefit brought by high frequency operation is the possibility to utilize PCB as transformer windings. PCB winding transformer features simple manufacture and very good parasitic control, and with further magnetic integration, the inductors in circuit like dual active bridge, LLC and CLLC can be integrated into the transformer utilize the its leakage inductance, shrinking the size and weight of the whole converter [11, 12]. However, compared with conventional litz-wire based transformer, the inter-winding capacitor of PCB winding magnetics increases significantly due to the much larger overlapping area and shorter distance between windings [13-15]. In addition, to minimize AC winding loss, interleaving is necessary for PCB winding magnetics under high frequency operations [16, 17], which results in even larger capacitor between primary and secondary windings.

The large inter-winding capacitor of PCB winding transformer forms a low impedance path for CM current, and together with the high *dv*/*dt* brought by the WBG devices, the resulted CM noise is significant. Higher level of CM noise requires larger CM choke to meet with the standards and regulations and as a result, the whole system efficiency and power density is compromised.

In order to reduce the transformer related CM noise, several methods have been proposed. In [18], the transformer windings are purposely designed so that the overlapped area is reduced, resulting in smaller inter-winding capacitor. However, this method also sacrifices the interleaving between primary and secondary windings and leads to larger AC winding loss. Moreover, the copper utilization is not very good. In [19], a compensation capacitor is added to connect the primary side and secondary side of the transformer to reduce CM noise .However, the voltage rating requirement of the capacitor is very high and it is not suitable for high power high voltage application. In [20-24], shielding is implemented between primary and secondary windings so that no CM current can flow through. The performance is very good with 20-30 dB CM noise reduction but it requires additional copper layers. Especially in PCB winding transformer with interleaved structure, the needed number of PCB layers is almost doubled and the total system cost is significantly increased. In [25-27], balance technique is used to cancel the CM noise in the system. By adding additional compensation capacitor, the total system CM noise is reduced. However, this method requires very good calculation or measurement of the parasitic capacitor of the transformer so that very accurate compensation can be achieved. Otherwise, the cancellation effect is compromised. In [28, 29], another shielding technique is proposed. By putting primary and secondary winding with the same *dv/dt* together in pairs, the primary windings are serving as shielding layers. As a result, there is no CM current generated between primary windings and secondary windings. However, this method has limitations with more than one turn per layer. Also, it is not suitable for matrix transformers, where there are more than one set of secondary side windings. In [30], a similar method is proposed, which also utilize the *dv/dt* between primary and secondary winding to reduce CM current. However, this method is only based on litz-wire

transformer where there is no interleave requirement, and the implementation of this method is complex, involving more switching devices.

For power electronics converter, the switching of MOSFETs is the major source of voltage pulsating. Primary side switches introduce severe *dv/dt* at switching nodes, which can be modeled as voltage sources [22, 31]. The same concept can be applied to the secondary side diode (or synchronized rectifier). For isolated converter, there are mainly two CM noise paths, as shown in Fig. 4.1. One is through parasitic capacitors between primary side devices (and their heatsinks) and ground (shown in blue dash line), and the other one is through transformer inter-winding capacitor (red solid line).

For full bridge configuration, the two CM noise sources on primary side have the same magnitude but are out-of-phase ($dV_{pA}/dt = -dV_{pB}/dt$). If the associated parasitic capacitors are the same ($C_{pa} = C_{pb}$), which is usually true with identical PCB layout and heatsink design, the CM current through this path cancels each other. However, for CM noise past through the inter-winding capacitor of the transformer, the cancellation effect depends on the symmetry of the circuit and transformer. In fact, with PCB winding transformer, this part is the major source of the system CM noise.

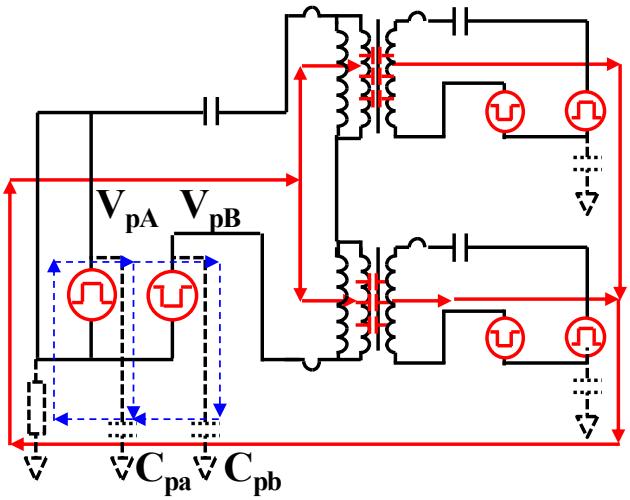


Fig. 4.1. CM noise path of CLLC resonant converter.

4.1 Analysis of CM current through inter-winding capacitor

In order to analyze the CM current through inter-winding capacitor for CLLC resonant converter, voltage potential for each transformer winding should be presented.

Fig. 4.2 shows the transformer terminal voltage potential of CLLC resonant converter when switching frequency equals to resonant frequency. V_{pp} and V_{pn} are positive and negative terminal voltage of primary side referenced to primary side ground; V_{sp} and V_{sn} are positive and negative terminal voltage of secondary side referenced to secondary side ground. Since ideally the two sets of output are the same, only one set is analyzed.

For positive terminal voltage of primary side, it is connected to switch node *pA* through primary side resonant capacitor. Therefore, its voltage potential is,

$$V_{pp} = V_{pA} - V_{rp} \tag{4.1}$$

Where V_{pA} is the voltage potential at switch node *pA* referenced to primary side ground. V_{rp} is the voltage across primary side resonant capacitor.

For negative terminal voltage of primary side, since it is directly connected to switch node *pB*. its voltage potential is,

$$V_{pn} = V_{pB} \tag{4.2}$$

Where V_{pB} is the voltage potential at switch node *pB* referenced to primary side ground.

Similarly, the terminal voltage of secondary side winding can also be calculated,

$$V_{sp} = V_{sA} + V_{rs} \tag{4.3}$$

$$V_{sn} = V_{sB} \tag{4.4}$$

Where V_{sA} and V_{sB} are voltage potential of switch node *sA* and *sB* referenced to secondary side ground. V_{rs} is the voltage across secondary side resonant capacitor.

According to the above equations, the voltage waveforms of transformer terminals are shown in Fig. 4.2.

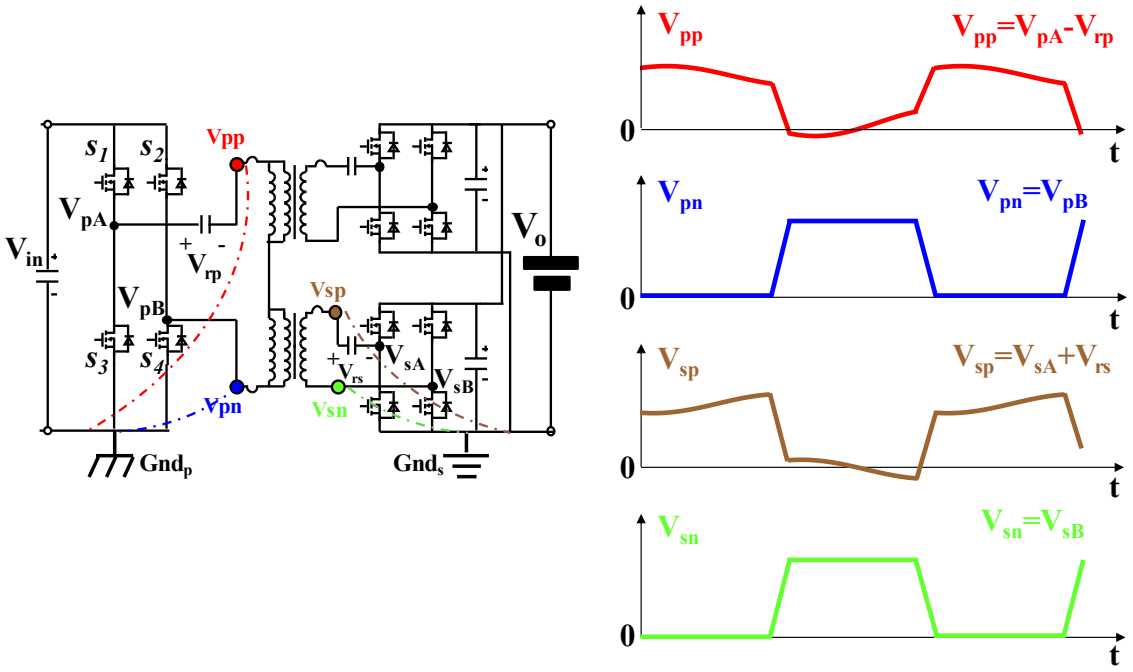


Fig. 4.2. Transformer terminal voltage waveform @ $f_s = f_o$.

Since the CM current is only related to *dv*/*dt*, the voltage-changing rate on each terminal can be calculated as,

$$\frac{dv_{pp}}{dt} = \frac{dv_{pA}}{dt} - \frac{dv_{rp}}{dt}$$

$$\frac{dv_{pn}}{dt} = \frac{dv_{pB}}{dt}$$

$$\frac{dv_{sp}}{dt} = \frac{dv_{sA}}{dt} + \frac{dv_{rs}}{dt}$$

$$\frac{dv_{sn}}{dt} = \frac{dv_{sB}}{dt} \tag{4.5}$$

Here, with full bridge operation, the gate signals of S_1 and S_4 are the same and the gate signals of S_2 and S_3 are the same. Therefore, we have,

$$\frac{dv_{pA}}{dt} = -\frac{dv_{pB}}{dt}$$

$$\frac{dv_{sA}}{dt} = -\frac{dv_{sB}}{dt} \tag{4.6}$$

If we analyze the voltage-changing rate on the four transformer terminals, we can see that they can be separated into two parts, as shown in Fig. 4.3.

For the first part,

$$\frac{dv_{pp1}}{dt} = \frac{dv_{pA}}{dt}$$

$$\frac{dv_{pn1}}{dt} = \frac{dv_{pB}}{dt}$$

$$\frac{dv_{sp1}}{dt} = \frac{dv_{sA}}{dt}$$

$$\frac{dv_{sn1}}{dt} = \frac{dv_{sB}}{dt} \tag{4.7}$$

And the second part is,

$$\frac{dv_{pp2}}{dt} = -\frac{dv_{rp}}{dt}$$

$$\frac{dv_{pn2}}{dt} = 0$$

$$\frac{dv_{sp2}}{dt} = \frac{dv_{rs}}{dt}$$

$$\frac{dv_{sn2}}{dt} = 0 \tag{4.8}$$

It is clear that for the first part we have,

$$\frac{dv_{pp1}}{dt} = -\frac{dv_{pn1}}{dt}$$

$$\frac{dv_{sp1}}{dt} = -\frac{dv_{sn1}}{dt} \tag{4.9}$$

We call it the complementary part since the voltage-changing rate for this part is complementary (same magnitude but reverse direction). However, for the second part, it does not have such feature, and we call it uncomplimentary part.

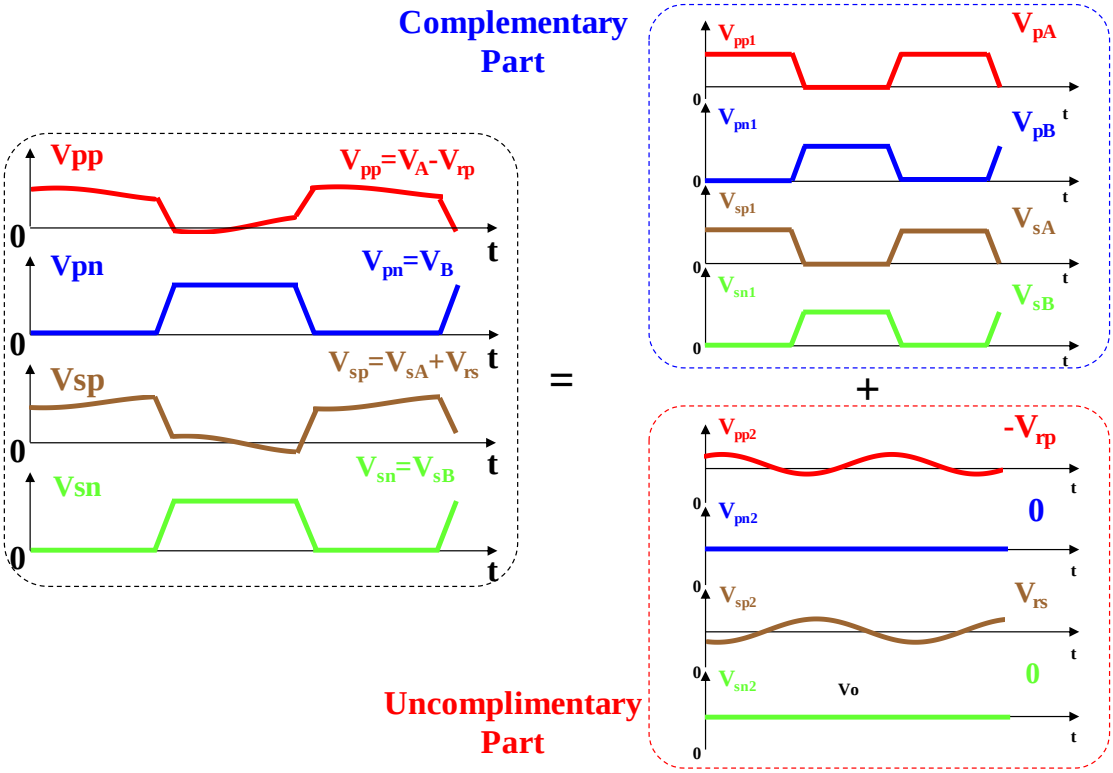


Fig. 4.3. Separation of transformer terminal voltage.

First, let us only consider the complementary part. Its distribution across the primary winding and secondary winding is shown in Fig. 4.4. Here, from top to bottom, the primary windings are numbered from P6 to P6' and the secondary windings are numbered from S3 to S3'. If we assume that *dv/dt* is evenly distributed across each winding, then the *dv/dt* across winding No. P*m* of primary side are $\frac{m}{6}\frac{dv_{pA}}{dt}$ and $\frac{m-1}{6}\frac{dv_{pA}}{dt}$. And the *dv/dt* across winding No. S*m* of secondary side are $\frac{m}{3}\frac{dv_{sA}}{dt}$ and $\frac{m-1}{3}\frac{dv_{sA}}{dt}$.

Similarly, the *dv*/*dt* across winding No. Pm' of primary side are $\frac{m'-1}{6}\frac{dv_{pB}}{dt} = -\frac{m'-1}{6}\frac{dv_{pA}}{dt}$ and $\frac{m'}{6}\frac{dv_{pB}}{dt} = -\frac{m'}{6}\frac{dv_{pA}}{dt}$, and the *dv*/*dt* across winding No. Sm' of secondary side are $\frac{m'-1}{3}\frac{dv_{sB}}{dt} = -\frac{m'-1}{3}\frac{dv_{sA}}{dt}$ and $\frac{m'}{3}\frac{dv_{sB}}{dt} = -\frac{m'}{3}\frac{dv_{sA}}{dt}$.

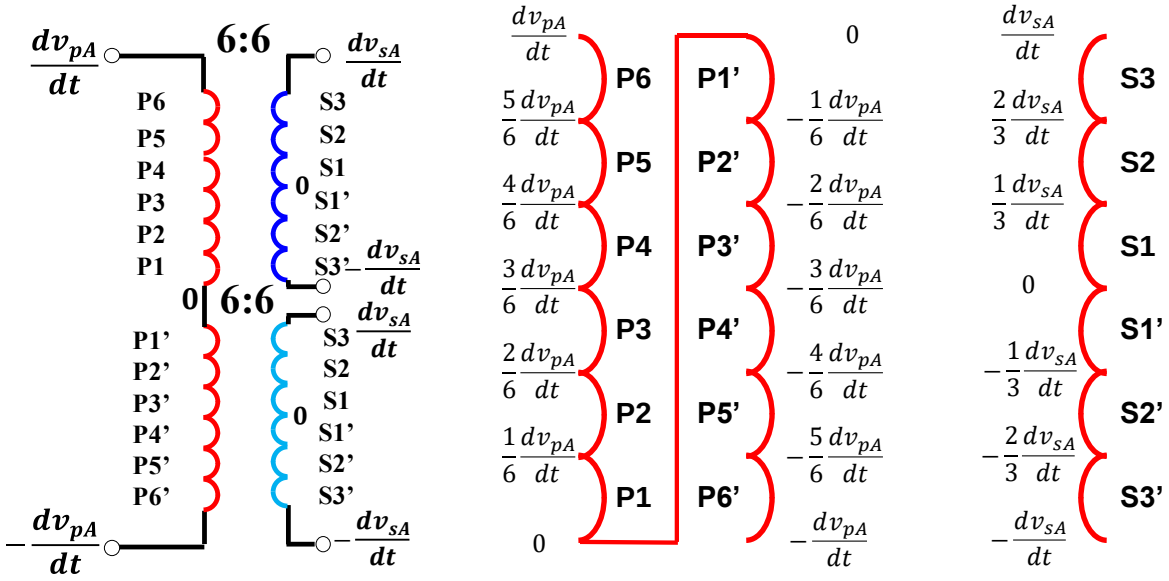
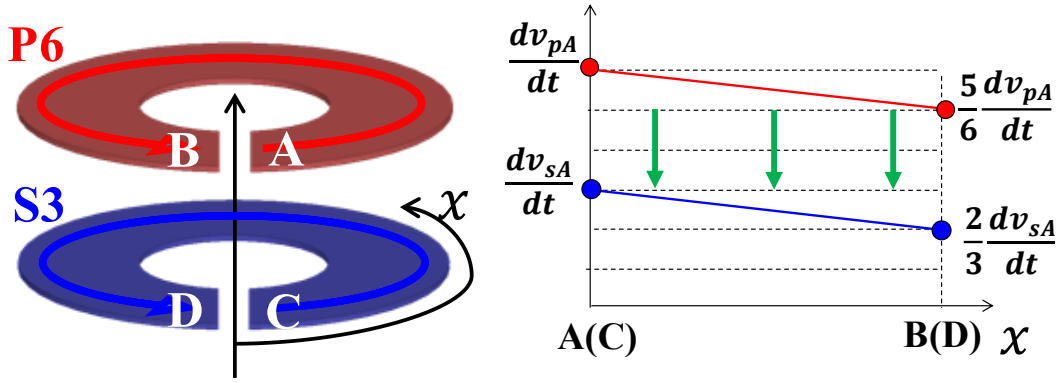


Fig. 4.4. Complementary part of *dv*/*dt* distribution across transformer windings.

If we take primary winding No. P6 and secondary winding No. S3 (in Transformer 1) as an example (assuming they are next to each other, as shown in Fig. 4.5 (a), the *dv*/*dt* distribution along the winding (from point A(C) to point B(D)) is shown in Fig. 4.5 (b).

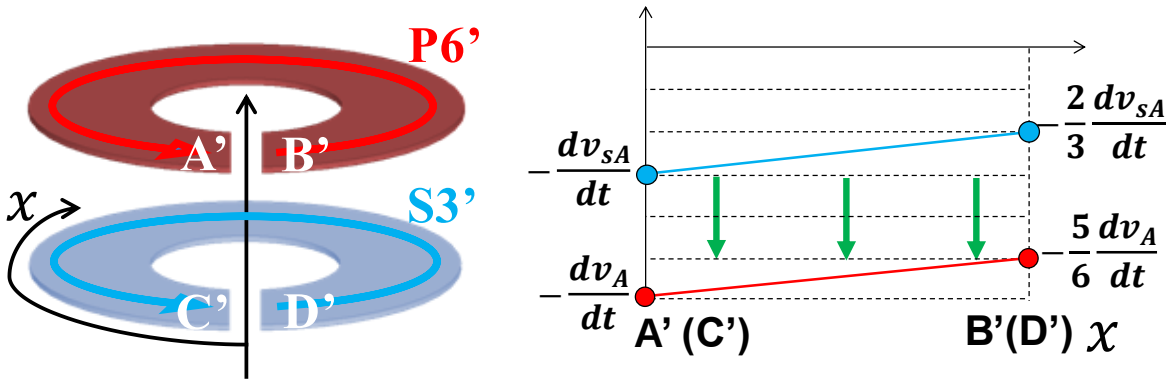


(a) (b)

Fig. 4.5. (a) primary winding No. P6 and secondary winding No. S3 and (b) the *dv*/*dt* distribution along them.

From Fig. 4.5, it is clear that there is *dv/dt* difference between winding P6 and S3. As a result, there is CM current flowing between P6 and S3.

On the other hand, if we take primary winding No. P6' and secondary winding No. S3' (in Transformer 2) as an example (assuming they are next to each other, as shown in Fig. 4.6 (a)), the *dv*/*dt* distribution along the winding (from point A'(C') to point B'(D')) is shown in Fig. 4.6 (b).



(a) (b)

Fig. 4.6. (a) primary winding No. P6' and secondary winding No. S3'. and (b) the *dv*/*dt* distribution along them.

From Fig. 4.6 (b), we can see that there is also *dv/dt* difference between winding. Therefore, there is common mode current flowing between P6' and S3'.

In fact, the inter-winding capacitor can be represented by a lumped model as shown in Fig. 4.7.

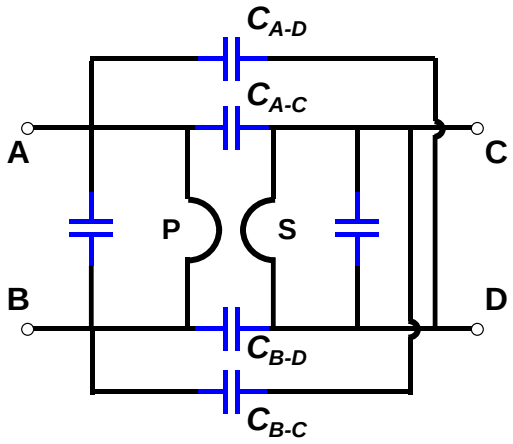


Fig. 4.7. Lumped inter-winding capacitor model.

Because of the winding symmetry, we have,

$$C_{A-C} = C_{B-D}$$

$$C_{A-D} = C_{B-C} \tag{4.10}$$

With this lumped inter-winding capacitor model, the total current flowing from primary winding to secondary winding is,

$$i_{cm} = C_{A-C}\frac{d(v_A - v_C)}{dt} + C_{A-D}\frac{d(v_A - v_D)}{dt} + C_{B-C}\frac{d(v_B - v_C)}{dt} + C_{B-D}\frac{d(v_B - v_D)}{dt}$$

$$= C_{A-C}\frac{d(v_A + \mathrm{v_B} - v_C - v_D)}{dt} + C_{A-D}\frac{d(v_A + \mathrm{v_B} - v_C - v_D)}{dt} \tag{4.11}$$

With the complimentary part of *dv*/*dt*, for primary winding No. P*m* and secondary winding No. S*n*, we have,

$$v_A = \frac{m}{6}v_{pA}$$

$$v_B = \frac{m-1}{6}v_{pA}$$

$$v_C = \frac{n}{3}v_{sA}$$

$$v_D = \frac{n-1}{3}v_{sA} \tag{4.12}$$

Therefore,

$$i_{CM-complimentary}(Pm \to Sn) = C_{A-C}\frac{d(v_A + \mathrm{v_B} - v_C - v_D)}{dt} + C_{A-D}\frac{d(v_A + \mathrm{v_B} - v_C - v_D)}{dt}$$

$$= \frac{2m-1}{6}(C_{A-C} + C_{A-D})\frac{dv_{pA}}{dt} - \frac{2n-1}{3}(C_{A-C} + C_{A-D})\frac{dv_{sA}}{dt} \tag{4.13}$$

For primary winding No. P*m'* and secondary winding No. S*n'*, we have,

$$v_A = -\frac{m'-1}{6}v_{pA}$$

$$v_B = -\frac{m'}{6}v_{pA}$$

$$v_C = -\frac{n'-1}{3}v_{sA}$$

$$v_D = -\frac{n'}{3}v_{sA} \tag{4.14}$$

Therefore,

$$i_{CM-complimentary}(Pm' \to Sn') = C_{A-C}\frac{d(v_A+v_B-v_C-v_D)}{dt} + C_{A-D}\frac{d(v_A+v_B-v_C-v_D)}{dt}$$
$$= -\frac{2m'-1}{6}(C_{A-C}+C_{A-D})\frac{dv_{pA}}{dt} + \frac{2n'-1}{3}(C_{A-C}+C_{A-D})\frac{dv_{sA}}{dt} \quad (4.15)$$

With Eq. (4.13) and Eq. (4.15), we have,

$$i_{CM-complimentary}(Pm \to Sn) + i_{CM-complimentary}(Pm' \to Sn') = 0 \quad (4.16)$$

Back to the example, the CM current between P6/S3 and P6'/S3' are,

$$i_{CM-complimentary}(P6 \to S3) = \frac{11}{6}(C_{A-C}+C_{A-D})\frac{dv_{pA}}{dt} - \frac{5}{3}(C_{A-C}+C_{A-D})\frac{dv_{sA}}{dt} \quad (4.17)$$
$$i_{CM-complimentary}(P6' \to S3') = -\frac{11}{6}(C_{A-C}+C_{A-D})\frac{dv_{pA}}{dt} + \frac{5}{3}(C_{A-C}+C_{A-D})\frac{dv_{sA}}{dt} \quad (4.18)$$

If we compare Eq. (4.17) and Eq. (4.18), we can find that,

$$i_{CM-complimentary}(P6 \to S3) + i_{CM-complimentary}(P6' \to S3') = 0 \quad (4.19)$$

This means for the two pairs of windings, the net CM current from primary side to secondary side generated by the complementary part *dv/dt* is zero.

However, there is also the uncomplimentary part of *dv/dt*. We can draw its distribution across primary winding and secondary winding, as shown in Fig. 4.8. If we assume that *dv/dt* is evenly distributed across each winding, then the *dv/dt* across winding No. P*m* of primary side are $-\frac{m+6}{12}\frac{dv_{rp}}{dt}$ and $-\frac{m+5}{12}\frac{dv_{rp}}{dt}$. And the *dv/dt* across winding No. S*m* of secondary side are $\frac{m+3}{6}\frac{dv_{rs}}{dt}$ and $\frac{m+2}{6}\frac{dv_{rs}}{dt}$.

Similarly, the *dv*/*dt* across winding No. P*m*' of primary side are $\frac{m'-7}{12}\frac{dv_{rp}}{dt}$ and $\frac{m'-6}{12}\frac{dv_{rp}}{dt}$, and the *dv*/*dt* across winding No. S*m*' of secondary side are $\frac{4-m'}{6}\frac{dv_{rs}}{dt}$ and $\frac{3-m'}{6}\frac{dv_{rs}}{dt}$.

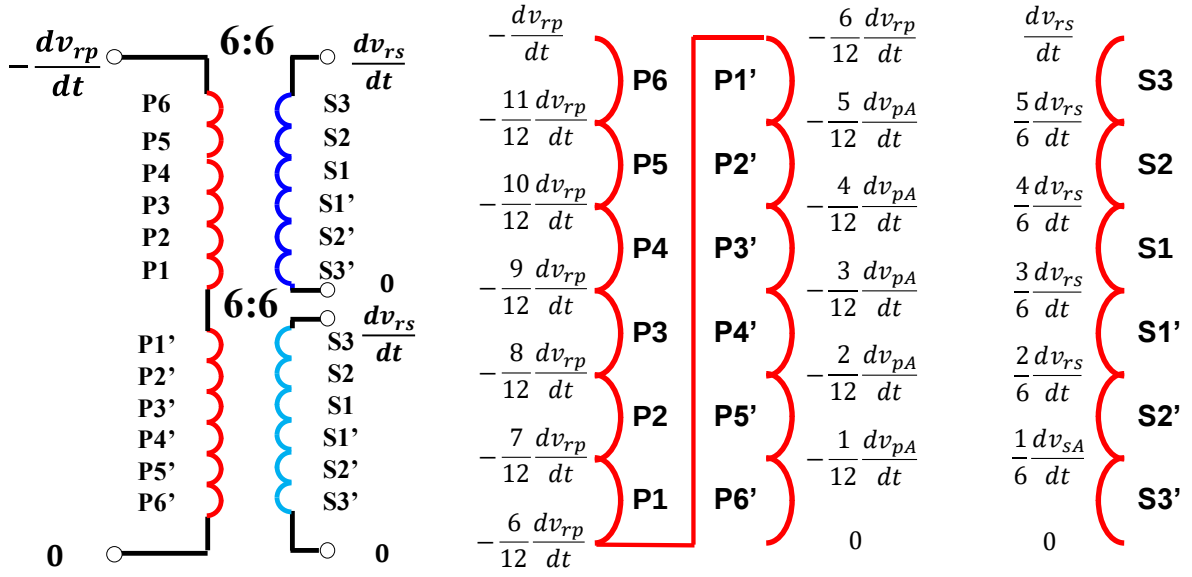
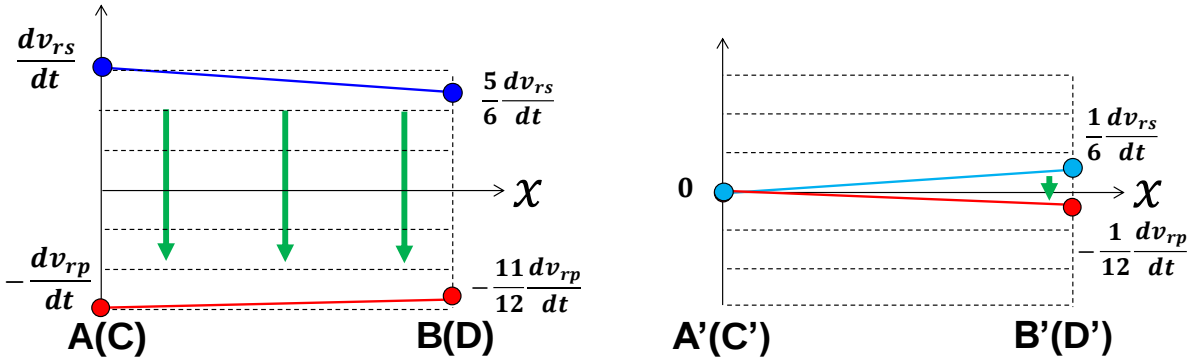


Fig. 4.8. Uncomplimentary part of *dv/dt* distribution across transformer winding.

We can also draw the *dv/dt* distribution between P6 and S3 as well as P6' and S3' using the same concept as before, and the results are shown in Fig. 4.9.



(a) (b)

Fig. 4.9. Uncomplimentary part of *dv*/*dt* distribution along (a) P6 and S3 and (b) P6' and S3'.

With the uncomplimentary of *dv*/*dt*, for primary winding No. P*m* and secondary winding No. S*n*, we have,

$$v_A = -\frac{m+6}{12} v_{pA}$$

$$v_B = -\frac{m+5}{12} v_{pA}$$

$$v_C = \frac{n+3}{6} v_{sA}$$

$$v_D = \frac{n+2}{6} v_{sA} \tag{4.20}$$

Therefore,

$$i_{CM-uncomplimentary}(Pm \to Sn) = C_{A-C}\frac{d(v_A+v_B-v_C-v_D)}{dt} + C_{A-D}\frac{d(v_A+v_B-v_C-v_D)}{dt}$$

$$= -\frac{2m+11}{12}(C_{A-C}+C_{A-D})\frac{dv_{pA}}{dt} + \frac{2n+5}{6}(C_{A-C}+C_{A-D})\frac{dv_{sA}}{dt} \tag{4.21}$$

For primary winding No. P*m'* and secondary winding No. S*n'*, we have,

$$v_A = \frac{m'-7}{12} v_{pA}$$

$$v_B = \frac{m'-6}{12} v_{pA}$$

$$v_C = \frac{4-n'}{6} v_{sA}$$

$$v_D = \frac{3-n'}{6} v_{sA} \tag{4.22}$$

Therefore,

$$i_{CM-uncomplimentary}(Pm' \to Sn') = C_{A-C}\frac{d(v_A+v_B-v_C-v_D)}{dt} + C_{A-D}\frac{d(v_A+v_B-v_C-v_D)}{dt}$$

$$= \frac{2m'-13}{12}(C_{A-C}+C_{A-D})\frac{dv_{pA}}{dt} - \frac{2n'-7}{6}(C_{A-C}+C_{A-D})\frac{dv_{sA}}{dt} \tag{4.23}$$

With Eq. (4.21) and Eq.(4.23), we have,

$$i_{CM-uncomplimentary}(Pm \to Sn) + i_{CM-uncomplimentary}(Pm' \to Sn') = -2(C_{A-C}+C_{A-D})\frac{dv_{pA}}{dt} +$$

$$2(C_{A-C}+C_{A-D})\frac{dv_{sA}}{dt} \tag{4.24}$$

Back to the same example winding, the CM current between winding P6 and S3 (in Transformer 1) as well as P6' and S3' (in Transformer 2) for the uncomplimentary part of *dv/dt* is,

$$i_{CM-uncomplimentary}(P6 \to S3) = -\frac{23}{12}(C_{A-C}+C_{A-D})\frac{dv_{rp}}{dt} + \frac{11}{6}(C_{A-C}+C_{A-D})\frac{dv_{rs}}{dt} \tag{4.25}$$

$$i_{CM-uncomplimentary}(P6' \to S3') = -\frac{1}{6}(C_{A-C}+C_{A-D})\frac{dv_{rp}}{dt} + \frac{1}{6}(C_{A-C}+C_{A-D})\frac{dv_{rs}}{dt} \tag{4.26}$$

Comparing Eq. (4.25) and (4.26), we find that,

$$i_{CM-uncomplimentary}(P6 \rightarrow S3) + i_{CM-uncomplimentary}(P6' \rightarrow S3') = -2(C_{A-C} + C_{A-D})\frac{dv_{rp}}{dt} + 2(C_{A-C} + C_{A-D})\frac{dv_{rs}}{dt} \quad (4.27)$$

This means CM current generated by the uncomplimentary part of *dv*/*dt* is not fully cancelled, and we will observe CM noise.

4.2 Proposed symmetrical transformer structure

From the analysis in Section I (Fig. 4.5, Fig. 4.6 and Eq. (4.19)), with the complimentary part of *dv/dt*, we have the opportunity to cancel the CM current. However, it needs a purposely-designed transformer winding arrangement so that we can pair the CM current in Transformer 1 and Transformer 2. If the two transformers are connected in a way as shown in Fig. 4.10, with the same principle we used in Section I, only the CM current between P6/S3 and P6'/S3' and between P1/S3' and P1'/S3 are in pair and can cancel each other (green arrow shown in Fig. 4.10). Other than that, there is no cancellation effect. For example, between P5/S3 and P6'/S2', the CM current is,

$$i_{CM-complimentary}(P5 \rightarrow S3) = \frac{3}{2}(C_{A-C} + C_{A-D})\frac{dv_{pA}}{dt} - \frac{5}{3}(C_{A-C} + C_{A-D})\frac{dv_{sA}}{dt}$$

$$i_{CM-complimentary}(P6' \rightarrow S2') = -\frac{11}{6}(C_{A-C} + C_{A-D})\frac{dv_{pA}}{dt} + (C_{A-C} + C_{A-D})\frac{dv_{sA}}{dt} \quad (4.28)$$

And

$$i_{CM-complimentary}(P5 \rightarrow S3) + i_{CM-complimentary}(P6' \rightarrow S2') = -\frac{1}{3}(C_{A-C} + C_{A-D})\frac{dv_{pA}}{dt} - \frac{2}{3}(C_{A-C} + C_{A-D})\frac{dv_{sA}}{dt} \quad (4.29)$$

The current without cancellation effect is shown in yellow and purple arrows in Fig. 4.10.

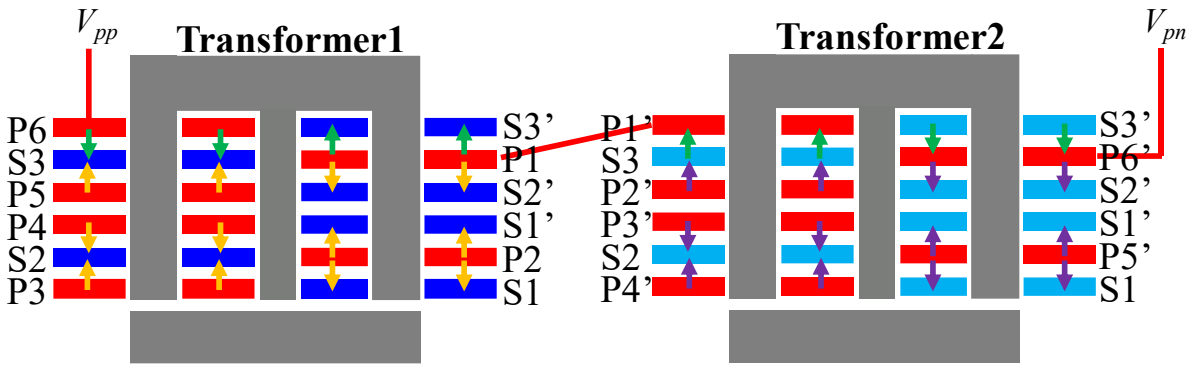


Fig. 4.10. Unsymmetrical transformer structure with compromised noise cancellation effect.

In order to pair all the CM current, we need to purposely connect the two transformer in a symmetrical manner. We can flip Transformer 2 and connect it with the first transformer in a way shown in Fig. 4.11. With this connection, we can find that all the CM current are in pairs now (P6/S3 and P6'/S3', P4/S2 and P4'/S2', etc.). As a result, the net CM current generated by complimentary part of *dv/dt* between the two transformers is zero, as shown in Fig. 4.12 (a).

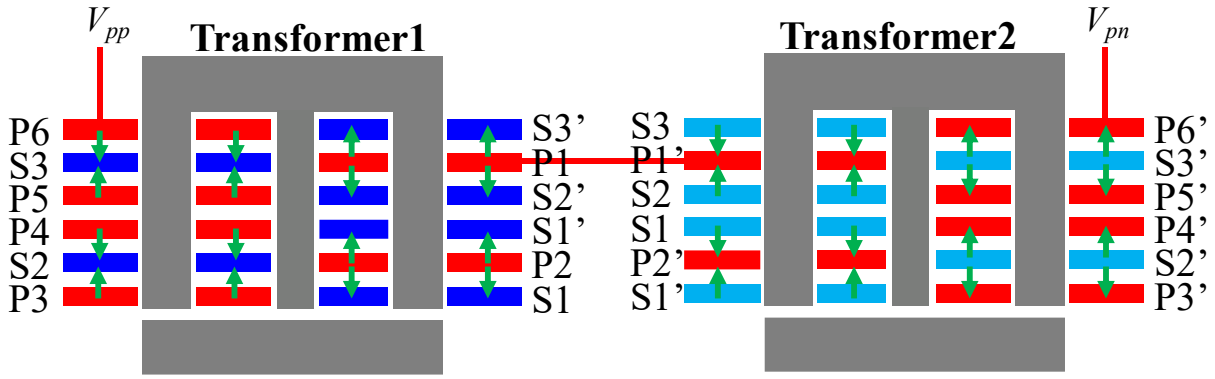


Fig. 4.11. Proposed symmetrical transformer structure with CM noise cancellation effect (for complimentary part of *dv/dt*).

However, according to previous analysis, even with this proposed symmetrical transformer structure, the net CM current generated by the uncomplimentary part of *dv/dt* is still not zero, as shown in Fig. 4.12 (b). We need to find out a way to eliminate CM current generated by the uncomplimentary part of *dv/dt*.

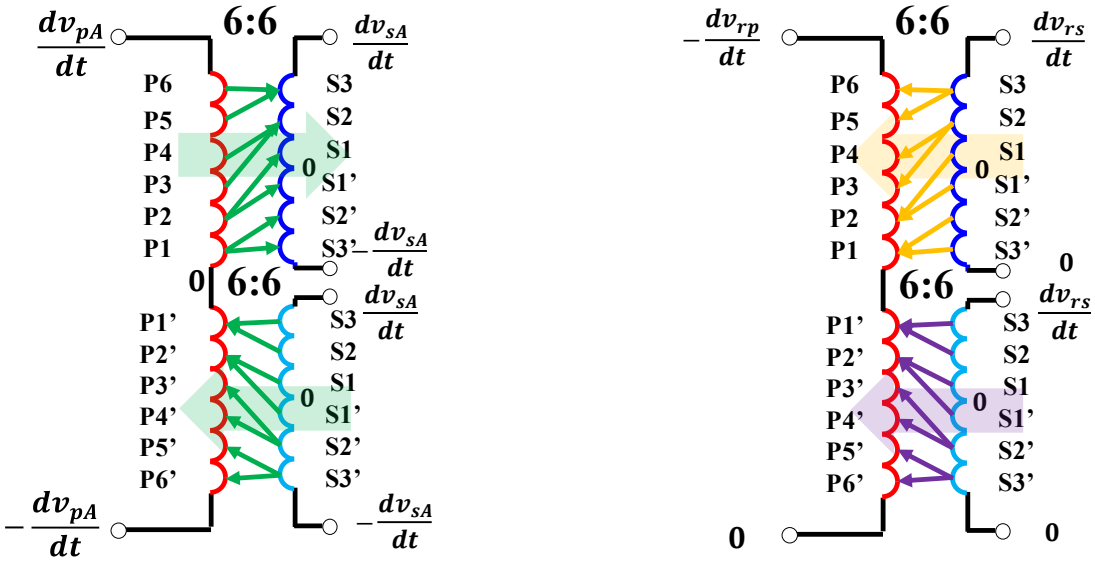


Fig. 4.12. The net CM current generated by (a) complimentary part of *dv/dt* and (b) uncomplimentary part of *dv/dt*.

4.3 Proposed symmetrical resonant converter structure.

In order to get rid of this uncomplimentary part of *dv/dt*, a symmetrical CLLC resonant converter with split resonant capacitor is used, as shown in Fig. 4.13. Here, the resonant capacitors are evenly split and distributed on both positive and negative terminals of the transformer.

The terminal voltage potential of transformer with split resonant capacitors is shown in Fig. 4.13, and their expressions are,

$$V_{pp} = V_{pA} - V_{rp}$$

$$V_{pn} = V_{pB} + V_{rp} = -V_{pA} + V_{rp}$$

$$V_{sp} = V_{sA} + V_{rs}$$

$$V_{sn} = V_{sB} - V_{rs} = -V_{sA} - V_{rs} \quad (4.30)$$

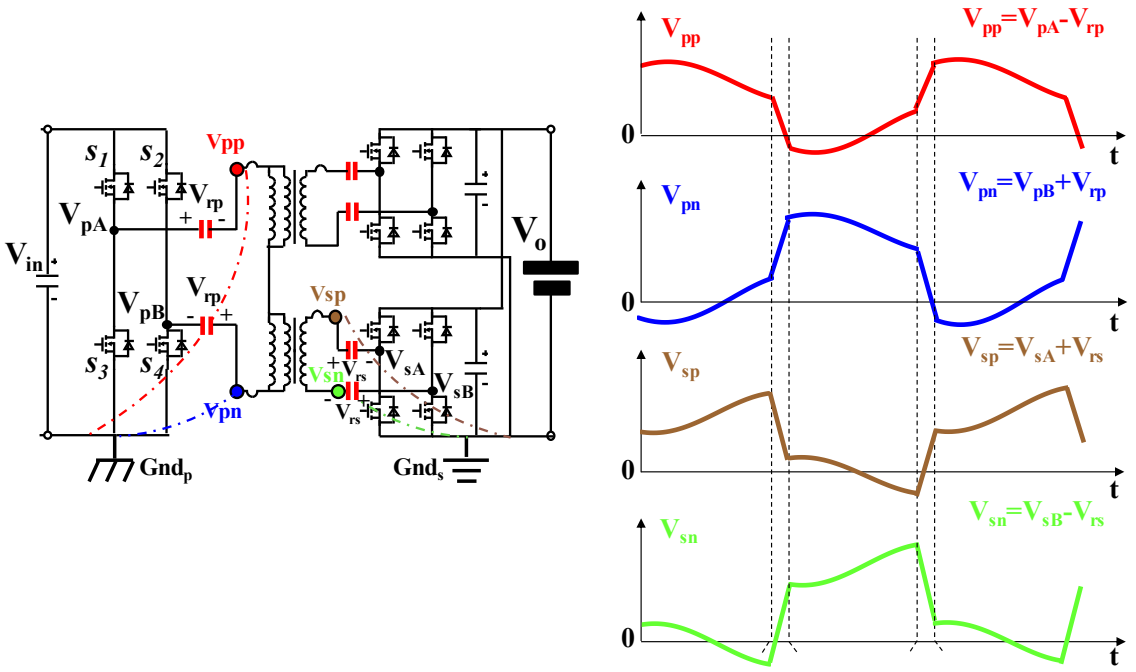


Fig. 4.13. (a) Proposed symmetrical structure and (b) its terminal voltage waveform @$f_s = f_o$.

If we look at the *dv/dt* of transformer terminal voltage potential, we have,

$$\frac{dV_{pp}}{dt} = \frac{dV_{pA}}{dt} - \frac{dV_{rp}}{dt}$$

$$\frac{dV_{pn}}{dt} = \frac{dV_{pB}}{dt} + \frac{dV_{rp}}{dt}$$

$$\frac{dV_{sp}}{dt} = \frac{dV_{sA}}{dt} + \frac{dV_{rs}}{dt}$$

$$\frac{dV_{sn}}{dt} = \frac{dV_{sB}}{dt} - \frac{dV_{rs}}{dt} \tag{4.31}$$

This time, the *dv/dt* on transformer terminals are all complimentary,

$$\frac{dV_{pp}}{dt} = -\frac{dV_{pn}}{dt}$$

$$\frac{dV_{sp}}{dt} = -\frac{dV_{sn}}{dt} \tag{4.32}$$

At this time, the total CM current between winding P6/S3 and P6'/S3'is,

$$i_{CM}(P6 \rightarrow S3) = \frac{11}{6}(C_{A-C} + C_{A-D})\frac{dv_{pp}}{dt} - \frac{5}{3}(C_{A-C} + C_{A-D})\frac{dv_{sp}}{dt} \quad (4.33)$$

$$i_{CM}(P6' \rightarrow S3') = -\frac{11}{6}(C_{A-C} + C_{A-D})\frac{dv_{pp}}{dt} + \frac{5}{3}(C_{A-C} + C_{A-D})\frac{dv_{sp}}{dt} \quad (4.34)$$

According to Eq. (4.33) and Eq. (4.34), we have,

$$i_{CM}(P6 \rightarrow S3) + i_{CM}(P6' \rightarrow S3') = 0 \quad (4.35)$$

By using the symmetrical transformer structure, the CM current between primary and secondary winding is shown in Fig. 4.14. This time, since there is only complimentary part of *dv/dt*, the net CM current is zero.

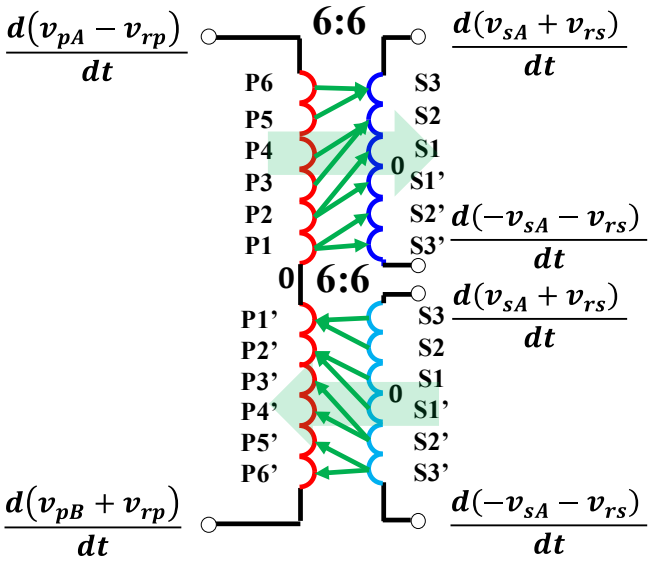


Fig. 4.14. *dv/dt* distribution across the transformer and the resulted CM current.

From the above analysis, if the symmetrical structure with split resonant capacitor as well as symmetrical transformer structure is used, ideally there is no CM current flowing through the two transformers and therefore, CM noise can be greatly reduced.

4.4 Extension to general cases

(1) Rotation of PCB winding

For PCB windig transformer, the windings are not always aligned with the same angle. Especially between primary winding and secondary winding. With different input and output terminal locations, the windings may rotate with certain angle. If we still use P6 and S3 as an example, the windings after rotation are shown in Fig. 4.15.

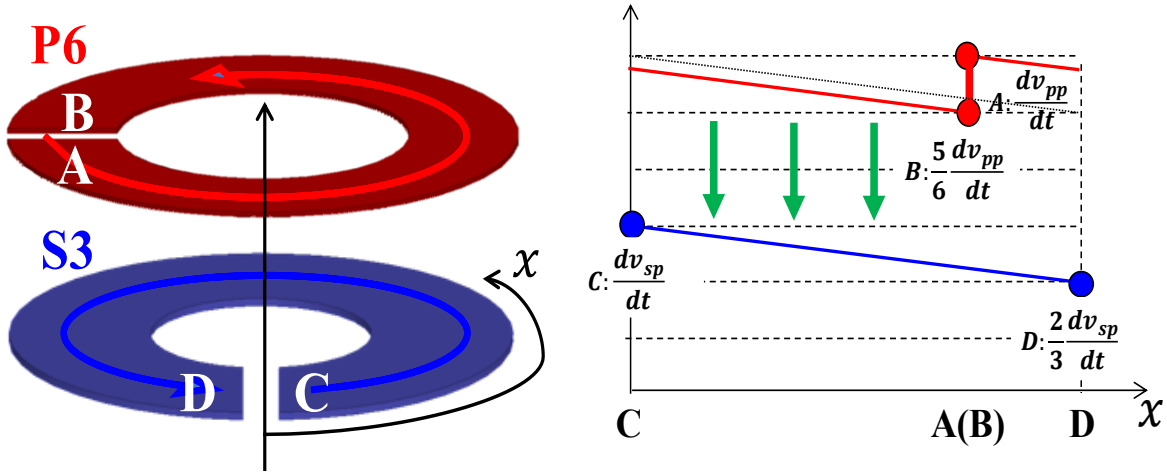


Fig. 4.15. Rotation between primary winding P6 and secondary winding S3.

If winding P6' and S3' has the same rotation angle, then the *dv*/*dt* along the winding can be shown in Fig. 4.16.

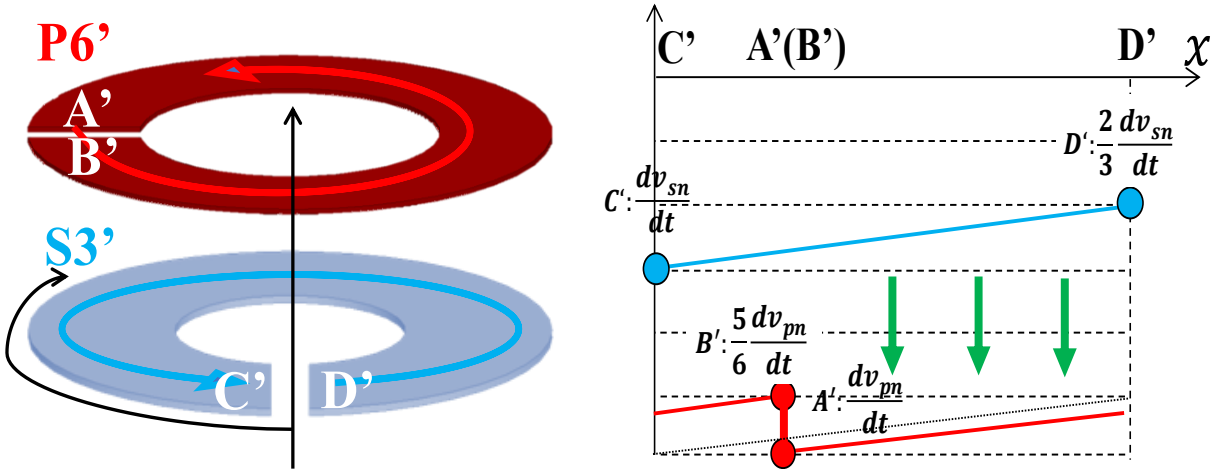


Fig. 4.16. Rotation between primary winding P6' and secondary winding S3'.

Using the same method, we can derive the CM current flowing from primary side to the secondary side.

Consider *x* is the rotation angle of primary side compared with secondary side in counter clockwise direction, the CM current between primary winding and secondary winding is,

$$i_{CM} = \frac{x}{2\pi}\left(C_{A-C}\frac{d\left(\left[v_B+\frac{x}{2\pi}(v_A-v_B)\right]-v_C\right)}{dt} + C_{B-D}\frac{d\left(v_B-\left[v_c-\frac{x}{2\pi}(v_c-v_D)\right]\right)}{dt} + C_{A-D}\frac{d\left(\left[v_B+\frac{x}{2\pi}(v_A-v_B)\right]-\left[v_c-\frac{x}{2\pi}(v_c-v_D)\right]\right)}{dt} + C_{B-C}\frac{d(v_B-v_C)}{dt}\right) + \frac{2\pi-x}{2\pi}\left(C_{A-C}\frac{d\left(v_A-\left[v_D+\frac{2\pi-x}{2\pi}(v_C-v_D)\right]\right)}{dt} + C_{B-D}\frac{d\left(\left[v_A-\frac{2\pi-x}{2\pi}(v_A-v_B)\right]-v_D\right)}{dt} + C_{A-D}\frac{d(v_A-v_D)}{dt} + C_{B-C}\frac{d\left(\left[v_A-\frac{2\pi-x}{2\pi}(v_A-v_B)\right]-\left[v_D+\frac{2\pi-x}{2\pi}(v_C-v_D)\right]\right)}{dt}\right) \quad (4.36)$$

And Eq. (4.36) can be simplified to,

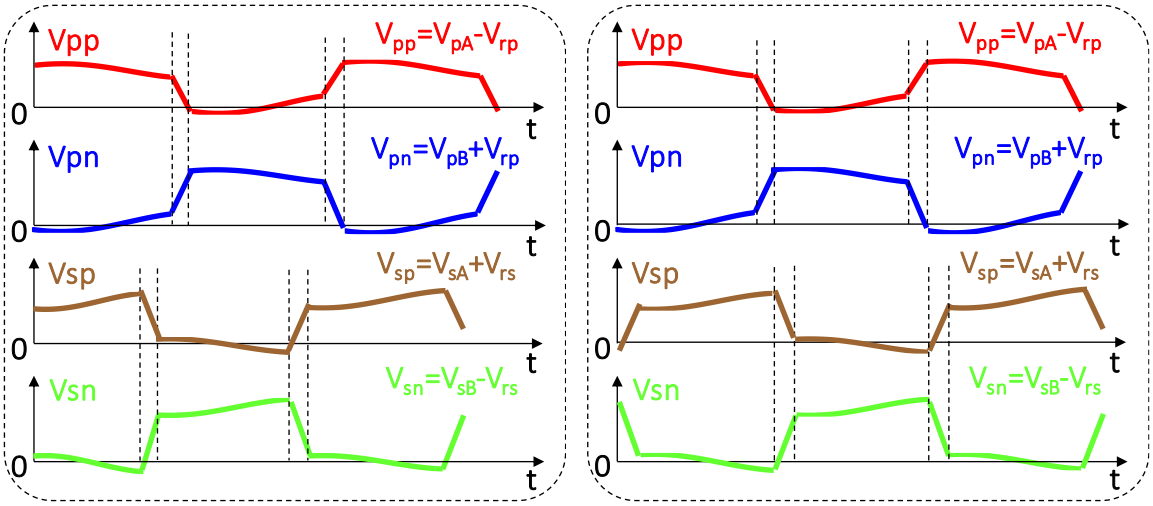
$$i_{CM} = (C_{A-C}+C_{A-D})\frac{d(v_A+v_B-v_C-v_D)}{dt} \quad (4.37)$$

Compare Eq. (4.37) with Eq. (4.11), it is clear that rotation angle doesn't impact the CM current between primary windings and secondary windings. As long as Transformer 1 and Transformer 2 keeps the same rotation angle, the cancellation effect still exists.

From the above analysis, even though windings are rotated, as long as the rotation angles between the two pairs of windings are the same, the total CM current is still zero with the proposed symmetrical transformer and symmetrical resonant converter structure.

(2) Changing of switching frequency

Although, all the above analysis is based on the case that switching frequency and resonant frequency are equal, it can be extended to general cases where the relation between switching frequency and resonant frequency are not fixed. In Fig. 4.17, the voltage potentials on transformer terminals are given. Although the switching instant between primary side and secondary side may not be synchronized, Eq. (4.32) still holds. As a result, the cancellation effect still exits.



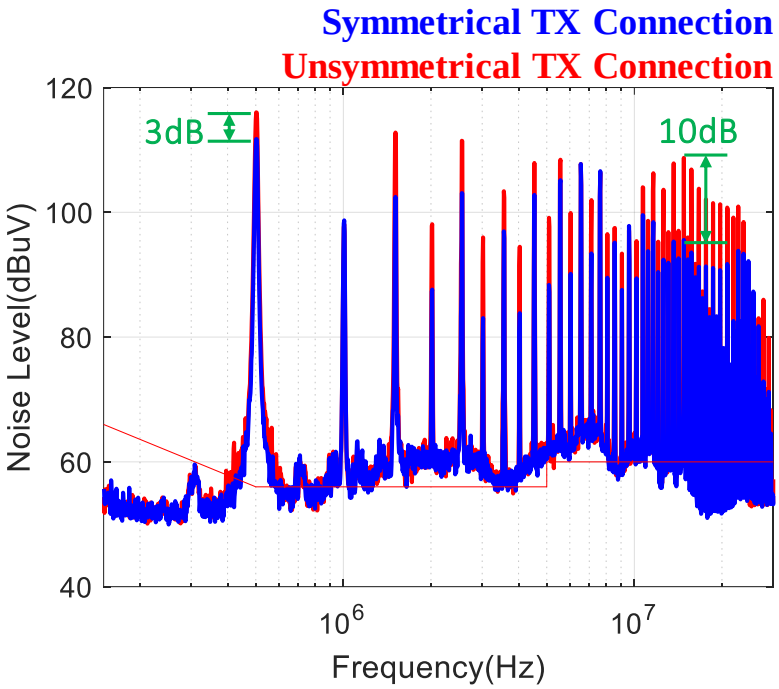
(a) $f_s < f_o$ (b) $f_s > f_o$

Fig. 4.17. Voltage potential on transformer terminal when $f_s \neq f_o$.

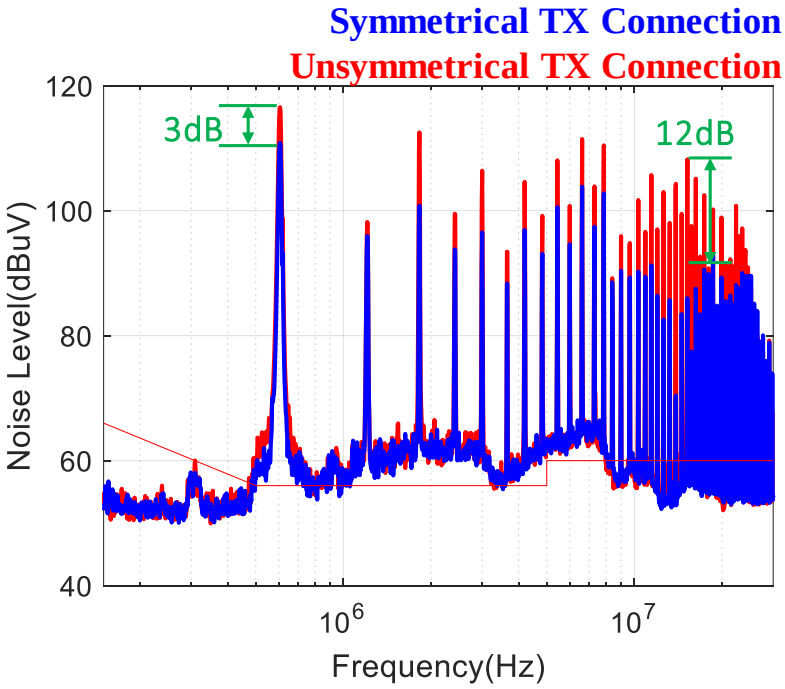
However, in order to achieve Eq. (4.32), the gate signal of primary side has to match with each, that is, gate signals of S_1 and S_4 are the same and gate signals of S_2 and S_3 are the same.

4.5 Experimental verification

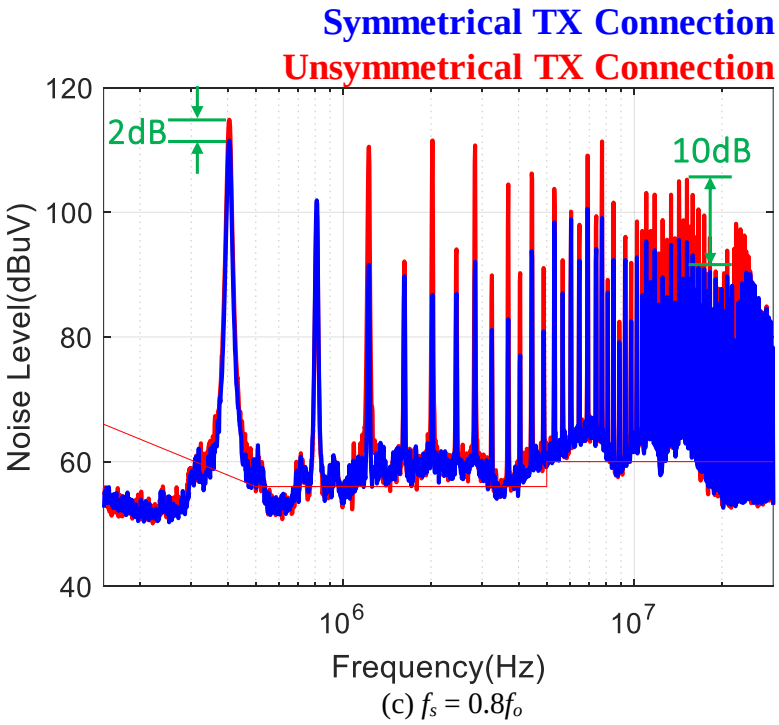
CM noise spectrum is tested to demonstrate the superior performance of the proposed symmetrical structure. The comparison between symmetrical transformer structure and unsymmetrical transformer structure are shown in Fig. 4.18.



(a) $f_s = f_o$



(b) $f_s = 1.2f_o$

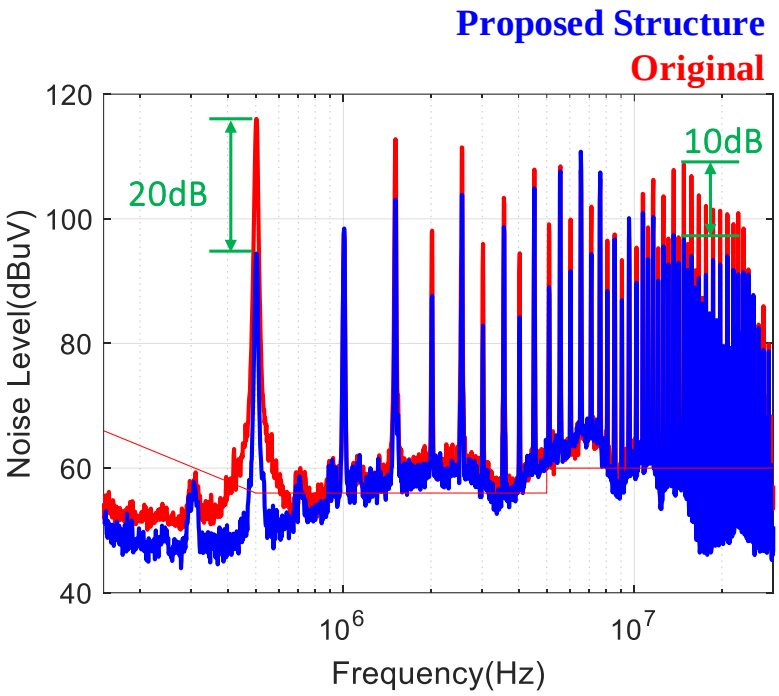


(c) $f_s = 0.8f_o$

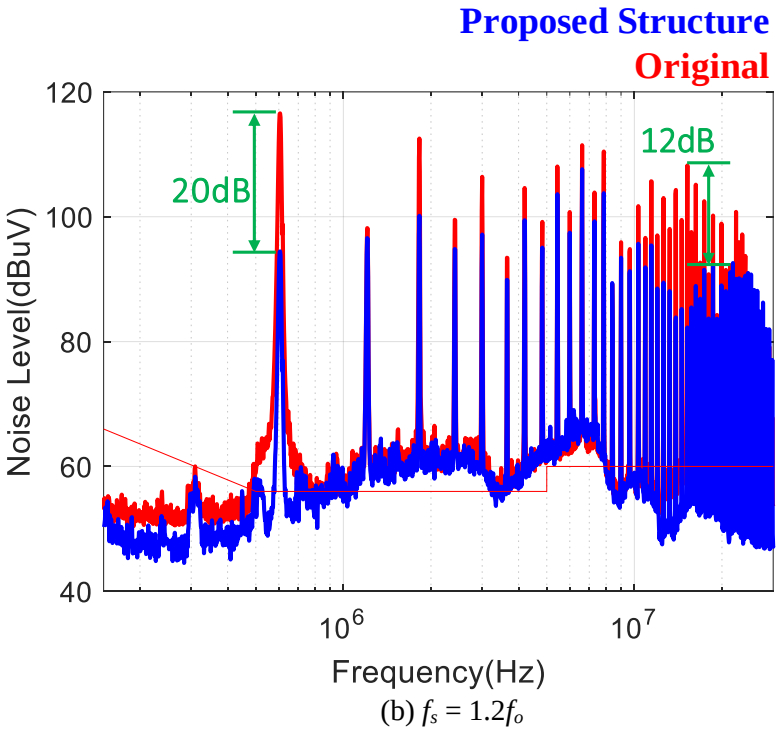
Fig. 4.18. Testing results of EMI performance comparison between symmetrical transformer and unsymmetrical transformer.

It is clear that by using the proposed transformer connection method, CM noise is reduced effectively, especially at high frequency range, which has over 10 dB reduction.

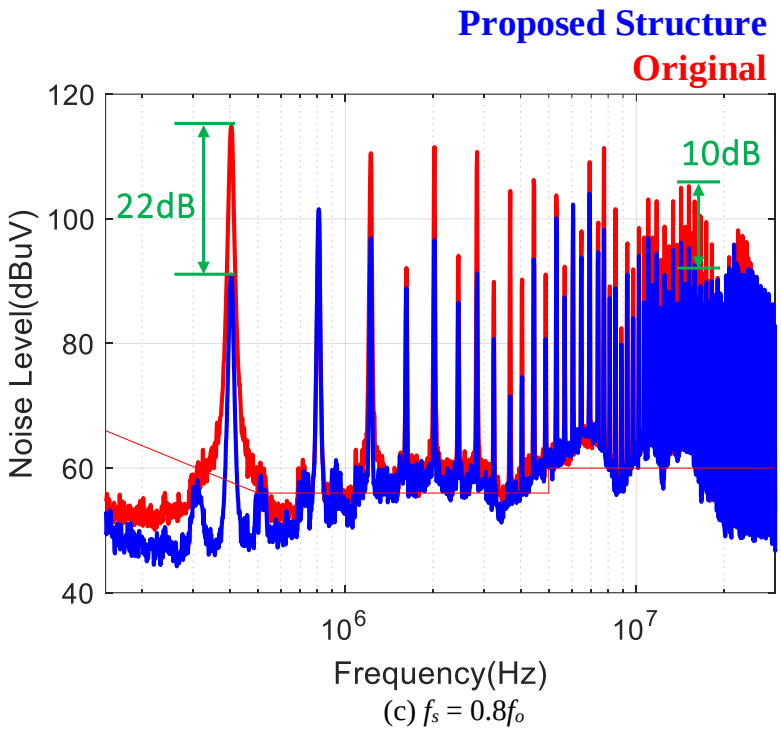
When the proposed split capacitor is also implemented, the resulted CM noise measurement are shown in Fig. 4.19.



(a) $f_s = f_o$



(b) $f_s = 1.2f_o$



(c) $f_s = 0.8f_o$

Fig. 4.19. Testing results of EMI performance with the proposed split capacitor and symmetrical transformer connection.

From the measurement results, we can see that the proposed symmetrical resonant converter structure and the symmetrical transformer structure can help to significantly reduce the CM noise in the system both for fundamental switching frequency and its high order harmonics.

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Chapter 5 **Interleaved CLLC Resonant Converter with Integrated PCB Winding Magnetics**

The time to fully charge an EV using the designed 6.6 kW on-board battery charger is shown in Fig. 5.1. It is around 25 mile/hrs charging rate. For household or local communication, it is enough with overnight charging. However, for long range transportation, the waiting time is too long compared with conventional vehicles with internal combustion engine

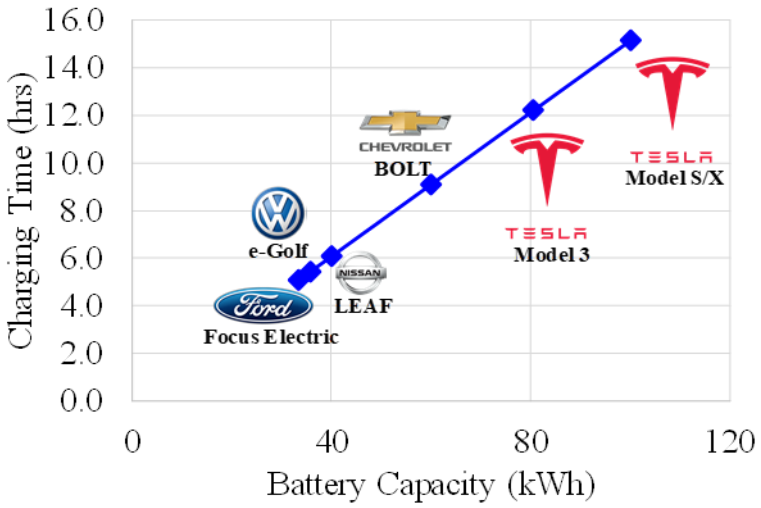


Fig. 5.1. Charging time of electric vehicle using 6.6 kW on-board charger.

Actually, Tesla is using a much larger power on-board charger to charge their EV. The on-board charger installed in a Tesla Model S has a power level of 11.5 kW (shown in Fig. 5.2), which charges the battery in almost half the time compared with the 6.6 kW on-board charger.

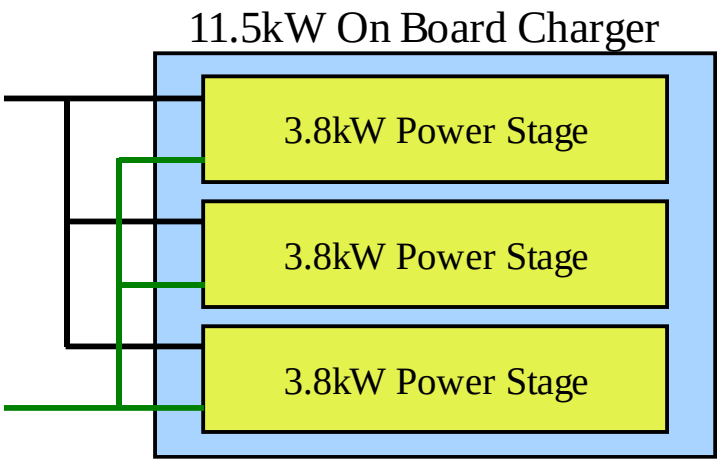


Fig. 5.2. Tesla 11.5 kW on-board charger structure.

Compared with on-board charger, DC charging (or off-board charging) is much faster. By moving the AC/DC conversion from on-board to off-board, the limitation of space and weight does not exist anymore. As a result, the power level can be greatly increased. Hundreds of kilo-watt charging power can be realized and the EV can be fully charged under 30 minutes.

Fig. 5.3 shows Tesla's modularized approach to build their Super Charger, with the power of 135 kW, which can fully charge a Model S/X within 45 minutes. 12 of their 11.5 kW on-board charger modules are put together in parallel (but in a three-phase configuration) to achieve the 135 kW total charging power.

Other companies are also using this modularized approach, as shown in Fig. 5.4. Different companies are building 15 kW AC/DC modules for the charging station application. By put multiple of these modules together in parallel, hundreds of kilo-watt power can be easily achieved.

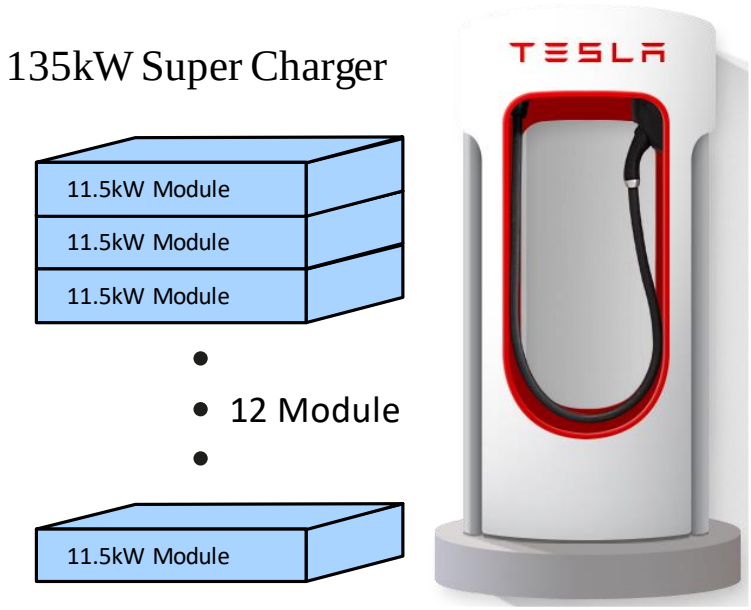


Fig. 5.3. Tesla's modular approach to achieve fast DC charging.

Fig. 5.4. AC/DC module for off-board charging.

In order to satisfy the need for faster charging, it is meaningful to extend the proposed 6.6 kW on-board charger concept to a higher power level and adopt the modularized approach.

In the previous proposed design, two transformers and two sets of full bridge outputs are adopted to achieve 6.6 kW output power. In order to increase the power, we can increase the number of transformers and output sets, as shown in Fig. 5.5. It is a three-phase resonant converter with a total of 12.5 kW power.

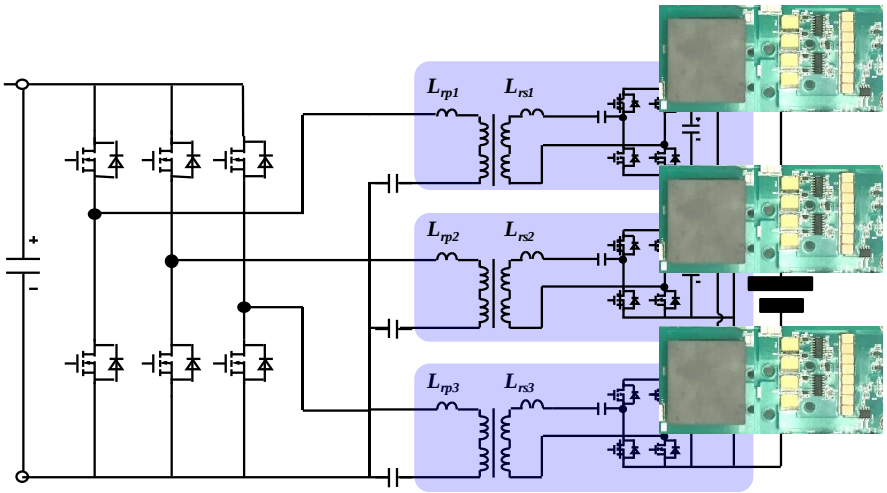


Fig. 5.5.. Extend the power level of the on-board charger using more sets of output.

The three-phase DC-DC resonant converter offers an attractive solution to high power applications due to the reduction in component stresses compared to single-phase resonant converter of the same power rating. There are different types of three-phase resonant converter. The most conventional one is three phases in simple parallel [1], as shown in Fig. 5.6 (a). However, this type of configuration has the problem of current sharing due to the tolerance among each resonant tank. Another option is to put the resonant tank in Y-connection [2, 3], as shown in Fig. 5.6 (b). The benefit of the Y-connection is that it doesn't have current sharing issue. The common Y-node guarantees automatic current balancing between the three phases. However, the voltage over the resonant capacitors always has DC bias, making the soft start-up complicated [4]. In [5], a primary side in Δ-connection (as shown in Fig. 5.6 (c)) series resonant converter is used. This configuration can solve the current sharing issue and also benefits the soft start-up process since the resonant capacitor has no DC bias [4].

Even though the three phase resonant converter has been investigated, the integration of the magnetics is still not fully achieved. In [1, 6], a three-phase integrated transformer is proposed. By using flux cancellation, three transformers are integrated together and the core volume is shrunk. However, they still need bulky resonant inductors, compromising the power density of the whole system. Also, all these transformer designs are litz-wire based, which can be very complicated for mass production, and suffer from bad parasitic control.

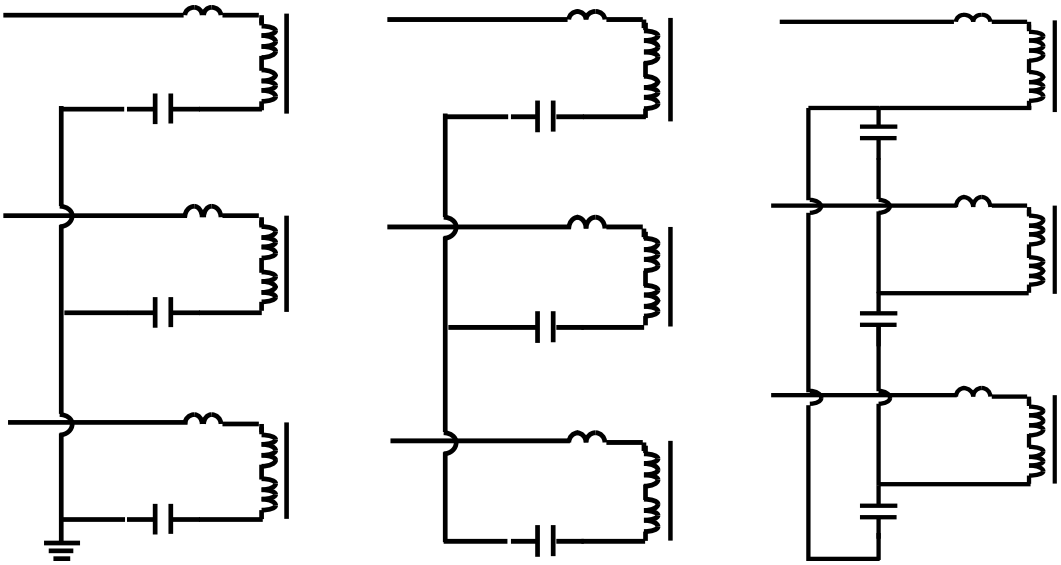


Fig. 5.6. (a) Simple parallel (b) Y-connection and (c) Δ-connection resonant tank.

By using wide bandgap devices (including both GaN and SiC devices), the switching frequency of power electronics converters can be pushed to several hundreds of kHz or even MHz, resulting in a much smaller voltage-second across the transformer. With similar flux density inside the core, the required number of turns becomes much less, making it possible to use PCB as transformer windings. In addition, because of high switching frequency, the required inductor value is also reduced, which makes it easier to achieve magnetic integration.

Compared with the well-known LLC resonant converter, CLLC resonant converter features the same soft switching technique for both primary side and secondary side devices and therefore is very suitable for high frequency operation. In addition, due to the symmetrical resonant tank structure, its bi-directional operation performance is much better by providing gain boost and reduction capability in both directions [7, 8].

5.1 Benefits of three-phase resonant converter

(1) Reduced conduction loss

To parallel resonant converter, one way is to simply connect the input and output in parallel, as shown in Fig. 5.7.

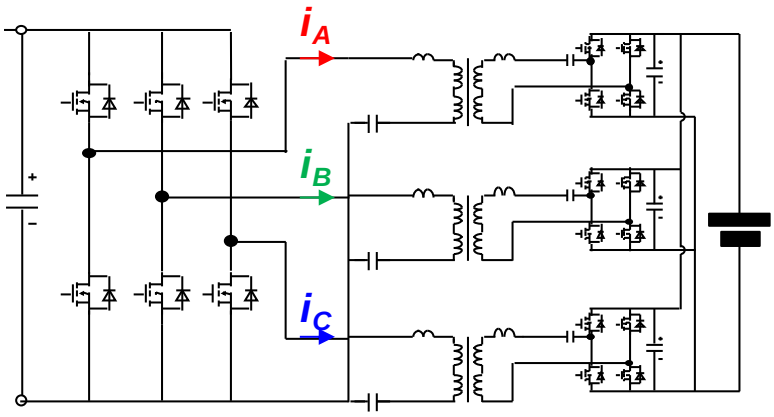


Fig. 5.7. Three single phase resonant converter in parallel.

Another way is to use previously mentioned Δ or Y connected resonant tank. The delta connected resonant capacitors structure is shown in Fig. 5.8.

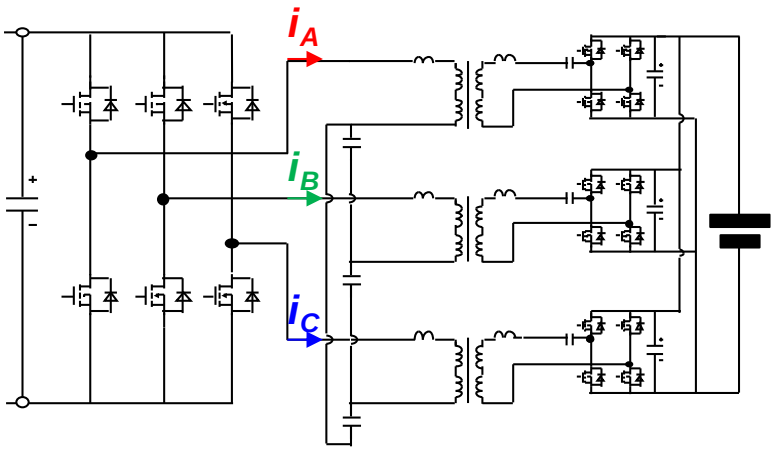


Fig. 5.8. Three-phase resonant converter with Δ-connected resonant capacitors.

To simplify the analysis, we assume the magnetizing inductance is infinite, and as a result, the primary side current waveform at resonant frequency can be drawn, as shown in Fig. 5.9.

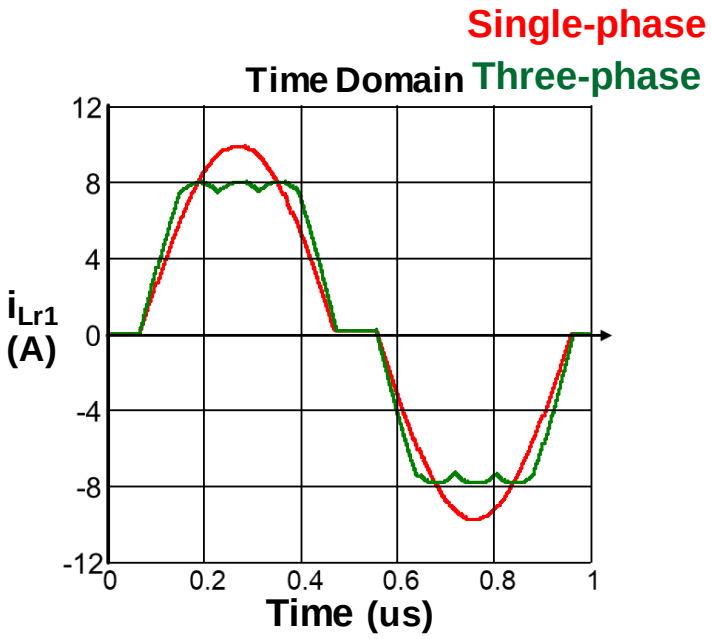


Fig. 5.9. Time domain waveform comparison of primary side current between three single-phase in parallel and three-phase resonant converter.

In addition, we can draw the resonant current and resonant capacitor voltage waveform at resonant frequency in the state trajectory, as shown in Fig. 5.10.

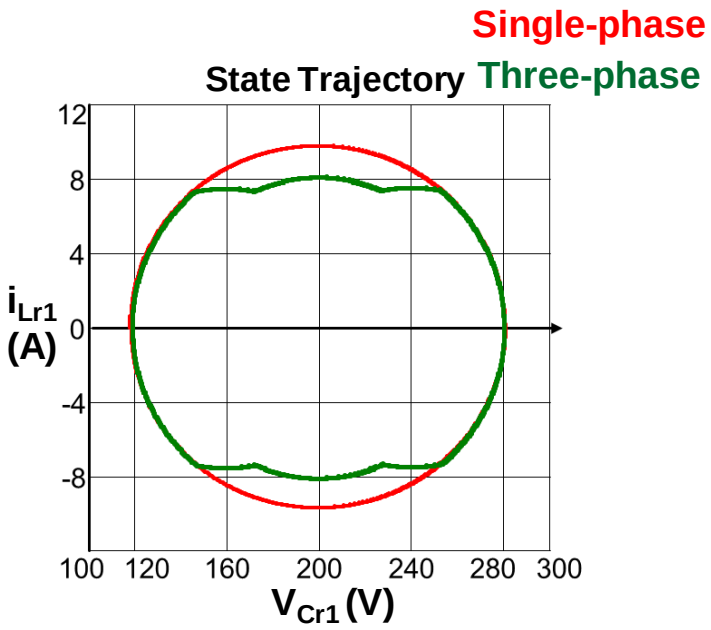


Fig. 5.10. State trajectory comparison of between three single-phase in parallel and three-phase resonant converter.

From this comparison, we can clear see that at resonant frequency, the conventional three single-phase parallel has sinusoid current and voltage waveform, which shows a circle in the state trajectory.

However, for the three-phase resonant converter due to the interaction between the three phases during dead time, the current waveform is reshaped, resulting in lower peak value (RMS value). This phenomenon can also be seen in the state trajectory, where the circle is smaller in vertical direction.

It should be noted that this RMS current reduction phenomenon is only shown when magnetizing inductance is involved in the resonance (switching frequency is equal or less than resonant frequency). When it is not involved, this phenomenon does not exist.

Due to the reduced RMS value, the conduction loss can be reduced.

(2) Automatic current balancing

Paralleling resonant converters with good interleaving is always challenging. Resonant converter relies on changing switching frequency to regulating the output voltage. However, different switching frequencies between the paralleled branches mean no fixed phase shift, which leads to bad interleaving.

With single phase parallel structure as shown in Fig. 5.7, to keep good interleaving, the switching frequency of each branch needs to be the same. However, if there is component mismatch between each phase, for example, Phase C resonant capacitor has 5% smaller value compared with Phase A and Phase B,

$$C_{rA} = C_{rB} = 1.05C_{rC} \tag{5.1}$$

Then the resonant frequency of phase C will be about 2.5% larger.

$$f_{rA} = f_{rB} = 0.976f_{rC} \tag{5.2}$$

However, this 2% larger resonant frequency mismatch can cause significant current sharing problem, as shown in Fig. 5.11.

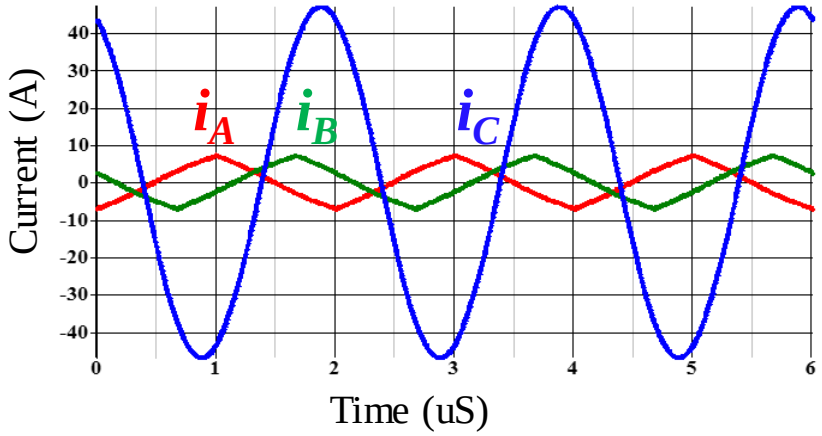


Fig. 5.11. Primary side current for three single-phase parallel with resonant capacitor mismatch.

The resonant behind this is straightforward. Because of the different resonant frequencies, the switching frequency of Phase C is larger than its resonant frequency, which means the gain of Phase C is actually higher than Phase A and Phase B. As a result, there is almost no current flowing through Phase A and Phase B.

However, with the three-phase configuration shown in Fig. 5.8, due to the Δ-connected resonant capacitors, the voltage across the resonant capacitors is balanced and impacts the current distribution. The resulted primary side resonant current is shown in Fig. 5.12.

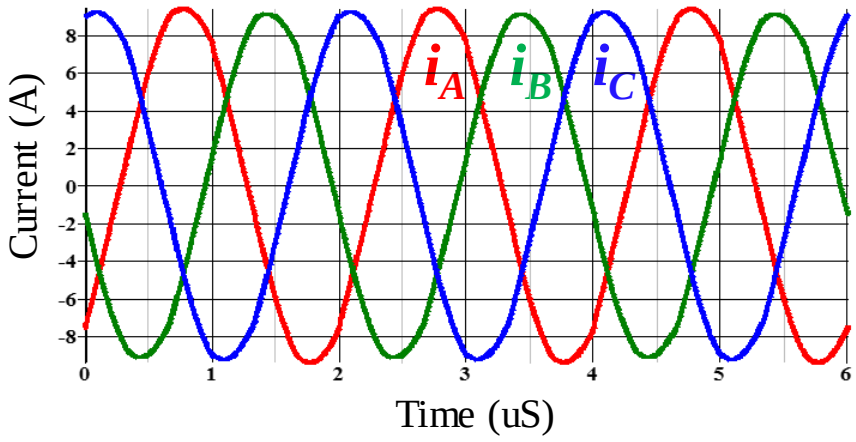


Fig. 5.12. Primary side current for three-phase resonant converter with resonant capacitor mismatch.

This automatic current balancing feature is very beneficial since the component mismatch is unavoidable in mass production.

(3) Magnetic integration

Another benefit of the three-phase resonant converter compared with three single-phase in parallel is the possibility of magnetic integration. Due to the Δ-connection on the primary side, the sum of primary side current is forced to be zero, along with the interleaving between the three phases, further magnetic integration can be achieved.

5.2 Evaluation of suitable 1.2 kV SiC MOSFET

The proposed three-phase CLLC resonant converter with Δ-connection on the primary side is shown in Fig. 5.13. The input voltage is 600 V - 800 V and the output voltage is 250 V - 450 V. The same variable DC-link voltage concept is adopted here as in the previously proposed on-board charger. As a result, 1.2 kV SiC devices are used for the primary side and 650 V GaN devices are selected for the secondary side. Also, due to the half bridge configuration on the primary side, only 1:1 turns ratio is required for the transformer in each phase.

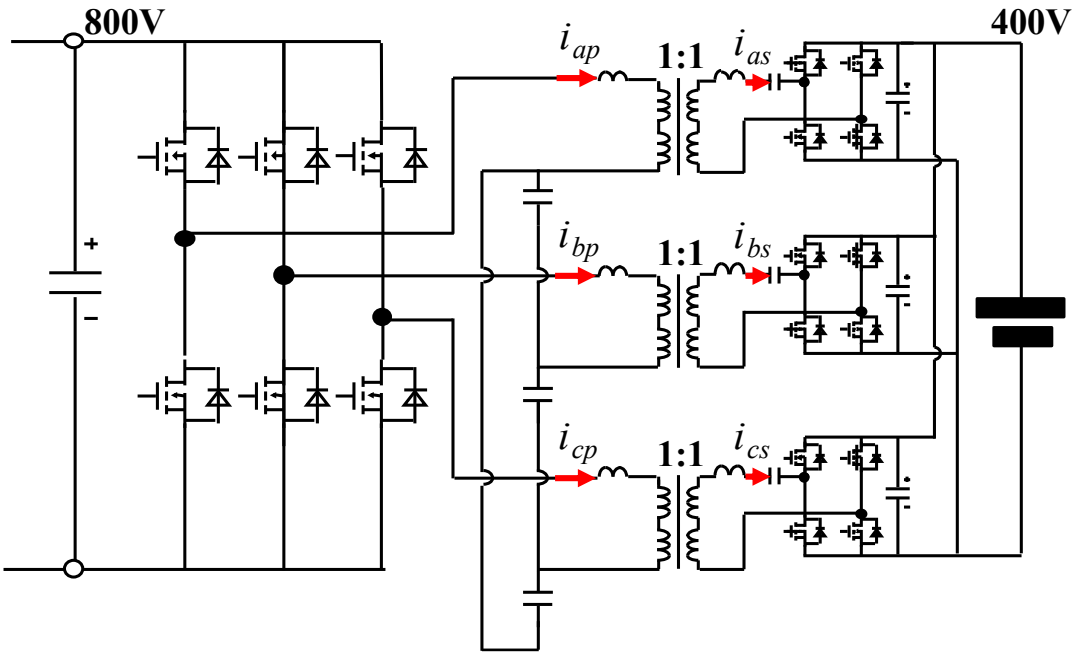


Fig. 5.13. Proposed three-phase CLLC resonant converter.

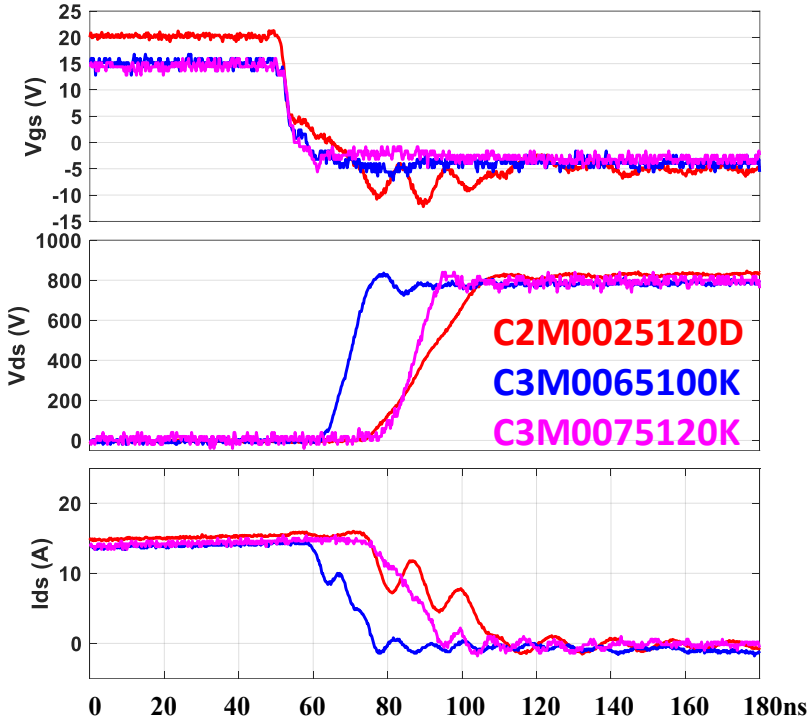
Three different SiC devices from WOLFSPEED are selected as primary side device candidates (as shown in Table 5.1). Since zero voltage switching (ZVS) is always guaranteed for resonant converters, we only need to focus on the device turn off.

Table 5.1. 1.2 kV SiC device candidates.

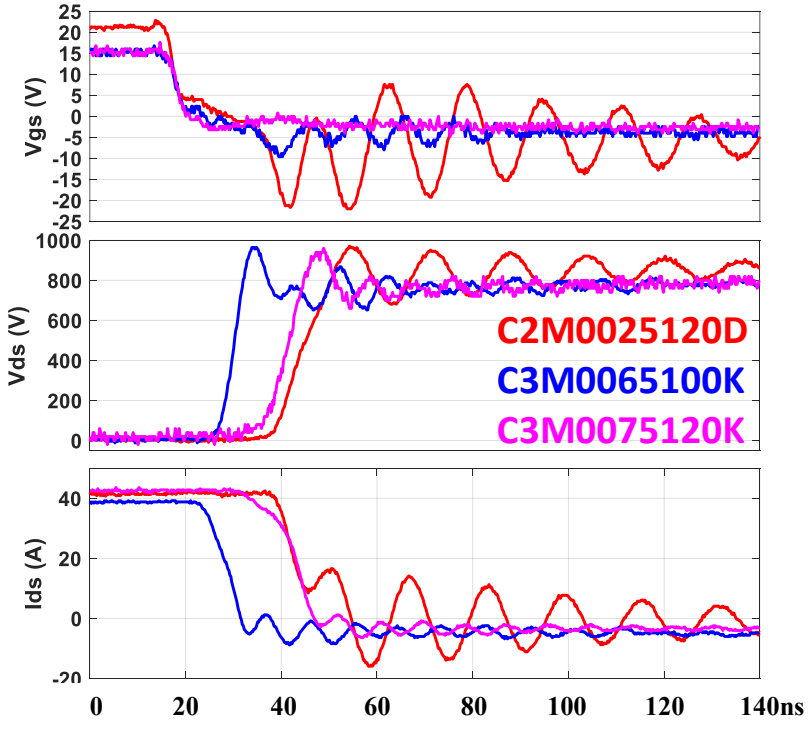
Device	Gen.2: C2M0025120D	Gen.3: C3M0065100K	Gen.3: C3M0075120K
V_{ds}	1.2 kV	1 kV	1.2 kV
I_d@100°C	60 A	22.5 A	19.7 A
R_{dson}@100°C	32.5 mΩ	75 mΩ	86 mΩ
Q_g	161 nC	35 nC	51 nC
C_{oss}	220 pF@V_{ds} = 1000 V	60 pF@V_{ds} = 600 V	58 pF@V_{ds} = 1000 V
R_{g_int}	1.1 Ω	4.7 Ω	10.5 Ω
Package	TO247-3L (w/o Kelvin Connection)	TO247-4L (w/ Kelvin Connection)	TO247-4L (w/ Kelvin Connection)

Their turn off performances are tested experimentally with 0 Ω external gate resistor. Fig. 5.14 (a) shows the turn off waveform comparison under 800 V and 15 A, while Fig. 5.14 (b) shows the turn off performance under 800 V and 40 A. From the testing results, we can find out that with the conventional TO-247-3L, the gate signal (V_{gs}) has a lot of ringing under high current turn off condition because of the coupling between power loop and driving loop (through common source inductance). Under 40 A turn off, the gate voltage reaches 5 V during the ringing, which is already above the threshold voltage 2.6 V, and the minimum gate voltage reaches -20 V, which is also beyond the gate voltage limit of the device: -10 V. Therefore, the convention 3 lead package is not suitable for high frequency operation.

In comparison, the Gen. 3 devices, which have the advanced 4 lead packages, perform much better. There is almost no ringing on the gate signal even with peak current turn off.



(a) turn off waveform at 800 V and 15 A.



(b) turn off waveform at 800 V and 40 A.

Fig. 5.14. Turn off waveform of the three SiC device candidates.

The turn off loss comparison of the three candidates is shown in Fig. 5.15. From this figure, we can see that the Gen. 3 1 kV device has the lowest turn off loss. While for the Gen. 3 1.2 kV device, due to the much larger internal gate resistor, the turn off loss increases significantly as the turn off current becomes larger. As a result, the Gen. 3 1 kV device is selected for the primary side of the converter.

As for the secondary side, 650 V GaN device GS66516T from GaN Systems is selected to lower down the conduction loss.

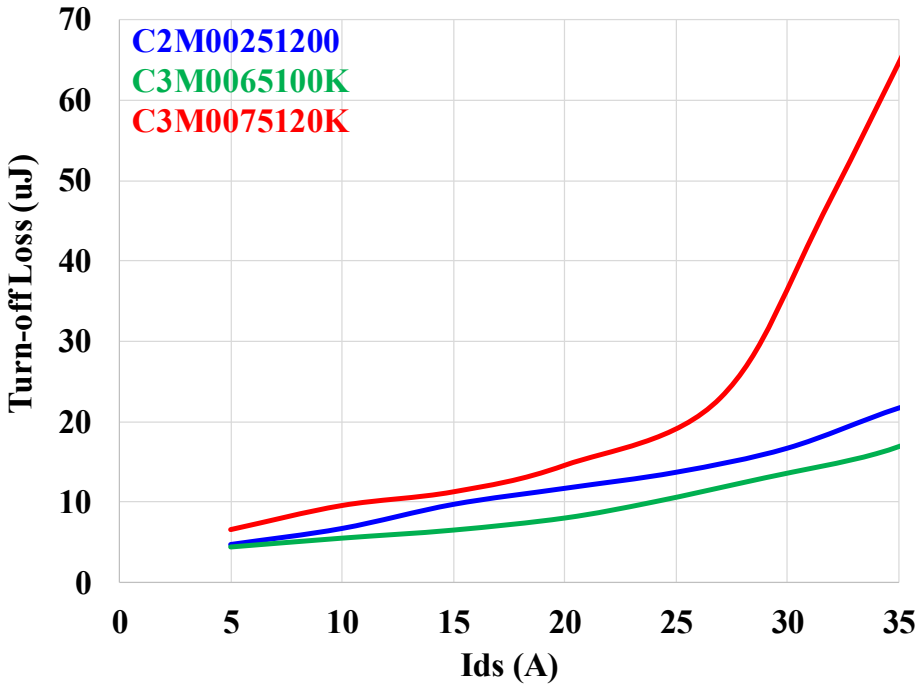


Fig. 5.15. Turn off loss comparison under 800 V.

5.3 Proposed integrated PCB magnetics with flux cancellation

The proposed single-phase integrated magnetic structure for CLLC bi-directional resonant converter in Chapter 3 can be easily extended to a much higher power level: 12.5 kW using three magnetic cells, as shown in Fig. 5.16.

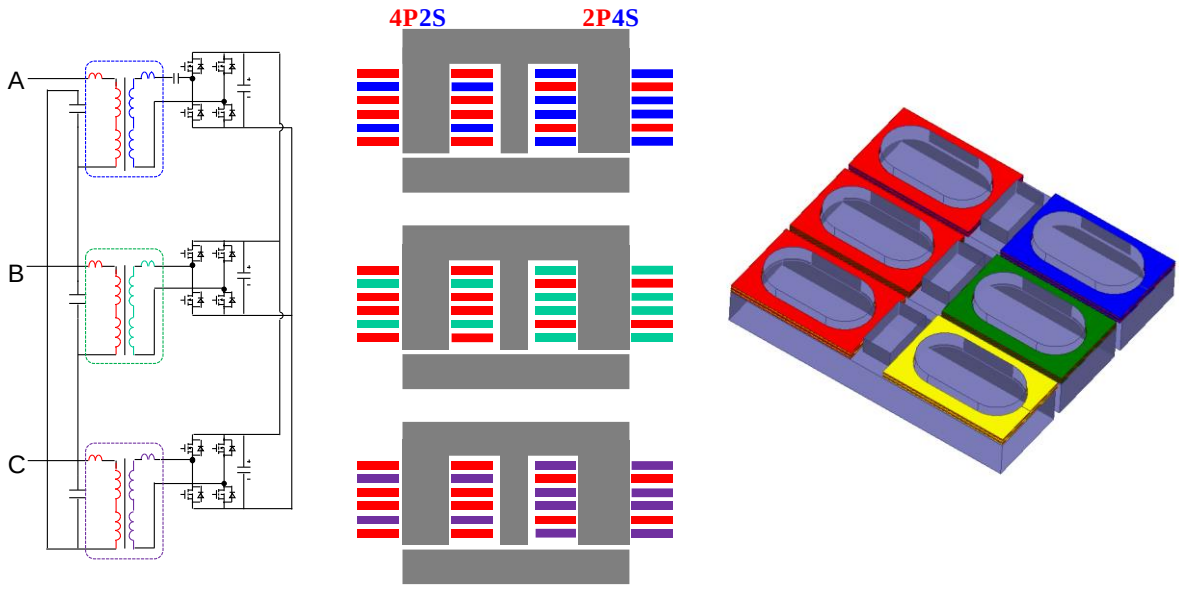


Fig. 5.16. 6-layer PCB winding transformer with integrated resonant inductors for three-phase CLLC resonant converter.

The magnetic reluctance model can be built based on the nine-post core structure, as shown in Fig. 5.17.

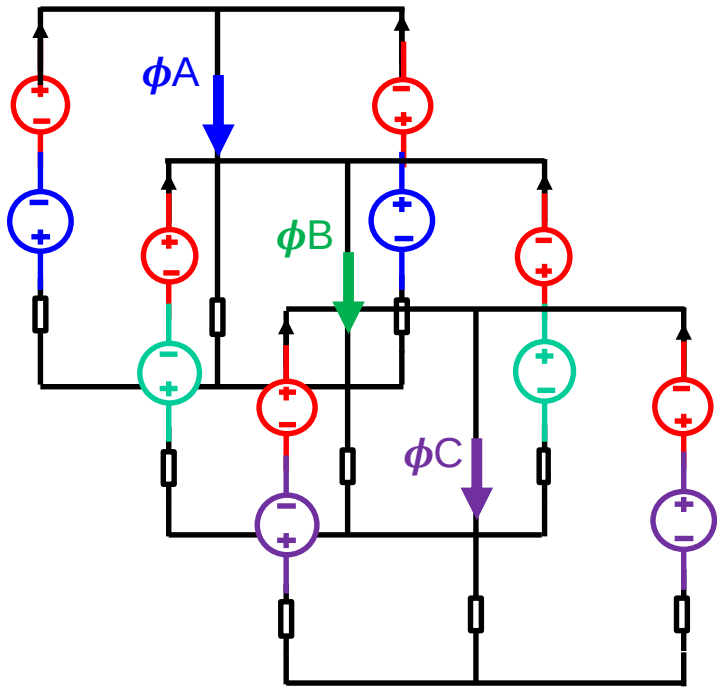


Fig. 5.17. Reluctance model of the three-phase discrete transformer.

By simply combining the top and bottom plates, the three single-phase transformers are further integrated into one magnetic component. However, this core structure is very complicated with totally nine posts, as shown in Fig. 5.18.

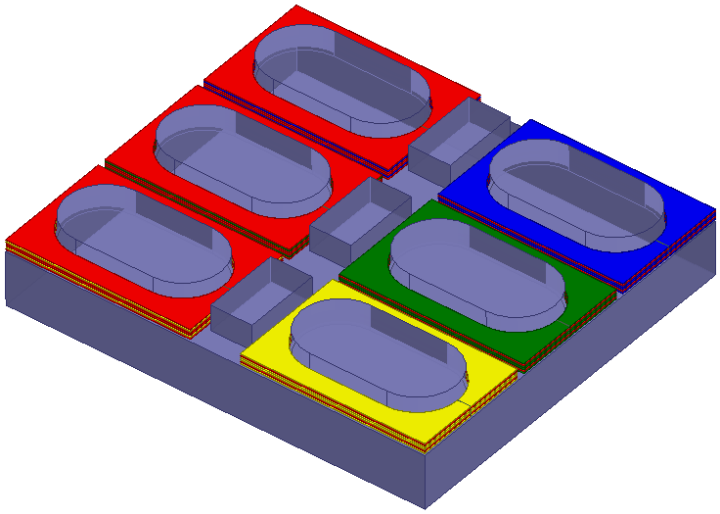


Fig. 5.18. Three-phase integrated magnetic with center posts.

At this time, the magnetic reluctance model becomes,

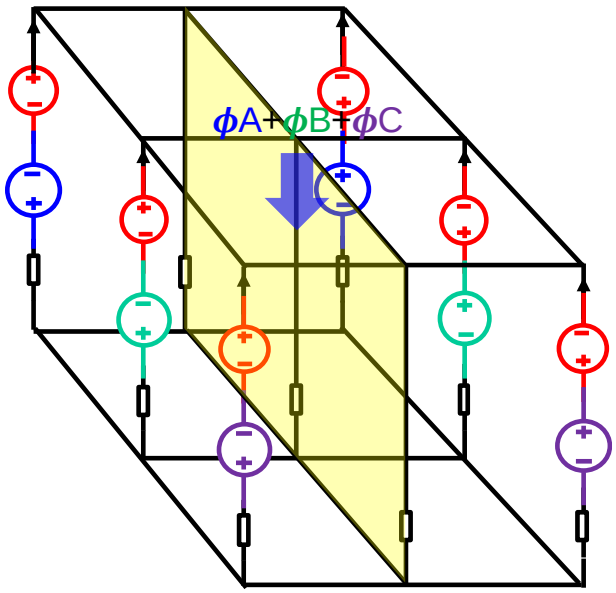


Fig. 5.19. Reluctance model of the three phase integrated transformer with center posts.

If we investigate the flux in the core, due to the 120° phase shift between each phase, the flux in the three center posts also have 120° phase shift, as shown in Fig. 5.20.

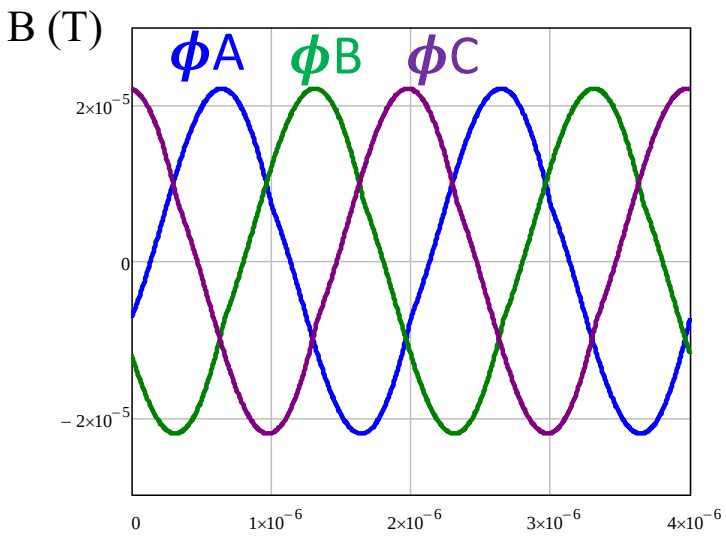


Fig. 5.20. Flux density in the three center posts.

As a result, the total flux in the center posts is cancelled out. This can be verified through 3D finite element analysis (FEA) simulation shown in Fig. 5.21. We can see that the flux in the three center posts is almost zero. Therefore, we can simplify the transformer structure by removing the three center posts.

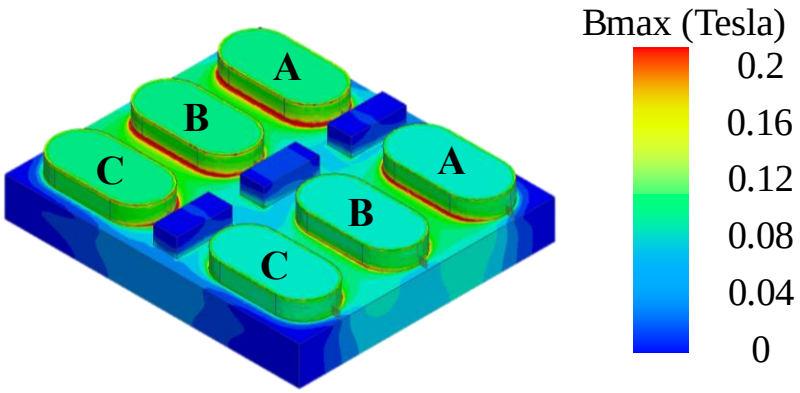


Fig. 5.21. 3D FEA simulation result of flux distribution.

Based on this transformer structure, a reluctance model can be built, as shown in Fig. 5.22. Here, two assumptions are made to simplify the model without losing accuracy.

1) The permeability of the core is much larger than one (permeability of the air).

2) Leakage flux in the air is very small and can be ignored.

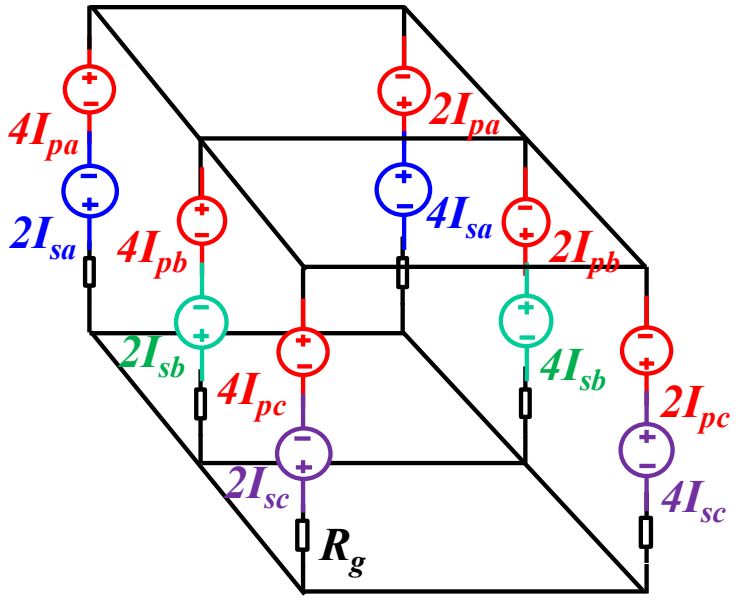


Fig. 5.22. Reluctance model of the proposed three phase transformer.

According to the reluctance model, we can get the following equations.

$$\begin{bmatrix} v_{ap} \\ v_{bp} \\ v_{cp} \\ v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \begin{bmatrix} L_1 & L_2 & L_2 & L_3 & L_4 & L_4 \\ L_2 & L_1 & L_2 & L_4 & L_3 & L_4 \\ L_2 & L_2 & L_1 & L_4 & L_4 & L_3 \\ L_3 & L_4 & L_4 & L_1 & L_2 & L_2 \\ L_4 & L_3 & L_4 & L_2 & L_1 & L_2 \\ L_4 & L_4 & L_3 & L_2 & L_2 & L_1 \end{bmatrix} \begin{bmatrix} \frac{di_{ap}}{dt} \\ \frac{di_{bp}}{dt} \\ \frac{di_{cp}}{dt} \\ \frac{di_{as}}{dt} \\ \frac{di_{bs}}{dt} \\ \frac{di_{cs}}{dt} \end{bmatrix} \tag{5.3}$$

Where,

$$L_1 = \frac{58}{3R_g}$$

$$L_2 = -\frac{2}{3R_g}$$

$$L_3 = -\frac{50}{3R_g}$$

$$L_4 = -\frac{2}{3R_g}$$

$$R_g = \frac{l_g}{\mu_0 A_e} \tag{5.4}$$

Where l_g is the air gap length and A_e is the core post cross section area.

The sum of primary resonant current is zero due to Δ-connected resonant capacitors. If we also assume that the sum of secondary resonant current is zero,

$$i_{ap} + i_{bp} + i_{cp} = 0$$

$$i_{as} + i_{bs} + i_{cs} = 0 \tag{5.5}$$

Then we have,

$$\begin{bmatrix} v_{ip} \\ v_{is} \end{bmatrix} = \begin{bmatrix} L_1 - L_2 & L_3 - L_4 \\ L_3 - L_4 & L_1 - L_2 \end{bmatrix} \begin{bmatrix} \frac{di_{ip}}{dt} \\ \frac{di_{is}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{20}{R_g} & -\frac{16}{R_g} \\ -\frac{16}{R_g} & \frac{20}{R_g} \end{bmatrix} \begin{bmatrix} \frac{di_{ip}}{dt} \\ \frac{di_{is}}{dt} \end{bmatrix} \tag{5.6}$$

Where $i = a, b, c$

It is clear that the three-phase integrated transformer is de-coupled into three single-phase transformers, and the equivalent turns ratio N, magnetizing inductance L_m, leakage inductance L_{kp} and L_{ks} for a transformer T-model are,

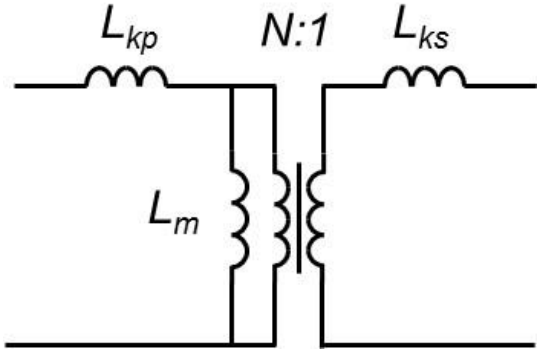


Fig. 5.23. Transformer T model.

$$N = 1 \qquad L_m = \frac{16}{R_g}$$

$$L_{kp} = L_{ks} = \frac{4}{R_g} \tag{5.7}$$

We can see that with this structure, the leakage inductance can also be controlled using the air gap and served as resonant inductors. In additional, we can benefit from the three phase integration for a smaller magnetic component size. However, compared with the single-phase transformer integration, magnetizing inductance and leakage inductance cannot be controlled separately due to the removal of center post. We can only get a fixed ratio between magnetizing inductance and leakage inductance.

In fact, the leakage inductance and magnetizing inductance value is related to the winding arrangement. If an 8-layer board is used, with the winding arrangement shown in Fig. 5.24.

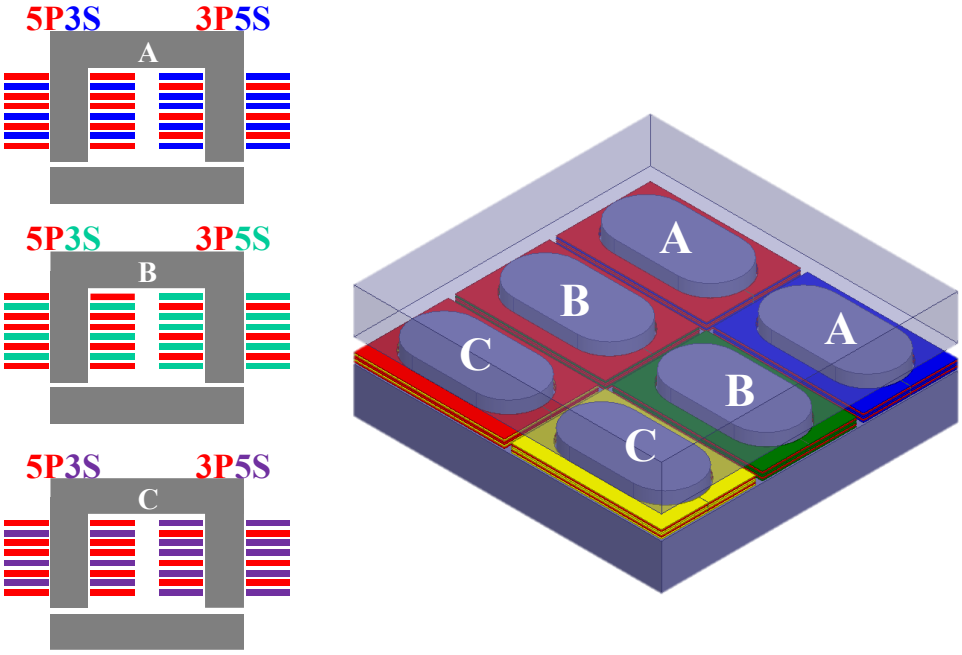


Fig. 5.24. Proposed three-phase integrated transformer with 8-layer PCB.

The leakage inductance and magnetizing inductance we can achieve is,

$$L_m = \frac{30}{R_g}$$

$$L_{kp} = L_{ks} = \frac{4}{R_g} \tag{5.8}$$

With the same amount of magnetizing inductance, the leakage inductance for the 8-layer board design is smaller than that of the 6-layer board design because of the different interleave structure.

In fact, the proposed magnetic structure has another way to implement, as show in Fig. 5.25.

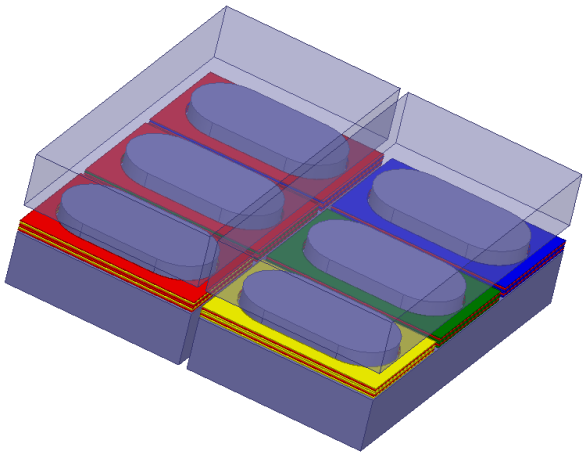


Fig. 5.25. Different way to implement the proposed three phase magnetic structure.

We can split the single core into two parts; each part is an EI core shape with three core posts. The corresponding reluctance mode is shown in Fig. 5.26 for a 6-layer design.

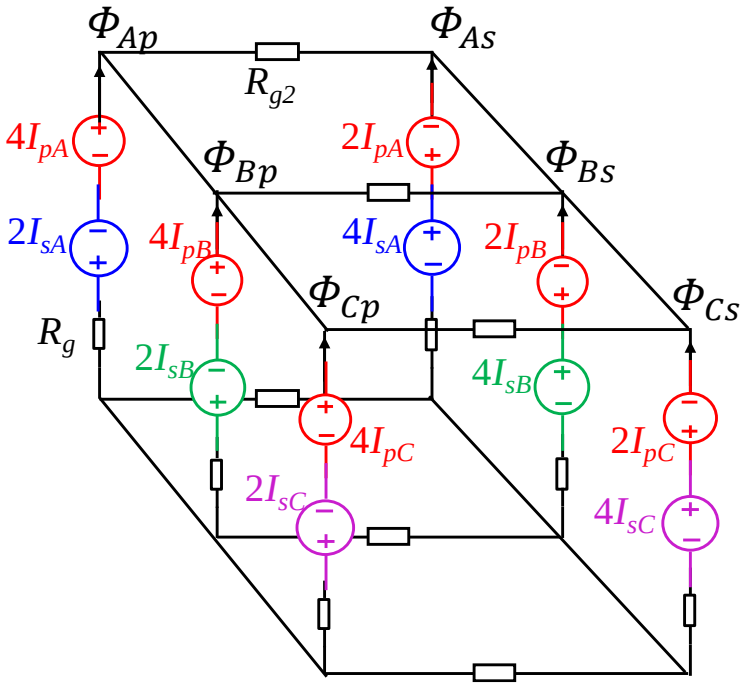


Fig. 5.26. Reluctance model of the two EI core implementation.

With this reluctance model, we can find the three-phase transformer matrix,

$$\begin{bmatrix} v_{ap} \\ v_{bp} \\ v_{cp} \\ v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \begin{bmatrix} L_1 & L_2 & L_2 & L_3 & L_4 & L_4 \\ L_2 & L_1 & L_2 & L_4 & L_3 & L_4 \\ L_2 & L_2 & L_1 & L_4 & L_4 & L_3 \\ L_3 & L_4 & L_4 & L_1 & L_2 & L_2 \\ L_4 & L_3 & L_4 & L_2 & L_1 & L_2 \\ L_4 & L_4 & L_3 & L_2 & L_2 & L_1 \end{bmatrix} \begin{bmatrix} \frac{di_{ap}}{dt} \\ \frac{di_{bp}}{dt} \\ \frac{di_{cp}}{dt} \\ \frac{di_{as}}{dt} \\ \frac{di_{bs}}{dt} \\ \frac{di_{cs}}{dt} \end{bmatrix} \tag{5.9}$$

Where,

$$L_1 = \frac{4(29R_g+30R_{g2})}{3R_g(2R_g+3R_{g2})}$$

$$L_2 = -\frac{4(R_g+15R_{g2})}{3R_g(2R_g+3R_{g2})}$$

$$L_3 = -\frac{4(25R_g+24R_{g2})}{3R_g(2R_g+3R_{g2})}$$

$$L_4 = -\frac{4(R_g-12R_{g2})}{3R_g(2R_g+3R_{g2})}$$

$$R_g = \frac{l_g}{\mu_0 A_e}$$

$$R_{g2} = \frac{l_{g2}}{\mu_0 A_{e2}} \tag{5.10}$$

Where l_{g2} is the air gap between left EI core and right EI core; A_{e2} is the cross section area of this air gap.

With R_{g2} = 0, Eq. (5.10) simplifies to Eq. (5.4).

We can see that even if we split the one large core into two smaller EI cores, the equivalent magnetizing inductance and leakage inductance for each phase stay the same.

5.4 Third order harmonic impact

From the proposed structure shown in Fig. 5.13, we can see that due to the primary side Δ-connection, the sum of the primary side current is zero. Therefore, there is no third order harmonic in the primary side. However, for the secondary side, there is no such connection and as a result, third order harmonic may exist.

If we define,

$$i_{as} + i_{bs} + i_{cs} = i_{3rd} \tag{5.11}$$

From Eq. (5.9), we have,

$$\begin{bmatrix} v_{ip} \\ v_{is} \end{bmatrix} = \begin{bmatrix} L_1 - L_2 & L_3 - L_4 & L_4 \\ L_3 - L_4 & L_1 - L_2 & L_2 \end{bmatrix} \begin{bmatrix} \frac{di_{ip}}{dt} \\ \frac{di_{is}}{dt} \\ \frac{di_{3rd}}{dt} \end{bmatrix} \tag{5.12}$$

If we consider the sum of three phase voltage on both primary side and secondary side, we have,

$$v_{Ap} + v_{Bp} + v_{Cp} = (L_1 - L_2)\frac{d(i_{Ap}+i_{Bp}+i_{Cp})}{dt} + (L_3 - L_4)\frac{d(i_{As}+i_{Bs}+i_{Cs})}{dt} + 3L_4\frac{di_{3rd}}{dt} \tag{5.13}$$

$$v_{As} + v_{Bs} + v_{Cs} = (L_3 - L_4)\frac{d(i_{Ap}+i_{Bp}+i_{Cp})}{dt} + (L_1 - L_2)\frac{d(i_{As}+i_{Bs}+i_{Cs})}{dt} + 3L_2\frac{di_{3rd}}{dt} \tag{5.14}$$

For the proposed structure, the sum of primary side current is zero,

$$i_{Ap} + i_{Bp} + i_{Cp} = 0 \tag{5.15}$$

Then we have,

$$v_{Ap} + v_{Bp} + v_{Cp} = (L_3 + 2L_4)\frac{di_{3rd}}{dt} \tag{5.16}$$

$$v_{As} + v_{Bs} + v_{Cs} = (L_1 + 2L_2)\frac{di_{3rd}}{dt} \tag{5.17}$$

Therefore, we can define,

$$L_1 + 2L_2 = L_{3rd} \tag{5.18}$$

From Eq. (5.16) and Eq. (5.17), we can find out that the third order harmonic current is determined by L_{3rd}. If the magnetic structure shown in Fig. 5.25 is used, from Eq. (5.10), it is clear that both R_g and R_{g2} determine L_{3rd}, as shown in Eq. (5.19)

$$L_{3rd} = \frac{36}{2R_g + 3R_{g2}} \tag{5.19}$$

The largest L_{3rd} we can achieve is,

$$L_{3rd-max} = \frac{18}{R_g} \tag{5.20}$$

And it is achieved at,

$$R_{g2} = 0 \tag{5.21}$$

The relationship between L_{3rd} and R_{g2} is shown in Fig. 5.27.

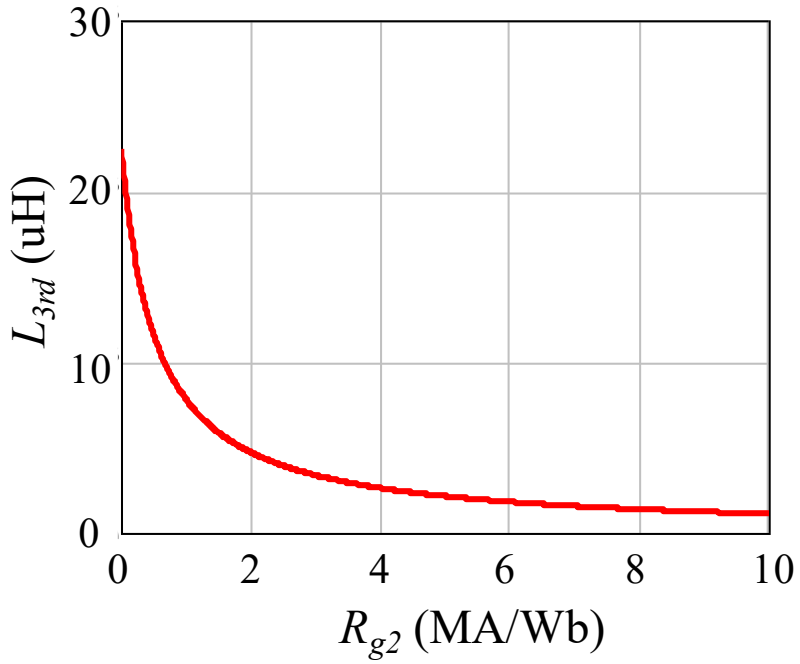


Fig. 5.27. The relationship between R_{g2} and L_{3rd}.

If the cross section area A_{e2} is 1200mm^2, we can find the relation between l_{g2} and L_{3rd}, as shown in Fig. 5.28.

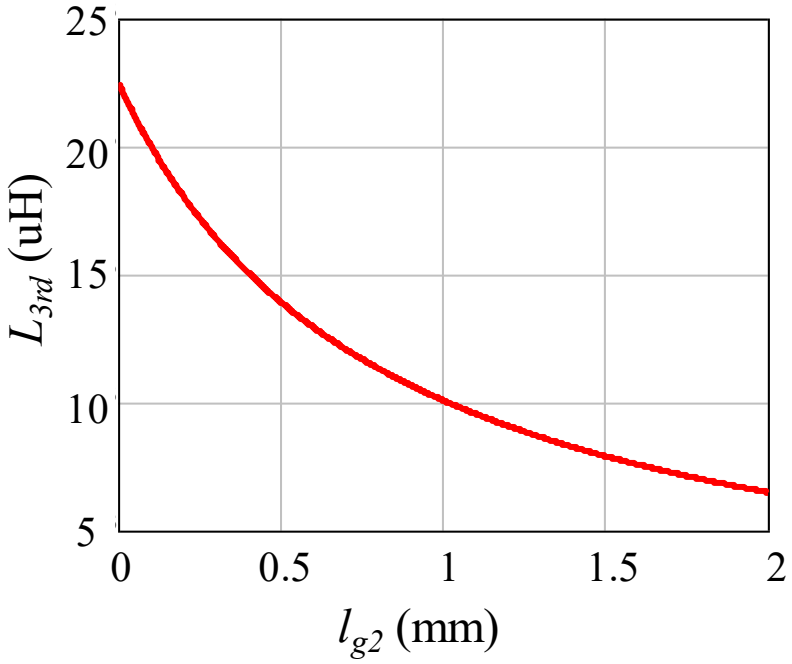


Fig. 5.28. The relationship between l_{g2} and L_{3rd}.

A simulation is conducted to evaluate how the air gap length l_{g2} impacts the third order harmonic, the results are shown in Fig. 5.29.

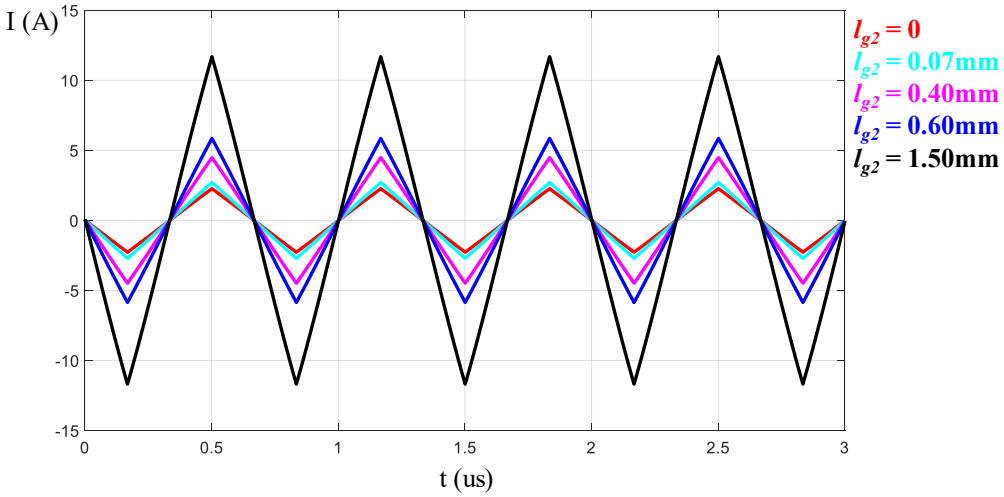


Fig. 5.29. Impact of Reluctance R_{g2} on third order harmonic.

We can see that when we increase the distance between left EI core and right EI core, the third order harmonic becomes larger.

The third order harmonic also affects the RMS current of both primary side and secondary side. The normalized (normalized with l_{g2} = 0 mm) RMS current of both primary side current and secondary side current are shown in Fig. 5.30.

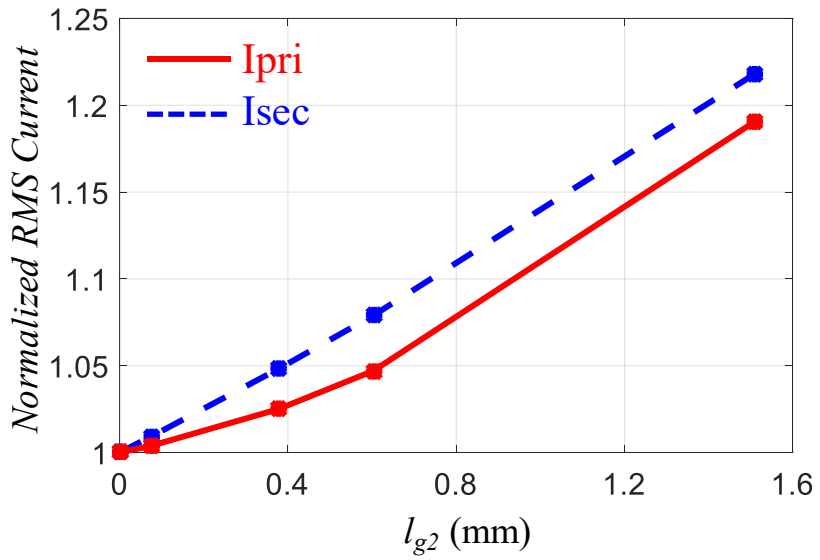


Fig. 5.30. Normalized RMS current of primary side (red solid line) and secondary side (blue dash line).

The impacts of third order harmonic on core loss is also shown in Fig. 5.31 (normalized with l_{g2} = 0 mm).

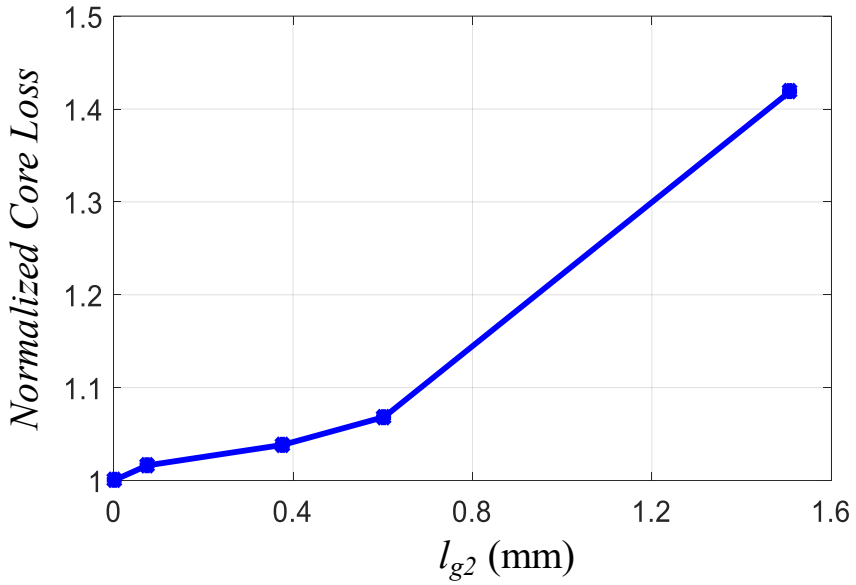


Fig. 5.31. Normalized core loss.

From the above figures, we can see that with larger air gap between left EI core and right EI core, the RMS value of both primary side current and secondary side current are increasing. As a result, the conduction loss of device and transformer winding will increase. In addition, larger third order harmonic results in larger core loss.

5.5 Three phase transformer loss model and optimization

In order to get the lowest loss from the transformer, a transformer loss model is built as well as an optimization procedure.

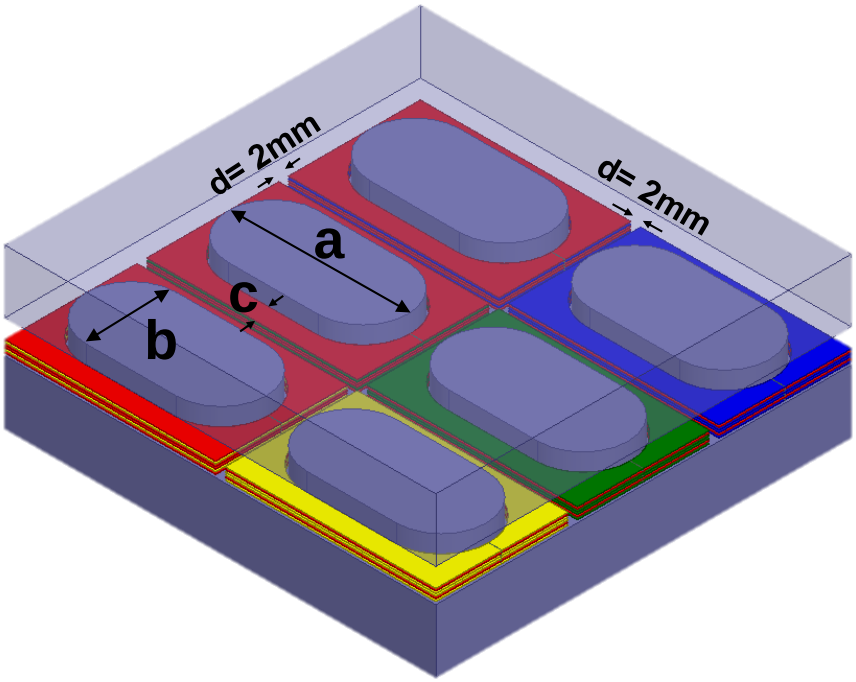


Fig. 5.32. Proposed three-phase transformer structure with integrated resonant inductors.

(1) Winding loss

The dimensions of the transformer are shown in Fig. 5.32. Here, a round shape core post is used to reduce the average winding length and the distance between windings is fixed at 2 mm. As a result, the transformer only has three design parameters, core post width *a*, length *b* and winding width *c*.

The winding loss is calculated using FEA simulation, and it is a function of the three design parameters, as shown in Eq. (5.22)

$$P_{winding} = f_w(a, b, c) \tag{5.22}$$

(2) Core loss

First, appropriate core material is selected based on core loss density under 500 kHz switching frequency, as shown in Fig. 5.33.

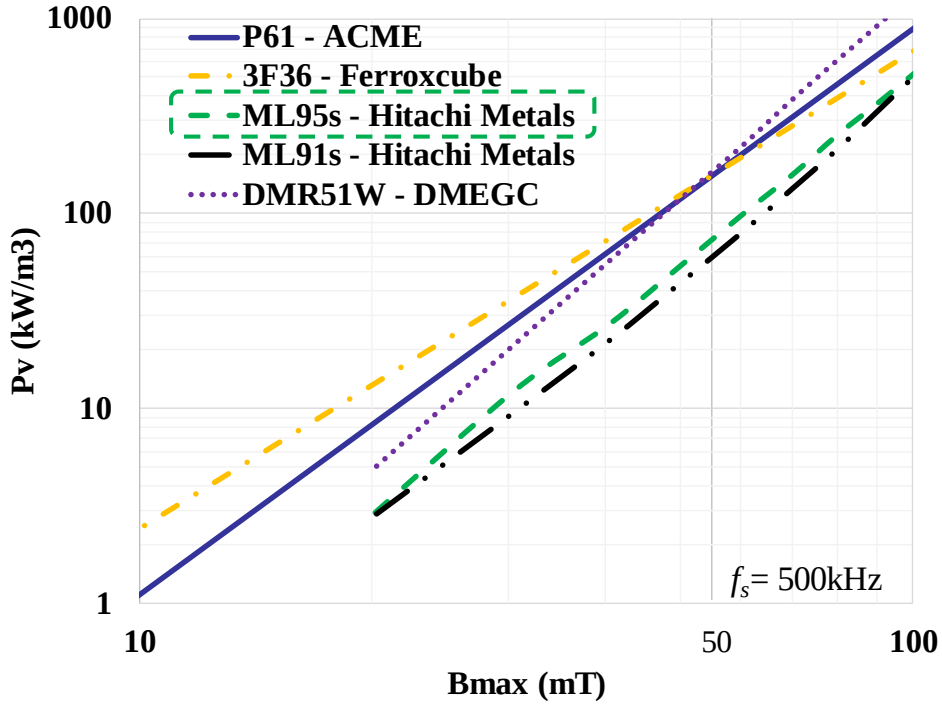


Fig. 5.33. Core loss density comparison between different core materials.

From this comparison, we can see that material ML95s from Hitachi Metals is the best in terms of loss.

For core loss calculation, conventional Steinmetz Equation (SE) is only good for sinusoid excitation. When the waveform shape changes, it becomes inaccurate.

In [9], a Modified Steinmetz Equation (MSE) is proposed to calculate core loss under arbitrary current input and in [10], an equivalent elliptical loop (EEL) method is proposed to calculated core loss also under arbitrary current input. The difference between MSE and EEL is that MSE is still based on frequency domain while EEL is based on time domain.

A comparison between MSE and EEL is conducted with the proposed transformer structure, and the results are shown in Fig. 5.34.

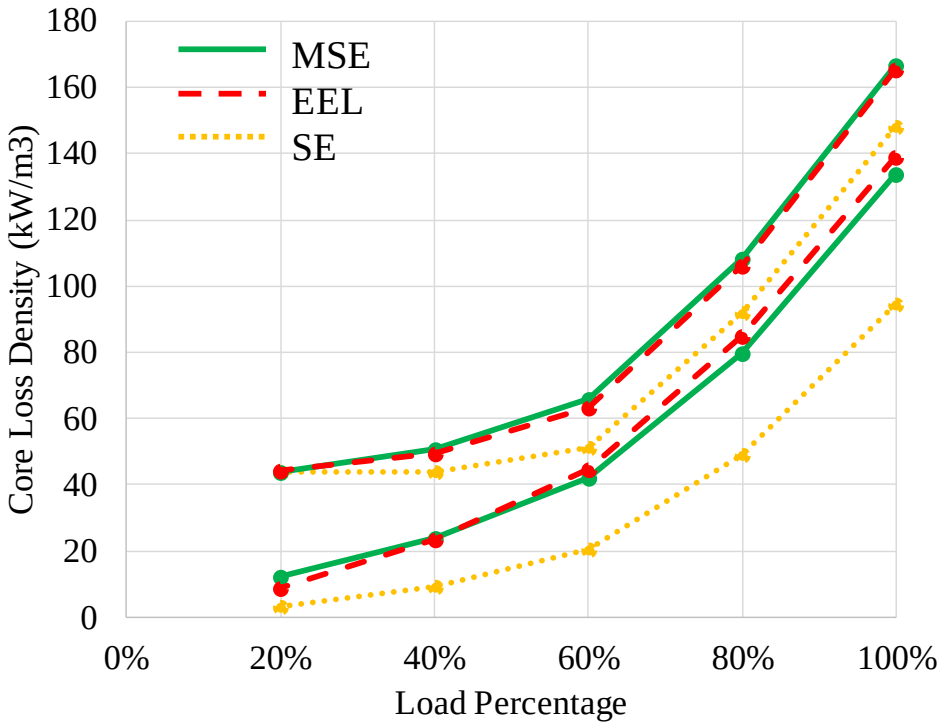


Fig. 5.34. Comparison between MSE, EEL and SE for core loss density calculation.

We can see that both MSE and EEL has the same core loss density predictions while SE has a much larger deviation. As a result, EEL is used for the core loss calculation for the proposed three-phase integrated magnetic structure.

According to the reluctance model, flux inside part of the core can be calculated as shown in Eq. (5.23).

$$\Phi_A(t) = \frac{11i_{ap}(t) - i_{bp}(t) - i_{cp}(t) - 7i_{as}(t) - i_{bs}(t) - i_{cs}(t)}{3R_g}$$

$$\Phi_B(t) = \frac{11i_{bp}(t) - i_{ap}(t) - i_{cp}(t) - 7i_{bs}(t) - i_{as}(t) - i_{cs}(t)}{3R_g}$$

$$\Phi_C(t) = \frac{11i_{cp}(t) - i_{bp}(t) - i_{ap}(t) - 7i_{cs}(t) - i_{bs}(t) - i_{as}(t)}{3R_g} \quad (5.23)$$

Where R_g is the reluctance of the air gap.

$$R_g = \frac{l_g}{\mu_r \mu_0 A_e} \quad (5.24)$$

l_g is the air gap length and A_e is the cross-section area of the core post.

So the flux density in each part of the core is,

$$B_A(t) = \frac{11i_{ap}(t) - i_{bp}(t) - i_{cp}(t) - 7i_{as}(t) - i_{bs}(t) - i_{cs}(t)}{3R_g A_e}$$

$$B_B(t) = \frac{11i_{bp}(t) - i_{ap}(t) - i_{cp}(t) - 7i_{bs}(t) - i_{as}(t) - i_{cs}(t)}{3R_g A_e}$$

$$B_C(t) = \frac{11i_{cp}(t) - i_{bp}(t) - i_{ap}(t) - 7i_{cs}(t) - i_{bs}(t) - i_{as}(t)}{3R_g A_e} \quad (5.25)$$

With the expression of flux density, core loss density can be calculated based on EEL, and the total core loss can be calculated based on the following equation.

$$P_{core}(a, b, c) = P_v(a, b)Vol(a, b, c) \quad (5.26)$$

Where P_v is the core loss density and *Vol* is the corresponding core volume.

However, with three parameters, it is hard to do the 3D optimization. In order to reduce the number of parameters, we can fix the transformer footprint first.

The transformer footprint is calculated by

$$footprint = (6c + 3b + 2d)(2a + 4c + d) \quad (5.27)$$

Where *d* is the fixed 2 mm distance between windings. By giving 7500 mm^2 footprint, the parameter *c* can be expressed by *a* and *b*, and the transformer total loss will only be related to *a* and *b*.

As a result, a 3D optimization curve can be drawn, as shown in Fig. 5.35 (a). The corresponding transformer loss contour is shown in Fig. 5.35 (b).

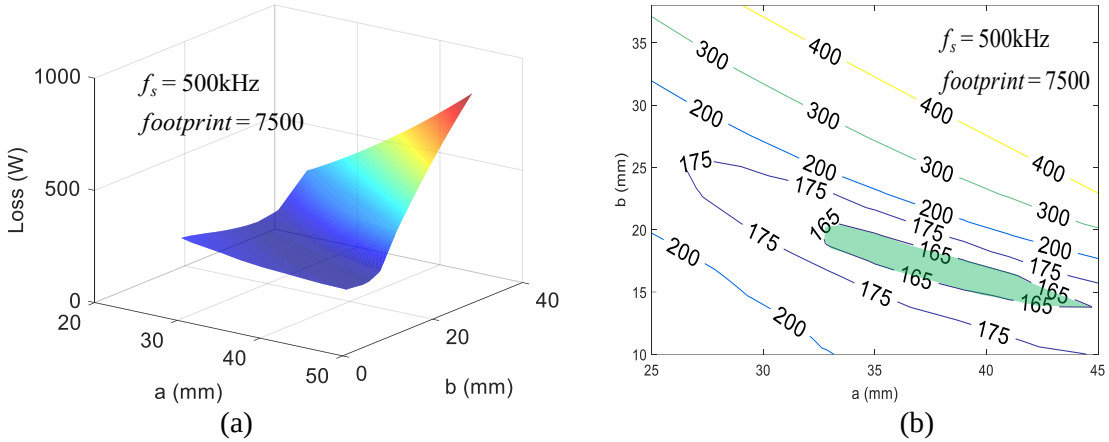


Fig. 5.35. (a) 3D loss curve and (b) corresponding loss contour.

From the 3D curve and contour, we can find the lowest loss point, where the loss is around 162 W.

Using the same procedure, we can find the minimum loss point under different footprint, as shown in Fig. 5.36. By increasing the transformer footprint, we can further reduce the total transformer related loss. So it is a tradeoff between efficiency and power density.

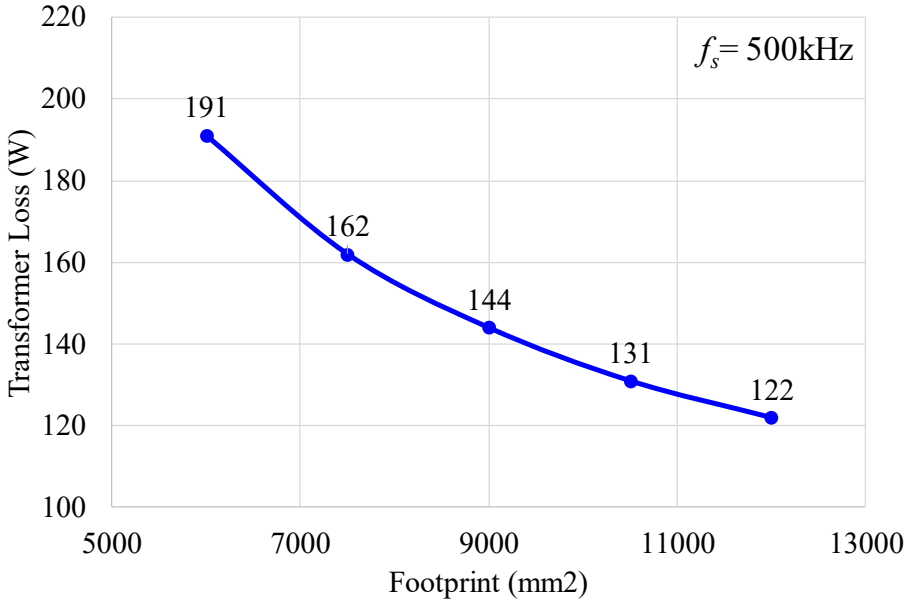


Fig. 5.36. Transformer loss vs. transformer footprint.

Also, 3D FEA simulation results of the current distribution is shown in Fig. 5.37. With the proposed integration method, interleaving between the primary winding and the secondary windings is maintained and the current is evenly distributed across the windings.

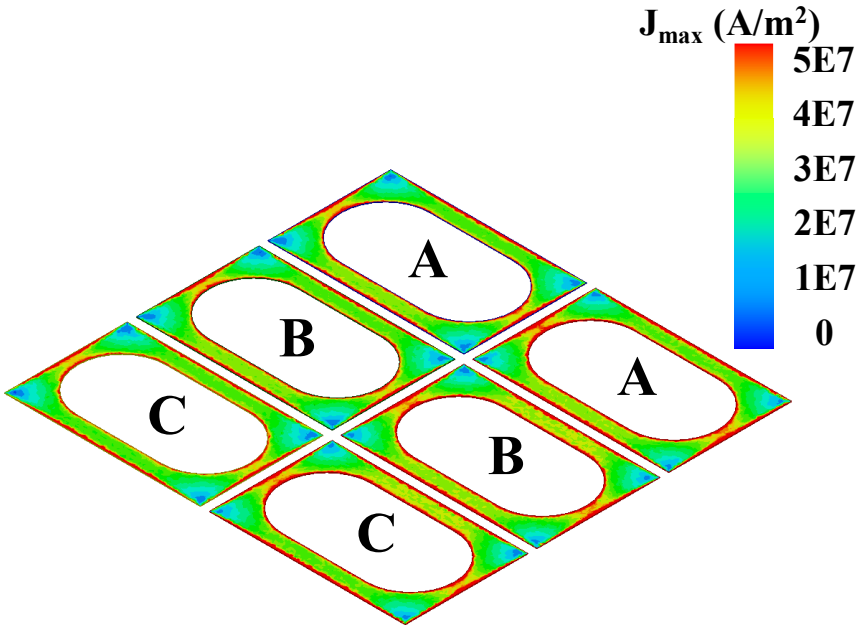


Fig. 5.37. Current distribution in simulation.

5.6 Light load efficiency improvement by phase shading

(1) Circuit operation under phase shading mode

In multi-phase Buck converter, phase shading is a very good way to improve the light load efficiency. By shutting down different number of phases, the load of operating phase can be maintained at the optimal level, which helps to improve the system efficiency.

For three-phase resonant converter, the same concept can be applied.

The circuit can operate with two phases by simply shutting down the driving signal of phase C, as shown in Fig. 5.38.

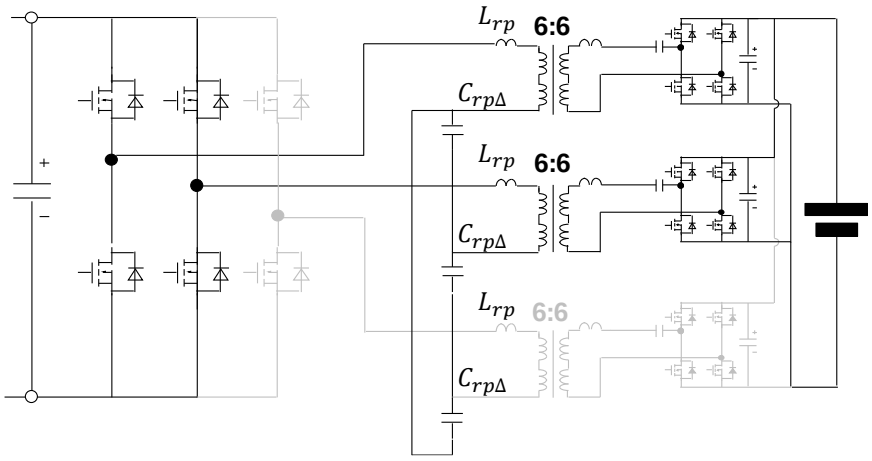


Fig. 5.38. Two-phase operation with Phase C shutting down.

By redrawing the circuit, we can get Fig. 5.39. This figure shows very clearly how the converter works with two phases. The two phase resonant inductors are in series while the resonant capacitor is in a parallel and series configuration.

After phase shading, the primary side is configured to a full bridge structure while the secondary side is still full bridge. However, at this time, the two phase transformers are also in series on the primary side, and as a result, the equivalent gain of the converter is still 2:1.

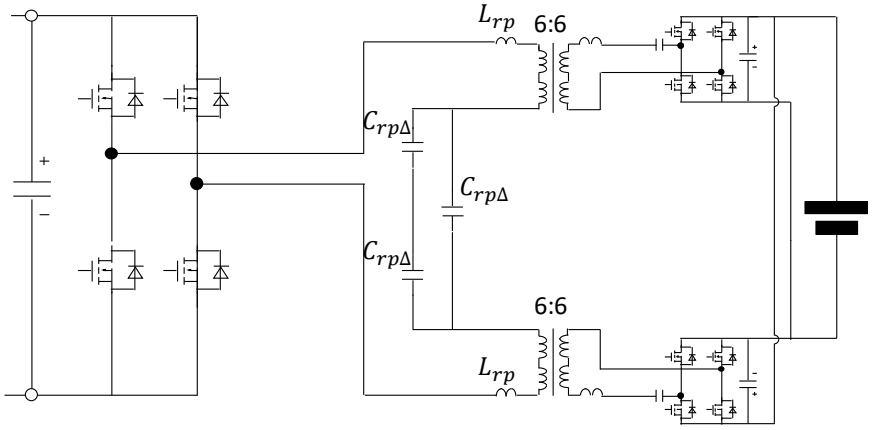


Fig. 5.39. Two-phase operation (redraw).

For three-phase operation, we have,

$$f_o = \frac{1}{2\pi\sqrt{L_{rp}C_{rp}}} = \frac{1}{2\pi\sqrt{3L_{rp}C_{rp\Delta}}} \tag{5.28}$$

Here we have the formation change between Y-connection and Δ-connection.

$$C_{rp} = 3C_{rp\Delta} \tag{5.29}$$

After changing to two-phase operation, the primary side is in a full bridge configuration, and the equivalent resonant inductor and resonant capacitor are,

$$L_r{}' = 2L_{rp}$$

$$C_r{}' = \frac{3}{2}C_{rp\Delta} \tag{5.30}$$

So the equivalent resonant frequency is,

$$f_o = \frac{1}{2\pi\sqrt{L_r{}'C_r{}'}} = \frac{1}{2\pi\sqrt{3L_{rp}C_{rp\Delta}}} \tag{5.31}$$

It is clear that the resonant frequency stays the same when changing from three-phase operation to two-phase operation.

(2) Magnetic analysis under phase shading mode.

Under three-phase operation, we have the assumption that,

$$i_{ap} + i_{bp} + i_{cp} = 0$$

$$i_{as} + i_{bs} + i_{cs} = 0 \tag{5.32}$$

However, under phase shading mode, there is no current flowing through phase C. If we ignore the common mode part, we can still have,

$$i_{ap} + i_{bp} = 0$$

$$i_{as} + i_{bs} = 0$$

$$i_{cp} = 0$$

$$i_{cs} = 0 \tag{5.33}$$

With the same inductance matrix,

$$\begin{bmatrix} v_{ap} \\ v_{bp} \\ v_{cp} \\ v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \begin{bmatrix} L_1 & L_2 & L_2 & L_3 & L_4 & L_4 \\ L_2 & L_1 & L_2 & L_4 & L_3 & L_4 \\ L_2 & L_2 & L_1 & L_4 & L_4 & L_3 \\ L_3 & L_4 & L_4 & L_1 & L_2 & L_2 \\ L_4 & L_3 & L_4 & L_2 & L_1 & L_2 \\ L_4 & L_4 & L_3 & L_2 & L_2 & L_1 \end{bmatrix} \begin{bmatrix} \frac{di_{ap}}{dt} \\ \frac{di_{bp}}{dt} \\ \frac{di_{cp}}{dt} \\ \frac{di_{as}}{dt} \\ \frac{di_{bs}}{dt} \\ \frac{di_{cs}}{dt} \end{bmatrix} \tag{5.34}$$

We still have the equivalent discrete magnetic in each phase,

$$\begin{bmatrix} v_{ip} \\ v_{is} \end{bmatrix} = \begin{bmatrix} L_1 - L_2 & L_3 - L_4 \\ L_3 - L_4 & L_1 - L_2 \end{bmatrix} \begin{bmatrix} \frac{di_{ip}}{dt} \\ \frac{di_{is}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{20}{R_g} & -\frac{16}{R_g} \\ -\frac{16}{R_g} & \frac{20}{R_g} \end{bmatrix} \begin{bmatrix} \frac{di_{ip}}{dt} \\ \frac{di_{is}}{dt} \end{bmatrix} \tag{5.35}$$

Which means, under phase shading mode, the resonant inductor and magnetizing inductance stay the same.

The reluctance model under phase shading mode is shown in Fig. 5.40.

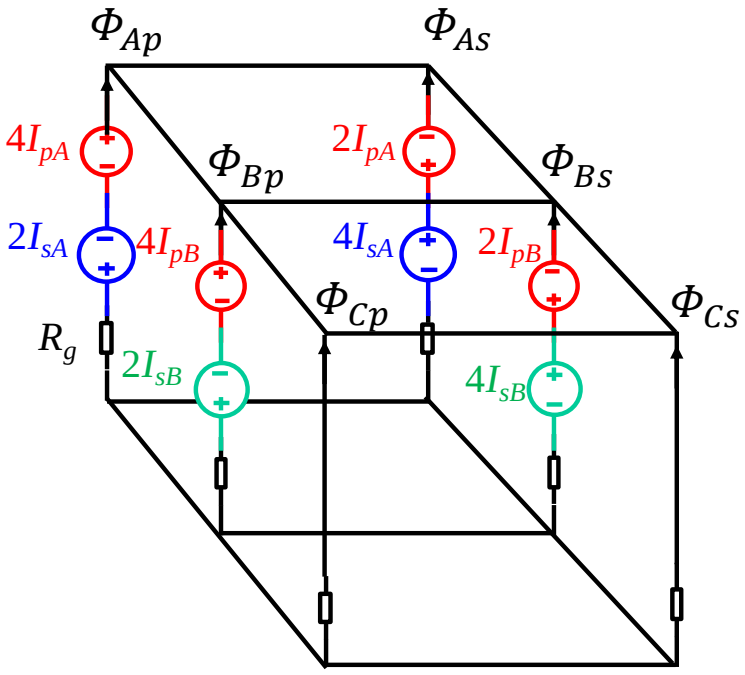


Fig. 5.40. Reluctance model of the three-phase integrated magnetics under phase shading mode.

With the excitation shown in Fig. 5.41, the flux inside each core post can be calculated, as shown in Fig. 5.42. From Fig. 5.42, we can see that since there is no excitation in phase C, there is also no flux in that phase's core posts.

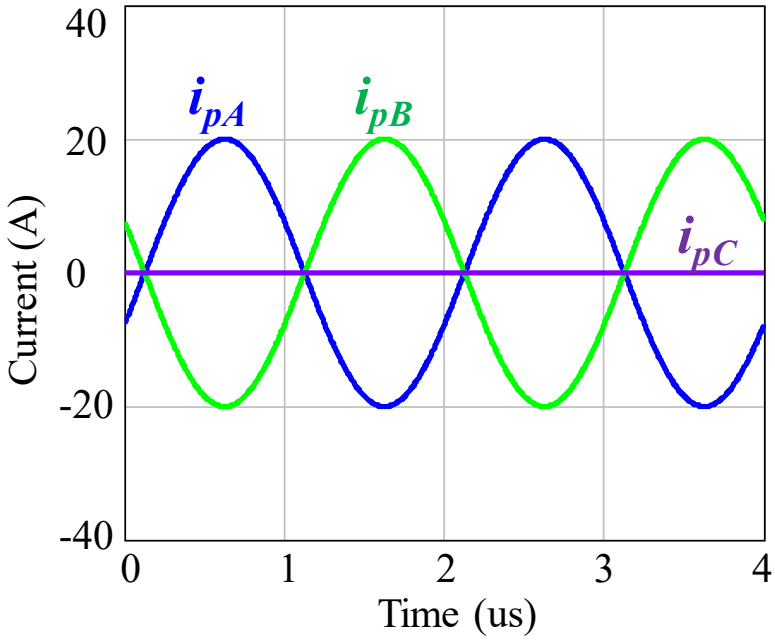


Fig. 5.41. Three phase current under phase shading mode.

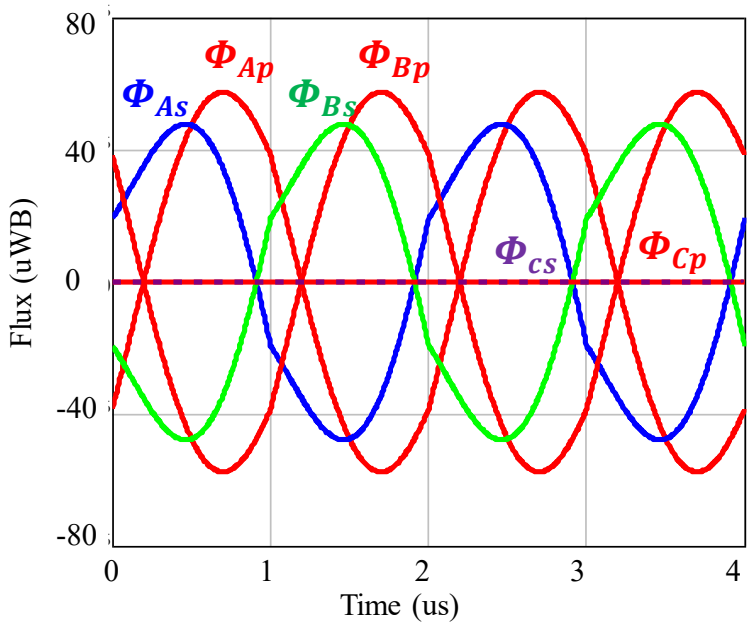
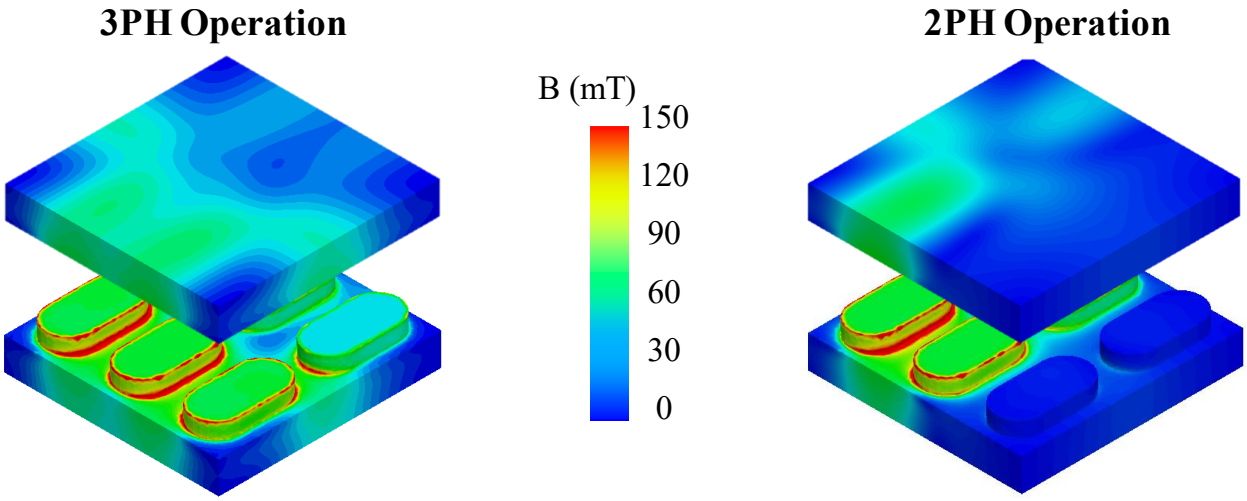


Fig. 5.42. Flux in each core post under phase shading mode.

Loss reduction, like switching loss, driving loss, under phase shading mode is very straightforward. For core loss reduction, 3D FEA simulation is conducted with 20% load (2500 W), and the results are shown in Fig. 5.43.



(a) Three-phase operation (b) Two-phase operation

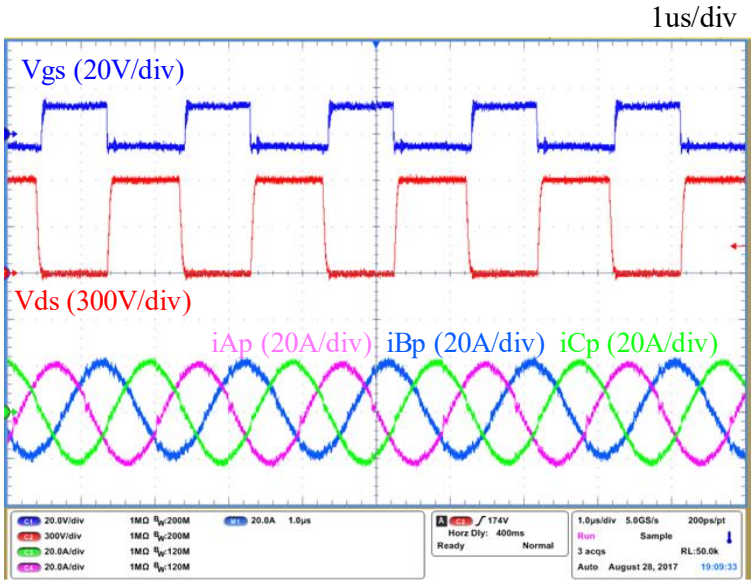
Fig. 5.43. Core loss simulation results with (a) three-phase and (b) two-phase operation.

For three-phase operation under 20% load, the core loss is 16.3 W while for two-phase operation, the core loss is reduced to 10.9 W.

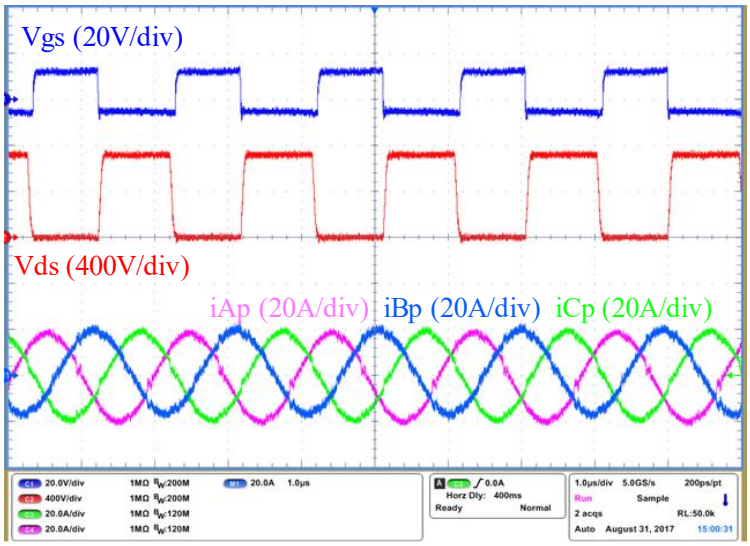
5.7 Experimental verification

(1) Forward operation

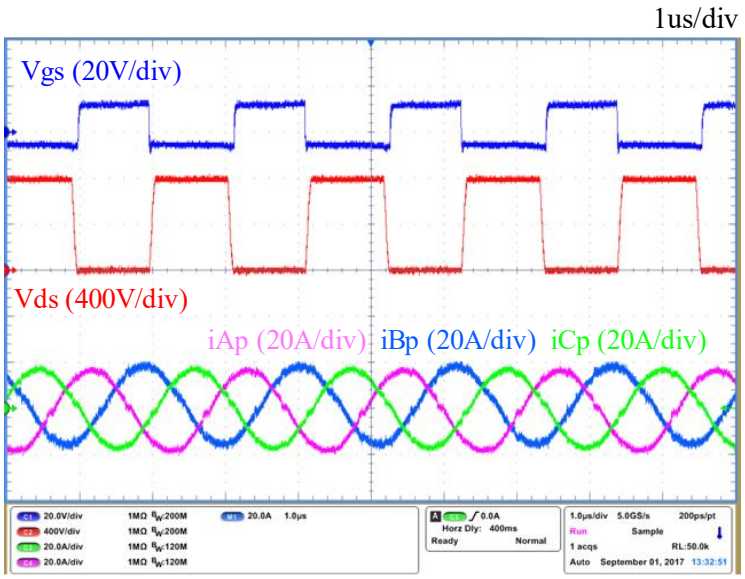
The three-phase CLLC resonant converter under forward operation is shown in Fig. 5.44 under different input output voltage and full load condition.



(a) 600V input 300V/41A output



(b) 700V input 350V/35A output

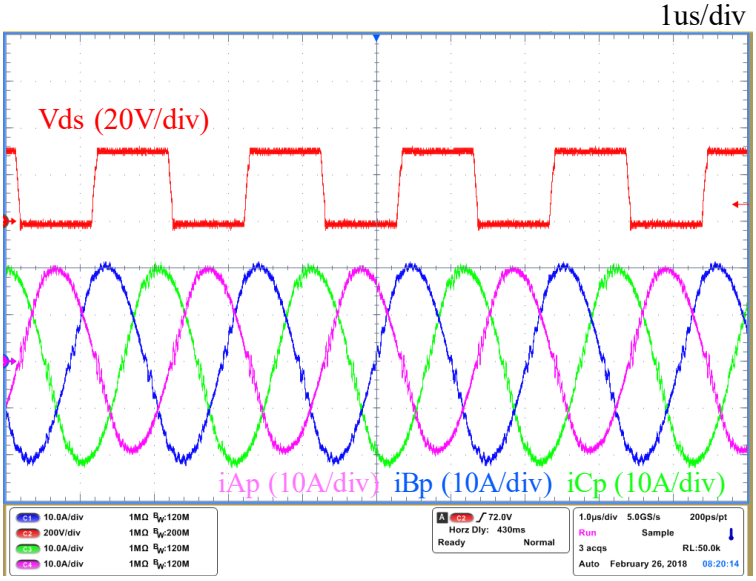


(c) 800V input 400V/31A output

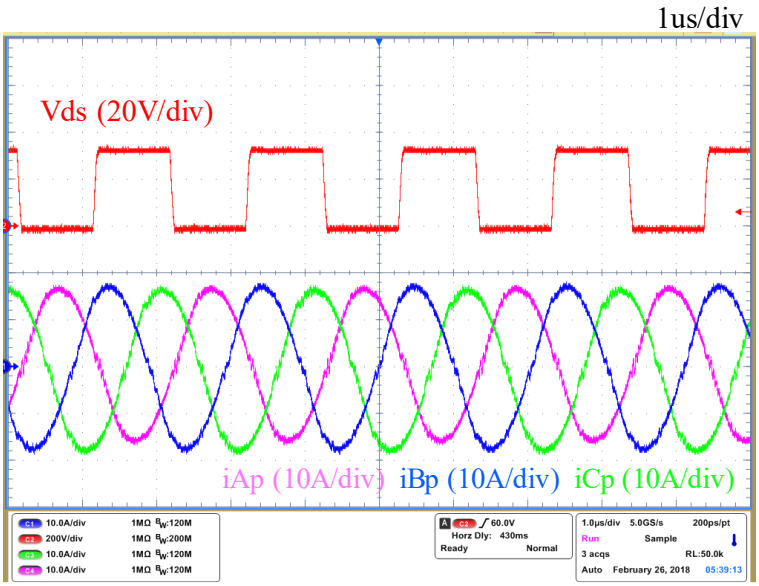
Fig. 5.44. Experimental results of forward operation at full load condition.

(2) Reverse operation

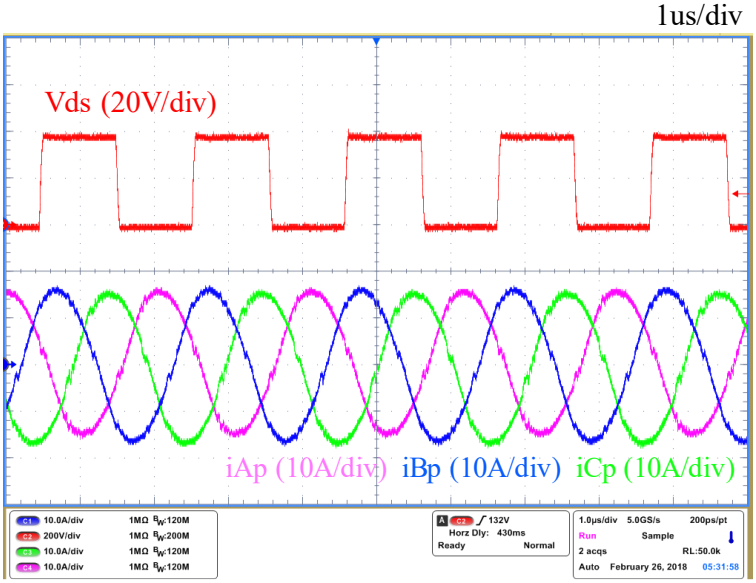
The three-phase CLLC resonant converter under forward operation is shown in Fig. 5.45 under different input output voltage and full load condition.



(a) 300V input 600V/20.5A output.



(b) 350V input 700V/17.5A output.



(c) 400V input 800V/15.5A output.

Fig. 5.45. Experimental results of reverse operation at full load condition.

(3) Third order harmonic test

The tested third order harmonic under 600V input voltage is shown in Fig. 5.46. We can see that the peak to peak is around 4A, which is what we predicted in the simulation (and calculation) (Fig. 5.29, l_{g2} = 0).

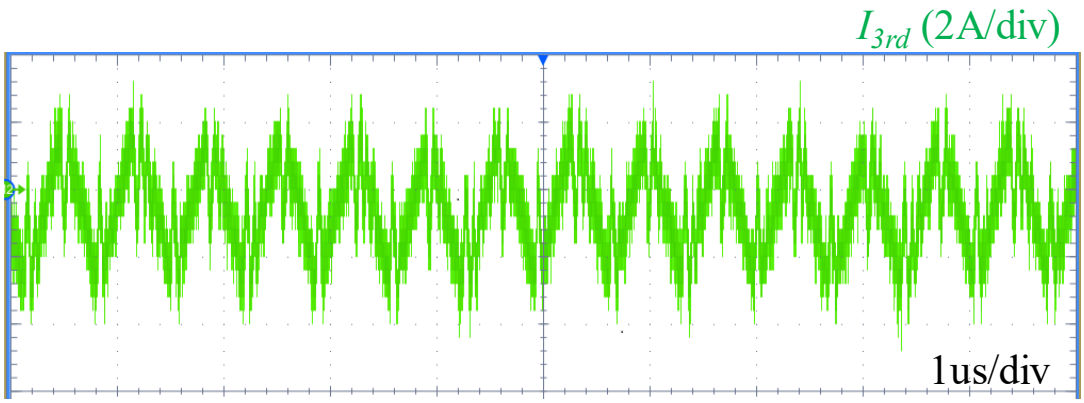
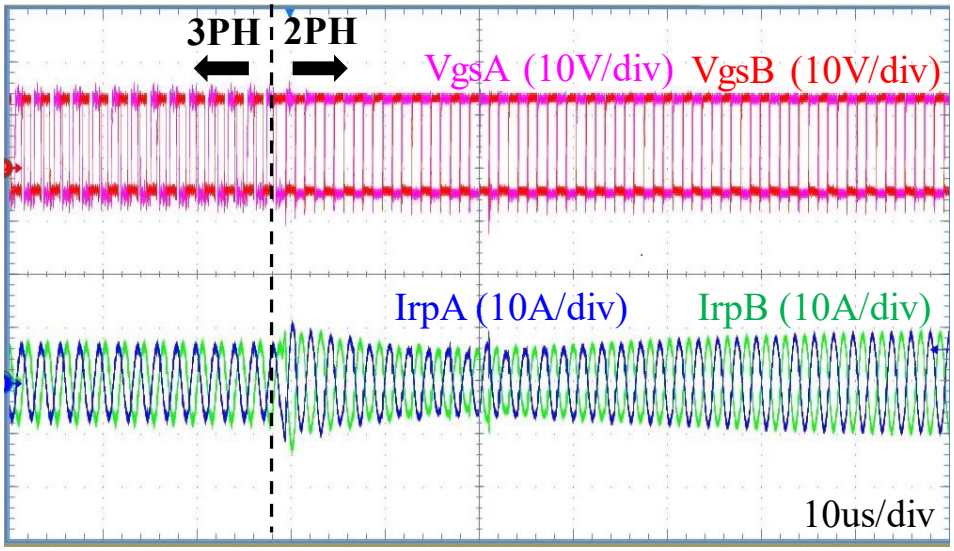


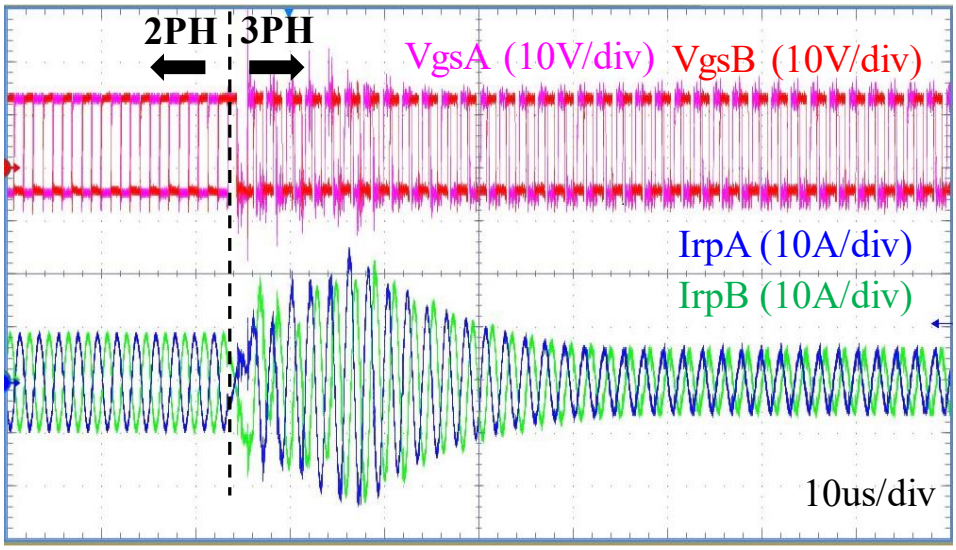
Fig. 5.46. Tested third order harmonic on secondary side under 600V input voltage.

(4) Phase shading operation

Under light load condition, the converter will change from normal operation to phase shading mode, and the transient waveform is shown in Fig. 5.47.



(a) transient from three-phase operation to two-phase operation.



(b) Transient from two-phase operation to three-phase operation

Fig. 5.47. Transient performance of phase shading operation under light load condition.

From Fig. 5.47, we can see that from normal operation to phase shading mode, the transient can be very smooth and fast. There is only 2A overshoot during the transient and the system is settled down within 40 us (20 switching cycles).

However, for transient from phase shading mode to normal operation mode, the overshoot is much larger. 10A overshoot is observed during the transient and the settling time is around 35 us (17 switching cycles).

(5) Efficiency testing results

The tested efficiency of the three-phase CLLC resonant converter for forward operation is shown in Fig. 5.48 with different input and output voltage. The peak efficiency achieved is around 98.2%. For input voltage between 600V-800V, the peak efficiency is always above 98%. Under full load condition, the efficiency is around 98% under 800V input voltage while under 600V input voltage, due to the much larger current, the efficiency drops to 97%.

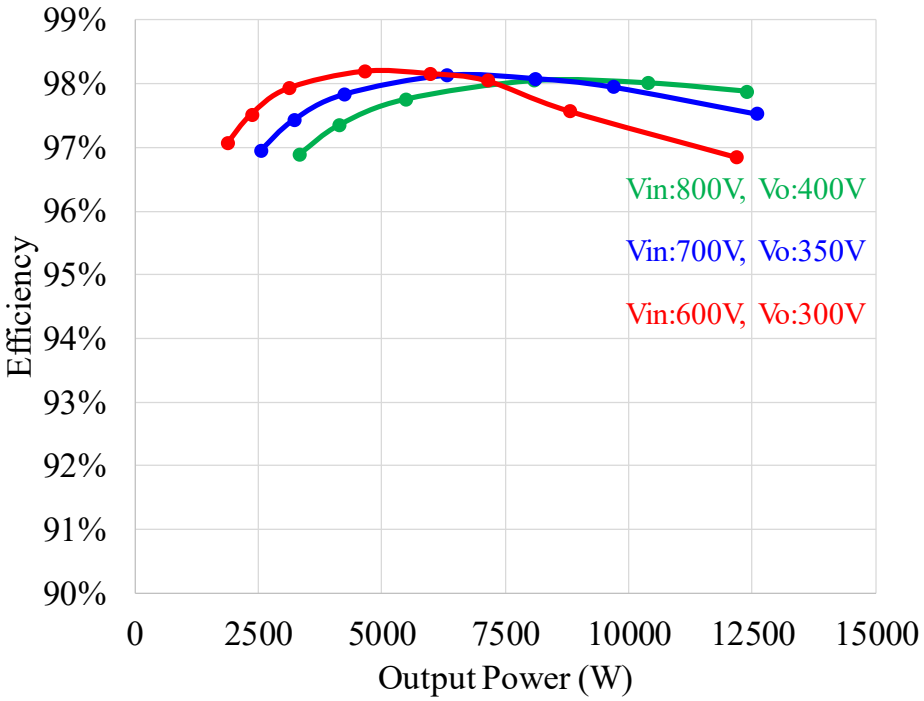


Fig. 5.48. Tested efficiency for forward operation mode under different input and output voltage.

The tested efficiency of the three-phase CLLC resonant converter for reverse operation is shown in Fig. 5.49 with different input and output voltage.

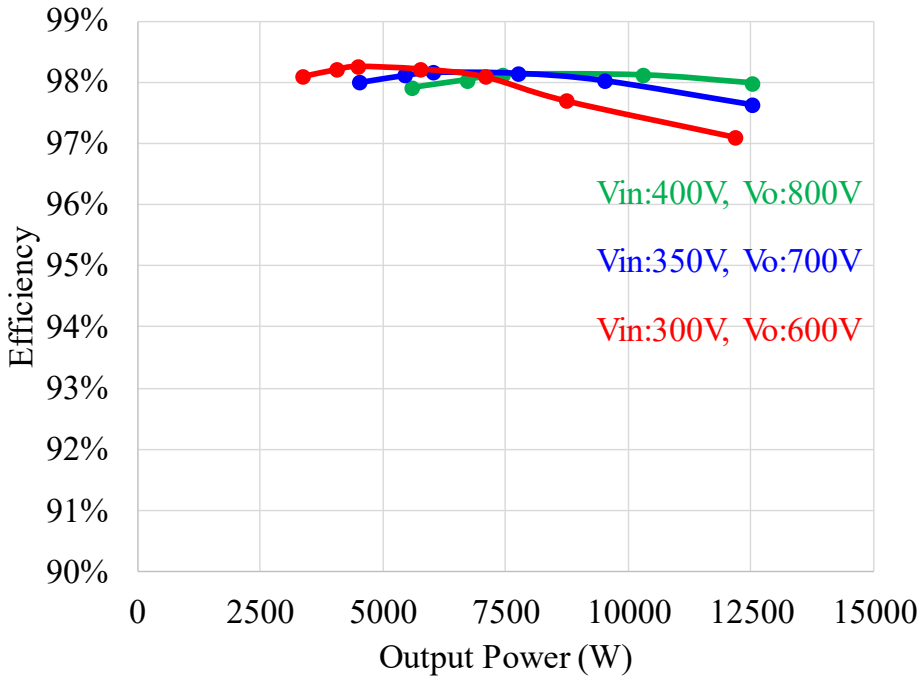


Fig. 5.49. Tested efficiency for reverse operation mode under different input and output voltage.

We can see that due to the symmetrical structure of the converter, the reverse operation almost has the same efficiency compared with the forward operation. Peak efficiency of 98.2% is achieved under different input voltage.

Efficiency under light load condition using phase shading is also tested, and the results are shown in Fig. 5.50.

We can see that around 1% efficiency is improved under light load condition due to the phase shading, which is over 30% loss saving.

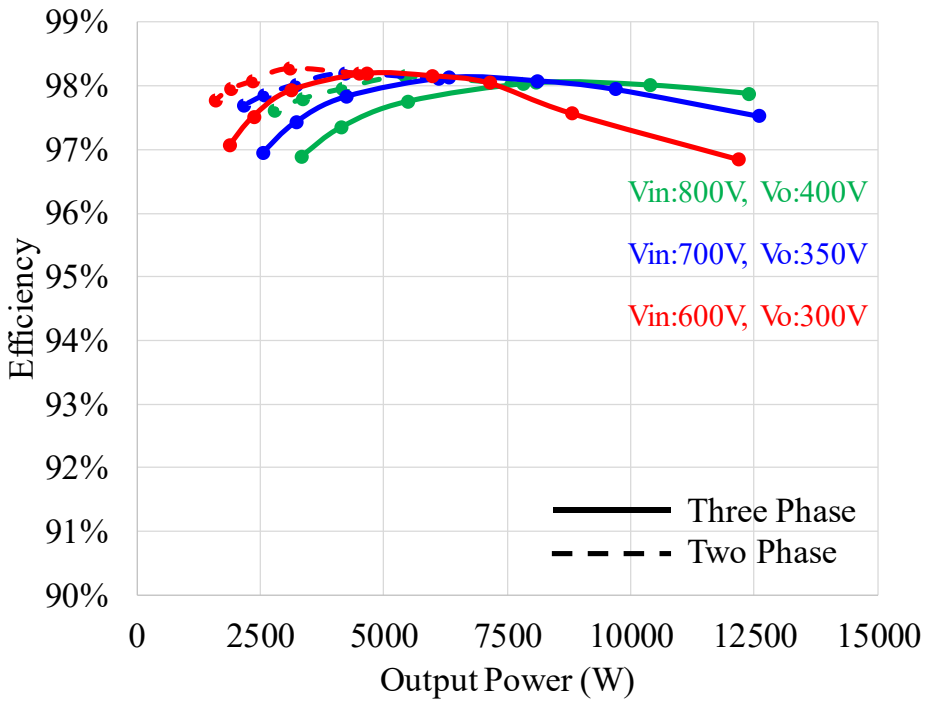


Fig. 5.50. Efficiency under light load condition using phase shading (solid line: three-phase; dash line: two-phase).

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Chapter 6 **Summary**

Due to the concerns regarding increasing fuel cost and air pollution, plug-in electric vehicles are drawing more and more attention. However, the commercialization of the PEV is impeded by the demands of a lightweight, compact, yet efficient on-board charger system. The emerging wide bandgap devices have demonstrated significant improvement comparing to silicon based devices. They provide the opportunity to greatly improve the efficiency and power density of power electronics converters.

First, a novel two-stage on-board charger structure is proposed. The first stage is a bridgeless totem pole AC/DC converter working at CRM so that soft switching can be achieved for all the fast switches. The second stage is a CLLC resonant converter. Similar with the well-known LLC converter, it can achieve soft switching under all conditions. In addition, due to the symmetrical resonant tank, it is more suitable for bi-directional operation. Variable DC-link voltage is adopted so that the DC/DC stage can always work at its optimized point, providing best efficiency over the entire battery voltage range. With soft switching technique, the switching frequency of AC/DC stage and DC/DC stage is pushed to 300 kHz and 500 kHz respectively.

Second, a novel integrated PCB winding transformer structure is proposed. Using matrix transformer concept, two UI core based transformers are integrated into one UI core, resulting in smaller footprint and 6-layer only PCB design. Also, by changing the UI core structure to a EI core structure, leakage inductance of the new transformer can be controlled by changing the cross section area of the center post. Therefore, it can serve as resonant inductor and achieve magnetic integration. In addition, the leakage flux is confined inside the core instead of flowing through the air, avoiding additional eddy current loss or EMI issues.

Regarding to the inter-winding capacitance issue of PCB winding transformer, a new symmetrical resonant converter and symmetrical transformer structure is proposed to cancel out the CM noise. This

method is not sensitive to PCB winding layout and switching frequency of the converter and have over 20 dB reduction for the CM noise.

Based on the above novel features, a two-stage 6.6 kW on board battery charger prototype with 96% efficiency and 37 W/in^3 power density is developed to demonstrate and verify the advantages of proposed two-stage structure.

In order to achieve faster charging, the on-board charger concept is also extended to a higher power level. A three-phase interleaved CLLC converter is designed to provide 12.5 kW power. Based on the single-phase integrated PCB winding magnetic, a three-phase integrated magnetic is proposed. Due to the interleave between the three phases, further integration can be done between and an even smaller footprint is achieved. A hardware prototype is built with 98.2% peak efficiency and 154W/in^3 power density to demonstrate and verify the proposed structure.

Appendix A. Hardware Design and Testing

In chapter 2, a variable DC-link two-stage on-board charger architecture is proposed, as shown in Fig. A. 1.

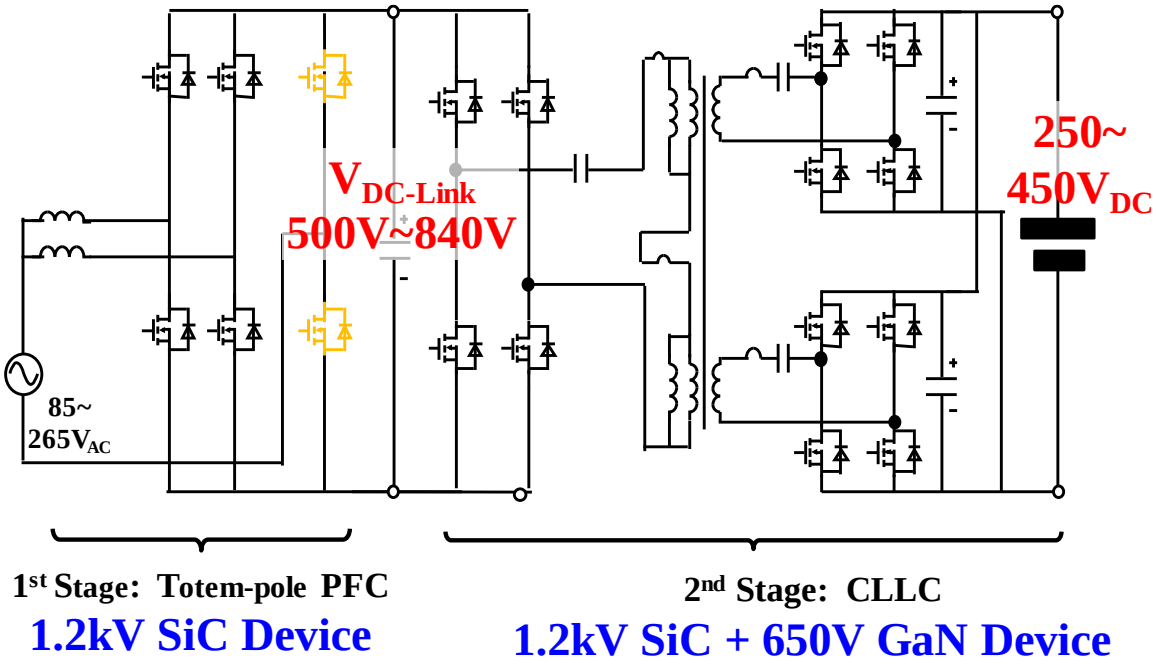


Fig. A. 1. Variable DC-link voltage structure without split capacitors.

According to the reference [1, 2], for GaN devices, soft switching (actually ZVS) is very critical for high frequency operation since the turn on loss is much larger than turn off loss. It is the same for the SiC devices. Comprehensive characterization of 1.2 kV SiC devices is done in references [3, 4]. It shows similar feature with GaN devices: the turn on loss is much larger than the turn off loss. In the proposed on-board charger design, AC/DC stage utilizes the bridgeless totem-pole structure with CRM operation while DC/DC stage adopts CLLC resonant converter. Both stages are able to achieve ZVS to eliminate the large turn on loss and have very high switching frequency.

A.1. Device candidates and evaluation

A.1.1. SiC device

The possible SiC candidates for the AC/DC stage and primary side of DC/DC stage is shown in Table. A. 1.

Table. A. 1. Possible SiC device candidates (from manufactures' datasheet).

	C2M0025120D	GE12N20L	GE12N025RF-3
I_d@100ºC	60A	75A	43A
V_{ds}	1200V	1200V	1200V
R_{dson}@25ºC	25mΩ	25mΩ	25mΩ
V_{th}	2.6V	3.2V	3.2V
R_{g_in}	1.1Ω	1Ω	1Ω
V_{gs} (recommend)	+20V/-5V	+18V/-5V	+18V/-5V
C_{iss}@500V	2788pF	3659pF	3164pF
C_{oss}@500V	230pF	216pF	199pF
C_{rss}@500V	17pF	15pF	21pF
Q_g	161nC	170nC	170nC
Package	TO-247	TO-247	DE-150

For all these three candidates, we can see that they have similar voltage and current rating. In addition, their on resistance and parasitic capacitance are very close. However, they do come with two different packages. One is conventional To-247 and one is DE-150, as shown in Fig. A. 2.

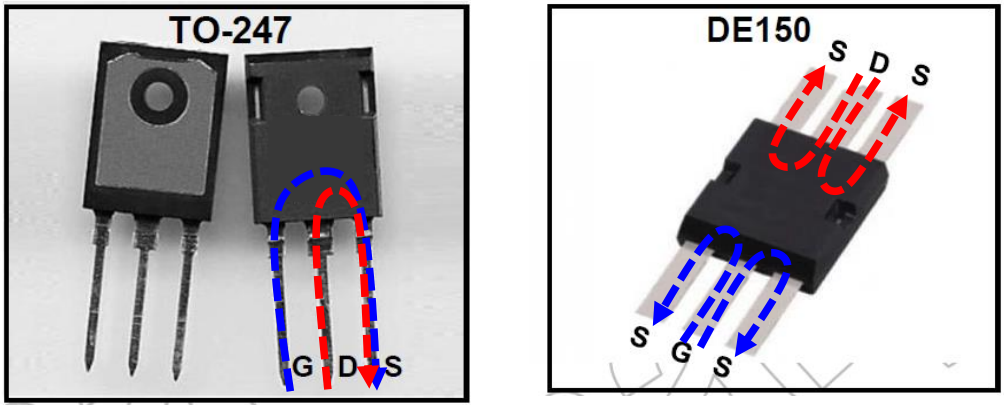


Fig. A. 2. Package comparison between To-247 and DE-150.

In order to understand the limitation of SiC device, a double pulse tester is built, as shown in Fig. A. 3 [5].

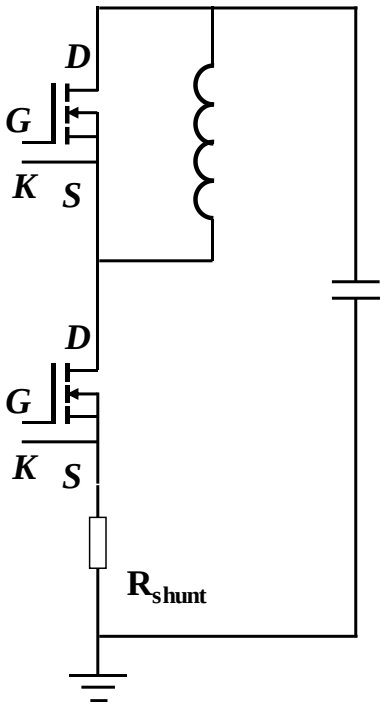


Fig. A. 3. Double pulse tester.

The configuration of the double pulse tester is a high bridge structure with both top and bottom devices to emulate the real operation condition. The inductor has very small equivalent parallel capacitance (EPC) to so that its impact on the device switching performance is kept minimum. A high speed gate driver IXDN614SI is used to drive the device with 20 V / -5 V for turn on gate voltage and turn off gate voltage respectively. To speed up the turn off transition, zero external turn off gate resistor is added to the circuit so that the turn off loss can be minimized. A 2 GHz high-bandwidth current shunt resistor (SSDN-10) is used to measure the drain source current flowing through the bottom device [6]. The drain source voltage waveform and the gate source voltage waveform of bottom device are measured with high voltage passive probe TPP0850, which has a bandwidth of 800 MHz and passive probe TPP1000 with a bandwidth of 1 GHz respectively.

Fig. A. 4 shows the tested turn off waveform with 800 V drain source voltage and 30 A current. The product of the drain source voltage and current is integrated to get the switching energy E_{OFF}. The waveform comparison shows that the GE device has lower turn off energy. However, quite significant parasitic ringing is observed with both devices, especially in the gate source voltage waveforms. The package related

parasitic inductances are the major reason for the ringing. For conventional TO-247 package, the long leads and long internal wire bonding bring signification parasitic inductance. In addition, the lack of Kelvin source connection generates very large common source inductance, which is the inductance shared by the power loop and the driving loop. As a result, the large *di*/*dt* in the power loop is coupled into the driving loop and generate significant amount of ringing.

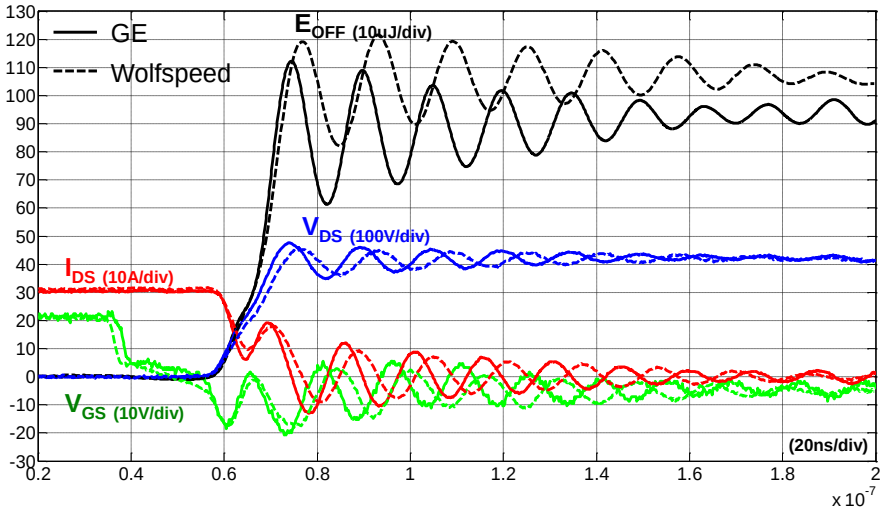
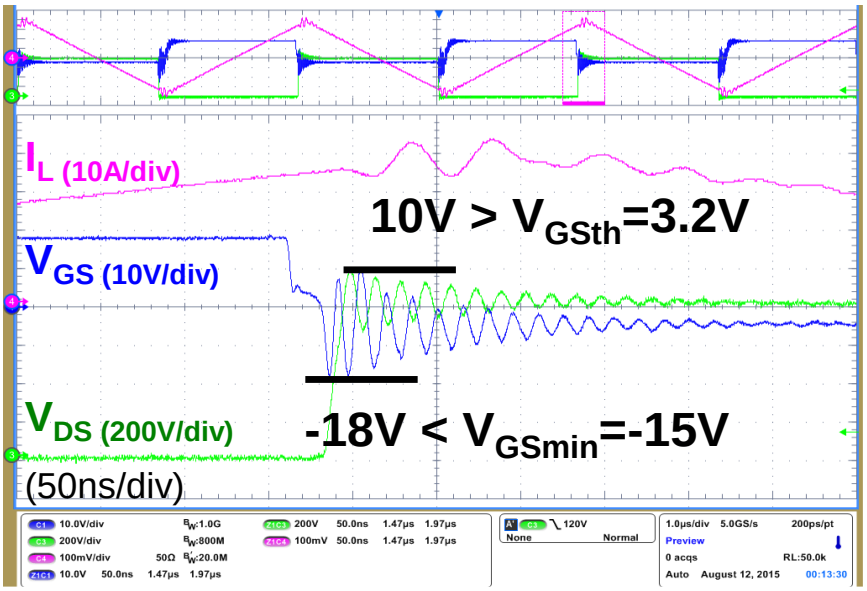
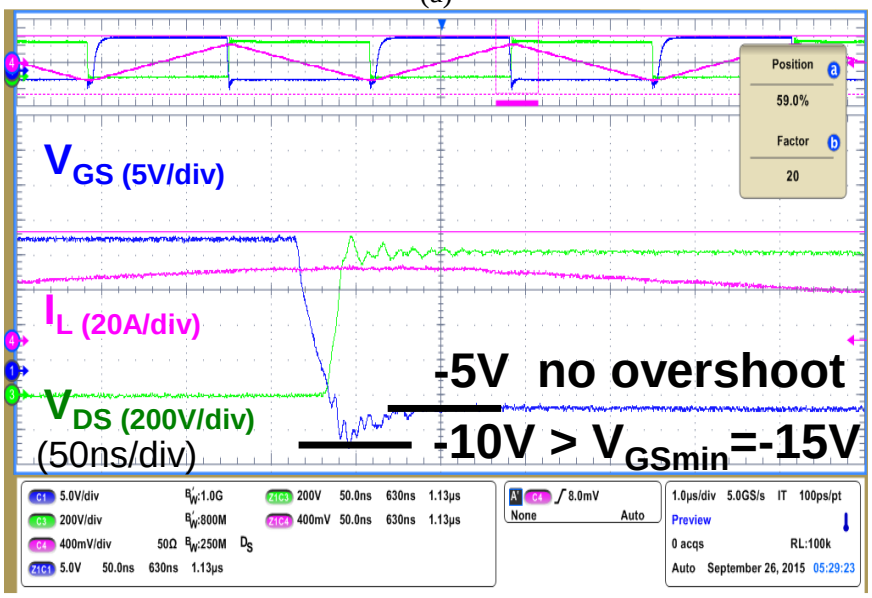


Fig. A. 4. Turn off waveform of GE SiC device (solid line) and WOLFSPEED SiC device (dash line) with 800 V voltage and 30 A current.

Large parasitic ringing on the gate source voltage brings two major concerns. One is the potential risk of false turn on since the positive voltage in the ringing is higher than the device turn on threshold voltage. This is detrimental to the converter because it causes circuit shoot through. The second one is the risk of device gate breakdown because the negative voltage in the ringing is lower than the datasheet claimed minimum negative voltage value.



(a)



(b)

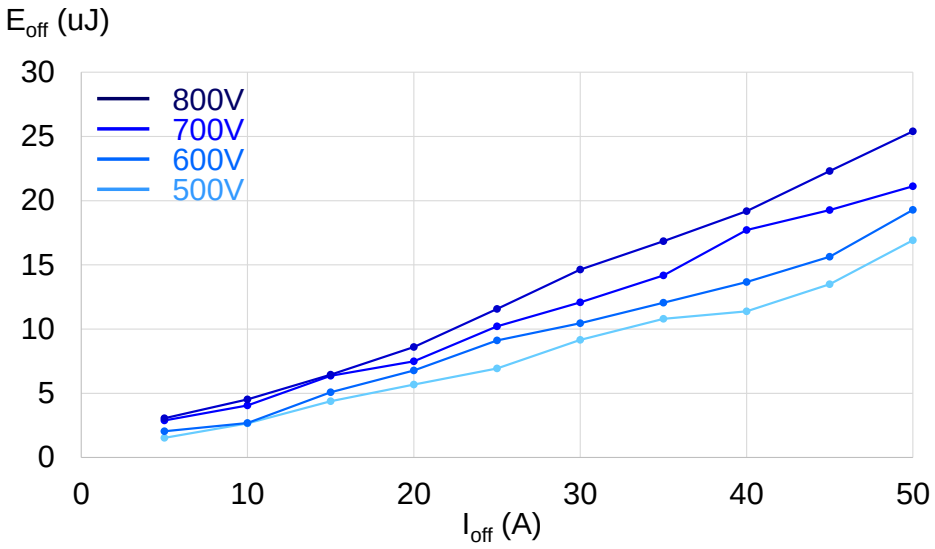
Fig. A. 5. Tested waveform under 800 V, 40 A and 300 kHz with (a) TO-247 package and (b) DE-150 package.

From the above testing result, it is clear that better package is necessary to achieve high frequency operation of SiC devices. There is another SiC device from GE with improved package, as known as DE-150. This is a device with radio frequency package. It provides decoupled power loop and driving loop, reduces parasitic inductors and has a symmetrical electric-magnetic field [7]. Therefore, the parasitic ringing is dramatically reduced compared to the TO-247 package. Fig. A. 5 provides a comparison between the two packages under the same 800 V, 40 A, 300 kHz, and 0 Ω turn-off gate resistor operating conditions.

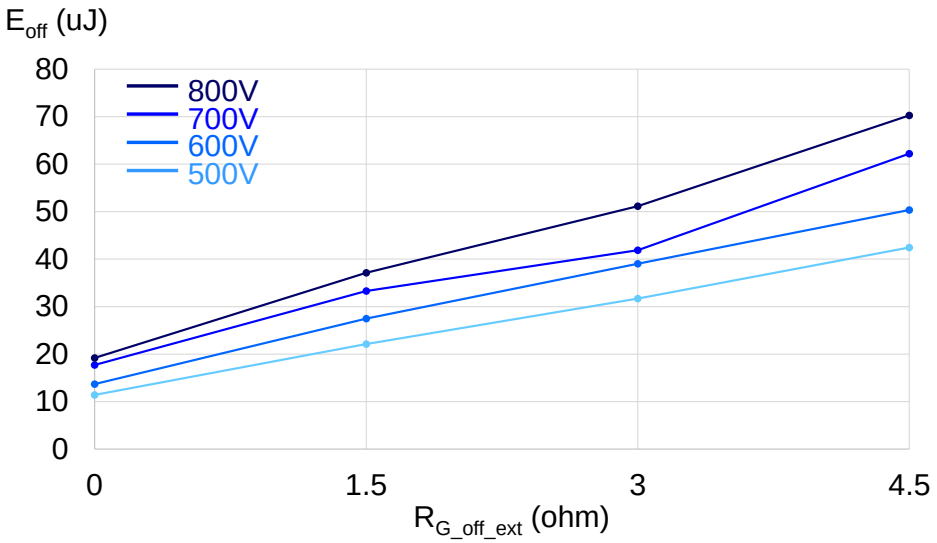
It can be seen that the SiC device with DE-150 package has much smaller parasitic ringing on the gate, eliminating the risk of false turn on and gate breakdown. In addition, the drain source voltage spike is reduced by about 50%.

From the comparison, it is obvious that the GE SiC with DE-150 package is more suitable for high frequency operation.

Since the proposed design has a variable DC-link voltage that ranging from 500 V to 840 V, the device turn off loss at different voltages and currents is tested and the results are shown in Fig. A. 6 (a). It is necessary to clarify that the energy stored in the output junction capacitor, often referred as E_{OSS}, is measured as a part of E_{off}. For hard switching, it is dumped in the channel of the device and dissipated during the turn on transition. But with ZVS, this part of energy is recycled. Hence, the E_{oss} is compensated from the measured E_{off} to reflect the real turn off loss.



(a)



(b)

Fig. A. 6. Tested turn off losses of the GE SiC MOSFET with (a) 0 ohm gate resistors at different voltages and currents; and with (b) different gate resistors at 40 A and different voltages

The gate resistor is another important factor that affects the turn off loss. The turn off loss with different gate resistors is also measured, as shown in Fig. A. 6 (b). This figure clearly shows that a smaller gate resistor leads to a smaller turn off loss.

A.1.2. **GaN device**

For the secondary side of DC/DC stage, 650 V GaN device is needed. The available GaN device on the market is shown in Table. A. 2.

Table. A. 2. 650 V GaN device candidates.

	E-Mode				D-Mode	
	Panasonic		GaN Systems		Transphorm	
	PGA26E08	PGA26E19	GS66508T	GS66516T	TPH3205	TPH3206
I_d@100ºC	15A@25ºC	13A@25ºC	25A	47A	22A	10A
V_{ds}	600V	600V	650V	650V	650V	650V
R_{dson}@25ºC	54mΩ	140mΩ	50mΩ	25mΩ	49mΩ	150mΩ
V_{th}	1.2V	1.2V	1.7V	1.3V	2.1V	2.1V
R_{g_in}	0.6Ω	0.8Ω	1.1Ω	0.34Ω	/	/
C_{iss}@400V	419pF	160pF	260pF	520pF	2200pF	720pF
C_{oss}@400V	218pF	28pF	65pF	130pF	135pF	46pF
C_{rss}@400V	40pF	0.2pF	2pF	4pF	23pF	5.5pF
Q_g	/	2.0nC	5.8nC	12.1nC	28nC	6.2nC

Enhancement mode (E-mode) MOSFET is a normally-off device, which can be directly used in the circuit [1] while depletion mode (D-mode) MOSFET is a normally on device, which needs to be configured in a cascode structure to perform like a normally-on device [8].

Similar with SiC device, double pulse tester is built with different GaN devices to shown their switching performance. Compared with SiC devices, to handle the even faster switching speed, most of the GaN devices have Kelvin source connection to de-couple the power loop with driving loop. As a result, the gate source voltage ringing is much better even with higher *dv*/*dt*.

The testing result of 400V, 15A turn off is shown in Fig. A. 7.

From double pulse testing result, we can see that GaN devices are very fast. The highest *dv*/*dt* is over 100V/ns, which is far beyond the current Si counterparts. Also, due to the Kelvin source connection in the package, gate source voltage is very clean even with 0V turn off voltage. (The special case here is PGA26E08 from Panasonic, which uses conventional PQFN package. It has larger parasitic inductance, which results in larger gate source voltage ringing.)

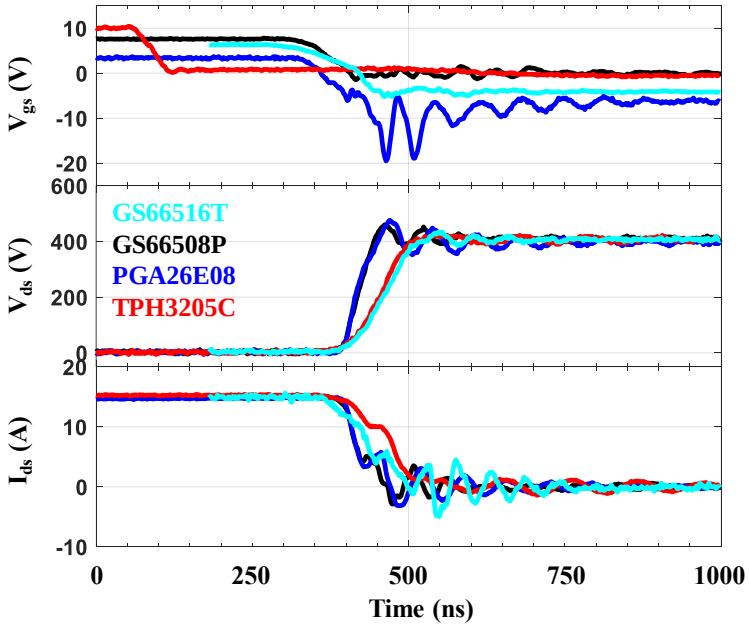


Fig. A. 7. Double pulse testing results of different GaN device turn off @400V, 15A.

The turn off loss comparison of the three devices is shown in Fig. A. 8.

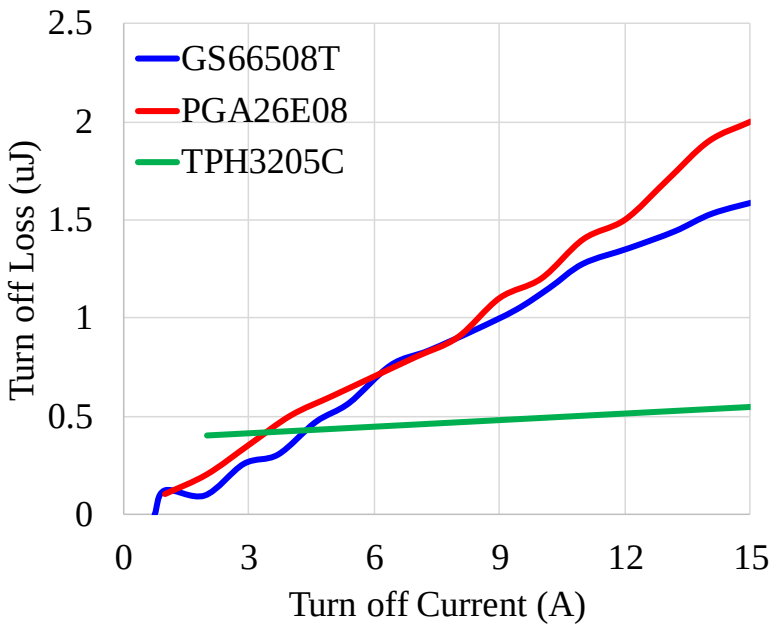


Fig. A. 8. Turn off loss comparison between GaN device candidates @400V.

However, it can be seen that most GaN devices have the current rating of 15-20A with on resistance in the range of 50 – 100 mΩ. This is too large for a 6.6 kW system even with two sets of output. The conduction loss is too large and the system efficiency will be compromised.

As a result, GS66516T from GaN Systems is selected as the DC/DC stage secondary side device.

If we compare the switching energy between GaN device and SiC device, we can find out that turn on energy is always much larger than turn off energy for both GaN device and SiC device, which justifies zero voltage switching under high switching frequency.

In addition, due to the smaller parasitic capacitance, GaN device is much faster than SiC and as a result, both turn on energy and turn off energy of GaN device is smaller than SiC device.

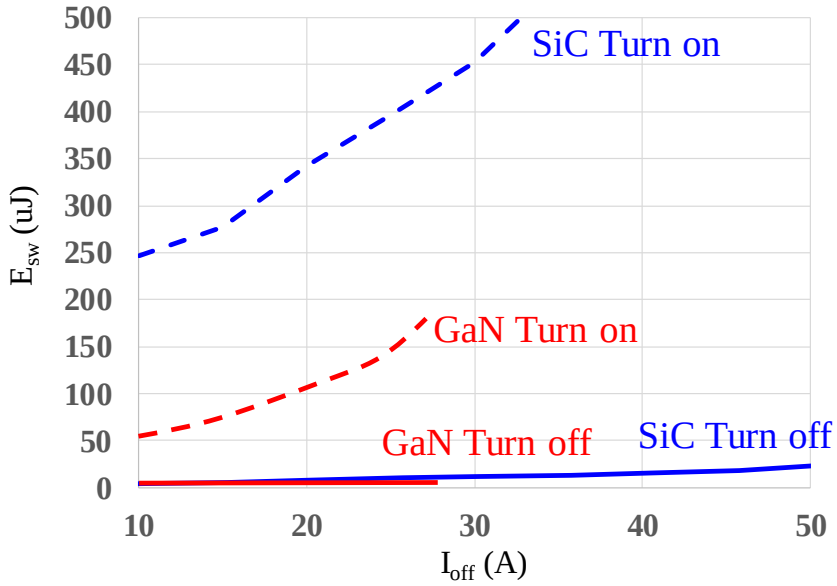


Fig. A. 9. Measured switching loss of GE's 1.2kV SiC device at 600V and 650 V GaN device GS66508P at 400V.

A.2. **Driving circuit design**

A.2.1. **Driving circuit for SiC**

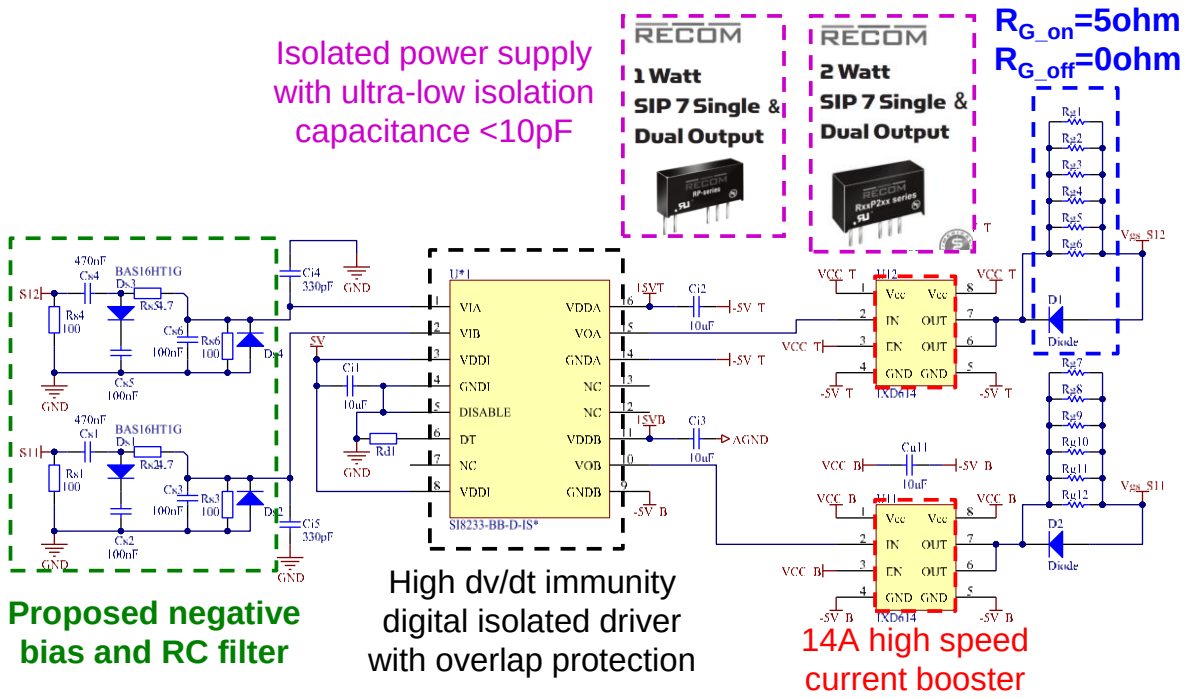


Fig. A. 10. Schematic of the SiC gate driver.

For SiC device, in order to shorten the turn off transition period and reduce turn off loss, larger sink current capability of the driver is required. However, the fast turn off speed also increases the *dv*/*dt* of the switch node and makes the common mode voltage immunity more challenging. With reference to work presented in [9], the schematic of the gate driver design in this work is shown as Fig. A. 10.

Two-stage driving architecture is adopted. The first stage performs isolation (>2500VRMS), gate signal protection (signal overlap protection) and matched delay time between top switch and bottom switch. The isolator is selected to have very high common mode voltage immunity capability up to 50 V/ns and have a very small input to output capacitance under 1.4 pF. The second stage is a simple current booster to provide larger sink current capability. In addition, a bias and filter circuit is designed to avoid interference between PWM signal and the power stage. A 5 Ω turn on gate resistor and 0 Ω turn off gate resistor is adopted to turn off the device as fast as possible to reduce turn off loss. Isolated power supplies with low parasitic capacitance (1 – 2pF) provide positive and negative driving voltage separately.

A.2.2. **Driving circuit for GaN**

Due to the much smaller gate charge of GaN device, the driving circuit is much simpler compared to SiC drivers.

The same two-channel isolator is enough to serve as both the isolator and the gate driver. Also, since there is no negative driving voltage, bootstrap circuit is used to provide the top switching driving voltage. The same bias and filter circuit is designed to avoid interference between PWM signal and the power stage as in the SiC driving circuit. A 5 Ω turn on gate resistor and 0 Ω turn off gate resistor is adopted to turn off the device as fast as possible to reduce turn off loss.

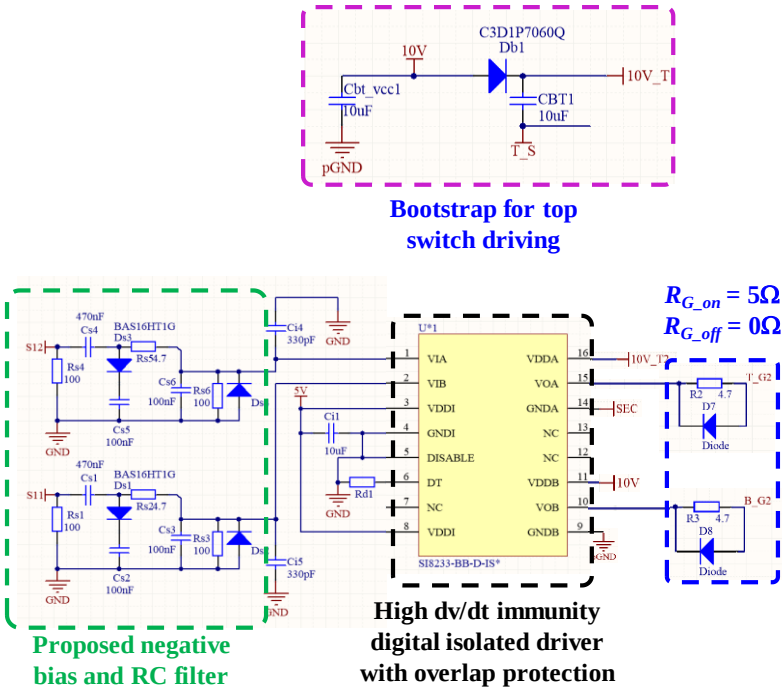


Fig. A. 11. Schematic of the GaN gate driver.

The detailed driving scheme is shown in Fig. A. 11.

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