Design and Implementation of a Radiation Hardened GaN Based Isolated DC-DC Converter for Space Applications

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ABSTRACT

Power converters used in high reliability radiation hardened space applications trail their commercial counterparts in terms of power density and efficiency. This is due to the additional challenges that arise in the design of space rated power converters from the harsh environment they need to operate in, to the limited availability of space qualified components and field demonstrated power converter topologies. Recently released radiation hardened Gallium Nitride (GaN) Field Effect Transistors (FETs) with their inherent radiation tolerance and superior performance over Silicon Power Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), however, offer a promising alternative to improve power density and performance of space power converters.

This thesis presents a practical implementation of the Phase Shifted Full Bridge DC-DC Isolated converter with synchronous rectification for space applications using newly released radiation hardened GaN FETs. A survey outlining the benefits of new radiation hardened GaN FETs for space power applications compared to existing radiation hardened power MOSFETs is included. In addition, this work summarizes the main design considerations to implement the selected converter topology for space applications. Furthermore, the overall design process followed to design the DC-DC converter power stage, as well as a comprehensive power loss analysis are included.

This work also includes details to implement a conventional hard-switched Full Bridge DC-DC converter using radiation hardened GaN FETs for this application. An

efficiency and component stress comparison was performed between the hard-switched Full Bridge design and the Phase Shifted Full Bridge DC-DC converter design. This comparison highlights the benefits of phase shift modulation (PSM) and zero voltage switching (ZVS) for GaN FET applications. Furthermore, different magnetic designs were characterized and compared for efficiency in both converters. The DC-DC converters implemented in this work regulate their outputs to a nominal 20 V, delivering 500 W from a nominal 100 V DC Bus input. Failure mode and effects analysis (FMEA) and protection circuitry required for complete radiation qualification of the Phase Shifted Full Bridge DC-DC converter topology are not addressed by this work.

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GENERAL AUDIENCE ABSTRACT

Recently released radiation-hardened Gallium Nitride (GaN) Field Effect Transistors (FETs) offer the opportunity to increase efficiency and power density of space DC-DC power converters. The current state of the art for space DC-DC power conversion trails their commercial counterparts in terms of power density and efficiency. This is mainly due to two factors. The first factor is related to the additional challenges that arise in the design of space rated power converters from the harsh environment they need to operate in, to the limited availability of space qualified components and field demonstrated converter topologies. The second factor lies in producing reliable radiation hardened power Metal Oxide Semiconductor Field Effect Transistors (MOSFETs).

GaN FETs not only have better electrical performance than power MOSFETs, they have also demonstrated inherent tolerance to radiation. This results in less structural device changes needed to make GaN FETs operate reliably under high radiation compared to their MOSFETs counterparts. This work outlines the design implications of using newly released radiation hardened GaN FETs to implement a fixed frequency isolated Phase Shifted Full Bridge DC-DC converter while strictly abiding to the design constraints found in space-power converter applications. In addition, a one-to-one performance comparison was made between the soft-switched Phase Shift modulated Full Bridge and the conventional hard-switched Full Bridge DC-DC converter. Finally, different magnetic designs were evaluated in the laboratory to assess their impact on converter efficiency.

To

Miriam Turriate

Gloria Gastulo

Godofredo Turriate

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Chapter 1 Introduction

1.1. Background

Power converters in high reliability space or military applications usually trail their commercial counter parts in terms of power density and efficiency. For space applications, there are two important factors affecting performance and power density of DC-DC converters. The first factor is related to the mission critical nature of space power converters, which favors the use of field-demonstrated isolated topologies such as the Forward and Flyback DC-DC converters [1-4]. The Forward and Flyback DC-DC converters operate with a single semiconductor switch on the primary side connecting an impedance (inductance) between the DC Bus and ground as shown in Figure 1. These two single ended converters are favored in space applications because a direct path from the DC Bus to ground cannot be formed during transient fault conditions generated by the single events effects (SEE) in [5, 6] impacting the primary side transistor. In addition, Flyback and Forward converters have simple transistor gate drive timing requirements with low side primary gate drive and easy implementation of low-side transistor gate drive for synchronous rectification.

However, isolated single ended topologies like the Forward and Flyback converters operate their transformer only in one quadrant of the magnetic B-H curve as shown in Figure 1. This results in suboptimal magnetic core utilization, which makes the Flyback and Forward converters less suited at power levels above 100 W and 300 W, respectively [7, 8]. Nevertheless, to overcome the power limits of single ended topologies in space applications demanding power in the kilo-watt range, Forward converters are used in paralleled or in multiphase arrangements in many cases at the expense of system efficiency and power density.

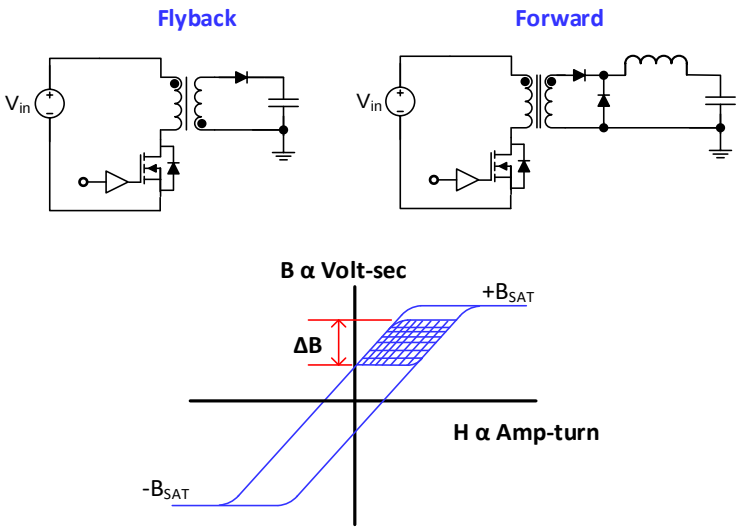

Figure 1. Common single ended isolated topologies used in space converters

Table 1 summarizes different power converter topologies in relation to the power levels at which they are traditionally used [7, 8]. For isolated converters delivering over 300 W, double-ended topologies such as push-pull, half-bridge, and full bridge converters are better suited. Double-ended converters use transformers more efficiently by allowing transformer operation over two quadrants in the magnetic hysteresis B-H curve as shown in Figure 2. The push-pull converter has a simple low-side power MOSFET gate drive; however, it requires two windings in the transformer primary side which over complicates its transformer design. In addition, the voltage stress in the primary side switches is two times the input voltage V_{IN}.

On the other hand, the half bridge and full bridge converters have better transformer window area utilization with only one primary winding required. In addition, the voltage stress on the primary side switches typically does not exceed the input DC voltage V_{IN}. For these two reasons, the half bridge and full bridge converters can yield better efficiency and power density than a push pull converter. Furthermore, implementing zero voltage switching (ZVS) schemes allow the half bridge and full bridge converters to achieve very high efficiencies, power density,

and reduced electromagnetic interference (EMI). However, the benefits of half bridge and full bridge converters come at the expense of complex transistor gate drive requirements involving high side and low side gate driver design and accurate gate control timing between all switches to avoid shoot-through failures.

Table 1. Common Power Levels for Different DC-DC Converter Topologies [8]

Topology	Power Range	Transformer Utilization	Active Switches	Switch Voltage Stress
Flyback	≤ 100 W	Single Ended	1	$V_{IN} + N_{PS} \bullet V_{OUT}$
Forward	50 W to 200 W	Single Ended	1	$V_{IN} / (1\text{-}D) = 2 \bullet V_{IN}$ @ D=50%
Active-Clamp Forward	50 W to 300 W	Semi-Double Ended	2	$V_{IN} / (1\text{-}D)$
Push-Pull	100 W to 500 W	Double Ended	2	$2 \bullet V_{IN}$
Half Bridge	100 W to 500 W	Double Ended	2	$V_{IN}/2$
Full Bridge	≥ 500 W	Double Ended	4	V_{IN}

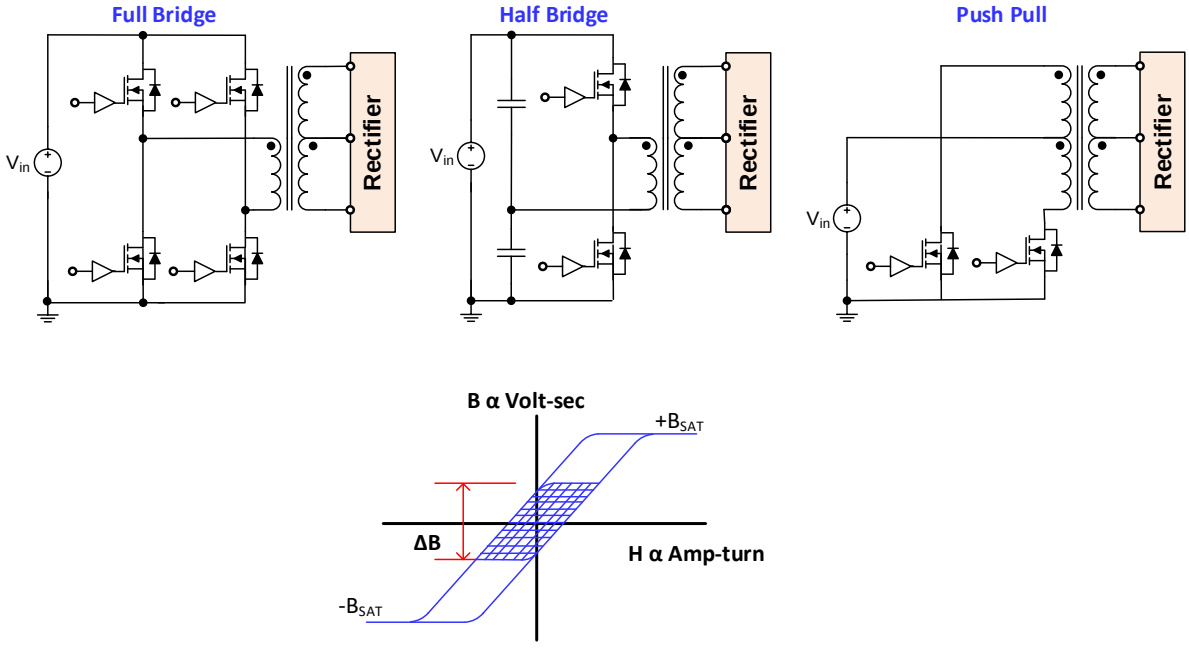

Figure 2. Common double ended isolated topologies

Even with proper gate driver design, radiation exposure in space can still cause the top and bottom switches in a half bridge or full bridge converters to falsely turn ON simultaneously resulting in shoot-through current and possibly catastrophic converter failure. For this reason, the implementation of the half bridge and full bridge converters for space applications becomes even more complex than what is normally encountered in commercial applications once radiation effects and failure modes encountered in space are considered.

Power Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are the second factor limiting performance and power density of space rated DC-DC converters. Power MOSFETs are very susceptible to damage and degradation from irradiation found in space, in special to ionizing radiation [6, 9, 10, 11]. Achieving radiation tolerance in power MOSFETs results in larger and less efficient devices [12, 13]. Radiation hardened power MOSFETs are also more expensive due to the extensive screening and qualification testing required. The next sections describe the main factors that make radiation-hardened power MOSFETs—and in turn space rated power converters—inferior in size and performance than their commercial equivalents.

1.2. Radiation Effects on Power Converters and Power MOSFETS

Radiation effects in microelectronics are classified according to irradiation types, with Single Event Effects (SEE), Total Ionizing Dose (TID) and Displacement Damage Dose (DDD) [5, 6, 9, 10] being the most relevant to space power converter applications. Radiation effects in electronic circuits are caused by heavy particles (protons, neutrons, ions) traveling through the microelectronic device atomic structure. In power converters, these charged particles can cause intrinsic p-n junctions to conduct inside power MOSFETs. They can also cause structural changes to the lattice of power MOSFETs resulting in electrical performance degradation [5]. In addition,

these particles can create electrical energy spikes at the input and outputs of power management and protection electronic circuits in power converters, which also adversely affects converter performance.

1.2.1. Single Event Effects

Catastrophic damage from SEE in power MOSFETs mainly take the form of Single Event Gate Rupture and Single Event Burnout. In Single Event Gate Rupture (SEGR), a heavy particle strikes the power MOSFET and punctures the device's gate-oxide layer. This causes the gate electrode to fuse producing a conductive path through the gate oxide of the MOSFET or any MOS type of device (e.g. CMOS or BiCMOS based microelectronics) [5]. The fact that power MOSFETs are more susceptible to SEE in their OFF state—when they are blocking a high voltage—exacerbates the effects of SEGR. Increasing the gate-oxide thickness and de-rating the voltage applied to power MOSFETs reduces its susceptibility to SEGR [5, 6, 14]. This results in larger power MOSFETs, which in turn have larger parasitic capacitances and ON-state resistance (R_{DSON}) than a power MOSET used in a commercial application. The higher figure of merit (FOM) due to high input capacitance and R_{DSON} negatively affect radiation hardened (rad-hard) power MOSFET's performance.

Furthermore, SEE from heavy ion radiation in power MOSFETs create current pockets that can result in turn ON of the parasitic bipolar junction transistor (BJT) inside the device. This creates a direct conductive path from drain to source in the power MOSFET causing destructive failure known as Single Event Burnout (SEB) [5, 14]. SEB is more frequent in N-channel power MOSFETs [5, 14], which are the heart of the majority of power converters for space. The parasitic BJT in an N-MOSFET is an NPN BJT device. This NPN BJT has higher current gain than its PNP BJT counterpart found in P-channel power MOSFETs. The higher current gain in a NPN BJT

means that very little base current from SEE is needed to turn on the parasitic BJT, resulting in SEB destructive failure of the MOSFET [5, 6, 14, 15].

On the other hand, non-destructive radiation effects in power converters due to SEE usually come in the form of Single Event Transients (SET). SET happen as charged particles strike microelectronics causing electric spikes at the inputs or outputs of electronic circuits [5, 6]. In power converters, SET can result in false triggering of comparators and operational amplifiers used in power converter telemetry and fault protection circuits. In addition, Single Event Transients can cause false triggering of gate control signals of power MOSFETs. Usually, only additional filtering and bigger decoupling capacitance are used to reduce the effects of SET in power converter circuits.

1.2.2. Total Ionizing Dose and Displacement Damage Dose

Total Ionizing Dose (TID) refers to cumulative long term effects of ionizing radiation in microelectronics. Radiation in space can cause charged particles to deposit in the oxide layers of microelectronic devices and accumulate over time. TID mainly affects devices with Silicon Dioxide (SiO_2) insulators such as the metal-oxide layers found in CMOS circuits and MOSFETs. BJTs are less susceptible to TID because they usually do not contain gate oxides. Therefore, TID is usually not a pronounced problem for BJT based circuits [5, 6, 14]. The main manifestation of TID in BJTs circuits come from devices using oxide isolation layers where charge trapping can affect minority carriers in the base. This results in reduced current gain, i.e. more base current injection required for the same collector current [5].

The effects of TID in power MOSFETs are due to trapped charge build-up causing lattice and oxide layer defects that result in changes in the power MOSFET threshold voltage [6]. Charge entrapment from TID cause N-MOSFETs threshold voltage to lower, making them harder to turn

OFF. Therefore, TID results in higher leakage current in N-MOSFETs. On other the hand, charge entrapment has the opposite effect in P-MOSFETs, resulting in harder to turn ON devices [5, 9, 14]. N-Type power MOSFETs are the workhorse of power converters, and TID has the potential of causing catastrophic converter damage if the power MOSFET device turns ON inadvertently from the altered threshold voltage level. TID mitigation involves reducing the oxide layer size in power MOSFETs [5, 14]. Thus, SEGR and TID robustness require a trade-off of gate oxide size to make power MOSFETs more robust to both type of radiation effects.

Displacement Damage Dose (DDD) radiation is due to heavy particles shifting atoms in the Silicon semiconductor lattice and altering the material's charge carrier concentrations [5, 6]. DDD usually affects minority carrier concentrations in semiconductors and reduce carrier mobility [5, 6]. BJTs use both minority and majority carriers (i.e. bipolar carrier conduction) for proper operation. BJT based analog circuits and BiCMOS (Bipolar and CMOS transistors) circuits will suffer degradation from DDD. Structural lattice damage from DDD in BJTs traps minority carriers, and in the same manner as TID, it results in reduced BJT current gain [5]. When selecting band-gap references, operational amplifiers, and comparators for peripheral circuitry in power converter applications, consideration of TID and DDD radiation effects is important. Changes in offset voltages and currents, bias currents, open loop voltage gain, and device saturation voltages are the main manifestation of performance degradation under radiation doses in BJT circuits [5]. Worst-case and tolerance sensitivity analysis via SPICE simulation are common methods to determine performance degradation of BJT circuits due to radiation effects. Power MOSFETs, unlike BJTs, are unipolar (i.e. only majority carrier) devices. Therefore, Displacement Damage Dose effects do not adversely affect power MOSFETs significantly [6, 9].

1.3. Commercial and Radiation Hardened Power MOSFETS

Radiation hardened Silicon (Si) MOSFETs are expensive due to the longer engineering development cycles, low quantities produced, and extensive qualification testing they require. Rad-hard power MOSFETs are also bulkier due to the structural changes required for reliable operation under radiation, which results in a high FOM and reduction of space power converter performance. Comparing the datasheet of a 300 kRad (Si) rad-hard power N-MOSFET to a similar commercial power N-MOSFET, the differences in performance, size, and cost are evident. For instance, the IRHNA67260 is a 300 kRad (Si) N-MOSFET from International Rectifier rated for 200V drain-source voltage (V_{DS}). This device has a room ambient R_{DSON} of 28mΩ at a 40 A test drain current, I_D. This device is available in a surface mount (SMT) SMD-2 package with dimensions of 13.56 mm x 17.65 mm, and height of 3.58 mm [16]. Cost information for the IRHNA67260 is not easily obtainable, but the cost of a similar 200V rad-hard power MOSFET, the JANSF2N7269U from Microsemi, is $570 per piece for a quantity of 50 order [17].

For a one-to-one comparison with a commercial device, Infineon's IRFS4227TRL and Toshiba's TPH2900ENH can be studied [18, 19]. Both of these N-MOFETS have R_{DSON} values from 26 mΩ to 29 mΩ, with 200V rated V_{DS} and 33 A to 62 A of rated current. Their cost is around $2.81 per piece for a quantity of 50 order. Deviating from a one-to-one comparison, superior commercial MOSFETs with 200 V V_{DS} are available, such as Infineon's IPT111N20NFD [20] with an R_{DSON} of 11 mΩ and costing around $7.78 per piece on a quantity of 50 order. These commercial N-MOSFET are not only cheaper and smaller, the all have better figure of merit than the rad-hard N-MOSFET from Microsemi and International Rectifier, as summarized in Table 2.

Table 2. Comparison of Rad-Hard and Commercial Power MOSFETs

Part Number	**JANSF2N7269**	**IRHNA67260**	**IRFS4227TRL**	**TPH2900ENH**	**IPT111N20NFD**
Manufacturer	Microsemi	International Rectifier	Infineon	Toshiba	Infineon
Type	Rad-hard	Rad-Hard	Commercial	Commercial	Commercial
R_{DSON} (25°C)	100 mΩ	28 mΩ	26 mΩ	29 mΩ	11 mΩ
Maximum Q_G	170 nC	240 nC	98 nC	22 nC	87 nC
FOM	**17 n**	**6.72 n**	**2.55 n**	**0.64 n**	**0.96 n**
V_{DS}	200 V	200 V	200 V	200 V	200 V
I_D (100°C)	16.0 A	56.0 A	62.0 A	33.0 A	96.0 A
Package Size	11.5 mm x 16 mm	13.56 mm x 17.65 mm	10.67 mm x 15.88 mm	5.2 mm x 6.3 mm	10.1 mm x 11.88 mm
Height	3.6 mm	3.58 mm	4.83 mm	1 mm	2.4 mm
Package Type	SMD-1	SMD-2	D2Pak	8-PowerVDFN	PG-HSOF-8
Volume	**663 mm^3**	**856.8 mm^3**	**818.4 mm^3**	**32.76 mm^3**	**288 mm^3**
Price (50 qty.)	$570	~$570	$2.88	$2.51	$7.78

To illustrate the differences in performance and power density between space-rated DC-DC converters and their commercial counterparts, state of the art high-reliability (HI-REL) and space hybrid isolated converters rated for 5.0 V outputs at 100 W are compared against similar commercial offerings. HI-REL converters from VPT, Inc. achieve 90% efficiency with 3.6 kW/L power density, while a space hybrid only gets to about 78% efficiency at 4.0 kW/L power density [1, 2]. In contrast, commercial DC-DC converters from Murata and Artesyn with similar specifications achieve 93% and 92% efficiencies, respectively. These two commercial rated DC-DC converters also have higher power densities than their HI-REL and space counter parts, achieving power densities from 4.4 kW/L to 4.8 kW/L [21, 22].

Power density in this thesis is defined as not only the power stage but the complete DC-DC power module solution that includes internal housekeeping power supplies, controller, gate drivers, fault protection and other periphery circuitry unless stated otherwise. Table 3 and Table 4 summarize the specifications and power densities for the HI-REL, space, and commercial DC-DC converter modules described in this section.

Table 3. High Reliability and Space Hybrid Isolated DC-DC Converters

Part Number	**VHR100+2805S**	**SVRFL2805S**
Manufacturer	VPT	VPT
Type	HI-REL	Space, Hybrid
Input Range	16 V to 40 V	18 V to 40 V
Nominal Input	28 V	28 V
Output Voltage	5 V	5 V
Typical Efficiency	90%	78%
Output Power	100 W	100 W
Power Density	3.6 kW/L (59 W/in^3)	4.0 kW/L (65 W/in^3)

Table 4. Commercial Rated Isolated DC-DC Converters

Part Number	**AVQ100-24S05**	**UVQ-5/20-D24P**
Manufacturer	Artesyn	Murata
Type	COTS	COTS
Input Range	18 V to 36 V	18 V to 36 V
Nominal Input	24 V	24 V
Output Voltage	5 V	5 V
Typical Efficiency	93%	92%
Output Power	100 W	100 W
Power Density	4.8 kW/L (79 W/in^3)	4.4 kW/L (72 W/in^3)

1.4. Benefits of Radiation Hardened GaN FETs

GaN FETs do not have many of the design challenges encountered in producing reliable rad-hard power MOSFETs. In recent years, radiation testing results show that the Enhancement mode GaN FETs, also known as high electron mobility transistors (HEMTs), are very tolerant to radiation environments found in space [23-28]. This is due to the strong atomic bond of the Gallium Nitride binary compound [27, 28], as well as the physical structure of enhancement mode GaN FETs (eGaN FETs).

Enhancement mode GaN FETs were tested in [24, 29] for SEE and total dose. SEE results from [24] show that many first-generation eGaN FETs from EPC mostly operated within their datasheet limits, with a few exceptions where the drain-source leakage increased or the devices catastrophically failed. In general, early radiation testing results for first-generation commercial

eGaN FETs from EPC demonstrated more robustness to SEE than their rad-hard power MOSFETs counter parts [24]. In addition, second-generation EPC eGaN FETs demonstrated higher SEE radiation robustness with no SEGR failures occurring, but with SEB occurring at voltages close to the device's drain-source ratings [29].

In addition, eGaN FETs are very robust to ionizing radiation due to the lack of a metal-oxide layer, which mitigates charge entrapment issues from TID in high radiation environments [24], [26]. Early radiation testing performed in first generation eGaN FETs from EPC showed less than 4% threshold voltage (V_{TH}) variation and less than 3% R_{DSON} changes with 5 V applied to the gate while exposed to 500 kRad (Si) ionizing doses. With the devices in the OFF stage, higher variation was reported (18% V_{TH}, and 8% R_{DSON} variation) [24]. Second-generation eGaN FETs from EPC showed no performance degradation from TID up to 1.0 MRad (Si) [29].

Accordingly, DC-DC converters using eGaN FETs have demonstrated superior power density and efficiency compared to power converters that use rad-hard power MOSFETs when exposed to similar doses of radiation [30]. Table 5 shows a brief comparison between power eGaN FETs and power MOSFETs under the most common types of radiation described in this thesis and obtained from [23, 24, 26].

Table 5. Radiation Effects between Power eGaN FETS and Power MOSFETs

Radiation Type	MOSFET	eGaN FET
Total Ionizing Dose And Displacement Damage	Atomic change in lattice: • Carrier concentration altered	Strong bond, reinjection of carriers from AlGaN/GaN interface • Carrier concentration in 2DEG less affected
	Metal Oxide layer traps charge: • Threshold voltage changes	Field Effect Transistor: • No oxide layer to trap charge
Single Event Effects	SE Gate Rupture (SEGR) • Catastrophic failure	SE Gate Rupture (SEGR) • No Catastrophic failure observed
	SE Burn Out (SEB) • Catastrophic failure	SE Burn Out (SEB) • Catastrophic failure
Conclusion	Bulkier die to meet tolerance levels	Almost no die change, mainly packaging
	Very susceptible to radiation	Very tolerant to radiation
	High FOM: low performance	Low FOM: good performance

There are currently two commercially available rad-hard enhancement mode GaN FET alternatives to 200 V rad-hard MOSFETs. One is the FBG20N18B from Freebird Semiconductor, and the other is the newly released ISL70024SEH from Intersil. Table 6 shows the main electrical and physical characteristics of these two rad-hard eGaN FETs [31, 32].

Table 6. Specifications of Currently available 200V Rad-hard GaN FETs

Part Number	**FBG20N18B**	**ISL70024SEH**
Manufacturer	Freebird Semiconductor	Intersil
Total Dose	300 kRad(Si)	100 kRad(Si)
Maximum RDSON	26 mΩ	45 mΩ
Maximum QG	6.0 nC	6.0 nC
FOM	0.156 n	0.270 n
V_{DS}	200 V	200 V
I_{DS} (25°C)	18.0 A	7.5 A
Package Size	3.8 mm x 5.6 mm	4.83 mm x 9.13 mm
Height	2.3 mm	2.02 mm
Volume	49 mm^3	89 mm^3

The FBG20N18B and ISL70024SEH rad-hard GaN FETs electrical parameters shown in Table 6 are greatly superior to the IRHNA67260 rad-hard MOSFET from International rectifier summarized in Table 2. In fact, the FOMs for both rad-hard GaN FETs are better than the FOMs

of the commercial MOSFET devices from Toshiba and Infineon as outlined in Table 2. Moreover, The FBG20N18B and ISL70024SEH rad-hard GaN FETs are also smaller by a factor of 7 to 10 compared to the rad-hard N-MOSFET from International Rectifier. GaN FETs performance under high radiation as described earlier, besides the benefits that GaN FETs offers in terms of FOM and power density compared to power MOSFETs, makes recently released rad-hard GaN FETS a very attractive replacement for rad-hard MOSFETs. Figure 3 and Figure 4 show the physical packages for the 200 V rad-hard eGaN FETs from Freebird and Infineon presented in this section.

Figure 3. Freebird Semiconductor FBG20N18B, 200V, 26 mΩ rad-hard GaN FET next to an SO-8 IC package

Figure 4. Intersil ISL70024SEH, 200V, 45 mΩ rad-hard GaN FET [32]

1.5. Research Scope and Objectives

The principal objective of this work is to validate Freebird Semiconductor's FBG20N18B rad-hard GaN FETs in the Phase Shifted Full Bridge topology while achieving a design with high efficiency and power density. The secondary objective is to understand the implications of achieving a practical design of a Phase Shifted Full Bridge DC-DC converter bounded by design

constraints found in space applications. In addition, the converter built in this work shall transition effortlessly into a version with space rated components for further rad-hard qualification testing of the topology. For this, however, the converter designed in this work might require additional circuitry to ensure proper fault protection and fault recovery management. Performance verification the converter under radiation and across temperature is outside the scope of this thesis. Table 7 summarizes the main specifications for the converter implemented in this work.

Table 7. DC-DC Converter Specifications

Parameter	Notes/Conditions	Minimum	Nominal	Maximum
Input Voltage		95 V	100 V	120 V
Output Voltage	Adjustable range	18 V	20 V	24 V
Output Voltage Ripple	0.25 % of nominal V_{OUT}, peak to peak			50m V
Output Power			400 W	500 W
Output Current	$V_{OUT} \leq 18$ V			22.22 A
	$V_{OUT} \geq 18$ V			P_{OUT_MAX}/V_{OUT}
Switching Frequency			500 kHz	
Efficiency Target	V_{IN} = 96.5 V - 100.5 V, V_{OUT} = 18 V, P_{OUT} = 300 W – 400 W	95 %		
Ambient Temperature		-25 °C	25 °C	100 °C
Height	Design goal			15 mm
PCB Area	~90.3 cm^2 (14in^2)			177 mm x 50 mm
Load Capacitance	Extra capacitor added by user at the load	0		300 µF

1.6. Thesis Outline

Pairing new radiation-hardened GaN FETs with topologies capable of achieve high efficiency and power density by better utilization of magnetics—such is the case in half and full bridge based topologies—can yield significant performance improvements for DC-DC converters in space applications. This work seeks to implement a practical design for a Phase Shifted Full Bridge DC-DC converter for space applications using newly released rad-hard GaN FETs. This thesis describes in detail the design considerations to implement the Phase Shifted Full Bridge DC-

DC converter with a Current Doubler Synchronous Rectifier for space applications. Freebird Semiconductor FBG20N18B 200 V, 18 A, 26 mΩ rad-hard GaN FET was selected for the Full Bridge and synchronous rectifier power stages. Converter topology selection, and in depth description of design considerations specific to space power converter applications are included. In addition, this thesis presents complete power-loss breakdown analysis for the selected topology, as well as final design choices to meet converter specifications. A Phase Shifted Full Bridge DC-DC converter prototype incorporating the design considerations outlined in this work was built and evaluated. In addition, a second converter operating as a conventional hard switched Full Bridge DC-DC converter making use of the same rad-hard GaN FETs and synchronous rectifier power stage was built. The performance of the hard switched Full Bridge DC-DC converter was compared against Phase Shifted Full Bridge design for efficiency and component stress.

Chapter 1 presents a brief introduction to radiation effects in power converters, followed by a comparison between commercial and rad-hard MOSFETs, as well as a comparison between commercial and high-reliability space state of the art DC-DC converter solutions. The potential of rad-hard GaN FETs for space power conversion to increase power density and efficiency for state of the art space power conversion, coupled by the use of double-ended topologies like the Phase Shifted Full Bridge is introduced.

Chapter 2 includes the considerations for topology selection, and it presents justifications for selecting a Phase Shifted Full Bridge on the primary side power stage, and a Current-Doubler synchronous rectifier on the output side power stage.

The first part of Chapter 3 describes in detail the design considerations and circuits solutions to implement a practical Phase Shifted Full Bridge DC-DC converter with a Current Doubler Synchronous rectifier for space applications. In particular, this chapter provides details

about isolated GaN FET gate driver design for the bridge and rectifier stages for soft switched and hard switched operation of full bridge based converters. The second part of this chapter provides details on the process followed to design the Phase Shifted Full Bridge converter. This section also includes a description on magnetics design, as well as power loss and efficiency approximation.

Chapter 4 provides details about the implemented hardware prototypes for the DC-DC converter as well as the gate driver boards for the Phase Shifted Full Bridge and Full Bridge converters. In addition, this chapter describes the design considerations followed for printed circuit board (PCB) layout and routing of the DC-DC converter power stage and sensitive auxiliary circuits, with special focus paid to rad-hard GaN FETs paralleling and GaN FET gate driver PCB layout and routing.

Chapter 5 presents all experimental results. Both soft-switched and hard-switched full bridge DC-DC converters were tested with their respective control loops closed to ensure magnetic devices flux balance and stability over load. Chapter 5 demonstrates gate-driver signal integrity for the phase shift modulated controller and the hard-switched controller boards. Power transformer voltage and current waveforms, gate-source control signals for all rad-hard GaN FETs, and efficiency comparisons between hard-switched and soft switched converters with different magnetics constructions are included in this chapter.

Chapter 6 provides a summary of the design, and includes an overall conclusion from the work conducted in this thesis. This chapter also includes suggestions for potential areas of research building up from this work.

Chapter 2 Topology Selection

2.1. Primary Side Power Stage Selection

In this document, *primary side* refers to the input side of a transformer. Table 8 presents a comparison of different options for isolated DC-DC power converters based on the half-bridge and full bridge converter topologies for this application. Any half-bridge based converter topology excite the power transformer to up ± ½ the input voltage V_{IN}. Full bridge based topologies on the other hand excite the power transformer all the way to ± the full DC bus V_{IN}. Therefore, half-bridge based converters have twice the RMS current on the transformer primary side compared to a full bridge based converter. This results in slightly higher efficiency for full bridge based topologies.

Table 8. DC-DC Double Ended Topologies Comparison

Topology	Frequency	Active Switches	Transformer Primary Voltage	Secondary Voltage Stress	Operation
Half Bridge	Fixed	2	$\pm V_{IN} / 2$	$V_{IN} / 2N_{PS}$	Hard-switched
Asymmetrical Half Bridge	Fixed	2	$\pm V_{IN} / 2$	$V_{OUT} / (1-D)$ $V_{OUT} \bullet D$	ZVS, load dependent
LLC Half Bridge	Variable	2	$\pm V_{IN} / 2$	$2 \bullet V_{OUT}$	Wide range ZVS
Full Bridge	Fixed	4	V_{IN}	V_{IN} / N_{PS}	Hard-switched
Phase Shifted Full Bridge	Fixed	4	V_{IN}	V_{PRI} / N_{PS}	ZVS, load dependent
ZVT Full Bridge	Fixed	4	V_{IN}	V_{PRI} / N_{PS}	ZVS, load dependent

There are four main requirements driving topology selection in this work. The first three are the nominal output power requirement of 400 W, maximum input voltage of 120 V, and minimum efficiency of 95 %. To achieve high power density and efficiency, a converter topology capable of achieving ZVS to reduce switching losses due to the 120 V input is preferred. In addition, operating in ZVS reduces EMI of the converter, which is especially important due to the

high *dv/dt* switching transitions achievable with GaN power devices. The fourth important requirement is fixed-frequency operation. Fixed-frequency pulse-width-modulation (PWM) is favored over frequency modulated control schemes in noise sensitive space and military applications. Power converters are the main source of electromagnetic interference (EMI). In military and space applications, it is important to know at which frequencies power converters are running. This allows synchronization of system's power converters oscillators for EMI reduction, and in addition allows for better optimization of local passive and active filtering at the system components. Managing EMI in military and space applications are key requirements to operate highly sensitive instrumentation and RF power amplifiers in space. For this reason, frequency modulated resonant topologies achieving ZVS DC-DC conversion like the LLC are often not desirable in space or military applications.

Based on the four main requirements mentioned, the two topologies suited for this application are the Phase Shifted Full Bridge topology and the conventional Full Bridge DC-DC converter topology. The Phase Shifted Full Bridge has the ability to achieve ZVS yielding high efficiency and lower EMI around medium to full load operation while operating with fixed frequency control. In addition, the small output capacitance C_{OSS} of the selected FBG20N18B rad-hard GaN FETs reduces the amount of circulating energy needed to achieve ZVS operation in the primary side. The main risk of implementing this topology for space power applications lies in the ability to effectively control dead times of the power transistors in the full bridge and synchronous rectifier stages over temperature and aging. For a Phase Shifted Full Bridge, the dead time between the top and bottom devices shown as Q_A and Q_B for one phase leg, and Q_C and Q_D for the other, must be accurately maintained over different operating conditions to avoid shoot-through power losses or catastrophic failures depending on the energy stress level.

The risk of shoot-through is lower in a conventional hard-switched full bridge because all the full bridge switches open during the OFF time, which can add robustness in power converter applications for space at the cost of lower efficiency and higher component voltage stress due to higher voltage ringing from increased *dv/dt* transitions. The Full Bridge converter would also create more EMI, especially if implemented using GaN FETs that have the ability to commutate very fast.

Table 9 and Table 10 present design comparisons between the Phase Shifted Full Bridge and the Full Bridge PWM DC-DC converter as part of topology selection for the primary side. Both converters were simulated at 500 W load, 100 V input, and 20 V outputs with transformer primary to secondary turns ratios set to 1.5 at different switching frequencies. Under the same operating conditions but with switching frequency varied from 200 kHz to 300 kHz, a switching frequency of 250 kHz results in the highest efficiency for the Phase Shifted Full Bridge. On the other hand, a lower switching frequency on the power stage would yield the highest efficiency in the hard switched Full Bridge. This is expected as the switching losses would be much higher in the conventional Full Bridge DC-DC converter. From this comparison, however, the Phase Shifted Full Bridge DC-DC converter running at a 250 kHz transformer switching frequency is the most efficient when compared to the traditional hard switched Full Bridge DC-DC converter under the same operation conditions. This comparison along with the four requirements previously outlined favor the use of the Phase Shifted Full Bridge shown in Figure 5 for this application.

Table 9. Phase Shifted Full Bridge efficiency over frequency at 100 V input, 500W load operation

Phase Shifted Full Bridge			
Power Stage Frequency	200 kHz	250 kHz	300 kHz
Output Voltage	20.62 V	20.65 V	20.58 V
I_{IN} RMS	6.79 A	6.71 A	6.66 A
I_{IN} PEAK	12.22 A	11.03 A	10.56 A
I_{PRI} RMS	8.27 A	8.00 A	7.79 A
I_{SEC} RMS	12.26 A	11.90 A	11.60 A
P_{OUT}	493.25 W	494.84 W	491.41W
P_{IN}	511 W	510.65 W	511.32 W
Efficiency	96.53%	**96.90%**	96.11%

Table 10. Conventional Full Bridge efficiency over frequency at 100 V input, 500W load operation

Full Bridge DC-DC Converter			
Power Stage Frequency	200 kHz	250 kHz	300 kHz
Output Voltage	20.73 V	20.78 V	20.81 V
I_{IN} RMS	7.13 A	7.11 A	7.25A
I_{IN} PEAK	12.78 A	12.33 A	12.15 A
I_{PRI} RMS	7.53 A	7.5029A	7.63 A
I_{SEC} RMS	11.25 A	11.219A	11.423A
P_{OUT}	498.07 W	500.17 W	501.68 W
P_{IN}	517.64 W	520.31 W	523.28 W
Efficiency	**96.22%**	96.13%	95.87%

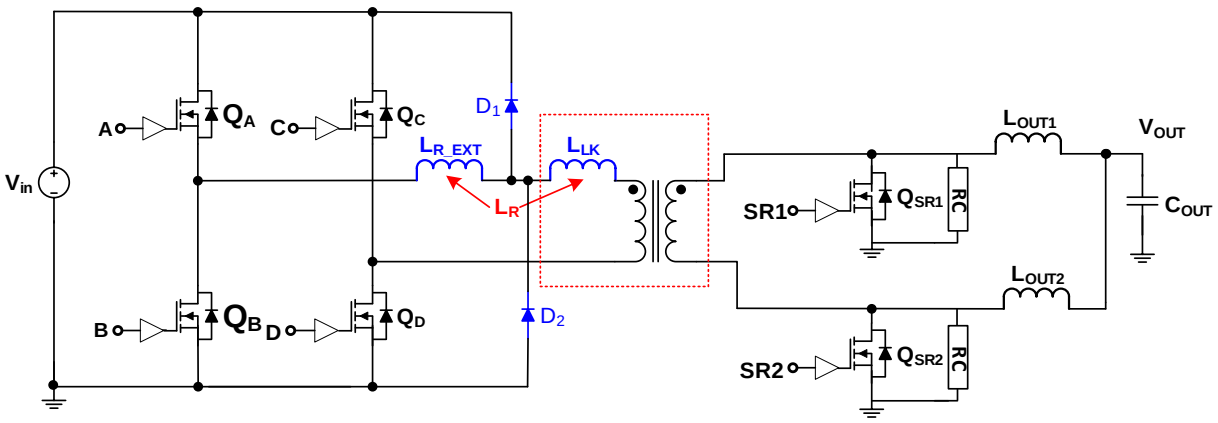

Figure 5. Phase Shifted Full Bridge DC-DC converter with Current Doubler Rectifier

2.2. Secondary Side Rectifier Selection

In this document, *secondary side* refers to the output side of a transformer. There are three full-wave rectifier topologies commonly used with double-ended isolated converters. These are the full wave rectifier using a center-tapped transformer secondary, the full bridge rectifier using four switches, and the Current Doubler rectifier. Figure 6 shows these three rectifier topologies shown with diodes for simplicity.

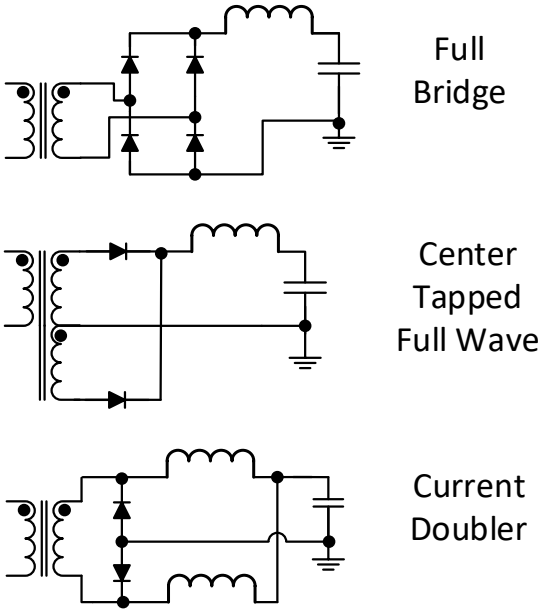

Figure 6. Common output rectifiers for isolated DC-DC converters

Table 11. Physical Comparison of Output Rectifiers

Type	**Full Bridge Rectifier**	**Center-Tapped Full Wave**	**Current Doubler Rectifier**
Secondary Windings	1	2	1
Switches	4	2	2
Gate Drive	High & Low Side	Low Side	Low Side
Complexity	High	Medium	Low
Inductor	1	1	2
Inductor Current	I_{OUT}	I_{OUT}	I_{OUT} / 2

Table 11 summarizes the key physical differences among the output rectifiers described in this section. Maximum output current, efficiency, and design complexity determined the selection of the output rectifier for the DC-DC converter implemented by this work. Table 12 presents a power loss comparison among all three output rectifiers running with a Phase Shifted Full Bridge converter running a 500 kHz PWM control signal (250 kHz on the power stage) to deliver 500 W at a regulated 20 V output from a 100 V DC input. From this comparison, the Current Doubler rectifier yields the highest efficiency for this application.

Table 12. Efficiency Comparison of Output Rectifiers

	Current Doubler	**Full Bridge**	**Center Tapped**
L_{OUT}	6.25 µH, 2 mΩ	3.125 µH, 2 mΩ	3.125 µH, 2 mΩ
Duty Cycle	0.70	0.73	0.70
I_{OUT} Peak to Peak Ripple	4.61 A	4.50 A	4.774 A
P_{OUT}	498.98 W	492.1 W	499.91 W
P_{IN}	532.76 W	561.17 W	536.95 W
Power Loss	33.78 W	69.07 W	37.04 W
Efficiency	93.66%	87.69%	93.10%
Normalization To CDR	1.00	0.94	0.99

The Current Doubler rectifier works similarly to a 2-phase Buck converter. It splits the load current into two inductors, which reduces the size and conduction losses of the output filter. The combined current at the output is two times the transformer switching frequency (F_{SW}), and the multi-phase behavior of the rectifier provides output ripple current cancellation. This results in a smaller RMS current stress in output capacitors, and reduces the amount of output filtering capacitance C_{OUT} required. Another advantage of the Current Doubler rectifier is that it requires a single secondary winding on the transformer. This reduces complexity and allows for better optimization of the power transformer. In addition, synchronous rectification can be implemented with low side (ground referenced) gate drive control signals, which reduces gate drive circuit complexity. Therefore, to reduce complexity of the gate control scheme for the synchronous

rectifier and power transformer design while achieving high efficiency, the Current Doubler synchronous rectifier presented in Figure 7 was selected.

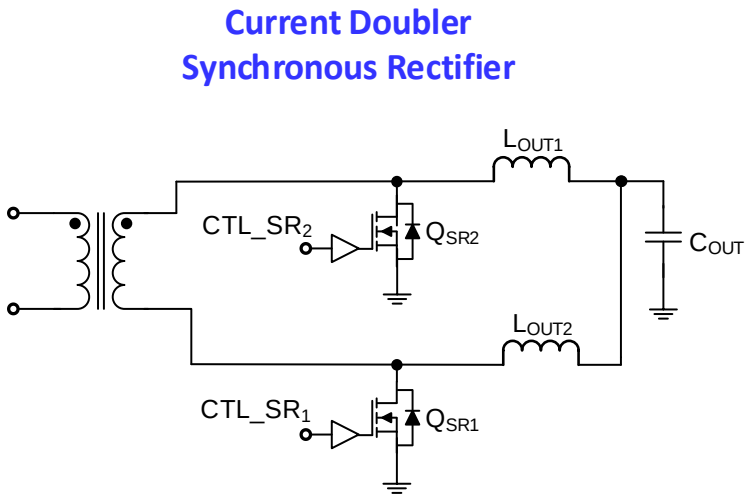

Figure 7. Current Doubler synchronous rectifier

Chapter 3 Isolated DC-DC Full Bridge Converter Design

3.1. Introduction

Space qualified digital controllers to implement control algorithms in a low power converter such as the one in this application add an extra layer of design complexity, qualification testing, and development cost. For practical implementations of low power DC-DC converters for space, an analog controller is usually better suited. Because rad-hard qualified electronic components are limited to elementary integrated circuits, common power converter control features such as under-voltage lockout, soft start, power enable, and current sensing commonly integrated at the silicon wafer level in modern commercial PWM controller chips must be designed externally using discrete components in space applications. These power management auxiliary circuits are usually designed using bipolar junction transistors (BJTs), basic logic gate integrated circuits (ICs), operational amplifiers, comparators, flip-flops, and other similar basic building blocks. In addition, due to the lack of digital isolators and opto-couplers that can work reliably in space, signal isolation must be implemented with pulse transformers. Driving pulse transformers increases the converter footprint not only from the size of the pulse transformers magnetic cores, but also from the additional external circuitry required to drive the pulse transformer correctly.

This limited component availability is a major challenge for space power converter design. The result is a highly complex discrete circuit design that extends engineering development and qualification testing efforts. This section describes the main design considerations related to limited space qualified components for the implementation of the Phase Shifted Full Bridge DC-DC converter topology. The final section of this chapter details the actual process followed to design the DC-DC isolated Full Bridge and current-doubler rectifier power stage. Magnetics

design and magnetic core selection, power loss analysis, and efficiency estimation are also included.

Figure 8 shows a detailed block diagram of the Phase Shifted Full Bridge DC-DC converter in this work. The analog PWM controller is located in the output side (transformer secondary side) to circumvent having an analog feedback signal crossing over the isolation barrier if the controller was placed on the primary side. The reason for this is to reduce circuity complexity by avoiding the use of magnetic feedback to close the control loop. With the PWM controller on the secondary side, only square wave signals to control the full bridge power stage switches need to cross the isolation barrier. Having the PWM controller on the secondary side also has the benefit of allowing for higher control loop bandwidth, which results in faster controller response to output voltage perturbations.

Furthermore, this chapter includes a section detailing the design solution implemented for a hard-switched Full Bridge converter using giant magneto-resistive (GMR) effect digital isolators for control signal isolation. GMR based digital isolators is a technology that has potential to find its way into space power converter applications in the future [33, 34]. Because there are no space qualified GMR isolators yet, a commercial grade GMR digital isolator was used to implement the hard-switched Full Bridge converter in this work [35]. This allows for higher common mode transient immunity (CMTI) such that issues due to the fast hard-switched transitions in the converter are reduced. In addition, the hard-switched Full Bridge operates with a variable duty cycle, adding additional complexity to the gate driver design if a pulse transformer is used for control signal isolation. For the hard-switched Full Bridge implementation, the resonant inductor L_{R_EXT} in Figure 5 is removed and replaced with a jumper, while the clamping diodes D_1 and D_2 in are removed from the circuit.

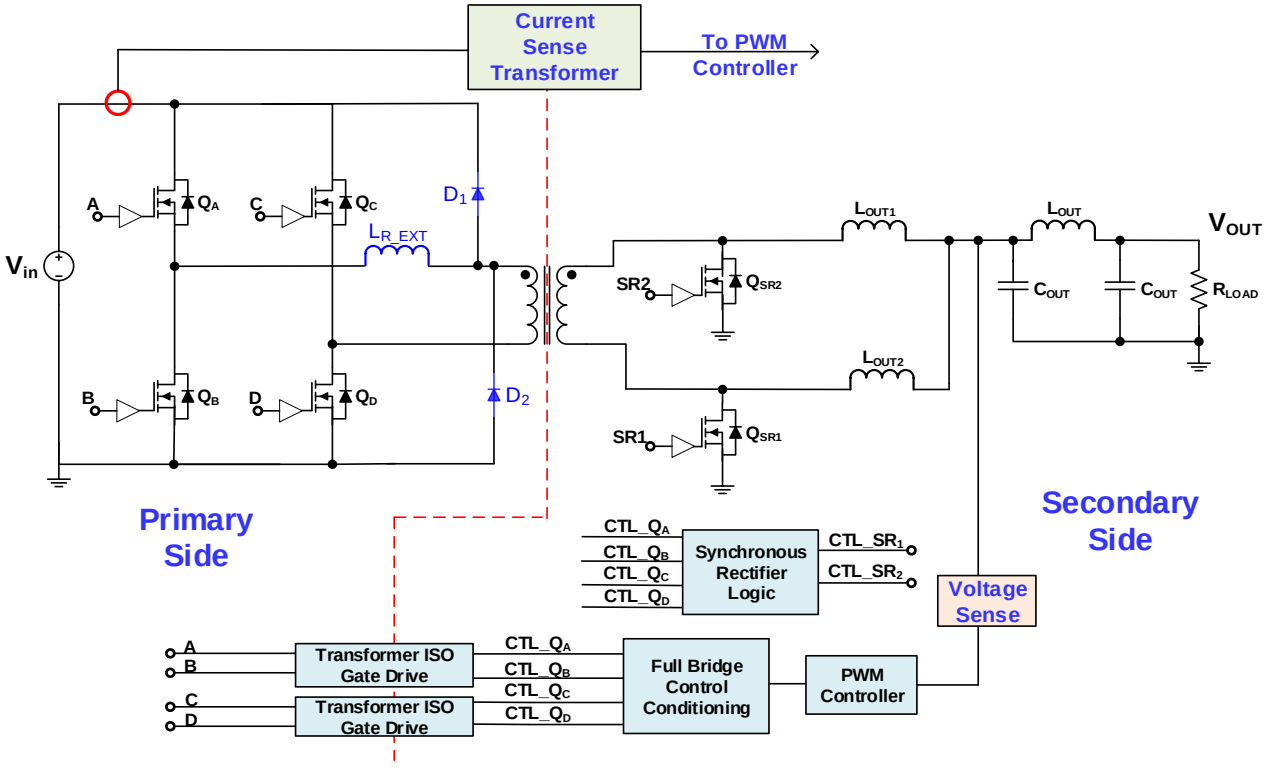

Figure 8. Block diagram for isolated DC-DC converter power stage and control

3.2. General Design Considerations

3.2.1. Signal Isolation for Space Power Applications

An important design challenge arises from the lack of rad-hard qualified digital isolators that can be used with newly released 200 V rad-hard GaN FETs to implement isolated gate drivers for the Full Bridge topology. Rad-hard digital isolators for this application need to have very small propagation delays, fast rise and fall times, and high common mode transient immunity (CMTI). In addition, signal isolation for power converters in space applications cannot be optical in nature. Radiation effects in opto-couplers have been tested in [36-40] with results demonstrating that opto-couplers are not suitable for space applications. One of the reasons is that the opto-coupler's current transfer ratio (CTR) is highly susceptible to displacement damage in space [36, 37]. In

addition, it is widely known in the power converter industry that an opto-coupler's CTR varies a lot due to thermal effects and suffer from degradation over time in terrestrial applications. For this reason, high reliability and mission critical space and military power conversion applications avoid the use of opto-couplers.

Commercial rated digital isolator performance under radiation have been studied in [33, 34] for TID, displacement damage and SEE. These studies concluded that the performance of existing digital isolator technologies under the radiation environments found in space missions is not acceptable [33]. However, GMR based digital isolators have demonstrated good performance up to 120 kRad (Si) for TID, as well as good tolerance to SEE [34]. GMR isolators are magnetically coupled and capable of higher than 70 kV/µs CMTI [35], which makes them a good fit for future isolated gate drivers for new rad-hard GaN FETs used in space applications.

To overcome the lack of suitable opto-coupler and digital isolator solutions, present space power converters use signal or pulse transformers instead. The Phase Shifted Full Bridge in this thesis uses pulse transformers for control signal isolation, while the Full Bridge DC-DC converter implementation uses GMR based digital isolators previously mentioned. Sections 3.3 and 3.5 describe in detail the isolated gate driver design for both converters.

3.2.2. Rad-hard GaN FET Gate Driver

At the start of this work, there were no GaN FET gate drivers qualified for rad-hard space applications. Very recently, Intersil released the ISL70040SEH GaN FET driver for space applications rated for 100 kRad (Si) [41]. The first version of the hardware prototype, however, uses the UCC27611 [42] low side GaN FET driver from Texas Instruments. The UCC26711 shares many similarities with the ISL70040SEH rad-hard GaN gate driver IC from Intersil; therefore, differences between the prototype version and a rad-hard compliant implementation are expected

to be small. Table 13 provides a comparison between the commercially available UCC27611 from TI and the new rad-hard GaN driver from Intersil.

Table 13. Commercial GaN Driver versus Rad-hard GaN Driver

Part Number	**UCC27611**	**ISL70040SEH**
Manufacturer	Texas Instruments	Intersil
Rise Time (1nF C_L)	5 ns	9.8 ns
Fall time (1nF C_L)	5 ns	9.8 ns
Turn ON delay	14 ns to 25 ns	15 ns to 65 ns
Turn OFF delay	14 ns to 25 ns	15 ns to 65 ns
Input High Threshold	1.85 V to 2.25 V	1.7 V to 2.0 V
Input Low Threshold	0.9 V to 1.3 V	1.0V to 1.4 V

3.2.3. Part Procurement and Prototyping Costs

Rad-hard electronic components for space power conversion are not only expensive; they require special procurement and have long lead times. Many industrial rated parts for PWM control, gate drivers, logic gates, amplifiers, comparators, diodes and bipolar junction transistors (BJTs) have similar electrical characteristics to their rad-hard counterparts. This allows using industrial rated parts with rad-hard equivalent versions for prototyping so that costs and procurement times can be more manageable. For this work, special care was taken to determine which circuits could use industrial rated parts instead of their space-qualified versions in the prototype assembly. This careful selection ensures an almost one-to-one relationship to go from basic prototype to a converter prototype than can be tested under radiation. Table 14 presents a list of the main commercial parts selected for this work and their space-qualified equivalents.

Table 14. Commercial Parts Used in Prototype and their Space Version Equivalents

Type	Commercial	Space/Military	Manufacturer
D-Type flip -flop	SN74AHC74	SN54AHC74	TI
NOR Gate	SN74AHC02	SN54AHC02	TI
AND Gate	SN74AHC08	SN54AHC08	TI
Op-Amp	LM7322	ISL70444SEHVF	TI Intersil
Comparator	LM2903	LM139AQML-SP	TI Intersil
NPN BJT	2N2222	JANTXV2N2222AUA	On-Semi Microsemi
PNP BJT	2N2907	JANTX2N2907AUB	On-Semi Microsemi
Silicon Diode	1N4148	JAN1N4148UB	Diodes, Inc. Microsemi
Schottky Diode	BAT54	JANTX1N6677	Diodes, Inc. Microsemi
GaN Gate Driver	UCC27611	ISL70040SEH	TI Intersil
PWM Controller	ISL8840A	ISL78840ASEH	Intersil
Rad-Hard GaN FET	None	FBG20N18B	Freebird Semiconductor

3.2.4. Gate Control for Power Transistors

The Phase Shifted Full Bridge topology has not been widely documented for space power applications. In [43-45] Phase Shifted Full Bridge power modules delivering 1 kW to 10 kW while operating in Boost-mode from a 100 V DC bus to provide 400 V to 500 V outputs for Hall Effect thrusters are described. From [43-45], however, no particular details on complete hardware implementation for are provided, and instead the focus is on providing a detailed discussions of the final power stage performance. Furthermore, [46] explored and developed a useful digital control algorithm for a space application of the Phase Shifted Full Bridge. However, there is no mention of actual hardware implementation to meet space applications requirements. For the DC-DC converter in this thesis, implementing digital control results in a bulkier and more expensive converter and adds an additional layer of qualification testing.

For the practical implementation in this work, an analog controller was determined to be better suited. An analog controller for a Phase Shifted Full Bridge converter qualified to radiation levels of 100 kRad (Si) or more is not currently available. The closest integrated controller for this application is the UC1875-SP available from Texas Instruments [47]. However, this controller is only qualified for a radiation tolerance of 50 kRad (Si) TID. For this reason, phase shift modulation control must be implemented with discrete components consisting of digital logic chips and a basic single-ended PWM controller IC. The targeted PWM IC for this work is the ISL78840ASEH single ended, current mode PWM controller from Intersil [48], with the ISL8840A commercial version from Intersil used for prototyping.

The main parameters considered to implement phase shift modulation control with discrete components are the timing characteristics of all ICs selected to derive control signals for the converter switches. It is important to minimize propagation delays, as well as rise and fall times, such that maximum duty cycle range of the final control solution is achieved. The SN54AHC (SN74AHC commercial) family of digital ICs was selected for flip-flops, AND gates, NOR gates to implement PWM to phase shift modulation (PSM) as well as hard-switched PWM Full Bridge modulation control. The Current Doubler synchronous rectifier control circuitry for the Phase Shifted and Full Bridge DC-DC converters use this family of digital logic ICs as well. The SN54AHC family of logic devices achieves worst-case propagation delays lower than 11 ns when driving a 50 pF load from a 4.5 V to 5.5 V supply over a -55 °C to 125 °C temperature range [49-51] as shown in Table 15. Typical input capacitance of digital logic IC's in this family is only 10 pF at each input pin.

Table 15. SNC54 Propagation Delays at 5V Logic over -55 C to 125 C Temperature

SN54AHC74 D-Type Flip Flop			
	From Input	**To Output**	**Propagation Delay**
low to high delay	CLCK	Q or Q	1ns to 11 ns
high to low delay			1ns to 11 ns
low to high delay	PRE or CLR	Q or Q	1ns to 10.5 ns
high to low delay			1ns to 10.5 ns
SN54AHC08 AND Gates			
	From Input	**To Output**	**Propagation Delay**
low to high delay	A or B	Y	1ns to 9 ns
high to low delay			1ns to 9 ns
SN54AHC02 NOR Gates			
	From Input	**To Output**	**Propagation Delay**
low to high delay	A or B	Y	1ns to 8.5 ns
high to low delay			1ns to 8.5 ns

3.2.5. Analog Control

There are two types of analog control schemes available for this type of application: voltage mode control (VMC) and peak current mode control (PCMC). To keep the volt-seconds applied across the transformer balanced without having to include a DC blocking capacitor on the primary side; both DC-DC converters implemented in this work use Peak Current Mode Control (PCMC). When the flux in the transformer walks towards saturation, the transformer magnetizing inductance decreases causing the primary side current peaks to increase. Peak Current Mode Control ensures the control pulses to the full bridge switches terminate when the transformer primary current peaks increase out of bound during transformer flux imbalances. This ensures the transformer's magnetic flux reduces over the next switching cycle maintaining the core outside of its saturation region. Using PCMC also helps maintain current sharing in the Current Doubler rectifier inductors more symmetrical because the peak currents on both inductors are ultimately controlled by the closed loop system. Figure 9 shows the PWM controller implementation for PCMC, along with auxiliary circuitry for slope compensation and soft start.

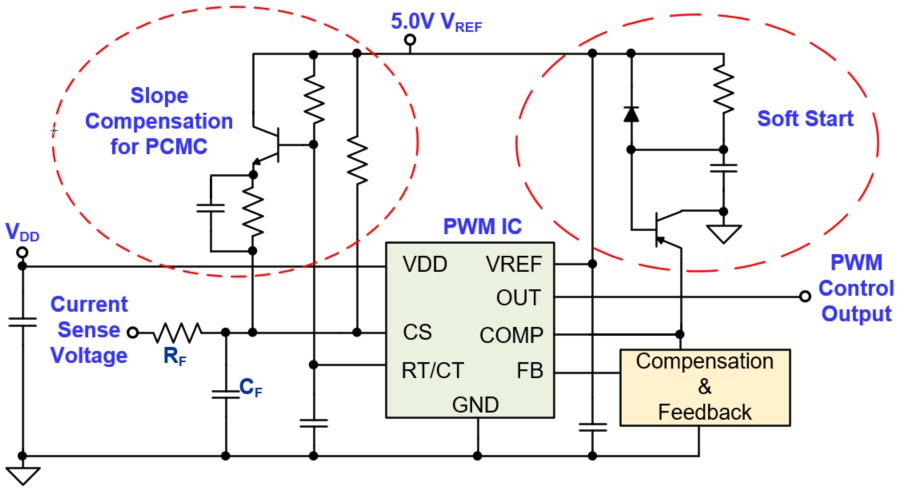

Figure 9. Single Ended PWM Controller and peripheral circuitry

On the contrary, voltage mode control for a Full Bridge based converter would require a high value DC blocking capacitor to maintain the transformer's flux balanced. The DC blocking capacitor value inserted at the primary side of the transformer needs to be greater than 1.0 µF and its final value becomes load depend and open to trial and error during laboratory testing. It is important to avoid using a DC blocking capacitor along with VMC for a Full Bridge based converter with Current Doubler rectifier. This is because balancing the transformer and the two inductors in the Current Doubler rectifier across operating conditions is very hard with VMC. Transformer balancing with a DC blocking capacitor and VMC is even harder to achieve in a conventional PWM hard-switched Full Bridge converter. This is because the resonant inductor in the Phase Shifted Full Bridge will drop some voltage across it, which helps maintain the transformer flux better balanced as the converter load increases.

3.2.6. Current Sensing for Peak Current Mode Control

One important factor of implementing peak current mode control in this topology is the current sensing mechanism used and the location of the current sensor. There are several methods to sense current in a full bridge converter. A common technique involves using a current sense resistor and amplifier to condition the signal sent to the controller. For a Phase Shifted Full Bridge implementation, a common location for the current sense resistor and amplifier is in the DC bus return path, as shown in Figure 10. Placing the sensor and signal conditioning amplifier in this location allows using a low common mode (CM) voltage rated operational amplifier. In this circuit, the gain is set by $\frac{R_F}{R_G}$, and the amplifier must be biased from the PWM controller 5.0 V reference output. However, this current sensing solution requires the PWM controller to be located in the primary side of the isolation, which results in using magnetic feedback to sense the converter output voltage to close the control loop. In addition, to reduce power losses from the current sense resistor, the resistance value must be minimized while considering signal to noise ratio (SNR) and current sense amplifier gain capabilities. Sense resistor values for this specific application would range from 1.0 mΩ to 10 mΩ. Therefore, the resistor sensed current signal must be amplified by a factor greater than 10 and conditioned before it can be sent to the PWM controller.

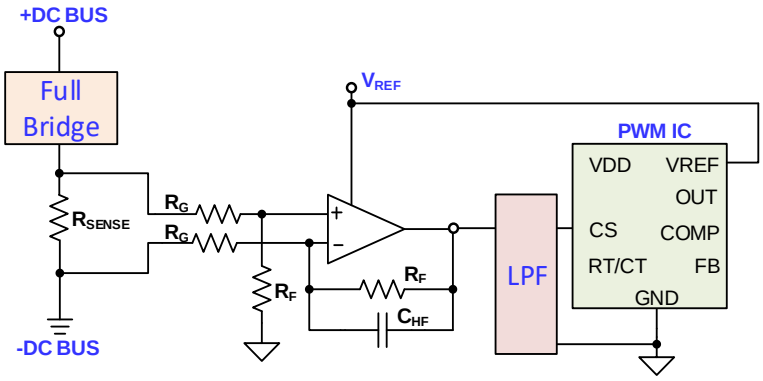

Figure 10. Current sensing on DC bus return path with a sense resistor and op-amp

The sensed current signal frequency and closed loop amplification gain at the inverting input (noise gain) determines the required gain-bandwidth product (GBW) of the amplifier as well as the required amplifier slew rate (SR). Higher noise gain results in a higher GBW amplifier required. For example, the converter in this work runs a PWM oscillator frequency of 500 kHz. Following Nyquist sampling criteria at least twice the signal bandwidth is required by the sampling system, including any low pass filtering, for proper signal resolution. Usually 4 to 5 times the signal fundamental frequency is recommended for signal bandwidth in practical implementations. This sets the frequency content of the measured signal between 2.0 MHz to 2.5 MHz, which for a noise gain of 10 requires a GBW in the amplifier of more than 20 MHz to 25 MHz for proper resolution of the current peaks.

The slew-rate required for the amplifier can be approximated by (1), where *SR* is slew rate in $V/\mu s$ and *NG* is the noise gain of the closed loop. For a GBW from 20 MHz to 25 MHz and a close-loop gain of 10, the minimum SR required from the amplifier is 12.6 $V/\mu s$ to 15.7 $V/\mu s$, respectively.

$$SR \geq 2\pi \frac{GBW}{NG} \tag{1}$$

The difference between using a 10 MHz and 100 M Hz GBW amplifier to condition the sensed current for a Phase Shifted Full Bridge DC-DC converter running a PWM oscillator frequency of 500 kHz is illustrated in Figure 11 from SPICE simulation.

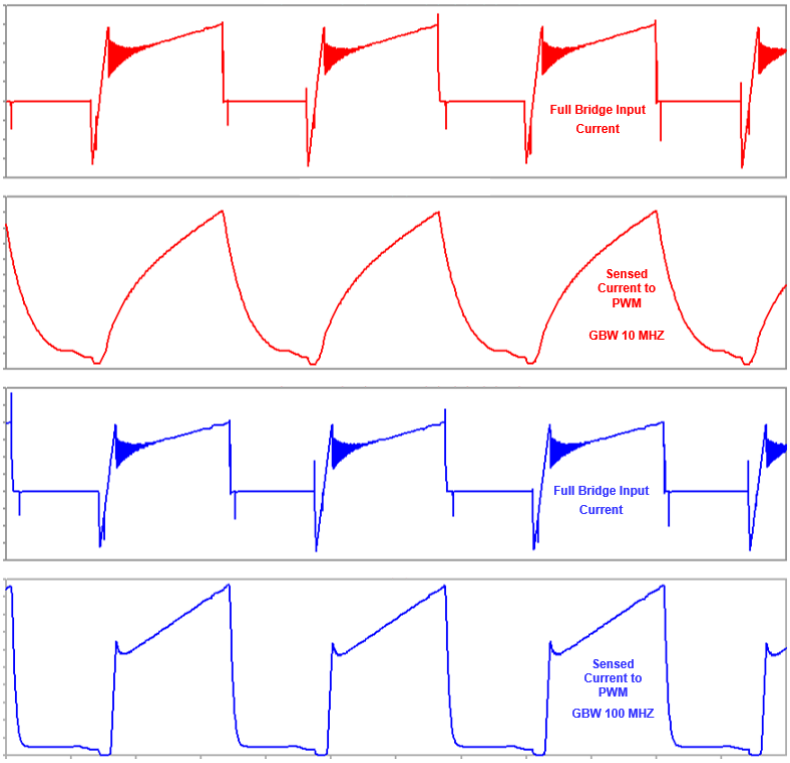

Figure 11. Sensed current output: 10 MHz (red) and 100 MHz (blue) op-amp GBW

Figure 11 illustrates the importance of using a high-speed, high performance amplifier in the current sense circuit to implement PCMC. A rad-hard amplifier with a GBW around 100 MHz or higher, and slew rate capability higher than 16 $V/\mu s$ is recommended for proper peak current resolution if a sense resistor of less than 10 mΩ is used. The LM7322 operational amplifier from Texas Instruments (ISL70444SEHVF rad-hard from Intersil) in Table 14 has a GBW of 20 MHz, which is not high enough for proper current sensing implementation of PCMC in this design. An amplifier better suited for this is the THS4304-SP from Texas Instruments, which has a GBW of 3 GHz and can operate from a supply as low as 2.7 V.

A second way of sensing current for close loop control involves using a current transformer (CT). This solution does not add major losses in the converter and its bandwidth is limited only by the parasitic elements in the current transformer. In addition, a CT does not constrain the location

of the controller to one side of the isolation barrier. The CT sensing solution, however, is bulkier and requires special care to ensure the magnetic core of the CT resets properly.

The preferred location for a CT sensor is the one less susceptible to noise created by the primary side switches in the converter. For instance, sensing the power transformer primary side current is not recommended for a Phase Shifted Full Bridge DC-DC converter. This is because this location places the current sensor in the middle of the noisiest area of the converter. In addition, the primary side transformer current peaks flatten out when the output load current is small so a single well-defined current peak for PCMC cannot be obtained at low loads. To avoid this issue and obtain well-defined current peaks for PCMC implementation, the preferred solution in this application is to have two CT sensors in each of the two half-bridge legs, or a single CT sensor at the DC bus input. The advantage of sensing current at each of the full bridge phase legs comes from the full bridge switches always operating at 50% duty cycle under phase shift modulation; thus, there is always a 50% OFF time for the CT core to reset. The main disadvantage with using two CT sensors is the added real state and the less than optimal high current path layout of the primary side power stage in addition to the added inductance in two high *dv/dt* paths.

Instead, this work uses a single CT located at the DC bus to minimize printed circuit board (PCB) real state without sacrificing the layout integrity of the converter. To extend the duty cycle range of the CT, the converter uses a scheme similar to the forced reset method from [52]. Because using a CT sensor to implement PCMC does not constraint the location of the PWM controller, the analog PWM controller in this work was placed on the secondary side of the transformer isolation. This eliminates the need for the output voltage-feedback signal to cross the isolation barrier via magnetic feedback. Figure 12 shows a schematic of the CT based current sense circuit implemented in this work for both, the Phase Shifted Full Bridge and Full Bridge DC-DC

converters. Figure 13 shows simulation results for the unfiltered CT sensed current compared to the DC Bus input current.

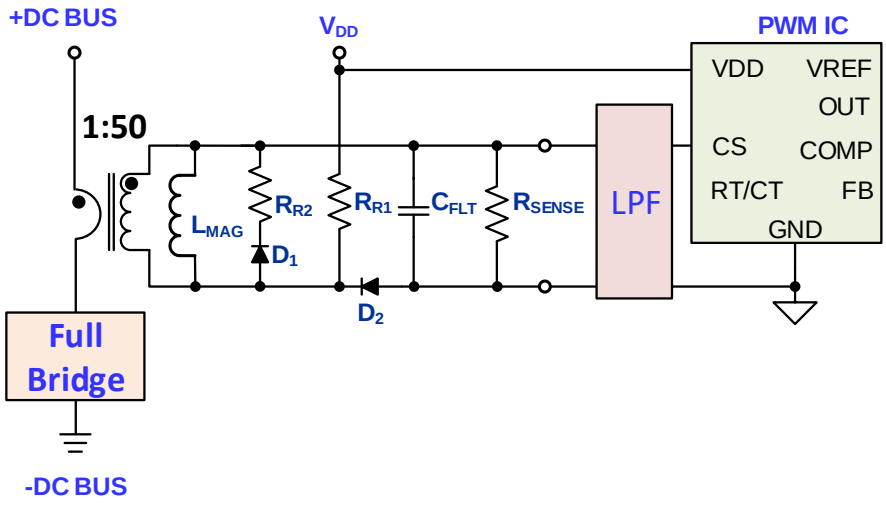

Figure 12. Current transformer with forced reset placed at positive DC bus

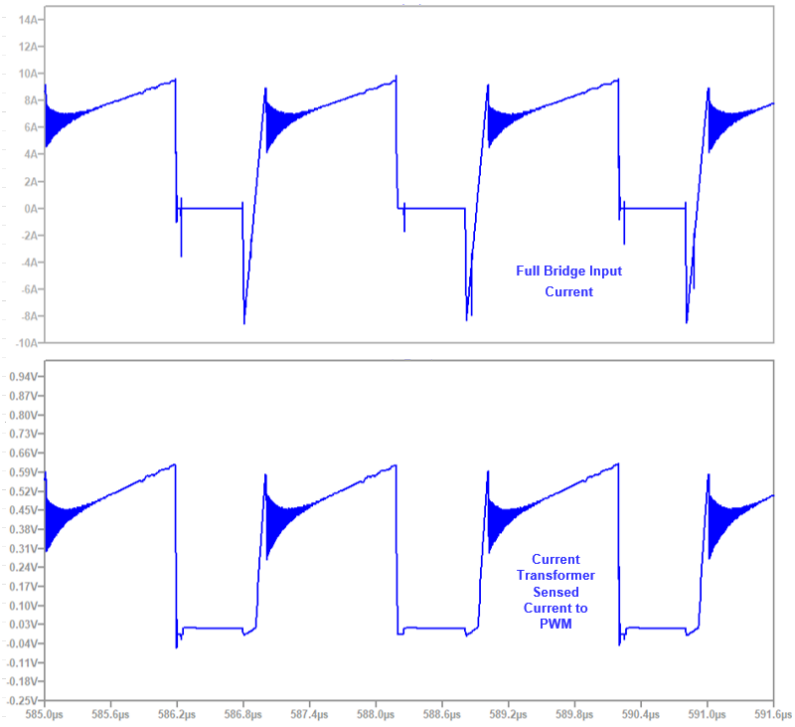

Figure 13. Current transformer sense: DC Bus current (top) and sensed current before low pass filter (bottom)

In the CT based current sense circuit of Figure 12, the magnetizing current increases with the DC Bus input current during the PWM control signal ON time (t_0 in Figure 14). During the PWM OFF time, the current on the DC Bus goes to zero (t_1 in Figure 14) and then negative (t_2 in Figure 14) as the phase shift modulated GaN FETs commutate. During the first portion of the OFF time (t_1 in Figure 14), the magnetizing current built on L_{MAG} decreases and flows through resistor R_{R2} and D_1. At the same time, R_{R1} injects more current into the circuit, which helps reset the transformer. Dead-time circulation causes the DC Bus current into the Phase Shifted Full Bridge to go negative (t_2 in Figure 14), R_{R2} and D_1 catch this negative current while additional current is injected by R_{R1} from V_{DD} to lower the current in L_{MAG} even further. These two mechanisms acting at the same time ensure the CT properly resets during the control signal OFF time. The CT sensor in this application operates with a small DC bias.

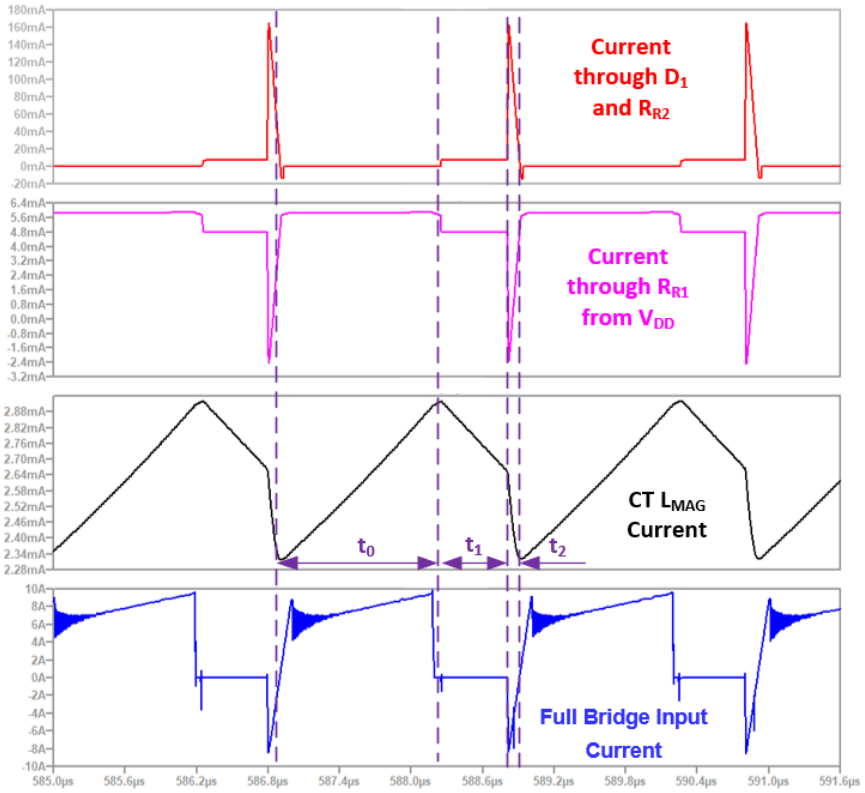

Figure 14. Current transformer sensor reset action during phase shift modulation

Table 16 shows the specifications for the selected core for the CT design. A toroid core is usually used for current sense transformers because of their high permeability since there are no air gaps in this shape. This is important because a high permeability core results in a high value for magnetizing inductance in the CT. This in turn results in a smaller magnetizing current on the secondary side. This magnetizing current combines with the reflected current from the primary side and creates an error in the measurement. Therefore, a small magnetizing current from having a large magnetizing inductance reduces error in the CT.

Common commercial off the shelf (COTS) current sense transformers are usually available with 1:50 and 1:100 turns ratios. For this design, a 1:50 CT was designed to maintain the core size as small as possible resulting from the lower number of turns. To calculate the current transformer magnetic flux density, the standard transformer design equations relating magnetic flux, number of turns, core area, etc. can be used. The following steps and set of equations were used to design the current sense transformer in this work. First, the maximum voltage at the current sense pin of the PWM controller IC V_{CS_MAX} is set to 1.0 V, from the controller datasheet. The approximate peak current of the converter is 11.5 A, with a 30% margin this current becomes 15.0 A. For a 50 turn secondary, the secondary side current on the CT I_{CT_SEC} becomes 0.30 A. Therefore, the sense resistor R_{SENSE} can be calculated using the expression below.

$$R_{SENSE} = \frac{V_{CS\_MAX}}{I_{CT\_SEC}} = \frac{1.0\ V}{0.30\ A} = 3.30\ \Omega \tag{2}$$

Magnetic core cross sectional area A_C can be calculated by setting a maximum flux density B_{CT_MAX} value in the CT magnetic core. For this design B_{CT_MAX} was initially set to 50 mT to account for transient conditions. Core cross sectional area can be calculated using the

volt-seconds relationship below, with the secondary voltage set at $V_{CS\_MAX\ plus}$ the diode voltage drop V_{FW} of 0.7 V at D_2 in Figure 12, and with F_{SW} set as the PWM oscillator frequency (500 kHz). In addition, the calculation is performed assuming the converter is running at maximum duty cycle operation set at 85% for initial calculations. This resulted in a minimum core cross section area A_C of 1.16 mm^2. Therefore, the 0F40603TC from Magnetics, Inc. was selected for this design and its specifications are provided in Table 16.

$$A_C = \frac{(V_{CS\_MAX} + V_{FW})D_{MAX}}{B_{CT\_MAX}N_{CT}F_{SW}} = \frac{(1.0V + 0.7V) \bullet 0.85}{50mT \bullet\ 50\ \bullet 500\ kHz} = 1.16\ mm^2 \quad (3)$$

Table 16. Current Sense Transformer Ferrite Core Specifications

Manufacturer	Magnetics, Inc.
Part Number	0F40603TC
Ferrite Material	F-Type
AL Nominal	1225 nH/T^2
Shape	Toroid
Outer Diameter	5.84 mm
Inner Diameter	3.05 mm
Height	3.18 mm
Cross-section Area, A_C	4.3 mm^2

After selecting a core for the CT, and ensuring windings window area are appropriate, the error in the CT can be calculated by first calculating magnetizing inductance from the core A_L factor of 1225 nH/T$_2$ (3.062 mH) and magnetizing current I_{MAG_CT} as shown below.

$$I_{MAG\_CT} = \frac{(V_{CS\_MAX} + V_{FW})D_{MAX}}{L_{MAG\_CT}F_{SW}} \sim 1\ mA \quad (4)$$

Error in the CT solution can be calculated from I_{MAG_CT} above, and I_{CT_SEC} (initially set to 0.30 A) using I_{MAG_CT} / I_{CT_SEC}. The calculated error is approximately only 0.33%. Table 17 summarizes the CT design specifications.

Table 17. Current Sense Transformer Specifications

Parameter	Designator	Value
Primary Inductance	L_{PRI}	1.225 µH
Secondary Side Inductance	L_{SEC}	3.062 mH
Primary to Secondary Turns-Ratio	N_{PS}	1:50
Primary Number of Turns	N_P	1
Primary Wire Gauge Diameter	18 AWG	1.024 mm
Secondary Number of Turns	N_S	50
Secondary Wire Gauge Diameter	34 AWG	0.16 mm
Primary series resistance	R_{PRI}	0.2 mΩ
Secondary series resistance	R_{SEC}	500 mΩ

3.2.7. Resonant Inductance for ZVS in Phase Shifted Full Bridge

ZVS is achieved when the primary side switches commutate to allow energy stored in the resonant inductance L_R to flow back into the circuit. During this time, the energy stored in inductor L_R in Figure 5 charges towards the DC bus, and discharges towards zero volts the output capacitance C_{OSS} of the top and bottom switches, respectively, in one of the half-bridge legs. This happens in reverse order in each half leg bottom switches, such that all the switches in the Full Bridge power stage achieve ZVS turn ON operation during the effective switching cycle (i.e. twice the PWM oscillator period). The resonant inductance L_R is composed of the transformer primary leakage, L_{LKG}, and any additional inductance L_{R_EXT} added to increase ZVS range, given by (5).

$$L_R = L_{LKG} + L_{R\_EXT} \tag{5}$$

The resonant inductance needed for ZVS, however, creates a phase delay in the converter primary side resulting in loss of duty cycle. An expression for duty cycle loss, ΔD, and detailed analysis for the Phase Shifted Full Bridge converter can be found in [53-56]. Duty cycle loss can be calculated from (6).

$$\Delta D = \frac{L_R \cdot I_{OUT} \cdot F_{SW}}{N_{PS} \cdot V_{IN} \cdot \eta}$$

(6)

Where I_{OUT} is output load current, F_{SW} is the PWM controller oscillator frequency (i.e. twice the power transformer frequency), N_{PS} is the primary to secondary power transformer turns-ratio, V_{IN} is the input voltage, and η is estimated converter efficiency. The PWM controller must command a duty cycle to the full bridge switches that is higher than normally needed to compensate for ΔD. The maximum duty cycle, D_{MAX}, commanded by the PWM controller is given by (7).

$$D_{MAX} = D_{EFF\_MAX} + \Delta D$$

(7)

Where D_{EFF_MAX} is the maximum effective duty cycle seen in the secondary side resulting in output voltage regulation. Maximum effective secondary side duty cycle for a Current Doubler rectifier on the secondary side is defined by (8).

$$D_{EFF\_MAX} = \frac{2 \cdot V_{OUT\_MAX} \cdot N_{PS}}{V_{IN\_MIN} \cdot \eta}$$

(8)

From (6), the amount of duty cycle loss is dependent on L_R, N_{PS}, and F_{SW}, and varies with output current I_{OUT} and input voltage V_{IN} operating points. Increasing L_R increases the amount of energy available to charge and discharge the capacitance in each of the full bridge half legs. However, this has the adverse effect of increasing duty cycle loss, which increases the maximum duty cycle that the PWM controller must command. Converter switching frequency, resonant inductance, transformer turn ratio, and required ZVS range must all be considered when selecting a value of L_R.

Another consideration when selecting a value for L_R is the voltage stress on the secondary side rectifier switches. Resonant inductance, L_R, resonates with the C_{OSS} of the synchronous rectifier power transistors and additional stray capacitances in parallel to these switches, creating ringing that needs to be clamped or snubbed. For this design, the power transformer is designed to minimize leakage inductance, and an external resonant inductor L_{R_EXT} is added to increase the ZVS range of the converter. Two diodes are used as outlined in [57] to recover the energy from the external resonant inductor L_{R_EXT} and circulate it back to the input source. These two diodes are shown as D_1 and D_2 in Figure 5. This mitigates secondary side ringing caused by L_{R_EXT}; therefore, only energy stored in the transformer leakage inductance L_{LKG} is reflected to the secondary side. Because transformer leakage is minimized in this design, it generates well manageable ringing at the output rectifier switches. Minimizing transformer leakage inductance can then allow to avoid additional snubbing or clamping on the secondary side for increased converter efficiency.

Another important factor to consider when selecting L_R relates to the dead-time t_d between switches Q_A and Q_B for the leading leg, and Q_C and Q_D for the lagging leg on the Phase Shifted Full Bridge DC-DC converter of Figure 5. For the converter to achieve ZVS on the primary side full bridge power stage, the maximum dead time t_D cannot exceed more than ¼ of the resonant period t_R of the tank circuit formed by L_R and C_R as defined in (9).

$$t_D \leq \frac{t_R}{4} = \frac{2\pi\sqrt{L_R C_R}}{4} = \frac{\pi\sqrt{L_R C_R}}{2} \tag{9}$$

Where C_R is the resonant capacitance formed by the top and bottom side GaN FETs output capacitance C_{OSS} multiplied by a factor of 4/3 to account for the non-linear variation of C_{OSS} plus any shunt parasitic capacitance from the power transformer expressed as C_{TX} in (10).

$$C_R = 2\left(\frac{4}{3}C_{OSS}\right) + C_{TX}$$

(10)

The dead time selected must be small enough to ensure ZVS operation at required load range, and large enough to account for tolerance of components and variation over temperature and life. For the design implemented in this thesis, dead-times were selected from 35 ns to 45 ns. Section 3.6 describes the power stage design and provides details on the final resonant inductor and dead time values selected for this design.

3.3. Gate Driver Design for Phase Shift Control

Digital isolator selection requirements for isolated GaN FET gate drivers include small propagation delays, fast rise and fall times, and common mode transient immunity (CMTI) from 50 kV/μs to 100 kV/μs [58]. These same considerations must also be accounted when using pulse transformers in lieu of digital isolators for GaN FET gate driver designs for space applications. However, in a pulse transformer based GaN gate driver implementation additional considerations for magnetic flux balance over duty cycle range and transient operation must be included. Furthermore, pulse transformer leakage inductance and magnetizing inductance, as well as pulse transformer primary to secondary parasitic capacitance can all have detrimental effects in integrity of the control signal if these are not carefully considered during the design process.

The 50% duty cycle operation of all the switches in a Phase Shifted Full Bridge DC-DC converter makes this topology especially suitable for a pulse transformer-based control signal isolation. Having the switches operating at 50% duty cycle eliminate concerns of pulse transformer saturation during steady state operation, allowing for a more robust control signal isolation implementation. The proposed gate driver scheme in this work utilizes a combination of pieces from previous work performed for MOSFET gate drivers [59-62] using pulse transformers. The gate driver scheme implemented by this work is distinctive in that it uses pulse transformers to provide control signal isolation for GaN FETs in a Full Bridge power stage, where digital isolators are commonly used.

3.3.1. Proposed Circuit

Figure 15 shows a system-level block diagram of the self-powered gate driver in this work. The Full Bridge power stage switches are labeled as Q_A, Q_B for the leading half-leg, and Q_C, Q_D for the lagging half-leg of the full bridge operating with phase shift modulation.

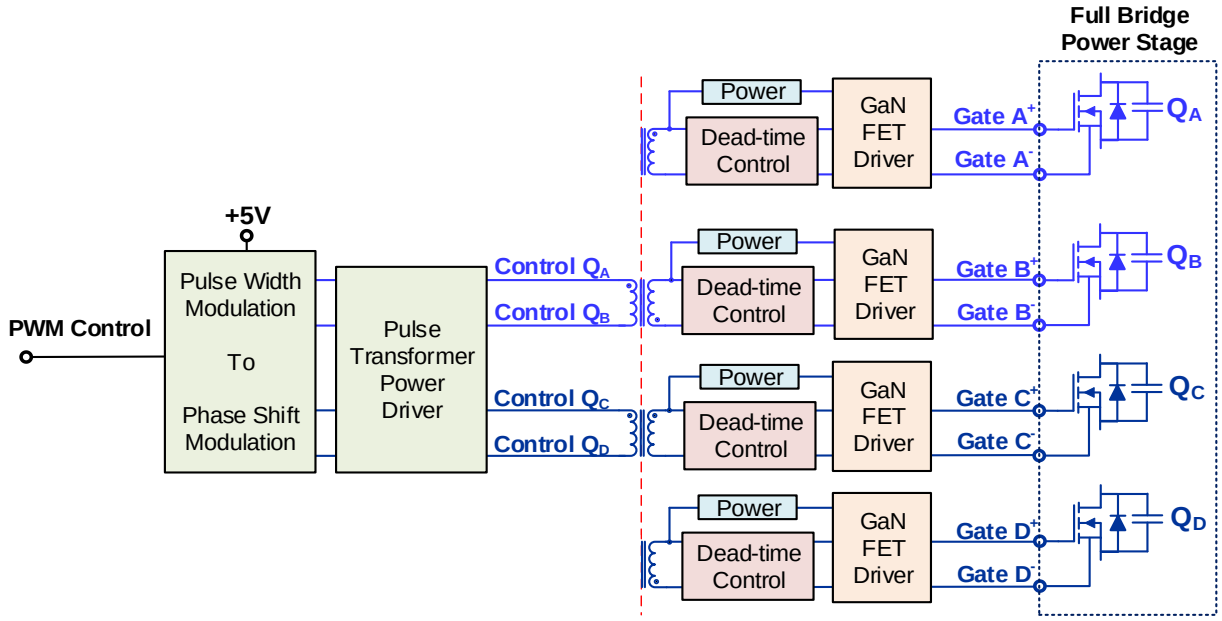

Figure 15. Gate driver block diagram for Full Bridge stage switches A, B, C, and D.

The proposed gate driver is divided into three main subcomponents. The first subcomponent contains circuitry that derives phase shift modulation (PSM) control signals for the Full Bridge power stage from a pulse-width modulation (PWM) control input. The second subcomponent is a bipolar junction transistor (BJT) based power stage that ensures enough energy is delivered to the pulse transformer to bias the GaN gate drivers across the isolation barrier shown in Figure 15. This circuit generates an unregulated voltage to power each of the GaN FET gate driver ICs placed in close proximity to the Full Bridge power stage. The selected GaN FET gate driver IC is described in more detail in the next sections, but the device targeted for this application contains an integrated low-dropout (LDO) linear regulator that ensures the gate-source drive voltage is set to 5.0 V to meet eGaN FETs requirements. The third subcomponent consists of a

half-wave rectifier and dead-time control circuit to condition the control signals driving each of the four Full Bridge power stage GaN FET gate drivers.

3.3.2. Pulsed Width Modulation to Phase Shift Modulation

The self-powered gate driver described in this section takes a PWM signal input and generates six control signals to implement phase shift modulation at the Full Bridge power stage and to drive the Current Doubler synchronous rectifier at the output. There is no integrated rad-hard solution to perform this task and the circuit is implemented with discrete components as shown in Figure 16. PWM to PSM control circuit operation was verified with SPICE simulations. Figure 17 shows the PWM to PSM outputs for the four switches in the Phase Shifted Full Bridge power stage (Q_A, Q_B, Q_C, and Q_D). These simulated waveforms are on the secondary side (PWM controller side); therefore, no dead time is observed in the top and bottom side control signals. Dead time control conditioning is located at the pulse transformer output side, i.e. on the DC-DC converter primary side.

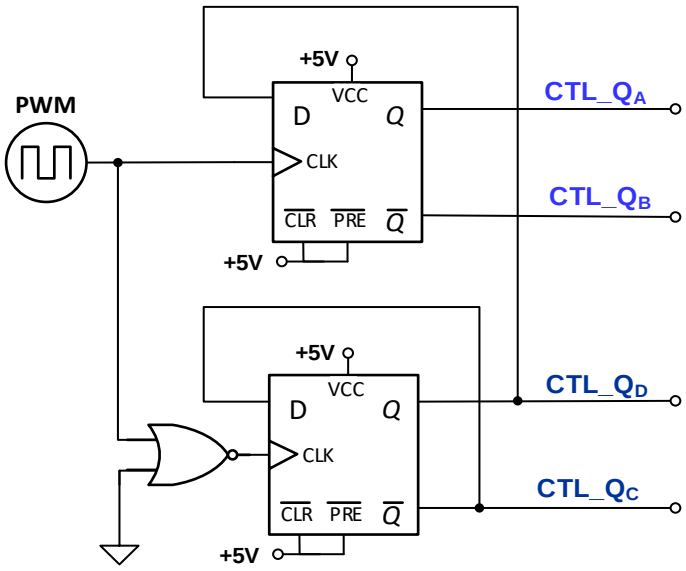

Figure 16. PWM to Phase Shift Modulation circuit for Full Bridge power stage.

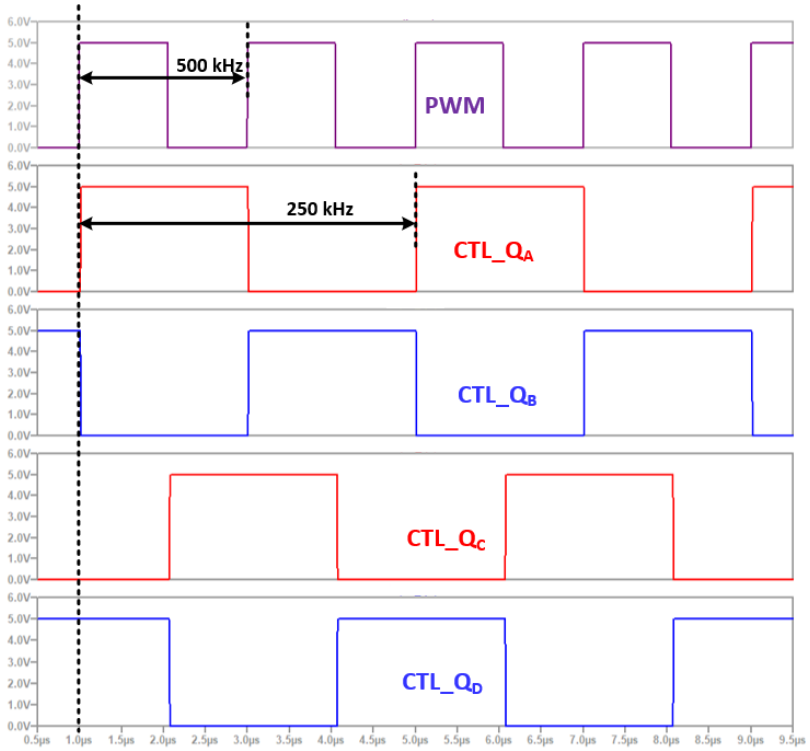

Figure 17. PWM to PSM simulation results from SPICE at 50% PWM duty cycle.

3.3.3. Current Doubler Control for Phase Shifted Full Bridge Converter

Figure 18 shows the circuit designed to derive the control signals for the Current Doubler synchronous rectifier for the Phase Shifted Full Bridge DC-DC converter. Components R_D, C_D, and D_D provide falling-edge delays at the outputs of the GaN gate driver ICs—the rising-edge *RCD* delay becomes a falling-edge due to use of inverting input at GaN gate driver IC. Furthermore, Figure 19 shows the Current Doubler synchronous rectifier control signal timing in relation to the phase shift modulated Full Bridge power stage on the primary side.

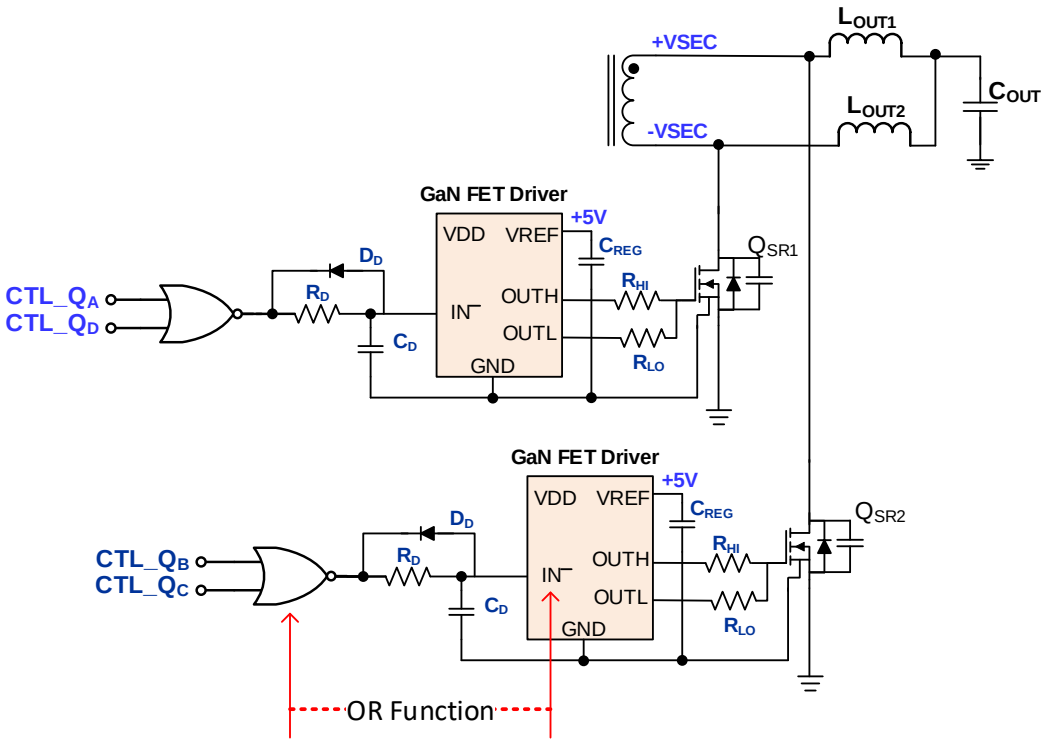

Figure 18. Current Doubler Synchronous Rectifier gate control for Phase Shifted Full Bridge DC-DC converter

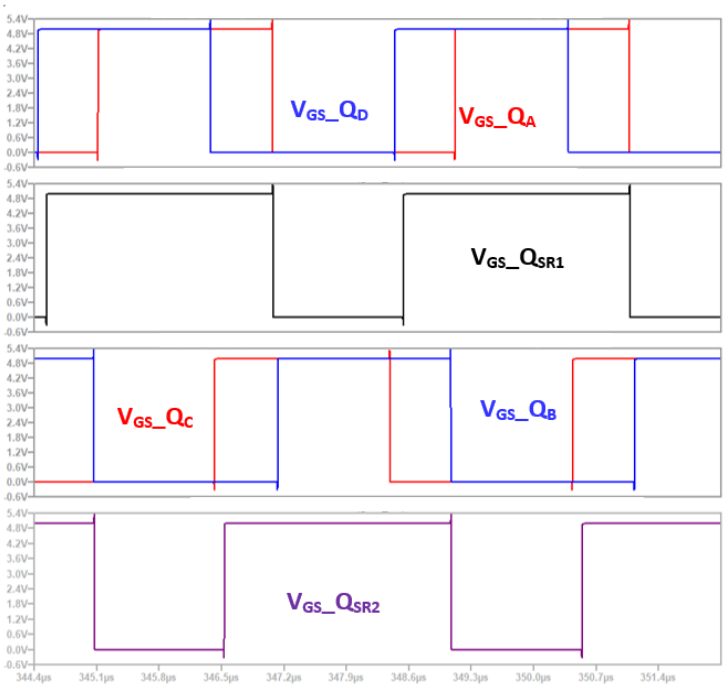

Figure 19. Current Doubler Synchronous Rectifier gate timing for Phase Shifted Full Bridge DC-DC converter

3.3.4. GaN FET Gate Driver Power

The targeted GaN FET gate driver IC for this application, Intersil's ISL70040SEH, contains an integrated low drop-out (LDO) linear regulator to ensure that the rad-hard GaN FETs are driven with a regulated 5.0 V signal. The minimum operating input voltage for the targeted GaN gate driver IC is 4.5V, but it is recommended to use an input voltage higher than 5.0 V to ensure the internal linear regulator operates outside its dropout region. Figure 20 shows the circuit used to provide a higher than 5.0 V input voltage to the GaN gate driver IC in one of the half-legs of the Phase Shifted Full Bridge power stage. The circuit in Figure 20 unburdens the D-Type flip-flops used to generate the control signal logic and ensures that enough energy is available to maintain a steady voltage at the GaN gate driver IC power input.

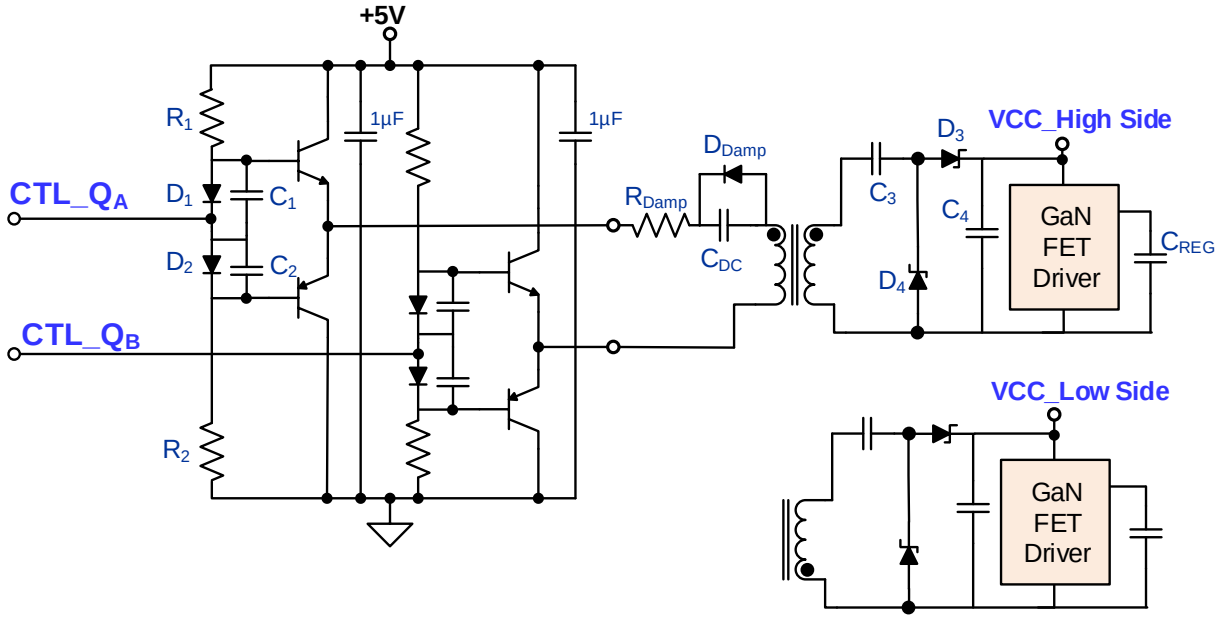

Figure 20. Pulse transformer push-pull power stage and isolated power supply for GaN FET gate driver IC for one half-leg

Furthermore, R_1, D_1, and C_1 as well as R_2, D_2, and C_2 in Figure 20 compensate for base-emitter (V_{BE}) voltage drops across the push-pull power stages, maximizing the voltage level received by the GaN gate driver IC on the opposite of the isolation barrier. The V_{BE} compensation

network uses a 1N4148 diode, 2.2 kΩ resistors at R_1 and R_2, and 10nF at C_1 and C_2. The fundamental operation of the V_{BE} compensation network is that of small voltage source and can be explained by focusing in one of the NPN BJTs pulling the output to the high voltage level. When the signal labeled as CTL_Q_A in Figure 20, for instance, goes low, the 5.0 V biasing supply charges capacitor C_1 through R_1. When the voltage in C_1 is charged to approximately 0.7 V, or one diode drop, D_1 becomes forward biased clamping the voltage across C_1. When the control signal CTL_Q_A transitions to its high state, then C_1 starts discharging primarily through the CTL_Q_A node. The value of R_1 and C_1 must be selected such that C_1 holds enough charge during the high state transition time. In this manner, approximately 0.7 V to 0.6 V are added to CTL_Q_A when this signal goes high making the input at the base of the NPN BJT to swing above 5 V to approximately 5.6 V to 5.7 V. This higher voltage at the base of the BJT is removed when the NPN BJT turns ON, subtracting a V_{BE} voltage of about 0.7 V back from the signal. Therefore, when the control input goes high, the output of the push pull at the emitter junction becomes very close to V_{DRIVE}, in this case 5.0 V. The output peak voltage can estimated from (11).

$$V_{DRIVE} + V_{FW} - V_{BE} - V_{CE\_SAT} \approx 4.8\,V \tag{11}$$

Where V_{DRIVE} is the D-Type flip-flop logic high state voltage level, V_{FW} is a diode voltage drop of 0.7 V, V_{BE} is the base-emitter junction voltage of 0.7 V, and V_{CE_SAT} is the ON state saturation voltage of a BJT of approximately 0.2 V.

The V_{BE} compensation resistor and capacitor were chosen to provide less than ±2% ripple at the high-level output of the push-pull stage as shown by simulation in Figure 21. The same logic applies to the PNP BJTs pulling the output of the push-pull power stages towards ground; but in this case, the input at the base of the PNP BJTs swings lower than ground to about -0.6 V. This is

illustrated in Figure 22 for the control signal path for the topside GaN FET Q_A in the full bridge leading leg.

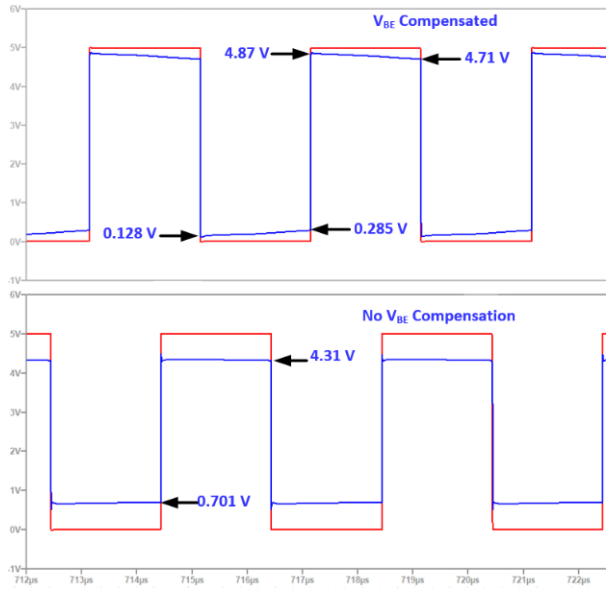

Figure 21. Base-emitter compensated push-pull output (top) versus uncompensated output (bottom)

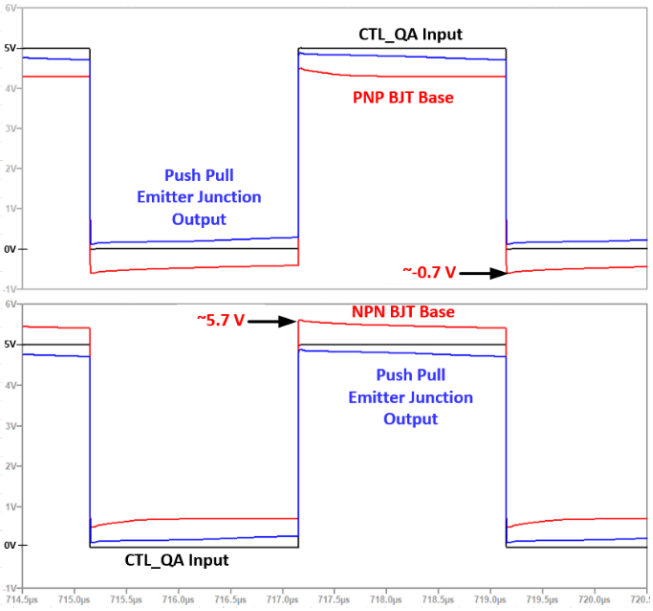

Figure 22. Base-emitter junction compensation signals showing input to PNP (top) and NPN (bottom) BJTs in the push-pull power stage at control signal for GaN FET Q_A

Without compensating for V_{BE} voltage drops, the total push-pull output voltage reduction is two V_{BE} drops, or approximately 1.4 V as shown in Figure 21. Note that a push-pull stage driving a high impedance node (very small current drawn) will not suffer as much from base-emitter voltage drops, only from V_{CE_SAT} voltage drops at its output. In this application, however, current must flow through the push-pull power stage to send energy across the pulse transformer. Therefore, mitigating voltage drops created at the push-pull power stage driving the transformer is important. In addition, the diodes in the V_{BE} compensation circuit can be replaced by a BJT connected as a diode (base connected to collector) using matched BJT pairs for better V_{BE} matching.

To power the GaN gate drivers for the top and bottom side GaN FETs in each of the Full Bridge half-legs, the design uses a voltage doubler rectifier formed by the capacitors C_3 and C_4 chosen as 1µF, and BAT54 Schottky diodes D_3 and D_4 selected to minimize voltage drops. Figure 20 shows these components. With 5.0 V logic at the D-type flip-flops, the voltage generated to bias the GaN gate driver IC after V_{BE} compensation can be approximated as:

$$V_{BIAS} = 2\,(V_{DRIVE} - 2\,V_{CE_{SAT}}) - 2V_{FW\_SCHOTTKY} \tag{12}$$

Where V_{BIAS} is the voltage generated to power the GaN gate driver IC, V_{DRIVE} is the digital logic level used to excite the pulse transformer, in this case 5.0 V, V_{CE_SAT} is the saturation voltage of the BJT approximated at 0.20 V, and $V_{FW\_SCHOTTKY}$ is the Schottky diodes D_3 and D_4 forward voltage drop approximated as 0.3 V. From (12), V_{BIAS} becomes approximately 8.6 V. This voltage is sufficient to maintain enough charge delivered to the GaN gate driver IC internal LDO linear regulator output capacitor C_{REG} and selected at 1.0 µF for this work. The current and power that the gate driver circuit must provide to turn ON and OFF the rad-hard GaN FETs used in this application can be calculated from (13).

$$P_{DRIVER} = I_Q V_{DD} + 2Q_G V_{REF} F_{SW} \tag{13}$$

For two rad-hard GaN FETs in parallel, the gate capacitance is 12 nC [31], while the quiescent current for the gate driver is about 180 µA. This results in 31 mW of power at each GaN FET gate driver IC on the full bridge power stage. Each leg of the Current Doubler synchronous rectifier in this design uses four rad-hard GaN FETs in parallel. The gate capacitance at each leg is 24 nC, which results in a power demand of approximately 61mW per leg. The total power demand for the six GaN FET gate drivers in the converter is 246 mW, putting an approximate total load of 50 mA at the self-powered gate driver board 5.0V power supply.

3.3.5. Control Signal Conditioning and Dead-time Control

The control signal at the GaN gate driver side is bipolar in nature and half-wave rectification is necessary to block the negative voltage part of the signal (with respect to GaN driver ground) at the Full Bridge power stage. In addition, the dead-time control components were placed at the GaN gate driver IC input to take advantage of the built-in Schmitt trigger at the control input of the GaN gate driver IC. For this application, rising-edge delays were used at each of the four rad-hard GaN FETs in the full bridge. In addition, falling-edge delays were used at each of the two rad-hard GaN FETs in the Current Doubler rectifier for the Phase Shifted Full Bridge. On the other hand, rising-edge delays were used at each of the Current Doubler rectifier legs in the hard switched Full Bridge DC-DC converter design.

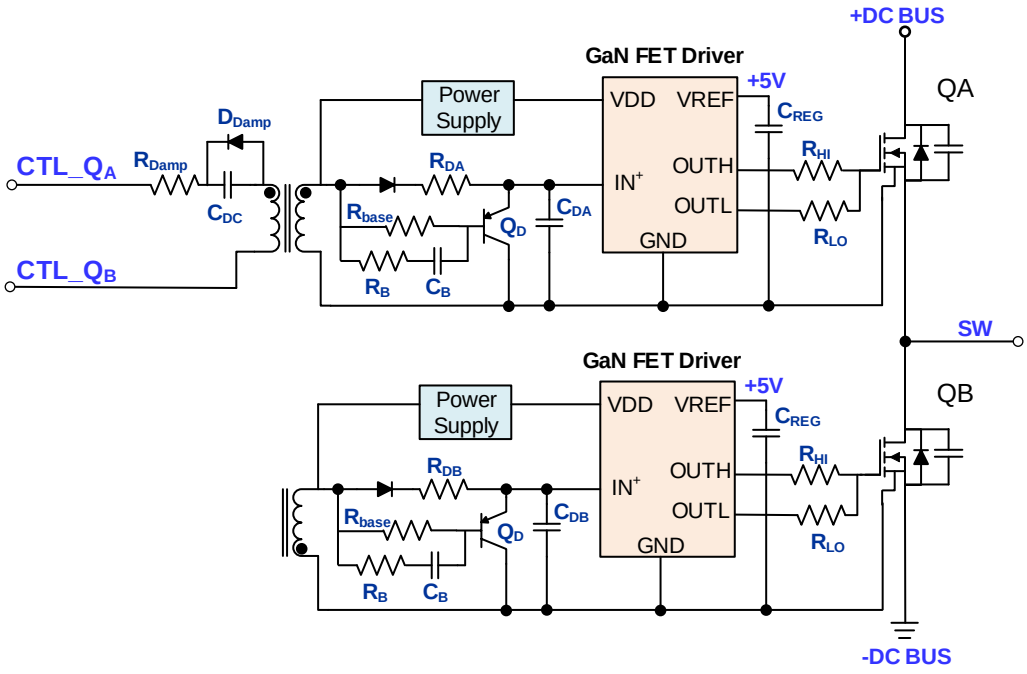

Figure 23. Control signal conditioning with PNP BJT fast turn OFF for one of the Full Bridge half-legs

Figure 23 shows the control signal conditioning circuit implemented in this work. The diodes in series with R_{DA} and R_{DB} block the negative piece of the control signal from the pulse transformer output. The PNP BJT allows for fast discharge of C_D when the control signal goes low, which in turn reduces turn OFF propagation delay.

Two considerations are important for the control signal conditioning circuit of Figure 23. The first one is related to using Q_{DA} and Q_{DB} as switches to discharge their corresponding C_D delay capacitors. To drive a BJT into saturation, a surge of charge current needs to be delivered to the transistor base, turning ON the device almost instantly. This base charge, however, needs to be removed for the device to turn OFF. If charge at the base of the BJT is not removed fast enough, then there is a propagation delay introduced. This can be solved with a Baker Clamp configuration or similarly by the introducing an additional base current path formed by R_B and C_B in Figure 23.

In this manner, additional charge stored in C_B is delivered to the base of the PNP BJT Q_D to speed up its turn OFF. Resistor R_B limits the amount of charge stored in C_B and delivered into the base of PNP BJT Q_D.

There second consideration in implementing the control signal-conditioning network of Figure 23 is related to achieving accurate dead time at the top side GaN FETs. The delay capacitor C_{DA} is referenced to the half-leg switch node SW. This node is tied to the source terminal of the high-side switches in the Full Bridge power stage and dynamically changes from zero volts to the DC bus voltage. The high *dv/dt* at this node can results in C_{DA} discharging if its capacitance value is too small. The initial value for this capacitor was initially set to 100 pF, but this proved to be too small for the fast rise and fall times of the rad-hard GaN FETs used in this design. With a 100 pF C_{DA} and a 1.0 kΩ R_{DA}, not enough charge can be stored and supplied into C_{DA} fast enough to maintain the input to the GaN gate driver from drooping and going negative. This problem is exacerbated as the input voltage to the converter rises, and it is worst at maximum input voltage. In addition, dead time variation with a low value C_{DA} and high value R_{DA} is also dependent on the converter output load, regardless of ZVS operation. This is because more current flows through the source node of the top side GaN FET (Q_{BA} in this case) and discharge C_{DA} faster as the output load of the converter increases, creating energy build up at the resonant inductor and a fast *dv/dt* transition at the switch node.

Increasing the value of C_{DA} and reducing the value of R_{DA} was required to achieve accurate dead time intervals for the top side rad-hard GaN FETs in the full bridge converter design of this work. The only caution for this is that the gate driver pulse transformer now has to drive higher current surges to maintain the increased C_{DA} capacitance charged so that the input to the GaN FET gate driver remains undistorted. Therefore, the impedance from the pulse transformer secondary

to the input of the dead time delay circuit must be reduced to allow enough current to charge C_{DA} faster than the current from the half-leg switch node discharges it.

A better way of mitigating this problem is by splitting the ground connection of the control signal from the ground connection of the GaN gate driver IC, which is also the source or gate return connection of the rad-hard GaN FET. Then, both connections can be kept at the same voltage potential in the printed circuit board (PCB) via a small trace (i.e. higher impedance trace). This will effectively separate the source/gate-return current from the ground current at the GaN gate driver IC input. Ideally, the silicon artwork of the GaN FET gate driver IC should provide two separate pins: one for the GaN FET gate-return or source connection to drive the FET and one for gate driver IC ground connection. In the PCB designed for in this work, the rad-hard GaN FET gate return (source) and GaN gate driver IC ground paths were connected with a small power plane to reduce parasitic inductance. The top side GaN FET dead time delay capacitor C_{DA} was connected to this low impedance gate return plane, which in turn caused problem described. This problem is not present in the low side switches because the GaN driver IC ground node is always fixed to zero volts.

3.3.6. Pulse Transformer Design Considerations

Figure 24 shows an equivalent circuit model for the pulse transformer that includes its parasitic elements. In this equivalent circuit, the magnetizing inductance is labeled as L_{MAG}, primary winding resistance is R_{PRI}, secondary winding resistance is R_{SEC}, transformer leakage inductance reflected to the primary side is L_{LK}, parasitic shunt capacitance from secondary side loads and windings is labeled as C_{PAR}, and primary to secondary inter-winding capacitance is labeled as $C_{I/O}$. In addition, the primary and secondary number of turns are N_P and N_S, respectively.

The pulse transformer turns-ratio is set to 1:1 to increase coupling coefficient and decrease leakage inductance.

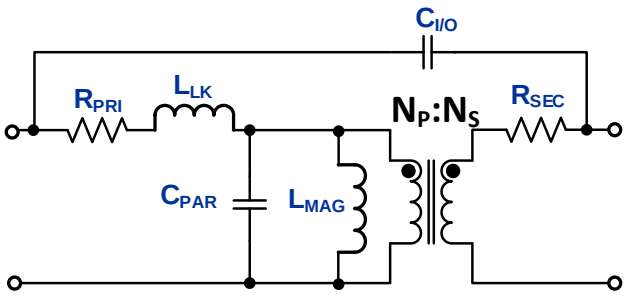

Figure 24. Pulse transformer equivalent circuit model

The inverting and non-inverting outputs of the D-Type flip-flops in Figure 20 provide the pulse transformer with a bipolar voltage excitation. This would create a DC voltage bias at the pulse transformer input side (primary) if the PWM input signal goes low for a few switching periods or during startup and shutdown. To avoid saturating the pulse transformer a DC blocking capacitor C_{DC} was added to the circuit shown in Figure 20. This capacitor also changes the damping factor for the tank resonant circuit created in conjunction with L_{MAG}.

The amount of voltage droop on the secondary side of the pulse transformer depends on the amount of magnetizing inductance L_{MAG}. Percent voltage droop can be approximated with (14), where K is a constant quantifying resistive loading effect from series and parallel terminations at the secondary side of the transformer, R_{OUT} is the transformer driver output resistance, D is the control signal duty cycle, and T_{SW} is the control signal switching frequency [63]. From (14), voltage droop minimization at the pulse transformer output requires an increase of L_{MAG}. This in turn requires increasing C_{DC} to obtain sufficient damping to prevent low frequency ringing at the pulse transformer output during startup and shutdown transient events.

$$\% V_{DROOP} = 100 \cdot \frac{K R_{OUT} D T_{SW}}{L_{MAG}} \tag{14}$$

In addition, R_{DAMP} in Figure 20 can be used for additional damping of the L_{MAG} and C_{DC} tank circuit at the expense of introducing extra power losses. The output resistance driving the pulse transformer, R_{OUT} in (14) then becomes R_{SOURCE}+R_{DAMP}. The value of R_{DAMP} can be calculated from:

$$Q = \frac{1}{R_{DAMP} + R_{SOURCE}} \sqrt{\frac{L_{MAG}}{C_{DC}}} \tag{15}$$

For critical damping, $Q = \frac{\sqrt{2}}{2}$ and the expression in (15) for R_{DAMP} becomes equals to:

$$R_{DAMP} = \sqrt{2 \cdot L_{MAG}/C_{DC}} - R_{SOURCE} \tag{16}$$

Furthermore, the added voltage doubler capacitors used to generate a bias voltage for the GaN FET gate driver chip can also increase the amount of low frequency ringing at the control signal. The diode D_{DAMP} shown in Figure 20 can be included to allow the tank circuit current to resonate only in one direction. With D_{DAMP} present, the control signal voltage only rings in the positive direction and can settle faster.

A very important consideration for the gate-drive pulse transformer design lies in the number of turns selected and the winding method used. The number of turns in the pulse transformer and the winding method directly affect the amount of input to output capacitance across windings $C_{I/O}$, as well as the amount of leakage inductance L_{LK} obtained. Input to output capacitance $C_{I\backslash O}$ governs the common transient immunity (CMTI) that can be obtained from the pulse transformer. From [64] and [58] a CMTI of 50 kV/µs to 100 kV/µs is recommended for wide

bandgap (WBG) devices such as GaN FETs. The input-output parasitic capacitance $C_{I/O}$ can be measured with an impedance analyzer or with a high quality LCR meter by shorting the primary and secondary windings and measuring the capacitance across the two shorted-winding terminals as shown in Figure 25.

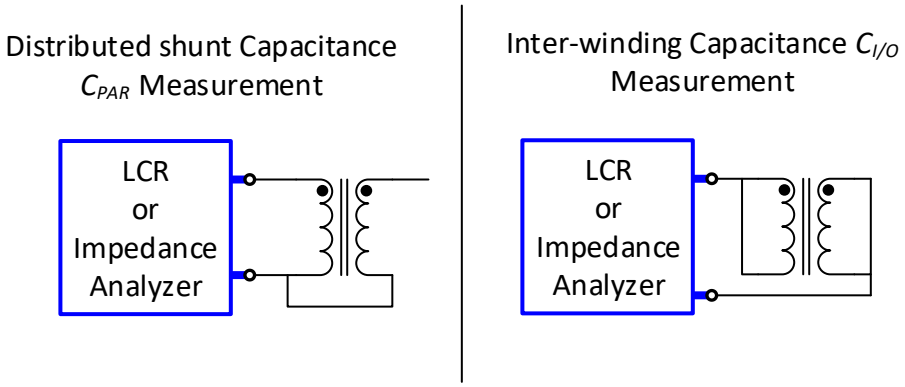

Figure 25. Pulse transformer parasitic capacitance measurement setup.

Knowing the switch-node voltage rate of change, the current injected back into the control circuitry can be approximated with the standard capacitor current to voltage relation provided in (17). The control circuit driving the pulse transformer must be able to sink this current. For this design, the bipolar push-pull BJT stage shown in Figure 20 provides at least 0.5A sink and source capability to drive the pulse transformer.

$$i_{CM} = C_{I/O}\frac{dV}{dt} \tag{17}$$

Finally, it is very important to reduce the amount of leakage inductance L_{LK} to avoid excessive ringing and to reduce propagation delay across the pulse transformer. The relation between L_{LK} and time delays can be understood from the fact that inductance opposes the flow of AC current, increasing the AC impedance in the signal path. This increased impedance resonates with parasitic shunt capacitance C_{PAR} in the pulse transformer creating ringing with a time constant

defined by L_{LK} and C_{PAR} influencing how fast the control signal voltage can transition from high to low and vice versa. Figure 25 shows the method to measure the pulse transformer distributed shunt-capacitance C_{PAR}.

3.4. Pulse Transformer Design

This section describes the design of the pulse transformer design. The first step is to select the number of turns based on maximum flux density with a 1:1 turn ratio. The pulse transformer in this application operates with a bipolar square wave excitation of ±5 V running at 50% duty cycle, and with a switching frequency of 250 kHz. Pulse transformer core flux density is selected such that enough margin exists to avoid core saturation during transient events or when the PWM signal is high or low for several switching cycles. For this design, it is set to 100 mT maximum for steady state operation. A high frequency ferrite core material from Magnetics, Inc. was selected [65], with its main parameters summarized in Table 18

Table 18. Pulse Transformer Ferrite Core Specifications

Manufacturer	Magnetics, Inc.
Part Number	0J40705TC
Ferrite Material	J-Type
AL Nominal	3758 nH/T^2
Cross-section Area, A_C	9.9 mm^2

Maximum flux density B_{MAX} can be calculated from the number of turns N_P, applied volt-seconds, switching period T_{SW}, and core effective cross-sectional area A_C using (18).

$$B_{MAX} = \frac{V_{HIGH} D T_{SW}}{N_P A_C} \tag{18}$$

Where V_{HIGH} is 5 V from the D-Type flip-flop logic voltage driving the pulse transformer. From (18) 10 turns on the primary and secondary are needed to keep B_{MAX} to about 100mT. This

also gives a primary magnetizing inductance L_{MAG} of 376µH from the core's datasheet inductance factor A_L. After calculating L_{MAG}, magnetizing current I_{MAG} can be calculated using (19).

$$I_{MAG} = \frac{V_{HIGH} D T_{SW}}{L_{MAG}} \tag{19}$$

The magnetizing current flowing through the gate driver circuit has a triangular shape due to the square wave voltage excitation at the pulse transformer, and has a peak value of 27 mA from (19).

The self-powered isolate gate driver designed in this this work for the Phase Shifted Full Bridge converter uses two pulse transformers for each of the phase legs. Each pulse transformer contains three windings: one primary and two secondary as shown in Figure 15. Each of the windings in the pulse transformers are wounded using 34 AWG magnet wires in a trifilar manner to reduce leakage inductance L_{LK} and input-output inter-winding capacitance $C_{I/O}$ (from small wire diameter). Since the transformer turns-ratio is set to 1:1, primary winding resistance R_{PRI} and secondary winding resistance R_{SEC} are the same. The 34 AWG wire selected has a nominal diameter of 0.16 mm. Winding DC resistance value can be calculated using (20).

$$R_{PRI} = R_{SEC} = \rho \frac{W_{LENGHT}}{W_{AREA}} \tag{20}$$

Where Annealed-Copper resistivity at room ambient temperature is defined as $\rho = 1.72 \times 10^{-8}$ Ωm, W_{LENGHT} is the total winding wire length in meters, and W_{AREA} is the wire's cross-sectional area in meters squared. The winding resistance value from (20) is 0.171 Ω at room ambient temperature. Moreover, a 1.0 µF C_{DC} is selected based on simulation and bench testing results. This value did not require an additional series-damping resistor R_{DAMP}. Therefore, neglecting loading effects from shunt impedances, series termination resistances and winding resistances the value for K in (14) can be set 1.0. Thus, the expected percent voltage droop with an L_{MAG} of 376

µH is 1.06%. This calculated percent voltage droop is small and validates the core size and number of turns selected for the pulse transformer design. Table 19 summarizes the calculated parameters for the pulse transformer.

Table 19. Calculated Pulse Transformer Parameters

Parameter	Designator	Value
Primary Inductance	L_{MAG}	376 µH
Magnetizing Current	I_{MAG}	26.6 mA
Number of Turns	$N_P : N_S$	10: 10
Wire Gauge Diameter	34 AWG	0.16 mm
Primary series resistance	R_{PRI}	0.171 Ω
Secondary series resistance	R_{SEC}	0.171 Ω
% Voltage Droop	$\%V_{DROOP}$	1.06 %
Flux Density Swing	BMAX	101 mT

3.5. Gate Driver Design for Full Bridge Control

This section describes the implementation for the isolated gate driver for a conventional hard-switched Full Bridge DC-DC converter. The power stage and control layout for this design is the same as the one shown in Figure 8 for the Phase Shifted Full Bridge DC-DC converter implementation. The main exceptions come from L_R being defined only as the power transformer leakage inductance, i.e. no external inductor is added to this configuration. In the prototyped power stage, the PCB footprint pads for L_{R_EXT} were shorted when running the power stage as a hard-switched Full Bridge DC-DC converter. In addition, clamping diodes D_1 and D_2 shown in Figure 8 must be removed from the power stage for proper operation. The gate driver for the hard-switched Full Bridge DC-DC converter implemented in this work uses similar circuits as the ones for the Phase Shifted Full Bridge gate driver, with some major differences highlighted in this section.

3.5.1. Full Bridge DC-DC Converter PWM Control

Full Bridge DC-DC converter control for PWM can be derived from the circuit of Figure 16, with two AND logic gates used to derive signals for the full bridge switches. During the first part of the switching cycle in a conventional Full Bridge, switches Q_A and Q_D turn ON at the same time to apply the positive DC Bus to the power transformer primary during PWM control ON time given by $D \cdot T_{SW}$. Then all four switches in the Full Bridge stage remain OFF during $(1-D) \cdot T_{SW}$ to complete ½ of a cycle. During the second half of the cycle the negative DC Bus is applied across the power transformer primary by turning ON switches Q_B and Q_C during the second PWM control ON time $D \cdot T_{SW}$, and then all switches are turned OFF during $(1-D) \cdot TSW$ period to complete a full cycle. The power transformer effective frequency is ½ of the PWM oscillator frequency. Figure 26 shows the circuit designed to implement the control logic for the hard-switched Full Bridge power stage. Figure 27 demonstrates the control signal timing obtained via SPICE simulation showing the PWM control signal input to the Full Bridge gate driver and the gate control signal outputs to drive all four FETs in the Full Bridge power stage.

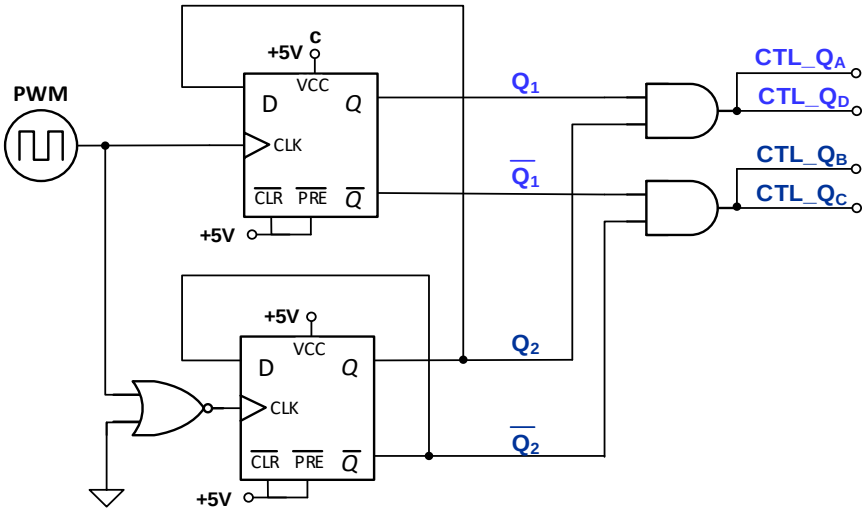

Figure 26. PWM control signal derivation for Full Bridge DC-DC converter

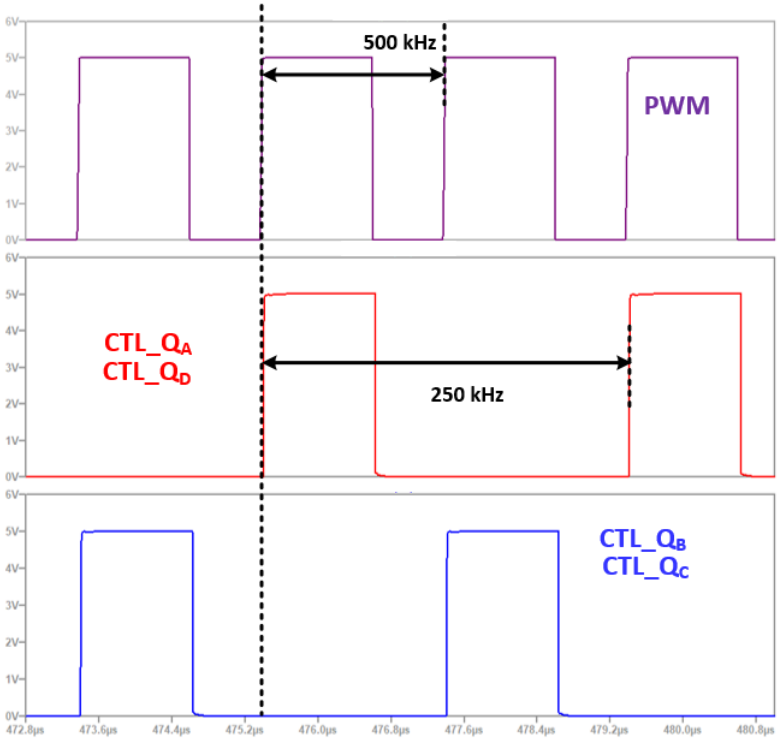

Figure 27. Hard-switched Full Bridge DC-DC converter gate timing

To power the GaN FET gate drivers, the same circuit from Figure 20 can be used, with the difference of using the non-inverting (*Q*) and inverting outputs (*Q!*) of the D-Type Flip Flop to

excite the pulse transformer. In this manner, the same bipolar drive and GaN gate drive IC bias voltage level as the phase shifted full bridge gate driver version is obtained. The other major difference with the phase shifted gate driver design previously described is that the Full Bridge gate driver design does not use pulse transformers to transmit control signals over the isolation barrier. This is because the switches in a conventional full bridge operate a variable duty cycle, unlike the fixed 50% duty cycle operation of the Full Bridge power stage switches operating in PSM.

Instead, the Full Bridge gate driver designed in this work uses the IL610 passive input digital isolator from NVE Corporation [35] to implement control signal isolation for the bridge power stage. These digital isolators make use of the Giant Magneto-resistive (GMR) effect, in which the resistance of a ceramic magnetic element changes drastically in the presence of a very small magnetic field [66, 67]. The GMR based isolator from NEV uses a coil on the primary side (input side) to set a magnetic field that excites a GMR based Wheatstone bridge. The change in resistance in the GMR Wheatstone Bridge is then sensed and conditioned at the output of the isolator IC to create high and low output voltage stages [67]. Figure 28 shows a circuit schematic of the Full Bridge gate driver circuit for one of the top side rad-had GaN FET (Q_A in this case).

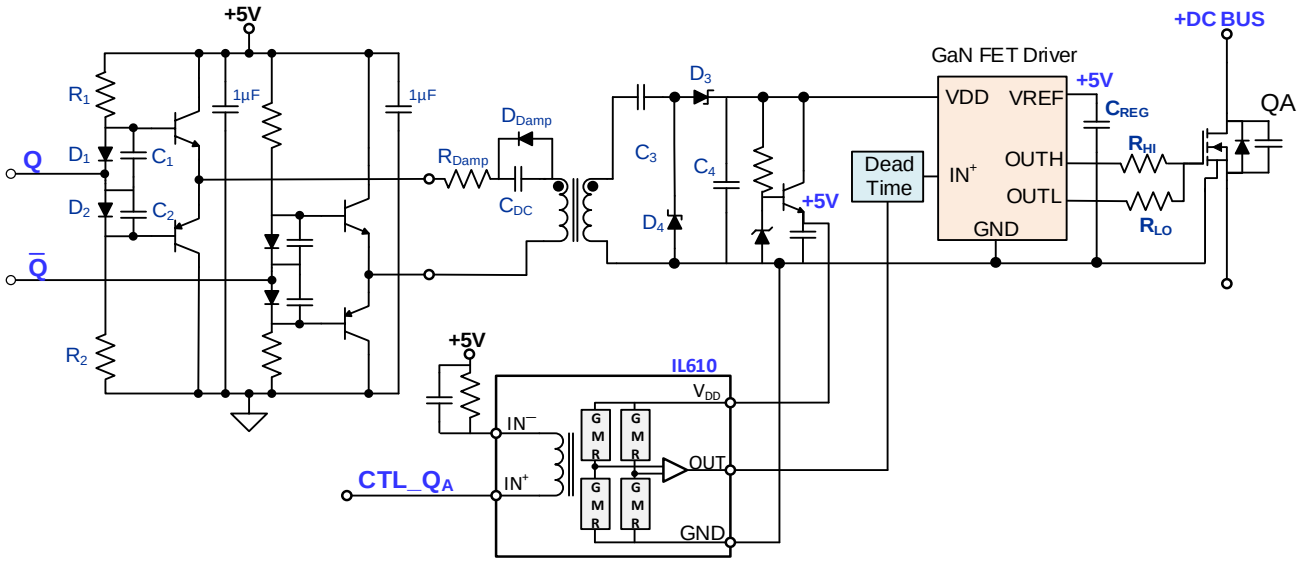

Figure 28. Self-powered gate driver for one GaN FET (Q_A) in Full Bridge DC-DC converter

3.5.2. Current Doubler Rectifier Control for Full Bridge Converter

Figure 29 illustrates the circuit to generate control signals for the rad-hard GaN FETs in the Current Doubler synchronous rectifier for the Full Bridge DC-DC converter designed in this work.

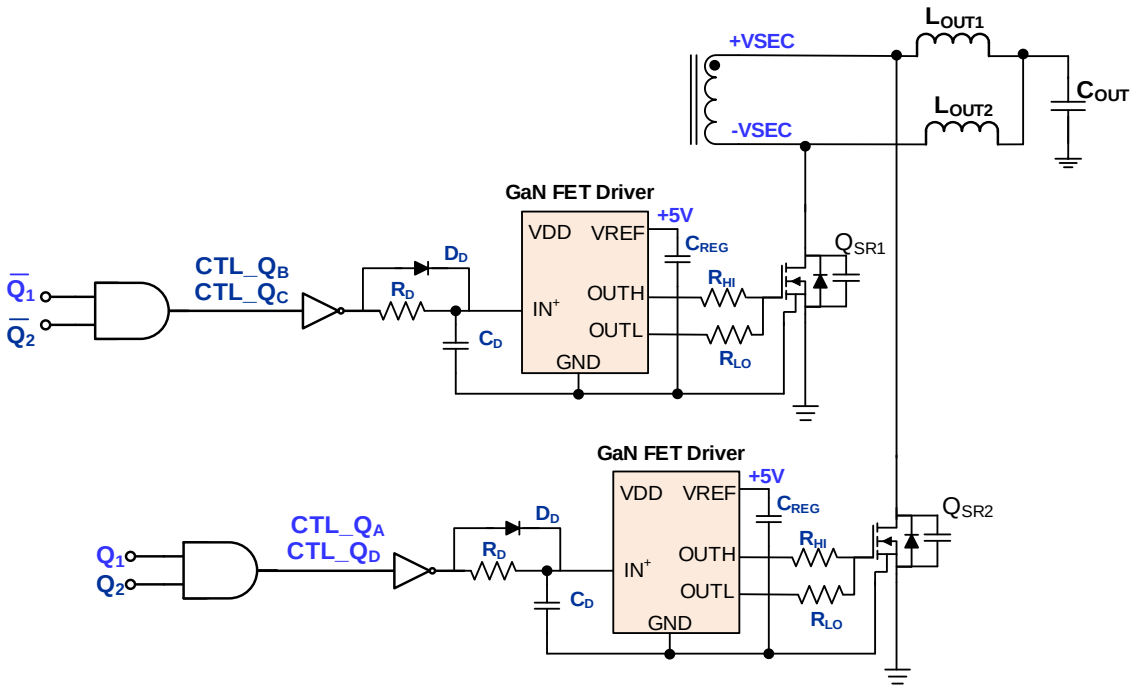

Figure 29. Current Doubler Synchronous Rectifier gate control for Full Bridge DC-DC converter

Because in the conventional Full Bridge power stage all the rad-hard GaN FETs are turned OFF simultaneously during the two OFF time $(1 - D)T_S$ intervals of the effective switching cycle (1/2 F_{SW}), shoot through between the top and bottom switches is not as high as a risk as it is for the Phase Shifted Full Bridge DC-DC converter. This is because in a Phase Shifted Full Bridge, the top and bottom side devices in each of the phase legs conduct right after each other with a dead time separation in the nano-second range. The conventional Full Bridge DC-DC converter with a Current Doubler rectifier, however, can go into shoot through if power transfer at the primary stage and the freewheeling period at the secondary stage rectifier overlap. The Current Doubler rectifier

turns ON both of its switches during the OFF time on the primary side full bridge (Q_A, Q_B, Q_C and Q_D are OFF) such that load current circulates through the output inductors and both Current Doubler switches (freewheeling period). One of the Current Doubler phase legs must be opened (turned OFF) right before the primary side full bridge starts to deliver power to the secondary side to avoid a short circuit of the transformer secondary. Figure 30 shows the full bridge control signals for all rad-hard GaN FETs (Q_A, Q_B, Q_C, and Q_D), and their timing relationship with the Current Doubler rectifier control signals for the rad-hard GaN FETs QS_{R1} and Q_{SR2}.

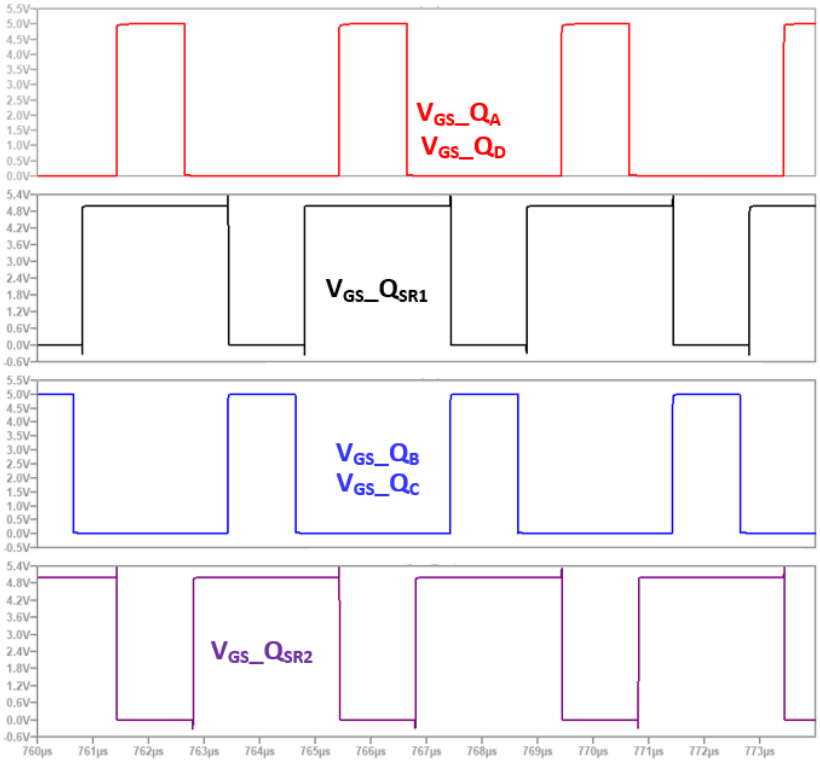

Figure 30. Current Doubler Synchronous Rectifier timing for hard-switched Full Bridge DC-DC converter

3.6. Phase Shifted Full Bridge Power Stage Design

This section describes the design process followed to design the power stage for the Phase Shifted Full Bridge DC-DC converter. Note that the Full Bridge DC-DC converter design uses the same power stage described here but with L_{R_EXT}, D_1, and D_2 in Figure 5 removed. One of the most important parameters for the design of the Phase Shifted Full Bridge DC-DC converter are the rad-hard GaN FET characteristics. Table 20 shows the rad-hard GaN FETs parameters needed to calculate resonant period, resonant inductance, and dead times for ZVS operation in the Full Bridge power sate operating in PSM, as well as the parameters needed for power loss and thermal analysis. Table 21 shows the rad-hard GaN FETs parameters used in power loss and thermal analysis for the Current Doubler synchronous rectifier stage.

Table 20. FBG20N18B 200 V, 18 A 26 mΩ Rad-Hard GaN FET Parameters for Full Bridge Stage

Description	Designator	Value
Number of FETs in parallel	--	2
Junction to Ambient Thermal Impedance	R_{TH_JA}	56 °C/W
Gate Charge	Q_G	6 nC
Gate-drain charge	Q_{GD}	1.5 nC
Gate-source charge	Q_{GS}	2 nC
Gate resistance	R_G	0.4 Ω
Voltage threshold	V_{TH}	2 V
Miller Plateau Voltage	V_{PLT}	2.5 V
Gate Drive Voltage	V_{DRIVE}	5.0 V
ON Resistance per FET	R_{DSON_PER}	26 mΩ
Equivalent ON Resistance	R_{DSON}	13 mΩ

Table 21. FBG20N18B 200 V, 18 A 26 mΩ Rad-Hard GaN FET Parameters for Rectifier Stage

Description	Designator	Value
Number of FETs in parallel	--	4
Equivalent ON Resistance	R_{DSON}	6.5 mΩ
Output Charge per FET	Q_{OSS}	3.5 nC
Output Charge Equivalent	Q_{OSS_EQ}	140 nC
Gate Charge Equivalent	Q_{G_EQ}	24 nC

The design process followed starts by defining maximum duty cycle in conjunction with turns-ratio for the power transformer. For worst case, maximum duty cycle occurs at maximum output voltage at minimum input voltage operation. Transformer turns-ratio is then calculated using pre-defined maximum duty cycle value. With an initial estimate for duty cycle loss and preliminary transformer turns ratio, effective duty cycle on the secondary side and target resonant inductance value can be calculated at full load operation. The rest of the converter parameters such as Current Doubler rectifier output inductors value and output capacitor can be calculated after.

Using transformer turns-ratio, initial targeted resonant inductance, and output inductor value, magnetics design can be carried out. Iteration is needed to calculate the final resonant inductance value for the desired ZVS range because there is not a closed form solution for resonant inductance calculation in the Phase Shifted Full Bridge DC-DC converter [53, 54]. The approach followed in this work was to minimize transformer leakage inductance by interleaving the windings, and add an external inductor with a selected initial value. The power transformer was then built and characterized with an impedance analyzer to measure leakage inductance value. The external resonant inductor L_{R_EXT} was adjusted during bench testing to obtain the correct amount of resonant inductance needed to achieve ZVS while maintaining feasible dead time intervals between all the switches in the converter.

The final step in the design process is power loss analysis for the switches and the magnetics in the power stage. A few iterations must be made to adjust switching frequency and transformer turns ratio, as well as total number of switches to achieve efficiency targets. Figure 31 captures the design process followed in this work.

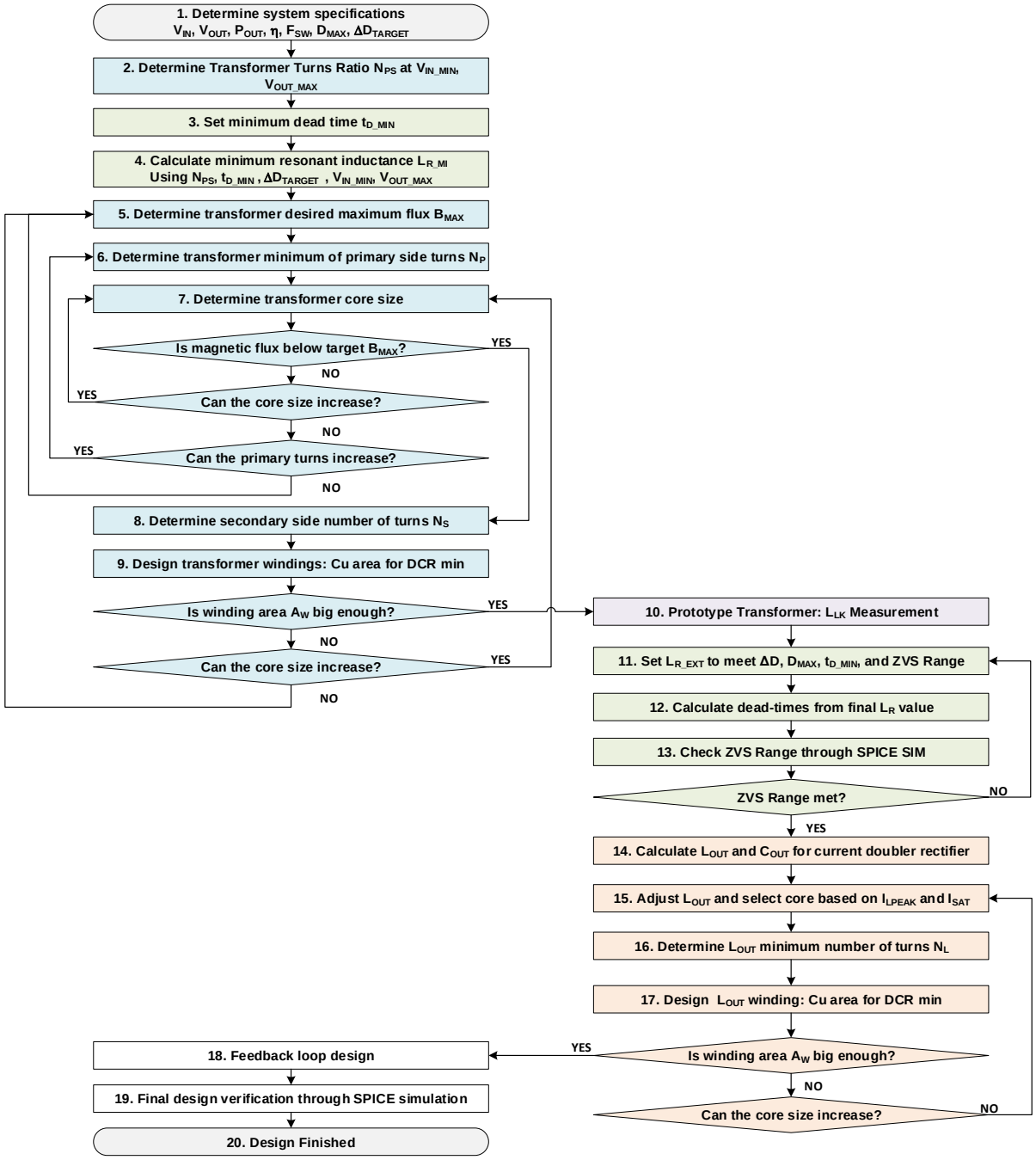

Figure 31. Power stage general design process

3.6.1. Initial Power Stage Calculations

A maximum duty cycle of 85% is selected to allow for enough margin at the PWM IC (limited to around 95%). In addition, switching frequency targeted for this design is set to 500 kHz at the PWM IC oscillator. This results in an effective switching frequency of 250 kHz at the power stage, with 500 kHz input and output currents. The targeted duty cycle loss for this design is set to 5%. From this, an effective duty cycle of 80% is obtained, which results in the following calculation for transformer turns ratio for a converter with a Current Doubler rectifier for the output side:

$$N_{PS\_initial} = \frac{D_{EFF\_MAX} \cdot V_{IN\_MIN} \cdot n_{TARGET}}{2 \cdot V_{OUT\_MAX}} = 1.502$$

(21)

Selecting the closest transformer turns ratio N_{PS} of 1.5, the preliminary turns are set to 6 turns for the primary side (N_P) and 4 on secondary side ($N_{S)}$. This results in an affective duty cycle of:

$$D_{EFF\_MAX} = \frac{2 \cdot V_{OUT\_MAX} \cdot N_{PS}}{V_{IN\_MIN} \cdot n_{TARGET}} = 0.789$$

(22)

Focusing on the worst case of operation point that maximizes duty cycle from the PWM controller (V_{IN_MIN}, V_{OUT_MAX}), for a 5% duty cycle loss target, the approximated resonant inductance can be calculated from (23) as 656nH.

$$L_{R\_MAX} = \frac{2 \cdot N_{PS} \cdot V_{IN\_MIN} \cdot n_{TARGET} \cdot \Delta D_{TARGET}}{2 \cdot \frac{P_{OUT}}{V_{OUT\_MAX}} \cdot F_{SW}} = 656\ nH$$

(23)

Another way of calculating L_R is based on an iterative process described in [53, 54]. This method revolves on calculating L_R for a specific output load, called critical load in. Critical load is

defined as the minimum load at the converter output at which ZVS on the leading leg of the full bridge (Q_A and Q_B) can be achieved [53, 54]. Because printed circuit board and transformer parasitic are difficult to predict without having a physical prototype, the approximation in (23) of L_R based on duty cycle loss and maximum duty cycle of the PWM controller is used in this design. In addition, due to concerns with component tolerance and variation over time from GaN FET gate driver Schmitt trigger thresholds, capacitance and resistance tolerance over lots, life, and temperature, the dead time in this design is set between *40 ns* to *45 ns*. This dead-time limit bounds the minimum resonant inductance that can be tolerated by the design. To ensure ZVS operation in the leading leg switches, Q_A and Q_B, dead-time must be set to ¼ of the resonant period t_R of the tank circuit formed by L_R and equivalent resonant capacitance C_R as shown in Figure 32.

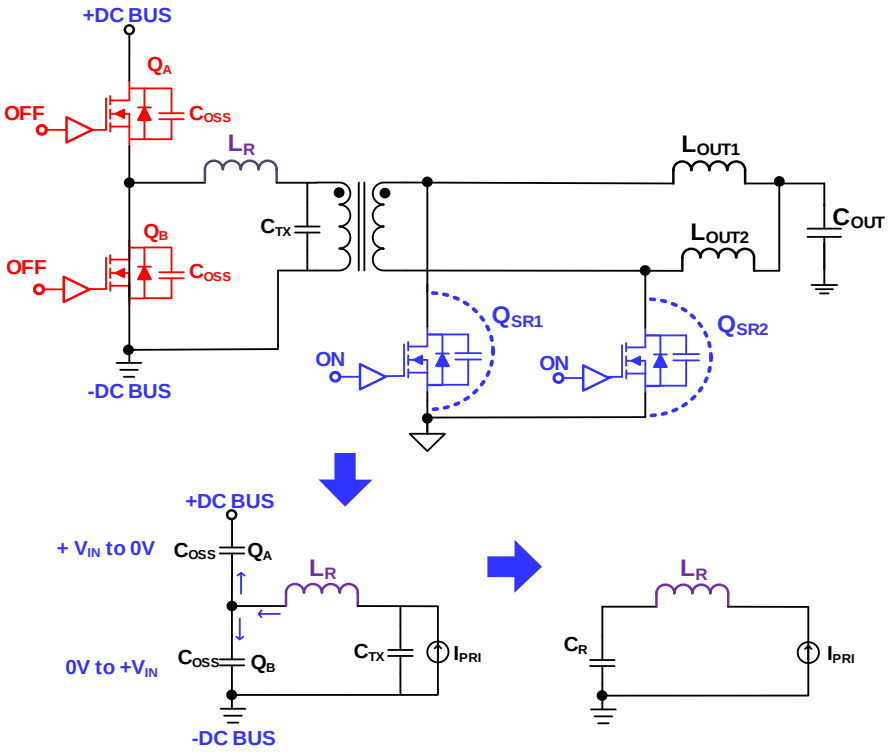

Figure 32. Leading leg resonant tank circuit for ZVS of Q_A

The maximum dead time to achieve ZVS in the leading leg can be calculated from (24).

$$t_{dead\_time} = \frac{t_R}{4} = \frac{\pi\sqrt{L_R C_R}}{2}$$

(24)

Where t_{dead_time} is maximum dead time, and C_R is equivalent resonant capacitance consisting of the output capacitance C_{OSS} of each of the rad-hard GaN FETs with a 4/3 term to average C_{OSS} non-linear behavior, and the shunt parallel capacitance of the transformer labeled as C_{TX}. Resonant capacitance C_R is defined by (25).

$$C_R = C_{TX} + 2\left(\frac{4}{3}C_{OSS}\right)$$

(25)

From (24), minimum resonant inductance value in relation to dead time is defined by (26). For 30ns to 40ns dead-time L_R must be set to between 400 nH to 720 nH, using 50 pF as an initial assumption for the transformer parallel capacitance C_{TX}. The total resonant inductance chosen for this design is approximately 600 nH, for an approximate maximum dead time of approximately 40 ns.

$$L_{R\_MIN} = \frac{1}{C_R}\left(\frac{2t_{dead-time}}{\pi}\right)^2$$

(26)

3.6.2. Output Inductor Design

Output inductor is designed based on ripple factor of 40%, and then iterated to minimize RMS losses on the converters primary side. For a Phase Shifted Full Bridge with Current Doubler rectifier, it is best to maximize inductance such that RMS losses are reduced. The expression in (27) is used to calculate output inductor value for the Current Doubler Rectifier. This equation

takes into account duty cycle and current ripple cancelation from the 2-phase interaction between the two output inductors in the Current Doubler Rectifier.

$$L_{OUT} = \frac{V_{OUT}\left(1 - \frac{V_{OUT} \cdot N_{PS}}{V_{IN} \cdot n_{TARGET}}\right)}{\Delta I_{LOUT\_TARGET} \cdot \frac{F_{SW}}{2}}$$

(27)

In addition, the value of L_R must set smaller than the output inductor value L_{OUT} to avoid an additional voltage loss from L_R reflected to the secondary L_R/N_{PS}^2. The final output inductance selected for this work is 6.25 µH. This selection was made based on core size and saturation current limitations. The resulting output inductor ripple current with this value becomes:

$$\Delta I_{LOUT} = \frac{V_{OUT}\left(1 - \frac{V_{OUT} \cdot N_{PS}}{V_{IN} \cdot n_{TARGET}}\right)}{L_{OUT} \cdot \frac{F_{SW}}{2}} = 8.8\ A$$

(28)

The maximum output inductor ripple happens at V_{OUT_MAX}, V_{IN_MAX}. This value is 10.6A; however, after accounting for a tolerance of 25.6% from RSS estimation of PWM IC oscillator frequency and inductance variation from the magnetic core permeability, the worst case peak to peak inductor ripple becomes 13.3 A. In addition, worst case peak inductor current happens at maximum input voltage of 120 V and minimum output voltage of 18 V (widest difference between input and output). The worst-case peak inductor current was calculated to be 18.3A peak, which after worst-case tolerance factorization becomes 19.44 A. From ripple cancelation at the Current Doubler rectifier, the combined output current ripple is:

$$\Delta I_{OUT} = \frac{V_{OUT}\left(1 - \frac{2 \cdot V_{OUT}.N_{PS}}{V_{IN} \cdot n_{TARGET}}\right)}{\frac{L_{OUT}}{2} \cdot F_{SW}} = 4.8\ A$$

(29)

The magnetic core selected for the inductor is the EQ30 from FerroxCube. The material selected is 3C95 due to its low loss at the targeted switching frequency of this design. An inductance factor of 250 nH/T^2 was specified for the 5 turns selected. This resulted in a worst-case flux density of 240 mT calculated from:

$$B_{peak} = \frac{L_{OUT} \cdot I_{LOUT_{PK}}}{A_C \cdot N_{LOUT}} = 237\ mT$$

(30)

For output inductor core losses, worst-case inductor current ripple is used to calculate AC flux density swing as shown below.

$$\frac{\Delta B_{AC_{WC}}}{2} = \frac{L_{OUT} \cdot \Delta I_{LOUT\_MAX}}{2 \cdot A_C \cdot N_{LOUT}} = 58\ mT$$

(31)

Table 22 summarizes the output inductor magnetic design for the Current Doubler synchronous rectifier in this work.

Table 22. Output Inductor Specifications

Description	Designator	Value
Magnetic Core		EQ30+PLT30 from FerroxCube, 3C95
Effective Cross Section of Core	A_{C_MIN}	95µ m^2
Number of Turns	N_{LOUT}	5 Turns
Inductance Factor (Air gap)	A_L	250 nH/T^2
Worst Case Inductor Current Ripple	ΔI_{LOUT}	13.3 A
Worst Case Inductor Peak Current	I_{LOUT_PK}	19.44 A
Worst Case Output Current Ripple	ΔI_{OUT}	7.73 A
AC Flux Density for Core Loss	B_{AC_WC}	88 mT
Maximum Flux Density	B_{PEAK}	256 mT
Wire Thickness	W_{THICK}	0.6 mm
Wire Width	W_{WIDTH}	5.2 mm
Wire Length	W_{LENGTH}	291 mm
DC Resistance at 100°C	DCR	2.26 mΩ

3.6.3. Transformer Design

Transformer design is performed by first setting maximum flux density to 100 mT to ensure core losses remain low. Magnetic core was selected based on cross sectional area A_C required to maintain peak flux to approximately 100 mT for initial selection of primary winding number of turns N_P equals 6. The EQ38 and PLT8 core pair from FerroxCube in 3C95 ferrite material was selected for this design. Peak to peak transformer flux density can be calculated from:

$$\Delta B_{MAX} = \frac{V_{IN_{MIN}} D_{EFF\_MAX}}{N_P \cdot A_C \cdot F_{SW}} = 210\ mT$$

(32)

Maximum peak flux density for core saturation and core loss calculation can be calculated using (33) below.

$$B_{PEAK} = \frac{\Delta B_{MAX}}{2} = 105\ mT$$

(33)

Magnetizing inductance for the power transformer, L_{MAG}, can be found in two ways. The first one by simply using inductance factor A_L of the core, which results in 368 µH. The second way is by calculating effective permeability μ_e based on A_L and using this value to calculate equivalent air-gap l_{gap} from magnetic path length l_e of the transformer core as shown in the equations below.

$$\mu_e = \frac{1}{\mu_0 \cdot \mu_r} \frac{A_L \cdot l_e}{A_C} = 2850$$

(34)

$$l_{gap} = \frac{l_e}{\mu_e} = 14.63\ \mu m$$

(35)

$$L_{MAG} = \frac{\mu_0 \cdot \mu_r \cdot A_C \cdot {N_P}^2}{l_{gap}} = 367.9\ \mu H$$

(36)

Where μ_0 is permeability of free space equals to $4\pi x\ 10^{-7}\ H/m$ and μ_r is relative permeability of air equals to 1. Peak to peak magnetizing current ΔI_{MAG} can be calculated using magnetizing inductance L_{MAG} and volt-seconds applied to the power transformer primary winding using the following expression.

$$\Delta I_{MAG} = \frac{V_{IN}\left(\frac{2 \cdot V_{OUT} \cdot N_{PS}}{V_{IN} \cdot \eta_{target}}\right)}{L_{MAG} \cdot F_{SW}} = 340\ mA$$

(37)

Table 23 summarizes the specifications of the power transformer magnetic design for the Phase Shifted Full Bridge DC-DC converter in this work.

Table 23. Transformer Design Specifications

Description	Designator	Value
Magnetic Core		EQ38+PLT80 from FerroxCube, 3C95
Effective Cross Section of Core	A_{C_MIN}	119µ m^2
Number of Primary Turns	N_P	6 Turns
Number of Secondary Turns	N_S	4 Turns
Inductance Factor (Air gap)	A_L	10220 nH/T^2
Magnetizing Inductance	L_{MAG}	368 µH
Magnetizing Current, Peak to Peak	I_{MAG}	339.4 mA
Maximum Flux Density	B_{MAX}	105 mT
Wire Thickness	W_{THICK}	0.3 mm
Wire Width	W_{WIDTH}	5.2 mm
Wire Length	W_{LENGTH}	291 mm
DC Primary Resistance at 100°C	DCR_{PRI}	6.81 mΩ
DC Secondary Resistance at 100°C	DCR_{SEC}	4.54 mΩ

3.7. Power Loss Analysis

This section describes the initial power loss analysis performed in the converter performed at the nominal operating point of 100 V in, 20 V out, and 500W load. AC resistance losses in the transformer and inductors were not modeled. The following RMS currents were calculated:

Table 24. RMS Currents calculated for Power Loss Analysis

Description	Designator	Model
Primary RMS Current	I_{PRI_RMS}	8.33 A
Secondary RMS Current	I_{SEC_RMS}	13.693 A
Primary FET RMS Current	I_{FET_RMS}	5.893 A
Secondary FET RMS Current	I_{SR_RMS}	18.54 A
Output Inductor RMS Current	I_{LOUT_RMS}	12.5 A
Output Capacitor RMS Current	I_{COUT_RMS}	1.409 A
Input Capacitor RMS Current	I_{CIN_RMS}	4.048 A

3.7.1. Transformer Power Losses

Transformer primary and secondary windings copper power losses can be calculated from the expressions below.

$$P_{PRI\_COND} = {I_{PRI\_RMS}}^2 DCR_{PRI} = 0.474\ W \tag{38}$$

$$P_{SEC\_COND} = {I_{SEC\_RMS}}^2 DCR_{SEC} = 0.853\ W \tag{39}$$

$$P_{TX\_COND} = P_{PRI\_COND} + P_{SEC\_COND} = 1.327\ W \tag{40}$$

Transformer core loss for the 3C95 ferrite material from FerroxCube calculated by looking at the ferrite material datasheet. The power loss per volume factor versus frequency curve and flux density curve gives a 200 mW/cm^3 power loss factor for the 3C95 ferrite material at 105 mT, 250

kHz frequency [68]. This result in an approximate core loss of 1.24 W using the effective volume V_e of the EQ38 core selected.

$$P_{CORE} = 200\frac{mW}{cm^3} \cdot V_e = 1.24\ W \tag{41}$$

The total power transformer power losses due to core loss and conduction loss from DC resistance of the primary and secondary windings is 2.565 W.

3.7.2. Inductor Power Losses

The power loss calculations for the output inductors are provided below. Conduction loss from the inductor windings is:

$$P_{LOUT\_COND} = {I_{LOUT\_RMS}}^2 \cdot R_{DC} = 0.309\ W \tag{42}$$

Core power loss for the output inductor is modeled from the material datasheet, in the same manner that it was done for the power transformer. From the material datasheet at the operating frequency and flux for the inductor, the core loss factor is 70 mW/cm^3. Power loss in the core is then modeled as follows:

$$P_{CORE\_LOUT} = 70\frac{mW}{cm^3} \cdot V_{e_{LOUT}} = 0.274\ W \tag{43}$$

The total output inductor L_{OUT} power loss is 1.166 W for both inductors in the Current Doubler rectifier. In addition, the external resonant inductor L_{R_EXT} power losses were estimated as follows:

$$P_{LR\_COND} = {I_{PRI\_RMS}}^2 R_{DC\_LR} = 0.072\ W \tag{44}$$

The core loss factor for the resonant inductor 3C95 ferrite core selected is 200 mW/cm^3. This results in a core loss of 0.392 W in L_{R_EXT}, for a total power loss of 0.464 W.

3.7.3. Full Bridge Power Stage Losses

Assuming ZVS operation, switching losses can be neglected for a first order power loss estimation of the GaN FETs in the full bridge power stage. Conduction loss for the primary side GaN FETs is the main source of power loss, and it is estimated with the expression below:

$$P_{FET\_COND} = {I_{FET\_RMS}}^2 R_{DSON} = 0.451\ W \tag{45}$$

ZVS only happens during turn ON of the full bridge power stage. Therefore, turn OFF power losses in the GaN FETs must be modeled as follows:

$$t_{OFF} = Q_{gd}\left(\frac{R_g}{V_{Miller\_plateau}}\right) + Q_{gs}\left(\frac{V_{Miller\_plateau} - V_{TH}}{V_{Miller\_plateau}}\right)\left(\frac{2 \cdot R_g}{V_{Miller\_plateau} + V_{TH}}\right) = 0.622\ ns \tag{46}$$

$$P_{FET\_OFF} = \frac{1}{2} \cdot I_{LOUT\_PEAK} \cdot \frac{1}{N_{PS}} \cdot V_{IN} \cdot F_{SW\_EFFECTIVE} \cdot t_{OFF} = 0.088\ W \tag{47}$$

Power Losses from Driving the GaN FETs in the primary stage can be approximated as shown below, where $F_{SW\_EFFECTIVE} = \frac{F_{SW}}{2} = 250\ kHz$.

$$P_{GATE\_DRIVE} = I_Q V_{DD} + 2Q_g V_{GATE\_DRIVE} F_{SW\_EFFECTIVE} = 32m\ W \tag{48}$$

The body diode loss during dead time is calculated below:

$$P_{DIODE\_SW} = \frac{I_{LOUT\_PK}}{N_{PS}}\ V_{FW}(t_{deadtime}) F_{SW\_EFFECTIVE} = 110\ mW \tag{49}$$

The total power loss, including gate driver losses for each of the primary side GaN FETs is estimated to be around 681 mW from the expression below, putting the total full bridge power loss at approximately 2.723 W.

$$P_{SW\_FET} = P_{FET\_COND} + P_{FET\_OFF} + P_{GATE\_DRIVE} + P_{DIODE\_SW} = 681\ mW \tag{50}$$

$$P_{BRIDGE} = 4\ P_{SW\_FET} = 2.723\ W \tag{51}$$

3.7.4. Rectifier Power Stage Losses

The power losses for the synchronous rectifier GaN FETs is estimated next. For the rectifier, both conduction and switching loss were considered as shown below:

$$P_{SR\_COND} = {I_{SR\_RMS}}^2 R_{DSON\_SR} = 2.234\ W \tag{52}$$

Synchronous rectifier switching loss is calculated as:

$$P_{SR\_Coss} = \frac{1}{2}(Q_{oss} + Q_{rr})\frac{V_{IN}}{N_{PS}}\ F_{SW\_EFFECTIVE} = 1.392\ W \tag{53}$$

Where Q_{rr} is the reverse recovery charge of the paralleled diodes used for dead time circulation in each of the Current Doubler legs (27n) and Q_{OSS} is the output charge of each rad-hard GaN FET (35nC). Gate driver loss for each of the GaN FET chains in the Current Doubler is calculated using the expression below:

$$P_{GATE\_DRIVE\_SR} = I_Q V_{DD} + 2Q_{g\_SR} V_{GATE\_DRIVE} F_{SW\_EFFECTIVE} = 62m\ W \tag{54}$$

The body diode loss during dead time is calculated below:

$$P_{DIODE\_SR} = \frac{I_{OUT\_PK}}{2} V_{FW}(t_{deadtime}) F_{SW\_EFFECTIVE} = 134\ mW \quad (55)$$

Finally, the total power loss per GaN FET leg in the Current Doubler rectifier is:

$$P_{SR\_FET} = P_{SR\_COND} + P_{SR\_Coss} + P_{GATE\_DRIVE\_SR} + P_{DIODE\_SR} = 3.90\ W \quad (56)$$

$$P_{SR\_RECTIFIER} = 2 \cdot P_{SR_{FET}} = 7.80\ W \quad (57)$$

3.7.5. Miscellaneous Power Losses

Other minor losses were modeled for the output capacitor, input capacitors, second stage filter inductor, and current sensing scheme. These are defined below.

$$P_{COUT} = {I_{COUT\_RMS}}^2 ESR_{COUT} = 20\ mW \quad (58)$$

$$P_{CIN} = {I_{CIN\_RMS}}^2 ESR_{CIN} = 33\ mW \quad (59)$$

$$P_{CT} = (I_{IN\_RMS}\ N_{PS_{CT}})^2\ R_{SENSE} + {I_{IN\_RMS}}^2\ R_{CT\_PRI} = 126\ mW \quad (60)$$

$$P_{LF} = {I_{OUT}}^2 R_{FILTER} = 0.156\ W \quad (61)$$

Where $R_{FILTER} = 1.03\ m\Omega$. In addition, there are extra losses from the clamping diodes on the primary. This loss was simulated and found to 1.576 W for both diodes at 500 W load, nominal input of 100 V and nominal output of 20 V.

3.7.6. Efficiency Approximation

The initial power loss estimate, not accounting for losses in the magnetic components from AC resistance for the power transformer and resonant inductor, are 16.63 W. This puts the

estimated efficiency at nominal point at 96.78% from analysis at nominal operating point of 100V input, 20 V output, and 500 W. This efficiency estimate analysis was verified via SPICE simulation. From simulation, efficiency at 500 W load, 100V input and 20 V output is 97%. This simulation result does not include magnetic core losses. After including the core loss from mathematical analysis, simulated efficiency is 96.63%, which validates the mathematical analysis performed in this section. Table 25 provides a summary of the estimated power loss from mathematical modeling, and Table 26 presents the results from SPICE simulation verification.

Table 25. Power Loss Breakdown at 100 V Input, 20 V Output, 500 W Load

Description	**Estimated Power Loss (W)**	**Percentage Loss**
Transformer	2.565	15.42%
Resonant Inductor	0.464	2.79%
Output Inductors	1.166	7.01%
Bridge Power Stage	2.723	16.38%
Current Doubler Rectifier	7.8	46.91%
2nd Stage Output Filter Inductor	0.156	0.94%
Current Sensing	0.126	0.76%
C_{IN} and C_{OUT}	0.053	0.32%
Clamping Diodes	1.576	9.48%
Total Loss	16.629	100.00%
Estimated Efficiency	96.78%	

Table 26. Power loss analysis validation, results from SPICE simulation

P_{OUT} no core loss	498.98 W
P_{IN} with no core loss	514.47 W
Power loss with no core loss	15.49 W
Efficiency with no core loss	96.99%
Additional core loss from calculations	1.902 W
Adjusted power loss including core losses	17.39 W
Adjusted Efficiency	96.63%

Figure 33 shows a relative comparison of loss contributors as percentages of the total estimated power loss in the converter. From Figure 33 and Table 25, most of the power loss is expected to come from the bridge rectifier rad-hard GaN FETs. In a synchronous rectifier, there is parallel diode circulation through the GaN FETs for some time prior to them turning ON. Because of this, switching losses are usually much lower than conduction losses. Efficiency can easily improve by using lower R_{DSON} GaN FETs on the synchronous rectifiers. In addition, due to the wide input and output voltage range requirements, transformer turns ratio and maximum duty cycle cannot be optimized to achieve highest efficiency at nominal operating point. At maximum duty cycle of approximately 85%, when the converter operates at V_{IN_MIN}, V_{OUT_MAX} with a 500 W load, efficiency estimation for this converter is 97.2%. At minimum duty cycle of 46.3%, when converter operates at V_{IN_MAX}, V_{OUT_MIN} with a 500 W load, approximated efficiency is 96.4%.

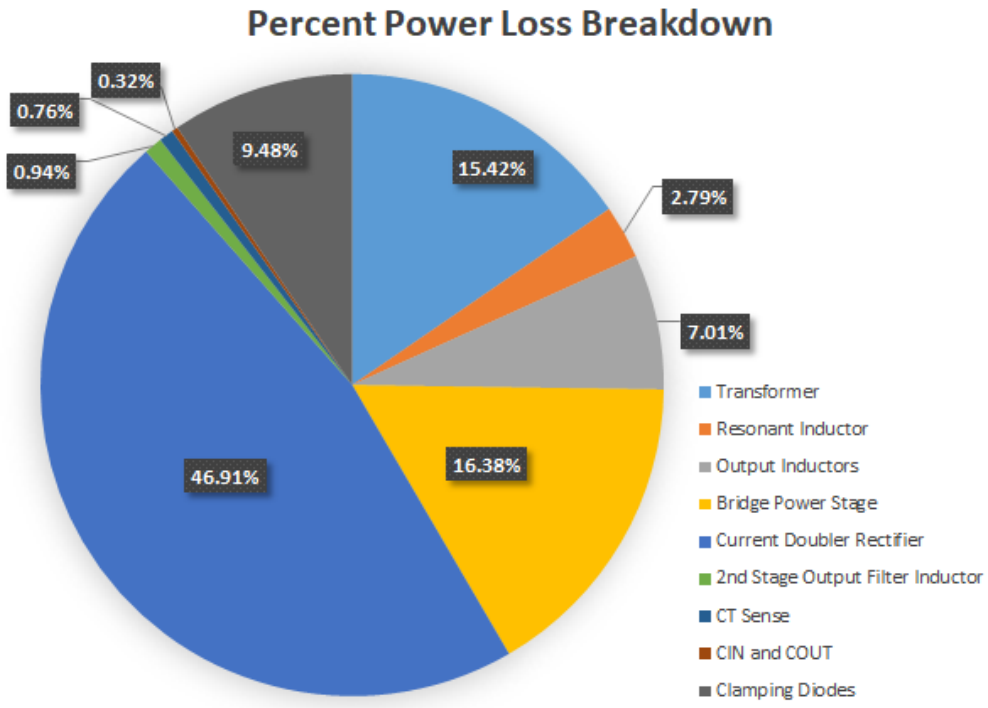

Figure 33. Phase Shifted Full Bridge estimated power loss distribution in percentage of total power loss at nominal operating point

Chapter 4 Hardware Implementation

4.1. Printed Circuit Board Layout

This section describes the areas that demand special attention during printed circuit board (PCB) design. This includes paralleling of rad-hard GaN FETs for the full bridge power stage on the primary side and for the Current Doubler rectifier secondary side. This also includes GaN gate driver IC layout and PCB power layer distribution to mitigate noise and inductive parasitics. In addition, this section describes the PCB layout and routing of the current sense circuity and PWM controller to implement analog PCMC, both very critical for proper converter operation.

4.1.1. Rad-Hard GaN FETs Paralleling

To push the output power capability of the converter while meeting efficiency requirements of more than 95%, the rad-hard GaN FETs on the primary and secondary side needed paralleling to reduce the total R_{DSON}. Optimal PCB layout for paralleling GaN FETs was studied in [69, 70]. The package of the rad-hard FBG20N18B GaN FETs from Freebird Semiconductor, however, is much different than the ones from the study in [69, 70]. For the rad-hard GaN FETs from Freebird Semiconductor, clustering the gate-source node close together as recommended in [69] comes at the expense of a widening the switching node. In addition, PCB area and manufacturability favors placing all rad-hard GaN devices on the same layer as the magnetics (i.e. top layer of the PCB). Therefore, all rad-hard GaN FETs were placed on the top layer of the PCB, while the GaN gate drivers were located on the bottom layer of the PCB, as close to the FETs as possible.

Figure 34 shows he placement implemented for the paralleled FBG20N18B rad-hard GaN FETs at each of the Full Bridge power stage switches. For this design, the gate to source node path was prioritized and kept as short and as symmetrical as possible. Note that the FBG20N18B GaN

FETs have a kelvin connection for the gate-source interface—i.e. control signal path is separated from main power path. The layout for the paralleled rad-hard GaN FETs on the Current Doubler follows the same approach shown in Figure 34. The layout of the paralleled rad-hard GaN FETs in the power stage PCB design was validated using an infrared camera to verify that the thermal distribution was even among each of the GaN FETs. In addition, the gate-source voltage waveforms at each of the paralleled rad-hard GaN FETs was measured under load to verify that all devices turn ON at almost the same time. For this, all oscilloscope probes used for measurements were calibrated using the probe's Deskew function in the oscilloscope. The rad-hard GaN FET paralleling implemented in this work resulted in very good power sharing verified by very even temperature distribution among all devices. In addition, the symmetrical layout of the rad-hard GaN FETs resulted in almost identical gate-source voltage propagation among all paralleled devices. Section 5.4 provides test results validating the rad-hard GaN FET paralleling scheme used in the full bridge and the Current Doubler synchronous rectifier power stages.

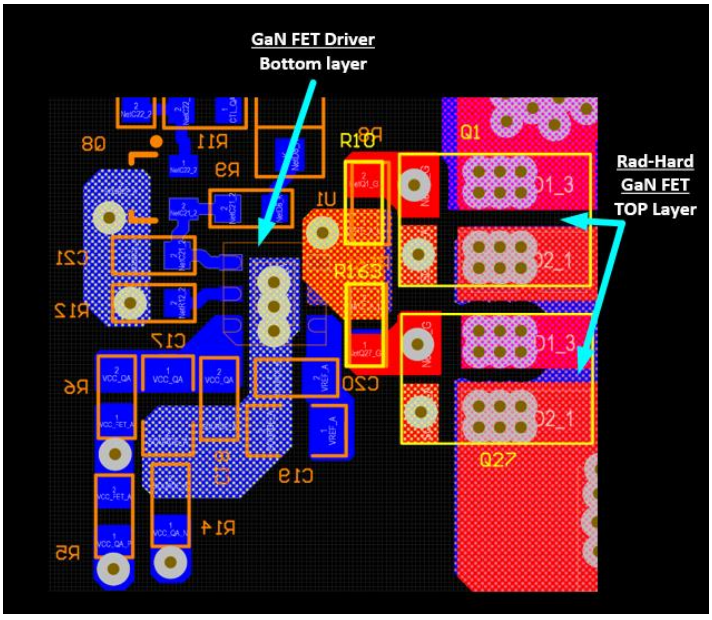

Figure 34. PCB layout showing top (red) and bottom (blue) layers for top switch Q_A in Full Bridge power stage

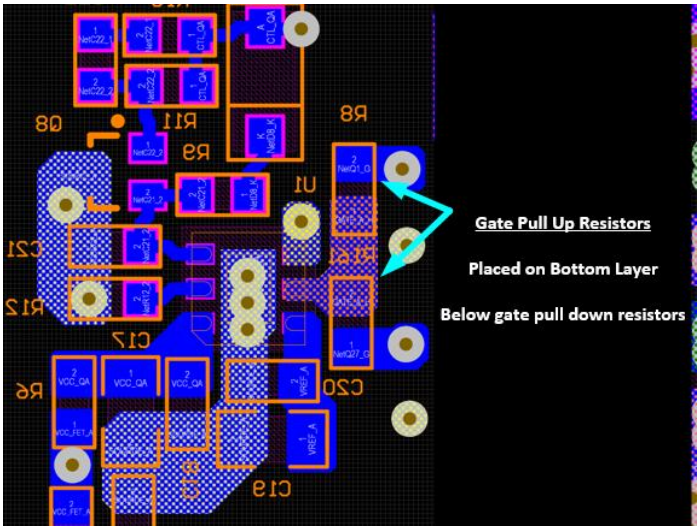

Figure 35. Gate pull up resistors on bottom layer (blue) for top switch Q_A in Full Bridge power stage

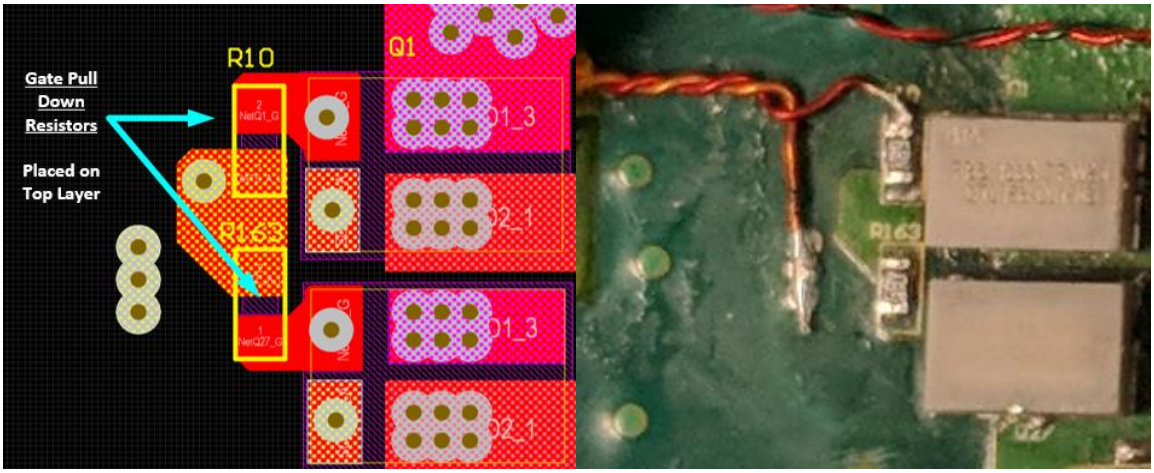

Figure 36. Gate pull down resistors on top layer (red) for top switch Q_A in Full Bridge power stage

Figure 37 shows the power flow on the primary side full bridge power stage and the power transformer. Current flows from the point labeled at "+DC BUS" to the DC bus return power plane, shown as all areas in green. Current flows through the two paralleled GaN FETs in location Q_A, then connecting one pad of L_{R_EXT} to the positive DC bus. The input current continues through an internal layer into the power transformer. The current then exits the

transformer on the top right corner of Figure 37 and into the lagging-leg parallel devices in location Q_D to return the current to the ground (green plane).

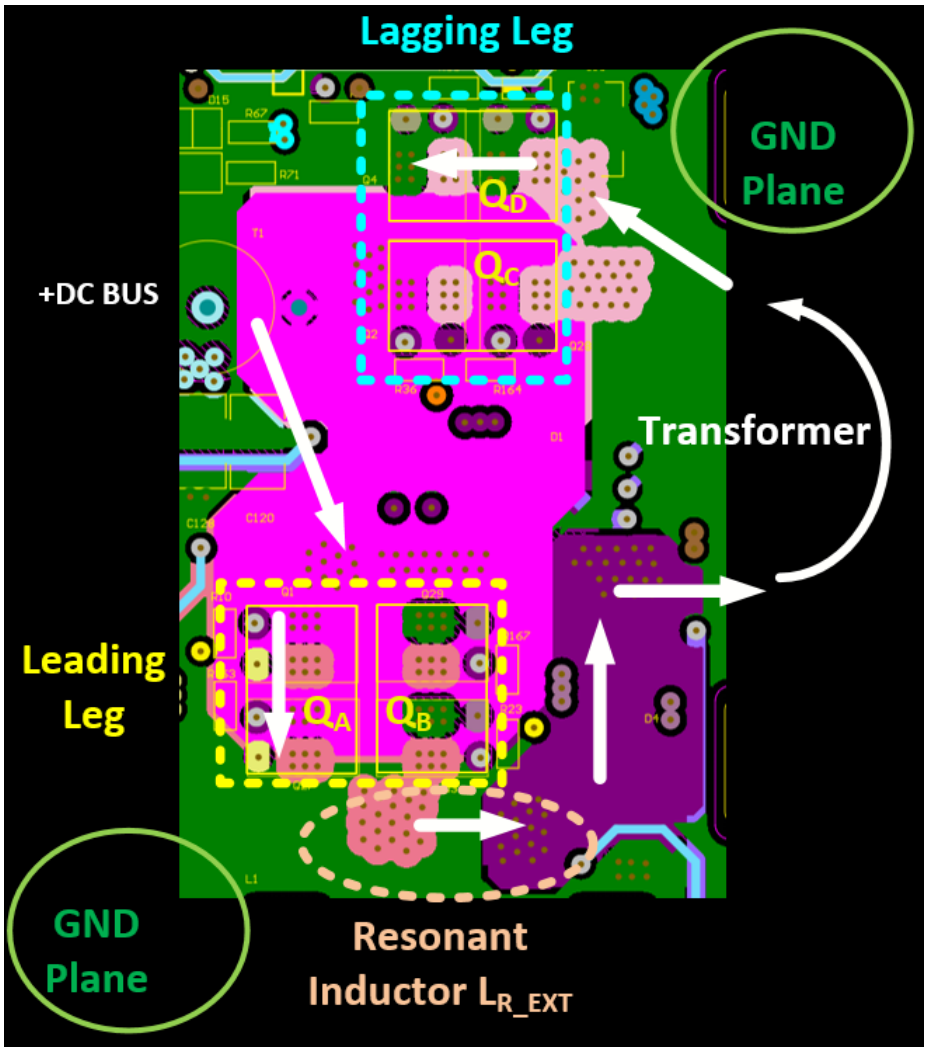

Figure 37. Full Bridge power stage input current flow from +DC Bus to -DC Bus return (ground, green plane)

4.1.2. GaN FET Gate Driver Layout Consideration

The scheme followed to layout the GaN drivers was to have the source or gate return path as a reference plane for the gate signal, i.e. on the immediate PCB layer below (or above) where the gate path was routed. The PCB used for the power stage has 12 layers. The gate pull-up resistors

were placed in the bottom layer (layer 12) along with the gate driver IC, while the pull down gate resistors were placed on the top layer (layer 1) along with the rad-hard GaN FETs. A small copper plane connects the gate return (kelvin source) from the GaN FETs to the gate driver IC ground (source connection). This gate-return or source plane was laid out to cover the gate signal path on the layer right above it. For example, the gate signal connecting the gate pull-up resistors routed in layer 1 has a reference gate-return plane on layer 2, while the gate signal connecting the gate pull-down resistors routed in the bottom has a gate-return plane on layer 11. This allows the gate signal paths to be fully referenced to their return planes via small power planes in layers 2 and 11. The same approach was followed for the Current Doubler rectifier. The gate-source waveforms were capture for the Full Bridge and Current Doubler power stages. Laboratory measurements showed very low inductive ringing at the gates of the rad-hard GaN devices. Section 5.4 provides waveforms taken of the gate-source voltages for the full bridge and Current Doubler power stages.

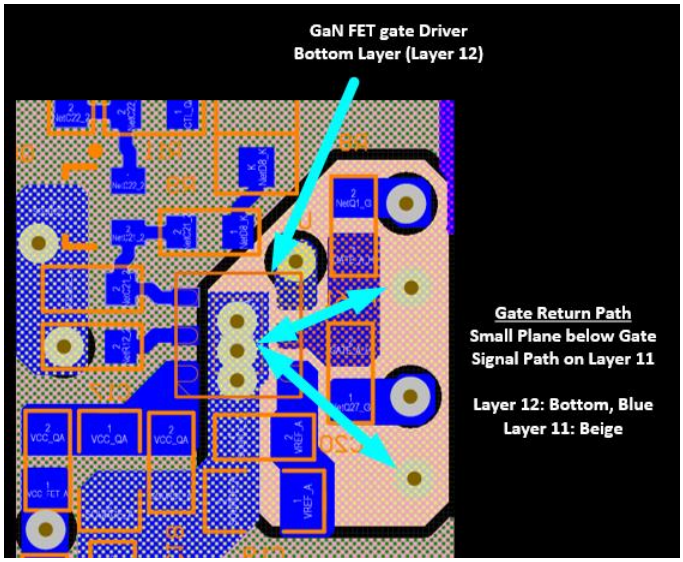

Figure 38. Gate driver layout showing rad-hard GaN FET gate return path, layer 12 (blue) and layer 11 (Beige).

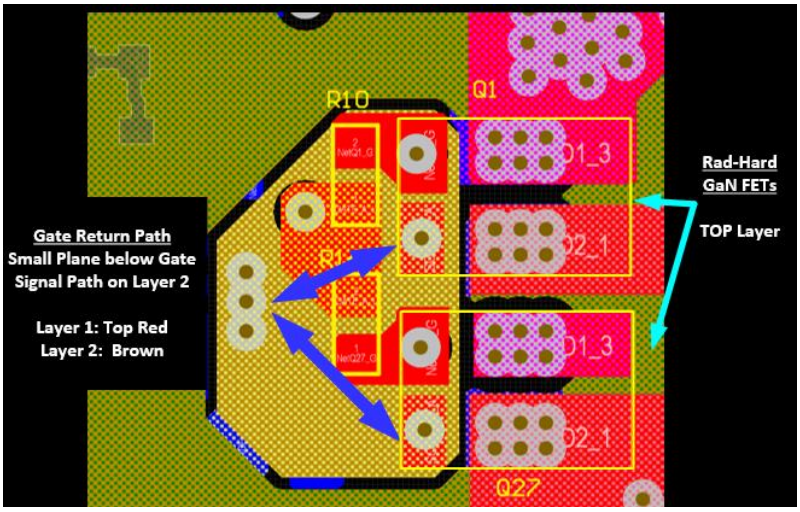

Figure 39. Gate driver layout showing rad-hard GaN FET gate return path, layer 1 (red) and layer 2 (brown).

4.1.3. Current Sense Layout

The location and PCB layout of the current sensor is critical for a Phase Shifted Full Bridge or Full Bridge DC-DC converter design. To avoid noise from the switching nodes from getting into the current sensing signal, the current sense transformer (CT) was located at the DC input Bus as discussed previously. The current sense resistor and diodes required to reset the CT were placed closest to the CT as shown in Figure 42. This allows for a low impedance signal carrying a voltage (instead of current) to be routed from the input side to the other side of the board where the PWM controller IC was located. Current sensing in this work was implemented successfully with no issues encountered due to noise nor CT core reset, with waveforms of the sensed current signal demonstrated in the next section. The converter operated stable under peak current mode control (PCMC) over input and output voltage range, and across output loads. In addition, temperature testing was successfully performed at hot temperature with zero noise or reset issues found. Figure 40 shows the location of the CT sensor and the PWM controller IC on the board. Figure 41 shows the way the signal carrying current information was routed across the board, from the CT sensor

on the left side of the figure to the PWM controller IC on the right side of the figure. The current sense signal was routed differentially with 10 mil traces and a separation of 12 mil in between positive source path and negative return path.

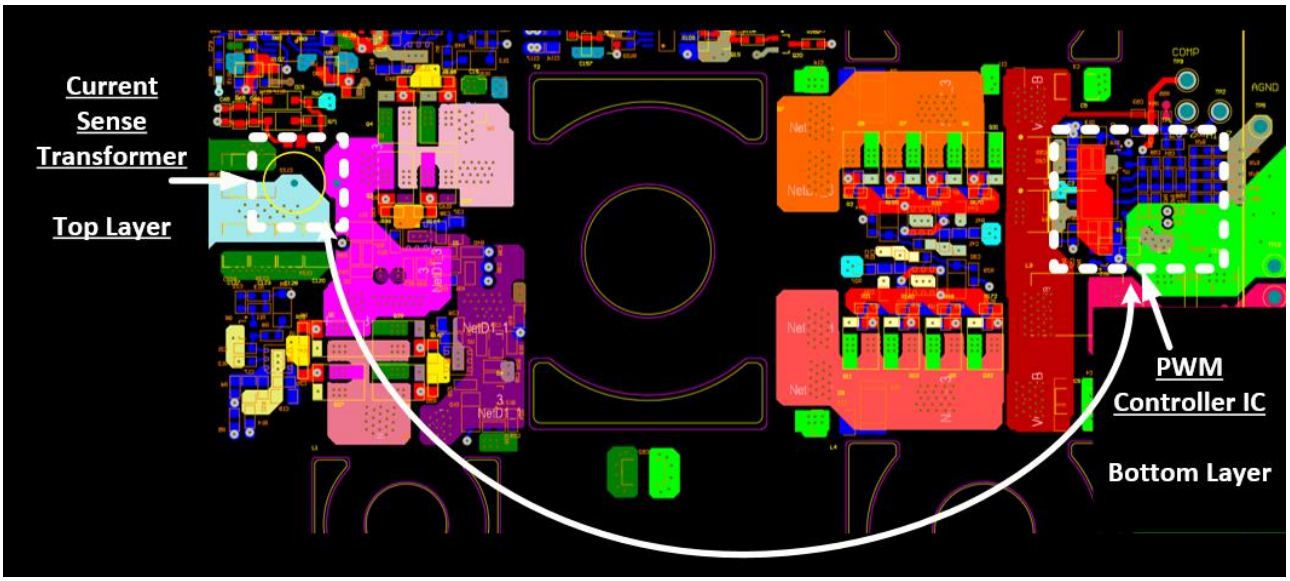

Figure 40. Location of current sense transformer sensing and PWM controller IC destination.

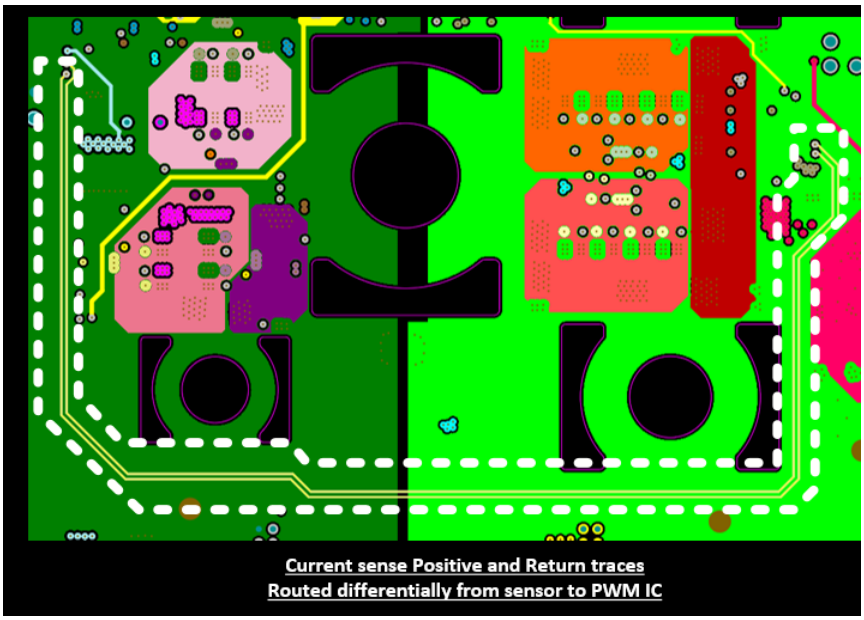

Figure 41. Differential current sense route for positive and return traces, from current transformer sensor to PWM IC input.

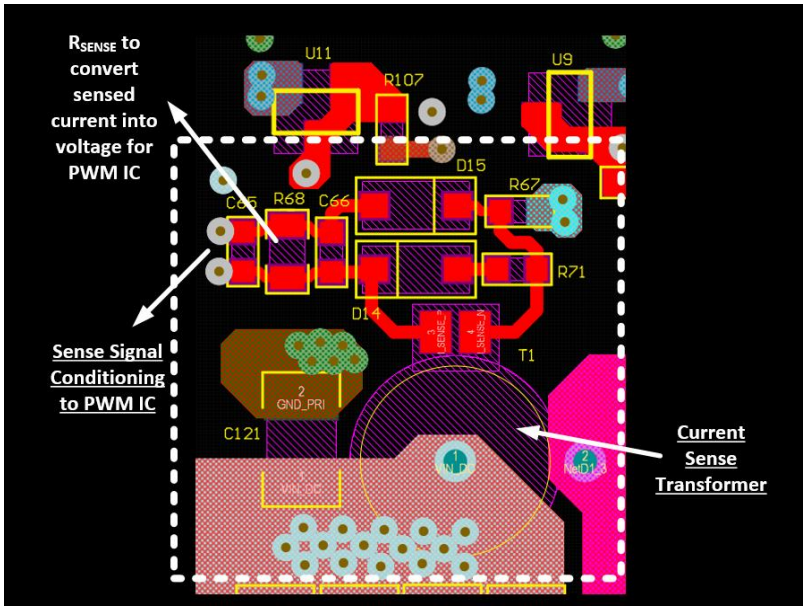

Figure 42. Current sensor layout, top layer in red.

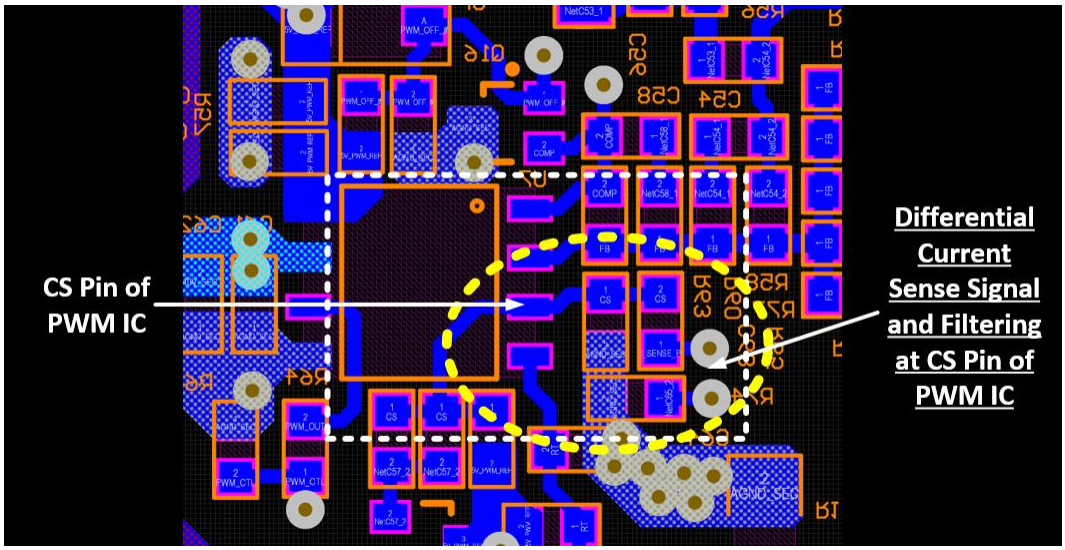

Figure 43. PWM IC Receiving end showing differentially routed current sense signal, input and filtering into CS pin of PWM IC.

4.2. Prototype Board Stack

The converter prototype consisted of a two-board stack that allowed evaluation of different modulation methods. The main power board contains the power stage and local gate drivers for

the GaN FETs, current and voltage sensing, PWM controller, housekeeping power supplies, and peripheral circuitry to ensure proper startup. All power transistors used in the main power stage board are the FBG20N18B rad-hard GaN FETs rated at 200V, 18A, 26 mΩ and manufactured by Freebird semiconductor [31] and shown in Figure 3. Daughter cards contained dedicated circuitry needed to condition the output of the PWM controller to implement different modulation schemes of the Full Bridge power stage. Two gate driver cards were designed to evaluate Phase Shift Modulation achieving ZVS operation, and conventional PWM modulation to control the Full Bridge power stage on the primary side of the converter. Figure 44 shows the converter prototype stack for the Phase Shifted Full Bridge DC-DC converter in this thesis.

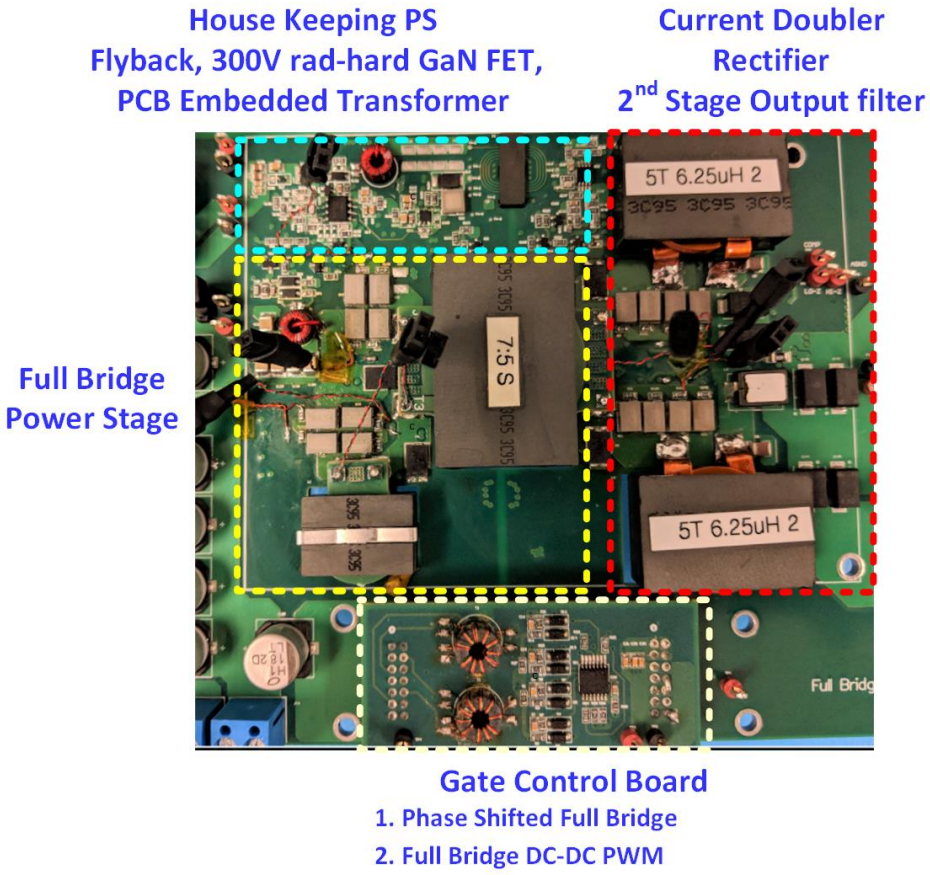

Figure 44. Phase Shifted Full Bridge Prototype Rev. 1.00.

The power converter including housekeeping power supply, gate drivers, and power management for startup and shutdown sequencing measures 10 cm x 8.0 cm with a maximum height of 1.3 cm. The power density obtained is 4.8 kW/mm^3 or 79 W/in^3. Figure 45 shows the dimensions of the converter. The gate-driver board components fit in the empty area the below the power transformer in the main power board. This area is highlighted with yellow ellipses in Figure 45.

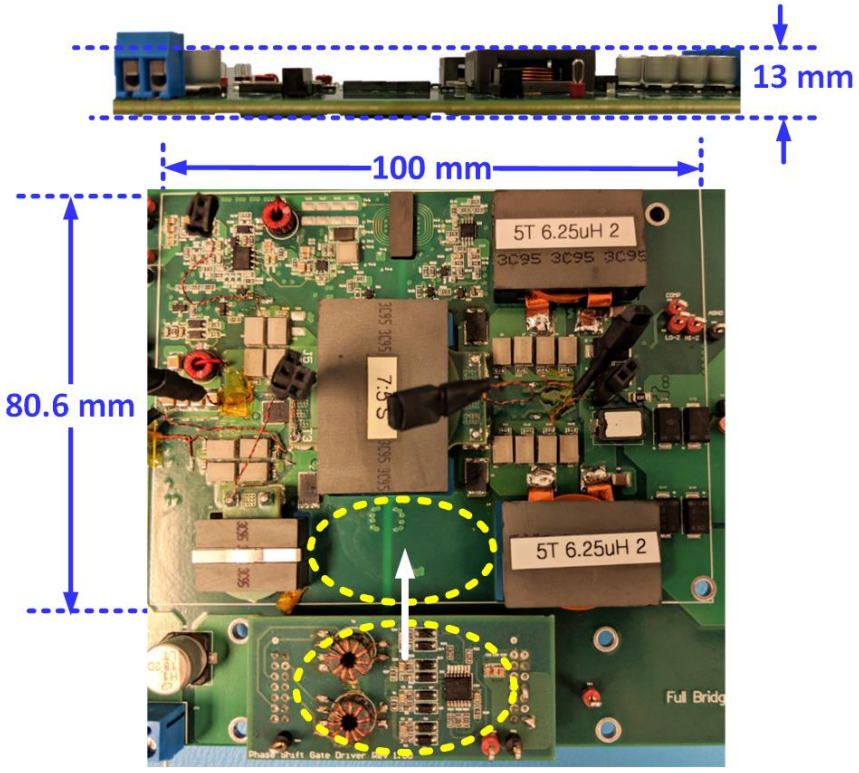

Figure 45. Phase Shifted Full Bridge DC-DC converter dimensions.

4.3. Phase Shift Gate Driver Board

Figure 46 shows the phase shift modulation gate-driver prototype board. This board requires a 5.0 V voltage input, and a PWM control input signal. It contains components that convert the control signal output from the PWM controller into six signals to control the Full Bridge power

stage and the Current Doubler synchronous rectifier using Phase Shift Modulation at the Full Bridge power stage. The phase-shift gate driver board also creates four output voltages to power the GaN FET gate driver ICs for the Full Bridge power stage switches Q_A, Q_B, Q_C and Q_D located in the main power stage board.

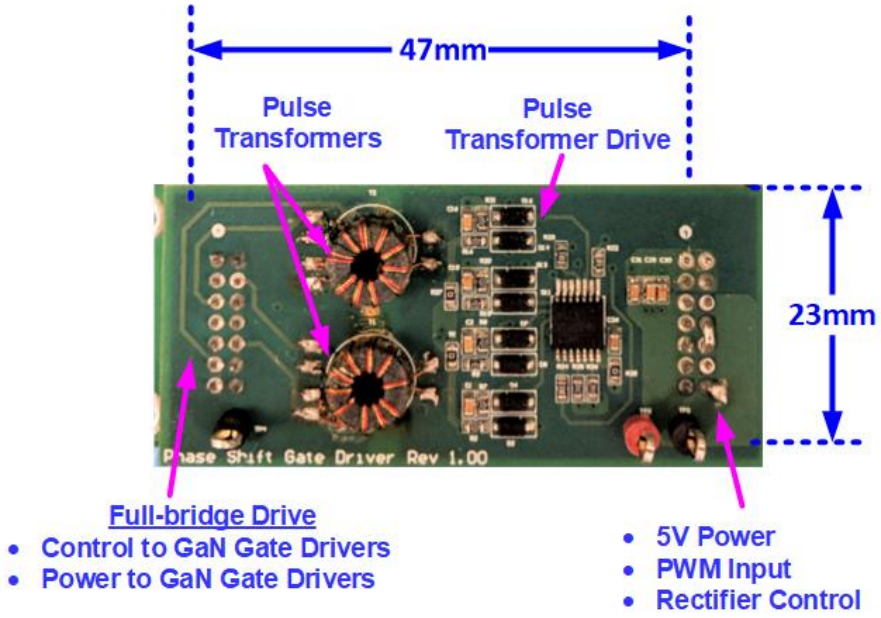

Figure 46. Self-powered gate driver for rad-hard GaN FET based Phase Shifted Full Bridge DC-DC converter

4.4. Full Bridge Gate Driver Board

Figure 47 shows the hard-switched Full Bridge modulation gate-driver prototype board. This board requires a 5.0 V voltage input, and a PWM control input signal. It contains components that convert the control signal output from the PWM controller into six signals to control the Full Bridge power stage and the Current Doubler synchronous rectifier using conventional hard switching for the Full Bridge power stage. The Full Bridge gate driver board creates two voltages to power the high side GaN FET gate driver ICs for the Full Bridge power stage switches Q_A and Q_C located in the main power board.

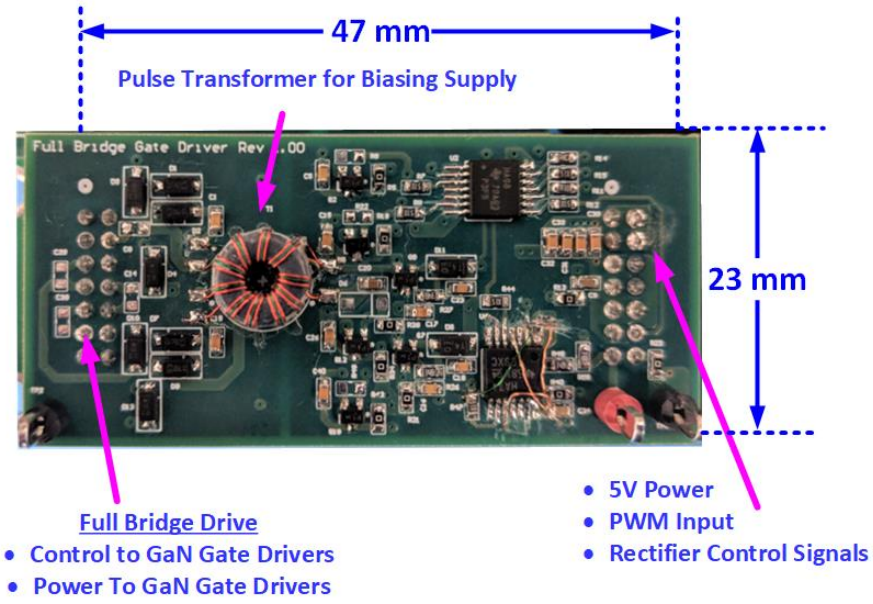

Figure 47. Self-powered gate driver for rad-hard GaN FET based Full Bridge DC-DC converter

Chapter 5 Experimental Results

This section presents the test results and evaluation conclusions for the Phase Shifted Full Bridge DC-DC converter and the Full Bridge converter designed in this work. Figure 48 shows the test setup and measurement equipment used to verify the operation of the two converters. All measurements were performed with calibrated, compensated voltage probes, with the oscilloscope bandwidth set to its limit of 500 MHz for proper signal resolution. In addition, twisted pairs were used to perform all voltage measurements (see Figure 36).

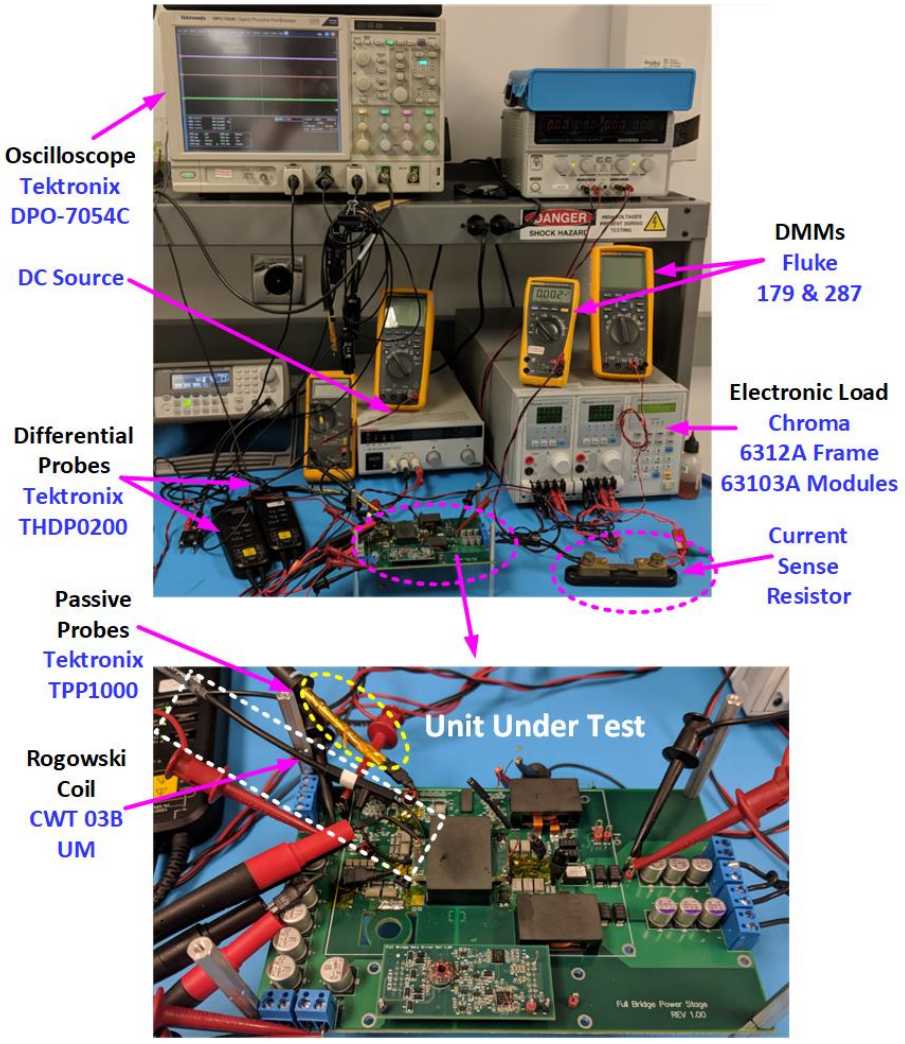

Figure 48. Test Setup and equipment

5.1. Phase Shift Gate Driver

5.1.1. Pulse Transformer Characterization

The pulse transformer designed for the self-powered phase-shift gate driver (also used in the Full Bridge driver) was characterized with an impedance analyzer and verified with a high quality LCR meter. Table 18 and Table 19 summarize the pulse transformer magnetic core specifications and the design calculations, respectively. Table 27 presents the measurements obtained during laboratory characterization of the pulse transformer for the isolated gate driver implementation.

Table 27. Pulse Transformer Characterization with Impedance Analyzer

Parameter	Designator	Value
Primary Inductance	L_{MAG}	385.7µH
Leakage Inductance	L_{LK}	107nH
Input-Output Capacitance	$C_{I/O}$	12 pF
Distributed Parallel Capacitance	C_{PAR}	53.2 pF
Primary series resistance	R_{PRI}	0.230 Ω
Secondary series resistance	R_{SEC}	0.202 Ω

5.1.2. Phase Shift Gate Driver Test Results

Operation for the proposed self-biased gate driver for the Phase Shifted Full Bridge DC-DC converter in this work was verified across the operating points of Table 7. The DC voltage obtained to power the GaN FET gate drivers on the main power board was approximately 8.6 V. Figure 49 shows the startup and shutdown waveforms for the supply voltage powering the GaN FET gate driver IC for the topside rad-hard GaN FET Q_A with the converter operating at the nominal point from Table 7.

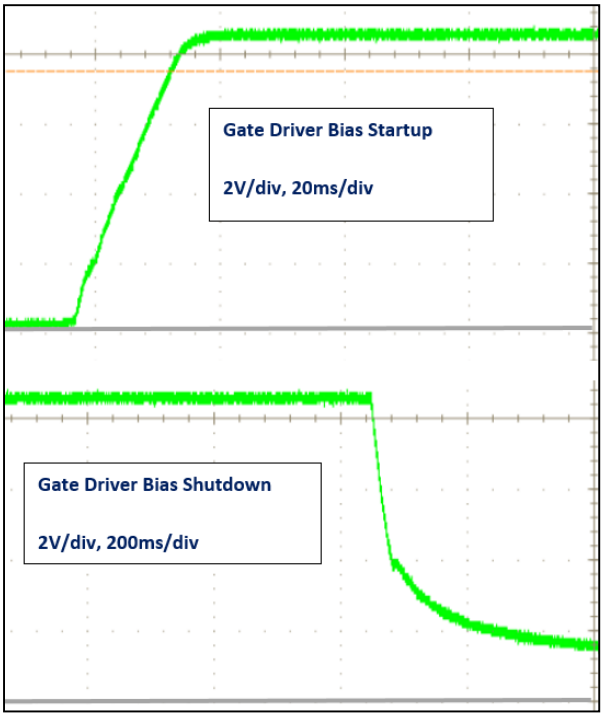

Figure 49. Gate driver generated startup and shutdown bias voltage waveforms for GaN gate driver chip

Figure 50 shows the gate-source gate drive voltages measured right at the rad-hard GaN FETs in the Full Bridge power sage with the converter operating at nominal point. These waveforms verify that proper dead-time delay was obtained, as well as very low ringing at the gate-source input to the rad-hard GaN FETs. Finally, Figure 51 demonstrates the output of the pulse transformer driving the dead time control circuitry (purple) and the output of the GaN FET gate driver IC for the low side rad-hard GaN FET Q_B. The waveform in Figure 51 shows very low ringing at the output of the gate drive pulse transformer, as expected from the approximately 100 nH of leakage inductance and very low parasitic capacitance of the pulse transformer. Gate to source rise times were set to approximately 18 ns, while fall times were set to approximately 6 ns.

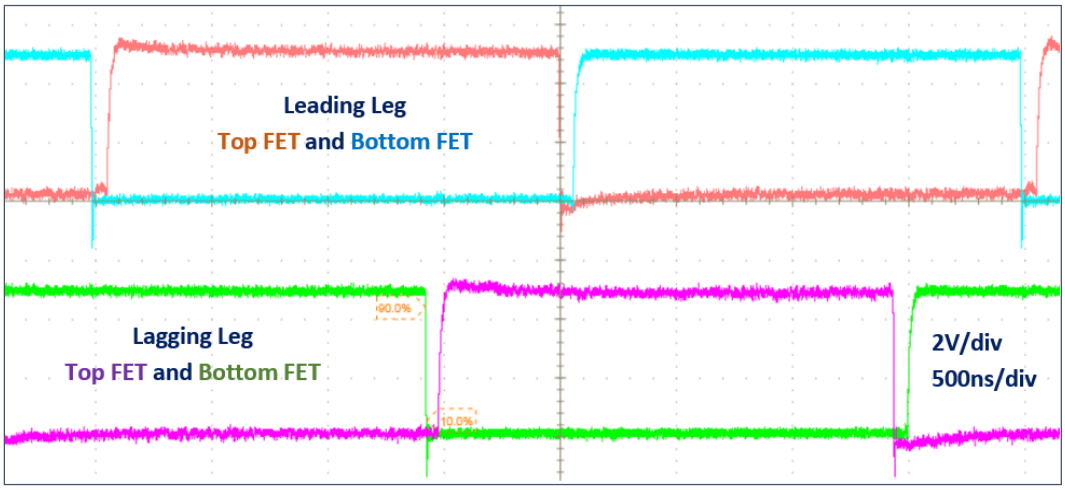

Figure 50. Gage-source voltage waveforms for leading leg (QA and QB) and lagging legs (QC, and QD) GaN FETs operating at 100V input, 400W load, 20V output

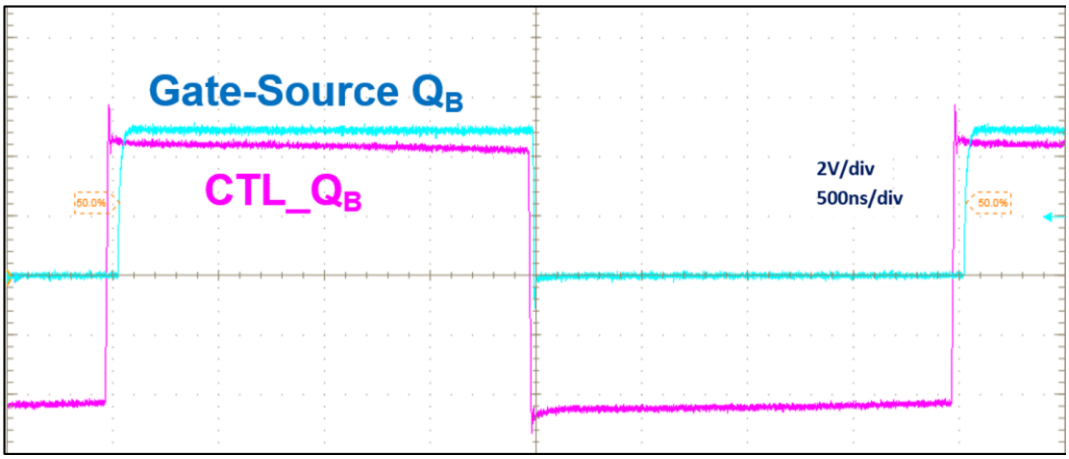

Figure 51. Pulse transformer output for low-side rad-hard GaN FET QB (purple) and GaN gate driver IC output directly the gate-source node of GaN FET QB (blue)

From Table 27, the pulse transformer design resulted in an input to output capacitance $C_{I\backslash O}$ of 12 pF. With the Phase Shifted Full Bridge DC-DC converter running from a 100 V DC bus to deliver 500 W at a 20 V output, the phase leg switch node *dv/dt* captured with an oscilloscope was 5.06 kV/µs. From (17), approximately 60 mA of peak current is injected through $C_{I/O}$. This injected current was small enough to be absorbed by the push-pull power stage shown in Figure 20 with no

issues. However, damping resistances in the control signal path had to be reduced to minimize voltage drops and signal distortion created by the flow of current along this signal path.

5.2. Full Bridge Gate Driver

This section presents waveforms for the Full Bridge DC-DC converter gate driver. For the full bridge gate driver, the dead time between the primary side full bridge power stage and the Current Doubler rectifier requires special attention as described in 3.5.2. Figure 52 shows the measured gate-source waveforms for the full bridge power stage operating under nominal conditions. Rise times of the gate-source control signal were set at around 25 ns, while fall times were set to approximately 6 ns.

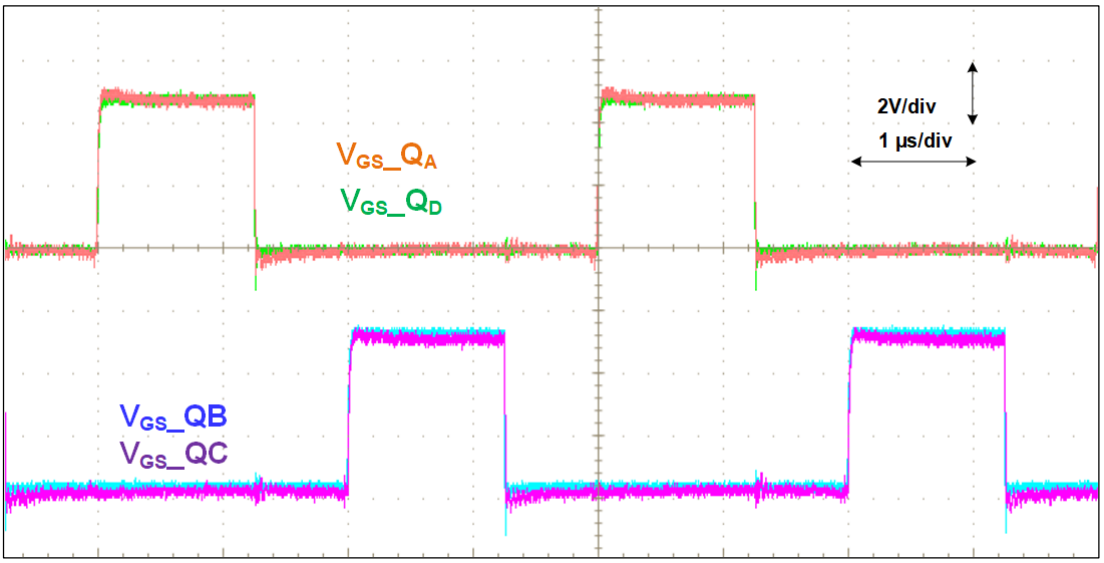

Figure 52. Full Bridge DC-DC Converter rad-hard GaN FET Gate-source voltage at full load, 100 V input, 20 V output

In addition, Figure 53 shows the Full Bridge control signals and their relation with the Current Doubler synchronous rectifier control with the converter running at full load, nominal input and output conditions. Approximately 45 ns of dead time was used between the Full Bridge power stage and the Current Doubler rectifier to avoid shorting the power transformer secondary.

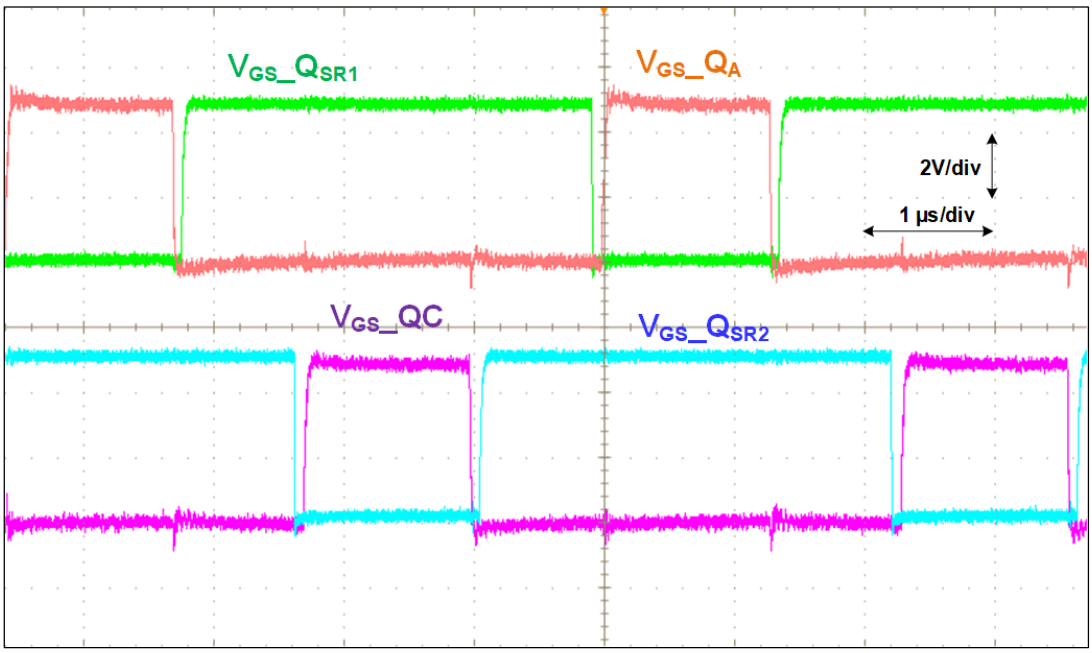

Figure 53. Full Bridge power stage and current double rectifier gate-source voltage waveforms for rad-hard GaN FETs running at 500 W, 100 V input, 20 V output.

5.3. Current Sense Signal for PCMC

Current sensing using a current transformer was successfully implemented by this work. Both converters, Phase Shifted Full Bridge and Full Bridge, operated with no issues with the current and voltage control loops closed. Only minor adjustments were required at the current sense circuit, mainly in the form of component value changes to increase filtering at the PWM controller current sense, and for slope compensation to achieve a stable control loop. Waveforms of the current sense signal are shown below for both converters.

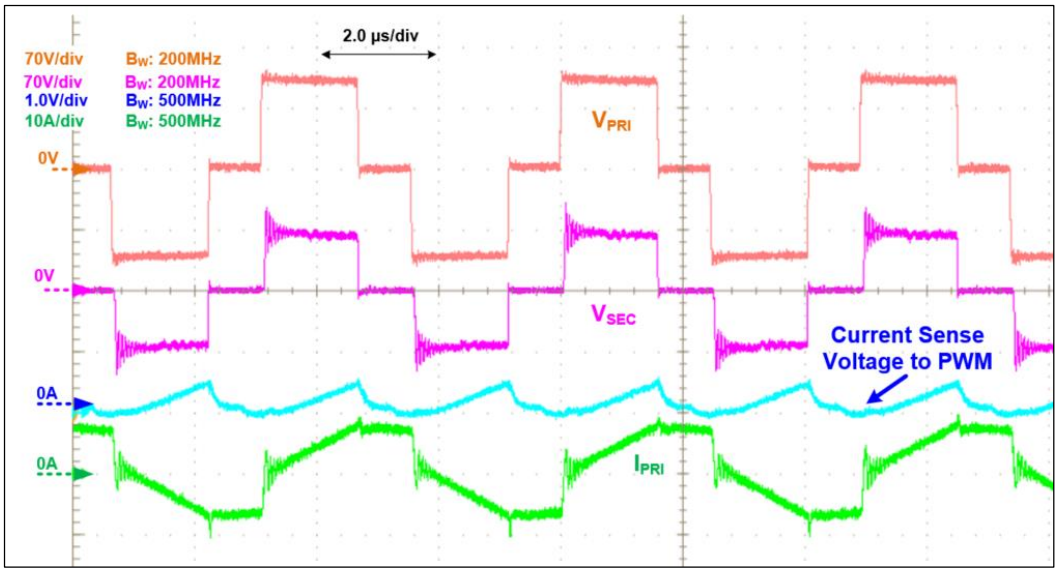

Figure 54. Current sense voltage into PWM current sense pin shown in blue for Phase Shifted Full Bridge operating at full load

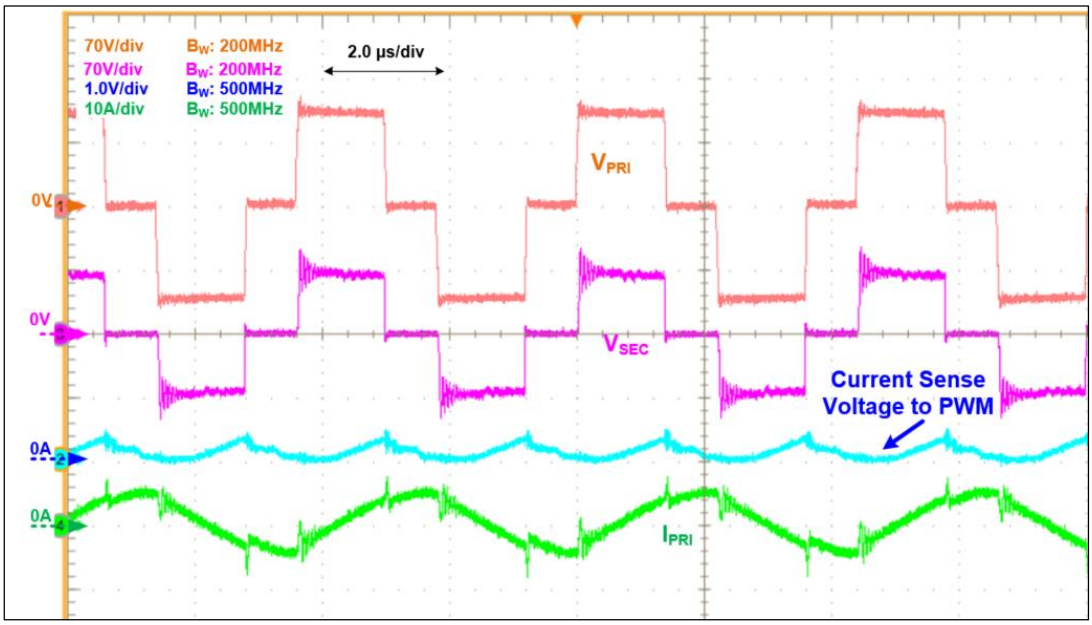

Figure 55. Current sense voltage into PWM current sense pin shown in blue for Phase Shifted Full Bridge operating at 1.0A load

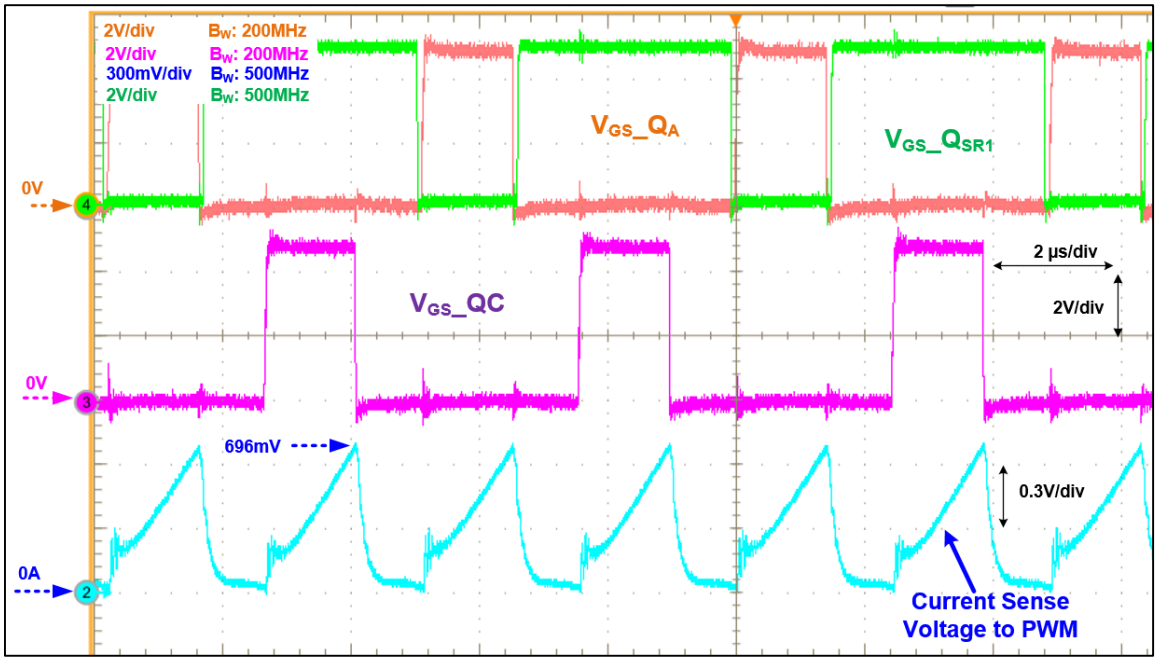

Figure 56. Current sense voltage into PWM current sense pin shown in blue for hard switched Full Bridge DC-DC converter operating at 400 W load

5.4. Rad-hard GaN FET Paralleling

Effective paralleling of the rad-hard GaN FETs in this work was verified using a FLIR thermal camera and by measuring each of the gate signals at the paralleled rad-hard GaN FETs. In this manner, uniform thermal distribution and time alignment among all gate control signals can be used to assess current sharing among the paralleled devices. Figure 57 shows a thermal image of the one of the phase legs switches in the Full Bridge power stage (lagging leg in phase shift modulation). Figure 58 shows a thermal image of both switches in the Current Doubler synchronous rectifier. Both thermal images were taken after more than 30 minutes of steady state operation at 400 W load, 100 V input, and 20 V output, with the converter sitting on the bench running at room ambient under natural convection. Figure 57 and Figure 58 thermal images show even heat distribution among all paralleled rad-hard GaN FETs in the Full Bridge and Current Doubler-rectifier power stages.

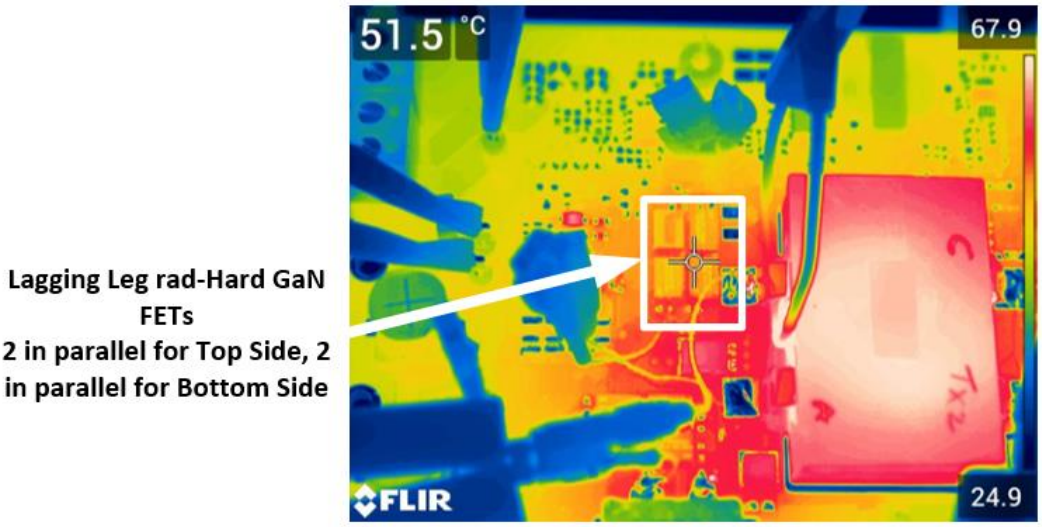

Figure 57. Thermal images showing good heat distribution at paralleled rad-hard GaN FETs in the lagging phase leg for the full bridge power stage 500 W load operation

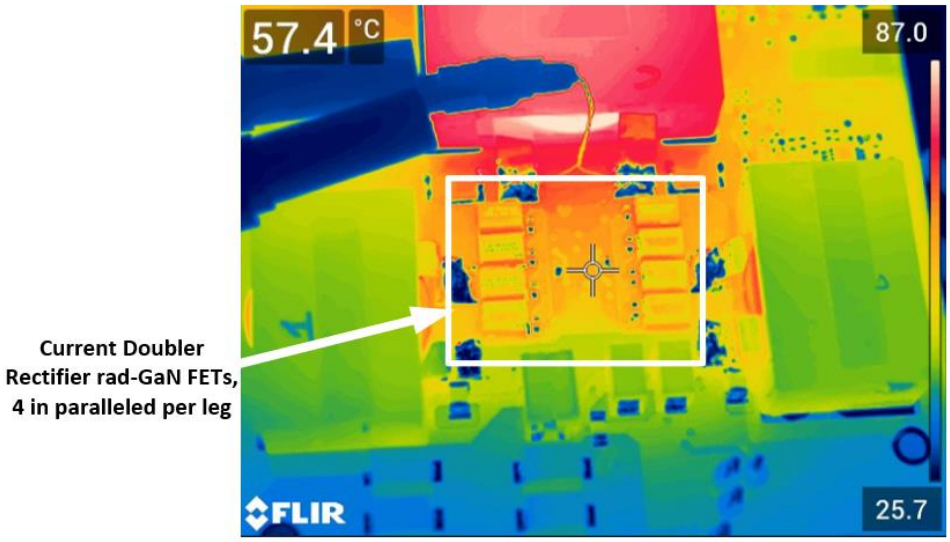

Figure 58. Thermal images showing good heat distribution at paralleled rad-hard GaN FETs in the Current Doubler rectifier for 500 W load operation

In addition, symmetry of the gate-source loops at the full bridge power stage and the Current Doubler-rectifier output stage were verified using an oscilloscope to measure the waveforms at each of the paralleled rad-hard GaN FETs. The oscilloscope channels and voltage

probes used for these measurements were time compensated to ensure accuracy of results. Figure 59 shows the gate-source voltages for each of the two paralleled rad-hard GaN FETs in the low side switch Q_B. Figure 60 shows the gate-source voltage waveforms for each of the four paralleled rad-hard GaN FETs in one of the phase legs of the Current Doubler rectifier. Both figures show that each gate control signal for the rad-hard GaN FETs are well time aligned; therefore, all each of the paralleled devices should be turning ON at around the same instants. The reduced propagation delay and low ringing between each of the paralleled devices demonstrated by these waveforms validate the PCB design, and it also serves to further confirm the results obtained from thermal images previously presented showing even power distribution among all paralleled GaN FETs.

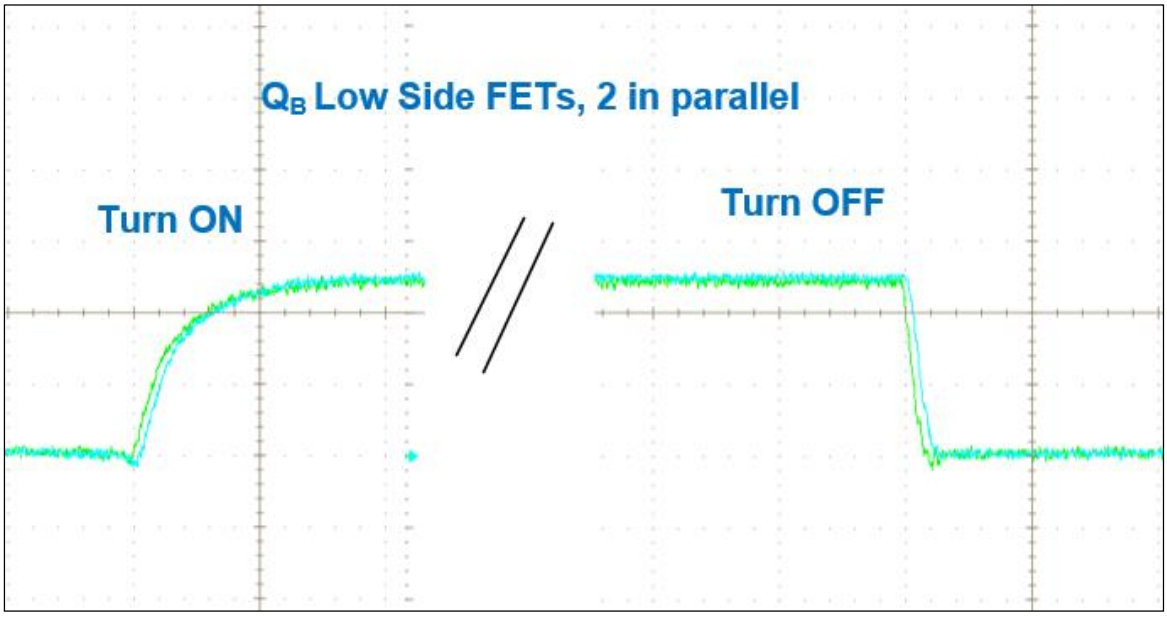

Figure 59. Q_B gate-source voltage waveforms for each of the two devices in parallel during turn ON and turn OFF, 400W load

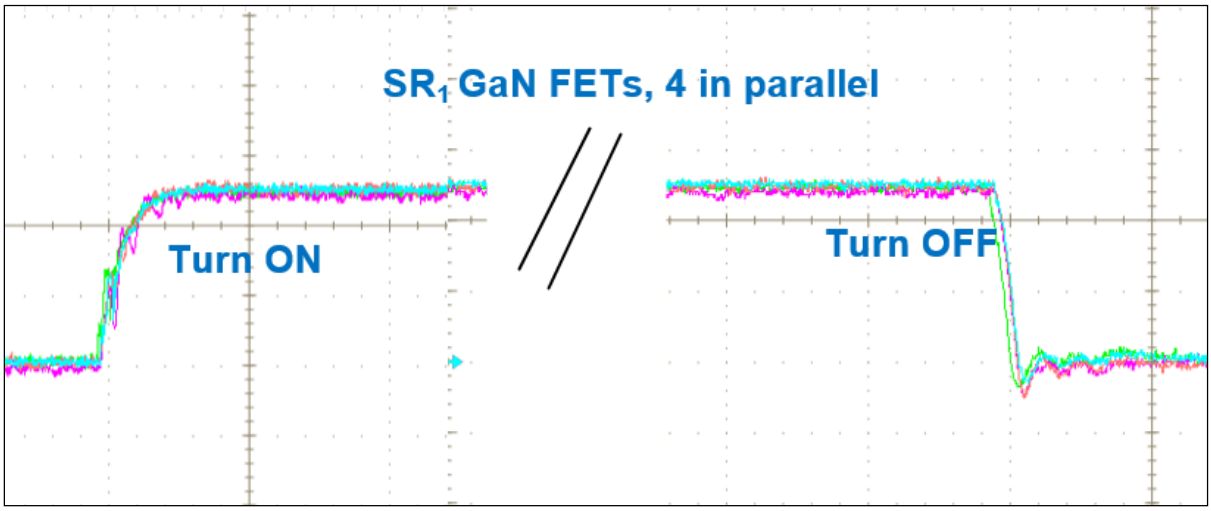

Figure 60. Rectifier rad-hard GaN FETs gate-source voltage waveforms for each of the four devices in parallel during turn ON and turn OFF

5.5. Efficiency Results

The efficiency performance of the Phase Shift Full Bridge DC-DC converter was measured with different magnetic designs. For the output inductors, helical flat wire windings and PCB embedded windings were considered, while for the power transformer helical flat wire windings, Litz wire, and PCB embedded windings were evaluated. In addition, the efficiency impact of the external resonant inductor L_{R_EXT} was studied by evaluating different inductor designs.

5.5.1. Transformer Evaluation

Table 28 summarizes the transformer designs evaluated in this work. In addition, Figure 61 shows the samples of transformer windings evaluated—Litz, Helical Flat wire, and PCB embedded windings. All windings were interleaved to minimize the effects of leakage inductive spike on the secondary side rectifiers. The secondary side spike from leakage inductance of the transformer was not clamped or snubbed to maximize efficiency. For ZVS operation in phase shift

modulation, an external inductor L_{R_EXT} was added, as previously mentioned. The energy from the external inductor was clamped by D_1 and D_2 shown in Figure 5.

Figure 62 shows a one-to-one comparison among all transformer windings. Efficiency curves for each of the 3 types of transformer windings were obtained for a 7:5 turns ratio design, and using the same external resonant inductor (1 µH custom inductor) and output inductors (6.25 µH). Efficiency was measured at 100 V input, 20 V output, with the converter running at room ambient temperature with natural convection. From Figure 62, Litz and Helical Flat wire based transformers were the most efficient, with Litz design being just slightly higher than helical flat wire. For manufacturability, helical flat wire was selected for the final design configuration due to its ease of assembly, especially when interleaving the transformer windings.

Table 28. Summary of Transformer Evaluation

Winding	Turns-Ratio	Efficiency	Manufacturability
Helical Flat Wire Winding	NP=7, NS=5	Best	Good
16 AWG Litz	NP=7, NS=5	Best	Poor
PCB Embedded	NP=7, NS=5	Poor	Best

Figure 61. Different transformer windings evaluated: Helical Flat Wire, PCB Embedded and Litz Wire

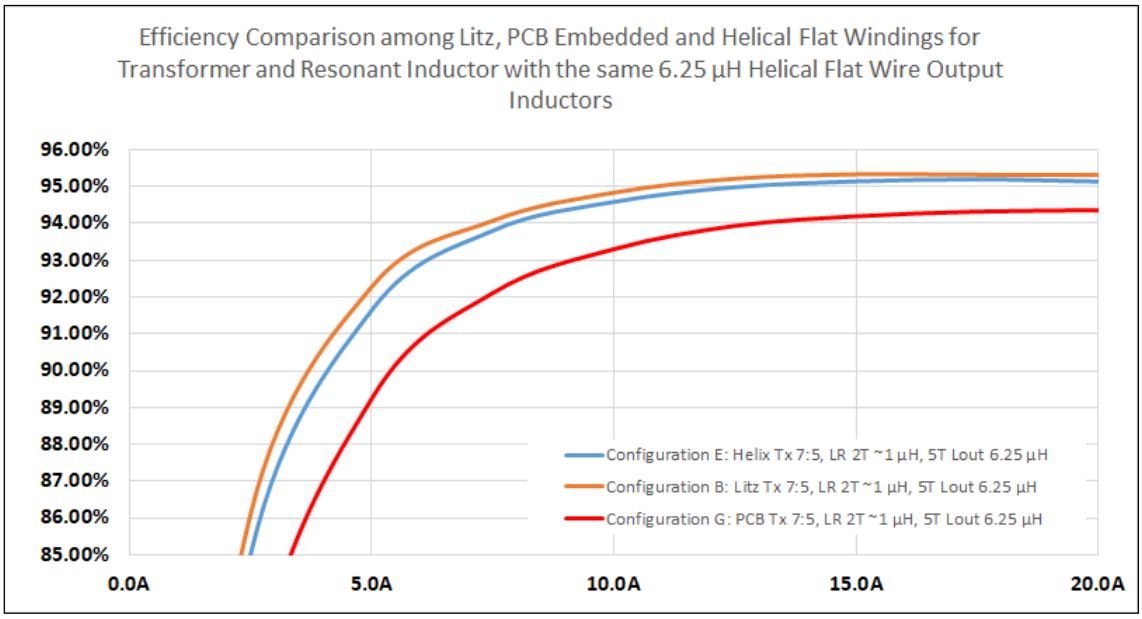

Figure 62. Efficiency comparison for Phase Shifted Full Bridge with different transformer windings

5.5.2. External Resonant Inductor Evaluation

A custom resonant inductor was designed based on the EQ20+PLT20 core from FerroxCube using 3C95 ferrite material. This inductor was evaluated with 1 and 2 turns of 16 AWG Litz wire, 1 and 2 turns of with 0.4 mm thick by 3.3 mm wide magnetic flat wire wounded as a helix, and with 2 turns made with PCB embedded windings with a least 15 oz. of copper weight per turn. Figure 63 show images of the different custom inductors made with the EQ20+PLT20 core.

The external resonant inductors based on the EQ20 ferrite were compared against commercial off the shelf (COTS) options from Coilcraft and Vishay. Table 29 summarizes the results for each of the external resonant inductors L_{R_EXT} evaluated during laboratory testing. During evaluation, the same power transformer (7:5 turns ratio with interleaved helical windings) and the same output inductors (6.25 µH), as well as input voltage, output voltage, dead times, and switching frequency were kept constant. Only the resonant inductors with values around 430 nH

to 1µH were varied to obtain a one-to-one comparison among the resonant inductor design samples.

Table 29. Summary of External Resonant Inductor Evaluation at 400 W, 100 V input, 20 V output

Inductor Type	Core Type	Winding Type	Number of Turns	Value	Efficiency	Core Temperature
EQ20+PLT20	3C95 Ferrite	16 AWG Litz	2	1 µH	95.15%	90.1°C
EQ20+PLT20	3C95 Ferrite	0.4 mm x 3.3 mm Flat Helical	2	1 µH	95.21%	87.4°C
EQ20+PLT20	3C95 Ferrite	0.5 mm (15 oz.) x 3.3 mm PCB Windings	2	1 µH	94.37%	105.3°C
EQ20+PLT20	3C95 Ferrite	0.4 mm x 3.3 mm Flat Helical	1	430 nH	95.20%	80.8°C
Vishay IHL6767-01	Powdered Iron	14 AWG Round Magnet Wire	3	470 nH	95.26%	60.8°C
Coilcraft SER2010-501NL	Unknown Ferrite	0.95mm x 2.35 mm Flat Helical	3	500 nH	94.96%	88.8°C
Coilcraft SER1590-501NL	Unknown Ferrite	0.95mm x 2.35 mm Flat Helical	3	500 nH	94.82%	98.1°C

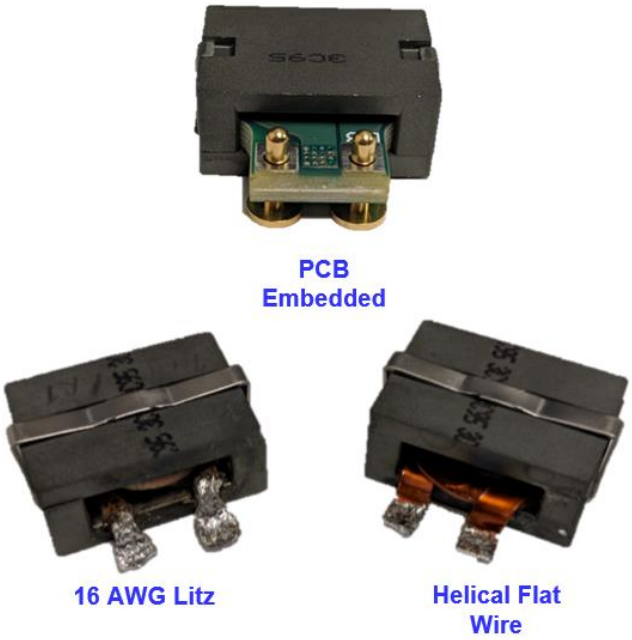

Figure 63. EQ20 3C95 ferrite magnetic core based resonant inductors with Litz (left) and Helical Flat Wire

Figure 64 provides an efficiency comparison showing the effects of each of the different resonant inductors evaluated. The test results showed that the Vishay IHLP-6767GZ-01 series with a 470 nH value yielded the highest efficiency (blue curve). Therefore, this part was selected for the final converter configuration for the Phase Shifted Full Bridge DC-DC converter.

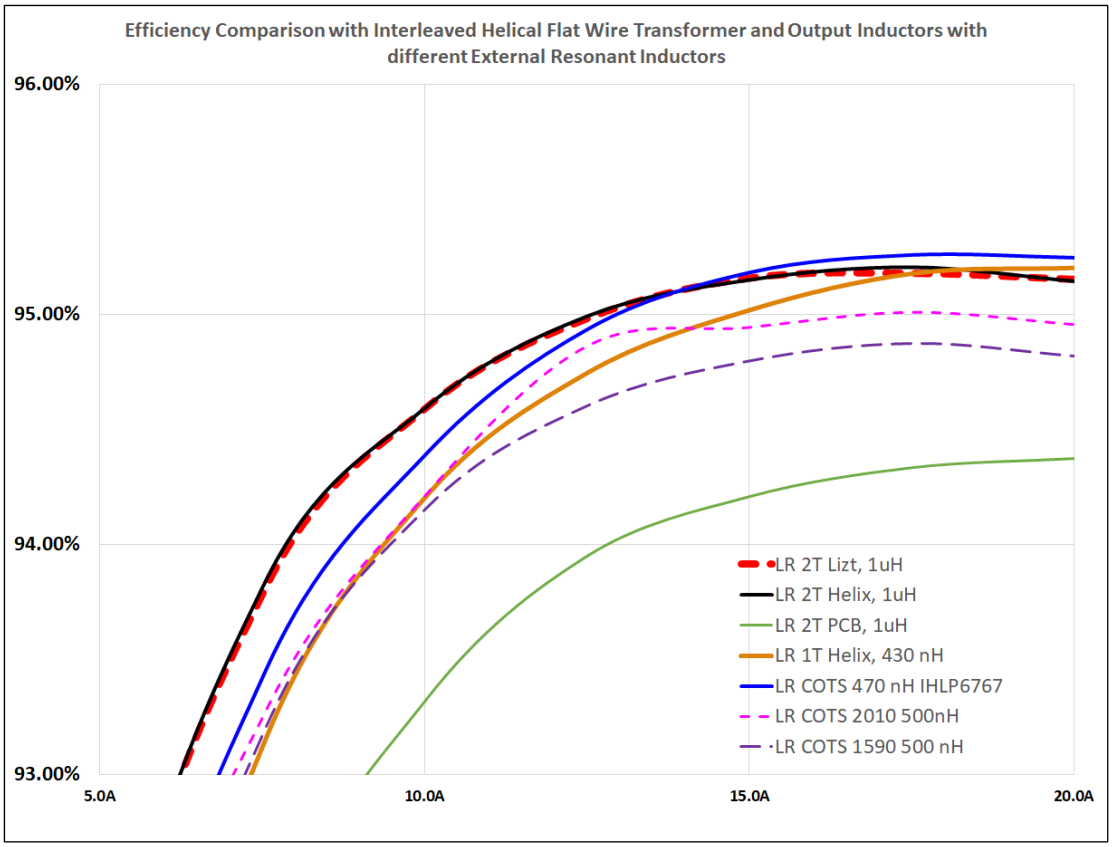

Figure 64. Efficiency comparison with Helical Flat wire transformer with 7:5 turns ratio and 6.25 µH flat wire helical output inductors for different resonant inductors constructions

5.5.3. Most Efficient Phase Shifted Full Bridge Configuration

After selecting the final external resonant from the previous section, the transformer turns ratio for the Phase Shifted Full Bridge converter was further optimized. The highest power converter efficiency was obtained from a 6:4 turns-ratio transformer with interleaved helical flat

wire on an EQ38 core from FerroxCube. In addition, this configuration used 5 turns of helical flat wire for each of the output inductors in the Current Doubler rectifier for an inductance of 6.25 µH. The powdered iron core inductor from Vishay proved to be the most efficient external inductor. The selected inductor came from the IHLP6767GZ-01 powdered iron inductor line from Vishay, with an inductance of 470 nH used in the final design. This brought the total resonant inductance to approximately 590 nH, including 120 nH from the leakage inductance of the power transformer. Figure 65 shows an efficiency curve for this configuration over output load at a100 V input, and 20 V output at room ambient temperature with natural convection.

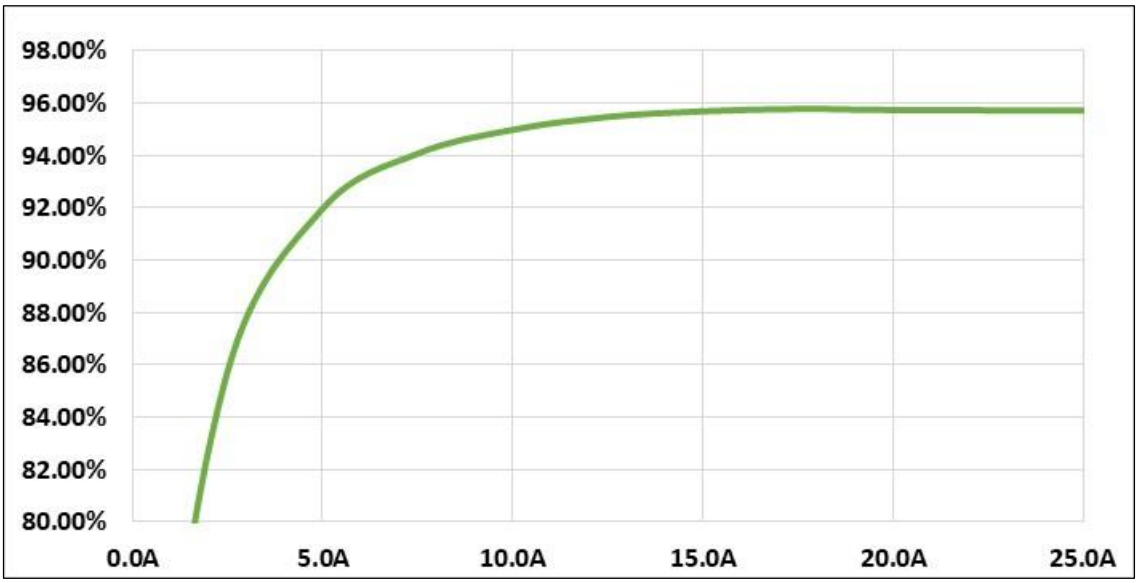

Figure 65. DC-DC Converter Efficiency with best magnetic winding configuration at 100V input, 20V output

The final converter configuration achieved a peak efficiency of 95.72% for a 100 V input, 20 V output at 500 W load. There is approximately 1% efficiency difference between predicted efficiency from modeling and the actual efficiency obtained during testing. This is in part due to the model not including the AC resistance loss in the power magnetics. Figure 66 shows a thermal image identifying the hottest components on the board after reaching thermal equilibrium under

natural convection, with an input of 100 V, and a load of 500 W at a 20 V output. From Figure 66, the power transformer and the external resonant inductor are the main source of power losses in the DC-DC converter.

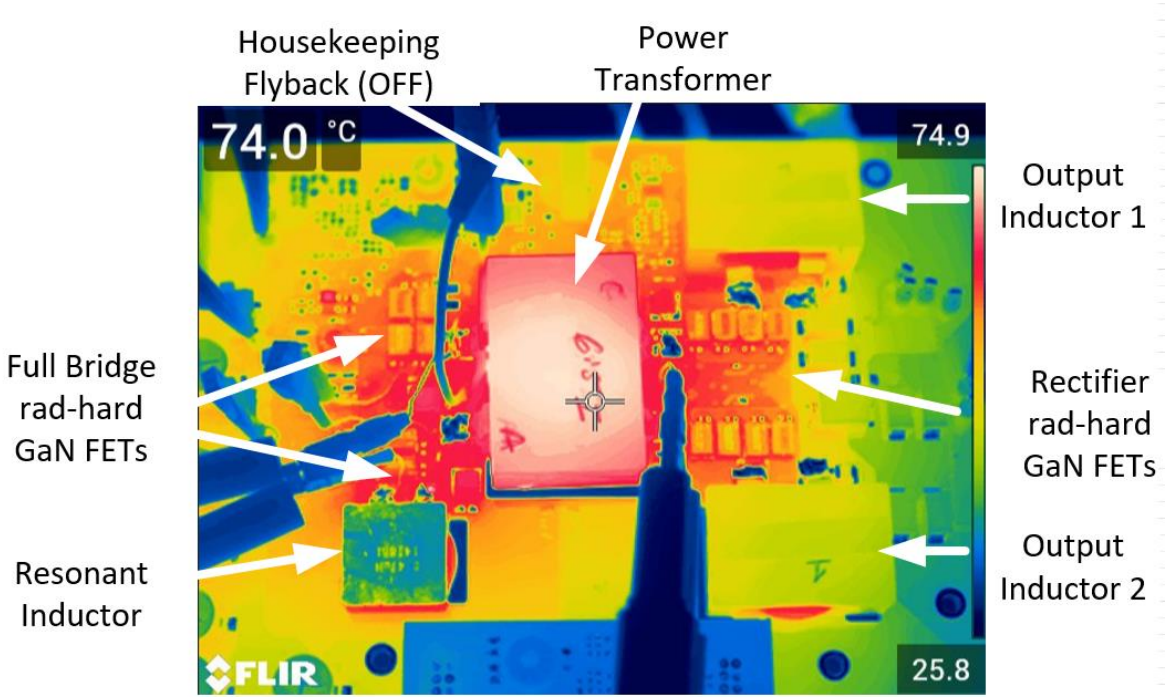

Figure 66. Thermal image of DC-DC Converter running at 500W load, 100V input, 20V output, 30 min operation, free-air

5.5.4. Phase Shifted Full Bridge versus Full Bridge Converter

This section describes the performance comparison between the Phase Shifted Full Bridge DC-DC converter achieving ZVS operation with the traditional hard switched Full Bridge DC-DC converter. The comparison focuses mainly in efficiency, power dissipation, and power stage stress. For this comparison, switching frequency, input voltage, output voltage, and magnetics design were kept constant. In addition, dead times were set to around 45 ns for both converters to ensure an almost one-to-one comparison between the two topologies. Figure 67 shows the efficiencies for both converters operating from no load to 400 W loads, with 100 V input, and 20

V regulated output. From this figure, it is clear that the Phase Shifted Full Bridge converter is more efficient, achieving efficiencies from 95.2% to 95.3% for 12.5A to 20A loads, respectively. On the other hand, the Full Bridge DC-DC converter achieved efficiencies from 94.5% to 95.1% at the same load range.

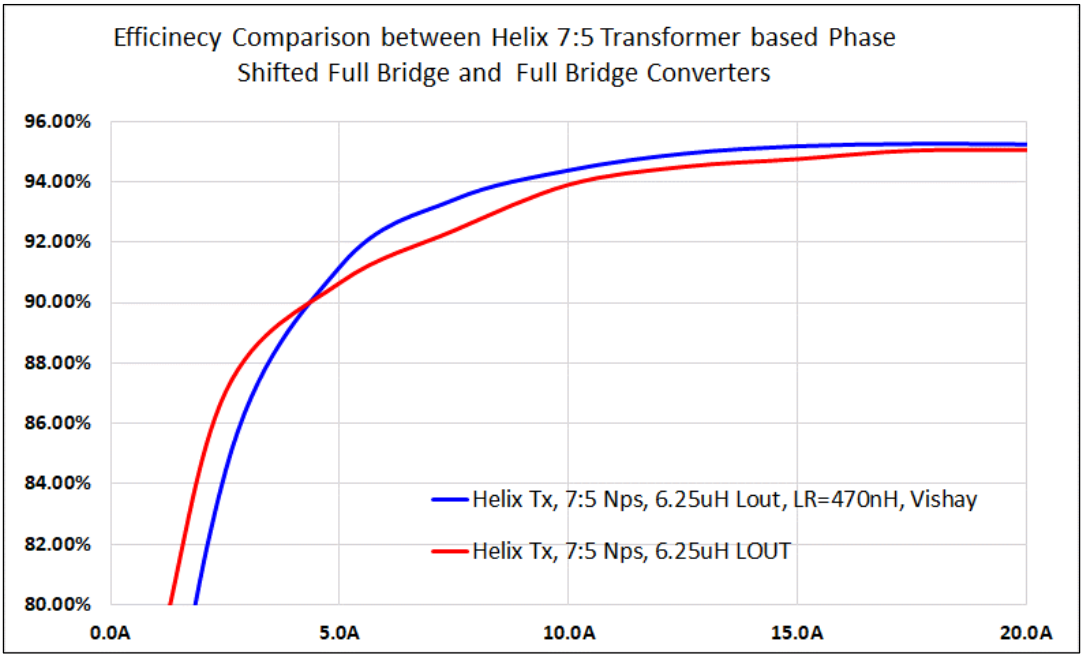

Figure 67. Efficiency comparison for Phase Shifted Full Bridge and conventional Full bridge converters

In terms of voltage stress, the Phase Shifted Full Bridge design was also better with very low parasitic ringing on the primary side at about 108V, and with around 103 V of voltage stress on the secondary side rectifiers FETs. For the same operating conditions (full load, 100 V input, 20 V output), the Full Bridge design resulted in 142 V of peak voltage stress on the primary side FETs, and approximately 170 V of voltage stress on the secondary side FETs. Note that both results were obtained with the same power transformer design achieving leakage inductances of approximately 120 nH. Assuming that all the energy in the external resonant inductor L_{R_EXT} is successfully circulated back to the input source by D_1 and D_2 in Figure 5, the soft-switched

operation of the Phase Shifted Full Bridge converter has the added benefit of lower voltage stress on the secondary side due to the slower *di/dt* excitation of L_{LK}. Figure 68 and Figure 69 show the component voltage stress in the rad-hard GaN FETs for both converters.

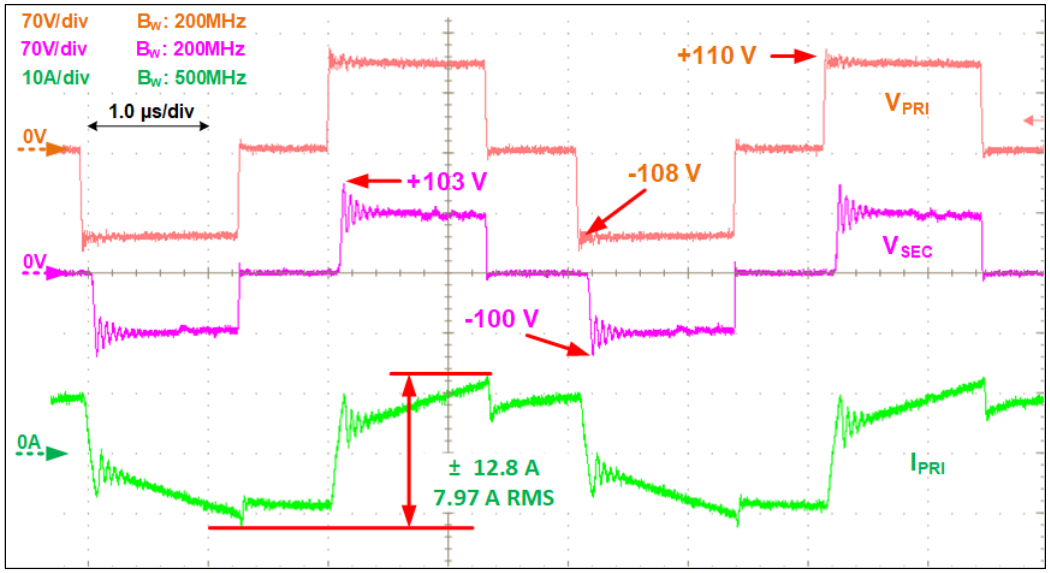

Figure 68. Phase Shifted Full Bridge DC-DC Converter: primary FETs peak voltage (orange), rectifier FETs peak voltage (purple), and transformer primary current (green) at 400 W load, 100V input, 20 V output

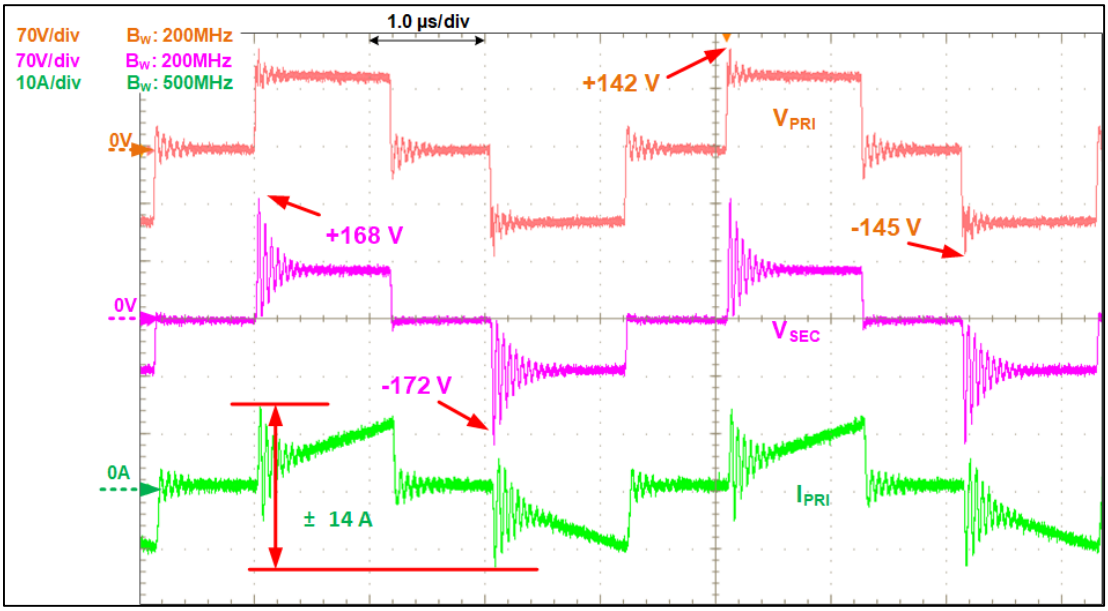

Figure 69. Full Bridge DC-DC Converter: primary FETs peak voltage (orange), rectifier FETs peak voltage (purple), and transformer primary current (green) at 400 W load, 100V input, 20 V output

From the comparisons made in this section, it is clear that the best option for this application is the Phase Shifted Full Bridge converter. The Full Bridge converter was only slightly less efficient than the Phases Shifted Full Bridge; however, the amount of ringing on the secondary side for the Full Bridge converter would require a more aggressive snubbing or clamping network to reduce voltage stress. For the Full Bridge DC-DC converter tested here, no snubbing or clamping was added at the secondary side such that a very close one-to-one comparison could be obtained.

Nonetheless, the efficiency of the Full Bridge converter was still good at around 95%. Furthermore, the power transformer was not optimized for this converter, thus there is opportunity to push the efficiency of this converter to values higher than 95% by optimizing the duty cycle and transformer turns ratio. This, as mentioned before, would come at the penalty of high secondary side voltage stress, additional power loss from rectifier snubbing or clamping, and higher EMI due to fast *di/dt* and *dv/dt* transitions from hard switching the rad-hard GaN FETs.

Chapter 6 Conclusions

6.1. Conclusions from Gate Driver Design

Section 3.3 describes the self-powered gate driver designed for the Phase Shifted Full Bridge DC-DC converter using recently released rad-hard GaN FETs. The proposed solution uses pulse transformers to overcome the lack of space qualified digital isolators with small propagation delays and fast rise and fall times required for new rad-hard GaN FETs. The gate driver was tested on a power stage that uses 200V, 18A, 26 mΩ rad-hard GaN FETs from Freebird Semiconductor. Section 5.1 presents laboratory validation results for this self-powered gate driver.

A full bridge power stage controlled using phase shift modulation operates with all the switches running at 50% duty cycle all the time. This avoids the risk of the pulse transformer not resetting during steady state operation, which in turn simplifies the pulse transformer based gate driver design. However, low input to output capacitance $C_{I/O}$ is hard to achieve in a pulse transformer so CMTI achieved was lower than what is commonly recommended for GaN applications [58]. The Phase Shifted Full Bridge DC-DC converter achieves ZVS operation as the output load increases. The smaller *dv/dt* obtained from soft switching in this converter alleviates the requirement of high CMTI at the pulse transformer.

The gate driver designed in this work uses the pulse transformer to provide control isolation for all the switches, and to provide energy for the GaN FET gate drivers for the switches in the full bridge power stage. A voltage doubler rectifier was used on the secondary side of the pulse transformer to provide approximately 8.6 V of bias voltage for the GaN FET gate driver ICs. The GaN gate driver IC targeted for this application has an internal LDO linear regulator to ensure a nominal 5.0 V gate drive is used for the rad-hard GaN FETs.

One of main challenges for the circuit described in 3.3 is achieving good dead time accuracy for both topside rad-hard GaN FETs. This problem arises from having the time delay capacitor C_{DA} in Figure 23 referenced to the gate return (source) node of the topside FET. This is the half-leg switch node and for GaN devices can transition very fast—5.1 GV/s in this design under ZVS operation. This can cause C_{DA} to discharge depending on the value selected, and requires current to flow back into the capacitor from the pulse transformer faster than the current from the common source node discharges.

Better accuracy (5ns error) was achieved by increasing the value of C_{DA} toward 1nF from a staring 100 pF value, and by adjusting R_{DA} between 56 Ω to 100 Ω depending on the dead-time interval required. In addition, the prototype included damping resistors along the path of the control signal from the pulse transformer to the input of the time delay circuit. All damping resistors were set closer to 1 Ω from 20 Ω to reduce resistance along the control signal path. Dead-time accuracy can be further improved by mounting the gate driver on the same PCB as the power stage. Furthermore, in the UCC27611 GaN gate driver used in this work does not have a dedicated GaN FET gate return pin. Therefore, the GaN FET gate return and the gate driver IC ground must be shared. Dedicated separate ground connections for the control signal input to the gate driver and the GaN FET's gate return are recommended in a high side gate drive implementation. This can be achieved by separating the return path of C_{DA} from the gate drive IC ground (which is also the FET gate return), and then tying it to the GaN gate driver IC ground via a smaller trace.

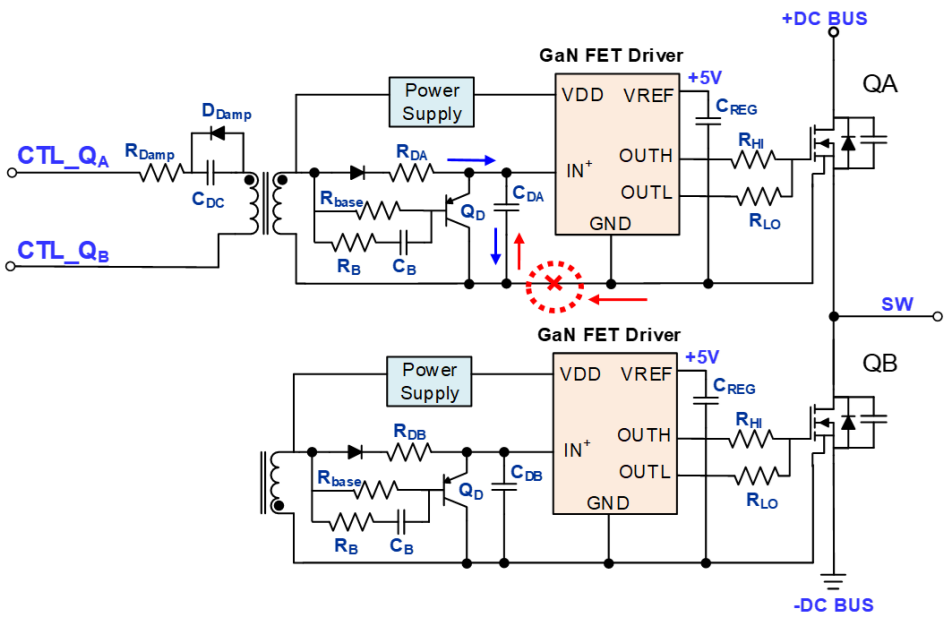

Figure 70. Dead time controller current flow from source node into C_{DA}, circled "x" is where signal must be separated by increasing trace impedance

In addition, section 3.5 describes a similar self-powered gate driver was designed to operate the converter using hard switched PWM modulation at the Full Bridge power stage. In this configuration, the control signal duty cycle is modulated at the full bridge switches so additional care must be taken if pulse transformers are used. Additionally, the high input to output capacitance $C_{I/O}$ of a pulse transformer can be more problematic in a hard switched GaN based Full Bridge converter because of the faster *dv/dt* transition at the half leg switching nodes. For the Full Bridge DC-DC converter implemented in this work, GMR digital isolators were used instead of pulse transformers for control signal isolation. These isolators are a potential option for future space applications [33, 34, 66], but no space qualified solutions are available yet. The GMR isolator used for the isolated gate driver for the Full Bridge DC-DC converter is the IL610 from NVE Corporation. This isolator can achieve approximately 70 kV/µs of CMTI by increasing the passive input drive current to approximately 10 mA. Section 5.2 presented laboratory verification results

of the isolated gate driver for the hard switched Full Bridge DC-DC converter design using the GMR isolators.

6.2. Conclusions from Power Stage Design

This thesis describes the implementation of a DC-DC Phase Shifted Full Bridge converter with synchronous Current Doubler rectifier for space applications. Recently available 200 V, 18 A, rad-hard GaN FETs from Freebird Semiconductor were successfully validated in the topology with a discrete analog peak current mode controller implementation. The controller uses a PWM controller that generates a single control signal that is then conditioned to create four control signals to operate the Full Bridge power stage with Phase Shift Modulation (PSM), and two additional signals to control the Current Doubler synchronous rectifier in the secondary side. Section 3.3 presents the proposed circuit for PWM to PSM control.

Main design considerations to implement the selected topology in a real space application are included in 3.2. Section 3.6 presents the design methodology followed to design the Phase Shifted Full Bridge converter. Section 4.1 provides details on PCB layout, with special focus on paralleling the FBG20N18B 200V rad-hard GaN FETs in the power stage. A converter prototype running Phase Shift Modulation and another operating as a typical hard switched Full Bridge were built and tested. Both converters achieved efficiencies around 95% at 400 W and above when operating with a 100V input, 20 V output. Further efficiency increase can be achieved by optimizing the power transformer turns ratio, and this was demonstrated in the Phase Shifted Full Bridge design. The additional efficiency improvement at 500 W load resulting from changing the power transformer primary to secondary turns ratio N_{PS} from 1.4 to 1.5 was approximately 0.5%. The converter input range for this work is 95 V to 120 V, with an output adjustment range of 18

V to 24 V which penalizes efficiency at nominal 100 V input, and 20 V output. Narrower input and output voltage ranges should result in a Phase Shifted Full Bridge DC-DC converter design achieving closer to 96% and higher efficiency.

Finally, the converter designed in this work can be easily migrated into a fully rad-hard compliant design for evaluation under radiation. For this, additional fault protection circuitry must be added to the design, especially after converter failure modes under radiation are better understood through radiation testing.

6.3. Collection of Practical Circuits

The final converter prototype included startup sequencing and under voltage lockout circuitry, as well as a startup bias and Flyback converter using 300V rad-hard GaN FETs from Freebird semiconductor with embedded PCB transformer windings. In addition, a second stage output LC filter was added to the design to meet output ripple requirements for this application. These converter sub-components are important pieces of a practical design approach; however, their description was not included in the main scope of this thesis. The focus of this thesis is on the power stage, gate driver design, and controller design for both soft switched and hard switched versions of the converter. The specific circuits that are included in this document are summarized in the table below for ease of referencing.

Table 30. Collection of Practical Circuits

Circuit Details	Section	Circuit
PWM Controller Implementation	3.2.5	Figure 9
Current sensing for both PSM and PWM Full Bridge DC-DC Converters	3.2.6	Figure 12
PWM to Phase Shift Modulation Control	3.3.2	Figure 16
Synchronous Current Doubler Rectifier Control for Phase Shifted Full Bridge	3.3.3	Figure 18
Self-biasing scheme for isolated GaN gate driver for Phase Shifted Full Bridge DC-DC Converter	3.3.4	Figure 20
Dead-time and Control Signal Conditioning for Full Bridge power stage	3.3.5	Figure 23
PWM to hard switched Full Bridge Control	3.5.1	Figure 26
Self-biasing scheme for isolated GaN gate driver for Full Bridge DC-DC Converter	3.5.1	Figure 28
Synchronous Current Doubler Rectifier Control for Full Bridge	3.5.2	Figure 29

6.4. Prospective Areas for Future Research

This work achieves a practical implementation of the Phase Shifted Full Bridge DC-DC converter for space applications using the FBG20N18B 200V rad-hard GaN FETs from Freebird Semiconductor. However, there are very important areas that were outside the scope of this work that can be explored by future research. One of them is in design optimization of the converter for power density and efficiency, mainly in relation to power magnetics design. Detailed power transformer and external resonant inductor modeling for AC resistance and related power losses are not included in this work. As a result, the loss model described in 3.7 has an unaccounted loss of approximately 4 W to 5 W. Figure 66 shows that the power transformer and resonant inductors are the hottest spots in the converter; therefore, the additional power loss not included in the loss model must be located in these two devices.

In regards to power density, and still related to magnetics design, resonant inductance integration into the power transformer that would result in a very controllable inductance value is important. For a practical application where high reliability is required over the life of the converter; therefore, repeatable and predictable resonant inductance in the form of power

transformer leakage inductance is necessary. This is not only important to maintain the ZVS range and efficiency of the converter, but also it is very important to worst-case analysis and lifetime stress analysis for the rad-hard GaN FETs in the Current Doubler rectifier. On the same line, integration and coupling of the Current Doubler inductors in one core has been proposed in several works [71-74] and can be applied to this converter to further increase power density.

The behavior of GaN FETs under long-term radiation is another potential research area that can be further explored. Literature review performed in this work related to this topic show that GaN FETs are very tolerant to radiation; however, there are also still open questions related to their long-term reliability in space [24-29]. For instance, long-term performance degradation specific to GaN FETs such as the effects of dynamic R_{DSON} over long-term exposure to radiation, for example, still require further understanding.

The Phase Shifted Full Bridge converter designed in this thesis provides a path for a one-to-one transition into a prototype built with space rated components such that the topology can be further studied under radiation exposure. Nonetheless, a complete failure mode study under exposure to total dose and single event effects needs to investigated and well understood. Future research topics cannot only study the Phase Shifted Full Bridge operation under radiation, but can also include fault mitigation to ensure the converter can be fully qualified under radiation. For example, an important fault protection mechanism that needs additional research is fast over current and short circuit protection integrated into the GaN FET gate drivers or implemented at the converter level.

The Full Bridge DC-DC converter implementation in this work uses GMR digital isolators instead of pulse transformers. Currently, there are no GMR digital isolators qualified for space applications. These type of isolators have passive magnetic front ends and can offer great potential

for future space applications as outlined in [33, 34, 66]. Therefore, another potential area of research is the study of GMR digital isolators under radiation, and their application for space power converter applications. In particular, GMR digital isolator performance and CMTI under radiation and the resulting effects on performance when used for topside isolated GaN FET gate drivers in half-bridge based converters can be explored.

References

[1] VPT, Inc., "VHR100+2800S Series High Reliability COTS DC-DC Converters," VHR100+2805S datasheet, 2017.

[2] VPT, Inc., "SVRFL2800S Series Space Qualified Hybrid DC-DC Converters," SVRFL2800S datasheet, 2018.

[3] International Rectifier HiRel, "High Reliability, High Efficiency Radiation Hardened DC-DC Converter, GH-Series," GH2805S datasheet, 2016.

[4] G. E. Aguiar, "DC-DC Converter for Aerospace Industry," M.S. Thesis, Technical University of Lisbon, Lisbon, Portugal, 2011.

[5] L. D. Edmonds, C. E. Barnes, and L. Z. Scheick, "An Introduction to Space Radiation Effects on Microelectronics," NASA Jet Propulsion Laboratory, JPL Publication 00-06, Pasadena, CA, 2000, pp. 11–59.

[6] L. Scheick, "Testing Guidelines for Single Event Gate Rupture (SEGR) of Power MOSFETS," NASA Jet Propulsion Laboratory, JPL Publication 08-10 2/08, Pasadena, CA.

[7] R. A. Mammano, Fundamentals of power supply design: technology from Unitrode/Texas Instruments Power Supply Design Seminars, 1st ed. Dallas, TX: Texas Instruments, 2017.

[8] B. Bell and A. Hari, "Topology Key to Power Density in Isolated DC-DC Converters," Power Electronics Technology, pp. 16–20, Feb-2011.

[9] J. Walden, "Radiation Induced Effects in Electronic Devices and Radiation Hardening by Design Techniques," M.S. thesis. Linkopings University, Sweden, Europe. 2014.

[10] J. L. Titus, "An Updated Perspective of Single Event Gate Rupture and Single Event Burnout in Power MOSFETs," IEEE Transactions on Nuclear Science, vol. 60, no. 3, pp. 1912–1928, 2013.

[11] Y. H. Lho and K. Y. Kim, "Radiation Effects on the Power MOSFET for Space Applications," ETRI Journal, vol. 27, no. 4, pp. 449–452, Sep. 2005.

[12] M. Inoue, T. Kobayashi, and A. Maruyama, "High Reliability Power MOSFETs for Space Applications," Fuji Electric Review, vol. 56, no. 2, pp. 69–73, 2010.

[13] M. Shaneyfelt, D. Fleetwood, P. Winokur, J. Schwank, and T. Meisenheimer, "Effects of device scaling and geometry on MOS radiation hardness assurance," IEEE Transactions on Nuclear Science, vol. 40, no. 6, pp. 1678–1685, 1993.

[14] P. M. Shea, "Lateral power MOSFETs hardened against single event radiation effects," dissertation, Orlando, FL, 2011.

[15] G. Johnson, J. Palau, C. Dachs, K. Galloway, and R. Schrimpf, “A review of the techniques used for modeling single-event effects in power MOSFETs,” IEEE Transactions on Nuclear Science, vol. 43, no. 2, pp. 546–560, 1996.

[16] International Rectifier Hi-Rel, “Radiation Hardened Power MOSFET Surface Mount (SMD-2),” IRHNA67260 datasheet, 2017.

[17] Microsemi, “Radiation Hardened N-Channel MOSFET, Reference 7T4-LDS-012,” JANSF2N7269U datasheet, 207, Rev. 2.0.

[18] International Rectifier, “IRFS422 PDP Switch,” IRFS4227TRLPBF datasheet, 2018.

[19] Toshiba, “Silicon N-channel MOS (U-MOS VIII-H),” TPH2900ENH datasheet, 2014, Rev. 3.0.

[20] Infineon Technologies, “OptiMOSTM3 Power Transistor, 200V,” IPT111N20NFDATMA1 datasheet, 2016, Rev. 2.1.

[21] Murata Power Solutions, “Low Profile Isolated Quarter Brick 2.5-40A DC-DC Converters” UVQ-5/20-D24P datasheet, 2018.

[22] Artesyn, “AVQ100-24 Series, 100 Watts” AVQ100-24S05 datasheet, 2015.

[23] N. E. Ives, J. Chen, A. F. Witulski, R. D. Schrimpf, D. M. Fleetwood, R. W. Bruce, M. W. Mccurdy, E. X. Zhang, and L. W. Massengill, “Effects of Proton-Induced Displacement Damage on Gallium Nitride HEMTs in RF Power Amplifier Applications,” IEEE Transactions on Nuclear Science, vol. 62, no. 6, pp. 2417–2422, 2015.

[24] A. Lidow J. B. Witcher K. Smalley "Enhancement mode gallium nitride (eGaNTM) FET characteristics under long term stress" Proc. GOMACTech 2011.

[25] A. Kalavagunta, A. Touboul, L. Shen, R. D. Schrimpf, R. A. Reed, D. M. Fleetwood, R. K. Jain, and U. K. Mishra, “Electrostatic Mechanisms Responsible for Device Degradation in Proton Irradiated AlGaN/AlN/GaN HEMTs,” IEEE Transactions on Nuclear Science, vol. 55, no. 4, pp. 2106–2112, 2008.

[26] A. Lidow, A. Nakata, M. Rearwin, J. Strydom, and A. M. Zafrani, “Single-Event and Radiation Effect on Enhancement Mode Gallium Nitride FETs,” 2014 IEEE Radiation Effects Data Workshop (REDW), 2014.

[27] A. Ionascut-Nedelcescu, C. Carlone, A. Houdayer, H. V. Bardeleben, J.-L. Cantin, and S. Raymond, “Radiation hardness of gallium nitride,” IEEE Transactions on Nuclear Science, vol. 49, no. 6, pp. 2733–2738, 2002.

[28] S. J. Pearton, F. Ren, E. Patrick, M. E. Law, and A. Y. Polyakov, “Review—Ionizing Radiation Damage Effects on GaN Devices,” ECS Journal of Solid State Science and Technology, vol. 5, no. 2, 2015.

[29] A. Lidow K. Smalley "Radiation tolerant enhancement mode gallium nitride (eGaNTM) FET characteristics" Proc. GOMACTech pp. 1-3 2012.

[30] A. Liddow, J. Strydom, M. Rearwin, "Radiation Tolerant Enhancement-Mode Gallium Nitride FETs for High Frequency DC-DC Conversion", Nuclear and Space Radiation Effects Conference 2014, 2014.

[31] Freebird Semiconductor, “Rad Hard e-GaN 200V, 18A, 6mΩ Surface Mount (FSMD-B),” FBG20N18B datasheet, 2016, Rev Q6.

[32] Intersil, “ISL70024SEH, ISL73024SEH 200V, 7.5A Enhancement Mode GaN Power Transistor,” ISL70024SEH datasheet, 2018, Rev 3.0.

[33] M. Wind, J. V. Bagalkote, P. Clemens, T. Kundgen, M. Latocha, W. Lennartz, S. Metzger, M. Poizat, S. Ruge, M. Steffens, and P. Beck, “Comprehensive radiation characterization of digital isolators,” 2016 16th European Conference on Radiation and Its Effects on Components and Systems (RADECS), 2016.

[34] M. A. Jacobson S. P. Buchner H. L. Hughes P. J. McMarr "SEE and TID results for commercial non-optogalvanic isolators for space application" Proc. IEEE Radiation Effects Data Workshop pp. 1-3 2011-Jul.

[35] NVE Corporation, “Passive-Input Digital Isolators-CMOS Outputs,” IL600 Series Isolators datasheet, 2017, Rev. AC.

[36] K. Label, S. Kniffin, R. Reed, H. Kim, J. Wert, D. Oberg, E. Normand, A. Johnston, G. Lum, R. Koga, S. Crain, J. Schwank, G. Hash, S. Buchner, J. Mann, L. Simpkins, M. Dordine, C. Marshall, M. Obryan, C. Seidleck, L. Nguyen, M. Carts, R. Ladbury, and J. Howard, “A compendium of recent optocoupler radiation test data,” 2000 IEEE Radiation Effects Data Workshop. Workshop Record. Held in conjunction with IEEE Nuclear and Space Radiation Effects Conference (Cat. No.00TH8527).

[37] A. H. Johnston and T. F. Miyahira, “Radiation Damage in Power MOSFET Optocouplers,” IEEE Transactions on Nuclear Science, vol. 54, no. 4, pp. 1104–1109, 2007.

[38] P. Adell, O. Mion, R. Schrimpf, C. Chatry, P. Calvel, and M. Melotte, “Single event transient propagation through digital optocouplers,” IEEE Transactions on Nuclear Science, vol. 52, no. 4, pp. 1136–1139, 2005.

[39] A. Johnston and B. Rax, “Proton damage in linear and digital optocouplers,” IEEE Transactions on Nuclear Science, vol. 47, no. 3, pp. 675–681, 2000.

[40] R. Reed, C. Poivey, P. Marshall, K. Label, C. Marshall, S. Kniffin, J. Barth, and C. Seidleck, “Assessing the impact of the space radiation environment on parametric degradation and single-event transients in optocouplers,” IEEE Transactions on Nuclear Science, vol. 48, no. 6, pp. 2202–2209, 2001.

[41] Intersil, “Radiation Hardened Low Side GaN FET Driver,” ISL70040SEH, ISL73040SEH datasheet, 2018, Rev 3.00.

[42] Texas Instruments, “Low Side GaN Driver,” UCC27611 datasheet, 2012, Rev 03-18.

[43] L. Pinero and G. Bowers, “Multi-Kilowatt Power Module for High Power Hall Thrusters,” 40th AIAA/ASME/SAE/ASEE Joint Propulsion Conference and Exhibit, Nov. 2004.

[44] L. Pinero and G. Bowers, “High Performance Power Module for Hall Effect Thrusters,” 38th AIAA/ASME/SAE/ASEE Joint Propulsion Conference & Exhibit, Jul. 2002.

[45] X. He, Y. Dong, C. Lu, T. Liu, K. Gao, and S. Liu, “Research on phase-shifted full-bridge converter applied in the anode-supply of hall electric propulsion,” 2015 IEEE 11th International Conference on Power Electronics and Drive Systems, 2015.

[46] P. K. Joseph, B. N. V, N. B. Sharma, and V. H. Jani, “Analysis of digital PWM design for Zero Voltage Transition Phase Shifted Full Bridge converters for space applications,” 2016 International Conference on Emerging Trends in Communication Technologies (ETCT), 2016.

[47] Texas Instruments, “UC1875 Phase Shift Resonant Controller,” UC1875 datasheet, 2007, Rev. C.

[48] Intersil, “Radiation Hardened, High Performance Industry Standard Single-Ended Current Mode PWM Controller,” ISL78840ASxH, ISL78841ASxH, ISL78843ASxH, ISL78845ASxH datasheet, 2018, Rev. 2.00.

[49] Texas Instruments, “Dual Positive-Edge Triggered D-Type Flip-Flops with Clear and Preset,” SN54AC74, SN74AC74 datasheet, 1995, Rev 10-03.

[50] Texas Instruments, “Rad-Tolerant Class V, Quadruple 2-Input Positive NOR Gates,” SN54AC02-SP datasheet, 2008, Rev 12-08.

[51] Texas Instruments, “Quadruple 2-Input Positive AND Gates,” SN54AHCT08, SN74AHCT08 datasheet, 1995, Rev 09-15.

[52] Todd P. C. “Extend current transformer range,” Unitrode Design Note DN-41, 1999.

[53] J. Sabate, V. Vlatkovic, R. Ridley, F. Lee, and B. Cho, “Design considerations for high-voltage high-power Full Bridge zero-voltage-switched PWM converter,” Fifth Annual Proceedings on Applied Power Electronics Conference and Exposition, 1990.

[54] Sable, D.M. and Lee, F.C. “The operation of a Full Bridge, zero-voltage-switched PWM converter”. Proceedings of the Virginia Power Electronics Center Seminar, pp. 92–97, 1989.

[55] V. Vlatkovic, J. Sabate, R. Ridley, F. Lee, and B. Cho, “Small-signal analysis of the phase-shifted PWM converter,” IEEE Transactions on Power Electronics, vol. 7, no. 1, pp. 128–135, 1992.

[56] S. Abdel-Rahman, “Design of a Phase Shifted Full-Bridge Converter with Current Doubler Rectifier,” Infineon Technologies North America Design Note DN-2013-01, 2013.

[57] R. Redl, N. Sokal, and L. Balogh, “A novel soft-switching Full Bridge DC/DC converter: Analysis, design considerations, and experimental results at 1.5 kW, 100 kHz,” 21st Annual IEEE Conference on Power Electronics Specialists.

[58] A. Chu, “Evaluation and Design of a SiC-Based Bidirectional Isolated DC/DC Converter,” M.S. thesis, Virginia Tech, Blacksburg, VA, USA, 2017.

[59] S. Biswas, B. Basak, and K. Rajashekara, “Gate drive methods for IGBTs in bridge configurations,” Proceedings of 1994 IEEE Industry Applications Society Annual Meeting.

[60] B. Kennedy, “Implementing an Isolated Half-Bridge Gate Driver,” Analog Dialogue 46-11 Back Burner, 2012.

[61] R. Ridley, “Gate Drive Design Tips,” Power Systems Design Europe, pp. 16–18, Dec-2006.

[62] L. Balogh, “Design and Application Guide for High Speed MOSFET Gate Drive Circuits,” Texas Instruments Application Note.

[63] V. J. Spataro, “Design High-Performance pulse transformers in easy stage,” EDN, 16-Mar-1995.

[64] “ADuM1100, iCoupler Digital Isolator, Data Sheet, Rev. K, 07/2015,” Analog Devices Inc.

[65] Magnetics, Inc., “Specifications for 0J4075TC,” 0J4075TC datasheet, 2018.

[66] Glenn Research Center, R. Patterson, A. Hammoud, and S. Panko, Operation of a Giant Magnetoresistive (GMR) Digital Isolator, Type IL510, Under Extreme Temperatures, IC., vol. DOC. NASA Technical Reports Server.

[67] NVE Corporation “GMR in Isolation,” Application Bulletin AB-7, ISB-AP-007; Rev. March 2008. http://www.Isoloop.com.

[68] FerroxCube, “3C95 Material Specification,” 3C95 Material datasheet, 2015, Rev 10-2015.

[69] D. Reusch and J. Strydom, “Effectively paralleling gallium nitride transistors for high current and high frequency applications,” 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), 2015.

[70] R. Ramachandran and M. Nymand, “Effectively paralleling GaN FETs to achieve ultra-high efficiency in an isolated DC-DC converter,” 2016 IEEE International Conference on Renewable Energy Research and Applications (ICRERA), 2016.

[71] H. Zhou, T. X. Wu, I. Batarseh, and K. D. T. Ngo, “Comparative Investigation on Different Topologies of Integrated Magnetic Structures for Current-doubler Rectifier,” 2007 IEEE Power Electronics Specialists Conference, 2007.

[72] T.-F. Wu, C.-T. Tsai, Y.-M. Chen, Y.-D. Chang, and Y.-D. Chang, “Analysis and Implementation of an Improved Current-Doubler Rectifier With Coupled Inductors,” IEEE Transactions on Power Electronics, vol. 23, no. 6, pp. 2681–2693, 2008.

[73] J. Abu-Qahouq, H. Mao, and I. Batarseh, “New coupled-inductors current-doubler topology,” IEEE 34th Annual Conference on Power Electronics Specialist, 2003. PESC 03.

[74] J. Sun, K. Webb, and V. Mehrotra, “Integrated Magnetics for Current-Doubler Rectifiers,” IEEE Transactions on Power Electronics, vol. 19, no. 3, pp. 582–590, 2004.