Chapter 4

Design Considerations of Low voltage integrated magnetic converters

This chapter presents detailed design guideline for the low voltage IM converters. At first, the design of an IM core is studied with the purpose of minimizing core size, preventing flux saturation, and minimizing ripple current. Optimization of the gate-drive technique for SR is then investigated. Several improvements are made to overcome the existing problems with direct self-driven synchronous rectification, which are discussed in Ch.1.

4.1. Design Considerations of Integrated Magnetic Core

The proposed integrated magnetic structure can be applied to any primary side topology. Since the flux distribution and loss distribution in the proposed IM core are not uniform, precautions should be taken to prevent partial flux saturation and local hot spots within the IM device. The design of an integrated magnetic core includes the designs of core leg cross-sectional areas, air gaps, and window areas.

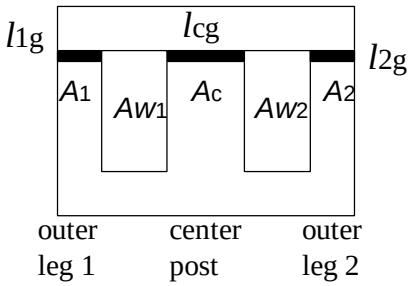


Figure 4-1 Definitions of cross-sectional areas, air gaps, and core window areas. Outer leg 1 hosts winding N_1, outer leg 2 hosts winding N_2 and center post hosts winding N_p

The proposed IM structure has the inherent ripple cancellation technique. As discussed in the previous chapter, there are three factors that can greatly influence the ripple current:

the turns ratio N, the ratio of two outer–leg cross-sectional areas A_1/A_2, and the ratio of two outer-leg gaps l_{1g}/l_{2g}. To simplify the design effort, the following guideline is recommended.

- Choose N to minimize the voltage/current stress on the semiconductor devices. This will result in a duty cycle range: $D_{min}<D<D_{max}$.
- Fix l_{1g}/l_{2g}, and design A_1/A_2 to minimize the ripple current. A_1/A_2 must be designed such that D_{crit} is in the middle of the duty cycle range: $D_{crit}=(D_{min}+ D_{min})/2$. Usually, an even gapping on the two outer legs, especially a spacer gap, may reduce the manufacturing cost, so it is preferred to choose $l_{1g}/l_{2g}=1$.
- Design outer leg gapping to prevent flux saturation in each core leg.

4.1.1. Core cross-sectional areas

In order to prevent a hot spot inside the core, the maximum ac flux density must be limited. According to the analytical results presented in Ch.3, the minimum core cross-sectional area of each core leg must meet the following requirements:

Outer Leg 1:

$$A_1 > A_{1,\min} = \frac{(V_o + V_D)D_{\max}}{2B_m N_s f_s}$$

Eq. 4-1

Outer Leg 2:

$$A_2 > A_{2,\min} = \frac{(V_o + V_D)(1 - D_{\min})}{2B_m N_s f_s}$$

Eq. 4-2

Center post:

$$A_c > A_{c,\min} = \frac{(V_o + V_D)}{2B_m N_s f_s}$$

Eq. 4-3

where V_D is the voltage drop on the rectifiers, and B_m is the maximum allowable ac flux density of the selected magnetic materials for the given switching frequency and core temperature.

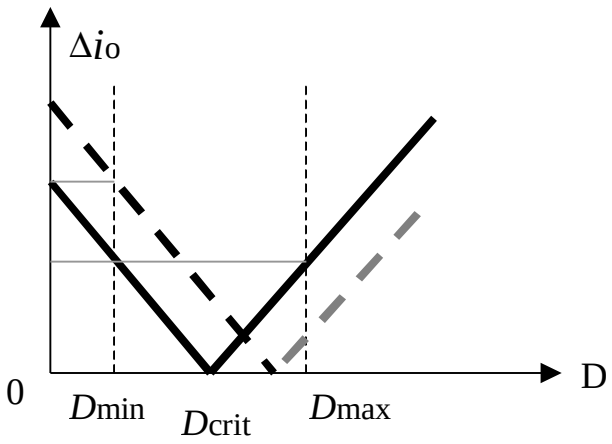


Figure 4-2 Relationship between maximum output ripple current and critical duty cycle point.

To lower the manufacturing cost, it is desirable to design equal gaps on the two outer legs. Spacer gap is always a low cost solution. By choosing $l_{1g}/l_{2g}=1$, the critical duty cycle for zero ripple current is estimated to be

$$D_{crit} = \frac{1}{\frac{l_{1g}}{l_{2g}}\frac{A_2}{A_1}+1} = \frac{1}{\frac{A_2}{A_1}+1}$$

Eq. 4-4

As shown in Figure 4-2, the worst-case ripple current is minimum when the critical duty cycle point is in the middle of the given duty cycle range.

Therefore, the critical duty cycle is chosen to be

$$D_{crit} = \frac{D_{\min} + D_{\max}}{2}$$

Eq. 4-5

By combining Eq. 4-4 and Eq. 4-5, the ratio of the outer-leg cross-sectional areas can be calculated to be

$$\frac{A_2}{A_1} = \frac{2-(D_{\min} + D_{\max})}{D_{\min} + D_{\max}}$$

Eq. 4-6

The final core cross-sectional areas of each core leg must satisfy Eq. 4-1, Eq. 4-2, Eq. 4-3, and Eq. 4-6 simultaneously. In practice, the maximum duty cycle of an HBI^{2}M circuit is

less than 50%, and the duty cycle range of FI^{2}M circuit is usually designed to be centered around 50% or lower, so $D_{\min}+D_{\max}$ is always no greater than 1. It can be seen from Eq. 4-1, Eq. 4-2, Eq. 4-3, and Eq. 4-6 that the optimum core design usually results in a core cross-sectional area in outer leg 2 no smaller than in outer leg 1.

4.1.2. Gapping design

The gapping of the proposed IM core is designed to prevent flux saturation in each portion of the core. Since the dc flux distributions in the IM core for HBI^{2}M and FI^{2}M are different, the gapping designs for these circuits must be addressed separately. In the following discussion, the fringing flux is neglected. As a result, the practically required gapping may be slightly different from the estimated values.

4.1.2.1. Gapping Design in FI^{2}M circuit

The maximum flux density in each core leg is approximated as the sum of the dc flux density and the ac flux density, which can be determined from Eq. 3-19 and Eq. 3-20. If the center post of the core is not gapped and the two outer legs are gapped equally, the minimum gapping needed is estimated to be:

$$l_{og} \cong \frac{m_0 I_o N_s A_2}{\min(j_{2dc,\max}, j_{cdc,\max})},$$

Eq. 4-7

where

$$j_{2dc,\max} \cong B_{sat} A_{2\min} - \frac{(V_o + V_D)(1 - D_{\min})}{2N_s f_s}$$
$$j_{cdc,\max} \cong B_{sat} A_{c\min} - \frac{(V_o + V_D)}{2N_s f_s},$$

Eq. 4-8

Usually, $j_{2dc,\max}$ is higher than $j_{1dc,\max}$.

4.1.2.2. Gapping Design in HBI^{2}M circuit

Similarly, to prevent partial flux saturation in an HB circuit, it is necessary that the maximum flux density in each core leg not exceed the saturation level for the given

magnetic materials. If there is no center post gap and the two outer leg gaps are equal, the minimum gapping required for each core leg are estimated to be:

$$l_{g,\min} \cong \max\left(\begin{array}{c} \dfrac{\left|(A_2+A_1)D-1\right|}{B_{\text{sat}}A_c-\dfrac{V_{\text{o}}T}{2N_{\text{s}}}} \\ \dfrac{1}{\dfrac{B_{\text{sat}}}{D}-\dfrac{V_{\text{o}}T}{2N_{\text{s}}A_1}} \\ \dfrac{1}{\dfrac{B_{\text{sat}}}{1-D}-\dfrac{V_{\text{o}}T}{2N_{\text{s}}A_2}} \end{array}\right)\mu_0 N_s I_o \qquad \textbf{Eq. 4-9}$$

If a spacer is inserted as an even gap for all three core legs, the minimum thickness of the spacer is estimated to be

$$l_{g,\min} \cong \max\left(\begin{array}{c} \dfrac{\left|A_2-D(A_1+A_2)\right|}{\left(B_{\text{sat}}-\dfrac{V_{\text{o}}T}{2N_{\text{s}}A_c}\right)(A_1+A_2+A_c)} \\ \dfrac{A_1+(1-D)A_c}{\left(B_{\text{sat}}-\dfrac{V_{\text{o}}(1-D)T}{2N_{\text{s}}A_2}\right)(A_1+A_2+A_c)} \\ \dfrac{A_2+DA_c}{\left(B_{\text{sat}}-\dfrac{V_{\text{o}}DT}{2N_{\text{s}}A_1}\right)(A_1+A_2+A_c)} \end{array}\right)\mu_0 N_s I_o \qquad \textbf{Eq. 4-10}$$

4.1.3. Core Window Area

The core window area should be large enough to accommodate all the windings. The core window areas are defined as shown in Figure 4-1. In the following discussion, we define:

- K_f: winding filling factor, practically, 20~40%

- J_{max}: maximum allowable current density, A/m^2, practically, 5~20MegA/m^2, or 5-20A/mm^2, depending on the type of windings

4.1.3.1. HBI²M circuit

For the primary winding, the required copper area is estimated to be

$$A_{cu,pri} \cong \frac{N_s I_o \sqrt{D(1-D)}}{J_{\max}}. \qquad \textbf{Eq. 4-11}$$

For the Outer Leg 1 winding, the required copper area is estimated to be

$$A_{cu,\sec 1} \cong \frac{N_s I_o \sqrt{D}}{J_{\max}}. \qquad \textbf{Eq. 4-12}$$

For the Outer Leg 2 winding, the required copper area is estimated to be

$$A_{cu,\sec 2} \cong \frac{N_s I_o \sqrt{1-D}}{J_{\max}} \qquad \textbf{Eq. 4-13}$$

So the required window areas are estimated to be

Window 1:
$$A_{w1} \cong \frac{N_s I_o \left[\max_{D_{\min}<D<D_{\max}} \left(\sqrt{D(1-D)} + \sqrt{D} \right) \right]}{J_{\max}} \qquad \textbf{Eq. 4-14}$$

Window 2:
$$A_{w2} \cong \frac{N_s I_o \left[\max_{D_{\min}<D<D_{\max}} \left(\sqrt{D(1-D)} + \sqrt{1-D} \right) \right]}{J_{\max}} \qquad \textbf{Eq. 4-15}$$

where D_{max}, and D_{min} are the maximum and minimum operation duty cycle, respectively.

4.1.3.2. FI²M circuit

For the primary winding, the required copper area is estimated to be

$$A_{cu,pri} \cong \frac{N_s I_o \sqrt{D}}{J_{\max}}. \qquad \textbf{Eq. 4-16}$$

For the Outer Leg 1 winding, the required copper area is estimated to be

$$A_{cu,\sec 1} \cong \frac{N_s I_o \sqrt{D}}{J_{\max}}. \qquad \textbf{Eq. 4-17}$$

For the Outer Leg 2 winding, the required copper area is estimated to be

$$A_{cu,\sec 2} \cong \frac{N_s I_o \sqrt{1-D}}{J_{\max}} \qquad \textbf{Eq. 4-18}$$

So the required window areas are estimated to be

Window 1:
$$A_{w1} \cong \frac{2N_s I_o \sqrt{D_{\max}}}{K_f J_{\max}} \qquad \textbf{Eq. 4-19}$$

Window 2:
$$A_{w2} \cong \frac{N_s I_o \left[\max_{D_{\min} < D < D_{\max}} \left(\sqrt{D} + \sqrt{1-D} \right) \right]}{K_f J_{\max}} \qquad \textbf{Eq. 4-20}$$

where $D_{\max}$, and $D_{\min}$ are the maximum and minimum operation duty cycle respectively.

If a symmetrical core structure is adopted, the window area is designed to be the larger of A_{w1} and A_{w2}.

4.2. Improving the Gate-Driving Design for Synchronous Rectifiers

Synchronous rectification technique is a "must" technique for low voltage, high current output applications. Usually, low $R_{ds,on}$ MOSFETs are used to implement synchronous rectifiers (SR). Since this kind of MOSFET has excessively large gate capacitance, the driving loss can be quite large at high switching frequencies. Thus, an optimum gate drive design is instrumental in achieving high performance. There are two popular driving schemes, as shown in Figure 4-3: the external drive scheme and the direct self-drive scheme.

If the external driving scheme shown in Figure 4-3(a) is adopted, high power loss associated with the gate drive at high switching frequency may offset the conduction loss saved by employing synchronous rectifiers. The gate timing must maximize the conduction time of the MOSFET portion in SR and avoid the cross-conduction of two rectifiers. The timing control can be tricky at high switching frequencies. Consequently, the practical switching frequency is limited to 30~50KHz for high current applications. The size of the

overall converter is large. Thus, the external driving technique is not suitable for high-density applications.

The direct self-driving scheme, as shown in Figure 4-3(b), utilizes the transformer secondary-side waveform to drive the synchronous rectifying MOSFETs. It is simple. Coupled with the soft-switching of the primary side switches, the gate driving loss can be minimized. If the transformer secondary voltage waveform is a square-wave with equal positive and negative magnitudes, the conduction loss on the rectifiers can be minimized.

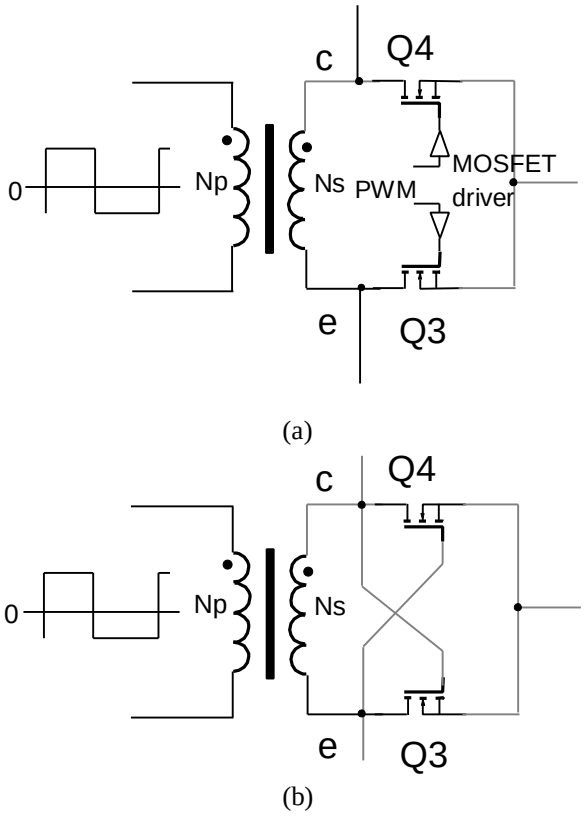


Figure 4-3 Gate drive schemes for SR (a) external driving, (b) self-driving

However, there are several limitations in this driving scheme as discussed in Ch. 1.

i. It is only suitable for circuit topologies whose secondary voltage has only two states: positive and negative. For circuits whose transformer winding sees zero voltage during

the certain interval of the switching period, e.g., two-switch forward, this technique is not suitable.

ii. It is unsuitable for very low output voltage.

iii. There is no over-voltage protection on the SR's gate.

iv. Modules with directly self-driven SRs cannot be paralleled.

Therefore, application of the direct self-drive schemes is very limited. Improvements have to be made on this gate drive scheme.

4.2.1. Issue 1: Extend Self-Driven SR to Circuits Whose Transformer Secondary Voltage Has Zero State

For circuits whose transformer secondary voltage has a zero state, the direct self-drive scheme is not suitable. For example, in a two-switch forward converter, after the transformer core is fully reset, the voltage on the transformer secondary winding drops to zero and Q4 loses the gate drive. The body diode of Q4 has to pick up the load current, increasing the conduction loss and the reverse recovery loss in the body diode of Q4.

At very low duty cycle or high input voltage, this increased loss may become unacceptable. To overcome the problem, a hybrid gate drive scheme is proposed, as shown in Figure 4-4. It still uses the transformer secondary voltage waveform to charge the gate capacitance of Q4 (through Dg1) directly. Since Dg1 will maintain the gate voltage of Q4 after the transformer is fully reset and its secondary voltage drops to zero, the MOSFET portion of the synchronous rectifier Q4 will continue its conduction of the load current when V_s=0. The discharging is completed by Qa and a small resonant inductor L_d. The gate-on signal of Qa leads the turn-on signals of the primary MOSFETs by t_d, as indicated in the waveform shown in Figure 4-4.

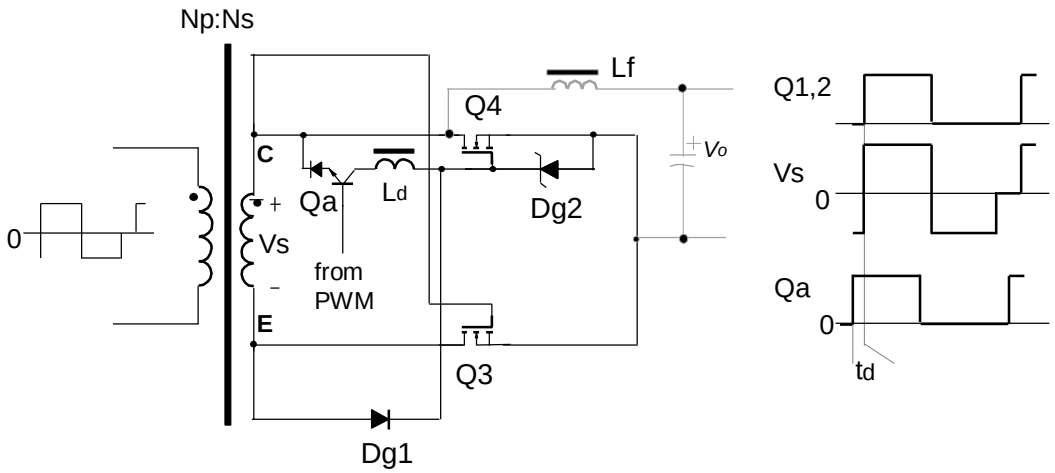


Figure 4-4 Scheme 1: Hybrid gate-drive scheme for SR in circuits whose transformer secondary voltage has a zero state

There are two steps in the discharging procedure.

Step 1: discharging C_g, as shown in Figure 4-5(a)

Qa is turned on. Because V_s is still zero, L_d resonates with C_g to bring down the voltage across the gate of Q4. After the C_g is completely discharged, Dg2 starts to conduct. Then the primary-side switch can be turned on without causing cross-conduction between Q3 and Q4. The minimum lead time between the rising edges of Qa and V_s is determined by

$$t_d = \frac{p}{2}\sqrt{L_d C_g} \qquad \textbf{Eq. 4-21}$$

where C_g is the gate capacitance of Q4. At the end of this stage, the energy initially stored in C_g is transferred to L_d.

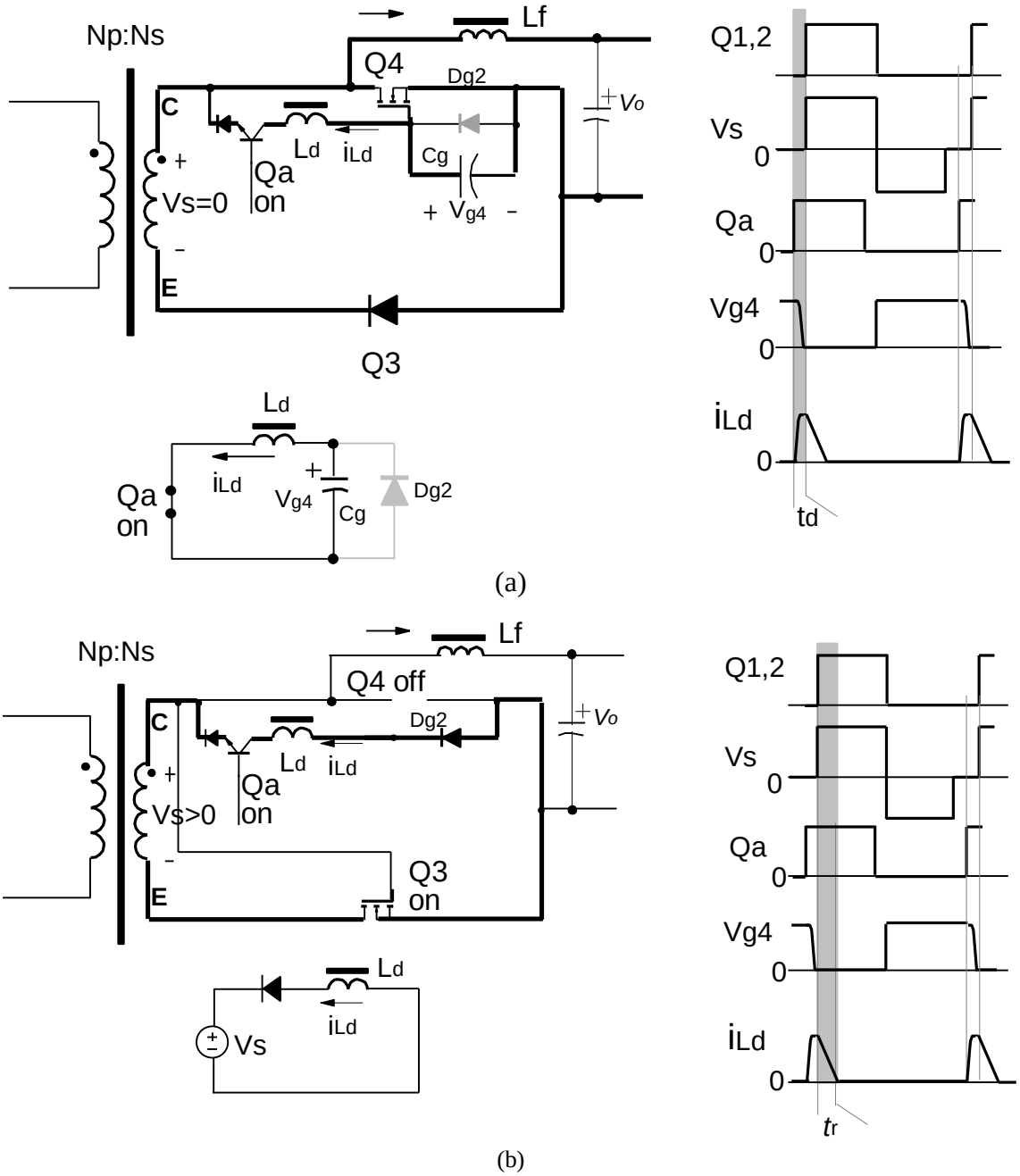


Figure 4-5 Discharging procedure of C_g: (a) Step 1, discharge of C_g, (b) Step 2: reset L_d

Step 2: Reset of L_d, as shown in Figure 4-5(b)

As V_s rises from zero to V_{sp} (due to the turn-on of the primary side switches), the current in L_d decreases linearly at a rate of V_{sp}/L_d. After the current in L_d decreases to zero, the diode in series with Qa prevents the reverse current in L_d. Qa can be turned off afterwards. The minimum reset time of L_d is estimated as

$$t_r = \sqrt{L_d C_g}\,\frac{V_{sn}}{V_{sp}}, \qquad \textbf{Eq. 4-22}$$

where V_{sn} and V_{sp} are the negative and positive peaks of V_s, respectively.

As shown in Figure 4-6, the generation of the gate voltage of Q4 is relatively easy. Qa receives the gate signal directly from the PWM chip. And the PWM signal is delayed by t_d before it is fed into the gates of the primary side switches.

A two-switch forward converter was constructed to verify the proposed technique. The input voltage is 48V, the output voltage is 1.2-1.65V. Each of the SRs employs three SUP75N03-04s in parallel. L_d was made from an MPP55025-A2 with 2 turns of AWG#26 wire. The inductance was measured to be about 0.4uH.

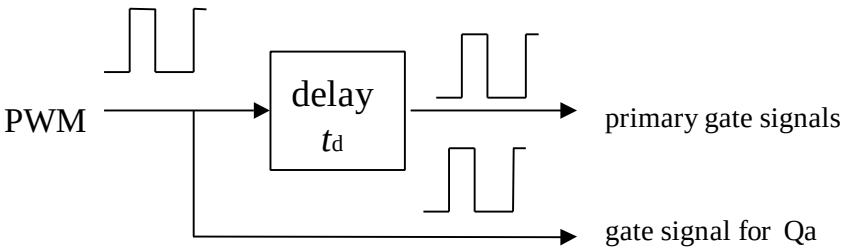
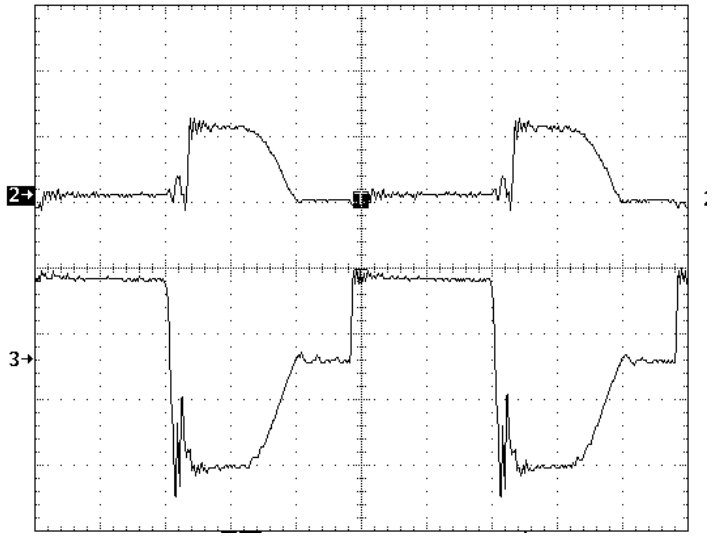
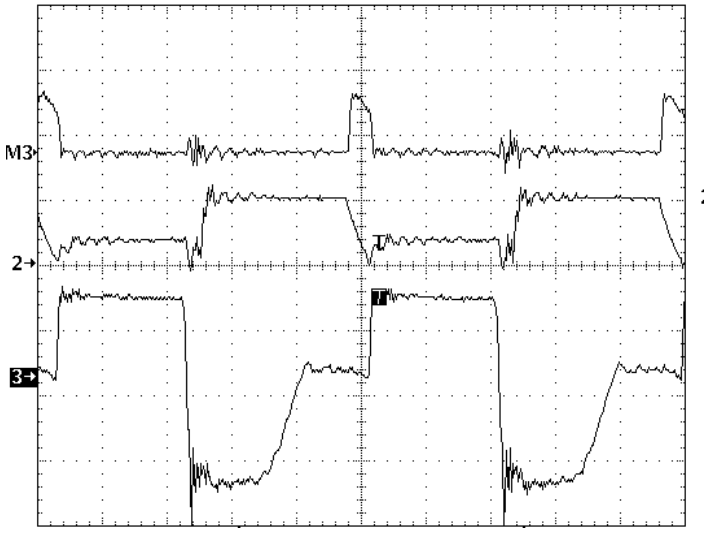


Figure 4-6 Generation of gate signals for Qa



(a)Direct self-driven waveform: top-$V_{gs,Q4}$ (5V/div), bottom-V_{pri} (40V/div);



(b) Improved hybrid drive: top-I_{Ld} (0.5A/div), middle-$V_{gs,Q4}$ (5V/div), bottom-V_{pri} (40V/div).

Figure 4-7 Experimental waveforms (example circuit: 2-switch forward, V_{in}=48V, V_o=1.2V, I_o=60A)

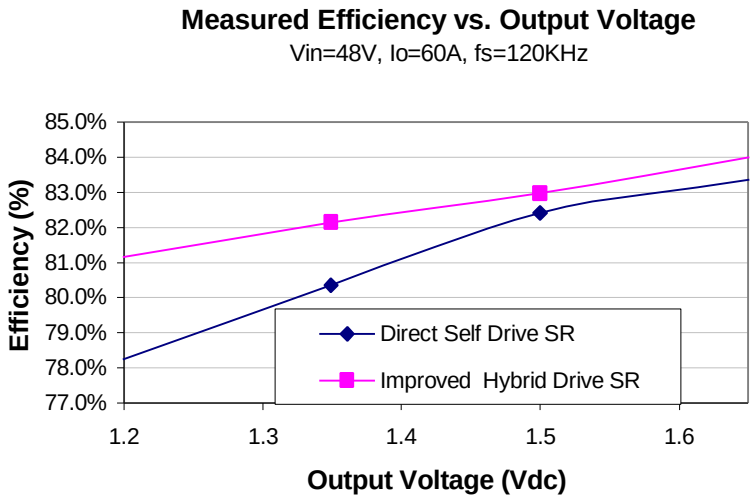


Figure 4-8 Measured efficiency comparisons

The experimental waveforms described in Figure 4-7 show that the proposed scheme is able to provide a good gate-driving waveform on the freewheeling SR (Q4) after the transformer reset is complete. At a lower duty cycle, the proposed technique provides much better efficiency than the direct self-drive synchronous rectification technique. This can be verified from the measured efficiency shown in Figure 4-8. Because this scheme uses control circuit timing to discharge the gate capacitance of the freewheeling SR and also uses the direct self-drive concept, it is called the hybrid gate-drive synchronous rectification technique, and is referred to as Scheme 1 in the later discussion.

4.2.2. Issue 2: Provide Over Voltage Protection and Module Direct-Parallel Capability

To protect the gates from over-voltage, it is natural for one to use a Zener diode in parallel with the gate-to-source of MOSFETs. It is necessary to insert an impedance between the Zener diode and the driving point of the transformer secondary winding. Otherwise, a high surge current might damage the Zener diode. If the impedance is a resistor, the charging and discharging current of the gate capacitance generates power loss on the resistor. Also, because the gate capacitance is usually large, even a small value of

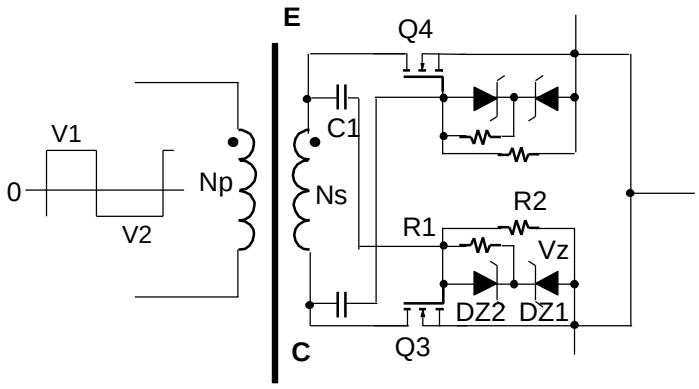


Figure 4-9 Scheme 2: improved self-drive scheme for SR with the capabilities of the gate over-voltage protection and the direct module-parallel operation

the resistor can cause a significant delay at turn-off of the synchronous rectifier, resulting in cross-conduction of SR during the switching transient.

Therefore, a capacitor (C_1) is employed together with Zener diodes (DZ1 and DZ2) to protect the gates of the MOSFET from suffering over-voltage, as shown in Figure 4-9. A resistor can be paralleled with C_1 to maintain the charge balance on C_1. But this allows the output voltage to be dc-coupled into the gates of the MOSFETs. So the charge-balance resistor is placed across DZ2 instead, as shown in Figure 4-9. R2 is placed across the gate and source of the MOSFET to ensure that no dc voltage will build up on the gates of the MOSFETs when the circuit does not work. Consequently, the proposed self-drive scheme is able to achieve over-voltage protection on the SR's gates, and the capability of the direct module-parallel operation.

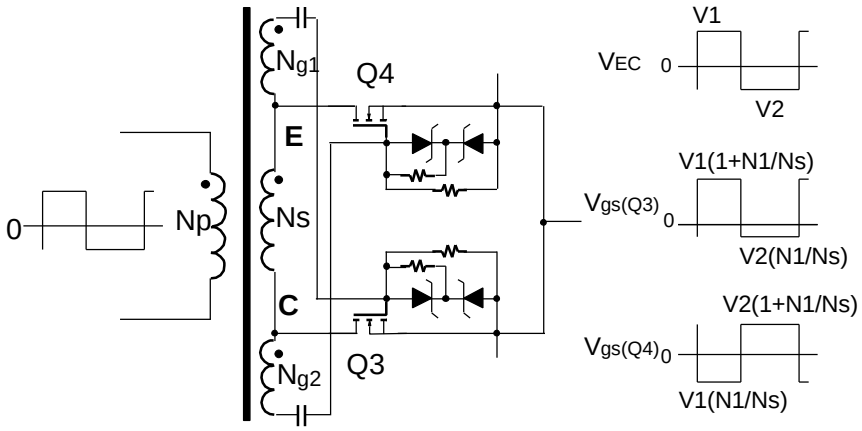
Because the proposed self-drive scheme clamps the voltage peak of the gate drive voltage, this scheme can also be applied to the circuit with a non-square-wave transformer voltage, for example, resonant reset forward converter. The scheme is shown in Figure 4-9 and will be referred to as Scheme 2.

4.2.3. Issue 3: Gate Driving Technique of SR for Very Low Output Voltage

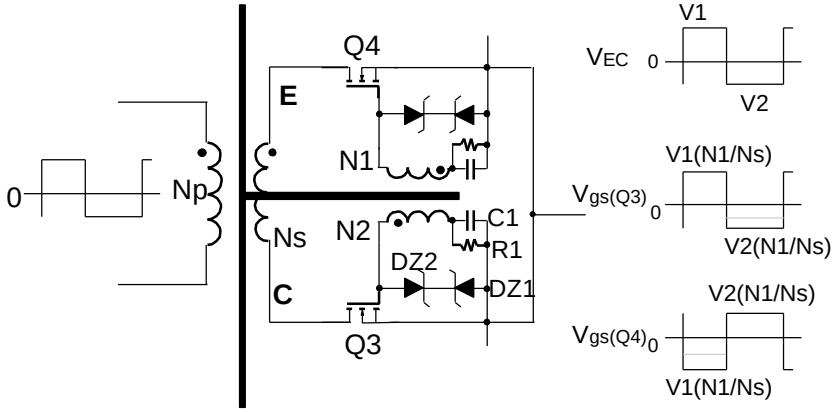
At 50% duty cycle, the amplitude of the transformer secondary voltage is about twice of the output voltage. For a logic gate MOSFET, the proper gate drive voltage is between 6-12V; for a regular gate MOSFET, the proper gate drive voltage is between 10-16V. Thus, if the output voltage is lower than 3V, for example, 1.8V, the conventional direct self-drive scheme shown in Figure 4-3(b) and the previous schemes cannot be used.

To boost the gate-driving voltage for SRs, separate gate-drive windings are added, as shown in Figure 4-10. N1 and N2 are chosen to obtain a proper gate-drive voltage. Note that in this section, N1 and N2 are the gate-driving windings instead of the outer-leg windings specified in the proposed IM structure. As shown in Figure 4-10, there are two schemes to accomplish this. Scheme 3A, as shown in Figure 4-10(a), utilizes power winding. Consequently, for the same amplitude of the positive gate voltage, the amplitude of the negative gate voltage in Scheme 3A is smaller than that in Scheme 3B. The power loss associated with the gate driving in Scheme 3A may be lower. Besides, Scheme 3A needs fewer turns of N1 and N2 for the same amplitude of the gate turn-on voltage. So, most of time Scheme 3A is preferred.

Combining Schemes 1-3, an improved hybrid gate drive scheme is developed as shown Figure 4-11. This scheme is also suitable for the resonant reset converter.



(a)



(b)

Figure 4-10 Scheme 3: improved gate drive schemes for low output voltage: (a) Scheme 3A, (b) Scheme 3B

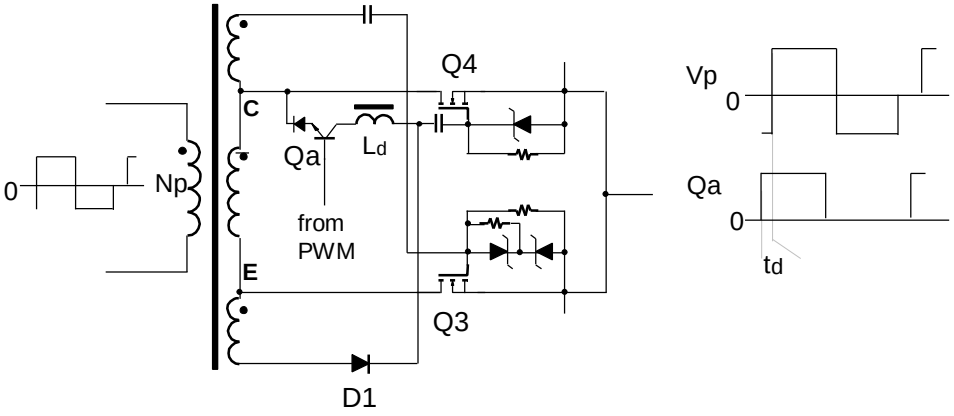


Figure 4-11 Improved hybrid gate-drive schemes for SRs in low voltage output circuits whose secondary voltage has zero state

4.2.4. Improved Self-Drive Synchronous Rectification Technique for High Output Voltage

For high-output applications, Scheme 4 (shown in Figure 4-12) or Scheme 3B can be adopted. Scheme 4 employs the tap points of the transformer secondary winding. It needs fewer windings than Scheme 3B. The amplitude of the negative gate voltage of Scheme 4 is smaller than that of Scheme 3B. But for very high output voltage, Scheme 3B is preferred.

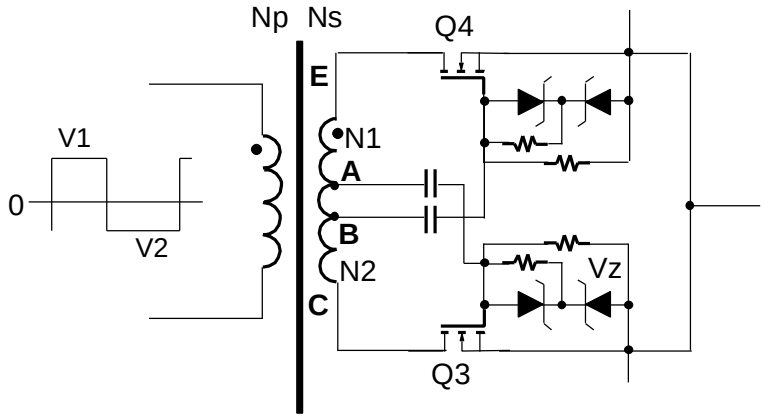


Figure 4-12 Scheme 4: Gate driving scheme of SRs for high output voltage using CZS technique