A VHF/UHF Voltage Controlled Oscillator in 0.5μm BiCMOS

by

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ABSTRACT

The dramatic increase in market demand for wireless products has inspired a trend for new designs. These designs are smaller, less expensive, and consume less power. A natural result of this trend has been the push for components that are more highly integrated and take up less real estate on the printed circuit board (PCB). Major efforts are underway to reduce the number of integrated circuits (ICs) in newer designs by incorporating several functions into a single chip. Availability of newer technologies such as silicon bipolar with complementary metal oxide semiconductor (BiCMOS) has helped facilitate this move toward more complex circuit topologies onto one die. BiCMOS achieves efficient chip area utilization by combining bipolar transistors, suited for higher frequency analog circuits with CMOS transistors that are useful for digital functions and lower frequency analog circuits. A voltage controlled oscillator (VCO) is just one radio frequency (RF) circuit block that can benefit from a more complex semiconductor process like BiCMOS.

This thesis presents the design and evaluation of an integrated VCO in the IBM 5S BiCMOS process. IBM 5S is a 0.5 μm, single poly, five-metal process with surface

channel PFETs and NFETs. The process also features self-aligned extrinsic base NPN bipolar devices exhibiting ft of up to 24 GHz.

The objective of this work is to obtain a VCO design that provides a high degree of functionality while maximizing performance over environmental conditions. It is shown that an external feedback and resonator network as well as a bandgap voltage referenced bias circuit help to achieve these goals. An additional objective for this work is to highlight several pragmatic issues associated with designing an integrated VCO capable of high volume production.

The Clapp variant of the Colpitts topology is selected for this application for reasons of robust operation, frequency stability, and ease of implementing in integrated form. Design is performed at 560 MHz using the negative resistance concept. Simulation results from Pspice and the Agilent ADS are presented. Implementation related issues such as bondwire inductances and layout details are covered. The VCO characterization is shown over several environmental conditions. The final nominal design is capable of: tuning over 150 MHz (22%) and delivering –4.2 dBm into a 50 Ohm load while consuming only 9mA from a 3.0V supply. The phase noise at these conditions is -92.5 dBc/Hz at a frequency offset of 10 kHz from the carrier. Finally, the conclusion of this work lists some suggestions for potential future research.

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Finally, I would like to thank my family, especially my wife Jennifer and children Joey and Elizabeth. Without their love, patience, and understanding this work would not have been possible. I also owe my parents Joseph Robert and Gloria Ann Bosley a large debt of gratitude for introducing me to their alma mater and helping me through my academic years. Their support allowed me to attend Virginia Tech. I feel fortunate to be able to add my name to a family legacy of VPI graduates dating back to the 1930s.

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1 Introduction

1.1 Motivation

Over the past few decades the demand for wireless devices of all kinds has enabled a burgeoning market for integrated circuits (ICs). Lowered cost, decreased circuit board size, reduced power consumption, and quicker time-to-market are design improvements that ICs have played a crucial role in achieving. As clock speeds in digital circuits and carrier frequencies in radio circuits continue upward, the advantages of high frequency packaging and semiconductor technology continue to find new applications.

One fundamental radio system block that has been benefited from implementation as an IC is the voltage controlled oscillator (VCO). Almost all wireless devices require at least one oscillator in order to do the necessary frequency conversion from baseband to some higher frequency or vice versa. VCOs are typically employed with phase locked loops to perform this function. Although there has been some effort to integrate the PLL and VCO onto the same chip, many designs still incorporate a stand-alone oscillator that has been optimized for performance within a particular system.

In classic radio designs the local oscillator (LO) has been implemented with a discrete active device. Passive components are used for the necessary bias, feedback, and resonator

networks. More recently, the trend has been to integrate of all these oscillator components onto a single semiconductor die. The aim of this work is to present the design and evaluation of a VCO which benefits from this integration. The IC presented attempts to maximize performance while maintaining a high level of utility. This is accomplished by using a BiCMOS process that provides both low-noise/high- frequency bipolar transistors for RF functions and CMOS components for lower frequency or logic functions.

Some observations about monolithic VCOs should be made here. First, there is a somewhat limited range of useful frequencies over which the proposed circuit may be successful. Frequencies between a few megahertz and a few gigahertz work best in IC form. At lower frequencies, the passive component sizes become too large to feasibly put onto the same chip with active devices. As the frequency increases past several gigahertz the substrate losses and package parasitics become too problematic for traditional oscillator design and more sophisticated microwave techniques are required.

The next observation concerns the performance of oscillators. There are several VCO specifications that are essential to the performance of wireless systems. As more RF devices are introduced, the allocated frequency bands become crowded. This finite bandwidth constraint requires higher order digital modulation schemes to efficiently use the available spectrum. Several new digital modulation techniques rely on dense constellations of phase shift keying (PSK) which place more stringent requirements on the phase noise of the VCO. To ensure reliable radio system performance, design engineers must consider several factors when attempting to meet these requirements. One of the most important factors controlling

phase noise is the loaded Q of the resonator. The treatment in Chapter 2 reveals that increasing the Q of the resonator is a simple and effective method for reducing phase noise in an oscillator. Other parameters associated with oscillator characterization include: supply pushing, load pulling, output level, harmonic content, and tuning sensitivity. These topics will also be covered in detail in Chapter 2.

1.2 Comparison of similar designs

Several companies are currently manufacturing oscillators in a variety of arrangements. The traditional discrete transistor and resonator design has been consolidated by industry into a monolithic module. This is essentially a standard VCO arrangement that has been designed using surface mount components on a small circuit board substrate. A module format offers the potential for superior performance over alternatives because of the flexibility to select components. Low loss dielectric substrates, high Q resonators, and low noise transistors yield the best performance in a packaged VCO. The disadvantage of a module is that the highest quality components result in catalog prices that are too high for most of the low cost radio components in production.

The extreme opposite of module design philosophy is the fully integrated semiconductor circuit. The ideal realization of this design would be a monolithic chip requiring interfaces to only a power source, tuning voltage, and oscillator output. This form offers some advantages and disadvantages over the module. The most obvious advantage is that all of the active components can be integrated into one monolithic semiconductor chip requiring an

absolute minimum of space on the radio circuit board. Several academic papers have been written on the subject of full integration of a VCO [1,2,3]. Many of these papers concentrate on attempting to optimize the phase noise of the VCO while maintaining all active and passive components on the IC. The results vary significantly depending on the particular semiconductor technology and circuit implementation used. Significant research effort has been put into improving the quality factor (Q) of inductors due to their inherently lossy nature. Most of the research has been done on oscillators operating at frequencies above 1 GHz. The physical size of spiral inductors would grow to unrealizable dimensions for frequencies in the hundreds of megahertz required of the design presented here. Additionally, the Q of an on-chip inductor decreases with decreasing frequency. This makes an on-chip inductor an unattractive solution for VHF band operation.

Despite the difficulty in integrating all the components onto a single semiconductor die there have been several manufacturers who have accomplished this. One example is the Maxim MAX2622. This IC combines an active oscillator circuit complete with LC tank and an output buffer amplifier. The MAX2622 performs well for an IC of this kind. However, the restricted tuning range and degraded phase noise performance are inherent limitations. Other chips, such as the Phillips NE602, use an oscillator that is integrated as part of another function. These circuits tend to be more difficult to implement when used in a synthesizer due to the lack of adequate output buffering.

The middle ground between a module and a fully integrated VCO is found in a class of ICs that have integrated active devices but require off chip resonators and tuning components. Some examples are the Motorola MC12148 (1648) and the Maxim MAX2620. These are the closest to the proposed VCO in terms of circuit topology. In comparison to the previously described solutions, these offer the best compromise between dense integration and high performance. Much greater flexibility in the frequency of operation and tuning range is also possible as a result of allowing for external resonator circuitry. Both ICs achieve low current and low phase noise resulting from high quality inductors and varactors implemented external to the chip. The one drawback to these chips is that they are susceptible to supply pushing and de-tuning from load variation. The VCO presented in this work exhibits 190 kHzpp frequency deviation when loaded with a 1.75:1 VSWR . Under similar operating conditions, the MAX2620 changes 340 kHzpp. An integrated buffer amp may be designed which minimizes the effect of perturbations in the battery voltage or load impedance.

It has been shown that there are several highly integrated VCO topologies currently available. Furthermore, the strengths and weaknesses of existing IC solutions have been reviewed. This thesis presents a VCO design that combines the advantages of a monolithic oscillator with the improved performance afforded by high Q resonator components.

1.3 Description of methodology

This thesis follows a basic method for the VCO design. Chapter 2 presents a review of basic oscillator theory. A summary of some classic circuit topologies and resonator components are presented. Chapter 2 ends with a synopsis of several standard performance related specifications. Chapter 3 deals with the negative resistance analysis as it is applied to the Clapp structure used in this thesis. Additionally, the buffer topology, biasing circuitry and various package considerations are covered in Sections 3.1- 3.4. Other issues associated with physical layout in a BiCMOS process are given treatment in Section 3.5. This is followed by the simulation setup and results in Chapter 4. Experimental results are presented and compared to simulation in Chapter 5. Conclusions are drawn from the experimental results in Chapter 6. Finally, Chapter 7 suggests some potential directions for further oscillator performance enhancement based on this work.

2 Oscillator Theory

2.1 Overview of Oscillator Theory

In this chapter, several fundamental topics will be covered. Section 2.1 is a review of basic oscillator theory as presented in most of the literature. The objective of this section is to outline the critical points of starting, maintaining, and controlling the frequency of a VCO. This section also concentrates on the issue of non-linearity associated with large-signal operation of bipolar transistors. Section 2.2 presents and compares several standard inductor-capacitor (LC) oscillator topologies. This section also covers the critical aspects of inductors and varactors in LC-tuned VCO design. Finally, Section 2.3 summarizes several common VCO performance specifications. Each specification is reviewed in terms of radio system performance.

2.1.1 Background

The idealized oscillator model, depicted in Figure 2.1, is described in control theory consisting of an amplifier and a feedback network [4].

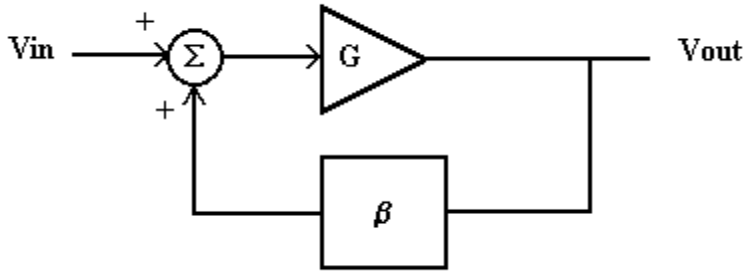


Figure 2.1: Oscillator Block Diagram

The equations for this system are derived from control theory as:

$$Vout = \frac{Vin \cdot G}{1 - G \cdot \beta} \tag{2.1}$$

Where Vin is the input voltage, Vout is the output voltage, G is the gain of the amplifier, and β is the transfer function of the feedback network.

The system in Figure 2.1 is normally analyzed in terms of providing an amplifier stabilized with negative feedback. However, this model provides positive feedback in order to establish an unstable state. The condition for instability, defined by Equation 2.2, is satisfied when the open-loop gain of the system is unity with a phase shift of 0 or 360°.

$$G \cdot \beta = 1 \tag{2.2}$$

When this condition is satisfied, the energy in the feedback path is the same magnitude and phase as the input. The summing node adds the original signal with the signal traversing the feedback loop. Unity gain and a 360° phase change around the feedback path lead to a zero in the closed-loop equation. The result is sustained oscillation and is described as the Nyquist or Barkhausen criterion. It should be noted that the Barkhausen criterion is a necessary but not sufficient[1] to ensure that a particular circuit is unstable and will oscillate [5].

The preceding theory is based on a feedback or transmission type framework and is useful for gaining insight into oscillator operation from a controls theory viewpoint. Another method called the negative resistance analysis method is widely used for microwave and high frequency design. This technique is useful for high frequency oscillator design where the circuit in question can easily be decomposed into a negative resistance and a resonator. Negative resistance theory is used in Chapter 3 to analyze stability conditions.

[1] Nguyen and Meyer show an example which shows an LC oscillator which satisfies Barkhausen but fails to oscillate.

A few caveats concerning basic theory should be raised at this point. First, the feedback network is not perfectly reactive, therefore a small margin of excess loop gain is required in order to counteract the resonator losses and begin oscillation buildup. However, this excess gain should not be made arbitrarily large just to ensure startup conditions are met. One possible consequence of very large loop gain is an undesirable level of harmonic energy. Another possible consequence of excess loop gain is a phenomenon called "squegging". This is a condition where the oscillator signal envelope is amplitude modulated by a low frequency bias fluctuation [6].

Another point to be raised is that practical oscillators require an initial input. Low-level thermal noise sources or turn-on transients are usually large enough to act as a starting input. These input signals are initially applied into the positive feedback system as low-level signals. The time interval just before steady state oscillation but after power has been applied is referred to as startup. A small-signal assumption can be made in determining the conditions necessary to guarantee sustained oscillation during startup. This assumption is based on the fact that the system is still acting as a linear amplifier for a short time until the signal level becomes large enough to cause the active device to enter the non-linear region of operation. It should be emphasized that this is the first part of a two-part analysis. The second part (limiting) consists of determining the steady state level of oscillation. This inherently presumes a large signal model. In practice, the active device used in the amplifier stage becomes non-linear as the level of oscillation increases. It is this non-linear nature that provides the limiting mechanisms in a transistor oscillator. These issues are given a more complete treatment in the next sections.

2.1.2 Amplitude Limiting and Startup

The previous section described positive feedback as a necessary mechanism for starting oscillation. In order for an oscillator to start it must have adequate gain and phase shift around the loop. When a supply voltage is initially applied to the VCO the bias transients and thermal noise sources excite the natural frequency of the resonator. The resulting signal is then amplified and fed back through the resonator to the input of the amplifier and the cycle repeats until this reaches steady state. The time required to reach steady state, referred to as startup time, is a function of excess gain and the time delay in the feedback path. Time delay is primarily determined by the loaded resonator Q and is described in by the following relation [7].

$$t_d = \frac{Q_l}{\pi \cdot f} \tag{2.3}$$

Where t_d is the time delay in seconds, f is the frequency in Hz, and Q_l is the loaded Q which is unitless.

Assuming that no control system (such as an automatic gain control circuit) is used to adjust the amplifier gain, the steady state signal amplitude is determined by the non-linearity in the active circuit.

In the case of a bipolar junction transistor VCO, the signal builds up to a level that begins to be impacted by an exponential characteristic. The level at which this occurs is termed the thermal voltage[2] and is defined in Equation 2.4.

$$V_t = \frac{k \cdot T}{q} \approx 26mV(silicon) \tag{2.4}$$

Where, T is the temperature in degrees Kelvin, q is the charge on an electron [1.602E-19 C], and k = Boltzmann's constant [1.602E-23 J/K]

A possible VCO implementation could be realized if a common emitter amplifier biased for constant DC collector current replaced the amplifier block of Figure 2.1. Analysis begins with the input voltage V_{in} defined as a sinusoid with a DC offset:

$$V_{in} = V_0 + V_1 \cdot \cos(\omega \cdot t) \tag{2.5}$$

Where, V_o is a dc bias voltage term, V_1 is the amplitude of the base-emitter voltage at the fundamental, and ω is the fundamental frequency of oscillation.

Once the oscillator starts, the magnitude of V_1 will begin to increase. Since the current in a bipolar transistor is an exponential function of the base-emitter voltage the resultant collector current (Equation. 2.6).

[2] Below this level of input voltage the device appears linear.

$$icc(t) = Is \cdot e^{V_0/V_t} \cdot e^{V_1 \cdot \cos(\omega \cdot t)/V_t} \tag{2.6}$$

Where $icc(t)$ is the time varying collector current and Is is the saturation current in a bipolar transistor.

As the value of V_1 approaches and eventually exceeds V_t, the harmonic content in the collector current increases[1] at the expense of the large signal transconductance (G_m) at the fundamental frequency. This effect causes the gain at the fundamental frequency to decrease until it exactly cancels the losses in the resonator and feedback circuits.

Figure 2.2 shows G_m as a function of x; where x is the peak fundamental voltage (V_1) normalized to the thermal voltage (V_t). The y-axis has been normalized to the small signal *gm* to show the magnitude to which the large and small signal transconductances diverge as a function of drive level. The Figure indicates that the normalized $G_m(x)$ decreases dramatically for peak input voltages where $x > 1$.

[1] Clarke and Hess give an exhaustive analysis of this phenomenon [6]

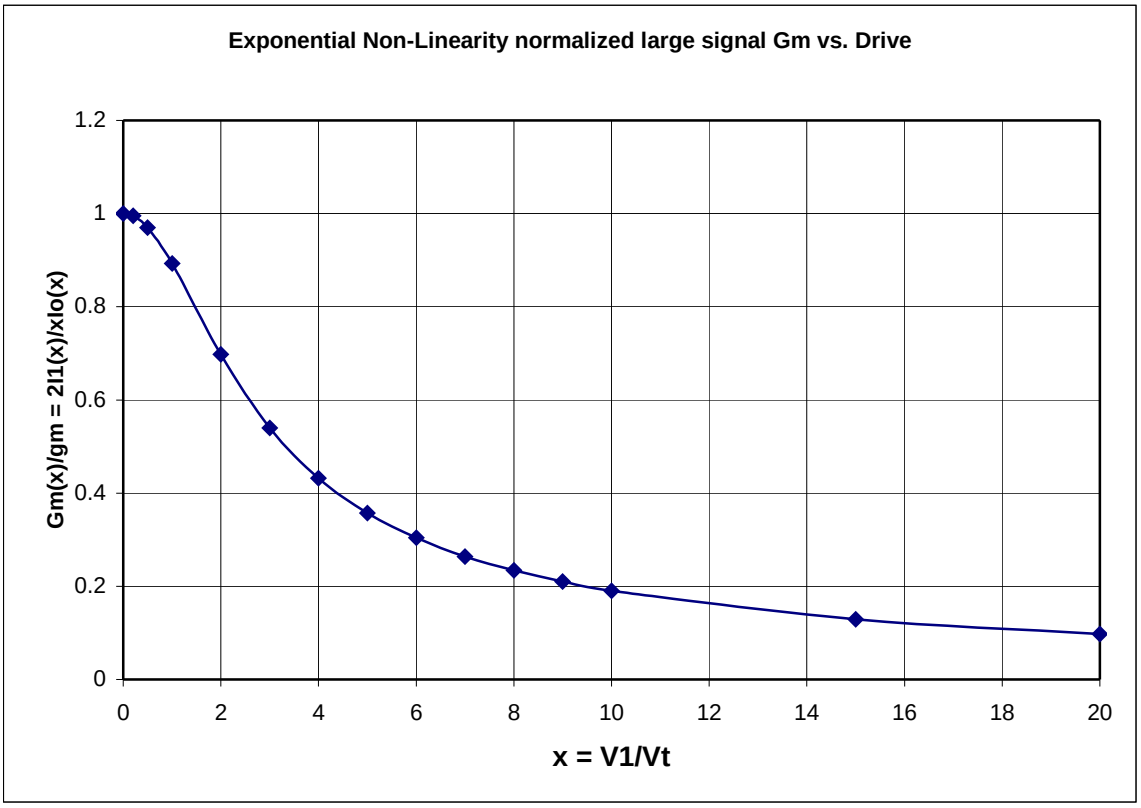


Figure 2.2: Normalized transconductance versus normalized voltage drive

The quantities in Figure 2.2 are defined as follows: G_m is the large signal transconductance and is equivalent to $I_1(x)/V_1$, where $I_1(x)$ is the magnitude of the fundamental component of collector current, V_1 is the same quantity as in Equation 2.5, $I_o(x)$ is the DC component of collector current, and *gm* is the small signal transconductance defined as I_{dc}/V_t *(I_{dc} is the quiescent collector current at x = 0)* [6,8].

The unfortunate by-product of this type of limiting is the increased harmonic content that appears in the oscillator output spectrum. In addition, the large signal swing drives the transistor into an operating region which causes non-linear mixing of noise to appear in the

output spectrum. Thus, phase noise is an inevitable result of the self-limited VCO. The topics of harmonic content and phase noise will be dealt with later in this section.

2.2 Oscillator Circuitry

This section covers some of the fundamental oscillator circuit topologies. The primary focus is on varactor tuned inductor-capacitor network. These circuits are a good match to the requirements of a VCO that requires a wide tune range and short time to begin and sustain oscillation while maintaining a high degree of performance. This section also covers the topics of the frequency determining elements - resonators and varactor diodes.

2.2.1 Classical Single transistor LC Architectures

Single transistor architectures are well covered in literature on oscillator design [6, 7, 8, 9,10]. The simplicity of a single active device lends itself to an easy analysis of VCO theory and design. Additionally, several options in circuit topology exist for oscillators of this type. A few of the more common inductor-capacitor (LC) topologies are shown in Figure 2.3

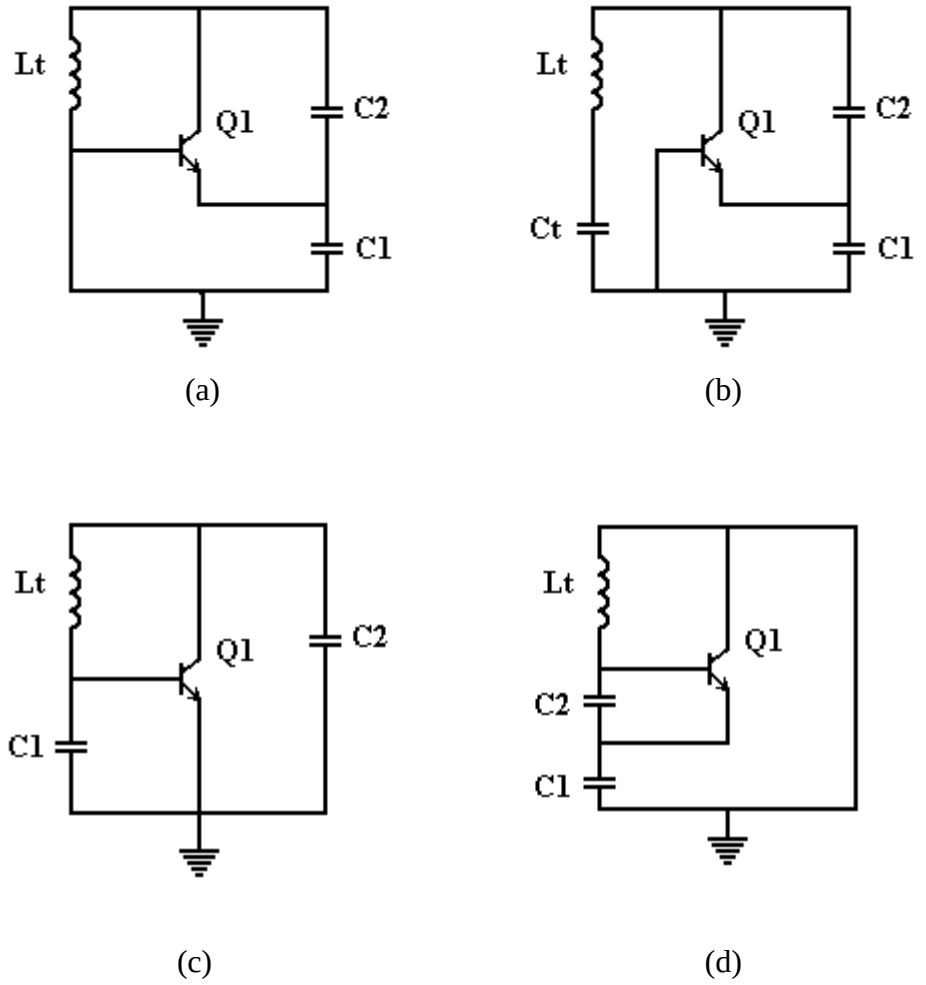


Figure 2.3: Classic single transistor LC oscillator topologies: (a) Colpitts, (b) Clapp, (c) Pierce, and (d) Modified Colpitts

Although each of the topologies in Figure 2.3 is distinct, it has been argued that they are inherent the same basic circuit with ground node shifted [7]. This is particularly obvious when comparing the Colpitts with the Pierce and modified Colpitts. These are the same circuit in an AC sense with the ground placed at the base, emitter, and collector respectively. The Clapp is essentially a Colpitts oscillator with the addition of capacitive reactance in the inductance path [11]. A Clapp type topology (Figure 2.4) was selected for this project but

differs slightly from the original (Figure 2.3 b) in that the effective ground is placed at the collector rather than the emitter. This network was selected for reasons of frequency stability and ease of implementation.

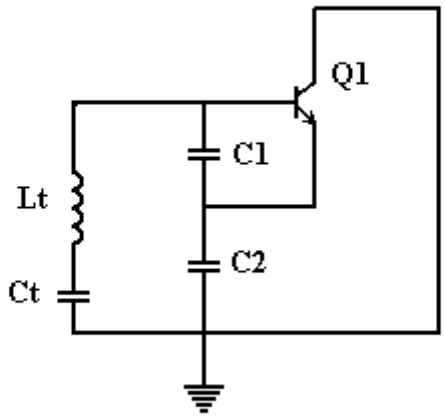
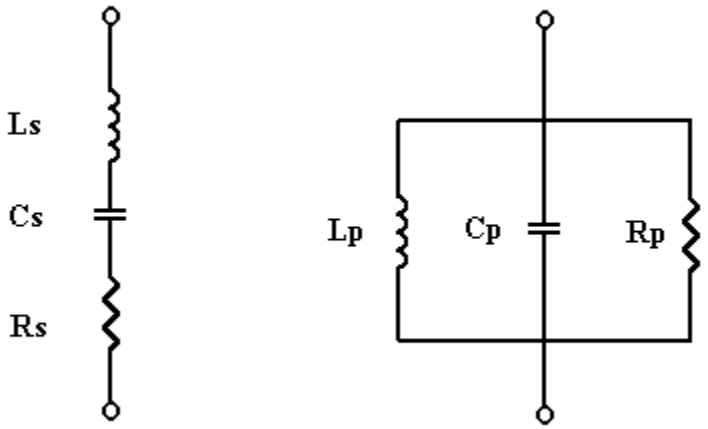


Figure 2.4: Active VCO core (Clapp topology) used in this work

2.2.2 Resonators

One unifying feature of most high quality oscillators is a low-loss resonator network. Appropriate implementation of the frequency selection components is critical in setting the tuning range, phase noise, harmonic content, and oscillation amplitude. The two basic resonator topologies (depicted in Figure 2.5) are series and parallel. In general, it is possible to reduce any resonator to an equivalent topology composed of these networks. The

resonators in this thesis will be confined to the discrete R-L-C variety for reasons, which will become apparent later in this section.



(a) (b)

Figure 2.5: (a) Series and (b) parallel resonant circuits

The loaded quality factor (Q_l) is of prime concern when considering resonators for VCO applications. Ultimately it is the Q_l of the resonator that determines the quality of the VCO output spectrum. The Q_l is defined by the amount of energy stored in the resonant circuit relative to the energy loss per cycle:

$$Q_l = 2\pi \cdot \frac{Peak\_Energy\_Stored}{Energy\_loss\_per\_cycle} \tag{2.7}$$

Alternatively, the Q may be defined in terms of the rate of phase change with respect to frequency (Eqation 2.8).

$$Q_l = \frac{\omega}{2} \cdot \frac{\partial \phi}{\partial \omega} = \pi \cdot f \cdot \tau_g \tag{2.8}$$

Where, ω is the angular frequency in radians/second, f is frequency in Hz, φ is the phase angle, and τ_g is the group delay defined as:

$$\tau_g = \frac{\partial \phi}{\partial \omega}$$

Still another definition of Q_l is the 3dB bandwidth (BW_{3dB}) of the resonator relative to the center frequency *fo* (eqn. 2.9)

$$Q_l = \frac{f_o}{BW_{3dB}} \tag{2.9}$$

An important distinction between the loaded and unloaded Q becomes apparent when the ideal resonator is separated from the loading effect presented by external impedances [7]. In the case of an oscillator, the active circuit will be connected to the resonator through some form of coupling and will tend to reduce the effective Q of the original network. So far in this section, Q_l of the entire resonator has been considered. This quantity differs from the Q of an individual component. The inductor is typically the dominant factor in determining the Q of an unloaded resonator since it tends to have the most loss associated with it. Surface mount inductors tend to have series resistance in the metal coils and skin effect resistance that result in a lower Q component than a lumped passive capacitor with equivalent reactance[3]. Therefore the Q of the resonator inductor (defined in eqn. 2.10) becomes an important issue.

$$Q_{inductor} = \frac{X_s}{R_s} = \frac{2\pi \cdot f_o \cdot L_s}{R_s} \tag{2.10}$$

[3] This may not be true when comparing lossy varactors, or higher Q inductance components (such as co-axial or waveguide)

Equation 2.10 holds for frequencies where f_o is below the self-resonance[4] (*fsr)* of the inductor. The effective inductor Q will increase as the test frequency approaches this point. Manufacturer models are available which have appropriate parasitic capacitive elements to take this into account. The basic equivalent model is shown in Figure 2.6 where the frequency dependent resistance is denoted by R(ω). A Pspice model and the typical values of inductance and Q versus frequency are shown in Appendix A. A Coilcraft® surface mount inductor is chosen for this work. The frequency dependent resistance, R(ω), is modeled with an ideal voltage to current converter shown in Figure A2 in the appendix. The frequency dependence is accounted for by a Laplace transform built into the simulation block.

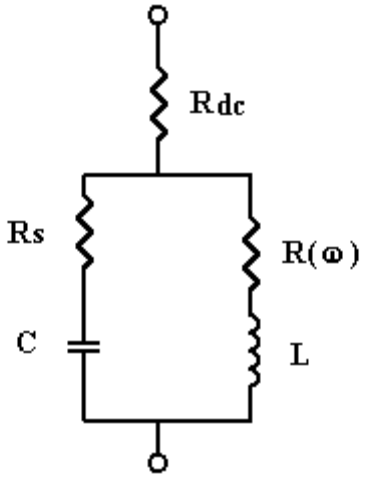


Figure 2.6: Monolithic inductor equivalent circuit

[4] The *fsr* of the inductor is the frequency at which the reactances of the inductance and parasitic capacitance cancel forming a parallel resonant circuit

2.2.3 Varactors

Most modern radios have discarded mechanical frequency tuning in favor of electrical means. This move has resulted from the widespread use of phase locked loop (PLL) circuits to accurately control frequency in a signal source. The PLL monitors the frequency difference between the VCO and some (usually crystal oscillator) reference signal. Any frequency difference produces a DC error voltage used to change the reverse bias on a semiconductor diode to "steer" the VCO frequency back to the desired output. Varactors are diodes that have been designed specifically to exploit the variable capacitance of a reverse biased P-N junction. The capacitance versus voltage characteristic of a varactor depends on the impurity density as a function of distance from the P-N interface [4]. The general equation for capacitance of a diode is expressed as:

$$C = \frac{k}{(V_d + V)^n} \tag{2.11}$$

Where, V_d is the contact potential of the diode, V is the applied reverse bias voltage, K is a constant, and n is a variable which is dependent on the diffusion profile of the diode.

A graded junction has a linear decrease in the impurity density with increasing distance from the P-N interface and has an *n* of approximately 0.33. Other diodes have an impurity density that increases with increasing distance from the P-N junction. These diodes are called hyper-

abrupt and may be manufactured with values of *n* greater than 0.5. The hyper-abrupt junction is designed primarily to achieve a larger tuning range for a specified voltage change.

While the preceding mathematical model is useful to determine the capacitance of a given varactor at a specific bias voltage, a more useful model is derived from an equivalent spice circuit. Spice models are typically provided in the manufacturer data and include the nonlinear effects of an exponential current to voltage characteristic. Accurate models become critical for simulations that incorporate nonlinear diode behavior to predict large signal effects. The equivalent circuit for spice models is depicted in Figure 2.7a. The symbol in Figure 2.7b depicts the symbol used in simulation schematics to represent the nonlinear and parasitic elements.

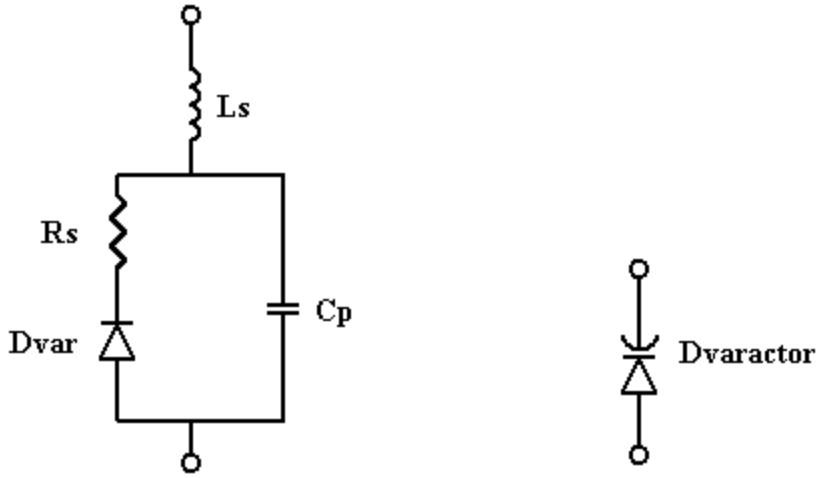


Figure 2.7: (a) Varactor electrical equivalent and (b) hierarchical symbol

The nonlinear model is imbedded in the diode (Dvar) while the bonding inductance (Ls), parallel capacitance (Cp), and DC series resistance (Rs) are incorporated as external parasitic

elements. Figure 2.8 shows the simulated tuning characteristic for the varactor used in this thesis for the SMV-1249[5] varactor model.

The varactor can be a critical component in VCO design for several reasons. Satisfying the required tuning range is only the first consideration. Varactors can also play a role in the phase noise performance of the oscillator. In addition to the noise current source associated with all active devices there is a phase noise degradation resulting from finite Q. The component Q is reduced by the inverse of the value of parasitic resistance. It will be shown in Section 2.3.2 that maintaining high Q is crucial to good phase noise performance.

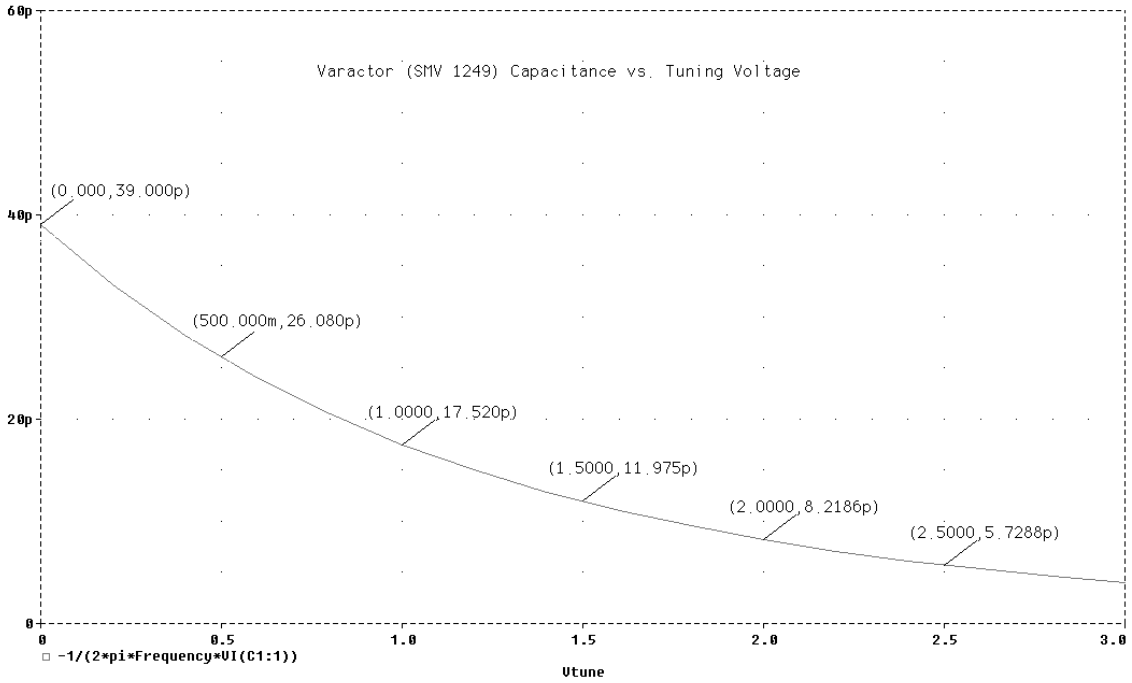


Figure 2.8: Simulated varactor capacitance versus tuning voltage

[5] This is the Alpha Inc. (now Skyworks™) part number for the varactor used in this work

2.3 Oscillator Parameters

Electronic components must conform to characteristic sets of specifications to operate properly. This generalization applies to VCOs as well. The following sections define several common oscillator specifications. The parameters presented, although not exhaustive, include those that have the most effect on system performance. The significance of these specifications on system performance is also covered.

2.3.1 Output Power

In a typical superheterodyne receiver the VCO output power must be adequate to drive a mixer as well as a PLL prescaler. For a transmitter, the VCO output must be able to supply enough to drive the power amplifier stages hard enough to obtain the appropriate level at the antenna. Thus, the output power requirement of a VCO is largely dependent on the signal levels required by the various radio subsections. Margin in the required output power is often accomplished with a buffer amplifier. One common method of ensuring adequate drive level is the use of a buffer amplifier between the output of the oscillator and the circuitry driven from the VCO. A buffer amplifier has the additional advantage of providing better isolation of the VCO from mismatched load impedance.

2.3.2 Phase Noise

Among the most touted specifications for signal sources in modern wireless devices is phase noise. This parameter is generally defined as the noise power level in a single sideband at a defined frequency offset from the free-running oscillator. The power is measured relative to the carrier in units of dBc/Hz. In standard measurements, the VCO output is observed on a spectrum analyzer and the noise level is measured in a low resolution bandwidth (RBW) and calibrated to a 1 Hz bandwidth. Figure 2.9 depicts the typical regions of VCO phase noise spectrum [4,12,13]. $L(f_m)$ is the noise power as a function of the frequency offset from the carrier.

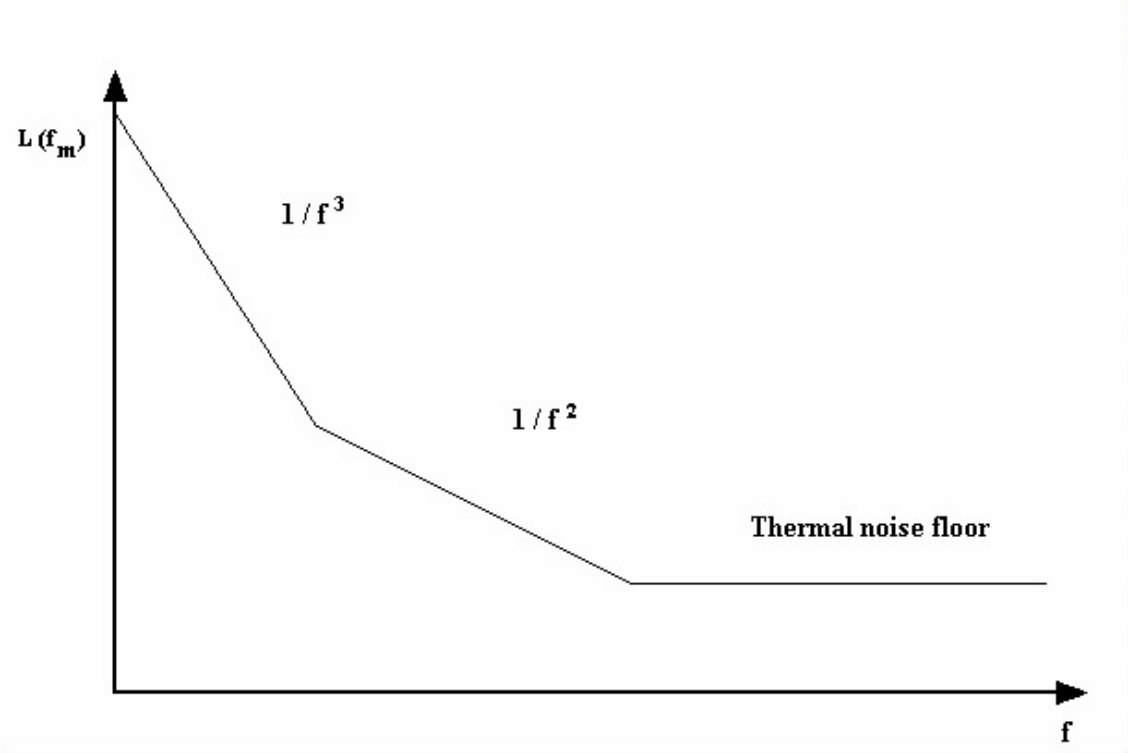


Figure 2.9: Typical oscillator phase noise spectrum

The subject of phase noise on the performance of radio systems has prompted several theoretical and experimental modeling efforts. D.B. Leeson[6] proposed an early model of phase noise that qualitatively describes the spectrum close to the center frequency of oscillation [14]. Leeson's model is primarily based on empirical data and incorporates three significant noise contributions: 1 - the upconversion of the 1/f noise present in the transistor, 2- the effect of the resonator Q in filtering noise about the natural frequency of resonance, and 3- the thermal noise contributed by the circuit. The well-known Leeson equation has been modified in several works to include the effect of varactor modulation [12,15]. The result usually takes a form similar to that of Equation 2.12.

$$L(f_m, K_{vco}) = 10 \cdot \log\left(\left(\frac{f_o}{2 \cdot Q_l \cdot f_m}\right)^2 \left[\frac{F \cdot k \cdot T}{2 \cdot P_{osc}} \cdot \left(1 + \frac{f_c}{f_m}\right)\right] + \frac{1}{2}\left(\frac{K_{vco} \cdot V_m}{2 \cdot f_m}\right)^2\right) \text{ [dBc/Hz]} \quad (2.12)$$

Where:
f_o = Frequency of oscillation in Hz
f_m = Frequency offset from the carrier in Hz
F = Noise figure of the transistor amplifier
k = Boltzmann's constant in Joules/Kelvin
T = Temperature in degrees Kelvin
P_{osc} = RF power produced by the oscillator in Watts
f_c = Flicker noise corner frequency of the active device in Hz
K_{vco} = Tuning sensitivity of the VCO in Hz/V
V_m = Total amplitude of all low frequency noise sources in V/ √ Hz

Other theoretical derivations based on the Leeson model have been introduced. These models rely mostly on a linear time–invariant approach to the problem [14,16,17]. More

[6] Leeson proposed one of the earlier models of phase noise which is often cited as a reasonably accurate first order approximation to phase noise in an oscillator.

recently, general theories have been introduced which provide quantitative predictions of phase noise [18, 19]. The model proposed by Hajimiri and Lee introduces the concept of an impulse sensitivity function. The Hajimiri and Lee model implies that time variance is an inherent part of VCO operation and the phase noise can be predicted by systematic analysis of circuit response to current impulses. Two versions of the Leeson model for phase noise are used in Chapter 4 to predict and minimize phase noise. Specifically, the Pspice simulation uses the Leeson style approximation whereas the ADS simulation uses a nonlinear harmonic balance approach. The peculiarities of each of these methods are covered.

The impetus for increased attention to accurate modeling, simulation, and measurement of phase noise is based on the impact it has on system performance. Demand for higher data throughput has driven the trend toward modulation schemes with higher density constellations. Condensed constellations imply a narrower margin of phase between adjacent data bits and an inherently increased sensitivity to perturbations in signal phase. The signal fidelity is directly influenced by the quality of the VCO in the system. Therefore it has become more important to concentrate design efforts to minimize phase noise in this section of the radio.

Another constraint on maximum allowable phase noise comes from reciprocal mixing effects [17]. This occurs when a signal source with large noise sidebands is used as a receiver LO. The non-linear operation within the mixer acts to multiply the oscillator with the incoming RF to produce an intermediate frequency (IF) at a suitable frequency for filtering. A problem arises when the desired RF signal injected into the receive mixer is accompanied by

a strong unwanted signal (or interferer signal) close by in frequency (Figure 2.10). If the noise in the LO sideband is sufficiently high the resultant IF output may be completely blanketed by the mixing product of the LO noise and interferer.

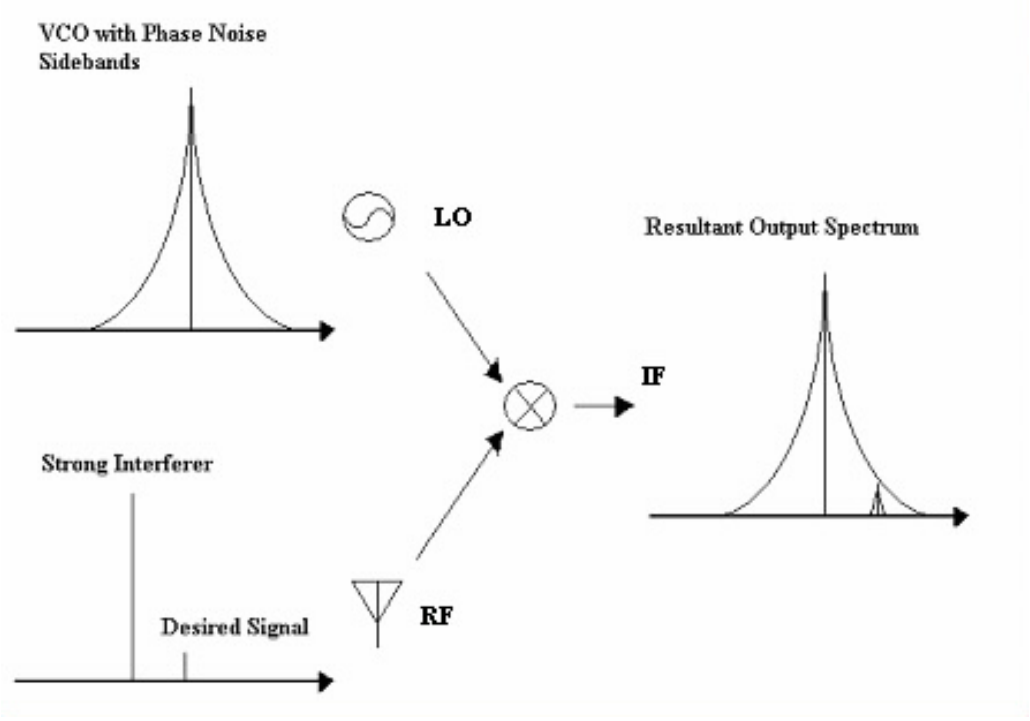


Figure 2.10: Reciprocal mixing effect in received signal spectrum due to poor phase noise

2.3.3 Supply Pushing

In many mobile wireless applications there can be a substantial drain on the main supply current that is transient in nature. The current switching can cause voltage changes on the supply to the VCO and can result in unwanted modulation sidebands that fall outside the PLL loop bandwidth. Therefore, there is a need to try to design an oscillator that has good supply rejection.

The term "supply pushing" refers to a measure of the sensitivity of a free-running VCO to variations in supply voltage. The measurement is typically taken by varying the supply voltage over a given range while measuring the VCO frequency. The frequency shift is divided by the voltage change to determine sensitivity in Hz/V. An ideal VCO has an output frequency that is independent of the supply voltage that provides power to the circuit. However, in most practical circuits there is some fluctuation in the output frequency as a function of supply. Well-designed VCOs have pushing factors between 5% and 10% of the main tuning-line sensitivity [12]. The best method to prevent this problem is to minimize the supply dependence of current and voltage references in the bias circuitry. Supply rejection allows the system to operate free from the influence of battery charging or low battery voltage conditions. For most modern portable applications the available supply is 3 Volts. A typical error tolerance allows for a range between 2.7 and 3.6 Volts. This supply range is assumed for the simulations and measurements described in this work.

2.3.4 Load Pulling

Insufficient isolation between the VCO and load impedance can degrade system-level performance. One common scenario where this occurs is when a VCO is loaded directly by a power amplifier (PA) in a cellular phone. To conserve battery power in a cellular application, the PA is normally activated only when a voice signal is present. Once activated, the abrupt change in the bias current causes the input impedance of the PA to change significantly and present a different load impedance to the VCO driving the transmit chain. Changes in load impedance tend to cause variations in output frequency and can result in the PLL slipping cycles or even completely losing phase lock.

Load pulling measures the sensitivity of a free-running VCO to load variations at the VCO output. Measurement[7] requires a load-impedance mismatch and a variable-length transmission line. The VCO is connected to the mismatched load, and the phase angle is varied (between VCO and load) through 360° by changing the length of the transmission line. The resulting peak-to-peak frequency change is then measured over the resulting impedance range. VCO load pulling specifications are defined in terms of the maximum peak-to-peak frequency shift over a given load VSWR. A 1.75:1 VSWR was used in this thesis to define the load pull data. Equation 2.13 shows the relationship between load VSWR and load-impedance mismatch.

[7] The measurement setup is depicted in Figure 5.10

$$VSWR = \frac{1+|\Gamma_o|}{1-|\Gamma_o|}; \qquad \Gamma o = \frac{Z_L - Z_o}{Z_L + Z_o} \qquad \text{(eqn 2.13)}$$

Where, VSWR is the voltage standing-wave ratio, Γ_O is load-reflection coefficient: the ratio (at the load) of the incident voltage wave to the reflected wave, Z_L is the load impedance, and Z_O is the transmission line's characteristic impedance.

Implementing a buffer amplifier is the most common technique for reducing a free-running VCO's sensitivity to load variations.

2.3.5 Tuning Sensitivity

Tuning sensitivity is also referred to as VCO gain particularly in literature discussing PLL terminology. This is a system-level parameter (measured in Hz/V) that relates the maximum available tuning voltage to the frequency tuning range. It is directly related to the impedance presented by the resonator circuit. In a capacitively tuned network the inductance value is fixed and a variable capacitance is used to change the resonant frequency of the tank network. As was mentioned in Section 2.2.3, varactor diodes are the dominant choice for variable capacitors. An important characteristic of varactors is the effective resistance associated with a given device.

Varactors with larger capacitance tuning ranges (ΔC for a given ΔV) tend to have a higher series resistance that lowers the Q of the device. Since phase noise performance is closely

tied to loaded tank Q, there is an inverse relationship between tuning range and phase noise in varactor tuned VCOs.

Variation of tuning sensitivity over the tuning-frequency range is another important consideration. The VCO is usually the highest gain device in a PLL with typical sensitivities in the tens of MHz/V. If tuning sensitivity varies too dramatically over the tuning band, the synthesizer performance suffers. Tuning sensitivity also impacts noise. Fundamentally, the VCO is a voltage-to-frequency converter. Unwanted side-bands are generated in the output as a result of noise voltage at the tuning port modulating the output frequency. This issue is particularly problematic at the steepest slope in the frequency versus tuning voltage characteristic. Therefore, caution must be exercised in ensuring that the tuning-port noise is minimized.

2.3.6 Harmonic Levels

Output harmonic level is a measure of the VCO energy at harmonics of the oscillation frequency. These harmonics, common at levels below -15dBc, are generated by the nonlinear self-limiting of active devices in the oscillator. Oscillators with large amounts of excess gain[8] will limit more severely thereby generating greater harmonic content in the output waveform. Good designs balance the need to keep harmonic levels low with the need for enough excess gain to ensure a reliable start-up. Ideally the amplifier in the VCO is operating in a region

[8] Excess gain describes any loop gain greater than the amount necessary to offset the resonator losses.

that is as linear as possible. This quasi-linearity presumes a soft limiting mechanism by the transistor junction. The large oscillator level passing through a subsequent buffer amplifier potentially creates additional harmonic energy.

2.3.7 Current Consumption

The trend toward more mobile wireless and computing devices has caused a demand for products that use less power to perform the same function. Consequently, industry research has emerged in the areas of better battery technology and higher power efficiency topologies. With regard to IC design, reduced current consumption has become much more critical for circuits used in battery operated devices. One popular method of reducing current drain has been to implement a power down mode. Usually a logic level control is provided which disables the entire circuit and forces a current consumption of less than a few microamperes. This slows the drain on the battery to a fraction of what it would be if the circuit were allowed to provide constant quiescent currents to all functional blocks. This scheme is employed within the bias circuit presented in this work.

3 Analysis and Design

3.1 Oscillator Circuit Analysis

One of the more complex analog circuits to analyze is an oscillator. The premise that an oscillator is designed for instability inherently goes against most tenets of good analog design. As has been previously established, positive feedback is required to generate the unstable system necessary to sustain oscillation. Since the feedback is part of the overall network it can be difficult to separate from the rest of the oscillator circuit. This chapter deals with some of the common analysis and design techniques used in dealing with the complex nature of VCOs. The first section outlines the core oscillator circuitry that is analyzed using the negative resistance concept. The next sections deal with the support circuitry including the biasing and buffer amplifier. Finally, some issues associated with packaging and layout are addressed in the last sections of this chapter.

3.1.1 Oscillator Topology

As discussed in section 2.2.1, the topology selected for this study is a modified version of the Clapp network. This version of the circuit has the addition of a varactor as part of the resonator network connected to the base of Q1. The primary reason for this selection is simplicity. This topology is well documented in VCO designs and it has proven to be robust

and amenable to integration into a monolithic form. The basic Clapp network is depicted in Figure 3.1 without buffer circuitry and it provides the platform for the rest of the design.

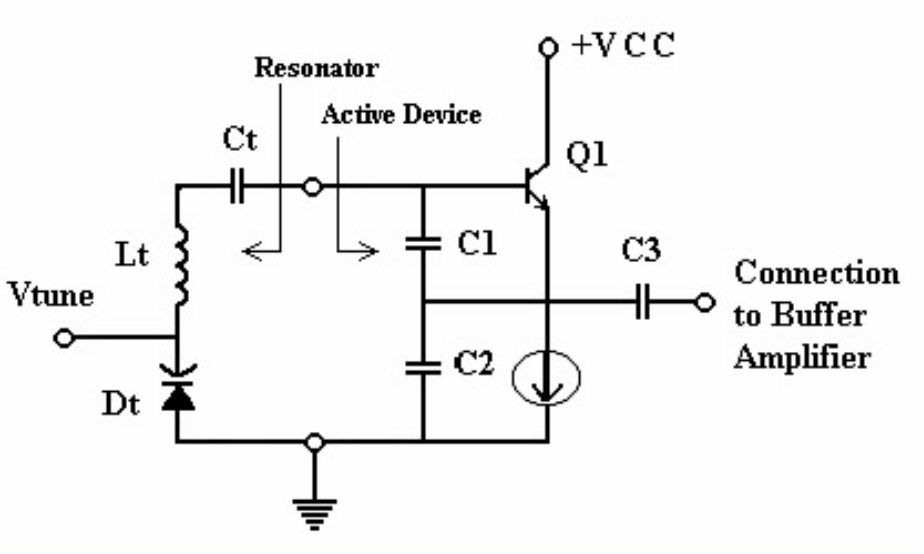


Figure 3.1: The VCO core used in this work

Energy is coupled into the buffer amplifier from the emitter of Q1 as shown in Figure 3.1. Coupling energy from the base would directly load the resonator Q and coupling energy out of the collector poses biasing issues. The emitter provides a convenient point to extract the VCO signal without causing significant resonator loading or bias problems. The emitter node also provides a smaller voltage swing than would be found at the collector.

In section 2.1.2, it was shown that non-linear distortion is a function of the peak voltage of a sinusoid driving a base-emitter junction. The non-linearity is necessary for the limiting function in oscillators but is undesirable in the buffer amplifier. A lower voltage swing is less likely to cause distortion when amplified by the buffer. The issue of the buffer amplifier loading the VCO is lessened by increasing the input impedance of the buffer.

The addition of a series capacitor from the oscillator output to the buffer input eliminates excess current drain from the buffer on the VCO and it allows a separate bias scheme to provide bias isolation between the two circuits. A large enough value capacitor must be used in order to allow low frequency signals to be passed to the buffer. This essentially sets up a high pass network and limits the frequency range over which the VCO will work. The main disadvantage in using a large capacitor as a coupling element is that it consumes significant die area[9].

3.1.2 Analysis

Oscillator circuit analysis can generally be classified into one of two methods. One method is called negative resistance analysis and the other method is referred to as transmission analysis[10]. Transmission analysis, as described in Chapter 2, is based on classical network techniques and considers the oscillator as a two-port network with a feedback path. Many arguments have been made that this method is superior to the negative resistance technique [7,20]. The claim is that better insight into oscillator operation is achieved when the feedback path is defined in terms of circuit components.

In contrast, the negative resistance is used in higher frequency oscillators where the feedback path is not as obvious. This technique considers active oscillator circuit and resonator as two

[9] The 5.5 pF capacitor used for the VCO presented here is 8,464 μm^2 which is larger than any other circuit component on the die.
[10] Network analysis and feedback analysis are names that have been used synonymously with transmission analysis.

separate one-port networks. One advantage of this method is that it more easily accounts for multiple parasitic impedances, which can be difficult to incorporate into a feedback network. Another advantage comes when the design is ready to test in the lab. One-port negative resistance measurements are easily made using network analyzers and can be used to verify simulation results.

In the end, both negative resistance and transmission analysis methods provide a starting point to evaluate the circuit and both have been described extensively in the literature [7,8,20,21]. However, the negative resistance technique is used in this thesis for the previously stated advantages.

The fundamental premise behind the negative resistance concept is that a single port circuit with a reflection coefficient greater than unity has the potential to oscillate. Evaluating Equation 2.13 for the reflection coefficient with Z_O set to 50 Ohms and Z_L represented by a negative number yields a magnitude which will always be greater than 1. Physically this means that the active device is reflecting or sourcing more power to the network test port than is being absorbed. The illustration in Figure 3.2 shows a generalized oscillator split into a negative resistance and a resonator.

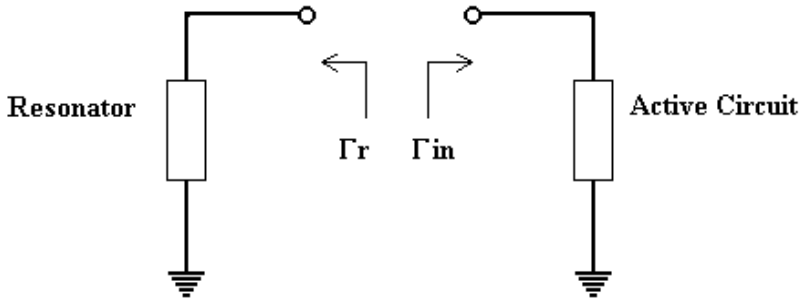


Figure 3.2: Negative resistance concept using reflection coefficients

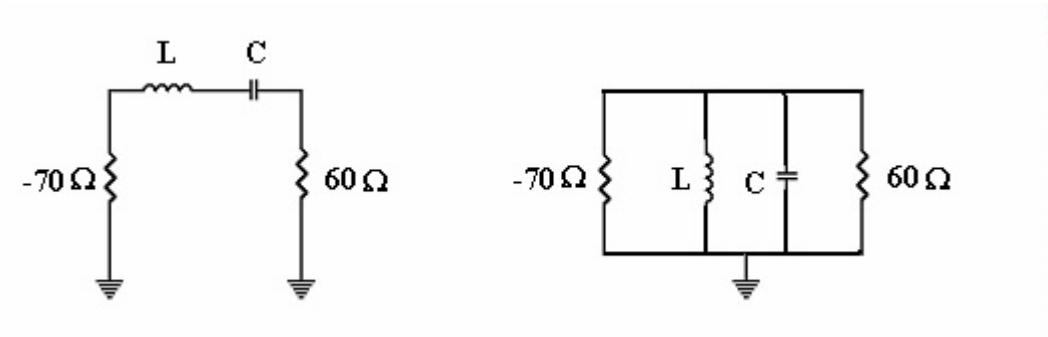
The reflection coefficient Γ_{in} represents the reflection coefficient looking into an active device and Γ_r represents the reflection coefficient of the passive resonator. Equation 3.1 describes the conditions necessary for oscillator starting in terms of reflection coefficient magnitudes and phases. Intuitively this is just a restatement of the Barkhausen criterion for a single port system.

$$\left|\Gamma_r\right\|\Gamma_{in}\left| > 1 \text{ and } \quad \phi_r + \phi_{in} = 0 \right. \tag{3.1}$$

Where ϕ_r and ϕ_{in} are the phases associated with the resonator and active device respectively.

Several papers have been written which use Figure 3.2 as a starting point for negative resistance theory [22,25,26,27,28]. However, most authors are quick to point out that care must be taken in determining the circumstances under which this expression can be applied. It has been shown that the preceding analysis is flawed for certain instances [22,23,24]. One potential for error can occur when a parallel tank network is connected to a negative

resistance port. The circuits in Figure 3.3 demonstrate this point. If one were using the conditions in Equation 3.1 to evaluate the potential for oscillation, one would erroneously arrive at the conclusion that both circuits are stable. Both circuits in Figure 3.3 would appear[11] to be stable ($\Gamma_{in} = 0.091$ and $\Gamma_r = 6$ resulting in $|\Gamma_r \cdot \Gamma_{in}| = 0.546$ which is less than 1). However, the circuit in Figure 3.3(a) is actually not stable when analyzed using real and imaginary impedances. The series resistance elements in Figure 3.3(a) add directly for a net –10 Ω resistance and the imaginary terms cancel at resonance. This result implies that the circuit will in fact be unstable which contradicts the prediction made using Equation 3.1.



(a) (b)

Figure 3.3: Basic negative resistance circuits

Similar mis-applications of Equation 3.1 have been presented. Nguyen has shown that a resonator may have several frequencies at which Equation 3.1 holds and may not provide stable amplitude at the desired frequency [24]. Another possibility is that as the oscillation amplitude builds up the operating impedances will shift such that the poles move into the left half plane and the oscillation is no longer sustained. It should be noted that the reflection coefficient does not imply anything about steady state operation, but rather just addresses the

[11] Evaluating at resonance in a 50 Ω system., the reactive components are presumed to have no loss.

concern as to whether or not the circuit is stable. As a result, Equation 3.1 provides a convenient but limited method for determining the potential of a circuit to oscillate. Other techniques can provide a more stringent stability criterion.

One method of evaluating stability in a simulation environment uses Nyquist's criterion applied with reflection coefficients. Figure 3.4 depicts the use of an ideal circulator to present the desired reflection coefficient at port 1 [22]. Stability is determined by plotting the result of a small signal S-parameter sweep on a polar graph. This allows the magnitude and phase to be expressed as a product of the resonator and active device reflection coefficients. According to Nyquist, if the curve encircles –1 as plotted over frequency then the system has the potential to oscillate. The Nyquist criterion is applied to the network[12] in Figure 3.1 to establish the conditions for oscillation.

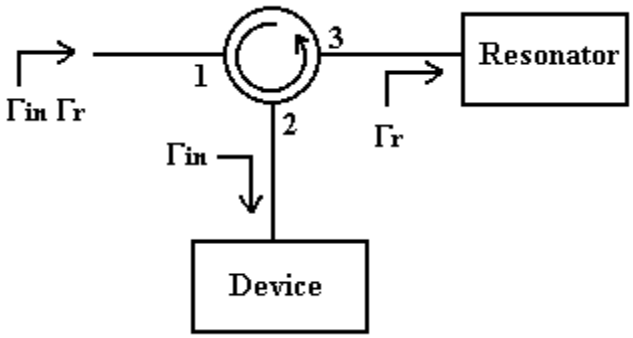


Figure 3.4: Simulation network used to determine stability criterion

[12] The resonator and active circuit are separated as indicated in figure 3.1 and the circulator shown in figure 3.3 is inserted between them.

The Nyquist plot shown in Figure 3.5 represents the simulation result for the Clapp topology used in this thesis. The simulation result depicts the reflection coefficient curve encircling –1. This system satisfies the Nyquist condition for an unstable system.

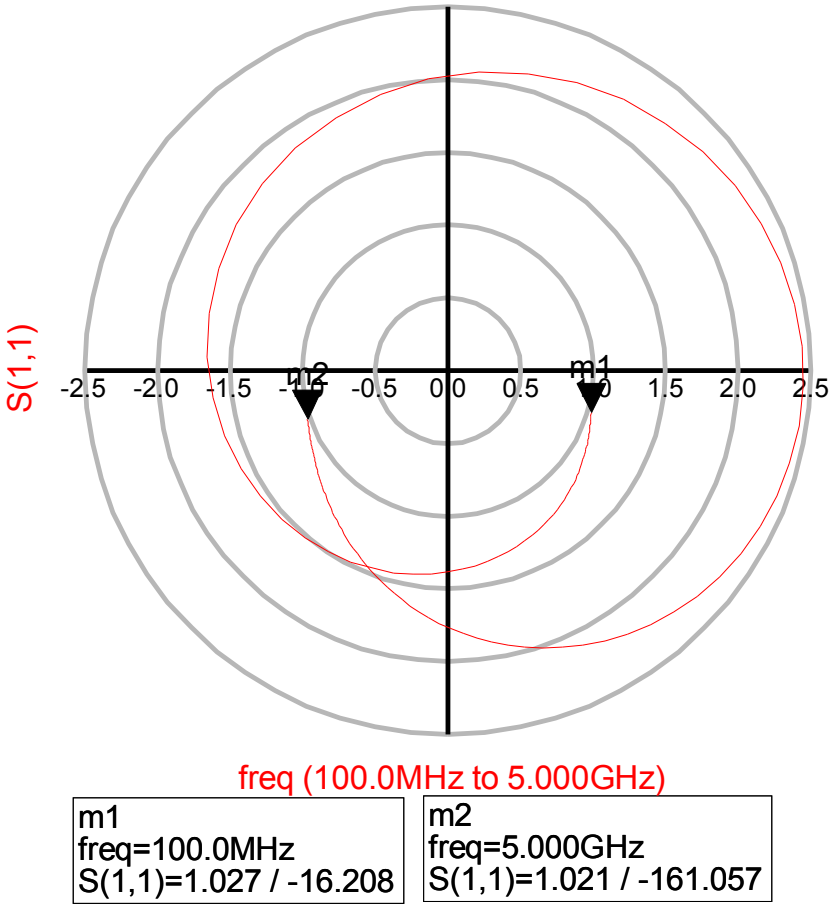


Figure 3.5: Nyquist stability plot for the VCO core

Another popular method for analyzing stability in an oscillator employs the Smith chart. Several authors have shown the negative resistance concept to be more easily evaluated when

the reflection coefficient is graphed [8,21,25]. This is typically done by solving the equation governing sustained oscillation and plotting the one-port reflection coefficients. Specifically, Equation 3.1 shows that a circuit is potentially unstable at the point where Γ_r is equal to the reciprocal of Γ_{in}. This may be interpreted graphically by plotting $1/\Gamma_{in}$ (evaluated as a function of the input amplitude A) and Γ_r (evaluated versus frequency ω) on the same Smith chart. This method, illustrated in Figure 3.5, provides an approximation of the oscillator operating conditions. The reason for this becomes apparent when considering the impedance of the active device at steady state. The line represented by $\Gamma_{in}^{-1}(A)$ represents a shift in the active device impedance relative to the input signal. Similarly, $\Gamma_r(\omega)$represents a shift in the resonator impedance as a function of frequency. The small signal condition for oscillation is satisfied if the starting point for $1/\Gamma_{in}(A)$ lies within the resonator $\Gamma_r(\omega)$ curve.

Increasing amplitude presented to the active device simulates the conditions exhibited by growing oscillations and causes $\Gamma_{in}^{-1}(A)$ to shift the Smith chart. This represents a decrease in the negative resistance that at some point will be equivalent to the positive resistance in the resonator. Thus, the intersection of the two curves indicates the point at which the condition described by Equation 3.1 is satisfied. This is indicated in Figure 3.6 as the *point of oscillation*.

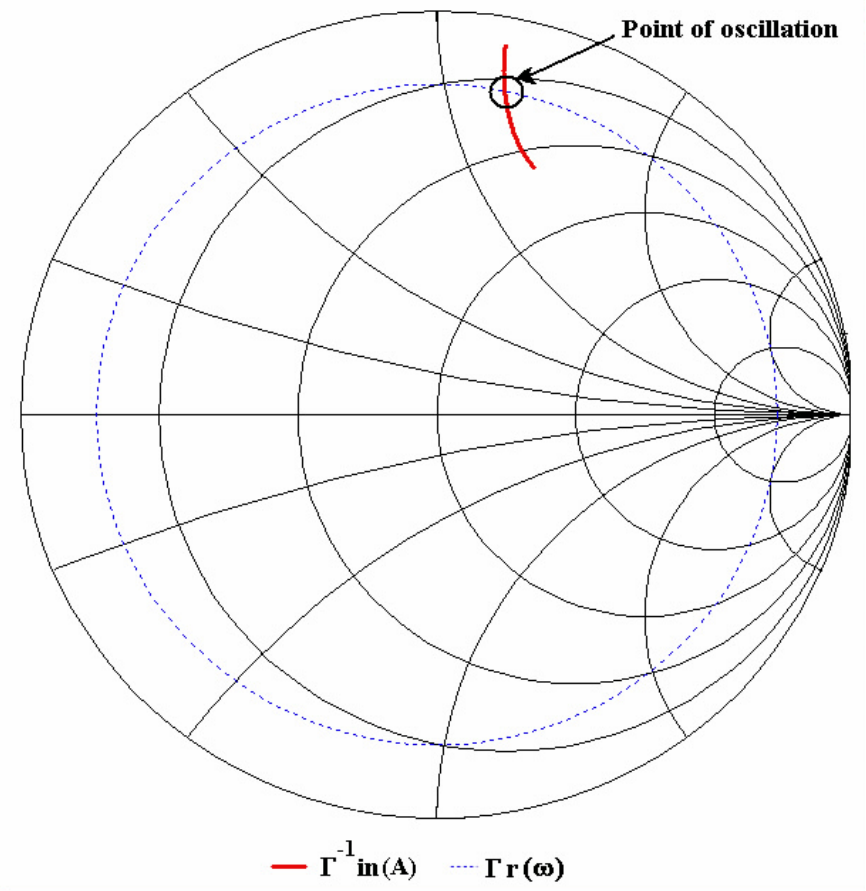


Figure 3.6: S-Parameter representation of negative resistance concept

Several papers have been written about the angle (α) formed between the two tangent lines [d Γ_{in}^{-1}(A)/dA and d Γ_r(ω) / dA) in Figure 3.7. Esdale and Howes[13] present a stability criterion that is based on the intersection of the reflection coefficient locus of the two curves shown in Figure 3.6. According to the theory, stable oscillation is achieved when α < 180°. This condition is satisfied when Γ_{in}^{-1}(A) intersects Γ_r(ω) at only one point where the trajectory of Γ_{in}^{-1}(A) starts inside the resonator curve and progresses toward the outer edge of the Smith chart. As the oscillator approaches steady state, Γ_{in}^{-1}(A) will decrease in

[13] This is the reflection coefficient equivalent of a derivation originally proposed by Kurokawa [21]

magnitude until it is equivalent to the $\Gamma_r(\omega)$. The steady state frequency is determined by the point at the intersection of the two curves in Figure 3.7. Exact operating amplitude is not predicted using this method because the resonator and VCO core are not actually loaded by each other but rather by a linear 50Ω source. The measurement technique to obtain the reflection coefficients requires that the circuit be broken into two separate measurements. The one-port measurements are taken on the resonator and active circuit separately. The result is that the non-linear loading of the active device by the resonator is not included. However, the value of A at the "point of oscillation" represents the cumulative result of the nonlinear behavior of the active device at the frequency of interest. It is therefore reasonable to use this value as an approximation of the steady state amplitude.

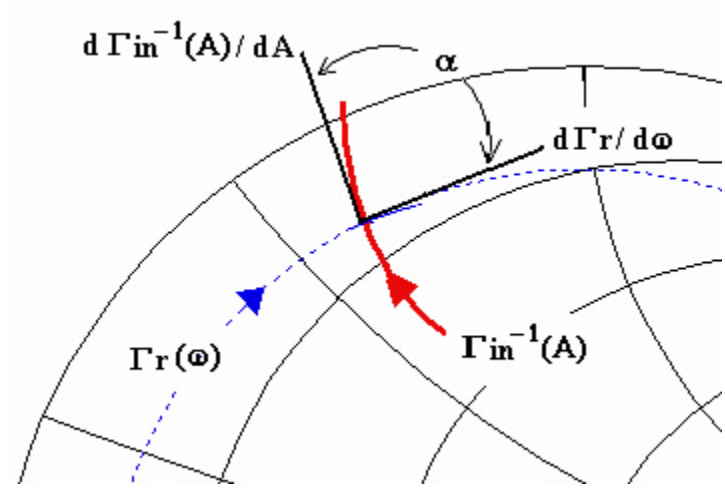


Figure 3.7: Steady state stability criterion using reflection coefficients

A useful byproduct of this type of analysis is the insight that may be obtained about the phase noise performance. Esdale and Howes claim that good noise performance may be achieved if the following conditions are met:

1) The angle α is 90°
2) The change of $\Gamma_r(\omega)$ with frequency is maximized (which is equivalent to maximizing Q
3) The change of $\Gamma_{in}^{-1}(A)$ with amplitude is minimized

The last and possibly most intuitive negative resistance technique to ensure oscillator startup uses traditional network elements. This is similar to the S-Parameter technique described previously but uses the real and imaginary circuit elements instead of a parameterized matrix. This method is attractive in that it incorporates information left out when only the reflection coefficients are used to establish stability.

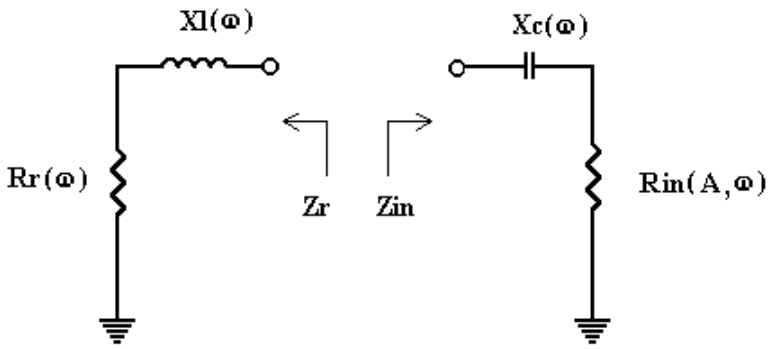


Figure 3.8: A generalized negative resistance oscillator

The real and imaginary parts of the negative resistance and resonator circuits are then defined as:

$$Z_{in} = R_{in}(A,\omega) + X_c(\omega) \quad \text{and} \quad Z_r = R_r(\omega) + X_l(\omega) \tag{3.2}$$

Where Z_{in} and Z_r are the input impedances of the active circuit and the resonator respectively. $R_{in}(A,\omega)$ and $X_c(\omega)$ are negative quantities, A = amplitude of oscillation, and ω = frequency of oscillation in radians/sec.

The condition for oscillation is then:

$$R_{in}(A,\omega) + R_r(\omega) < 0 \quad \text{and} \quad X_l(\omega) + X_c(\omega) = 0 \tag{3.3}$$

A first order verification of the VCO starting conditions requires an estimate of the impedances expressed in Equation 3.3 where the amplitude A is low enough to assume small signal conditions. This is accomplished by replacing the resonator with an ideal AC current source. This source is used to inject a test signal into the negative resistance generating circuit (Figure 3.9).

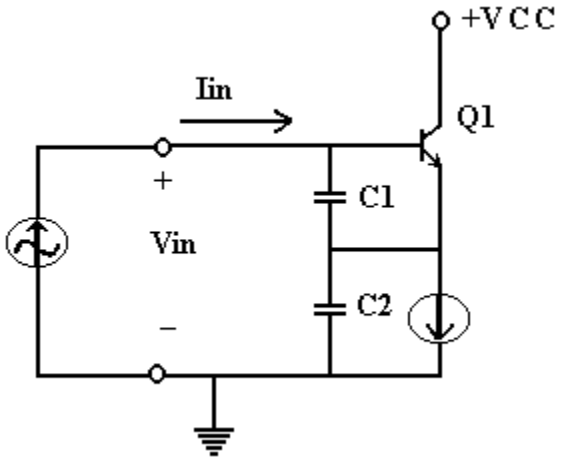


Figure 3.9: Test circuit to find the input impedance of the negative resistance generator

The impedance looking into the active circuit is then found by Equations 3.4 and 3.5 [4].

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{(1+\beta)X_{C1} \cdot X_{C2} + h_{ie}(X_{C1} + X_{C2})}{X_{C1} + h_{ie}} \tag{3.4}$$

$$Z_{in} = \frac{V_{in}}{I_{in}} \approx \frac{-gm}{\omega^2 \cdot C1 \cdot C2} + \frac{1}{\sqrt{j\omega(C1 \cdot C2/(C1+C2))}} \tag{3.5}$$

Where C_1 and C_2 are the capacitances in Figure 3.8. XC_1 and $XC_{2\ are}$ the reactances of C_1 and C_2 β is the current gain, h_{ie} is the input impedance h-parameter for a common emitter amplifier.

To start oscillation an inductor is required to tune the capacitive reactance. The series resistance (R_r) in the tank circuit must be less than the real part of the input impedance.

$$R_r(\omega) < \left| \frac{-gm}{\omega^2 \cdot C1 \cdot C2} \right| \tag{3.6}$$

$$\frac{-gm}{\omega^2 \cdot C1 \cdot C2} \geq \frac{1}{j\omega \cdot C1} + \frac{1}{j\omega \cdot C2} \tag{3.7}$$

The resonant frequency f_o is determined from Equation 3.8. The inductance L in this equation is the total effective inductance once the reactance of Ct has been subtracted.

$$f_o = \frac{1}{2\pi\sqrt{L(C1 \cdot C2/(C1+C2))}} \tag{3.8}$$

In the preceding equation it is assumed that the reactances of C1 and C2 are much less than the effective base emitter resistance r_π and the load resistance (Rload) of the circuit respectively [4].

3.2 Buffer Circuit

In order to prevent loading of the VCO a buffer amplifier is typically used. This helps to isolate the active oscillator from the load impedance and avoid potential shifts in frequency and output power. In this work, it was required that the buffer circuit have a large bandwidth to accommodate the operating frequencies. One topology that has superior bandwidth and isolation properties is a two-stage amplifier composed of a common emitter followed by a common base. This configuration is commonly referred to as a cascode amplifier.

3.2.1 Cascode Topology

The basic cascode network depicted in Figure 3.11 has several properties that satisfy the requirements of a VCO buffer amplifier. As outlined in the previous section, this configuration affords excellent isolation and high bandwidth. This results from the high output resistance and minimal high-frequency feedback that occurs through the decreased Miller capacitance. In a common emitter configuration (of the type depicted in Figure 3.10)

the Miller capacitance contributes significantly to RF energy coupling to the output. The gain of an ordinary common emitter amplifier loaded by a resistance R_l is defined as:

$$A_v \cong -gm \cdot R_l \tag{3.9}$$

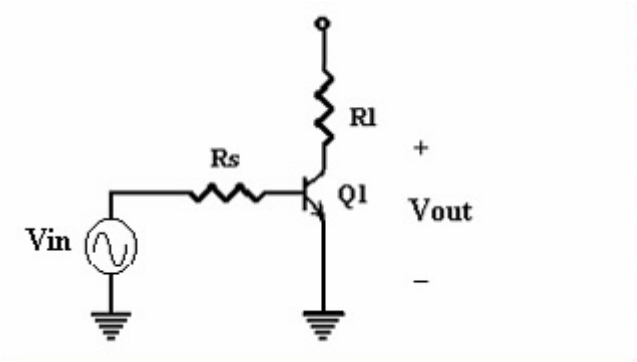


Figure 3.10: Common emitter amplifier

The frequency response of this type topology is limited by the so-called Miller capacitance C_M:

$$C_M \cong (1 + Av)C_\mu \tag{3.10}$$

This is the apparent base-to-collector capacitance in a common emitter amplifier. C_M is effectively larger than C_μ by a factor roughly equal to the voltage gain Av. A typical frequency response is then limited by the pole set by the sum of C_π and C_M seen across the base-emitter junction.

One solution to this problem is to use a two stage common emitter – common base (CE-CB) amplifier known as a cascode configuration. The network (Figure 3.11) significantly reduces the Miller effect because the load impedance on Q1 is very low and the voltage gain is directly related to the load impedance. The result is that the *Av* term in Equation 3.10 becomes low enough to cancel out the Miller capacitance. The cascode network is then no longer constrained by this dominant pole resulting from Miller capacitance.

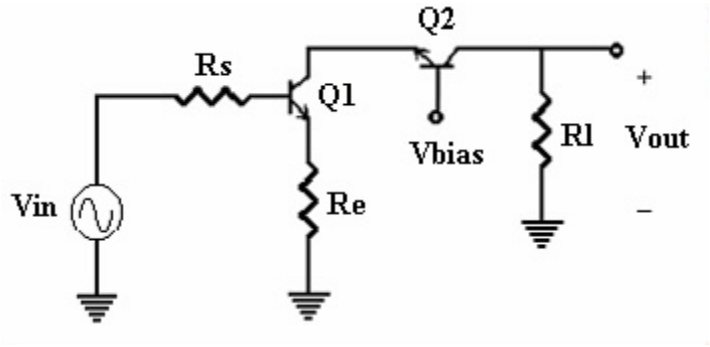


Figure 3.11: Basic cascode amplifier topology

The equivalent model depicted in Figure 3.12 allows easier visualization of the loading effect on Q1.

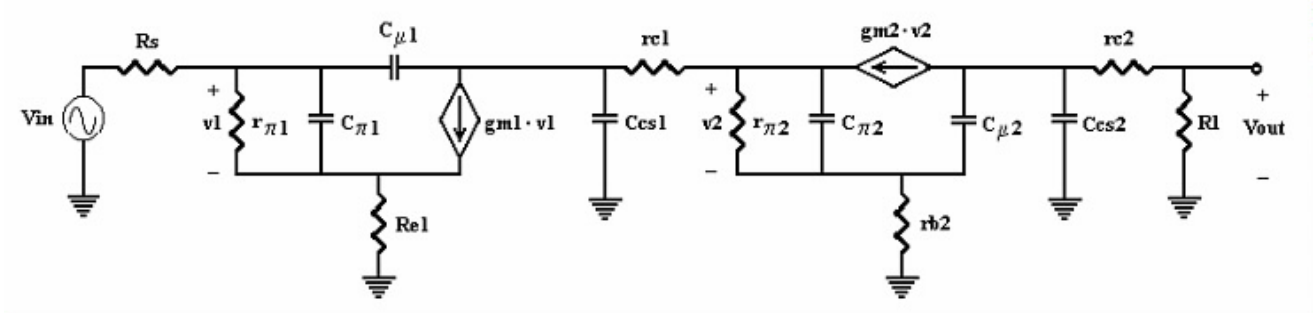


Figure 3.12: Cascode AC equivalent model showing parasitic elements

The load resistance presented to the collector of Q1 has been reduced by the common base stage that can be approximated as:

$$Rin2 \cong \frac{1}{gm2} = \frac{Vt}{Ic} \tag{3.11}$$

For bias currents in the 10mA range, the load impedance seen at the collector of Q1 will be only a few ohms in parallel with $C_{\pi 2}$. The result is an effective increase in the usable frequency response of the amplifier. Another advantage is the increased isolation of the cascode topology. The output impedance at the collector of a common base amplifier is determined predominantly by the load presented to it. This fact, coupled with the very low inter-stage impedance between the CE-CB stages, provides excellent immunity to load pulling effects.

The last issue in the buffer circuit design is the DC bias network. A fixed reference voltage bias is applied to the base of the common emitter stage. The reference voltage, covered later in this chapter, essentially sets the common emitter stage as a current sink for the common base stage. This is preferred over the method used in the VCO core bias for voltage limitation reasons. The specified supply voltage *VCC* presumed for this work could go as low as 2.7V. A current mirror bias as used in the VCO core would require at least three diode drops to accommodate the base-emitter bias condition. This would consume almost all the available voltage and leave little margin for signal voltage swing. The circuit depicted in Figure 3.13 shows the bias network used in the buffer amplifier for this thesis.

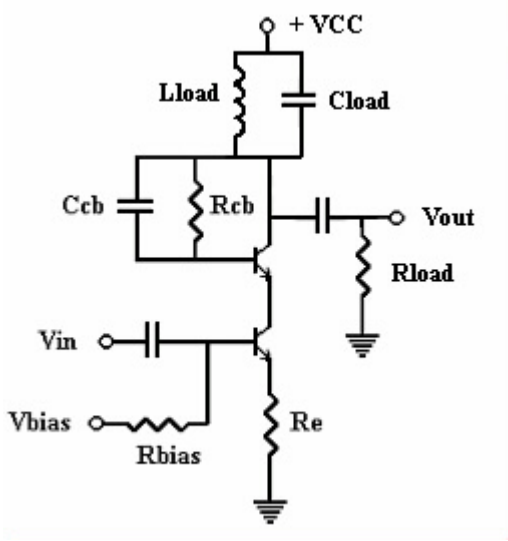


Figure 3.13: Cascode configuration used in this work

3.2.2 Oscillator Coupling

The term oscillator coupling refers to the method by which power is coupled into and out of the active device. The degree of coupling between the resonator and active device tends to be more critical as it directly impacts the resonator loaded Q. The value of Ct in Figure 3.1 provides a DC block for the varactor tuning voltage but also establishes the amount of resonator coupling. The effect of this capacitance may also be viewed in terms of the overall series resonator network. When the impedance of Ct is comparable to the impedances of other elements in the tank network it will influence the resonant frequency.

Coupling energy out of the active device is also an important issue to consider. The subsequent buffer stage input impedance should be made sufficiently large so as to have a negligible loading impact on the VCO.

3.2.3 Output Load

The ultimate goal in oscillator design is to deliver power into a specified load. Since the output impedance of the buffer amplifier is rarely the same impedance as the load into which power is to be delivered, some form of matching network is required. The purpose of the VCO will define what type of match is required. In some cases, the oscillator output is loaded directly by the final power amplifier in the radio. In this case, it may be desirable to attempt to match the output for optimum efficiency or maximum drive. Other applications may require that the oscillator output spectrum have a minimum harmonic content. In this work, it was deemed more important to minimize harmonic content than extract the last possible dB of power from the buffer amplifier. The impedance seen at the output is the open collector of the buffer amplifier. The collector represents a high impedance compared to the desired load of 50 ohms. A simple parallel tuned LC tank (formed by Cload and Lload in Figure 3.13) was used to provide the necessary DC path required by the VCO buffer and aid the objective of low impedance harmonic termination. The result is a parallel resonant circuit that has a low effective Q due to the loading of the 50Ω terminating impedance.

3.3 Bias Circuit

The bias circuitry in a VCO is as important as the rest of the design. Properly designed biasing accomplishes several goals which include: providing constant output power,

maintaining bias levels over process and temperature, and minimizing variation in oscillator performance as a function of battery voltage. Bias circuits also have an impact on noise power and should be optimized to lessen the noise injected into the VCO core.

The logic behind providing a constant output power stems from radio system requirements. A receiver system needs a certain minimum oscillator output level to ensure the mixer and PLL prescaler will work properly. A transmitter system often requires a range of input power so that the resultant power at the antenna is neither too low nor too distorted.

Maintaining a constant bias level with changes in process and temperature has the benefit of fixing a constant small signal transconductance (*gm* defined in eqn. 3.12 in terms of the collector current *Ic* and the thermal voltage V_t) through the active devices. This sets the initial gain for the oscillator and ensures that startup will occur. The quiescent current through the active device will also set the operating conditions and allow consistent limiting of the VCO. This defines the RF operating level at in steady state. Another inherent advantage of a constant current is that the drain on the battery can more accurately be defined.

$$gm = \frac{Ic \cdot q}{k \cdot T} = \frac{Ic}{V_t} \tag{3.12}$$

In this VCO core, the bias is set by a current mirror connected to the emitter of the active device. This allows a known fixed current to flow through the active device and set the gm of the VCO. The alternative would be to use a high side device to source collector current

into the active device. The latter of the two methods is undesirable due to the large signal swings on the collector of the active device.

The disadvantage of this bias technique in a VCO is that because the output is pulled from the emitter the noise in the bias circuit will be directly added into the output spectrum. Therefore care must be taken to minimize this effect. The concern of the impedance of the current sink loading the oscillator is reduced by the fact that the relative impedance looking into the collector of a transistor is quite high. The final VCO bias network is shown in Appendix C and each part will be described in the subsequent sections.

3.3.1 Temperature Dependent Current Reference

Current references that are proportional to absolute temperature (PTAT) have been widely used to compensate for temperature based performance variation in integrated circuits. The PTAT circuit, shown in Figure 3.14, is used to generate a reference current to compensate for the temperature variation of the bandgap reference voltage covered in the next section. The combination of these circuits results in a reference voltage with good power supply and temperature characteristics.

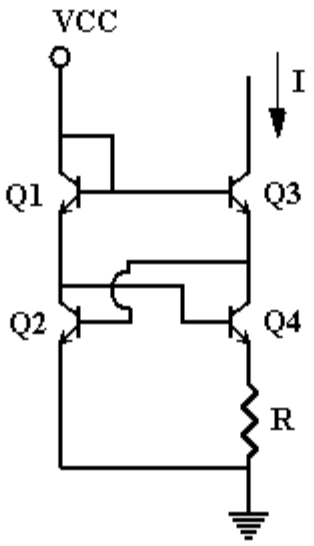


Figure 3.14: PTAT current reference generator

The temperature dependence of this circuit is based on a ratio of transistor emitter areas. This can be seen by analyzing the circuit with traditional techniques. Applying KVL to the circuit in Figure 3.14 gives the following equations:

$$VCC = Vbe_2 + Vbe_3 \tag{3.13}$$

$$VCC = Vbe_1 + Vbe_4 + I \cdot R \tag{3.14}$$

Equating the two yields an expression that relates the voltage drop across the resistor to the sum of the base emitter voltages.

$$I \cdot R = Vbe_3 + Vbe_2 - Vbe_1 - Vbe_4 \tag{3.15}$$

Then the approximate (forward bias) equation for the base-emitter voltage is expressed as a function of the thermal voltage (V_t), emitter current (*Ie*), and the saturation current (*Is*):

$$Vbe = V_t \cdot \ln(Ie / Is) \tag{3.16}$$

Where Vt is the thermal voltage from Equation 2.4, Ie is the emitter current, and Is is the saturation current defined in Equation 3.18

Now substituting and simplifying gives:

$$I = \frac{T}{R}\left(\frac{Is_1 \cdot Is_4}{Is_2 \cdot Is_3}\right) \tag{3.17}$$

$$Is = q \cdot A \cdot \eta_i^{\,2} \cdot \overline{D_n} / Q_B \tag{3.18}$$

Where q is the charge of an electron, A is the emitter area of the device, η_i is the intrinsic carrier concentration of silicon, $\overline{D_n}$ is the average effective electron base diffusion constant, and Q_B is the base doping density.

After substitution, it becomes apparent that all the constants cancel and the following expression remains:

$$I = \frac{T}{R}\left(\frac{A_1 \cdot A_4}{A_2 \cdot A_3}\right) \tag{3.19}$$

Where the subscript of each A term identifies which transistor with which it is associated.

Therefore, the resultant output current I is determined only by the ratio of the emitter areas in devices Q1 and Q4 as the value of the resistance R. This is a significant result since the current may effectively be expressed as a constant multiple of the temperature. The PTAT current can then be used to compensate the temperature variation in other circuits throughout the circuit.

3.3.2 Band Gap Voltage Reference

The availability of a supply independent reference voltage is often desirable in monolithic IC design. A VCO benefits in several ways from the stable reference. Most notably, bias references, that are constant with respect to supply, may be used to provide constant operating current. The advantage here is that the available power, transconductance, and relative impedance of active devices can be made more consistent over operating conditions.

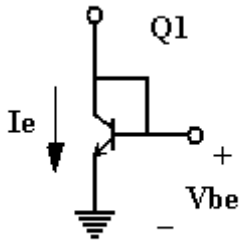


Figure 3.15: Diode connected bipolar transistor

The bandgap voltage is derived from the inherent P-N junction at the base-emitter of a diode connected bipolar transistor (depicted in Figure 3.15). The *Vbe* potential is a decreasing function of temperature and is described by rewriting Equation 3.18 to include the temperature dependence of the saturation current. The resulting equation is obtained from Equation 4.212 in Gray and Meyer [29,30]:

$$Is = C_1 \cdot A \cdot \eta_i^{\,2} \cdot \mu_n \cdot T \tag{3.20}$$

Where C_1 is a temperature independent constant, A is the area of the transistor and the other terms are defined as follows:

$$\mu_n = C_2 \cdot T^{-3/2} \tag{3.21}$$

$$\eta i^2 = C_3 \cdot T^3 \cdot e^{-V_{GO}/Vt} \tag{3.22}$$

$$V_{GO} = 1.11 \text{ V} \tag{3.23}$$

Where C_2 and *C_3 are temperature independent constants and V_{GO} is the bandgap voltage of silicon*

Substituting these into the equation for *Is*, combining the temperature independent constants[14] into a single term *C* and solving for *Vbe* results in Equation 3.24 that describes *Vbe* as a function of temperature.

$$Vbe = V_{GO} + \frac{k}{q} \cdot \ln\left(C \cdot \frac{Ie}{A}\right) \cdot T - n \cdot \frac{k}{q} \cdot \ln(T) \cdot T \tag{3.24}$$

This relation shows that *Vbe* has a constant, a linear, and a non-linear term. This complicates the goal of generating a voltage reference that is temperature independent. Fortunately, the

[14] The constants must be determined for the specific process used.

linear term dominates the equation and to a reasonable approximation the voltage has a slope of about –1.8 mV / ˚C.

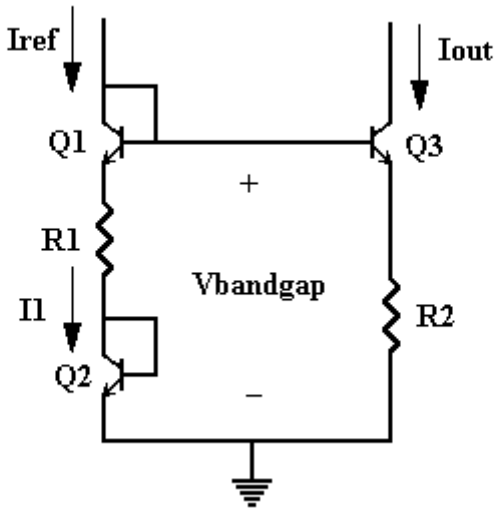


Figure 3.16: Bandgap circuit

With the temperature dependence of Vbe defined it may now be used in conjunction with other devices to counteract the voltage slope. Figure 3.16 is used to establish a temperature independent current *Iout.* Analysis begins by evaluating voltages across the diode-connected devices Q1 and Q2.

$$Vbe_1 + Vbe_2 + I1 \cdot R1 = Vbandgap \tag{3.25}$$

If it assumed that the base current in Q3 is much less than the current I1, and Q1 is well matched to Q2 then the equation may be simplified to:

$$2 \cdot Vbe + Iref \cdot R1 = Vbandgap \tag{3.26}$$

It has been established that the base-emitter voltage is a negative function of temperature. The bandgap reference uses a PTAT current with a positive temperature coefficient as a reference (*Iref*) to establish a positive function of temperature. The sum of these two as represented in Equation 3.26 results in a voltage reference that is much less dependent on temperature than uncompensated bipolar circuits. The resistor R1 is used to adjust the voltage characteristic of the bandgap and R2 helps maintain beta independence for Q3.

$$Iout = Is \cdot e^{(Vbandgap - Ie \cdot R2)/V_t} \tag{3.27}$$

The current *Iout* (eqn. 3.27) is established as a collector current through Q3 in Figure 3.16 and can be mirrored to several other parts of the circuit using PMOS current mirrors [29].

3.3.3 Buffer Amplifier Bias cell

Once a band gap reference has been established, it must be adequately isolated to prevent load-induced variation in the reference voltage. The circuit in Figure 3.17 provides DC bias to the base of the common emitter stage in the buffer amplifier. *Iref* is a reference current mirrored from the bandgap used to establish a bias voltage. This current sets the *Vbe* drops in Q1 and Q2 that essentially act as a degenerated voltage regulator. Using R1 and R2 for level adjustments, the voltage at the base Q3 is set with a reasonably supply independent reference. The result is that Q3 is now capable of supplying a supply independent current to the base of the buffer amp at the correct voltage at Vbias. The emitter-follower configured Q3 causes minimal loading on the circuit supplying *Iref*. Ignoring the effect of the

resistances, the transistors Q1 and Q2 add two *Vbe* voltages and Q3 drops one. The common emitter stage of the buffer amplifier will then see one *Vbe*, which is the desired result.

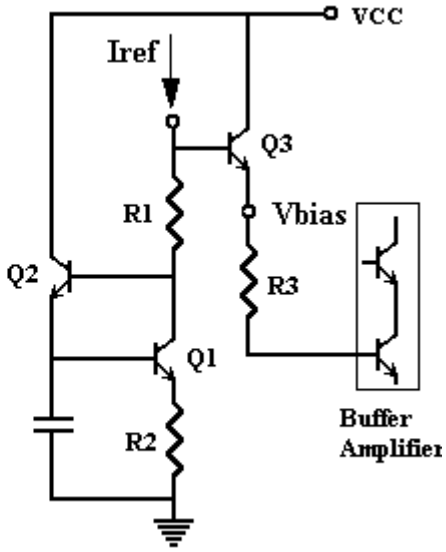


Figure 3.17: Voltage bias cell

Supply rejection is a term that describes the ability of a circuit to suppress unwanted signals on the supply line from leaking into critical signal paths. The circuit in Figure 3.17 exhibits good supply rejection because the only voltage bias for Q3 is referenced from a supply independent voltage source. High frequency voltage signals on *VCC* are attenuated with supply bypass capacitors external to the chip. Low frequency voltage signals on the collector of Q3 will not impact the buffer amplifier bias unless the supply voltage drops low enough to turn Q3 off. A minimum supply of 2.7V ensures that adequate bias levels are maintained.

Other biasing techniques[15] are less desirable because of their supply and temperature dependence. These techniques would tend to cause problems with proper circuit operation.

3.3.4 Current Mirror

Current mirrors are used in several places within the VCO presented. The primary function of this circuit is to provide an isolated representation of a desired reference current. It is often useful to have several independently scaled versions of a single accurate reference current. A basic PMOS current mirror Figure 3.18

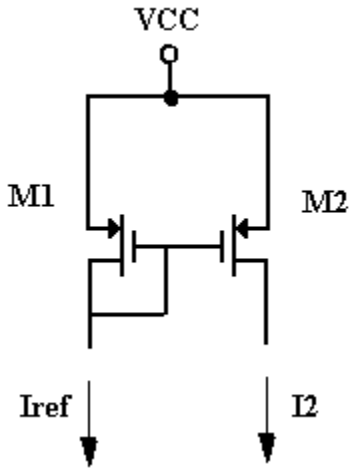


Figure 3.18: Generic PMOS current mirror

[15] Traditional techniques use voltage dividers referenced directly from the supply voltage. These techniques are less desirable in an IC design due to the availability of bandgap references.

The drain current in a MOSFET device is shown in Equation 3.28. Once the device geometry is fixed in a given process, and presuming there is adequate drain to source voltage, the current is defined by the gate-source potential relative to the threshold voltage. The other parameters in the equation are considered constants.

$$I_D = \frac{\mu \cdot C_{OX}}{2} \cdot \frac{W}{L} \cdot \left(V_{GS} - V_t\right)^2 \tag{3.28}$$

Where μ is the electron mobility in the channel,
C_{OX} is the gate oxide capacitance per unit area,
W is the width of the gate in μm, L is the length of the gate in μm,
V_{GS} is the gate to source voltage and V_t is the threshold voltage

If M1 and M2 in Figure 3.18 represent an ideal current mirror, the constants in Equation 3.28 are considered identical for both devices. In practice, well-matched transistors will have a negligibly small difference between the constants. Since M1 is connected as a diode, the gate to source voltage will be identical to M2. Therefore the current I2 should be nearly identical to Iref. Actual differences in the two currents result primarily from mismatch between M1 and M2. The issue of matching is treated in section 3.5.2. The versatility of this circuit is that current I2 may be easily scaled by changing the *W/L* ratio between M1 and M2. This generic form is used in the bias circuit (Appendix C) to mirror the reference current from the bandgap circuit to other parts. Bipolar devices are also used in current mirror applications. The principle is similar to MOS devices in that a reference current is forced through a device that is then scaled by the area of the mirrored bipolar device. The current is then scaled by the area because the two devices are connected to have the same V_{be}.

3.4 Packaging Parasitics

Accurate high frequency design typically includes the effect of parasitic elements into the simulation. This is even more critical in higher frequency applications where the impact of simply connecting the device to the outside world can dramatically change the circuit characteristics. The VCO presented in this thesis only operates up to 1 GHz. At these lower frequencies an approximation of bondwire and package impedance elements is adequate.

The basic interconnections in a conventional packaged IC, depicted in Figure 3.19, are shown as the bondwires and solder leads. The semiconductor die is attached to the package with conductive epoxy. Gold bondwires are used to connect the semiconductor die to the solder leads. The entire assembly is then encased in plastic mold compound. This robust enclosure allows the circuit to be soldered onto a printed circuit board with minimum damage to the semiconductor die. The plastic casing also prevents moisture from corroding the bonding pads on the die.

The primary parasitic impedance comes from the bond wires that connect the die to the package and the package solder leads. This appears as an inductance with some mutual coupling between adjacent wires. A much smaller parasitic is the capacitance associated with the metal bondpad on the semiconductor die. Secondary parasitics arise from the solder leads. These issues are treated in the next sections.

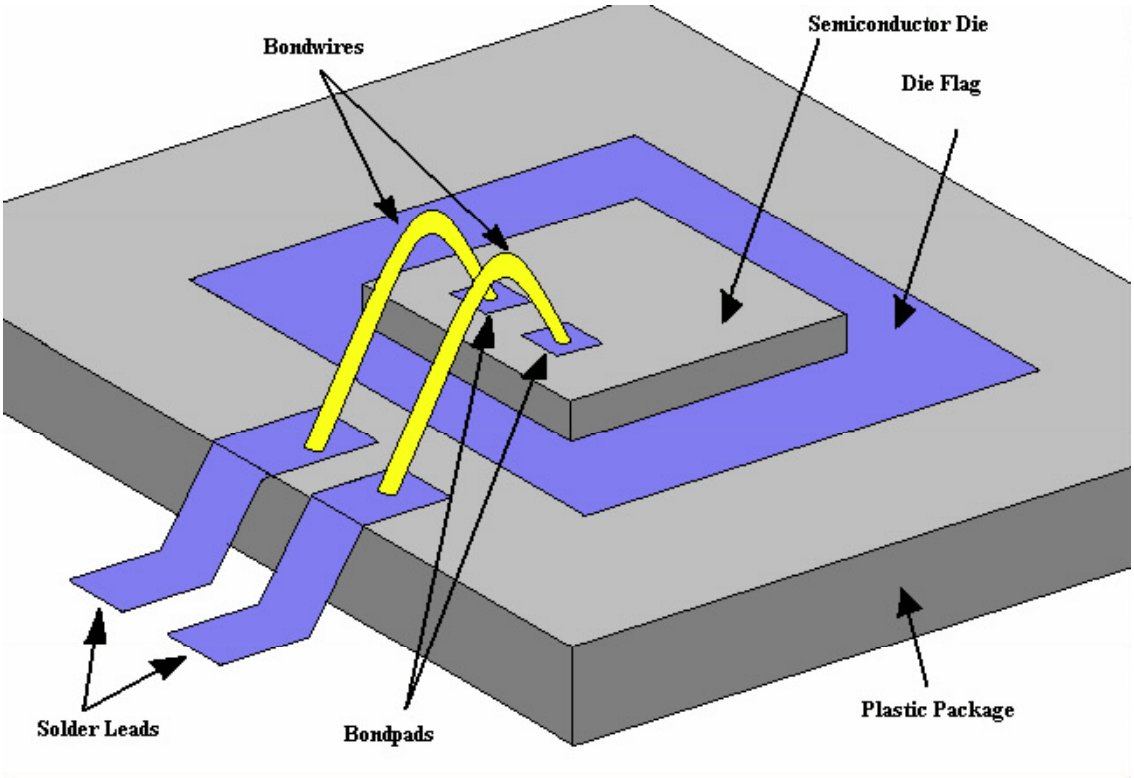


Figure 3.19: IC package interconnection

3.4.1 Bondwire Model

Bondwires are a significant part of the parasitic packaging model in high frequency designs. The impedance of the interconnection between the semiconductor die and the external package can have a dramatic impact on the performance of an RFIC. It is important to account for these impedances when attempting to accurately model a circuit. A first order approximation incorporates a model of the form in Figure 3.20. The model assumes that the bondwire may be viewed as a straight conductor with a circular cross section. This assumption is used to allow easier calculation of the self-inductance and series resistance in a single bondwire.

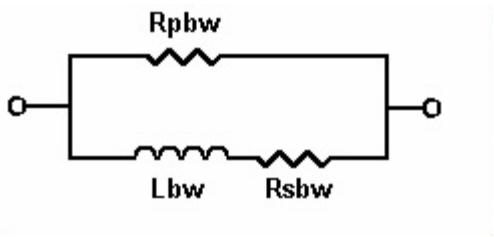


Figure 3.20: Bondwire self-inductance and parasitic resistance model

The resultant model consists of a series combination of an inductor L_{bw} and resistor R_{sbw} that are both in parallel with another resistor R_{pbw}. The series L and R model the DC resistance and intrinsic inductance of the bondwire while the parallel resistance is related to the Q of the inductor at higher frequencies. Grover provides the inductance portion of Equation 3.29 to approximate this self-inductance in a straight conductor [31].

$$L_{bw} = 0.002 \cdot \ell_{bw} \cdot \left[\ln\left(\frac{2 \cdot \ell_{bw}}{r_{bw}}\right) - \frac{3}{4} + \frac{\ell_{bw}}{r_{bw}} \right] \quad \text{and} \quad R_{pbw} = \frac{\left(2 \cdot \pi \cdot f \cdot L_{bw}\right)^2}{R_{sbw}} \tag{3.29}$$

Where l_{bw} is the length of the bondwire in centimeters, r is the radius of the wire in centimeters, f is the frequency in Hz, and R_{sbw} is calculated in Equation 3.30

The DC bondwire resistance is approximated in 3.30 using a conductive cylinder as a model.

$$R_{sbw} = \frac{\rho_{gold} \cdot \ell_{um}}{\pi \cdot \left(r_{bw}\right)^2 - \pi \cdot \left(r_{bw} - \delta_{bw}\right)^2} \tag{3.30}$$

Where, ℓum the length of the bondwire in micrometers, and δbw is the skin depth effect defined in Equation 3.31

$$\delta bw = \sqrt{\frac{\rho_{gold}}{\pi \cdot f \cdot \mu_o}} \tag{3.31}$$

Where ρ_{gold} is the resistivity of gold = 1.512μΩ/m, f is the frequency in Hertz, and μ_o is the permeability of free space.

The other component in bondwire modeling to be considered is the effect of mutual inductive coupling between adjacent bondwires. The circuit in Figure 3.21 is used to model this effect.

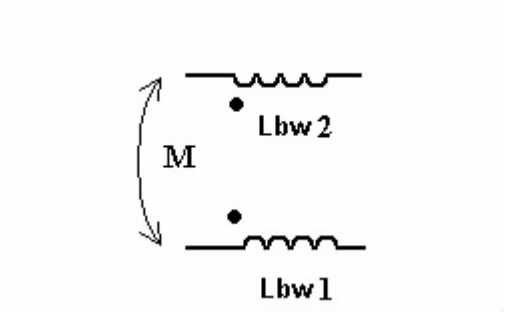


Figure 3.21: Bondwire mutual inductance model

The coefficient of mutual coupling *M* is calculated in Equation 3.32 [31].

$$M = 0.002 \cdot \ell_{bw} \cdot \left[\ln\left(\frac{\ell_{bw}}{d} + \sqrt{1 + \frac{\ell_{bw}^{\,2}}{d^2}} \right) - \sqrt{1 + \frac{d^2}{\ell_{bw}^{\,2}}} + \frac{d}{\ell_{bw}} \right] \tag{3.32}$$

Where d is the distance between the bondwires in micrometers.

The model presented thus far does not include the capacitive parasitics necessary to account for self-resonance effects in the bondwire. The capacitance between bondwires has been approximated to be in the tens of femtoFarads. The frequency at which these capacitance values would affect circuit performance was determined to be high enough above the operating frequency to ignore. A small capacitance is used in the model for this work but

does not appear to have a significant impact. The basic model has proven adequate to account for the real and imaginary impedances at the frequencies of interest.

3.4.2 Package Model

As is the case with bondwires, the package model is another implementation issue that is sometimes overlooked. The package model is provided by the manufacturer and only incorporates the parasitic elements associated with the metal lead frame of the package. The primary impedances resulting from the plastic package are the series inductance and resistance associated with each individual solder lead. Some pin-to-pin capacitance is also modeled in the manufacturer data sheets. A typical model for an MSOP type 8-pin plastic package of the variety used in this work is shown as part of the complete packaging parasitic model in Figure C3.

3.5 Physical Layout

The geography of the die layout is generally dictated by the pin configuration. In this design, the MSOP package used provides two rows of four pins. Figure 3.22 illustrates the MSOP package dimensions, relative die placement, and bonding configuration. The VCO layout, shown in Figure 3.23, depicts a bonding pad arrangement that roughly approximates the solder pin positions.

With the bonding pad arrangement defined, the functional circuit blocks are arranged in such a way as to try to prevent long traces meandering across the entire die. Therefore, it is desirable to group circuitry close to the bond pads where the associated signals are to be injected or extracted.

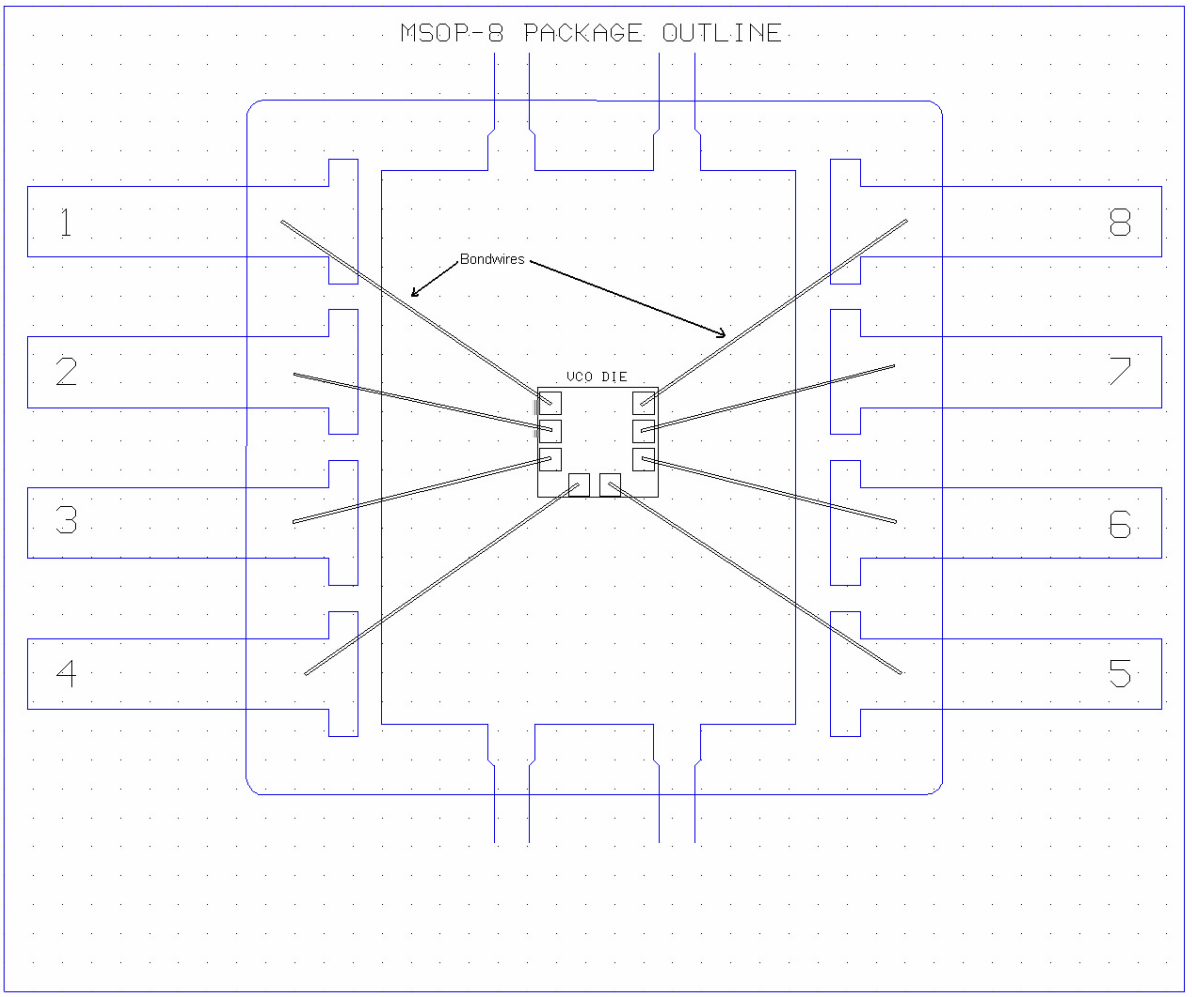


Figure 3.22: MSOP-8 package and bonding configuration

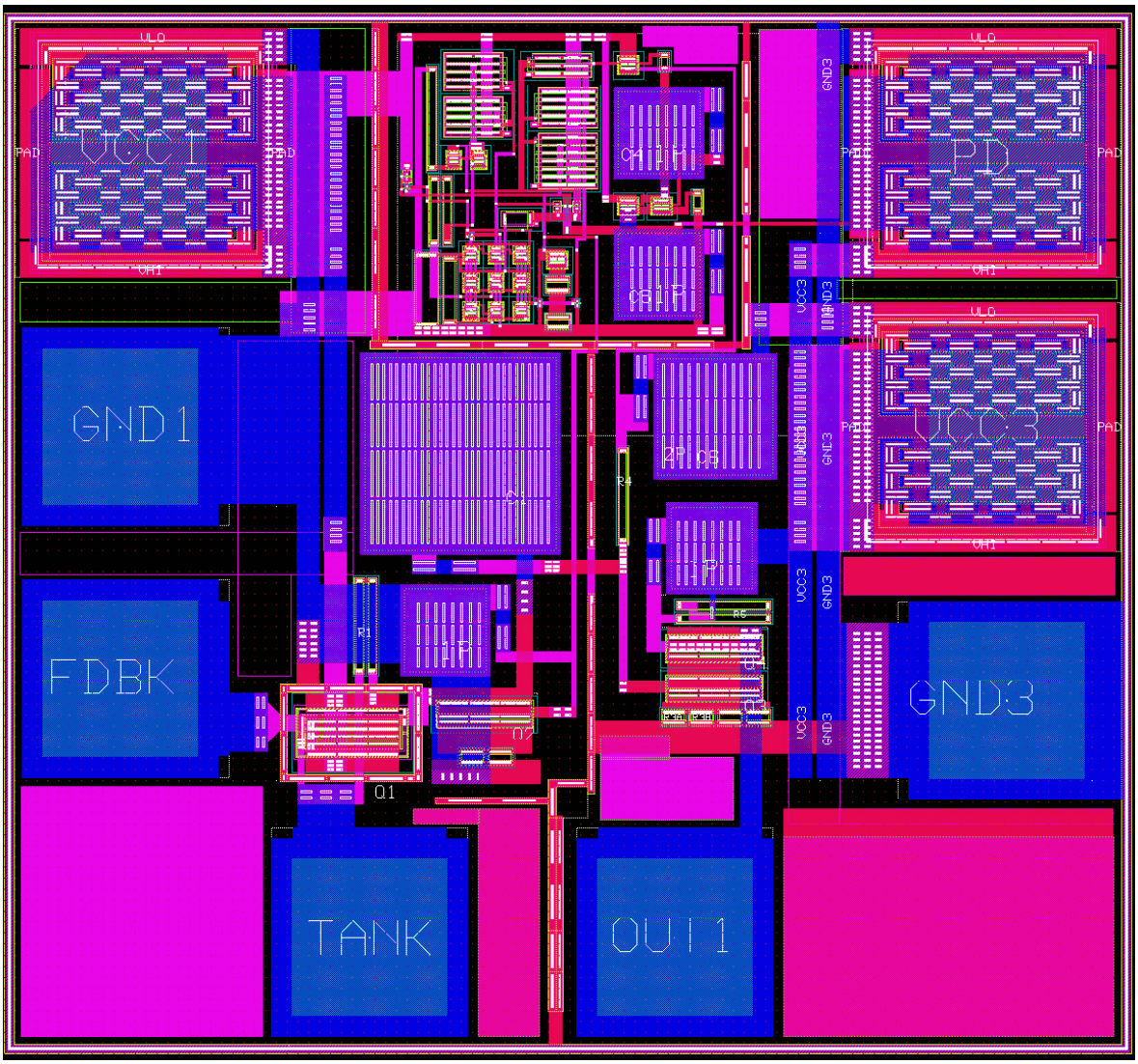


Figure 3.23: Complete die layout

The active VCO is placed at the bottom left of the layout. The VCO core transistor Q1 is surrounded by substrate contacts in an attempt to shield it from noise in surrounding circuits. Additionally, the device is physically separated from much of the other active circuits. The base and emitter of Q1 are connected to the bondpads labeled FDBK and TANK respectively. The bondpad labeled VCC1 feeds the DC into the collector of Q1 and the bondpad designated by GND1 is the ground for the VCO core and the bias circuits. The large

capacitor C1 in the center couples the energy from the VCO into the buffer amplifier located at the bottom right of the layout.

The bondpads labeled OUT1, VCC3, and GND3 are the collector, bias, and ground for the buffer amplifier respectively. The PD bondpad in the upper right corner of the layout is used to apply the power down signal in current saving mode. It is obvious that several of the bondpads (namely VCC1, PD, and VCC3) appear different from the other metal bondpads. The difference is that they contain the standard electrostatic discharge devices (ESD) for the process used. Although not covered in this work, adequate ESD protection of integrated circuits is a serious issue. It should suffice to note that static discharge protection, particularly in CMOS devices, should be carefully addressed in any design. The bondpads not protected by ESD structures in Figure3.23 are not connected directly to any sensitive MOS device nodes. Figure 3.24 shows a block diagram of the entire VCO circuit as a reference.

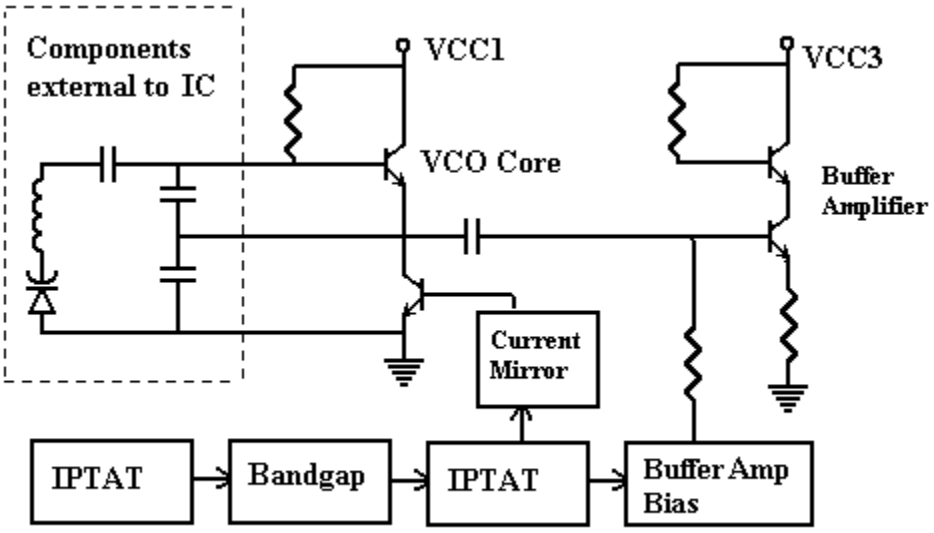


Figure 3.24: Simplified schematic of VCO, buffer, and bias

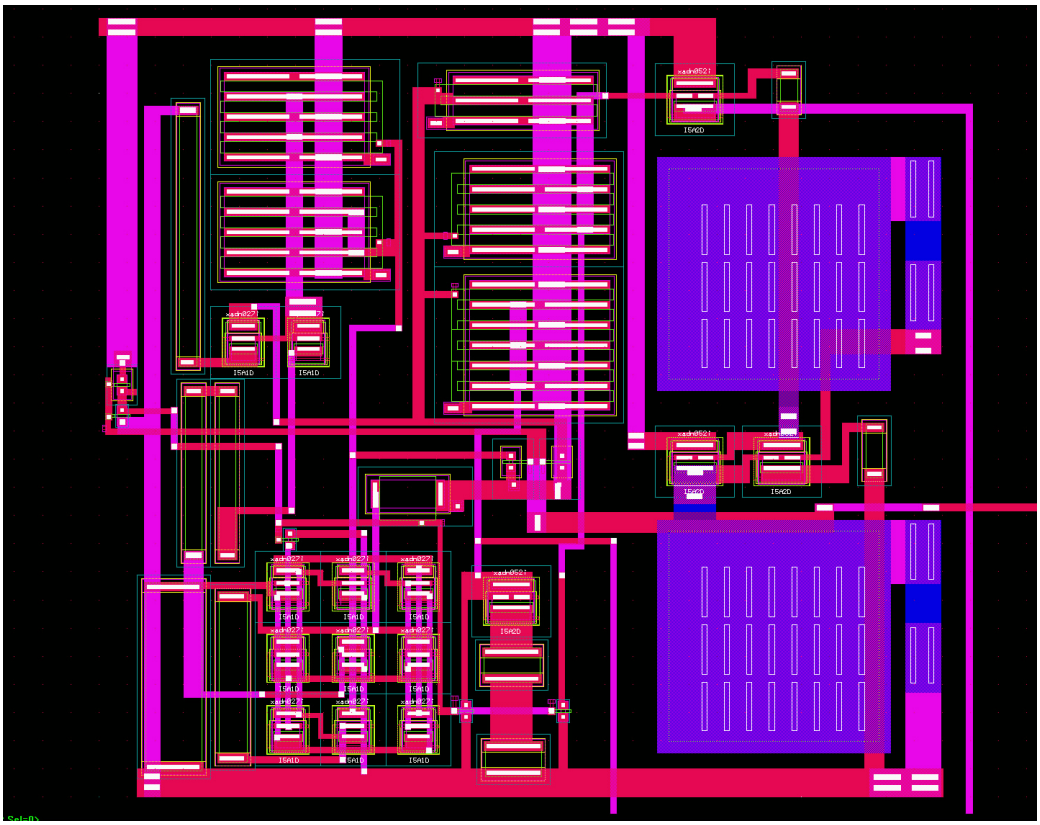


Figure 3.25: Bias network layout

Figure 3.25 depicts a close up of the bias network layout. The corresponding schematic drawing is shown in Figure C2. The top center of the layout shows the PMOS current mirrors used to distribute the reference currents to their respective circuits. Along the left side are the poly resistors used in setting bias currents. The center bottom of the figure is where the IPTAT bipolar devices are arranged in a common centroid[16] [32]. Two large capacitors are seen on the right of the layout and are used to decouple noise from one of the bias circuits.

[16] Common centroid layout is described in more detail in section 3.5.2 on device matching

3.5.1 Devices

The objective of this section is to provide an overview of the devices used in this work and to present some rationale for the device selections that were made. The intent is not to cover the specific model parameters or device physics for any particular component in great detail, but to summarize the salient features of the components used in the final design.

3.5.1.1 Bipolar Devices

In general the high frequency bipolar devices available in the IBM 5S process are all capable of producing an adequate VCO. The selection of a particular transistor is based on desired performance characteristics. The devices selected for use in the VCO design presented have superior noise performance and high frequency operation[17] as compared with other devices in the process. This performance enhancement is achieved by the foundry through optimization of transistor geometry. The devices are characterized by the foundry and the electrical parameters are available in the design kit models. Once a particular device geometry is selected, the device size is scaled to optimize particular operating characteristics.

[17] The VCO core and buffer circuits use devices with a peak *ft of 24GHz, w*here *ft* describes the frequency where the small signal current gain drops to 1.

Device size refers to the physical dimensions[18] of the transistor. This parameter determines several characteristics. Larger devices have higher maximum current handling, better β and *Vbe* matching between devices, and lower base spreading resistance. Good matching between devices is important for predictable circuit operation and bias conditions and lower base spreading resistance translates to lower phase noise. For these reasons, larger devices are more attractive.

3.5.1.2 MOS FETs

There is only one type of n-channel and one p-channel device available in the process used in this work. The only design choice for these devices is that of gate dimensions. The width and length (*W* and *L*) of a MOS gate is largely dependent on the application. Drain current, defined in 3.29, is a function of the gate geometry. The frequency response of a MOS device is also heavily dependent on device size. Equation 3.33 represents the maximum useable frequency of an NMOS device in terms of *W* and *L* [29].

$$f_t = \frac{1}{2\pi \cdot C_{gs}} \cdot \sqrt{2 \cdot \mu \cdot C_{OX} \frac{W}{L} \cdot I_D} \tag{3.33}$$

Where C_{gs} is the gate to source capacitance and the other parameters are defined in Equation 3.28.

[18] Size is typically described in terms of integer multiples of a nominal device area. A transistor with an area of two may be comprised of a single transistor which is twice the nominal area or two unity area transistors in parallel. A more precise description uses the exact dimensions of the device (e.g. Emitter area in square microns for a bipolar device)

Generally, narrower transistors are used for faster applications. The MOS devices used in this thesis are used almost exclusively in DC bias networks. Therefore, these devices do not require high frequency optimization.

The advantage of using these MOSFETs in biasing is that the insulating gate does not draw bias current. This eliminates design concerns related to base current in bipolar devices. Also, availability of the complementary N and P type devices allows maximum flexibility in the bias networks.

3.5.1.3 Poly Resistors

There are five types of resistors in the IBM process used for this work. The design differences are distinguished by sheet resistance and temperature coefficient. An undoped polysilicon resistor with a sheet resistivity[19] of 360 Ω/square is selected for use in the VCO design presented. This represents the second largest value for all available resistors and is desirable as it allows more efficient use of space in the layout than resistors with values in the tens of Ω/square. The polysilicon resistor selected was determined by the author to be the best trade between matching parameters, temperature, and voltage coefficient, and sheet resistivity.

[19] Sheet resistivity is a measure of the material resistance per unit area expressed in Ohms per square. A square is unitless since in a length/width calculation the units will always cancel.

3.5.1.4 MIM Caps

The Metal-Insulator-Metal capacitor structures available in the IBM 5S process are superior to other types of capacitors in that they use metalization for both capacitor plates. The alternative MOS capacitor structure uses a semiconducting layer for the plates. The MOS exhibits much higher capacitance per unit area (2.74 fF/μm^2 versus 0.7 fF/μm^2) but suffers from several drawbacks. The MOS capacitor has much lower Q due to parasitic losses in the semiconducting layers. Lower operating voltage and increased temperature dependence make the MOS less desirable than MIM capacitors.

3.5.2 Device Matching

The term device matching refers to the degree to which measured component values align between similar devices. Two semiconductor devices with identical geometry may have different electrical characteristics based on process variation[20] across the die material. This change in process across an IC can have an impact on circuit performance. This is especially true if the circuits like current mirrors and PTATs derive their accuracy from the assumption that two transistors have nearly identical electrical characteristics. Device beta is one example of a transistor parameter which can change across a given semiconductor die. Increasing the distance between identical devices increases the probability that they will have different values of beta. Therefore, it is desirable to place devices close together if close parameter matching is to be achieved. Other techniques such as common centroid layouts

[20] Variations result from limited resolution of the photolitography and non-uniform diffusion and implantation processes during fabrication.

help mitigate process gradient effects between critical devices. The common centroid employs a matrix of devices centered on a common point and interleaved in the x and y dimensions. This reduces mismatch for process gradients that change from one side of the die to the other [32].

Another consideration is that the size of some devices, particularly resistors and capacitors, directly affects the degree to which two equally sized components will have the same electrical value. As the physical size of a device increases, the magnitude of variations in fabrication or device constants tends to average out. One method for improving passive device matching is the use of interdigitation. The staggering of multiple series or parallel devices between one another aids in providing homogeneous device characteristics.

3.5.3 Isolation

ICs that carry significant RF currents, such as power amplifiers and VCOs, require substantial physical isolation between neighboring functional circuit blocks. The possibility of coupling energy from one circuit to another through the semi-conductive substrate or between overlapping metal lines can be reduced by appropriate layout techniques. The layout in this work makes use of a liberal application of substrate contacts. The substrate contact provides an electrical connection between metal layers and the bulk wafer material known as the substrate. The contact has at least one signal level metal that allows a connection to a local “low-noise” ground and forces the potential of the substrate in the

vicinity of the contact to a low potential. This technique helps to prevent any stray substrate current from leaking to other parts of the circuit.

Other RF processes employ trench mechanisms[21] to provide an isolation barrier to prevent cross-talk between adjacent RF circuits. Although not available on the process presented in this work, deep trench isolation is becoming more popular in RF silicon processes

[21] A trench is made of an insulating material which is implanted down into the substrate to provide local circuit isolation on a semiconductor die.

4 Simulation

The simulation results are provided for DC, small signal, and large signal (time domain and harmonic balance) simulations. The majority of the design, including the initial negative resistance and DC simulations, is performed in MicroSim Pspice version 8.0. The Hewlett Packard[22] Advanced Design System (ADS) simulation suite was primarily used to verify the phase noise performance and steady state output spectrum. The harmonic balance capability in ADS provides a much faster approximation of these quantities than the equivalent transient simulation in PSpice. The phase noise measurement in particular is more accurate because of the ability of ADS to perform non-linear noise analysis.

4.1 PSpice DC Simulations

A good starting point in any circuit simulation is the DC operating point. In this design there are two main paths for current drain as shown in Figure 4.1. The VCO is represented by the hierarchical block HS1. And, although they do not play an important role in DC simulations, the bondwire, package parasitic, and device models are imbedded in the symbolic box labeled HS1[23]. The rest of the components, including the varactor, are external to the design

[22] ADS is now supported by Agilent Technologies.
[23] The entire hierarchical schematic represented by the HS1 block is shown in Appendix C

presented and are represented with standard circuit elements. The DC voltage supply is shown as V1. In Figure 4.1 the two supplies (VCC1 and VCC3) have been connected so that the supply voltage can be varied as they would in a battery operated environment. The objective for the supply current was to maintain less than 10mA total current drain for a supply voltage from 2.7 to 3.6 V and over a temperature range from –27 to 85 ˚C.

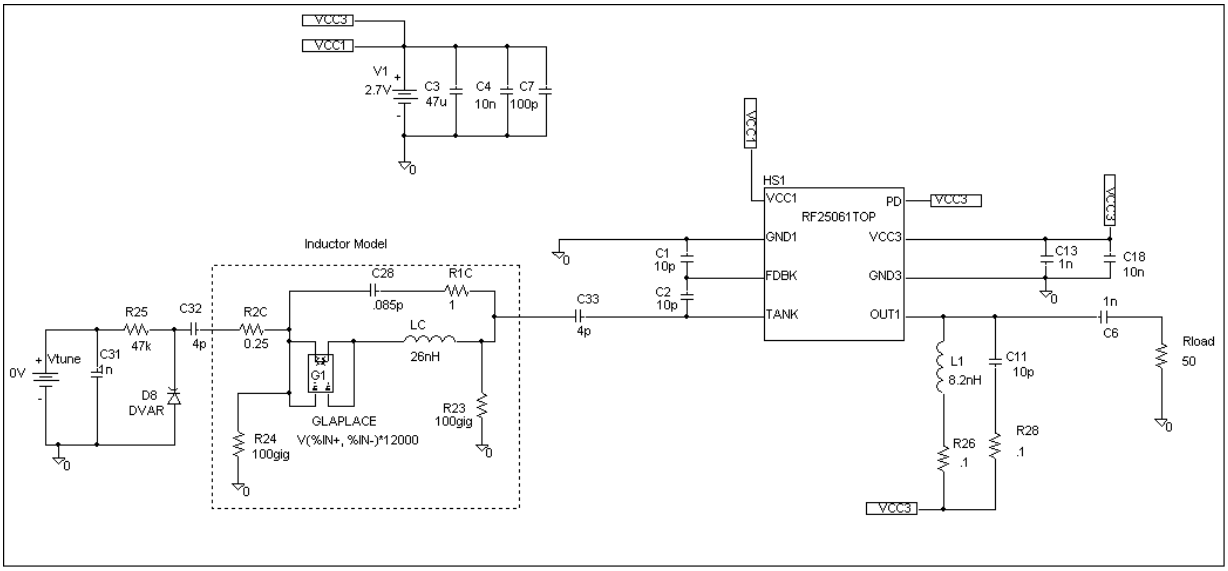


Figure 4.1: PSpice schematic used for DC simulations

The limitation on total current constrains how much current each circuit block can consume. The partition for current is set at 4.3 mA in the VCO core and 4.3 mA in the cascode buffer leaving about 2.4 mA for the bias circuitry. Some margin needs to be built into the total current consumption for variation in supply voltage and temperature.

PSpice simulations were used to optimize the quiescent operating point and evaluate the effectiveness of the temperature compensation network. The simulation result for the total

bias current versus DC supply voltage is shown in Figure 4.2. This plot represents the sum of all DC supply currents plotted as a function of a single supply voltage and swept for temperatures of –25, 27, and 85 ºC. Simulation results indicate approximately 3% change in DC current over the supply voltage range at a given temperature. The total error in current is about 10% over voltage and temperature. This is within acceptable limits to maintain bias levels over environmental extremes of temperature and battery voltage. The maximum current is maintained below the 10 mA limit. DC shifts resulting from large-signal rectification are not included in the data in Figure 4.2. Errors in bias current caused by large signal effects are minimized by the bias topology.

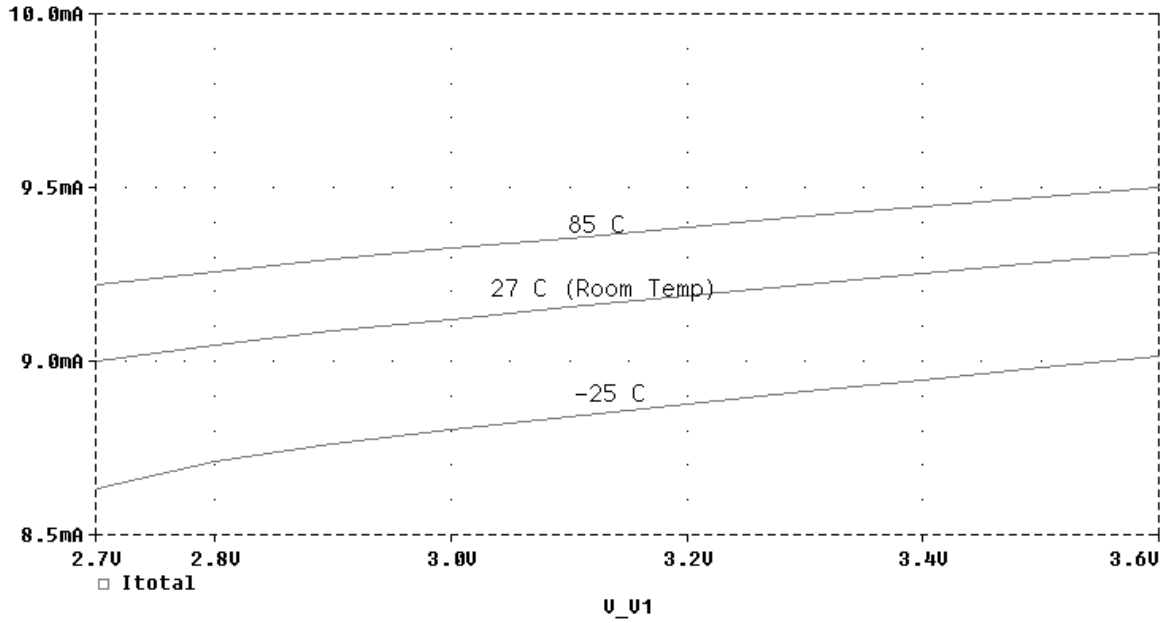


Figure 4.2: Simulated DC bias current versus temperature and supply voltage

4.2 PSpice Negative Resistance Simulation

The first simulation in PSpice after the DC bias is a negative resistance approximation. Initially, ideal DC voltage and current sources are assumed in an effort to minimize the impact of secondary biasing effects on high frequency performance. Ideal sources are also more easily adjusted to optimize startup conditions. For this section, the input impedance of the VCO core and resonator circuits are evaluated separately and plotted on the same graph as a function of varactor tuning voltage. This provides insight into the frequency at which the circuit will tend to oscillate as well as the relative impedances of the two circuits. The following values were used as a starting point for iterative simulations: $C1=C2=10\text{pF}$, f=frequency=560 MHz, and Ic=4.37 mA. The effective negative resistance is calculated in Equation 4.2

$$Rs = -\frac{gm}{\omega^2 \cdot C1 \cdot C2} = -\frac{(Ic/V_t)}{(2\pi \cdot f)^2 \cdot C1 \cdot C2} \tag{4.1}$$

$$Rs = -\frac{(4.37mA/0.026mV)}{(2\pi \cdot 560MHz)^2 \cdot 10\,pF \cdot 10\,pF} \approx -136\Omega \tag{4.2}$$

A comparison of the Rhode analysis (Section 3.1.2.2) to simulated results shows some discrepancy. Figure 4.2 reveals that the magnitude of the impedance is different from the calculated value by almost a factor of two. This may be explained by the fact the Rohde

analysis presumes that the circuit is only biased by perfect current source and has no other loading impedances associated with it. For the purposes of a first order approximation this result works well and does accurately represent the general trend of the negative impedance as a function of frequency. Also, it is expected that some error will be compensated by empirical adjustment of the resonator.

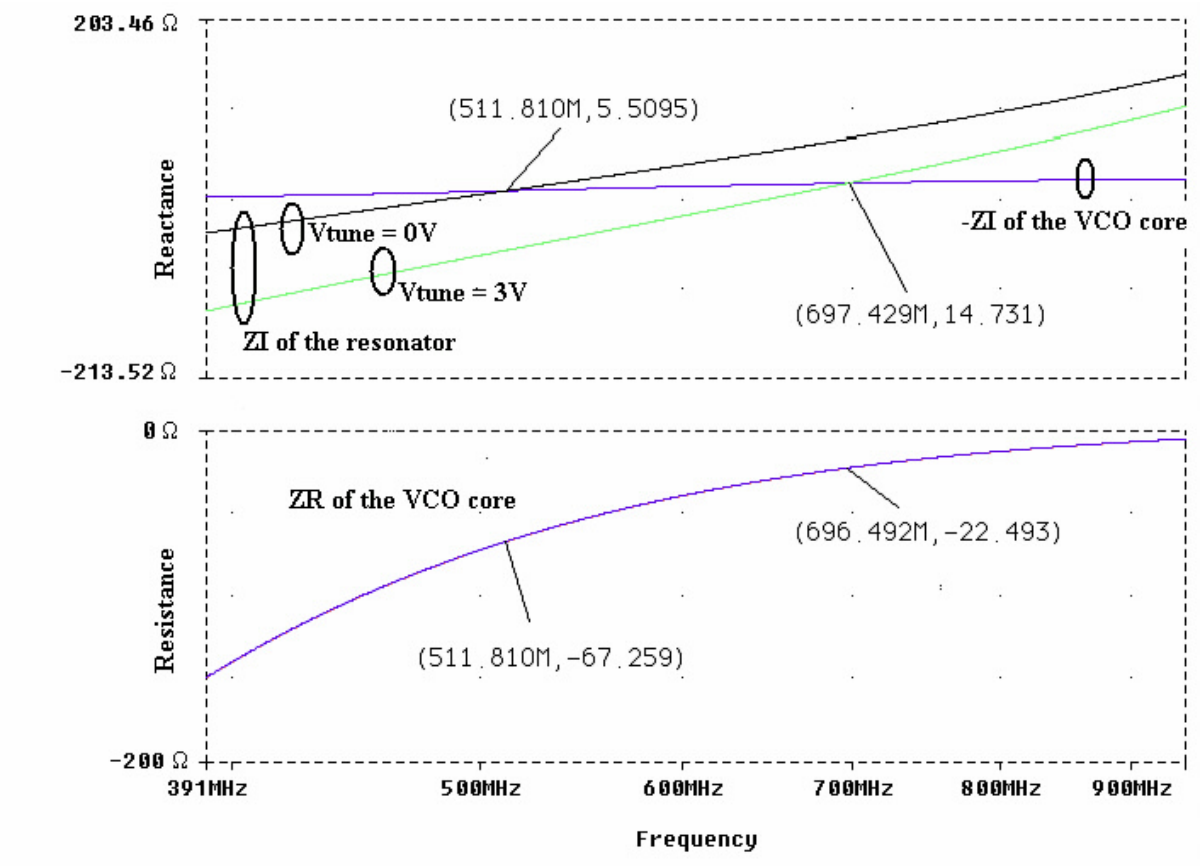


Figure 4.3: Resonator and active VCO impedances

The upper plot in Figure 4.3 depicts the imaginary impedance component of the resonator for 0 and 3V Vtune voltages on the same graph with the negative imaginary impedance looking

into the active device. The impedance intersections are plotted for limits of Vtune applied to the varactor diode in order to determine the approximate limits of the tune range. This information represents a confirmation that the input to the active device does indeed present a negative real. It also shows that there is a unique solution for the unstable system and that there are no alternative stable regions that could prevent oscillation.

The lower plot of the simulation data in Figure 4.3 shows the magnitude of the negative real impedance of the active circuit versus frequency. It should be noted here that this data is obtained from a small-signal assumption in an AC simulation. When the circuit undergoes oscillation the increasing signal level will tend to cause the input impedance to shift and as a result will change the frequency tuning range. Therefore this simulation is used only as a first order approximation to the actual frequency of oscillation that may be expected under normal operating conditions. Large signal assumptions are made in the next sections and are used in simulation to predict the steady state parameters.

A separate negative resistance simulation was performed in PSpice to obtain an approximation of the S-parameters of the active device. Figure 4.4 shows the simulation circuit used to approximate S11.

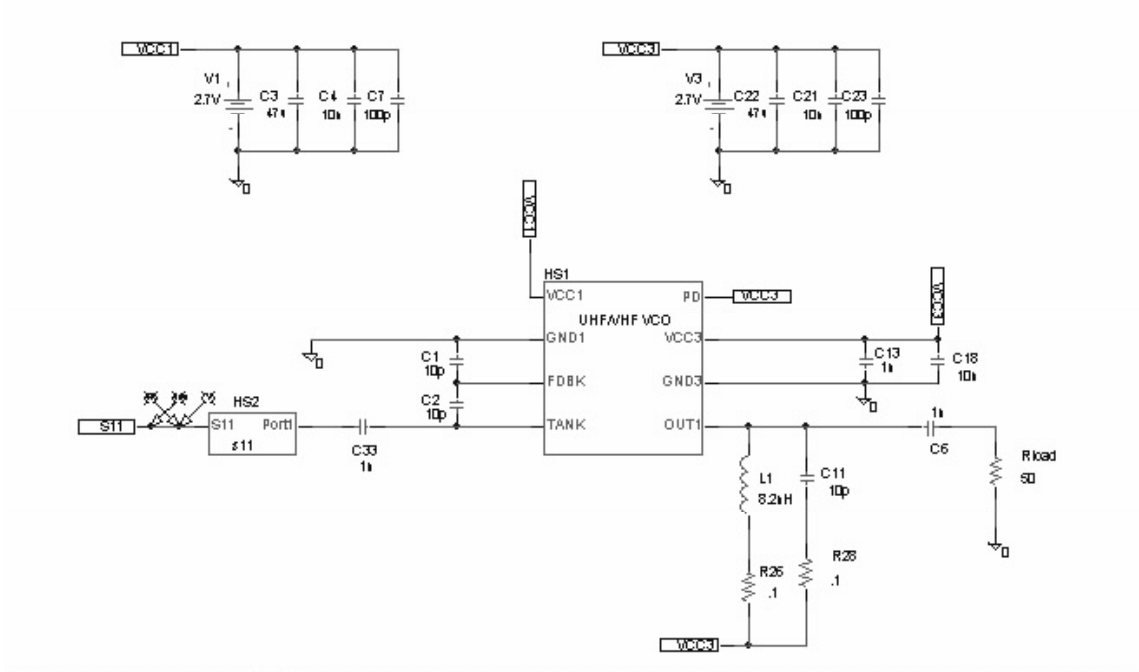


Figure 4.4: PSpice VCO S11 simulation

The S11 block in the simulation is essentially a small signal AC source with some arithmetic modifications. Equation 4.3 shows the expression for S11 as a mathematical relation between the impedance to be determined (Z_L) and the characteristic impedance (Z_O).

$$S11 = 2 \cdot \left(\frac{Z_L}{Z_L + Z_O} \right) - 1 \tag{4.3}$$

The block in Figure 4.5 presents a unity valued voltage source and measures the impedance at port 1 voltage across a 1 Ω resistor. The voltage at port 1, presented through a 50 Ω source resistance, is multiplied by 2 in the ideal voltage-to-voltage converter E1. The voltage is reduced 1V by the voltage source V2 and is then imposed across the resistor R2. The resulting voltage at the S11 node is equivalent to the expression in Equation 4.3. This is one

technique for measuring small signal S-Parameters in a Spice simulator that lacks the pre-defined functions of more sophisticated RF simulation software [33].

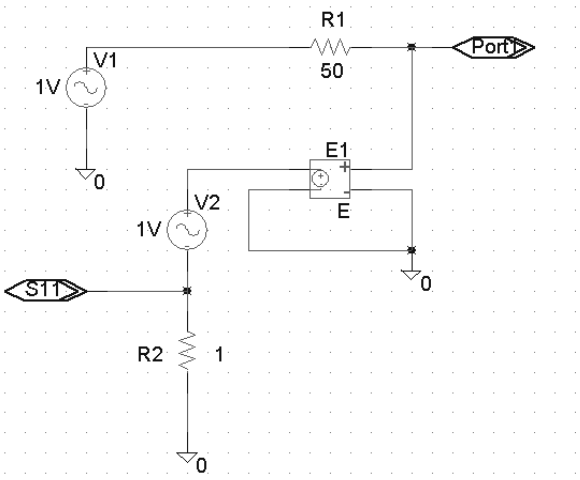


Figure 4.5: PSpice S-Parameter simulation block

The result of the PSpice S-Parameter simulation is shown in Figure 4.6. The plot confirms that the magnitude of S11 presented by the VCO core is greater than 1 and has the potential to oscillate. The prior simulation corroborates this result. S11 magnitude and phase information are also determined in this simulation for comparison against measured results.

A drawback of this method is that only small signal information may be obtained. To date, PSpice does not have the capability to perform swept large signal simulations[24]. This feature is desirable in VCO design. An additional shortcoming is that there is no convenient way to plot the S-parameter data on a Smith chart.

[24] PSpice is, at the time of this writing, still much less expensive than other more sophisticated simulation software. The comparison is made here to show the degree of accuracy improvement.

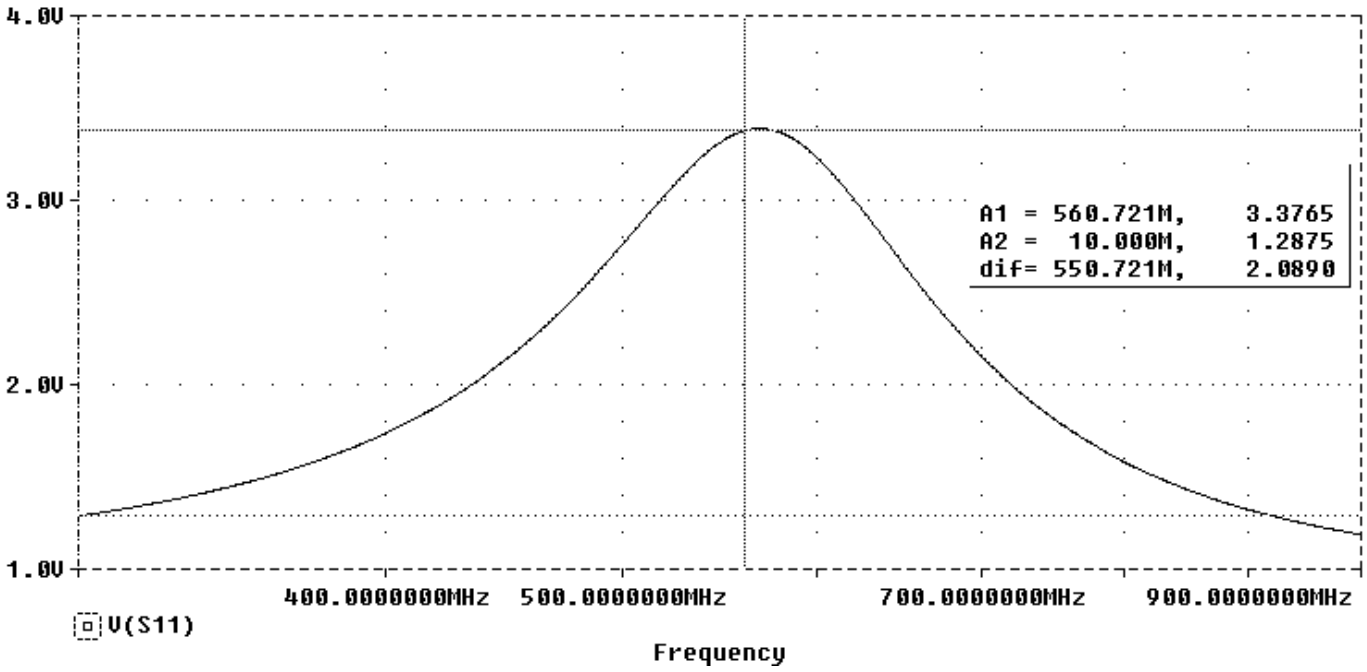


Figure 4.6: PSpice S11 simulation

4.3 PSpice Time Domain Simulations

Obtaining results from a transient oscillator simulation is often a challenge. One of the biggest hurdles is getting the simulation circuit to start oscillating. The simulated noise energy generated by passive components and startup transients may not be of a large enough level or at the appropriate frequency to begin signal buildup. One method to force an oscillatory state is shown in the circuit of Figure 4.7. This technique employs a current pulse injected between the VCO core and resonator. The pulse contains enough energy at the tank resonant frequency to act as a signal catalyst. The resulting signal approximates the noise currents that would be present in a real circuit.

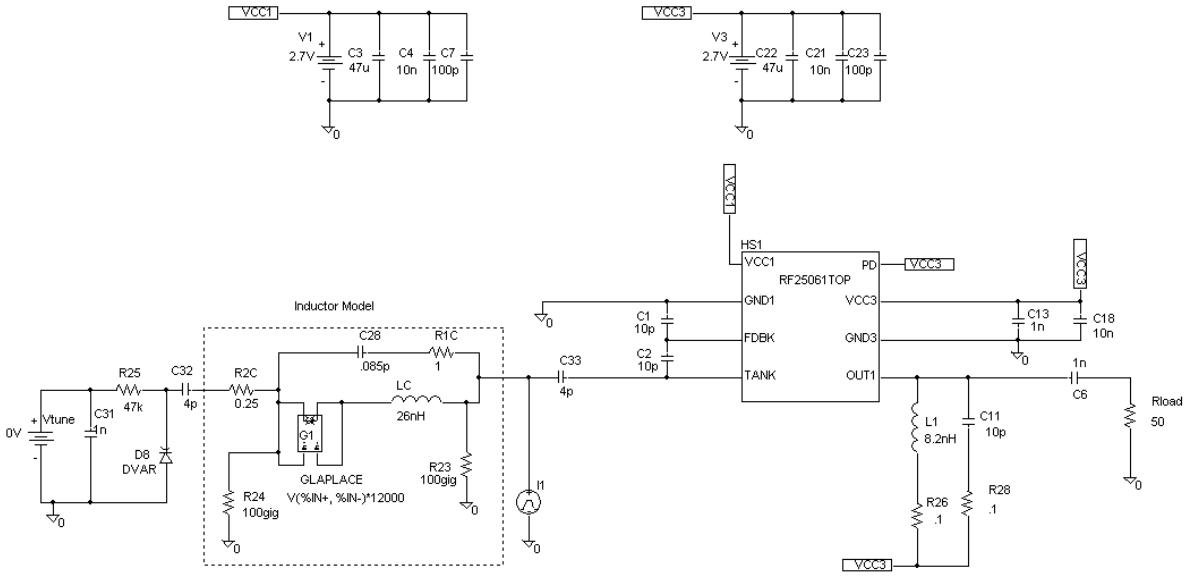


Figure 4.7: PSpice time domain simulation schematic (I1 is the start-up current)

The steady state[25] transient voltage across the 50 Ω load (designated as R3 in the time domain schematic) is shown in Figure 4.7. The time domain waveform in Figure 4.8 exhibits sustained oscillation at a frequency of 552 MHz with some distortion resulting from harmonic content. Figure 4.9 displays the spectrum of the signal including the second and third harmonics. The peak fundamental voltage across R3 is simulated to be 253.5 mV. This represents a power of –1.9 dBm. These results are consistent with the expected level of oscillation for this design.

[25] Startup conditions are not considered in this simulation due to the artificially fast method used to begin oscillation.

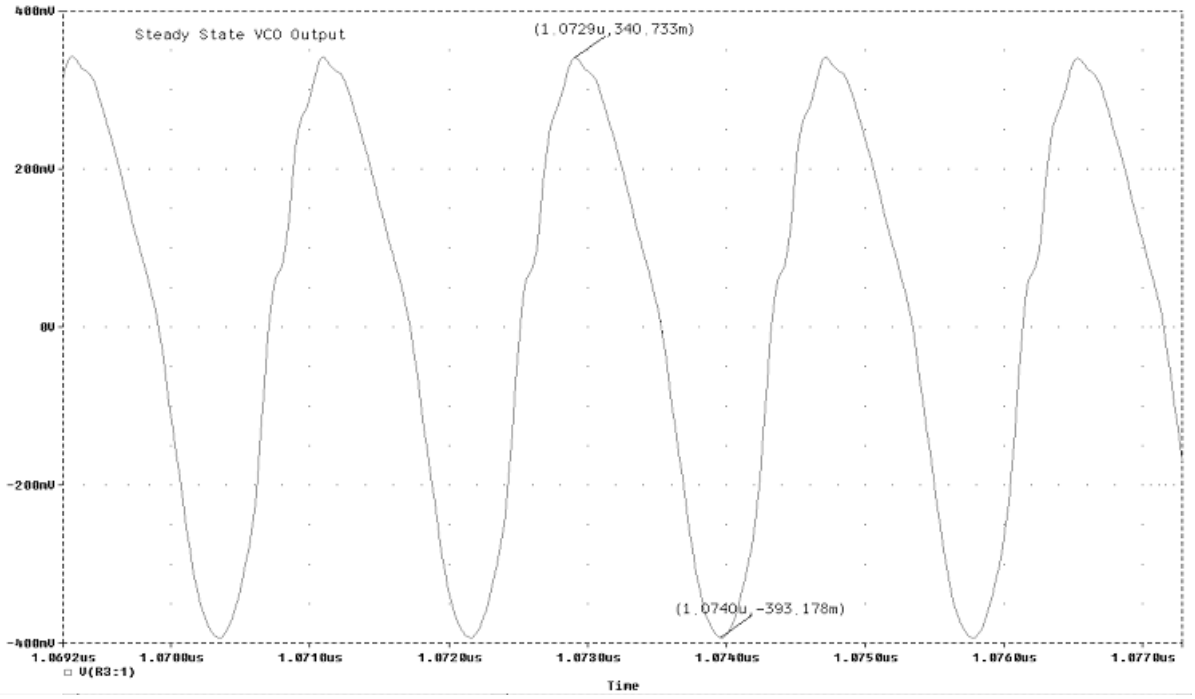


Figure 4.8: PSpice time domain output

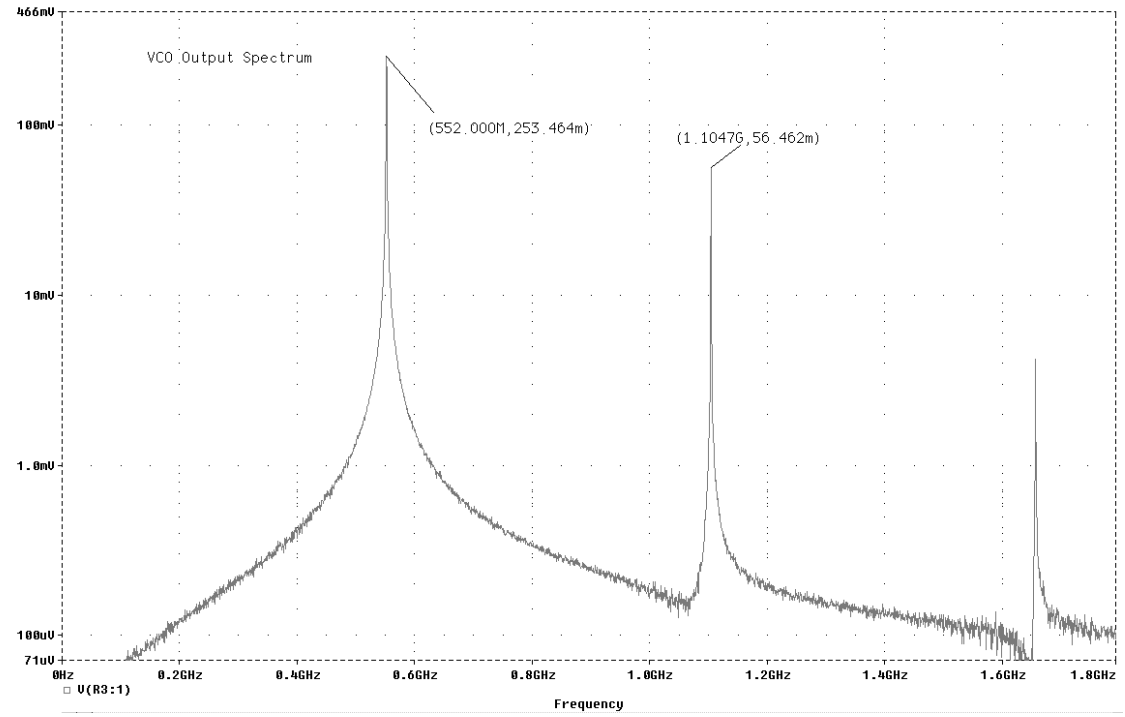


Figure 4.9: PSpice output spectrum

4.4 PSpice Phase Noise Simulation

The goal of the simulation in this section was not to obtain a highly accurate phase noise but rather to get an approximation for comparison with other data. Part of the relaxed accuracy requirement is based on the simulation software. The version of Pspice used in this work does not include a convenient method to simulate nonlinear noise. Therefore, any phase noise simulation then must be derived from the basic noise sources in a small signal frequency sweep. The actual simulation schematic is almost identical to the time domain setup in Figure 4.7 except that it is a small signal noise simulation. The Leeson style phase noise is then calculated using Equation 2.12.

Several large signal parameters are required in order to solve the phase noise equation. The oscillator output level (*Posc*) is determined in the time domain simulation in section 4.3. The tuning sensitivity (*Kvco*) is obtained in section 4.2. For simplicity, *Kvco* is approximated as a constant MHz/V slope between the tuning endpoints of 511.8 and 695.5 MHz. The loaded resonator Q (*Ql)* is found in yet another simulation not shown here. And, the small signal noise power generated by the active devices (*No*) is estimated in the phase noise simulation. All the quantities mentioned, except *No*, are represented as constants. These constants are inserted into the schematic as AC voltage sources with the magnitude of the desired quantity. The calculated phase noise is then plotted in dBc versus the offset frequency from the carrier.

An important consequence of approximating phase noise by this method is degraded accuracy. The non-linear contributions to phase noise are not represented by the frequency conversion mechanisms but rather by the equation constants. Absent from this simulation is the effect of the variation in tuning sensitivity on the overall output spectrum. This is more prevalent when the VCO is tuned to a steeper point on the frequency versus tuning voltage curve [15]. Also absent from this simulation is the effect of the nonlinear loading of the active device which occurs as a result of limiting and transconductance reduction.

The constants used in calculating the plot shown in Figure 4.10 are listed as follows:

$$Kvco = 66.88 \text{ MHz/V}, \; fo = 560 \text{ MHz}, \; Ql = 15, \; fc = 10 \text{ kHz}, \; Posc = 642.6 \; \mu\text{W}$$

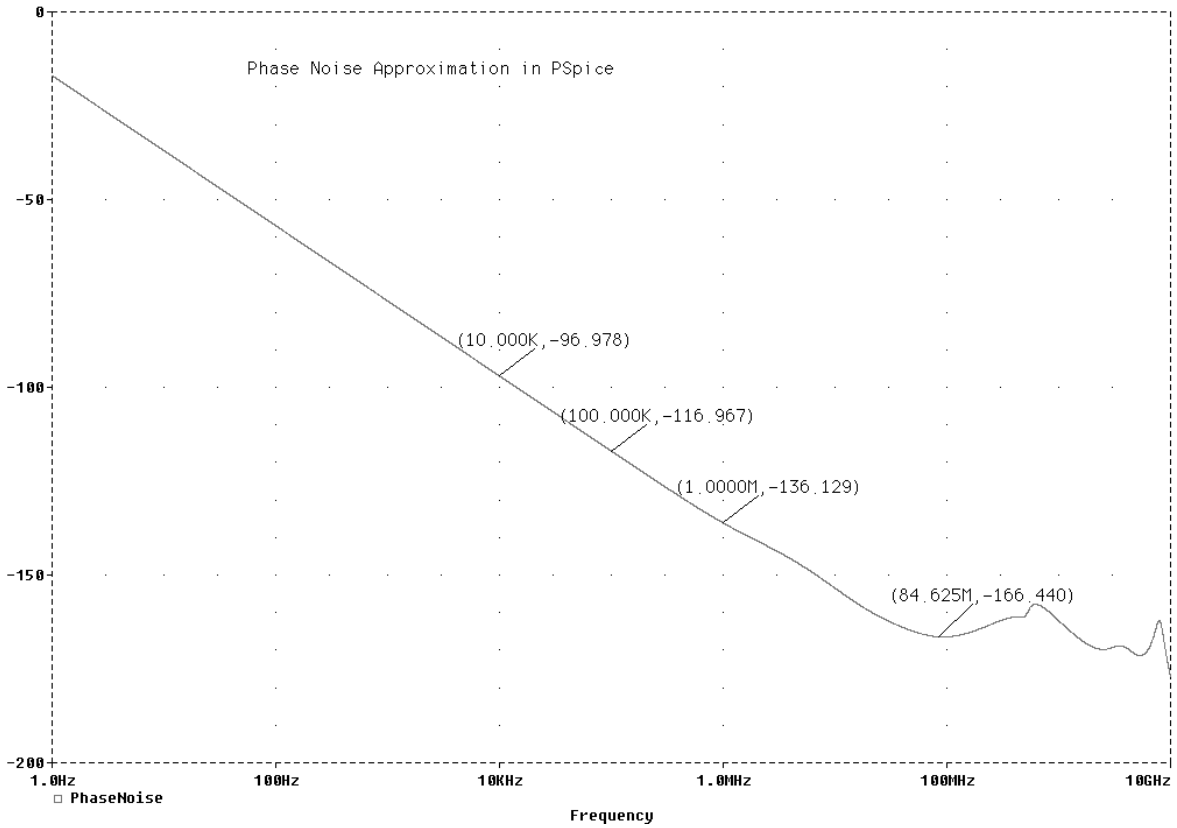


Figure 4.10: PSpice phase noise simulation

This simulation is a linear approximation to an inherently non-linear process and is only intended to provide a basis for comparison. The resultant phase noise plot clearly shows the expected 1/f characteristic of noise power as a function of offset frequency. At 10 kHz the phase noise is –96.98 dBc/Hz . At roughly 84 MHz the slope flattens and the thermal noise floor is established in the –166 dBc/Hz range.

4.5 ADS Output Spectrum Simulation

The ADS software was used primarily to simulate harmonic performance and phase noise. Large and small signal S-parameters were also simulated so that the models could be verified against measured results. The advantage of ADS over PSpice is that many of the idiosyncrasies of oscillator design are built into the simulator. Oscillator simulation begins by inserting a component called an "OscPort" into the circuit between the active VCO core and the resonator. When the harmonic balance simulation begins, the OscPort converts itself into a short circuit at all harmonic frequencies except the fundamental. This part of the simulation is an open loop evaluation[26] of the frequency at which the loop gain is greater than one. The simulator then uses this information as a starting point for the non-linear simulation. The non-linear harmonic balance simulator is required to account for the limiting and subsequent gain reduction of the oscillator in steady-state. Harmonic balance is an iterative search algorithm. It is based on the premise that for a given sinusoidal excitation there exists a steady-state solution that can be approximated by a finite Fourier series. In the

[26] Note that this is essentially an automated version of the PSpice simulation in section 4.2.

actual simulation, the circuit node voltages take on a set of amplitudes and phases for every frequency component. The currents flowing out of the nodes into linear elements are determined by a frequency-domain linear analysis. The currents flowing into non-linear elements are determined in the time-domain. Fourier analysis is employed to transform from the time to the frequency-domain. Kirchoff's Current Law (KCL) requires that all currents flowing into and out of a given node should sum to zero. The harmonic balance simulation performs KCL on the frequency-domain representation of the currents. The degree to which KCL is violated in a given iteration of the analysis represents an error function [34]. The simulation is complete when the error function is reduced to within an acceptable limit.

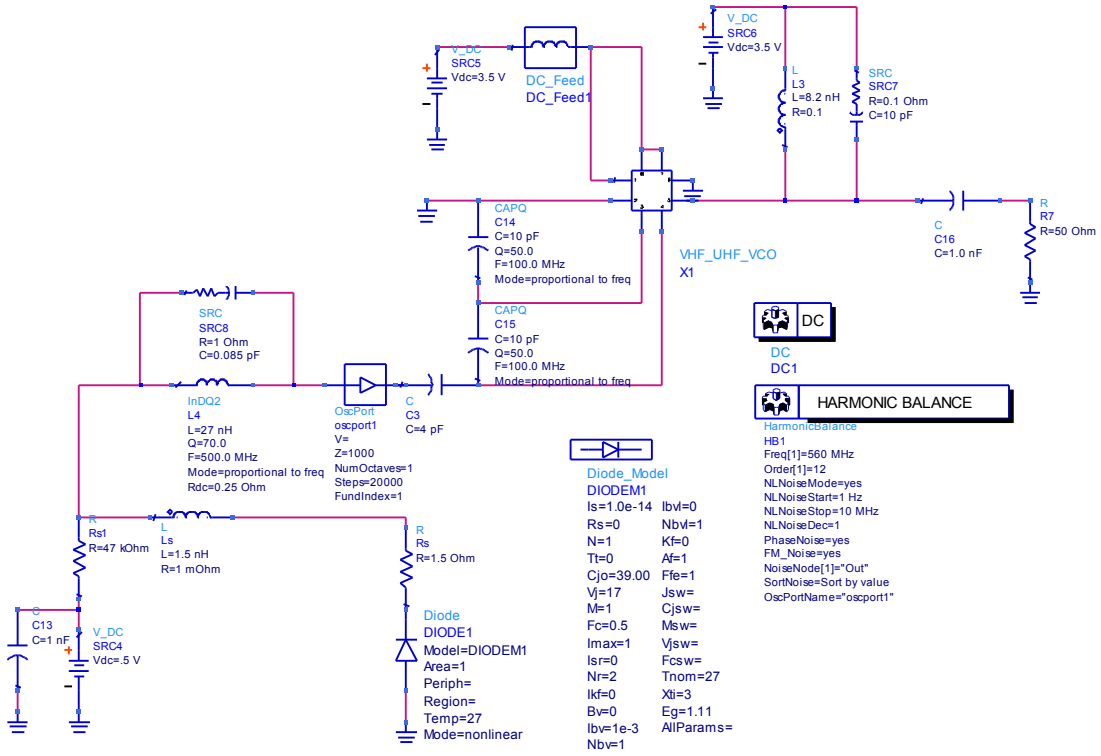


Figure 4.11: ADS output spectrum simulation schematic

The simulation result in Figure 4.12 expresses the power in individual harmonic components in dBm. A harmonic index ("harm index") is used to identify the frequency of the component instead of the actual frequency in Hz. Table 4.1 gives the data from Figure 4.12 in a tabular format with the actual frequency reference of each harmonic index. As shown in the data, the power delivered to the 50Ω load at the fundamental frequency is –4.8 dBm. This is about 3dB lower than that predicted in the PSpice simulation. This deviation is reasonable based on the differences between the two simulations.

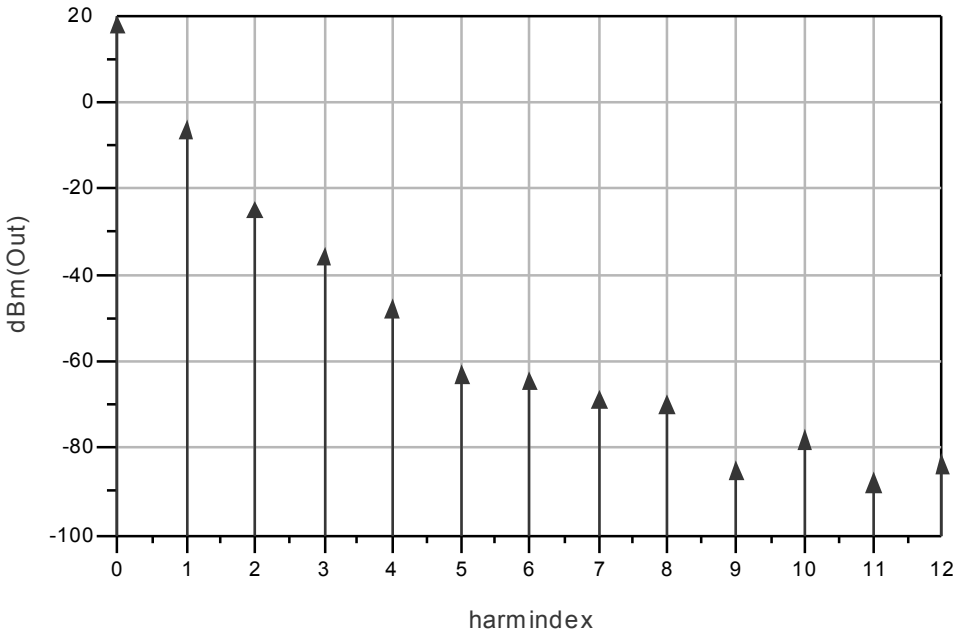


Figure 4.12: ADS spectrum magnitude plot

harmindex	freq	dBm(Out)
0	0.0000 Hz	19.542
1	572.2MHz	-4.816
2	1.144GHz	-23.489
3	1.716GHz	-34.374
4	2.289GHz	-46.385
5	2.861GHz	-61.478
6	3.433GHz	-63.270
7	4.005GHz	-67.449
8	4.577GHz	-68.576
9	5.149GHz	-83.680
10	5.722GHz	-76.524
11	6.294GHz	-86.722

Table 4.1: ADS spectrum magnitude data

4.6 ADS Phase Noise Simulation

The phase noise simulation in ADS is theoretically better than the PSpice equivalent described in Section 4.4. This is because phase noise data in ADS is generated using a large signal simulation that includes non-linear effects. These effects include: normal frequency conversion, amplitude-noise-to-frequency-noise conversion, frequency translation of noise caused by component nonlinearities in the presence of large-signal oscillator signals, upconverted flicker noise, and noise power effects resulting from DC bias shifts.

The data in Figure 4.13 and Table 4.2 represents the phase noise results obtained from the ADS harmonic balance simulation. At 10 kHz the phase noise was determined to be –91.32

dBc/Hz. This is about 6.6dB worse than that predicted by the PSpice simulation. Based on the additional accuracy afforded by the ADS some degree of phase noise performance is expected. Several additional non-linear noise contributions could account for the difference.

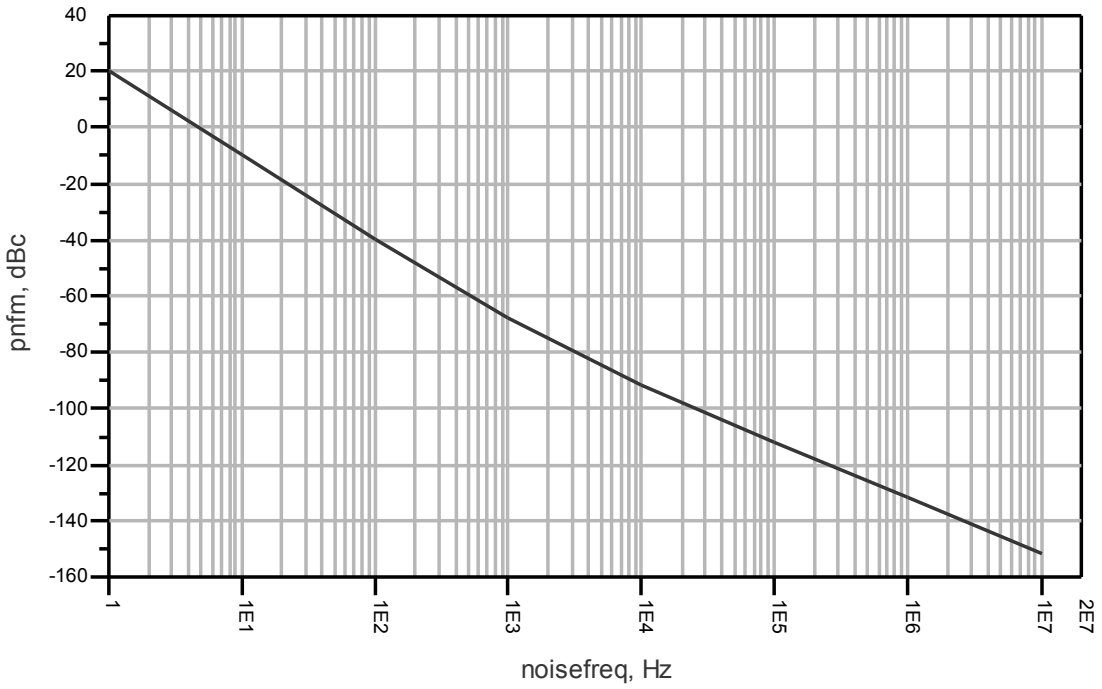


Figure 4.13: ADS phase noise simulation

noisefreq	pnfm
1.000 Hz	20.03 dBc
10.00 Hz	-9.944 dBc
100.0 Hz	-39.70 dBc
1.000kHz	-67.84 dBc
10.00kHz	-91.32 dBc
100.0kHz	-111.9 dBc
1.000MHz	-131.9 dBc
10.00MHz	-152.0 dBc

Table 4.2: ADS phase noise simulation

5 Experimental Results

5.1 Measurement Results Overview

Upon receiving the silicon die from fabrication, some basic experiments were performed to ensure that the circuit was operating to a first order as the simulation data predicted. This verification data was compared to the simulation data to evaluate the degree of correlation. The data presented includes: small and large signal S11 of the VCO core, phase noise, tuning sensitivity, output power versus tuned frequency, load pull sensitivity, and DC current consumption versus supply and temperature. The printed circuit board (PCB) used in the evaluations presented in this section

5.2 Small Signal S-Parameters

Experimental verification of the small signal (so-called “start-up”) S-parameters is performed using the Agilent 8753ES Network Analyzer. Figure 5.1 shows the experimental setup for both the small and large signal measurements. This test setup is equivalent to the Pspice simulation schematic illustrated in Figure 4.4. The important distinction about these

measurements is that the resonator has been removed and replaced with a 0Ω jumper. This allows the negative input impedance of the VCO device under test (DUT) to be measured directly.

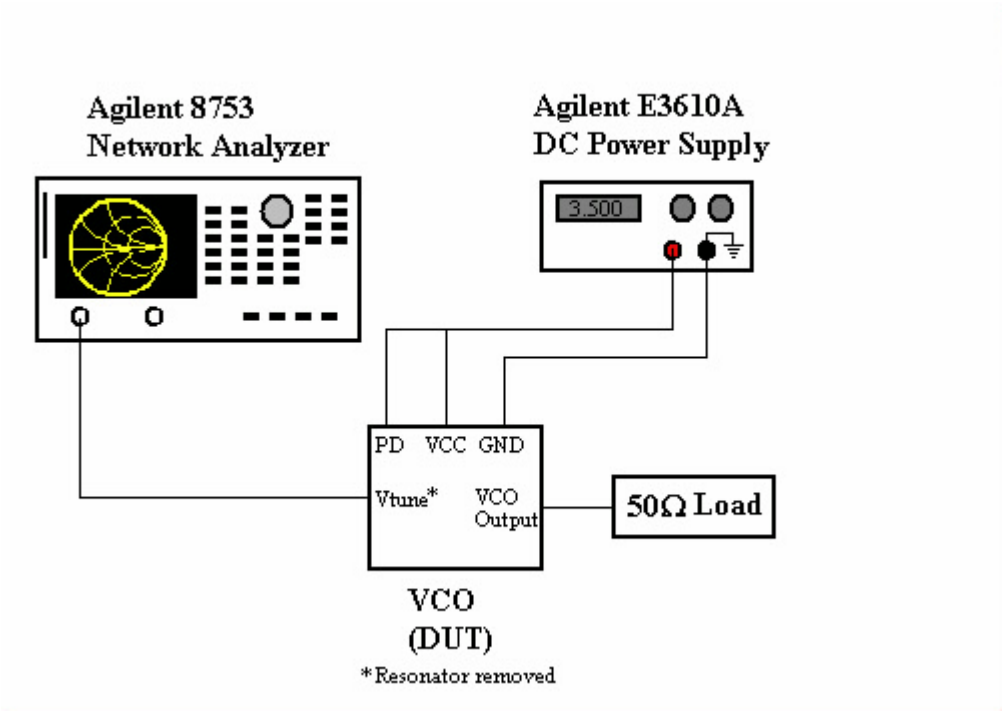


Figure 5.1: S-Parameter measurement setup

The measured S11 data was imported into ADS and plotted on the same Smith chart as the ADS simulation results. Figure 5.2 shows good correlation between the lab measurement and the ADS simulation. The primary difference is that the simulated S11, indicated by marker m2, indicates a slightly larger negative real component than the measured result at marker m1. This would indicate that the actual circuit is slightly lossier than was predicted in simulation. Loss in a real circuit may be explained by parasitic resistance that is greater than those in the simulation models.

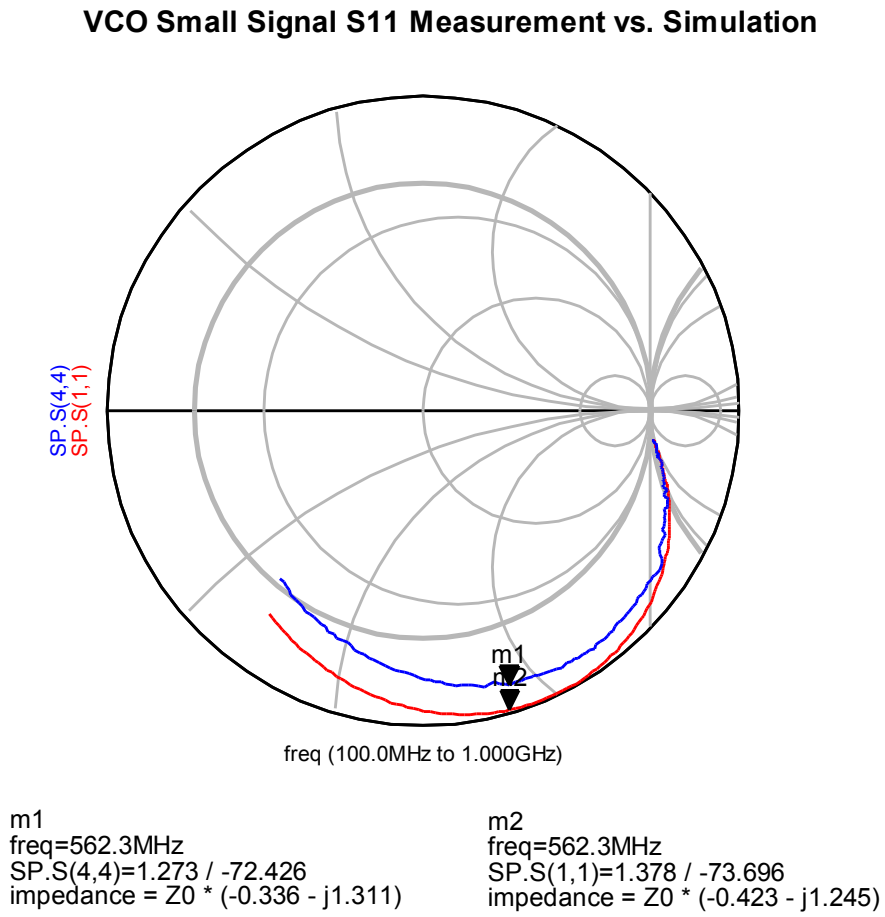


Figure 5.2: Measured versus simulated S11 (m1 is measured and m2 is ADS simulation)

The PSpice data was not in a convenient format for importing into ADS but is presented with the other simulation and measured data in Table 5.1. The ADS simulation seems to agree more closely with the measured data. The discrepancy between the measured and simulated is small enough to regard as simple parasitic losses that were not adequately accounted for in the simulation model. The PSpice simulation is slightly further from measurement than the ADS result but is still reasonable as a first pass approximation.

Method	S11 Data (Magnitude and Angle)
PSpice	1.4 ∠ -69.1
ADS	1.38 ∠ -74.76
Measured	1.27 ∠ -72.43

Table 5.1: Small signal S-Parameter summary

5.3 Large Signal S-Parameters

Large signal S-parameters were taken by performing a linear frequency sweep for S11 while incrementally increasing the test port power injected into the active device. Alternatively, the data could have been collected in a power sweep at a single frequency. The data shown in Figure 5.3 depicts the cumulative measured results for network source power levels of -30, -10, 0, and 10 dBm to the input of the DUT. The Smith chart scale is modified to show the values of negative resistance.

The data clearly indicates that the real impedance component begins at a negative value and moves toward a positive value for increasing input power levels. This is the expected result predicted in negative resistance analysis. The increasing power level approximates the effect of oscillation start-up conditions once the loop is closed by adding the resonator.

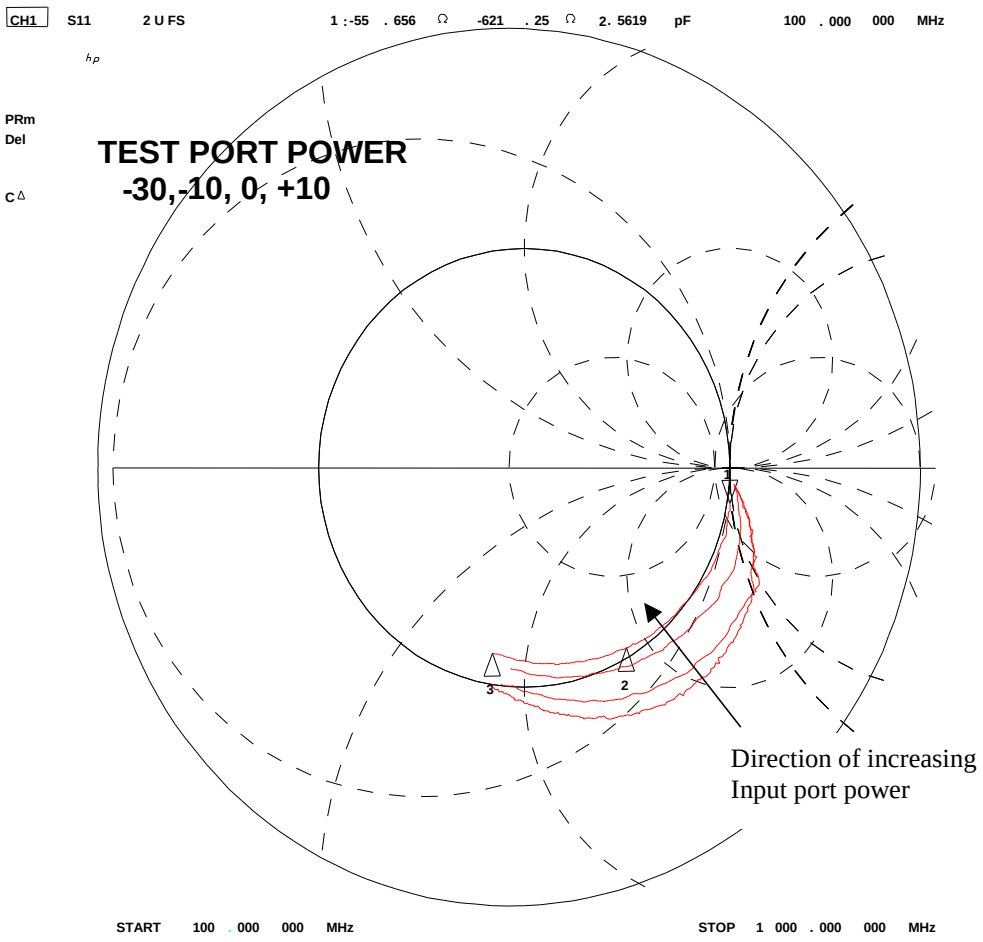


Figure 5.3: S11 versus frequency for stepped input power

5.4 VCO Output Spectrum:

The fundamental oscillator output power and frequency are determined using the measurement setup shown in Figure 5.4. Harmonic power levels are also measured for comparison against simulated results. The VCO in this case is connected as a closed loop system.

The output spectrum is shown in Figure 5.5. Two points become apparent in reviewing the data. The first point is that both the transient and harmonic balance simulations provide reasonably close approximations to the fundamental output power. The Pspice simulation is about 2 dB optimistic whereas the ADS simulation is much closer at about 0.6 dB lower than measured.

The next point is that the level of the second harmonic is well off the mark of both the PSpice and ADS simulation. After some investigation it was determined that the self-resonant frequency of the capacitor in the output resonant tank was to blame. The self-resonant frequency of the10 pF capacitor was much lower than the manufacturer model had suggested. When the impedance is viewed on a network analyzer the actual resonance is measured to be very close to the second harmonic of the oscillator fundamental frequency. This is an unintentional but beneficial result. The low second harmonic impedance improves the efficiency of the output buffer and helps to eliminate unwanted harmonic energy.

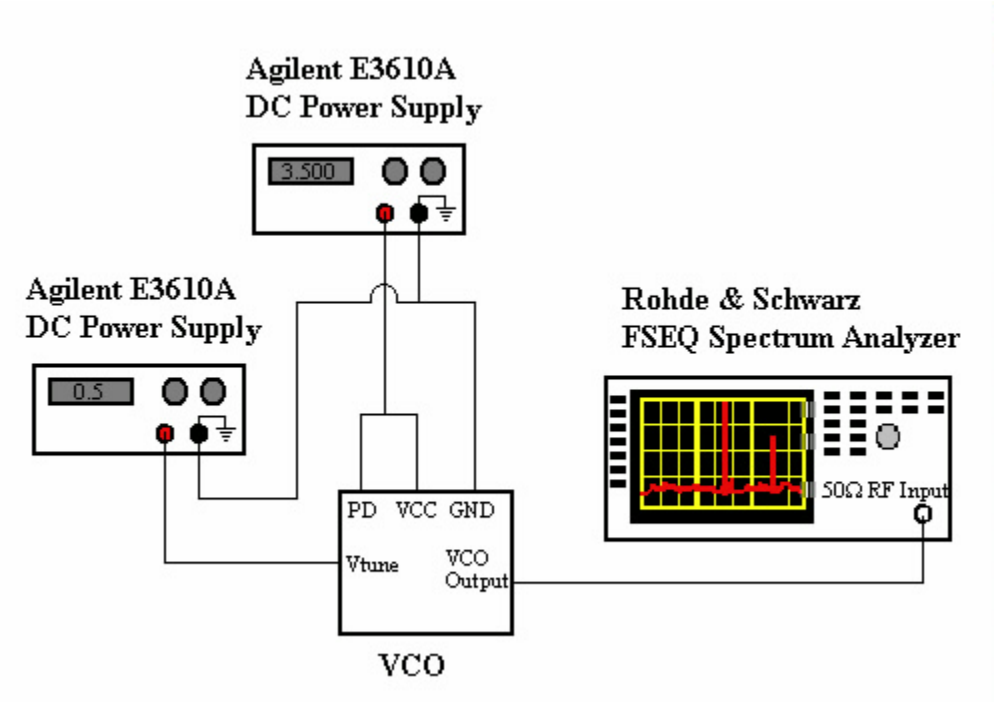


Figure 5.4: VCO output spectrum measurement setup

Method	Fundamental Power (dBm)	Second Harmonic Power (dBm)
PSpice	-1.9	-15.04
ADS	-4.81	-23.489
Measured	-4.22	-35.95

Table 5.2: Simulated versus measured output spectrum

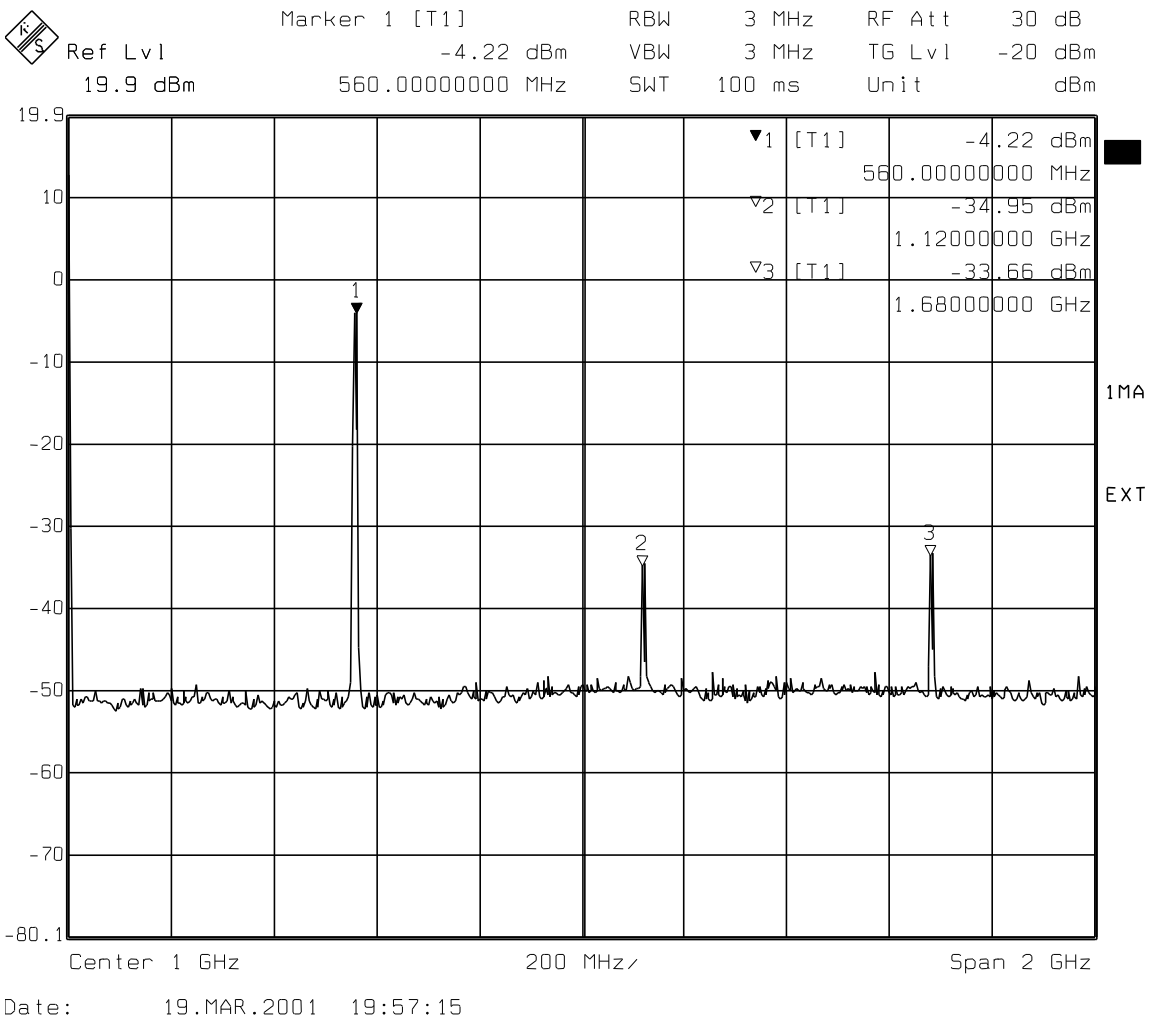


Figure 5.5: VCO spectral output

5.5 Phase Noise

The phase noise measurement was made using the HP4352B VCO/PLL Signal Analyzer. There are several advantages to using this system to measure the phase noise performance of an oscillator. The measurement device incorporates a self-contained low noise DC supply

with a frequency counter, power detector, mixer/downconverter, PLL, and quadrature detector. All of the specifications described in section 2.3 can be measured with this piece of test equipment with maximum reliability. Figure 5.6 illustrates the block diagram of a phase noise measurement made with the HP4325B. Measurements performed with this piece of test equipment are particularly convenient because of a built in carrier-lock mode PLL. The output from the second mixer is continuously sampled to lock the IF at the same frequency as the downconverted VCO input. This feature eliminates the measurement inaccuracy due to VCO drift that results from environmental (particularly temperature) variables. The low noise DC supply is also quite helpful in that it eliminates supply noise that could otherwise superimpose AM to PM noise into the VCO output spectrum.

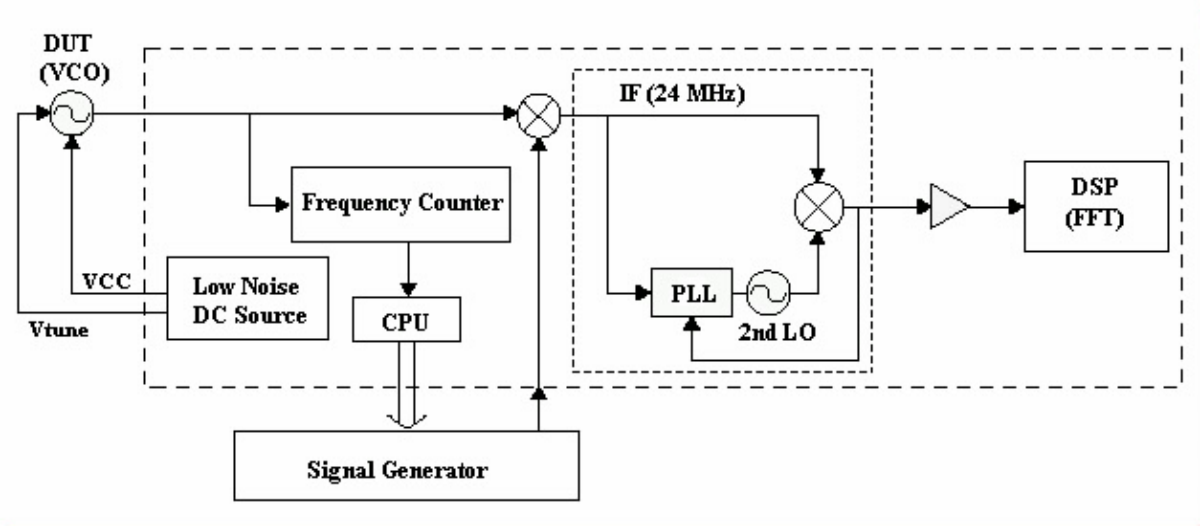


Figure 5.6: Block diagram of the HP4352B VCO/PLL signal analyzer measurement

The phase noise measurements were all carried out in a Faraday cage to ensure that environmental noise did not interfere with the measurement. The measurement results are shown in Figure 5.7.

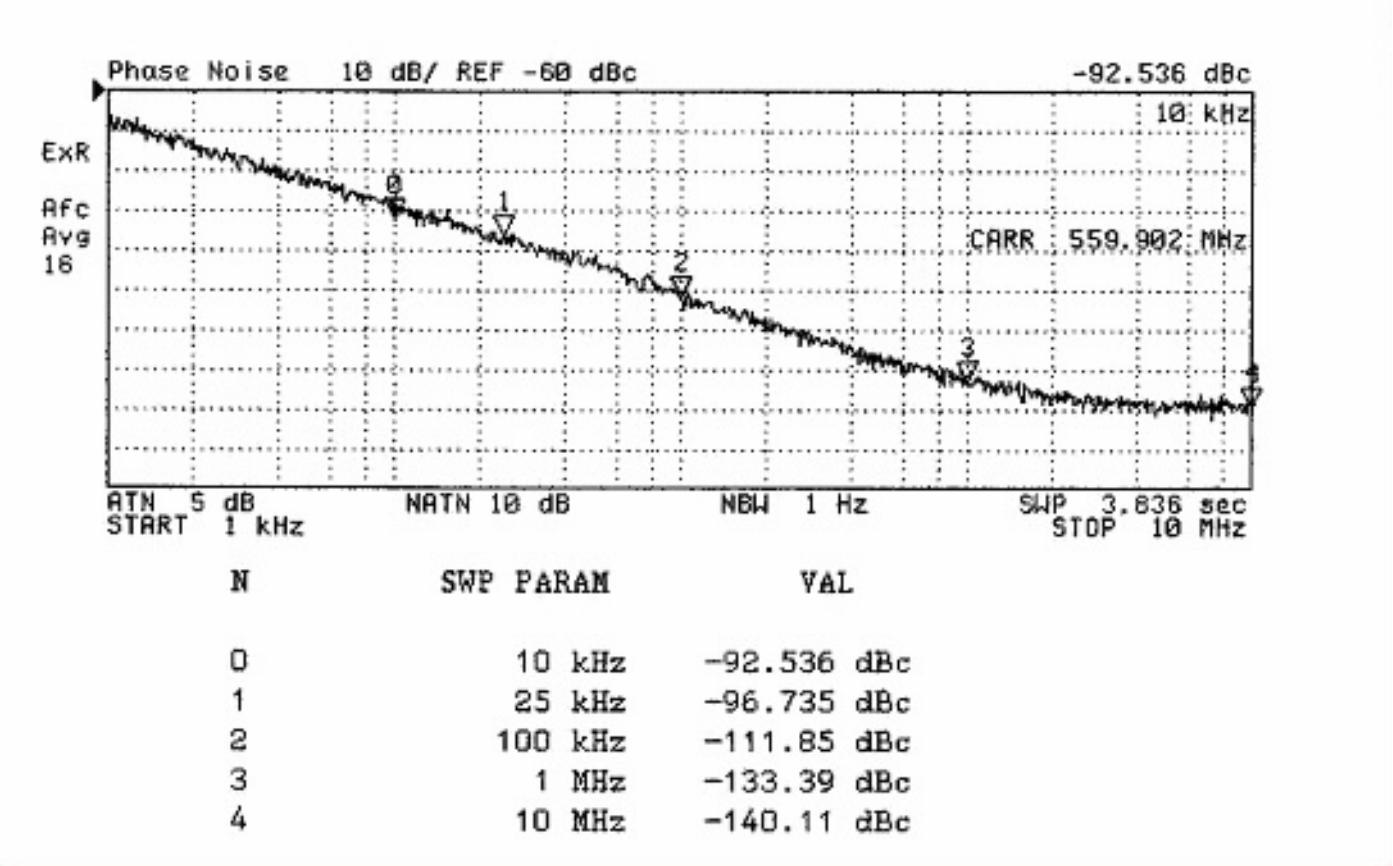


Figure 5.7: Phase noise results obtained with the HP4352B

The measured data is compared with the simulated data in Table 5.2. A 10 kHz offset was used as a point of reference for both simulations and the measurement. The measurement of –92.54 dBc/Hz is between the two simulated values but comes much closer to the ADS simulated value of –91.32 dBc/Hz. The accuracy in the ADS harmonic balance simulation is validated by the proximity to measured data.

Method	Phase Noise Data (dBm/Hz at 10kHz)
PSpice	-96.98
ADS	-91.32
Measured	-92.536

Table 5.3: Simulated versus measured phase noise

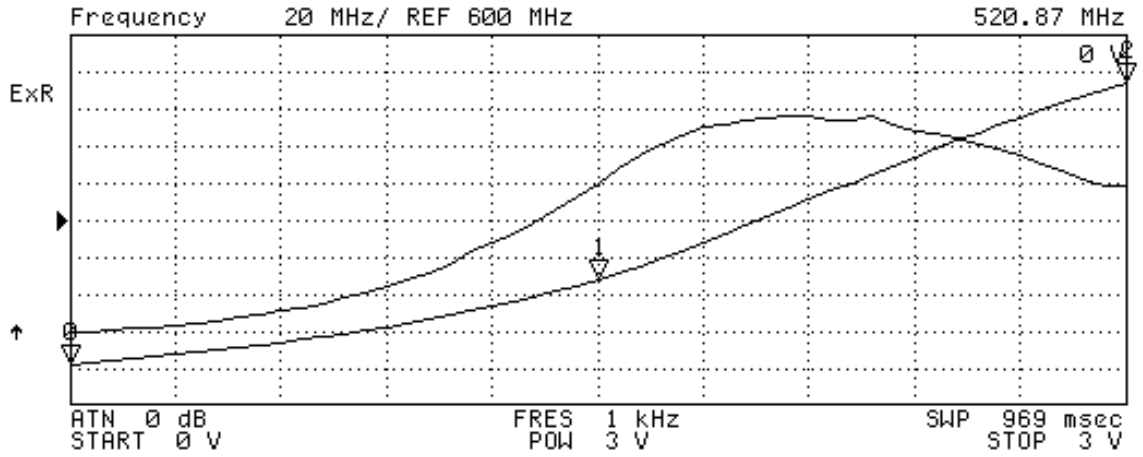
A final note about the measured phase noise data concerns the change in value as a function of tuning voltage. The shift in phase noise as a function of VCO frequency is largely a function of the tuning network. Noise present in the tank network will modulate the frequency of the carrier to a degree determined by the tuning sensitivity. Another effect of the tuning network on phase noise occurs when there is a significant change in the Q of a passive component. The overall effect is that the phase noise minimum occurs at the lowest tuning sensitivity[27] and increases to a maximum at the highest tuning sensitivity. The overall variance is about 9 dB and is heavily influenced by the choice of components in the tuning network.

5.6 Tuning Sensitivity

The importance of this parameter is highlighted in previous sections. Tuning sensitivity represents the slope of the frequency versus tuning voltage curve and is measured in MHz/V.

[27] For circuit presented, the lowest sensitivity occurs at the lowest frequency.

This is a very convenient measurement to make using the HP4352B. Figure 5.8 depicts two sets of data on the same graph. The markers lie on the plot of VCO output frequency versus tuning voltage. The second plot in the graph shows the derivative of the first curve. Discrete data points for both plots are presented in Table 5.3. A 3 volt sweep on the VCO tuning input causes over 153 MHz frequency shift of the oscillation frequency. This sensitivity data was not simulated, but the tuning range is close to the simulated data



N	SWP PARAM	VAL
0	0 V	520.87 MHz
1	1.5 V	567.675 MHz
2	3 V	674.344 MHz

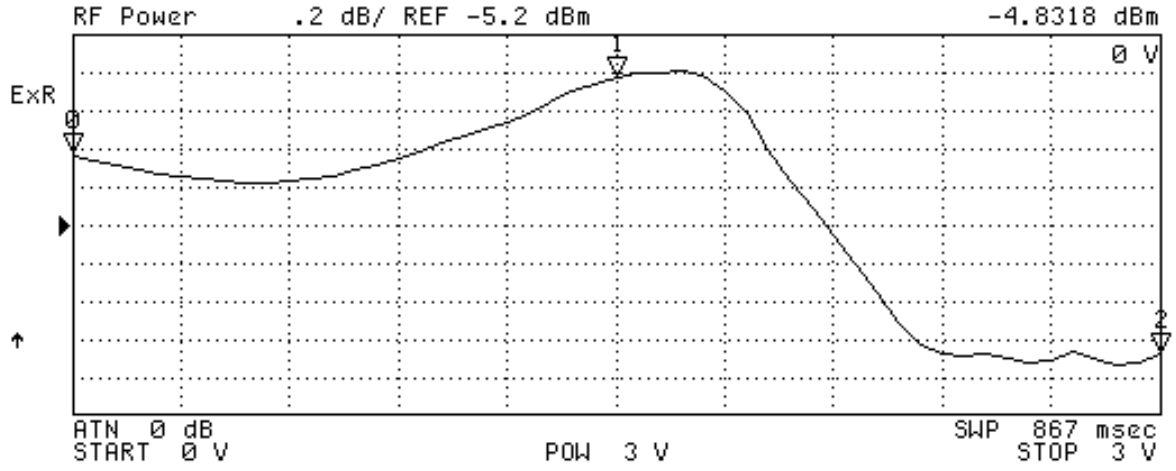
Figure 5.8: Measured VCO tuning characteristic

Tuning Voltage (V)	Output Frequency (MHz)	Tuning Sensitivity (MHz/V)
0	520.87	19.57
1.5	567.68	59.88
3.0	674.34	59.28

Table 5.4: Measured tuning sensitivity

5.7 Output Power versus Frequency

The total variance in output power as a function of tuning range directly influences system performance. As described previously, the VCO may be used to directly drive a power amplifier that requires a certain range of input signal level to maintain acceptable performance. This quantity was not simulated because the measurement result is strongly related to the impedance of the output matching network that was finalized empirically. However, the output power correlates well with the nominal[28] simulation result. The measured data in Figure 5.9 reveals that the power fluctuates by 1.05 dB across the tuning range.



N	SWP PARAM	VAL
0	0 V	-4.8318 dBm
1	1.5 V	-4.4251 dBm
2	3 V	-5.8817 dBm

Figure 5.9: Measured VCO output power versus frequency characteristic

[28] Measured at 560MHz with Vcc=3.0 V at room temperature

5.8 Load Pull Measurement

The load pull measurements were made with using the setup shown in Figure 5.10. The variable impedance was presented by attaching a known fixed value resistive load through a coaxial line-stretcher. The VSWR as measured on a network analyzer prior to the load pull indicated very close to a 1.75:1 ratio throughout the phase sweep on the Smith chart. As previously indicated, the measurement consists of a peak-to-peak frequency excursion over the phase sweep. The result was a 190kHzpp change in frequency over all phases.

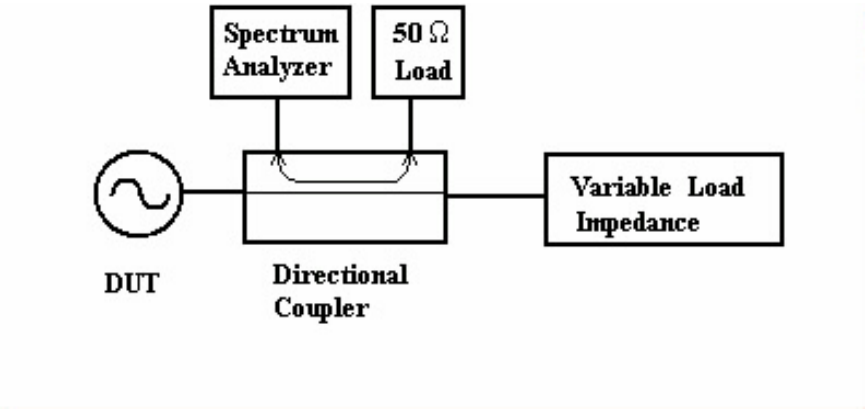


Figure 5.10: Test setup for measuring VCO load sensitivity

5.9 DC Measurement

The results of the DC measurements are shown in Figure 5.11. The graph represents the total quiescent current as a function of supply voltage and ambient temperature. The resonator was removed from the circuit in order to prevent oscillation from introducing self-biasing

effects. These effects could cause shifts in bias current consumption and may distort the DC measurement. Also, total bias current with no oscillation is how the PSpice DC simulation is performed. Therefore, the measured data in Figure 5.11 should be an accurate comparison.

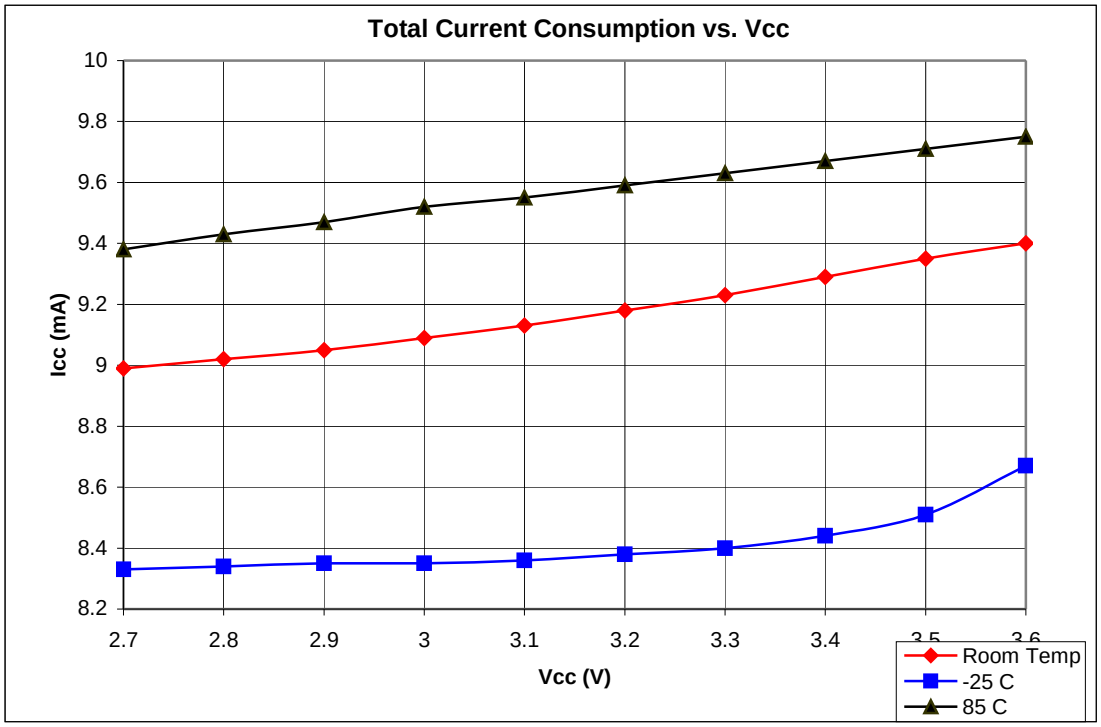


Figure 5.11: Total current consumption versus supply voltage (for T=-25, 27, and 85 ˚C)

The comparison of measured data to simulation shows reasonable agreement with two slight discrepancies. At room temperature simulation appears reasonably accurate with quiescent current at the nominal supply of 3.0 Volts with a magnitude difference[29] of 300 μA or about 3 %. However, over the temperature extremes of 85 and –25 ˚C, the difference between simulated and measured was more significant than at room temperature. The fundamental

[29] This is a difference between 9.12 for the PSPice simulation versus 9.09for the measured data.

difference, as summarized in Table 4.4, is that the relative difference between room temperature and either temperature extreme is more pronounced in the measured data than in the simulation.

Ambient Temp (˚C)	Measured (mA)	PSpice Sim. (mA)
-25	8.35	8.80
27	9.09	9.12
85	9.52	9.32

Table 5.5: Simulated versus measured quiescent current (at Vcc = 3.0V)

The other difference between measured and simulated data is the upturn in quiescent current at –25 ˚C. The measured current appears to begin to change slope at higher supply voltages and was not predicted in simulation.

6 Conclusion

A VCO design has been presented which has several desirable traits. It has the flexibility to be customized for a wide range of oscillating frequencies. The VCO is capable of maintaining desired power and frequency within acceptable limits even when exposed to changes in supply voltage, temperature, and output load mismatch. Nominal output power of –4.5 dBm at 560 MHz with 22% tuning range and –92.6 dBc/Hz at 10 kHz carrier offset has been demonstrated. This performance is measured with 9.6 mA of DC current consumption. It has been shown that better phase noise performance may be achieved with varactor tuning at the expense of tuning range. This performance is within acceptable limits for several radio air standards requiring an IF VCO.

Most of the simulation data is in reasonable agreement with measured results. The output power and large signal simulation corroborate particularly well. The level of the second harmonic was one measured data point that was not in agreement with simulation. The simulated data in both PSpice and ADS indicated that the harmonic energy should have been much larger than was measured in the lab. In retrospect, the surface mount devices should have been more carefully modeled. A shift in the actual self-resonant frequency of the capacitor in the output LC tank was determined to have caused a series resonant trap at the second harmonic. This low impedance at the output of the device helps to account for the discrepancy. Other measured parameters were within reasonable proximity of simulation.

7 Suggestions for future research

In reviewing the results from the fabricated VCO a few potential areas for improvement become apparent. One area worth investigating is to simply change the design to a lower noise process. Silicon Germanium (SiGe) has been adopted by several foundries as a superior low-noise process. This would be a natural fit for the design presented in this paper since most SiGe processes have the same basic BiCMOS devices. Cost may be a concern with this approach since the process is unique to RF design and tends to run at lower production volumes than a microprocessor process like CMOS.

Another possible improvement concerns the addition of an AGC feedback loop to improve the current consumption and phase noise performance. A few papers have been written about the promising results of detecting the oscillator output level and using a DC correction to adjust the VCO bias level. This technique would have the additional benefit of providing a more constant power level out of the VCO.

Investigation of different biasing topologies to reduce the amount of injected low frequency noise is also an area with potential value. Some of the difficulty in providing a VCO bias is that there are few ways to bias the VCO core without degrading performance. Some clever bias techniques may help to minimize the amount of injected low frequency noise or degrading the resonator Q.

Appendix A

Coil Craft Inductor Pspice Model

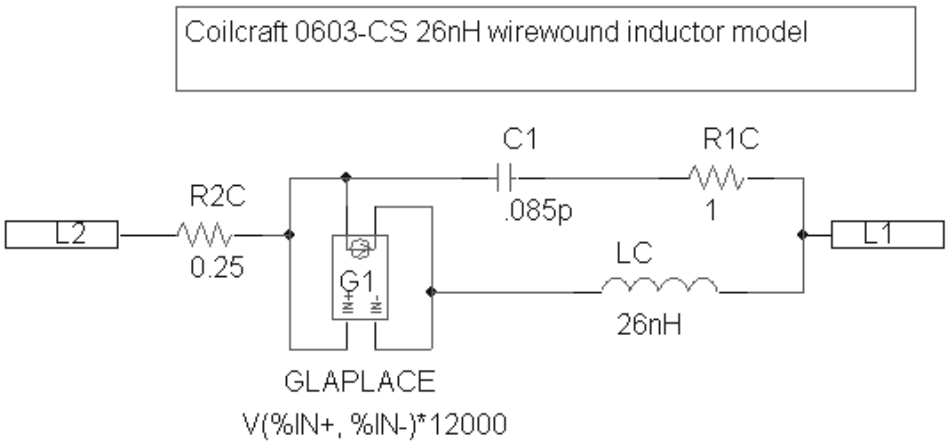


Figure A1: PSpice Inductor model using a frequency dependent conductance

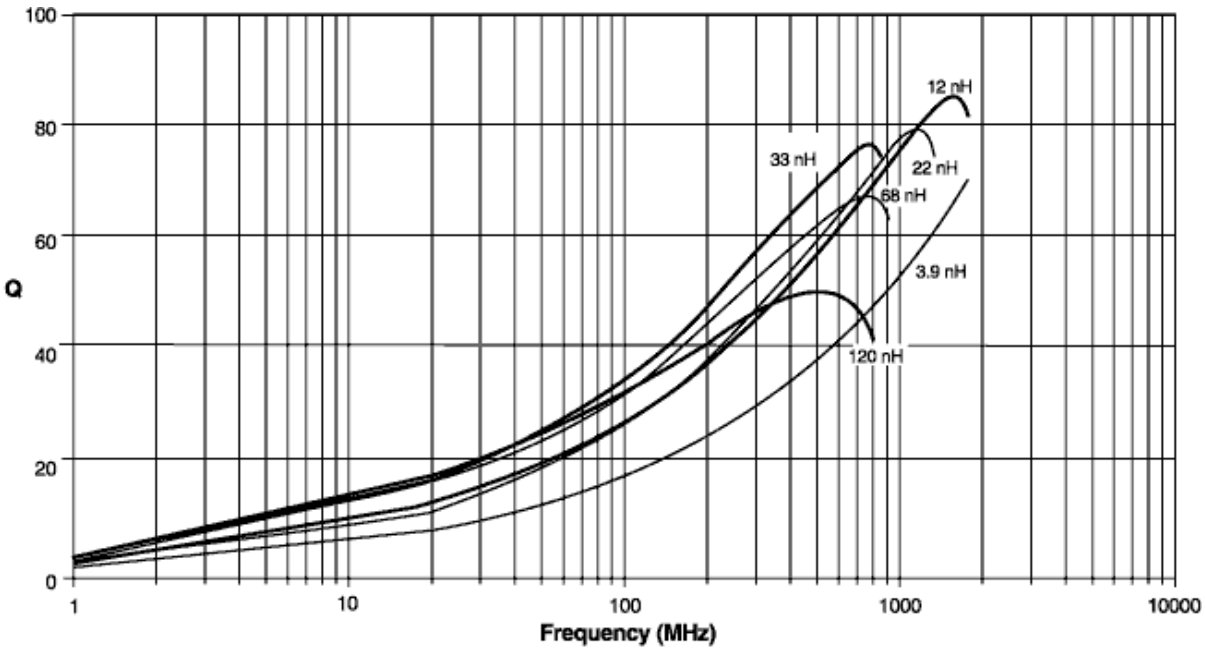


Figure A2: Inductor Q versus frequency (Reprinted with permission from Coilcraft®)

Appendix B

Alpha Varactor Pspice Model and Specifications[30]

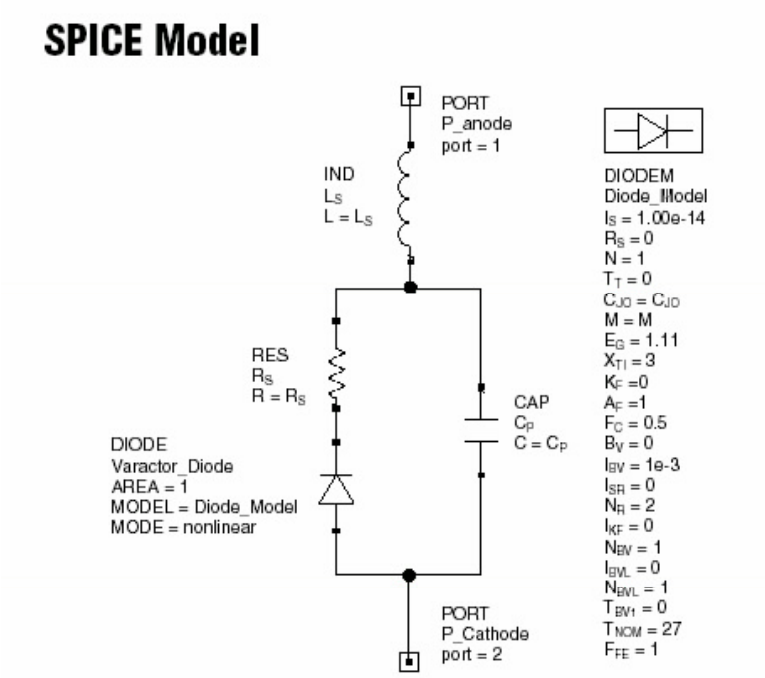


Figure B1: Alpha Varactor Spice model

Part Number	C_{JO} (pF)	V_J (V)	M	C_P (pF)	R_S (Ω)
SMV1249	39.00	17	14.0	0	1.5

Table B1: Specifications for the varactor used in this thesis

[30] Alpha Semiconductor Inc. is now Skyworks. All varactor data is reprinted with permission.

Appendix B continued

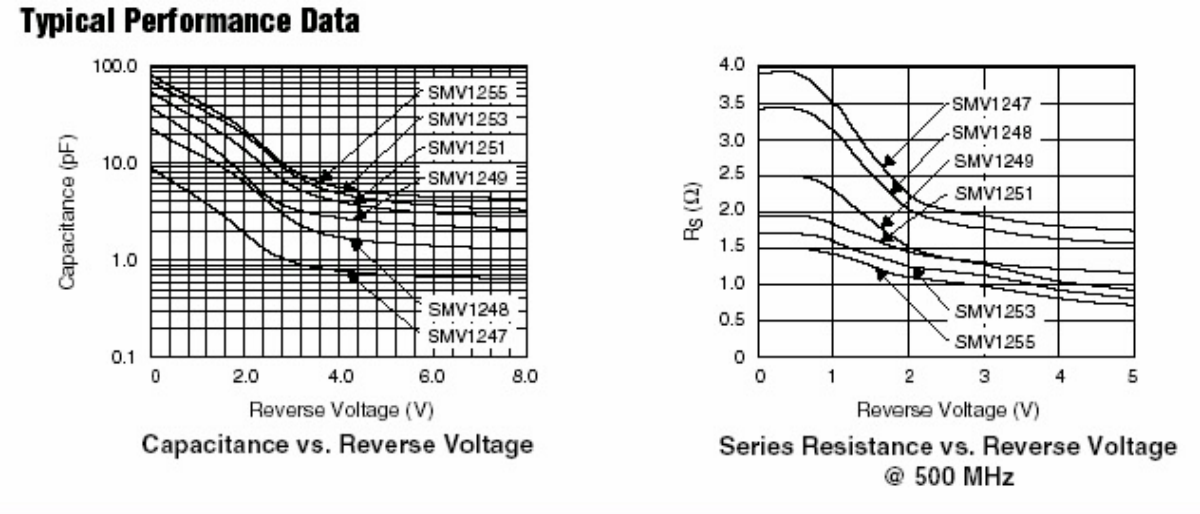


Figure B2: SMV-1249 capacitance and resistance characteristics versus reverse voltage

Appendix C

Complete Circuit Schematic

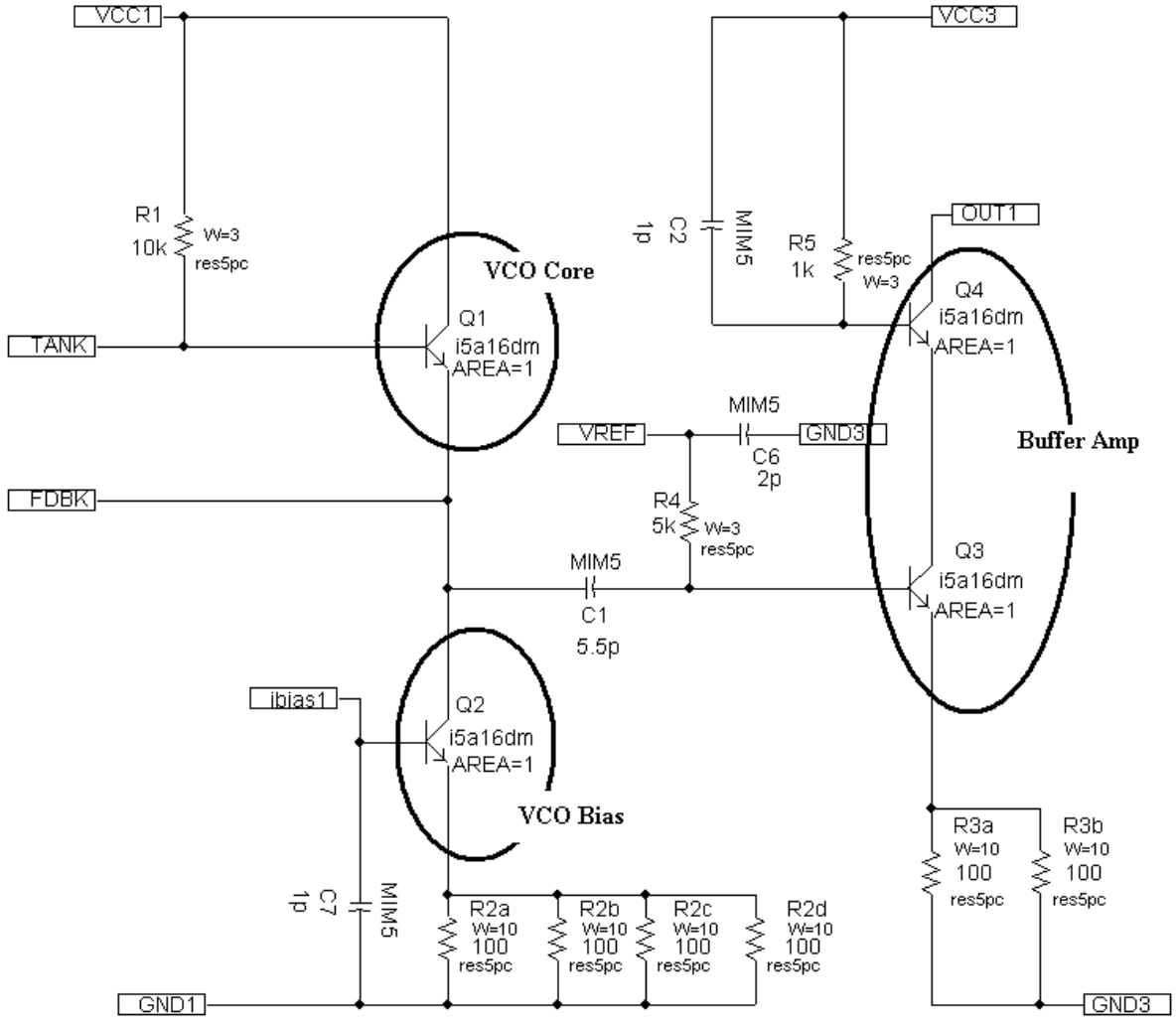


Figure C1: VCO core and buffer amplifier schematic

Appendix C (continued)

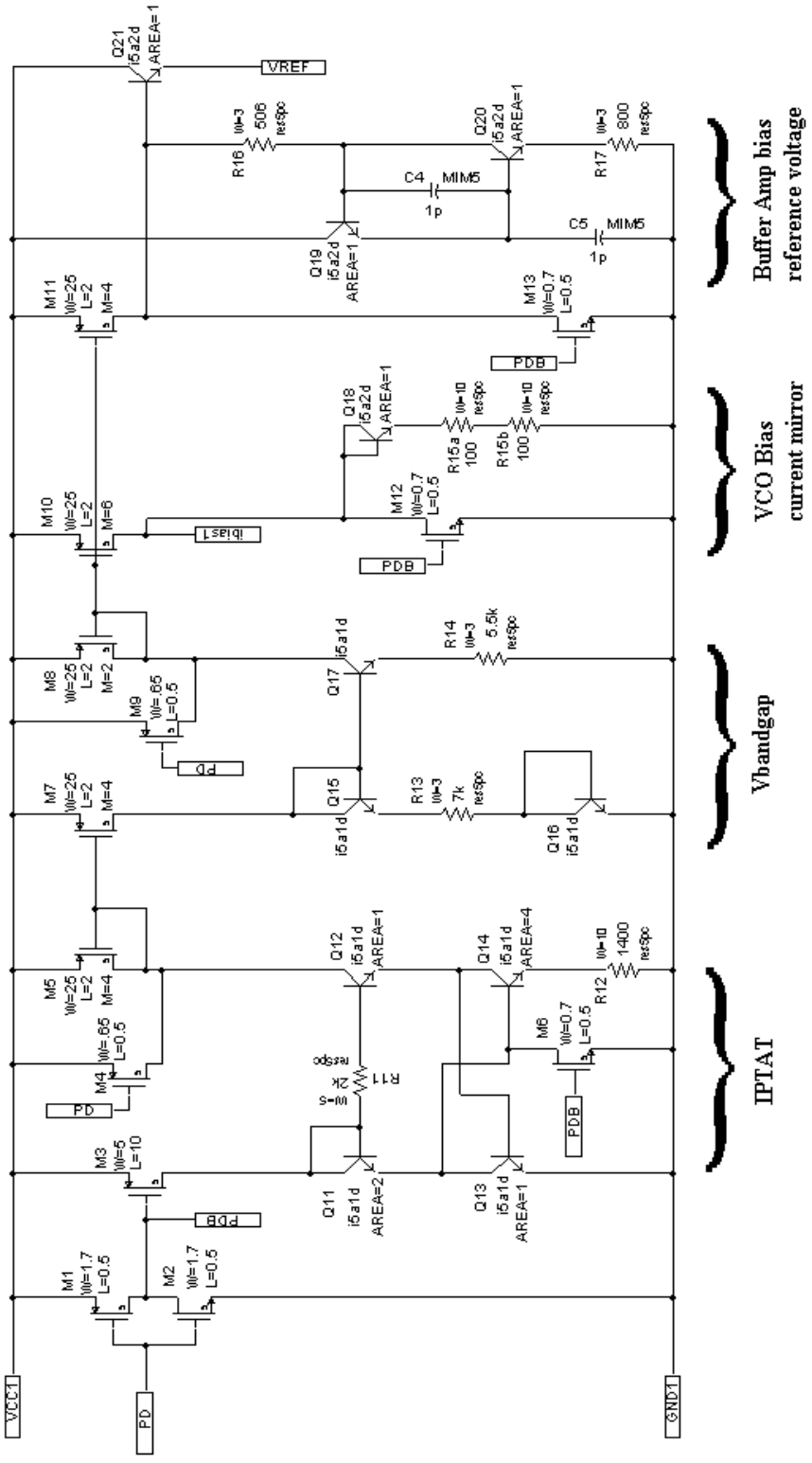


Figure C2: Bias and reference generator schematic

Appendix C (continued)

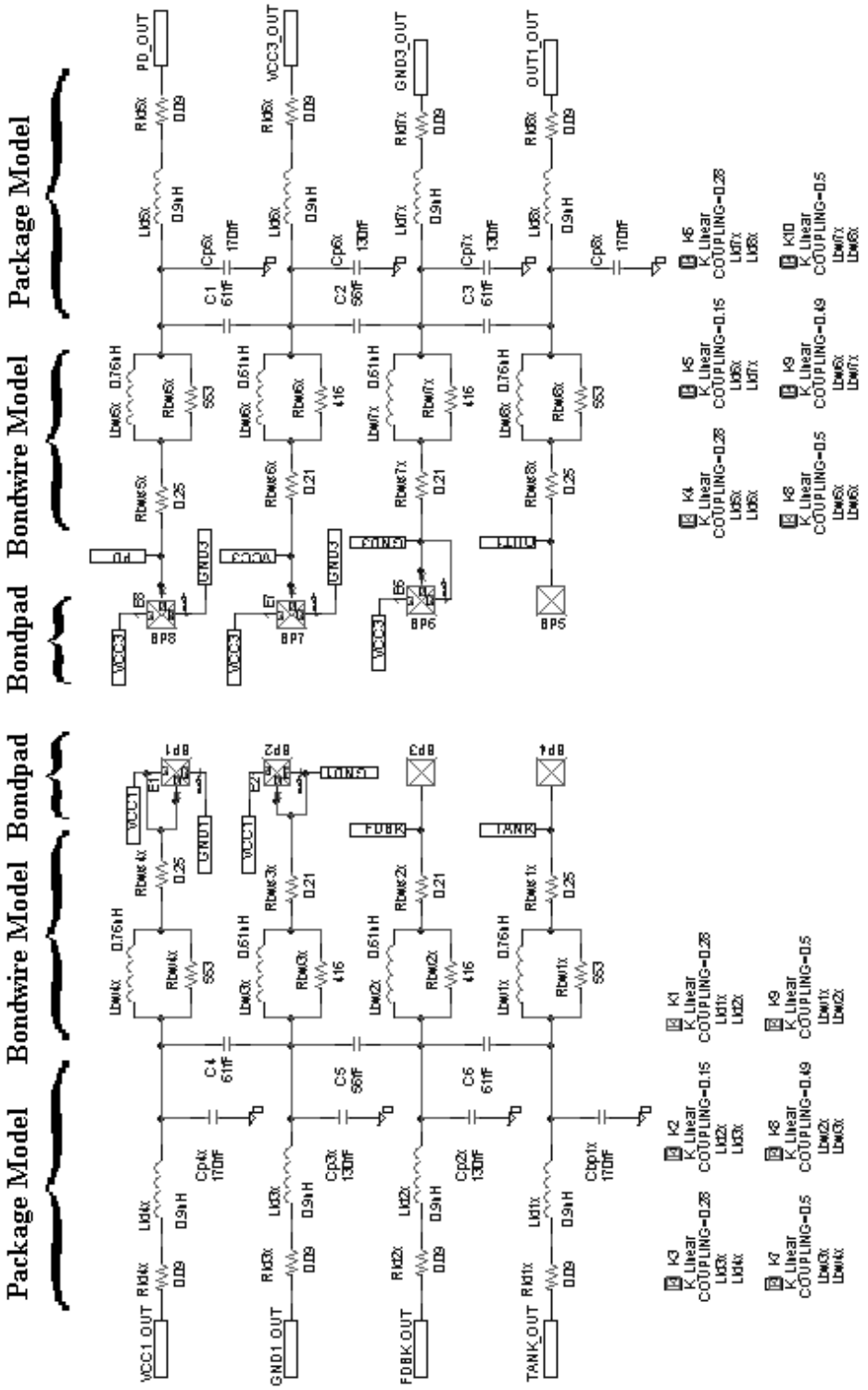


Figure C3: Complete package model including all simulated parasitics

Appendix D

Evaluation PCB Schematic and Picture

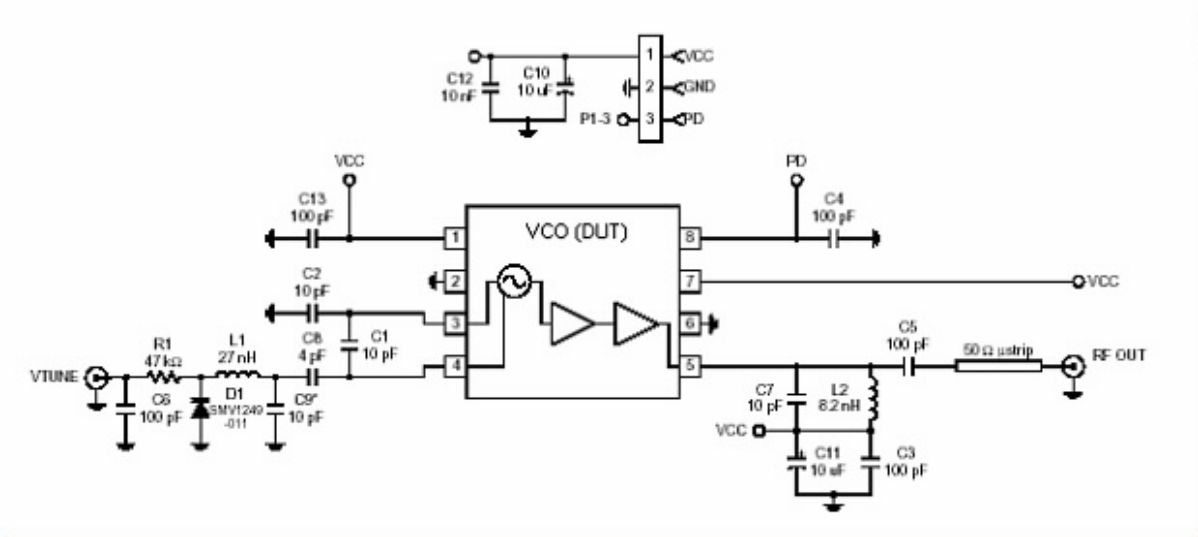


Figure D1: Evaluation schematic

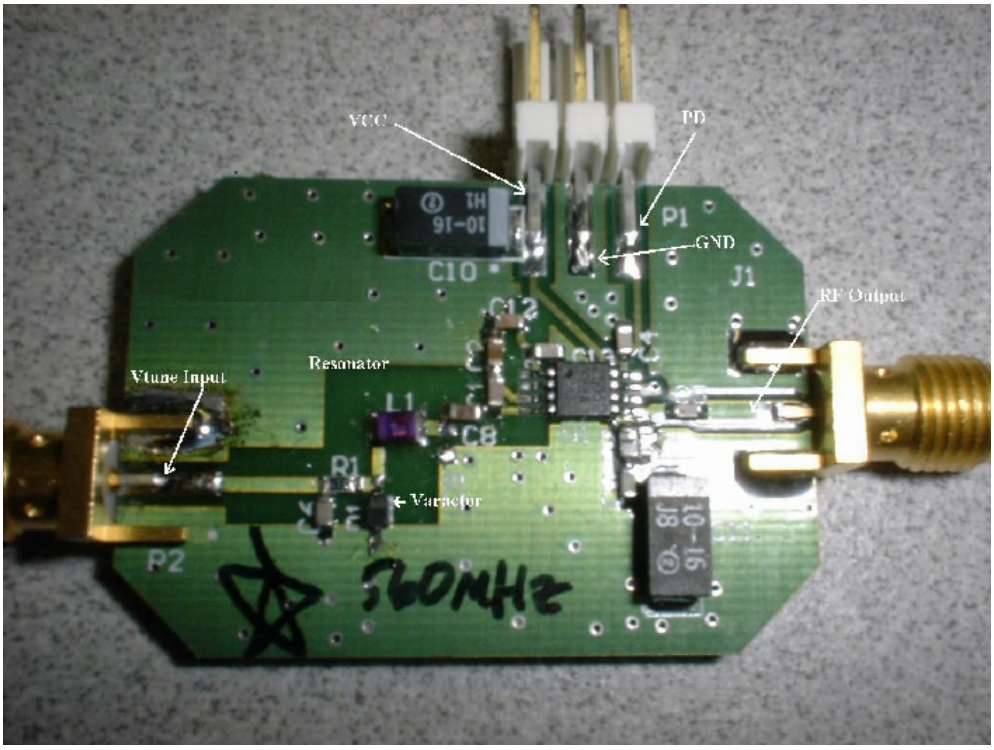


Figure D2: Evaluation PCB

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VITA

Ryan Travis Bosley was born on July 23, 1971 in Raleigh, North Carolina. He grew up in Chesterfield County just south of Richmond, Virginia and graduated from Monacan High School in 1989. Ryan enrolled at Virginia Tech and was accepted into the Bradley Department of Engineering. He completed his Bachelor of Science degree in December of 1994.

After graduation, Ryan worked on high speed digital fiber optic components for Force, Inc. of Christiansburg, VA. The work in high frequency electronics spurred an interest in pursuing additional education in the field of RF design. This interest led Ryan back to Virginia Tech where he enrolled in the Masters program within the Electrical Engineering Department. He completed all the required coursework in August 1997 but did not finish the thesis requirement before accepting a position as an design engineer with RF Micro Devices. Ryan has been working to complete his thesis while employed. He will have completed all the requirements for Master of Science in Electrical Engineering in January of 2003. After graduation, Ryan will continue to work as a design engineer at RF Micro Devices.