Development of Integrated "Chip-Scale" Active Antennas for Wireless Applications

Jun Zhao

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Sanjay Raman, Chair
Warren L. Stutzman
Dennis G. Sweeney

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(ABSTRACT)

With the rapid expansion of wireless communication services, ultra-miniature, low cost RF microsystems operating at higher carrier frequencies (e.g. 5-6 GHz) are in demand for various applications. Such applications include networked wireless sensor nodes and wireless local area data networks (WLANs). Integrated microstrip antennas coupled directly to the RF electronics, offer potential advantages of low cost, reduced parasitics, simplified assembly and design flexibility compared to systems based on discrete antennas. However, the size of such antennas is governed by physical laws, and cannot be arbitrarily reduced. The critical patch antenna dimension at resonance needs to be $\sim \lambda_g/2$ (where λ_g is the guided wavelength given by $\lambda_g = \lambda_0/\sqrt{\epsilon_r}$) . Several methods are available to reduce the physical size of the antenna to enable on-chip integration. A high dielectric constant substrate reduces the guided wavelength. Grounding one edge of the microstrip patch enables the resonant antenna length to be further reduced to $\sim \lambda_g/4$. However, these techniques result in degraded antenna efficiency and bandwidth. Nonetheless, such antennas still have potential for use in low power/short range applications.

In this work, "electrically small" (small with respect to λ_o) square-shaped microstrip patch antennas, grounded on one edge by shorting posts, have been investigated. The antenna input impedance depends on the feed position; by adjusting the feed point, the antenna can be tuned to match a 50 Ω or other system impedance. The antennas were designed on a GaAs substrate, with a high dielectric constant of 12.9. The size of the patch antenna is further reduced by utilizing shorted through substrate vias along one edge. The size of the antenna is about 4.2mm$\times$4.2mm, which is $\sim$1/13 of λ_o at $\sim$5.6GHz. The antennas are practical for integration on chip. Due to the size reduction, the simulated peak gain of the antenna is only -10.2 dB ($\sim$ 3.2% radiation efficiency). However, this may be acceptable for short-range wireless communications and distributed sensor network applications.

Based on the above approach, integrated GaAs "chip-scale" antennas with match-

ing power amplifiers have been designed and fabricated. Class A tuned MESFET power amplifiers (PAs) were designed with outputs directly matched to the antenna feed point. The antenna is fabricated on the backside of the chip through backside patterning; the PA feeds the antenna through a backside via. The structure is then mounted such that the antenna faces up, and is compatible with flip-chip technology. The measurement of a 50 Ω passive (no PA) antenna indicates a gain of –12.7dB on boresight at 5.64 GHz, consistent with the antenna size reduction. The measurement of one active antenna (50 Ω system) shows a gain of -4.3dB on boresight at 5.80 GHz. The other version of active antenna (22.5 Ω system) shows a gain of -2.9 dBi on boresight at 5.725 GHz. The active circuitry (PA) contributes an average of ∼9 dB gain in the active antenna, reasonable close to the designed PA gain of 12.7dB. The feasibility of direct integration of a PA with an on-chip antenna in a commercial GaAs process at RF frequencies was successfully demonstrated.

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Above all, this is for my wife.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

With the rapid expansion of wireless communication services, ultra-miniature, low cost RF microsystems operating at higher carrier frequencies are in demand for various applications. Traditional RF front-end implementations require a large board area for off-chip passive components and packaged ICs; the integration of the front-end will therefore enable wireless transceivers with potentially lower cost, reduced size and higher reliability. The development of RFIC technologies has led to a continuous reduction in the size of wireless systems, which are now approaching "system-on-chip" solutions. Current wireless transceivers employ 4-5 RFICs and a number of off-chip components; for example, the RF component count in a GSM mobile phone has been reduced from ∼500 in 1994 to ∼50 in 2002 [1].

As the transceiver size shrinks dramatically with newer technology and improved architectures, it is potentially desirable to have the *antenna* integrated on-chip for lower cost and ease of matching. The integration of an antenna on-chip is quite a different matter than integrating the rest of the front-end, since antenna size is governed by physical laws rather than technological limitations and can not be arbitrarily reduced [2]. However, if some degradation in antenna performance can be accepted, antenna size reduction for the purpose of on-chip integration can be achieved.

In the milimeter-wave (mm-wave) regime, antennas have been integrated with transceivers to achieve better performance and lower cost [3][4]. As the operating frequency increases, the parasitics of bondwire interconnections between off-chip antennas and transceiver electronics could degrade the performance of the system. Integrating the

antenna directly with the electronics can help to reduce the effects of these parasitics. The wavelengths at mm-wave frequencies are generally smaller than the size of a typical transceiver chip; since antenna size is normally some fraction of the operating wavelength, it can be integrated on-chip in a reasonably straight forward manner. On the other hand, at lower microwave frequencies (e.g. 5-6 GHz), the operating wavelength is very large compared to the size of a typical transceiver chip, so antenna size reduction is a very critical in order for the antenna to be integrated directly on the RFIC chip. Such reduced size antennas are considered "electrically small", i.e. small with respect to the wavelength of interest in free space [5].

The 5-6 GHz frequency range is currently of significant interest for short range, high-speed wireless digital communications (e.g. wireless LANs). 300 MHz of spectrum, referred to as the U-NII (Unlicensed National Information Infrastructure) band was recently made available by FCC [6]. The U-NII band spectrum is located in the frequency ranges 5.15-5.25, 5.25-5.35 and 5.725-5.825 GHz. The corresponding maximum EIRPs (effective isotropic radiated powers) are 200mW, 1W and 4W, respectively, providing coverage from inside buildings up to $\sim$6 miles radius. This frequency range will be the focus of the integrated RF antennas to be developed in this work.

Flip-chip technology offers many advantages over the standard wirebond technology [7]. Instead of using wirebond connections from the die to the package, the bare die is flipped upside down and connected directly to a carrier substrate. Flip-chip technology has the potential for high level of integration, lower cost, smaller overall chip size and improved performance. One of the various attachments for flip-chip technology is solder attachment (ball grid array) which offers the lowest cost.

In order to achieve on-chip antenna integration at RF frequencies, one approach under consideration is the use of a flip-chipped microsystem with an electrically small patch antenna fabricated on the backside of the chip (Fig. 1.1). As a proof of concept, a standard GaAs MESFET process ($125\mu m$ thick substrate) with backside patterning is to be employed. The electronics are fabricated on the "top" of the chip through a standard fabrication process. The patch antenna will be defined on the backside of the chip using backside processing. The chip will be mounted backside up to facilitate antenna radiation. Since the electronics will be very close to the nearby ground plane, there are several potential advantages. The source connections of the MESFET are typically made to the ground through backside vias, resulting in unwanted parasitic

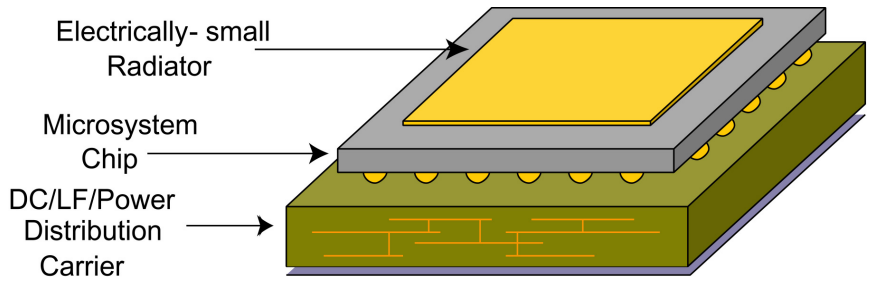


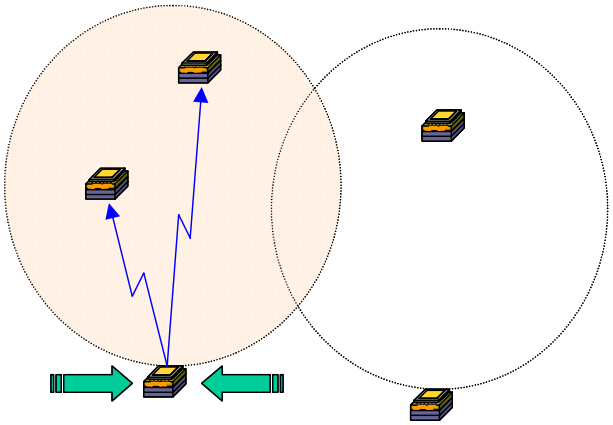
Figure 1.1: Conceptual flip-chipped microsystem with electrically small antenna on backside of the chip.

inductances and capacitances. In a flip-chip approach, since the electronics are much closer to the system ground, the parasitics can be reduced significantly. In addition, heat dissipation is an important issue for GaAs power devices since GaAs is not a good thermal conductor. By having the electronics close to the ground, heat can be transferred more efficiently from the power devices to the heat sink.

As will be discussed in Chapter 2, electrically small integrated antennas suffer from lower efficiency and bandwidth. However, such antennas still have the potential for use in low power, low data rate applications such as distributed wireless sensor networks [Fig. 1.2(a)] for environmental monitoring, condition-based maintenance, etc. [8]. Such integrated antennas could also find application in dense wireless information networks [9], composed of embedded nodes offering medium to high data rates [Fig. 1.2(b)].

1.1 Microstrip Antennas

Microstrip antennas have the advantages of low profile, small size, low weight, low cost and ease of fabrication. The possibility of planar fabrication makes microstrip antennas attractive candidates for on-chip integration. A microstrip antenna consists a thin patterned metal layer located a small fraction of a wavelength above a ground plane. There are many different shapes of microstrip antennas: square, circular, trapezoidal, H-shaped, etc. A half-wavelength rectangular patch antenna can be modeled as two radiating slots separated by $\lambda_g/2$ so that the radiation field sums at the normal direction resulting in a broadside radiation pattern.



(a)

(b)

Figure 1.2: (a) A distributed wireless sensor network. (b) A wireless information network.

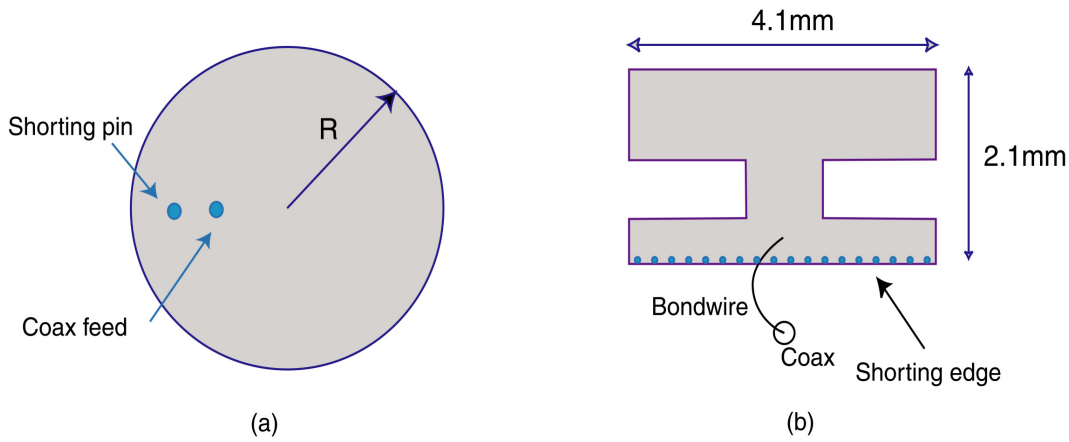


Figure 1.3: Electrical small antennas: (a) circular antenna with shorting post; (b) small H-shaped antenna with shorting posts.

Several methods can be used for small microstrip antenna design: (a) optimization of the shape of the antenna; (b) use of higher ε_r material resulting in shorter guided wavelength which in turn significantly reduces the antenna size; (c) introducing shorting pins or shorting walls between the antenna and the ground. The above techniques can also be combined together to further reduce antenna dimensions. The trade-off is reduced bandwidth and efficiency.

Various small antennas have been built and reported in the literature using the above techniques. Probe fed circular microstrip antennas with shorting posts [10][11] can reduce the overall size of the antenna [Fig. 1.3(a)]. One reported circular antenna has a diameter of $\sim 0.21\lambda_g$ (resonant frequency at $\sim$1.535 GHz, gain not reported). A small H-shaped antenna shorted along one side [12] was demonstrated on a GaAs chip with wirebond feeding [Fig. 1.3(b)]. The reported H-antenna is $0.29\lambda_g \times 0.15\lambda_g$ (resonant frequency at $\sim$5.98 GHz) in size and demonstrated a gain of -9.4dBi. A similar design is chosen for the integrated antennas in this work, and will be discussed at length in Chapter 2.

1.2 Power Amplifier

The power amplifier (PA) is the last active (amplifying) stage in the transmitter before the signal is radiated through the antenna. PAs require high output power

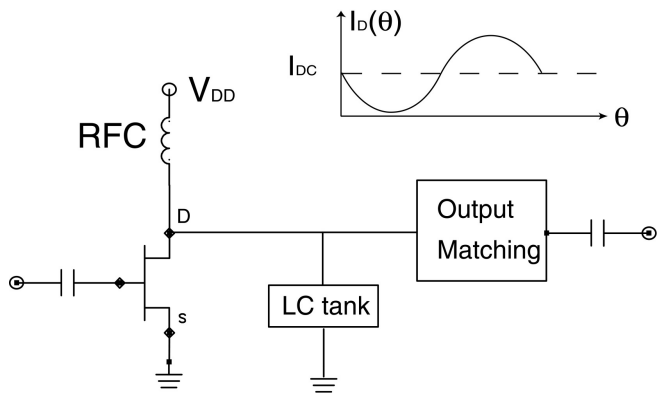


Figure 1.4: Class A power amplifier with the corresponding conduction angle plot.

and high DC-to-RF efficiency. Power amplifier design involves trade-offs between efficiency, linearity, complexity and power consumption [13][14]. The bias voltage is used to control the quiescent drain current and the conduction angle. The conduction angle is a measure of how much of a given cycle the transistor is on. For example, if the transistor is on during the entire circle, then it will have a conduction angle of 360°. If the biasing can be designed to reduce the fraction of a cycle over which drain current and drain voltage are simultaneously nonzero, the transistor DC power dissipation will decrease resulting in better DC-to-RF efficiency.

The well-known class A power amplifier (Fig. 1.4) is very similar to a small-signal linear amplifier except that the swing of the ac signal is large comparable to the DC bias level. The Class A PA conducts current 100% of the time and has a maximum theoretical efficiency of 50%. On the other hand, class B (push-pull) amplifiers normally require two transistors; each transistor conducts current 50% of the time and the resulting amplifier circuit has a maximum efficiency of 78.5%. However, the improved efficiency of a class B amplifier comes with a cost–distortion. This illustrates the well-known trade-off between efficiency and linearity. Class AB amplifiers offer a compromise between efficiency and linearity. Class AB designs conduct current 50%-100% of the time, somewhere between Class A and B amplifiers. Other amplifier classes (D, E, F, etc.) can achieve up to 100% efficiency in theory, but at the cost of linearity, complexity, and/or bandwidth.

Power amplifier design is significantly different from the small-signal amplifier design. Small-signal S-parameter simulations can not accurately predict the performance of

the amplifier [15]. Stability is a very important concern; generally a good PA design must be stable over a wide frequency range from DC to the upper operating range of the device. The maximum power transfer theorem used in small-signal/low-noise amplifier design is not generally useful at the output of the PA, since efficiency and output power need to be optimized rather than signal-to-noise ratio.

1.3 Active Integrated Antennas

By having the antenna and active circuits (e.g. amplifier) fabricated together, an active integrated antenna (AIA) could help to realize miniaturization of the RF circuitry, eliminate interconnection losses and allow matching directly between the antenna and the active devices. A receive-mode AIA at ~2.1 GHz was reported by Andrenko, *et al.* [16]; the antenna and low noise amplifier are matched directly for both gain and noise performance. Another AIA at $\sim$ 10 GHz was reported by Fusco, *et al.* [17]; by fabricating a patch directly on a high resistivity Si substrate, a Schottky diode is formed between the patch and the ground. With DC bias applied on the patch, the active antenna serves to directly modulate the CW microwave signals. Two class B GaAs FETs (field effect transistors) integrated with a patch antenna operating at $\sim$ 2.48 GHz were reported by Radisic, *et al.* [18]. The center of the patch was shorted to tune out the second harmonic. The integrated antenna with tuning shows improvements in both the PAE (power-added efficiency) and output power.

In this work the active antenna will be fabricated on GaAs, which is a low-loss semi-insulating substrate. To achieve fully on-chip *active* antennas, a power amplifier is designed to be completely integrated with the antenna using on-chip inductors, capacitors and/or transmission line matching networks. Inductors and transmission lines built on GaAs generally offer much lower loss compared with those on standard Si substrates. In the flip-chip scenario, inductors and transmission lines are placed very close to the system ground plane. Consequently, the Q and the self-resonant frequency of the flip-chipped inductors may be reduced considerably due to increased parasitic capacitances, and the impedances, etc. of transmission lines will also be affected. Therefore inductors and transmission lines need to be carefully modeled for this implementation.

1.4 Objective

The objective of this work is to demonstrate the possibility of integrated electrically small microstrip antennas for wireless system-on-chip applications in the 5-6 GHz band. Microstrip antennas have the potential to be integrated directly with other electronic components such as power amplifiers and low noise amplifiers to realize a single chip RF transceiver, reducing the size of the overall chip, improving the reliability, and lowering the cost. The electrical performance of antennas and circuitry in the flip-chipped scenario will be investigated; the near-by ground plane effect on both the passive and active components is a concern and will also be investigated.

This thesis will discuss the design procedures for both the passive antennas and the active power amplifier circuits, as well as the direct matching of the antenna and the amplifier. Active antennas will be designed on a GaAs chip and fabricated through a commercial foundry. Several issues will be addressed: (1) performance and size reduction of the antenna; (2) power amplifier performance in the flip-chip environment; (3) active antenna performance compared to the passive antenna; and (4) the matching and the interactions between the active circuitry and the radiating antenna.

1.5 Overview of Thesis

This chapter has presented the background and motivation for on-chip integration of electrically small antennas in wireless microsystems. The second chapter will cover small microstrip antenna theory and design issues. Antenna size reduction and impedance matching will be investigated, as well as the GaAs technology used to realize the integrated antenna solutions. The power amplifier design will be discussed in the Chapter Three; the power amplifier performance is simulated using HP EESOF Series IV [19]. Measurement results of active devices (MESFETs, power amplifiers), and passive devices (inductors, bondwires, backside vias, and coplanar transmission lines) will be presented in Chapter Four. Chapter Five will present measured performance of both passive and active antennas. Chapter Six will present conclusions drawn from this work and suggest directions for future research.

Chapter 2

Design of Small Microstrip Antennas

This chapter will cover design issues regarding electrically small microstrip patch antennas. First, the structure and radiating mechanisms of conventional patch antennas will be discussed. Then antenna properties such as bandwidth, efficiency and related design trade-offs will be covered. Next, issues and limitations of electrically-small antenna integration on an IC chip are considered. In this work, a high ε_r substrate is used to reduce the guided wavelength which helps to reduce the antenna size. The patch antenna is also shorted to ground along one side to further reduce the overall antenna size. A 5× scaled prototype antenna was fabricated on a Duroid substrate to validate the simulation results. Measured performance of this prototype is presented.

2.1 Microstrip antennas

2.1.1 Basic theory of microstrip antennas

A conventional microstrip antenna (Figure 2.1) consists of a metal patch placed on a thin grounded substrate with dielectric constant ε_r [20][21]. Figure 2.2 shows a side views of a conventional rectangular half-wavelength ($L = \lambda_g/2$) microstrip patch antenna fed by a microstrip line. As the RF current flows on the patch, an EM

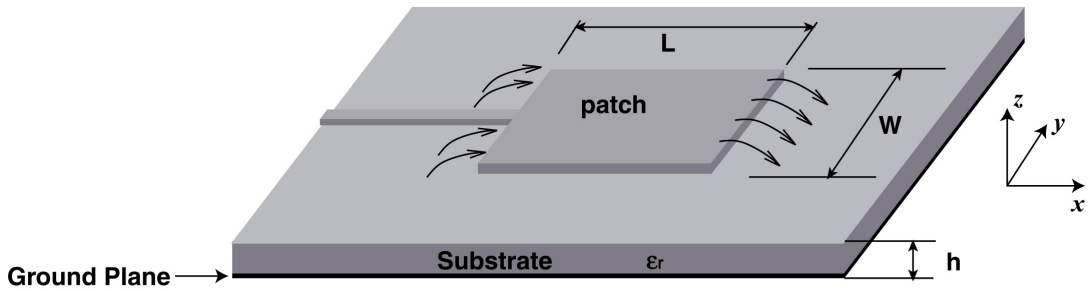


Figure 2.1: A half wavelength microstrip patch antenna.

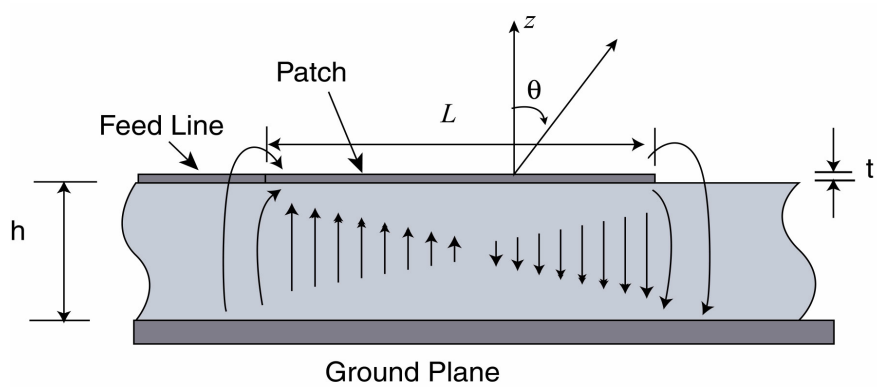


Figure 2.2: Side view of a half wavelength microstrip patch antenna.

wave is coupled to the substrate. Applying the EM boundary conditions, the E-field is perpendicular to the ground plane at the substrate to ground interface, and perpendicular to the patch at the patch-substrate interface. At the edge of the patch, there are discontinuities between the metal, substrate and air, resulting in fringing fields. These fringing fields contribute to the radiation of the microstrip antenna and also tend to increase the effective length of the antenna.

The fringing fields can be modeled as two radiating *slots* (magnetic current elements) formed at the two ends of the patch, separated by $\sim \lambda_g/2$. The patch and the ground plane form a microstrip transmission line. The guided wave experiences a 180° phase shift through the patch. The z components of the fringing fields will cancel each other in the far field since they are 180° out of phase with each other. On the other hand, the x-components of the fringing fields are in phase (as shown in Figure 2.3)

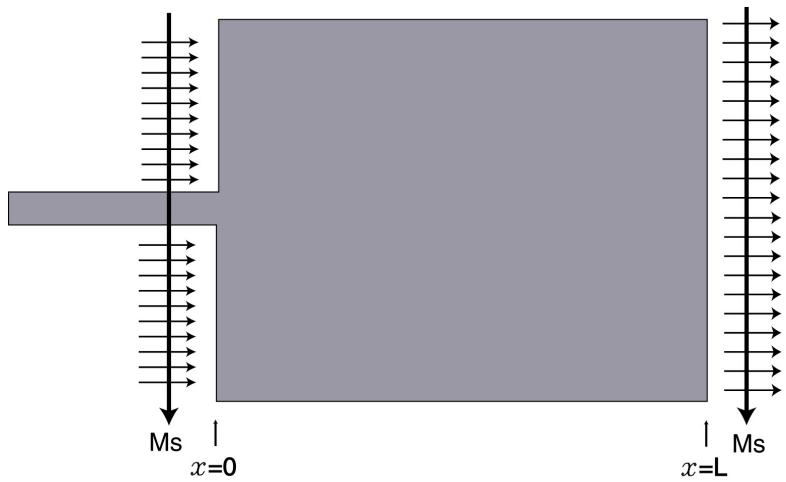


Figure 2.3: Top view of a half wavelength microstrip patch antenna showing fringing fields and equivalent magnetic current elements.

and separated by $\lambda_g/2$. From the equivalence principle, each slot can be modeled as a magnetic dipole:

$$\overrightarrow{M_S} = \begin{cases} -2\widehat{n} \times \overrightarrow{E_x} & at\ each\ end\ of\ the\ patch \quad (x = 0, x = L) \\ 0 & elsewhere \end{cases} \tag{2.1}$$

where $\widehat{n}$ is the normal direction to the patch. Therefore, a two-element array is formed by the two radiating slots. The far-field radiation will be in-phase along the z-direction, resulting in broadside radiation which is normal to the microstrip patch.

The field under the patch can be modeled as a cavity defined by two electric conductors (patch and ground plane) and magnetic walls around the perimeter of the patch. From the field distribution, the directivity, radiation conductance, and resonant frequency can be calculated. By solving Maxwell's equations for a rectangular patch of width (w) and length (l), the resonant frequency is:

$$f_{mn} = \frac{1}{2\pi\sqrt{\mu_0\varepsilon}}\sqrt{\left(\frac{m\pi}{l}\right)^2 + \left(\frac{n\pi}{w}\right)^2} \tag{2.2}$$

where $m = 0, 1, 2, 3\ldots$ and $n = 0, 1, 2, 3\ldots$. If $l > w, (m, n) = (1, 0)$ gives the fundamental mode resonant frequency:

$$f_{10} = \frac{1}{2l\sqrt{\mu_0 \varepsilon}} \tag{2.3}$$

However, this modeling technique cannot be used to calculate antenna input impedance. For this, full-wave techniques such as the method-of-moments (MOM) must be used.

Microstrip antennas typically have small bandwidths (on the order of $< 1\%$ to $\sim 5\%$), placing them to the resonant antennas category. Their bandwidth can be improved by increasing the thickness of the substrate (h), or using a lower dielectric constant substrate. However, this approach could increase losses due to surface wave radiation. Other methods to increase the bandwidth include defining slots in the patch to increase the inductance, or by adding reactive components to reduce the voltage standing wave ratio [22]. The radiation efficiency:

$$\eta_{rad} = \frac{Total\ radiated\ power}{Net\ Input\ power\ to\ Antenna} \tag{2.4}$$

of microstrip antennas can be improved by increasing the thickness of the substrate, or by using a lower dielectric constant material for substrate. However, this increases the size of antenna and may obviate on-chip integration.

2.1.2 Common Shapes

Microstrip patch antennas can be made in a variety of different shapes; square, rectangular, circular, and elliptical patches are commonly used because they are simple to fabricate and analyze. Microstrip antennas can be made on a single layer dielectric substrate, or a sandwiched multilayer substrate. The latter is a more complex structure, but offers some desirable features. For example, an electromagnetically-coupled microstrip patches in a stacked configuration with an additional parasitic radiating element can be designed to provide improved bandwidth, higher gain and dual-frequency operation.

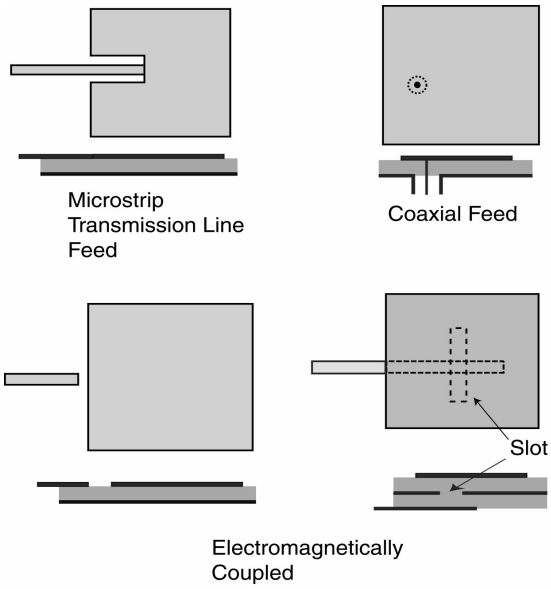


Figure 2.4: Microstrip antenna feeding structures.

2.1.3 Feeding Structure

Several different methods have been developed to feed microstrip antennas. These methods can primarily be divided into three groups based on the coupling scheme and the specific patch structure:

1) The patch can be fed using a microstrip transmission line with narrower width (Fig. 2.4). The input impedance (Z_{in}) can be set by the location of the feed point (inset). Microstrip impedance transformers can also be included to match the antenna Z_{in} to the system impedance Z_o.

2) A coaxial cable with its center conductor attached to the patch through the substrate and its ground shield attached to the system ground. The feed point is chosen to match the characteristic impedance of the coaxial cable.

3) The patch can be electromagnetically coupled to the feed line on the same layer or a different layer, or through aperture coupling in a stacked structure.

For the direct feeding (microstrip feed and coaxial), the input impedance of the antenna can be modified by changing the position of the feeding. As for the electromagnetically coupled structure, more design parameters are available to adjust the

input impedance.

2.1.4 Substrate Radiation

There are two substrate radiation mechanisms that must be considered when designing the microstrip antenna: surface waves and leaky waves [22][23].

EM waves coupled to the substrate can become trapped inside the dielectric layer as surface waves. Surface waves steal part of the antenna input energy, thereby contributing to the loss of the antennas (or other circuits). Surface waves result from a total internal reflection mechanism with most of the field contained near or in the dielectric layer. The field becomes tightly bound to the dielectric at higher frequencies [24].

Surface waves in a grounded dielectric substrate exist in the form of TE and TM modes. The phase velocity of these modes is a function of dielectric constant (ε_r) and substrate thickness (h). If a quasi-TEM wave is present under the microstrip patch with a phase velocity close to the phase velocity of a surface wave mode, strong mode coupling can occur. The lowest-order TM_0 mode has zero cut-off frequency, but power loss to this mode can be minimized by making the substrate thinner or using a lower ε_r material. For higher order TE & TM modes, the cutoff frequency is given by:

$$f_c = \frac{nc}{4h\sqrt{\varepsilon_r - 1}} \tag{2.5}$$

where c is the free space velocity of light, $n = 1, 3, 5...$ for TE_n modes and $n = 2, 4, 6\ldots$ for TM_n modes. Generally speaking, the substrate thickness must be chosen to avoid coupling to the first higher surface wave mode.

Surface waves can in turn lead to leaky wave radiation. Such leaky waves leak from substrate to air; leaky waves will increase the side lobes and cross polarization levels, as well as the end fire radiation [25].

2.1.5 Loss

Two dominant loss mechanisms in patch antennas are conductor loss in the metal, and dielectric loss in the substrate. Dielectric loss is typically expressed using the loss tangent:

$$\tan\delta = \frac{2\sigma}{\varepsilon f} \tag{2.6}$$

where σ is the electrical conductivity, ε is the dielectric constant, and f is the frequency. Conductor loss depends strongly surface roughness and frequency. The roughness of metal can be reduced by choosing a substrate that allows deposition of a very smooth metal surface. As the frequency increases, the skin depth will decrease. Therefore, conductor loss will be more severe at higher frequencies. Dielectric loss depends on the dielectric constant and loss tangent of the substrate; the loss tangent increases with frequency. Generally speaking, the dielectric loss is lower than the conductor loss at microwave frequencies and can be reduced by using low-loss materials.

The dielectric loss for a microstrip line is given by [24]:

$$\alpha_d = \frac{k_0 \varepsilon_r (\varepsilon_e - 1) \tan\delta}{2\sqrt{\varepsilon_e}(\varepsilon_r - 1)} \; Np/m \tag{2.7}$$

where k_0 is the free space wave number $2\pi/\lambda_0$, ε_e is the frequency-dependent effective dielectric constant, ε_r is the substrate dielectric constant, and λ_0 is the free-space wavelength.

The attenuation due to conductor loss for microstrip line is given by [24]:

$$\alpha_c = \frac{R_s}{Z_0 W} \; Np/m \tag{2.8}$$

where $R_s = \sqrt{\omega\mu_0/2\sigma}$ is the surface resistivity of the conductor.

2.2 Integrated Electrically Small Antenna Concept

In the last section, the basic theory of microstrip antennas was discussed. This will serve as a reference for the following discussion on designing electrically small

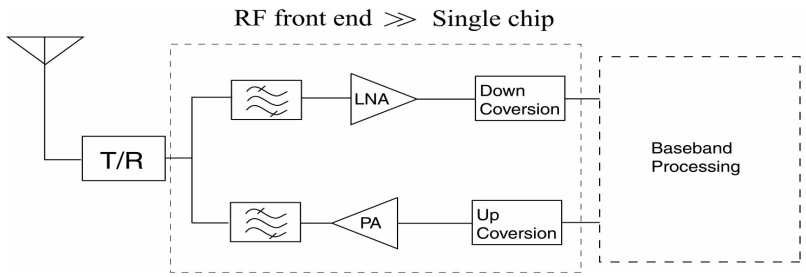


Figure 2.5: A transceiver chip set.

microstrip antennas, including how to choose the structure and materials to maximize performance.

2.2.1 Microstrip antenna for IC integration

As mentioned in the introduction, IC technologies have been improving dramatically over the past several decades, producing smaller and higher density circuits. The wireless industry has directly benefited from this growth in the pursuit of highly integrated transceivers. Indeed, there is a trend toward a "single-chip radio"(Figure 2.5), where all the functions of a transceiver are integrated into the same IC chip (RF, digital & analog).

Bearing this in mind, this research focuses on the possibility of integrating the antenna itself on the radio chip. The microstrip antenna is a very good candidate for IC integration because it offers advantages such as planar structure, low profile and ease of fabrication. However, physical laws rather than IC technology scaling govern the antenna dimensions; antenna size cannot be arbitrarily reduced without suffering a degradation in performance. Since the microstrip patch antenna is a resonant antenna, its size is generally about half a guided wavelength. As a matter of fact, resonant antennas have been integrated on chip in the millimeter wave regime given the much smaller guided wavelength at those frequencies [3][4]. However, at RF/microwave frequencies, the wavelengths are relatively long. For example, the free space wavelength at 5.6 GHz is about 53.6 mm, much larger than the size of a typical RF IC transceiver.

As has been observed, the use of a high dielectric constant substrate material will

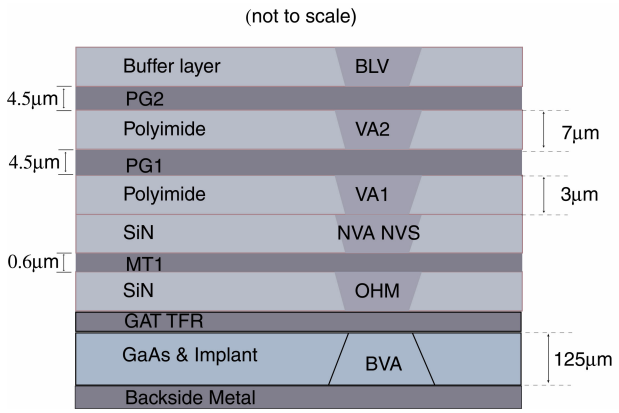


Figure 2.6: MA-COM 5A GaAs SAGFET process stack-up (thickness not to scale).

lead to a shorter guided wavelength, thus reducing the size of a resonant patch. However, the use of a high dielectric constant substrate is detrimental to the antenna radiation properties. Surface wave loss is of concern since it tends to increase with the dielectric constant and will reduce the radiation efficiency and increase the sidelobe levels. These effects must be considered in the antenna design.

In this project, GaAs technology has been chosen for fabrication of the integrated antennas. GaAs offers a high dielectric constant ($\varepsilon_r = 12.9$) and low-loss properties. Silicon also has a high dielectric constant ($\varepsilon_r = 11.7$), but is typically only available as a low-resistivity substrate resulting in higher dielectric losses. High-resistivity Si substrates can be realized, although they are typically not compatible with BiCMOS electronics (however, this is changing). The antenna is designed to be inductively loaded, i.e. it has one side of the patch shorted to the ground using vias, such that its size is reduced by half compared to the open ended patch antenna. Other low-loss substrates (quartz, alumina) could be used as long as backside vias are possible in the given technology.

The M/A-COM 5A GaAs MESFET process [26] ($125\mu m$ thick substrate) with backside patterning was employed in this work to fabricate the integrated antennas. This is a standard three metal layer process with a $125\mu m$ GaAs substrate (Fig. 2.6), one thin metal layer (M1) and two plated gold layers (PG1 and PG2). The GaAs semi-insulating substrate has a relative permittivity (ε_r) of 12.9 and dielectric loss tangent ($\tan\delta$) of 0.0005. Backside vias (BVA) can be fabricated through the substrate con-

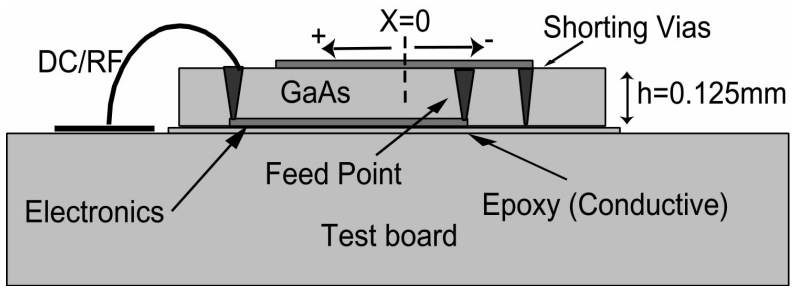


Figure 2.7: Two-dimensional side view of the chip mounted on the test board.

necting top metal layers to the backside metal for purpose such as grounding the source of a MESFET. Substrate thinning is required to achieve good repeatability and yield from the via process. The metal layers can be used for passive components, active components, or interconnections. Both PG1 and PG2 layers are 4.5μm thick; they are capable of handling large current densities and have relative low resistive loss. The metal 1 layer is 0.6μm thick and supports less current density compared to PG1 and PG2. The metal layers are separated by different inter-metal dielectric layers and can be connected using vias. There is a polyimide layer ($\varepsilon_r = 2.9$) with thickness of 7μm between the PG1 and PG2 layers. Between PG1 and MT1, there are two layers (polyimide 3μm and SiN 0.2μm). A optional buffer layer ($\sim$10μm) can be fabricated on top of the PG2 to protect the chip. Openings in this layer are used for typical bondwire connections, probe pads, etc. The backside patterning includes several steps: (1) the wafer is mounted and thinned; (2) via holes are formed; and (3) backside metallization (electroplating) is performed.

As shown in Figure 2.7, for this project the chip will be mounted face-down on the printed circuit test board using conductive silver epoxy; a dielectric layer separates the interconnects and electronics from the expoxied ground layer. Consequently, the patch antenna will be facing up and the electronics (e.g. transmit PA) will be facing down.

A side view of the proof-of-concept chip layers assignment is shown in Figure 2.8. One edge of the patch is grounded by a wall of shorting vias. The PG2 serves as the system ground layer. Since the electronics will be directly over the PC board (only separated by a thin epoxy layer), very good thermal dissipation could be realized. The RF input GSG bond pads on the backside of the chip will be wire bonded to

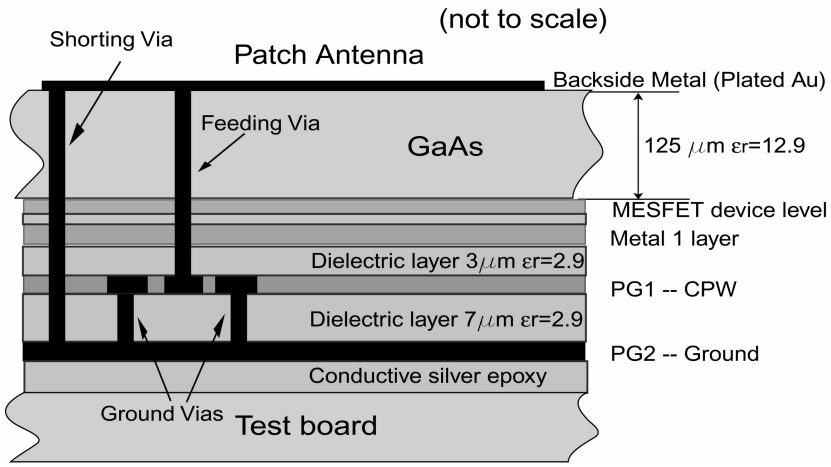


Figure 2.8: Two-dimensional side view of the proof-of-concept technology.

a 50 Ω coplanar transmission feeding line on the board. The input signal then goes through backside vias to the electronics side of the chip. The signal is fed to the RF circuitry (i.e. power amplifier) through a 50 Ω coplanar feed line. DC bias is distributed to the PA in a similar manner. The output of the power amplifier is then fed to the patch antenna at the appropriate feed point through another backside via.

The "flip-chip" configuration employed for the PA/antenna chip in this work requires that the top metal layer (PG2) cover the entire chip and serve as the ground plane. This is significantly different from the standard chip structure where PG2 is normally used for interconnections or passive components. In this case, the ground plane is located 7 to 10μm away from the passive and active devices fabricated on the front side of the chip which in turn will be affected by the nearby ground plane. This effect will change the device characteristics. Passive components such as transmission lines and inductors were therefore modeled in this work using IE3D [27]. The simulated S-parameters of these components were subsequently used in the circuit CAD software for simulating overall circuit performance.

2.2.2 Microstrip patch with Shorting Vias

The microstrip antenna resonant frequency can be tuned by inductive or capacitive loading of the patch. Antenna size can be reduced significantly by using inductive

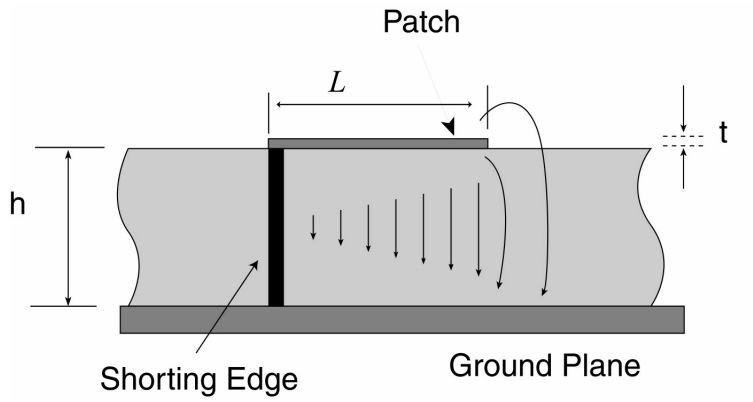


Figure 2.9: Side view of a quarter wave patch antenna with one side short circuit.

shorting posts to the ground. Normally, patch antennas have magnetic walls at both radiating edges. One approach used to reduce the antenna size is to apply shorting posts along one edge of the patch [28]. In this case, on the shorted side of the patch, there will be a minimum in the electric field (electric wall). On the other side of the patch, there will be a maximum in the electric field (radiating edge). This is equivalent to a half wavelength patch antenna cut in half. The physical size of the patch is therefore $\sim \lambda_g/4$.

The patch antenna in this work was designed to be a square shaped patch for the simplicity of modeling and simulation; the main purpose of this work is to show the integration of antenna and electronics using a commercial IC technology. The antenna size was estimated by using equation 2.9:

$$L = \lambda_g/4 = (\lambda_0/\sqrt{\varepsilon_r})/4 \tag{2.9}$$

For a GaAs substrate ($\varepsilon_r = 12.9$) at 5.6 GHz, the size of the patch $L = 3.73mm$ (the guided wavelength $\lambda_g = 14.9mm$). λ_g is calculated assuming the antenna has a $125\mu m$ GaAs substrate between the radiating patch and the ground plane. This simplified calculation only gives an estimated antenna size since in the actual structure there exists a $\sim 10\mu m$ polyimide layer ($\varepsilon_r = 2.9$) above the ground plane (PG2) under the GaAs substrate. The polyimide layer increases the overall λ_g, resulting in larger patch size. Therefore, the antenna was simulated using a full-wave EM program (MoM) Zeland IE3D [27] to obtain more rigorous results. In addition, the

MoM simulations provide accurate information concerning antenna input impedance.

2.3 Antenna Design

Zeland IE3D is a full-wave, method-of-moments based electromagnetic simulator which can solve for the current distribution on 3D and multilayer structures of general shape. IE3D was used extensively in this work to simulate antenna and passive components. For the antennas, an infinite ground plane was used in the simulation to reduce the simulation time. Also, the shorting vias (spacing$<< \lambda_g$) at the edge of the patch were modeled by a shorting wall for the same reason. A comparison of simulation results using vias vs. using a shorting edge, showed that the difference is negligible.

2.3.1 Antenna size

Simulations of the antenna structure with a 125μm-thick GaAs-only substrate predicted a resonant length at 5.6 GHz of ~3.8mm, very close to the calculated results discussed above. When the two polyimide layers (~10μm total thickness) were added to the model, it was found that the resonant frequency was shifted higher (as expected). The patch size was increased to about 4.2 mm to give resonant frequency of 5.6 GHz.

2.3.2 Antenna characteristic vs. feed position

Antenna properties such as radiation efficiency, pattern, directivity etc. are mainly affected by the antenna structure and the substrate material. The antenna input impedance strongly depends on the feed position. This was investigated thoroughly using IE3D by adjusting the feed position from the radiating edge to the shorting edge as shown in Figure 2.10. Simulations were performed for different feeding positions away from the center of the patch (x=-1.5 mm, -1.4 mm, -1.3 mm, -1.2 mm, -1.05 mm, -0.5 mm, 0 mm, and 0.5 mm) to examine how the input impedance and radiation efficiency are affected by the feeding position.

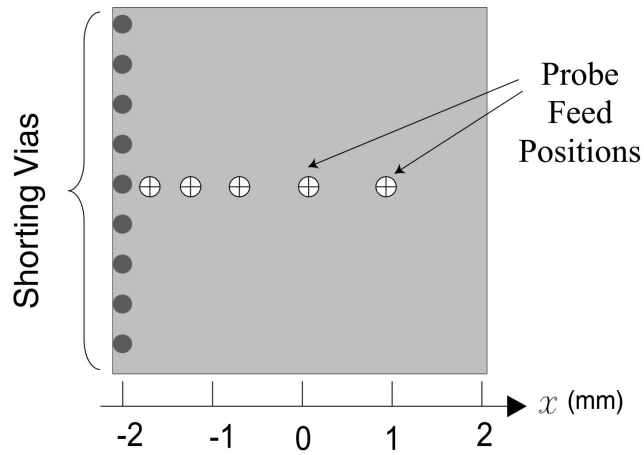


Figure 2.10: Top view of a quarter wavelength microstrip patch antenna.

The radiation efficiency η_{rad} is given in Eq. 2.4; this does *not* include the impedance mismatch at the input port of the antenna (return loss). The overall antenna efficiency η_{ant} is defined as:

$$\eta_{ant} = \frac{Total\ radiated\ power}{Incident\ Power\ from\ source\ at\ input\ of\ antenna\ feedline} \tag{2.10}$$

and *does* include the input return loss. These efficiency definitions will be used throughout this chapter.

Figure 2.11 shows a plot of radiation efficiency vs. frequency for different feeding positions. A relatively flat range at an efficiency of about 3.6% exists for $f \simeq 5.6$ $GHz - 10$ GHz with feeding position $x = 0$ (center of patch). This region could be moved to a lower frequency range by increasing the antenna size. The radiation efficiency is low due to several reasons: (1) the higher dielectric constant material lowers the radiation resistance; (2) at higher frequencies, the conductor losses become more significant; (3) the high ϵ_r, thin substrate couples more of the field to ground resulting in much smaller radiating (fringing) fields. Another way of looking at (3) is that more of the fields are trapped in the cavity formed under the patch; in other words the antenna has a high radiating Q [29].

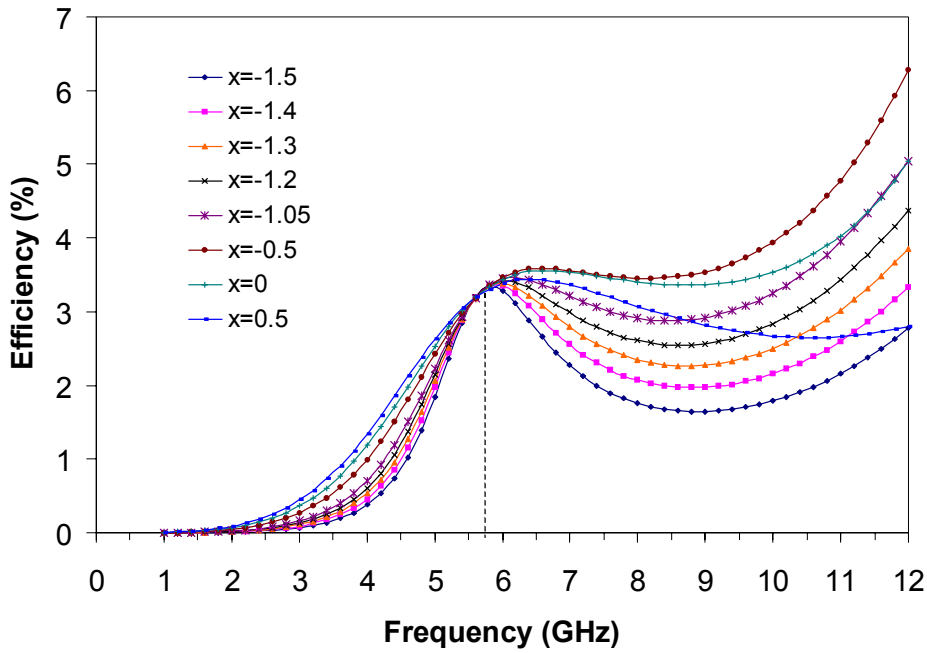


Figure 2.11: Simulated radiation efficiency vs. frequency at different feeding positions.

To evaluate the effect of the dielectric constant and thickness of the substrate material on the antenna radiation efficiency, the quarter-wavelength patch antenna was simulated using IE3D with various substrate parameters. The antenna size was scale to $\sqrt{\varepsilon_r}$ to keep the resonant frequency at ~5.6 GHz. One group of simulations were performed with the substrate thickness also scaled by $\sqrt{\varepsilon_r}$; the second group of simulations were performed with substrate thickness = 125 μm. For both groups of simulations, the radiation efficiency drops significantly when ε_r ranges from 1 to 12.9 (Fig. 2.12). The antenna with substrate thickness varying with $\sqrt{\varepsilon_r}$ exhibits higher radiation efficiency due to the thicker substrate. With the higher dielectric constant substrate, the fields are more confined under the patch resulting in lower radiation efficiency.

The antenna input impedance is composed of real and imaginary parts:

$$Z_A = R_A + jX_A \tag{2.11}$$

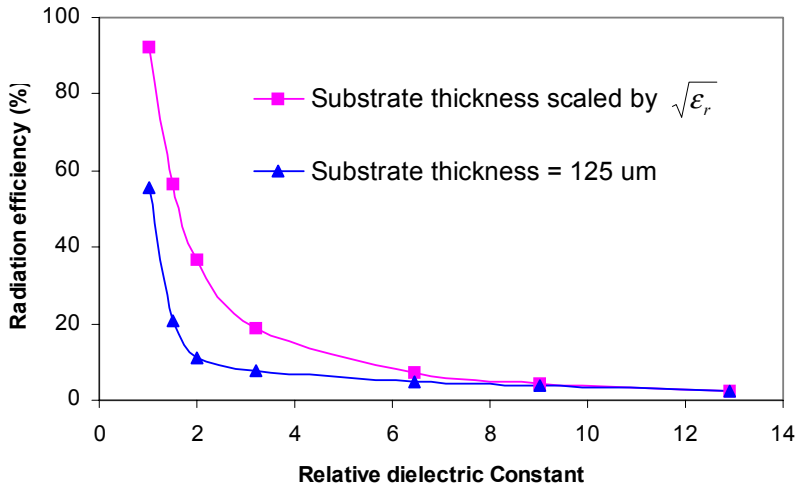
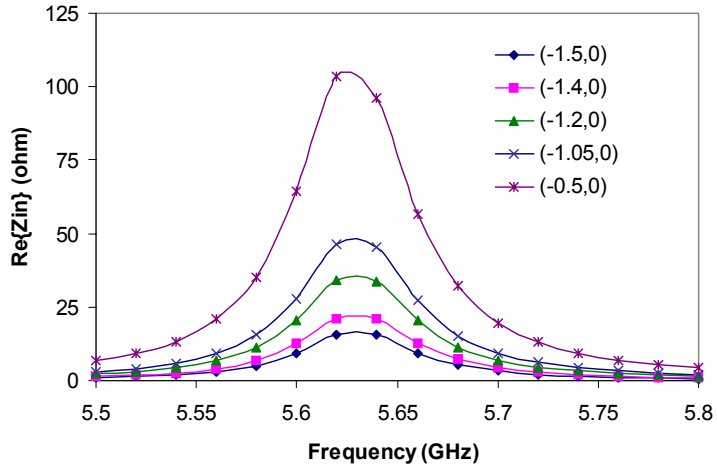


Figure 2.12: Simulated radiation efficiency vs. substrate relative dielectric constant and thickness.

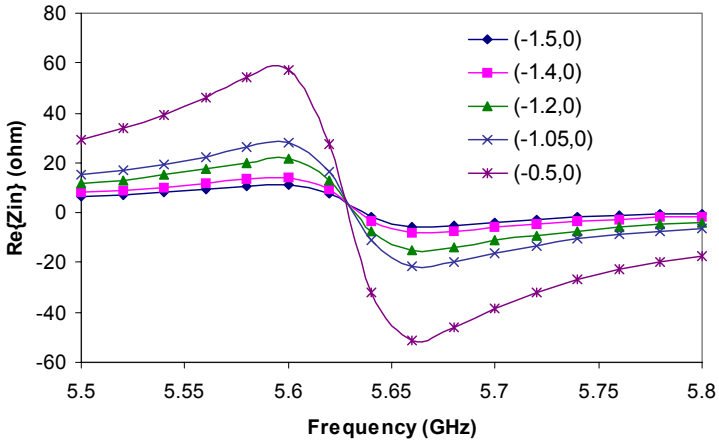
The real part R_A has two terms: (1) the power radiated or coupled to other modes (radiation resistance); (2) the ohmic loss associated with the antenna structure. The imaginary part represents the power stored in the near field of the antenna. For maximum power transfer to the antenna, the antenna input impedance should be equal to complex conjugate of the output impedance of the previous stage. It is typically desired to design an antenna with a 50 Ω input impedance in order to match standard RF components. However in this project, since the electronics and antenna are co-designed on the same chip, it is not strictly necessary to have the antenna Z_{in} and electronics Z_{out} designed to be 50 Ω. Instead, other values could be used to improve the design and while still delivering maximum power to the antenna.

As the feed position moves from the radiating edge to the shorting edge, the input impedance of the antenna changes accordingly. The simulated real and imaginary parts of the input impedance vs. frequency curves at different feed positions are shown Figure 2.13(a) and Figure 2.13(b).

As the feed moves towards the shorted edge, the magnitude of input impedance drops gradually. By choosing a specific feed position, the antenna can be designed to have a desired input impedance, effectively becoming part of the matching network of the



(a)



(b)

Figure 2.13: (a) Re(Z_{in}) and (b) Im(Z_{in}) vs. frequency and feeding point position (x, y in mm).

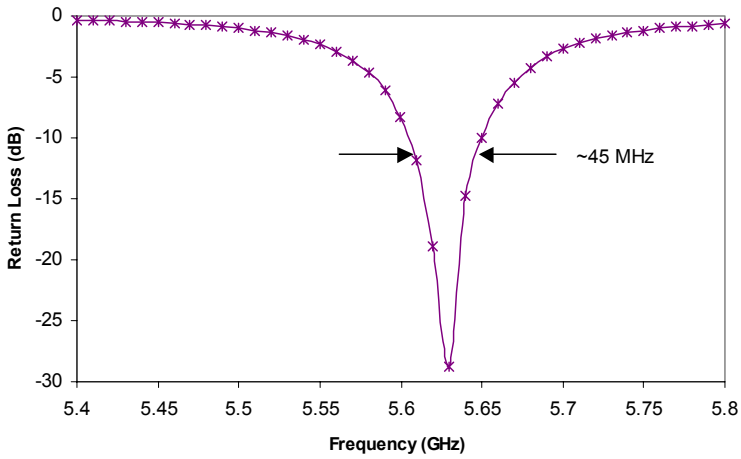


Figure 2.14: Simulated return Loss vs. frequency (50 Ω system).

previous stage. At the resonant frequency, the antenna presents a purely real input impedance. By offsetting slightly from the resonant frequency, the imaginary part of the input impedance could be tuned to different values. Moving the feed position in y direction has no significant effect on the antenna input impedance and efficiency.

Using the design curves [Figures 2.11 - 2.13] and tuning the feeding position, an antenna resonant at 5.63 GHz with 50 Ω input impedance was designed. The feeding position was x = 1.05mm (Figure 2.10). Simulated results (Figure 2.14) show that the antenna design has a minimum return loss of 28 dB at 5.63 GHz and a 10 dB return loss bandwidth of about 45 MHz ($\sim$ 1% Bandwidth), which would be practical for low-to-moderate data rate communications. The narrow bandwidth could also serve as a filter, potentially blocking unwanted spurious radiation.

Given the antenna efficiency of 3.2%, the antenna has a gain curve peaking at -10.1 dB with a 3 dB gain bandwidth of 135 MHz (2%) (Figure 2.15). The antenna gain is relatively low compared with conventional patch antennas because the thin high ϵ_r substrate couples fields strongly to ground resulting in much smaller radiating (fringing) field. The antenna has a maximum directivity of 4.8 dBi. The E-plane and H-plane gain patterns (Figure 2.16) are similar to conventional microstrip patches, except with a higher peak cross polarization (~ -12 dB).

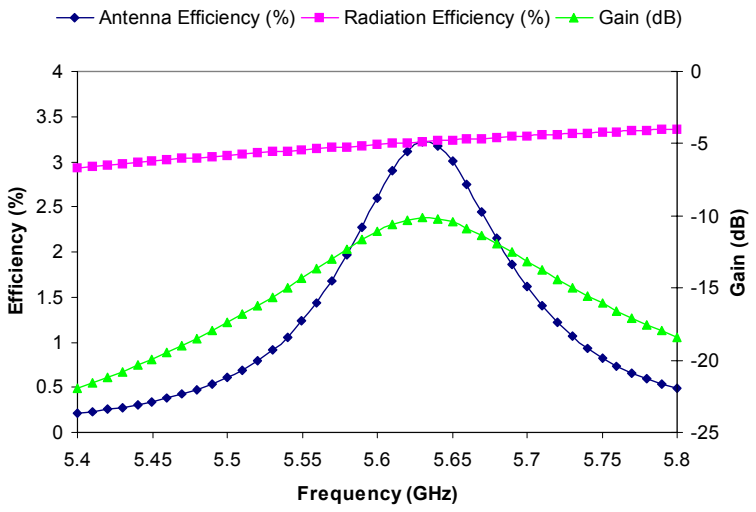


Figure 2.15: Simulated radiation efficiency, antenna efficiency and gain of 50Ω antenna.

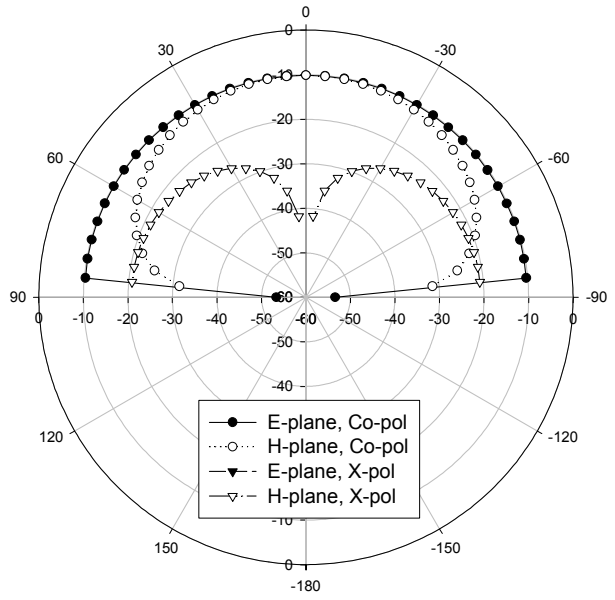


Figure 2.16: Simulated gain patterns (50 Ω GaAs antenna), Co-pol & X-pol.

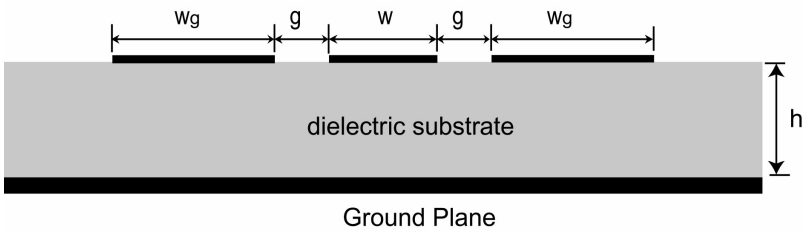
2.4 Transmission line feeds to the patch

In the case of the 50 Ω antenna design, the output of the RF electronics (e.g. a power amplifier) will feed the patch through a 50 Ω coplanar transmission line and backside vias. In addition, 50 Ω lines will be used at the RF input to the electronics. This section discusses the design of these feedlines.

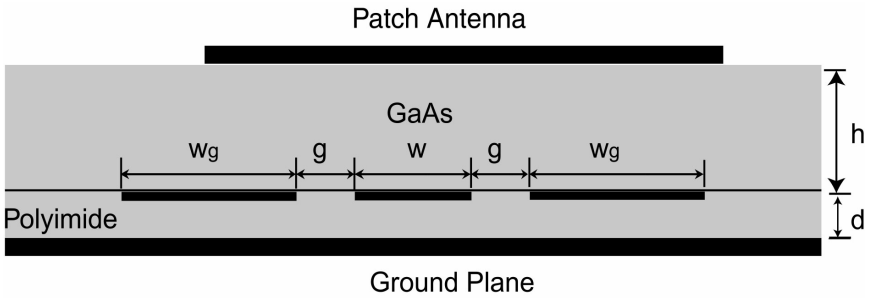
2.4.1 Coplanar Waveguide

Coplanar waveguide (CPW) is a popular transmission line choice for microwave/mm-wave integrated circuit applications. It is composed of a center conductor in close proximity to two coplanar ground planes on either side [Fig. 2.17(a)]. Normally the substrate thickness (h) is large compared to the gap, and the electric field lines are confined between the center conductor and the coplanar ground planes. The CPW line can support even (slotline) or odd (CPW) quasi-TEM modes, depending on whether the E-fields in the two slots are in opposite directions or same direction [24]. The odd mode is the desired mode for most applications. For typical CPW lines, Z_0 is mainly affected by the ratio of the center conductor (w) and the overall line width (w+2g). In the "flip-chip" structure used in this work, the CPW lines are located very close to the lower ground plane [Fig. 2.17(b)]. This complicates the modeling of the CPW line performance, necessitating the use of full-wave techniques in the design process.

CPW was chosen for the transmission line interconnections in this project for the ease of future transition to flip-chip applications. The CPW lines are designed to be fabricated in the PG1 layer (Fig. 2.8), which is separated from the ground by 7 μm of polyimide. The coplanar waveguide structure was simulated using IE3D. A plot of the characteristic impedance and effective dielectric constant vs. the width of the center conductor (w) is shown in Fig. 2.18(a). The minimum gap design rule for the PG1 layer is 6 μm. To be safe, an 8μm spacing was adapted for the CPW gaps (g=8μm). Since the polyimide thickness (d) is comparable to the gap (g) between the center and the ground conductor of the CPW, both the microstrip mode and the CPW mode will be present in the structure. For simplicity, the width of the adjacent ground planes (w_g) is set to w_g=w+2g. The 50 Ω CPW is designed by varying the width of the center conductor, therefore varying the ratio of w/(w+2g). As shown

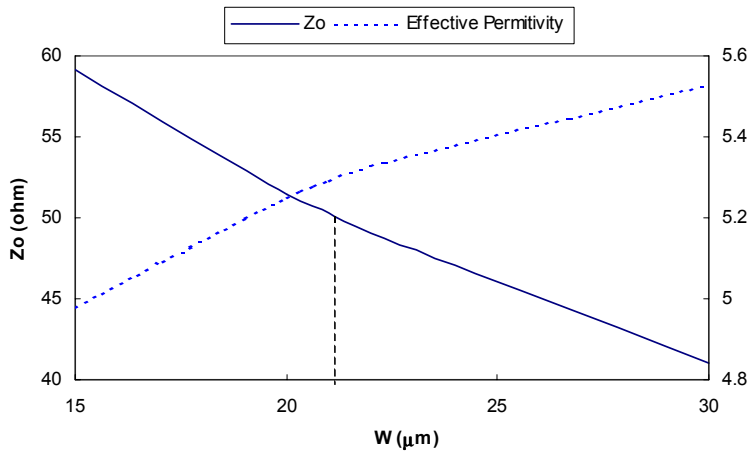


(a)

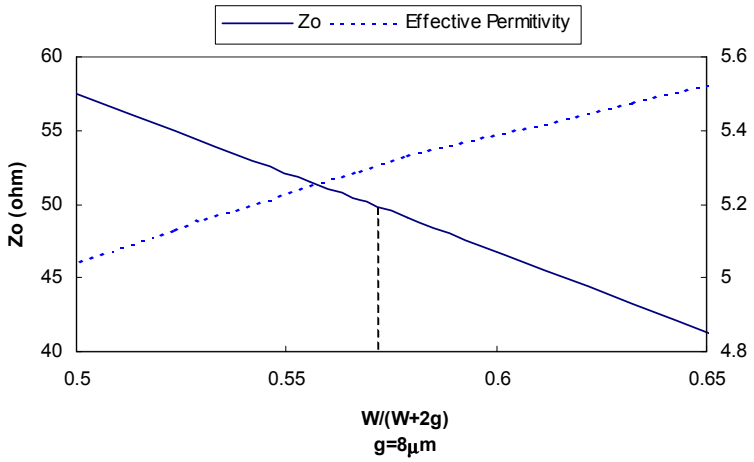


(b)

Figure 2.17: (a) Cross-sectional view of a conventional coplanar transmission line; (b) Cross-sectional view of a coplanar waveguide transmission line with a nearby ground plane.



(a)



(b)

Figure 2.18: (a) Characteristic impedance and relative permitivity of CPW vs. width; (b) Characteristic impedance and relative permitivity of CPW vs. w/(w+2g)

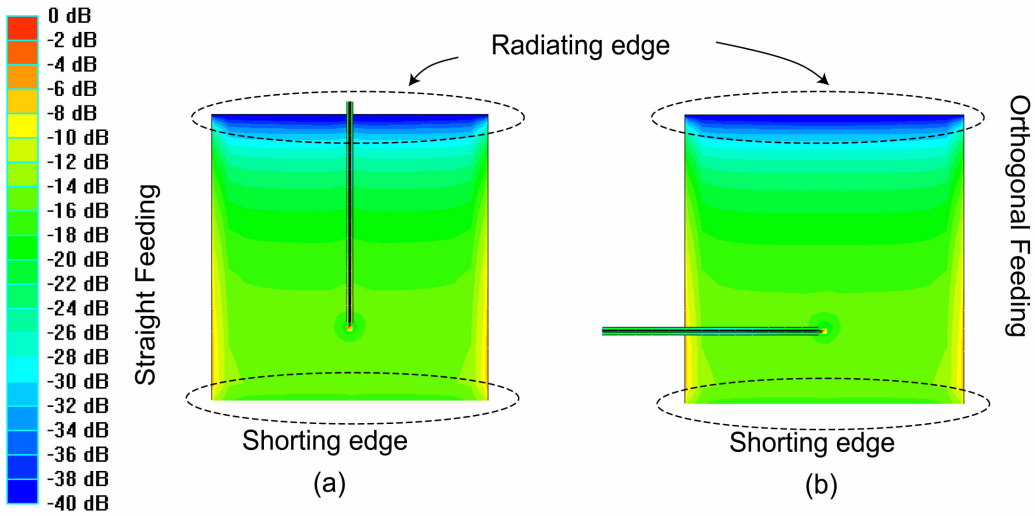
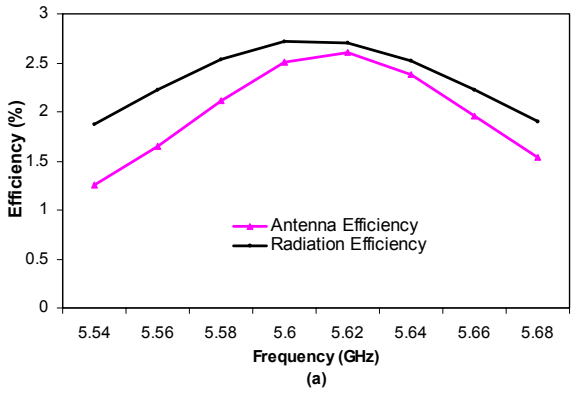


Figure 2.19: Top view of chip-scale patch antennas: direct feed vs. orthogonal feed.

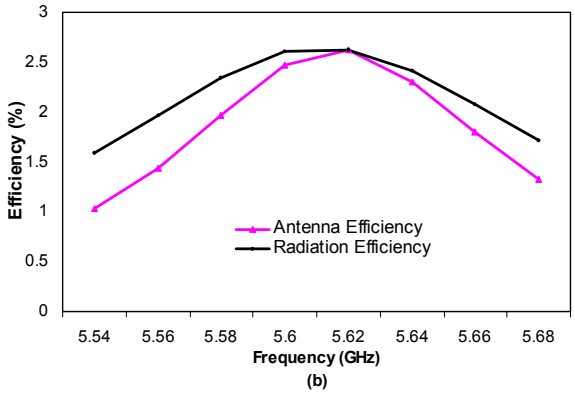
in Figure 2.18(b), as the ratio of w/(w+2g) increases, the characteristic impedance will decrease and the effective dielectric constant will increase. The 50 Ω CPW line dimension can be found from the plot (w=21μm, g=8μm, w_g=37μm).

2.4.2 Direct (symmetric) feeding vs. orthogonal feeding to the antenna

Two different feeding topologies (Fig. 2.19) were investigated: direct feeding vs. orthogonal feeding. The current density distribution on the patch is shown in the gray scale: darker corresponds to lower current density while brighter corresponds to higher current density. On the radiating edge, the current density is lower. The radiating edge is equivalent to an open circuit, so the current experiences a null and the voltage reaches its maximum. At the shorting edge, the current density is high and reaches its maximum, while the voltage reaches its minimum. The orthogonal feeding topology avoids interference between the feeding path and the antenna radiating edge, and is better from the layout point of view. Specifically, the RF electronics can be located away from the radiating edge to avoid potential interference. The efficiency vs. frequency plot for the two feeding topologies is shown in Figure 2.20. The orthogonal feeding shows slightly higher radiation efficiency than the straight



(a)



(b)

Figure 2.20: Chip-scale patch [(4.2mm by 4.2mm, feed position (-1.05,0)], radiation and antenna efficiency. Results include feedline losses. (a) direct feeding. (b) orthogonal feeding.

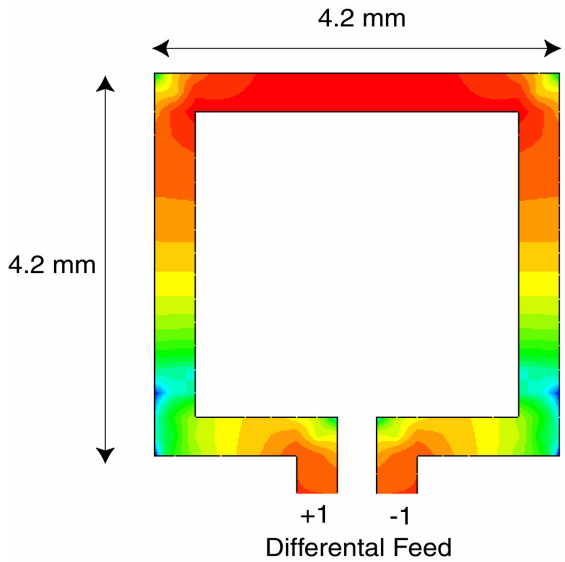


Figure 2.21: Small loop antenna on GaAs (h = 0.125 mm).

feeding. Its antenna efficiency is slightly lower due to the mismatch loss, but this can be tuned out in a straightforward manner by slightly varying the feed position.

2.5 Alternate Shaped Antennas

Other alternate small antenna structures (Figure 2.21 - 2.24) were also simulated, such as loop and spiral shaped antennas. The dimensions were chosen to be similar to the scale of the integrated patch antenna discussed above. In these cases, differential signals were applied at the inputs of the antennas. The resulting efficiencies are lower than for the microstrip patch antennas over the frequency range of interest. More importantly, the input impedance is almost purely reactive in the frequency band of interest, making it very hard to match with the electronics, and resulting in very poor overall radiation efficiency. Slots antennas were not chosen because such antennas will tend to radiate preferentially into substrate modes due to the high dielectric constant GaAs substrate. Slot antennas may be practical on lower dielectric constant materials [30].

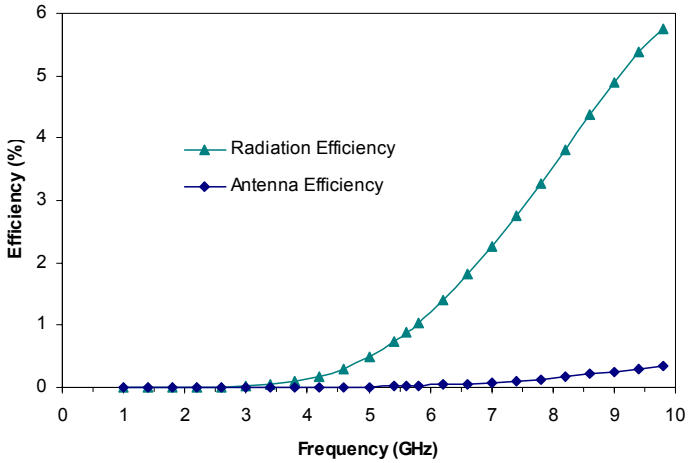


Figure 2.22: Radiation efficiency and antenna efficiency of the loop antenna shown in Fig. 2.21.

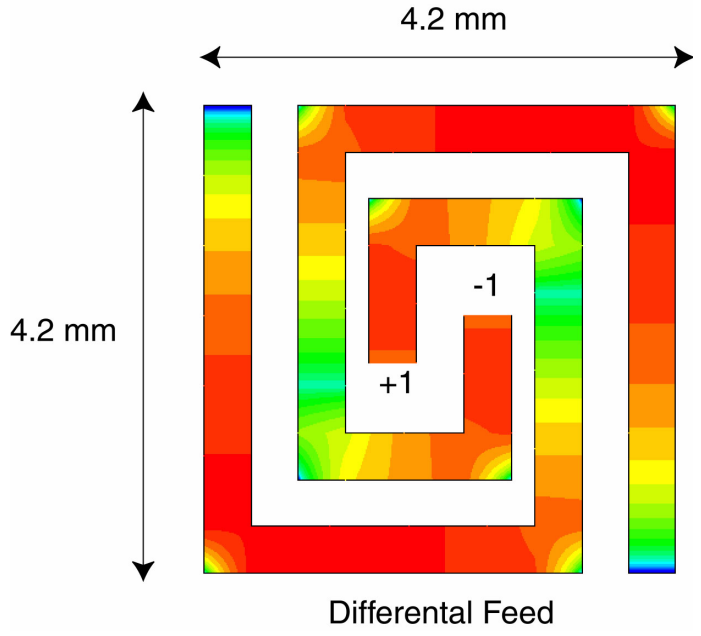


Figure 2.23: Small spiral antenna on GaAs (h = 0.125 mm).

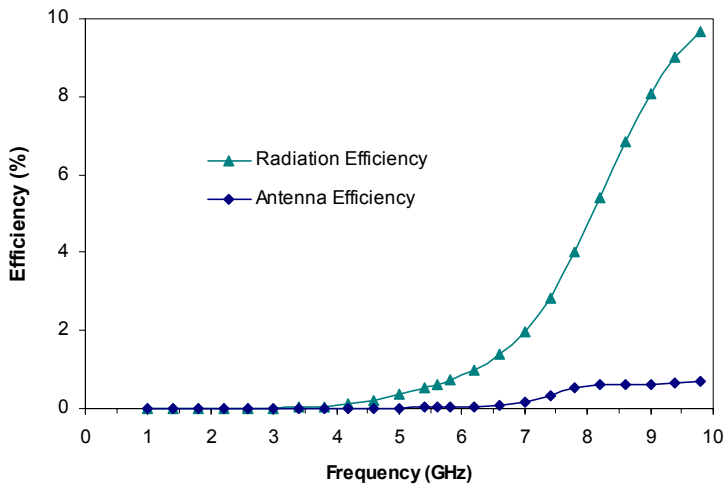


Figure 2.24: Radiation efficiency and antenna efficiency of the spiral antenna shown in Fig. 2.23.

2.6 Prototype fabrication and measurement results

Since IC fabrication is an expensive and complicated process, a prototype antenna was constructed to validate the simulation results (Fig. 2.25). A prototype 5X scaled model of the simulated antenna was simulated and then fabricated on a Duroid 6010 substrate (ε_r = 10.5, thickness = 0.635 mm $\sim$ 0.125 mm $\times$ 5). The scaled model patch size is 19 mm $\times$ 19 mm, about 5 times larger than the GaAs version. All the dimensions of the prototype were scaled roughly 5 times, including size of the antenna, substrate thickness, as well as metal thickness.

The prototype antenna had a measured return loss of is 30 dB at 1.1925 GHz ($\sim$1/5 of 5.6 GHz). The radiation pattern was measured using the VT Antenna Group anechoic chamber (AntCom Near-Far Field system). A standard gain antenna DRG-118A was used to calculate the gain values. The co-polarized and cross-polarized gain patterns are shown in Figure 2.26. The maximum measured prototype antenna gain is -7.7 dB; this is $\sim$3.3dB higher than the simulated antenna (on GaAs) gain of -10.9dBi. This measured gain for the prototype is higher than the simulated results (on GaAs) due to several factors: (1) the measured maximum directivity of the prototype antenna is 6.7dB, which is 1.9 dB higher than the simulated directivity (on GaAs)

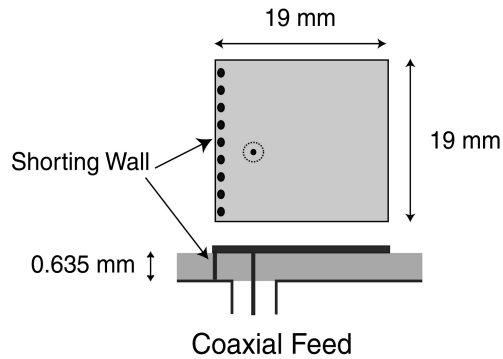


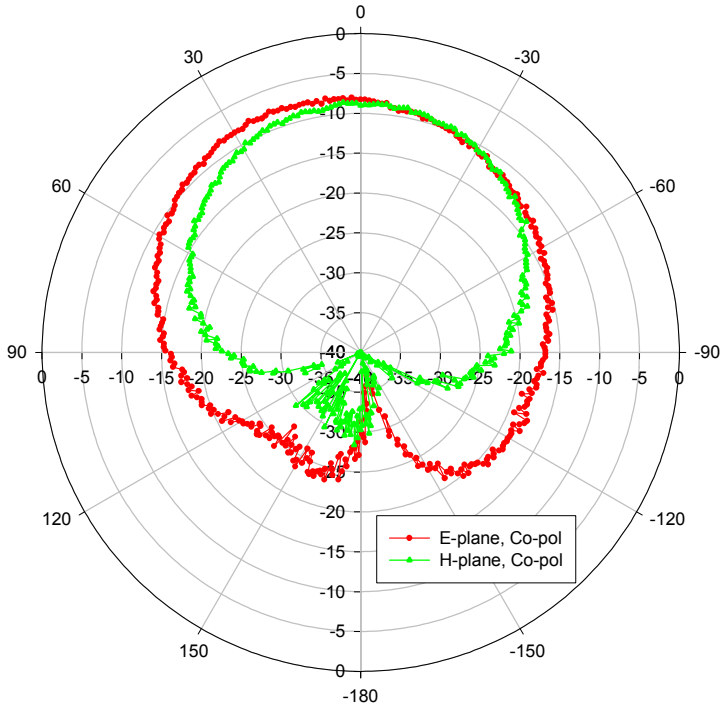
Figure 2.25: A prototype 5X scaled model fabricated on a $\varepsilon_r = 10.5$ Duroid substrate.

of 4.8dB; (2) the prototype is built on Duroid with an $\varepsilon_r = 10.5$ instead of GaAs with an $\varepsilon_r = 12.9$, resulting in a 1.7 dB gain increase; (3) the antenna measurement system error is ∼1dB.

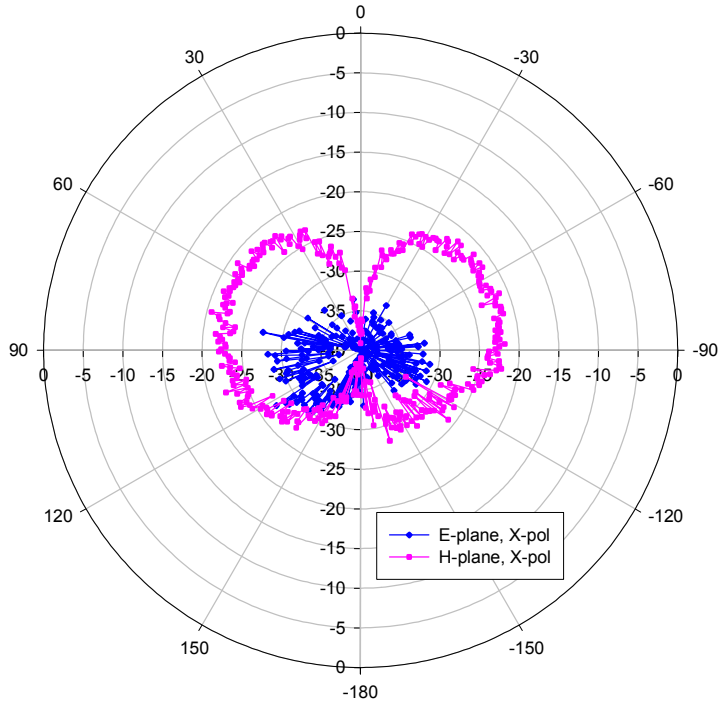
The simulated antenna pattern for the 50 Ω GaAs antenna is shown in Figure 2.16, and shows a peak cross polarization level ∼-21 dB. The measured radiation pattern for the prototype has a peak cross polarization level of ∼ -22 dB, which agrees reasonably well with the simulated results. The E-plane and H-plane Co-polarization pattern shapes also show very good agreement with the simulated results. It should be noted that the measured results show some amount of backside radiation. In the measurement, a large metal plate (∼12cm×12cm) is attached to the back of the prototype antenna in order to reduce the finite ground effect. But since the prototype antenna has a finite ground plane instead of an infinite ground plane (as was used to simulate the antenna), a small amount of backside radiation results. The backside radiation is relatively small compared to the broadside radiation, so the assumption of a infinite ground plane in the simulation is reasonably valid to predict the antenna performance while saving a great amount of simulation time.

2.7 Summary of the Chapter

The basic theory of microstrip antennas has been discussed as well as their advantages for on-chip integration. Design issues for electrically small patch antennas required for integration on a GaAs MMIC chip were discussed. Trade-offs between the antenna



(a)



(b)

Figure 2.26: Measured E and H plane radiation patterns of the 5× scaled prototype antenna at 1.1925 GHz: (a)Co-pol; (b) X-pol.

size and its electrical performance have also been addressed. Some alternate shaped antennas were simulated and compared with the microstrip patch antennas. A 5× prototype antenna was fabricated and measured, and the measured results are in good agreement with the full-wave EM simulations.

Chapter 3

Power Amplifier Design

In this chapter, the design and technology issues regarding the integrated RF power amplifier will be discussed. The considerations for the design of a power amplifier are quite different from those for small-signal amplifiers. A power amplifier operates in a *large signal* non-linear regime, so the analysis used for small-signal amplifier design cannot be used directly. First, the basic concepts of the MESFET (Metal-Semiconductor-Field-Effect-Transistor) will be given, including fabrication, device parameters, biasing condition, and layout issues. Then power amplifier design issues will be discussed, including operating modes, efficiency, and loadpull techniques. This will be followed by a discussion of the fabrication process used in this project: M/A-COM process $5A$. Finally, the design and simulation of a class A amplifier based on the above concepts will be presented.

3.1 GaAs MESFETs

Gallium Arsenide is a III-V compound semiconductor; it has the advantages of high carrier mobility and high resistivity which are of interest for RF applications. GaAs can be easily grown as a semi-insulating material; therefore substrate loss is typically much less than with standard silicon substrates. This also leads to lower interconnection parasitic capacitances and higher Q passives (particularly inductors). However, GaAs also suffers from some disadvantages such as higher cost, fragility, lower thermal conductivity, smaller available wafer sizes (6" vs. 12" standard), etc. GaAs MES-

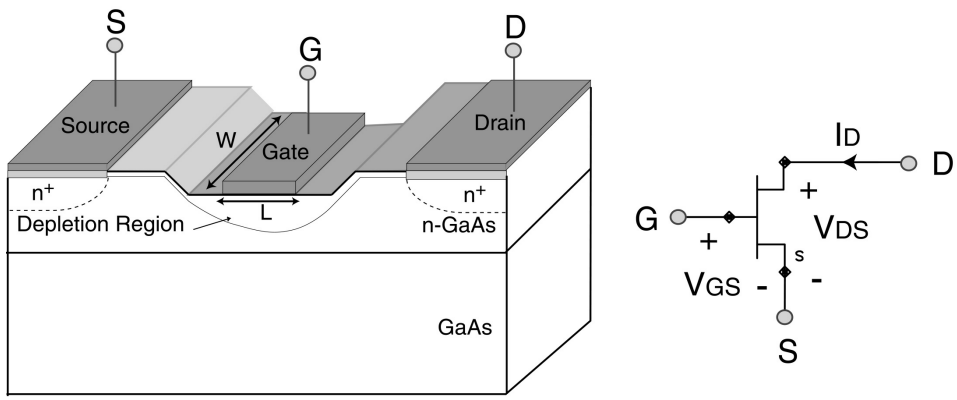


Figure 3.1: Basic MESFET structure.

FETs are now prevalent for high frequency applications, although there are significant recent developments in RF Si and SiGe technologies.

The GaAs MESFET is a voltage-controlled device. As shown in Fig. 3.1, the GaAs MESFET consists of a gate contact fabricated directly on the semiconductor adjacent to source and drain ohmic contacts. The gate metal and semiconductor have different work functions and form a Schottky junction at their interface. The Schottky junction results in a depletion layer under the gate; the depletion depth is controlled by the gate bias voltage. By increasing the reverse bias across the Schottky junction, the depletion layer can expand throughout the channel and restrict the current flow. This is the basic operating mechanism of the depletion mode MESFET. Typically, a Schottky junction has a forward voltage of $\sim 0.8V$, and a reverse breakdown voltage of $\sim$ 6-30V [31]. When applying bias to a depletion mode MESFET, the negative gate voltage should be applied first, followed by the drain to source voltage (V_{DS}). Otherwise, the transistor may draw a very large current I_D and potentially damage the device. Enhancement mode MESFETs, with a depletion region existing in the channel at zero bias, can be made as well.

The common-source bias scheme shown in Figure 3.2 has the advantages of low noise, high gain, high power, and high efficiency [32]. However, for depletion mode devices, a bipolar power supply is required to provide negative gate bias V_G ($\sim -2V$) and positive drain voltage V_D ($\sim 5 - 8V$). This increases the complexity of PA RFICs in mobile applications. There has been recent interest in enhancement mode devices since they can be biased from a single polarity supply.

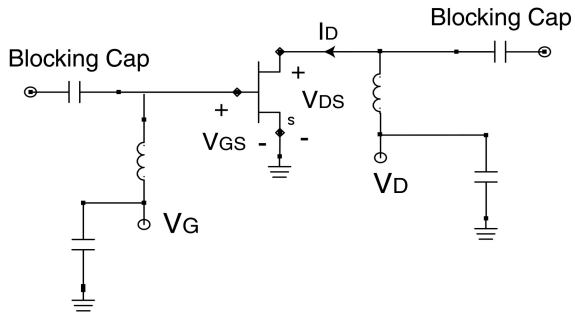


Figure 3.2: Common source MESFET bias configuration. The two inductors and shunt capacitors serve as RF chokes.

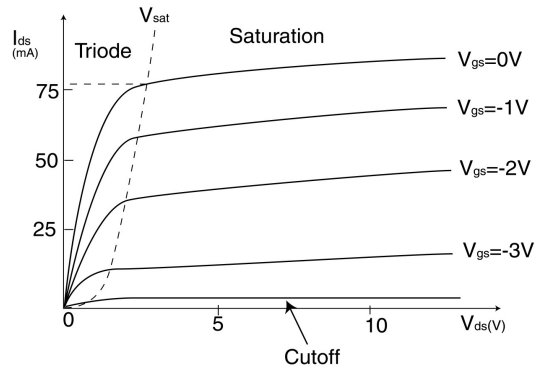


Figure 3.3: Typical depletion mode MESFET I-V curves.

A typical depletion-mode MESFET DC I-V characteristic is shown in Figure 3.3. The small-signal GaAs FET model is shown in Figure 3.4. The *intrinsic* FET model, shown inside the dotted box, accounts for the ideal operation of the transistor. Other parasitic resistors are shown outside the box. These unwanted parasitics can be reduced by careful design, but can never be totally eliminated. A frequently used benchmark parameter for transistors is the unity-current-gain frequency, f_T. f_T is the frequency at which $h_{21} = \frac{i_2}{i_1}|_{drain\ short-circuited} = 1$ (0dB), where i_2 is the output current, and i_1 is the small-signal current applied to the gate, and can be calculated from:

$$\text{unity current gain frequency } f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \approx \frac{g_m}{2\pi C_{gs}} \tag{3.1}$$

where g_m is the intrinsic small-signal transconductance. g_m will be greater than the transconductance measured externally due to the parasitic source resistance. The

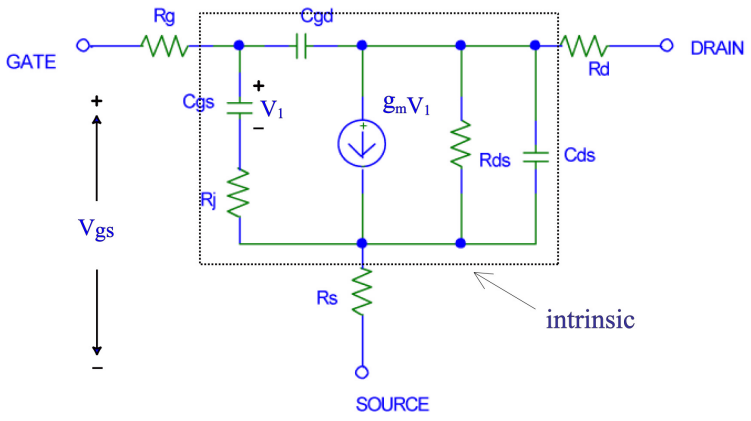


Figure 3.4: MESFET small signal model.

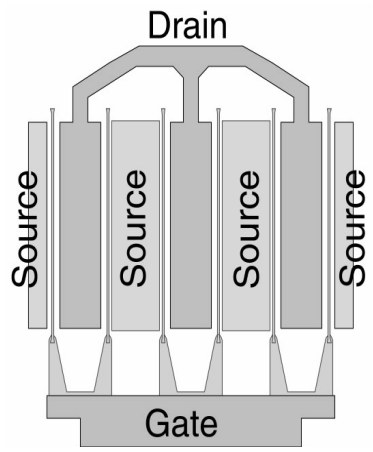


Figure 3.5: A multiple finger MESFET.

small-signal device model can be extracted using RF scattering parameter measurements, DC measurements (e.g. source resistance), and computer modeling.

To realize high power operation, a large gate periphery device is required to handle the required current. The large device size results in excess phase shift (transmission line effects) and parasitic resistance, so the use of a multiple finger, inter-digitated gate structure is very common (Figure 3.5). The source regions are connected to the chip ground directly through vias. The inter-digitated FET structure has the advantage of providing a large amount of total width within a compact area, therefore minimizing the transmission line effects. Some fabrication techniques can be used to

improve the performance of a power FET, including self-aligned gate or gate-recess techniques [31]. In addition, power MESFETs will generate excess heat, which will affect the performance and reliability of the devices. Since GaAs is not a very good thermal conductor, the GaAs substrate for power operation is normally thinned to $50\mu m$-$150\mu m$ thick [31].

3.2 Basic theory of power amplifier design

A small-signal amplifier is typically designed to be conjugate matched at both input and output. For a power amplifier, the maximum power transfer theorem still plays a role in the input matching network design, although the small-signal matching is replaced by large-signal impedance matching. At the output, the optimum load impedance is ideally determined by the desired output power, as shown below:

$$R_L = \frac{(V_{DD} - V_{Sat})^2}{2P_o} \tag{3.2}$$

where R_L is the load resistance required at the device output, V_{DD} is the DC supply voltage, V_{sat} is the device saturation voltage, and P_o is desired RF power output. This equation assumes that the device's own output impedance can be neglected.

The Class A amplifier is very similar to a small-signal amplifier, except that it operates in the saturation region with a large-signal swing between triode and cutoff (Fig. 3.6). The output signal is a substantial portion of the bias drain current. Since the current gain is not constant as the drain current changes, distortion occurs as the drain current swings cover a large range. When the power amplifier operates at its 1dB compression point (where the actual power gain is 1dB less than the small signal linear gain), the resulting harmonics generated will degrade the amplifier's performance. Additional tank circuits (harmonic traps) can be added to reduce the harmonic content.

For the low noise amplifier, the primary concern is the input signal level since it is typically very weak at the receiver front end. On the other hand, a power amplifier is not optimized for signal-to-noise ratio, but for output power and efficiency. The drain efficiency of a power amplifier is defined as:

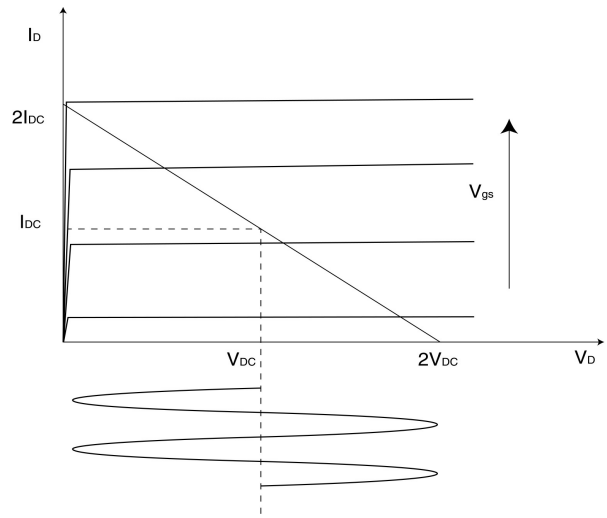


Figure 3.6: Ideal I-V curve of MESFET.

$$\eta = \frac{P_1}{P_{DC}} \tag{3.3}$$

where P_1 is the output power at the fundamental frequency, and P_{DC} is the DC supply power. Another term widely used in power amplifier design is the power added efficiency (PAE) defined as:

$$PAE = \frac{P_1 - P_{IN}}{P_{DC}} \tag{3.4}$$

where P_{IN} is the input RF power at the fundamental frequency. PAE is the ratio of the net increase in the power at the fundamental frequency to the DC supply power. When the gain is large, PAE$\sim \eta$.

The transistors in a Class A PA conduct current 100 percent of the time; in other words the PA has conduction angle of 2π (360°). For high power applications, the load line needs to stay within the saturation (active) region as much as possible. The limiting factors here are the maximum current and the saturation voltage. If ideal conditions for Class A PA operation are assumed, and the saturation voltage V_{sat} is assumed to be zero, the maximum output power and efficiency can be found as follows:

$$
\begin{aligned}
i_{_D} &= I_{_{DC}} + i_{RF} && (3.5)\\
v_{RF} &= i_{RF} \cdot R_{Load} && (3.6)\\
R_{Load} &= V_{_{DC}} \ / \ I_{_{DC}} && (3.7)\\
P_o &= 0.5 \cdot v_{RF} \cdot i_{RF} && (3.8)\\
i_{RF} &= I_{_{DC}} && (3.9)
\end{aligned}
$$

$$
\eta = \frac{P_o}{P_{_{DC}}} = \frac{0.5 \cdot v_{RF} \cdot i_{RF}}{V_{_{DC}} \cdot I_{_{DC}}} = \frac{0.5 \cdot i_{RF} \cdot R_{Load} \cdot i_{RF}}{V_{_{DC}} \cdot I_{_{DC}}} = \frac{0.5 \cdot i_{RF}^2 \cdot V_{_{DC}} \ / \ I_{_{DC}}}{V_{_{DC}} \cdot I_{_{DC}}} = 0.5 \tag{3.10}
$$

where $i_{_D}$ is the drain current, $I_{_{DC}}$ is the DC bias drain current, $i_{_{RF}}$ is the RF output current to the load, $V_{_{DC}}$ is the DC bias voltage, $V_{_{RF}}$ is the RF output voltage on the load, P_o is the RF output power on the load, $P_{_{DC}}$ is the total DC power drawn from the DC source by the power amplifier. Therefore, the theoretical optimum efficiency of an ideal class A PA is 50 percent. Also, as long as the signal swing lies in the saturation region, the class A PA has good linearity. In reality, V_{sat} is not zero, and the output mismatch will further lower the efficiency of the device.

3.2.1 Effect of saturation voltage

It is useful to examine the effect of the saturation voltage on the overall power amplifier efficiency. In the triode region, the MESFET acts like a voltage-controlled resistor (Fig. 3.3). To avoid this region, the optimum load resistance must be reexamined to accommodate the effect of the knee voltage. To remain in the active region, the output voltage should swing between V_{sat} and $2(V_{DC} - V_{sat})$ (Fig. 3.7).

If we assume the device is operating at its maximum current I_{DC}, then the optimum load resistance is:

$$
R_{opt} = \frac{V_{DC} - V_{sat}}{I_{DC}} \tag{3.11}
$$

At the fundamental frequency, the maximum output power P_1 is:

$$
P_1 = \frac{1}{2} I_{peak} \cdot V_{peak} = \frac{1}{2} I_{DC} \cdot (V_{DC} - V_{sat}) \tag{3.12}
$$

The efficiency is the ratio between output power and the dc input power:

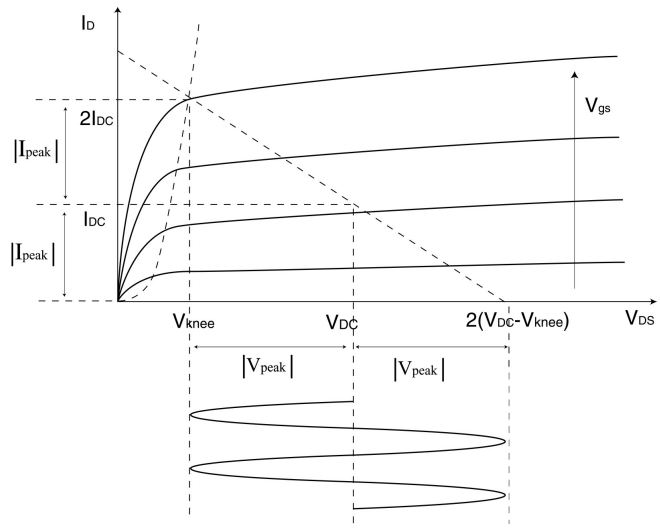


Figure 3.7: IV curve with knee voltage.

$$\eta = \frac{P_1}{P_{DC}} = \frac{\frac{1}{2} I_{DC} \cdot (V_{DC} - V_{sat})}{V_{DC} \cdot I_{DC}} = 0.5 \cdot \frac{(V_{DC} - V_{sat})}{V_{DC}} = 0.5 \cdot (1 - \frac{V_{sat}}{V_{DC}}) \tag{3.13}$$

Choosing $V_{sat} = m \cdot V_{DC}$:

$$\therefore \eta = 0.5 \cdot (1 - m) \quad m < 1 \tag{3.14}$$

Using the equation above, if a transistor is operating at a DC bias voltage of $\sim 5V$, and its V_{sat} is about $1.5V$, the factor m can be calculated to be $V_{sat}/V_{DC} = 0.3$. The maximum efficiency for a class A amplifier in this case is therefore:

$$\eta = 0.5 \cdot (1 - m) = 0.5 \cdot (1 - 0.3) = 35\% \tag{3.15}$$

3.2.2 The loadpull technique for PA design

The load-pull technique is used to find the optimum load impedance to be presented to the amplifier. The real and imaginary parts of the load impedance are systematically varied and contours of constant output power are then drawn on the Smith chart, allowing the optimum load impedance to be determined. The variation of the load

impedance will affect the PA's voltage and current swing, and will therefore affect its output power and efficiency.

Assuming the transistor is modeled as an ideal current source in class A operation, ideal theoretical loadpull contours of certain power levels can easily be drawn on the Smith chart [14]. First, the optimum load resistance $R_{opt} = V_{DC}/I_{DC}$ for P_{opt} is plotted on a Smith chart as a reference point. The contour with power P_{opt}/k ($k > 1$, the power is reduced by the factor k) will cross two real load points $R_{LO} = R_{opt}/k$ and $R_{HI} = R_{opt} \cdot k$. At the current limited point, with a load of $R_{LO} = R_{opt}/k$, the output current is at the maximum value I_{DC} and the voltage is V_{DC}/k. While keeping the maximum output current, a reactance X_m can be added to R_{LO} without affecting the output power:

$$P_{out} = \text{Real}\ (I \cdot V^*) = \text{Real}\ \{I_{DC} \cdot [I_{DC} \cdot (R_{LO} + j \cdot X_m)]^*\} = P_{opt}/k \qquad (3.16)$$

Therefore, an arc with constant output power can be plotted on the constant resistance circle through R_{LO}. At the voltage limited point, with a load of $R_{HI} = R_{opt} \cdot k$, the voltage is at the maximum value V_{DC} and the current is I_{DC}/k. An arc with constant output power P_{opt}/k can be plotted on the constant conductance circle through $1/R_{HI}$. As shown in Figure 3.8, the two arcs will intersect each other, forming the P_{opt}/k power contour on the Smith chart. As the power reduction factor k changes, a series of load pull contours with the respective constant power levels can be plotted on the Smith chart. The ideal case of the load-pull contour method is presented above. In reality, there will be other factors such as output capacitance, bondwires, package parasitics (for discrete PAs) etc. These factors tend to move the entire load-pull contour reactively on the Smith chart from the ideal contour location, so simulation software is used to achieve better design results.

3.3 Design of the power amplifier

The technology used in this project is the standard M/A-COM 5A GaAs self-aligned gate (SAG) MESFET process (see Section 2.2.1). Recall that in this project the chip is to be mounted on a printed circuit test board "top side" down to approximate a flip-chipped structure as shown in Figure 2.8. The backside metal is patterned

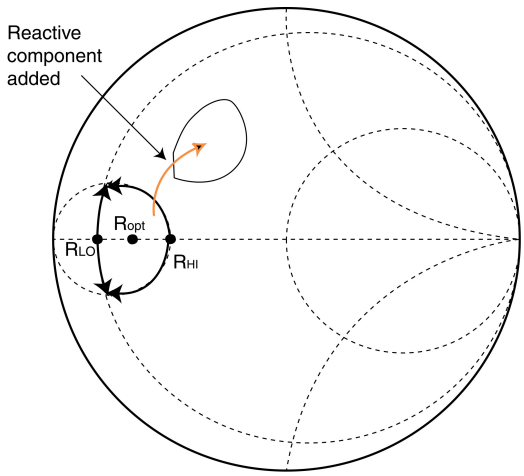


Figure 3.8: Theoretical loadpull contour for a transistor modeled as an ideal current source.

to define the patch antenna. In this case the PG2 layer will cover the entire chip and serve as the ground, and the buffer layer is omitted (BLV is opened over entire chip). A thin conductive silver epoxy is then applied between the chip ground (PG2 layer) and the board metal. This serves as both the connection to the system ground and the heat sink. PG1 and MT1 layers are used to form the passive components such inductors and capacitors; PG1 is also used to form the CPW transmission line interconnections.

The design of the "flip-chip" PA is quite different from the standard procedure, since the electronics will be facing down and there is only $\sim 7\mu m$ of polyimide between the electronics and the ground plane. In the standard process, the backside metal serves as the chip ground and the chip faces up such that the ground plane is more than $125\mu m$ away. In the standard M/A-COM process, the $5A$ MESFET model corresponds to a $125\mu m$ GaAs substrate, with the source of transistor grounded through backside vias. Therefore, device models and parameters had to be used with caution and remodeled where necessary. The M/A-COM 5A process MESFET models were still used in the design; however, passive components were modeled using IE3D.

For simplicity, the power amplifier is designed to operate in class A mode. A simple single-stage common-source design was chosen for proof-of-concept integration with the antenna. Agilent EESof Series IV Libra [19] was used to simulate the power amplifier's performance. The DC bias was chosen to be $V_G = -2V$ and $V_D = 5V$; the bias current is $\sim 69.4\ mA$ (Fig. 3.9). From the $I - V$ curve, we can estimate that g_m

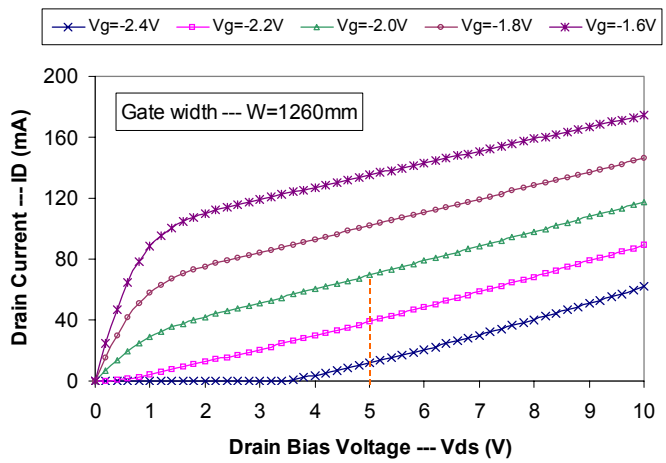


Figure 3.9: Simulated common-source MESFET I-V curve (W=1260 μm).

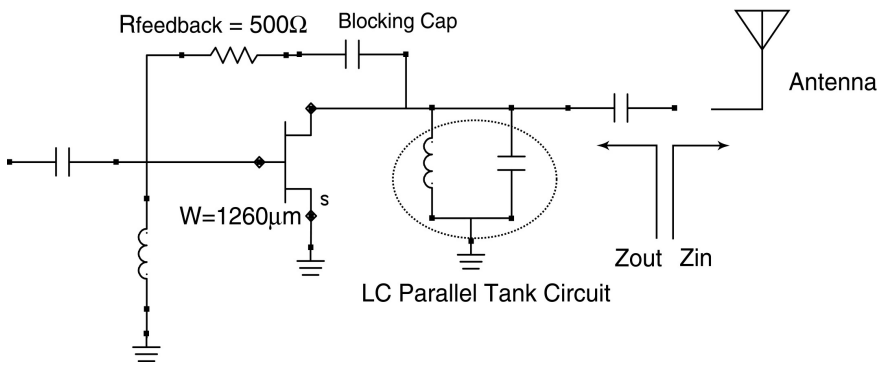


Figure 3.10: Simplified power amplifier RF schematic (biasing not shown).

$\sim 150ms$ $(\Delta I_D/\Delta V_G)$, $R_{ds} \sim 100\Omega$ $(\frac{1}{\Delta I_D/\Delta V_D})$.

A parallel feedback resistor is used to stabilize the transistor at the cost of reduced gain. Parallel feedback MMIC amplifiers have the advantage of very flat gain, good input and output matches, and stability (Fig. 3.10). A DC blocking capacitor is used in the feedback path to isolate positive drain bias from the negative gate bias. Since the input impedance of the MESFET is almost purely reactive, the feedback moves the real part of the input impedance to roughly 50Ω (Miller effect) and simplifies the input matching. A shunt inductor (to resonate out the gate source capacitance) is used for input matching to a 50Ω source, and serves as the DC gate bias path as well.

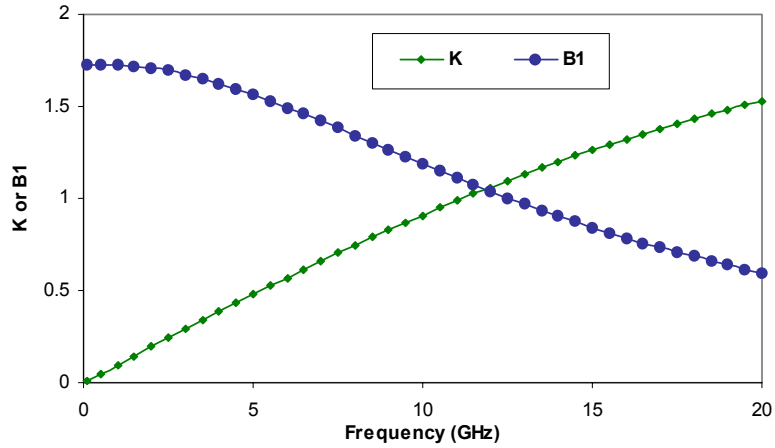


Figure 3.11: Simulated stability curve vs. frequency of a stand alone MESFET (V_{gs} = -2V, V_{ds} = 5V).

3.3.1 Device Stability

The simulated stability of a stand-alone MESFET transistor (V_G = -2V, V_D = 5 V) is plotted in Figure 3.11. It is found that the Rollett stability factor K [15] falls below one at frequencies less than 11 GHz – the circuit will be potentially unstable if no measures are taken. On the other hand, the stability measure $B1$ [15] is greater than zero over the plotted frequency range as desired.

Curves of K and $B1$ vs. frequency over a range of feedback resistances are shown in Figure 3.12 - 3.13. As the feedback resistance increases from 100Ω to 1100Ω, the range of K values falls gradually. It should be noted that the K factor is lower at lower frequencies compared to higher frequencies. One of the reasons for this is that the device gain drops dramatically at higher frequencies, leading to more stability.

3.3.2 Input Matching

A simplified intrinsic MESFET model with feedback resistor is shown in Figure 3.14. The input admittance can be calculated using this model with typical device parameters. ($R_j = 3\Omega$, $C_{gs} = 1.0pF$, $C_{gd} = 0.09pF$, $C_{ds} = 0.4pF$, $f = 5.6GHz$, $g_m = 150mS$, $R_{ds} = 100\Omega$). The calculated input admittance vs. feedback resistance

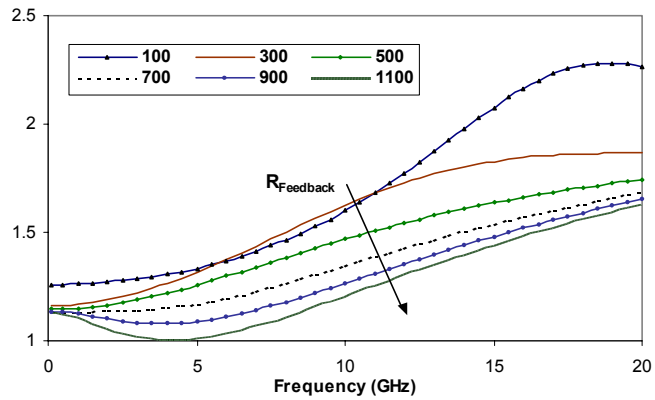


Figure 3.12: Simulated stability curve K vs. frequency with different feedback resistor values (V_{gs} = -2V, V_{ds} = 5 V). Note that $K \geq 1$ for entire freqency range for a range of feedback resistors (100 - 1100 Ω)

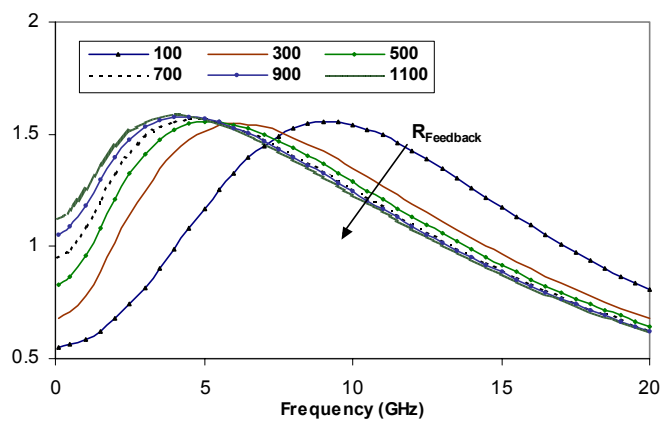


Figure 3.13: Simulated stability curve $B1$ vs. frequency with different feedback resistor values (V_{gs} = -2V, V_{ds} = 5V).

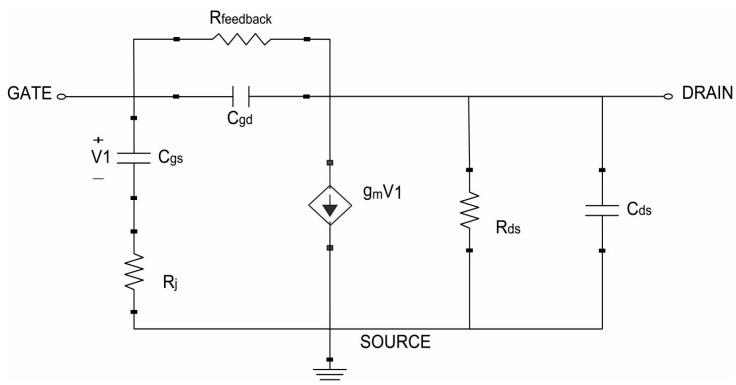


Figure 3.14: Small-signal model of MESFET with parallel feedback.

curve using Matlab [33] is plotted in Fig. 3.15 using these typical MESFET model parameters. In this case, it is assumed that the output load resistance is 50Ω.

The admittances are normalized to 50Ω. From the real admittance curve, it is found that when the feedback resistor is at $\sim$ 500Ω, the normalized real part of the admittance is very close to one, so only a shunt inductor is needed to match the input to 50Ω. This feature could significantly simplify the input matching network since only a parallel inductor is needed to achieve very good return loss. In reality, the actual device parameters will be different from the above typical values, so iteration in the simulation is needed to find the optimum feedback resistor value to achieve both good stability and input matching over the frequency range of interest.

A single MESFET (biased at V_G = -2V, V_D = 5 V, width = 1260 μm) with a parallel feedback resistor is simulated using a linear small-signal S-parameters simulation in Libra. In Figure 3.16, the small-signal S_{11} vs. feedback resistor value for the individual MESFET is plotted. As the value of the feedback resistor increases, S_{11} crosses the unity conductance circle (1+jb). At $R_{feedback}$= 500, the real part of the input admittance is very close to unity.

Since the PA operates in the large-signal regime, the large-signal S-parameters must also be considered. The large-signal S_{11} vs. input power curve with $R_{feedback}$= 500 is plotted in Figure 3.17. Notice that the S_{11} does not vary significantly as the input power is increased from $0dBm$ to $20dBm$. Therefore, only small modification is needed in the design to optimize the matching at large signal.

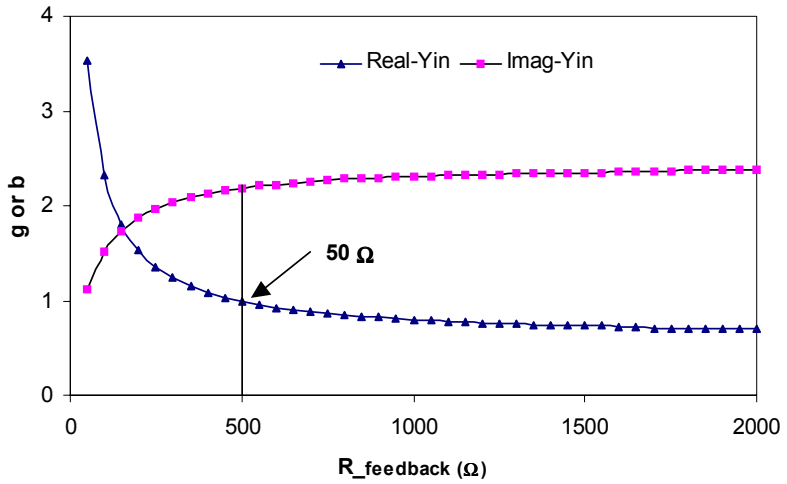


Figure 3.15: Simulated (normalized to 50 Ω) input admittance vs. feedback resistor values.

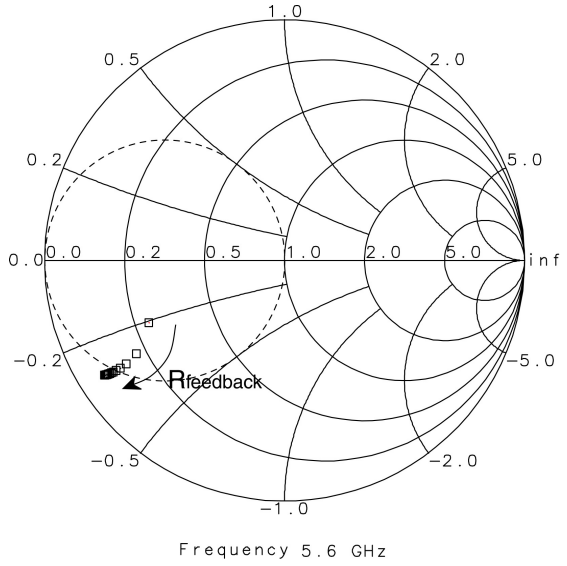


Figure 3.16: Simulated small-signal S_{11} vs. feedback resistor value at $5.6GHz$.

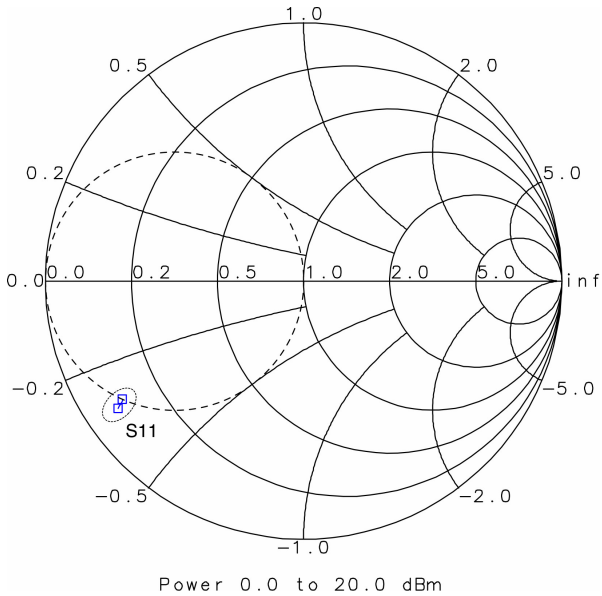


Figure 3.17: Simulated large signal S_{11} with feedback resistor (500Ω) at $5.6GHz$.

With a feedback resistor of 500 Ω, the normalized input admittance with a input power of 10dBm is $1.0029 + 3.063j$, very close to the unity conductance circle. Therefore, only a shunt inductor placed at the gate is needed to match the PA to a 50Ω source. The gate inductor also serves as a DC bias (V_G) path. The RF signal passes through bondwires, bonding pads, backside vias, and the CPW feedline before reaching the input of the transistor (Figure 3.18). The normalized admittance looking into the source with these components is $0.86 + 0.25j$ at the input of the transistor. Since the real part of the admittance is very close to one, to preserve the simplicity of the circuit only a shunt inductor (Figure 3.19) is used to tune the input network and improve the input return loss. For an estimate of the inductor value the suceptance is calculated to be:

$$B = (-3.063 - 0.25)/50 = -0.066\,26\ . \tag{3.17}$$

This yields an inductor value of 0.42 nH @ 5.6 GHz:

$$L = \frac{1}{jB \times j\omega} = \frac{1}{0.06626 \times 2 \times \pi \times 5.6 \times 10^9} = 4.\,289\,2 \times 10^{-10} = 0.42nH \tag{3.18}$$

An ideal inductor with value of 0.42 nH will provide relative good match at the input

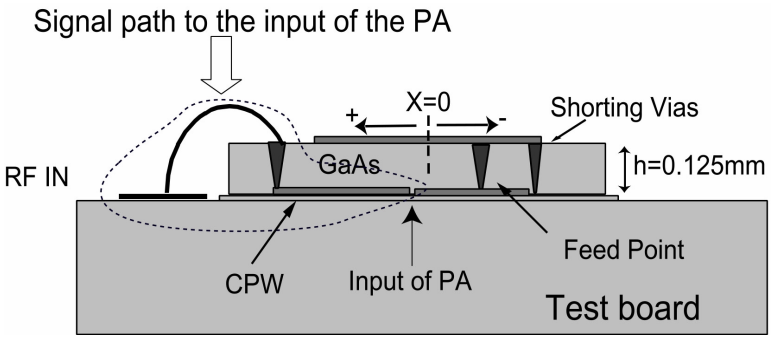


Figure 3.18: Input signal path to PA.

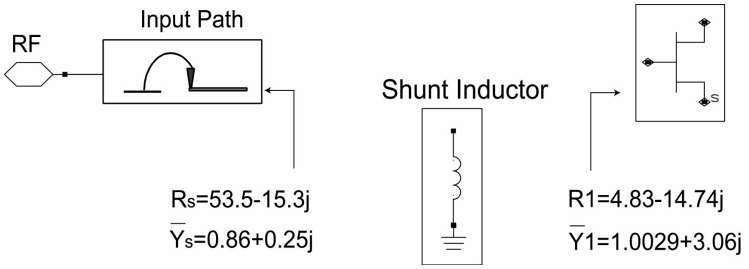


Figure 3.19: Schematic of input match to PA.

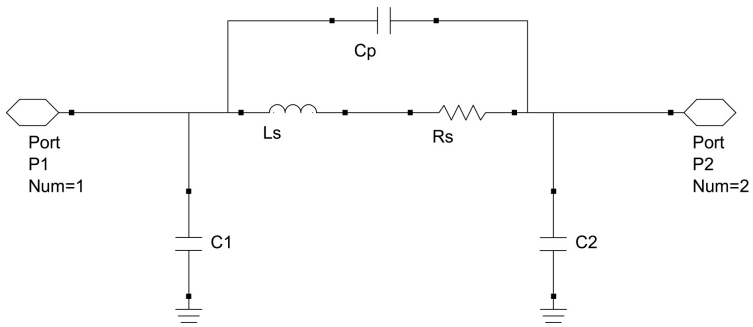


Figure 3.20: Integrated inductor equivalent circuit model.

of the power amplifier.

Integrated Inductor

The inductors used in PA circuits were remodeled due to the presence of the nearby ground plane since the image current effect and parasitic capacitance to the ground may be significant. Monolithic square shaped spiral inductors are commonly used in the RFIC/MMIC applications. An equivalent circuit model [34] is shown in Figure 3.20. Square inductors were chosen over circular or octagonal inductors for simplicity of layout and simulation. In the inductor model, the inductor L_S represents the actual inductance of the spiral; at first order it is affected by the number of turns and overall size of the inductor, as shown in equation 3.19.

$$L_s = \mu_0 n^2 r \tag{3.19}$$

where, μ_0 is permeability of free space, n is the number of turns, r is the radius of the spiral inductor. The resistor R_s in series with the inductor L_s accounts for the loss of the metal trace and other interconnections. R_s is function of the frequency — it tends to increase at higher frequencies due to the skin effect — and is given by the equation:

$$R_S \approx \frac{l}{w \cdot \sigma \cdot \delta(1 - e^{-t/\delta})} \tag{3.20}$$

$$\text{where, } \delta \text{ is the skin depth} = \sqrt{\frac{2}{\omega \mu_0 \sigma}} \tag{3.21}$$

and where, l is the total trace length, t is the metal thickness, w is the width of the trace, σ is the conductivity of the metal, and ω is the radian frequency. A parallel capacitor C_P models the inter-trace parasitics (Eq. 3.22). Two parallel capacitors C_1 and C_2 (Eq. 3.23), model the parasitics between the metal trace of the inductor and the ground plane.

$$C_P = n \cdot w^2 \cdot \frac{\varepsilon_{poly}}{t_{poly}} \tag{3.22}$$

$$C_1 \ or \ C_2 = w \cdot l \cdot \frac{\varepsilon_{poly}}{t_{poly}} \tag{3.23}$$

where, ε_{poly} and t_{poly} are the permittivity and thickness of the polyimide, respectively.

Effect of transmission lines connecting to the inductor

The inductors for the input matching need to be connected through transmission lines on both sides. The actual matching network inductors on the chip consist of a transmission line in series with the on-chip square spiral inductor. The input impedance of a load connected though transmission line is given by [24]:

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan \beta l}{Z_o + jZ_L \tan \beta l} \tag{3.24}$$

where β is the propagation constant, Z_0 and l are the characteristic impedance and length of the transmission line, and Z_L is the load impedance. If the transmission line is shorted on one side ($Z_L = 0$):

$$Z_{in} = Z_0 \frac{0 + jZ_0 \tan \beta l}{Z_o + j \cdot 0 \cdot \tan \beta l} = jZ_o \tan \beta l = j\omega L_{eq} \tag{3.25}$$

$$L_{eq} \approx \frac{Z_0 l}{v} \tag{3.26}$$

where v is the phase velocity. As can be seen, the shorted transmission acts like an inductor. Since the transmission line connections of the gate inductor increase the actual inductance, a smaller gate spiral inductor is needed for the input matching.

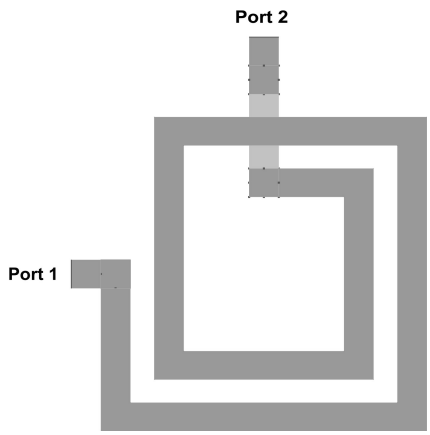


Figure 3.21: Gate inductor layout.

Gate Inductor

Figure 3.21 shows the shunt tuning inductor designed for the gate of the MESFET (width = 1260 μm) transistor. The gate inductor was simulated using IE3D; the trial design has a trace width $w = 10\ \mu m$, gap $g = 8\ \mu m$, radius $r = 55\ \mu$, and number of turns $n = 1\frac{3}{4}$. The input and output ports of the inductor are oriented 90° from each other for ease of layout. An estimate of the corresponding equivalent circuit model values can be calculated using equations 3.19 to 3.23. The simulated series inductance L_s is 0.26 nH; this value is smaller than the required 0.42 nH since the transmission line connections are also inductive.

Simulation results of input match

A one-port linear simulation was performed for the shunt inductor with all transmission line connections (to power supply and ground) and bypass capacitors included; it is found that the normalized admittance is $0.33 - j3.87$. The suceptance is very close to the calculated value of $-j3.3$.

The large signal return loss (S_{11}) and gain (S_{21}) of the input-matched MESFET with feedback are plotted in Figure 3.22. If the load impedance changes, the input match will be affected, but to a lesser extent than the effect of source impedance on the output match. The effect of mismatch at the input resulting from the change in the

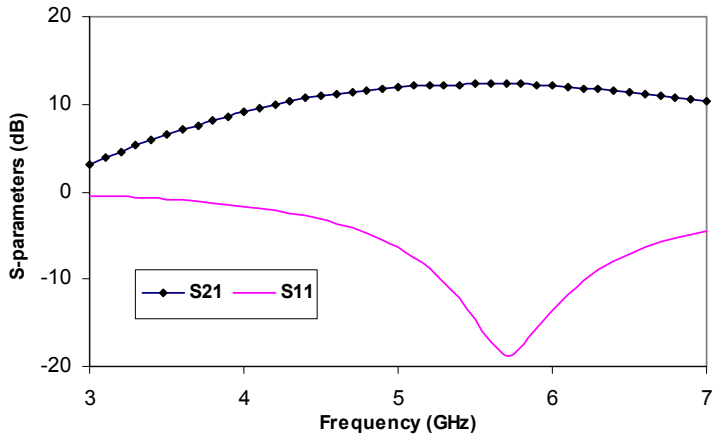


Figure 3.22: Simulated large signal S_{11} and S_{21} vs. frequency of input matched MESFET.

load can be tuned out after the optimum load impedance has been found.

3.3.3 Output matching

The results of an output load pull simulation are shown in Figure 3.23. The loadpull contours are plotted on the Smith chart by varying the load reflection coefficient and plotting P_{out}. The input RF signal power is $10dBm$. Three contours are shown, corresponding to output powers of $23dBm$, $22dBm$, $21dBm$, respectively. The optimum load power is $23.19dBm$ at a load reflection coefficient of $\Gamma_L = 0.432\angle 133.33^o$. As can be seen from the loadpull results, the $23dBm$ output power circle crosses the unit conductance circle.

In the initial integrated active antenna design, the antenna input was designed to be 50 Ω, and the output of the PA was fed to the antenna feed point through a backside via directly using a CPW transmission line; no bondwires or pads are present in the output signal path. A shunt inductor was designed to move the impedance looking towards the antenna to the desired load impedance at the drain of the transistor. The output matching network was first designed using ideal components, then modified for transmission line and physical component implementations. Optimization was used to further adjust the values to achieve the desired performance. The final design had a simulated normalized admittance of $1.22 - 0.83j$ looking towards the load from

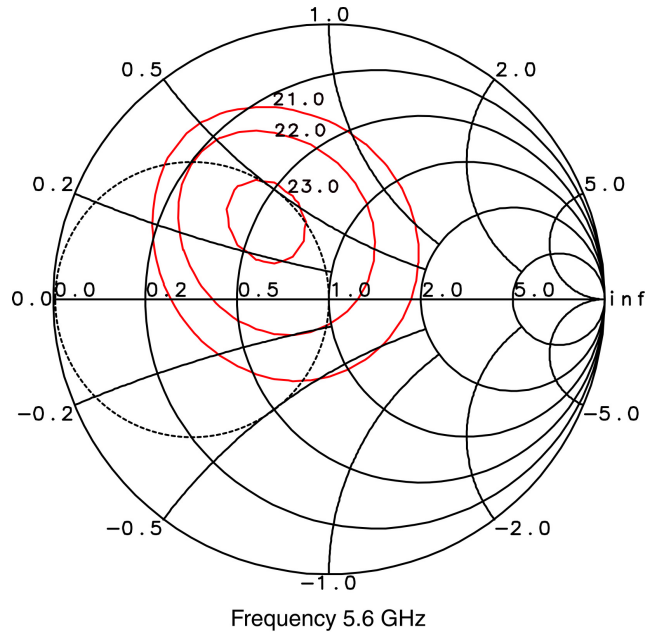


Figure 3.23: Simulated output power loadpull contours (P_{out} = 21, 22, 23 dBm) of the input matched MESFET (W = 1260 μm).

the drain of the FET (Fig. 3.24).

Drain Inductor design for 50 Ω antenna (Drain Inductor 1)

The drain inductor design has a trace width $w = 12\ \mu m$, gap $g = 8\ \mu m$, radius $r = 100\ \mu m$, number of turns $n = 2\frac{1}{4}$ (Fig. 3.25). The metal trace is laid out using plated gold (PG1) and the cross-under is laid out using metal (MT1). The MT1 layer is much thinner than the plated gold and made from a different material. Therefore, the DC current handling capability of the MT1 layer is much less than the PG1 layer. To provide handling for $\sim 100\ mA$ of DC current, the cross-under in the inductor was made proportionally wider than the traces in the plating gold layer. It should be noted that this wide cross over will affect the parasitic capacitance of the inductor. However, placing the inductor port with the wide cross-under to the ground side, the parasitic capacitance arising from the wider trace becomes part of the bypass capacitor and has positive effect on the PA circuit operation. Note that this is not an issue for the gate inductor based on the very low current drawn by the gate. The inductor has a simulated series inductance L_s of 0.57 nH. Simulations and

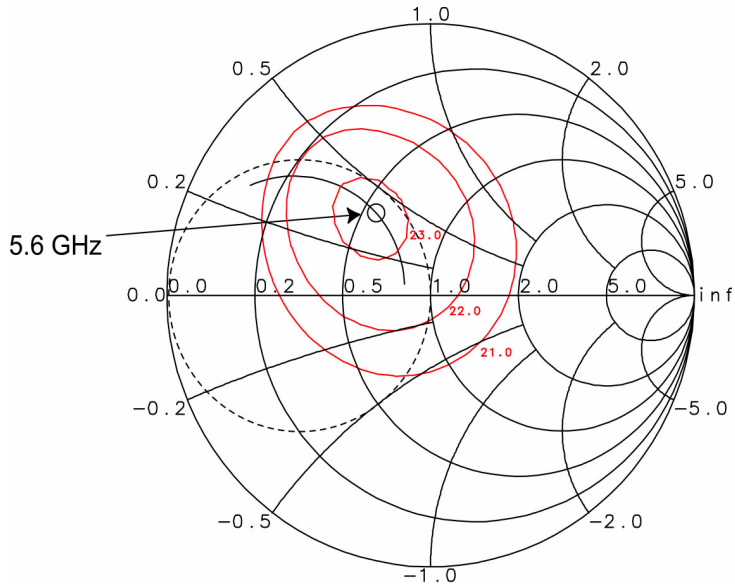


Figure 3.24: S_{11} of the Output matching network (50 Ω case).

measurements will be compared in Chapter 4.

3.4 PA performance simulations

A simplified schematic of the power amplifier design is shown in Figure 3.10. As discussed earlier, the parallel feedback 500Ω resistor is used to achieve both stability and input matching. A DC de-coupling capacitor is connected in series with the feedback resistor to isolate the gate and drain bias from each other. At the input, a simple shunt inductor is used for the input matching. At the output, a parallel LC network is utilized to transfer a 50Ω load (Z_{in} of the antenna) to the optimum load impedance.

The simulated stability curve of the final PA design is shown in Figure 3.26. As can be seen the K factor is greater than 1.7 from 100 MHz to 20 GHz. The $B1$ factor is greater than zero over the same band. The simulated circuit is unconditionally stable.

Large-signal S-parameter simulations show that the power amplifier has a linear gain of 12.7 dB and a $\sim$ 10 dBm 1-dB compression point at 5.6 GHz (Fig. 3.27). From

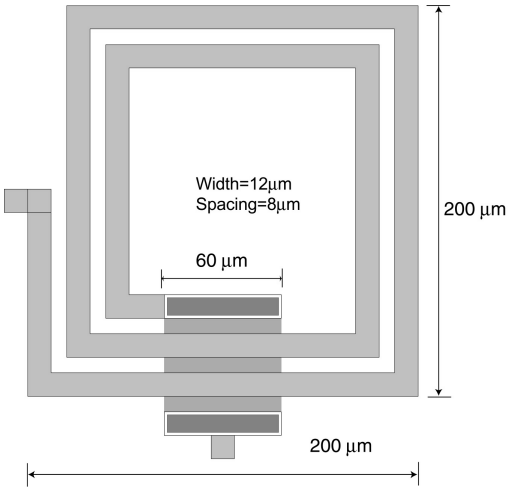


Figure 3.25: Drain inductor -1 layout.

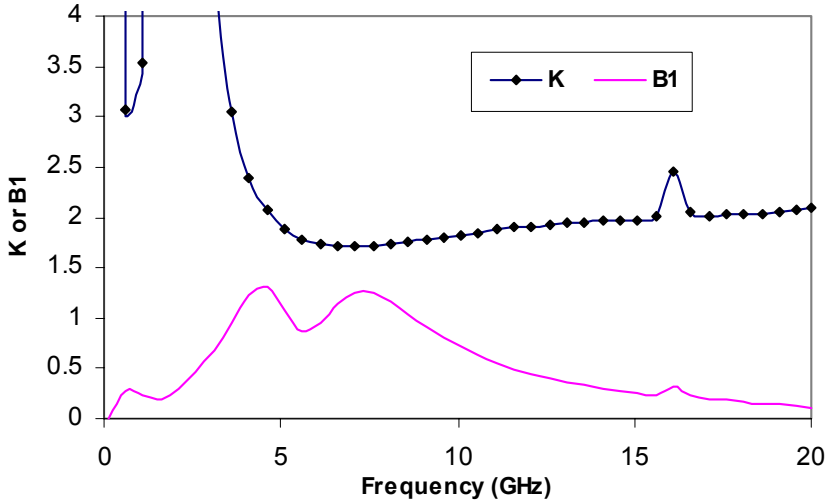


Figure 3.26: Simulated stability factor of the PA.

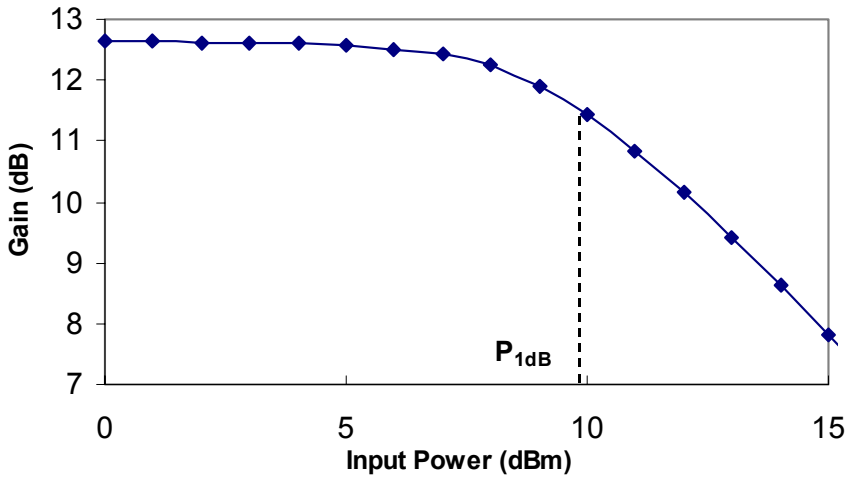


Figure 3.27: Simulated large signal S_{11} of the PA.

Harmonic Balance simulations, it is found that the power amplifier has a return loss of 14.7 dB, a fundamental output power of 21.4 dBm (P_{in}=10 dBm), and a power added efficiency of 31% (Figure 3.28). Based on the calculation of the knee voltage effect, the saturation voltage lowers the efficiency by about 15%.

3.4.1 PA matched to a 22.5 Ω antenna.

Since the antenna input impedance can be adjusted by moving the feeding position of the patch, the amplifier does not necessarily have to be designed to match to a 50 Ω antenna. Instead, an alternative convenient input impedance may be chosen to simplify the output-matching network design of the amplifier. This provides an extra degree of the freedom for the antenna and amplifier co-design. Another version of power amplifier was designed to match an antenna with an input impedance of 22.5 Ω. Matching to the 22.5 Ω antenna results in reduced sizes of the inductor and capacitors in the output-matching network. The final design has a normalized admittance of $1.65 - j0.69$ looking towards the load from the drain of the transistor, which lies inside the $23dB$ output power circle (Fig. 3.29).

The alternate power amplifier design has a simulated return loss of 18 dB, a gain of

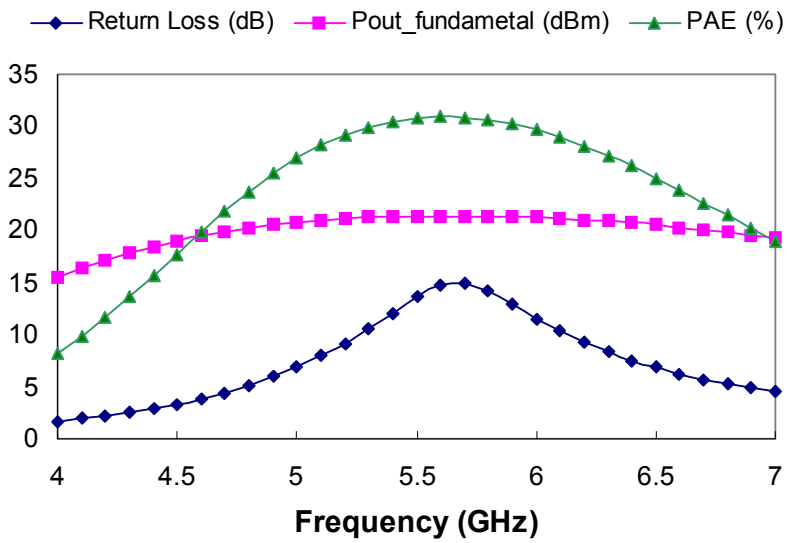


Figure 3.28: Simulated P_{OUT}, PAE and RL vs. frequency.

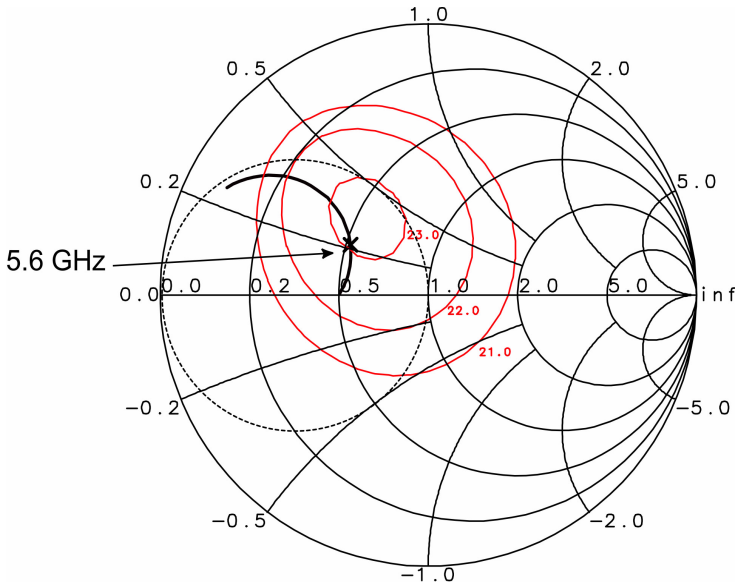


Figure 3.29: S_{11} of the Output matching network ($R_{load} = 22.5\Omega$).

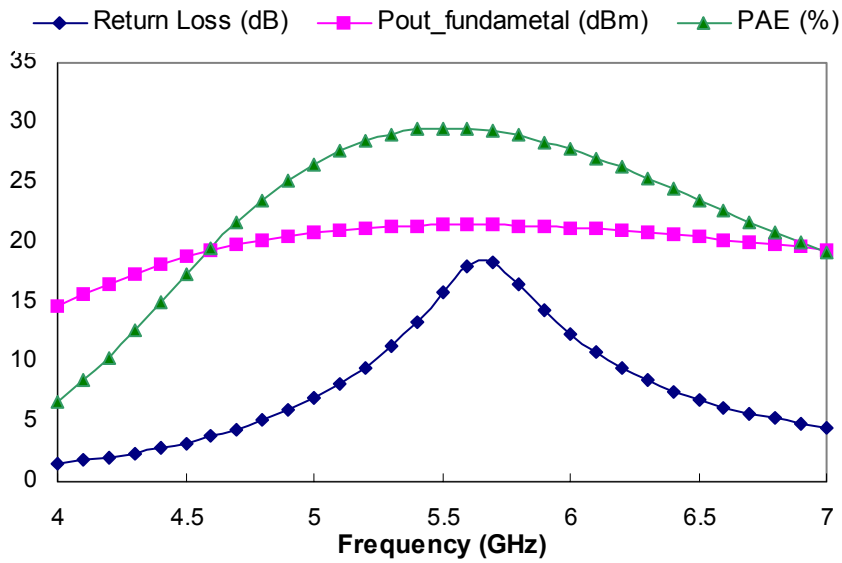


Figure 3.30: Simulated P_{OUT}, PAE and RL vs. frequency (Load impedance = 22.5 Ω).

11.5 dB ($P_{in} = 10dBm$), and a power added efficiency of 29.5% with a 22.5 Ω load. (Figure 3.30).

Drain Inductor design for 22.5 Ω antenna (Drain Inductor 2)

Another version of the drain inductor was designed for the PA design matched to the 22.5 Ω antenna input impedance. After optimization, the desired inductor dimensions are found to be trace width $w = 12\ \mu m$, gap $g = 8\mu m$, radius $r = 80\ \mu m$, and number of turns $n = 2\frac{1}{4}$. The inductor has a simulated series inductance L_s of 0.43 nH. Simulations and measurements will be compared in Chapter 4.

3.5 Summary of the Chapter

The design issues for the integrated power amplifier have been discussed in this chapter. Parallel feedback between drain and gate of the MESFET was used to improve the stability and input matching. A simple shunt inductor matching network was used at the input of the PA. Loadpull simulations were used to design the output

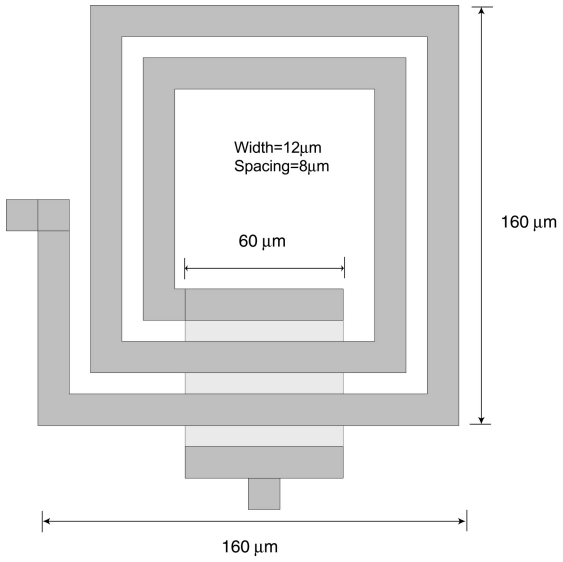


Figure 3.31: Drain inductor - 2 layout

matching network. Two versions of the power amplifier were designed to match two different antenna input impedances (50 Ω and 22.5 Ω). Passive components were simulated and optimized using IE3D. The PAs have a simulated RL better than ∼15 dB, input 1dB compression point of ∼10 dBm, and PAE of ∼30%.

Chapter 4

Fabrication and On-wafer Measurement

4.1 Layout and Fabrication

The GaAs chips containing passive and active integrated antennas, as well as test structures were fabricated at M/A-COM, Roanoke, VA, using their $5A$ process with the backside patterning. There are a total of four different die layouts on the reticle with dimensions of 7mm $\times$ 7mm each (Fig. 4.1):

- Layout (a) includes the 50 Ω active antenna with two individual MESFETs with gate widths of 630 μm and 1260 μm respectively [Fig. 4.1 (a)].
- Layout (b) includes calibration testing structures: TRL standards, inductors, stand-alone power amplifier, and resistors [Fig. 4.1 (b)].
- Layout (c) includes the 50 Ω passive antenna and some testing capacitors [Fig. 4.1 (c)].
- Layout (d) includes the 22.5 Ω active antenna, testing capacitors and resistors [Fig. 4.1 (d)].

The fabricated dies were diced into separate GaAs chips for bondwire connections or on-wafer measurements. Note that for the purpose of accurate comparison, the

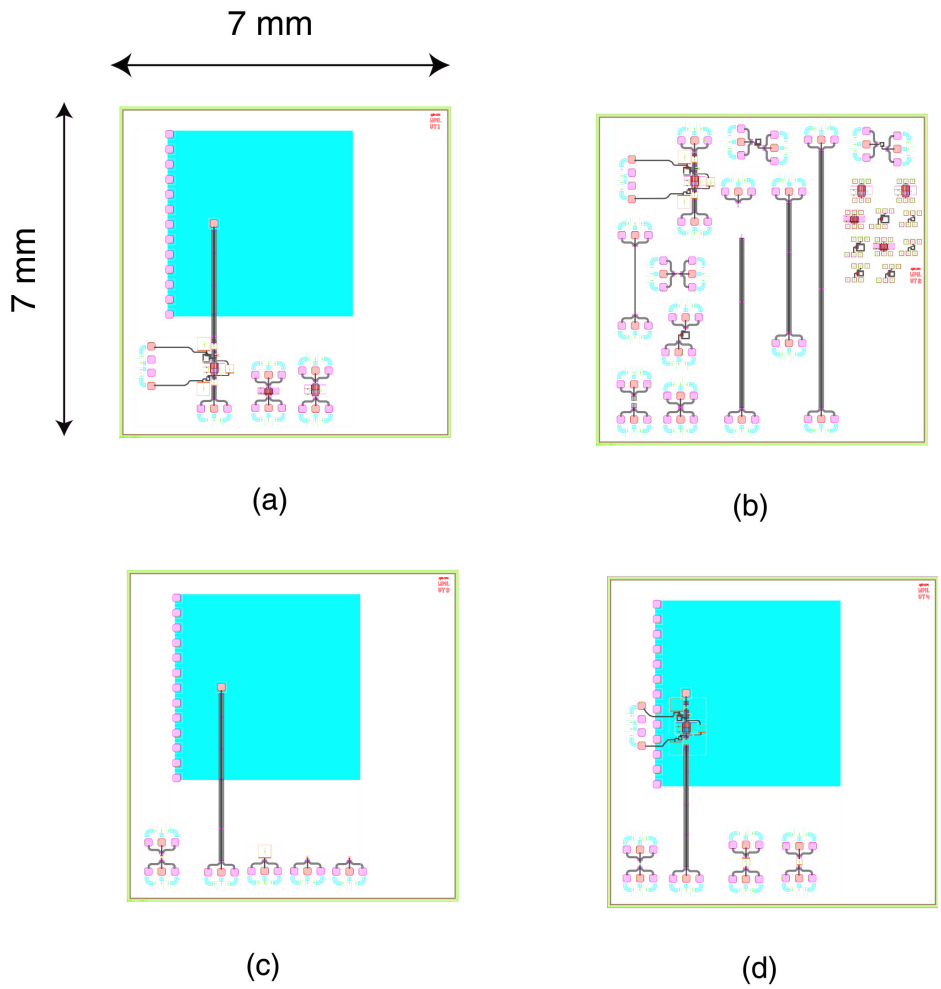


Figure 4.1: Four different die layouts from the reticle: (a) 50 Ω active antenna; (b) Testing structures; (c) Passive 50 Ω antenna; (d) 22.5 Ω active antenna;

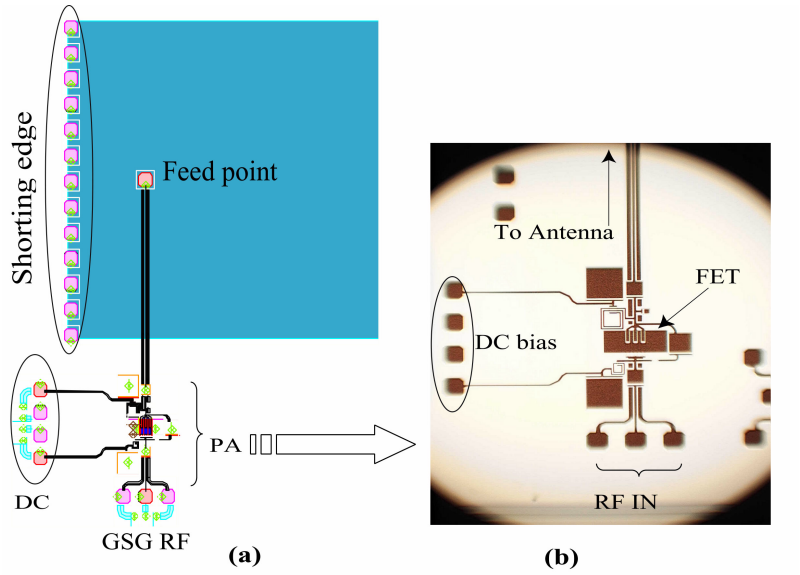


Figure 4.2: (a) Layout of the 50 Ω PA/Antenna. (b) Micrograph of the power amplifier prior to PG2 deposition.

three antenna designs are laid out at same position on their respective chips, and the CPW feeds to the antennas are also kept at the same positions relative to their own chips. Orthogonal feeding was adopted to avoid the interference between the antenna radiating edge and the electronics.

The power amplifier in the 50 Ω active antenna is positioned immediately at the input of the CPW feedline while the power amplifier in the 22.5 Ω active antenna is positioned at the feed point of the patch antenna. It should be noted that a 50 Ω CPW line in front of the 50 Ω antenna will not shift the input impedance, while a 50 Ω CPW line in front of the 22.5 Ω antenna could rotate the input impedance to a different undesired value. The positioning of the PAs relative to the antennas was also done to provide a means to compare coupling effects between the radiating antenna and the PA. It was originally surmised that the 50 Ω version would see less coupling effects. The layout of the integrated PA/antenna design (50 Ω antenna input) is shown in Fig. 4.2(a). A micrograph of the fabricated power amplifier (before PG2 deposition) is shown in Fig. 4.2(b).

CPW transmission lines were adopted for the signal feed line for the advantages of low radiation and ease of fabrication. The layout of the RF input signal path on the

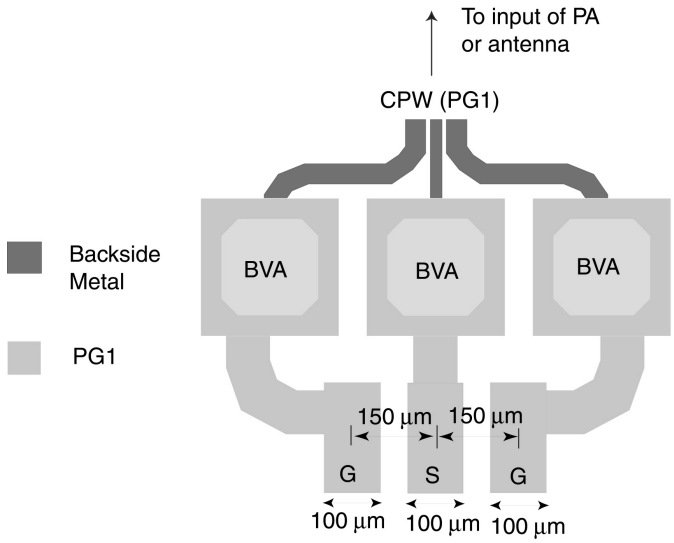


Figure 4.3: Input path: GSG pads, backside vias and CPW line.

chips is shown in detail in Fig. 4.3. The input signal is fed to the backside GSG (Ground-Signal-Ground) bonding pads either using on-wafer probes or bondwires, and then goes through backside vias (BVA) to the coplanar waveguide transmission line (CPW) on the PG1 layer (see Fig. 2.8). The GSG pads are fabricated in the backside metal layer with dimensions of $100\mu m \times 100\mu m$, and a pitch of $150\mu m$ to accommodate available RF GSG probes. The backside vias connect the signal path from the backside of the chip to front side metal layer (PG1). The size of the vias is dictated by processing constraints. The transmission line is built in the PG1 layer since it is relatively thick (4.5μm plated Au) and therefore has less loss. Transmission line 90° bends were laid out as curved structures to reduce discontinuity effects. The baseline CPW line is designed to have a characteristic impedance (Z_0) of 50 Ω and effective dielectric constant (ε_{eff}) of 5.3. The DC signal pad (shown in Fig. 4.4) carries the DC bias for both the gate and the drain of the MESFET. The ground pads for the DC supplies are laid out in the center, while the DC bias pads are on the outside to avoid potential interference or feedback between the gate and the drain.

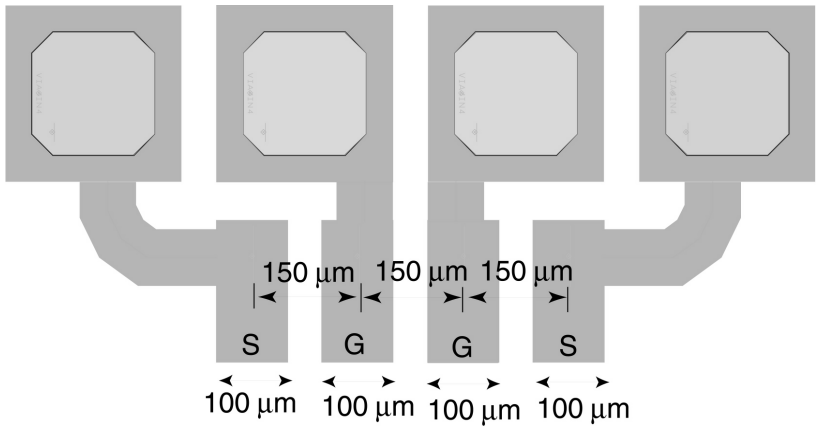


Figure 4.4: DC supply pads.

4.2 On-wafer Measurements

After fabrication, accurate measurements of the RF electronics were performed using an on-wafer probe station. On-wafer probing has the advantages of accuracy, repeatability, and simplicity of calibration, and enables VNA measurement reference planes to be located by the designer on chip. On-wafer calibration structures such as through, short (reflect), and delay lines are used to calibrate the VNA to a desired *reference plane* at the input of the device under test (calibrating out the error contributions from bonding pad, vias, etc) using TRL calibration techniques [25].

As discussed in Section 2.2.1, the simulation of the electronic system performance involved remodeling of some of the passive components (e.g. inductors, backside vias, etc.). Similarly, careful measurements not only need to be taken at the circuit level, but also for every individual component. All the components used in the various power amplifier designs were laid out the on the chips with their own testing pads, so the characterization of all the details of the system could be analyzed

4.2.1 Coplanar Transmission Lines

A Cascade probe station and an *HP* 8510*C* vector network analyzer was used in the on-wafer measurements (Fig. 4.5). The on-wafer Thru-Reflection-Line (TRL) calibration is performed using MultiCal developed by the NIST/Industrial Measurement

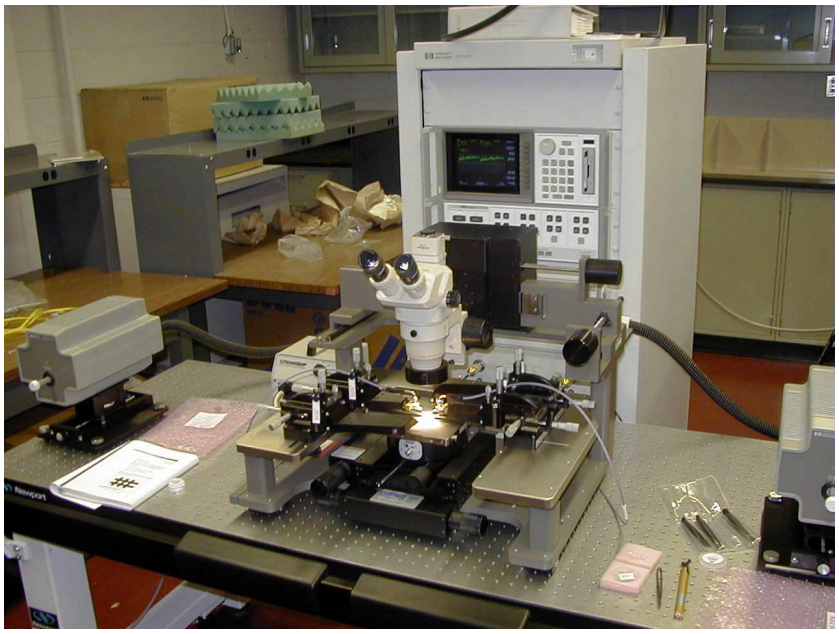


Figure 4.5: Cascade probe station and HP 8510C network analyzer.

Consortium [35]. Four CPW standards were laid out on-chip for calibration (Fig. 4.6); through line, short (reflect), delay line one (length = 2.984 mm) and delay line two (length = 5.787 mm). The two delay lines are designed to be 1/8 and 1/4 of the guided wavelength respectively. After TRL calibration, the reference plane is moved to be the center of the through line and subsequent measurement results will not include the bonding pad, backside via and transition effects.

The simulated and the measured results of the effective dielectric constant of 50 Ω CPW vs. frequency are shown in Figure 4.7. The effective dielectric constant has a measured value of 4.7 vs. the simulated value of 5.3 at 5.6 GHz. The attenuation has a measured value of 1.6 dB/cm vs. simulated value of 2.4 dB/cm (Fig. 4.8).

The simulation and measurement results show reasonably good agreement. The difference may be due to a simulation issue using IE3D. When the chips are actually fabricated, the intermetal dielectric layers will be kept have the same thickness everywhere; i.e. if a metal trace is laid down under a dielectric layer, the chip becomes thicker at that point [Fig. 4.9(a)]. In the IE3D modeling, the thicknesses of the dielectric materials are given as absolute values in the z direction [Fig. 4.9(b)]. The bulge over the metal traces is not taken into account in the calculations. Therefore,

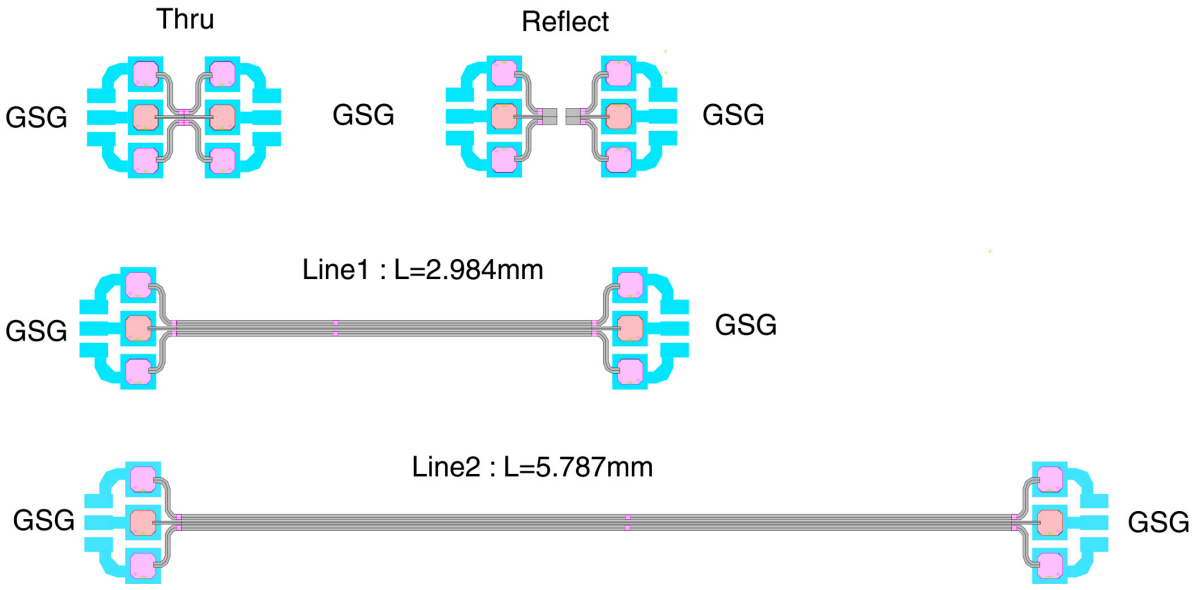


Figure 4.6: Four standards for the on-wafer TRL calibration.

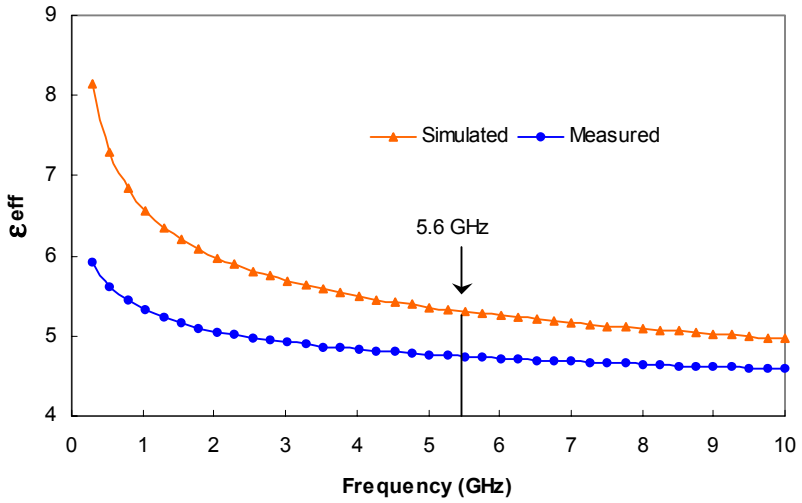


Figure 4.7: Measured and simulated effective dielectric constant of the CPW lines.

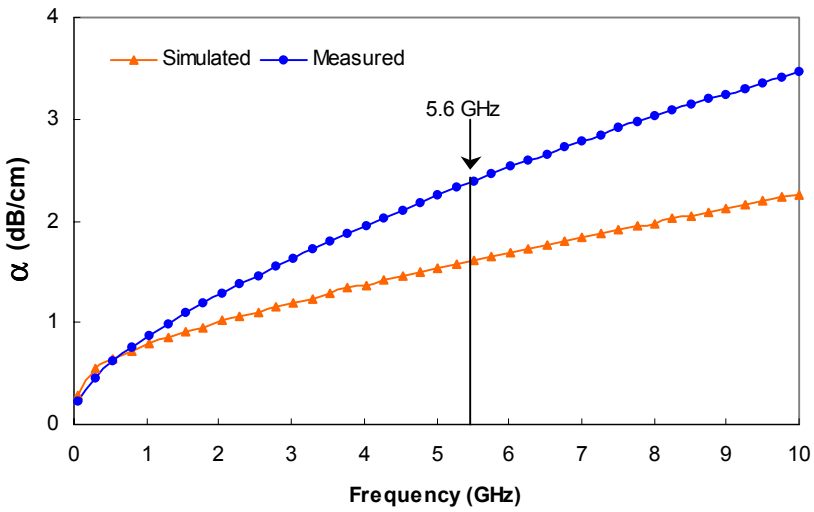


Figure 4.8: Measured and simulated loss (dB/cm) of the CPW lines.

wherever there are metals traces, the software will treat the dielectric layer as being thinner than the rest of the chip. This results in a higher effective dielectric constant of the CPW transmission line in the simulation.

4.2.2 Integrated Inductors

Gate Inductor

The gate inductor was laid out individually for on-wafer characterization as shown in Figure 4.10. A two-port on-wafer measurement is performed using the probe station and two-port S-parameter data was taken to extract the inductor model parameters. The measured S-parameters of the inductor can be converted to a π-network using Y-parameters (Fig. 4.11) [24]. Since port 2 of the inductor will be grounded in the PA circuits, the impedance of the inductor can be can then be calculated using [36]:

$$Z_L = \frac{1}{Y_{11}} \tag{4.1}$$

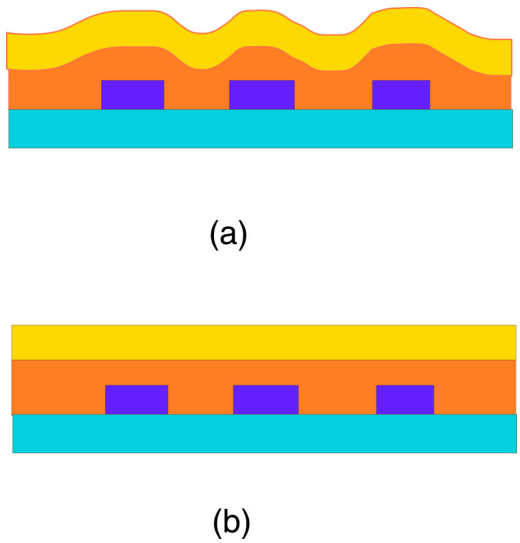


Figure 4.9: (a) side view of actual fabricated layers; (b) side view of layers in IE3D simulation.

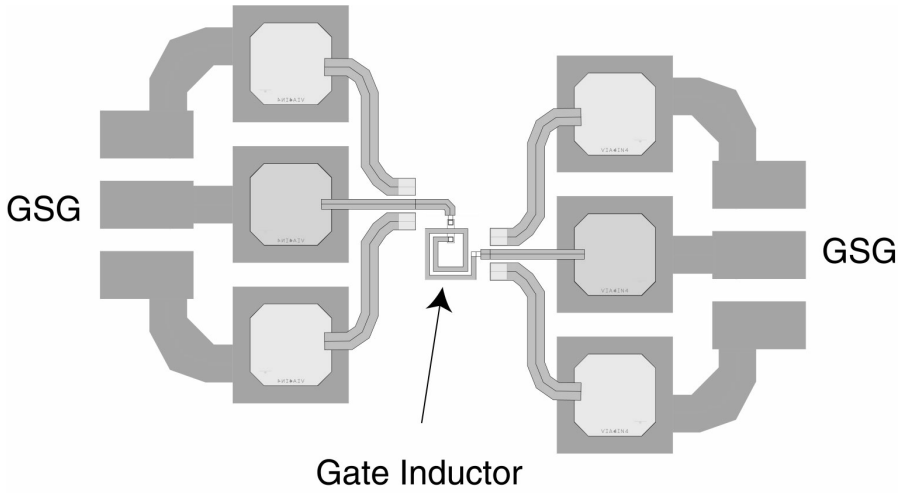


Figure 4.10: Individually laid out gate inductor for on-wafer measurement.

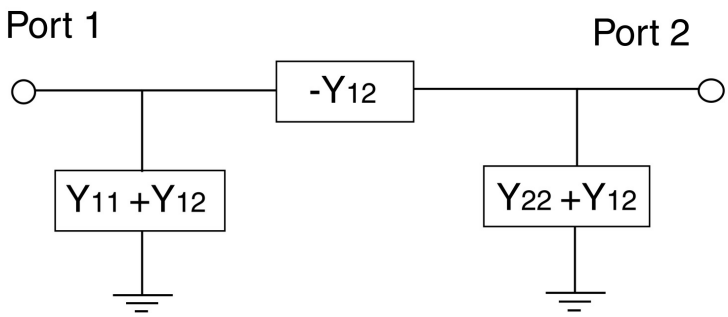


Figure 4.11: π equivalent circuit for a inductor using Y-parameters.

The effective inductance and Q are then given by:

$$L_{eff} = \frac{\mathrm{Im}(Z_L)}{2\pi f} \tag{4.2}$$

$$Q = \frac{Im(Z_L)}{Re(Z_L)} \tag{4.3}$$

The simulated and measured quality factor (Q) and effective inductance of the gate inductor are shown in Figures 4.12 and 4.13 respectively. The fabricated inductor has a measured Q of 8.0 vs. a simulated value of 9.3, the equivalent series inductance has a measured value of 0.41 vs. a simulated value of 0.27.This difference in the inductor values will affect the matching of the power amplifier circuits. The difference between the simulated and the measured results may due to the device modeling in IE3D as discussed in Section 4.2.1. Since the inductors are laid out in PG1 (4.5 μm) and are very close to the ground (7 μm), the deviation in the modeling will have a significant impact on the inductor performance (lower inductance values).

The calculated (Eq. 3.19 - 3.23), simulated and measured parasitics of the inductor are summarized in Table 4.1. Optimization in EEsof libra (Appendix A) was used to extract the equivalent model parameters from the simulated and measured S-parameter data. The measured L_s is larger than the calculated and simulated values. When using the measured S-parameter file of the gate inductor in the one-port simulation, the normalized admittance looking into the shunt inductor with connections is $0.30 - j2.81$. The absolute reactance value is smaller than the simulated results ($j3.87$). This will result in the input match moving to a lower frequency.

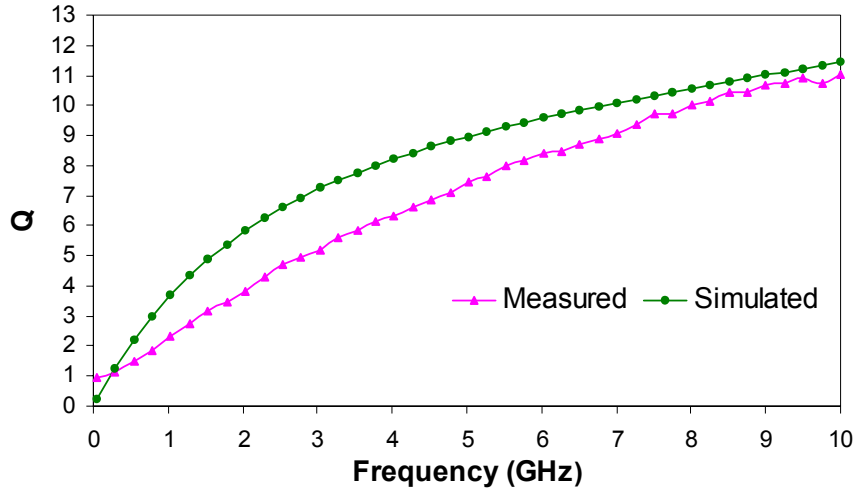


Figure 4.12: Q of the gate shunt inductor as a function of frequency (Measured and Simulated).

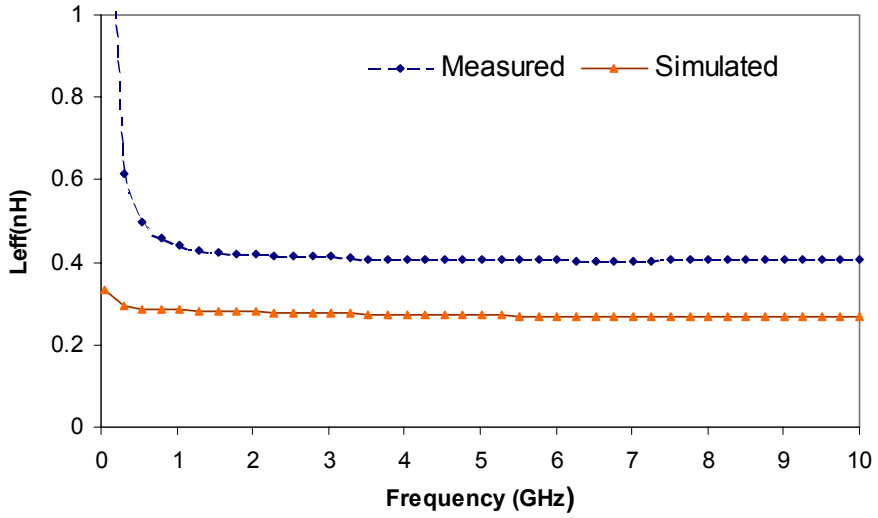


Figure 4.13: Equivalent inductance of the gate shunt inductor as a function of frequency (Measured and Simulated).

	Calculated	Simulated	Measured
$L_s(nH)$	0.25	0.26	0.39
$\delta(\mu m)$	0.97	–	–
$Rs(\Omega)$	1.63	0.92	1.30
$C_p(pF)$	0.00064	0.02	0.03
$C_1(pF)$	0.024	0.02	0.02
$C_2(pF)$	0.024	0.04	0.04

Table 4.1: Calculated, simulated and measured component values (Gate Inductor)

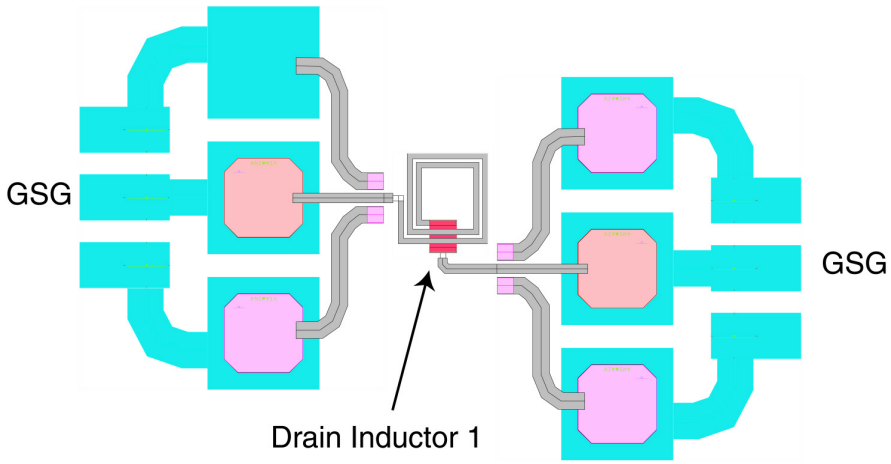


Figure 4.14: Individually laid out drain inductor 1 for on-wafer measurement.

Drain Inductor 1 (50 Ω antenna system)

The drain inductor 1 (50 Ω antenna system, Fig. 4.14) has a simulated Q of 9.2 compared to the measured value of 10.5 (Fig. 4.15). The measured inductance (0.92 nH) is higher than the simulated results (0.62 nH) (Fig. 4.16). The drain inductor is parallel connected at the drain of the MESFET. With a lager measured effective inductance value, the load impedance at the drain of the MESFET will move outside of the desired loadpull circle, resulting in reduced output power.The extracted effective inductor L_s from the calculated, simulated and measured results are $0.75nF$ $0.57nF$ and $0.85nH$ respectively (Table 4.2).

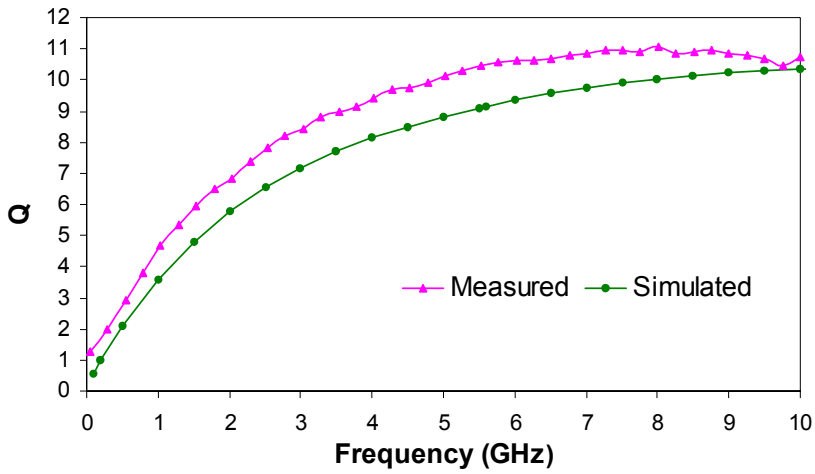


Figure 4.15: Q of Drain Inductor 1- 50 Ω load as a function of frequency (Measured and Simulated).

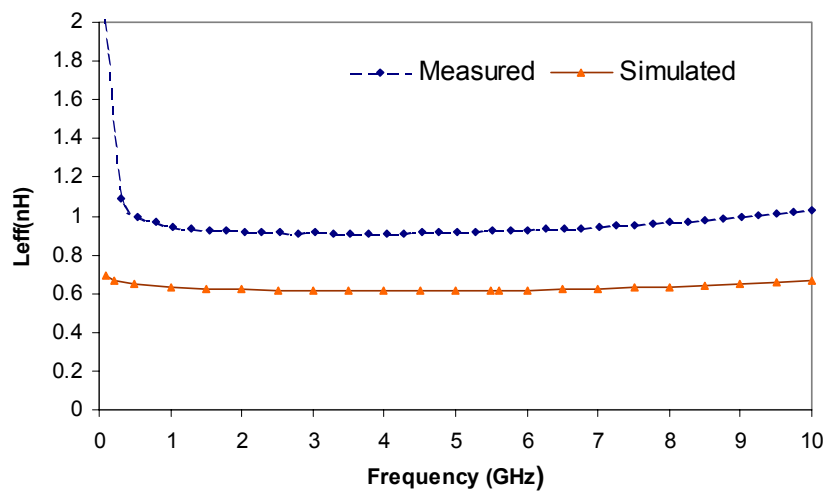


Figure 4.16: Equivalent inductance of Drain Inductor 1 - 50 Ω load as a function of frequency (Measured and Simulated).

	Calculated	Simulated	Measured
$L_s(nH)$	0.75	0.54	0.83
$\delta(\mu m)$	0.97	–	–
$Rs(\Omega)$	3.19	1.90	1.60
$C_p(pF)$	0.00149	0.12	0.04
$C_1(pF)$	0.066	0.07	0.06
$C_2(pF)$	0.066	0.08	0.08

Table 4.2: Calculated, simulated and measured component values for Drain inductor 1.

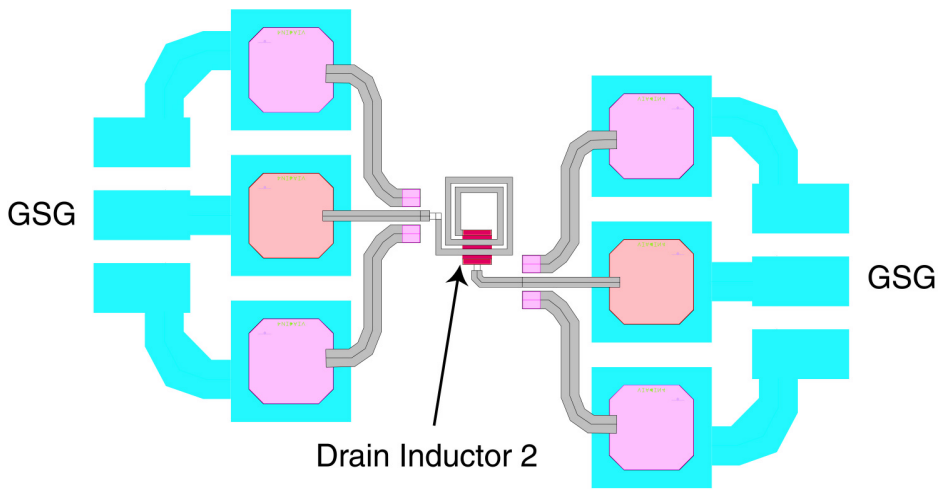


Figure 4.17: Individually laid out drain inductor 1 for on-wafer measurement.

Drain Inductor 2 (22.5 Ω antenna system)

The drain inductor 2 (22.5 Ω antenna system) has a measured Q of 10.9 vs. simulated value of 9.5 (Fig. 4.17). The measured L_s is about $0.67nH$ which is larger than the $0.45nH$ for the simulated case (Fig. 4.18 - 4.19).The extracted effective inductor L_s from the calculated, simulated and measured results are $0.60nF$ $0.43nF$ and $0.63nH$ respectively (Table 4.3). The larger effective inductance will result in a mismatch at the output and reduce the output power delivered to the load.

4.2.3 MESFET

The MESFET (w = 1260 μm) was laid out individually on chip in a common-source configuration with GSG pad connections at gate and drain for on-wafer measurement

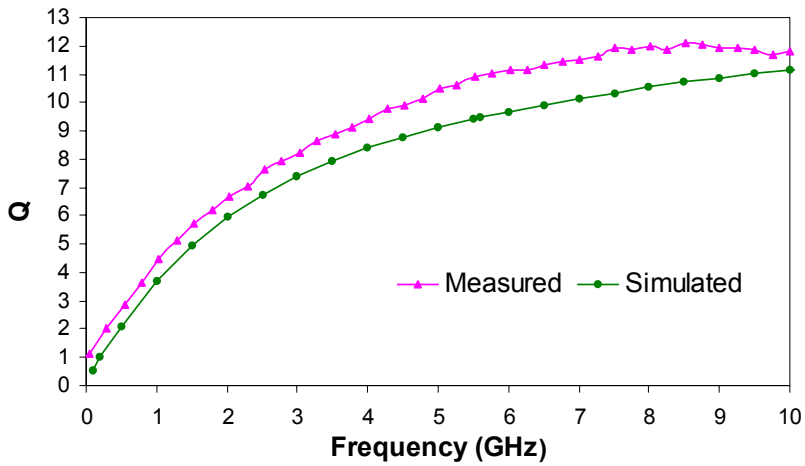


Figure 4.18: Q of Drain Inductor 2 - 22.5 Ω load as a function of frequency (Measured and Simulated).

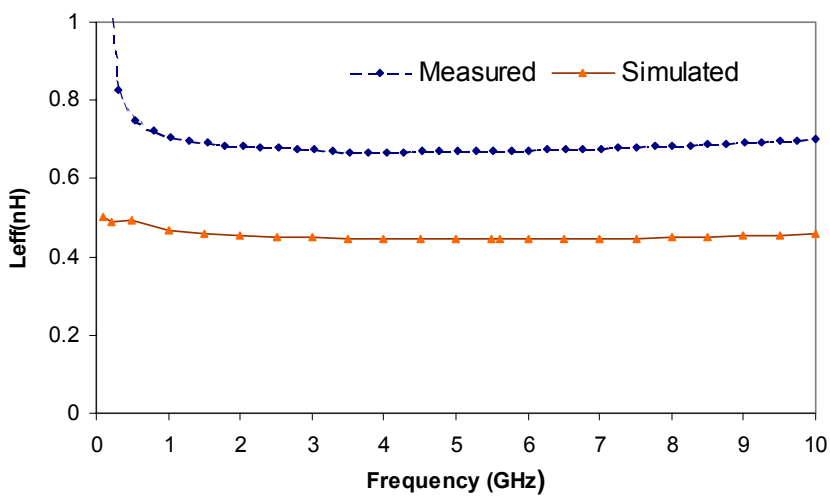


Figure 4.19: Equvalent inductance of Drain Inductor 2 - 22.5 Ω load as a function of frequency (Measured and Simulated).

	Calculated	Simulated	Measured
$L_s(nH)$	0.60	0.43	0.60
$\delta(\mu m)$	0.97	–	–
$Rs(\Omega)$	2.46	1.62	1.16
$C_p(pF)$	0.0012	0.0003	0.08
$C_1(pF)$	0.051	0.06	0.05
$C_2(pF)$	0.051	0.06	0.06

Table 4.3: Calculated, simulated and measured component values for Drain inductor 2.

(Fig. 4.20). The source contacts are tied to the system ground with vias to the PG2 layer. The S-parameter of the device were measured and the results are shown in Figure 4.21. The MESFET was biased at V_{gg} = -2V and V_{dd} = 5V using external bias tees (the bias tees were calibrated out of the measurements). The measured data is valid from 4GHz up to ~8.8GHz; beyond 8.8GH_Z, S_{22} rises above 0dB indicating that the device might not be stable in this range. Both the simulated and measured S_{11} for the device are shown on the Smith chart in Figure 4.22. At 5.6 GH_Z, S_{11} was shifted from 0.57+j3.33 (simulated) to 0.55+j1.88 (measured). The reactive component shows a significant difference between the simulation and measurement. This shift may be due to following reasons: (1) the parasitics between the electronics and the nearby PG2 ground; (2) the grounding vias at the source of the MESFET are inter-metal vias instead of backside vias as is the case in the standard process — the inter-metal vias are much shorter than the backside vias and reduce the inductive parasitics from source to the ground. The change of measured MESFET S_{11}will result in a shift in the input match of the power amplifier from the simulated design.

4.2.4 Power amplifier

The layout of a stand-alone PA (50 Ω output match) for on-wafer measurement is shown in Figure 4.23. The DC pads are located somewhat far from the transistor in order to allow a fair comparison with the two PA/Antenna structures.

In the case of the PA-Antenna structures mounted on a test board, the input signal goes through an RF connector, CPW line on the board, bondwires, pads, backside vias, CPW line on chip, and finally to the PA input (Fig. 3.18). However, the output signal from the PA goes directly to the antenna (50 Ω input) through a 50 Ω CPW

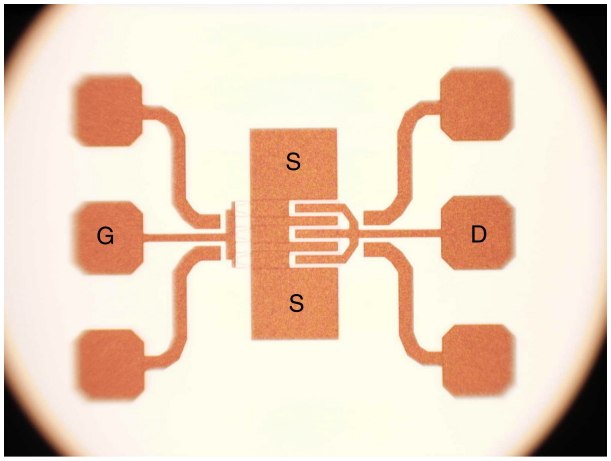


Figure 4.20: A micrograph of the MESFET (w=1260μm) prior to PG2 deposition.

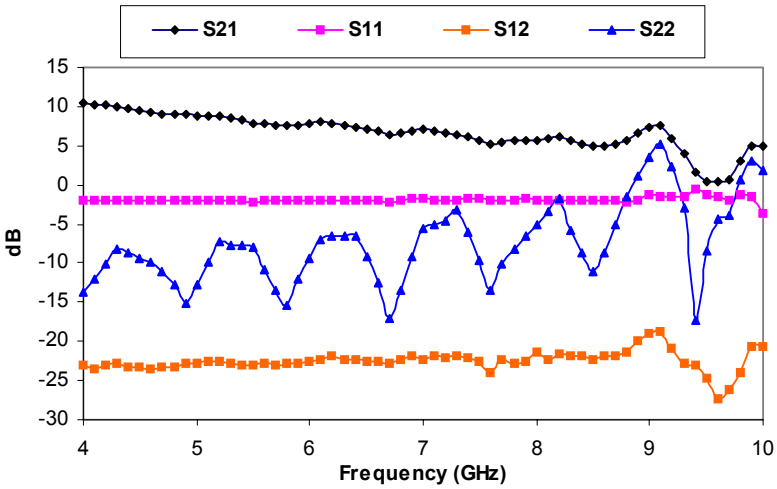


Figure 4.21: Measured S-parameters of the MESFET (W=1260μm).

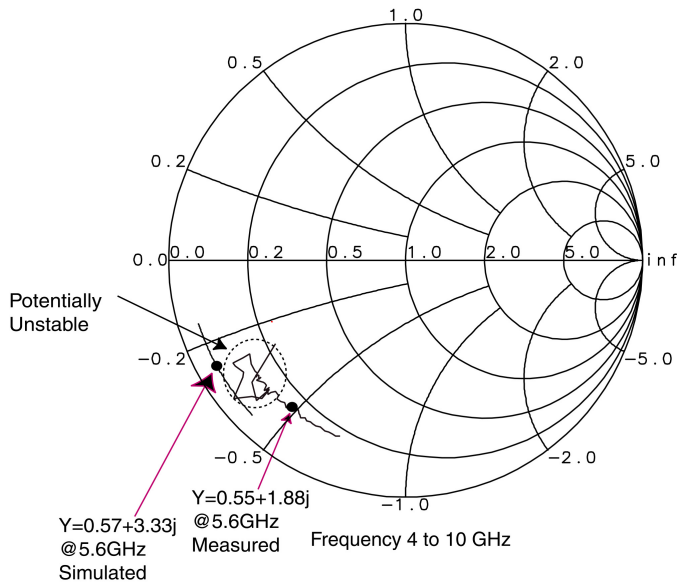


Figure 4.22: Simulated and measured S_{11} of the MESFET (w=1260μm).

transmission line and backside via. On the other hand, for the on-wafer measurement, the input signal goes directly to the PA through backside vias, so the effect of the bondwires is not present in the measurements. Furthermore, the output now leaves the PA, goes up through backside vias to the output probe pads. Therefore, the on-wafer measured data is not expected to match the simulations from Chapter 3.

The small-signal performance of the PA was measured using the probe station and the 8510 network analyzer. A 20 dB attenuator is inserted in line from the PA output to port 2 of the network analyzer in order to avoid damage of the equipment (calibrated out of measurements). The input matching was found to be shifted to ∼8GHz (Fig. 4.24). At the design frequency of 5.6 GHz, the PA has a return loss of 4.3 dB, a gain of 5.04 dB and S_{22} of -11.7 dB. The discrepancy between the simulated and measured results of the PA is believed to result from the deviations in the device model due to the nearby ground plane effect as well as the different input/output configurations. The measured S-parameters of the MESFET were then substituted for the device model in the simulation. The re-simulated PA linear response is shown in Figure 4.25. This simulation only uses the measured S-parameters from the MESFET; the other components in the design are still modeled versions. The result shows that

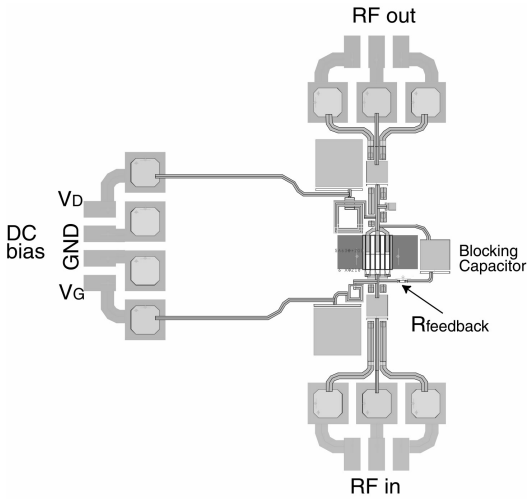


Figure 4.23: Layout of the power amplifier circuit (50 Ω output match) for on-wafer measurement.

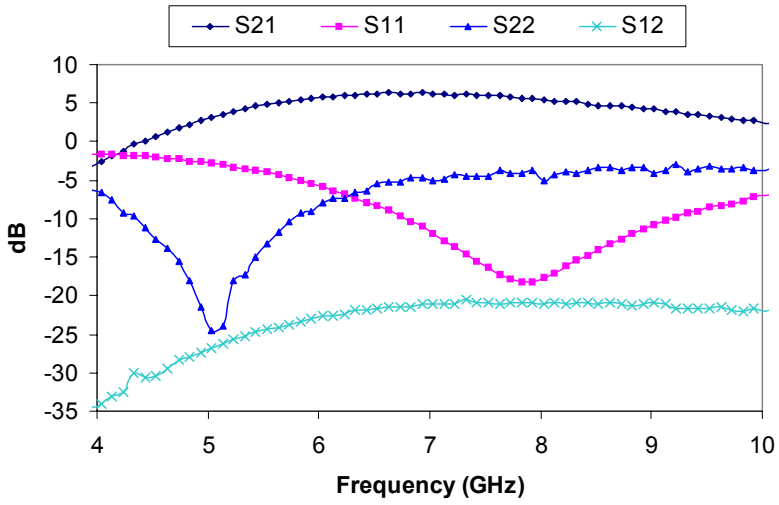


Figure 4.24: Measured small signal performance of the PA (50 Ω input/output).

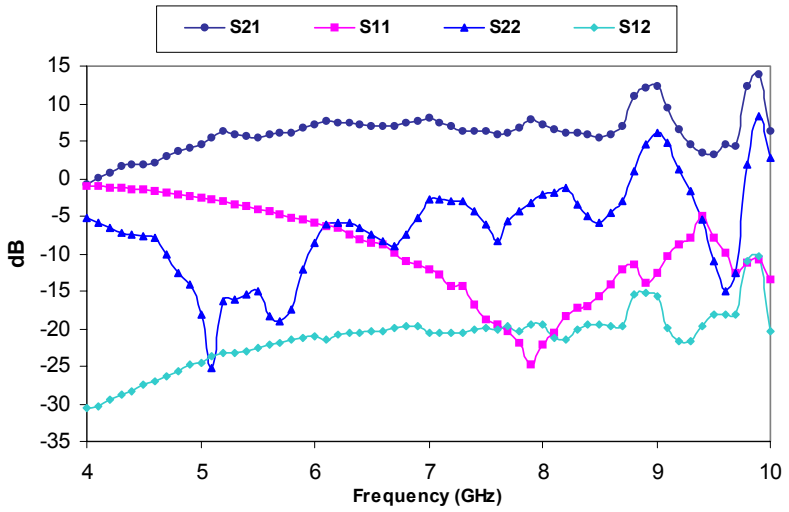


Figure 4.25: Re-simulated linear response of the PA using measured MESFET data.

the variation of the MESFET device parameters has a significant impact on the PA performance. In particular, the variation is largely responsible for the shift in input match to ~8GHz. The deviation in the PA performance is also affected by the limited accuracy of the inductor and transmission lines models from IE3D simulations.

4.3 Summary of the chapter

Four GaAs chip layouts were fabricated in the M/A-COM 5A GaAs MESFET process, with two active PA/antenna versions, one passive antenna version, and various test and calibration structures. On-wafer measurement results using Cascade probe station and 8510C VNA were presented along with the simulated results. TRL calibration was used to accurately measure the device and component parameters. The CPW transmission line results show good agreement with the simulated results. The measured on-chip inductors results show higher effective inductance values when compared with the simulated results, possibly due to the difference between the IE3D model and the actual fabricated structure. The measured S-parameters of the MESFET are significantly different from the foundry provided models because of the nearby ground effect, and therefore affect the power amplifiers design results.

Chapter 5

Antenna Measurements

In order to accurately measure antenna performance, the VT Antenna Group anechoic chamber (AntCom Near Field-Far Field system) was used. The tapered anechoic chamber is suitable for both far field measurements and near-to-far-field conversions. Antenna pattern, gain, directivity, efficiency, impedance, and polarization are the main performance parameters to be measured. A printed circuit test board was designed to accommodate the passive and active antenna chips, facilitating measurements in the anechoic chamber. The passive antenna and both active antennas were measured in the chamber and the results are compared. A standard gain horn antenna was used in the calibration to obtain the absolute gain of the antennas under test.

5.1 Test board

A custom test board was designed to support the antenna chips for the purpose of mounting in the anechoic chamber for pattern measurements. The test board was designed on five layer FR-4 material with the following parameters: roughness = 0.1 mil (2.54 μm), tanδ = 0.012, σ =4.1e7 S/m, ε_r=4.3 (Fig. 5.1).

The top metal layer was used for signal paths and DC supply connections. In this case the remaining four layers were only used as ground. The RF input signal paths were designed to be 50 Ω CPW lines using IE3D. Grounding vias were laid out judiciously

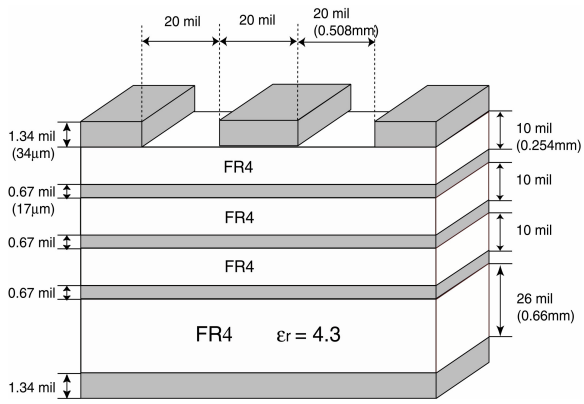


Figure 5.1: Test board layer assignment.

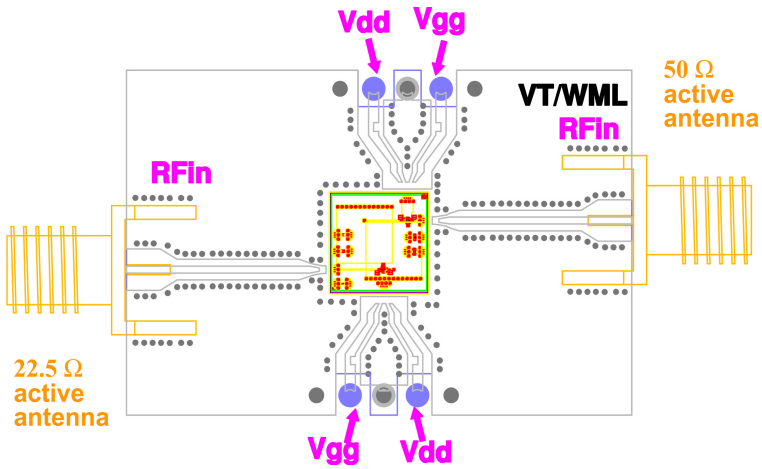


Figure 5.2: Layout of the standard custom testing board. The different RF input correspond to different versions of the antennas

along the signal paths and around the chip to help reduce cross-talk interference and to dissipate the heat generated by the power amplifier. The layout of the test board is shown in Figure. 5.2. The RF and DC feed lines on the board must be properly aligned to the bond pads on the chip for wirebonding. Since the two versions of the active antennas have their DC and RF pads at different relative positions, separate DC and RF inputs were designed on the same board to accommodate both antennas. The 50 Ω antenna and 22.5 Ω antenna chips are mounted 180° opposite to each other on their respective test boards.

A through line was fabricated on a separate test board to estimate the loss and

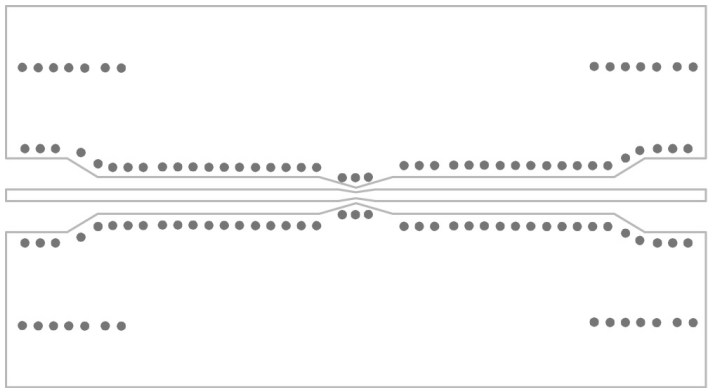


Figure 5.3: Printed circuit test board calibration through line.

characteristic impedance of the RF feeding line (Fig. 5.3). This line is essentially a back-to-back version of the RF input CPW lines on the antenna test board. The measured S_{11} and S_{21} of the through line is shown in Fig. 5.4-5.5. The results show that the CPW line is very close to the designed characteristic impedance of 50 Ω. The transmission loss is less than 1 dB and the return loss is better than 20 dB near 5.6 GHz, so that they will have little effect on the measured results for the antennas when mounted on board.

5.2 Antenna layouts

Three antenna designs were fabricated: one passive antenna with a 50 Ω input impedance; and two active antennas—one with an antenna input impedance of 50 Ω and the other with an antenna input impedance of 22.5 Ω. In order for a fair comparison, the three microstrip patches were laid out at the same positions on their 7 mm × 7 mm dies. No other test circuits were laid out along the radiating sides of the patches to avoid possible interference. The RF GSG pads were also located at the same position on the dies for all three antennas (Fig. 5.6). For the PA feeding the 50 Ω antenna, the power amplifier was located away from the patch and to one side; this was done to avoid interference between the antenna and the power amplifier circuits. The feeding line from the PA to the antenna input point is a 50 Ω CPW transmission line such that the PA sees a 50 Ω load impedance. In the case of the PA feeding the 22.5 Ω antenna, the power amplifier circuit is located below the patch

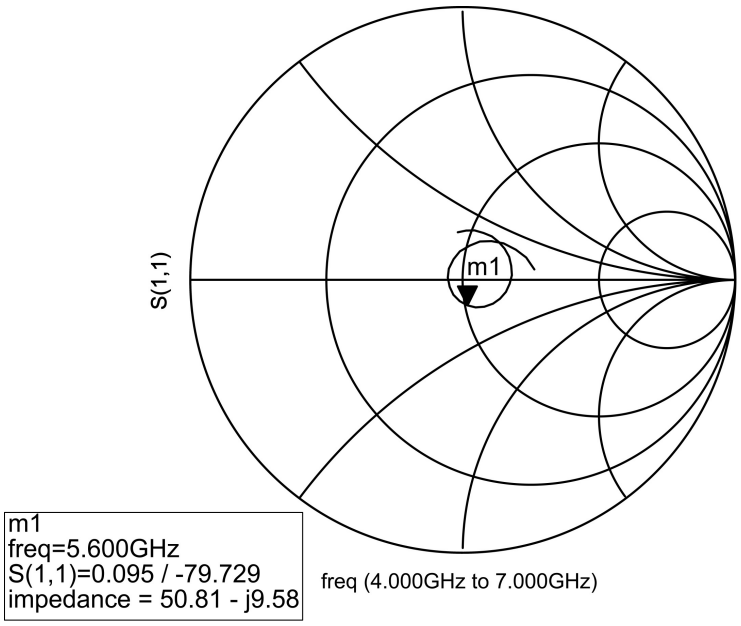


Figure 5.4: Measured S_{11} of the printed circuit test board.

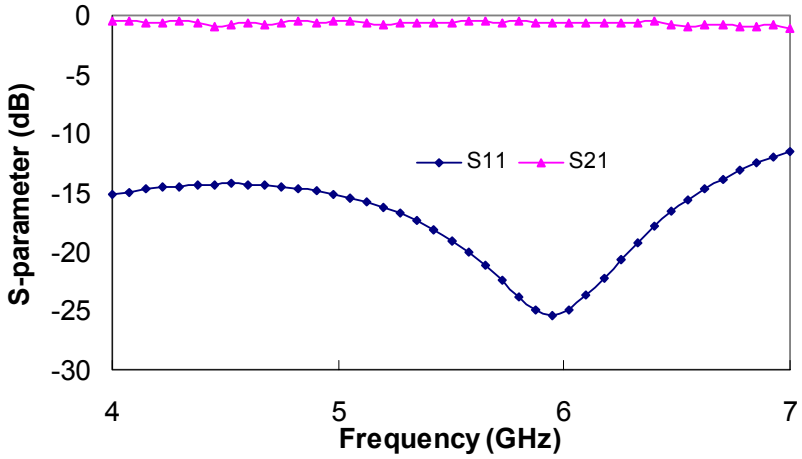


Figure 5.5: Measured S_{11} and S_{21} of the CPW transmission line on-board

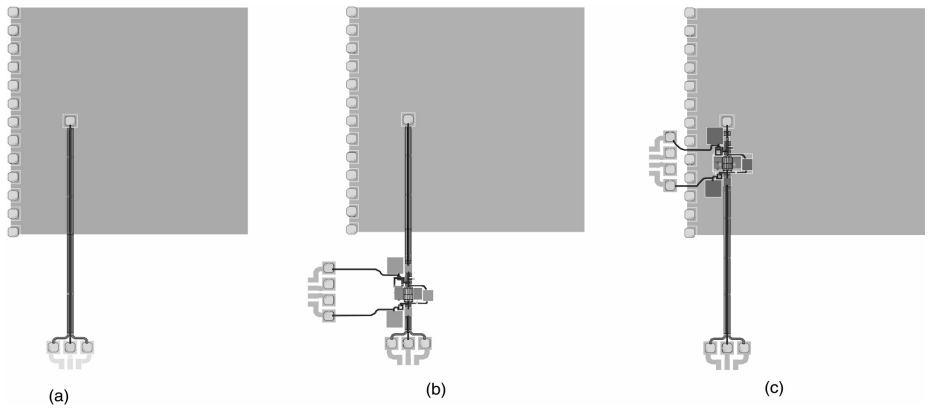


Figure 5.6: Layout of the three versions of antennas: (a) passive (b) active with 50 Ω input (c) active with 22.5 Ω input.

antenna and directly under the feeding point. Placing the power amplifier directly under the feeding point eliminates the transmission line between the output of the PA and the input of the antenna, so the PA output will still see a load of 22.5 Ω. This also allows investigation of the performance of the PA located directly under the antenna compared to the PA located away from the patch antenna.

5.3 Integrated antenna measurements

The backside of a fabricated and diced GaAs Active antenna chip is shown in Figure 5.7(a). Feeding GSG pads and backside vias can be seen on the micrograph since their fabrication involves backside processing. All the active circuitry is fabricated on the other side of the chip (front side) and covered by the ground plane (PG2), and can not be seen. As mentioned earlier, the RF signal will be fed to the GSG pads (either using probes or through bondwires—probes are shown in the photograph), and then will go through the backside vias to the electronics on the other side of the chip. The signal is then amplified by the PA and fed to the patch antenna to radiate. Fig. 5.7(b) shows an active antenna mounted in the anechoic chamber for pattern measurement. The antenna chip is mounted to the test board using conductive silver epoxy. The DC and RF GSG input pads are wirebonded to feeding lines on the test board (Fig. 5.8).

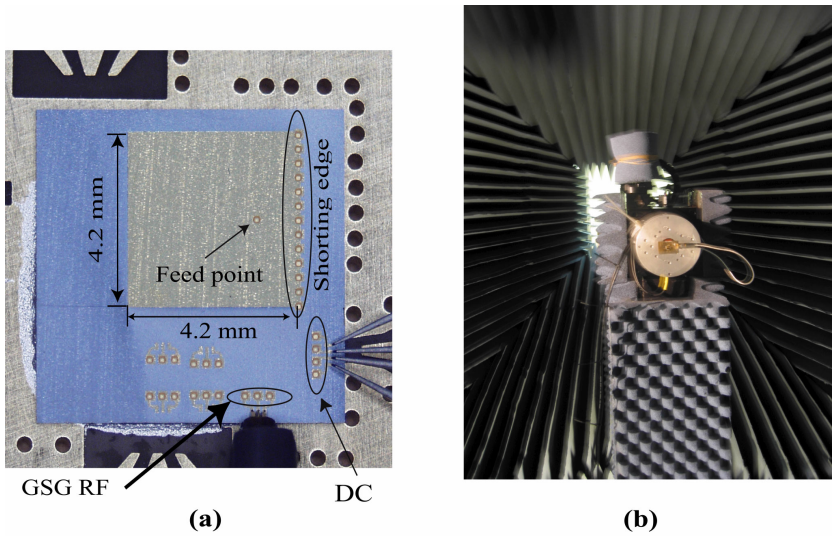


Figure 5.7: (a) Active antenna (backside view). The passive antenna is similar but without the DC pads. (b) Antenna mounted in the anechoic chamber for pattern measurements

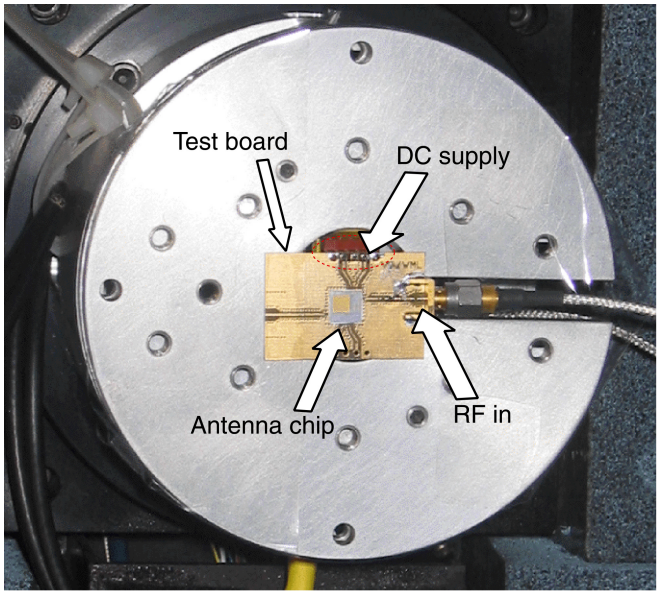


Figure 5.8: Photograph of an active antenna on a test board mounted on the antenna chamber positioner.

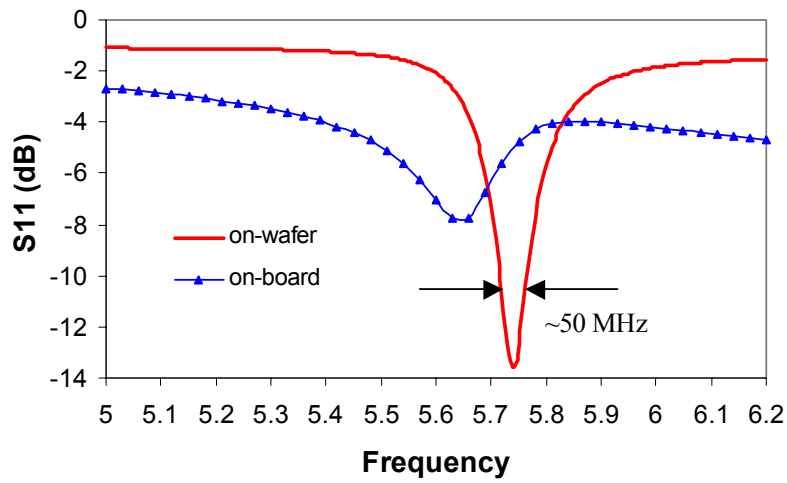
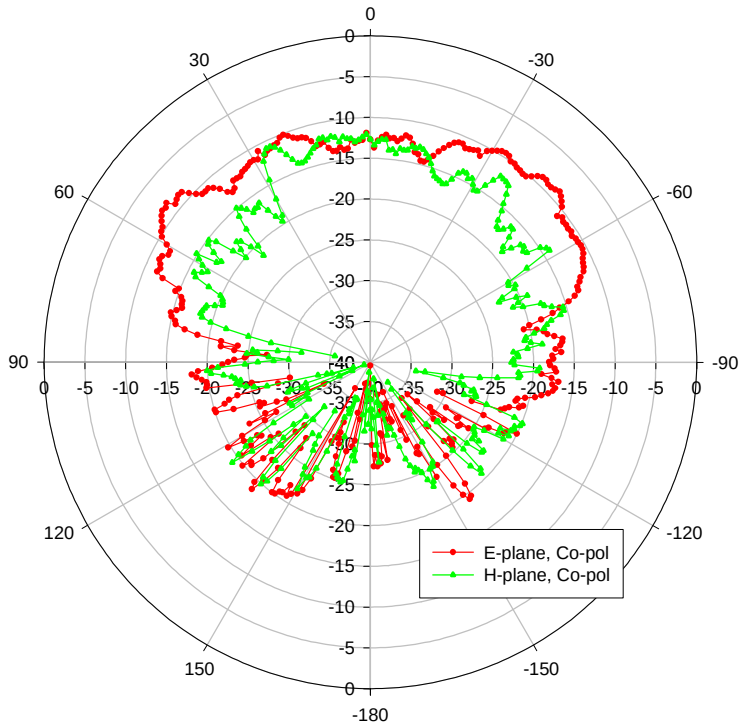


Figure 5.9: Measured passive antenna return loss: on-wafer vs. mounted on board with bondwire connections.

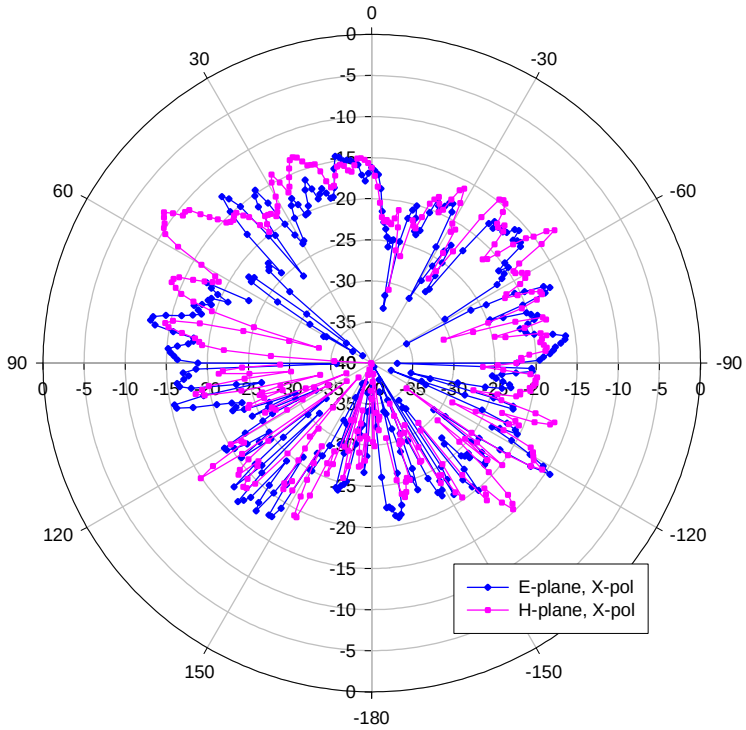
5.3.1 Passive Antenna

The passive antenna has a minimum on-wafer measured return loss of 13.6 dB at 5.74 GHz. When mounted on the test board for antenna chamber measurements, the input feed line and bondwires shift the antenna resonant frequency to 5.64 GHz (Fig. 5.9). The return loss is degraded to ~8dB. The measured E & H plane patterns are shown in the Figure 5.10. The gain on boresight is ~ -12.7 dB and the peak gain is ~ -8.8 dB. Note that the measured antenna gain includes board loss. The ripple in the pattern and the increase in cross-polarized radiation compared to the low frequency prototype (Section 2.6) is due to radiation from the board structure, bondwires, and transmission line. Since the 5× prototype (Figure 2.26) has a ripple free pattern, it is expected that future implementations with a BGA-type backside feed will have similar improved patterns.

In order to evaluate the effect of the test board and bondwires on the radiation pattern, another chip was fabricated with a 50 Ω resistor termination replacing the patch antenna at the feed point. This chip was mounted on the board in the same way as the passive antenna and patterns were measured (Fig. 5.11). Theoretically, the terminating resistor (50Ω) should absorb most of the energy instead of radiating it; therefore, the observed pattern should be due primarily to the board structures (e.g.

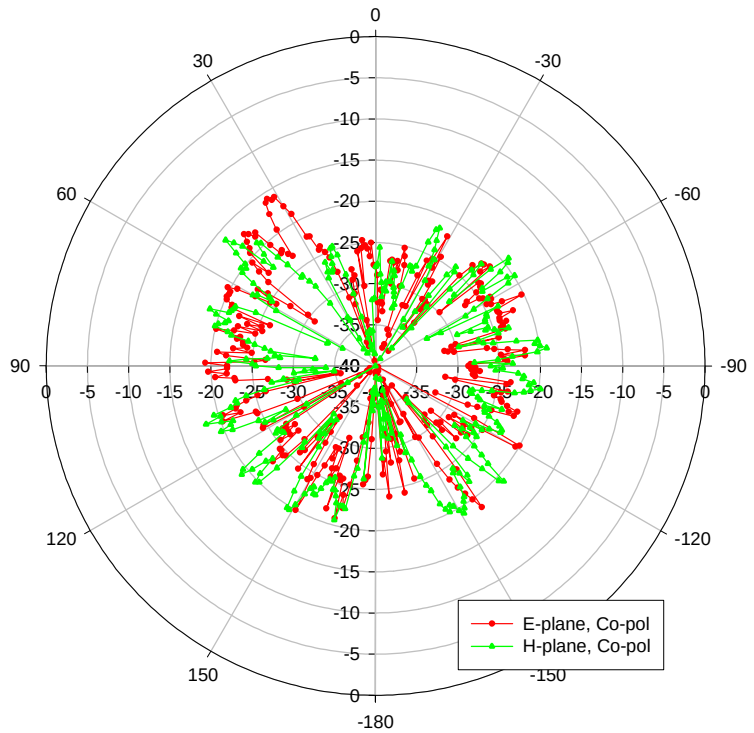


(a)

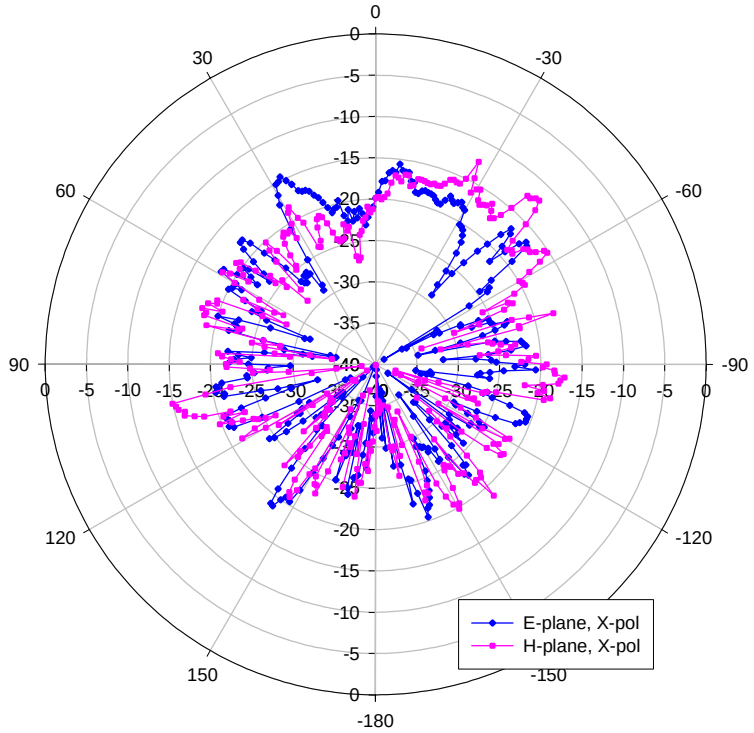


(b)

Figure 5.10: Measured E and H plane gain patterns of a passive antenna at $5.64\ GHz$: (a)Co-pol; (b) X-pol.



(a)



(b)

Figure 5.11: Measured E and H plane gain patterns of 50 Ω matched CPW line at $5.64\ GHz$: (a)Co-pol; (b) X-pol.

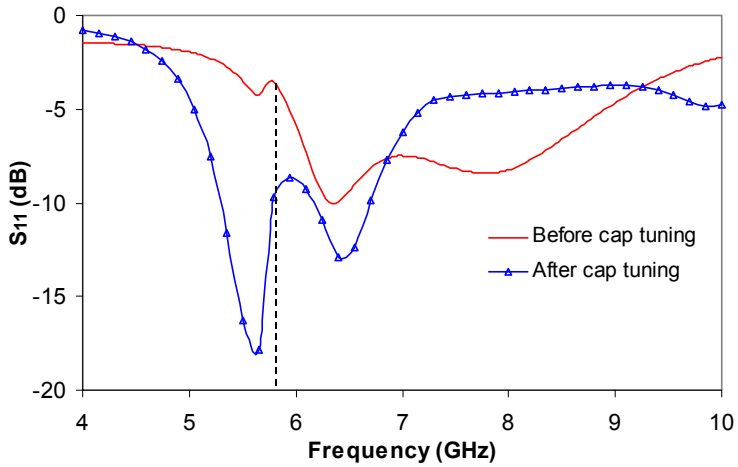


Figure 5.12: The input return loss of the 50 Ω active antenna (with and without 10 pF shunt tuning capacitor).

feedlines, bondwires etc.). However, on-wafer measurements show that the terminating resistor has a value of 78 Ω, so some of the input signal is reflected back resulting in further radiation from the board structures. The radiation from the resistor board is not symmetrical and peaks at $\sim 10^o$ - 50° to the right of the boresight. Therefore, the board structure does have some effect on the antenna patterns. However, the antenna radiation patterns are more symmetrical and well above the resistor pattern for a large range of angles. It can be concluded that the radiation from the passive antenna test board is mainly due to the patch antenna radiation.

5.3.2 Active Antennas (50 Ω)

As discussed in section 4.2.6, on-wafer measurements indicated that the power amplifier has its return loss peaked at ∼8 GHz. This is believed to primarily result from deviations in the MESFET device model due to the nearby ground plane. The active version of the 50 Ω antenna has its input match shifted to ∼6.4 GHz (Fig. 5.12). To compensate for this shift, a shunt capacitor (10pF) was placed on the test board to tune the input match to the desired frequency of ∼5.8 GHz.

The transmission coefficient (S_{21}) between the antenna under test (AUT) and test

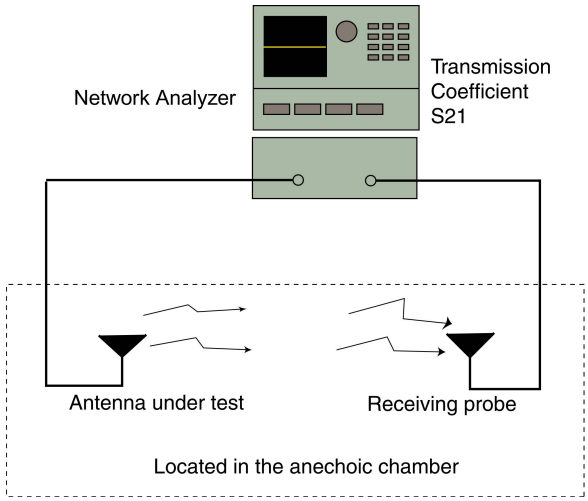


Figure 5.13: Measurement setup for S_{21} between the AUT and receiving reference antenna in the anechoic chamber using VNA 8530.

system antenna was measured to estimate the boresight gain of both the passive and active antennas. The AUT was mounted and aligned in the anechoic chamber as the transmitting unit, and the receiving probe served as the receiving antenna (Fig. 5.13). A Scientific-Atlanta 12F-3.9 standard gain reference horn antenna was used to calibrate the gain data. The passive antenna showed an S_{21} peaked ∼-11.97dB @ 5.705 GHz (Fig. 5.14). The 50 Ω active antenna shows a gain of -9.87dB @ 5.795 GHz when biased at V_G=-2V, V_D=5V, I_D=81mA. It was found that the gain of the 50 Ω active antenna was extremely sensitive to the DC bias voltage, and the bias was subsequently adjusted to optimize the gain of the active antenna. The boresight gain of the active antenna peaks at ∼-4.46dB @ 5.795GHz when biased at V_G=-1.45V, V_D=1.45V, I_D=124mA.

In order to measure the active antenna patterns, the test board was mounted on the positioner in the anechoic chamber. The positioner rotates 360° in azimuth in order to measure the horizontal cut of the pattern. Since the active antenna requires a DC power supply, long DC wires were required in order to use a standard power supply. The long DC supply wires introduced additional uncertainty into the measurements, and were difficult to install since they interfered with the rotation of the positioner. Therefore, a battery operated regulator (using LM317 regulator chips) was constructed and mounted conveniently on the positioner for proper biasing of the

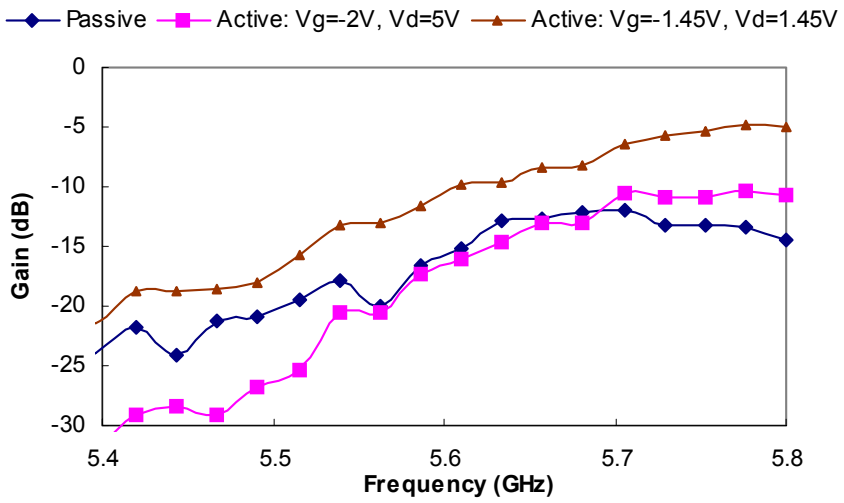


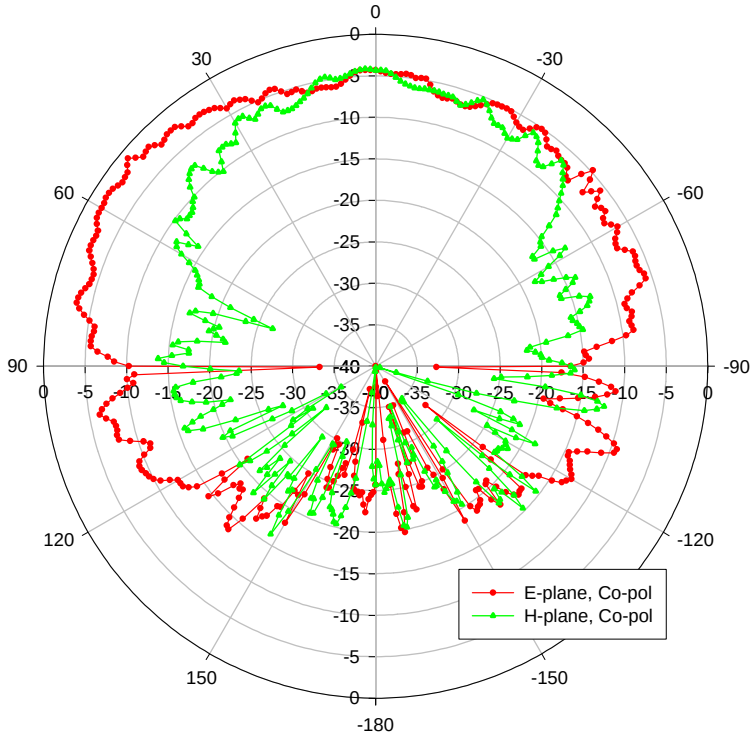
Figure 5.14: Measured boresight S_{21} with the 50 Ω antenna under test in the anechoic chamber.

active antenna (See Appendix B).

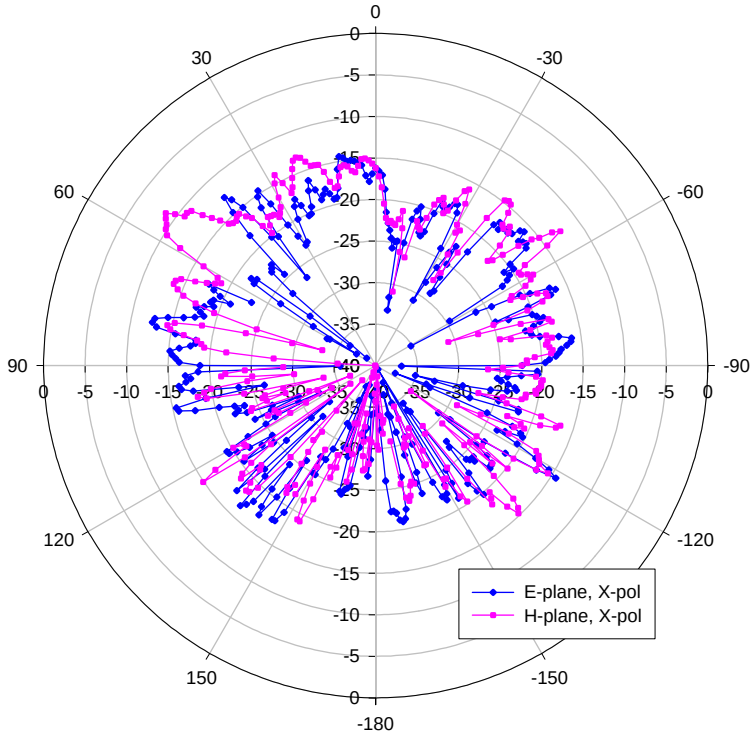
Antenna patterns of the retuned active antenna (50 Ω) were taken using the regulated battery supply. Gain sensitivity to bias condition was still encountered. The retuned active antenna has its radiation maximum at 5.80 GHz. It has a gain of –4.3dB on boresight and –1.1dB peak with the PA biased at V_G=-1.5V, V_D=1.6V (Fig. 5.15). Comparing the active with passive antenna patterns (Fig. 5.10), the shapes are very similar (both co-pol and x-pol) with the exception of the gain. The patterns indicate a ∼8.4dB gain resulting from the integration of the power amplifier on-chip with the antenna. This result is reasonably close to the designed PA gain of 12.7 dB. The cross-pol pattern of the active antenna shows a gain of –16.2 dB at boresight compared to a gain of –25.9dB from the passive antenna. This is also consistent with the gain improvement from the co-pol pattern of the active antenna.

5.3.3 Active Antennas (22.5 Ω)

The input impedance of the active antenna (22.5 Ω) is tuned to ∼5.7 GHz using a 10 pF capacitor on board with a return loss of ∼14 dB at ∼5.7 GHz (Fig. 5.16). Again, the S_{21} between the active antenna (AUT) and receiving reference antenna



(a)



(b)

Figure 5.15: Measured 50 Ω active antenna radiation patterns at 5.80 GHz: (a)Co-pol; (b) X-pol. The power amplifier is biased at V_{GG}=-1.5V, V_{DD}=1.6V using regulated battery supply.

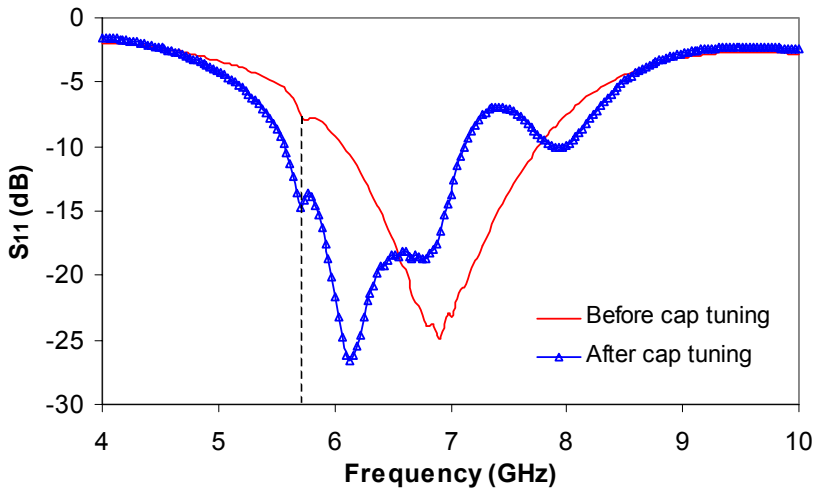


Figure 5.16: The input return loss of the active antenna (22.5 Ω) (with and without 10 pF shunt tuning capacitor).

was measured to estimate the boresight gain of both the passive and active antenna. The active antenna radiation of the 22.5 Ω active antenna was *not* sensitive to the bias voltage. The S_{21} shows a peak of –4.1 dB with PA biased at the designed bias voltage (V_{gg}=-2V, V_{dd}=5V) (Fig. 5.17).

The radiation pattern of the 22.5 Ω active antenna was measured at resonant frequency 5.725 GHz. The power amplifier was biased at Vgg=-2V, Vdd=5V using the battery operated regulator. The measured gain pattern of the active antenna shows a gain of -2.9dB at boresight and –2.5dB at its maximum (Fig. 5.18). The measured gain of the active antenna is 9.8 dB higher at boresight than that of the passive antenna. The measured cross polarization level of the active antenna at boresight is less than –13 dBi.

5.4 Summary of the chapter

The measured results of the passive and two active antenna were discussed in this chapter. Gain and efficiency results of the passive antenna agree reasonable well with the simulation results. The active antennas show 8.4–9.8 dB better gain than the

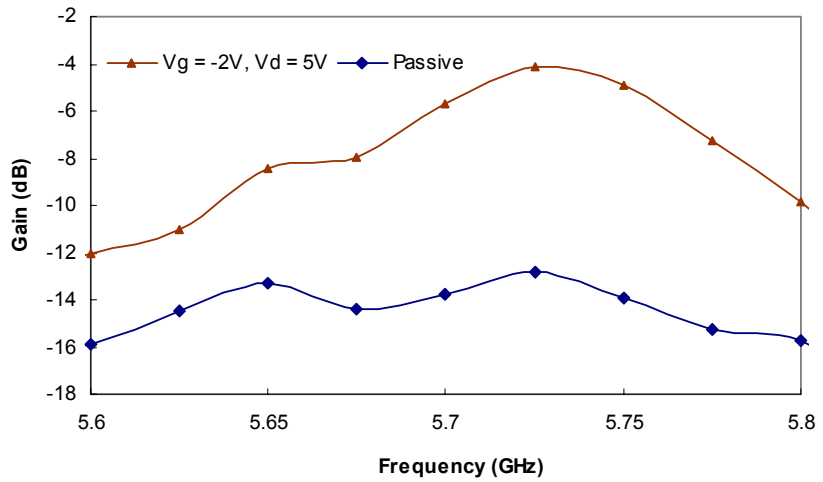
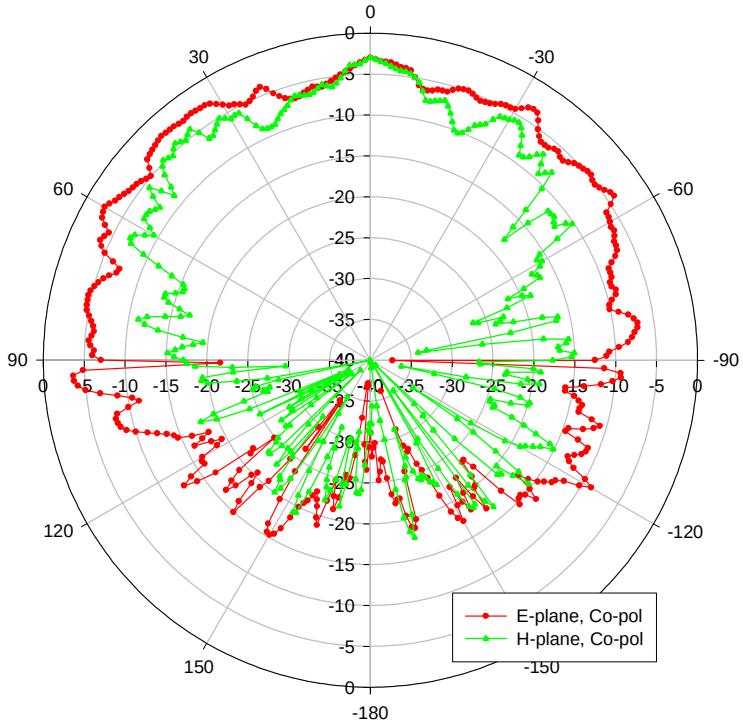
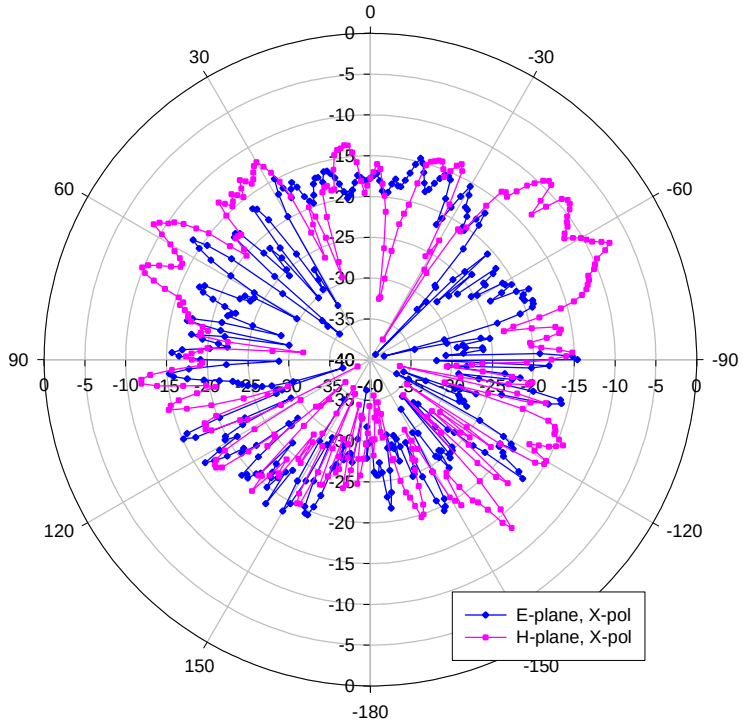


Figure 5.17: Measured boresight S_{21} with the antenna under test (22.5 Ω) in the anechoic chamber.

passive antenna (after input tuning); the gain is contributed by the power amplifier in front of the antenna. The gain of the 50 Ω active antenna was found to be very sensitive to DC bias, while the gain of the 22.5 Ω active antenna was not sensitive to the DC bias. This is believed to be due to the different positions of the power amplifiers relative to the patch antennas in the two cases. The PA for the 22.5 Ω active antenna was fabricated directly under the feed point and protected from coupling effects, while the PA of the 50 Ω active antenna was located outside the patch and was potentially affected by the radiation field. In retrospect, the PA of the 50 Ω active antenna should also have been located under its patch. In any event, the feasibility of direct integration of a PA with an on-chip antenna in a commercial GaAs process at RF frequencies was successfully demonstrated.



(a)



(b)

Figure 5.18: Measured 22.5 Ω active antenna radiation patterns at 5.725 GHz: (a)Co-pol; (b) X-pol. The power amplifier is biased at V_{GG}=-2V, V_{DD}=5V using regulated battery supply.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

The co-design of integrated chip-scale antennas and power amplifiers in GaAs IC technology has been investigated. The antennas were designed on a GaAs substrate, with a high dielectric constant of 12.9. The size of the antenna is about 4.2mm×4.2mm, which is ∼1/13 of λ_o at ∼5.6GHz. The antenna input impedance depends on the feed position; by adjusting the feed point, the antenna can be tuned to match a 50 Ω or other system impedance. The integrated antenna suffers from relatively low radiation efficiency ($\sim 3\%$) and bandwidth ($\sim 1\%$), but has the potential for ultra-miniature, short-range, low power wireless microsystem applications. The integrated passive antenna has a measured boresight gain of $\sim -12.7\ dB$, the low gain is due to the combination of high ε_r and thin substrate resulting lower radiation (fringing) fields.

Class A tuned MESFET power amplifiers (PAs) were designed with outputs directly matched to the antenna feed point. The antenna is fabricated on the backside of the chip through backside patterning; the PA feeds the antenna through a backside via. The structure is then mounted such that the antenna faces up, and is compatible with flip-chip technology. The integration of a PA offsets most of the gain degradation of the small antenna. For the 50 Ω active antenna, the gain of the integrated PA was found to be very sensitive to the DC bias. A gain of ∼8.4 dB due to the PA was observed. For the 22.5 Ω active antenna, the gain of the integrated PA was not

sensitive to the DC bias. A gain of $\sim$ 9.8dB due to the PA was observed. This gain sensitivity difference is believed to be due to the different positions of the power amplifiers relative to the patch antennas in the two cases. The PA for the 22.5 Ω active antenna was fabricated directly under the feed point and protected from coupling effects, while the PA of the 50 Ω active antenna was located outside the patch and was potentially affected by the radiation field. In any event, the feasibility of direct integration of a PA with an on-chip antenna in a commercial GaAs process at RF frequencies was successfully demonstrated.

6.2 Future Work

Future work includes:

- True flip-chip technology implementation (Fig. 6.1). Based on comparison with 5X prototype, the ripple in the active antenna patterns should be largely reduced by eliminating the need for bondwires and backside pad feeding structures. Accurate modeling of transistors and on-chip passive components in the flip-chip environment are essential for further success in the active antenna design.
- Integration of Antenna, T/R switches, PA and LNA to realize fully integrated RF transceivers (Fig. 6.2).
- Some other methods can be used to improve the bandwidth and efficiency: for example, the use of thicker substrates with non-via feeding schemes or slightly lower ε_r substrates.
- Other RFIC technologies such as SiGe may be used to enable highly integrated system-on-chip solutions given that high-resistivity substrates and via hole processes are available in said technologies.

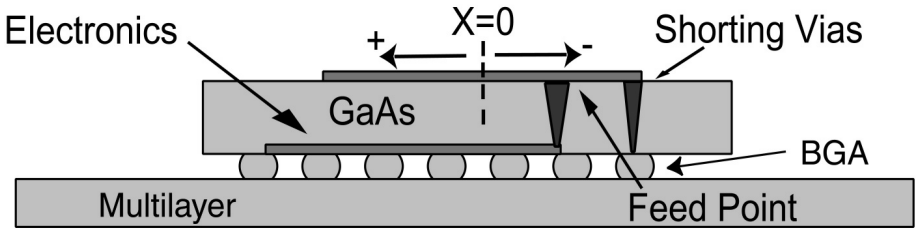


Figure 6.1: Flip-chip implementations of the integrated active antennas.

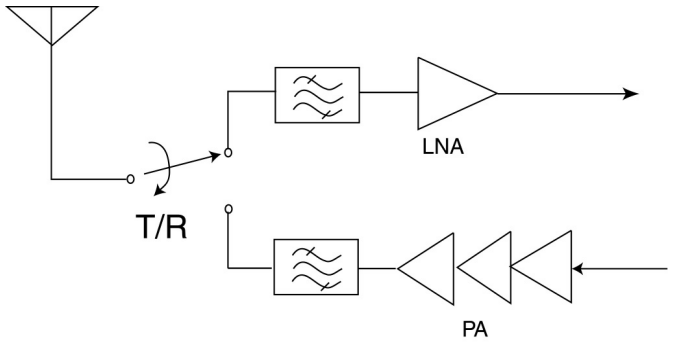


Figure 6.2: Full transceiver implementation.

Appendix A

PA Analysis with Series IV

This appendix contains the HP EEsof Libra circuit test bench for inductor circuit extraction (Fig. A.1), test bench for the power amplifier simulation (Fig. A.2), and the schematic of the 50 Ω power amplifier circuits (Fig. A.3).

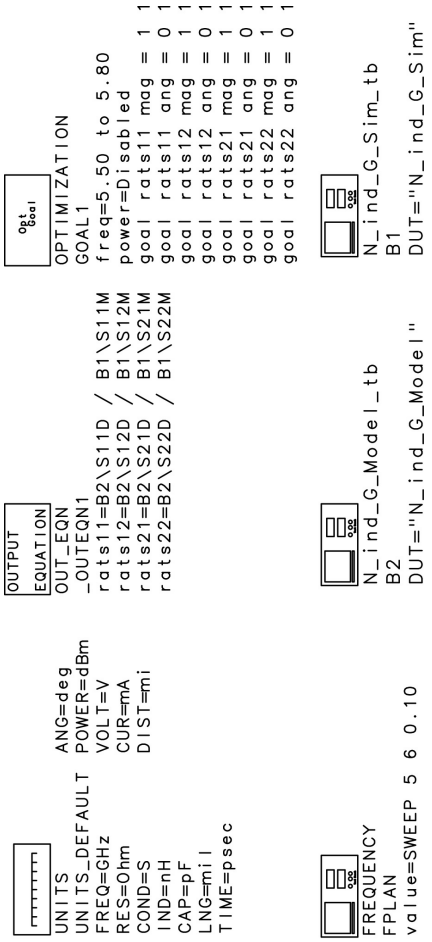


Figure A.1: A schematic of the optimization test bench used to extract inductor parasitic values from S-parameters data. The testbench N_ind_G_Sim_tb is the 2-port S-parameter data file and the test bench N_ind_G_Model_tb is the circuit shown in Fig. 3.20 with optimizable components.

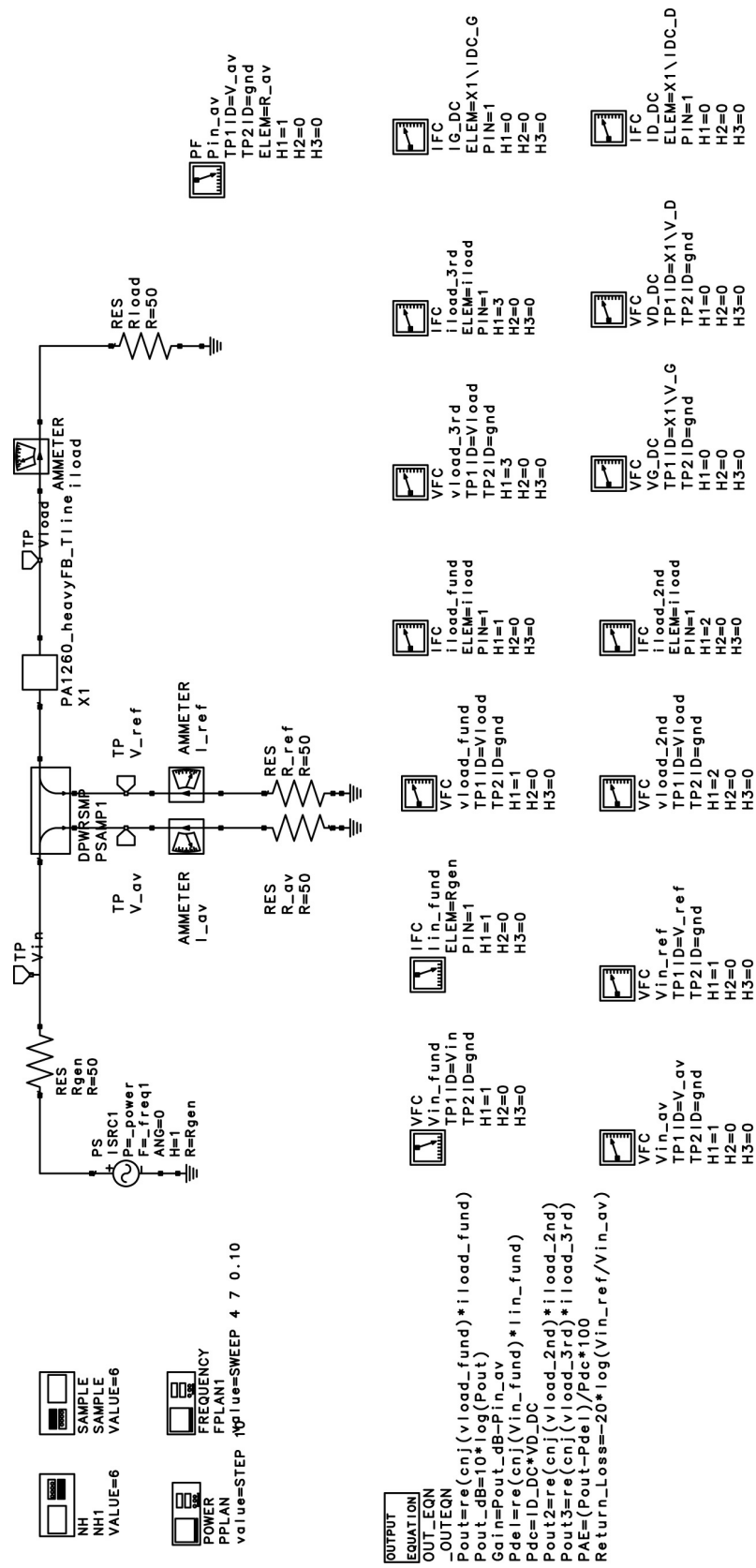


Figure A.2: Power amplifier test bench.

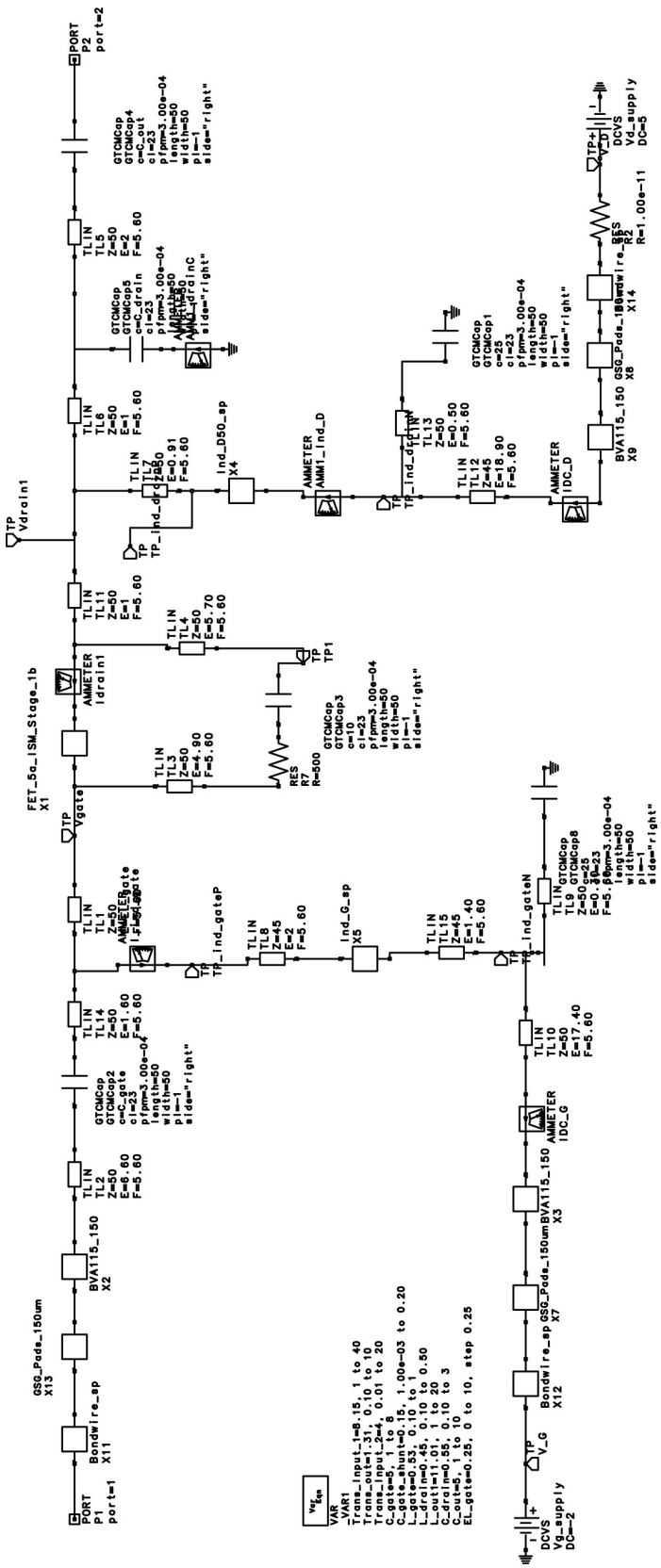


Figure A.3: A schematic of the PA (50 Ω) circuit.

Appendix B

Regulator for active antenna measurement

This appendix contains a circuit schematic of the regulator circuits used to provide DC power to the active antennas in the antenna measurement chamber(Fig. B.1).

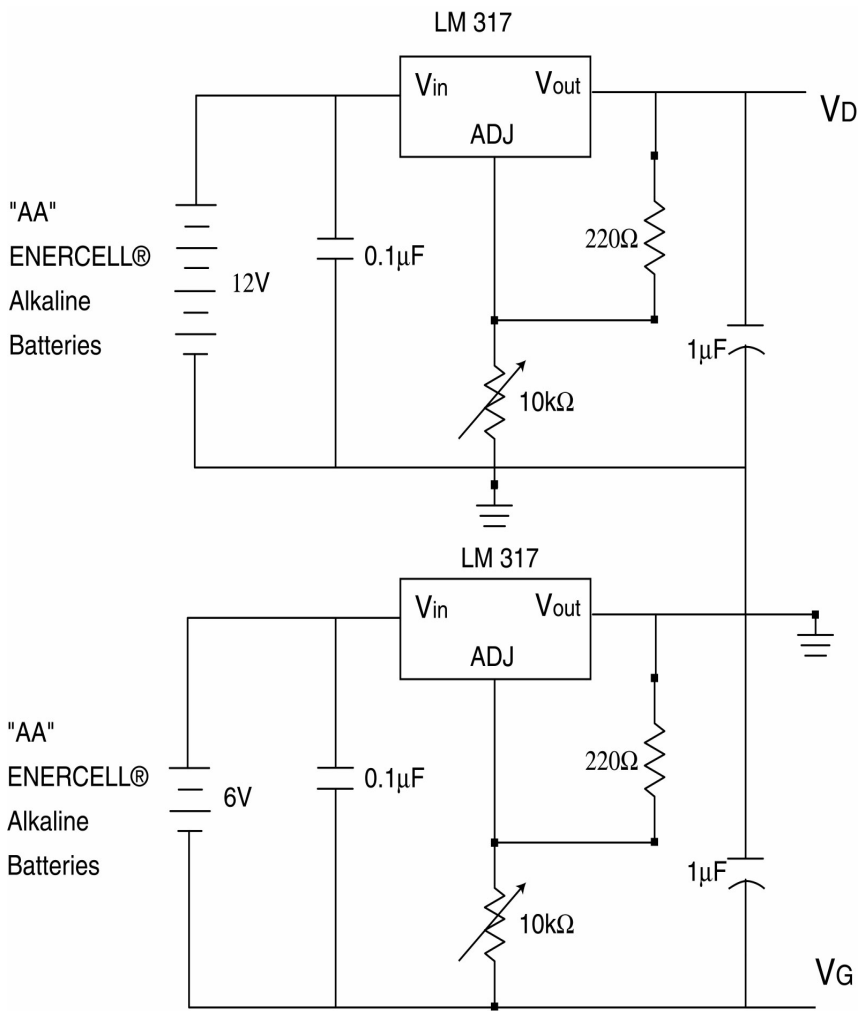


Figure B.1: A schematic of the regulator circuits

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Vita

Jun Zhao was born in Beijing, China. He received his Bachelor of Science degree from Peking University, China. Then he came to the U.S. and received Master of Science degree in physics from Montana State University. Jun Zhao will have completed the requirements for the Master of Science degree in Electrical Engineering at Virginia Tech in August 2002.