Advanced Energy-Efficient Devices for Ultra-Low Voltage System: Materials-to-Circuits

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ABSTRACT

With the proliferation of connected computing devices into consumer, medical, and communication application spaces (i.e., the internet of things, IoT), device-circuit co-design has become increasingly relevant to the development of energy-efficient embedded electronics. Similarly, power dissipation has become a key issue for portable and embedded systems in which supply power is limited due to limited battery lifetimes. An effective approach to reduce power dissipation has been a continual reduction in supply voltage, thereby quadratically scaling active power dissipation. However, as state-of-the-art silicon (Si) CMOS devices enter sub-threshold operation in the ultra-low supply voltage regime, their drive current is noticeably degraded. Consequently, additional transistors must be incorporated in order to maintain low voltage circuit functionality. As a result of the large number of functional blocks in modern integrated circuits (ICs), these extra transistors contribute to significant additional power dissipation, thereby nullifying the benefits gained from supply voltage reduction. Therefore, new energy-efficient devices and circuits must be introduced. In this work, tunnel field-effect transistors (TFETs), which exploit the band-to-band tunneling (BTBT) mechanism as a means of source injection, are investigated. The steep subthreshold dynamics and high drive current (at low operating voltages) of TFETs enable full functional scaling into the ultra-low voltage operating regime. Additionally, comprehensive material and interface analysis is performed in order to investigate the feasibility of mixed As/Sb and Ge/InGaAs TFETs. Subsequent TFET design and optimization, performed via numerical simulation using a computer aided design (CAD) suite, is undertaken to provide device performance guidance under ideal and non-ideal

operation. These results are further leveraged in the development of TFET-based static random-access memory (SRAM) cells due to the proliferation of low-voltage embedded devices and increasing areal density of on-chip memory. Lastly, a novel, TFET-based adiabatic logic architecture (TBAL) is introduced. Adiabatic logic is an alternative approach to conventional combinational logic wherein a logical operation is, ideally, a reversible adiabatic process. Consequently, the change in energy level in an adiabatic circuit is significantly lower than that of conventional combinational logic, leading to almost no energy dissipation. Combined with the previously discussed technologies, this work proposes an advanced complimentary metal-oxide-semiconductor (CMOS) platform that could save considerable energy and reduce power consumption in next-generation, ultra-low voltage applications.

Advanced Energy-Efficient Devices for Ultra-Low Voltage System: Materials-to-Circuits

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GENERAL AUDIENCE ABSTRACT

The overall energy consumption of portable devices has been projected to triple over the next decade, growing to match the total power generated by the European Union and Canada by 2025. The rise of the internet-of-things (IoT) and ubiquitous and embedded computing has resulted in an exponential increase in such devices, wherein projections estimate that 50 billion "smart" devices will be connected and "online" by 2020. In order to alleviate the associated stresses placed on power generation and distribution networks, a holistic approach must be taken to conserve energy usage in electronic devices from the component to the circuit level. An effective approach to reduce power dissipation has been a continual reduction in operating voltage, thereby quadratically down-scaling active power dissipation. However, as state-of-the-art silicon (Si) complimentary metal-oxide-semiconductor (CMOS) field-effect transistors (FETs) enter sub-threshold operation in the ultra-low supply voltage regime, their drive current is noticeable degraded. Therefore, new energy-efficient MOSFETs and circuit architectures must be introduced. In this work, tunnel FETs (TFETs), which operate leveraging quantum mechanical tunneling, are investigated. A comprehensive investigation detailing electronic materials, to novel TFET device designs, to memory and logic digital circuits based upon those TFETs is provided in this work. Combined, these advances offer a computing platform that could save considerable energy and reduce power consumption in next-generation, ultra-low voltage applications.

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For

My Parents,

and

My Beloved.

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Chapter 8 - **Conclusion and Future Prospects**

Chapter 1

Introduction

1.1 Internet of Things: Challenges

As the twenty first century progresses, the world continues to become a smaller place, with an unprecedented scale of human connectivity, enabled by a network of interconnected intelligent devices. The quality of human life has been significantly improved through this network of embedded devices for sensing, signal processing, communication, and data analysis, which constitute the so-called Internet of Things (IoT). According to a recent report, there will be over 50 billion connected devices by the year 2020, with each individual having an average of 6 devices online at the same time, as shown in Figure 1.1 [1]. Furthermore, IoT will be deployed for a variety of applications including sensor networks (e.g. for environmental control), body-area networks (for mobile and medical uses), and home networks (control, security). Majority of these IoT devices are powered by limited capacity batteries or energy harvesters. There is need for an optimized balance between cost (for massive numbers of IoT devices), performance (for multipurpose devices), and energy requirements (for limited power resources) for embedded devices and systems. As a result, device-circuit-system co-design becomes extremely important to achieve an effective solution of power consumption.

In contrary to the past 40 years of Moore's Law scaling, IoT devices reshaped modern technological trend from higher performance to energy-efficiency. In the past few decades, the scaling of complementary metal-oxide-semiconductor (CMOS) and the innovation in lower-power circuits have decreased power consumption significantly, which has made IoT feasible even with limited powered resources. However, conventional CMOS transistors face

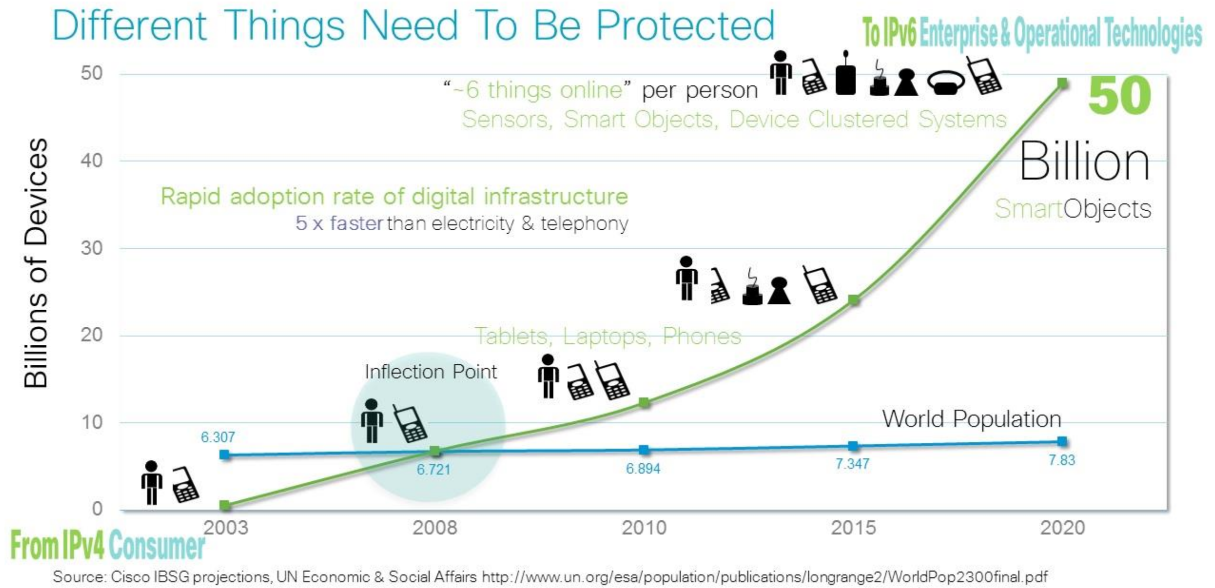


Figure 1.1: The numbers of connected devices for IoT application [1].

challenges while pursuing further power reduction into the ultra-low power regime. Therefore, it is essential to develop new devices, circuits, and logic from the standpoint of power management for the ultra-low power IoT application space.

1.2 Power Consumption in IoT Devices and Limitation of CMOS Technology

The net power consumption by a CMOS logic is given by [2]:

$$P_{total} = P_{active} + P_{passive}$$
$$= \alpha C V_{DD}^2 f + I_{off} V_{DD} \quad (1.1)$$

where α is activity factor, C represents the system capacitance, f is operation frequency, V_{DD} represents supply voltage and I_{off} is OFF-state currents. According to Eq. 1.1, reduction of supply voltage V_{DD} is the most efficient way to cut down power consumption due to the quadratic and linear dependence on active power and passive (OFF-state) power, respectively. Passive power consumption can be further reduced by suppressing I_{off} in standby mode. For

IoT applications, a chip will spend most of its time in hibernation, waking up occasionally to execute assigned tasks. As a consequence, leakage current is critical in OFF-state (deep sleep mode). On the other hand, active power is almost unchangeable since there is no additional design freedom in Eq. 1.1. Therefore, new logic design must be implemented to further reduce the power consumption while ensuring no significant change in existing algorithms.

In addition, supply voltage scaling also heavily impacts the transistor ON-state current and device performance. The ON current for conventional CMOS at saturation can be expressed by [3],

$$I_{ON} = \frac{1}{2}\frac{W}{L}\mu_{eff}C_{ox}(V_{DD} - V_{th})^2 \tag{1.2}$$

where I_{ON} is the ON current, W is the transistor width, L is the transistor length, μ_{eff} is effective carrier mobility, C_{ox} is the oxide capacitance, and V_{th} is the threshold voltage. With the reduction of V_{DD}, I_{ON} also decreases consequently, and thus, deteriorating the device and circuit performance. There are four ways to enhance ON current while reducing V_{DD}: (i) scaling down the channel length L, (ii) enhancing carrier mobility, (iii) increasing oxide capacitance, and (iv) reducing threshold voltage. Over the past few decades, the miniaturization of Si-based

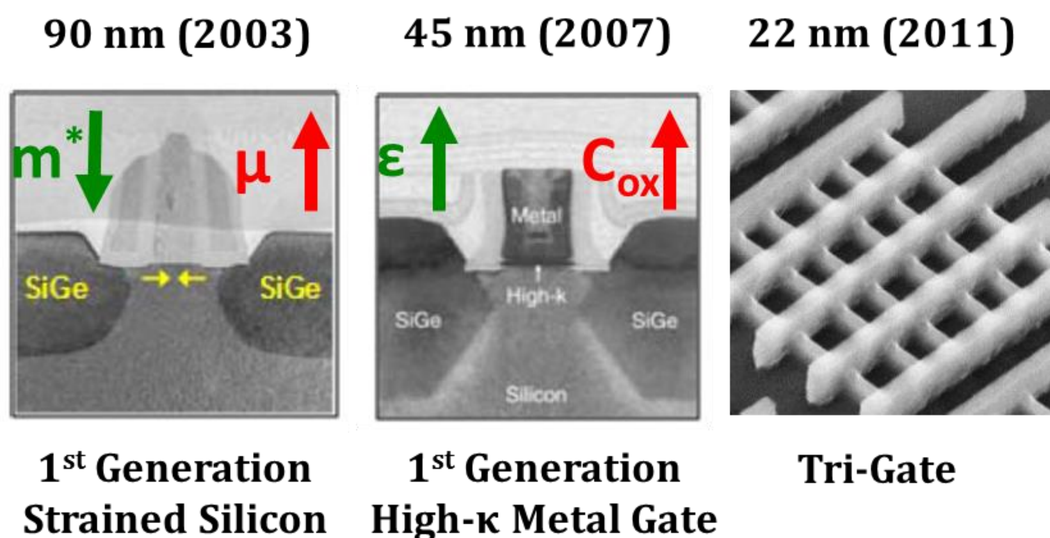


Figure 1.2: Important changes in the Si-based MOSFET [4].

metal-oxide-semiconductor field effect transistors (MOSFETs) has been the primary pathway to increase device density, and computing performance. As shown in Figure 1.2, at the 90 nm technology node, SiGe source/drain was used to introduce compressive train to silicon channel. As a result of this compressive strain, the effective mass of electrons in channel decreased and hence the increase in electron mobility. At 45 nm technology node, high-κ dielectric and metal gate were implemented to further enhance I_{ON} by increasing C_{ox}. Furthermore, at the 22 nm node, a novel Fin Field-Effect-Transistor (FinFET) design was implemented, yielding more gate control and thus less leakage current at lower gate voltages [4]. By implementing FinFET, the leakage current could be suppressed due to better gate control to the device channel. As shown in Figure 1.3, using Tri-gate technology FinFETs could reduce leakage by an order while maintain ON current. However, the leakage current increases if we reduce threshold

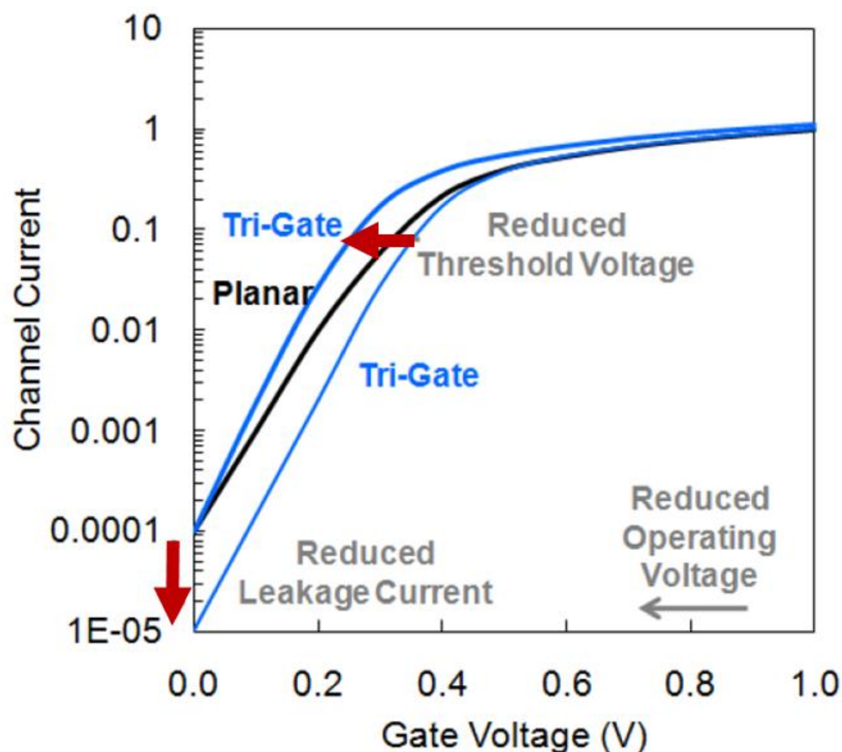


Figure 1.3: Comparison of the transfer characteristics of Tri-gate FinFET and Planar MOSFET [4].

voltage for decreasing supply voltage. Hence, a trade-off is reached between low OFF-currents and low V_{th} which constraint further power reduction.

The trade-off happens due to the fundamental limitation of thermionic emission based devices such as MOSFET and FinFET. For MOSFETs, I_{OFF} exponentially increases with V_{th} reduction and is expressed by following equations [3]:

$$I_{OFF} = I_{ds,V_{th}} e^{-qV_{th}/mkT} = I_{ds,V_{th}} e^{-ln10 \times V_{th}/SS} \quad (1.3)$$

$$I_{ds,V_{th}} = \frac{W}{L} \mu_{eff} C_{ox} (m-1) \left(\frac{kT}{q}\right)^2, m = 1 + \frac{C_{dm}}{C_{ox}} \quad (1.4)$$

where m is a factor greater than one and related to subthreshold slope (SS) and body effect, k is Boltzmann constant and T is temperature. $I_{ds,V_{th}}$ is defined as the drain-to-source current at threshold. The OFF-current is dominated by the ratio between V_{th} and SS. To further reduce in power consumption, V_{th} must be reduced. However, the OFF-current increases exponentially with decreasing V_{th}. To relieve/alleviate the impact of V_{th} reduction, SS must be minimized. Unfortunately, SS of thermionic devices has a lower bound which makes low I_{OFF} hard to achieve under low supply voltage. SS is independent to any voltage operation and can be expressed as follow [3]:

$$SS = \left(\frac{d(logI_{ds})}{dV_{gs}}\right)^{-1} = 2.3\frac{mkT}{q} = 2.3\frac{kT}{q}\left(1 + \frac{C_{dm}}{C_{ox}}\right), \quad (1.5)$$

and is typically 70-100 mV/decade for MOSFETs. The high-κ dielectrics are chosen to remove capacitance related terms making m=1 leading to lower bound $2.3\frac{kT}{q}$ $(60mV/decade)$ at room temperature. This lower bound is a thermal emission related term and independent of any device parameters. In other words, all thermionic emission based devices will suffer under this trade-off between the I_{OFF} and the V_{th}.

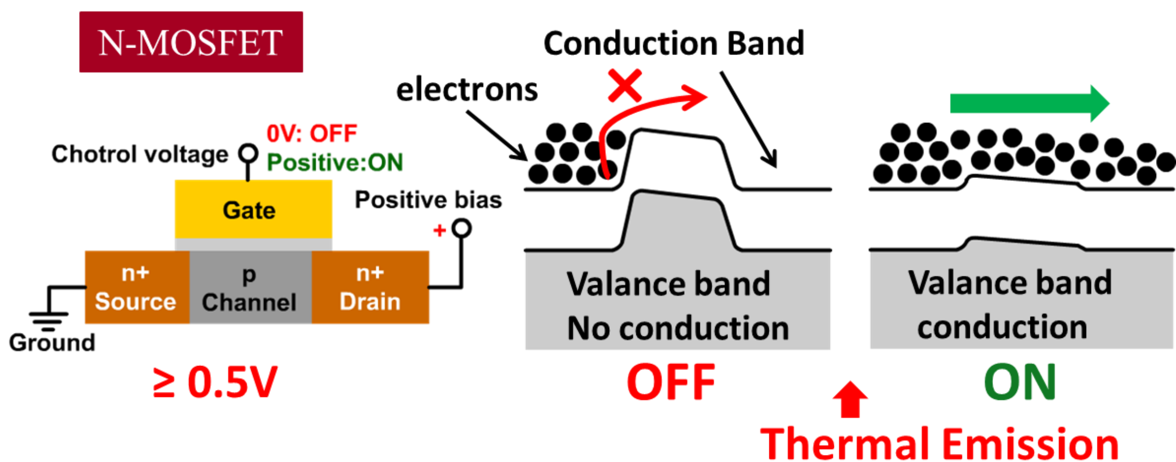
1.3 Fundamentals of Device Operation: MOSFETs and TFETs

To further understand the role of SS on device operation, we focus on the device operation principle of n-MOSFET, shown in Figure 1.4. A MOSFET consists of three terminals: source, channel and drain. Source and drain of a conventional MOSFET are heavily doped with same type of dopants. Therefore, MOSFETs are symmetric devices which could switch polarity by varying the applied voltage (V_{DS} or V_{SD}) without any influence on the device's performance. By applying gate voltage V_{GS}, the barrier height of MOSFET in channel is suppressed and initiates/enables charge conduction. The SS can also be defined as the ratio between the surface potential (ψ_S) and the applied gate voltage (V_{GS}), which is given by [5]:

$$SS = (\frac{d(logI_{ds})}{dV_{gs}})^{-1} = 2.3\frac{kT}{q}\frac{dV_{GS}}{d\psi_S} = 2.3\frac{kT}{q}\left(1 + \frac{C_{dm}}{C_{ox}}\right). \qquad (1.6)$$

The major mechanism for carriers to overcome the barrier is thermal emissions, which cause the lower bound of SS. Hence, thermionic emission based device (i.e., MOSFETs) have theoretical limitation on voltage scaling. Hence, a fundamentally novel device based on new working mechanism must be used in future ultra-low voltage applications.

Figure 1.4: Structure and working principle of a MOSFET.



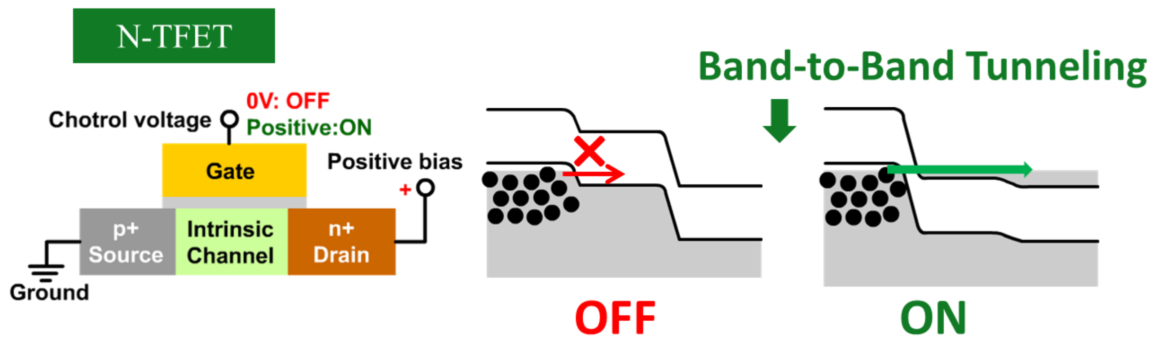


Figure 1.5: Structure and working principle of a TFET.

Recently, Tunnel Field-effect-transistor (TFET) based on inter-band to band tunneling (BTBT) injection are being investigated as a potential candidate to obtain steep SS characteristics, and thereby greatly reducing the static power consumption through low supply voltage device operation [6-15]. The TFET is a p-i-n or n-i-p gated Zener (or Esaki tunnel) diode working as a Boolean (digital) switch. A schematic of an n-type TFET and corresponding band diagrams are shown in Figure 1.5. From the OFF-state band diagram of a TFET, electrons in the source could not tunnel through due to the lack of allowed states within the bandgap

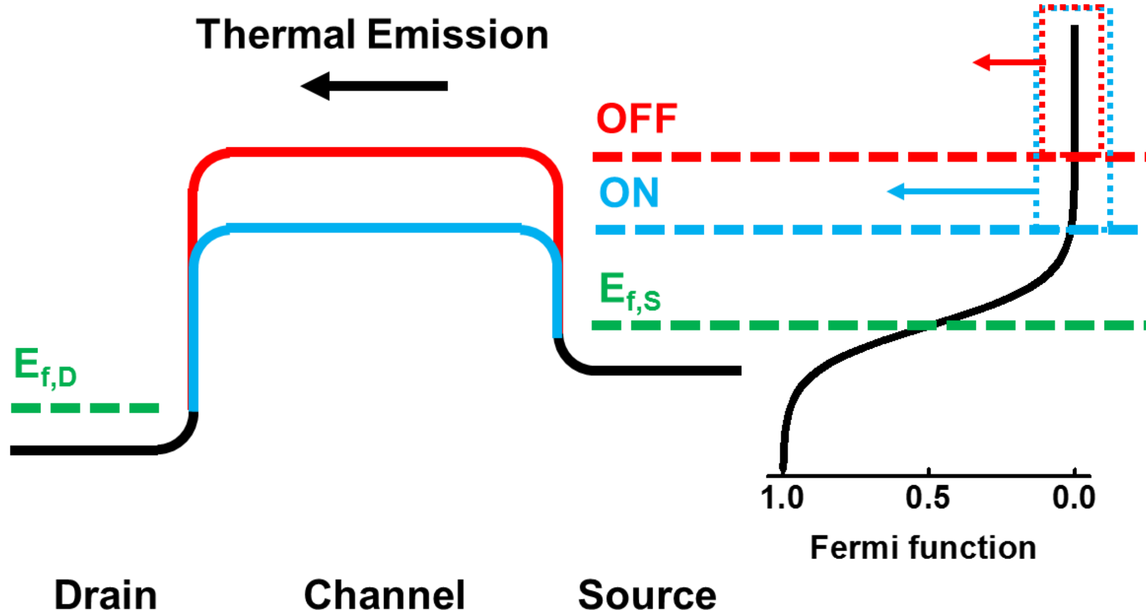


Figure 1.6: Band diagram of an n-type MOSFET and its Fermi-Dirac distribution at ON- and OFF- state.

(forbidden states). On the other hand, for ON-state, positive gate voltage (V_{GS}) lowers down channel potential, and thus, electrons in the valance band of source begin to tunnel through junction to conduction band of channel. Therefore, TFETs do not have a lower bound of SS due to BTBT mechanism instead of thermal emission.

To further understand SS in a TFET, let us focus on the physics of a MOSFET shown in Figure1.6. One can find that only the electrons in high energy band tail participate in the conduction/electron transport in MOSFET. In the energy tail region of the source, the Fermi-Dirac distribution can be approximated to a Maxwell-Boltzmann distribution, which is given by:

$$f(E) = \frac{1}{1+e^{\frac{E-E_f}{kT}}} \xrightarrow{E \gg E_f} e^{-\frac{E-E_f}{kT}} , \quad (1.7)$$

where E_f is Fermi energy level. Thus, SS is proportional to derivative of ON current as a function of applied voltage, which can be expressed as follow [16-17]:

$$I_{DS} \propto f(E), SS = (\frac{\partial \log(I_{DS})}{\partial V_{GS}})^{-1} = \ln(10) \left(\frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial V_{GS}}\right)^{-1} \sim \ln(10) \frac{kT}{q} \quad (1.8)$$

The result reflects that the working principle of a MOSFET is based on thermal emission of high energy carriers. On the other hand, the conduction band of source region in a TFET inhibits tunneling of the carriers in the high energy band tail due to forbidden states in band gap which are depicted in Figure 1.7. In ON-state, the valance band of channel cut-off the lower energy exponential tail. As a result, the junction operates as a band-pass filter allowing the carriers carrying energy around Fermi level to tunnel. In addition, the sharp change of Fermi-Dirac distribution around Fermi level mitigates TFETs from dominance of thermal emission in high or low energy tails. In conclusion, it is theoretically possible that a TFET can exhibit

superior SS than MOSFET by BTBT injection which make an ideal candidate for ultra-low power IoT application.

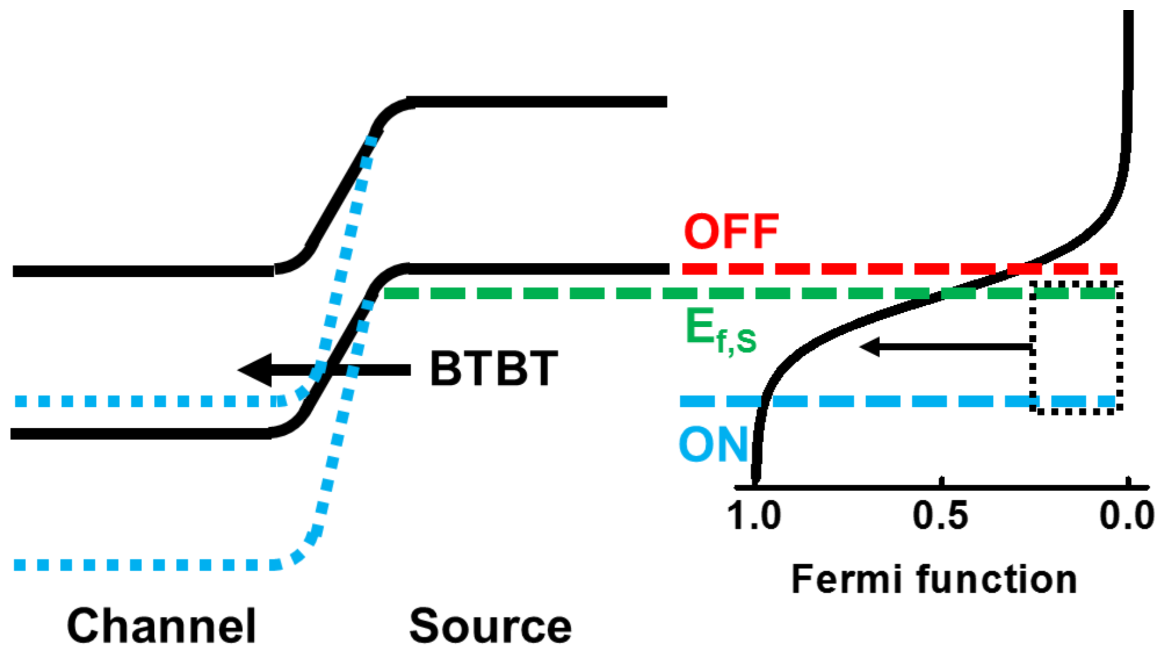


Figure 1.7: Band diagram of n-type TFET and its Fermi-Dirac distribution at ON- and OFF-state.

1.4 Thesis Objective and Organization

The objective of this research is to provide a feasible solution for ultra-low power applications which covers (i) integration and feasibility of possible material systems, (ii) systematic and comprehensive study of electrical and material properties of selected material systems, (iii) evaluation of TFETs' performance, (iv) investigation of ultra-low power TFET based SRAM, and (v) novel logic design using TFETs.

This thesis is organized in to eight chapters. ***Chapter 2*** investigates the criteria and consideration for a TFET design. ***Chapter 3*** presents the heterointerface engineering for mixed As/Sb material systems. ***Chapter 4*** presents the suitability and quality of high κ/GaAsSb system. ***Chapter 5*** presents a comprehensive investigation of bi-axial tensile strained Ge/InGaAs TFETs using TCAD simulation. ***Chapter 6*** presents the simulated performance of

the 7T TFETs based SRAM. ***Chapter 7*** proposes and estimates the performance of TFET based adiabatic logic design. ***Chapter 8*** summarizes the conclusion of the thesis and presents prospects for future research and investigation based upon the results obtained in this work.

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Chapter 2

Critical Criteria for Design of Tunnel Field Effect Transistors

2.1 Tunnel Current and Subthreshold Slope in TFETs

As described in *Chapter 1*, BTBT is the main working mechanism for current conduction in TFETs. Therefore, a detailed examination of tunneling behavior in TFETs is necessary for further design and optimized TFETs. The device current in a standard TFET can be expressed as follows by using the Landauer equation [1-2]:

$$I_{S\rightarrow D} = \frac{2q}{h}\int f_S(E)D_{S,v}(E)T(E)[1-f_D(E)]D_{D,c}(E)v(E)dE, \tag{2.1}$$

$$I_{D\rightarrow S} = \frac{2q}{h}\int f_D(E)D_{D,C}(E)T(E)[1-f_S(E)]D_{S,v}(E)v(E)dE, \tag{2.2}$$

$$I_{tunnel} = I_{S\rightarrow D} - I_{D\rightarrow S} = \frac{2q}{h}\int D_{S,v}(E)D_{D,C}(E)T(E)[f_S(E)-f_D(E)]v(E)dE, \tag{2.3}$$

$$= \frac{2q}{h}\int M(E)T(E)[f_S(E)-f_D(E)]dE, \tag{2.4}$$

where $f_S$and f_D are Fermi-Dirac distribution of source and drain respectively, $D_{S,v}(E)$ is the density of sates in the valance band of source, $D_{D,c}(E)$ is the density of state in the conduction band of drain, the tunneling probability $T(E)$ is assumed to be equal for both direction, $v(E)$ is the group velocity of electrons. $M(E)$ is the number of conduction mode, which is combined with the average velocity and the density of states [2-4], and can be written as [3]:

$$M(E) = g_v D_{S,v}(E)D_{D,C}(E)v(E) \tag{2.5}$$

where g_v is the valley degeneracy. To further simplify and estimate Eq. 2.5 in different dimensionality, we assume ballistic transport and TFETs made with same material. Eq. 2.3 could be reformulated as:

$$I_{tunnel} = \frac{2q}{h}\int g_v D_{nD}(E)\langle v(E)\rangle T(E)[f_S(E) - f_D(E)]dE. \quad (2.6)$$

The average velocity $\langle v(E)\rangle$ in a TFET device can be expressed as:

$$\langle v(E)\rangle = v(E)\langle cos\theta\rangle = v(E)\frac{1}{\pi}\int_{-\frac{\pi}{2}}^{\pi/2} cos\theta d\theta = \frac{2}{\pi}v(E), \quad (2.7)$$

where θ is the angle respect to transport direction. We further assume the parabolic dispersion and the isotropy of electron velocity, given by

$$v(E) = \frac{1}{\hbar}\frac{dE(k)}{dk}\bigg|_{k=k_0} = \frac{\hbar k}{m^*} = (\frac{2(E-E_c)}{m^*})^{1/2}, \quad (2.8)$$

where m^* is effective mass of electron and E_C is the conduction band edge. For different dimensionality of devices, conduction modes are given by [3]:

$$M_{nD}(E) = \frac{h}{4}g_v\langle v(E)\rangle D_{nD}(E) = \begin{cases} M_{1D}(E) = \frac{h}{4}g_v(\frac{2(E-E_c)}{m^*})^{1/2} \times (\frac{2m^*}{(E-E_c)})^{1/2} \\ M_{2D}(E) = \frac{h}{4}g_v(\frac{2(E-E_c)}{m^*})^{1/2} \times \frac{2m^*}{\pi\hbar^2} \\ M_{3D}(E) = \frac{h}{4}g_v(\frac{2(E-E_c)}{m^*})^{1/2} \times \frac{m^*\sqrt{2m^*(E-E_C)}}{\pi\hbar^2} \end{cases}.$$

TFET current can be described as a single integral in general form [5]:

$$I_{nD} = \frac{2q}{h}\int\big(f_S(E) - f_D(E)\big)T(E)[2\pi mE/h^2]^{(n-1)/2}, \quad (2.9)$$

where n=1,2,3, according to the dimensionality of devices.

From Eq. 2.4, we understand the tunnel current in TFETs consists of three major parts: (i) Fermi distribution difference, (ii) tunneling probability, and (iii) density of energy states. Next step is to derive the subthreshold slope from aforementioned current equations. By introducing

joint density of states $D_J(E)$ to Eq. 2.3 which is product of density of states on source and drain sides, we can reformulate the tunneling current as follows [6]:

$$I_{tunnel} \propto \frac{2q}{h} \int D_J(E)T(E)[f_S(E) - f_D(E)]dE. \quad (2.10)$$

This could be depicted in Figure 2.1.

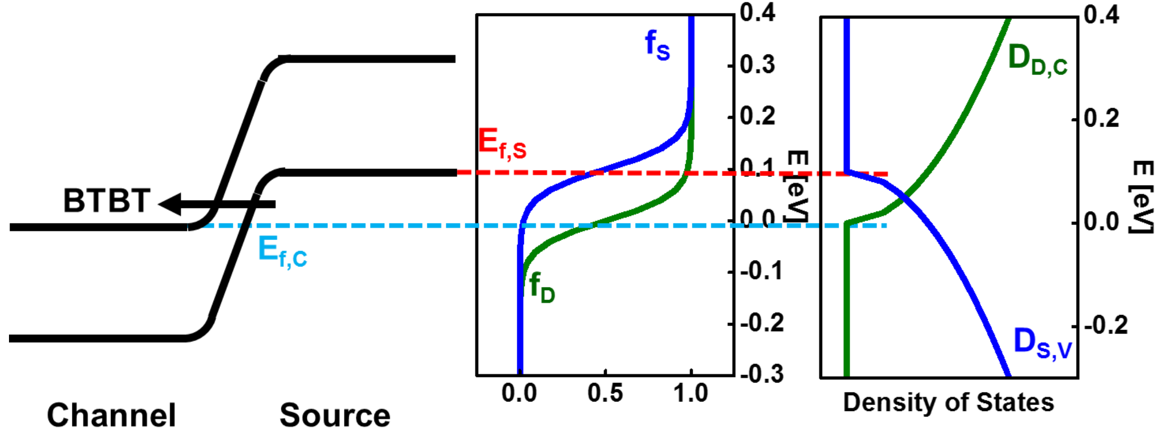

Figure 2.1: Schematic representation of BTBT tunneling in a P/N junction include Fermi distribution and density of states.

We manipulate and divide by the integral of the Fermi distribution to Eq.2.10 [6]:

$$I_{tunnel} \propto \int (f_C - f_V)dE \times \frac{\int (f_c - f_v)TD_J dE}{\int (f_c - f_v)dE}$$

$$= qV \times \langle T(E)D_J(E) \rangle \quad (2.11)$$

Integration of the differences of two Fermi distribution can be approximated to a constant number if we consider only small voltage across a junction. In small bias regime, the difference of Fermi level between channel and source leaves the tunneling window relatively small. In other words, any arbitrary energy level within tunneling window has to be close to E_{fC} of channel and E_{fV} of source. Consequently, we can apply Taylor expansion on the integral [7]:

$$f_C - f_V = \frac{1}{e^{(E-E_{fc})/k_B T}} - \frac{1}{e^{(E-E_{fv})/k_B T}} \approx \frac{E_{fc}-E_{fv}}{4k_B T} = \frac{qV_{apl}}{4k_B T}, \quad (2.12)$$

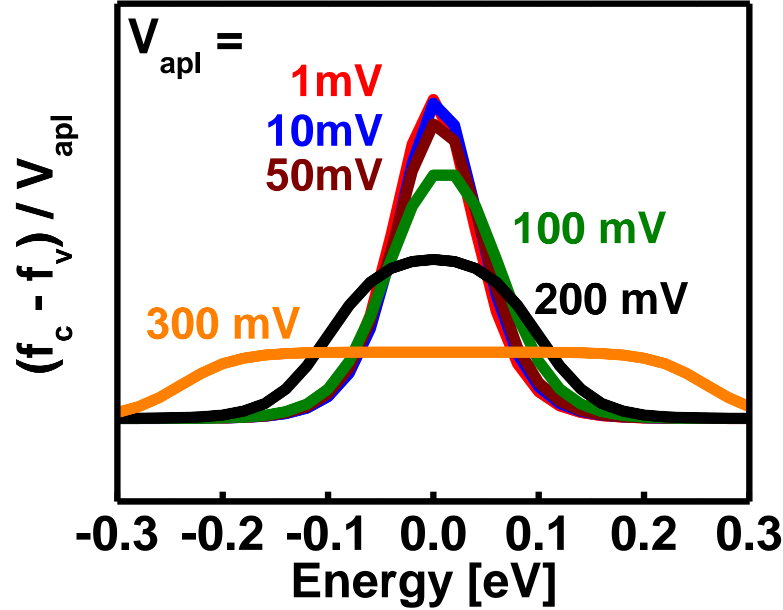

Figure 2.2: $(f_c - f_v)/ V_{apl}$ is plotted to illustrate the influences of applied voltage on Fermi distribution.

where E_f are Fermi levels and V_{apl} is applied voltage across junction. Figures 2.2 shows the $(f_c - f_v)/ V_{apl}$ as a function of energy. The areas under the curves at low applied voltage are the same which implies integrals of $f_c – f_v$ are proportional to the applied voltage. In Eq. 2.11, the second term becomes a weighted average of tunnel probabilities and density of states. We can remove the effect from Fermi distribution by dividing current with apply voltage. Therefore, the steepness of tunneling joint density of states in mV/decade is given by

$$S_{T\times D} \equiv [\frac{d\log\langle T(E)D_J(E)\rangle}{dV}]^{-1} \approx (\frac{d\log(I/V)}{dV})^{-1}. \tag{2.13}$$

This semilog conductance swing voltage could give a fairly comparable metric for prediction of SS in TFETs without any effect from the gate insulator/semiconductor interface [6,8-10]. We can break down the two effects independently by approximating $\langle T(E)D_J(E)\rangle \approx \langle T(E)\rangle\langle D_J(E)\rangle$ [11]. Thus, the conductance swing is given by the sum of two separate steepness terms in mV/decade:

$$S_{T\times D} = \left[\frac{dlog\langle T(E)D_J(E)\rangle}{dV}\right]^{-1} = \left[\frac{d(log\langle T(E)\rangle + log\langle D_J(E)\rangle)}{dV}\right]^{-1} = \left[\frac{1}{S_T} + \frac{1}{S_{DOS}}\right]^{-1}. \quad (2.14)$$

Eq. 2.14 could be applied on any tunneling junction (or two terminal devices). S_T is the steepness causing by tunneling. S_{DOS} is the joint density of states which is affected by band-tail inside bandgap. In high current density of states cases, $\langle T\rangle \sim 1$, it diminishes tunneling term and leads to S_{DOS} dominating the conductance swing. To compare these values with SS in TFETs, we insert Eq. 2.11 into Eq. 1.5, SS can be reformulated to

$$SS^{-1} \equiv \frac{dlog(I_D)}{dV_G} \sim \frac{d}{dV_{apl}}\frac{dV_{apl}}{dV_G}\log\left(V_{apl} \times \langle T(E)D_J(E)\rangle\right)$$

$$= \left(\frac{C_{ox}}{C_{ox}+C_{dm}+C_{it}}\right)\frac{d}{dV_{apl}}\log\left(V_{apl} \times \langle T(E)D_J(E)\rangle\right)$$

$$= \left(\frac{C_{ox}}{C_{ox}+C_{dm}+C_{it}}\right)\frac{d}{dV_{apl}}\left(logV_{apl} + log\langle T(E)D_J(E)\rangle\right)$$

$$= \left(\frac{C_{ox}}{C_{ox}+C_{dm}+C_{it}}\right)\left(\frac{1}{V_{apl}} + \frac{d}{dV_{apl}}log\langle T(E)D_J(E)\rangle\right)$$

$$= \left(\frac{C_{ox}}{C_{ox}+C_{dm}+C_{it}}\right)\left(\frac{1}{V_{apl}} + \frac{1}{S_{\langle T\times D_J\rangle}}\right)$$

$$\sim \left(\frac{C_{ox}}{C_{ox}+C_{dm}+C_{it}}\right)\left(\frac{1}{V_{apl}} + \frac{1}{S_T} + \frac{1}{S_{DOS}}\right).$$

Thus,

$$SS \sim \left(1 + \frac{C_{dm}+C_{it}}{C_{ox}}\right)\left(\frac{1}{V_{apl}} + \frac{1}{S_T} + \frac{1}{S_{DOS}}\right)^{-1}. \quad (2.15)$$

There are three important components in Eq. 2.15: (i) oxide capacitance, (ii) tunneling probability, and (iii) joint density of states. These factors not only determine SS but also the maximum current in TFETs. Therefore, for all subsequent sections in this chapter, we will discuss the criteria for these three components accordingly.

2.2 Criteria I: Tunneling Probability (WKB Approach)

The basic approach to estimate tunneling probability of BTBT is using WKB (Wentzel-Kramers-Brillouin) approximation. Let us begin with Schrödinger's equation with an arbitrary shape barrier V(x):

$$-\frac{\hbar^2}{2m}\frac{\partial^2\psi(x)}{\partial x}+V(x)\psi=E\psi. \tag{2.16}$$

In the case of tunneling, the barrier potential should be higher than the energy of particle. We can rewrite Eq. 2.16 as follows:

$$\frac{\partial^2\psi(x)}{\partial x}=k'(x)^2\psi(x),\ k'(x)=\sqrt{\frac{2m(V(x)-E)}{\hbar^2}}. \tag{2.17}$$

In general, the wave function is a complex function so that we can write it in a polar form as

$$\psi(x)=A(x)e^{i\phi(x)}, \tag{2.18}$$

where A(x) is amplitude and ϕ(x) is the phase. Inserting Eq. 2.18 into Eq. 2.17, we get

$$\frac{\partial^2 A}{\partial x^2}+2i\frac{\partial A}{\partial x}\frac{\partial\phi}{\partial x}+iA\frac{\partial^2\phi}{\partial x^2}-A\left(\frac{\partial\phi}{\partial x}\right)^2=k'^2A. \tag{2.19}$$

We can get two differential equations by separating the real and imaginary parts:

$$\begin{cases}Real: & \frac{\partial^2 A}{\partial x^2}-A\left(\frac{\partial\phi}{\partial x}\right)^2=k'^2A\\ Imaginary: & 2i\frac{\partial A}{\partial x}\frac{\partial\phi}{\partial x}+iA\frac{\partial^2\phi}{\partial x^2}=0\end{cases}. \tag{2.20}$$

The imaginary part of equation is equivalent to

$$\frac{\partial}{\partial x}\left(A^2\frac{\partial\phi}{\partial x}\right)=0 \tag{2.21}$$

Thus, the solution of Eq. 2.21 can be expressed as

$$A=\frac{C}{\sqrt{\left|\frac{\partial\phi}{\partial x}\right|}}, \tag{2.22}$$

where C is a real constant. Due to equations depend on arbitrary potential V(x), the real part of Eq. 2.20 could not be solved analytically without further assumptions. Therefore, we assume the envelope of wave function varies slowly with position and thus, $\frac{A''}{A}\sim 0$. Eq. 2.20 can be reformulated to

$$\left(\frac{\partial\phi}{\partial x}\right)^2=-k'^2,\phi(x)=\pm i\int|k'(x)|dx,$$

$$\psi(x)=\frac{C}{\sqrt{k\prime(x)}}e^{\pm i\int|k'(x)|dxt}. \tag{2.23}$$

By applying this solution to the rectangular barrier case [12], we can get the tunneling probability T as

$$T \sim \exp\left[-2\int_{x_L}^{x_R} |k'(x)|dx\right], \quad (2.24)$$

where x_R and x_L are the classical turning points (or boundaries). We next proceed to calculate the tunneling probability in a P/N junction shown in Figure 2.3. The tunneling barrier in P/N junction can

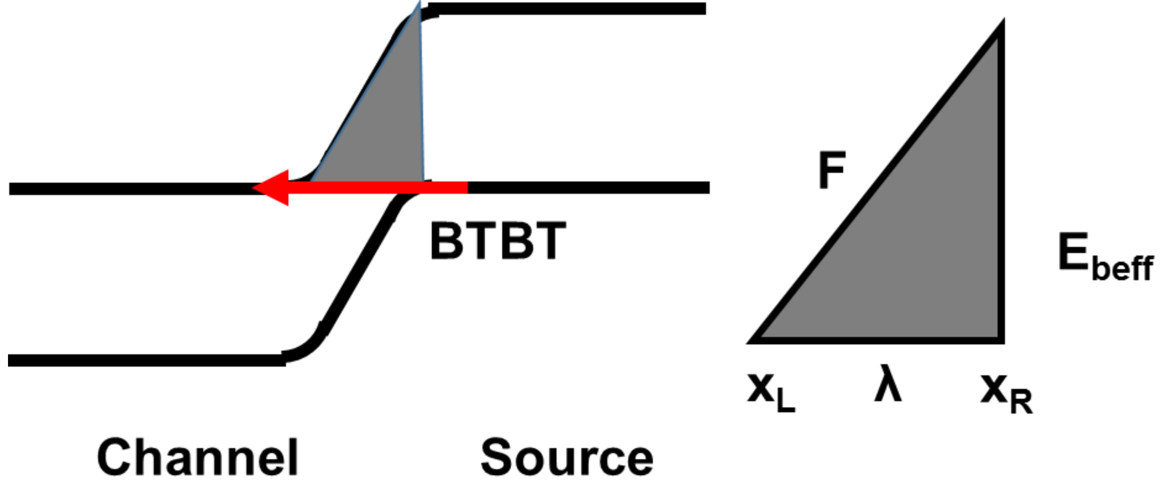

Figure 2.3: Tunneling in a P/N junction.

be treated as a triangular shape barrier. Its height is the effective barrier (E_{beff}), base is the tunneling distance (λ), and slope is the electric field (F). Barrier potential, V(x), becomes

$$V(x) = qF(x - x_L) + E_C, \quad (2.25)$$

where F is constant electric field. If we assume the carrier locates at the conduction band edge, by inserting Eq. 2.25 into Eq. 2.17, we can get the imaginary part of wave vector inside barriers and can be expressed as:

$$k'(x) = \sqrt{\frac{2m((qF(x-x_L)+E_C)-E_C)}{\hbar^2}} = \sqrt{\frac{2m(qF(x-x_L))}{\hbar^2}}. \quad (2.26)$$

Substituting Eq. 2.26 to Eq. 2.24 yields

$$T \sim \exp\left[-2\int_{x_L}^{x_R}\left(\frac{2m(qF(x-x_L))}{\hbar^2}\right)^{\frac{1}{2}}dx\right] = \exp\left[-\frac{2\sqrt{2m}}{\hbar}\int_{x_L}^{x_R}(qF(x-x_L))^{\frac{1}{2}}dx\right]$$

$$= \exp\left[-\frac{4\sqrt{2m}}{3\hbar qF}(qF(x_R-x_L))^{3/2}\right] = \exp\left[-\frac{4\sqrt{2m^*}E_{beff}{}^{3/2}}{3q\hbar F}\right]. \quad (2.27)$$

From the result, it is clear that to acquire higher tunneling current, we should have smaller effective mass and effective barrier, and stronger electric field. In addition, by using different materials into device structure, we can have three types of band alignment which affect E_{beff}: (i) Homojunction, (ii) Staggered-Gap, and (iii) Broken Gap, shown in Figure 2.4. Due to non-constant electric field in real applications, tunneling distance (λ) is a more fitting parameter to estimate the tunneling probability. We can convert the relationship between λ, F, and E_{beff} easily by using the triangle in Figure 2.3. In a homojunction system, E_{beff} is equal to materials bandgap (E_g) and tunneling distance is trivial to obtain from aforementioned relationship. If channel and source of TFETs are different materials and forming

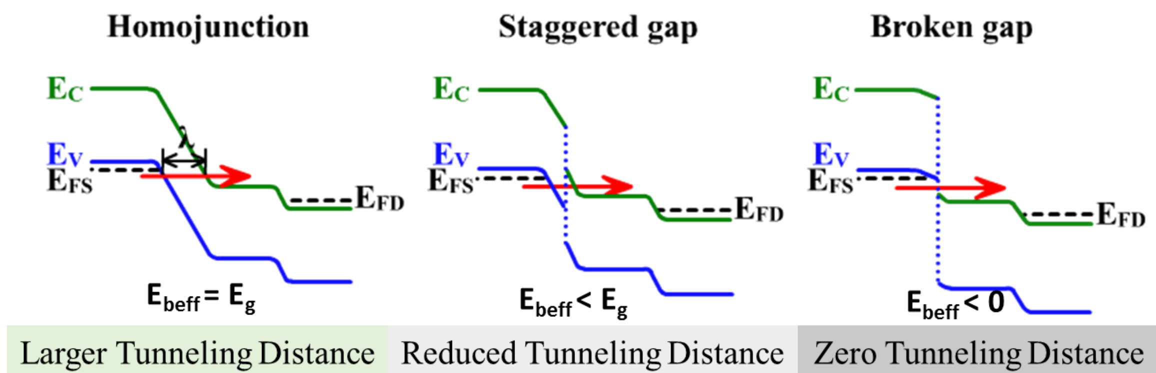

Figure 2.4: Different band alignments for tunnel junction.

staggered gap, E_{beff} becomes the band offset in the system. Thus, both E_{beff} and λ are reduced compared to the homojunction system. In the extreme case, for a broken gap system, E_{beff} is diminished to zero and nullifies λ. This system can thus provide highest tunneling current for TFETs due to absence of tunneling barrier. Therefore, heterojunction TFETs (H-TFETs) are being extensively investigated

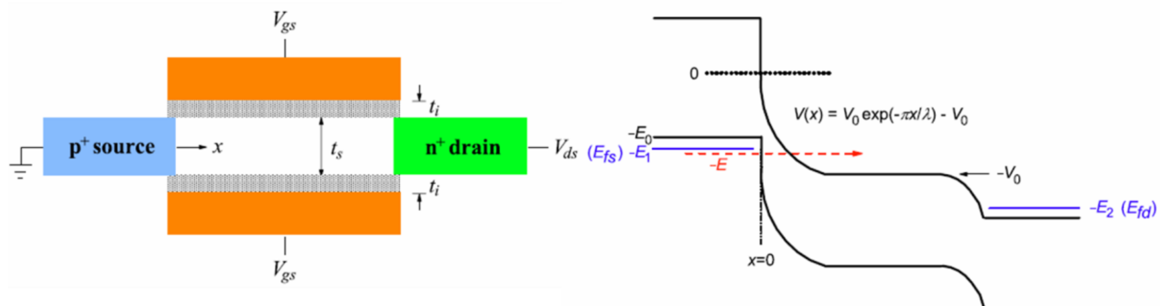

Figure 2.5: Schematic of DG H-TFET and corresponding band diagram biased in saturation. [13]

recently.

To leverage the benefit of heterojunction material system, further understanding of tunneling probability in H-TFET is necessary. Yuan Taur and his group have developed a series of models to investigate analytical solution for DG H-TFETs [5, 13-17]. For a DG H-TFET delineate in Figure 2.5, the barrier can be describe as an exponential barrier with band offset which is illustrated in Figure 2.5 and can takes the form

$$V(x) = V_0 \exp\left(-\frac{\pi x}{\lambda}\right) - V_0,\ \lambda = t_s + 2\frac{\epsilon_s}{\epsilon_i} t_i, \tag{2.28}$$

where V_o is mainly controlled by gate voltage and λ is scale length which is determined by body thickness (t_s), insulator thickness (t_i), channel material's permittivity (ε_s), and insulator's permittivity (ε_i) [13, 18-20]. According to Eq. 2.24, the WKB integral is given by [13]:

$$\begin{aligned} T(E) &= exp\left\{-\frac{2\sqrt{2m}}{\hbar}\int_0^d \sqrt{V(x)-(-E)}dx\right\} \\ &= exp\left\{-\frac{2\sqrt{2m}}{\hbar}\int_0^d \sqrt{V_0 \exp\left(-\frac{\pi x}{\lambda}\right) - V_0 + E dx}\right\} \\ &= exp\left\{-\frac{4\lambda\sqrt{2m}}{\pi\hbar}\left[\sqrt{E} - \sqrt{V_0 - E}\sin^{-1}\sqrt{E/V_0}\right]\right\}. \end{aligned} \tag{2.29}$$

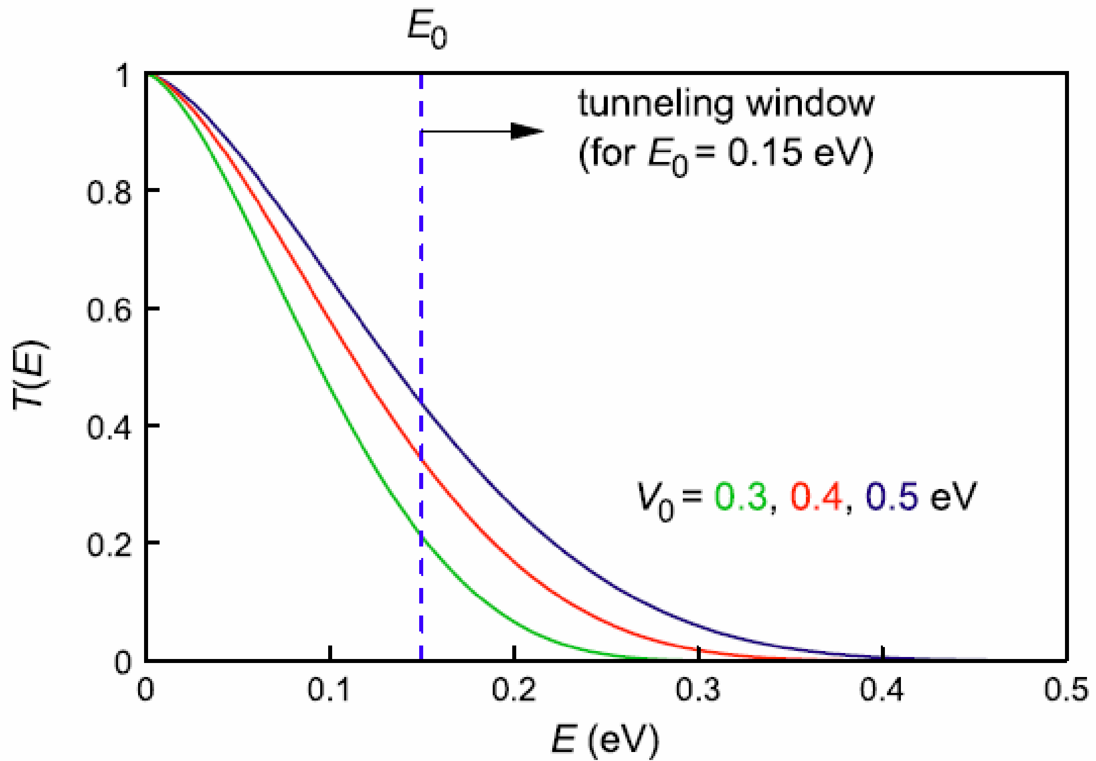

Figure 2.6: Tunneling probability with tunneling window $E_0 < E < V_0$. [13]

where V(d)+E=0 and $V_0 = E_0 + qV_{ds}$. Figure 2.6 shows T(E) as function of carrier energy with tunneling window ($E_0 < E < V_0$). It is clear that lowering the band offset (E_0) could significantly enhance tunneling probability. Therefore, to obtain maximum area underneath curves, heterojunction TFETs are preferable, especially near-broken or broken gap systems.

2.3 Criteria I: Tunneling Probabilities (Numerical Approach)

In the previous section, we investigated tunneling probability using an analytical approach. In reality, modern VLSI devices have complexity in structure. Hence, the solution we acquired from section 2.3 could deviate from real circumstance. There are two ways to estimate the tunneling current in using numerical simulation: the semi-classical and the full quantum approach. In this work, all simulations have been performed by a semi-classical simulator primarily due to the good balance between simulation complexity and accuracy of results. We have modeled BTBT by adding an additional tunneling generation term in the drift-diffusion equation at each mesh point. Therefore, the current behavior of each device is the numerical summation of the contributions from all mesh points in the simulated device's structure. There are two types of BTBT models in the numerical semi-classical simulator: local tunneling and non-local tunneling.

Kane's model:

E. O. Kane developed the first complete tunneling model for direct and indirect BTBT in 1959 [21-22]. For local tunneling model, the tunneling formalism is solved in k-space (momentum space). In other words, it implies that electron-hole pairs are generated at the same location and in a constant electric field. Since no generation (G) or recombination (R) term is included in the G-R rate model, the current is only affected by the tunneling probability. We begin with Landauer's equation [23], which estimates the current density:

$$J = \frac{e}{4\pi^3 \hbar} \int_{-\infty}^{\infty} \int T(E, \vec{k}_\perp)[f_v - f_c] d\vec{k}_\perp \, dE, \qquad (2.30)$$

where $\vec{k}_{\perp}$ is transverse wave-vector which is perpendicular to the channel direction. To simplify Eq. 2.30, we set $f_v - f_c$ is equal to 1. In addition, generation rate could be determined from continuity equation by

$$\begin{cases} \frac{dJ}{dx} = eG_T \\ dE = e|F|dx \end{cases} \Rightarrow G_T(E) = |F|\frac{dJ(E)}{dE}. \quad (2.31)$$

We proceed to substitute Eq. 2.30 into Eq. 2.31 and remove vector $\vec{k}_{\perp}$ by applying polar coordinate in integrating Eq.2.30:

$$G_T(E) = \frac{e}{4\pi^3\hbar}2\pi\int_0^{\infty} T(E, k_{\perp}) \times k_{\perp}dk_{\perp}. \quad (2.32)$$

The tunneling probability can be expressed by using WKB approximation [21]:

$$T(E, k_{\perp}) = \frac{\pi^2}{9}exp\left(-2\int_{x_L}^{x_R} Im(k_x)dx\right). \quad (2.33)$$

Next step, we employ the Kane's two-band E-k dispersion relation for energy in the bandgap [21-22]:

$$E^{gap}(\kappa) = \frac{E_G}{2} - \frac{\hbar^2\kappa^2}{2m_0} \pm \frac{1}{2}\sqrt{E_G^2 - \frac{E_G\hbar^2\kappa^2}{m_r}}, \quad (2.34)$$

where m_0 is the electron mass and m_r is the reduce mass. For tunneling, due to carrier energy being smaller than barrier potential, k_x should be imaginary ($k_x^2 = -Im(k_x)^2$), and thus, $\kappa^2 = -k^2 == -Im(k_x)^2 - k_{\perp}^2$. To further estimate the value of the integral in constant field F, we set the tunneling region start from x_L=0 (E=0) to x_R=eE_G/F, and the electric potential set as $E^{gap} = e|F|x$. If we neglect the kinetic energy term in Eq. 2.34, and the imaginary part of k_x inside the bandgap is given by:

$$Im(k_x) = \sqrt{\frac{m_r}{E_G\hbar^2}} \times \sqrt{E_G^2 + E_G\frac{\hbar^2k_{\perp}^2}{m_r} - 4\left(e|F|x - \frac{E_G}{2}\right)^2},$$

$$T(k_{\perp}) = \frac{\pi^2}{9}exp\left(-\pi\frac{\sqrt{m_r}E_G^{1.5}}{2}\right)exp\left(-\frac{\pi\hbar k_{\perp}^2}{2e|F|}\sqrt{\frac{E_G}{m_r}}\right). \quad (2.35)$$

By substituting Eq. 2.35 in Eq.2.32, we can get the result for direct BTBT [21]:

$$G_{T,direct} = \frac{F^2 {m_r}^{0.5}}{18\pi\hbar^2 E_G^{0.5}} exp\left\{\frac{-\pi m_r^{0.5} E_G^{1.5}}{2\hbar|F|}\right\}. \quad (2.36)$$

For indirect BTBT, this is given by

$$G_{T,indirect} = \frac{F^{2.5} {m_r}^{0.5}}{18\pi\hbar^2 E_G^{0.5}} exp\left\{\frac{-\pi m_r^{0.5} E_G^{1.5}}{2\hbar|F|}\right\}. \quad (2.37)$$

In a TCAD simulation tool, the equation can be simplified to the empirical fitting form:

$$G_T = AF^{\alpha} \exp\left(-\frac{B}{|F|}\right), \quad (2.38)$$

where α is 2 for direct tunneling and 2.5 for indirect tunneling. A and B are material dependent parameters. Due to momentum conservation, it is necessary to have phonons provide additional momentum. Thus, the absorption of phonon becomes a three particle process and tunneling probability/current is dramatically reduced for indirect BTBT tunneling. Therefore, direct bandgap tunneling material systems are more suitable for BTBT operation.

Dynamic Non-local BTBT Model:

The local tunneling model we discussed previously is only valid in a constant electric field in tunneling path. Therefore, it tends to overestimate BTBT probability of the sharp junction in modern VLSI devices. Furthermore, BTBT behavior may not be precisely described by local model due to its position-independent nature, which implies that the electron-hole pairs are always generated at the same location. Dynamic non-local BTBT model was developed based on Kane's model and non-local path finding. It can give us an accurate and precise model based on the nature of device structure.

In TCAD [24], the tunneling path is determined dynamically based on the energy band profile rather than predefined by non-local mesh or manual assignment. The simulator dynamically searches the tunneling path, which starts from the valance band in the model-active region. The tunneling path is a straight line with its direction opposite to the gradient of the valence band at the starting position and ending at the conduction band without energy difference compared

to the start point. The tunneling energy is equal to the valance band energy at the starting position and the conduction energy plus band offset at the ending position. After using dynamic tunneling path finding, Kane's model in Eq. 2.38 has to be revised to include spatial dependence.

To begin, let's revise Kane's two-band dispersion relation [21-22, 24] in eq. 2.34:

$$\kappa = \frac{1}{\hbar}\sqrt{m_r E_{G,eff}(1-\alpha^2(x))},$$

$$\alpha(x) = -\frac{m_0}{2m_r} + 2\sqrt{\frac{m_0}{2m_r}\left(\frac{E-E_V(x)}{E_{G,eff}}\right) + \frac{m_0^2}{16m_r^2} + \frac{1}{4}}, \quad (2.39)$$

where, $E_{G,eff}$ equals to effective bandgap including the band offset. We further assume $\frac{k_\perp}{\kappa}$ is small which implies large k_x in tunneling direction. Thus, $Im(k_x) = \sqrt{\kappa^2 + k_\perp^2} \sim \kappa + \frac{k_\perp^2}{2\kappa}$ and tunneling probability is given by:

$$T = \frac{\pi^2}{9} exp\left(-2\int_{x_t}^{x_f} \kappa dx\right) exp\left(-k_\perp^2 \int_{x_t}^{x_f} \frac{dx}{\kappa}\right), \quad (2.40)$$

where $x_i = 0, and\ x_f = l$, for a given tunneling path, l. Inserting the results into Eq. 2.33, we have the direct BTBT generation rate [22-24]:

$$G_T(E) = |\nabla E_V(0)| C_d exp\left(-2\int_0^l \kappa dx\right)[f_c(l) - f_v(0)], \quad (2.41)$$

$$C_d = \frac{g\pi}{36\hbar}\left(\int_0^l \frac{dx}{\kappa}\right)^{-1}\left[1 - exp\left(-k_m^2 \int_0^l \frac{dx}{\kappa}\right)\right], \quad (2.42)$$

where g is the degeneracy factor and k_m is the maximum transverse momentum, determined by the maximum valance-band energy ε_{max} and the minimum conduction-band energy ε_{min} :

$$k_m^2 = min(k_{vm}^2, k_{cm}^2) = min\left(\frac{2m_V(\varepsilon_{max}-E)}{\hbar^2}, \frac{2m_C(E-\varepsilon_{min})}{\hbar^2}\right). \quad (2.43)$$

The indirect BTBT generation rate can be written as [22-24]:

$$G_T(E) = |\nabla E_V(0)| C_p exp\left(-2\int_0^{x_0} \kappa_V dx - 2\int_{x_0}^l \kappa_C dx\right)[f_c(l) - f_v(0)] \quad (2.44)$$

$$C_p = \int_0^l \frac{g(1+2N_{op})D_{op}^2}{2^6\pi^2\rho\varepsilon_{op}E_{G,eff}}\sqrt{\frac{m_V m_C}{\hbar l\sqrt{2m_r E_{G,eff}}}}dx\left(\int_0^{x_0}\frac{dx}{\kappa_V}\right)^{-1}\left(\int_{x_0}^l \frac{dx}{\kappa_C}\right)^{-1} \times \cdots$$

$$\cdots \times \left[1 - exp\left(-k_{vm}^2 \int_0^{x_0} \frac{dx}{\kappa_V}\right)\right]\left[1 - exp\left(-k_{cm}^2 \int_{x_0}^{l} \frac{dx}{\kappa_C}\right)\right] \quad (2.45)$$

where $D_{op}, \varepsilon_{op}, and\ N_{op} = \left[\exp\left(\frac{\varepsilon_{op}}{KT}\right) - 1\right]^{-1}$ are the deformation potential, energy, and number of optical phonons, respectively, ρ is the mass density, and κ_C, κ_V are the magnitude of the imaginary wavevectors from Keldysh dispersion relation:

$$\kappa_V = \frac{1}{\hbar}\sqrt{2m_V|E - E_V(x)|}\Theta\big(E - E_V(x)\big) \quad (2.46)$$

$$\kappa_C = \frac{1}{\hbar}\sqrt{2m_C|E_C(x) + \Delta_C - E|}\Theta(E_C(x) + \Delta_C - E) \quad (2.47)$$

and x_0 is the location where $\kappa_C = \kappa_V$.

This result is similar to Eq. 2.38, hence we can use an empirical fitting form [24]:

$$G_T = A(\frac{F}{F_0})^P \exp\left(-\frac{B}{F}\right), \quad (2.48)$$

where F_0 = 1V/cm, P = 2 for the direct tunneling process, and P = 2.5 for the phonon-assisted tunneling process. A and B are the prefactors which can be expressed as follows for the direct tunneling [24]:

$$\begin{cases} A = \frac{g\pi m_r^{0.5}(qF_0)^2}{9h^2 E_{G,eff}{}^{0.5}} \\ B = \frac{\pi^2 m_r^{0.5}\left(E_{G,eff}\right)^2}{qh} \end{cases}. \quad (2.49)$$

For the phonon-assisted tunneling process, A and B can be expressed as [24]:

$$\begin{cases} A = \frac{g(m_C m_V)^{1.5}\left(1+2N_{op}\right)D_{op}^2(qF_0)^{2.5}}{2^{21/4}h^{5/2}m_r^{5/4}\rho\varepsilon_{op}E_{g,eff}^{7/4}} \\ B = \frac{2^{7/2}\pi m_r^{1/2}\left(E_{G,eff}\right)^{3/2}}{3qh} \end{cases}. \quad (2.50)$$

Table 2.1 list the values of A, and B parameters for common materials. We can find that direct bandgap materials have higher prefactors. It reflects the nature of indirect tunneling process involving three particles and resulting in a dramatically reduced tunneling probability and hence, the lower tunneling current. Therefore, direct bandgap III-V semiconductors or other direct bandgap materials are more suitable for TFETs in order to achieve higher tunneling

Materials	A [$cm^{-3}s^{-1}$]	B [Vcm^{-1}]	P
Si	4×10^{14}	1.9×10^{7}	2.5
Ge	9.1×10^{16}	4.9×10^{7}	2.5
GaAs	2.7×10^{20}	1.2×10^{7}	2

Table 2.1: Parameters for Kane's tunnel model.

probability and tunneling current.

2.4. Criteria II: Junction Abruptness and Band Tail in Bandgap

From Eq. 2.15, the joint density of states has a strong influence on the SS. The density of states for both valence band (D_v) and conduction band (D_v) could be expressed as follow [25]:

$$\begin{cases} D_c = g\frac{\sqrt{2}}{\pi^2}\frac{m_{d,e}^{3/2}}{\hbar^3}(E-E_c)^{1/2} \\ D_v = g\frac{\sqrt{2}}{\pi^2}\frac{m_{d,h}^{3/2}}{\hbar^3}(E_v-E)^{1/2} \end{cases}, \quad (2.51)$$

where g is the number of minimum energy valleys, $m_{d,e}$ is electron effective density-of-states mass, $m_{d,h}$ is hole effective density-of-states mass, E_c and E_v are the band edge of conduction and valance respectively. In Figure 2.7, density of states in a P/N junction are illustrated in linear and semilog plots. D_v and D_c both show null states in band gap and provide an abrupt edge which terminates at the band edge. Therefore, the tunneling current is sharply enabled after the conduction and valance bands overlap. However, in reality, there is a band tail exponentially decaying into the band gap due to the following reasons: (i) heavy doping on source side, (ii) geometrical disorder, and (iii) interface defects.

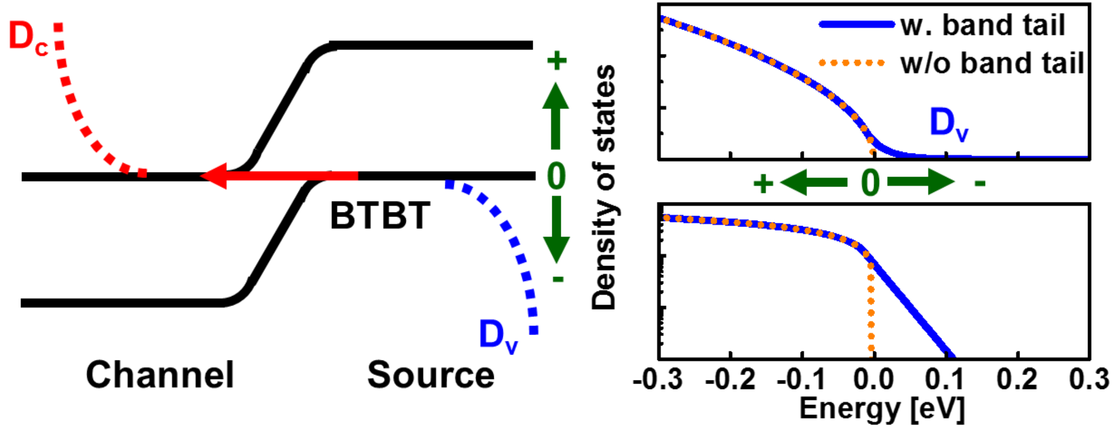

Figure 2.7: **(a)** The density of states in BTBT. **(b)** The linear and semilog plot for density of states as function of energy with and without band tail.

The high doping concentration for BTBT in TFETs may cause significant increase of band tail due to several reasons [26]. First, the spatial overlap of impurity levels merge and smear the boundary of conduction and valance bands, especially for high doping concentrations. Second, the localized strain from impurities might also spatially fluctuate the band gap leading to perturbation of conduction and valance band edges. Third, the Coulomb interaction between carriers and impurities also changes the local conduction and valance band energy. On the other hand, the degree of abruptness of heterointerface also affects the band tail states. The geometrical disorder which is unintentionally introduced during semiconductor material growth in a heterojunction lumps the locally disturbed band energies together, creating an additional band tail states. Finally, interface defects not only change the band alignment at the heterointerface but also introduce band tail states in the bandgap. Overall, we could use the Urbach band tail to model the exponential decay of band tail states [6, 11, 26-28] shown as follow:

$$D_C(E) = \begin{cases} g_C \frac{\sqrt{2}}{\pi^2} \frac{m_{d,e}^{3/2}}{\hbar^3} (E - E_C)^{1/2}, E \geq E_C \\ D_{C0} \times e^{-(E_C - E)/qV_0}, E < E_C \end{cases} \tag{2.52}$$

$$D_V(E) = \begin{cases} g_v \frac{\sqrt{2}}{\pi^2} \frac{m_{d,h}^{3/2}}{\hbar^3} (E_V - E)^{1/2}, E \leq E_C \\ D_{V0} \times e^{-(E-E_V)/qV_0}, E > E_C \end{cases}. \quad (2.53)$$

The first part of the expression is still the ideal energy dependent DOS. However, the second part of DOS is the Urbach band tail with Urbach parameter (qV_0) and constant prefactors D_{C0} and D_{V0} where $D_C(E_C)=D_{C0}$. Urbach parameters are determined by using optical measurements

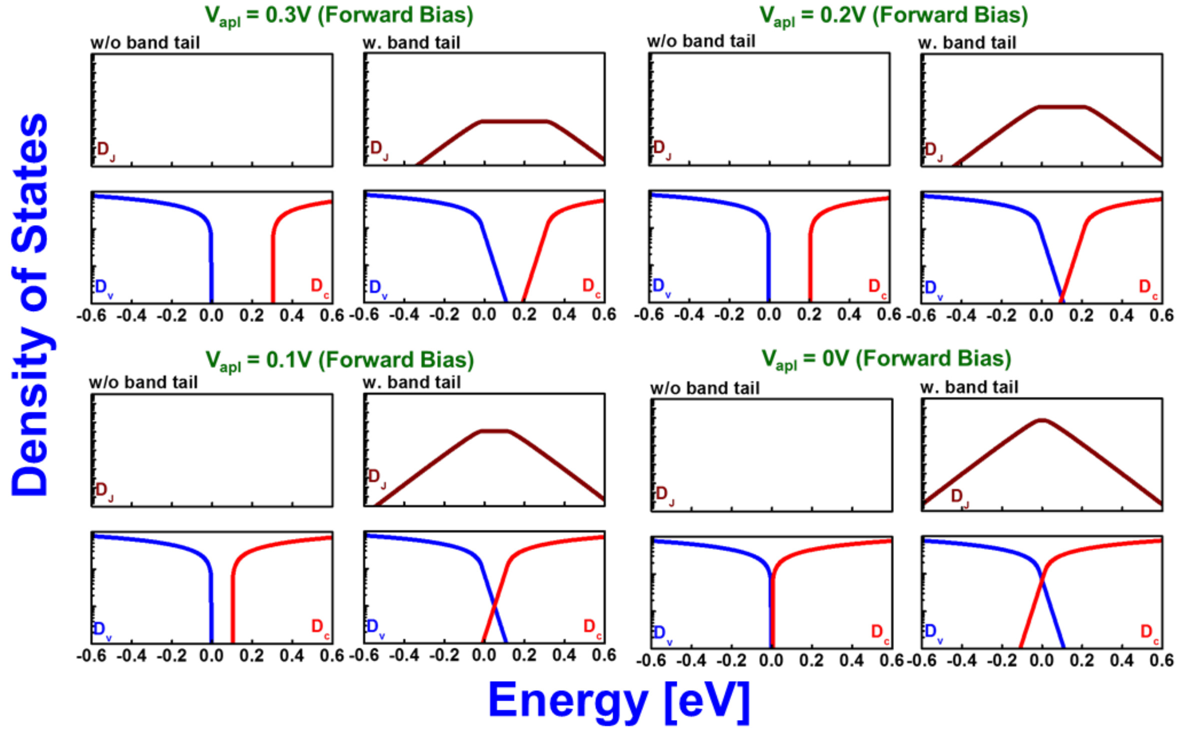

Figure 2.8: The joint density of states (D_J) under forward bias with varied applied voltage.

and it is typically 0.15 eV for GaSb and 3-6m eV for GaAs [26, 29]. The joint density of states (D_J) under forward bias and reverse bias with varied applied voltage are shown in Figures 2.8 and 2.9, respectively. The band tails of conduction and valance bands convolve even when two band edges don't overlap. These extra D_J introduce unwanted currents before the BTBT currents occur resulting in lower SS. I_D and V_{GS} of GaSb/InAs TFET for a range of Urbach parameters (qV_0) is shown in Figure 2.10. It can be observed that small qV_0 values could have

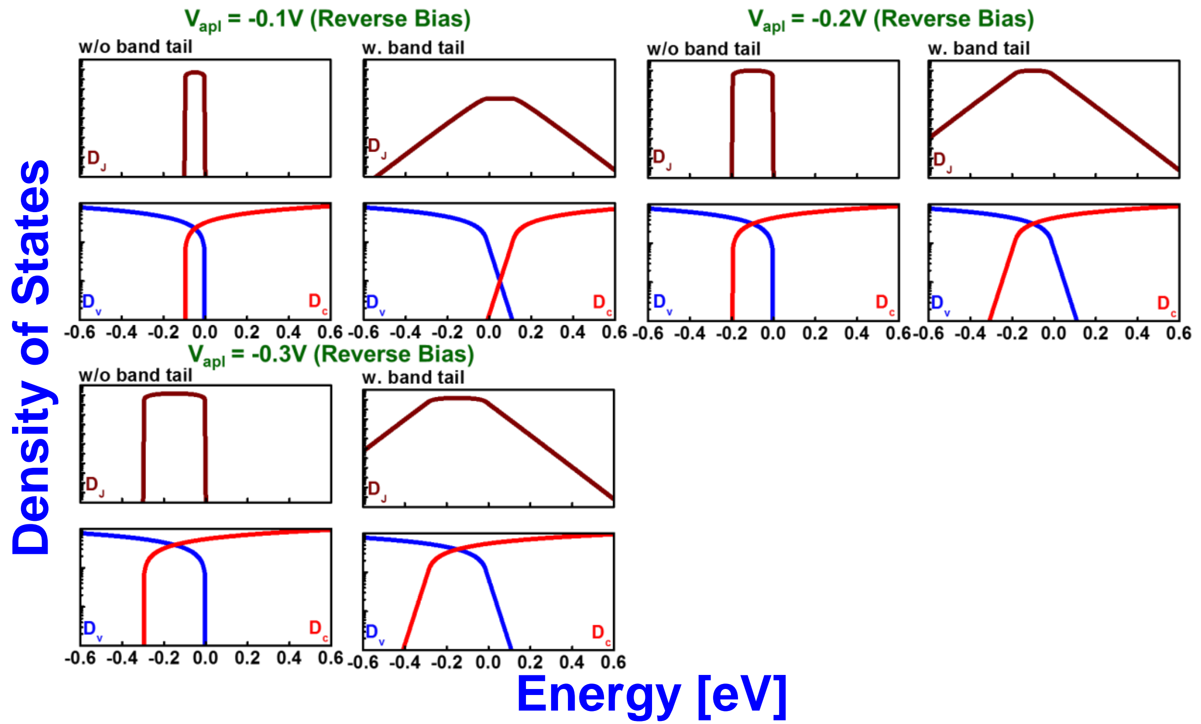

Figure 2.9: The joint density of states (D_J) under reverse bias with varied applied voltage.

significant enhancement on leakage currents and degradation on SS. Therefore, heterointerface engineering is a critical challenge for keeping SS within 60mV/decade.

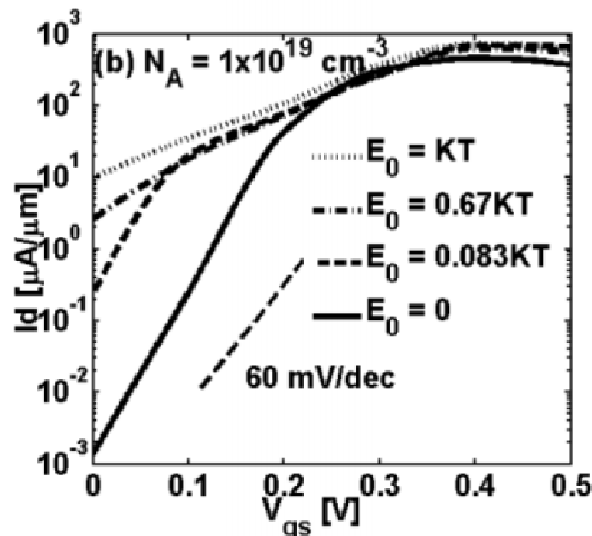

Figure 2.10: $I_D - V_g$ characteristic with the different Urbach parameters [27].

2.5. Criteria III: High κ Oxide

From Eq.2.15, we know that the gate oxide and interface traps have strong influence on SS. By revisiting Eq. 2.27, we could express the triangle barrier as follows [30]:

$$F = \frac{E_{beff} + \Delta\Phi}{\Lambda}, \tag{2.54}$$

where Λ is the length of the tunneling region at the source-channel interface. The tunneling length could be divided into two parts: screening length and scale length of channel. The screening length is a Debye length with doping N_D which could be described as [25],

$$\lambda_{dop} = \sqrt{\frac{\varepsilon_{Si} kT}{q^2 N_D}}. \tag{2.55}$$

On the other hand, the scale length of channel could be written as [31-33],

$$\lambda_{ch} = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{ox} t_{Si}}, \tag{2.56}$$

where ε_{ox}, t_{ox} are the permittivity and the thickness of gate dielectric for double gate TFETs (DG-TFETs), respectively. In normal cases, λ_{ch} (~nm) dominates over λ_{dop} (< nm) in tunneling distance. Therefore, we can insert Eq. 2.56 into Eq. 2.27 resulting

$$T = \exp\left[-\frac{4\sqrt{2m^*} E_{beff}^{\frac{3}{2}}}{3q\hbar\left(E_{beff} + \Delta\Phi\right)} \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{ox} t_{Si}}\right]. \tag{2.57}$$

The expression indicates that thinner gate dielectric or higher κ materials could enhance not only SS performance but also tunneling current. Hence, applying high-κ gate dielectric on TFETs are the necessary parts for high performance TFETs.

In summary, for steep subthreshold slope TFETs, we must fulfill the following requirements:

(i) High tunneling probability,

(ii) High quality (abrupt, defect-free) heterointerface,

(iii) High-κ gate dielectric.

We shall investigate these parameters in subsequent chapters.

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Chapter 3

Heterointerface Engineering of Broken-Gap InAs/GaSb

According to the design criteria for TFETs discussed in *Chapter 2*, we can select a material system which provides a tunable E_{beff} and abrupt, defect-free heterointerface. Recently, mixed arsenide/antimonide based $In_xGa_{1-x}As/GaAs_{1-y}Sb_y$ TFET device structures with variable arsenic (As) and antimony (Sb) alloy compositions for a wide range of adjustable effective tunnel barrier height (E_{beff}), such that these two layers are internally lattice matched, were extensively studied by several researchers [1-3]. In such configurations, controlling alloy compositions while simultaneously maintaining the internally lattice matched condition is extremely challenging due to the formation of an unwanted layer by surface termination of atoms at the source/channel heterointerface. For extreme case such as InAs/GaSb TFET, the ideal band alignment would be a broken gap configuration. However, the local strain at the InAs/GaSb interface depends on two types of interfacial bonds: tensile Ga−As bonds and compressive In−Sb bonds [4]. As a result of these interfacial bonds, the interface could be GaAs-like due to Ga/In exchange during the growth of an InAs/GaSb TFET structure. Moreover, different types of interfacial layers have distinct strain relaxation properties and one (GaAs-like) will introduce large number of dislocations at the 0.62% tensile strained InAs on GaSb substrate that will increase the OFF-state current in an InAs/GaSb TFET [5]. On the other hand, the formation of InSb-like interfacial layer at the InAs/GaSb heterointerface would compensate the tensile strain, and an additional compressive strain amount will help to decrease the defect density and prevent strain relaxation. As a result, one could achieve strain balanced InAs/GaSb multilayer heterostructures by controlling proper thicknesses of each layer and

switching sequences of As, Sb, indium (In), and gallium (Ga) at each heterointerface during growth.

3.1. InAs/GaSb Interface Characterization

Figure 3.1(a) shows the schematic of the InAs/GaSb multilayer heterostructure selected for this work, where the thickness of each layer is indicated in this figure, and Figure 3.1(b) shows the shutter sequences for this InAs/GaSb multilayer heterostructure growth. The nominal thickness of each layer is about 15 nm, and the lattice mismatch between the InAs and GaSb is about 0.62%. To achieve well-controlled coherent heterointerface, GaAs-like interfacial layer must be prevented during growth. In the shutter sequence, two methods were used to form InSb-like interfacial layer: (1) InSb stacking and (2) Sb soaking. After the completion of GaSb layer growth, the Sb flux was left open for 6 s followed by 4 s of In exposure to create an artificial thin InSb layer in between the GaSb and InAs layer. The As_2 flux was open for the duration of the InAs layer growth, and prior to the GaSb deposition, the InAs surface was soaked by Sb_2 for 6 s. Since the vapor pressure of As is higher than that of Sb, the exposure of Sb on the surface of InAs for a short duration helps prevent As from escaping the surface of InAs prior to GaSb layer growth. Thus, through the subtle control of the InAs/GaSb epitaxial

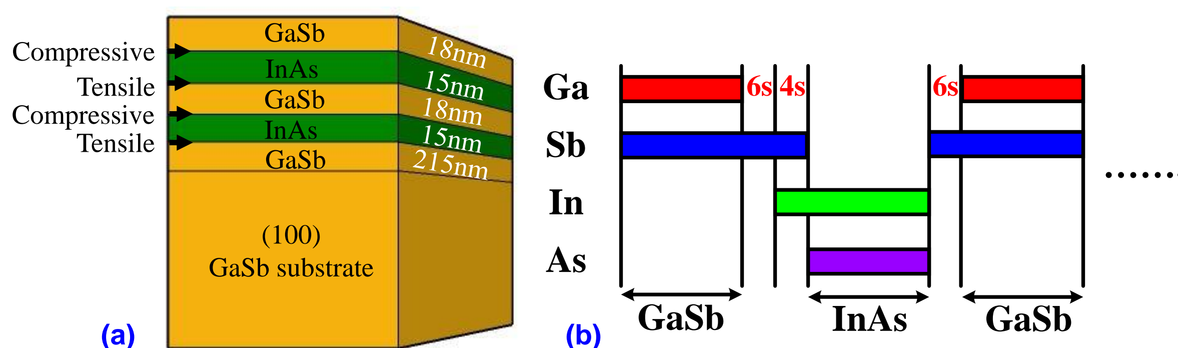

Figure 3.1: (a) Schematic diagram of InAs/GaSb multilayer heterostructure and (b) MBE shutter sequence for this multilayer growth with InSb deposition at the GaSb/InAs and antimony soaking at the InAs/GaSb heterointerface. The layer InAs/GaSb substrate interface is tensile, and the GaSb/InAs interface is compressive, as indicated.

heterointerface, we could achieve the overall strain balanced structure, and both the InAs and GaSb layers are internally lattice matched in the growth sequence studied here. The InAs/GaSb substrate interface is tensile (T) and GaSb/InAs interface is compressive (C) as indicated in Figure 3.1(a), and the equal number of C/T layers balances the strain, which can be seen from the cross-sectional TEM as well as X-ray analysis below.

The InAs/GaSb multilayer heterostructure was investigated by cross-sectional TEM measurement and analysis. Figure 3.2(a-b) shows the high-resolution TEM micrographs of the InAs/GaSb multilayer stack consisting of 4 layer (2 tensile interface and 2 compressive interface). In this figure, each layer and interface were labeled to match with the growth

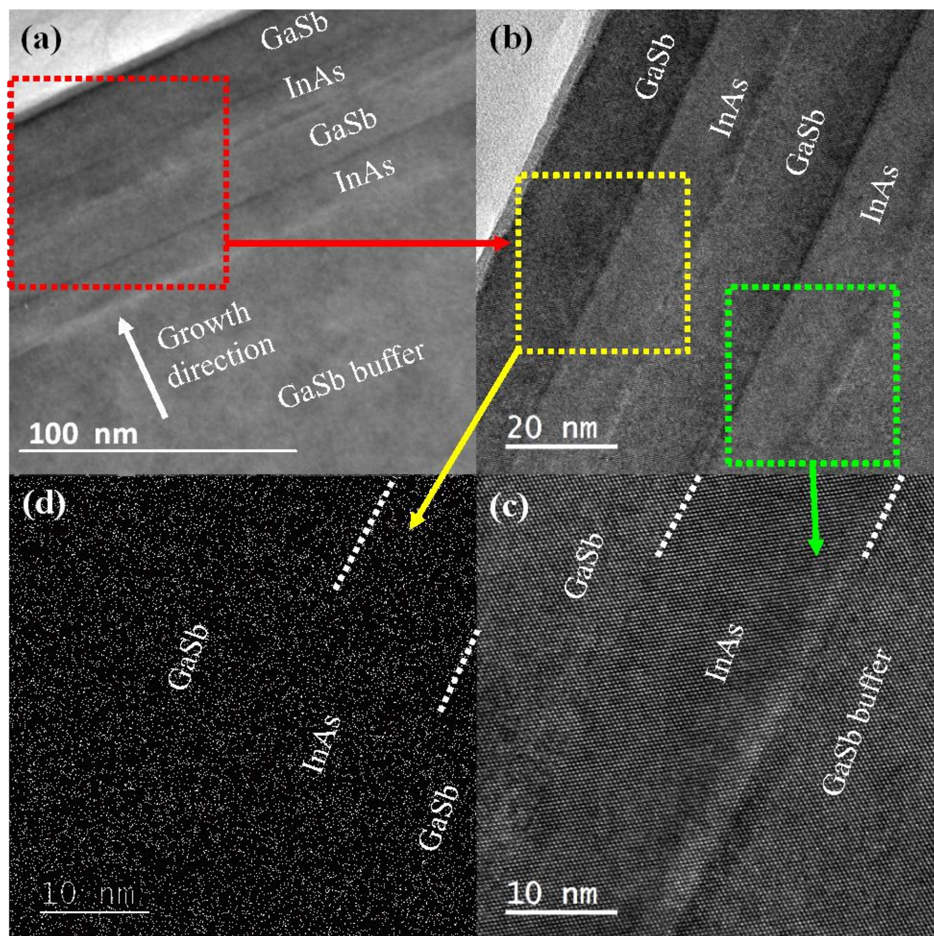

Figure 3.2: (a) High-resolution cross-sectional TEM micrograph of InAs/GaSb multilayer structure and (b−d) lattice indexing of the GaSb/InAs/GaSb stack showing each abrupt heterointerface.

sequence of the multilayer stack, as shown in Figure 3.1(a). Figure 3.2(c-d) shows high resolution lattice indexing of the epitaxial InAs layer on GaSb buffer layer and epitaxial GaSb on InAs epilayer, respectively. These TEM micrographs showed that the epilayers were homogeneous and with smooth heterointerfaces. In the InAs-on-GaSb interface, an intentionally added 4 s of growth time enabled the InSb interfacial layer to achieve a high-quality heterointerface, and this layer will compensate the tensile strain amount of 0.62% between InAs and GaSb. The mixture fluxes of both In and Sb limited the As coverage, which tends to form GaAsSb, thus accumulating more tensile strain at the InAs-on-GaSb heterointerface [4,6]. Furthermore, Sb soaking after the InAs deposition also restricted As coverage and prevented the formation of a GaAs-like layer. In fact, the exposure of Sb on the surface of InAs prior to GaSb growth prevents the As from escaping the InAs surface and acts as a surfactant during growth. Both methods tailored to create InSb-like interfacial layer at each heterointerface. The InSb-like interfaces provide strain compensation and virtually defect-free heterointerfaces. Each interface exhibited an abrupt heterojunction, which is essential for high-performance TFET structure that can reduce the leakage current under reverse gate voltage.

High-resolution X-ray diffraction was used to investigate the strain relaxation properties of InAs/GaSb multilayer layer structure. Figure 3.3 shows X-ray rocking curve of 18 nm GaSb/ 15 nm InAs/18 nm GaSb/15 nm InAs/GaSb substrate structure. A simulation was performed to identify the position of the InAs peak from thickness fringes. In Figure 3.3, a green line shows the simulated rocking curve from 15 nm InAs layer on GaSb substrate with the addition of an ultrathin 0.5 nm InSb interfacial layer. One can locate the InAs peak position with respect to the GaSb substrate peak. However, the simulated rocking curve with 0.5 nm InSb interfacial layer at InAs on GaSb and GaSb on InAs heterointerface exhibited that the InAs layer was affected in the multilayer configuration. Besides, InAs layers provide an envelope function for fringes next to the GaSb peak and have a peak-pulling effect due to the multilayer structures.

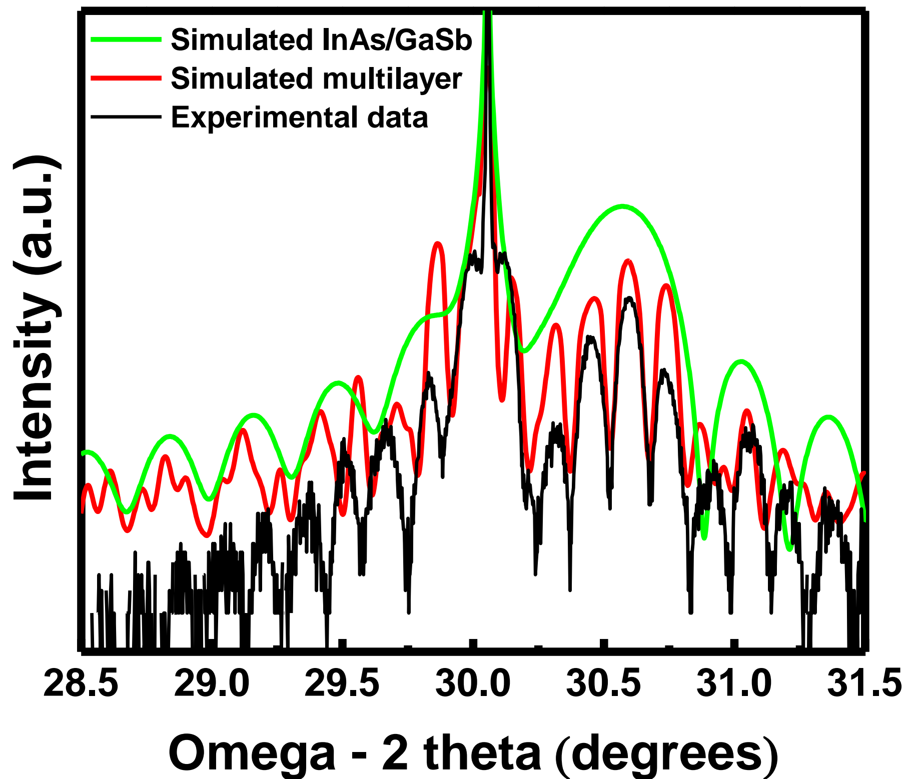

Figure 3.3: (Black) Symmetric experimental (004) rocking curve and(red) simulated rocking curve of InAs/GaSb multilayer structure, and (green) simulated rocking curve of only 15 nm InAs on GaSb with an ultrathin 0.5 nm layer of InSb. The thickness fringes demonstrate the superior quality of this heterostructure. The envelope line of three secondary fringes were InAs epilayers affected by multilayer structures.

The simulated rocking curve also shows the complexity of fringes due to InAs/GaSb multilayer structure with an InSb interfacial layer. The simulation further confirms the existence of interfacial layers, shown in Figure 3.2(b–d). Figure 3.4 shows the symmetric (004) and asymmetric (115) reciprocal space maps (RSMs) of the layer structure, respectively. As Figure 3.4(a) shows, the thickness fringes become the contours of intensity, and the InAs reciprocal lattice point (RLP) is in agreement with the X-ray rocking curve. The stronger intensity of the InAs RLP (shown by an arrow) provided the information on the layer separate from the thickness fringes. Moreover, the RLP of the GaSb substrate and the InAs is in the same vertical

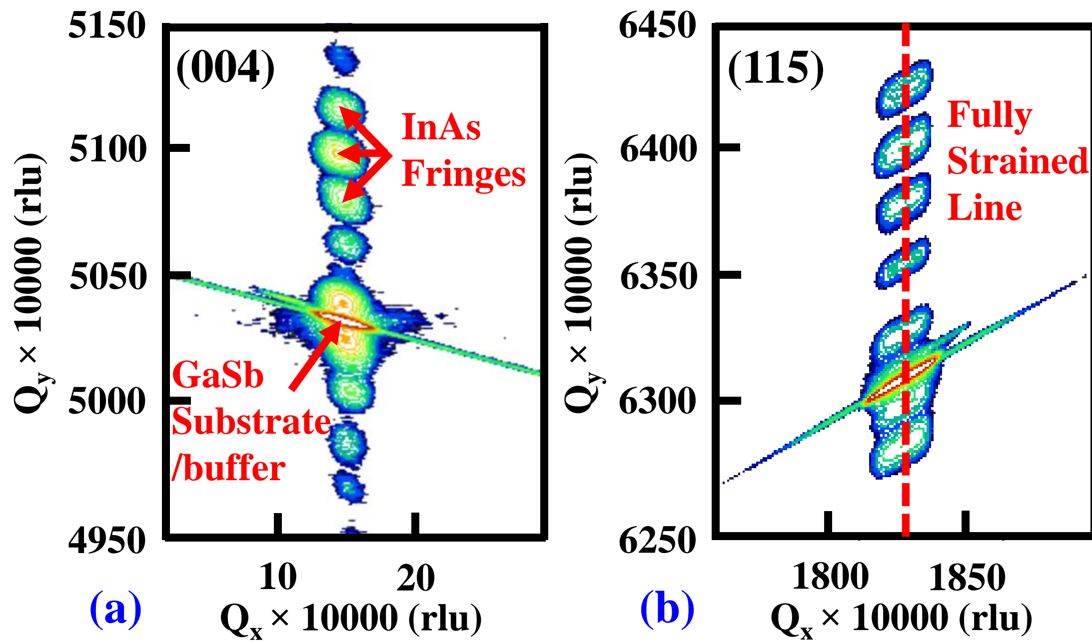

Figure 3.4: (a) Symmetric (004) and (b) asymmetric (115) reciprocal space maps of InAs/GaSb multilayer structure. The thickness fringes become contour of intensity. All the thickness fringes of InAs and GaSb RLPs lie along the fully strained vertical line.

line indicates minimal or no lattice tilt, as expected since the entire layer structure is strain balanced. Further, the properties of relaxation and strain state could be obtained from asymmetric (115) RSM, shown in Figure 3.4(b). One can find that all of the RLPs are lying on the fully strained line, which further confirms the balanced strain generated by compressively strained GaSb-on-InAs and tensile strained InAs-on-GaSb by proper heterointerface engineering. The aligned vertical line indicates the same in-plane lattice constant of InAs and GaSb, supported by the TEM results discussed above. One can anticipate that a GaAs-like interfacial layer might abolish the strain balance system by introducing additional tensile strain in the structure [6]. An intentionally inserted ultrathin InSb interfacial layer at the bottom interface and an InAsSb layer due to As/Sb exchange balanced the strain in interface, thus creating a strain balanced structure. Thus, an abrupt heterointerface and well-controlled strain compensation are suitable for further high-performance n- and p-channel TFET applications.

The layer structure was further characterized using AFM. Figure 3.5 shows the surface morphology from the surfaces of 2× 2 µm and 5 × 5 µm area scans. The surface root-mean-square (rms) roughness were found to be ~0.42 and 0.55 nm, respectively. Smooth surface

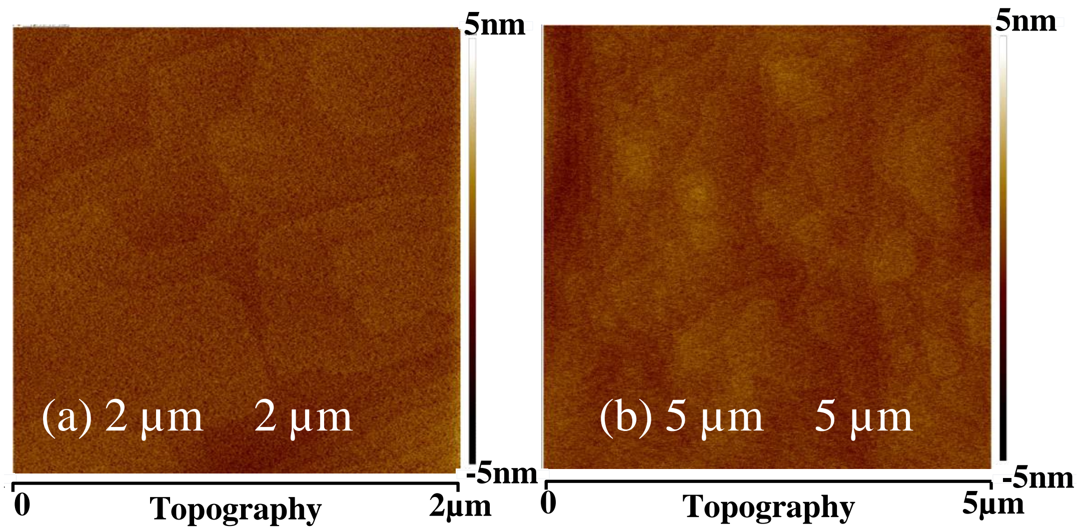

Figure 3.5: Surface morphology of multilayer structures were investigated by AFM. The root-mean-square (rms) surface roughness of 0.42 and 0.55 nm were recorded from (a) 2 × 2 µm and (b) 5 × 5 µm area scan, respectively.

morphology implies minimal dislocations inside the epitaxial layer structure, which is supported by both TEM and X-ray analysis above. Furthermore, lower surface roughness can also be related to well-controlled elements switching during growth. In fact, lower rms surface roughness was reported by creating an ultrathin layer of InAs-like interface during the growth of InGaAs/ GaAsSb TFET structure [5].

3.2 Band Alignment Measurement of InAs/GaSb

The band offset parameters at the InAs/GaSb heterointerface are an important design parameter for a broken gap InAs/GaSb based tunnel FET structure. X-ray photoelectron spectroscopy spectra revealed binding energy information for each materials. The core levels (CLs) and valence band maxima (VBM) spectra were recorded to determine the band alignment between the GaSb and the InAs layer. The band alignment properties were determined by

Kraut's method [7]. The valence band offset (VBO) between the GaSb and the InAs can be expressed as

$$\Delta E_V = \left(E_{Sb\,4d_{5/2}}^{GaSb} - E_{VBM}^{GaSb}\right) - \left(E_{As\,3d_{5/2}}^{InAs} - E_{VBM}^{InAs}\right) - \Delta E_{CL} \quad (3.1)$$

where $E_{Sb\,4d_{5/2}}^{GaSb}$ and $E_{As\,3d_{5/2}}^{InAs}$ are CL binding energy of Sb $4d_{5/2}$ and As $3d_{5/2}$ from GaSb and InAs layer, respectively; E_{VBM}^{GaSb} and E_{VBM}^{InAs} were VBMs for respective material. $\Delta E_{CL} = E_{Sb\,4d_{5/2}}^{GaSb} - E_{As\,3d_{5/2}}^{InAs}$ is the difference in CL binding energy from the GaSb and InAs

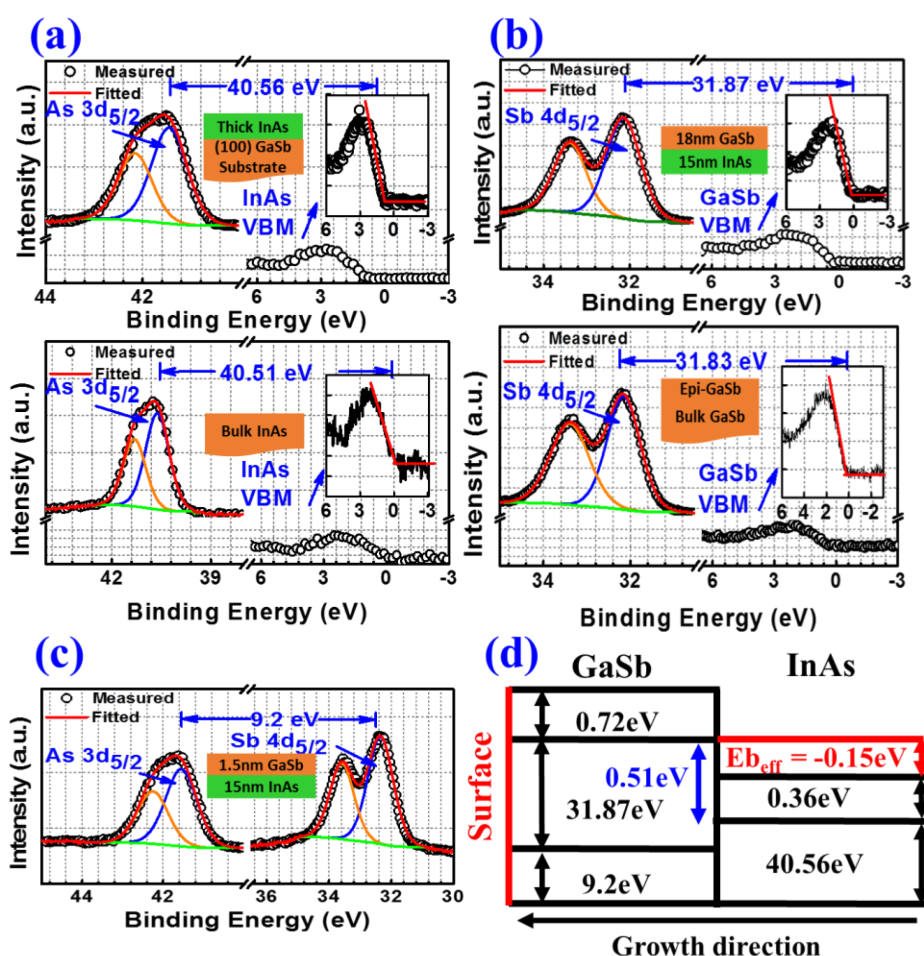

Figure 3.6: XPS spectra of (a) As 3d core level ($E_{As\,3d}^{As}$) and valence band maximum, VBM (E_{VBM}^{InAs}) from thick InAs film, (b) Sb 4d ($E_{Sb\,4d}^{Sb}$) core level and VBM (E_{VBM}^{GaSb}) from thick GaSb film, (c) As 3d, Sb 4d core levels from ~1.5 nm GaSb/InAs interface, and (d) energy-band alignment of the GaSb/InAs heterointerface, respectively.

heterointerface. Figure 3.6 shows the CL binding energies and corresponding VBMs from the (a) thick InAs layer, (b) thick GaSb layer and (c) the GaSb/InAs heterointerface, respectively. Using the measured data and the equation above, the VBO was determined to be 0.51$\pm$0.05eV. During the XPS measurement, constant flow of electrons was used throughout the measurement to compensate the charging effect. Using the bandgap values of InAs ($E_G^{InAs} = 0.36eV$) and GaSb ($E_G^{GaSb} = 0.72eV$) at 300K, the effective barrier height, $E_{beff} = E_G^{InAs} - \Delta E_V$ of -0.15 eV was determined, as shown in Figure 3.6(d). It is worth nothing that the band bending effect caused by the semiconductor-to-semimetal transition should be considered during determining the band alignment especially in the broken gap system [8-10]. To address this issue, we have measured XPS spectra from the bulk InAs and homoepitaxial 1 μm thick epi-GaSb on GaSb substrate. The energy difference between the CL and the VBM for a thick 20 nm epi-InAs and the bulk InAs substrate are 40.56 and 40.51 eV, respectively, as shown in Figure 3.6(a). Similarly, the energy differences are 31.87 and 31.83 eV for 18 nm GaSb and 1 μm thick epi-GaSb on GaSb substrate, respectively, shown in Figure 3.6(b). One can find from Figure 3.6(a-b) that the difference (CL to VBM) between the epilayer and the bulk are 0.05 and 0.04 eV for InAs and GaSb, respectively. These values are within the XPS measurement error bar [11]. This E_{beff} value is in agreement with the previously reported results [12-14]. Here, the negative value indicates the broken gap configuration at the GaSb/InAs heterointerface. This E_{beff} value determines the ON- and OFF-state current of a mixed As/Sb based tunnel FET device structure.

3.3. Band Alignment Engineering of InGaAs/GaAsSb

To correlate the experimental band alignment values and hence the E_{beff} as a function of In and Sb alloy compositions in InGaAs/GaAsSb TFET structure, we performed the modeling using TCAD Sentaurus, version H. Figure 3.7(a) shows both simulated and experimental E_{beff}

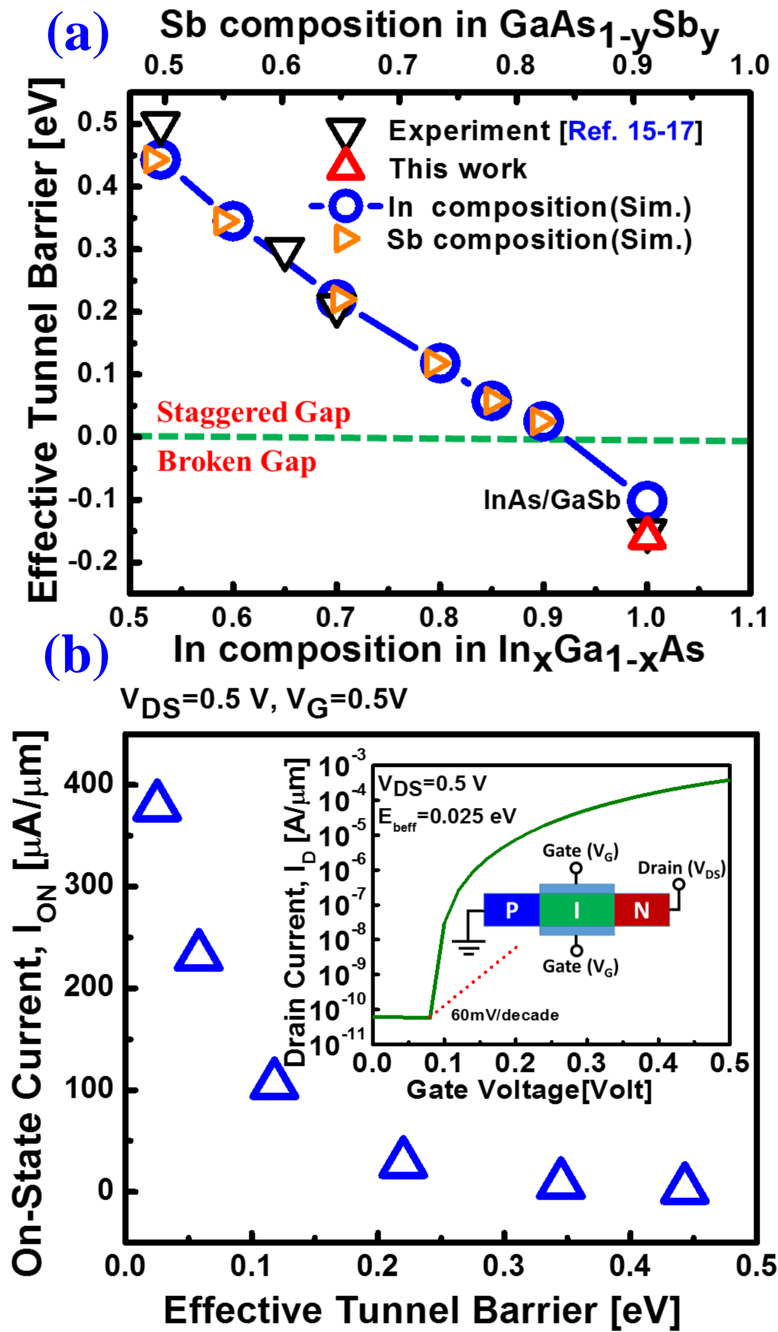

Figure 3.7: (a) Experimental and simulated E_{beff} as a function of In and Sb compositions in $In_xGa_{1-x}As/GaAs_{1-y}Sb_y$ material system. The experimental results are in agreement with the simulated prediction. (b) Simulated I_{ON} as a function of effective tunnel barrier height.

corresponding to a various In and Sb compositions in $In_xGa_{1-x}As/GaAs_{1-y}Sb_y$ system such that for each In and Sb composition, the InGaAs and GaAsSb layers are internally lattice matched.

Simulation model was calibrated with the experimental band alignment value with the In composition of x = 0.7 and the Sb composition of y = 0.65 [15]. One can find from this Figure 3.7(a) that the E_{beff} value decreases from 0.44 eV where x = 0.53 and y = 0.49 (staggered gap) to −0.1 eV where x = 1 and y = 1 (broken gap) with increasing In and Sb compositions. The lowest simulated staggered gap E_{beff} is 0.06 eV for ann$_{0.9}$Ga$_{0.1}$As/GaAs$_{0.1}$Sb$_{0.9}$ TFET structure. The results of simulated I_{ON} as a function of E_{beff} are shown in Figure 3.7(b). The inset shows the drain current, I_D, with gate voltage swing. To improve the ability of gate control in a nanoscale TFET, the double gate p-i-n TFET (channel thickness of 5 nm), long channel (channel length of 40 nm), and low equivalent oxide thickness (EOT of 1 nm) were used in this simulation. Asymmetric doping of source and drain values of 4×10^{19} cm^{-3} and 6×10^{17} cm^{-3}, respectively, were considered to prevent ambipolar current conduction. It was found that the I_{ON} current is strongly dependent on the E_{beff} under $V_{GS} = V_{DS} = 0.5$ V conditions. The increase in I_{ON} in this material system is believed to be due to the increase in tunneling probability compared with the material system of 0.35 eV tunnel barrier height. However, compositions lower than $In_{0.9}Ga_{0.1}As/GaAs_{0.1}Sb_{0.9}$ system, the E_{beff} is negative, and even higher ON current can be attainable, but measures must be taken to reduce the OFF-state leakage of such structure. The quantization and strain effect were not taken into account in this calculation. This first-order E_{beff} calculation, which is in agreement with the experimental results [15-17], provides critical guidance for designing mixed As/Sb-based tailor-made tunnel FET device structure.

In summary, high-quality broken gap strain balanced InAs/ GaSb multilayer structure, grown using solid source MBE, with InSb-like interfacial layer were demonstrated by analyzing structural, morphological, and band alignment properties. A smooth surface morphology with surface roughness of about 0.5 nm was achieved. The effective barrier height at the GaSb/InAs heterointerface was determined to be −0.15 eV by X-ray photoelectron spectroscopy, which is in agreement with other reported results. Thus, one can tailor the energy barrier of internally

lattice matched GaAsSb/InGaAs heterointerface by precisely controlling the growth sequences of antimony- and arsenide-based material systems.

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Chapter 4

Tailoring the Valence Band Offset of Al_2O_3 on Epitaxial $GaAs_{1-y}Sb_y$ with Tunable Antimony Composition

In *Chapter 2 Section 2.5*, we explained why we need high κ dielectric for reducing effective oxide thickness (EOT) and enhancing SS. In addition, in *Chapter 3*, we studied the possible candidate material system (InGaAs/GaAsSb) to achieve high I_{ON} and low SS TFETs. For a complementary p-channel TFETs, $GaAs_{1-y}Sb_y$ material was used to serve as a channel material in GaAsSb/InGaAs TFET configuration. However, integration of a superior high-κ gate dielectric on the GaAsSb material system for any Sb composition remains elusive to date due to the formation of complex native oxides on the GaAsSb surface [1]. Thus, there is a major challenge in achieving a low interface density at the high-κ gate dielectric/GaAsSb heterointerface that necessitates the surface passivation of $GaAs_{1-y}Sb_y$ dangling bonds for tunable Sb compositions ($0 \leq y \leq 1$). In the past, Al_2O_3 high-κ dielectric was used on GaAs and GaSb materials using atomic layer deposition (ALD) for transistor applications [2-4]. Unlike SiO_2 grown on Si, the native oxide of $GaAs_{1-y}Sb_y$ is a complex mixture of GaO_x, AsO_x, and SbO_x, as investigated by several researchers [1, 5-8]. Developing a proper technique for the replacement of native oxide and passivation of oxide-semiconductor interface would make it possible to achieve a precise band alignment determination of Al_2O_3 on Sb compositionally dependent $GaAs_{1-y}Sb_y$. Although, sulfur (S) passivation and the band alignment of both Al_2O_3/GaAs and Al_2O_3/GaSb were reported [9-10], the surface passivation and the energy band alignment of Al_2O_3 on $GaAs_{1-y}Sb_y$ with tunable Sb composition is sparse and remains unknown. This study focuses on the properties of sulfur passivated GaAsSb surfaces with

higher Sb compositions as well as Sb compositional dependent valence band and conduction band offsets of $Al_2O_3/GaAs_{1-y}Sb_y$ interfaces. The compositional dependent band alignment and detailed surface passivation schemes on the $GaAs_{1-y}Sb_y$ films are a significant step toward the development of $In_xGa_{1-x}As/GaAs_{1-y}Sb_y$ -based transistor and multifunctional device applications.

4.1. TEM Analysis of High-κ Dielectric on $GaAs_{1-y}Sb_y$

Figure 4 shows the high-resolution cross-sectional TEM micrograph of the $Pt/Al_2O_3/GaAs_{0.49}Sb_{0.51}$ MOS structure. The relative uniformity of the $Al_2O_3/GaAs_{0.49}$ $Sb_{0.51}$ interface is clearly visible in the high-resolution TEM micrograph. This micrograph also demonstrates the abrupt nature of the heterointerface. Further, the TEM results demonstrate the high degree of coherency of the ALD deposited 6.8 nm thick amorphous Al_2O_3 layer on $GaAs_{0.49}$ $Sb_{0.51}$ layer. The observed uniformity at the interface between the amorphous Al_2O_3 and the $GaAs_{0.49}$ $Sb_{0.51}$ layer is indispensable in minimizing interface scattering for carrier

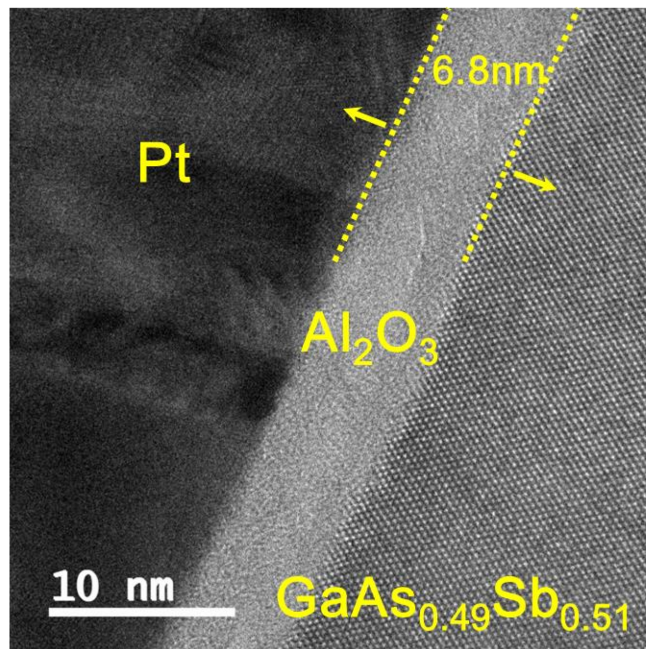

Figure 4.1. High-resolution TEM micrograph of the $Pt/Al_2O_3/GaAs_{0.49}Sb_{0.51}$ interface, demonstrating a sharp heterointerface between Al_2O_3 and $GaAs_{0.49}Sb_{0.51}$.

transport in future GaAsSb based MOS devices. Utilizing this Al_2O_3/$GaAs_{0.49}$ $Sb_{0.51}$ heterointerface, one can achieve superior transport characteristics such as lower interface states, reduced frequency dispersion, lower capacitance−voltage hysteresis, and targeted equivalent oxide layer thickness, all needed for ultra-low power TFETs.

4.2. Surface Passivation of $GaAs_{1-y}Sb_y$ via XPS Analysis

The Sb compositional dependent valence band and conductance band offsets of GaAsSb with high-κ dielectrics, such as Al_2O_3, has great significance for tunable tunnel barrier height InGaAs/GaAsSb based heterojunction TFETs. The formation of complex native oxides on the GaAsSb surface (i.e., Sb_2O_3, As_2O_3, Ga_2O_3, etc) [6,11] makes the GaAsSb material system difficult to control the interface defect density especially for p-channel TFETs application. Various wet chemical processes to passivate the surface of either GaAs or GaSb materials have been prescribed by several studies [8-10, 12-13]. However, the surface passivation study on the GaAsSb material system is unclear or remains unknown. Here, ***we have systematically studied*** the surface passivation schemes of $GaAs_{0.45}Sb_{0.55}$ layers by XPS. This Sb composition was selected since it is almost the mid-point composition of the GaAs-GaSb material system. Different combinations of cleaning processes were developed and implemented on the selected composition of epitaxial $GaAs_{0.45}Sb_{0.55}$, GaAs, and GaSb surfaces for this study. In this particular work, four samples were selected to investigate the effect of pre-clean and surface passivation prior to the deposition of ALD Al_2O_3 layer on $GaAs_{0.45}Sb_{0.55}$: (i) as-received $GaAs_{0.45}Sb_{0.55}$ layer, (ii) HCl-treated $GaAs_{0.45}Sb_{0.55}$ epi-layer, (iii) $(NH_4)_2S$-treated $GaAs_{0.45}Sb_{0.55}$ epi-layer, and (iv) HCl plus $(NH_4)_2S$-treated $GaAs_{0.45}Sb_{0.55}$ epi-layer.

Figures 4.2(a) and 4.2(b) show the Ga3d and O2s as well as As3d and Sb4d CL spectra recorded from the surface of each sample, respectively. The peak positions of each sample were

s hifted as well as aligned vertically to observe the peak evolution due to the surface cleaning and passivation methods. The Ga-O (21.0eV), As-O (44.7eV), and Sb-O (34.2eV) peaks were found from the as-grown $GaAs_{0.45}Sb_{0.55}$ layer, as expected, due to the lack of surface pre-cleaning prior to the XPS measurement. The as-grown $GaAs_{0.45}Sb_{0.55}$ sample was pre-cleaned using HCl and the subsequent XPS measurement demonstrated minimal amount of Ga-O and As-O peaks, as shown in Figure 4.2(a) and 4.2(b), indicating the effectiveness of HCl to remove the native oxides of Ga-O and As-O from the surface of $GaAs_{0.45}Sb_{0.55}$. On the other hand, the HCl has limited effect for the removal of the Sb-O native oxide peak. The as-grown $GaAs_{0.45}Sb_{0.55}$ sample was then passivated using $(NH_4)_2S$ without pre-cleaning by HCl and the corresponding peaks are also shown in Figure 4.2(a) and 4.2(b). One can find that the native

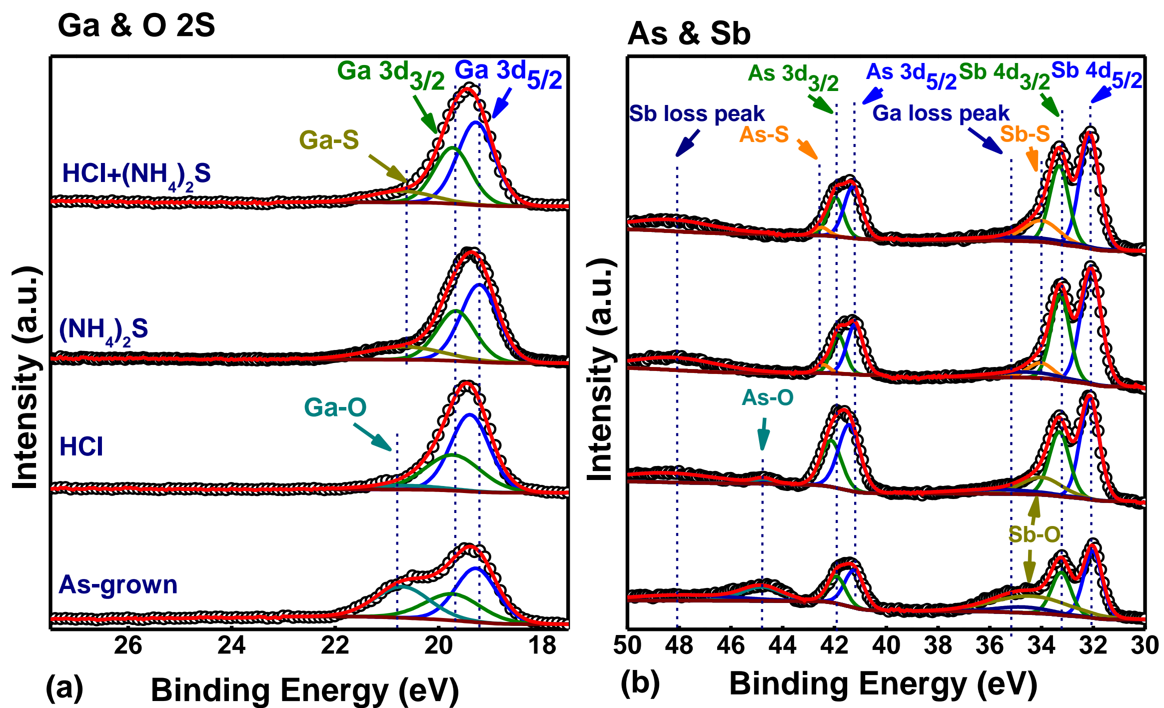

Figure 4.2. (a) Ga 3d and O 2s and (b) As 3d and Sb 4d XPS spectra, respectively, showing the chemical state evolution as a function of surface pre-clean and passivation on $GaAs_{0.45}Sb_{0.55}$. The peak positions of each sample were shifted as well as aligned vertically to observe the peak development due to the surface cleaning and passivation.

oxides (i.e., a mixture of Ga-O, As-O, and Sb-O) were effectively removed from the surface of as-grown $GaAs_{0.45}Sb_{0.55}$ by $(NH_4)_2S$. Furthermore, the Ga-O and Sb-O peaks unable to be removed by HCl were successfully removed by $(NH_4)_2S$ passivation. It is interesting to note that the Ga and Sb remain bound to S via $(NH_4)_2S$ processing even after a 30 min window between the initial passivation and when the samples were loaded and the XPS spectra recorded. This indicates that the Ga-S and Sb-S bonds are stable for at least 30 min in atmosphere, which is important where a long pause between the surface passivation and the deposition of high-κ dielectric could not be avoided. Finally, the as-grown $GaAs_{0.45}Sb_{0.55}$ sample was pre-cleaned by HCl and subsequently passivated using $(NH_4)_2S$ and the corresponding XPS spectra are shown in Figures 4.2(a) and 4.2(b). As can be seen in Figures 4.2(a) and 4.2(b), the Ga and Sb were bound to S and the As-O peak was eliminated by this combined wet chemical process. Therefore, one can conclude that either $(NH_4)_2S$ or the combination of HCl and $(NH_4)_2S$ processes on mixed As-Sb based GaAsSb materials are essential to clean and passivate the surface prior to the deposition of high-κ dielectrics.

1.5 nm ALD Al_2O_3 with HCl and $(NH_4)_2S$ surface passivation of GaAs and GaSb surfaces: The combined HCl and $(NH_4)_2S$ scheme was used to passivate the $GaAs_{0.45}Sb_{0.55}$ sample prior to the deposition of Al_2O_3. Besides passivated $GaAs_{0.45}Sb_{0.55}$, an as-grown $GaAs_{0.45}Sb_{0.55}$ sample was used along with GaAs and GaSb samples. The GaAs and GaSb samples were cleaned and passivated (HCl and $(NH_4)_2S$), and placed in the ALD chamber for the deposition of the 1.5 nm Al_2O_3 layer. The combination of an HCl pre-clean, sulfur passivation and ALD deposited 1.5 nm Al_2O_3 were considered as a prescribed solution for the removal of native oxides on GaAs and GaSb samples [14-15]. Here, we have utilized these steps on the GaAs and GaSb samples to observe the effect of passivation. All 4 samples (as-grown $GaAs_{0.45}Sb_{0.55}$,

passivated $GaAs_{0.45}Sb_{0.55}$, GaAs and GaSb) were loaded together into the XPS chamber for measurement.

Figures 4.3(a) and 4.3(b) show the Ga3d and O2s as well as As3d and Sb4d spectra recorded from the surface of each sample for different passivation conditions, respectively. In these figures, peak positions of each sample were shifted vertically to make all binding energies for

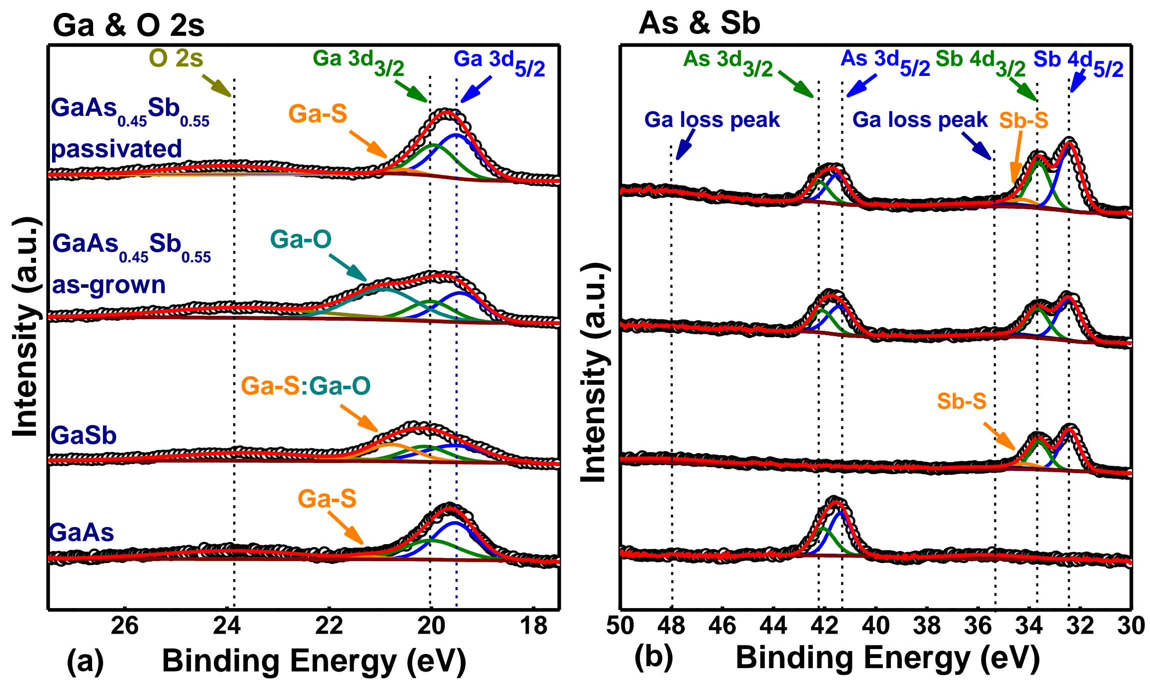

Figure 4.3 (a) Ga 3d and O 2s and (b) As 3d and Sb 4d XPS spectra, respectively, showing the existence of bonds as a function of surface pre-clean, passivation and atomic layer deposited Al_2O_3. Peak positions of each sample were shifted vertically to make all main element binding energies are aligned to the same position. The Ga-O peak from the as-grown $GaAs_{0.45}Sb_{0.55}$ with Al_2O_3, and the mixture of the Ga-O and Ga-S peaks from the GaSb sample after the HCl pre-clean, sulfur passivation and 1.5 nm Al_2O_3 layer shows the difficulty to make GaSb-based MOS devices. These peaks were eliminated from the GaAs and the $GaAs_{0.45}Sb_{0.55}$ layers after the HCl pre-clean, sulfur passivation and 1.5 nm Al_2O_3 layer, which can significantly affect the device performance.

of main element are aligned to the same position. From the XPS spectrum of GaAs and GaSb samples shown in Figure 4.3(b), the As-O (44.7eV) and Sb-O (34.2eV) bond peaks were eliminated due to the combined effect of pre-clean, sulfur passivation, and ALD deposited Al_2O_3 layer by trimethylaluminum (TMA) precursor [8,13]. It has been reported that the self-cleaning mechanism requires lower Gibbs free energy of material [13]. Indeed, the Al_2O_3 material has lower Gibbs free energy (-377.9 kcal/mol) than the energies of native oxides, which are Ga_2O, Ga_2O_3, As_2O_3, As_2O_5, Sb_2O_3 (-75.3 kcal/mol, -238.6 kcal/mol, -137.7 kcal/mol, -187.0 kcal/mol, and -151.5 kcal/mol) [6,16]. Therefore, the Al_2O_3 layer is more stable during the formation of Al_2O_3 oxide by ALD and further, it assisted in the removal of surface native oxides [12]. The TMA used in ALD for the Al_2O_3 deposition has an energetic preference to the native oxides on GaAs. In this case, the Gibbs free energy of As-O bonds were higher than Ga-O bonds, indicating that Ga-O bonds were more stable than As-O bonds during Al_2O_3 deposition, which has been shown in Figure 4.3(a). The peak position of the Ga-O bond (~21 eV) in the GaAs sample after sulfur passivation and Al_2O_3 layer deposition, is replaced by the presence of the Ga-S bond (dark orange color), indicating the strong surface passivation of the GaAs layer with the combined effect of pre-clean, sulfur passivation and Al_2O_3 layer deposition. On the other hand, the mixture of Ga-S and Ga-O bond peaks both at ~21 eV were observed from the GaSb sample, where the integrated peak area (orange color) with respect to the background is significantly higher than on the GaAs sample with the same cleaning process, exhibiting the less pronounced passivation as well as self-cleaning effect on the GaSb sample. The presence of the Ga-O (or Ga-S) peak at ~21 eV (which is difficult to decouple due to the similar binding energies of Ga-O and Ga-S) [12] even after sulfur passivation and Al_2O_3 deposition, one can find the difficulty to achieve superior quality metal-oxide-semiconductor (MOS) capacitor characteristics for future low power electronic devices. Thus, the surface passivation of the GaSb is more challenging than the GaAs under the same

HCl pre-clean and sulfur passivation conditions. It is interesting to investigate the detailed surface passivation of the mixed $GaAs_{0.45}Sb_{0.55}$ sample with different passivation conditions and the self-cleaning (if any) by Al_2O_3 deposition. This passivation study will provide information as to whether this material would exhibit either GaAs-like or GaSb-like passivation behavior since it is not well-understood in the literature.

1.5 nm ALD Al_2O_3 with HCl and* $(NH_4)_2S$ *surface passivation of GaAsSb surface: Figures 4.3(a) and 4.3(b) also show the Ga3d and O2s as well as As3d and Sb4d spectra, respectively, recorded from the surface of $GaAs_{0.45}Sb_{0.55}$ samples: (i) 1.5 nm Al_2O_3 on an as-grown sample and (ii) 1.5 nm Al_2O_3 on the HCl pre-cleaned and sulfur passivated sample. One can find from Figure 4.3(a) that the as-grown sample exhibits a strong Ga-O peak around 21 eV (cyan color), even after the atomic layer deposited 1.5 nm Al_2O_3, which indicates that the $GaAs_{0.45}Sb_{0.55}$ surface is not self-cleaned by TMA during the Al_2O_3 deposition. It is interesting to note that the Sb-O related peak (~34.2 eV) was not observed from the as-grown sample after Al_2O_3 deposition. Also, the As-O related peak (~44.7 eV) was not observed from the as-grown sample. These indicate that both As-O and Sb-O bonds can easily be removed during Al_2O_3 deposition from as-grown $GaAs_{0.45}Sb_{0.55}$ sample. The absence of As-O and Sb-O peaks from the surface of $GaAs_{0.45}Sb_{0.55}$ layer by ALD deposited Al_2O_3 is believed to be due the effect of the “self-cleaning” process observed for the first time to our knowledge. The measures must be taken to remove or passivate the Ga-O peak from the $GaAs_{0.45}Sb_{0.55}$ surface. The as-grown $GaAs_{0.45}Sb_{0.55}$ film was pre-cleaned with HCl and passivated with sulfur prior to the deposition of 1.5 nm Al_2O_3 to investigate the effect of pre-cleaning and sulfur passivation on the Ga-O bond. One can find from Figure 4.3(a) that the Ga-O peak which was observed in the as-grown sample, was eliminated by the above passivation scheme. The Ga-S and Sb-S peaks were observed around 20.5 eV and 34.2 eV, respectively. In the passivated $GaAs_{0.45}Sb_{0.55}$, the S

passivation suppressed the formation of Ga-O bonds and contributed to Ga-S and Sb-S bonds, shown in Figure 4.3(a) and 4.3(b) (the existence of S 2s peak not shown here confirmed the S related bonds). The S atom replaced the surface positon of oxygen atoms that were previously bonded with Ga and Sb atoms, thus preventing the formation of GaO_x and SbO_x native oxides. The Ga-O peak from the as-grown $GaAs_{0.45}Sb_{0.55}$ with Al_2O_3, and the mixture of Ga-O and Ga-S peaks from GaSb sample after the HCl pre-clean, sulfur passivation and 1.5 nm Al_2O_3 layer, shows the difficulty to demonstrate GaSb-based MOS devices. These peaks were eliminated after the HCl pre-clean, sulfur passivation and 1.5 nm Al_2O_3 layer deposition. Therefore, the surface passivation effect on $GaAs_{0.45}Sb_{0.55}$ has a close resemblance with the GaAs surface, which is beneficial for the electrical transport characteristics of GaAsSb-based MOS devices.

4.3. Band Alignment Analysis of $Al_2O_3/GaAs_{1-y}Sb_y$

High-resolution XPS was performed to determine the valence band offset (ΔE_v) of Al_2O_3/ $GaAs_{1-y}Sb_y$ with tunable Sb composition (0≤y≤1). The band alignments were determined by the energy difference between the core levels (CLs) and the valance band maxima (VBM) spectra recorded from each Al_2O_3 and $GaAs_{1-y}Sb_y$ surface. Kraut's method [17] was used to calculate ΔE_v by using these following equations:

$$\begin{aligned}\Delta E_{v,Sb} &= (E_{Sb4d_{5/2}}^{GaAsSb} - E_{VBM}^{GaAsSb}) - (E_{Al2p}^{Al_2O_3} - E_{VBM}^{Al_2O_3}) - (E_{Sb4d_{5/2}}^{GaAsSb} - E_{Al2p}^{Al_2O_3}) \\ \Delta E_{v,As} &= (E_{As3d_{5/2}}^{GaAsSb} - E_{VBM}^{GaAsSb}) - (E_{Al2p}^{Al_2O_3} - E_{VBM}^{Al_2O_3}) - (E_{As3d_{5/2}}^{GaAsSb} - E_{Al2p}^{Al_2O_3})\end{aligned}, \quad (4.1)$$

where, $\Delta E_{v,Sb}$ and $\Delta E_{v,As}$ are the valence band offset based on the VBM and CL of Sb and As, respectively. This will provide the difference in band offset value (if any) for a given Sb composition using either As or Sb CL spectrum. In order to determine the band offset, the following spectra were recorded: (i) the binding energy difference between the $Sb4d_{5/2}$ ($As3d_{5/2}$) CL and VBM of GaAsSb, $(E_{Sb4d_{5/2}}^{GaAsSb} - E_{VBM}^{GaAsSb})$ ($(E_{As3d_{5/2}}^{GaAsSb} - E_{VBM}^{GaAsSb})$) from the bulk

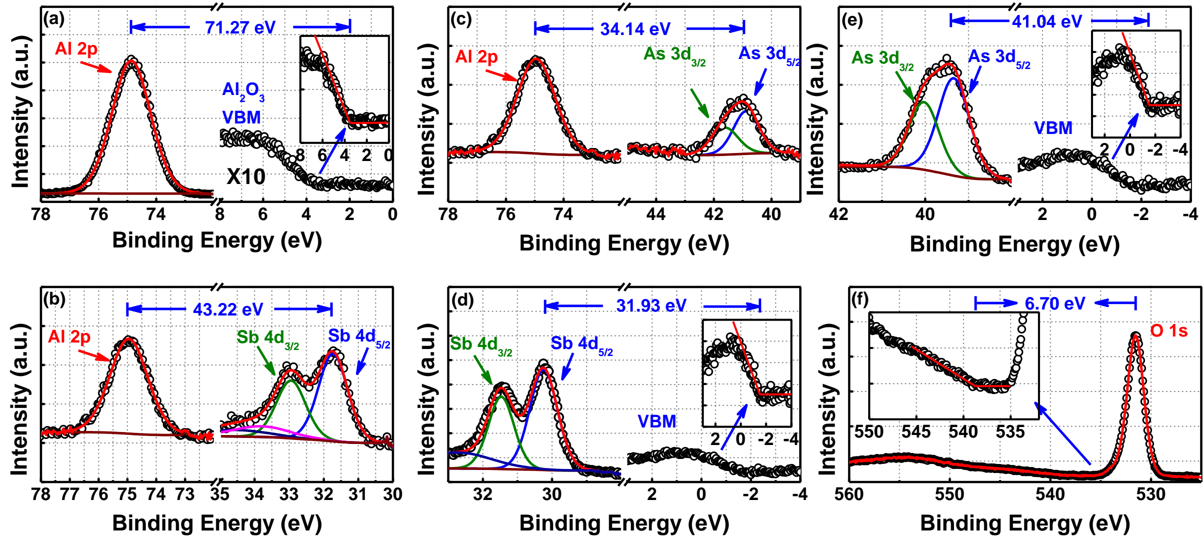

Figure 4.4. XPS spectra of (a) Al 2p from the 10 nm Al_2O_3, (b) from the interface of 1.5 nm Al_2O_3/ $GaAs_{0.49}Sb_{0.51}$ with Sb as a reference CL, (c) from the interface of 1.5 nm Al_2O_3/ $GaAs_{0.49}Sb_{0.51}$ with As as a reference CL, (d) Sb CL and valence band maximum, (e) As CL and valence band maximum, and (f) O 1s spectrum.

$GaAs_{1-y}Sb_y$ surface; (ii) the binding energy difference between the Al 2p CL and the VBM of Al_2O_3, $(E_{Al2p}^{Al_2O_3} - E_{VBM}^{Al_2O_3})$, from 10-nm-thick Al_2O_3; (iii) the binding energy difference between the Al_2O_3 and Sb (As) $(E_{Sb4d_{5/2}}^{GaAsSb} - E_{Al2p}^{Al_2O_3})$ $(E_{As3d_{5/2}}^{GaAsSb} - E_{Al2p}^{Al_2O_3})$ CLs from the interface of 1.5 nm Al_2O_3/$GaAs_{1-y}Sb_y$, respectively and the results of such spectra are shown in Figure 4.4. As shown in Figure 4.4, the passivated sample showed the suppression of oxygen bonds and enhanced passivation of dangling bonds by sulfur. Since the Ga peak has a stronger coupling between Ga-O and Ga-S bonds and the Ga CL, the Sb and As CL peak references would allow for the independent confirmation of the band alignment results. Utilizing equation 4.1 and the measured XPS spectra, $\Delta E_{V,Sb}$ ($\Delta E_{V,As}$) for $GaAs_{1-y}Sb_y$ samples with tunable Sb compositions were determined. For the GaAs and GaSb samples, the corresponding spectra were recorded.

The band gap (E_g) value of ALD deposited Al_2O_3 for each Sb composition was determined by using the energy-loss peak of O1s spectrum [18,19]. The binding energy was calculated from the difference in the total photoelectron energy minus the kinetic energy due to the loss in photoelectron energy by inelastic collision processes within the sample. The minimum inelastic loss is equal to the bandgap energy. The intersection of the linear extrapolation of the loss energy spectra and "zero level" shows the onset of inelastic losses. Thus, the bandgap energy is the energy difference between the O1s peak and the onset of inelastic spectra. The results shown in Figure 4.4(f) for 10 nm ALD Al_2O_3 is approximately 6.70 eV. All parameters and energies acquired from XPS measurements are listed in Table 4.1.

Based on the experimental data of ΔE_v , E_g, and theoretical bandgap of $GaAs_{1-y}Sb_y$ (y=0, 0.21, 0.34, 0.51, 1) [20] shaded white in Figure 4.5(a), the conduction band offset, ΔE_c as a function of tunable Sb composition can be expressed as :

$$\Delta E_c = E_{g,Al_2O_3} - E_{g,GaAsSb} - \Delta E_v \ . \qquad (4.2)$$

The band alignment parameters are summarized in Figure 4.5(a) as well as listed in Table 1. Figure 4.5(a) also visualizes the detailed band alignment parameters of $Al_2O_3/GaAs_{1-y}Sb_y$ for different Sb compositions. The electron affinity of GaAs and GaSb are 4.07 eV and 4.06 eV, respectively, so the electron affinities for different Sb compositions in GaAsSb are very similar. It implies that the major changes in band offset are contributed from the change in valence band as a function of Sb composition. It is interesting to note that the ΔE_v determined by both Sb and As CL spectra showed very similar results, shown in Table 4.1, thereby reinforcing the ΔE_v values for each As or Sb composition in $GaAs_{1-y}Sb_y$ acquired from XPS measurements. One can find that the ΔE_v and ΔE_c values are both larger than 2 eV for different Sb compositions. The higher band offset values are needed to suppress the leakage current between the dielectric and the GaAsSb channel material. The Anderson band alignment model

[22] was used to validate the ΔE_v trend as a function of Sb composition, shown in Figure 4.5(b). One can find that the Anderson band alignment model is in agreement with the measured ΔE_v

TABLE 1
BINDING ENERGY DIFFERENCE

Material and Interface	Binding Energy Difference	GaAs [eV]	$GaAs_{0.79}Sb_{0.21}$ [eV]	$GaAs_{0.66}Sb_{0.34}$ [eV]	$GaAs_{0.49}Sb_{0.51}$ [eV]	$GaAs_{0.38}Sb_{0.62}$ [eV]	GaSb [eV]
Thick Al_2O_3 (10 nm)	$E_{Al\ 2p}^{Al_2O_3} - E_{VBM}^{Al_2O_3}$	71.28	71.20	71.13	71.27	71.10	71.04
Interface (1.5 nm Al_2O_3 on GaAsSb, using Sb peak)	$E_{Sb\ 4d_{5/2}}^{GaAsSb} - E_{Al\ 2p}^{Al_2O_3}$	N.A.	-43.20	-43.16	-43.22	-43.17	-42.90
Interface (1.5 nm Al_2O_3 on GaAsSb, using As peak)	$E_{As\ 3d_{5/2}}^{GaAsSb} - E_{Al\ 2p}^{Al_2O_3}$	-33.72	-34.06	-34.07	-34.14	-34.07	N.A.
Thick GaAsSb (Epitaxy, using Sb peak)	$E_{Sb\ 4d_{5/2}}^{GaAsSb} - E_{VBM}^{GaAsSb}$	N.A.	31.66	31.71	31.93	31.78	32.37
Thick GaAsSb (Epitaxy, using As peak)	$E_{As\ 3d_{5/2}}^{GaAsSb} - E_{VBM}^{GaAsSb}$	40.92	40.73	40.74	41.04	40.91	N.A.
E_g (Al_2O_3)	From this work	6.74	6.75	6.71	6.70	6.69	6.71
E_g (GaAsSb)	$1.2y^2 - 1.9y + 1.43$, y = Sb composition	1.42	1.08	0.92	0.77	0.71	0.73
$\Delta E_v = (E_{VBM}^{Al_2O_3} - E_{VBM}^{GaAsSb})$ (estimated by Sb peak)	$(E_{Sb\ 4d_{5/2}}^{GaAsSb} - E_{VBM}^{GaAsSb}) - (E_{Al\ 2p}^{Al_2O_3} - E_{VBM}^{Al_2O_3}) - (E_{Sb\ 4d_{5/2}}^{GaAsSb} - E_{Al\ 2p}^{Al_2O_3})$	N.A.	3.65	3.74	3.88	3.86	4.23
$\Delta E_v = (E_{VBM}^{Al_2O_3} - E_{VBM}^{GaAsSb})$ (estimated by As peak)	$(E_{As\ 3d_{5/2}}^{GaAsSb} - E_{VBM}^{GaAsSb}) - (E_{Al\ 2p}^{Al_2O_3} - E_{VBM}^{Al_2O_3}) - (E_{As\ 3d_{5/2}}^{GaAsSb} - E_{Al\ 2p}^{Al_2O_3})$	3.36	3.59	3.69	3.91	3.88	N.A.
ΔE_c (estimated by Sb peak)	$E_g^{Al_2O_3} - E_g^{GaAsSb} - \Delta E_v$	N.A.	2.02	2.05	2.05	2.11	1.75
ΔE_c (estimated by As peak)	$E_g^{Al_2O_3} - E_g^{GaAsSb} - \Delta E_v$	1.95	2.08	2.10	2.02	2.09	N.A.

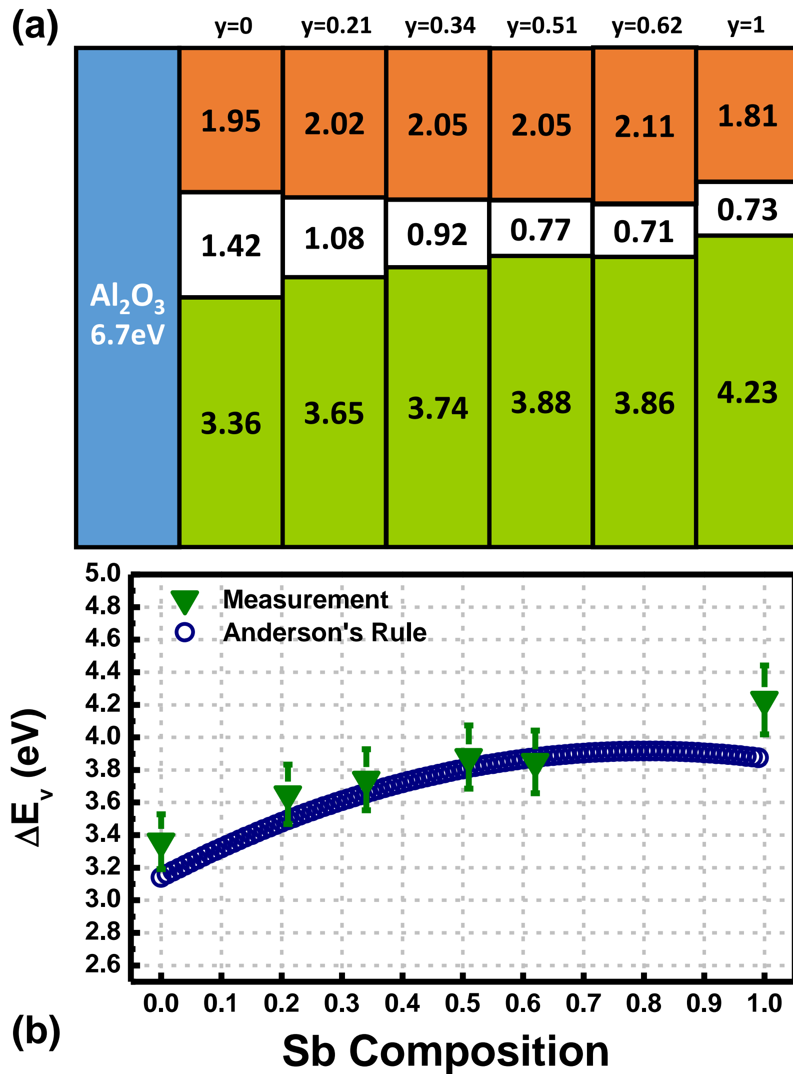

Figure 4.5. (a) Energy band parameters for A_2O_3 on $GaAs_{1-y}Sb_y$ with tunable Sb composition and (b) the measured valence band offset as a function of Sb composition along with the modeled band alignment results obtained using Anderson's rule.

values. There is a discrepancy between the model and the experimental results on GaSb compared with GaAsSb samples. In Anderson's model, the valence band offset between the Al_2O_3 and epitaxial GaAsSb materials are determined by considering (i) the electron affinity difference between those materials and (ii) the bandgap of each GaAsSb. Both the measured XPS data and Anderson's model predicted very similar conduction band offset value for GaAsSb samples. However, the presence of native oxides on GaSb sample, even after sulfur

passivation and Al_2O_3 layer deposition, affects the valence band offset and the resulting conduction band offset due to the differences in GaSb bandgap and the measured valence band offset. Thus, we believe that due to difficulty in cleaning and passivation of GaSb surface, there is a difference in conduction band offset between Al_2O_3 and GaSb sample. Combining the benefits of the nature of the band alignments between GaAsSb/InGaAs and the higher energy barrier of Al_2O_3/GaAsSb, Al_2O_3 has been found to be a promising high-κ gate dielectric on mixed As-Sb based GaAsSb materials. A valence band offset of > 2 eV for all Sb compositions, indicating the potential of utilizing Al_2O_3 on $GaAs_{1-y}Sb_y$ ($0 \leq y \leq 1$) for p-type metal-oxide-semiconductor device applications. Moreover, Al_2O_3 showed a conduction band offset of ~ 2 eV on $GaAs_{1-y}Sb_y$, suggesting Al_2O_3 dielectric can also be used for n-type MOS device applications. Therefore, the surface passivation and the detailed band alignment analysis of Al_2O_3 on tunable Sb composition, $GaAs_{1-y}Sb_y$, provides a pathway to utilize $GaAs_{1-y}Sb_y$ materials in multifunctional device applications.

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Chapter 5

Operation Principle and Performance of Ge/InGaAs TFETs

In *Chapter 2,* we investigated the criteria for high tunneling probability and steep SS in TFETs. In *Chapter 3&4*, we further discussed the superior properties of mixed As/Sb system at the material level to obtain these criteria. In this chapter, we are going to investigate the operation principles of TFETs so that we can fully leverage the advantages of chosen material systems for ultra-low voltage devices. In addition, we will introduce another novel alternative material system (strained Ge/InGaAs) and evaluate the performance of TFETs using TCAD simulations and benchmark their performance with mixed As/Sb-based TFET devices.

5.1. Analytic Model of TFETs

Proceeding from the derivation in Eq. 2.29, we can apply this result to the Landauer equation so that the drain current could be expressed as follows [1]:

$$I_{ds} = \frac{2q}{h}\int_{E_0}^{V_0}(f_s - f_s)T(E)dE$$

$$= \frac{2q}{h}\int_{E_0}^{V_0}\left[\frac{1}{1+e^{\frac{(E_1-E)}{kT}}} - \frac{1}{1+e^{\frac{(E_2-E)}{kT}}}\right]$$

$$\times\, exp\left\{-\frac{4\lambda\sqrt{2m}}{\pi\hbar}\left[\sqrt{E} - \sqrt{V_0 - E}\,\sin^{-1}\sqrt{E/V_0}\right]\right\}dE \quad (5.1)$$

where E_0 is valance band of source, E_1 is the Fermi level of source, E_2 is the Fermi level of drain, V_0 is the energy potential of channel, and E_2=E_1+qV_{ds}. For the case, V_{ds} > V_{gs}, the channel potential are controlled by the gate voltage so that V_0=E_0+qV_{gs}. On the other hand, in high V_{ds}, V_0 is reduced due to the present of inversion charge layer in channel surface resulting

$V_0 = E_0 + q\ (V_{gs} - Q_{inv}/C_{ox})$. The inversion charge ($Q_{inv}$), can be calculated from following equations [1,2]:

$$Q_{inv} = \frac{4kT\varepsilon_s}{qt_s}\beta tan\beta, \quad (5.2)$$

$$\frac{q(V_{gs}-V_{ds}-d_1)}{2kT} - ln\left[\frac{2}{t_s}\sqrt{\frac{2\varepsilon_s kT}{q^2 N_c}}\right] = ln\beta - ln[cos\beta] + \frac{2\varepsilon_s t_i}{\varepsilon_i t_s}\beta tan\beta, \quad (5.3)$$

where N_c is the effective density of state of the conduction band and d_1 is the source degeneracy. By using these continuous current characteristics, we can examine the drain current of a TFET. There are several works to further revise the current model discussed in these references [3-7], however, Eq. 5.1-5.3 will provide a reasonably qualitative estimation of TFET characteristics.

5.2. Transfer Characteristics of TFETs (I_{ds}-V_{gs})

Figure 5.1 shows the simulated transfer characteristics of DG-TFET at V_{DS} = 1.0V [8, 9]. In general, we can separate the transfer characteristics of TFET into three domains: (i) OFF-state, (ii) Subthreshold, and (iii) ON-state.

In OFF-state, the tunneling window at source/channel is blocked and the device current is negligible. However, in reality, leakage currents are dominant in this regime. There are three major leakage paths within this voltage domain [10]. The first component is the direct tunneling from source to drain which makes TFETs sensitive to channel length. The second component is the thermionic emission from source to drain. Normally the thermionic leakage current is dominated in OFF-state [11] and could be suppressed by using large bandgap materials. The

third component is due to the ambipolar behavior of TFET, which will be discussed in later in this chapter.

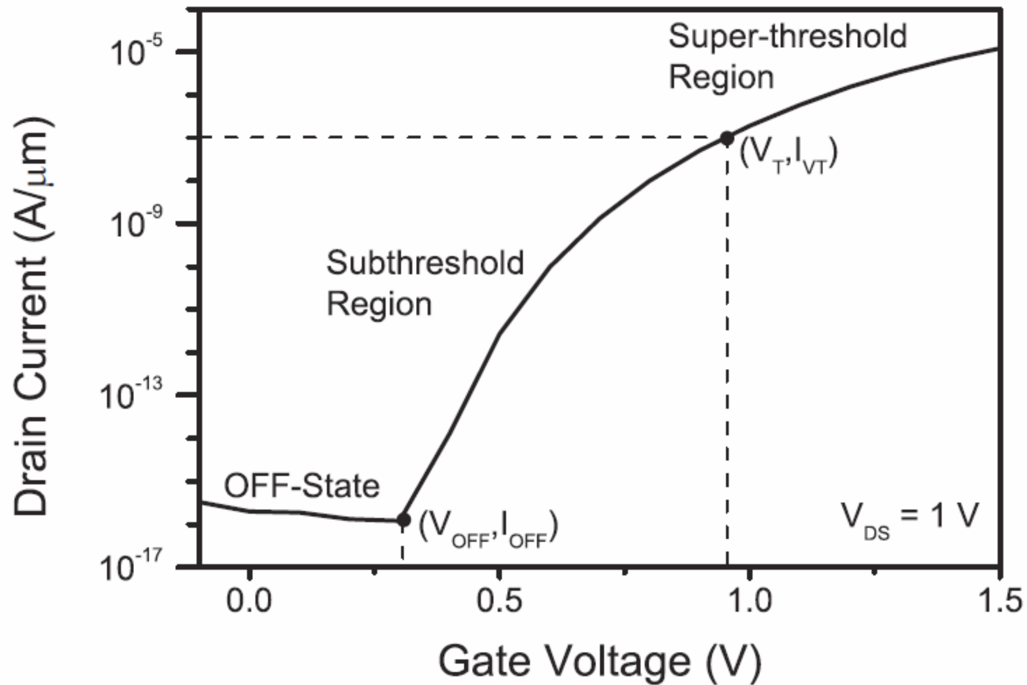

Figure 5.1: Simulated transfer characteristics of the DGTFET at VDS = 1.0 V [8,9].

In the subthreshold region, current increases rapidly due to applied V_{gs} lowered down the conduction band of channel and widens the tunneling window. Unlike a conventional MOSFET, the SS of TFET is gate-voltage dependent due to the complex integral from different factors shown in Eq. 2.15. Hence, point SS is used to replace the traditional average SS, and can define as follows:

$$SS_{point}\Big|_{V_{gs}} = \left(\frac{dV_{gs}}{dlog(I_{ds})}\right)_{V_{gs}}. \tag{5.4}$$

A good TFET should outperform a MOSFET in terms of lower point SS (SS_{point}), for several decades of drain current at lower gate voltage.

In ON-state, the tunneling current increases due to decrease in tunneling distance and increase in tunneling window while increasing gate voltage. However, in the case of high gate voltage operation, especially for $V_{gs} > V_{ds}$, the increment of drain current with increasing V_{gs} becomes lower than the increment at low V_{gs} regime due to channel potential pinning. The formation of the inversion layer effectively shorts the device drain to channel, leading to similar potential in both channel and drain regions. As a result, the channel potential is controlled by V_{ds}, not by V_{gs}. Therefore, the energy band in channel doesn't significantly change with a further increase in gate voltage. In other words, although the number of electrons and energy states increases, the tunneling lengths associated with these energy states are very large and this leads to their negligible contribution to tunneling current. On the other hand, for $V_{ds} < V_{gs}$, the potential of channel is solely dependent on gate voltage leading to the increase of drain current.

5.3. Output Characteristics of TFET (I_{ds}-V_{ds})

Figure 5.2 shows the I_{ds}-V_{ds} characteristics of DG-TFET [1]. The output characteristics can be separated into two parts: linear and saturation regimes. To understand the fundamental difference between linear and saturation behavior, we have to revisit aforementioned "potential pinning" (or debiasing) effect. When $V_{ds} < V_{gs}$, the inversion layer forms and screens (or debiases) gate voltage. The conduction band of channel is pinned by the drain voltage as shown in Figure 5.3 [12]. Thus, the full V_{ds} drops across the tunneling junction because of the negligible channel resistance. Therefore, I_{ds} increases with ramping V_{ds} in linear region. On the other hand, in the case of $V_{ds}>V_{gs}$, pinch-off occurs in TFET same as MOSFET. The inversion layer/region is eliminated around the channel/drain interface and depletion region is formed, as shown in Figure 5.3. The lateral electric field from the drain no longer penetrates into the

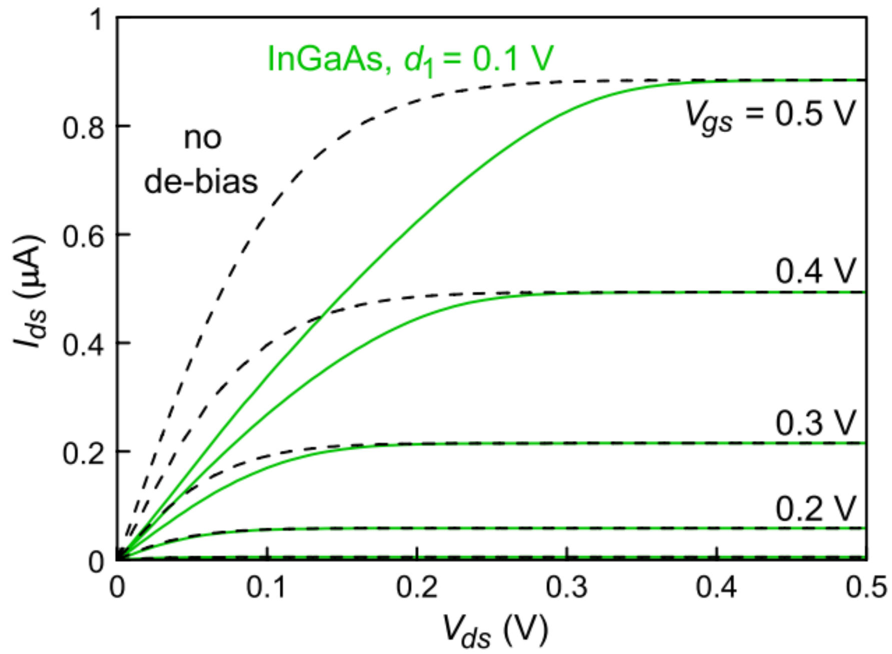

Figure 5.2: Model generated I_{ds}-V_{ds} characteristics for the different debiasing (channel potential pinning) conditions [1].

tunneling junction, and hence the tunnel junction remains unaffected by further increase in

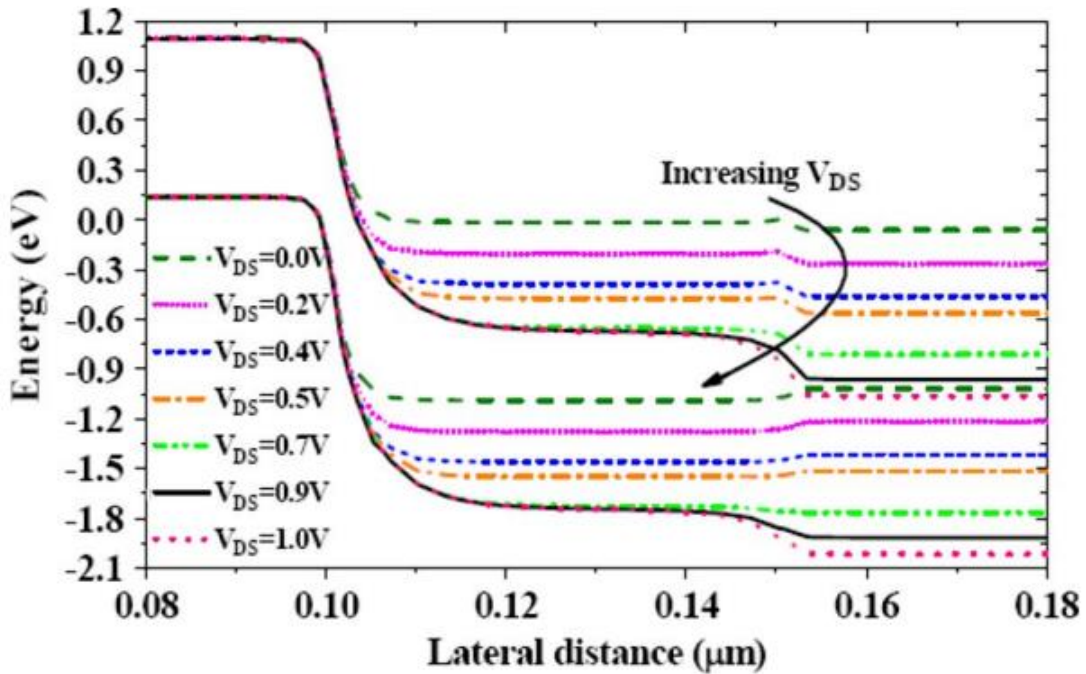

Figure 5.3: Simulated energy band diagram at a distance of 1 nm below the top oxide–semiconductor interface for different VDS corresponding to VGT = 0.5 V for the DG n-TFET [12].

drain voltage. This condition results in drain current saturation and high output resistance. The potential pinning effect (or debiasing) only reduces the current in linear region and push saturation voltage (V_{dsat}) in higher without impacting the maximum drain current (shown in Figure 5.2) and hence, is called "late saturation". Late saturation effect can severely degrade the transconductance and switching speed of TFET and hence in turn affect the performance of analog and digital circuits.

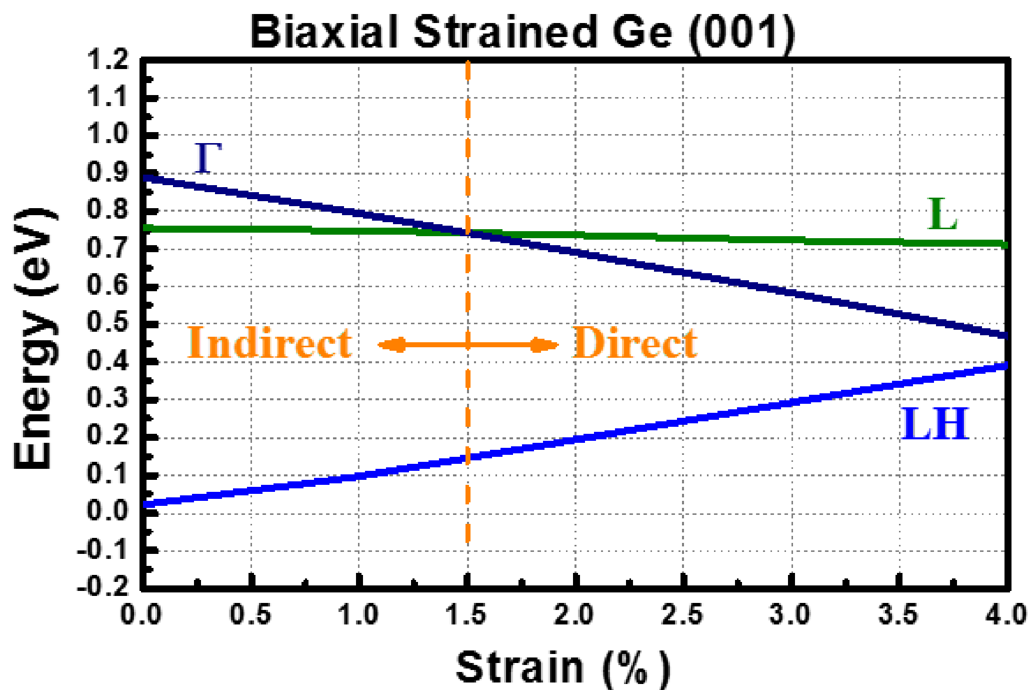

Figure 5.4: Calculated conduction and valence band shifts with in-plane biaxial tensile strained Ge (001).

5.4. Ge/$In_xGa_{1-x}As$ Heterojunction

Despite the high compatibility to Si platform, group IV TFETs were not under spotlight due to its indirect bandgap in nature. Of particular interest for future H-TFET architectures, biaxial tensile-strained Ge (ε-Ge) epitaxially grown on III-V template [13] provides a method for achieving high ON-state current (I_{ON}) via the conversion of Ge from an indirect-to-direct band

gap semiconductor, thus resulting in an enhanced tunneling probability. The energy separation of conduction band valleys (L- and Γ- valley) is ~130 meV for pseudo bandgap Ge material and this separation can be modulated by incorporating the bi-axial tensile strain through III-V strain template. Staggered gap band alignment is the core of ε-Ge/$In_xGa_{1-x}As$ H-TFETs. The effect of (i) quantization and (ii) the heterojunction band alignment were included in our TFET simulation model. For ε-Ge /$In_xGa_{1-x}As$ heterointerface, we employed 30×30 k·p model [14] to the energy band structure of in-plane biaxial tensile strained Ge (001). Figure 5.4 shows the calculated conduction and valence band shifts with in-plane biaxial tensile strained employed in Ge (001). With increased tensile strain, the lowest conduction band energy in L- and Γ-valley crossed over at about 1.5% strain, which is an excellent agreement with the previous reported value [15]. However, high tensile strain (>1.5%) will provide not only the smaller band gap but also the direct bandgap in nature. The advantage for direct band gap Ge was to enhance the tunneling probability by eliminating the phonon from the tunneling processes, as discussed earlier. On the other hand, $In_xGa_{1-x}As$ material is a direct bandgap material system for any composition of In. As a result, ε-Ge /$In_xGa_{1-x}As$ heterojunction system can provide Γ-

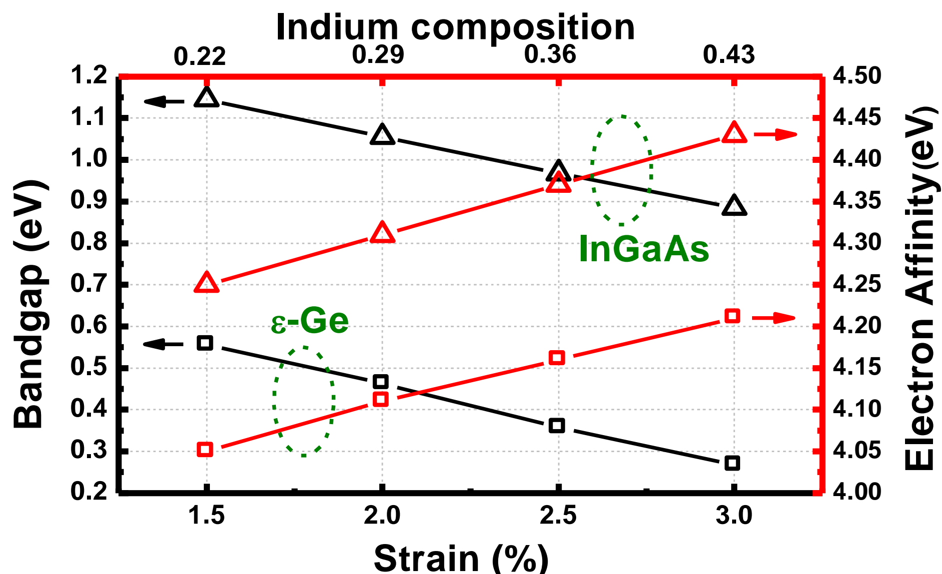

Figure 5.5: Calculated direct bandgaps (black) and electron affinity (red) for Ge (squares) and InGaAs (triangles).

Γ BTBT from ε-Ge to $In_xGa_{1-x}As$, which was originally L-Γ BTBT process. In this work, we have considered the highly tensile strained systems (>1.5%) in our model. We have also used the bandgap relation $E_g = 1.456 - 1.5x + 0.4x^2$ as a function of gallium (Ga) alloy composition in InGaAs, and the electron affinity was estimated using Vegard's law, $\chi_{In_xGa_{1-x}As} = x \cdot \chi_{InAs} + (1-x) \cdot \chi_{GaAs}$ [16]. Figure 5.5 shows the calculated direct bandgaps of Ge and InGaAs, and electron affinity for both materials as a function of strain.

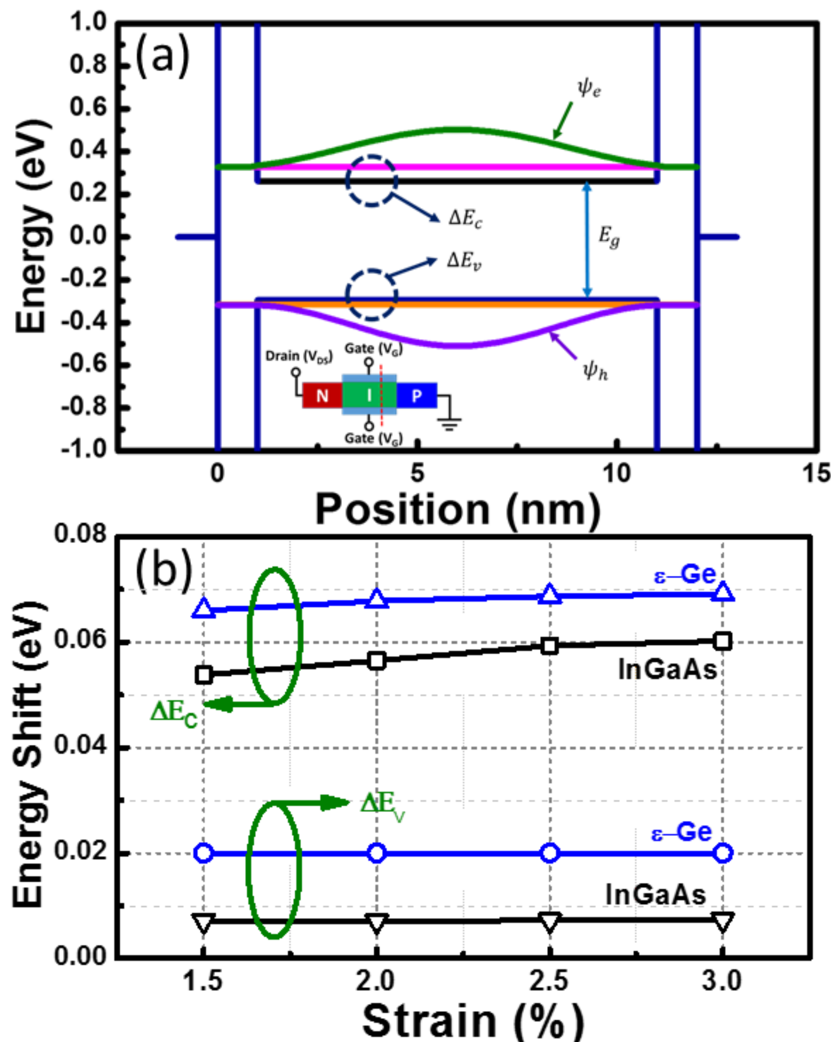

Figure 5.6: (a) Band diagram of $SiO_2/Ge/SiO_2$ (1 nm/10 nm/1 nm) for quantum confinement simulation. (b) Valance band shift, ΔE_v and conduction shift, ΔEc as a function of strain in Ge and InGaAs channel.

TABLE 5.1
SIMULATION PARAMETERS

Parameter Description	Value Used	Parameter Description	Value Used
Gate Length (L_g)	40 [nm]	Channel Length (L_c)	40 [nm]
Body Thickness (t_b)	10 [nm]	EOT	1 [nm]
Doping, N_{source}=N_{drain}	1×10^{19} [cm-3]	Source/Drain Length (L_s,L_D)	30 [nm]
A^1_{InGsAs}	0.0476 [eV]	C^1_{InGaAS}	0.0032 [eV]
A^2_{Ge}	8.15[eV]	C^2_{Ge}	2.03[eV]
Germanium Strain (%)	m_{r_dir} (m_0)	A_{dir} ($cm^{-3}s^{-1}$)	B_{dir} (MV/cm)
1.5	0.025	1.67e20	5.25
2.0	0.024	1.69e20	4.85
2.5	0.024	1.72e20	4.49
3.0	0.023	1.73e20	4.14
Germanium Strain (%)	$m_{c,ip}$ (m_0)	$m_{c,op}$ (m_0)	$m_{v,op}$ (m_0)
1.5	0.043	0.033	0.037
2.0	0.042	0.027	0.037
2.5	0.041	0.022	0.035
3.0	0.040	0.017	0.035
Germanium Strain (%), Indium Composition (%)	Electron affinity (eV) (Ge, InGaAs)	Bandgap (eV) (Ge, InGaAs)	
1.5, 22	4.05, 4.25	0.56, 1.15	
2.0, 29	4.11, 4.31	0.46, 1.06	
2.5, 36	4.16, 4.37	0.36, 0.97	
3.0, 43	4.21, 4.43	0.27, 0.89	

1. Pre-factors for the Jain-Roulston band gap narrowing model for n-type $In_xGa_{1-x}As$ [20].
2. Pre-factors for the Jain-Roulston band gap narrowing model for Γ-valley Ge [21].
3. Effective mass value, A_{dir} and B_{dir} are extracted from [18].

To simulate improved channel control, a long-channel, double-gated TFET configuration was utilized in conjunction with a low effective oxide thickness. Both conduction and valence band edge shifted due to the quantum confinement effect in this structure. The influence of quantum confinement effects, shown in Figure 5.6(a) using Nextnano3, on device performance were considered [17]. This Nextnano3 simulator solve Schrödinger-Poisson equation in 1D with SiO_2/Ge/SiO_2 structure for 1.5% strain and a device band diagram along a 1D cut perpendicular to gate electrode is shown in the inset of Figure 5.6(a). The new ground state energies created by quantization effect are located below and above the original band edges (shown in orange and pink color), where ΔE_c and ΔE_v are the conduction and valence band shift, respectively. These energy shifts due to quantization effect further changed the effective bandgap, electron affinity, and band alignments. For strained Ge, the effective mass also changed with different amount of strain. Moreover, with increasing strain, the ΔE_c and ΔE_v are

also increased further (shown in Figure 5.6(b)) due to the decrease in out-of-plane [001] electron effective mass ($m_{c,op}$). The change in out-of-plane [001] effective mass as a function of strain amount used in simulation were extracted from Ref. 18 and also listed in Table 5.1.

Utilizing two main mechanisms (i.e., quantization and strain effect) for band alignment calculation, the schematics of p-type and n-type strain-engineered Ge/$In_xGa_{1-x}As$ H-TFETs studied in this work are shown in Figure 5.7(a) and 5.7(b), respectively. The band gap narrowing (BGN) effect was also considered in source/drain regions of these tunnel FET structures. Therefore, the final values of electron affinity as well as bandgaps of Ge and InGaAs used in this work are also listed in Table 5.1. Figure 5.7 shows the simulated band diagrams of the strain-engineered Ge/$In_xGa_{1-x}As$ H-TFETs studied in this work, including (i) a p-type n^+-$In_xGa_{1-x}As$/i-Ge/p^+-Ge H-TFET (Figure 5.7(a)), and (ii) an n-type p^+-Ge/i-$In_xGa_{1-x}As$/n^+-

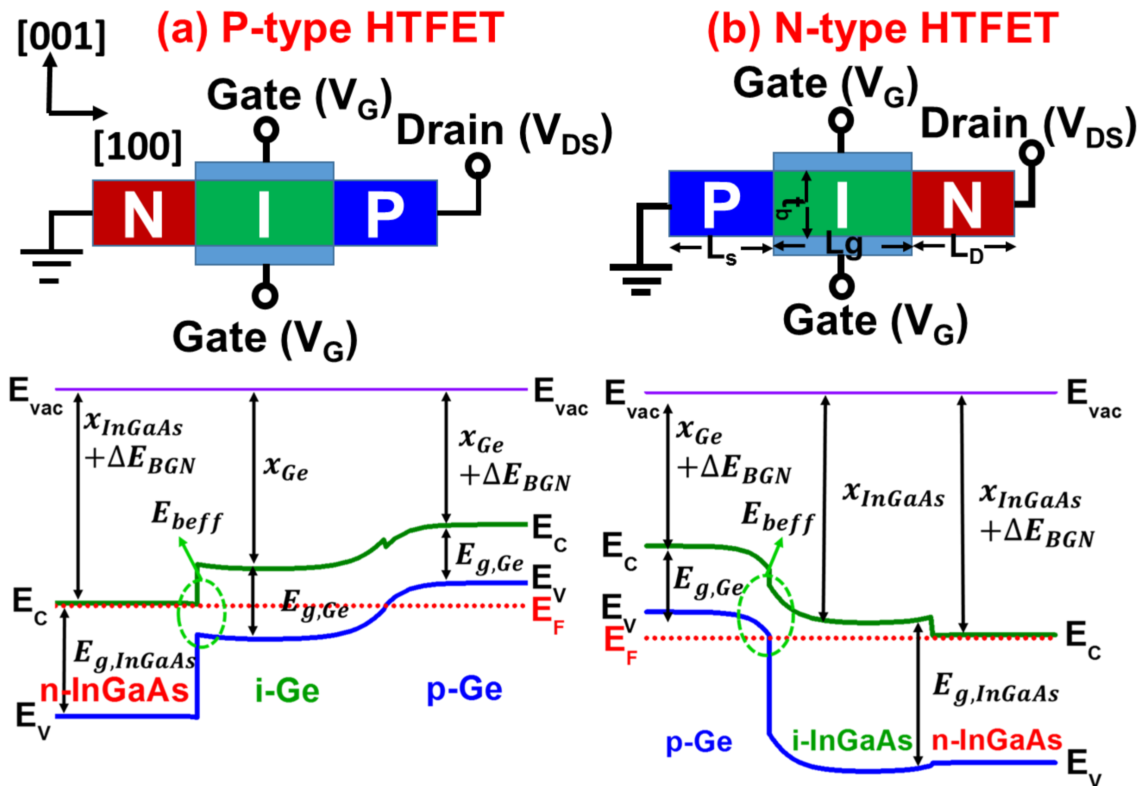

Figure 5.7: Structural models and simulated schematic band diagrams used in the numerical device simulation of (a) p-type and (b) n-type heterojunction (ε-Ge/$In_xGa_{1-x}As$) TFETs.

$In_xGa_{1-x}As$ H-TFET (Figure 5.7(b)). The selection in channel material for each device efficiently leverages the increased carrier mobilities of both materials (i-$In_xGa_{1-x}As$ for n-type and i-Ge for p-type structures). One can find from Figure 5.7, the band diagrams exhibited a staggered (or type-II) band alignment, thereby assisting in reduction of E_{beff} and increase in tunneling probability and hence ON-current of a H-TFET. Moreover, the presence of high-strain (≥ 1.5%) within the ε-Ge layers is expected to convert the pseudo bandgap Ge to a direct-gap semiconductor [18], further enhancing the Γ-Γ tunneling probability from ε-Ge to $In_xGa_{1-x}As$.

5.5. Simulation Model and Parameters

For tensile strained direct bandgap Ge, the direct BTBT model determining the generation rate per unit volume is expressed by [19]:

$$G = A_{dir}(F)^P \exp\left(-\frac{B_{dir}}{F}\right), \tag{5.4}$$

where F (volt/cm) is the electric field, P = 2 are for the direct BTBT transition. Pre-factors A_{dir} and B_{dir} are calculated from Ref.13. In the case of BGN, Jain-Roulston model was used and expressed as [20], [21]:

$$\Delta E_{BGN,InGaAs} = A_{InGaAs}\left(\frac{N}{18}\right)^{1/3} + C_{InGaAs}\left(\frac{\mathrm{N}}{18}\right)^{1/4}, \tag{5.5}$$

$$\Delta E_{BGN,Ge} = A_{Ge}\left(\frac{N}{18}\right)^{1/4} + C_{Ge}\left(\frac{\mathrm{N}}{18}\right)^{1/2}, \tag{5.6}$$

where, A and C are pre-factors. In this work, we have considered double-gated TFET structures with ultra-thin body to gain the ability of gate control. The channel length (L_c) was equal to the gate length (L_g) of the device and the channel was entirely covered by the gate. Symmetrically doped source and drain regions were utilized at first in our device simulation that helped us to

understand the unipolar or ambipolar behavior of a TFET device structure. Synopsys' Sentaurus TCAD software [22] was used to simulate the double-gated p-i-n TFET structures using a Fermi-Dirac statistics model, a drift-diffusion carrier transport model, a doping-dependent mobility model [23], Auger and Shockley-Read-Hall generation/recombination models, a doping-dependent band-gap-narrow model, strained density of state mass [24], and the dynamic non-local path BTBT model at 300 K. Table 5.1 summarizes all model parameters used in the TFET device simulation.

5.6. Band Alignments and Effective Barrier Heights

The most important design parameter for a tunnel FET device is the effective tunnel barrier height that control the tunneling probability and hence the I_{ON} of the device. Thus, the effective

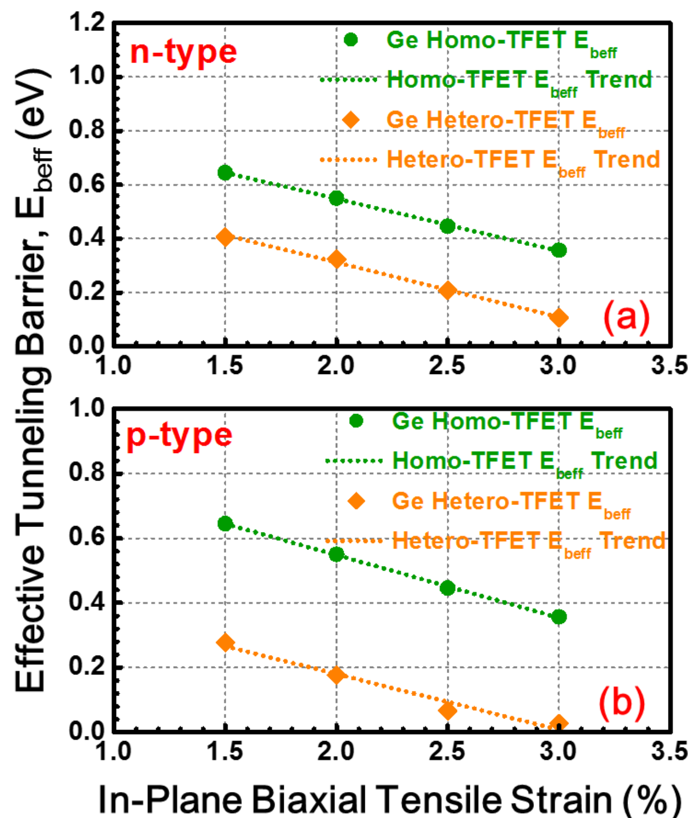

Figure 5.8: Strain-induced reduction of the effective tunneling barrier height for (a) n-type and (b) p-type homojunction (ε-Ge) and heterojunction (ε-Ge/$In_xGa_{1-x}As$) TFETs.

barrier height (E_{beff}) can be expressed by: $E_{beff} = (\chi_{InGaAs} + \Delta E_{BGN,InGaAs}) - (\chi_{Ge} + E_{g,Ge})$ for n-type, and $E_{beff} = (\chi_{InGaAs}) - (\chi_{Ge} + E_{g,Ge} + \Delta E_{BGN,Ge})$ for p-type, shown in Figure 5.7, respectively. Figure 5.8 shows E_{beff} as a function of increasing biaxial tensile strain for n-type and p-type TFETs. Both ε-Ge-based TFET architectures benefited from strain-induced lowering of E_{beff}, however, H-TFETs experienced further reduction in E_{beff} due to a larger intrinsic band discontinuity at the ε-Ge/$In_xGa_{1-x}As$ heterointerface [13]. This band discontinuity can be explained as a result of increasing In composition into the $In_xGa_{1-x}As$ layers translating into (i) increased Ge strain, (ii) a lowering of both ε-Ge and $In_xGa_{1-x}As$ band gaps, and (iii) a corresponding increase in the electron affinity of both materials. As a result, H-TFETs show superior modulation of E_{beff} through bandgap and strain-engineering. Moreover, p-type H-TFETs further benefited from doping-induced BGN in the n-$In_xGa_{1-x}As$ source. The unequal shift of the band edges in heavily-doped $In_xGa_{1-x}As$, corresponds to a reduction in E_{beff} in p-type H-TFETs that is absent in n-type structure due to the intrinsic nature of the $In_xGa_{1-x}As$ at the source-channel heterojunction.

5.7. I-V Characteristics of Strain Ge-InGaAs TFETs

Figure 5.9(a) and 5.9(b) show the simulated I_{DS}-V_{GS} characteristics as a function of overdrive voltage, $V_{GS} - V_{OFF}$, for the n-type and p-type homo- and H-TFETs under 2% biaxial strain, respectively. The OFF-state leakage current is matched at 200 pA/μm for all devices at V_{OFF} voltage. Both n- and p-type H-TFETs demonstrated superior I_{ON} over similarly-strained homo-TFETs. The substantial enhancement in I_{ON} was attributed due to the smaller E_{beff} at the source-channel heterointerface in both H-TFETs. Further enhancement can also be expected for n-type H-TFETs due to the improved electron mobility in the i-$In_xGa_{1-x}As$ channel as compared to the strained i-Ge channel. The E_{beff} was found to be 0.55 eV for both homo-TFETs under 2% strain,

whereas n- and p-type H-TFETs exhibited E_{beff} of 0.32 eV and 0.18 eV, respectively, resulting in an enhanced tunneling probability. Also shown in Figure 5.9 (c) and 5.9 (d) are the SS characteristics for n- and p-type homo- and H-TFETs, respectively. The SS of both structures

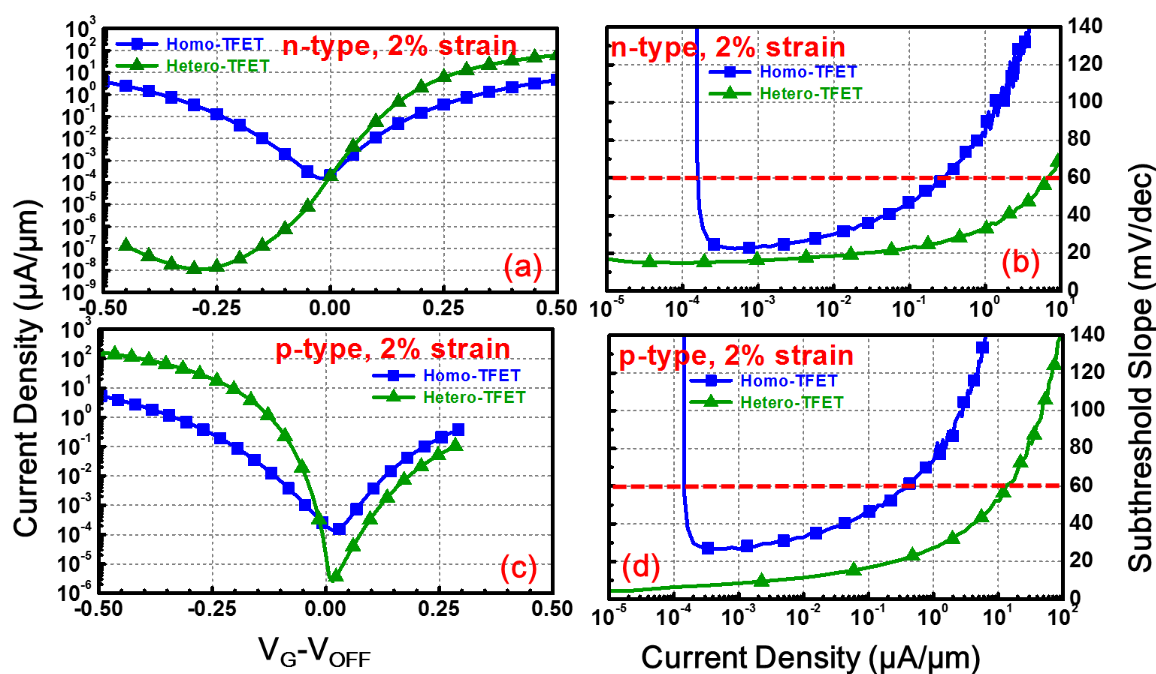

Figure 5.9: Current-voltage and subthreshold swing characteristics of the (a)-(b) n-type and (c)-(d) p-type homojunction (ε-Ge) and heterojunction (ε-Ge/$In_xGa_{1-x}As$) TFETs.

were below 60 mV/decade, which is the limitation of conventional MOSFET devices. Moreover, the SS depends on the device structure and the channel passivation. Furthermore, p-type H-TFETs exhibited enhanced SS reduction due to the lower E_{beff}, compared to n-type H-TFETs.

5.8. Ambipolar Behavior of H-TFETs

N-type H-TFETs exhibited significantly reduced I_{OFF} in comparison with both homo-TFETs and p-type H-TFETs. This reduction in I_{OFF} is due to the increased drain-channel tunneling barrier at the i-$In_xGa_{1-x}As$/n$^+$-$In_xGa_{1-x}As$ interface in n-type TFETs (higher bandgap for $In_xGa_{1-x}As$), thereby suppressing the ambipolar behavior of the symmetrically-doped devices.

Conversely, the i-Ge/p^{+}-Ge channel-drain interface in p-type H-TFETs mirrors the ε-Ge homo-TFET structure, thus indicating that the dominate leakage mechanism in p-type H-TFETs results from the ambipolar behavior of the device during the OFF-state. Moreover, though strain-modulation reduces the ε-Ge band gap and reduces E_{beff} between the source and channel, it can be clearly seen from Figure 5.9 (a) and 5.9 (c) that the lowering of E_{beff} for ε-Ge-based homo-TFETs drastically reduced I_{ON}/I_{OFF} ratio due to the ambipolar characteristic, as discussed above.

Asymmetrically doped source and drain were commonly used for suppression of ambipolar current in a tunnel FET structure [25]. Lowered doping concentration of drain enlarged the tunnel barrier width and reduced electric field at channel-drain heterointerface. The tunneling probability decreased exponentially with increasing tunnel barrier width. The I_{ON} depends on the BTBT current at the source-drain heterointerface, so it was less important to change in drain doping concentration. Figure 5.10 shows the drain current with two different drain doping concentrations (10^{19} and 10^{18} cm^{-3}) with 2.0% strain in a p-type H-TFET. One can find that the I_{OFF} reduced as the doping concentration decreased and meanwhile the I_{ON} still remains the same, which is an agreement with the mechanism described here.

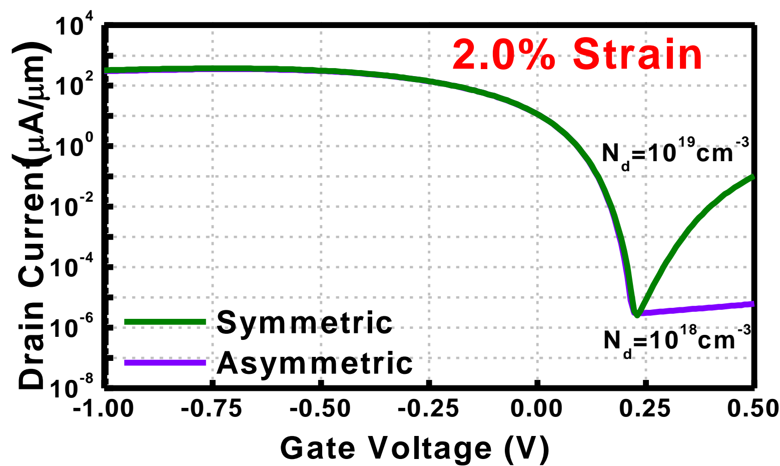

Figure 5.10: Drain current as a function of gate voltage with two different drain doping concentrations.

5.9. Performance Evaluation with Different Strain

Figure 5.11 shows I_{ON} as a function of increasing biaxial tensile strain for n-type and p-type TFETs. Both homo- and hetero- junction ε-Ge-based TFET architectures benefited from enhanced strain, however, H-TFETs have significant reduction of effective barrier by staggered gap alignment. Consequently, n-type H-TFETs showed a stronger dependence of I_{ON} on strain,

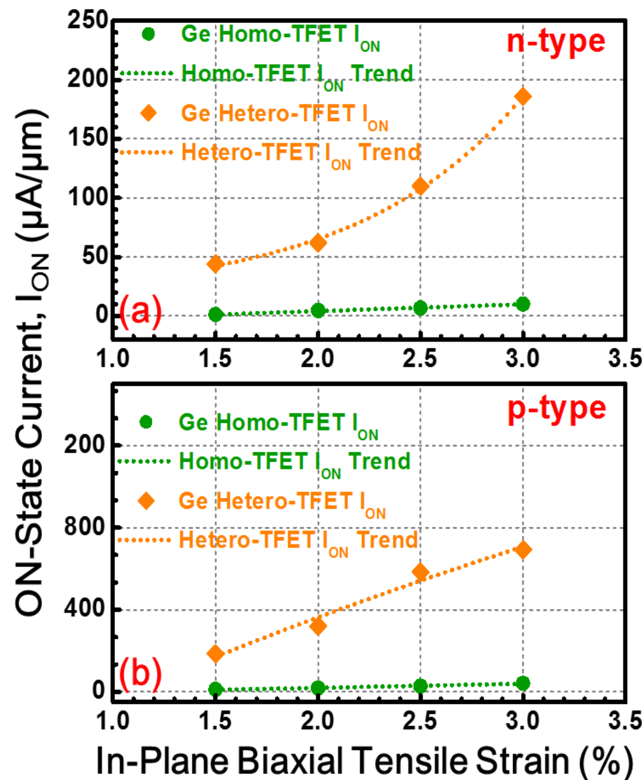

Figure 5.11: Strain-induced enhancement of ON-state current for n-type and p-type homojunction (ε-Ge) and heterojunction (ε-Ge/InxGa1-xAs) TFETs.

as shown in Figure 5.11, revealing an 18.6× increase in I_{ON} for n-type H-TFETs at 3% tensile strain, whereas similarly-strained p-type H-TFETs observed a 16.9× increase in I_{ON}. In summary, we have evaluated the band structure, subthreshold swing characteristics, modulation of the effective tunneling barrier height, and the electrical performance of ε-Ge/$In_xGa_{1-x}As$ n- and p-type H-TFETs for the first time using numerical device simulation. N-type H-TFETs demonstrated a substantial reduction in leakage current due to the higher

tunneling barrier at the channel-drain interface. Both n- and p-type H-TFETs exhibited a significant enhancement in I_{ON} (18.6× and 16.9×, respectively, at 3% strain) and which was attributed to both increased in strain and band discontinuities at the ε-Ge/$In_xGa_{1-x}As$ source-channel interface. Furthermore, the p-type H-TFETs also benefited from a reduced conduction band offset as a result of doping-induced band-gap-narrowing, thereby further reducing E_{beff}. In addition, point and average SS was reduced for both H-TFETs as compared to ε-Ge homo-TFETs. Therefore, the Ge-based H-TFETs show a great promise for low-power complementary TFET logic due to their ability to leverage improved channel carrier mobilities and a tunable E_{beff}, as recently demonstrated by strain-engineering and composition modulation [13], to achieve high drive current and low leakage TFET devices.

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Chapter 6

An Energy-Efficient Tensile-Strained Ge/InGaAs TFET 7T SRAM Cell Architecture for Ultra-low Voltage Applications

In previous chapters, the design of energy-efficient TFETs was comprehensively investigated. The results agreed that TFETs are potential devices for ultra-low voltage applications. To further reduce power dissipation for IoT applications, performance of TFETs based circuits must be evaluated. Currently, static random-access memory (SRAM) is heavily utilized as on-chip microprocessor cache, and as a consequence, occupies greater than 70% of total die area [1-2]. Accordingly, the performance optimization of each SRAM cell could lead to considerable improvements in microprocessor power consumption. The intrinsic steep *SS* characteristics of TFET devices would permit low voltage operation while concurrently leveraging the uni-directionality of TFETs to reduce leakage current and hence OFF-state power dissipation, while maintaining the I_{ON} current.

6.1. Simulation Methodology of SRAM

Figure 6.1 outlines the simulation methodology used to investigate the performance of the proposed ε-Ge/InGaAs TFET SRAM architecture. Building on our previously reported results [11-12], this work utilizes work function-tuning to realize a fixed OFF-state leakage current, I_{OFF}, of 100 pA/μm at a $|V_{DS}|$ of 0.3 V. Due to the lack of a conventional TFET model for use in TCAD circuit-level simulation, we have implemented a Verilog-A device model as prescribed by several other researchers [3]-[9]. The Verilog-A model used herein is comprised

of three look-up tables tabulating the I_{DS} (V_{GS}, V_{DS}), C_{gs} (V_{GS}, V_{DS}), and C_{gd} (V_{GS}, V_{DS}) characteristics of the ε-Ge/InGaAs TFET devices within the working bias range invested in this work (*i.e.*, -0.6 V < V_{DS} and V_{GS} < 0.6 V). Using this custom Verilog-A model, static and dynamic circuit analysis was then performed *via* HSpice circuit simulator.

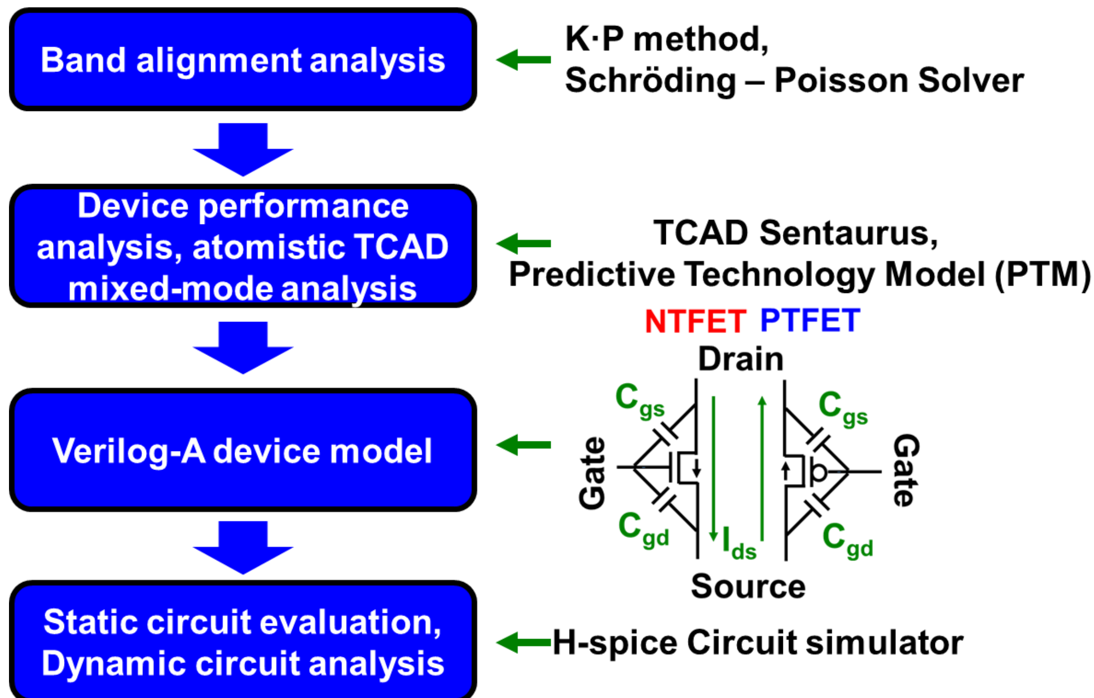

Figure 6.1: Flow chart outlining the simulation methodology used in the design and modeling of the ε-Ge/$In_xGa_{1-x}As$ TFET-based memory circuit.

6.2. TFET and MOSFET Operating Characteristics

In this work, tunable tensile-strained Ge/$In_xGa_{1-x}As$ heterojunction TFETs (H-TFETs) were used to investigate the performance impact of strain-state on SRAM operation in the sub-0.5 V supply voltage regime. Moreover, these results were benchmarked against matching Si CMOS-based SRAM cells (implemented using the 45 nm high-performance CMOS model provided by NIMO) in order to demonstrate the viability of the proposed SRAM design under continued supply voltage scaling [13]. Figure 6.2 highlights the simulated *p*- and *n*-type TFET

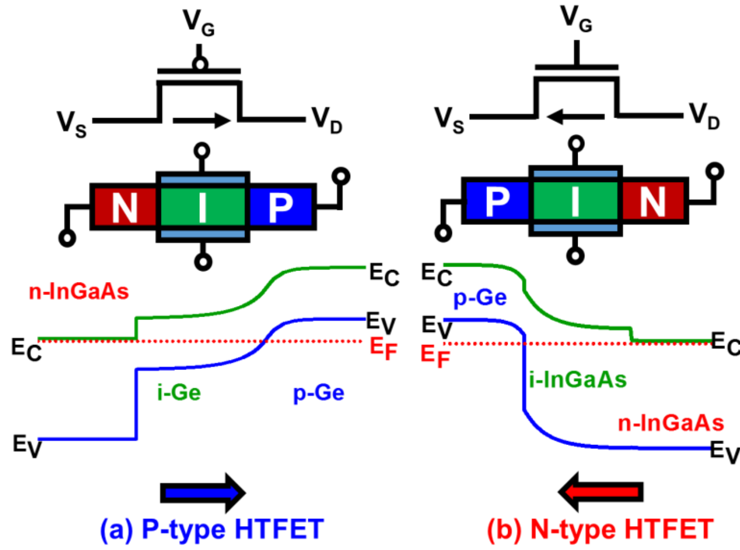

Figure 6.2 Simulated band alignments and circuit representations of (a) a *p*-type TFET (*n*-InGaAs/*i*-Ge/*p*-Ge) and (b) an *n*-type TFET (*p*-Ge/*i*-InGaAs/*n*-InGaAs).

energy band diagrams, device structures, and circuit schematic symbols used in this work. Correspondingly, Figure 6.3 shows the I_{DS}-V_{GS} characteristics ($|V_{DS}|$ = 0.3 V) for the *p*- and *n*-type ε-Ge/$In_xGa_{1-x}As$ H-TFETs using 1.5% and 3.0% ε-Ge strain-states. Also shown in Figure 6.3 are the transfer characteristics for the 45 nm *n*- and *p*-MOSFETs as well as the thermionic emission limit to MOSFET *SS*, *i.e.*, 60 mV/decade at 300 K. As previously discussed, the gate

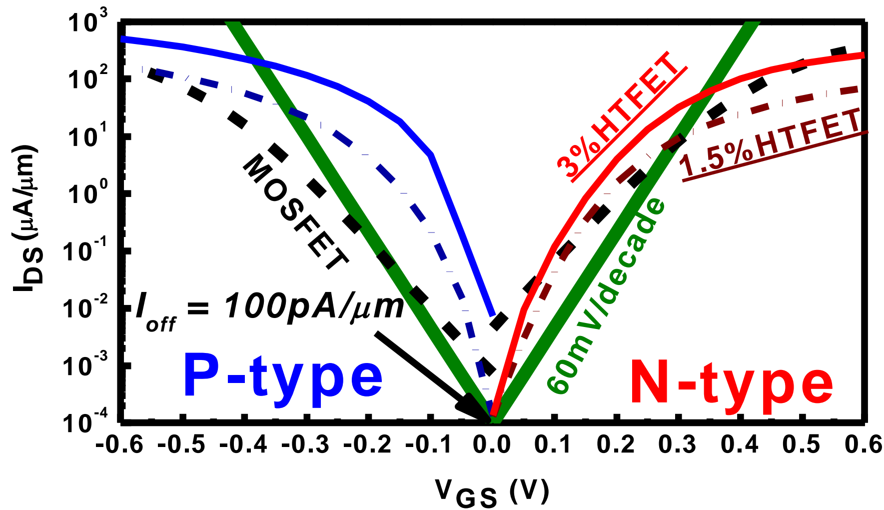

Figure 6.3 I_{ds}-V_{GS} characteristics ($|V_{DS}|$ = 0.3 V) for the *p*- and *n*-type ε-Ge/$In_xGa_{1-x}As$ H-TFETs using 1.5% and 3.0% ε-Ge strain-states as compared with the MOSFET thermal limitation to *SS* and the 45 nm CMOS benchmark.

work function in the simulated ε-Ge/$In_xGa_{1-x}As$ H-TFETs was independently tuned in order to realize an I_{OFF} of 100 pA/μm for each strain configuration. Under these operating conditions, the ε-Ge/$In_xGa_{1-x}As$ H-TFETs exhibited a sub-60 mV/decade *SS* and enhanced drive current with respect to the benchmarked 45 nm *n*- and *p*-MOSFETs. Moreover, an increase in the ε-Ge/$In_xGa_{1-x}As$ H-TFET strain-state (up to 3.0%) corresponded to an order of magnitude improvement in I_{ON}, thereby allowing the 3.0% strained H-TFETs to significantly outperform their MOSFET counterparts at a supply voltage of 0.3 V. Figure 6.4 shows the I_{DS}-V_{DS} characteristics for the (a) *p*-type and (b) *n*-type ε-Ge/InGaAs H-TFET at 1.5% strain (2.0%-3.0% I_{DS}-V_{DS} not shown here). One can find from Figure 6.4 that both H-TFETs demonstrated unidirectional operation at reverse bias, which can be attributed to the asymmetric TFET device structure utilized in this work. As a result, it is expected that 6T SRAM cell operation, which implicitly utilizes the bi-directionality of standard MOSFET access transistors, would be adversely affected by transitioning to a TFET-based design. Additionally, the *n*-type ε-Ge/$In_xGa_{1-x}As$ H-TFET displayed an increased reverse saturation current as compared to the *p*-type device. Whereas homojunction TFETs exhibit an approximately uniform E_{beff} at the

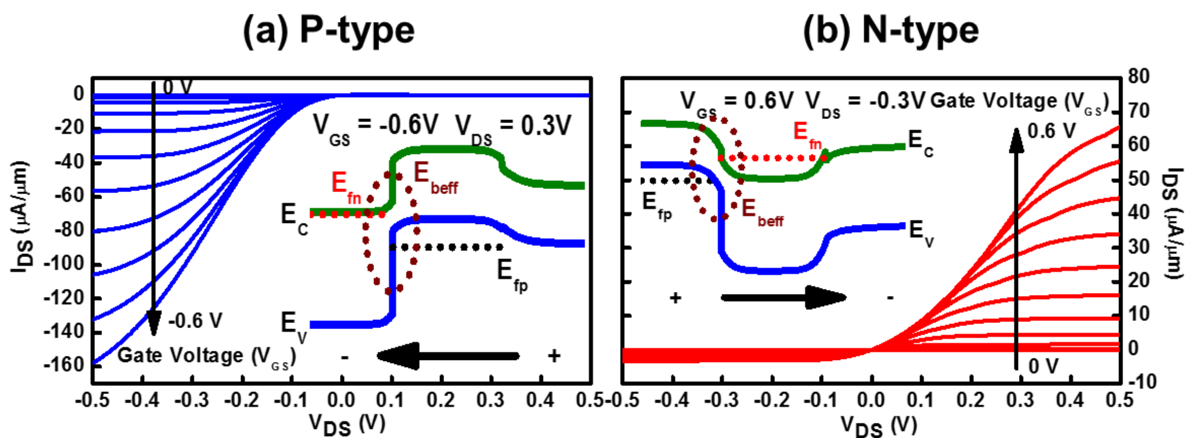

Figure 6.4 I_{DS}-V_{DS} characteristics for the (a) *p*-type and (b) *n*-type ε-Ge/$In_xGa_{1-x}As$ H-TFETs at 1.5% strain. Both insets show corresponding band diagrams under positive gate bias and a reverse bias from drain to source ($|V_{DS}| = 0.3$ V, $|V_{GS}| = 0.6$ V).

source-channel and drain-channel junctions, H-TFETs, by nature, exhibit asymmetric source and drain tunneling barriers. As shown in the insets of Figure 6.4, the asymmetries in E_{beff} and source/drain material bandgaps in H-TFETs can give rise to reverse bias conditions that result in enhanced reverse bias leakage current [11]. In this work, at a V_{DS} of -0.3 V and V_{GS} of 0.6 V, the simulated *n*-type ε-Ge/$In_xGa_{1-x}As$ H-TFET energy band diagram revealed an electron quasi-Fermi level that was above the hole quasi-Fermi level within the $In_xGa_{1-x}As$ channel. This, in conjunction with the availability of states in the source, directly resulted in the generation of a tunneling current between the drain and source, mirroring the negative differential resistance process in a tunnel diode structure. Moreover, the reduced source-channel E_{beff} (due to the nature of the H-TFET structure) resulted in an enhancement of the reverse tunneling probability, thereby increasing reverse bias leakage current as compared to a homojunction TFET device. Conversely, although the *p*-type ε-Ge/$In_xGa_{1-x}As$ H-TFET exhibited considerable hole accumulation in the channel, a lack of available states within the source prevented the generation of a reverse tunneling current, leading to stronger uni-directionality as compared to the *n*-type ε-Ge/$In_xGa_{1-x}As$ H-TFET.

The dependence of the ε-Ge/$In_xGa_{1-x}As$ H-TFET gate capacitance on gate bias was also investigated, as shown in Figure 6.5. One can find from Figure 6.5 that a large gate-drain (C_{gd})

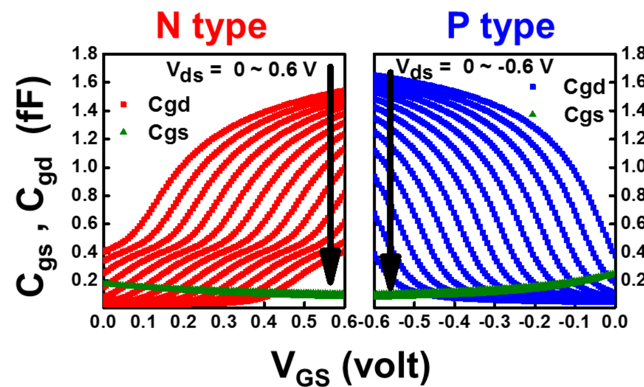

Figure 6.5 Gate capacitances C_{gs} and C_{gd} as observed in the n- and p-TFETs at 1.5% strain as a function of gate voltage. C_{gd} was found to exhibit a strong dependence on gate voltage.

capacitance was observed, which would lead to a substantial Miller capacitance during the complimentary operation of *p*- and *n*-type ε-Ge/$In_xGa_{1-x}As$ H-TFETs. The enhanced C_{gd} can be attributed to inversion layer formation occurring in close proximity to the drain, whereas a strong depletion region is formed at the source-channel interface, thereby resulting in lowered gate-source capacitance (C_{gs}).

6.3. SRAM Cell Design and Static Noise Margins for Read and Write Operations

In a standard 6T SRAM cell, two end-to-end inverters create the bi-stable latch circuit used to store a single bit. The read and write operations, as signaled by a complementary pair of bit lines (BL and BLB), are completed *via* two access transistors (ATs) controlled by a word line (WL). As a result, data retention can be significantly affected by the operational characteristics of the ATs, thereby impacting overall SRAM performance. Figure 6.6 shows the possible 6T SRAM configurations utilizing MOSFETs and TFETs.

Due to the unidirectional nature of TFETs, the standard 6T SRAM cell becomes limited to two AT configurations, as denoted by the direction of current flow: (i) inward, and (ii) outward.

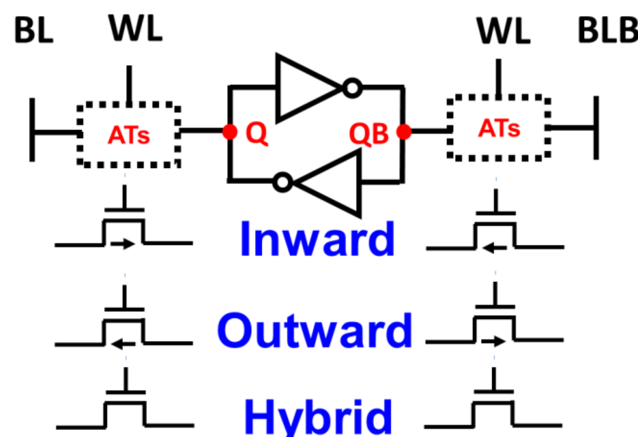

Figure 6.6 Circuit schematic for the 6T SRAM cell and investigated access transistor configurations.

In both configurations, the TFET uni-directionality enhances one operation (either read or write) while detrimentally affecting the other. Thus, by blocking either the charging or discharging of the cell, the TFET uni-directionality results in a single-ended operation, which could hence lead to the inoperability of the SRAM cell. As an example, writing a “1” onto node Q (“0”) of Figure 6.6 while using the inward configuration is trivial as current can freely flow from BL to Q. On the other hand, performing the same operation utilizing outward ATs greatly restricts the charging of Q, thereby potentially resulting in a read-fail. Similar difficulties can be observed for access to node QB, leading to the conclusion that both inward and outward TFET accessing schemes exhibit single-ended access characteristics. To overcome this issue, several researchers have developed a ‘hybrid’ design in which TFETs are used for bit storage whereas conventional MOSFETs are used for accessing the latch [3], [8]. Nevertheless, under ultra-low supply voltage operation, the current mismatch between the two devices could inhibit SRAM performance, as will be discussed shortly.

An SRAM cell’s static noise margin (SNM) during read or write operations serves as an important quantifiable metric in order to gauge the cell’s robustness. The SNM is typically taken to be the maximum DC noise value for which the SRAM’s stored data remains intact [14]. In order to visualize and evaluate both read and write SNMs (RSNM and WSNM,

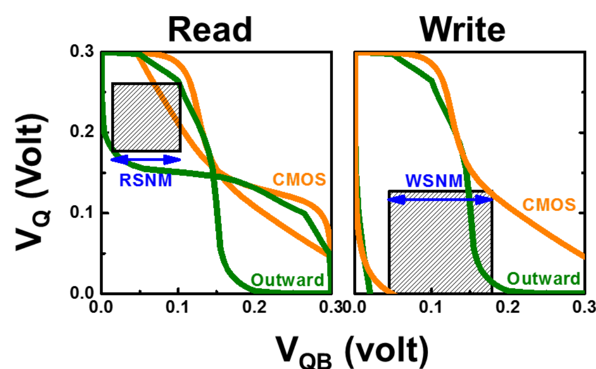

Figure 6.7 Butterfly curves for MOSFET and outward TFET AT configurations under read and write operation. The black square shows a graphical definition of RSNM and WSNM.

respectively), butterfly curves were generated, as shown in Figure 6.7. During a read operation, BL and BLB (Figure 6.6) are charged to V_{DD}, thereby charging Q ("1") and discharging QB ("0"). To mimic this behavior, half-circuit voltage transfer characteristics for two inverters are generated. Analysis of the transfer characteristics results in a square of maximal area inscribed between each curve. The RSNM is then defined as the length of one side of the fit square. Similarly, during a write operation, BL is charged to V_{DD} while BLB remains grounded, thereby discharging Q ("0") and charging QB ("1"). Analysis of the half-circuit voltage transfer characteristics yields the WSNM.

6.4. The Impact of Late Saturation on Noise Margins

Figure 6.8 shows the butterfly chart for a read operation as a function of strain from 1.5% (not shown) to 3.0% and effective threshold voltage. From Figure 6.8, one can observe that lower V_{TH} devices exhibit reduced RSNM, especially at higher strain levels. This is due to an

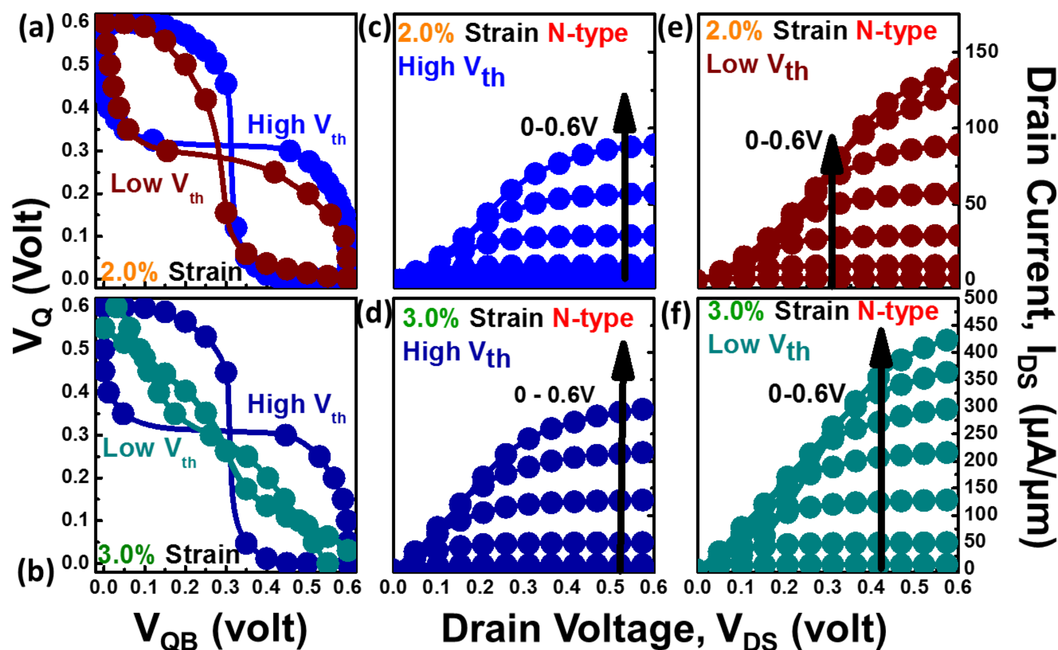

Figure 6.8 Butterfly charts for different V_{TH} ε-Ge/InGaAs TFET-based SRAM cells during a read operation with (a) 2.0% and (b) 3.0% strain at $V_{DD} = 0.6$ V. I_{DS}-V_{DS} plots for high V_{TH} and low V_{TH} *n*-type TFETs with 2.0% strain (c) and (e), and 3.0% strain (d) and (f).

increase in the drain current saturation delay for increasing strain [7]. Although higher strain and a lower V_{TH} can provide considerable drive current, the current in this case saturates at higher voltage, which further increases the transition region between the OFF- and ON-states and deteriorates the stability of read operations. This can be explained as follows. The voltage across a device is divided into two parts, *i.e.*, the channel and junction resistances. Additionally, the high strain and low V_{TH} devices are flooded with carriers that have less channel resistance, thus a higher voltage drop is placed across the junction and enhanced tunneling current is observed. On the other hand, a larger voltage drop across the channel results in less voltage across the junction and a reduction in tunneling carrier generation. These results indicate that V_{TH} control remains a key issue affecting TFET device performance. In this work, we have intentionally tuned the effective V_{TH} for all ε-Ge/$In_xGa_{1-x}As$ H-TFETs such that I_{OFF} is fixed at 100 pA/µm, thereby minimizing variability in our results due to saturation delay.

6.5. *Static Read and Write Operations using H-TFETs*

Figure 6.9 shows the (a-b) RSNM and (c-d) WSNM for different SRAM cell architectures operating at 0.3 V and 0.6 V supply voltages. We note that 1.5% strained Ge/$In_xGa_{1-x}As$ H-TFETs were used in the TFET-based SRAM architectures. One can find from Figure 6.9 that as the ratio between the cell access and inverter pull-down transistor widths increased (*i.e.*, W_{AT}/W_{PD}), the RSNM was observed to decrease. This result was due to the sensitivity of the node voltage at Q (or QB) to the magnitude of the charging current provided by the ATs as well as the ability of the inverter pull down transistors to sink current. Consequently, a larger W_{AT}/W_{PD} ratio indicates an increased AT charging current wherein the inverter pull-down transistor cannot sink the excess current. As a result, charge accumulated at node Q (QB), resulting in a 'flip' of the stored data. It can therefore be posited that the ability of the AT to source current has a significant impact on the stability of the SRAM cell. For the case of inward

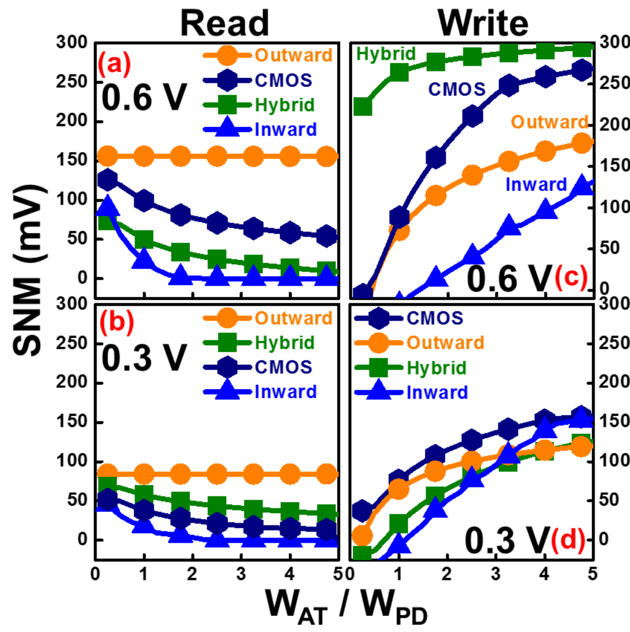

Figure 6.9 (a-b) RSNM and (c-d) WSNM for different SRAM cell architectures operating at 0.6 V and 0.6 V supply voltage, respectively, as a function of the access transistor (AT) and pull-down transistor (PD) width ratio.

TFET ATs, the charging current magnitude is large in comparison to the other accessing schemes, resulting in a disturbance of the stored data. Similarly, for outward ATs, the uni-directionality of the TFETs under reverse bias served to further isolate the SRAM cell by inhibiting current flow to Q (QB). To circumvent these issues, the hybrid approach utilized bi-directional MOSFETs as ATs. As shown in Figure 6.9, the hybrid SRAM cell design provided similar RSNM and WSNM performance to the standard HP CMOS SRAM cell. However, due to the ability of the inverter pull-down transistor (in this case a TFET) to sink additional current at 0.3 V as compared to a standard MOSFET, the hybrid SRAM cell design exhibited a larger RSNM under ultra-low supply voltage operation.

Additionally, Figs. 6.9(c) and 6.9(d) show the WSNM for the investigated SRAM cell architectures, again using supply voltages of 0.3 V and 0.6 V and a ε-Ge strain-state of 1.5%. Under these conditions, a trend opposite that observed for the RSNM was found. In this case, 'flipping' the stored data necessitates that the BL (BLB) charging current magnitude be greater

than the ability of the inverter pull-down transistors to sink current. Hence, an increase in the W_{AT}/W_{PD} ratio resulted in an increase in the observed WSNM. Moreover, as predicted, the inward and outward TFET AT schemes yielded single-ended write operability. This is in comparison to the hybrid and standard CMOS accessing schemes, which resulted in symmetric write operability. This can be explained as follows. For inward TFET ATs, only the AT at the grounded node (either Q or QB) is under forward bias. Likewise, for outward TFET ATs, only the AT at the high node (again, either Q or QB) is under forward bias. Correspondingly, unlike the standard CMOS or hybrid accessing schemes wherein operating on stored data occurs simultaneously through bidirectional MOSFET operation, the write process for TFET accessing schemes occurs *via* one AT and propagates through the remainder of the cell. As a result of this behavior, the WSNM is reduced for uni-directional TFET accessing schemes. Moreover, it was observed that *n*-TFETs exhibited an enhanced ability to sink current as outward ATs, thereby corresponding to an increased WSNM over outward accessing schemes [3]. At a V_{DD} of 0.6 V, the hybrid SRAM cell design was observed to leverage the enhanced drive current of the bi-directional MOSFETs and the strong latch behavior of the H-TFETs so as to deliver an enhanced WSNM. On the other hand, under a 0.3 V operating voltage, the hybrid accessing scheme suffered from degraded charging/discharging currents due to the sub-threshold operation of the MOSFET ATs, resulting in a dramatically reduced WSNM. We therefore conclude that for 6T SRAM cell architectures, a trade-off exists between the ability to read and write as a function of W_{AT}/W_{PD} as well as accessing scheme. Correspondingly, we have selected the outward and hybrid accessing schemes for further investigation due to the poor SNM observed under the inward AT scheme.

6.6. The Effect of Strain on Static Noise Margins

In order to understand the impact of ε-Ge/$In_xGa_{1-x}As$ strain-state on the observed SNMs, RSNM and WSNM as a function of supply voltage is plotted in Figure 6.10 for each strain level and accessing scheme. Due to the poor performance of inward TFET ATs, as previously discussed, we hereon focus on the hybrid, outward, and standard MOSFET accessing schemes. As can be seen in Figs. 6.10(a) and 6.10(b), increasing the ε-Ge strain level has little effect until the strain-state reaches 3.0%. This difference is even further suppressed under the hybrid SRAM cell design, as can be observed in Figure 6.10(b). Regarding the hybrid accessing scheme, for operating voltages above 0.4 V, the MOSFET ATs provided higher drive currents than the constituent latch H-TFETs, thereby resulting in a limitation to the extracted RSNM due to the H-TFET drive current. Conversely, for supply voltages below 0.4 V, the hybrid accessing scheme exhibited superior performance as compared to the standard CMOS SRAM

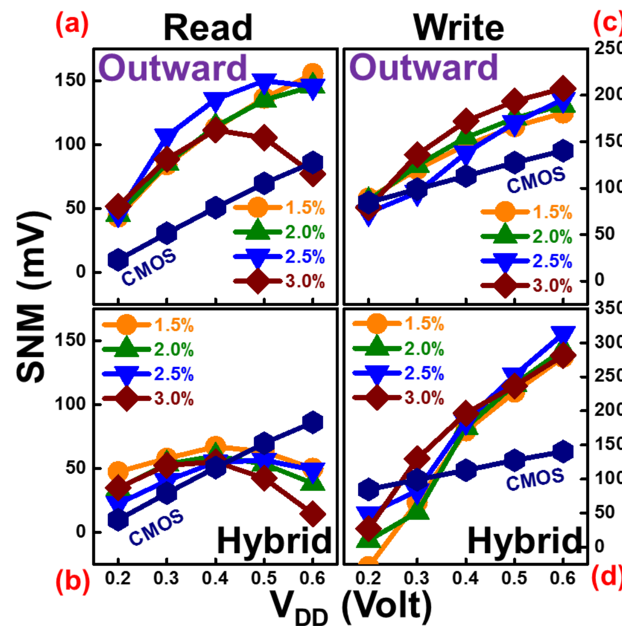

Figure 6.10 RSNM and WSNM as a function of supply voltage under different ε-Ge strain-states. Outward AT configurations exhibit superior RSNM and WSNM as compared to the MOSFET benchmark regardless of strain amount or supplied voltage.

cell. This result stems from the sub-threshold operation of the MOSFETs, thereby leading to reduced MOSFET drive current in comparison to the H-TFETs. For the outward AT scheme, all strain levels demonstrated improved SNMs as compared to the 45 nm CMOS benchmark. However, the high strain (3.0%)-based SRAM cells exhibited a significant drop in RSNM as a result of intrinsic NDR behavior, as discussed in Section 6.2.

Figs. 6.10(c) and 6.10(d) show the WSNM as a function of supply voltage for the investigated strain-states and accessing schemes. Due to the large charging/discharging current observed under the outward TFET accessing scheme, the WSNM for the outward TFET AT SRAM cell was markedly larger than that of the CMOS benchmark. For supply voltages above 0.3 V, the hybrid accessing scheme also demonstrated improved WSNM performance as compared to the CMOS benchmark. However, for lower operational voltages, the sub-threshold operation of the MOSFET ATs limited the overall WSNM of the hybrid accessing scheme. Correspondingly, the outward TFET accessing scheme provides the widest SNMs under both read and write conditions, outperforming the 45 nm CMOS benchmark up to 0.6 V supply voltage.

6.7. Dynamic Performance of 6T and 7T SRAM Cells

In this section, we investigate the dynamic performance of the previously discussed SRAM cell architectures. We note that the convention used hereon for the write and read delays are the times required for the storage node to charge to 90% V_{DD} or for ($V_{BLB} - V_{BL}$) to reach 10% V_{DD}, respectively. Moreover, a 20 fF capacitance was used to represent the line capacitance of metal interconnects.

Figure 6.11(a) shows the read delay times for the studied accessing schemes. The delay time for the outward TFET AT configuration was observed to be largest due to the uni-directional nature of the TFET and the resultant limitation to the cell discharging current. To resolve this

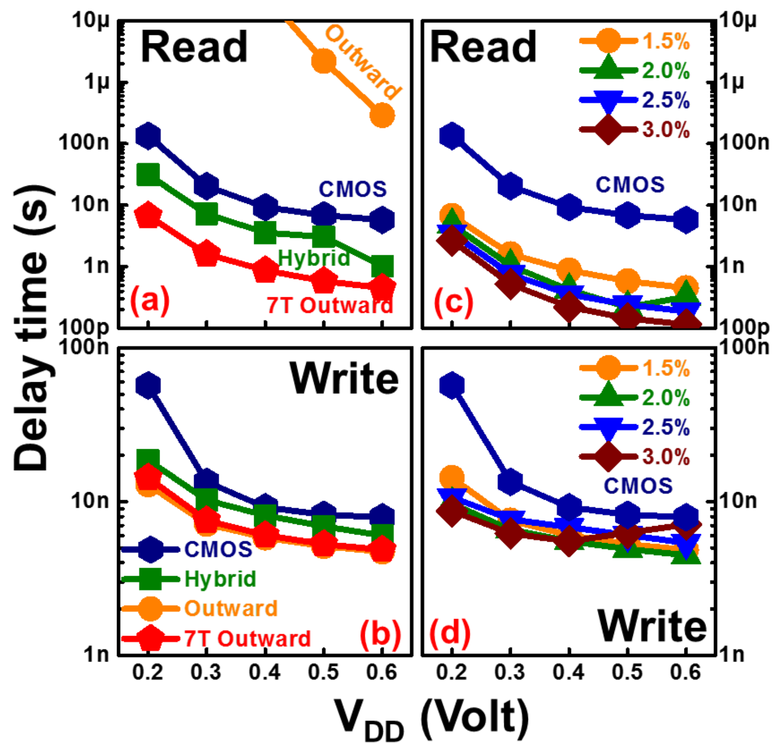

Figure 6.11 (a-b) Delay times for different SRAM architectures as function of applied voltage. (c-d) Delay times for the investigated strain levels of 7T H-TFET SRAM as a function of applied voltage.

issue, a 7T SRAM cell architecture, as reported by Lee et al. [8], is proposed. As can be seen in Figure 6.12, this modified SRAM cell design incorporates an additional transistor with its gate connected to Q, its drain connected to the read bit line (RBL), and its source connected to the read word line (RWL). During a read operation, RWL becomes grounded and RBL is charged to V_{DD}. If data is stored at Q, RBL will be discharged to ground. By leveraging the uni-directional nature of TFETs, undesirable reverse leakage current can be suppressed. Moreover, the SRAM cell is allowed to stay in data retention mode during the read operation, thereby allowed for robust readability. Consequently, the proposed 7T H-TFET SRAM cell design exhibits a superior read delay as compared to the alternative cell architectures, as shown in Figs. 6.11(a-b).

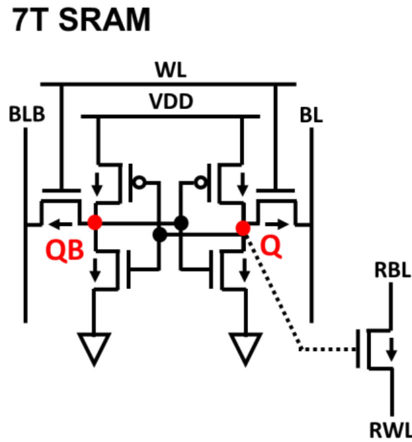

Figure 6.12 (a-b) Delay times for different SRAM architectures as function of applied voltage. (c-d) Delay times for the investigated strain levels of 7T H-TFET SRAM as a function of applied voltage.

Under write operation, the write delay time of the outward and 7T outward AT SRAM cell configurations were observed to significantly outperform the CMOS-based designs for supply voltages below 0.3 V. This was due to the sub-threshold operation of the MOSFETs within this operating regime. Similarly, the proposed 7T SRAM cell design was found to display lower read and write delay times, with respect to the 45 nm CMOS benchmark, across all investigated strain-states and operating voltages.

6.8. SRAM Energy Dissipation

Figure 6.13 compares the SRAM cell standby power as a function of supply voltage for the 45 nm CMOS benchmark and the ε-Ge/$In_xGa_{1-x}As$ H-TFET cell designs. The standby power was found to reduce for decreasing operational voltages, as expected. Moreover, at a V_{DD} of 0.6 V, the standby power of the 7T H-TFET SRAM cell was observed to be 52.7×, 47.6×, 20.7×, and 4.91× lower than the CMOS benchmark for the 1.5%, 2.0%, 2.5%, and 3.0% strain-states, respectively. At a 0.2 V supply voltage, the difference in standby power was observed to decrease to 12.5×, 12.4×, 9.8×, and 2.86× for the 1.5%, 2.0%, 2.5%, and 3.0% strain-states, respectively. Although higher strain H-TFETs provide some performance improvement, the

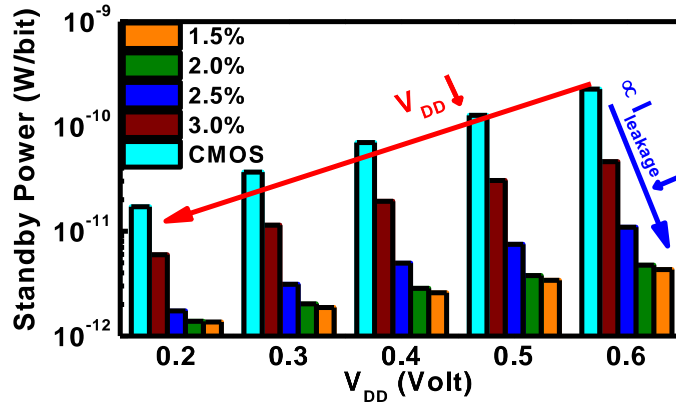

Figure 6.13 SRAM cell standby power as a function of supply voltage for the 45 nm CMOS benchmark and the ε-Ge/$In_xGa_{1-x}As$ H-TFET cell designs. All configurations take advantage of supply voltage scaling to save power. The 7T H-TFETs SRAM cells exhibit reduced standby power in comparison to the 45 nm MOSFET benchmark due to low H-TFET I_{OFF}.

3.0% strained H-TFETs exhibit significant standby power consumption, thereby limiting their usage in future ultra-low voltage applications. Moreover, 1.5%-2.0% strained H-TFETs are more easily realizable due to their larger critical layer thickness during growth, thus preserving a defect-free tunneling interface [12].

Additionally, Figure 6.14 highlights the extracted RSNM and WSNM for the 7T H-TFET SRAM cell in comparison with previously published results. The proposed 7T H-TFET SRAM cell design was found to outperform the competing SRAM architectures utilizing seven or less

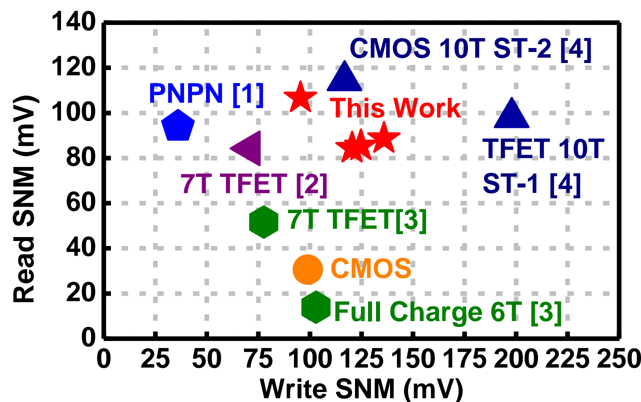

Figure 6.14 RSNM and WSNM for the 7T H-TFET SRAM cell in comparison with previously published results at 0.3V supplied voltage. Top-right corner is desirable region for high performance SRAM cells.

transistors while approaching the performance of comparable 10T SRAM design. As can be seen in Figure 14, the balance between cell area, RSNM and WSNM achieved by our proposed 7T design suggests the feasibility of utilizing ε-Ge/$In_xGa_{1-x}As$ H-TFET-based SRAM cell architectures in order to improve performance and reduce power consumption for ultra-low-power applications.

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Chapter 7

TBAL: Tunnel FET-Based Adiabatic Logic for Energy-Efficient, Ultra-Low Voltage IoT Applications

With the proliferation of connected computing devices into the consumer, medical, and communication application spaces (*via* the internet of things, IoT), device-circuit co-design has become increasingly relevant to the domain of energy-efficient embedded electronics. Similarly, power dissipation has become a key issue in portable and embedded systems where power supply is limited by battery capacity. In previous chapters, we explored solutions to achieve energy-efficiency on the ultra-low voltage platform. However, these efforts were focused on reducing the OFF power by using TFETs which provide low leakage current in the OFF-state. On the other hand, the active power dissipation is still untouched and needs further investigation. Therefore, in this chapter, an advanced logic scheme (Adiabatic Logic) which addresses the active power dissipation will be investigated in detail, utilizing complementary TFETs to maintain low OFF-state power.

Power dissipation in combinational CMOS logic is unalterable due to the fact that it discharges after each operation through the load capacitor [1]-[4]. In contrast, Adiabatic logic is an alternative approach to conventional combinational logic wherein a logical operation is, ideally, a reversible adiabatic process. These circuit topologies can inject and then return the charge by using a specially designed power-clock voltage source. Furthermore, by virtue of the working principle of adiabatic logic, the evaluation of the power consumption becomes the

energy dissipation per cycle, which will be discussed further in Section 6.3. Consequently, the energy consumption per cycle is scaled in proximity to Landauer's limit. Based on Landauer's principle [5]-[6], a corresponding entropy is needed to complete any logically irreversible manipulation of information, such as bit erasure. The energy loss associated with such an operation is $kTln2$ (Joule), where k is Boltzmann's constant and T is the temperature. Furthermore, adiabatic logic operates efficiently at frequencies below 1 GHz, making it a suitable candidate for IoT applications demanding moderate frequency requirements (*e.g.*, RFID ~ 13.56 MHz) [4], [7], [8].

7.1. *TFET, FinFET, and MOSFET Operating Characteristics*

In this work, heterojunction TFETs (H-TFETs) were used to evaluate the performance of competing adiabatic logic implementations operating at or below 0.6 V supply voltage. TFETs can be described as gated *p-i-n* diodes in which the gate, residing over the channel, controls the tunneling probability at the source/channel junction through an applied gate voltage. The electrons (or holes) tunneling from source-to-channel experience a heterostructure-dependent tunneling barrier, thereby affecting their tunneling probability and hence the device current.

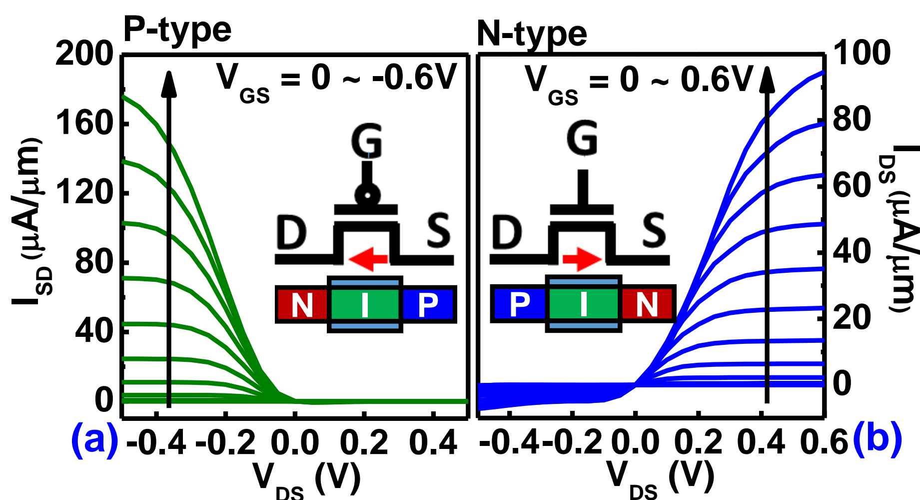

Figure 7.1 Output characteristics of strain and bandgap engineered SG Ge/InGaAs *p*- and *n*-TFETs exemplifying their unidirectional nature.

Due to their asymmetric device structure, TFETs also exhibit unidirectional behavior, as illustrated in Figure 7.1. From Figure 7.1, one can find that drain current is limited to leakage current with reverse bias application for both *p*- and *n*-TFETs. Consequently, one must account for the unidirectionality of TFETs when designing TFET-based adiabatic logic circuits. Thus, in this work, we propose a solution to overcome the unidirectional nature of TFETs and realize functional TFET-based adiabatic logic Furthermore, in order to investigate the performance impact of TFET design on adiabatic logic circuit operation, both staggered-gap (SG) and near broken-gap (NBG) TFETs were considered in this work. In these TFETs, the effective tunneling barrier height, E_{beff}, is described by the energy band alignment at the source/channel interface and plays a key role in determining ON- and OFF-state current. For SG TFETs, E_{beff} is smaller than the bandgap of either source or channel material. On the other hand, for NBG TFETs, E_{beff} approaches zero. Figure 7.2 highlights the drain current versus gate voltage (I_{DS}-V_{GS}) characteristics of *n*- and *p*-type 45 nm high-performance (HP) MOSFETs [13], 20 nm low-power (LP) FinFETs [13], 20 nm HP FinFETs [13], strain and bandgap engineered SG TFETs (2.0% tensile-strained Ge/InGaAs) [9], and NBG TFETs (3% tensile-strained Ge/InGaAs) [9]. LP FinFETs were found to maintain similar I_{ON} as compared to planar

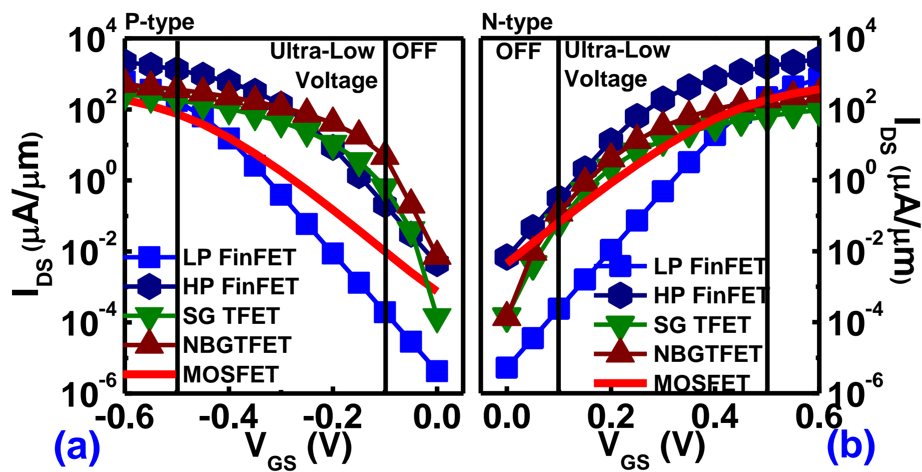

Figure 7.2 I_{ds}-V_{GS} characteristics ($|V_{DS}|$ = 0.6 V) for the *p*- and *n*-type FETs.

MOSFETs (SS ~ 110 mV/dec) and simultaneously suppress I_{OFF} due to enhanced gate control, thereby leading to improved subthreshold behavior (SS ~ 62 mV/dec). Conversely, LP FinFETs could not supply sufficient I_{ON} below V_{DD} = 0.4 V. Alternatively, HP FinFETs exhibited increased I_{ON} at the penalty of degraded I_{OFF} due to their lower SS (~64 mV/dec). However, SG TFETs exhibited superior subthreshold dynamics (SS ~ 38 mV/dec), leading to reduced I_{OFF} and comparable I_{ON} under low-voltage operation. Moreover, the constrained tunneling probability at higher operating voltages was found to limit SG TFET I_{ON} above V_{DD} = 0.6 V. Similarly, NBG TFETs (SS ~ 34 mV/dec) were observed to provide high I_{ON}, due to the near-zero tunneling barrier, and low I_{OFF}. Table 7.1 summarizes the device characteristics of the FETs investigated in this work for low and conventional operating voltages. From this comparison, one can find that TFETs offer a potential route for the development of energy-efficient adiabatic logic circuits.

TABLE 7.1
DEVICE PERFORMANCE SUMMARY

Device Type	I_{OFF}	I_{ON}	
		Ultra-low Voltage (<0.5V)	Normal Voltage (> 0.5V)
LP FinFET	Low	Low	Comparable
HP FinFET	High	High	High
SG TFET	Low	High	comparable
NBG TFET	Comparable	High	High

7.2. *The Adiabatic Switch*

The energy dissipation in conventional combinational logic can be understood *via* a simple case study: the CMOS inverter. In a basic inverter circuit, the pull-up network, pull-down network, and load capacitance can be modeled as an ideal switch in series with a resistor (R) and load capacitor (C) supplied by a constant voltage source (V_s), as shown in Figure 7.3(a). Throughout the duration of the switching process, V_s transfers a charge Q (equal to CV_{DD}) and energy E (CV_{DD}^2) to the load capacitor. However, the capacitor can only story an energy

equivalent to $\frac{1}{2}CV_{DD}^2$. Thus, half of the system's energy loss occurs during the charge transfer from V_s to the load (*i.e.*, during the charging process). Likewise, the remainder of the energy dissipation occurs during the pull-down, or discharging, process. As a result, the entirety of the energy supplied is consumed during each switching cycle. Figure 7.3(c) shows the capacitor voltage as a function of time for different time constants (τ). One can find from Figure 7.3(c) that only the charging speed is affected by the system's time constant. Thus, the resistance of

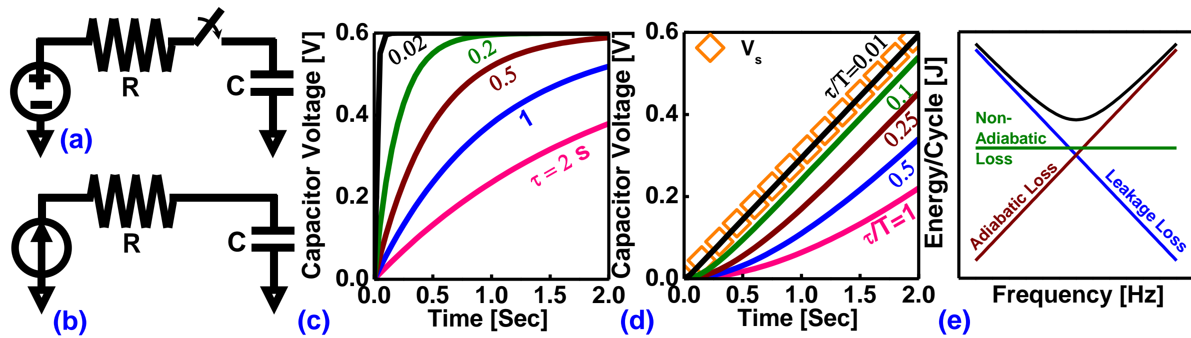

Figure 7.3 RC circuit model of (a) a conventional inverter and (b) an adiabatic switch. Capacitor voltage charging of the (c) conventional inverter and (d) adiabatic switch as a function of charging time and time constant. (e) Frequency dependence of the three energy loss mechanisms in AL.

the pull-up and pull-down networks of a conventional combinational logic circuit only affect the circuit's charging and discharging time, and not its dynamic power dissipation.

Alternatively, an adiabatic switch can be modeled as a constant current source in series with a resistor (*R*) and capacitance (*C*), as shown in Figure 7.3(b). Unlike conventional combinational logic, adiabatic logic circuits gradually ramp the supply voltage. As long as the ramping period is sufficiently large (several times larger than the time constant of the system), the voltage drop across *R* becomes arbitrarily small and the source provides virtually constant current. Thus, the capacitor voltage (V_C) in the system can be expressed as:

$$\frac{V_S(t)-V_C(t)}{R} = C\frac{dV_C(t)}{dt} \tag{7.1}$$

$$\frac{dV_C(t)}{dt} + \frac{1}{RC}V_C(t) = \frac{V_{DD}}{TRC}t \tag{7.2}$$

where V_s is the voltage of the ramped supply source and τ = RC. By applying non-homogeneous, first-order linear differential equations [14], V_C, the voltage drop across resistance R (V_R), and the current i(t) can be expressed as:

$$V_C(t) = V_{CC}\left(\frac{t}{T}\right) + V_{CC}\left(\frac{\tau}{T}\right)\left[e^{-\frac{t}{\tau}} - 1\right], \tag{7.3}$$

$$V_R(t) = V_{CC}\left(\frac{\tau}{T}\right)\left[1 - e^{-\frac{t}{\tau}}\right], \tag{7.4}$$

$$i(t) = V_{CC}\left(\frac{C}{T}\right)\left[1 - e^{-\frac{t}{\tau}}\right], \tag{7.5}$$

where *T* is the switching period (*i.e.*, ramping interval). From the above, one can find that smaller time constants reduce V_R, which acts as the source of power dissipation in this model. Figure 7.3(d) shows V_C as a function of time for different τ/T ratios, wherein V_s is ramped to 0.6 V in a 2.0 s interval. For small τ/T, V_C closely follows V_s due to the direct relation between V_R and τ/T. This result explicitly reinforces the previous assumption regarding the necessity of sufficiently long ramping intervals for the supply. Subsequently, the voltage source can be treated as a constant current source through the following expression:

$$i(t) = C\frac{dV_c(t)}{dt} = C\frac{dV_S(t)}{dt} = C\frac{V_{DD}}{T} \tag{7.6}$$

To further estimate the energy dissipation in an adiabatic switch, the energy of the entire system can be expressed as:

$$E = \int_0^T p(t)dt = \int_0^T V_S(t)i(t)\,dt,$$

$$= \int_0^T R\frac{C^2V_{DD}^2}{T^2}dt = \frac{RC}{T}CV_{DD}^2. \tag{7.7}$$

Furthermore, full adiabatic logic consists of two phases: energy supply and energy recovery. It is important to note that each phases dissipates the same amount of energy; thus, the total

energy dissipation is $E_{AL} = 2\frac{EC}{T}CV_{DD}^2$. This is in parison to a conventional CMOS inverter, wherein the energy dissipation is $E_{CMOS} = CV_{DD}^2$. Comparing the expressions for energy dissipation between adiabatic and conventional combinational logic, one can find that the adiabatic implementation introduces a new degree of freedom, time, thereby permitting additional reductions in energy dissipation. The necessary condition for which the energy dissipation of an adiabatic implementation is lower than that of a conventional implementation is given by:

$$E_{AL} < E_{CMOS},$$

$$2\frac{RC}{T}CV_{DD}^2 < \frac{1}{2}CV_{DD,}^2$$

$$T > 4RC \tag{7.8}$$

This result reveals that the adiabatic switch conserves more energy with respect to the conventional switch under two conditions: (i) a long switching period (*i.e.*, a lower clock frequency), and (ii) a lower time constant. Furthermore, the channel resistance (*i.e.*, ON resistance) plays an important role in dictating energy dissipation in an adiabatic switch, as compared to its non-existent influence on conventional combinational logic energy dissipation.

In any circuit, leakage power cannot be recovered; therefore, the estimated power loss due to all leakage mechanisms is an important figure of merit. To this end, the totality of leakage mechanisms in a system can be combined into an average leakage current, I_{leak}, which leads to the leakage-dependent energy dissipation given by:

$$E = V_{DD}I_{leak}T = V_{DD}I_{leak}\frac{1}{f}. \tag{7.9}$$

Since the leakage current is predominately independent of time, the energy dissipation is constant as a function of time. However, additional energy would accumulate during increased

operational time (*i.e.*, at lower frequencies). In addition to energy dissipation due to leakage current, another form of energy dissipation that cannot be recovered is non-adiabatic loss, as given by [15], [16]:

$$E = \frac{1}{2} C V_{th,p}^2. \tag{7.10}$$

Figure 7.3(e) illustrates all of the energy dissipation mechanisms heretofore discussed as a function of frequency. One can find that an optimal frequency exists at which a minimum energy dissipation occurs. This is a result of the opposing linear dependencies of the adiabatic and non-adiabatic losses on frequency. Thus, the challenge is to design adiabatic circuits at an optimal frequency (f_{op}) for IoT applications.

7.3. Four-Phase Power Clocked Adiabatic Logic

One method of establishing a ramping voltage source is to use a power clock as opposed to a constant voltage supply. Four-phase power clocks have been widely used in several adiabatic logic implementations [17]–[20]. In order to demonstrate the operation of adiabatic logic, efficient charge recovery logic (ECRL) is considered here. Figure 7.4 shows the waveforms and schematic circuit representation of an ECRL inverter. Each power clock cycle consists of four phases having the same duration, that is: wait, evaluate, hold, and recover. Initially, the power clock (CLK) and $\overline{in}$ are low, the complementary output (out, $\overline{out}$) are low, and in is awaiting an input signal. During the wait phase, P1 and P2 are OFF due to CLK being connected to ground, thus out and $\overline{out}$ are also low. During the evaluation phase, the input signal is evaluated and generates a corresponding output. When in remains high and $\overline{in}$ remains low, N1 and N2 are ON and OFF, respectively. As CLK is ramped above $V_{th,p}$, P1 and P2 are turned ON. Conversely, out remains unchanged due to N1 remaining ON. This ensures that

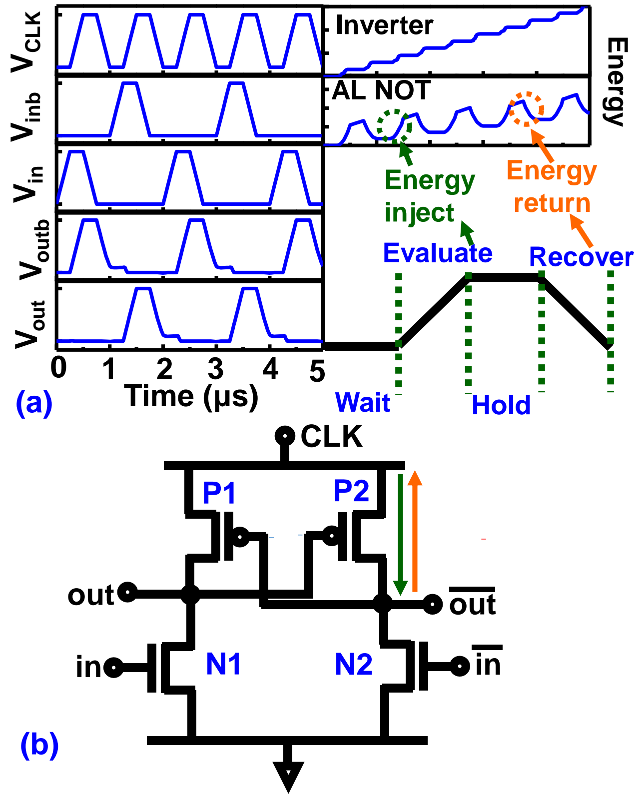

Figure 7.4 (a) Output waveforms and four-phase operation CLK for HP FinFET PFAL. Energy is injected from CLK to output (green) in the evaluate phase and returned to CLK during the recover phase. (b) ECRL circuit schematics. The returned current and injected current are illustrated by orange and green arrows.

P2 remains on during the evaluation phase and $\overline{out}$ mirrors the ramping supply voltage. During the hold phase, all signals are kept at their current status, thereby supplying subsequent logic gates with stable inputs. Finally, in the recovery phase, CLK is ramped from V_{DD} to ground. Since the voltage at $\overline{out}$ is now higher than CLK, current flows from $\overline{out}$ to CLK. However, $\overline{out}$ requires a minimum voltage, $V_{th,p}$, such that P2 remains ON; thus, a minimum, non-adiabatic energy ($\frac{1}{2}CV_{th,p}^2$) remains at $\overline{out}$ for reuse during the next cycle.

The energy dissipation of conventional CMOS and adiabatic inverters as a function of time is shown in Figure 7.4(a). One can find that the energy dissipation in a conventional CMOS inverter accumulates with increasing operation cycles. However, under adiabatic operation, the energy injected into the system during the evaluation phase is returned to the voltage source

during the recovery phase. Thus, the effective energy consumption of the adiabatic inverter is significantly reduced compared to that of the conventional CMOS inverter. Furthermore, the critical path in adiabatic circuit operation can be identified as the pull-up network, which functions as the current injection (Figure 7.4(a), green arrow) and recovery (Figure 7.4(a), orange arrow) route for the ECRL circuit.

7.4. Design of TFET-Based Adiabatic Logic

In this section, we will discuss adiabatic logic circuit topologies utilizing TFET devices. Three major implementations of adiabatic logic (ECRL, PFAL, and 2N-2N2P) were considered in this work, as illustrated in Figure 7.5. In contrast to the bidirectional current flow in conventional MOSFETs, TFETs provide unidirectional current. Consequently, the pull-up network in an adiabatic circuit requires additional design considerations in order to provide a pathway for charge injection and recovery. In this work, we propose the incorporation of additional recovery transistors to provide a charge recovery path to the supply source, as highlighted in red in Figure 7.5. Unlike conventional MOSFETs, wherein the drain and source regions are distinguished by the applied voltage (*i.e.*, they are ambipolar), H-TFETs utilize distinct drain and source materials, thus they behavior as unipolar, asymmetric devices. As a result, current flow is restricted to the *n*- or *p*-type H-TFET during injection or recovery, thus correct adiabatic logic circuit functionality is only realizable when utilizing both polarities in the adiabatic pull-up network.

Figure 7.5(a) shows a schematic diagram of an ECRL circuit consisting of a set of latched pull-up transistors supplied by a power clock. It should be noted that the ECRL configuration utilizes the fewest transistors; however, during the wait phase, all outputs remain floating, potentially resulting in incorrect signal chains or soft errors during operation [4]. In order to

mitigate this issue, the 2N-2N2P topology was proposed [20]. Figure 7.5(b) diagrammatically illustrates a 2N-2N2P circuit wherein two cross-coupled *n*-TFETs are added in parallel to the *n*-function blocks. Here, the added transistors behave similar to a latch cell used in static

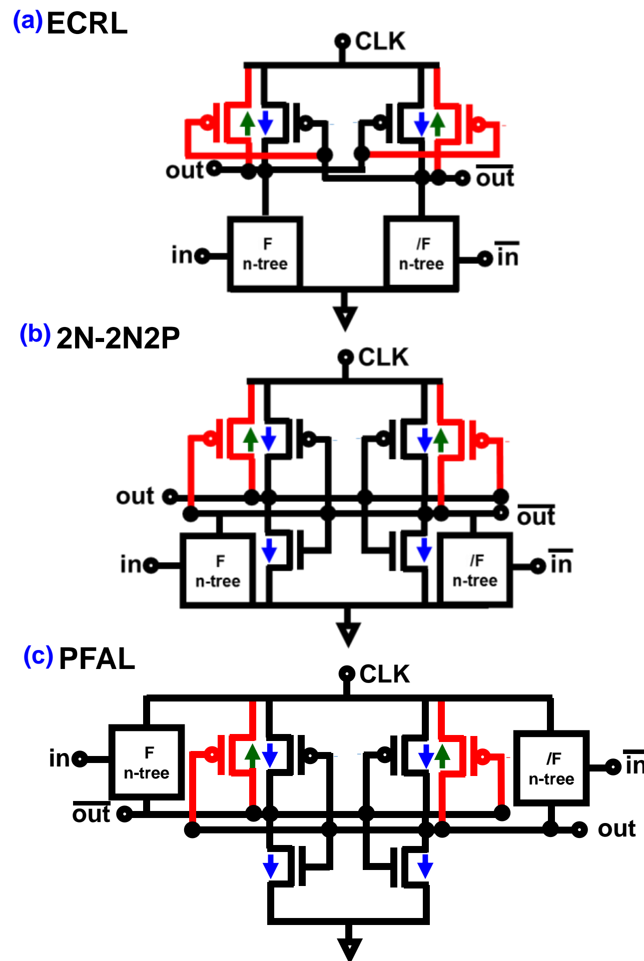

Figure 7.5 Circuit schematics of (a) ECRL, (b) 2N-2N2P, and (c) PFAL. The 'black boxes' represent *n*-type function trees. Red FETs indicate an additional TFET added to compensate for TFET unidirectionality.

random-access memory (SRAM) designs, providing a path to ground as well as avoiding

TABLE 7.2
ADIABATIC LOGIC PERFORMANCE SUMMARY

Circuit Type	Advantage	Drawback
ECRL	Fewest transistors	Floating nodes
2N-2N2P	No floating nodes	Extra transistors
PFAL	Lowest resistance	Extra transistors

floating nodes during operation. However, due to the additional transistors and push-pull functionality, 2N-2N2P exhibits increased energy dissipation as compared to ECRL.

Lastly, Figure 7.5(c) shows a schematic diagram of the final adiabatic logic implementation investigated in this work: positive feedback adiabatic logic (PFAL). A key difference between PFAL and 2N-2N2P is that the *n*-tree function blocks are in parallel with the pull-up network as opposed to the pull-down network. As a result, the overall resistance decreases during node charging [4], thereby reducing the energy dissipation due to adiabatic losses. Table 7.2 summarizes the advantages and disadvantages of the adiabatic logic designs proposed in this work.

7.5. Performance Analysis of TBAL

To more accurately compare the performance of the proposed adiabatic logic circuits (*i.e.*, ECRL, 2N-2N2P, and PFAL), the geometry of all FETs has been optimized to provide matching drive currents at V_{DD} = 0.5 V and equivalent rise and delay times at an operational frequency of 500 MHz. We note that the load capacitance was set to a nominal value of 20 fF [15]. Due to the four-phase operation of the investigated adiabatic circuits, instantaneous and average power consumption do not reflect the true energy dissipation within the circuit. Hence,

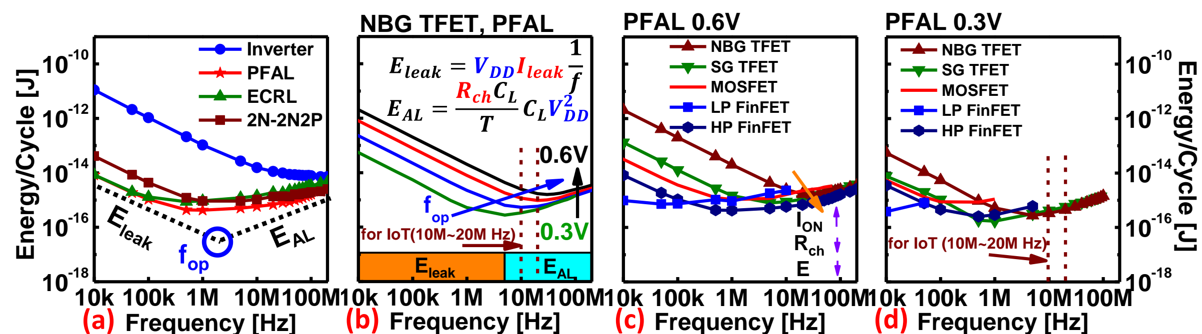

Figure 7.6 Energy/cycle for (a) all studied HP AL designs, (b) NBG TFET PFAL architecture for 0.3 V < VDD < 0.6 V, (c) and (d) frequency optimization for all investigated FET types using the PFAL architecture operating under 0.6 V and 0.3 V VDD.

in this work, the energy dissipation per cycle as a function of frequency is used as a performance metric for comparison between the applicability of each adiabatic logic design towards low power applications.

Figure 7.6(a) shows the energy dissipation per cycle for each investigated adiabatic logic design implemented using HP FinFETs operating at V_{DD} = 0.6 V. According to Eq. 7.9, leakage-related losses are dominate at lower frequencies due to the extended operation time. On the other hand, at higher operating frequencies, one can find that the energy dissipation of a conventional inverter remains constant due to the absence of adiabatic processes. Conversely, the energy dissipation per cycle of the adiabatic logic circuits is observed to increase with increasing frequency. This is due to a breakdown in the adiabatic process at higher frequencies (lower T), as detailed in Eqs. 7.7 and 7.8. A complete breakdown of adiabatic operation occurs when the load capacitance is unable to effectively charge following the source voltage. Additionally, PFAL exhibited the lowest energy per cycle due to its minimal ON resistance. Consequently, we will next investigate the impact of operational voltage (V_{DD} = 0.3 V and 0.6 V) and device architecture (*e.g.*, MOSFET, FinFET, TFET) on the energy dissipation in PFAL circuits.

The energy dissipation per cycle for PFAL implemented using NBG TFETs operating at 0.3 V < V_{DD} < 0.6 V is shown as a function of frequency in Figure 7.6(b). The resulting energy dissipation can be decomposed into two main constituents: energy loss due to leakage and energy loss due to adiabatic losses. With respect to the former, the energy per cycle decreases for decreasing operating voltage due to a reduction in I_{leak} and the linear dependence of E_{leak} on V_{DD}. On the other hand, adiabatic losses decrease as a function of V_{DD}^2. Thus, although channel resistance increases as the supply voltage is reduced, the quadratic dependence of adiabatic losses on operating voltage dominates their associated energy dissipation. Additionally, one

can find that the optimized working frequency (f_{op}) shifted to higher frequencies with increasing supply voltage. However, the corresponding increase in the energy dissipation minima negates the benefit of TBAL adoption. Thus, it becomes critical to estimate the energy dissipation per cycle within a select range of f_{op} required by IoT applications, *e.g.*, 10 MHz – 20 MHz.

After investigating the impacts of adiabatic logic architecture and operating voltage on energy dissipation per cycle, we will now discuss the role of device architecture (*i.e.*, MOSFET, FinFET, TFET) on adiabatic circuit performance. Figure 7.6(c) shows the energy per cycle as a function of frequency for PFAL implemented using five different device types (*i.e.*, MOSFET, LP FinFET, HP FinFET, SG TFET and NBG TFET) operating at V_{DD} = 0.6 V. As previously discussed, the energy per cycle arcs in Figure 7.6(c) can be decomposed into their leakage and adiabatic loss contributions. With regards to leakage-dominated losses, one can find that the LP FinFET-based PFAL circuit exhibited minimal energy dissipation due to the low leakage current device design (see Figure 7.2). Similarly, for V_{DD} = 0.6 V, both FinFET architectures exhibited lower leakage, as compared to their TFET counterparts, due chiefly to the superior gate control of the FinFET devices. In terms of adiabatic losses, LP FinFETs exhibited the highest energy dissipation of all investigated devices due to the drive current sacrifice made during device design (*i.e.*, the *SS*-limited trade-off between I_{ON} and I_{OFF}). Consequently, the channel resistance (R_{ch}) increase in LP FinFET devices directly correlated with increased energy per cycle. Conversely, HP FinFETs exhibited the lowest adiabatic losses due to their high I_{ON} (low R_{ch}) at V_{DD} = 0.6 V. As a result, the HP FinFET-based PFAL circuit demonstrated the lowest energy per cycle for all investigated device types (V_{DD} = 0.6 V) due to the reduced adiabatic and leakage losses.

Similarly, Figure 7.6(d) shows the energy per cycle for PFAL implemented using each aforementioned device type operating at V_{DD} = 0.3 V. From Figure 7.6(d), one can find that both MOSFET- and LP FinFET-based PFAL circuits failed to function as designed beyond f = 1 MHz due to the limited I_{ON} (increased R_{ch}) of both devices when operating in the subthreshold bias regime. As a result of the degraded ON current and R_{ch}, both MOSFET- and LP FinFET-based circuits exhibit larger time constants ($\tau = RC$), resulting in adiabatic breakdown at lower frequencies relative to the HP FinFET- and TFET-based designs. Similarly, HP FinFET-based PFAL was also observed to be limited to f < 10 MHz due to the subthreshold operation and loss of drive current at V_{DD} = 0.3 V. On the contrary, both SG and NBG TFET-based PFAL circuits were found to be capable of operating at ultra-low voltage, demonstrating a minimum in energy dissipation comparable or lower than that observed for the HP FinFET devices at V_{DD} = 0.3 V or 0.6 V. Moreover, as compared to the NBG TFET-based PFAL design, the SG TFET-based PFAL circuits exhibited less energy dissipation at lower operating frequencies due to the reduced leakage current of the SG TFET architecture (see Figure 7.2).

Figure 7.7 benchmarks the lowest energy per cycle (E_{op}) for all investigated device (MOSFET, LP FinFET, HP FinFET, SG TFET, and NBG TFET), circuit (ECRL, 2N-2N2P, and PFAL), and operating voltage (V_{DD} = 0.3 V, 0.4 V, 0.5 V, and 0.6V) combinations as a function of frequency. The optimal design solution space, *i.e.*, that which exhibits the lowest energy per cycle at the highest operating frequency, is indicated at the bottom-right of Figure 7.7. One can find that FinFET- and TFET-based circuits outperformed planar MOSFET-based designs under all investigated operating conditions. However, LP FinFET-based adiabatic logic circuits exhibit relatively low optimal operational frequencies due to their limited drive currents and corresponding increase in adiabatic losses. Conversely, HP FinFET-based adiabatic logic designs exhibit low energy dissipation per cycle, but fail to function at higher frequencies when

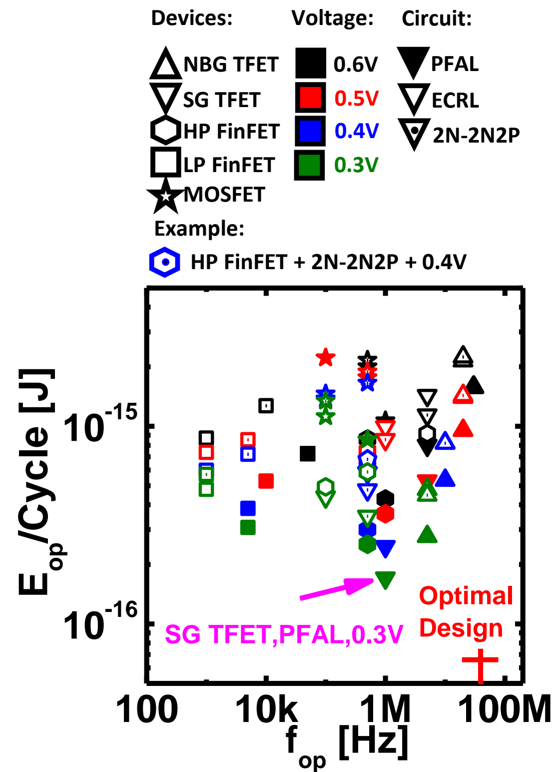

Figure 7.7 Optimized energy/cycle for each AL design, device-type, and operating voltage highlighting fop. Optimal design located in bottom-right (red cross). SG TFET-based PFAL shows the lowest energy consumption at 0.3 V.

operating in the ultra-low voltage regime. Both SG TFET- and NBG TFET-based adiabatic logic circuits solve these challenges, providing low energy per cycle at operating frequencies above 1 MHz when utilized at V_{DD} = 0.3 V. However, due to their enhanced drive current at low operating voltages as compared to SG TFETs, NBG-TFET-based adiabatic logic designs exhibit the lowest energy dissipation in the targeted 10 MHz – 20 MHz frequency range utilized in many IoT applications. To further clarify these results, we will next investigate the impact of device and circuit architecture in the 0.3 V < V_{DD} < 0.6 V supply range for a designated working frequency of 10 MHz.

7.6. *Voltage-Dependent TBAL Performance Analysis (f = 10 MHz)*

Unlike the previous discussion, we will now quantify the impact of operating voltage, device type, and circuit topology explicitly in the adiabatic loss regime. Thus, given identical load capacitances (20 fF), the resistance in each system will become the most significant factor that will affect the energy dissipation of a given adiabatic logic circuit. Correspondingly, the differing drive currents (and thus R_{ch}) of each device type (for a given V_{DD}) are expected to correlate to the energy per cycle exhibited by the adiabatic circuit. However, at ultra-low voltage, we note that the drive current of thermionic emission-based MOSFETs is governed by the subthreshold current, as given by [3], [15]:

$$I_{sub} = Ae^{\frac{q(V_{GS}-V_{th})}{mkT}}\left(1 - e^{\frac{-q(V_{DS})}{kT}}\right), \quad (7.10)$$

where A is a device related factor, V_{th} is the threshold voltage, T is the temperature, k is Boltzmann's constant, and m is the body effect factor. The channel resistance can then be derived from Eq. 7.10, leading to:

$$R_{ch} = \frac{dV_{ds}}{dI_{sub}} = \frac{1}{A'}e^{-\frac{q}{kT}\left(\frac{1}{m}(V_{GS}-V_{th})-V_{DS}\right)}, \quad (7.11)$$

Thus, the adiabatic loss of thermionic emission-based devices can be calculated by inserting Eq. 7.11 into Eq. 7.7 and replacing V_{GS} with V_{DD}, *i.e.*:

$$E = \frac{CR_{ch}}{T}CV_{DD}^2 = \frac{C^2}{A'T}e^{-\frac{q}{kT}\left(\frac{1}{m}(V_{DD}-V_{th})-V_{DS}\right)}V_{DD}^2 \quad (7.12)$$

$$E \propto e^{-\frac{q}{kT}(V_{DD})} \times V_{DD}^2. \quad (7.13)$$

From Eq. 7.13, one can clearly observe that the adiabatic energy loss term simultaneously depends quadratically on V_{DD} as well as decays exponentially in proportion to V_{DD}. In other words, the increased channel resistance negates the quadratic reduction in energy loss due to V_{DD} scaling, resulting in a weak dependence of the energy per cycle in HP FinFET-based adiabatic logic on the supply voltage, as shown in Figure 7.8(a). Conversely, from Figure 7.8(a) one can find that the energy per cycle of a conventional inverter decreases with decreasing V_{DD} due to the nominal quadratic dependence of energy dissipation on V_{DD} for non-adiabatic processes. On the other hand, NBG TFET-based adiabatic logic exhibited a significant decrease in energy per cycle as a function of reducing supply voltage, as shown in Figure 7.8(b). As previously discussed, this is a result of the low threshold voltage of TFET devices, allowing for device operation in the saturation regime at ultra-low operating voltages. Consequently, and unlike thermionic emission-based FETs, TFETs do not experience an exponential increase in channel resistance when operating at $V_{DD} < 0.6$ V, resulting in reduced adiabatic losses.

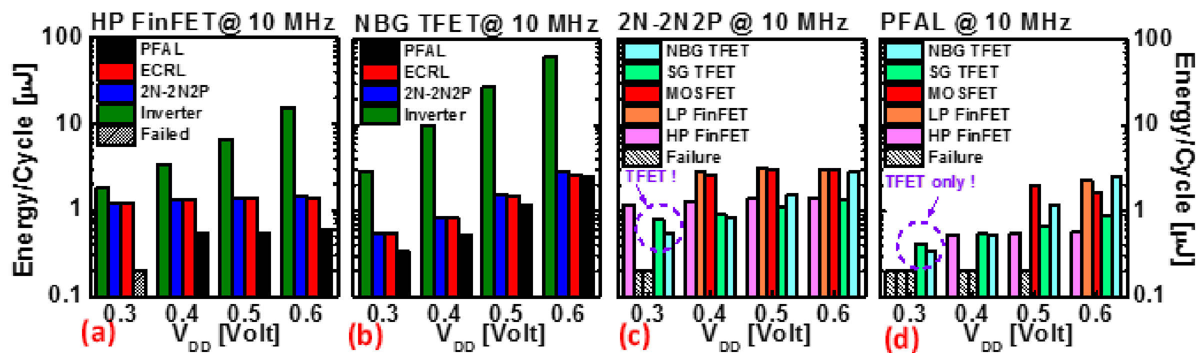

Figure 7.8 Energy per cycle as function of V_{DD} for (a) HP FinFET and (b) NBG TFET AL designs at 10 MHz. Comparison of energy consumption for (c) 2N-2N2P and (d) PFAL using different devices as function of supply voltage at 10 MHz.

Figs. 7.8(c) and 7.8(d) shown the energy dissipation per cycle for 2N-2N2P and PFAL designs utilizing each device type and operating voltage hitherto mentioned. As discussed above, thermionic emission-based devices exhibited weak relations between supply voltage and energy dissipation. On the contrary, tunneling-based devices exhibited continued voltage scaling of energy dissipation due to their enhanced drive currents at ultra-low operating voltages. Moreover, at $V_{DD} = 0.4$ V and below, NBG TFET-based adiabatic logic was found to

provide the lowest energy dissipation due to the high I_{ON}, and therefore lower channel resistance, of NBG TFET devices.

Figure 7.9(a) benchmarks the energy/cycle as a function of FET-type and adiabatic logic circuit design for an operational frequency of 10 MHz. The horizontal red lines are a guide for

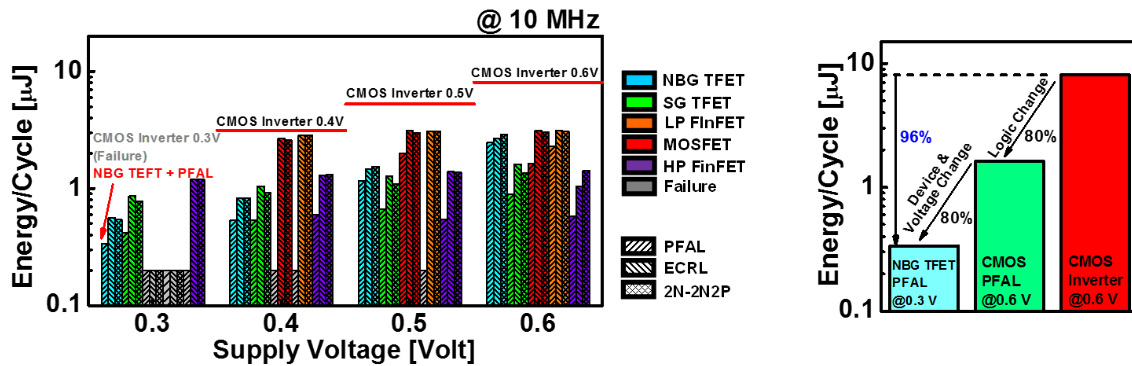

Figure 7.9 Energy dissipation for each AL design, device-type and operating voltage for f = 10 MHz (*i.e.*, IoT application frequency). NBG TFET-based PFAL exhibits the lowest energy consumption at 0.3 V. (b) Optimized TBAL energy/cycle benchmarked with conventional logic.

the eye representative of the baseline energy dissipation of planar CMOS inverters at each investigated supply voltage. One can find that at V_{DD} = 0.3 V, the high channel resistance of conventional MOSFET devices significantly increased the adiabatic circuit charging and discharging times such that the output node could neither be fully charged nor discharged, thereby leading to functional failure. In contrast, the more optimal TFET-based designs, in particular the NBG TFET-based PFAL design, provided unhindered adiabatic logic circuit functionality at low operating voltages due to the increased I_{ON} and lower channel resistance of TFET devices operating at low V_{DD}.

7.7. *TBAL Performance Degradation due to TFET Non-ideality*

In the preceding sections, we have estimated the energy reduction offered by adopting TBAL utilizing ideal TFETs, i.e., without considering parasitic effects such as interface charge and

contact resistance. However, in reality, TFET non-ideality is expected to undermine the overall performance of TBAL. In this regard, there are three important factors to consider when analyzing the impact of TFET non-ideality on TBAL operation, namely: (i) interface trap states at the dielectric/semiconductor interface; (ii) gate overlap of the source; and (iii), contact resistance. Interface traps at the oxide/semiconductor interface have a considerable impact on SS, as discussed in *Chapter 2*, particularly when utilizing high-κ dielectrics. To this end, we will investigate the impact of utilizing Al_2O_3 as a gate dielectric for the complementary TFET designs proposed in *Chapter 6*. For n-type TFETs, the channel consists of the InGaAs/Al_2O_3 heterointerface, whereas for p-type TFETs, the channel consists of the ε-Ge/Al_2O_3 heterointerface. The corresponding interface trap densities as a function of energy (D_{it}) for Al_2O_3 on InGaAs [21] and Ge [22] are shown in Figure 7.10 along with Gaussian fittings of the same. Contact resistance (R_c) has also been taken into account, wherein titanium (Ti) is here considered for both Ge (6.1×10^{-8} Ω-cm^2) [23] and InGaAs (4×10^{-8} Ω-cm^2) [24] due to its low contact resistance to each material (parenthesis). Lastly, a 3nm gate oxide overlap (t_{ol}) at the tunnel interface (source/channel) [25] is also modeled in the following analysis.

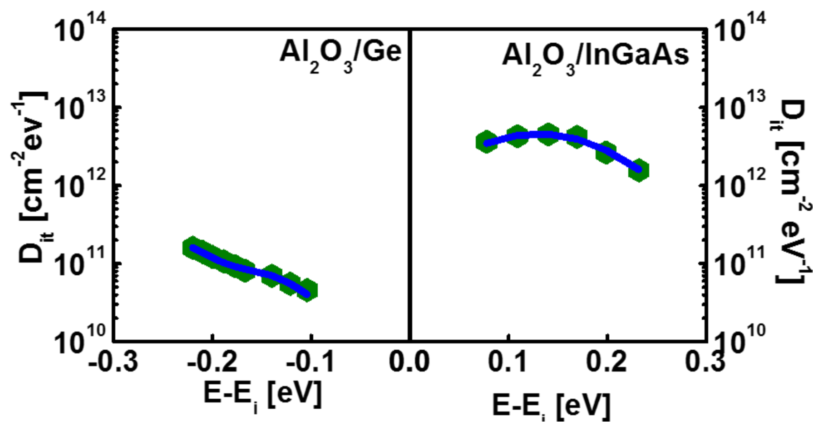

Figure 7.10 D_{it} distribution for Al_2O_3 on Ge and InGaAs as function of energy.

By considering these parasitic factors, the simulated I-V results for n- and p-type 3% strain Ge/InGaAs TFETs are shown in Figure 7.11. With respect to n-type TFETs, D_{it} detrimentally effects SS, whereas R_c has a limited impact on I_{ON}. On the other hand, with respect to p-type TFETs, there is no significant deterioration in device performance when incorporating, D_{it} and R_c. This is due, in part, to the reduction in D_{it} as a result of the incorporation of an ultra-thin GeO_x interfacial passivation layer at the Al_2O_3/Ge interface. Moreover, Ti provides low contact resistance for both Ge and InGaAs. From Figure 7.11, one can find that the major influence on TFET I-V characteristics is the introduction of the gate oxide overlap (t_{ol}) at the source/channel interface. This 3 nm extension over the source results in the gate voltage being dominate at the tunneling interface, thereby reducing the tunneling probability and degrading both I_{ON} and SS. On the other hand, p-type TFETs were found to be immune to the detrimental effects of oxide overlap due to the wider bandgap of the InGaAs source. Consequently, evaluation of non-ideal n- and p- type TFET behavior revealed a 2.59× current mismatch between n- and p-type devices, which leads to weaker pull down network.

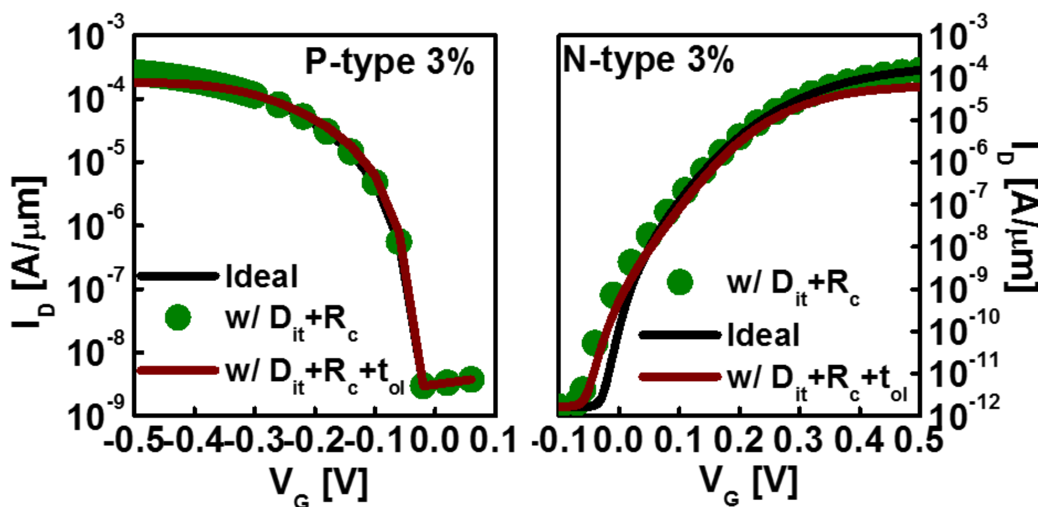

Figure 7.11 I_D for p-e and n-type 3% strain Ge/InGaAs TFETs incorporating interface trap states (D_{it}), contact resistance (R_C), and a 3 nm gate oxide overlap, with respect to the source, as a function of gate voltage.

Figure 7.12 shows the energy dissipation for PFAL when using ideal and non-ideal TFETs (NI-TFETs). One can find from Figure 7.12 that the energy dissipation of non-ideal TFET-based PFAL is higher than that of the ideal TFET-based design, and moreover, that the optimal frequency increases beyond the frequency range for IoT applications. This is due to the inability of non-ideal TFETs to provide sufficient I_{ON} (hence suffering from increased adiabatic loss) as well as their larger leakage current (hence increased leakage loss). Consequently, within the 10 MHz – 20 MHz frequency window, NI-TFET-based PFAL were found to have higher energy/cycle as compared to standard CMOS. As a consequence, the further application of TBAL to IoT applications will require careful investigation of TFET non-idealities in order to minimize energy/cycle and maintain ultra-low voltage performance scaling.

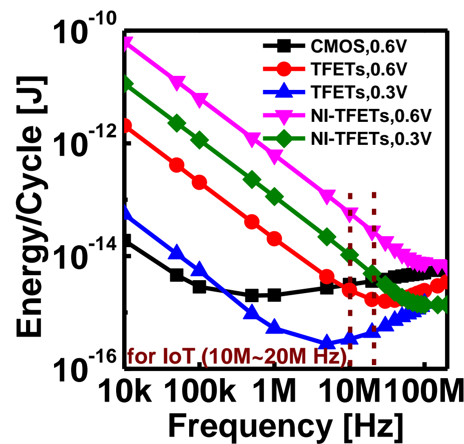

Figure 7.12 Energy/cycle for TFET-, non-ideal TFET- (NI-TFETs), and CMOS-based PFAL as a function of operating frequency.

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Chapter 8

Conclusion and Future Prospects

8.1. Summary

This thesis provides an overview of tunnel field-effect transistors from the selection of material systems to applications in memory and logic circuits. In *Chapter 1*, it is shown that there is an urgent need for ultra-low voltage and ultra-low power systems for IoT applications. Further, TFETs have been proposed and predicted to be a steep-slope-switch under ultra-low voltage conditions while maintaining sufficient drive current. In *Chapter 2*, we discussed the design criteria for an ideal TFETs. To achieve sub-60mV/decade, the criteria are summarized below:

(i) High tunneling probability. To obtain high drive currents, TFETs must have high tunneling currents. Both GaAsSb/InGaAs and Ge/InGaAs systems are potential candidates for providing high tunneling probability by using staggered gap heterointerface while maintain lattice match.

(ii) High quality heterointerface. Band tail states provide uncontrolled leakage paths and degrade device SS. As a result, doping control and growth control at heterointerface are critical to reduce density of band tail states.

(iii) High κ dielectric. To obtain better gate control to the channel, high κ dielectric should be used due to reduction of effective oxide thickness (E_{OT}) and maximization of oxide capacitance (C_{OX}).

Following the aforementioned criteria, in *Chapter 3*, the superior properties of GaAsSb/InGaAs heterointerface has been demonstrated. High-quality broken gap strain

balanced InAs/ GaSb multilayer structure, grown using solid source MBE, with InSb-like interfacial layer were demonstrated by analyzing structural, morphological, and band alignment properties. Thus, one can tailor the energy barrier of internally lattice matched GaAsSb/InGaAs heterointerface by precisely controlling the growth sequences of antimony- and arsenide-based material systems for future TFETs or detector applications.

In *Chapter 4*, we examine the suitability of Al_2O_3 (high-κ) for InGaAs/GaAsSb TFETs. X-ray photoelectron spectroscopy was used to determine the chemical state evolution as a function of surface pre-clean and passivation, as well as valence band and conduction band offsets, energy band parameters, and bandgap of atomic layer deposited Al2O3 on GaAsSb. A valence band offset >2 eV for all Sb compositions indicates the potential of utilizing Al_2O_3 on GaAsSb for p-type metal-oxide-semiconductor device applications. Moreover, Al_2O_3 showed a conduction band offset of ~2 eV on GaAsSb, suggesting Al2O3 dielectric can also be used for n-type MOS device applications.

In *Chapter 5*, we proposed a strained Ge/InGaAs TFETs and predicted its performance using numerical device simulation. Both n- and p-type H-TFETs exhibited a significant enhancement in I_{ON} (18.6× and 16.9×, respectively, at 3% strain) and which was attributed to both increased in strain and band discontinuities at the ε-Ge/InGaAs source–channel heterointerface. The Ge-based H-TFETs show great promise for low-power complementary TFET logic due to their ability to leverage improved channel carrier mobility and a tunable E_{beff}.

In *Chapter 6*, we proposed, simulated, and analyzed the performance of Ge/InGaAs based TFETs. Adoption of a 7T SRAM cell architecture resulted in a reduction in read delay time. The ε-Ge/InGaAs TFET-based 7T SRAM cell standby energy was observed to strongly depend on both operational voltage and the Ge strain level. Strain modulation between 1.5% and 3% revealed considerable reduction in cell standby energy when compared with similar, CMOS-based SRAM designs under ultralow voltage operation.

In *Chapter 7*, to fully leverage the steep-slope nature of TFETs, a novel, tunnel FET-based adiabatic circuit topology has been proposed and evaluated based upon its energy dissipation per cycle. By incorporating adiabatic logic functionality into standard combinational logic, an 80% reduction in energy/cycle was realized as compared to standard combinational logic. In addition, a further 80% reduction in energy/cycle was demonstrated by utilizing NBG TFET devices, resulting in a 96% reduction in energy/cycle as compared to conventional Si CMOS. Through co-optimization at the device and circuit levels, this work aims to enable energy-efficient computing architectures for IoT applications.

8.2. Prospects for Future Work/Research

In order to fully exploit the advantages of TFET devices, additional research can focus on the following subjects:

(i) Material integration on silicon platform. The aforementioned material systems are heterogeneous to silicon which is the standard platform for all devices applications. Any promising buffer layers should be carefully redesigned to accommodate the lattice mismatch between silicon and desired active layer stacks. Furthermore, the buffer layers must confine dislocations and defects at different temperatures due to the harsh working conditions of IoT applications.

(ii) Surface passivation for antimony based materials. For mixed As/Sb material systems, high κ/InGaAs interface was intensively studied for several decade due to the suitability for photonic applications. However, passivation for GaAsSb still remains unknown. SbO_x is really notorious for Sb segregation under normal process temperature. This will further prohibit the usage of any applications which require antimony elements.

(iii) Special device designs for overcoming short channel effect. Scalability is always an issue for potential solution of post-CMOS applications. Some researchers point out TFETs might suffer from short channel effect due to pinning channel effect, as discussed in *Chapter 5*. As a result, special design strategies are necessary to overcome short channel effects.

(iv) Dynamic random access memory. In *Chapter 6*, we comprehensively studied the TFET based SRAM. The other massively used memory component in IoT chips are DRAMs. However, the unidirectional behavior of TFETs greatly deteriorates the refresh time and operation frequency of TFET based DRAMs. Therefore, redesign of TFET based DRAMs is necessary to realize complete TFETs devices on IoT chips.

(v) Digital adiabatic logic circuits based on TFETs. In Chapter 7, we only employed the simplest NOT gate for demonstrating the dramatic energy reduction of TBAL. To further verify the usage of TBAL, simulation of TFETs based digital array or function blocks are required.

Appendix

List of Publications

JOURNAL PAPERS:

[1] **J. -S. Liu**, M. Clavel, and M. K. Hudait, "Performance Evaluation of Novel Strain Engineered Ge-InGaAs Heterojunction Tunnel Field Effect Transistors", IEEE Transactions on Electron Devices 62 (10): 3223-3228 (2015).

[2] **J. -S. Liu**, and M. K. Hudait, "A Novel Tensile-Strained Ge/InGaAs TFET-based 7T SRAM Cell Architecture." IEEE Transactions on Electron Devices 64 (5): 2193-2200 (2017).

[3] **J.-S. Liu**, Y. Zhu, P. Goley, and M. K. Hudait, "Heterointerface Engineering of Broken-Gap InAs/GaSb Multilayer Structures", ACS Applied Materials & Interfaces 7: 2512–2517 (2015).

[4] **J. -S. Liu**, M. B. Clavel, R. Pandey, S. Datta, M. Meeker, G. A. Khodaparast, and M. K. Hudait,"Growth and characterization of metamorphic InAs/GaSb tunnel heterojunction on GaAs by molecular beam epitaxy", J. Appl. Phys. 119 (24): 244308-1-11 (2016).

[5] **J. -S. Liu**, M. Clavel, and M. K. Hudait, "Tailoring the Valence Band Offset of Al2O3 on Epitaxial GaAs1-ySby with Tunable Antimony Composition", ACS Applied Materials & Interfaces 7 (51): 28624-28631 (2015).

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[7] S. K. Saluru, **J.-S. Liu**, and M. K. Hudait, "Performance Analysis of TaSiOx Inspired sub-10nm Energy Efficient $In_{0.53}Ga_{0.47}As$ Quantum Well Tri-gate Technology" IEEE J. Electron Devices Society 5 : 496-503 (2017).

[8] P. Nguyen, M. B. Clavel, **J. -S. Liu**, and M. K. Hudait, ”Investigating FinFET Sidewall Passivation Using Epitaxial (100)Ge and (110)Ge Metal-Oxide-Semiconductor Devices on AlAs/GaAs″, IEEE Transactions on Electron Devices 64: 4457-4465 (2017).

[9] M. K. Hudait, M. B. Clavel, **J.-S. Liu**, A. Ghosh, N. Jain, and R. J. Bodnar, “Transport Across Heterointerfaces of Amorphous Niobium Oxide and Crystallographically Oriented Epitaxial Germanium,” ACS Applied Materials & Interfaces 9 (49): 43315-43324 (2017).

[10] **J. -S. Liu**, M. B. Clavel, and M. K. Hudait, “TBAL: Tunnel FET-Based Adiabatic Logic for Energy-Efficient, Ultra-Low Voltage IoT Applications.” (under review).