High Power Density and Overcurrent Protection Challenges in the Design of a Three-Phase Voltage Source Inverter for Motor Drive Applications

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ABSTRACT

The voltage source inverter (VSI) is certainly the most popular topology used in dc to ac power conversion. Virtually every commercial electric motor is driven by a VSI. There is a need for smaller and more efficient drives in high performance applications that is dictating unprecedented power density requirements on airborne motor drive systems. In reply to this need, higher switching frequencies are being sought and new switching devices like Silicon Carbide (SiC) JFETs have emerged. Although faster switching rates favor a reduction in the size of passive components and alleviate the current ripple in the inverter, a penalty is paid on switching losses. Owing to their low switching energy profile, SiC JFETs stand as promising candidates in high switching frequency environments. Their normally-on nature, however, raises a level of discomfort among designers due to the added complexities in the gate drive circuitry and the increased risk of dc bus shoot-through faults in voltage source inverters. Despite of these challenges the use of SiC JFETs continues proliferating in high power density applications. In an effort to study the new challenges introduced by this trend a 2 kW IGBT-based three-phase voltage source inverter operating at 65 kHz was designed, built, and tested. In addition a novel overcurrent protection residing in the inverter dc link is proposed in response to the concern of using normally-on devices in voltage source inverters. Successful hardware validation of both the VSI and the overcurrent protection circuit is supported with experimental results.

To my parents,
whose unconditional love and support
set the foundations of this work

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Chapter 1 INTRODUCTION

1.1 The Driving Force Behind Electric Motors

The development of efficient, compact, and low cost power conversion systems that has ever characterized the power electronics industry becomes more evident nowadays with the rise of portable electronic devices, renewable energy sources, electric vehicles and more electric aircrafts. It comes with no surprise that as we incorporate into the second decade of this millennium, challenges continue to emerge entailing the size, weight, and efficiency of power conversion systems. The latter is strongly palpable in the design of *motor drives* for high power density electric motors. Steadily, the electric motor continues to gain popularity over the long-established fuel engine due in part to the existing environmental concerns associated to global warming and the present oil crisis in the world. The electric motor offers a more efficient and environment friendly replacement to the traditional fuel engine. A vivid example of this is the development of more electric cars and aircrafts as well as the utilization of renewable energy sources. It becomes clear that as the interest in the electric motor increases, so does the need for high power density motor drives to operate them. Figure 1-1 depicts some applications that demand high efficiency and high power density motor drives. Also shown is the trend to reduce the volume and weight of power conversion units while maximizing power delivery (Figure 1-1e).

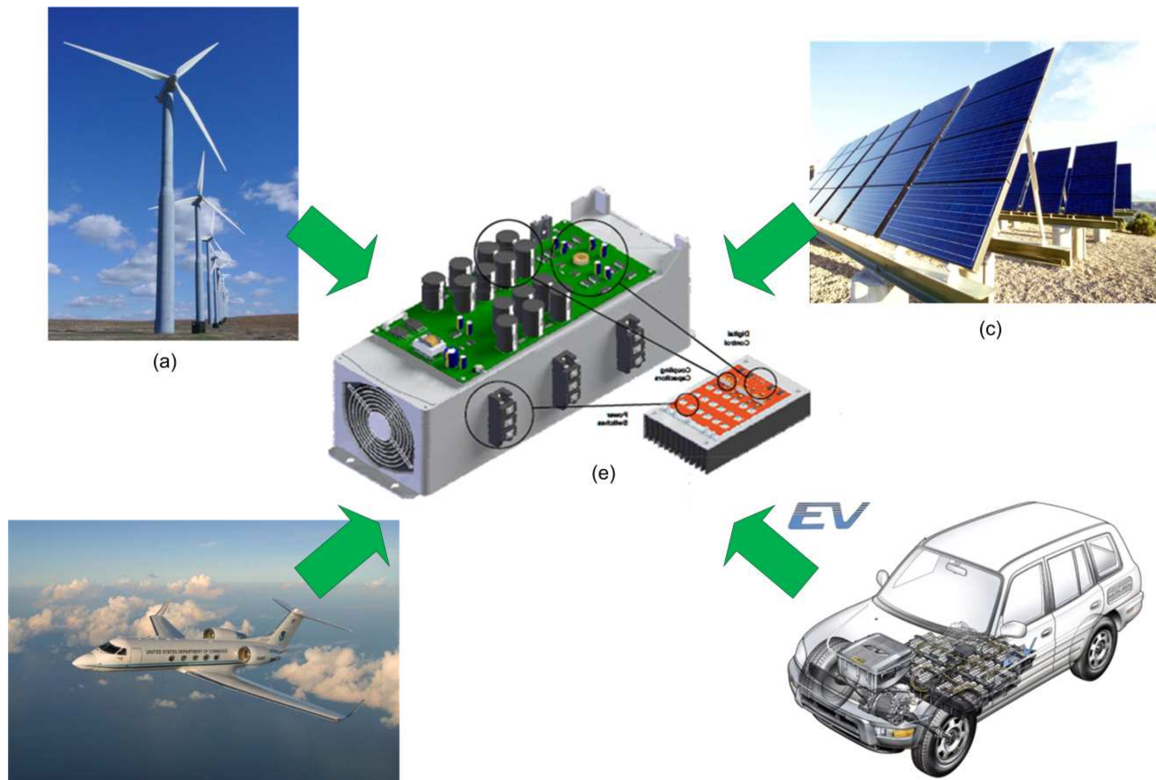


Figure 1-1: Typical applications that demand high power density. Renewable energy sources – wind (a) and solar (c), and means of transportation – aircrafts (b) and electric vehicles (d). Trend to compact and higher power density conversion units (e)

The motor drive in Figure 1-1e is an illustrative summary of the goals and challenges that motor drive designers face continuously: more power in smaller volume. To better understand these challenges it is proper to first define what a motor drive is and to describe its functionality. Motor drives are conversion units that condition the power from an ac voltage source – usually the ac mains – before transferring it over to the electric motor. Simply put, motor drives serve as intermediaries between the ac mains and the electric motor. Comprehensive analysis, however, reveals that motor drives are indeed compound systems. The block diagram of a typical three-phase motor drive is shown in Figure 1-2 as reference. It comprises a rectifying unit, a dc bus (or dc link), an

inverting stage, and a controlling unit. Typically, a filter stage precedes the rectifying unit as shown.

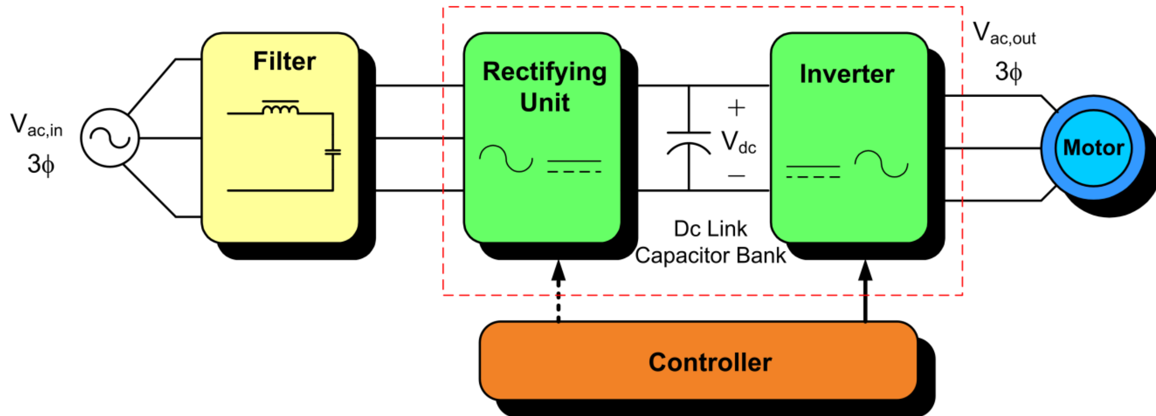
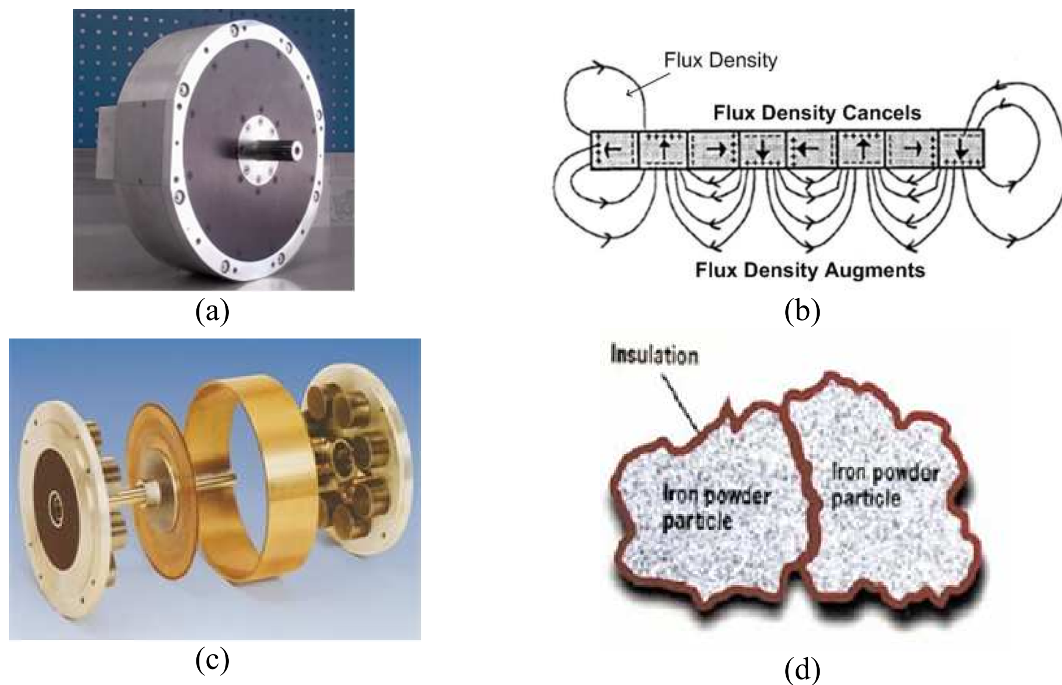


Figure 1-2: Block diagram of a typical motor drive

The system in Figure 1-2 depicts a voltage source based motor drive because its energy storage element is capacitive (dc link capacitor bank). In motor drives of this type operation is as follows: the rectifying unit – which can be either diode based (uncontrolled) or active (controlled) – converts the ac input voltage into a dc voltage with ripple. The ripple is then filtered by the dc link capacitor bank and a steady dc voltage is produced. The dc voltage is fed to the inverting unit where it is converted back to ac and delivered to the motor. The controller overlooks the operation of the motor drive and commands the action of the inverter and rectifying units (in the case of active rectifiers) allowing variation of the operating frequency and magnitude of the output voltage. This work is centrally devoted to the dc to ac conversion section of motor drives. As it is oriented towards the design methodology and challenges associated to the inverter unit of motor drive systems.

1.2 High Power Density Motor Drives

Power density in motor drives refers to the power-to-weight ratio of the converter-motor unit expressed in W/kg or W/lb. High power density motor drives exhibit more output power capability per unit of weight compared to standard motor drives and it is a desired trait in compact designs where low weight is required. In the aircraft industry low weight systems translate to fuel economy therefore high power density motor drives are most wanted in airborne applications. Achieving high power density is usually a result of incorporating a lightweight motor, utilizing compact and more efficient switching devices, or a combination of the two. From the motor standpoint a lot of progress have been reported in power density improvement with the introduction of the axial flux permanent magnet machine [1-3], Halbach magnet arrays for increased flux density [4, 5], ironless structure machines [6-8] and the use of new materials like soft magnetic composite [9, 10]. These advances are summarized in Figure 1-3.



(a) (b) (c) (d)

Figure 1-3: Advances in motor technology. Axial flux motor (a), Halbach magnet array (b), ironless motor (c), soft magnetic composite material (d)

On the other hand the advent of faster IGBTs and the development of new semiconductor materials like silicon carbide (SiC) have allowed researchers to push the envolope of inverter switching speeds. In addition to reducing the size of passive components like the dc link capacitors and filter inductors, it has been shown that increasing the switching frequency of the inverter 1) improves the quality of the line current (low THD) because of current ripple reduction [11], 2) reduces I^2R losses in the motor and inverter associated to current ripple [12], and 3) does not affect the overall motor iron losses for switching frequencies above 5 kHz [13]. From the motor perspective it makes sense to increase the switching frequency of the inverter, but given that switching losses are a function of frequency as shown in (1.1) it soon becomes clear that there is a practical limit that must be observed.

$$P_{sw} = V_g \times Q_g \times f_{sw} \quad (1.1)$$

Where V_g, Q_g and f_{sw} are the gate drive voltage, total gate charge of the switching device, and switching frequency, respectively.

Higher switching losses translate into bulkier heat sinks which end up upsetting the power density of the motor drive. Recent advances in semiconductor technology have allowed the commercialization of SiC diodes and the close commercialization of power switching devices like SiC JFETs. When compared to similar voltage rating silicon MOSFETs, SiC JFETs tops its counterpart with low specific on-resistance, high temperature operation, and fast switching capability [14, 15] hence allowing the benefits of high switching frequency to excel again. Researchers have assessed these benefits in dc-to-dc converters [16, 17], current-fed active rectifiers [14], and voltage source inverters for motor drives [18-21]. It is clear therefore that the trend in hard-switched power converters is moving towards higher switching frequency thanks to the better

properties of SiC over traditional silicon devices. This technology trend comes with its own challenges as discussed next in section 1.3.

1.3 Challenges in High Power Density Motor Drives

As new solutions are introduced to address high power density requirements new challenges emerge that require attention. For example high switching frequency helps reducing the size of passive components and lowering current THD in inverters, but on the other hand it is associated with increased switching losses, EMI noise, and computational burden on digital controllers. Yet another example of emerging challenges is the adaptation of gate drive and protection circuits to incorporate the SiC JFET – a normally-on device – into voltage source inverters. In the absence of gate drive voltage, SiC JFETs are in full conduction mode and require a negative voltage applied to its gate-source terminals to effectively bring the device to a non-conductive state as shown in Figure 1-4. This behavior is opposite to the traditional normally-off MOSFETs and IGBTs and therefore represents an opportunity for new gate drive and protection circuits.

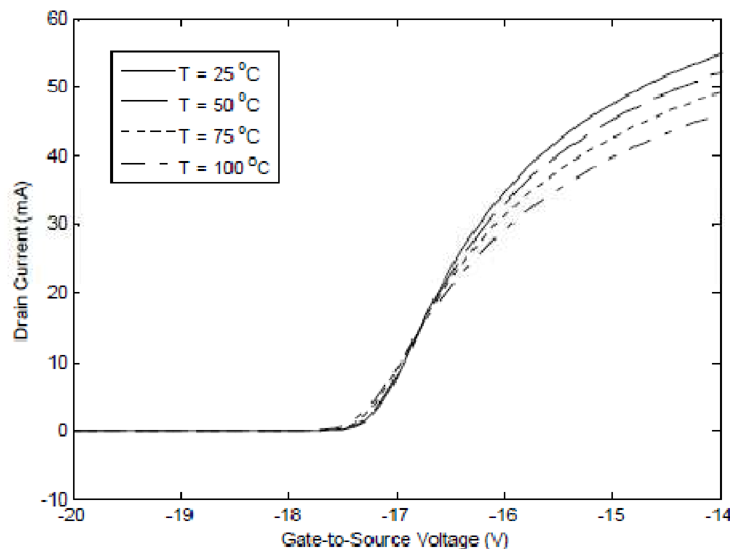


Figure 1-4: Turn-off voltage of a normally-on SiC JFET as published in [14]

Other challenges that stem from high power density requirements include high temperature operation, cooling mechanisms, compactness, and integration of both the motor and driving units in a single structure. The latter is being addressed at the Center for Power Electronics Systems with the Integrated Modular Motor Drive approach shown in Figure 1-5.

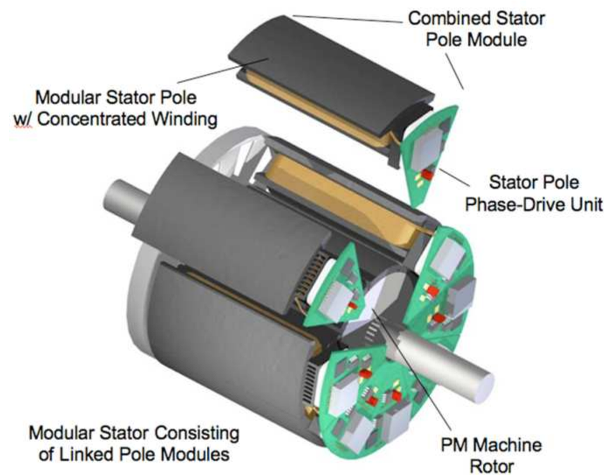


Figure 1-5: Integrated modular motor drive approach developed at CPES to increase motor drive power density

Achieving this level of integration requires smaller passives components, a task that can be accomplished by increasing the switching frequency of the rectifying and inverting units. In doing so the converter switching losses increase and so does the thermal management system, thus defeating the purpose of integration. This is where new switching devices like SiC JFETs fit in the picture with their better switching performance over traditional silicon devices. SiC JFETs however give rise to other challenges for being *normally-on* type devices as mentioned earlier. Therefore, a need exists for the study of high switching frequency inverters and overcurrent protection challenges motivated by 1) the need for high power density motor drives and 2) the introduction of normally-on devices to the domain of voltage source inverters.

In an effort to study the challenges introduced by fast switching and the utilization of normally-on devices in voltage source inverters a discrete 2kW IGBT-based three-phase inverter switching at 70 kHz was designed and tested in the lab. The challenges associated to component selection, board layout and high switching frequency operation of the VSI are assessed in Ch. 2 and 3. The VSI topology and operation are reviewed in the next section for completeness.

1.4 Voltage Source Inverter Topology

Conversion from a dc source to a three-phase ac output can be achieved with the power stage depicted in Figure 1-6. This topology is used extensively in motor drive systems and has become the standard for three-phase power conversion. The output of the VSI shown is connected to a three-phase resistive-inductive (RL) load. Each switching device has been identified with respect to its location in the power stage using the following notation: X_{yz}, where

$$X = \begin{cases} S, switch \\ D, diode \end{cases}; \quad y = \begin{cases} a, phase\ A \\ b, phase\ B \\ c, phase\ C \end{cases}; \; z = \begin{cases} p, positive\ dc\ link \\ n, negative\ dc\ link \end{cases}$$

For example, S_{ap} refers to the switch that connects phase A to the positive dc link $+V_{dc}$. S_{an} in the other hand connects phase A to the negative dc link $-V_{dc}$. The dc link is the energy storage section of the VSI. Typically the dc bus capacitance is achieved with a series/parallel combination of capacitors. Due to the high voltage contained in the dc link a split configuration of the dc link capacitor is often. The node at which the split capacitors connect together is commonly known as midpoint or node o.

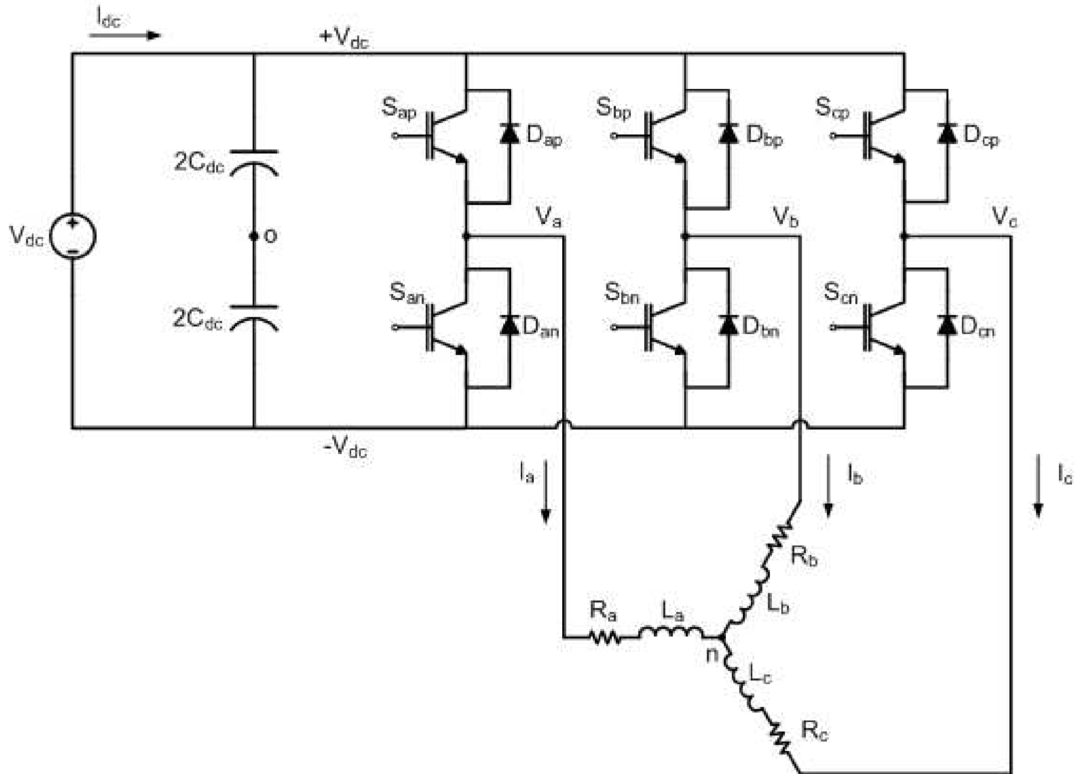


Figure 1-6: Voltage source inverter topology with RL load

1.5 Modulation

Modulation in power electronics converters is the action of varying the duty cycle of the converter switches at high switching frequency to generate a desired output voltage and operating frequency. The two most popular techniques to achieve this goal in voltage source inverters are sinusoidal pulse-width modulation (PWM) and space vector modulation (SVM). Sinusoidal PWM compares a low frequency target sinusoid against a high frequency carrier giving place to a series of pulses for driving the converter switches as depicted in Figure 1-7.

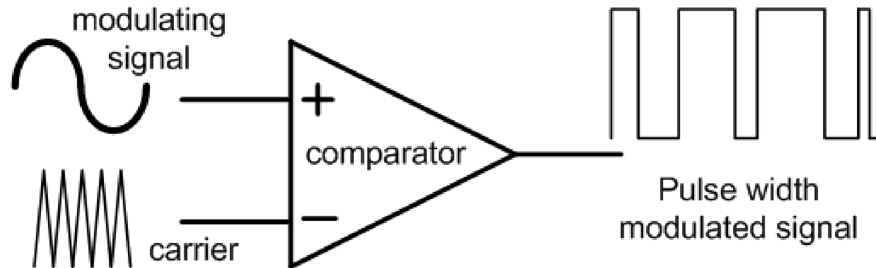


Figure 1-7: Sinusoidal pulse width modulation

SVM on the other hand allows explicit variation of the pulse placement providing advantages over the sinusoidal PWM technique. The discussion that follows in sections 1.5.1 and 1.5.2 is devoted to the SVM technique.

1.5.1. Space Vector Modulation

Space vector modulation (SVM) is an alternative method to carrier-based pulse width modulation (PWM) for determining switch pulse widths in ac to dc and dc to ac power converters. The commutation action of both modulation techniques is equivalent; however inherent benefits make SVM the modulation technique of choice in high performance applications [22]. The key advantage of SVM over its PWM counterpart is the explicit identification of pulse placement as an additional degree of freedom [23]. This liberty translates into other benefits, for example: 1) maximum bus utilization, 2) harmonic content reduction, 3) precise digital implementation, and 4) switching loss reduction [22, 24].

In a three-phase voltage source inverter the principle of SVM is based on the fact that the inverter can only adopt eight possible states while observing the following constraints: 1) the dc link must never be shorted and 2) the load currents must be continuous. In other words, no two switches of the same leg must conduct at the same

time and a conduction path must exist for the output current at all times. The eight legal switching states are described in Figure 1-8.

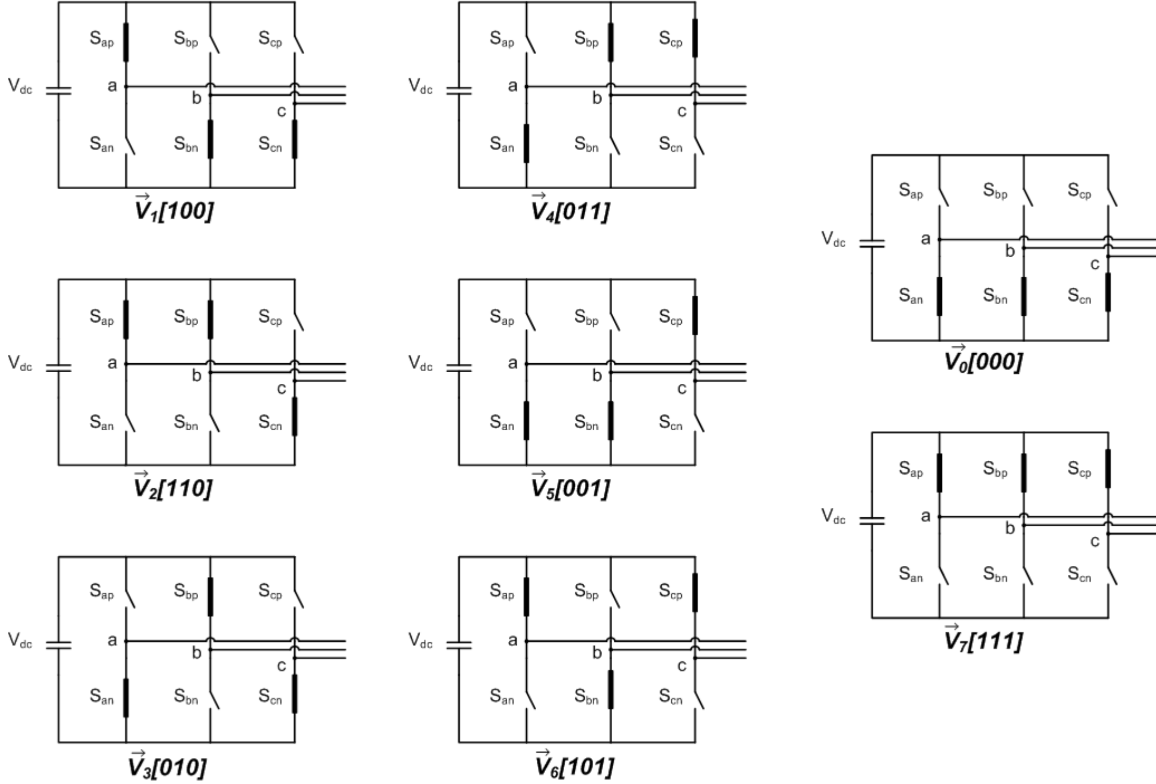


Figure 1-8: Switching states of a three-phase voltage source inverter

Each sate is represented by a space vector that describes the way nodes *a*, *b*, and *c* connect to the dc rail. The switching states defined by space vectors $\vec{V}_1$ to $\vec{V}_6$ suggest that line-to-line voltages V_{ab}, V_{bc}, and V_{ca} can adopt a magnitude of V_{dc}, 0 or $-V_{dc}$. For example, $\vec{V}_1[100]$ indicates that node *a* is connected to the positive dc rail and nodes *b* and *c* are connected to the negative dc rail. The line-to-line voltages generated by this space vector are:

$$V_{ab} = V_{dc}$$
$$V_{bc} = 0 \qquad (1.2)$$
$$V_{ab} = -V_{dc}$$

On the other hand, space vectors $\vec{V}_0$ and $\vec{V}_7$ can only generate a magnitude of 0, hence their name zero vector or null vector.

The eight space vectors exist on a stationary αβ plane as shown in Figure 1-9. Space vectors $\vec{V}_1$ to $\vec{V}_6$ are equally spaced from each adjacent vector by 60° and have magnitude of $\sqrt{2} \cdot V_{dc}$. The two zero vectors coexist at the center point as shown and have zero magnitude. By connecting the tip of each space vector a hexagon is obtained. Each adjacent vector comprises a sector of the hexagon (I through VI).

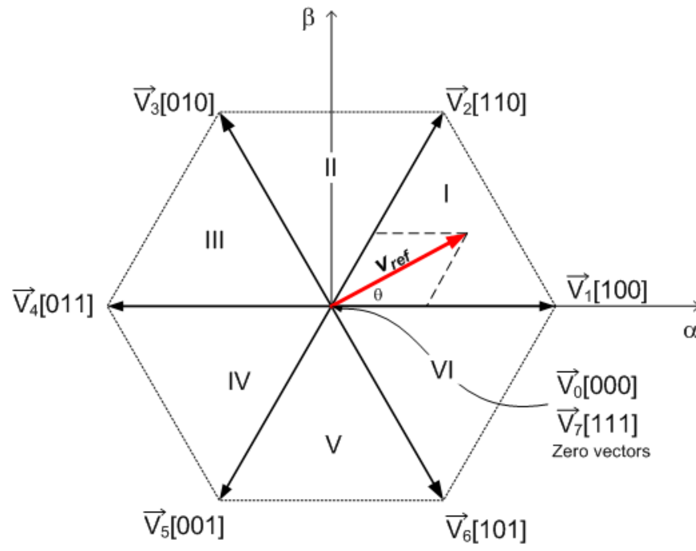


Figure 1-9: SVM state map

The modulator action of SVM is based on the averaging of a predetermined sequence of the space vectors $\vec{V}_0$ to $\vec{V}_7$ over a sampling period T_s in order to obtain the desired output voltage vector v_{ref}. For the example shown in Figure 1-9, v_{ref} lies on sector I and can be expressed as

$$v_{ref} = \vec{V}_1 \cdot T_1 + \vec{V}_2 \cdot T_2 + \vec{V}_{0,7} \cdot T_0 \tag{1.3}$$

Where T_1, T_2, and T_0 are the amount of time that $\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_{0,7}$ are applied during a sampling period, respectively. The sequence in which the space vectors are applied and the way their active time is distributed within a sampling period is the basis for different SVM schemes. Each sequence influences the converter performance in terms of harmonic distortion and switching losses differently.

1.5.2. Discontinuous SVM

The SVM technique adopted in this work to drive the VSI is the widely adopted *discontinuous* SVM or D-SVM. This sequence allows the sequential clamping of the inverter phase-legs to either the positive or negative dc link for 60° intervals each, thus reducing the number of commutations per switching cycle when compared to conventional SVM [22, 23]. Switching losses are further reduced by implementing an algorithm that selects the clamping phase-leg based on the current magnitude of each phase and not switching the phase leg with the highest current [25, 26].

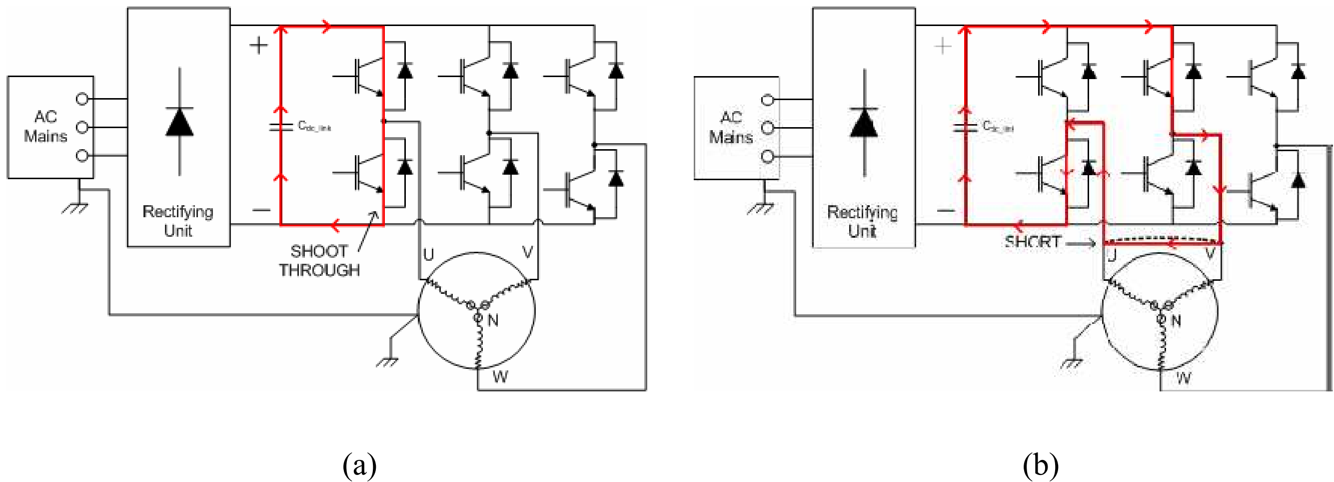
1.6 Overcurrent Fault and Normally-on Devices

The second half of this thesis is devoted to the study of overcurrent faults in phase-leg converters with particular attention to the shoot-through fault. The advent of silicon carbide (SiC) power switching devices has opened a new world of opportunities in the design of high power density converters. Higher junction temperature, faster switching, and low switching losses [14] are some of the advantages that SiC switching devices promise over its silicon counterpart. At the present time the most mature SiC switching device is the SiC JFET. Companies like SICED have developed and demonstrated normally-on SiC JFETs with low specific on-resistance and high junction temperature [15, 27]. Others have assessed the benefits of SiC JFETS in dc-to-dc converters [16, 17],

current-fed active rectifiers [14], and voltage source inverters for motor drives [18-21]. The *normally-on* property of SiC JFETs however generates some level of discomfort within the industry community due to the added complexities of the gate drive circuit. When no voltage applied between the gate and source terminals the natural state of SiC JFET is conductive (turned-on). To effectively turn off the device the gate drive must apply a negative voltage $-V_{gs}$. This property of the SiC JFET not only introduces complexity to the gate drive but also elevates the risk of shoot-through faults (shorting of the dc link) in voltage-fed phase-leg converters like the VSI. As stated in section 1.5.1, switches of the same phase-leg are not allowed to conduct simultaneously as this would generate short-circuit currents that could be fatal for the VSI. Such catastrophic scenario could trigger if a gate drive mishap involving either the loss of gate drive power or failure of the gate drive component occurs in a SiC JFET-based VSI. At such a level of risk and with technology moving forward with SiC devices overcurrent protection becomes imperative in high performance applications.

1.6.1. The DC Link Short-Circuit Fault

The toughest faults to contain and the most disastrous ones are perhaps those that arise when the dc link becomes shorted. In a motor drive inverter this condition can take place if any of the following occurs: 1) switches of a same phase-leg are switched *on* simultaneously as shown in Figure 1-10a or 2) two or more motor windings become shorted as shown in Figure 1-10b.



(a) (b)

Figure 1-10: DC link short-circuit faults. (a) Shoot-through fault and (b) line-to-line fault.

The former is typically referred to as dc link *shoot-through* because it describes the sudden increase in current magnitude as a result of shorting the dc link. In the second case (Figure 1-10b) the dc link is shorted through the motor winding. In both cases the low impedance path provided by the dc bus capacitor will allow a theoretically infinite amount of current that, if not interrupted in a timely manner, will destroy the inverter power devices involved in the fault. There is, however, a higher impedance path in a line-to-line fault than in a solid shoot-through fault, because in addition to the dc link capacitor and the impedance of the power stage switches, the fault current is limited by the motor winding impedance as well. Therefore, the shoot-through fault exhibits the highest current level and the most detrimental impact on the inverter and hence deserves special attention.

In the simplest form a shoot-through fault can be represented as the discharge of a RLC branch provided the dc power source that feeds the dc bus is neglected as shown in Figure 1-11b. Initially the dc link capacitor is charged to V_{dc}. The instant the shoot-through occurs C_{dc} dumps its energy into L_{eq} and R_{eq} as depicted in Figure 1-11c, where

C_{dc} is the total dc link capacitance, L_{eq} is the total stray inductance of the loop, and R_{eq} is the equivalent resistance of the loop as defined in (1.4), (1.5), and (1.6), respectively.

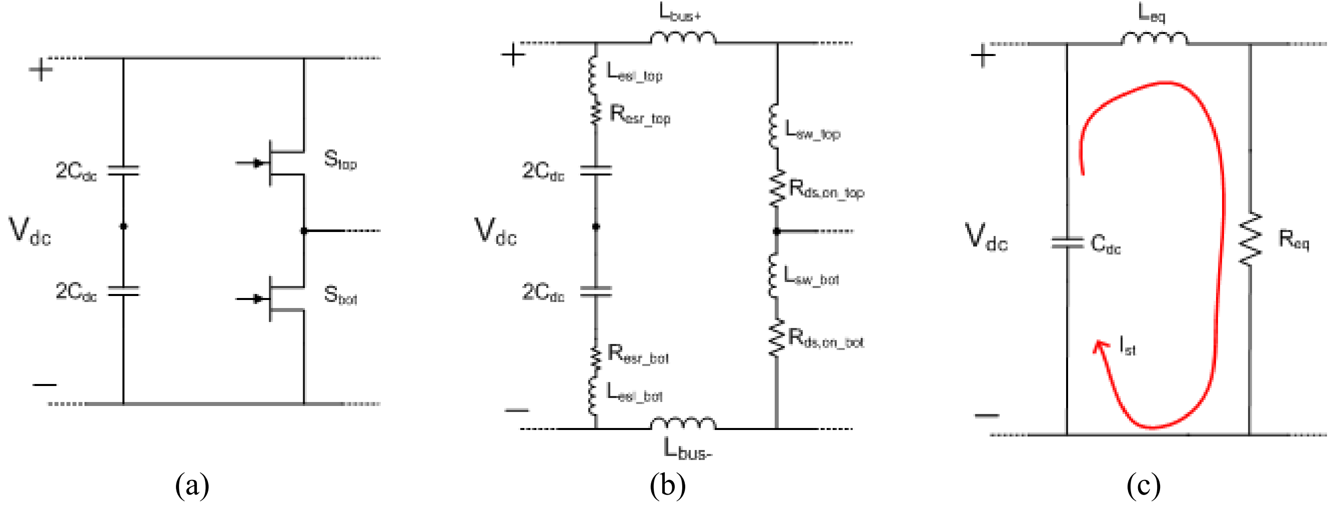


Figure 1-11: Representation of the shoot-through fault with a RLC circuit

$$C_{dc} = 2C_{dc} + 2C_{dc} \tag{1.4}$$

$$L_{eq} = L_{esl_top} + L_{esl_bot} + L_{bus+} + L_{bus-} + L_{sw_top} + L_{sw_bot} \tag{1.5}$$

$$R_{eq} = R_{esr_top} + R_{esr_bot} + R_{ds,on_top} + R_{ds,on_bot} \tag{1.6}$$

The only impedance seen by the short-circuit current I_{st} is that of the dc link capacitors and the intrinsic parasitic elements of the loop as shown in Figure 1-11b. The equation governing the magnitude of the peak shoot-through current of a RLC circuit is given by (1.7).

$$I_{st,pk} = \begin{cases} \dfrac{V_{dc}}{\omega_o L_{eq}} e^{-\frac{R_{eq}\cdot\pi}{L_{eq}\cdot\omega_o}}, \text{underdamped if } R_{eq}^2 < \dfrac{4L_{eq}}{C_{dc}} \\ \dfrac{V_{dc}}{R_{eq}}, \text{overdamped if } R_{eq}^2 > \dfrac{4L_{eq}}{C_{dc}} \\ \dfrac{2V_{dc}}{e \cdot R_{eq}}, \text{critically damped if } R_{eq}^2 = \dfrac{4L_{eq}}{C_{dc}} \end{cases} \tag{1.7}$$

Where ω_o is defined in (1.8) for the underdamped case as

$$\omega_o = \sqrt{\frac{1}{L_{eq}C_{dc}} - \left(\frac{R_{eq}}{2L_{eq}}\right)^2} \quad (1.8)$$

For increasing values of R_{eq} the peak magnitude of the short-circuit current decreases as shown in Figure 1-12.

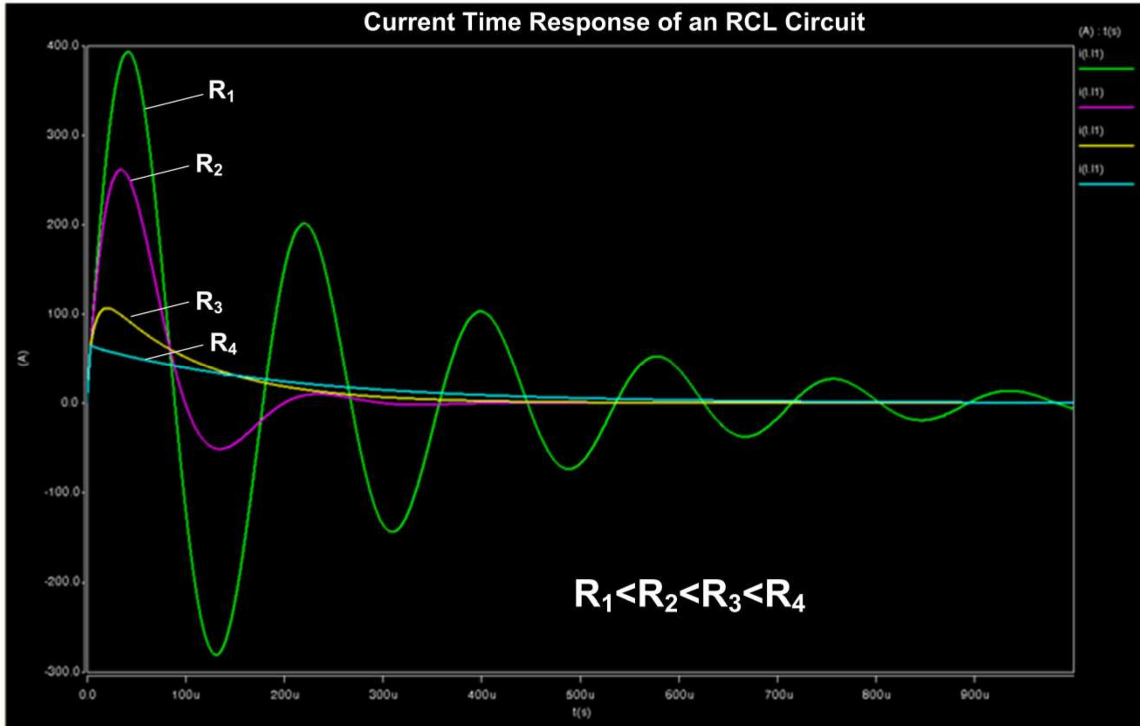


Figure 1-12: Time response of the short-circuit current in an RLC circuit for increasing values of resistance

Provided that the dc link parasitics are small compared to the dc link capacitance the shoot-through fault behaves as a second-order underdamped circuit. This is a reasonable assumption because typically R_{eq} is in the order of 10^{-3} and L_{eq} and C_{dc} are in the order of 10^{-9} and 10^{-6}, respectively. The behavior depicted in Figure 1-12 for increasing values of resistance will prove useful in the development of the innovative overcurrent protection system presented in Chapters 4 and 5.

1.6.2. Protection Circuits

With the increase of SiC JFETs in motor drive inverters shoot-through protection becomes imminent. Traditional overcurrent protection systems rely on fuses, expensive current sense transformers or shunt resistors. These methods may be acceptable on less demanding environments, but on high performance high power density airborne motor drives they fall short by adding unwanted inductance, weight, and power loss. Moreover the reaction time of some of these protection methods is too slow to detect and extinguish the shoot-through fault in time [28].

Various overcurrent protection circuits have been proposed in literature to address the normally-on issue introduced by the SiC JFET but most of them rely on protection meant for normally-off devices. For instance in [20], [29], and [30] desaturation detection circuits are implemented on SiC JFETs directly. The desaturation detection technique consists of monitoring the voltage drop across the switching device during conduction mode. In normal operation this voltage drop is low, but increases significantly during short-circuit according to the output transfer characteristic of the device. The protection circuit is set to trip at a predetermined level when the voltage across the device increases disproportionally. For example, an IGBT has a typical output transfer characteristic as shown in Figure 1-13. When the IGBT is driven at $V_{ge} = 10\ V$ the corresponding voltage drop across the device while operating at 20 A is $V_{ce} = 1.5\ V$. Point A is considered normal operation. A sudden rise in collector current due to an overcurrent event, i.e. a short-circuit, will cause the IGBT operating point to shift right along the output transfer characteristic curve. At 60 A (point B) V_{ce} has more than quadrupled with respect to point A, an indication of excessive current. The desaturation detection circuit in Figure 1-14 compares V_{ce} to a preset limit V_{ref} and commands the IGBT to turn-off when this

threshold is exceeded during the IGBT conduction period, hence protecting the power stage from excessive current.

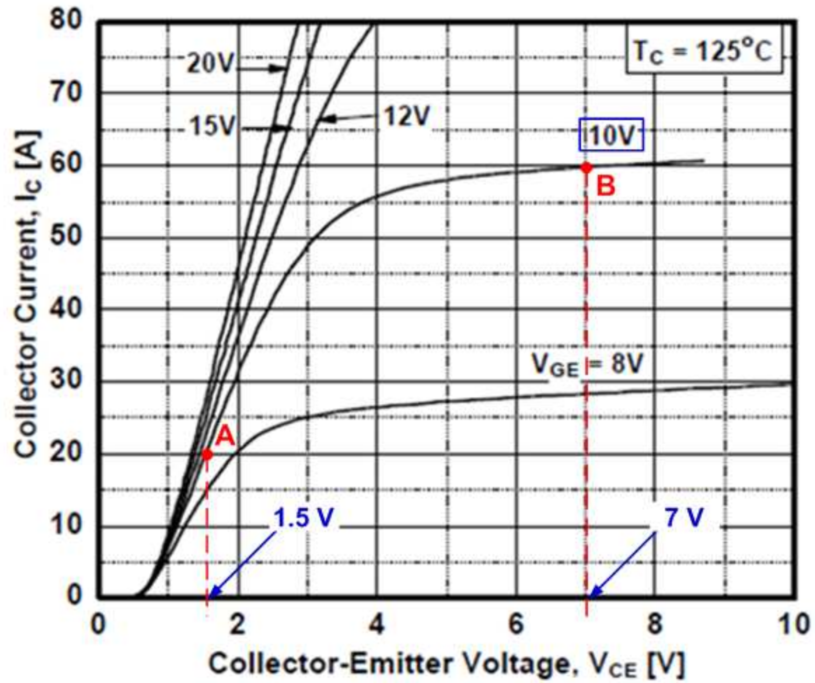


Figure 1-13: Typical output transfer characteristic of an IGBT

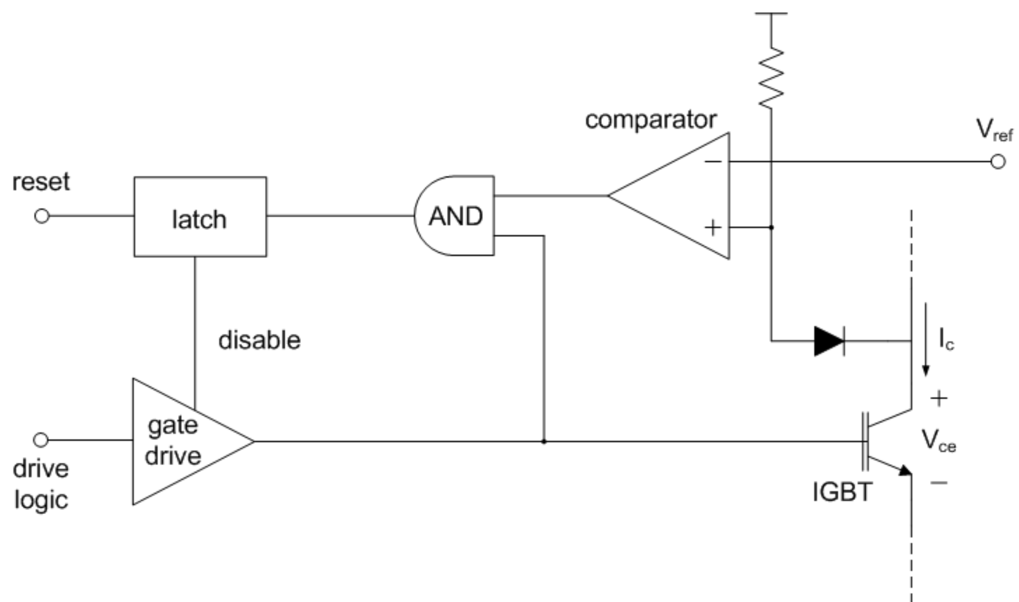


Figure 1-14: Desaturation detection circuit

Although desaturation detection has proven useful in IGBTs, there are uncertainties with this method when used with SiC JFETs. For example, setting the desaturation limit for the JFET is not a straightforward task considering that at the time of this publication the SiC JFET remains a prototype device. As such information like output transfer characteristic and pulse current rating are not always readily available from the manufacturer or even consistent among samples of the same batch as shown by a study in [21]. The lack of published data and moreover the variation of the device properties creates uncertainties about setting an appropriate current limit. Although desaturation is popular in three-phase inverters it exhibits yet another disadvantage: in order to protect the devices of a phase-leg each branch must be protected individually. That is, at least three individual desaturation circuits are needed to monitor the current in each inverter leg. This approach not only upsets the reliability of the converter, but also raises the converter part count and cost and reduces PCB real estate. The dc link protection circuit proposed in Chapter 4 and later tested in Chapter 5 tackles these challenges by 1) reducing the number of components and 2) making the protection circuit independent of the type of device (i.e. IGBT, JFET, MOSFET) used in the inverter power stage, hence increasing the versatility of the circuit.

1.7 Thesis At a Glance

This work has been organized in two main parts. The first part deals with the design aspects of a compact three-phase voltage source inverter. The second half of this work presents a novel overcurrent protection circuit for phase-leg converters like the VSI. In Ch. 2 the power stage design of a 2 kW VSI switching at 70 kHz is discussed in detail. This chapter includes the system specifications, selection of hardware components to

tackle the challenges presented in section 1.3, gate drive design, PCB layout, power dissipation calculation, and an in-depth description of the inverter thermal design. The VSI hardware validation is presented in Ch. 3 with particular emphasis in laboratory results and power density. Waveforms are shown for an IGBT-based 2 kW inverter operating at 65 kHz. Power density is assessed and a system weight breakdown is presented in this chapter. Chapter 4 is devoted to the discussion of a novel overcurrent protection circuit that resides in the VSI dc link. The mechanism behind the proposed circuit is presented and design aspects are covered. The dc link protection circuit proposed in Ch. 4 is further analyzed in Ch. 5 where experimental results validate the concept. Four variations of the protection circuit are presented with one of them yielding the faster reaction time. Chapter 6 collects the findings of this work and presents them in a summarized fashion. It also provides a collection of future work ideas that may aid the interested researcher in expanding the horizons of this thesis. Finally, supplementary information supporting the content of this work has been included in the Appendix.

Chapter 2 DESIGN METHODOLOGY OF A HIGH POWER DENSITY INVERTER

2.1 Design Specifications

To better understand the impact of high power density on motor drive inverters a 2 kW VSI was designed and built using the aircraft electrical system as baseline for the definition of the inverter design specifications. As such, inverter requirements resemble the power and frequency levels typical to airborne applications. Two purposes are served with this design: 1) study the impact of high power density requirements with regards to high switching frequency operation and selection of power stage components, and 2) provide a hands-on guideline to designers of similar circuits. The design specifications are summarized in Table 2-1

TABLE 2-1
INVERTER DESIGN SPECIFICATIONS

DC Link Voltage, V_{dc}	500 V
Line-to-Line RMS Voltage	350 V
Line RMS Current	5 A
Load Power factor	0.99 lagging
Nominal Output Power	2 kW
Max. Switching frequency, f_{sw}	70 kHz
Line AC frequency, f_{ac}	400 Hz

To maximize dc bus utilization the inverter is to operate with modulation index close to unity. In the linear region modulation index is defined in (2.1) as the ratio of the peak line-to-line output voltage of the VSI, V_m, and the dc link voltage V_{dc}.

$$M = \frac{V_m}{V_{dc}} \tag{2.1}$$

For the voltage specifications in Table 2-1 the modulation index equals 0.99.

The inverter is to feed a 2 kW resistive-inductive (RL) load with power factor of 0.99 lagging (at f_{ac}= 400 Hz). Full load operation will be demonstrated at high switching frequency up to 70 kHz.

2.2 A Discrete Approach

The ever increasing need for compact and lightweight designs in power electronics has forced semiconductor manufacturers to offer integrated versions of their discrete products. Today, the market that targets motor drive applications offer so called *co-pack* devices (IGBT and anti-parallel diode packaged together), single phase-leg modules, three phase-leg modules, and even intelligent power modules (IPM) that integrate IGBTs, anti-parallel diodes, gate drive circuitry, and protection features in the same unit. These advances have helped increase the power density of motor drives significantly. Despite the integrated solutions available today, a discrete approach was preferred in this study. The flexibilities of a discrete approach offered the following advantages:

- Access to individual devices in a module is seldom available; thus switching waveforms of individual devices cannot be studied
- Use of silicon carbide (SiC) schottky barrier diode (SBD) in the design
- Provides a means for identifying large weight contributors that upset power density in the design

For these reasons a discrete solution better suited the needs of this work and hence was selected as the preferred approach.

2.3 Power Stage Design

This section is devoted to the power stage design and hardware selection of the inverter. The step-by-step description of the design includes the selection of power semiconductor devices and gate drive design. The selection of hardware components for the inverter was driven by the need for high power density; therefore, particular attention was given to compactness and weight.

2.3.1. Power Devices Selection

Undeniably, the power switch and freewheeling diode constitute the back-bone of the inverter power stage and yet the main source of power dissipation. For this reason careful selection of power devices is crucial to not upset the inverter power density. Three main goals drive the power stage devices selection:

- high switching frequency capability- to minimize the size of passive components
- low power dissipation- to minimize thermal management components and achieve high efficiency
- compactness- light and small form factor devices are preferred for achieving high power density.

For a 2 kW design, the TO-220 package shown in Figure 2-1 represents a good trade-off between size and power capability.

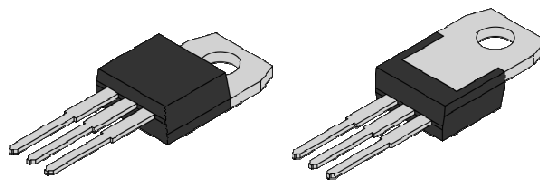


Figure 2-1: TO-220 package

Not only does each individual TO-220 package weighs a mere 1.44 grams, this package features one of the smallest leaded footprints for the given power level that are commercially available, thus saving PCB real estate and weight.

In addition to compactness the selection of power switches and freewheeling diodes was based on fast switching capability and low power dissipation as shown next in sections 2.3.1.1 and 2.3.1.2.

2.3.1.1. IGBT

In the mid-power range, IGBTs and MOSFETs are the most popular switching devices used in motor drives. In terms of switching speed MOSFETs are traditionally known for outperforming IGBTs. For the most part, this is due to the so-called tail current that IGBTs exhibit at turn-off. High voltage MOSFETs, in the other hand, suffer from large on-resistance $R_{ds,on}$, leading to increased conduction losses in applications requiring voltages in excess of 500 V. Therefore, IGBTs are the device of choice in mid-voltage (600 V – 1200 V) applications despite their tail current signature. Fortunately, advances in semiconductor technology have allowed Punch-through (PT) IGBTs to achieve switching speeds comparable to that of MOSFETs. PT IGBTs as opposed to Non-punch-through (NPT) IGBTs can achieve switching frequencies in excess of 100 kHz because the minority carrier lifetime responsible for their trademark tail current is shorter. This in turn decreases the total switching energy of PT IGBTs and allows high switching operation – a desired trait in this work. For comparison purposes, the switching energy of a PT and a NPT IGBT of similar current rating is shown in Figure 2-2.

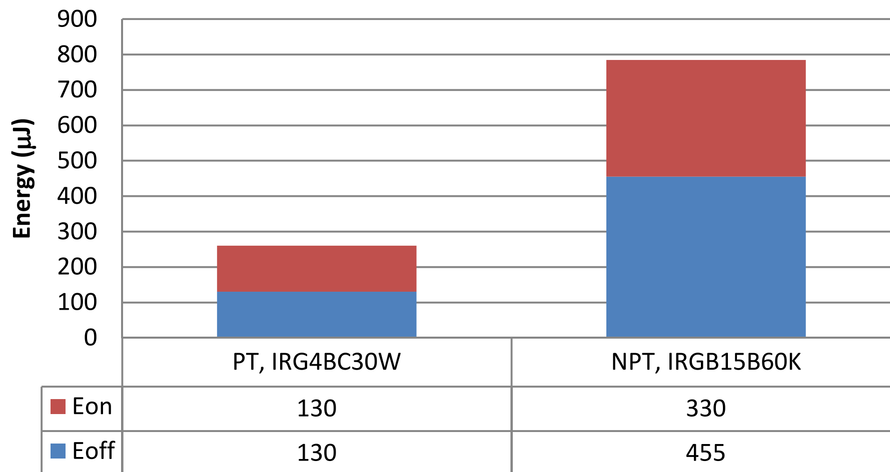


Figure 2-2: Switching energy comparison between PT and NPT IGBTs

The shorter tail current of the PT IGBT represents an improvement in turn-off energy, thus minimizing total switching losses in the inverter. The PT IGBT, however, has limited short-circuit capability as opposed to its counterpart: the non-punch-through IGBT. Although this appears a disadvantage, it will become apparent that using the overcurrent protection scheme proposed in Chapter 4 the IGBT can be protected effectively against short-circuit events.

Fast PT IGBTs are obtainable from semiconductor manufacturers like Microsemi, International Rectifier, and IXYS. Given that the IGBTs must block the entire dc link voltage (V_{dc}= 500 V) 600 V parts or higher are needed in the design. Five commercial 600 V fast PT IGBTs are compared in Figure 2-3 in terms of turn-off energy.

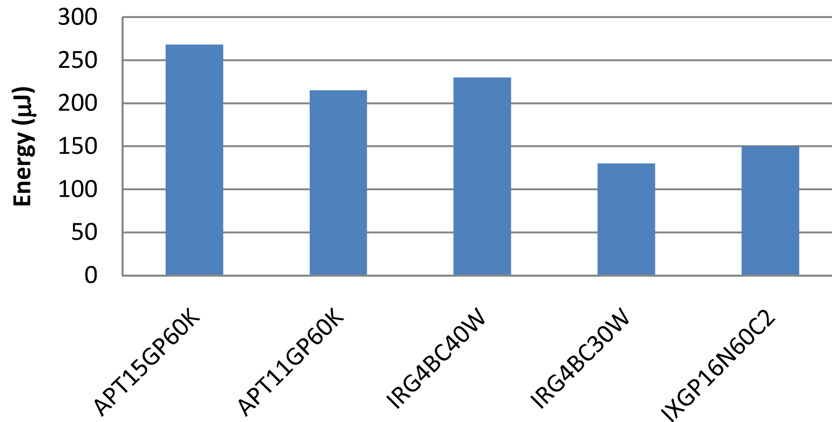


Figure 2-3: Turn-off energy, $E_{off,}$ of fast 600 V PT IGBTs from various manufacturers

The data in Figure 2-3 was obtained directly from the IGBT datasheet. It should be noted that the IGBTs are of similar current rating (12 to 20 A) and exhibit comparable saturation voltage, $V_{ce(on)}$ (2.5 to 3.0 V) as shown in Figure 2-4.

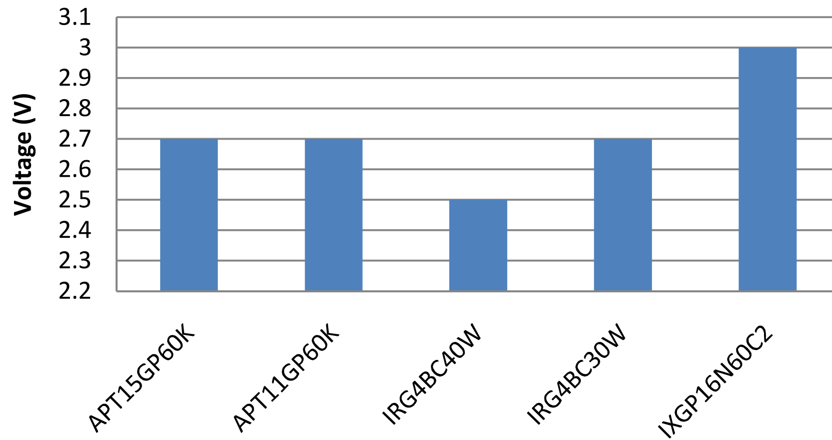


Figure 2-4: Saturation voltage, $V_{ce(on)}$, of various PT IGBTs

However, the test conditions – i.e. gate resistance and junction temperature – at which the data was recorded, vary slightly from manufacturer to manufacturer. Another fact that is worth mentioning is that the maximum switching speed of the IGBTs varies

among the three manufacturers as follows: IXYS, 100 kHz; International Rectifier, 150 kHz; and Microsemi, 200 kHz. In terms of switching speed, saturation voltage, and turn-off energy two attractive solutions can be identified: APT11GP60K (Microsemi), IRG4BC30W (International Rectifier). The characteristics of these IGBTs are summarized in Table 2-2.

TABLE 2-2
600 V FAST SWITCHING IGBTS

IGBT Part Number	Manufacturer	Switching Speed	$V_{ce(on)}$	E_{off}
APT11GP60K	Microsemi	200 kHz	2.7 V	215 μJ
IRG4BC30W	International Rectifier	150 kHz	2.7 V	130 μJ

The IGBTs exhibit similar traits and either one would have been a good fit for the inverter power stage. In the end the IGBT from International Rectifier was chosen (IRG4BC30W) for two reasons: its slightly better turn-off performance over Microsemi's IGBT and secondly, its availability at the time of building the prototype.

2.3.1.2. Freewheeling Diode

Whenever an inductive load is subject to switching, freewheeling diodes are needed to ensure uninterrupted flow of the current and hence avoid harmful inductive kickback. They are connected as shown in Figure 1-6: in anti-parallel fashion across the IGBT allowing current to flow during switching transitions. Freewheeling diodes, however, are known for increasing the turn-on switching losses of IGBTs due to the reverse recovery action of the diode. To address this issue, ultrafast silicon diodes have replaced general purpose diodes in motor drive applications. Although silicon Schottky diodes are inherently faster than ultrafast diodes, their use is limited to applications under 200 V due to the moderate field strength of silicon [31]. Favorably, recent advances in SiC

technology have enabled the development of SiC Schottky barrier diodes in both 600 V and 1200 V ratings with ultralow reverse recovery charge. Figure 2-5 shows experimental results of the reverse recovery phenomena reported in [32].

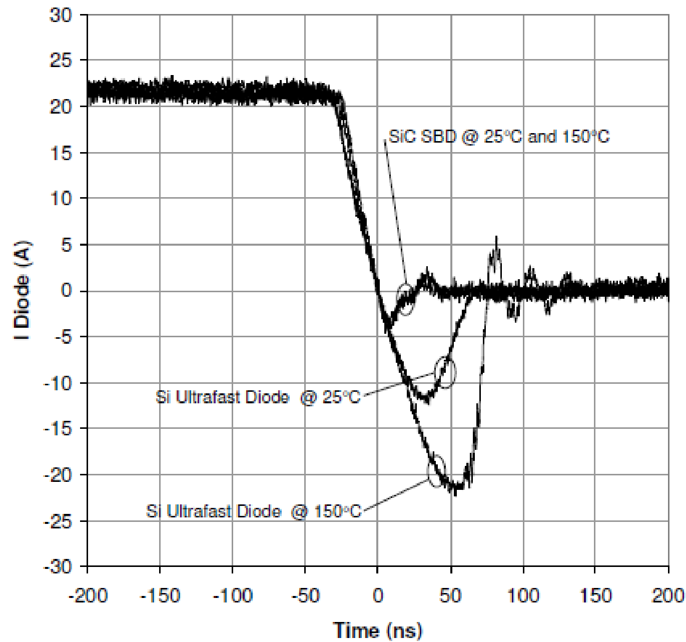
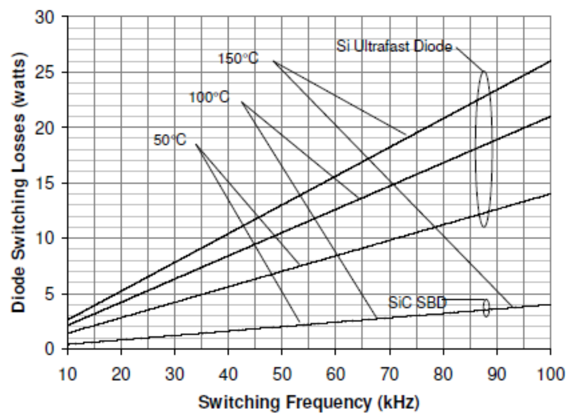
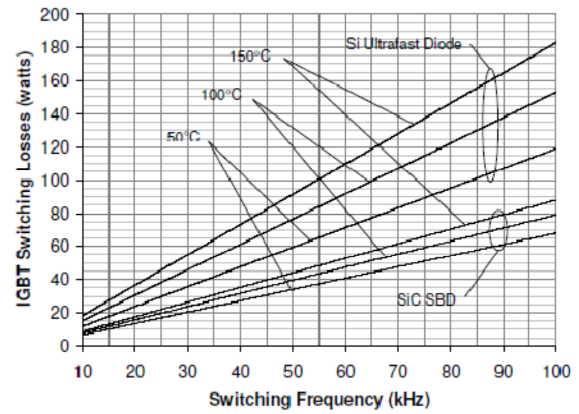


Figure 2-5: Reverse recovery phenomena of 600 V Si ultrafast and SiC Schottky diodes.

Figure 2-5 reveals an important trait of the SiC Schottky diode: nearly zero reverse recovery time. Moreover, reverse recovery of SiC Schottky diodes is not temperature dependent as is the case with silicon diodes. The current magnitude of the Si ultrafast diode appears to double from 25°C to 150°C and the overall recovery time increases. The virtual elimination of reverse recovery in SiC Schottky diodes translates into lower commutation losses in the freewheeling diode as well as in the IGBT. The improvement in switching losses can be seen in Figure 2-6 as published in [32].



(a)



(b)

Figure 2-6: (a) Diode and (b) IGBT switching loss comparison using Si Ultrafast and SiC Schottky diodes (as reported in [32])

The reduction of switching losses using SiC Schottky diodes is evident and makes them an attractive solution in high power density applications. The virtually zero reverse recovery of SiC Schottky diodes and the high field strength of SiC make them a perfect fit for motor drives. The inverter described in this chapter uses six prototype SiC Schottky barrier diodes (SBD) supplied by Infineon. These SBDs are rated at 1200 V and 15 A and exhibit virtually zero reverse recovery charge. At 5 A these SBDs have a typical forward voltage drop of 1.2 V [14].

2.3.2. Gate Drive Design

This section presents a step-by-step design of the inverter gate drive circuit based on the gate charge properties of the switching device. It is certain that the gate drive circuit is a vital part in any switching converter. Proper selection of components and good layout of the circuit makes the gate drive robust against electromagnetic interference and improves the switching performance (i.e. turn-on and turn-off times, switching losses).

2.3.2.1. Gate Drive Power

There are three key parameters that impact the design of the gate drive circuit:

- gate drive voltage V_g,
- gate charge Q_g, and
- switching frequency f_{sw}

These parameters are all related to the switching device and they determine the total gate drive power needed to switch the IGBT. The total gate drive power is the product of the three abovementioned parameters as expressed in (2.2)

$$P_g = V_g \times Q_g \times f_{sw} \tag{2.2}$$

The gate drive design begins by choosing the gate drive voltage at which the IGBT will be driven such that conduction losses are minimized. The selected IGBT is fully conducting when driven at 15 V. Therefore, V_g was set to 15 V in order to minimize conduction losses. Selecting a gate drive voltage greater than 15 V would only improve conduction losses marginally while adding the negative effect of increasing the total power dissipation of the gate drive circuit.

The second step in the gate drive design is to calculate the amount of power required to switch the IGBT. The total gate charge of the IGBT must be found at the conditions (voltage and current levels) at which the IGBT will operate. This information is extracted from the gate charge plot in the device datasheet as shown in Figure 2-7. At V_{ge}= 15 V, the total gate charge is 51 nC. The gate charge plot, however, shows the IGBT typical values and may not represent the worst case charge. Therefore, the maximum gate charge value provided in the *Switching Characteristics* section of the datasheet was used: 76 nC.

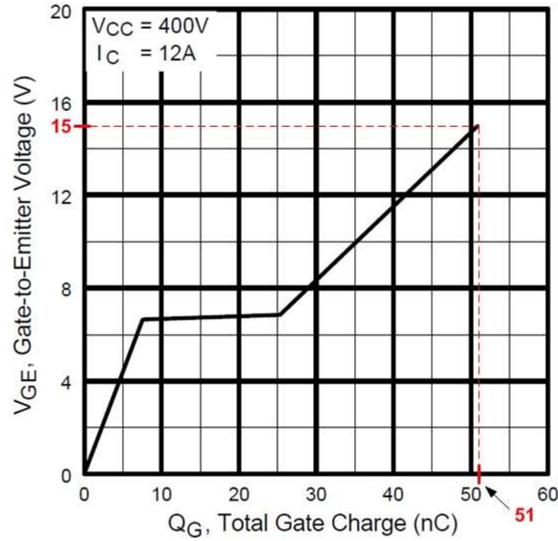


Figure 2-7: Gate charge versus gate-emitter voltage plot of IGBT IRG4BC30W

Lastly, the VSI is to be operated at a maximum switching frequency of 70 kHz. Inserting the corresponding values in (2.2) yields the power dissipated by each gate drive circuit:

$$P_g = (15) \times (76 \times 10^{-9}) \times (70 \times 10^{3}) = 79.8 \text{ mW}$$

Together, the six gate drive circuits consume nearly 0.48 W. As a critical part of the inverter power stage, each gate drive circuit must be powered individually by an isolated power supply. That is, six independent power supplies are needed to power each gate drive individually. Although this requires more PCB area and adds to the total weight of the inverter, it eliminates cross-talking (conducted noise) between gate drive circuits and isolates the gate drive power from the control power rail. More detail on the type of power supply used for powering the gate drive circuit is provided in section 2.4.3.

2.3.2.2. Gate Resistance

It is known that proper selection of the gate resistance R_g of a gate drive circuit is critical as it governs the turn-on and turn-off performance of the IGBT and therefore affects switching losses. It also dictates the amount of conducted and radiated noise

associated to the rise and fall times of the switch voltage and current. While increasing R_g reduces the sharp edges of these waveforms and therefore alleviates EMI pollution, switching losses on the other hand increase due to the slow charging of the gate capacitance. A clear tradeoff between switching losses and EMI noise accompanies the selection of R_g. In applications where low EMI noise is crucial, a trade-off must be made between the size of the EMI filter and that of the thermal management components. In this work, priority was given to switching losses to minimize the size and weight of the cooling system.

The plot in Figure 2-8 shows the total switching losses of the IGBT as a function of R_g as published in the device datasheet. This information allows selecting a gate resistance that yields a good tradeoff between switching losses and fast switching. In this design R_g= 15 Ω was selected, which keeps switching losses on the low end for the selected IGBT and yet allows fast charge and discharge of the gate capacitance.

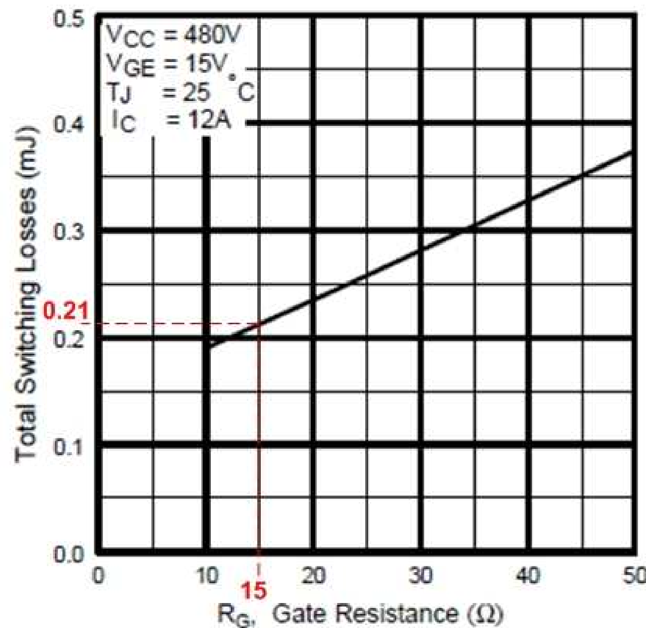


Figure 2-8: Total switching losses of device IRG4BC30W versus gate resistance

The time it takes to fully charge/discharge the gate capacitance is expressed in (2.3).

$$t_{ch} = 5 \times R_g \cdot C_{ge} = 5 \times R_g \cdot \left(\frac{Q_g}{\Delta V_g}\right) \tag{2.3}$$

Where, C_{ge} is the gate-to-emitter capacitance and ΔV_g represents the total gate drive voltage swing (0 – 15 V). With R_g= 15 Ω, Q_g= 76 nC, and ΔV_g= 15 V the total charging/discharging time of the gate is 380 ns. The peak gate current needed to turn-on and turn-off the IGBT is given by (2.4).

$$\mathrm{I_{g,pk}} = \left(\frac{V_g}{\mathrm{R_g}}\right) = 1\ \mathrm{A} \tag{2.4}$$

The gate drive circuit must source and sink a peak current of 1 A at turn-on and turn-off, respectively. The gate drive chip selection is described next.

2.3.2.3. Gate Drive Chip and Isolation Barrier

The gate drive circuit is the interface between the *power* stage and the *control* circuitry. Isolation is therefore required to avoid circulating currents that may compromise the integrity of the controller. In this design the opto-driver chip HCNW-3120 from Avago Technologies was selected to drive the IGBTs. This chip is a monolithic gate driver that provides optical isolation between the control signal and the power stage. In addition, this chip can be used to drive the IGBT directly as it can source/sink a maximum peak current of 2.5 A – sufficient to satisfy the peak gate current of 1 A. Lastly, this monolithic approach saves space and minimizes part count.

With the selection of the gate drive chip the gate drive circuit is complete. The final schematic of the gate drive circuit is shown in Figure 2-9. Note the use of bypass capacitors and common mode chokes at both the input and output of the gate drive circuit. Bypass capacitors help filter out the electrical noise (ac ripple) at the input and output of the gate driver chip. Common mode chokes in the other hand provide

attenuation of common mode noise caused by interactions in the power supply line. Adding a CM choke at the input side of each power supply minimizes interaction (cross-talking) in the 28 V rail among power supplies. Ferrite beads were added at the input and return line of each power supply to attenuate differential mode noise.

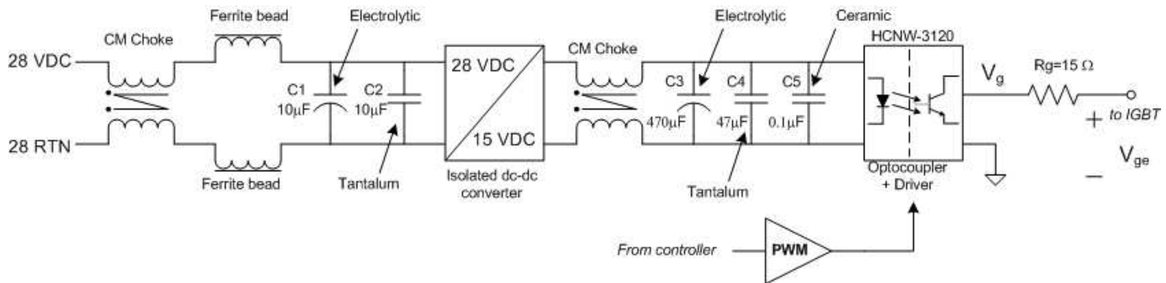


Figure 2-9: Gate drive schematic

2.3.2.4. Gate Drive Switching Performance

Proper operation of the gate drive circuit was verified by observing the gate-emitter voltage V_{ge} of each IGBT individually. The V_{ge} waveform is shown for the bottom switches of each phase-leg in Figure 2-10. Note that the magnitude of the gate drive voltage is 13 V approximately; enough to fully drive the IGBTs.

Figure 2-10: Gate drive voltages (bottom switches). 20 V/div, 10 μs/div

The switching performance was verified by inspecting the IGBT voltage V_{ce} and current I_c waveforms during full load operation. The switching waveforms of switch S_{an} (phase A, bottom IGBT) are shown in Figure 2-11. V_{ce} exhibits a clean waveform at both turn-on and turn-off. The IGBT current, on the other hand exhibits high frequency oscillation at turn-on and moderate oscillation at turn-off. There are two explanations for this behavior: 1) the relatively low gate resistance (R_g=15 Ω) and 2) sensitivity of the Rogowski coil. The low R_g allows faster switching and therefore higher di_c/dt and dv_{ce}/dt. The faster rise/fall time excites the parasitic elements (i.e. stray inductance in the IGBT pins and copper traces, IGBT junction capacitances) of the circuit causing high frequency ringing in the IGBT current.

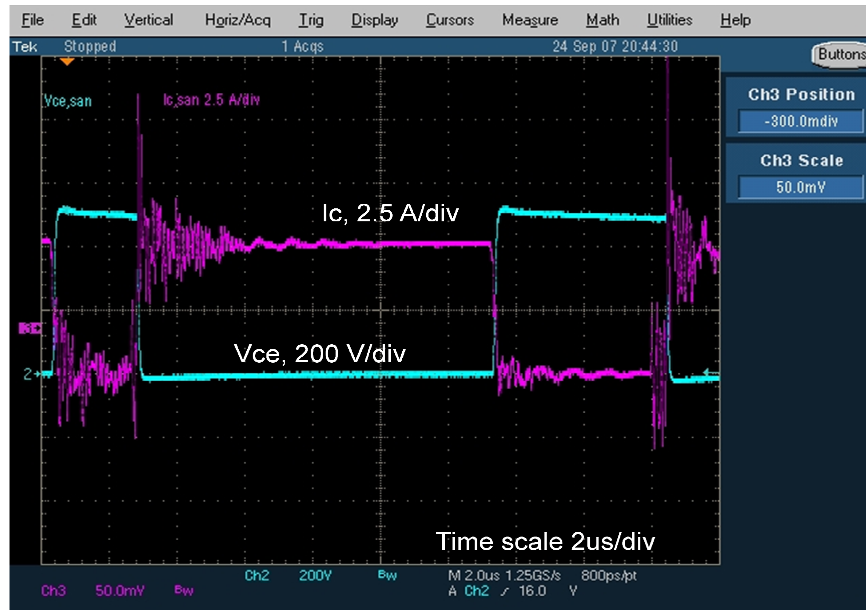


Figure 2-11: Switching waveforms of IGBT S_{an} at f_{sw}= 65 kHz. IGBT current I_c (light blue) and IGBT voltage, V_{ce} (magenta)

A Rogowski coil like the one shown in Figure 2-12 was used to measure the IGBT current. Despite the known advantages of the Rogowski coil, its sensitivity to EMI noise could have potentially introduced errors to the current measurement.

Figure 2-12: IGBT current measurement using Rogowski coil

Both effects combined, low R_g and the Rogowski coil EMI sensitivity, are responsible for the current switching performance observed in this section. The results obtained reveal that particular attention must be given to the length of copper traces to avoid undesired high frequency ringing.

To conclude the gate drive design topic, a protection feature added to the gate drive circuit is discussed in section 2.3.3. This important feature prevents accidental conduction of same phase-leg IGBTs as will be shown next.

2.3.3. Anti-shoot-through Logic

The gate drive has been enhanced with an *anti-shoot-through* circuit that prevents accidental turn-on of same phase-leg IGBTs (see Figure 2-13c). In essence, it does not allow two IGBTs on the same phase-leg to be commanded *on* simultaneously. The circuit is meant to protect against glitches or bugs on the controller side rather than turn-on's triggered by dv/dt on the power stage side. This protection is achieved using the logic described in Figure 2-13a. Note that when both IGBTs are commanded *on* simultaneously (shoot-through case) the output of the logic circuit $S_{p,out}$ and $S_{n,out}$ is low (Figure 2-13b), thus preventing the controller from mistakenly commanding a shoot-through event. Successful operation of the anti-shoot-through logic is verified in Figure 2-14.

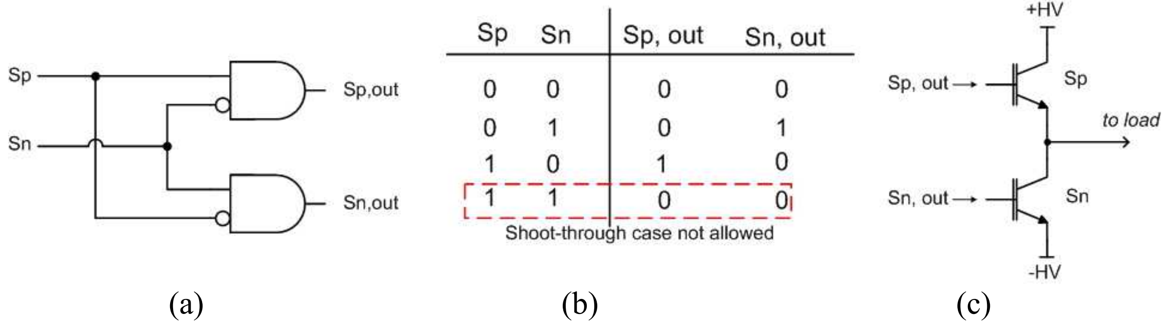


Figure 2-13: Anti-shoot-through logic (a), truth table (b), and phase-leg IGBTs (c)

Figure 2-14: Anti-shoot-through logic test for S_n = HIGH

The control signals S_p and S_n command the turn-on and turn-off of the top and bottom IGBTs in a phase-leg, respectively. Based on these signals the gate drive applies voltages $V_{ge,Sp}$ and $V_{ge,Sn}$ to the IGBTs. In Figure 2-14, S_p is pulsing high-low repeatedly while S_n is kept high, consequently, the gate drive circuit commands the bottom IGBT to turn on and off. On the other hand, the top IGBT never turns on because its turn-on signal coincides with S_n being high. The logic forbids both IGBTs from being on at the same

time; as a result $V_{ge,Sp}=V_{ge,Sn}=0$ during this period and a potential shoot-through is avoided.

With this the selection of power stage components and gate drive design is complete. The next section describes the printed circuit board (PCB) and layout of the inverter as well as the selection of other peripheral components.

2.4 PCB Layout

Detail of the inverter PCB layout and the selection of several hardware power stage components is provided in this section. The PCB was kept as compact as possible in the best interest to improve the power density of the inverter. At the same time proper clearance between conductors and traces was observed to ensure a reliable design.

The PCB consists of six layers – top, bottom and four internal mid-layers – of FR-4 material and copper as shown in Figure 2-15. Each layer exercises a particular function as depicted in Figure 2-15b.

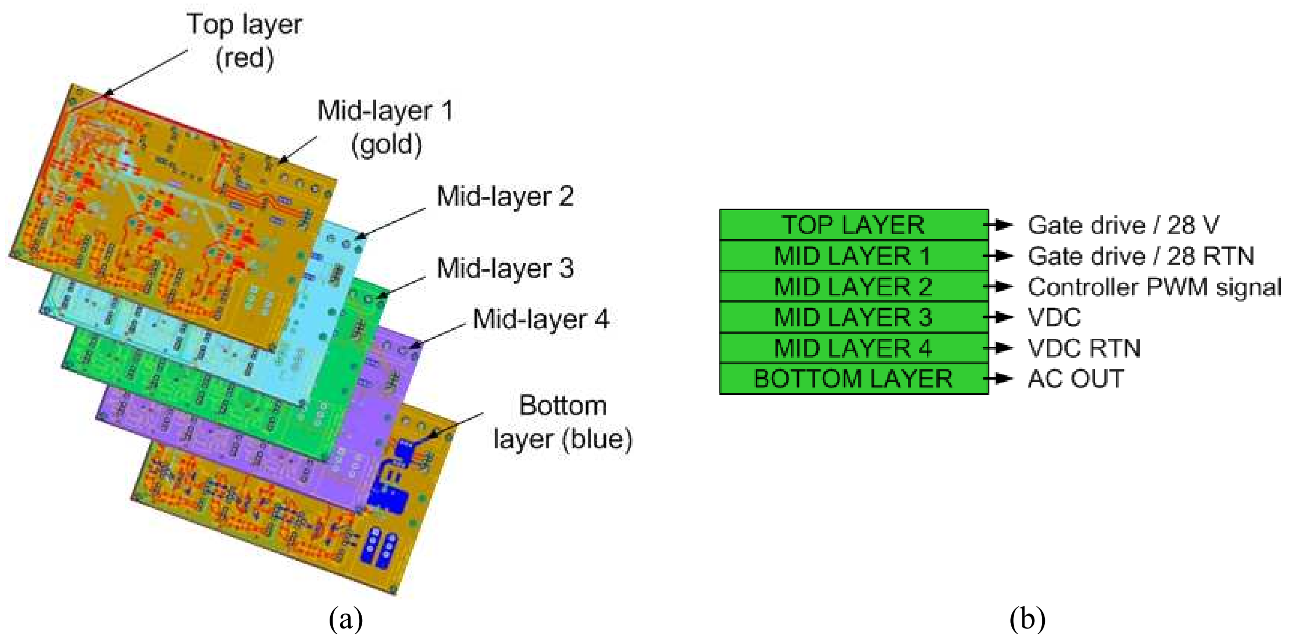


Figure 2-15: PCB stack-up. (a) Exploded view of the PCB layers and (b) function by layer

Top Layer

The top layer is reserved for the gate drive signals and control power (positive 28 V dc rail). Most of the gate driver circuitry, connectors, and power supplies sit on this layer too. Gate drive traces are kept in this layer separated from the power planes to avoid signal corruption. In Figure 2-16 the top layer traces are shown in red.

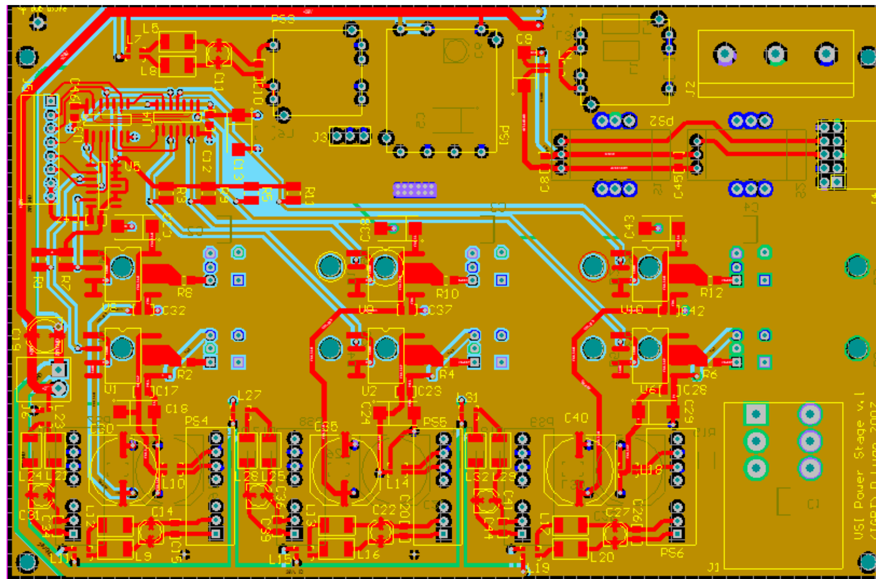


Figure 2-16: Traces and planes of the PCB top layer (red) and mid-layer 1 (gold)

Mid-layer 1

Mid-layer 1 can be found immediately under the top layer. The function of this layer is similar to its predecessor. Gate drive signals make use of mid-layer1, as well as the 28 V return of the control power. The gold color traces and planes in Figure 2-16 show the extent of mid-layer 1. The areas that are not in use by the traces in this layer are filled up with *dead* copper (copper not connected to any power trace or plane). This practice was adopted in all other mid-layers to provide EMI shielding to the more sensitive

components and signals of the top layer. The dead copper from all the mid-layers is connected together and is accessible on the top-layer, where a connection to earth ground has been provided to channel undesired noise that may interfere with the gate drive signals.

Mid-layer 2

In mid-layer 2 (third layer from the top) a signal ground plane has been provided for the optocouplers that process the PWM signals from the controller. The plane helps reduce any ground loops that may deteriorate the gate drive signal. The cut-out portion in light blue shown in Figure 2-17 is the signal ground plane, which has been conveniently located under the gate drive optocouplers.

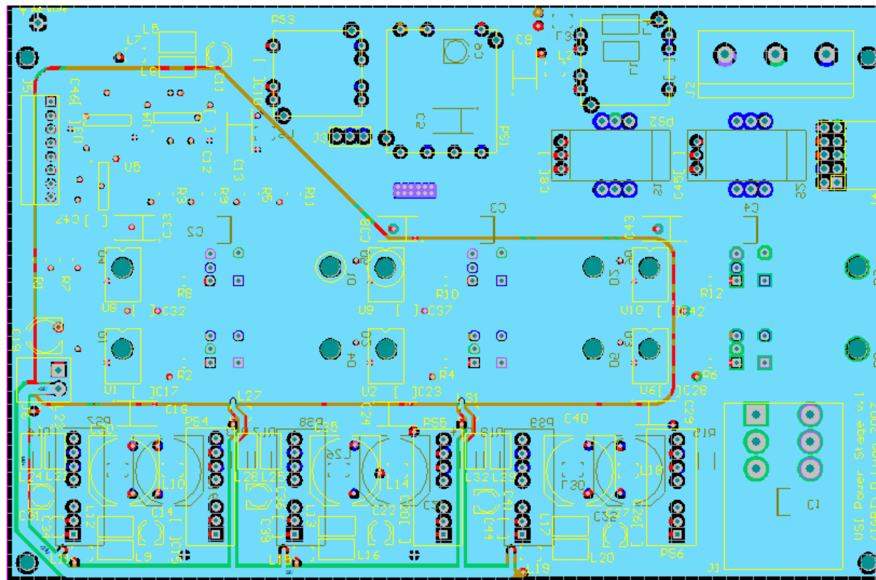


Figure 2-17: Traces and planes of the PCB mid-layer 2 (light blue)

Other uses of this layer include routing of the positive 28 V to power components on the bottom half of the PCB. As in mid-layer 1, unused area was filled up with copper to serve as shield.

Mid-layer 3 and Mid-layer 4

Mid-layers 3 and 4 are reserved exclusively for the positive and negative dc rails, respectively. Figure 2-18 shows the positive dc rail plane (cut-out green plane) extending under the IGBT and diode footprints. The collector pin of all the top IGBTs is connected to the positive dc rail; hence a plane facilitates this connection and minimizes stray inductance in the bus. On the other hand, Figure 2-19 depicts a similar power plane for the negative dc rail (cut-out purple plane). In this case, the emitter pin of the bottom IGBTs are referenced to this point. For the reasons explained before, unused portions in mid-layer 3 and mid-layer 4 were covered up with copper.

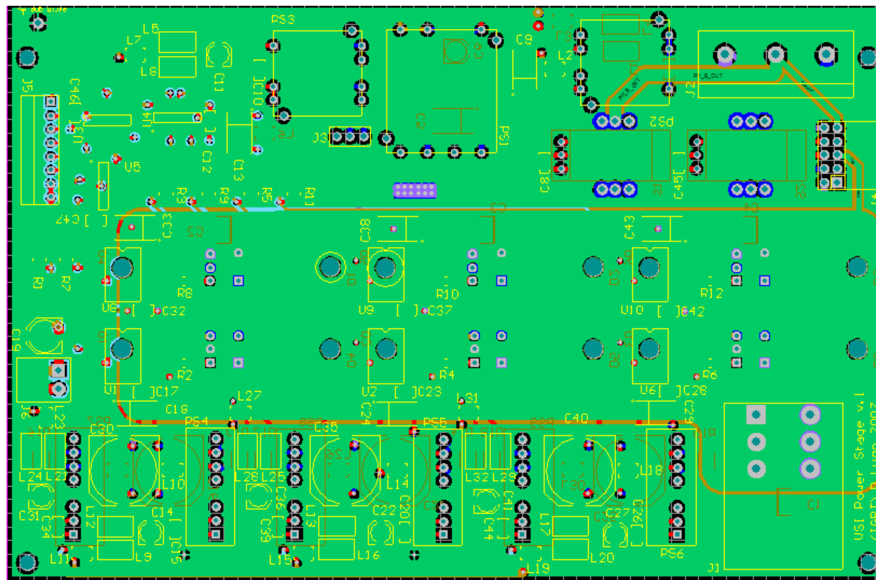


Figure 2-18: Traces and planes of the PCB mid-layer 3 (green). Positive dc rail.

Bottom layer

Lastly, the bottom layer is utilized to carry the three-phase output of the VSI and half of the gates drive power supplies. It is on this side of the board that the power semiconductor devices connect to the PCB. They were arranged such that the IGBTs and diodes are *sandwiched* between the PCB and the heat sink (as shown in Figure 2-20) to

reduce the trace length between the gate driver and the IGBT. The routing of this layer is shown in Figure 2-21.

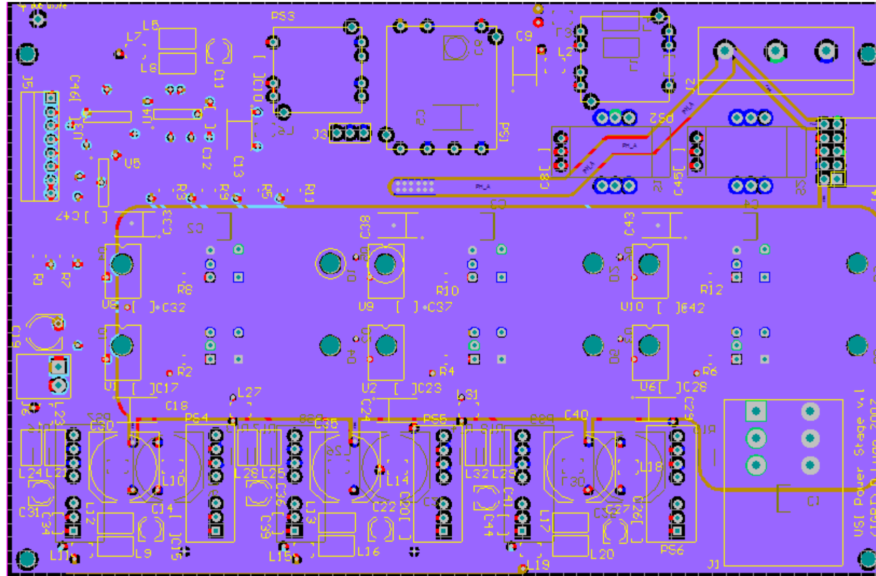


Figure 2-19: Traces and planes of the PCB mid-layer 4 (purple). Negative dc rail.

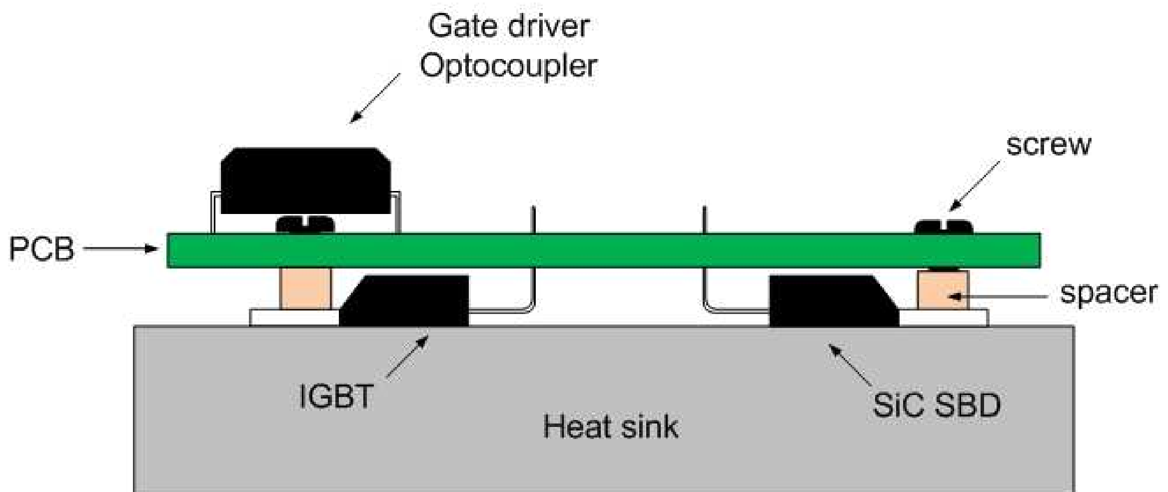


Figure 2-20: Side view of the PCB showing placement of the semiconductor devices between the heat sink and the PCB

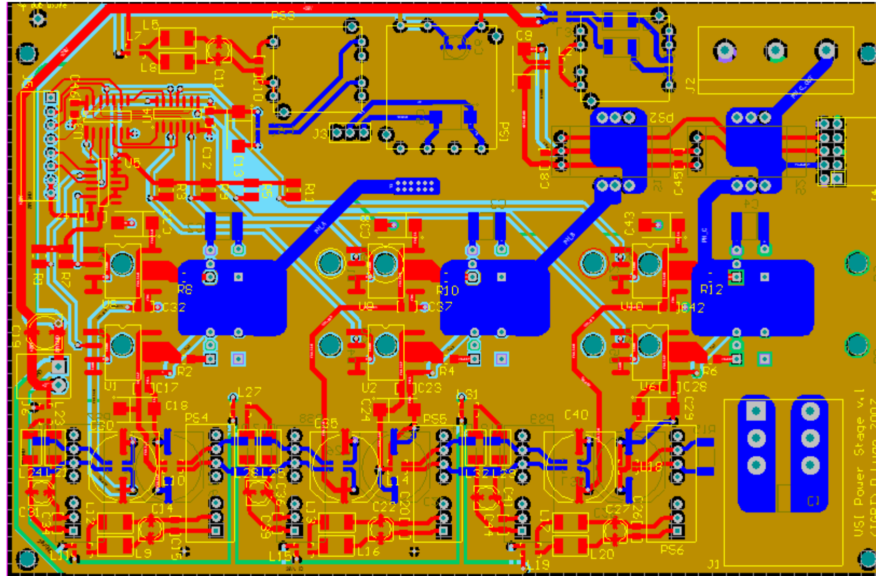


Figure 2-21: Traces and planes of the PCB bottom layer (blue)

The top and bottom sides of the finished unpopulated PCB are shown in Figure 2-22 and Figure 2-23, respectively.

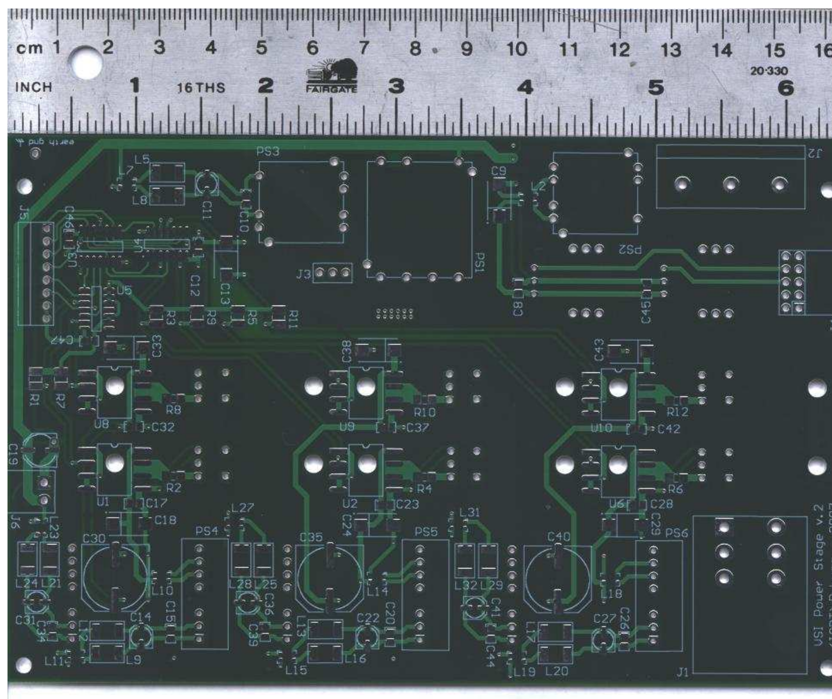


Figure 2-22: Unpopulated PCB- Top side

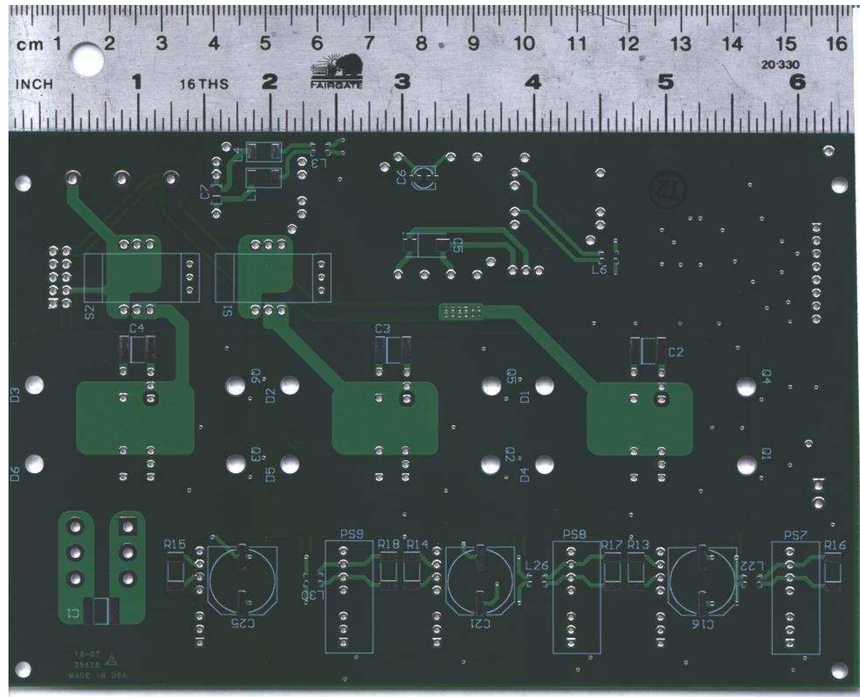


Figure 2-23: Unpopulated PCB- Bottom side

The PCB is 6.5 in (16.5 cm) long by 4.25 in (10.8 cm) wide for a total real estate of 27.62 in^2 (178.2 cm^2). The board is divided into eight main segments:

- DC link voltage input
- Control dc voltage input
- Gate PWM signal input
- Three-phase AC output
- Gate drive power supplies
- Gate driver / Optocouplers
- Current sensors
- Power devices (IGBTs and diodes)

These segments are shown on a populated PCB in Figure 2-24 and Figure 2-25 for the top and bottom sides, respectively.

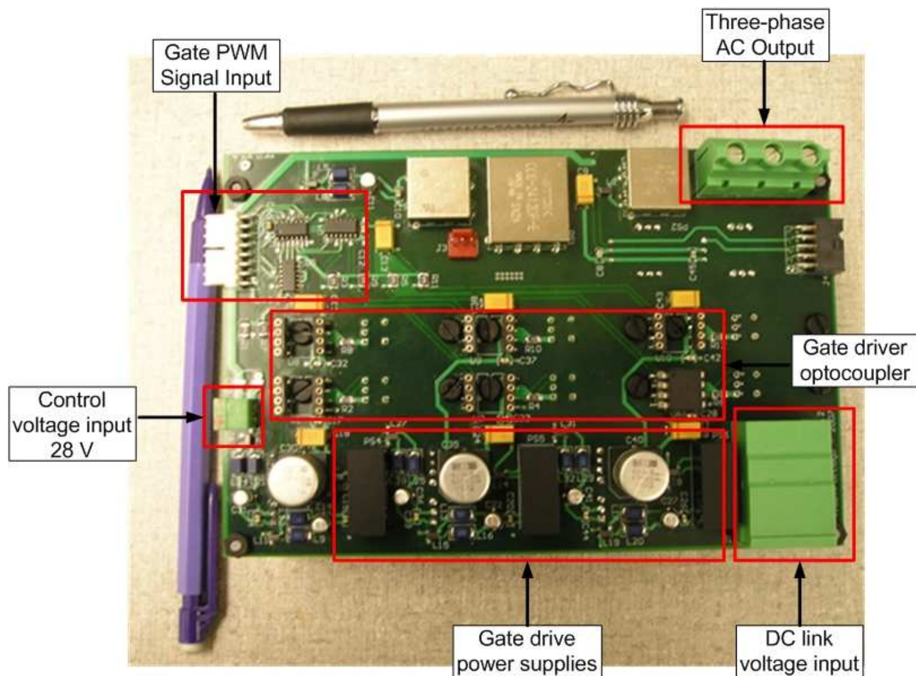


Figure 2-24: Populated PCP, top view

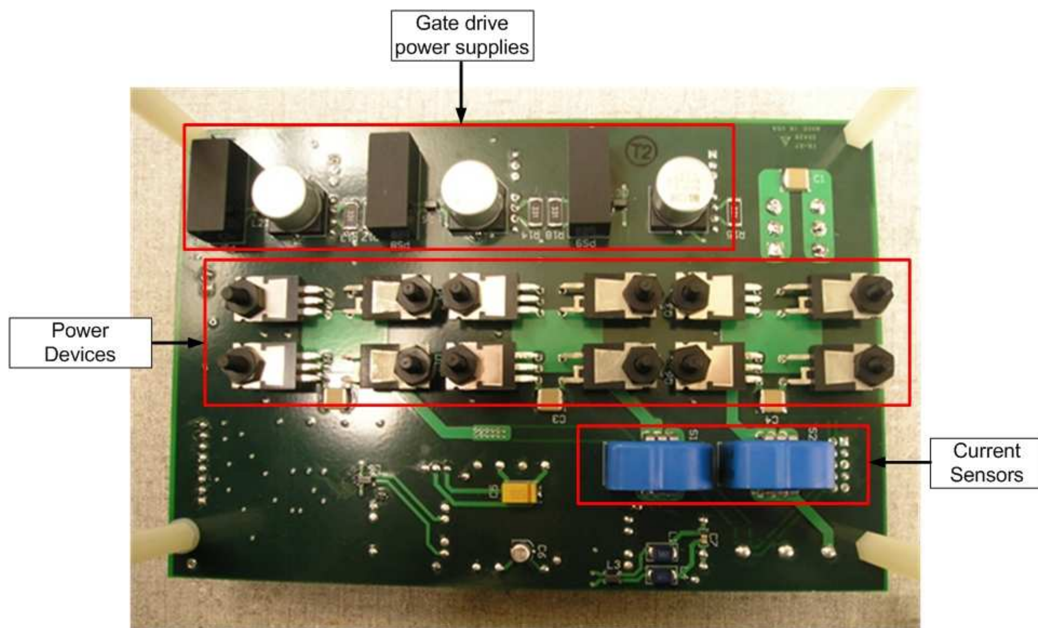


Figure 2-25: Populated PCB, bottom view

The next subsections explain the selection of hardware components and their location on the PCB, as well as a description of the power flow on the board. Selection of components was based on performance and the motivation for a small and lightweight inverter.

2.4.1. DC Link Input, Control Voltage Input, and Three-Phase AC Output

Power from the dc supply that feeds the 480 V bus enters the PCB at the lower right-hand corner of the board on the top side (refer to Figure 2-24). The control voltage that provides power to the peripheral components – gate drive power supplies, current sensors, fan, and logic devices – is fed from a 28 V dc input (resembling the 28 V dc bus used in aircrafts) at the left-hand side of the board (top side). Finally, the ac output is located at the top right-hand corner (opposite of the dc link input) providing easy access for inverter-load interfacing.

2.4.2. Gate PWM Signal Input

Just above the 28 V input, the six gate drive signals from the controller enter the PCB. The signals are fed to the anti-shoot-through logic circuit described earlier in section 2.3.3 before reaching the IGBT gate driver. The length of the cable carrying the PWM input signals was crucial for the correct operation of the inverter. This issue was corroborated during the early stages of the inverter testing and became one of the *lessons-learned* from this work (see Appendix A.1).

2.4.3. Gate Driver and Gate Drive Power Supplies

Isolation is required between the controller and the power stage circuit to protect the more sensitive control circuitry from power stage noise. Optical isolation was provided using chip HCNW-3120 from Avago Technologies. This is a dual purpose chip that serves as an optocoupler and driver, thus saving board real-estate. The chip can output a peak current of 2.5 A (sufficient to drive the IGBTs) and provides 15 kV/µs of common-mode rejection. The gate drive chip was placed as closed as possible to the IGBTs as shown in Figure 2-20 to minimize the gate drive loop area and thus reduce EMI hazards.

Six isolated power supplies power each gate drive chip individually to avoid cross-coupling interference back into the 28 V dc bus due to circulating currents flowing through the common source connection between the switching devices as indicated in [23]. This, of course, comes at the expense of PCB real estate; thus stressing the need for compact dc/dc gate drive power supplies. The small footprint dc/dc converter TMR-2423 from Traco in Figure 2-26 is a space saver as it only occupies 0.3 in^2 per gate drive.

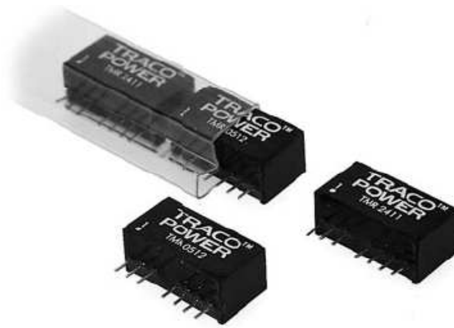


Figure 2-26: Traco dc/dc converter TMR 2423 [datasheet]

2.4.4. Current Sensors

The inverter PCB was equipped with two current sensors that measure two of the output line currents. The PCB mountable current sensor LTS 15-NP is a hall-effect based sensor in a lightweight small profile package (see Figure 2-27). These properties made it a desired candidate for the inverter.

Figure 2-27: Hall-effect current sensor LTS 15-NP

2.4.5. Power Devices

As discussed in section 2.3.1.1 and 2.3.1.2 the switching devices are 600 V, 12 A fast switching IGBT (IR IRG4BC30W). The freewheeling diodes are 1200 V SiC schottky barrier diodes from Infineon. Both power devices were arranged along the center of the board and connect to the PCB from the bottom side of the board as depicted in Figure 2-28c. Two precautions were taken to minimize the impact of dv/dt and di/dt transitions during each switch commutation. First, the inductance between commutating devices was minimized by placing them as close as possible while observing minimum clearance between traces. Commutating devices in a phase-leg are the top switch / bottom diode pair and the bottom switch / top diode pair as shown in Figure 2-28a. The switching transition (commutation) between switch-diode pairs occurs when the switch is turned off and the anti-parallel diode of the other switch picks up the load current. This in turn produces overvoltage stress on the switch being turned off due to the parasitic inductance of the commutation path; hence the importance of minimizing the distance between commutating devices. In a design with discrete semiconductors this is more critical, because the length of the leads on each device adds to the total parasitic inductance of the path. The physical arrangement of the commutating IGBTs and diodes adopted in the design is depicted in Figure 2-28b. This layout brings the emitter of the top IGBT and the cathode of the bottom diode close to each other, as well as the collector of the bottom IGBT and the anode of the top diode; hence diminishing the impact of parasitic inductance during switching transitions.

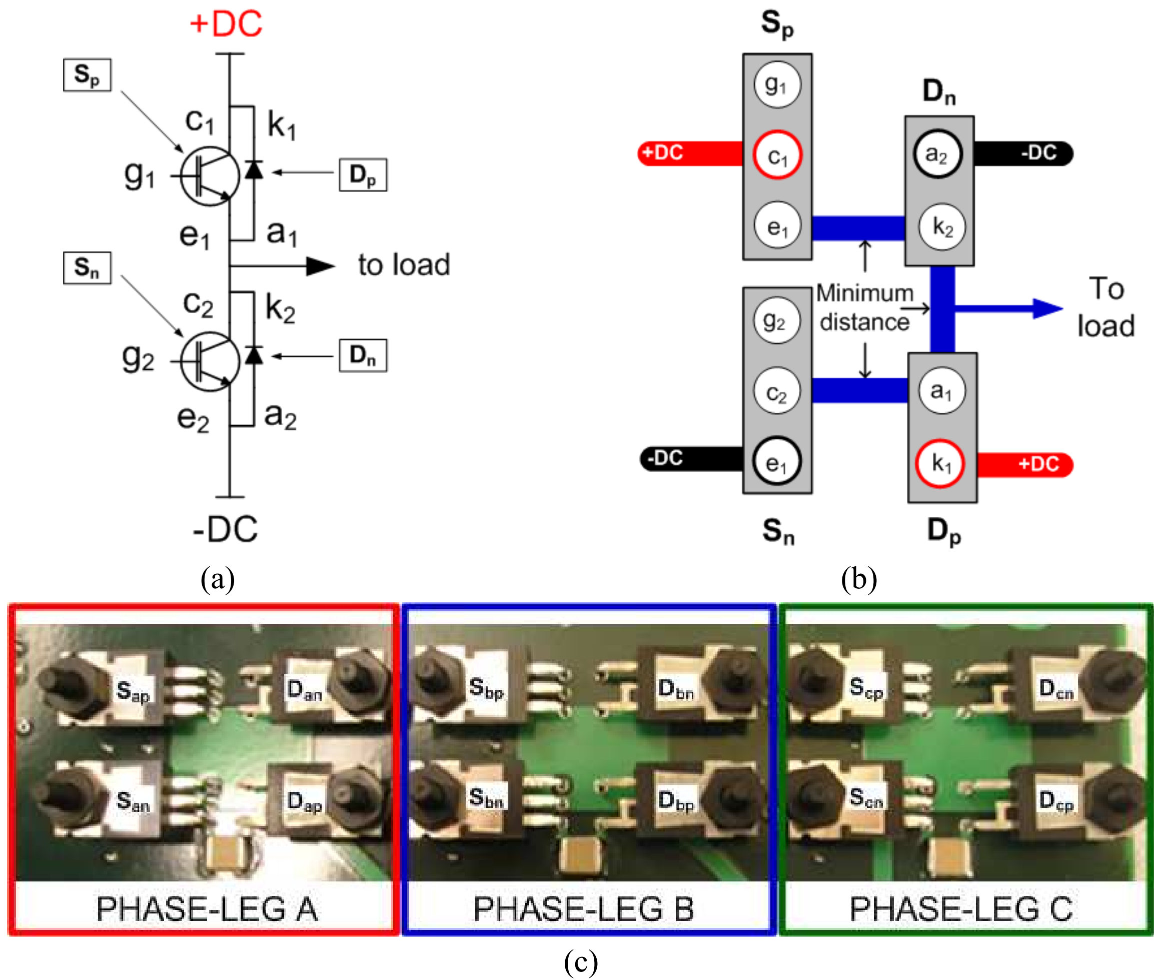


Figure 2-28: Layout for minimum distance between commutating devices. (a) Phase-leg schematic, (b) physical layout, (c) PCB layout

2.5 Controller

To command the inverter a reconfigurable controller designed and developed in CPES, namely Universal Controller (UC) [33] was used. The UC commands the power stage switching based on received information from an external signal conditioning board as depicted in the block diagram of Figure 2-29. Based on the output voltage and current information received the UC generates the gate drive pulses accordingly.

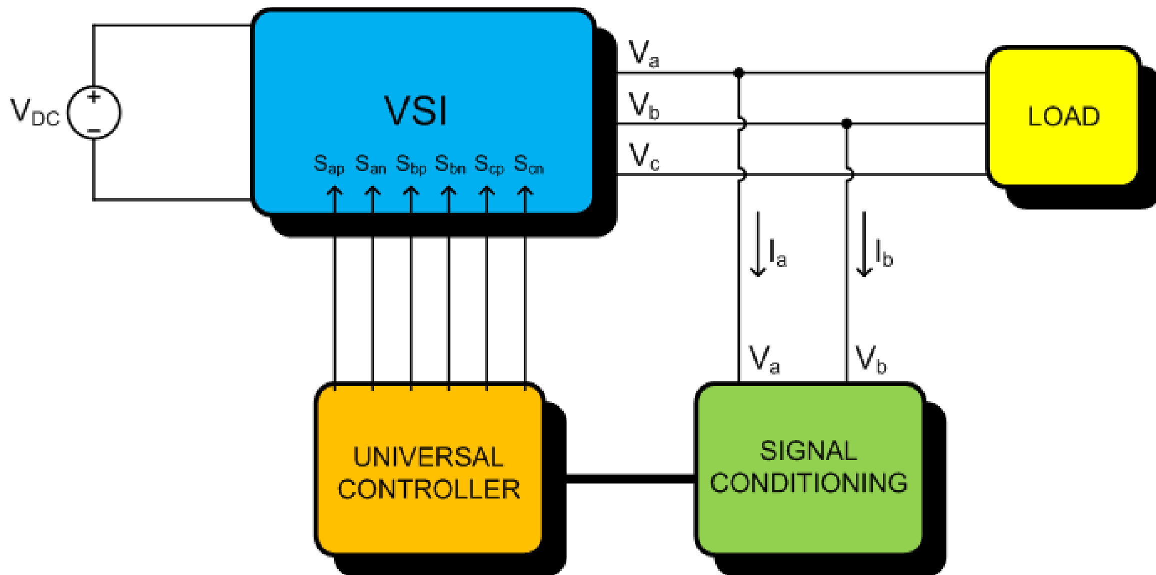


Figure 2-29: Inverter and Universal Controller interface

The controller's DSP executes the control algorithm and performs the calculations required for space vector modulation. An on-board FPGA supports the DSP operation and generates the pulses that drive the inverter switches. More details about this reconfigurable controller can be found in [33].

2.6 Power Loss Calculation

During the power conversion process some energy is inevitably lost from the inverter in the form of heat. The total energy dissipated is a combination of conduction and switching losses – also known as commutation losses – in the IGBTs and freewheeling diodes. Conduction losses are the result of current flowing through the device in the presence of forward or *on* voltage across the device. Switching losses in the other hand are associated to the commutation action of the device as it changes from *on*-state to *off*-state and vice versa. The IGBT and diode conduction losses for SVM inverters based on [34] are expressed in (2.5) and (2.6), respectively.

$$P_{cond,igbt} = \frac{V_{T0} \cdot I_m}{2\pi}\left(1 + \frac{\pi}{4} M \cos\varphi\right) + \frac{K_T \cdot I_m^2}{2\pi}\left(\frac{\pi}{4} + \frac{2M}{3}\cos\varphi - \frac{2M}{15 \cdot 4}\cos 3\varphi\right) \tag{2.5}$$

$$P_{cond,diode} = \frac{V_{D0} \cdot I_m}{2\pi}\left(1 - \frac{\pi}{4} M \cos\varphi\right) + \frac{K_D \cdot I_m^2}{2\pi}\left(\frac{\pi}{4} - \frac{2M}{3}\cos\varphi + \frac{2M}{15 \cdot 4}\cos 3\varphi\right) \tag{2.6}$$

Similarly, expressions for IGBT and diode switching losses are defined in (2.7) and (2.8), respectively.

$$P_{sw,igbt} = \frac{K_{ST} \cdot I_m \cdot f_{sw}}{\pi}\left(1 - \frac{1}{2}\cos\varphi\right) \cdot \frac{V_{dc}}{600} \tag{2.7}$$

$$P_{sw,diode} = \frac{K_{DT} \cdot I_m \cdot f_{sw}}{\pi}\left(1 - \frac{1}{2}\cos\varphi\right) \cdot \frac{V_{dc}}{600} \tag{2.8}$$

Where,

I_m - Peak phase current in [A]

V_{T0} - Linear approximation of IGBT *on*-voltage at zero current [V]

V_{D0} - Linear approximation of diode forward voltage at zero current [V]

M - Modulation index [V/V]

K_T - IGBT equivalent resistance [V/A]

K_D - Diode equivalent resistance [V/A]

φ - Inverter phase angle between the fundamentals of the output phase voltage and phase current [degrees]

K_{ST} - IGBT switching energy per amp [mJ/A]

K_{DT} - Diode switching energy per amp [mJ/A]

f_{sw} - Inverter switching frequency [Hz]

V_{dc} - Dc link voltage [V]

IGBT parameters V_{T0}, K_T, and K_{ST} were extracted from the IGBT datasheet. The estimated values are: V_{T0}= 1.2 V, K_T= 0.11 and K_{ST} =0.0382 mJ/A. For the SiC SBD, parameters V_{D0}, K_D, and K_{DT} were estimated at 0.8 V, 0.125 V/A, and 0, respectively.

The total power loss calculation of the inverter was obtained from (2.5) – (2.8): $P_{loss,total}$= 42.04 W. Figure 2-30 shows the individual contribution of the IGBTs and diodes to the total power loss and Figure 2-31 shows the power loss breakdown in the inverter. Clearly the IGBT losses dominate the overall power dissipation. In fact, IGBT conduction and switching losses account for 53% and 43% of the total inverter losses, respectively. On the other hand the contribution of the SiC SBD is 4% only. A single IGBT dissipates 6.73 W, whereas a single SiC SDB dissipates a mere 0.278 W. Thermal management is treated in the next section in detail.

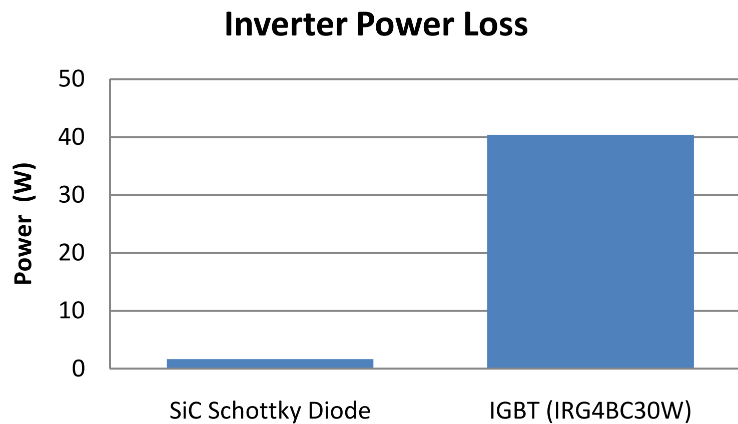
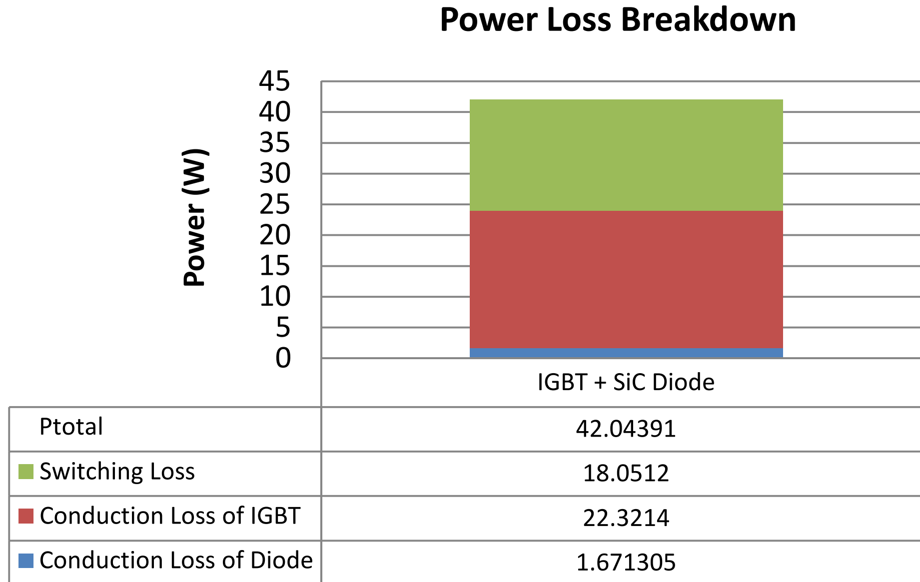


Figure 2-30: Power loss of the six SiC SBDs and the six IGBTs



	IGBT + SiC Diode
Ptotal	42.04391
Switching Loss	18.0512
Conduction Loss of IGBT	22.3214
Conduction Loss of Diode	1.671305

Figure 2-31: Breakdown of power losses in the inverter

2.7 Thermal Design

The thermal design was based on the total power loss of 42.04 W calculated in section 2.6. Accounting for operating temperatures required in a number of airborne applications the ambient and maximum junction temperatures of the devices were set to 70° C and 150 °C, respectively. The static thermal network of the inverter is described in Figure 2-32 for one IGBT-diode pair.

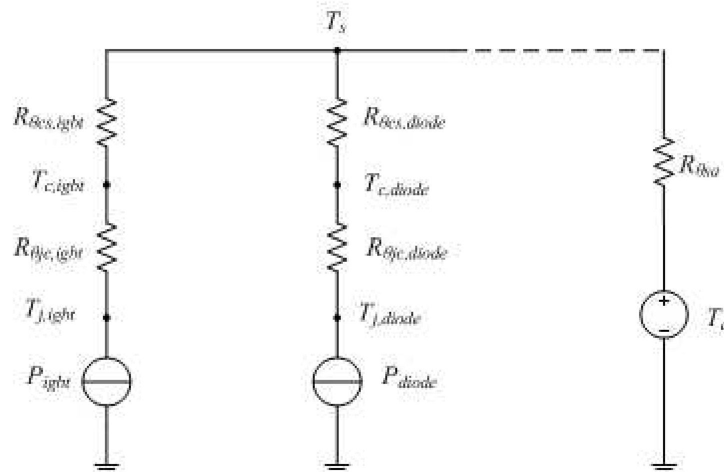


Figure 2-32: Static thermal network of a single IGBT-diode pair

Where:

- P_{igbt} : power loss (conduction and switching) of a single IGBT
- P_{diode} : power loss of a single diode
- T_j : junction temperature
- $R_{\theta jc}$: junction-to-case thermal resistance
- T_c : device case temperature
- $R_{\theta cs}$: case-to-heat sink thermal resistance
- $R_{\theta sa}$: heat sink-to-ambient thermal resistance
- T_a : ambient temperature

In order to design an appropriate heat sink design for the inverter the value of $R_{\theta sa}$ was obtained from the static thermal network. It was shown in section 2.6 that the losses of the IGBT are greater than the diode; consequently, the junction temperature of the IGBT is expected to be the highest. Applying KVL around the loop that contains the IGBT power loss in Figure 2-32 yields,

$$T_{j,igbt} = T_a + P_{igbt}(R_{\theta jc,igbt} + R_{\theta cs,igbt}) + 6(P_{igbt} + P_{diode})R_{\theta sa} \tag{2.9}$$

The term $6(P_{igbt} + P_{diode})$ represents the total power loss of the inverter, 42.04 W. Solving for $R_{\theta sa}$ in (2.9) gives,

$$R_{\theta sa} \leq \frac{T_{j,igbt} - T_a - P_{igbt}(R_{\theta jc,igbt} + R_{\theta cs,igbt})}{6(P_{igbt} + P_{diode})} \tag{2.10}$$

$R_{\theta jc,igbt}$ is specified in the IGBT datasheet as 1.2 °C/W. A 0.02” thick gap pad (Berquist 1500 material) was placed between the device and heat sink to provide electrical isolation. The case-to-heat sink thermal resistance $R_{\theta cs}$ of the gap pad was estimated at

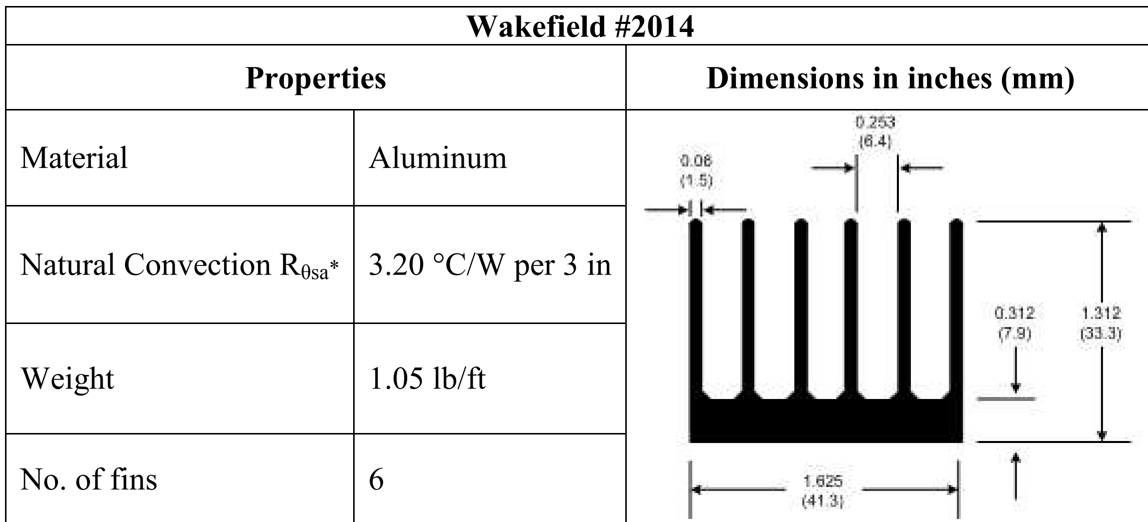
1°C/W. After substituting the corresponding values in (2.10), the calculated heat sink-to-ambient thermal resistance is,

$$R_{\theta sa} \leq 1.55 \text{ °C/W}$$

The heat sink $R_{\theta sa}$ was finally set to 1.0°C/W to allow margin and ensure that the devices do not exceed their maximum junction temperature of 150°C.

In addition to $R_{\theta sa}$, heat sink compactness and weight are characteristics sought in the thermal design to satisfy the demands of a high power density design. An aluminum extrusion heat sink from Wakefield #2014 was chosen to cool the semiconductor devices. The properties of this heat sink are summarized in Table 2-3.

TABLE 2-3
HEAT SINK PROPERTIES

Wakefield #2014		
Properties		**Dimensions in inches (mm)**
Material	Aluminum	
Natural Convection $R_{\theta sa}$*	3.20 °C/W per 3 in	
Weight	1.05 lb/ft	
No. of fins	6	

*$R_{\theta sa}$ is the heat sink thermal resistance specified at a temperature rise of 75°C

As seen in Table 3-2, the value of $R_{\theta sa}$ is provided for a 3 in long heat sink piece and for a temperature rise of 75°C. A 5 in long heat sink piece was used to accommodate the twelve discrete devices of the inverter power stage. Hence, the thermal resistance indicated in Table 3-2 must be corrected using an appropriate length correction factor according to [35]. For 5 in, the correction factor is 0.78; thus $R_{\theta sa}$ is $3.2\text{°C/W} \times 0.78 =$

$2.5\ ℃/W$. This value, however, is for a temperature rise of 75°C. The actual temperature rise for the calculated $R_{\theta sa}$ is:

$$\Delta T_{sa} = R_{\theta sa} \cdot P_{total} \tag{2.11}$$

$$\Delta T_{sa} = 1.55\ ℃/\mathrm{W} \cdot 42.04\ \mathrm{W} = 65.16\ ℃$$

Since the thermal resistance of 2.5°C/W is for a temperature rise of 75°C, the resistance of the heat sink for a temperature rise of 65.16°C will be increased by a temperature correction factor of 1.037 according to the Temperature Rise Correction Factor Table in [35]. Therefore, the new natural convection thermal resistance at 65.16°C is $2.5\ ℃/W \times 1.037 = 2.59℃/W$. This resistance is obviously larger than the desired thermal resistance of 1.0°C/W; thus additional cooling was provided with a fan. The required airflow to bring $R_{\theta sa}$ down to 1.0°C/W was 600 linear feet per minute (LFM). Fan *San Ace 40L* from Sanyo Denki is a small profile fan that delivers 687 LFM (with 80% derating) and has the same cross-section area of the heat sink window; therefore, it was selected to assist with the cooling of the semiconductor devices. The total weight of the cooling system is 0.559 lb (253.45 g). A picture of both the heat sink and fan is shown in Figure 2-33.

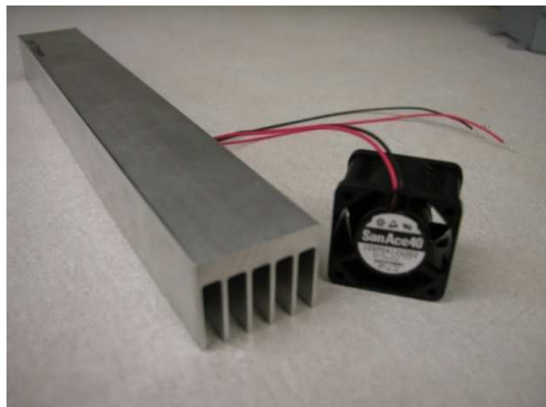


Figure 2-33: Inverter cooling system. Heat sink Wakefield #2014 (left) and fan San Ace 40L (right)

Chapter 3 VOLTAGE SOURCE INVERTER HARDWARE VALIDATION

3.1 Hardware Validation

To validate the electrical and thermal design of the VSI presented in Ch. 2 the inverter was tested under the conditions depicted in Table 3-1.

TABLE 3-1
INVERTER TEST PARAMETERS AND DESIGN SPECIFICATIONS

Parameter	Test	Design Specs
DC Link Voltage, V_{dc}	500 V	500 V
Line-to-Line RMS Voltage, V_m	350 V	350 V
Load Current	4.8 A	5 A
Output AC frequency, f_{ac}	400 Hz	400 Hz
Power factor	0.99 lagging	0.99 lagging
Nominal Output Power	2 kW	2 kW
Switching frequency, f_{sw}	10 – 65 kHz	70 kHz

A series of tests were performed allowing assessment of the VSI performance on the following areas:

- Full load operation at high switching frequency
- Current quality as a function of switching frequency
- Inverter overall efficiency
- Maximum junction temperature of switching devices
- Power density

3.2 Test Setup and Equipment

The test setup is shown in Figure 3-1. The dc link voltage was supplied from a Sorensen 600 V, 16 A dc power supply. One bench dc power supply provided the 28 V

bus and two additional supplies were used for powering the controller and the signal conditioning board.

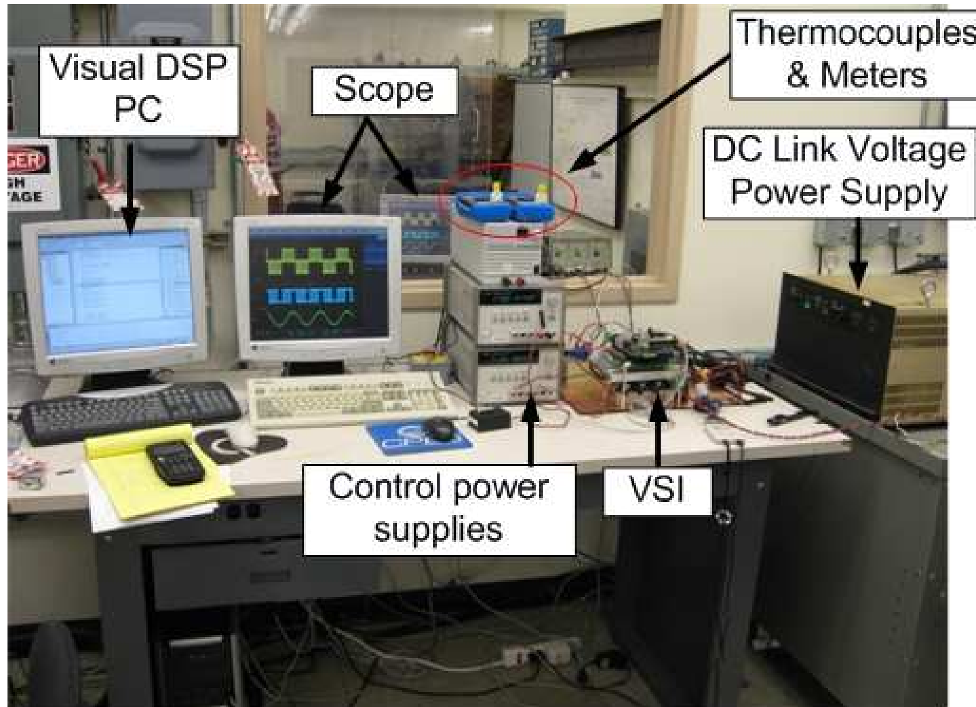
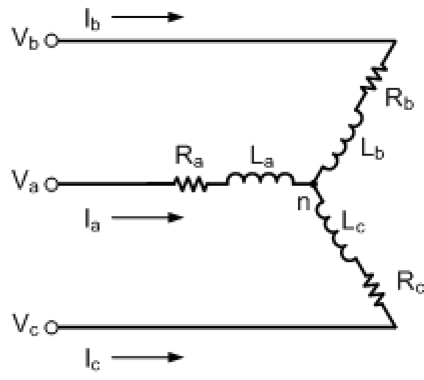
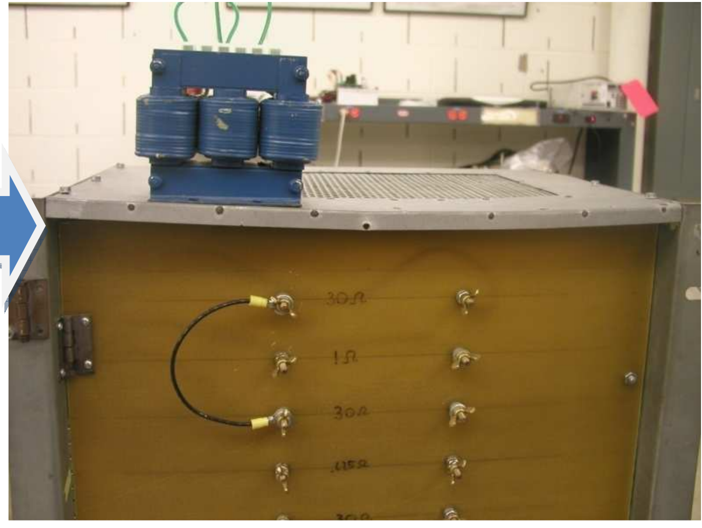


Figure 3-1: VSI test setup

A 30 Ω resistor bank in series with a 1.4 mH three-phase inductor (shown in Figure 3-2) were used for loading the VSI (Y-connected load). Waveforms were monitored and recorded using a Tektronix oscilloscope.

The modulator was implemented digitally using the universal controller (UC) described earlier in section 2.5. An additional external board is dedicated for signal conditioning. It contains voltage and current sensors, A/D converters, and necessary filters. The power stage was designed such that the signal processing board and the controller board could be stack-mounted on the inverter as shown in Figure 3-3.





(a) (b)

Figure 3-2: Three-phase RL load. (a) Schematic and (b) hardware

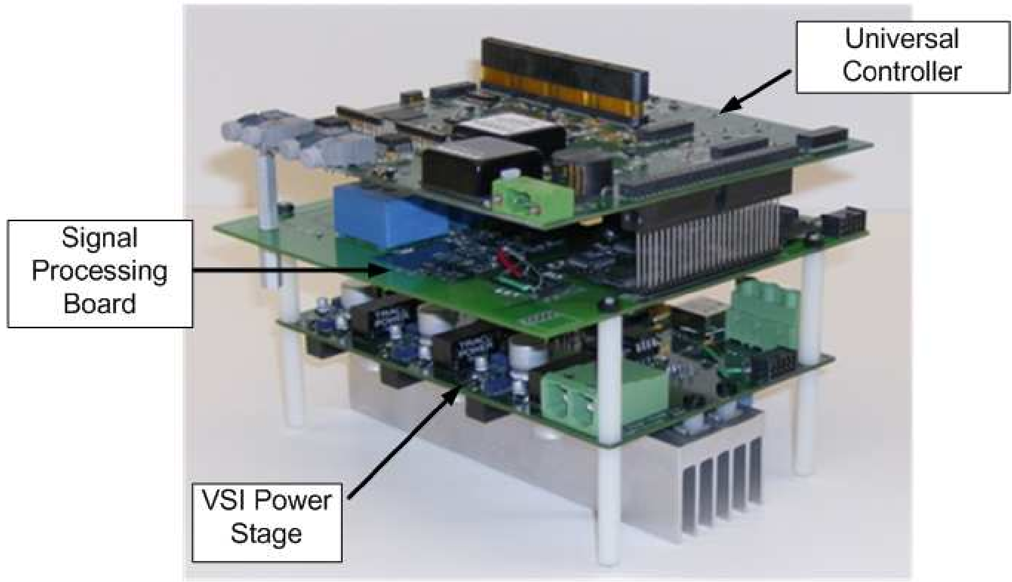


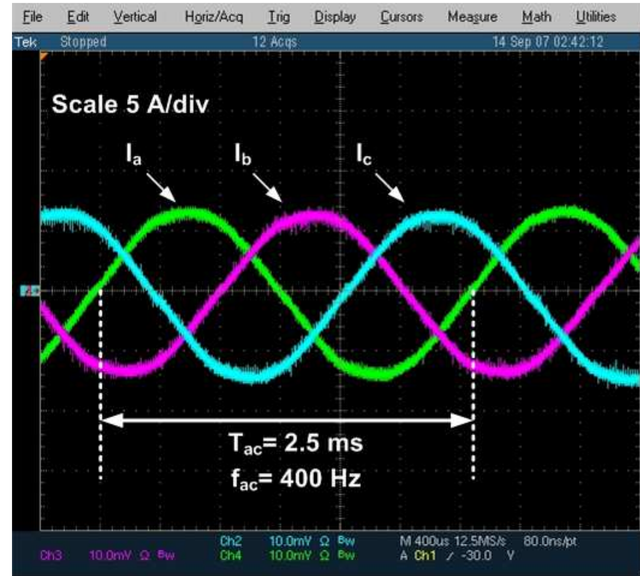
Figure 3-3: Inverter, signal processing board and universal controller

3.3 Test Results

3.3.1. Full Load Operation

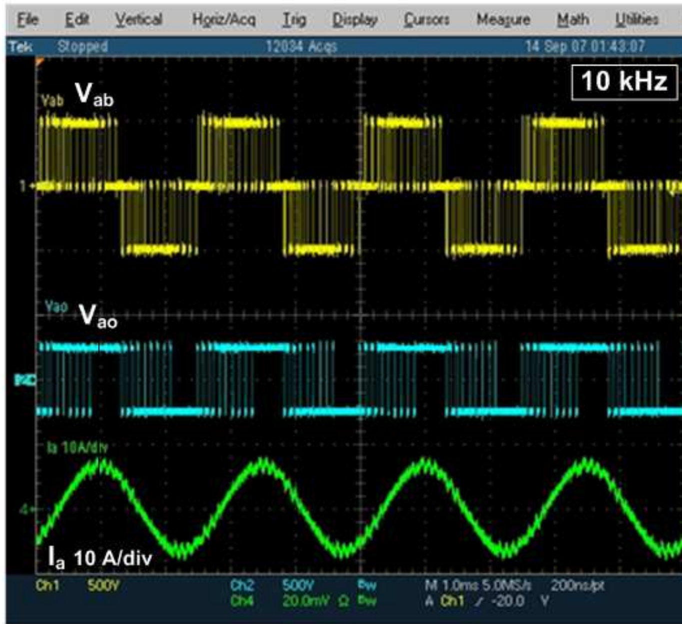
The line-to-line voltages and full load currents of the inverter are shown in Figure 3-4 at f_{sw}= 65 kHz. Figure 3-5a to 3-5d are scope waveforms of the line-to-line voltage V_{ab}, line to midpoint voltage V_{ao}, and load current I_a at 10, 20, 40, and 65 kHz,

respectively, for the test conditions described in Table 3-1. These figures verify the correct operation of the inverter at full power (2 kW) over a range of switching frequencies up to 65 kHz, thus demonstrating the high switching frequency capability of the inverter.

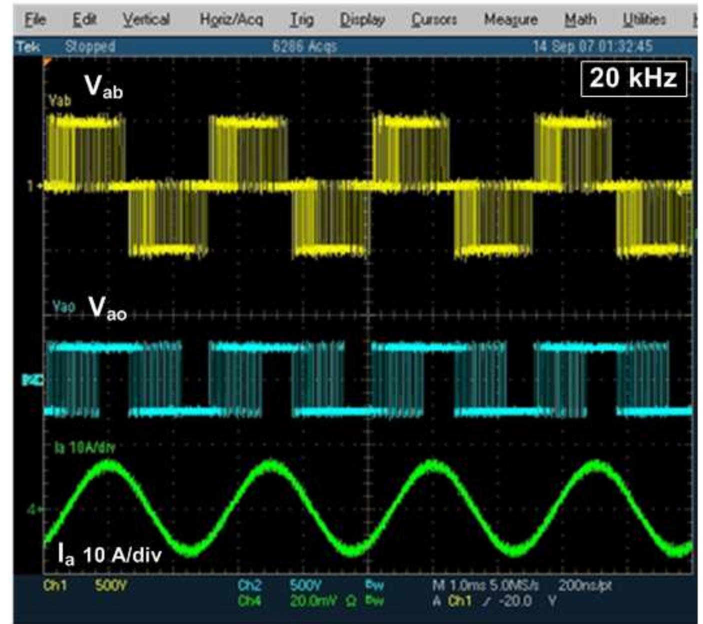


(a) (b)

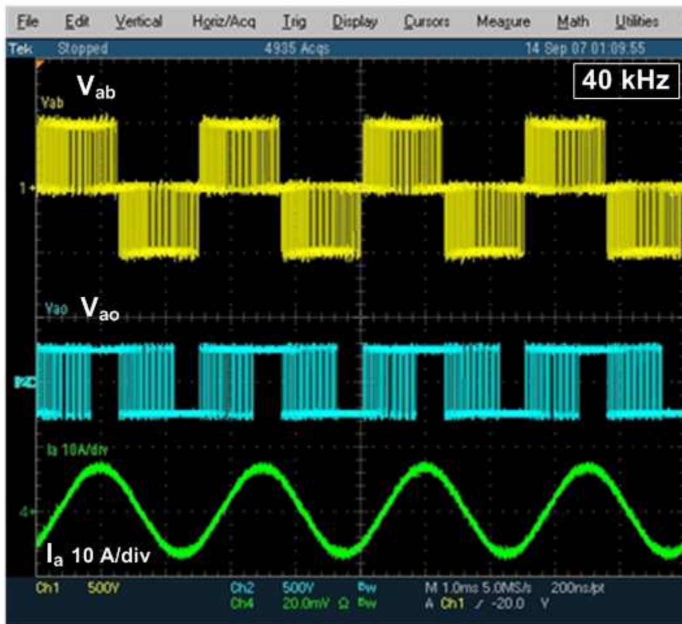
Figure 3-4: Inverter (a) line-to-line voltages and (b) load currents at full load, f_{sw}= 65 kHz. Scale: 800 V/div, 5 A/div, 400 μs/div



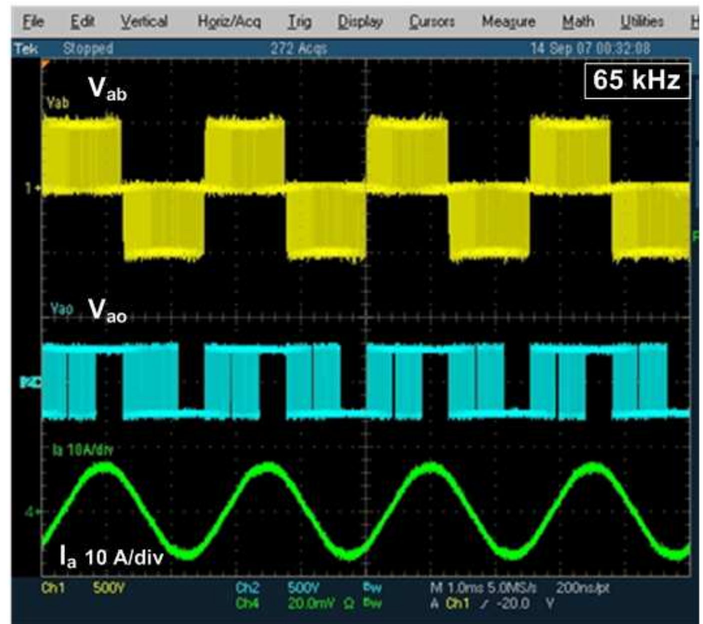
(a)



(b)



(c)



(d)

Figure 3-5: Inverter phase A waveforms at (a) f_{sw}= 10 kHz, (b) f_{sw}= 20 kHz, (c) f_{sw}= 40 kHz, (d) f_{sw}= 65 kHz. Scale: V_{ab} 500 V/div, V_{ao} 500 V/div, I_a 10 A/div. Time 1 ms/div

Note that the maximum switching frequency shown in Figure 3-4 and Figure 3-5 is 65 kHz. Although the design contemplated 70 kHz operation, the maximum switching frequency achieved in test was 65 kHz. It was soon realized that the 70 kHz design spec

exerted an excessive computational burden on the controller that prevented the inverter to operate stable above 65 kHz. The explanation to this limitation resides in the DSP control period being longer than the inverter switching period. At f_{sw}= 70 kHz the corresponding switching period is 14.29 μs. The DSP however took 14.7 μs to complete the SVM calculations and update the FPGA before the beginning of the next switching cycle. In theory the maximum switching frequency with the code and type of DSP used is $f_{sw,limit} = \frac{1}{14.7\times10^{-6}} = 68$ kHz, but it was verified that the operation of the inverter became unstable and intermittent above 65 kHz. The lack of processing speed therefore limited the maximum achievable switching frequency.

3.3.2. Load Current Quality

As switching frequency increases from 10 to 65 kHz the load current ripple becomes smaller. The contrast in current ripple at 10 and 65 kHz is shown in Figure 3-6. As the ripple becomes smaller the quality of the current improves. This is desirable in motor drive applications because it helps reduce the motor copper and iron losses [12, 13]. In order to quantify the benefits of high switching frequency on the inverter current quality, the total harmonic distortion (THD) of the load current was extracted from the measured waveforms and plotted against switching frequency as shown in Figure 3-7.

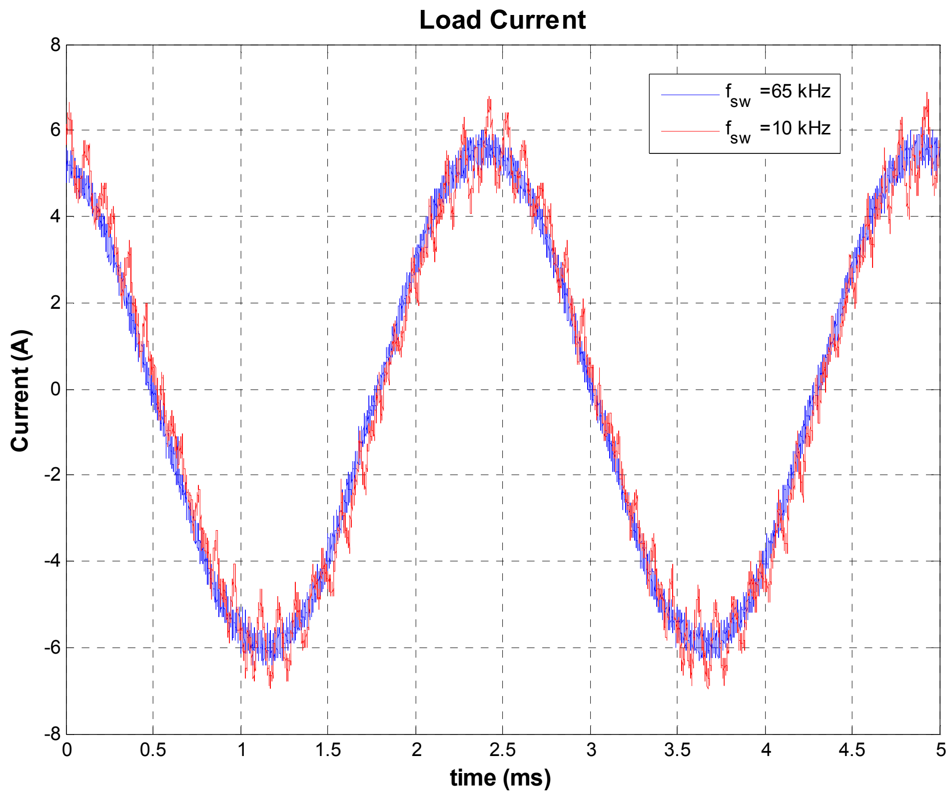


Figure 3-6: Load current at f_{sw}= 10 kHz (red) and 65 kHz (blue)

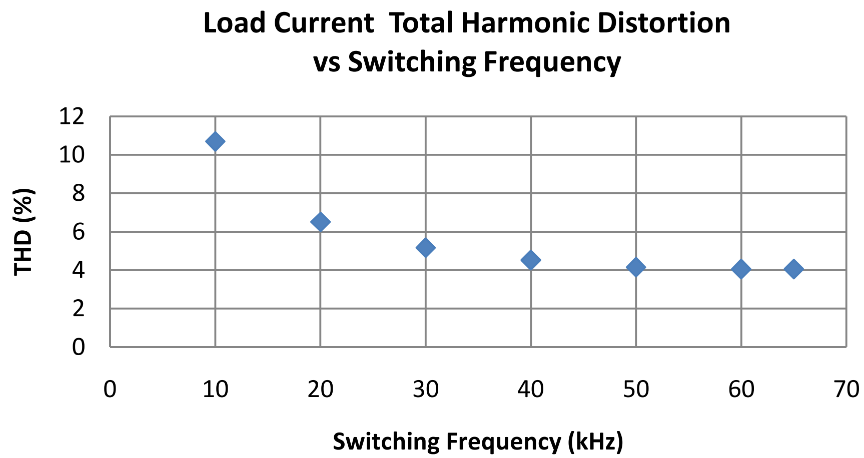


Figure 3-7: Load current THD versus switching frequency

Significant improvement of the current THD is observed from low switching frequencies up to 40 kHz. Beyond this point the benefits of high switching frequency on current quality are only marginal.

3.3.3. System Efficiency

The overall efficiency of the inverter system was calculated from the dc input and ac output waveforms depicted in Figure 3-8. The input power P_{in} was obtained simply from (3.1).

$$P_{in} = V_{dc} \times I_{dc} \tag{3.1}$$

The instantaneous power (voltage and current product) and the moving average of the input power are shown in Figure 3-9. The average of the product in (3.1) results in $P_{in,av}$= 2065 W. On the other hand the three-phase average power measured at the output terminals of the VSI was obtained from (3.2).

$$P_{out} = 3 \times \frac{1}{T_{ac}} \int_{t_0}^{t_0+T_{ac}} v_{ao}(t) \cdot i_a(t)\, dt \tag{3.2}$$

Where, $T_{ac} = \frac{1}{f_{ac}}$ is the period corresponding to the fundamental output frequency.

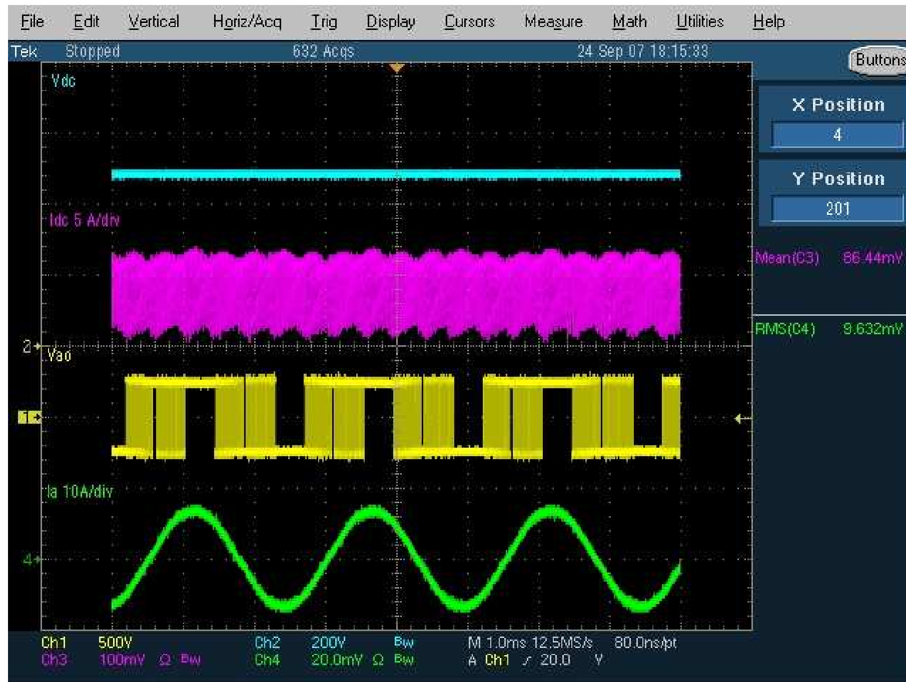


Figure 3-8: Inverter waveforms used for power calculation at f_{sw}= 65 kHz, Vdc= 480 V and I_{rms}= 4.8 A. From top to bottom: V_{dc} 200 V/div, I_{dc} 5 A/div, V_{ao} 500 V/div, and I_a 10 A/div. Time scale 1 ms/div

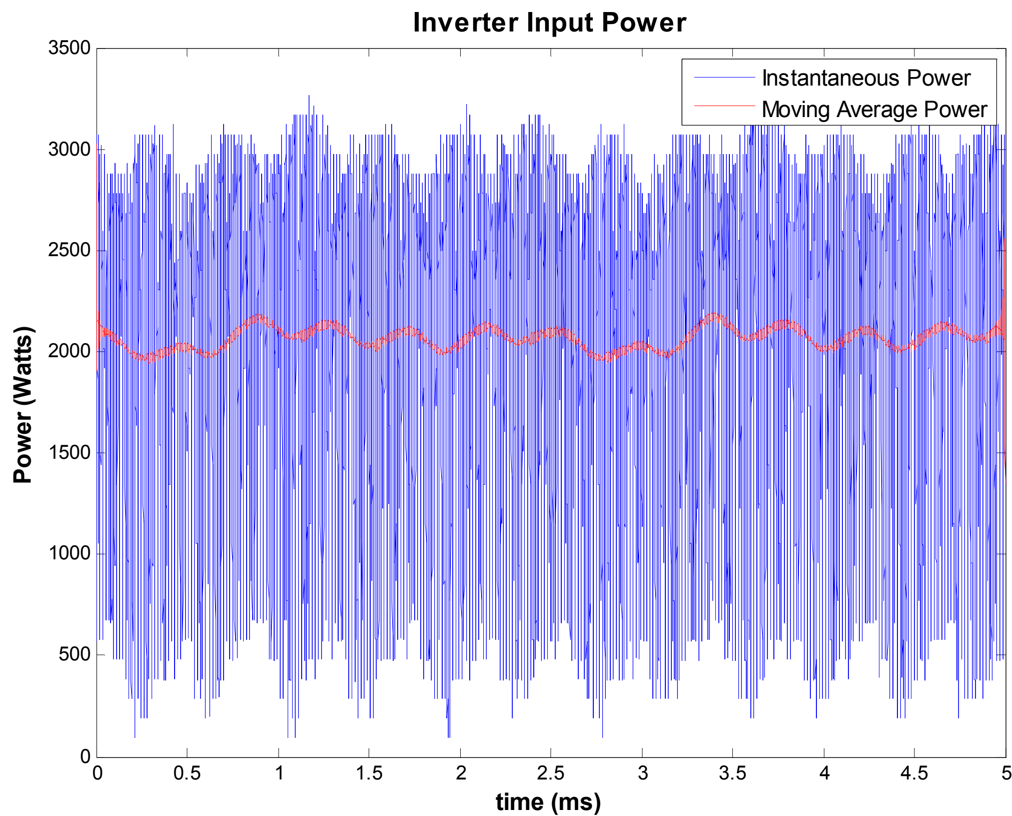


Figure 3-9: Instantaneous and moving average input power

The single phase instantaneous output power is plotted in Figure 3-10. Integrating this waveform over one ac cycle and multiplying by 3 yields the average output power: P_{out}= 1993 W. The overall efficiency of the system as measured from the input and output power waveforms is:

$$\eta = \frac{P_{out}}{P_{in,av}} = \frac{1993}{2067} = 96.4\% \tag{3.3}$$

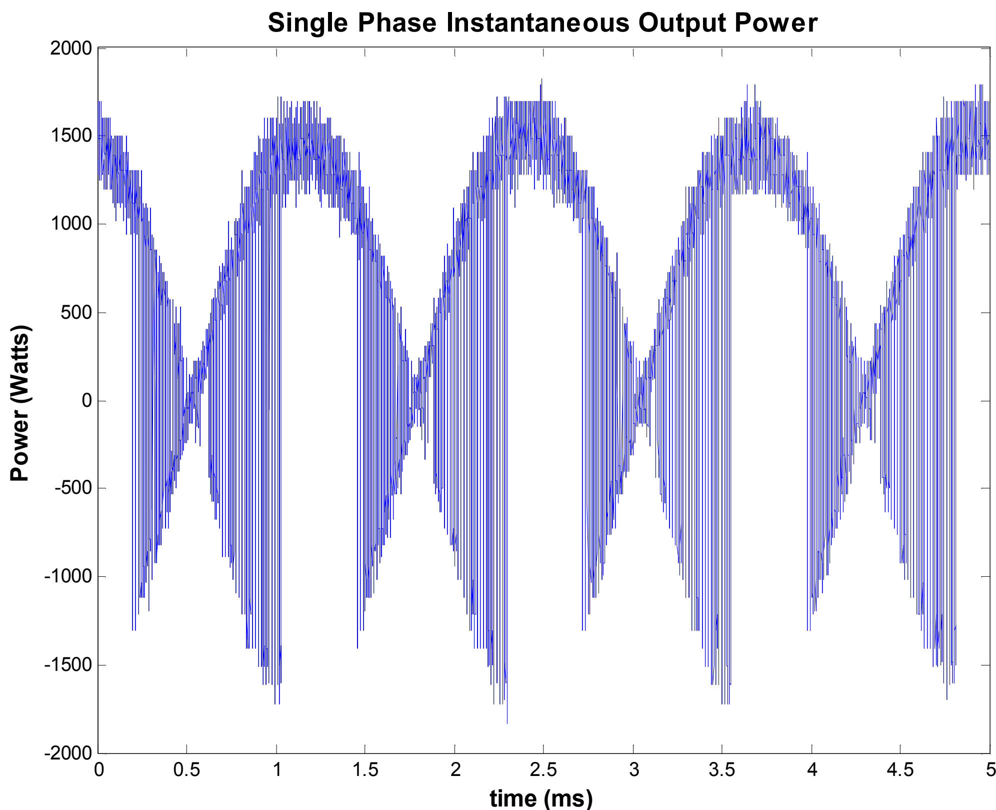


Figure 3-10: Instantaneous output power of a single phase

Therefore the total power loss of the inverter is 74 W. This is 57% higher than calculated in section 2.6. Revisiting the power loss calculation of the IGBT it was found that the approximation of parameters V_{T0} and K_T was too conservative and therefore the conduction loss calculation yielded a lower value. A closer look at the output characteristic plot of IGBT IRG4BC30W reveals that a better approximation of these

parameters is V_{T0}= 2.1 V and K_T= 0.431 V/A. Recalculating the total power loss with the revisited parameters yields 77.29 W which better agrees with the measured value of 74 W. Although the thermal design was based on the original power loss calculation (42.04 W) the validation of the thermal design in section 3.4 confirms that the cooling provided is sufficient to not exceed the maximum junction temperature of the devices.

3.4 Thermal Design Validation

The thermal design was validated by monitoring the IGBT and diode temperatures while operating the inverter at full power and at several switching frequencies. As most of the heat in the devices transfers downward through the case back plate, a K-type thermocouple was placed underneath IGBT S_{ap} and its anti-parallel diode D_{ap}. Since the thermocouples that were used are not insulated, they had to be placed between the gap pad and the heat sink to avoid direct contact with the conducting back plate of the devices. Therefore, the recorded temperature was in fact the heat sink temperature T_s as measured under the device. Figure 3-11 describes the setup used for the thermal design validation and shows the location of the thermocouple under the semiconductor device. The thermocouples were connected to Tektronix DMM916 multimeter from which the temperature measurements were read.

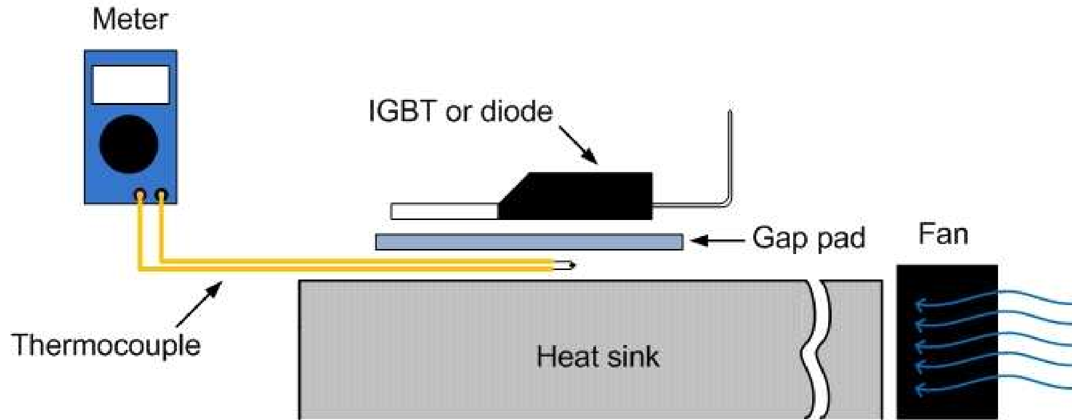


Figure 3-11: Measurement setup for thermal design validation

Temperature was recorded after the inverter had dwelled at full load for 10 minutes to assure stable temperature readings. The conditions of this test are summarized in Table 3-2.

TABLE 3-2
THERMAL DESIGN TEST CONDITIONS

Ambient temperature, T_a	26.4 °C
Fan mode	Active
Output Power	2 kW
Load RMS Current	4.8 A
Switching frequency, f_{sw}	10 – 65 kHz
Line AC frequency, f_{ac}	400 Hz
DC Link Voltage, V_{dc}	500 V

The recorded data, which corresponds to the heat sink temperature T_s, is displayed in Table 3-3 for switching frequencies up to 65 kHz.

TABLE 3-3
MEASURED HEAT SINK TEMPERATURE AT T_A= 26.4°C

Switching Frequency, f_{sw} (kHz)	**$T_{s,igbt}$ (°C)**	**$T_{s,diode}$ (°C)**
10	41.0	39.4
20	42.1	40.5
30	43.5	41.9
40	44.7	42.5
50	46.1	43.6
60	47.4	44.6
65	47.8	45.2

As indicated in (2.7) and (2.8) the switching losses are proportional to switching frequency, therefore, the device temperature increases for higher values of f_{sw}. The results in Table 3-3 suggest that at T_a= 26.4°C, the junction temperature of the IGBT and diode increases an average of 1.28 °C and 1.04°C, respectively, per 10 kHz of switching frequency. Using Figure 2-32 as reference, the junction temperature can be expressed as:

$$T_j = P_{loss} \cdot \left(R_{\theta jc} + R_{\theta cs}\right) + T_s \tag{3.4}$$

Where, P_{loss} is the power loss of a single IGBT (P_{igbt}) or diode (P_{diode}) as defined before. In principle, P_{loss} should be measured from the current and voltage waveforms of the device such that the conduction loss and switching energy information can be extracted from them. Given the compact layout of the inverter, direct measurements of each IGBT and diode resulted unfeasible; hence the theoretical P_{loss} calculated in section 2.6 was used instead (42.04 W). Given that the IGBT dissipates more heat than the diode, the junction temperature of the IGBT represents the worst-case scenario. The heat sink and junction temperature of the IGBT versus switching frequency at T_a= 26.4°C is plotted in Figure 3-12. Test data at T_a= 70°C was not measured directly, but instead was extrapolated from the measurements at T_a= 26.4°C. It can be seen that the heat sink temperature – and thus junction temperature – is highly linear with switching frequency. If we assume, in addition, that T_s increases linearly with ambient temperature, a new heat sink temperature $T_{s,new}$ can be obtained at any desired ambient temperature as follows:

$$T_{s,new} = T_s \cdot \left(\frac{T_{a,new}}{T_a}\right) \tag{3.5}$$

Where, $T_{s,new}$ is the new heat sink temperature corresponding to the new ambient temperature $T_{a,new}$; T_s and T_a are the original measured values.

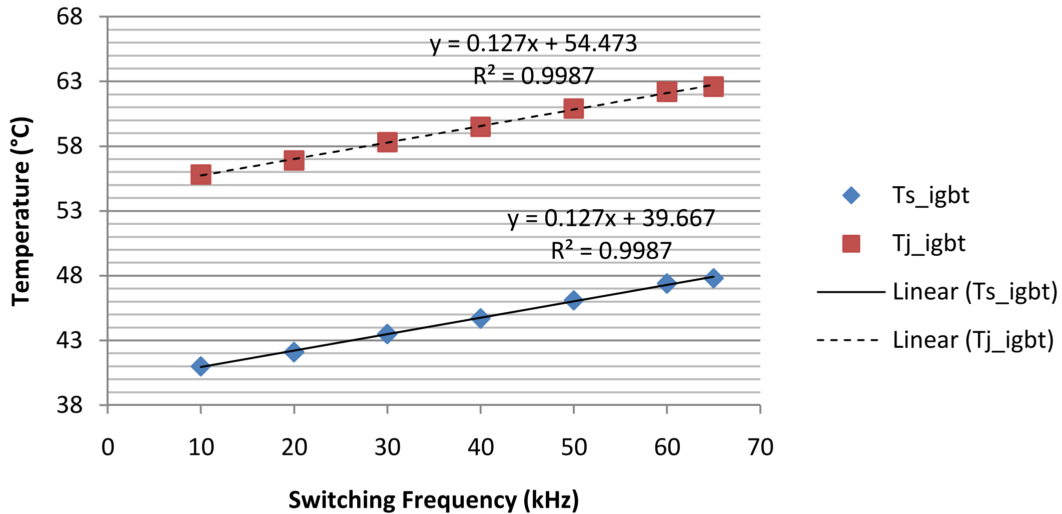


Figure 3-12: Heat sink and IGBT junction temperature at T_a= 26.4°C

Since the thermal design assumed an ambient temperature of 70°C and a maximum junction temperature of 150°C, the heat sink temperature must be proportionally scaled to the desired ambient temperature using (3.5). The new values are depicted in Table 3-4.

TABLE 3-4
PROJECTED HEAT SINK TEMPERATURE FOR T_A= 70°C
BASED ON MEASUREMENTS AT T_A= 26.4°C

Switching Frequency, f_{sw} (kHz)	**$T_{s,igbt}$ (°C)**	**$T_{s,diode}$ (°C)**
10	108.7	104.5
20	111.6	107.4
30	115.3	111.1
40	118.5	112.7
50	122.2	115.6
60	125.7	118.3
65	126.7	119.8

As before, the IGBT junction temperature at T_a= 70°C was obtained from (3.4). The plot in Figure 3-13 shows the projected values of T_j and T_s versus switching frequency

for an ambient temperature of 70°C. Additional points are shown beyond the recorded data to predict the switching frequency at which the IGBT junction temperature exceeds 150°C. This extrapolation is reasonable because the relation between junction temperature and switching frequency is highly linear.

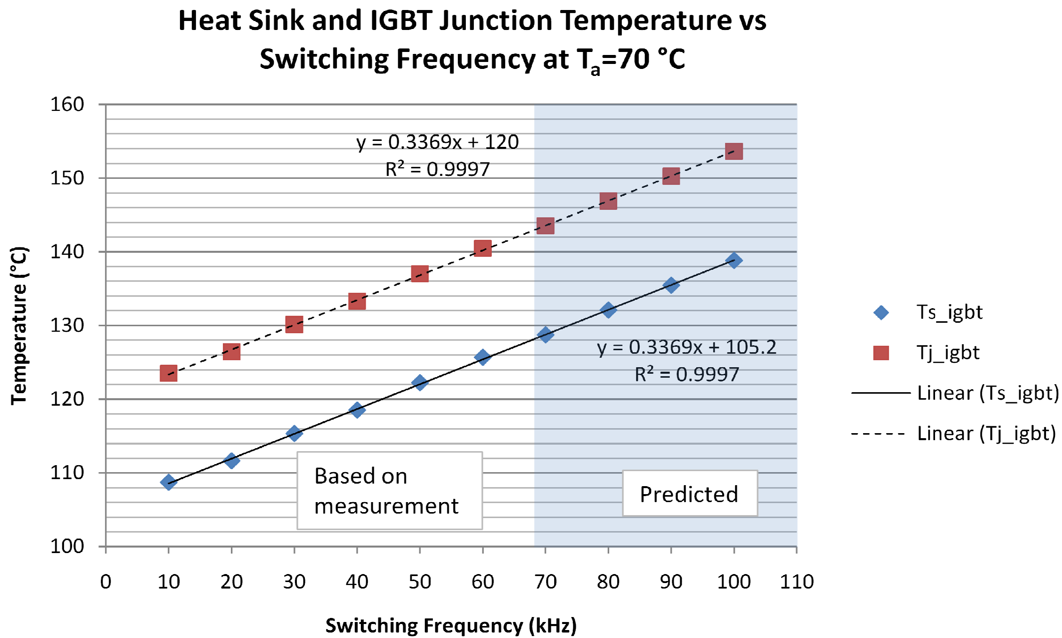


Figure 3-13: Projected IGBT heat sink and junction temperature at T_a= 70°C

It can be seen that the IGBT junction temperature reaches 143.5°C at the design specifications of T_a= 70°C and f_{sw}= 70 kHz; hence the thermal design provides enough cooling to maintain the IGBT below its maximum junction temperature (150°C). These results conclude the validation of the thermal design. In the following section the power density of the VSI is quantified.

3.5 Power density

High power density is one of the major goals of this work. As such, the overall weight of the inverter power stage receives special attention and motivated the careful selection of components throughout the design. Surface mount technology (SMT) allows space and weight savings on the PCB; therefore SMT components were preferred over through-hole (TH) technology to achieve compactness and weight reduction. Figure 3-14 shows a picture of the complete inverter system: power stage (bottom), signal conditioning board (middle) and controller (top).

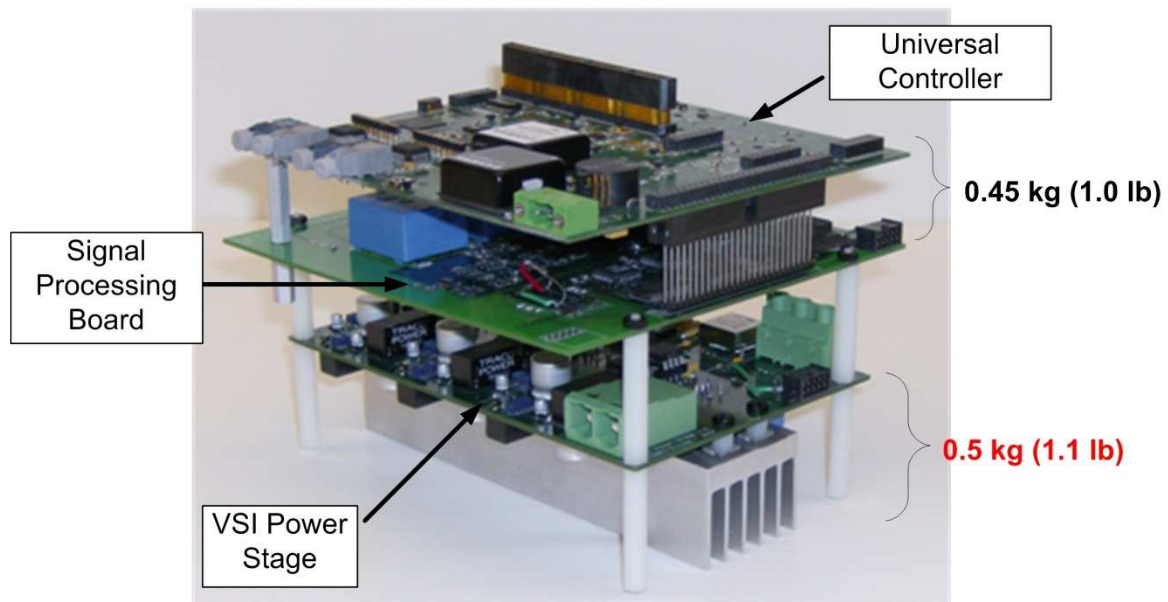


Figure 3-14: Inverter power stage and controller weight

The power stage board including the heat sink and fan weighed 500 g (1.1 lb), approximately. On the other hand the signal conditioning and controller boards together weighed 450 g (1.0 lb). The signal conditioning board and UC are excluded from the power density discussion as they are external to the VSI. The total power density of the inverter power stage is:

$$P_{density} = \frac{P_{out}}{weight} = \frac{2000\text{ W}}{500\text{ g}} = 4\text{ kW/kg} \tag{3.6}$$

3.5.1. Weight Contribution Breakdown

In an effort to identify the largest weight contributors, the inverter power stage components were grouped in eight categories as shown in Table 3-5 with their respective weight contribution.

TABLE 3-5
CLASSIFICATION OF POWER STAGE COMPONENTS AND THEIR WEIGHT CONTRIBUTION

Category	Component	Weight
Thermal Management	heat sink, fan	253.45 g
Auxiliary Power Conversion	15 V, 12 V and 5 V power supplies	41 g
Power Semiconductor	IGBT, SiC diode	17.28 g
Connectors		21.40 g*
Sensors	current sensors	20 g
Passives	resistors, capacitors, CM chokes, ferrite beads	29.05 g
Logic	Optocoupler with DIP socket, AND gate, hex inverter	5.49 g
Mechanical	DIP sockets, bare PCB, nylon screws, nylon spacers, nylon stand-offs, gap pad	112.33 g**
TOTAL		**500 g**

*Includes the following connectors: dc link, 3-phase output, 28 VDC input, PWM signal input, sensor output, and fan supply.
**Calculated from the difference of 500 g (total weight of power stage) and the sum of the weights of each category (387.67 g) excluding Mechanical.

Table 3-5 facilitates identification of the heaviest components on the board. The total weight of the inverter power stage is 390.73 g. It should be noted that in the Mechanical category, the six DIP sockets that hold the optocoupler chips weigh 3.06 g. Unfortunately, an accurate weight measurement of the bare PCB, nylon screws, spacers, and thermal gap components was not available, yet their combined weights was estimated

at 109.27 g or 22% of the total power stage weight. Most part of this 22% comes from the bare PCB as the nylon screws, spacers and thermal gap have negligible weight when compared to the PCB alone. Lastly, it is worth mentioning that wires that connect to the board (dc link input, ac output, control voltage, sensor signals) were not accounted for in the total weight calculation. The chart in Figure 3-15 illustrates the weight contribution of each group of components.

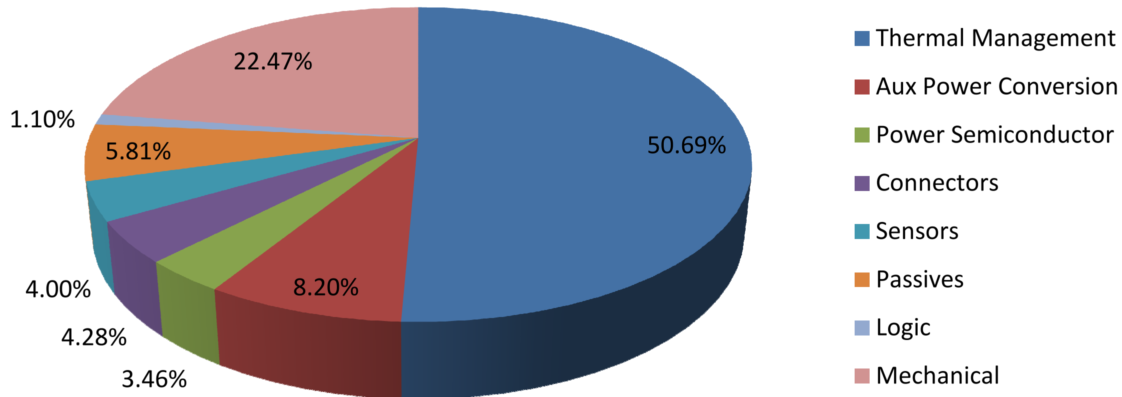


Figure 3-15: Weight contribution of power stage components

It is evident that Thermal Management is by far the heaviest group of the system with 50.69% of the total weight. The next heaviest contributor is the Mechanical group (22.47%) followed by the Auxiliary Power Conversion group with 8.20% of the total weight. Passives occupy the fourth place with 5.81%. Each remaining category, contribute less than 5% of the system total weight.

The results of this section show that thermal management, mechanical components, and auxiliary power conversion are areas that deserve special attention in high power

density inverters. The emerging SiC technology promises lower power dissipation which could help reduce the size and weight of motor drives significantly. It has been mentioned however that the normally-on characteristic of SiC JFETs for instance forces the designer to take special precautions in reference to gate drive circuitry and potential shoot-through events. The latter is treated in detail in Ch. 4 and 5.

Chapter 4 DC LINK OVERCURRENT FAULT PROTECTION

4.1 The Shoot-Through Fault

The second part of this work is devoted to overcurrent protection challenges in voltage source inverters. Inverters, particularly those in motor drive systems, ought to be protected against overcurrent and overvoltage faults. Although different in nature, these two types of fault have detrimental impact on the inverter power stage and the motor windings. Unattended, these faults affect the reliability and durability of both the inverter and motor, and could ultimately inflict sufficient damage causing malfunction, undesired downtime and repair costs. The amount of damage will be dictated by the nature and magnitude of the fault, as well as the response time of the protection circuit. The subsequent discussion is relevant to the overcurrent fault that arises from simultaneous conduction of the switches on a same phase-leg, namely *shoot-through*. This type of fault is shown in Figure 4-1.

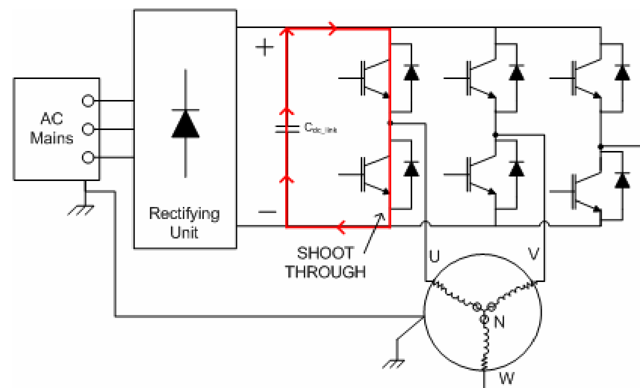


Figure 4-1: Dc link shoot-through fault

A shoot-through fault originates when the top and bottom switches of the same phase-leg conduct simultaneously, effectively shorting the dc bus. This dangerous fault is the result of a faulty gate drive, a latched-up switch, a dv/dt induced turn-on, improper dead-time between complimentary switches, or a glitch in the modulator code. Regardless of the cause, high performance motor drives must be equipped with adequate shoot-through protection. Recent advances in normally-on SiC technology have tightened the necessity for shoot-through protection and robust gate drive design.

In this chapter a novel shoot-through fault protection is proposed and verified experimentally. It will be shown that this protection circuit proves advantageous for inverters based on both normally-off devices like IGBTs and MOSFETs, and normally-on devices, like SiC JFETs. Experimental results validate the functionality and effectiveness of this protection circuit in Ch. 5.

4.2 DC Link Overcurrent Fault Protection

In this section a novel circuit is described and presented as a viable protection mechanism against shoot-through faults. The motivation behind the proposed protection circuit arises from the necessity of protecting the increasingly popular SiC JFET that, among other properties, is well known for its *normally-on* behavior. Nevertheless, the benefits of the protection scheme presented in this section are not device dependent and can be extended to the more traditional normally-off devices like IGBTs and MOSFETs. It will be shown that a simple modification to the VSI dc link can provide additional overcurrent protection regardless of the power stage devices. This is possible owing to the fact that the proposed protection circuit utilizes the dc link midpoint – common node between the dc link capacitors – as the venue to extinguish the shoot-through current.

4.2.1. Protection Scheme

The novel protection mechanism proposed in this section was conveniently named *dc link protection*[1] in direct reference to its location in the circuit. Figure 4-2 shows a conceptual picture of the dc link protection in a motor drive application (VSI + motor). The protection circuit which comprises a bidirectional switch and a high impedance path is connected between the two dc link capacitors as shown in the figure.

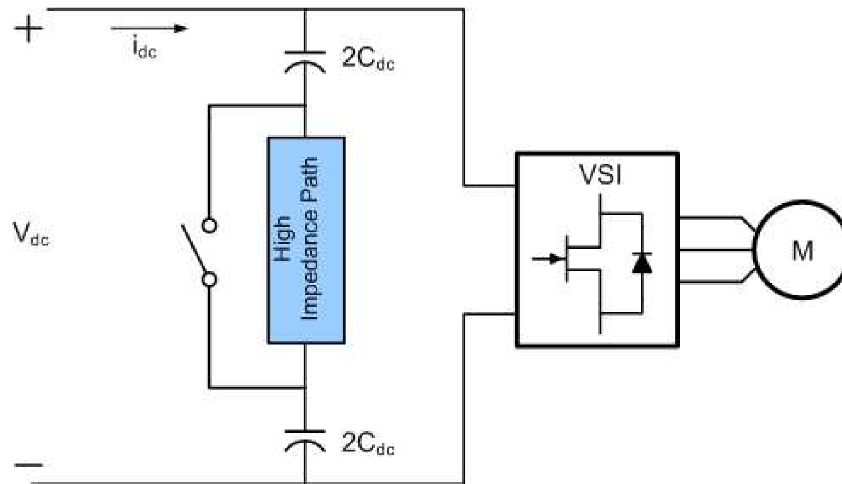


Figure 4-2: Dc link protection concept

It should be noted that the dc link midpoint is established by means of the bidirectional switch. When the switch is closed, a low impedance path exists between the dc link capacitors. In contrast when the switch is open the midpoint is disrupted and a high impedance network is inserted between the dc link capacitors. During shoot-through the fault current flows through the dc link capacitors because they provide a low impedance path. With the dc link protection in place, the short-circuit current is effectively diverted to the high impedance path. By doing so, the current is now limited by the impedance of the new path and both the dc link capacitors and power stage

[1] The dc link protection concept was first proposed by CPES researcher and PhD candidate Rixin Lai in January, 2007. The concept was later studied and implemented by the author of this work. In an effort to acknowledge and give proper credit to the originator of this idea the name *dc link protection* has been adopted in this work.

switches in the VSI are protected. A convenient byproduct of this method is the additional inrush limiting function that is obtained at system startup. From the system point of view, it is necessary to pre-charge the dc link capacitors before the power is transferred to load. This limits the amount of inrush current when power is first applied and avoids exposing the controller to the extreme case of no voltage in the dc link. Proper synchronization of the bidirectional switch allows *slow* pre-charge of the dc link capacitors through the high impedance path.

An illustration of the modes of operation of the dc link protection is shown in Figure 4-3. At system startup (Figure 4-3a), bidirectional switch S_{bi} is commanded off such that the high impedance path Z_{high} appears across the dc link midpoint. The dc link capacitors are then pre-charged slowly at a rate dictated by Z_{high} thus mitigating the inrush current. Once the capacitors have been pre-charged, S_{bi} closes and bypasses Z_{high} to establish the dc link midpoint as shown in Figure 4-3b. This state represents the normal operation mode of the VSI. When a shoot-through fault occurs, the equivalent circuit at the dc link can be simplified as shown in Figure 4-3c. The shoot-through current is confined to the loop formed by the dc link capacitors, the stray inductance $L_{parasitic}$, and the equivalent resistance R_{eq} of the loop. R_{eq} in turn is the sum of the bus resistance, the dc link capacitor ESR, and the equivalent on-resistance of the phase-leg power switches involved in the fault. Note that each capacitor is charged to half of the dc link voltage prior to the fault.

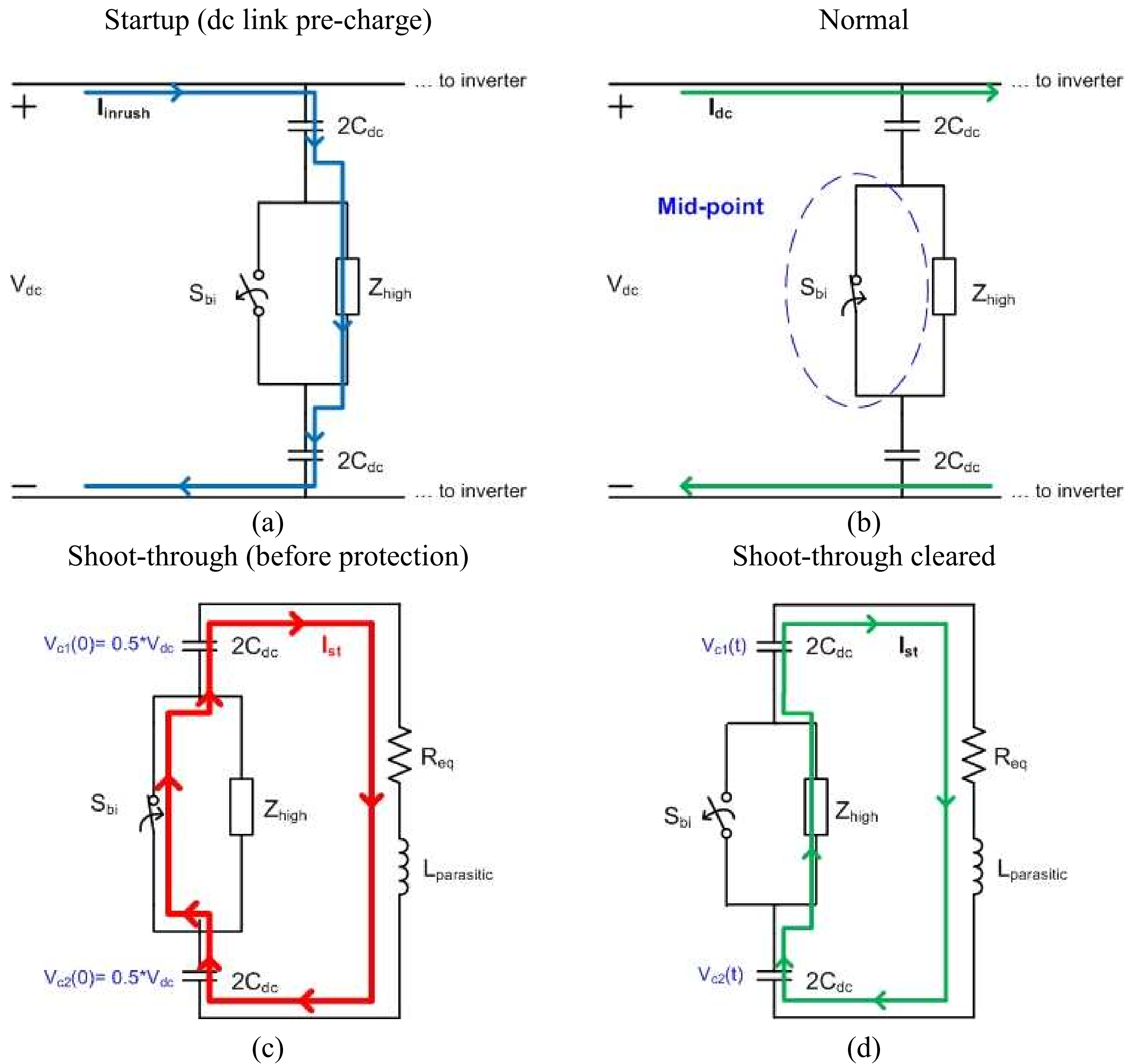


Figure 4-3: Modes of operation of the dc link protection: (a) startup, (b) normal, (c) fault before protection, (d) fault cleared

When the overcurrent fault is detected, S_{bi} opens and the midpoint is disrupted. The shoot-through current is contained by forcing it to flow through the high impedance path. This in turn allows the dc link capacitors to discharge at a slower rate dictated by Z_{high}.

Neglecting the front-end dc source that feeds the dc link voltage, the circuit in Figure 4-3c can be regarded as an underdamped RLC circuit as stated in section 1.6.1. With this

assumption in place the shoot-through current as a function of time is described by (4.1) and the peak shoot-through current by (4.2) as defined earlier in section 1.6.1.

$$i_{st}(t) = \frac{V_o}{\omega_o L} e^{-\frac{R}{2L}t} \cdot \sin(\omega_o t) \tag{4.1}$$

$$I_{st,pk} = \frac{V_o}{\omega_o L} e^{-\frac{R_{eq}\pi}{L\omega_o}} \tag{4.2}$$

Where, V_o is the dc link voltage prior to the fault, $L=L_{parasitic}$ (total parasitic inductance of the path), $R=R_{eq}$ (total parasitic resistance of the path) and ω_o is the frequency of oscillation of the RLC network defined previously in (1.8) and shown again in (4.3) for convenience.

$$\omega_o = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2} \tag{4.3}$$

The effect of the loop equivalent resistance becomes apparent in Figure 4-4 where (4.2) is plotted for several values of R_{eq}.

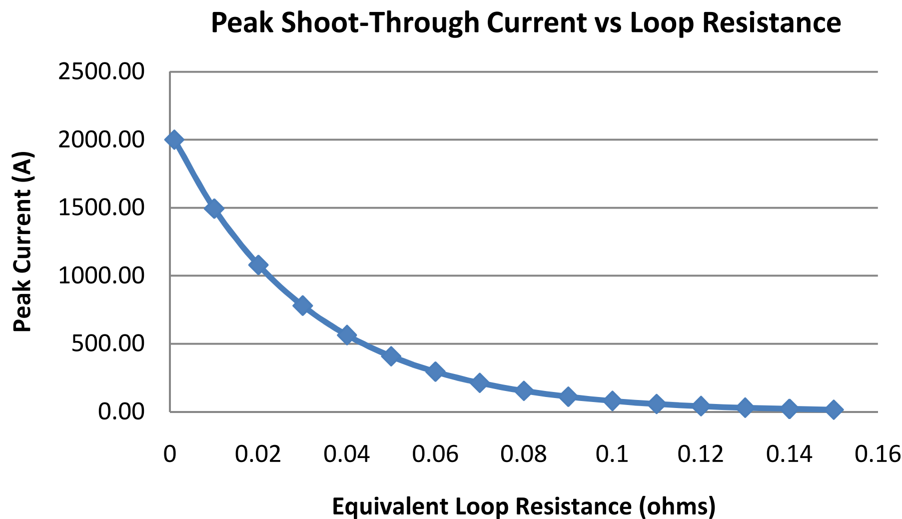


Figure 4-4: Effect of equivalent loop resistance on peak shoot-through current

Not only does R_{eq} damp the current oscillation, it also acts as a limiting agent to the shoot-through current. More properly, R_{eq} dictates the behavior of the RLC network by configuring the circuit into an underdamped, critically damped, or overdamped system. The damping and current limiting effect of R_{eq} was shown in Figure 1-12. Inserting the high impedance path Z_{high} in the dc link effectively adds to the total equivalent resistance seen by the shoot-through current. From Figure 1-12 it is evident that increasing R_{eq} reduces the peak current during fault. Note that the proposed dc link protection increases the equivalent impedance of the loop only at start-up (inrush limit) and a during shoot-through fault. During normal steady-state operation, the high impedance network remains effectively disconnected from the circuit.

4.2.2. Dc Link Protection Circuit

Until now the new protection scheme has been presented and its operation has been described. In this section the practical implementation of the dc link protection circuit is illustrated in detail. As discussed in section 4.2.1 the dc link protection comprises a bidirectional switch and a high impedance path. Figure 4-5 depicts a circuit that implements the proposed protection scheme. The bidirectional switch is accomplished with an electromechanical relay (S_1) and a solid-state switch (S_2). The solid-state switch is an IGBT with anti-parallel diode D. Electromechanical switches like contactors and relays have the ability to conduct current in both directions, but their reaction time is typically in the order of several milliseconds; too slow to protect against shoot-through faults. Additionally, they suffer from inherent contact *bouncing* – also known as re-ignition.

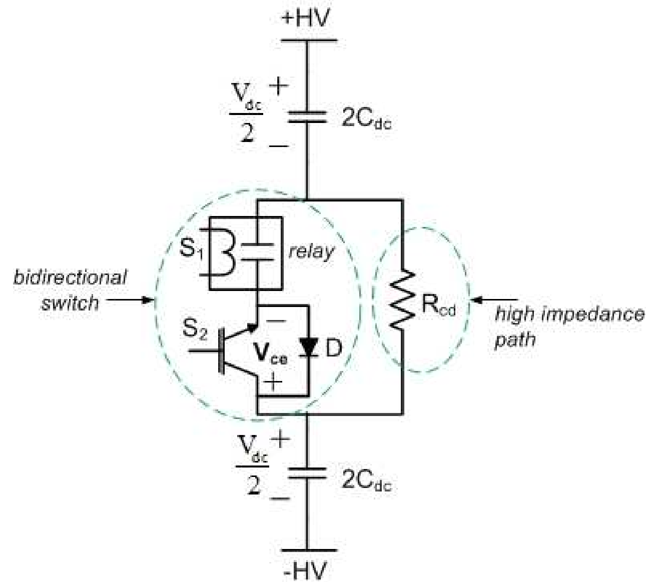


Figure 4-5: Dc link protection circuit implementation

Although optimized for unidirectional operation, solid-state switches have typical turn-on and turn-off times in the order of nanoseconds and do not experience re-ignition at turn-on or turn-off. Solid-state switches however exhibit higher conduction losses than typical relays, thus favoring a hybrid solution for implementing the bidirectional switch. Therefore, the bidirectional switch in Figure 4-5 takes advantage of the very low conduction resistance of electromechanical relays and the fast response of solid-state switches. In addition, solid-state switches exhibit current monitoring capability via desaturation detection as discussed in section 1.6.2. Note that S_1 and S_2 allows current to flow in both directions. During normal operation the ac component of the dc link current is filtered by the dc link capacitors and current flows through S_1 and D (positive ac cycle) or via S_2 and S_1 (negative ac cycle). When a shoot-through fault occurs current follows the path depicted in Figure 4-3c via S_2 and S_1. Therefore, the bidirectional switch allows filtering of the dc link current during normal operation, and shoot-through current, during fault mode.

The high impedance path of the dc link protection circuit is realized with a sufficiently large resistor R_{cd} as shown in Figure 4-5. R_{cd} restrains the fault current and thus dissipates the shoot-through energy stored in the dc link capacitors. Recall that the R_{cd} path is only available at system startup – to limit inrush current – and, following a shoot-through fault. Aside from these two cases, R_{cd} remains shunted by the bidirectional switch to allow normal operation of the inverter.

Overcurrent detection in the dc link protection circuit is performed via desaturation detection on S_2. Excessive current in S_2 will generate a correspondingly high voltage drop across the switch as the device abandons its saturation region. The voltage across S_2 is then compared to a preset limit that, if exceeded, will cause S_2 and S_1 to open which in turn diverts the fault current to R_{cd}. Obviously, the inherent slow response of the relay will cause a significant delay in S_1 as referenced to S_2. Nevertheless, this difference is negligible since it takes one switch to disrupt the midpoint and successfully divert the current to R_{cd}.

4.3 Design Considerations

The proposed dc link protection requires proper setting of the current trip level as well as appropriate sizing of the components in the protection circuit. In this section an approach to setting the desired current limit is presented based on the characteristics of the phase-leg switches. In addition, this section covers the selection of the protection circuit components used in the design including the desaturation detection circuit.

4.3.1. Current Limit

When using the dc link protection or any traditional protection circuit in an inverter, the devices to be protected are the power stage switches; hence they determine the current

limit. The *pulse current rating* of the switches which is typically several times their rated current indicates the maximum current a device is guaranteed to tolerate without damage for a finite amount of time. The pulse duration is usually a few microseconds. To set an appropriate current limit one must consider two parameters: 1) nominal current of the inverter and 2) pulse current of the switches. The following example is provided to explain current limit setting in the dc link protection circuit and also serves as the baseline for the protection design covered in this chapter.

Example: Current Limit Selection

A 10 kW, 230 V_{rms} three-phase inverter using SiC JFETs is to be protected using the dc link protection circuit. The full load RMS current is about 15 A or 21.21 A peak. Actual SiC JFETs from SiCED® are rated at 5 A RMS, thus requiring at least three JFETs connected in parallel to achieve full power (15 A, RMS). Setting the current limit close to peak rated current (21 A) of the three paralleled SiC JFETs would be too conservative and may cause nuisance tripping of the system. Switching devices in general are capable of withstanding high peak currents for a short time. For that reason, the pulse current rating of the device should be examined to determine a more appropriate current limit. The pulse current rating of a single 3 mm x 3 mm SiC JFET die from SiCED® is estimated at 22 A. Therefore, three SiC JFETs in parallel have a maximum pulse current rating of 66 A. The pulse duration can be assumed to be a few microseconds. The protection current limit can now be set to a value that satisfies the inequality in (4.4).

$$I_{peak} < I_{limit} < I_{pulse} \tag{4.4}$$

Where, I_{peak}, I_{limit}, and I_{pulse} are the peak nominal current of the inverter, the current trip limit of the protection circuit, and the pulse current rating of the switching

devices, respectively. I_{limit} was set to 35 A, just above 50% of I_{pulse}. The selected trip point allows adequate margin between the current limit and both the nominal peak current and the pulse current rating of the protected devices. This in turn provides better immunity against false tripping. On the other hand, the 35 A limit is below the pulse current rating of the three paralleled SiC JFETs; hence the current capacity of the devices is not exceeded.

Although the example above utilizes SiC JFETs, the same principle can be extended to IGBT or MOSFET based inverters, thus making the proposed protection circuit *device independent*. Now that a current limit has been set, the components of the dc link protection circuit are selected next.

4.3.2. Component Selection

This section covers practical aspects in the selection of components for the dc link protection circuit. The bidirectional switch The combination of electromechanical and solid-state technologies to form the bidirectional switch responds to the need for low power dissipation, fast response, and current monitoring capability. The relay offers very low power dissipation, whereas the IGBT provides fast response and current detection capability via desaturation.

4.3.2.1. Relay, (S_1)

A relay and IGBT were proposed in section 4.2.2 to accomplish bidirectional switching. The key parameters in selecting the relay are size, weight, and low contact resistance. These parameters must be minimized to reduce total weight and losses. The selected relay is a single-pole-single-throw low profile miniature power relay from Tyco Electronics, whose characteristics are summarized in Table 4-1.

TABLE 4-1
PROPERTIES OF TYCO ELECTRONICS RELAY (P/N: OUDH-SH-112DM)

Property	Value
Dimensions	0.86 in x 0.67 in x 0.6 in (21.8 mm x 17.1 mm x 15.3 mm)
Weight	10 g
Contact resistance	100 mΩ
Current rating	10 A
Operate time	10 ms
Release time	5 ms
Termination	PCB mountable

The selected relay is a normally open switch; contact is made by energizing the relay coil. In other words, its coil must be energized for the relay to conduct. In the absence of enough voltage across the coil, the relay de-energizes and goes back to its original open state.

4.3.2.2. IGBT (S_2)

The selection of the IGBT was driven by three aspects primarily: 1) low conduction loss, 2) high pulse current rating, and 3) small form factor. In addition, the output transfer characteristic of the device plays an important figure of merit when selecting the IGBT as this information is vital for tuning the desaturation detection circuit accurately. Switching performance is not crucial, since the IGBT is meant to conduct current continuously and only required to turn off during overcurrent faults. Also, the location of the IGBT in the dc link midpoint reduces the necessity for a large blocking voltage device given that the IGBT is not subjected to the dc bus voltage stress. Ideally, neither during normal operation nor fault condition is the IGBT blocking any voltage. This turns out to be an advantage in the selection of a low conduction loss IGBT since $V_{ce,on}$ tends to decrease as the rated blocking voltage of the device decreases. It will be shown experimentally,

however, that the IGBT is indeed subjected to voltage stress for a short time during the shutdown sequence of the protection circuit.

In the search for an IGBT with the characteristics described above, several candidates were considered and it was found that IGBTs optimized for plasma display panels (PDP) exhibit the characteristics needed for the dc link protection circuit. The repeated energy recovery and discharging of capacitive circuits in PDP applications make them suitable for the proposed overcurrent protection. This type of IGBTs are optimized for high peak current capability, low forward voltage drop, and fast turn-on capability [36]. The high discharge current in PDP systems resembles the dc link discharge current during a shoot-through fault. As PDP IGBTs are optimized to handle high discharge currents repeatedly, their latch-up current is high, thus making them a perfect fit to handle shoot-through events. Furthermore, the low conduction voltage associated to PDP IGBTs favors their use in continuous conduction operation.

Various semiconductor manufacturers like Fairchild Semiconductor and International Rectifier offer IGBTs optimized for PDP applications in the 250 to 400 V range and in compact packages like the TO-220. Fairchild's FGPF30N30 IGBT was selected for its output transfer characteristic. The plot is shown in Figure 4-6 as obtained from the manufacturer datasheet. The example in section 4.3.1 showed that protecting SiCED's SiC JFETs would require setting the current limit to 35 A. In Figure 4-6, the curve for V_{ge}= 8 V shows that the protection IGBT saturates close to 30 A. Similarly, at V_{ge}= 10 V the current saturates at 60 A. Since I_{limit} has been set to 35 A, the protection IGBT must be driven as close to 8 V as possible to benefit from the saturation characteristic at V_{ge}= 8 V. In the event of a shoot-through fault, the voltage across the

IGBT follows the I_c vs V_{ce} curve for V_{ge}= 8 V in Figure 4-6, hence activating the desaturation detection circuit.

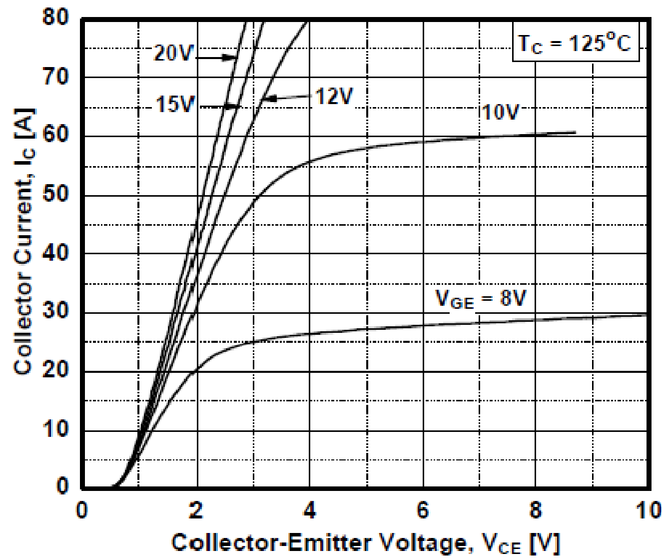


Figure 4-6: IGBT FGPF30N30 output transfer characteristic per device datasheet

Nevertheless, measurement of the output transfer characteristic of the selected IGBT on a curve tracer revealed that there is a moderate discrepancy between the real saturation current and the one published on the datasheet. The curve tracer measurements are shown in Figure 4-7.

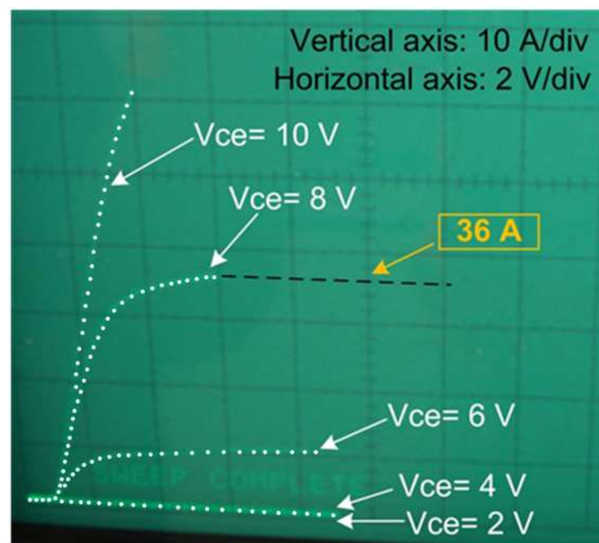


Figure 4-7: Output transfer characteristic of IGBT FGPF30N30 as measured with the curve tracer. Vertical axis: I_c 10 A/div, horizontal axis: V_{ce} 2 V/div

The curve tracer plots indicate that the IGBT current saturates around 36 A for V_{ge}= 8 V and beyond 60 A for V_{ge}= 10 V – moderately different from the datasheet values. A short-circuit test in the actual protection circuit confirmed the IGBT current saturation level as shown in Figure 4-8. The IGBT is being driven at 8 V and the current saturates at 34 A approximately, which confirms the results obtained with the curve tracer. When selecting the protection IGBT (S_2), datasheet information must be validated with the real measurement of the IGBT output transfer characteristic so that the gate voltage is adequately sized and the desired current saturation level is achieved in accordance with the preset current limit.

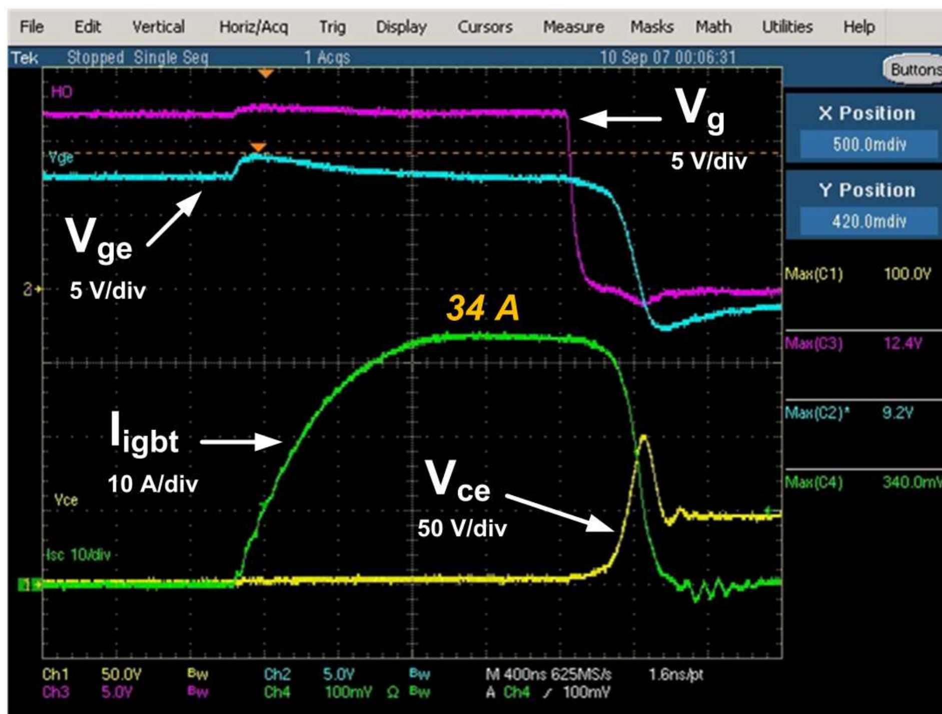


Figure 4-8: Saturated IGBT current (green) for V_{ge}= 8V. I_{igbt} scale 10 A/div

4.3.2.3. Diode (D)

Low forward voltage drop is the main drive in the selection of diode D. The diode is only required to conduct during normal operation of the inverter. Together with the relay

the diode establishes a low impedance path or quasi-midpoint between the two dc link capacitors. To retain the low impedance characteristic of the midpoint, the diode must be designed for low forward voltage drop. As with the IGBT, the diode is only subjected to low voltage stress. This however is an idealistic statement that ignores the effect of stray inductance and relay reaction time. The test results in Ch. 5 will show that when these non-idealities are factored in the diode must withstand the voltage stress that appears across the IGBT at turn-off. With these considerations in mind the selected diode is MUR1560 from ON Semiconductor. This is a low forward voltage drop ultrafast rectifier rated for 15 A and 600 V. The forward characteristic of the diode is shown in Figure 4-9 as obtained from the manufacturer datasheet.

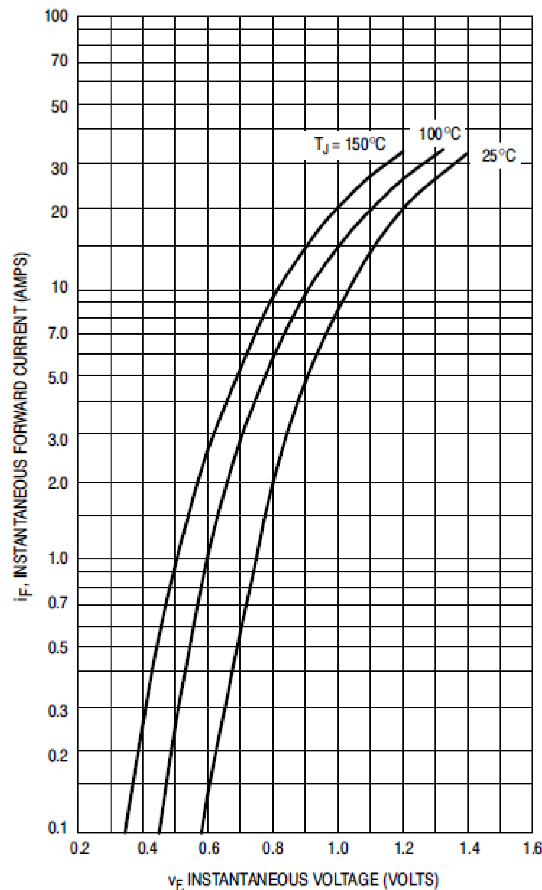


Figure 4-9: MUR1560 datasheet forward characteristic

Since the diode is expected to carry only a fraction of its rated current, the voltage drop is anticipated to be low. Therefore, the series combination of the relay contact resistance and the diode equivalent resistance is low enough to retain the low impedance characteristic of the inverter midpoint.

4.3.2.4. Gate Drive / Desaturation Detection

The gate drive circuit serves the dual purpose of 1) driving the IGBT and relay and 2) detecting overcurrent via desaturation detection. As opposed to switching applications where the gate drive circuit is continuously sourcing and sinking current to and from the switching device, the nature of the dc link protection demands a constant gate drive voltage to allow the IGBT to conduct continuously during normal operation. The gate drive voltage is disabled when the desaturation detection circuit has been triggered as a result of excessive current, thus forcing the IGBT to turn off. The driving and desaturation detection functions were addressed using chip IR2127 from International Rectifier[2] – a monolithic gate driver chip that implements both functions in the same package. This approach helped in reducing dc link protection part count and optimizing PCB real estate. The operation of IR2127 is similar to traditional gate driver chips in that it receives a logic signal that enables or disables the gate drive voltage, but in addition it incorporates a desaturation detection feature that overwrites the enable logic signal. The pin-out and basic functions of the IR2127 chip are shown in Figure 4-10.

[2] An alternate solution is part MC33153 from ON Semiconductor whose capabilities are similar to the IR2127 chip but was not available at the time of this work.

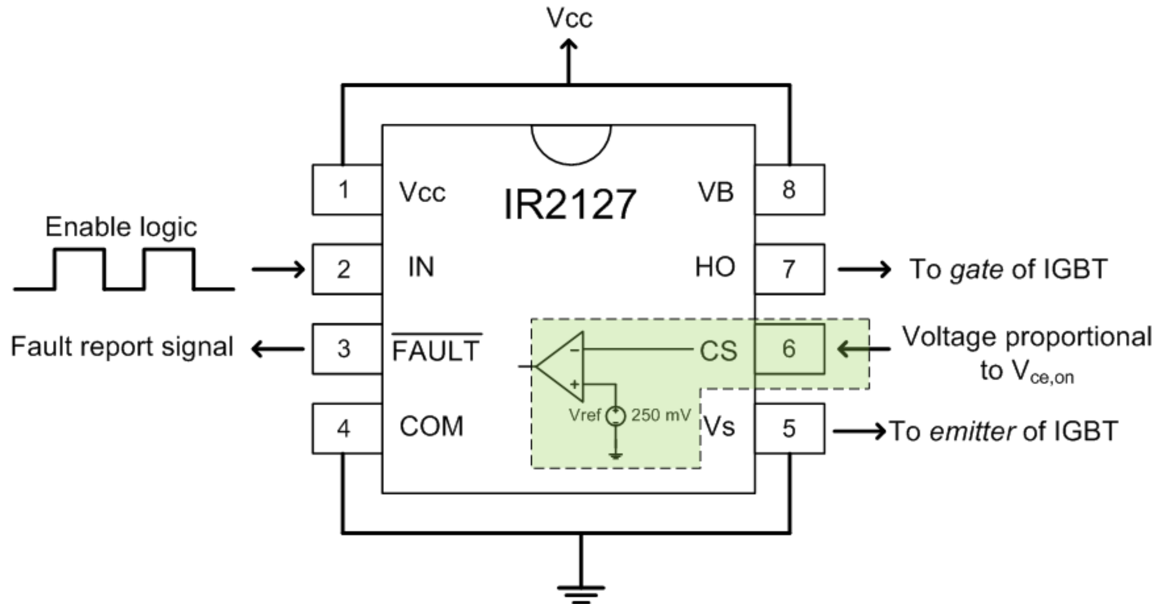


Figure 4-10: Pin-out of gate driver chip IR2127

The floating capability (high side switch operation) of the IR2127 is not required in the dc link protection and can be bypassed by connecting the V_{cc} and V_B pins to the supply voltage and the COM and V_s pins to ground as shown in Figure 4-10. The IN pin receives the enable logic signal. When the signal at this pin is high the output HO is enabled and the IGBT is on. The inverse applies when the signal is low. Proper operation of the dc link protection requires the enable signal to be high at all times (IGBT on). The CS or *current sense* pin implements the desaturation protection feature by comparing a voltage proportional to $V_{ce,on}$ with an internal 250 mV reference as shown by the highlighted region in Figure 4-10. This allows the user to custom set the current limit by adjusting the resistor values of the $V_{ce,on}$ voltage divider. Using the information from the current limit example in section 4.3.1 and the selected IGBT characteristics discussed in section 4.3.2.2, the voltage threshold at pin CS was chosen to be proportional to 30 A. When the voltage at CS exceeds 250 mV –indication of IGBT desaturation– the following events take place: the enable logic signal (at pin IN) is ignored, the output HO

becomes low, the IGBT turns off diverting the fault current to R_{cd}, and an active low signal at pin FAULT reports the shoot-through fault. This signal could then be used to initiate a power down sequence of the inverter if deemed necessary. From the system level perspective, the elapsed time between disabling the output HO and reporting the fault to the system is critical and should be minimized. The fault report time of IR2127 was measured as shown in Figure 4-11.

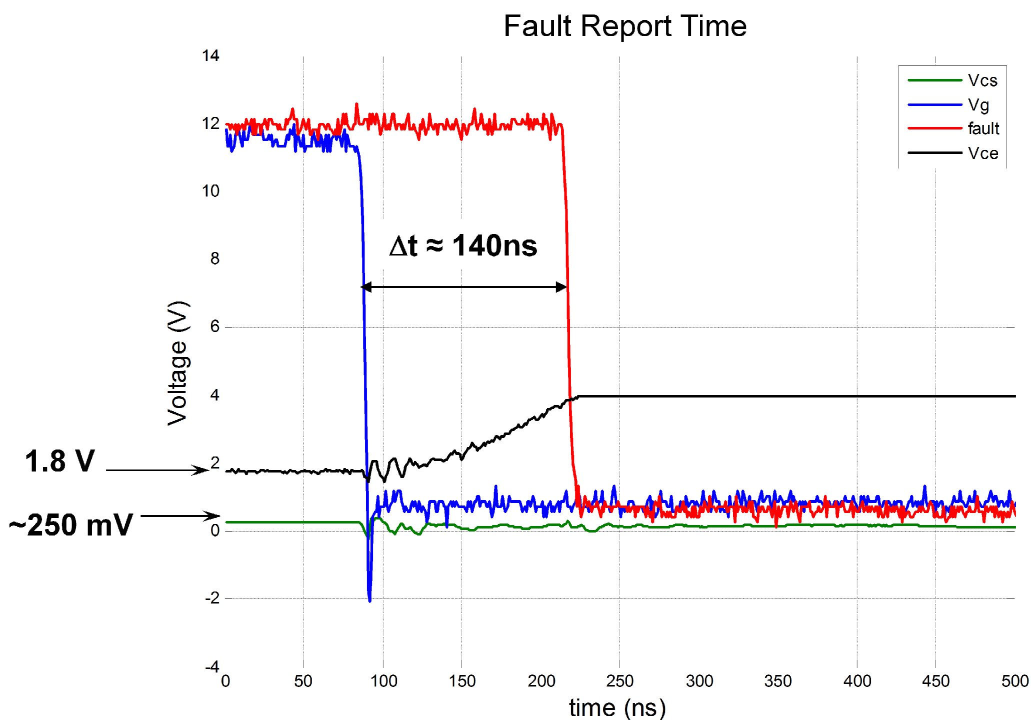


Figure 4-11: Fault report time of the IR2127

Note that the trip voltage was set to $V_{ce,on}$= 1.8 V which corresponds to a switch current of 15 A with the selected IGBT. When V_{CS} exceeds the internal 250 mV reference the gate voltage V_g (same as HO) is disabled and the fault report signal triggers low after 140 ns.

4.3.2.5. Resistor (R_{cd})

Resistor R_{cd} is the high impedance path to which the shoot-through current is redirected when the protection system triggers. The energy in the dc link capacitors is dissipated here; therefore R_{cd} must be designed to withstand the peak energy contained in the dc link capacitors. In addition, the voltage rating of R_{cd} must be greater than the dc link voltage. The energy stored in the capacitors before the shoot-through fault is determined by (4.5).

$$E_c = \frac{1}{2} C_{dc} (V_{dc})^2 \tag{4.5}$$

Where C_{dc} and V_{dc} are the total dc link capacitance and the total dc link voltage, respectively. For the purpose of this work a total dc link capacitance of 20 μF and a dc link voltage of 200 V were used. Substituting these values in (4.5) results in 400 mJ. Other inverters, however, operate from a 600 V dc bus with a dc link capacitance in the order of hundreds or even thousands of microfarads. According to (4.5) the energy stored in a 600 V, 1000 μF dc link would be 180 Joules! This amount of energy is several times higher than the fusing energy of most general purpose and even some high energy resistors. Therefore the selection of R_{cd} should not be treated lightly. After all, the purpose of R_{cd} is to dissipate the shoot-through energy that otherwise would have been dissipated in the phase-leg switches giving way to their destruction.

The second parameter that must be considered in the design of R_{cd} is the resistance value itself. This in turn determines the capacitor discharge time and the fault current magnitude. Certainly, higher resistance reduces the peak current but increases the discharging time of the dc link capacitors. A R_{cd} of 1 kΩ provides a good compromise between peak current (4.6) and discharging time (4.7):

$$I_{pk} = \frac{V_{dc}}{R_{cd}} = \frac{200}{1000} = 200 \text{ mA} \tag{4.6}$$

$$t_d = 5 \times R_{cd} C_{dc} = 5 \times 1000 \times 20 \times 10^{-6} = 100 \text{ ms} \tag{4.7}$$

For V_{dc}= 200 V and C_{dc}= 20 μF the high impedance path R_{cd}= 1000 Ω limits the peak fault current and dissipates 400 mJ in 100 ms.

In summary the shoot-through protection circuit presented in this chapter offers a novel and inexpensive solution against shoot-through faults. By residing in the inverter dc link midpoint the circuit is activated only when excessive current flows through the dc link. The components required to realize this protection are readily available: an IGBT, a small relay, a diode, a driver with enable function, and a limiting resistor. Guidelines for the selection of these components were provided in section 4.3.2. In chapter 5, the dc link protection circuit is tested on a prototype board and its performance is verified.

Chapter 5 DC LINK PROTECTION VALIDATION

5.1 Test Setup and Methodology

To validate the functionality of the dc link protection, the circuit in Figure 5-1 was built on a prototype board using two 40 μF capacitors and the components described in section 4.3.2. Note that the protection circuit has been inserted in the midpoint between the two dc link capacitors. The capacitors appear in series through relay S_1 and diode D for a total dc link capacitance of 20 μF. The chip IR2127 drives the IGBT S_2 and also provides enough voltage to energize the relay coil. A voltage divider at the gate of S_2 maintains the gate voltage at 8 V with respect to the emitter. Diode D_{desat} monitors $V_{ce,on}$ and feeds a proportional voltage V_{cs} to the current sense pin CS of the IR2127 chip through another resistor divider. The divider was set such that the protection triggers when the current in the dc link exceeds 35 A. The terminals on the right-hand side of the circuit are used for shorting the dc link, thus resembling a shoot-through fault. Initially, the dc link capacitors are completely discharged and contactor K_1 is open. The experiment begins by closing contactor K_1 and allowing the capacitors to charge up to 200 V. During this step output HO of IR2127 is low so that relay S_1 and IGBT S_2 are open and the charging current is limited by R_{cd}. Once the capacitors have been charged, K_1 opens and the dc power supply is effectively removed from the circuit. Next, the gate voltage HO energizes relay S_1 and turns on IGBT S_2 to establish the low impedance midpoint. The capacitors remain charged while this process takes place. To emulate the shoot-through fault, the positive and negative dc bus rails are shorted on the right side

terminals of the circuit using a copper wire. As the dc link capacitors discharge through the wire the current increases rapidly and the protection circuit reacts to the fault. The results of this experiment are presented next in section 5.2.

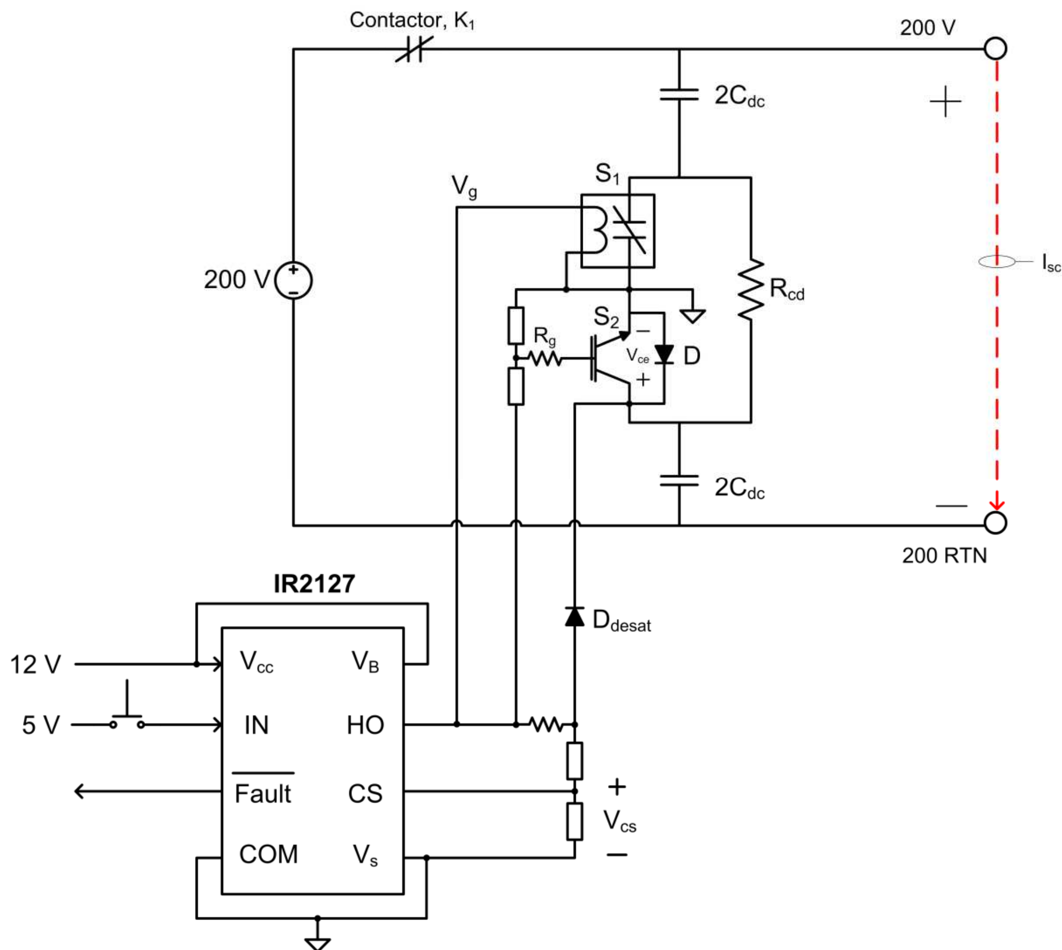


Figure 5-1: Dc link protection testbed circuit

5.2 Test Results

Testing of the dc link protection circuit was carried out on a prototype PCB developed in-house. The transient waveforms generated during the shoot-through fault were used to validate the functionality of the protection system. Figure 5-2 shows the gate driver voltage HO, the gate-emitter voltage V_{ge} measured at the IGBT terminals, the collector-emitter voltage V_{ce}, and the short-circuit current I_{sc} during the shoot-through

test. Note that prior to the fault, HO is 12 V and V_{ge} is held at 8V – keeping S_1 and S_2 in their conduction mode – thus creating a low impedance path at the dc link midpoint.

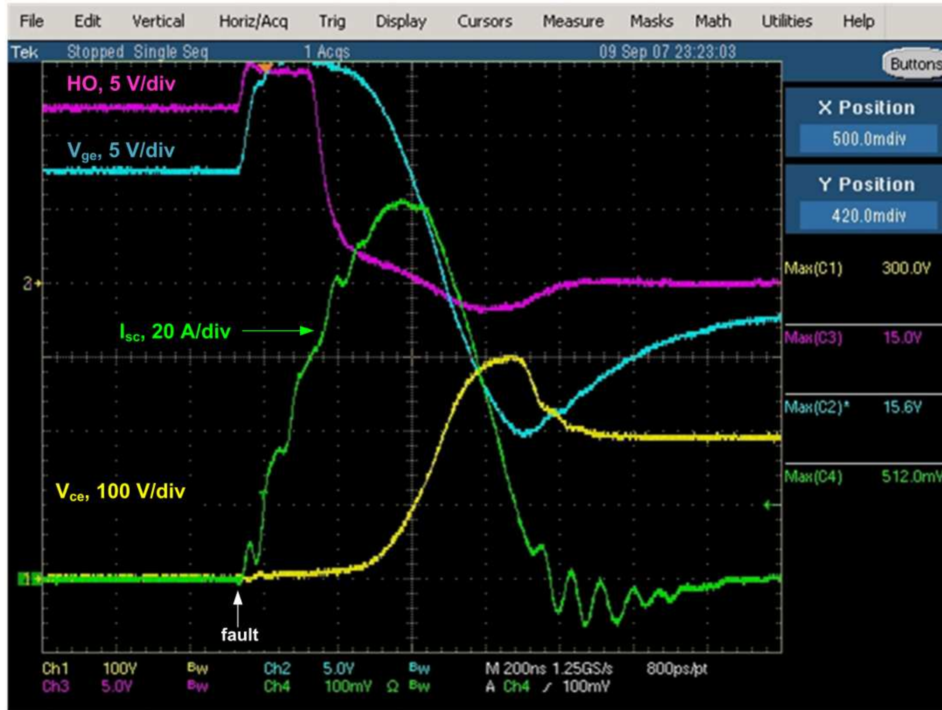


Figure 5-2: Shoot-through fault experimental waveforms. V_{ce} 100 V/div (yellow), V_{ge} 5 V/div (blue), HO 5 V/div (magenta), I_{sc} 20 A/div (green), time scale 200 ns/div

When the dc link terminals become shorted the current I_{sc} increases vigorously and the voltage V_{ce} across S_2 also increases. As V_{ce} exceeds the preset limit the desaturation detection circuit of IR2127 triggers reducing HO to zero. Correspondingly, V_{ge} drops to zero and the IGBT no longer conducts. The current I_{sc} drops as it is being diverted to the R_{cd} path and a slower discharge of the dc link capacitors begins. A snapshot of the discharging waveforms is shown in Figure 5-3 for one dc link capacitor, R_{cd} and V_{ce}. Note that the reaction time of relay S_1 is several times longer than the IGBT's. This delay causes the IGBT to see the entire dc link voltage for a finite time t_{relay} after HO has decreased to 0 V. In addition, the due to the rapid decrease of I_{sc} and the parasitic inductance of the short-circuit loop causes a 100 V spike on the dc link voltage (see

Figure 5-2) when the current is interrupted; stressing the importance of sizing the IGBT and anti-parallel diode D accordingly.

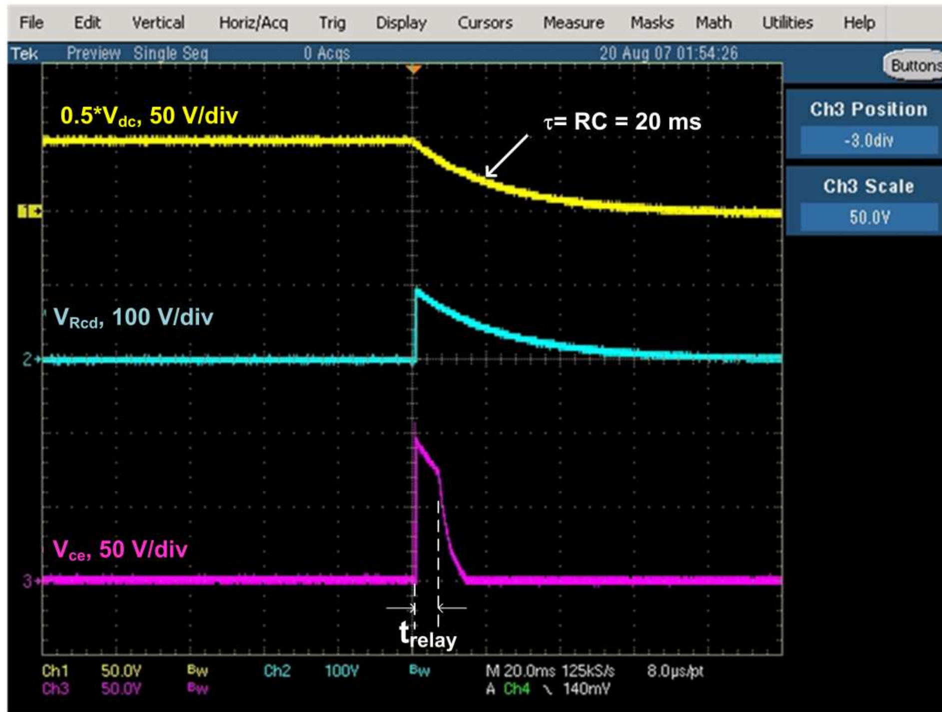


Figure 5-3: Discharging waveforms following the shoot-through fault. Waveforms: 0.5*Vdc, 50 V/div (yellow); V_{Rcd}, 100 V/div (blue); V_{ce}, 50 V/div (magenta). Time scale 20 ms/div

At approximately 100 ms (or 5τ), the capacitors are fully discharged. Note that R_{cd} follows the discharging waveform of the dc link capacitors while the IGBT voltage reduces to zero after S_1 has fully opened. One additional observation is the 100 V overshoot on the dc link voltage (see Figure 5-2) that results from $L\frac{di}{dt}$ in the short-circuit path when the protection triggers. The IGBT and diode must be sized accordingly to withstand this voltage transient.

The experimental results demonstrate that the fault was detected successfully and the dc link protection extinguished the fault current in less than 1 μs. Nevertheless a closer look at Figure 5-2 reveals that by the time the dc link protection begins to clear the fault,

the short-circuit current has reached 104 A! This is 3 times greater than the desired current limit and poses the risk of exceeding the pulse current rating of the inverter switching devices. Analysis of the V_{ge} waveform in Figure 5-2 reveals that when the fault current increases V_{ge} also increases reaching 15.6 V. As V_{ge} increases the output transfer characteristic of the IGBT changes and more current is required to pull the IGBT into desaturation. The preset trip limit is lost during the transient due to the IGBT Miller capacitance.

5.3 Miller Capacitance Effect

The sudden increase in V_{ge} is caused by the rapid voltage increase at the IGBT collector terminal in response to the fast increasing fault current. A zoomed in snapshot of the V_{ce} waveform is shown in Figure 5-4.

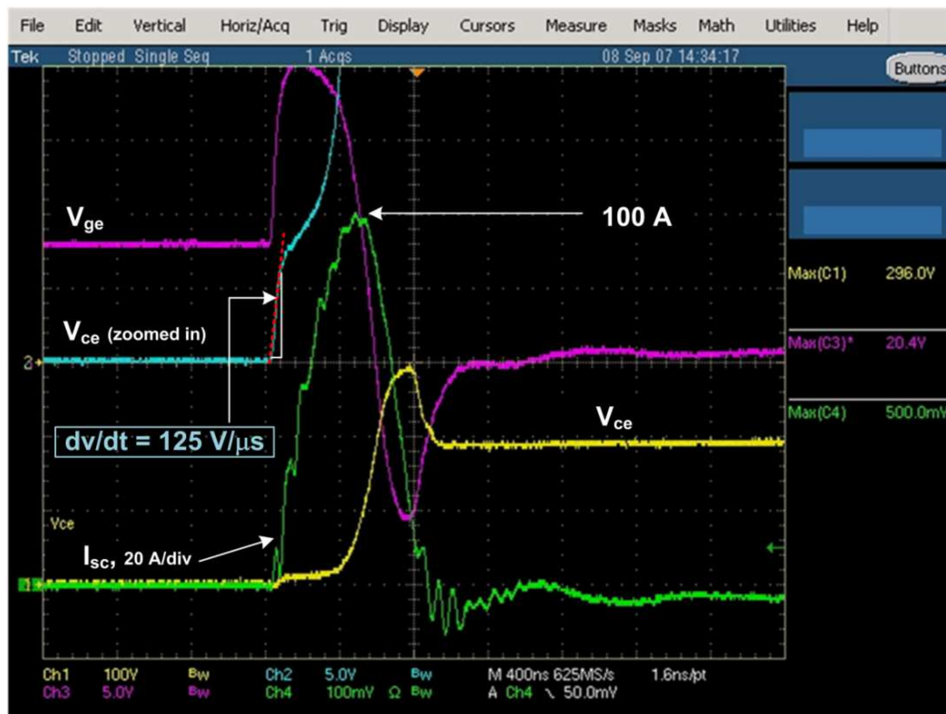


Figure 5-4: Test waveforms showing rate of change of V_{ce}. V_{ce} 100 V/div (yellow), $V_{ce,zoomed}$ 5 V/div (blue), V_{ge} 5 V/div (magenta), I_{sc} 20 A/div (green), time scale 400 ns/div

Note that the initial increase in fault current produces a steep increase in V_{ce} at a rate of 125 V/μs. The high dv/dt induces a current i_{gc} that couples into the gate drive circuit through the IGBT's parasitic capacitance C_{gc} –also known as Miller capacitance. The circuit in Figure 5-5 describes the impact of the Miller capacitance on the gate drive circuit.

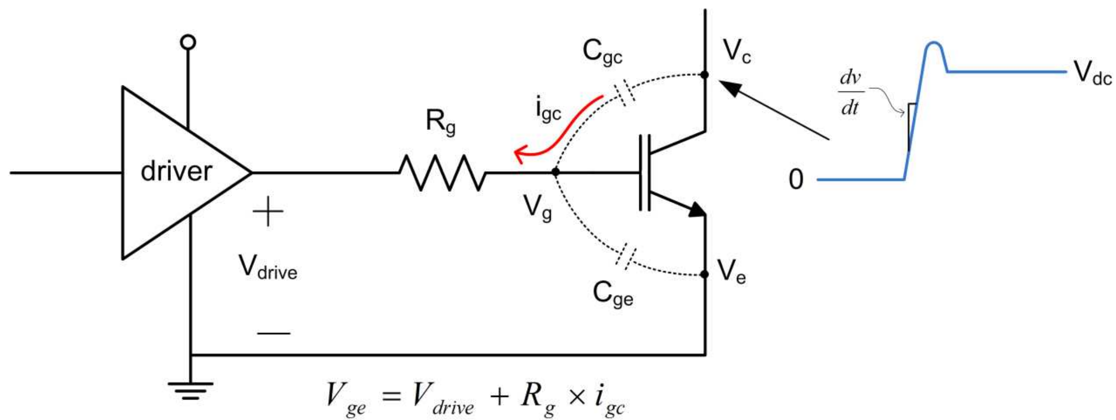


Figure 5-5: Miller effect in gate drive circuit

The induced current i_{gc} is the product of the dv/dt at the collector terminal and the Miller capacitance as expressed in (5.1).

$$i_{gc} = C_{gc} \frac{dV_{ce}}{dt} \tag{5.1}$$

This current couples with the gate drive circuit generating a voltage across R_g. Applying KVL around the gate drive loop yields:

$$V_{ge} = V_{drive} + R_g \times i_{gc} \tag{5.2}$$

It is evident from (5.2) that the gate voltage is augmented by the term $R_g \times i_{gc}$, which inevitably causes the IGBT to operate above the intended 8 V supplied by V_{drive}. This undesired phenomenon is referred to as *induced turn-on* or *dv/dt turn-on* and it has been reported in [37] for an IGBTs under load fault (see Figure 5-6).

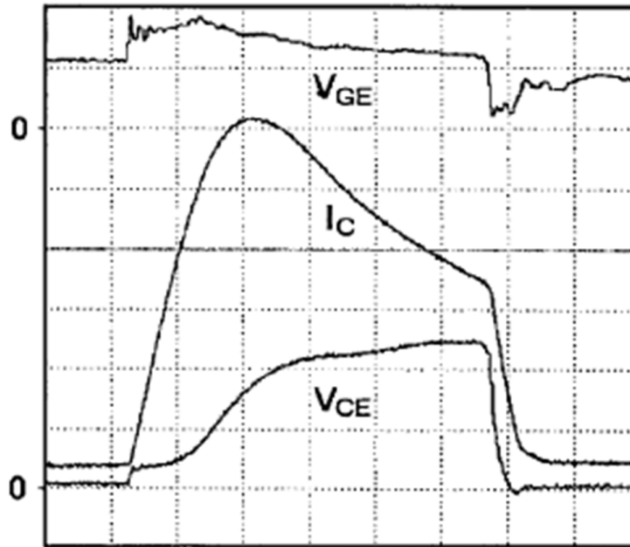


Figure 5-6: IGBT waveforms demonstrating the Miller capacitance effect as published in [37] for a fault under load test

5.4 Modified DC Link Protection Circuit

The information gained from the experimental results in sections 5.2 and 5.3 motivated the modification of the test circuit as shown in Figure 5-7. A zener diode D_z was connected between the gate and emitter of the IGBT and a turn-off diode D_{off} was added to the IGBT gate. D_z absorbs the transient spike in V_{ge} by clamping the gate-emitter voltage to 8.2 V, therefore obligating the IGBT to operate according to the desired output transfer characteristic curve. The reasoning behind D_{off} is to bypass the external gate resistance R_g during turn-off allowing the gate driver chip to sink the current from the IGBT gate in a shorter time; propitiating a faster turn-off. The shoot-through test was repeated on the modified circuit and the results are presented in Figure 5-8.

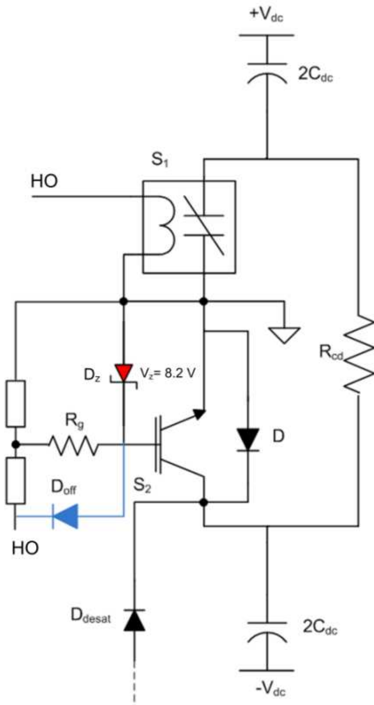


Figure 5-7: Modified dc link protection circuit for improved turn-off performance

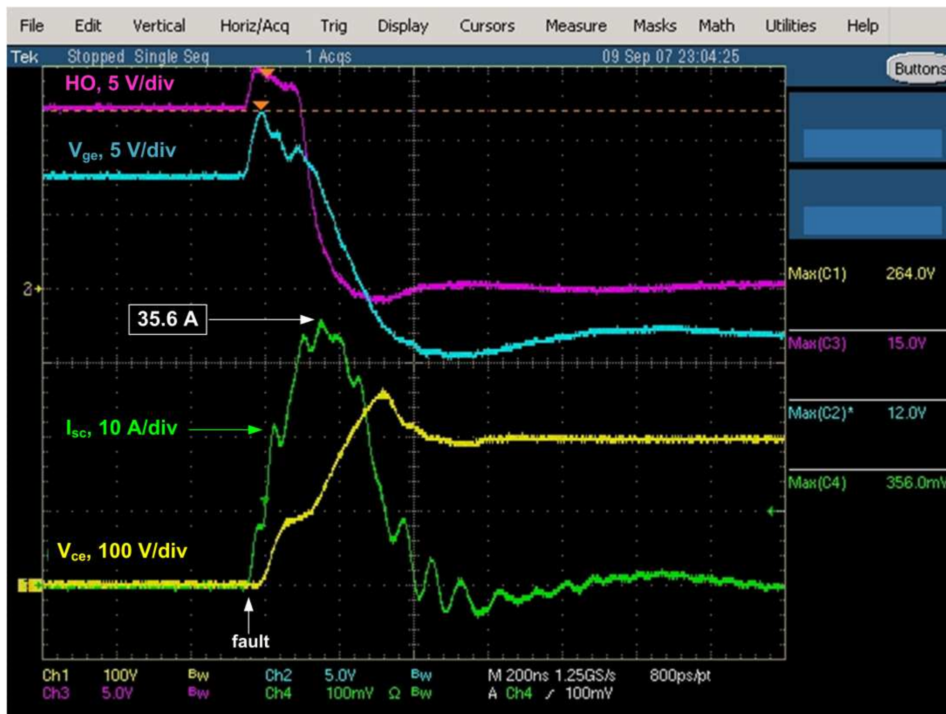


Figure 5-8: Shoot-through fault experimental waveforms using modified circuit for improved turn-off performance. V_{ce} 100 V/div (yellow), V_{ge} 5 V/div (blue), HO 5 V/div (magenta), I_{sc} 20 A/div (green), time scale 200 ns/div

A significant improvement in the peak shoot-through current is obtained with the modified circuit. The dc link protection effectively limits the peak fault current to 35.6 A – close to the desired trip level of 35 A. The clamping action of D_z absorbs much of the voltage transient of V_{ge}, thus keeping the IGBT closer to the desired output transfer characteristic curve. Note that the reaction time of the zener diode plays an important role in the protection circuit. It can be observed that although D_z reacts to the transient in tens of nanoseconds, V_{ge} reaches 12 V before clamping to its avalanche voltage. The turn-off diode D_{off}, on the other hand, reduces the duration of the current surge by aiding the IGBT turn-off.

5.5 Effect of D_z and D_{off}

The plot in Figure 5-9 shows how D_z and D_{off} affect the magnitude and duration of I_{sc} under the same test conditions.

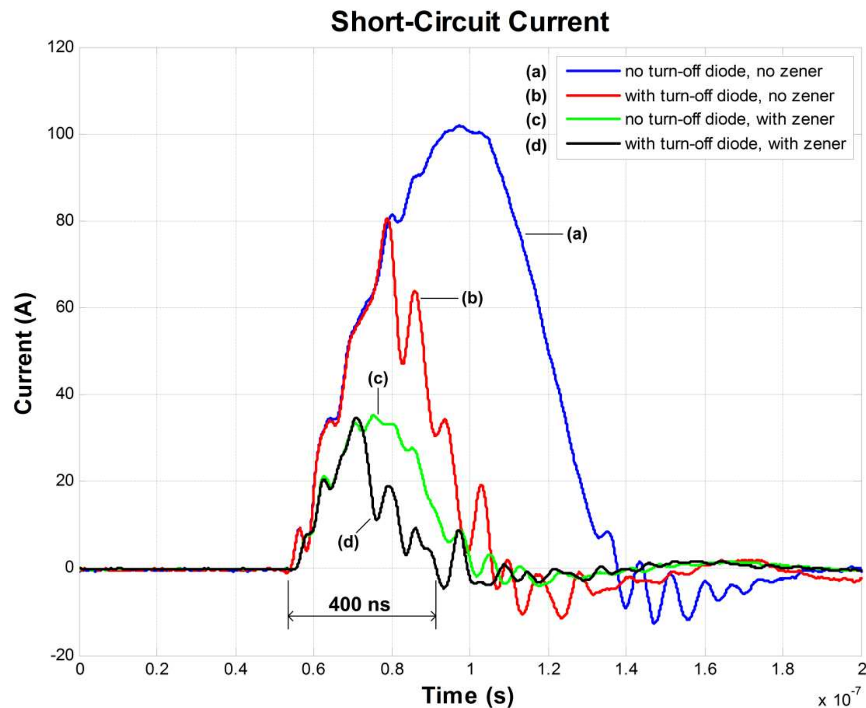


Figure 5-9: Effect of turn-off diode D_{off} and zener diode D_z on short-circuit current I_{sc}

It is evident that D_{off} alone (Figure 5-9, plot b) improves the IGBT turn-off time, thus reducing the pulse duration of the short-circuit current. In fact I_{sc} crosses zero 320 ns earlier than the case where no diode or zener are used (Figure 5-9, plot a). The peak current is also reduced from 104 A to 80 A as a result of the faster turn-off. Plot (c) in Figure 5-9 shows the effect of D_z alone. The zener diode clamps the gate voltage during the fault transient such that the peak current barely reaches 36 A. Clamping the gate, allows I_{sc} reach zero faster and also shortens the current pulse duration. Combining the benefits of both D_{off} and D_z clearly improves the performance of the dc link protection circuit by limiting the peak current to 35.6 A and extinguishing the fault in 400 ns (Figure 5-9, plot d).

5.6 DC Link Protection Summary

The results in this section provided successful validation of the proposed dc link protection circuit. Owing to its location in the dc link midpoint the protection circuit is entirely independent of the inverter power stage switches. Therefore the results in this section can be easily extrapolated to any type of switching device composing the phase-leg of a voltage fed inverter, thus making the proposed protection circuit universal. The discussion and experimental results presented in this chapter establishes a starting point for the development of the proposed protection system. Conscious of the numerous details entailing the proposed protection circuit, the author recognizes the need for additional investigation of the proposed protection circuit and with the results presented in this chapter wishes to awaken the interest for further development of this approach.

Chapter 6 Conclusions and Future Work

6.1 Summary

The voltage source inverter is certainly the most popular topology used in dc to ac power conversion including motor drive application. The technology trend for smaller and more efficient drives is setting unprecedented power density requirements on airborne applications. In reply to this need higher switching frequencies are being sought and new switching devices like SiC JFETs have emerged. In an effort to study the new challenges introduced by this trend a 2 kW IGBT-based three-phase VSI was designed, built, and tested as part of this work. In addition a novel shoot-through protection was proposed to address the concern of using normally-on devices (like SiC JFETs) in voltage source inverters.

6.2 Voltage Source Inverter Accomplishments

The key goals of the 2 kW VSI design were to: 1) provide guidelines for the design of similar high power density circuits, 2) assess the electrical and thermal performance of the inverter at high switching frequency, 3) verify the limitations associated to high switching frequency operation, and 4) identify major contributors to the overall power stage weight. A complete approach to the design of a 2 kW inverter was compiled in Ch. 2 for the benefit of the interested designer. In Ch. 3 the performance of the inverter was evaluated at full load operation and various switching frequencies up to 65 kHz. Measurements revealed that the inverter is 96.4% efficient and that the key contributor to the overall losses is the IGBT conduction losses.

One key challenge in the design of high switching frequency converters implementing digital control is the processing speed of the DSP. This was experimented first hand when trying to prove the design at 70 kHz unsuccessfully. It was verified that 70 kHz exerted sufficient computational burden on the given DSP as to not allow the inverter to operate correctly making 65 kHz the maximum achievable switching frequency. It was confirmed that the control period (time required by the DSP to process and update data before the next switching cycle) was longer than the inverter switching period resulting in inadequate performance of the power stage. This mishap however did not prevent from evaluating the quality of the inverter load current across a range of switching frequencies. Noticeably as the switching frequency increased from 10 kHz to 65 kHz the current ripple became less and the THD of the current improved. Beyond 40 kHz, however, the benefits of high switching frequency to enhance the current THD are only marginal.

Although power losses were not measured as a function of switching frequency, the junction temperature (indirect indication of losses) of the devices was recorded at various switching frequencies. The results revealed that using the cooling system (heat sink and fan) designed in Ch. 3 the junction temperature of the IGBTs increases from 56°C to 63°C when the switching frequency varies from 10 to 65 kHz, thus keeping the devices cool and below their maximum junction temperature.

Finally, the inverter power stage power density was estimated at 4 kW/kg. The weight breakdown study in section 3.5.1 revealed that the top weight contributor is the cooling system followed by the bare PCB and other miscellaneous mechanical components. In third place come the components associated to auxiliary power

conversion like gate drive power supplies. This last area offers great opportunity for size and weight reduction. In order to increase the power density of the power stage, alternate methods for powering the gate drive power supplies could be sought. For example, instead of six independent dc/dc converters a single flyback converter with multiple outputs could be used for powering the gate drive circuits, thus saving weight and real estate.

In summary, the design of a high power density and high switching frequency voltage source inverter was shown and validated with experimental results. The challenges associated to this design have been enumerated and a step-by-step design approach has been documented in Ch 2.

6.3 Dc Link Overcurrent Protection Accomplishments

In response to the concern of using normally-on SiC JFETs in voltage source inverters, a novel dc link overcurrent protection circuit was proposed in Ch.4 and validated in Ch. 5. The circuit resides in the inverter dc link midpoint and contrary to plain desaturation detection circuits the proposed protection circuit is independent of the type of power stage switches. The dc link protection circuit monitors the midpoint current via desaturation detection of a strategically placed IGBT. When excessive current is detected during a shoot-through fault the protection circuit reacts by disrupting the dc link midpoint and diverting the fault current to a high impedance path. The implementation of this circuit is relatively simple and comprises inexpensive components: IGBT, small relay, diode, IGBT driver with desaturation function, and a resistor. A guideline for the selection of these components was provided in Ch. 4.

The dc link protection concept was verified successfully in Ch. 5 by shorting a pre-charged dc link. The test allowed assessing the performance of the circuit in terms of reaction time and current limiting. During the initial tests of this protection scheme the circuit effectiveness was threatened by the IGBT Miller capacitance. It was seen that due to the high dv/dt experienced at the collector node during the short-circuit fault, current was coupling to the gate drive loop through the Miller capacitance of the IGBT effectively increasing the gate drive voltage. This in turn caused the IGBT to operate outside the intended output transfer curve; completely defeating the purpose of the strategically selected operating curve. The problem was resolved by adding a clamping diode across the IGBT gate-emitter terminals. In addition the reaction time was sped up with a turn-off diode in the drive circuit. With the small modifications in place the protection circuit was capable of extinguishing the fault in 400 ns and limiting the short-circuit current to 35.6 A. Experimental waveforms supported the successful validation of the dc link protection concept.

6.4 Future Work

The author understands that additional investigation of some topics could further enrich this thesis work and expand our knowledge of the challenges associated to the design of high power density inverters. The following list enumerates some of these topics:

1. Achieving higher switching frequency (>70 kHz)

Due to the processing limitations of the controller the maximum switching frequency achieved on the inverter power stage was 65 kHz. Operation of the inverter at higher

frequencies would be of interest to fully verify the design specifications of the inverter and assess its impact on power density.

2. Use of alternate power supplies for VSI gate drives

It was shown that auxiliary power accounts for 8.2% of the total inverter weight. This area presents an opportunity for exploring other methods of supplying power to the inverter gate drive circuits. An in-house flyback converter with multiple outputs could be considered to save weight and volume.

3. Silicon vs SiC diode in relation to weight

There is a need for quantifying the benefits of using SiC diodes versus silicon diodes in terms of weight saving. The inverter design presented in this work made use of Infineon SiC schottky barrier diodes. Assessing their performance over the traditional fast switching silicon diode is topic for a future study.

4. Impact of dc source on dc link protection circuit

Throughout the development of the dc link protection circuit it was assumed that the dc source is effectively removed from the circuit. This allowed treating the short-circuit loop as a second order underdamped RLC circuit. In reality, the inverter is fed from a rectifying unit and assessment of its impact on the dc link protection circuit is yet to be studied.

5. Soft turn-off circuit for dc link protection

It was seen that the Miller capacitance of the IGBT in the dc link protection circuit plays an important role because it couples the power circuit to the gate drive loop. The

impact of the Miller capacitance was mitigated with a clamping diode that limited the excursion of the gate drive voltage; nevertheless the problem has not been eradicated completely. Miller capacitance coupling can be minimized by reducing the dv/dt at the collector node due to the abrupt interruption of the fault current. A soft turn-off circuit could be added to the existing protection circuit to limit the amount of current coupling into the gate drive loop, therefore minimizing the impact on the drive voltage and on the IGBT desaturation limit.

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APPENDIX

A.1 Lessons Learned

During the early stages of testing the author came across several hardware issues that prevented correct operation of the VSI. The intent of this brief section is to share with the reader some of the lessons learned during the hardware validation phase with particular emphasis on the gate drive circuit.

Lesson Learned 1: Keep inverter-controller interface short

Although this is a rule of thumb, how short is *short*? The answer seems to be: as short as physically possible. Figure A-1 shows the PWM signal cable that connects the controller with the inverter power stage. This cable carries the switching pulses from the FPGA to the inverter power stage. Its length is crucial to the correct behavior of the inverter.

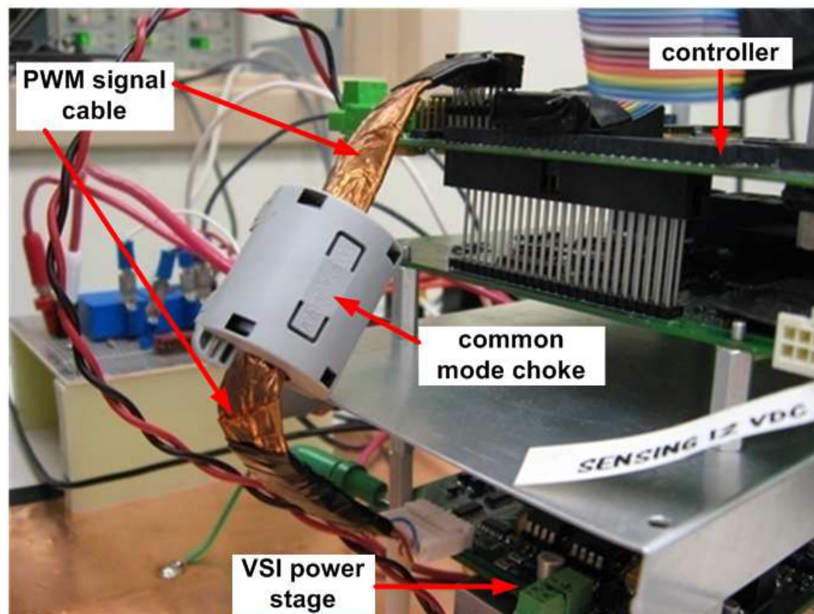

Figure A-1: Inverter – controller interface

Due to the stacked configuration of the system this cable extends from the top board (controller) to the bottom board (inverter power stage). Initially an unshielded ribbon cable (more than 6 in long) was used and the inverter would operate inconsistently. Three steps were taken to minimize EMI pollution on this cable:

1. Shortened the cable to just the necessary length
2. Wrapped copper foil around the cable to serve as shield
3. Added an external common mode choke to filter common mode noise

An immediate improvement was observed in the gate drive signals and on the operation of the inverter.

Lesson Learned 2: Beware of small footprint common-mode chokes

Common-mode chokes were used in the gate drive circuit to filter noise as shown in Fig. A-2. Note that the CM choke filters unwanted noise from the 28 V line and also filters the output of the gate drive power supply.

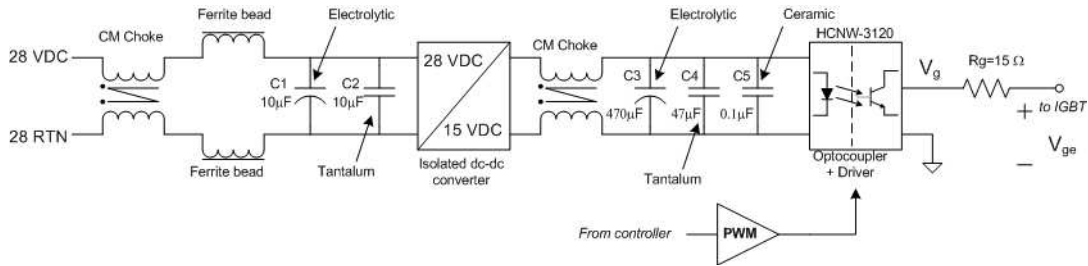

Figure A-2: Common-mode chokes in the gate drive circuit

Their location in the power path introduces a level of unreliability especially when a cold solder joint is experienced in one of its terminals. The CM choke used in the inverter power stage was selected primarily for its compactness. Its footprint (shown in Fig. A-3) is very small and delicate. As such the gate drive CM choke was the source of many

hardware issues caused by bad contact or cold solder joints. Appropriate land pads are to be provided to guarantee good power flow to the gate drive circuit.

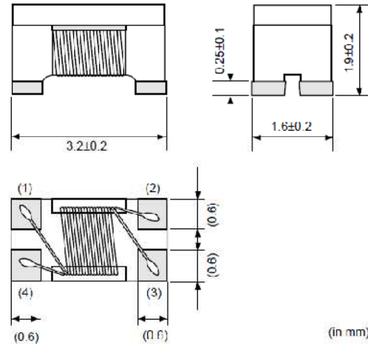

Figure A-3: Dimensions of CM choke used in gate drive circuit

A.2 VSI Bill of Materials

Ref. Designator	Description	Qty	Manufacturer	Manufacturer P/N
C1, C2, C3, C4	Ceramic Chip Capacitor 1kV	4	Murata Electronics	GRM55DR73A104KW01L
C5, C9, C13, C18, C24, C29, C33, C38, C43	Tantalum cap	9	Kemet	T491X476K035AT
C6, C11, C14, C22, C27, C31, C36, C41	10 uF cap	8	United Chemi-Con	EMVA350ADA100MD55G
C7, C8, C10, C12, C15, C17, C20, C23, C26, C28, C32, C34, C37, C39, C42, C44, C45, C46, C47	Ceramic Chip Capacitor - Standard 0.1uF	19	Yageo Corporation	CC0805KRX7R9BB104
C16, C21, C25, C30, C35, C40	Electrolytic cap 470 uF	6	United Chemi-Con	EMVA350ARA471MKE0S
C19	Electrolytic cap 100 uF	1	United Chemi-Con	EMVA350ADA101MF80G
D1, D2, D3, D4, D5, D6	SiC Shottky diode	6	Infineon	SAMPLE
J1	2 position header	1	Phoenix Contact	1913646
J2	Phoenix 7.62mm Header, 3 pins	1	Phoenix Contact	1714984

J3	3 position header	1	Molex	22-05-3031
J4	10 position, double row, power header	1	Samtec	IPL1-105-01-S-D-RA
J5	Header, 8-Pin	1	Molex	22-05-3081
J6	Header, 2-Pin	1	Phoenix Contact	1844210
L1, L4, L5, L8, L9, L12, L13, L16, L17, L20, L21, L24, L25, L28, L29, L32	smd ferrite bead	16	TDK	NLC453232T-560K-PF
L2, L3, L6, L7, L10, L11, L14, L15, L18, L19, L22, L23, L26, L27, L30, L31	surface mount common mode choke	16	Murata Electronics	DLW31SN222SQ2L
PS1	TDK CC6xxxxDF-E power supply 6W	1	TDK	CC6-2412DF-E
PS2, PS3	Single output 5V power supply 1.5W, 24V input	2	TDK	CC1R5-2405SF-E
PS4, PS5, PS6, PS7, PS8, PS9	Dual output +/-15V power supply 2W, 24V input	6	Traco Power	TMR 2423
Q1, Q2, Q3, Q4, Q5, Q6	Insulated Gate Bipolar Transistor	6	International Rectifier	IRG4BC30WPBF
R1, R3, R5, R7, R9, R11	Resistor	6	Panasonic	ERJ-P14J271U
R2, R4, R6, R8, R10, R12	Metal Film Resistor, 2 Ohm to 1M Ohm Range, 0.5% and 1% Tolerance, 0.25 W	6	Yageo Corporation	RC1206FR-0715RL
R13, R14, R15, R16, R17, R18	Thick Film Chip Resistor, 1 Ohm to 1M Ohm Range, 5% Tolerance, 2512 Size, 1 W	6	Panasonic	ERJ-1TYJ331U
S1, S2	Current sensor	2	LEM	LTS 15-NP
U1, U2, U6, U8, U9, U10	2.5A Optocoupler driver (wide package)	6	Agilent	HCNW-3120
U1, U2, U6, U8, U9, U10	Gull wing DIP sockets 8-pins	6	Mill-Max	110-93-308-41-105000
U3	HEx inverter	1	Fairchild Semiconductor	74AC14SC
U4, U5	Quadruple 2-Input Positive-AND Gate with Open-Collector Outputs	2	Texas Instruments	SN74LS09D

A.3 Weight Contribution by Component

Component	Qty	Weight in g	Component Total Weight in g	% of total
heat sink	1	198.45	198.45	50.7898
fan Sanyo Denki	1	55	55	14.0763
Traco power supply	6	4.8	28.8	7.3709
current sensor	2	10	20	5.1187
J2 AC Output	1	9.53	9.53	2.4390
J1 DC input	1	8.75	8.75	2.2394
igbt	6	1.44	8.64	2.2113
SiC SBD	6	1.44	8.64	2.2113
5V power supply	2	3.2	6.4	1.6380
12V power supply	1	5.8	5.8	1.4844
Tantalum Cap	9	0.5	4.5	1.1517
Ferrite Bead	16	0.18	2.88	0.7371
J6 28 V input	1	0.757	0.757	0.1937
unpopulated PCB	1	N/A	N/A	N/A
Ceramic Cap 1kV	4	0.32	1.28	0.3276
Electrolytic Cap 10uF	8	0.15	1.2	0.3071
Ceramic Cap 0.1uF	19	0.019	0.361	0.0924
Electrolytic Cap 470 uF	6	2.9	17.4	4.4532
Electrolytic Cap 100 uF	1	0.53	0.53	0.1356
J3	1	0.391	0.391	0.1001
J4	1	0.91294	0.91294	0.2337
J5	1	1.062	1.062	0.2718
CM Choke	16	0.038	0.608	0.1556
Min Load Resistor	6	0.016	0.096	0.0246
Gate Resistor	6	0.016	0.096	0.0246
Pull-up resistor	6	0.016	0.096	0.0246
Optocoupler	6	0.85	5.1	1.3053
Gull Wing Socket	6	0.51	3.06	0.7832
Hex inverter	1	0.129	0.129	0.0330
AND gate	2	0.129417	0.258834	0.0662
plastic screws	6	N/A	N/A	N/A
gap pad	12	N/A	N/A	N/A
solder alloy	-	N/A	N/A	N/A

A.4 VSI Power Stage Schematic

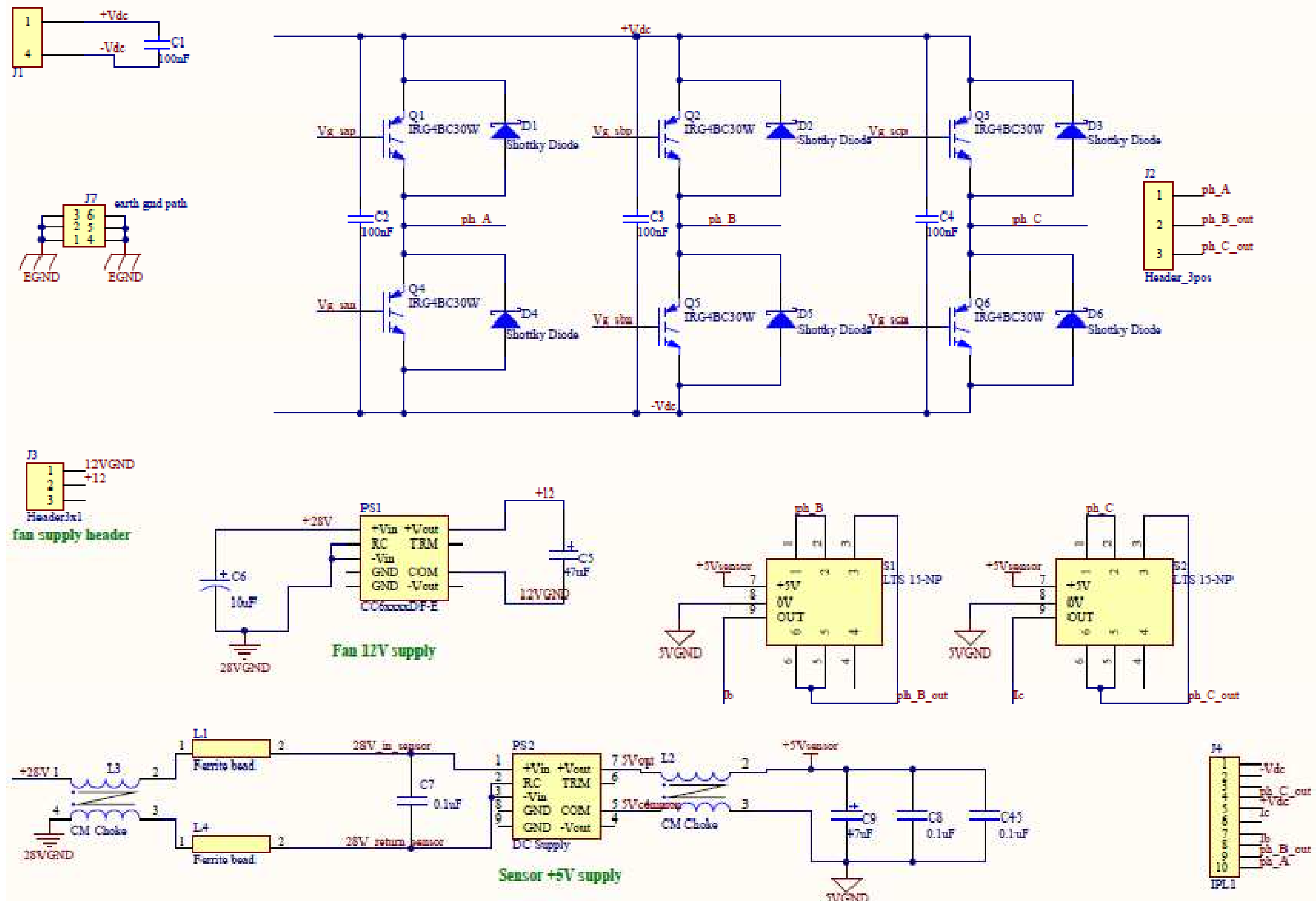

Figure A-4: VSI power stage

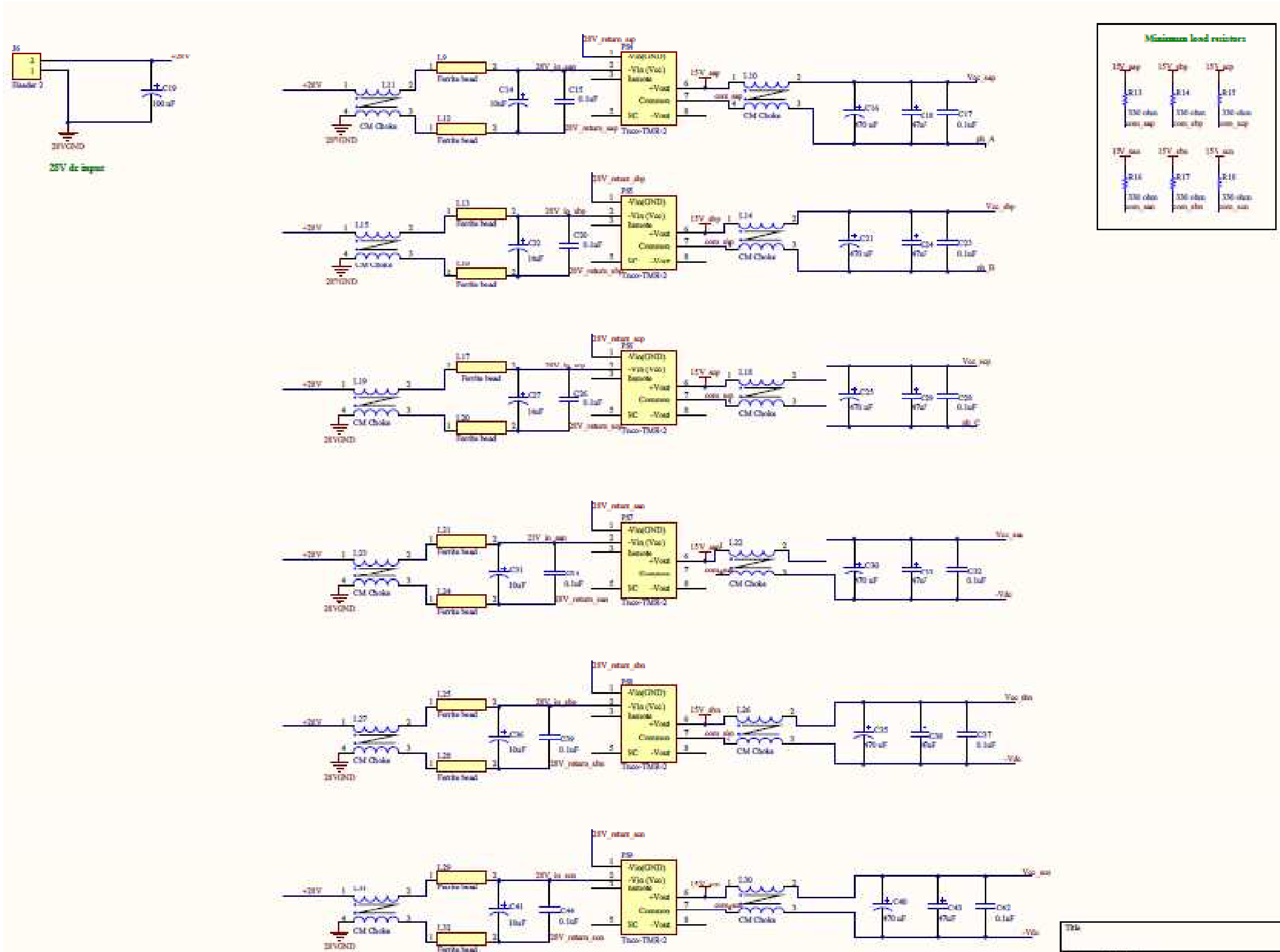

Figure A-5: Gate drive power supply circuitry

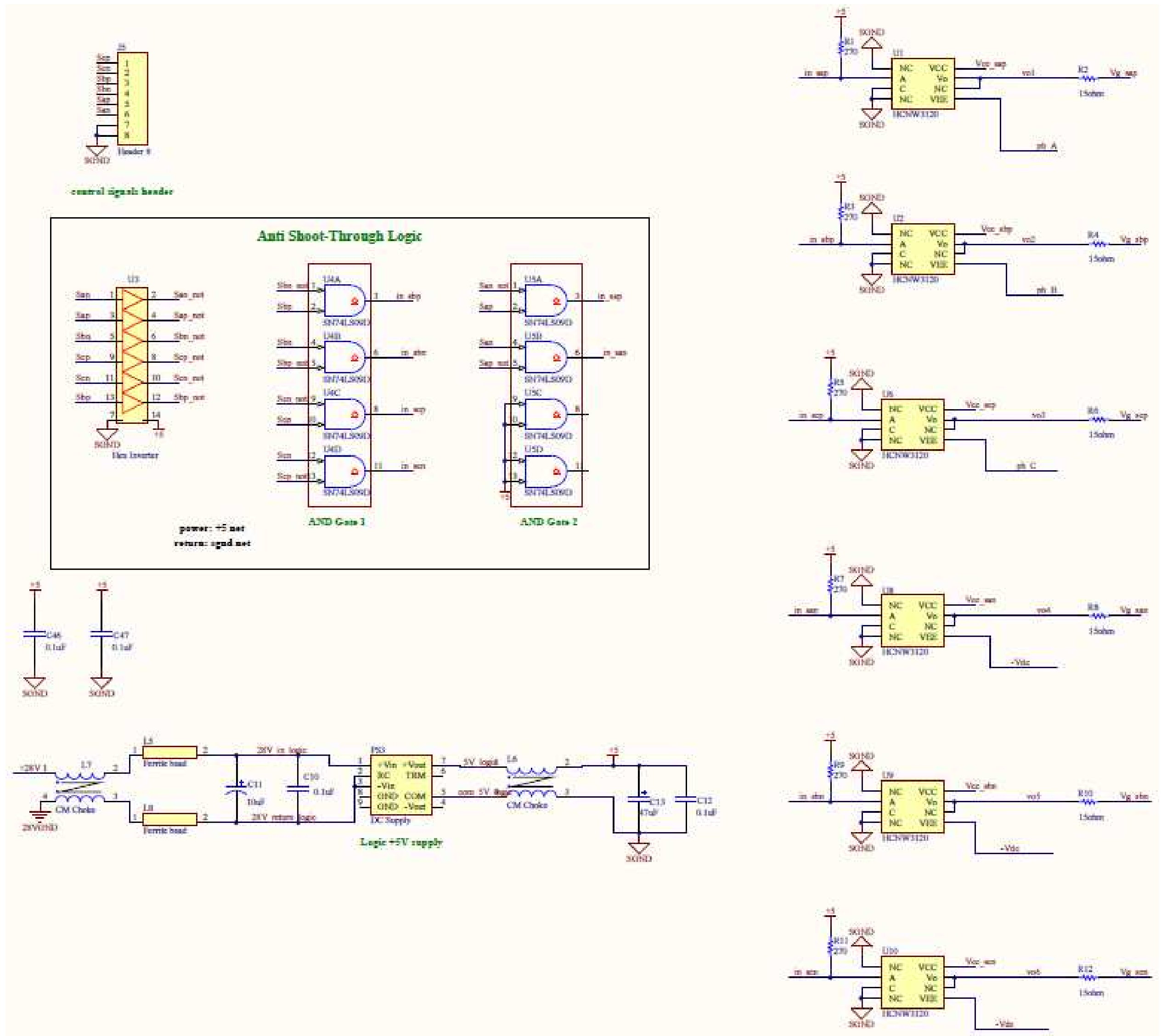

Figure A-6: Anti-shoot-through and gate drive circuit