ANALYSIS OF THE POWER CONDITIONING SYSTEM FOR A SUPERCONDUCTING MAGNETIC ENERGY STORAGE UNIT

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Thesis submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

in

Electrical and Computer Engineering

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August 2000

Blacksburg, Virginia

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ABSTRACT

Superconducting Magnetic Energy Storage (SMES) has branched out from its application origins of load leveling, in the early 1970s, to include power quality for utility, industrial, commercial and military applications. It has also shown promise as a power supply for pulsed loads such as electric guns and electromagnetic aircraft launchers (EMAL) as well as for vital loads when power distribution systems are temporarily down. These new applications demand more efficient and compact high performance power electronics.

A 250 kW Power Conditioning System (PCS), consisting of a voltage source converter (VSC) and bi-directional two-quadrant DC/DC converter (chopper), was developed at the Center for Power Electronics Systems (CPES) under an ONR funded program. The project was to develop advanced power electronic techniques for SMES Naval applications. This thesis focuses on system analysis and development of a demonstration test plan to illustrate the SMES systems' ability to be multitasked for

implementation on naval ships. The demonstration focuses on three applications; power quality, pulsed power and vital loads.

An integrated system controller, based on an Altera programmable logic device, was developed to coordinate charge/discharge transitions. The system controller integrated the chopper and VSC controller, configured applicable loads, and dictated sequencing of events during mode transitions.

Initial tests with a SMES coil resulted in problems during mode transitions. These problems caused uncontrollable transients and caused protection to trigger and processors to shut down. Accurate models of both the Chopper and VSC were developed and an analysis of these mode transition transients was conducted. Solutions were proposed, simulated and implemented in hardware. Successful operation of the system was achieved and verified with both a low temperature superconductor here at CPES and a high temperature superconductor at The Naval Research Lab.

ACKNOWLEDGEMENTS

I am grateful to my advisor Dr. Dušan Borojević for his guidance through out my work here at CPES. He truly has a gift for teaching others and unselfishly gives of himself in sharing his knowledge and experiences.

I also wish to thank Dr. Fred Lee. His contributions to the power electronics community are truly astounding. He has surrounded himself with leading power electronics faculty, Dr. Alex Huang, Dr. Jason Lai, Dr. Dan Chen, and the brightest students. Consequently he has built an unparalleled program here at Virginia Tech.

I would like to thank Dr. Sriram Chandrasekaran for his endless bounty of knowledge and dedication to helping myself and others in the lab. He has spent countless hours teaching me about electronics, culture and friendship. I would also like to thank Kevin Motto and Yuxin Lee for their technical support, hours of philosophical distractions and friendship, and to all of the other members of CPES who have been great friends over the years.

I would like to express love and admiration to my parents who always offer an encouraging word. They have been untarnished role models in every aspect of my life, and to Jaime for her support, patients, kindness, inspiration and love.

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1 INTRODUCTION

The concept of Superconducting Magnetic Energy Storage (SMES) was developed in the early 1970's. Its concept was simple; circulate a DC current in a superconducting coil and store energy in its magnetic field with essentially zero losses. However, implementing this concept efficiently and economically has proven to be quite challenging. Development of several key technologies has severely limited the wide spread use and acceptance of SMES. They include the superconducting materials and manufacturing techniques, the cryogenic refrigeration systems and the power electronics.

High temperature superconductors (HTS) have turned out to be very brittle ceramic material and thus very difficult to manufacture. Improvements also need to be made in coil winding processes. In addition, the current density of HTS wire is not as high as that of low temperature superconducting (LTS) wire. Development of superconducting materials will have the biggest impact on SMES. It can reduce the demand on the power electronics and significantly reduce the cooling requirements. However, development in this area is the most difficult and requires a large capital investment [1].

Progress has been made recently in the development of reliable and inexpensive cryogenic coolers that make the concern of cooling the unit less substantial. Research in cryogenic refrigeration looks promising and could help propel the use of micro-SMES in industrial and commercial applications for power quality. Currently, several companies are involved in the development of efficient and reliable complete helium liquefier systems that can be used with micro-SMES units.

The power electronics for SMES systems can be complicated, unreliable and

expensive. According to a study completed by Sandia National Laboratories [1], for SMES systems the most significant advances would result from development of power electronics that are specifically suited to SMES devices. This was deemed as "high-priority R&D for SMES". It is also believed that this can be accomplished with moderate costs [1]. It is therefore advantageous to pursue research and development of the power conditioning system (PCS) for SMES. Research on advanced power electronic techniques for SMES was undertaken here at the Center for Power Electronic Systems (CPES) at Virginia Tech. This thesis addresses particular system control issues with the above-mentioned PCS and looks at the system performance.

1.1 SMES: An Overview – Past to Present

The idea of SMES started in the utility industry as a means of load leveling in an era when nuclear power generation was thought to be the future and fossil fuels were to be phased out. It was thought that SMES could be used to store energy in the off peak demand hours and then supply power during peak demand, thus, alleviating the need for expensive fossil fuels to be used to supplement periods of heavy load [2]. The need for load leveling still exists, however. Most power plants work at full capacity to supply power during peak demand and, for economic reasons, continue at full capacity even during periods of light load. In this respect, SMES could be used in place of other energy storage systems, such as, battery systems, pumped-hydro or compressed air.

Capitalizing on the economics of scale, initially most SMES systems envisioned for load leveling had energy storage capabilities of 5000 MWh or more and were approximately 1 km in diameter [2]. It has been found that more near term applications

of SMES lie in the area of power quality [1]-[6]. In 1976 Los Alamos National Laboratory constructed a 30 MJ, 10MW SMES for stability support. It was installed in Bonneville Power Authority Pacific Intertie located in Tacoma Washington. The unit operated for a year. In that time over a million charge/discharge cycles took place and successfully demonstrated its capability to stabilize the 500kV network [3]. To this day it remains the only SMES unit to be fully connected to a utility grid.

Micro-SMES units have found a market niche in industrial and commercial areas. Here they address applications such as transmission line stability, spinning reserve, static VAR compensation and voltage support for critical loads [7]-[9]. In such industries as textiles and automotive, continuous operation of the plant is very important. Momentary power outages or poor power quality can cause temporary shut downs and consequently cost millions of dollars. The EPRI study reported that short-term outages and power quality issues cost US industry approximately $29 billion a year. Micro-SMES is a viable energy storage mechanism to provide continuous support in these critical industries and is already in use in some locations. For example, American Superconductor Corporation has a typical product that can deliver 1 MW for 1 second. The system response time is within 5 ms of a disruption in the line. It currently has 9 units installed worldwide that are contained in transportable semi trailers [1].

The military has also sponsored research and development of SMES systems. In 1987, the Strategic Defense Initiative started the SMES Engineering Test Model program to design and build a 20 MWh coil to be used as a power supply for the Free Electron Laser and also to demonstrate utility applications. Two initial designs were completed and one was to be selected for the actual construction. The two designs were drastically

different from one another and the second phase of the project was never pursued [2]. Since then, no major R&D projects have been undertaken by the military. However, several smaller R&D programs have developed. The SMES program, sponsored by The Office of Naval Research (ONR), was started at CPES in 1995. It was to develop advanced power electronics specifically to demonstrate the effectiveness of SMES in Naval applications.

1.2 SMES Applications

SMES has branched out from its application origins in the early 1970s to include power quality for utility, industrial, commercial and military applications. It has also shown promise as a power supply for pulsed loads such as electric guns and electromagnetic aircraft launchers (EMAL) as well as for vital loads when power distribution systems are temporarily down [3],[7],[10]-[15].

1.2.1 Utility Applications

Several different applications for SMES exist in the utility industry and on basically two different levels. On the substation level, SMES can be used for transmission stability, voltage/VAR support and load leveling. At the generation plant level applications include frequency control, spinning reserve, dynamic response and load leveling [2]. For these applications different system specifications are needed. For example, in the case of voltage support a PCS rating of several hundred megawatts is needed with a discharge time of a few hundred milliseconds. For load leveling at the plant, a PCS rating of hundreds to thousands of megawatts is needed with discharge times

on the order of hours. Figure 1.1 illustrates these different types of applications with their PCS ratings and discharge time [2].

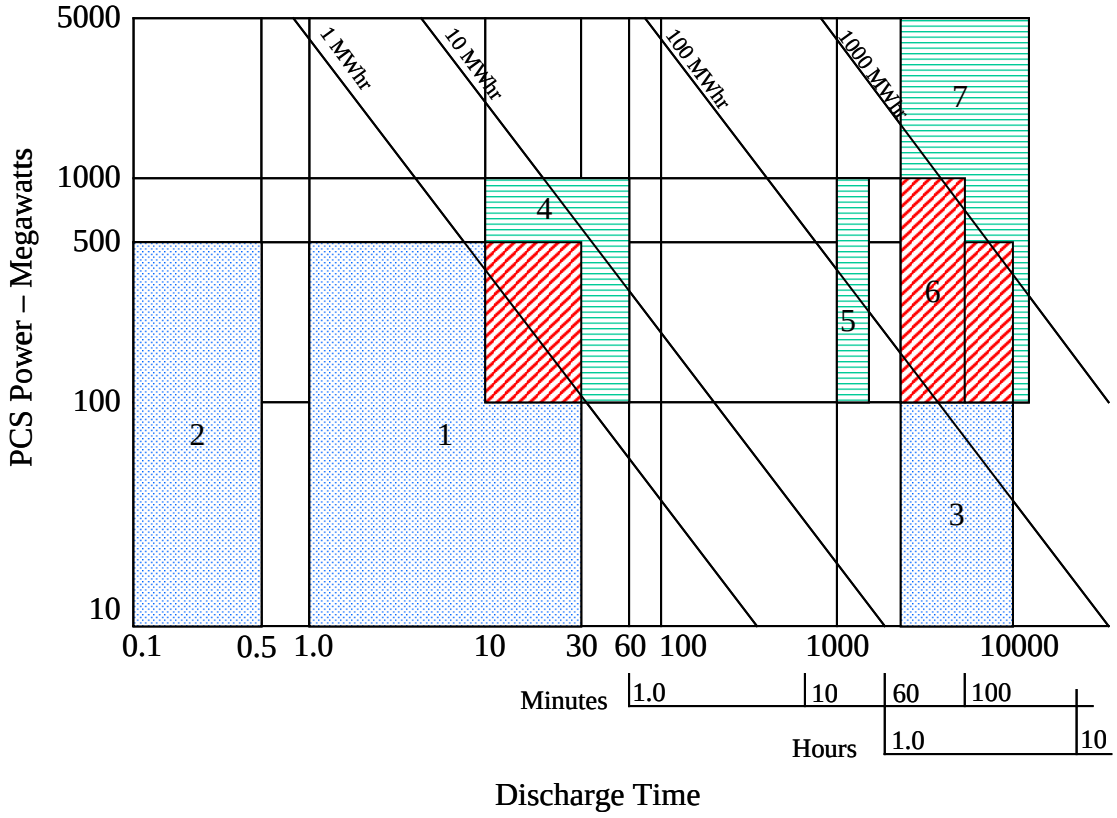


Figure 1.1 SMES utility applications (Transmission Substation Applications: 1. Transmission Stability, 2. Voltage/VAR Support, 3. Load Leveling: Generation System Applications: 4. Frequency Control, 5. Spinning Reserve, 6. Dynamic Response, 7. Load Leveling [2]

1.2.2 Naval/Shipboard Applications

For many years there has been a push for a new all electric aircraft carrier. This all-electric ship would eliminate the nuclear plant, making the aircraft carrier smaller, lighter, quicker and cheaper. Of course the elimination of nuclear power would eliminate the availability of steam and require steam catapults to be replaced by EMAL. Along with EMAL the ship would convert all of its hydraulic and pneumatic actuators to

electrical actuators and replace hydraulic aircraft arresting gear with an electromagnetic arrester capable of recovering energy. It would likely incorporate an advanced electrical defense system and electrically powered weaponry [3]. These new additions as well as the additions of more advanced controls and navigation equipment will require a means of energy storage to smooth transients on the distribution system and maintain clean, reliable power. Development of a SMES that can be multi-tasked to handle all of these requirements can offer efficient and reliable power quality as well as power for the required pulsed loads.

The PCS here at CPES was developed to demonstrate the use of SMES in these naval applications. Three basic operations must be demonstrated successfully in order to show that SMES can meet the unique requirements of the all electric ship. They are power quality, pulsed power and control of vital loads.

1.2.2.1 Power Quality

Power quality is an issue on naval ships as it is an issue with the utility industry. However, there are obvious differences in distribution systems for naval ships that dictate the need for different requirements in the SMES system. The generation system on a naval ship is not as "stiff" as that of the utility power plant. Ships have a system that is on the order of several megawatts while utility plants have systems that are several giggawatts. Hence, a load of a hundred kilowatts can significantly load the distribution system on a naval ship. In addition, many loads on naval ships are pulsed loads. Radar, sonar and electrical actuators all require pulsed power and contribute to the degradation of power quality.

SMES has been slated as a very promising technology for the Integrated Power System (IPS) on naval ships. The availability of SMES in the IPS as an uninterruptible power supply (UPS) could accomplish the following; replace emergency ship service gas turbine generator set, provide auxiliary power to start gas turbines, provide sufficient power to start power generation module (PGM), enable orderly load shed of equipment, provide real power for power quality and provide pulsed power [3]. Energy storage requirements for this application are approximately 600 MJ. The PCS power requirements would be between 0.5 and 4 MW with output voltage requirements of 4160 V AC and 775 V DC, which are the IPS bus voltages. It would also need to produce 450 V AC for starting of the PGM [3]. Power quality must meet specified military standards.

1.2.2.2 Pulsed Power

Another major focus for SMES in the navy is for pulsed power applications. SMES has the ability to charge and discharge very quickly, thus supplying large amounts of pulsed current for short durations. A SMES coil, for all practical purposes, can be cycled through the charge/discharge cycle infinitely many times. In applications such as pulsed power, where charge/discharge cycles occur often, SMES could prove to be more reliable and have a much longer life expectancy then current technology such as batteries or flywheel energy storage. Batteries have a life expectancy of approximately 1000 charging cycles and could produce excessive heat if cycled quickly, where flywheels are subject to mechanical wear and inertial stresses during rapid acceleration and deceleration of the flywheel.

The use of SMES for pulsed power applications is something that is unique to the

military. These applications include EMAL, missile/torpedo launchers, electric guns and remote piloted (RPV) and unmanned aerial vehicles (UAV). EMAL requires the largest amount of stored energy; therefore, system specifications are based on this requirement. The SMES system for EMAL would consist of two 450 MJ coils. This would allow for three launches per coil of an F-18 aircraft, which is assumed to be the largest load. Calculations are based on 95 MJ required to launch the aircraft with 65 % efficiency for the launch motor and 95% efficiency for the PCS, thus a total of 147 MJ per launch [3].

1.2.2.3 Vital Loads

It is sometimes necessary that vital loads on a ship be started at a time when the required power is not available. A vital load would be defined as any load that is essential to the operation of the ship or the survival of the crew. This could include blowers, pumps or any number of systems in a submarine or ship that are needed to successfully operate the vessel. If there is a temporary power outage it could be imperative that these systems start operating or continue operation. The SMES unit could store energy for these vital loads. When numerous systems need to be brought up simultaneously quite often the power system cannot handle the start up transients. The PCS could be used to soft start the motors and eliminate startup transients that could degrade power quality and shut down sensitive equipment. In the case where power is not immediately available the PCS could run loads at a fraction of full power until auxiliary generators are brought on line.

1.3 Obstacles

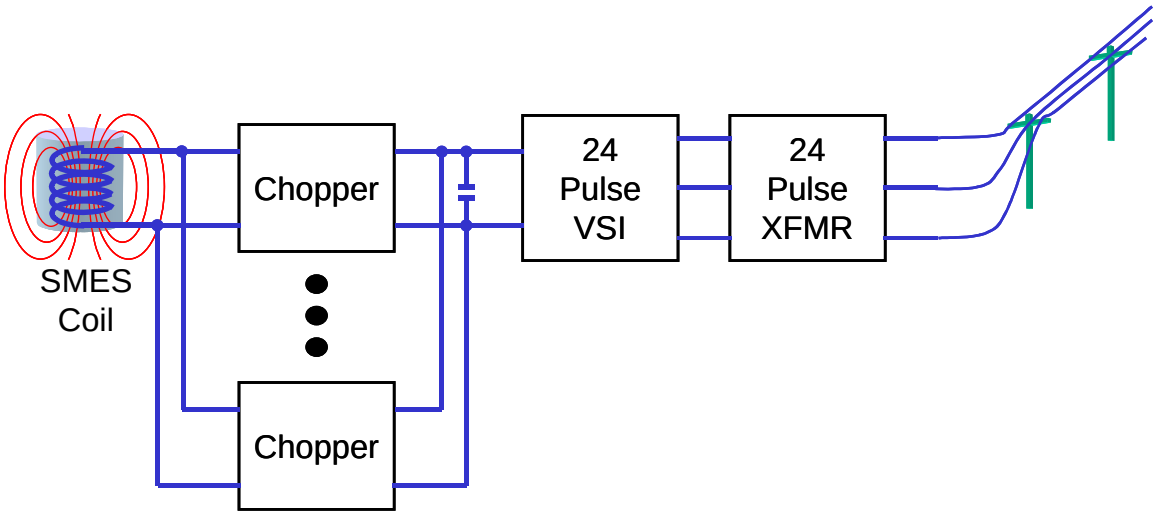
The controls for a SMES PCS have some inherent difficulties, such as the large inductance of the superconducting coil which provides the system with a virtual current source. There are several issues that arise from this system characteristic. One, the current in the inductor is always in the same direction and, under normal operation, never goes to zero. Thus, there must always be a path for the current. Second, when the system is in standby and the current is freewheeling through the chopper, a small voltage must be applied to compensate for the voltage drop across the semiconductor devices and the current leads. Hence, the system is in a "trickle charge" mode. There are unique control issues that govern this type of operation, which will be discussed later in this thesis. Also, seamless, bi-directional operation with is one of the biggest control issues.

For pulsed power applications rapid charge and discharge are needed. In order to accomplish this, the system must be capable of producing a high voltage across the magnet and the capability of sustaining high current for several seconds.

In a system where dynamic response is important it is necessary to push the switching frequency as high as possible. Technically, by increasing the switching frequency a higher control bandwidth can be achieved. It is with this thought process that the topology and devices for this system where chosen.

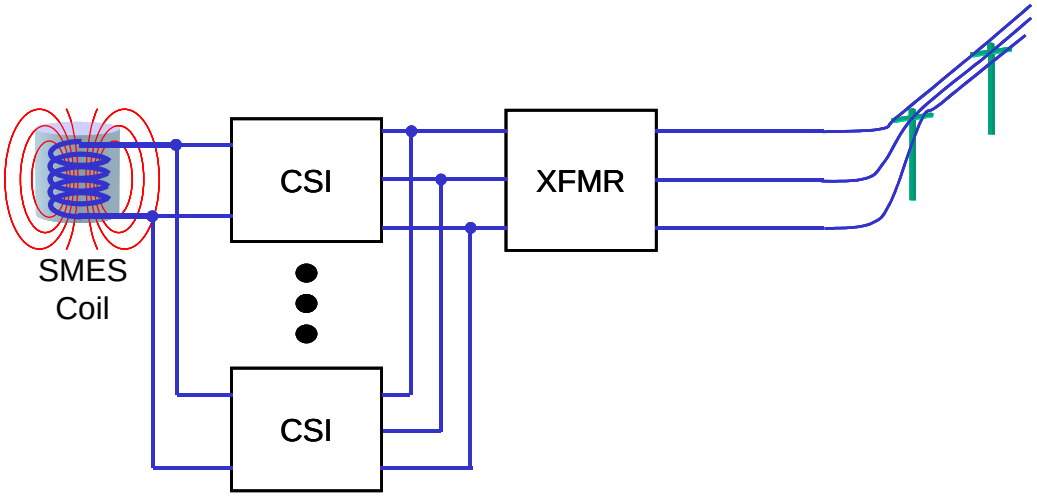
1.4 CPES PCS Overview

Two different PCS designs were considered, the PCS proposed by Westinghouse that incorporated the voltage source inverter (VSC) followed by a dc-dc bi-directional



- Chopper : 2 Quadrant Boost
- 24 Pulse VSI : 4 of 6 Pulse VSI

Figure 1.2 Block diagram of Westinghouse proposed PCS



- CSI : 2 SCR and 4 GTO Converters
- XFMR : Y-Y and Y- Δ

Figure 1.3 Block diagram of General Electric proposed PCS

chopper, shown in Figure 1.2, and the current source inverter (CSI), proposed by General Electric, which is shown in Figure 1.3. It was found that the VSC would have lower system energy loss and system cost than the CSI approach. More advanced techniques, such as multi-level topologies and soft switching which can help improve overall system dynamics, size and weight, are more available with the VSC than with the CSI [16]. It is for these reasons that the VSC approach was chosen.

Both VSC and chopper construction was based on the PEBB concept. This entails developing one module - in this case the module is one phase leg - that can be duplicated and connected in such a way to produce power electronics equipment to perform a specific task. The PEBB cell is identified in Figure 1.4. Three of the PEBB cells make up the VSC or inverter portion of the PCS, each one representing one phase, and two modified PEBB cells, as can be seen in Figure 1.4, make up the bi-directional chopper. The actual PEBB module or phase leg for the VSC is shown in Figure 1.5 [17].

1.4.1 Topology

The three-level topology provides for a higher voltage rating relative to the two-level topology. This is true because each switch only sees half the DC-link voltage at any given time. A voltage rating of 1800 V is obtained using the Powerex 400 A, 1200 V IGBT module. Since only one device is switched every switching cycle with only half the DC-link voltage, the inductor current ripple is reduced and switching losses are decreased by approximately 50 percent. Three-level technology also eliminates the voltage sharing problems that plague series connected devices [16], [17].

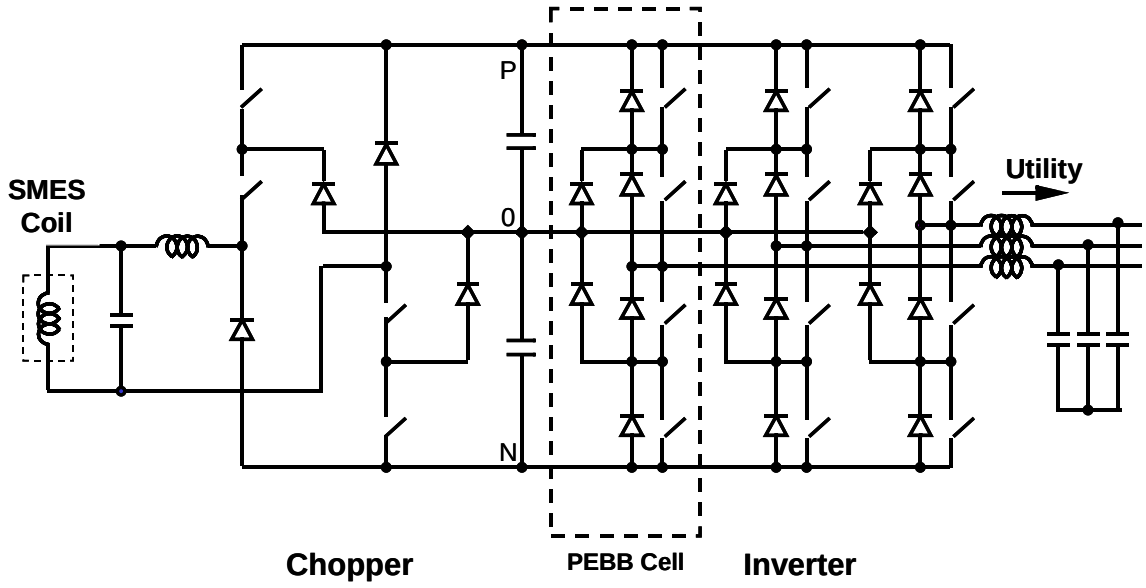


Figure 1.4 Overall structure of the SMES PCS

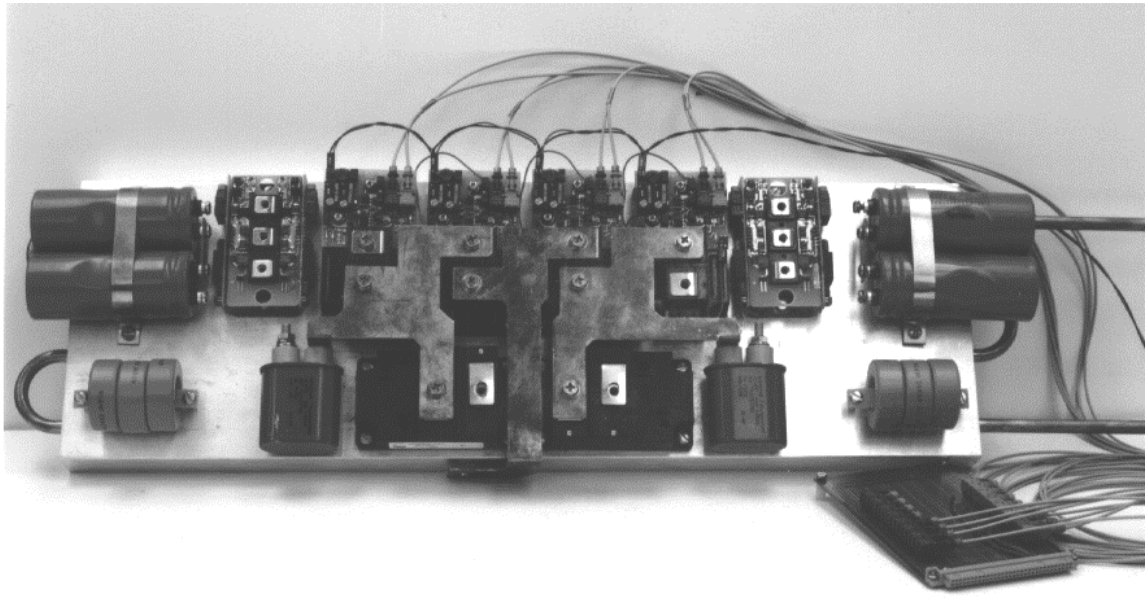


Figure 1.5 Actual PEBB module

Both the VSC and chopper employ zero-current transition (ZCT) pulse width modulation. ZCT alleviates bulky inefficient snubber components, reduces device

stresses and simplifies thermal management. In addition, soft switching allows the switching frequency to be increased [16], [17]. The switching frequency of the VSC and chopper is 20 kHz. This increased switching frequency results in an improvement in controller bandwidth and in turn improves overall system dynamics. With this improved dynamic performance bulky passive components on the DC-link and magnet can be significantly reduced while maintaining the ability to quickly respond to line fluctuations before sensitive equipment is effected.

1.4.2 Devices Considerations

Most SMES applications demand a relatively high power rating from the PCS, greater than 1 MW. Due to this power requirement the scope of possible devices is mainly limited to the GTO and IGBT. The main advantage of the GTO is the conduction voltage drop. Conduction losses in a GTO are approximately 25 % that of the IGBT. This is a particularly important detail if current from the magnet is intended to circulate through the chopper for an extended period of time.

However, for this converter the IGBT has many more advantages. The conduction voltage drop is higher than that of the GTO but switching losses are considerably less. This allows the switching frequency to be increased and consequently can lead to smaller reactive components and an overall smaller and cheaper system design. Another disadvantage to the GTO is the need for a snubber circuit. This criteria definitely favors the IGBT as no snubber circuit is needed. The GTO is more difficult to turn off. The GTO requires approximately 1/5 of the anode current to gate the device, where the IGBT only requires a small gate current to charge the device gate capacitance

[16].

Since the design stage of this project, the IGCT, built by ABB [19], and ETO [20], developed at CPES, have shown significant improvements in device technology. These devices have the voltage and current ratings and conduction voltage drop benefits of the GTO with reduced switching losses comparable to the IGBT. A 2 MW or higher PCS for SMES is slated for the next phase of the project. At this power level the IGCT or ETO come into heavy consideration as their benefits begin to outweigh those of the IGBT.

2 DEMONSTRATION and SYSTEM CONTROL ISSUES

2.1 Demo Location and Magnet Specifications

Two SMES demonstrations, sponsored by the Office of Naval Research (ONR), has been planned in this project. The first is a high temperature superconducting (HTS) SMES demo at the Naval Research Lab (NRL) in Washington, D.C. The second demo is with a low temperature superconducting (LTS) magnet at the National High Magnetic Field Lab (NHMFL) in Tallahassee, FL.

2.1.1 NRL HTS Magnet

The magnet at NRL, shown in Figure 2.1, is a 7.25 T, 12 H, high temperature superconducting (HTS) magnet. Energy storage capabilities of the magnet are determined by the inductance, 12 H, and maximum rated current, 120 A at 7.25 T. The energy stored, $E = 0.5*L*I^2$, is 86 kJ. The maximum current during the demonstration will be 100 A. To date this demonstration would set a world record for energy stored in a HTS magnet at approximately 60 kJ, some 50 kJ higher then the previous record. The operational voltage of the magnet, L*di/dt, is 240V and the absolute maximum voltage rating is 500 V. The operating parameters of this HTS magnet work well with the new power electronics. The PCS has been routinely operated between 200 – 500 V at 100 A.

This magnet was designed and built by American Superconductor (ASC). It consists of the magnet system with the above specifications, a Leybold compressor for cooling the magnet to its operational temperature of 17 K at zero field, a power supply and control cabinet [18]. Interfacing the CPES power electronics with the magnet is not a

trivial issue as safety elements could be bypassed with the retrofitting of the new power system. This work will be done in conjunction with ASC to insure continuous protection of the magnet and minimize risk to the system.

Figure 2.1 86 kJ HTS magnet at NRL

2.1.2 NHMFL LTS Magnet

The LTS magnet, shown in Figure 2.2, at the NHMFL is much. The LTS magnet has a current capability of 2000 A and an inductance of 32 H, resulting in maximum

energy storage of 64 MJ. Unfortunately, the majority of the energy storage capabilities of this magnet cannot be utilized because of the parameter mismatch between the power electronics and the magnet. The operational parameters of the LTS magnet are 200V and 2000A while the PCS is 1800V and 150A.

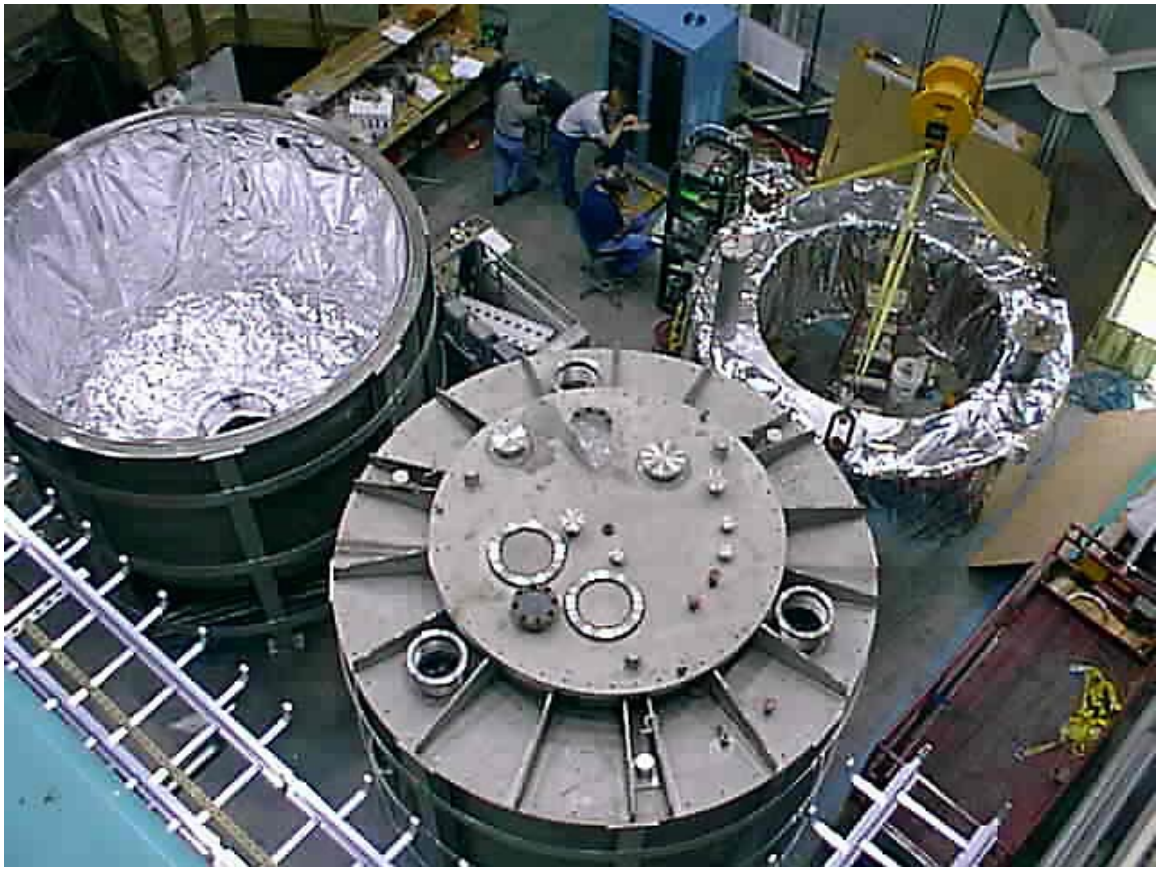


Figure 2.2 64 MJ LTS magnet at NHMFL

2.2 Demonstration Objectives

There are several main objectives for the demonstration. They are to successfully demonstrate the following:

- Integration of the PCS and Superconducting Magnet
- Diversification of the PCS
- Utility stabilization/Power Leveling
- Uninterruptible Power Supply (UPS)
- Naval Applications
    - Pulse Power
    - Motor Drives
- Importance of Future Work

2.2.1 Demonstration Scenario

The following demonstration scenario is based on the LTS SMES at the NHMFL in Florida. The input to the PCS will be 208 Vrms, 3 phase.

2.2.1.1 Charge

In all charging scenarios the output to the magnet will be on average 4 kW, with a maximum power output of 8 kW at 150 A and 53 V. The current and voltage waveforms at the terminals of the magnet during charging can be seen in Figure 2.3. The magnet will be fully charged to 150 A in approximately 94 seconds. After maximum operating current is reached the current will freewheel through the chopper and a small voltage will be applied to compensate for the voltage drop across the semiconductor devices and the current leads until the magnet is ready to be discharged.

2.2.1.2 Discharge

The first objective to be demonstrated, aside from the successful integration of the PCS and magnet, is the ability for the electronics to push power back onto the utility grid. This will demonstrate the systems ability to work as an uninterruptible power supply, utility stabilizer and to be used for load leveling. After charging the magnet, the VSC will remain connected to the utility and power will be delivered from the magnet back onto the utility grid with a constant power of 4kW for approximately 70 seconds. During discharge, the current direction in the magnet cannot be changed. Therefore, the chopper must reverse the voltage polarity across the magnet terminals in order to have power flow in the other direction. This discharge scenario is illustrated in Figure 2.4.

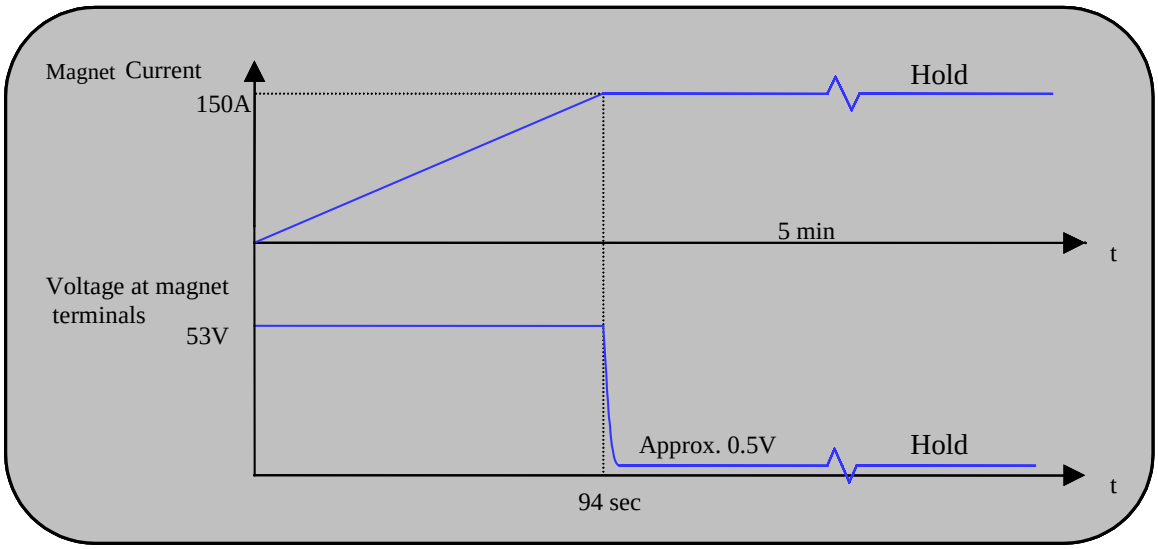


Figure 2.3 Magnet current and voltage during charge mode

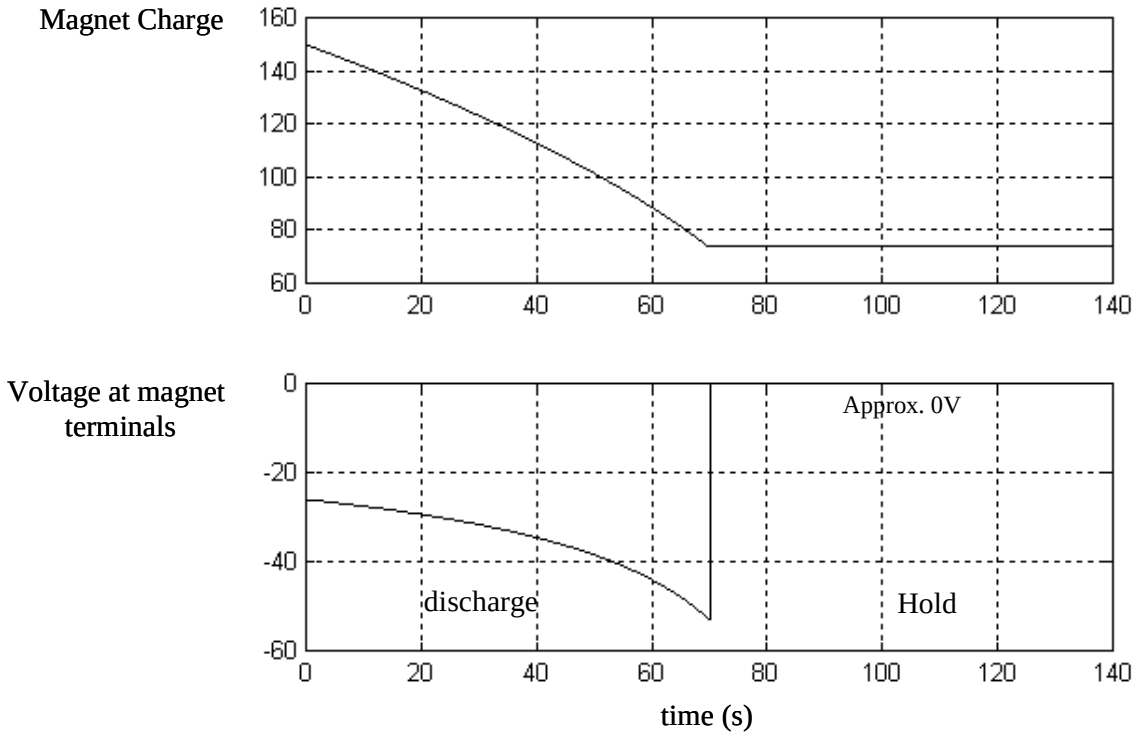


Figure 2.4 Magnet current and voltage during utility discharge mode

2.2.1.3 Vital Load

The next stage of the demonstration is to show the ability of the system to operate as a constant power source to vital loads. In the demo, a 5 hp motor with a blower is used to simulate a vital load on a ship. Three possible scenarios are to be demonstrated, two soft starts and one normal start. On a ship there could arise a situation that requires many vital loads to come on line at once. To avoid an unacceptable strain on the power distribution system, the SMES electronics could be used to soft start the loads by using voltage/frequency control as illustrated in Figure 2.5. The first scenario will soft start the motor to half speed and the second soft start to full speed. The time required for soft start and the operating speed can be adjusted very easily by only changing a single constant in

the control software. This versatility also is to be shown. Another desired control objective is to bring a vital load up to speed as fast as possible in the case of an emergency. The motor is to be brought up to speed as quickly as possible by instantaneously applying the full voltage, as if the motor where directly connected to the utility.

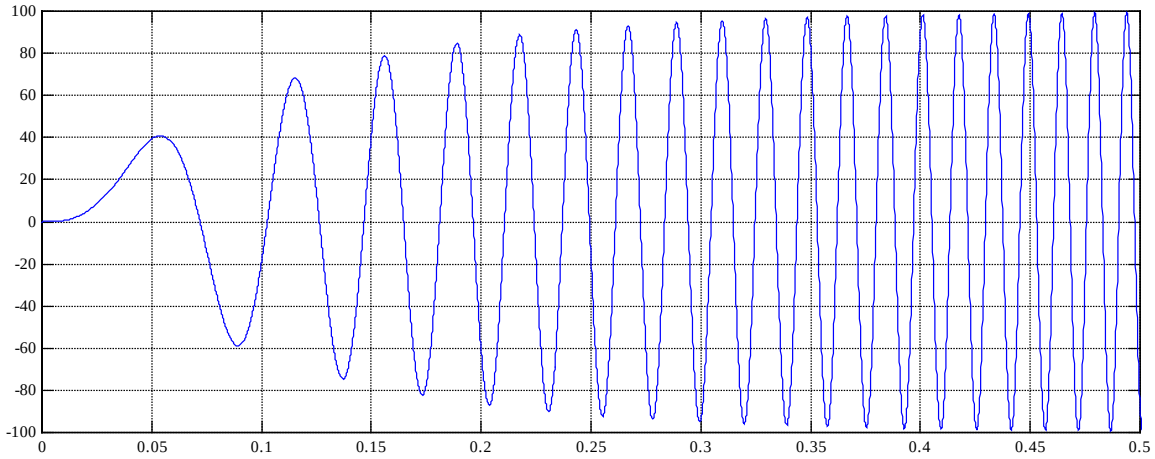


Figure 2.5 Motor soft start – voltage/frequency control

2.2.1.4 Pulse Load

The final demo objective is to show the use of SMES for pulsed power applications. A load bank that uses six, 5 kW stadium light bulbs will be used. A possible scenario is shown in Figure 2.6, where three pulses, 30 kW each, of approximately 3 seconds in length at about 85 A and 208 V are shown. The current at the magnet terminals is decreased over the duration of the pulse while the voltage is increased, thus, a constant power output is maintained.

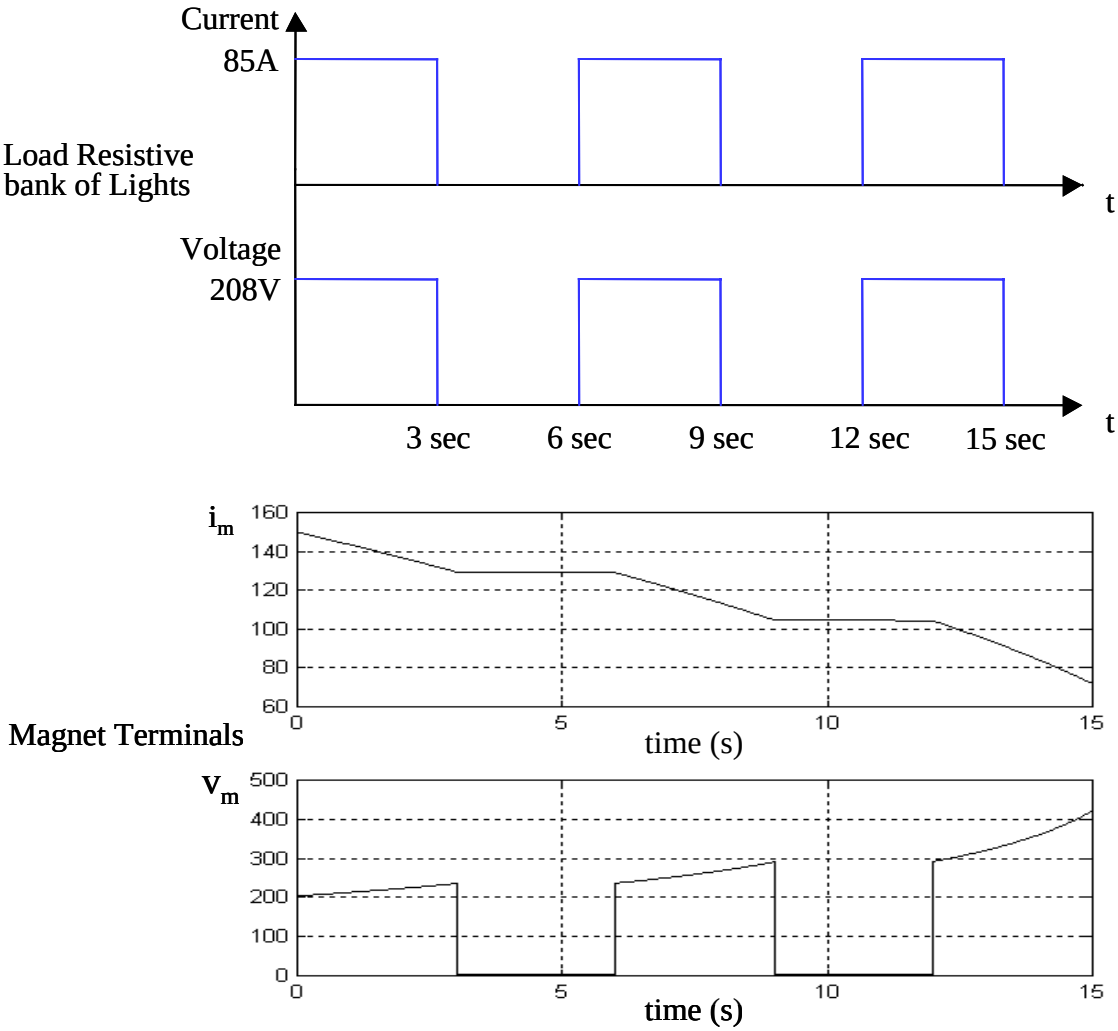


Figure 2.6 Pulse load demonstration

2.3 VSC/Chopper Responsibilities

The responsibilities of the VSC and the chopper change throughout the course of the demonstration depending on which mode of operation is being exercised. There are six different modes of operations. They are hold, standby, charge, discharge, motor and pulse as can be seen in Figure 2.7. During magnet charge the VSC is operating as a boost rectifier and the chopper is operating as a dc/dc buck converter as it controls the charge

rate of the SMES coil. The charge rate is normally minimized to reduce losses within the magnet and consequently cause excessive warming of the coil. In the magnet discharge mode the VSC operates as a voltage source inverter and draws power from the DC link while the chopper, operating as a dc/dc boost converter, maintains the DC link voltage making sure not to exceed the charge rate limit of the SMES. As can be seen in Figure 2.7, in transition from the charge to discharge mode the system must pass through the hold mode. In this mode the VSC continues to maintain the DC link voltage and the chopper trickle-charges the SMES coil to make up for the losses in the non-superconductive portion of the system. The system remains in this mode until power from the SMES is needed. The standby mode is similar to the hold mode except the VSC is disconnected from the utility and the current in the magnet decreases very slowly as it freewheels through the chopper without any compensation for the drop across the semiconductor devices or leads. This is basically a dead time as the VSC is switched from the utility to a particular load. This mode will only be utilized for a short period of time. In both the motor and pulse modes the VSC is operating as a voltage source inverter and the chopper maintains the DC link voltage. Depending on whether the desired mode is pulse or motor the VSC will produce a short pulse or the desired motor start sequence, respectively.

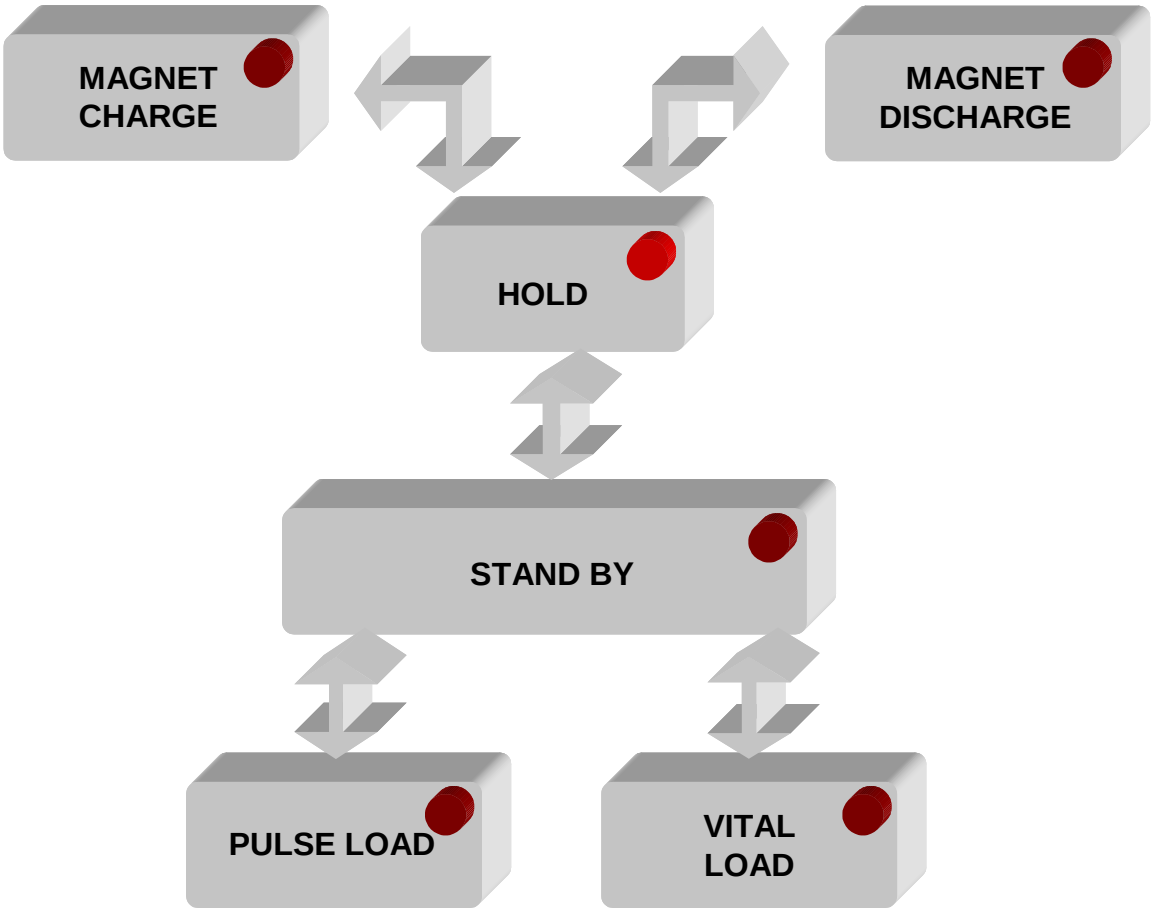


Figure 2.7 Main demonstration modes

A typical charge/discharge scenario entails as follows. During the charge mode, the VSC will be working as a boost rectifier and has the responsibility of maintaining the DC link voltage and the chopper draws power from the DC link to charge the magnet at the desired rate. At any given time during the charge sequence the operator has the ability to switch from the charge mode to the hold mode, if this is not exercised the controller automatically transitions to the hold mode. In the hold mode, the chopper would be trickle-charging the magnet to maintain the present current level. When power is needed from the magnet, the operator would switch the system into the discharge

mode. At which point the chopper stops trickle-charging the magnet and the VSC stops maintaining the DC link. The chopper would then begin to maintain the DC link and the VSC would shortly thereafter transition to operate as a voltage source inverter and begin drawing power from the DC link and powering the load or providing power to the utility grid. It is these types of charge/discharge transitions that have caused problems in the control of both the VSC and chopper. These transitions will be discussed in more detail later as they are a major motivation for this thesis.

2.4 Control Issues

There are unique control issues that arise when interfacing the chopper with the magnet. First, the chopper must at all times maintain a freewheeling path for the current in the magnet. Failure to provide this path, if not properly protected, could prove catastrophic to the PCS as well as the magnet. While the chopper is maintaining a constant current in the magnet the voltage applied to the magnet is very low (on the order of a few volts) to compensate for the voltage drop across four semiconductor devices and the leads from the PCS to the SMES magnet. Because of duty cycle limitations the chopper, at these low voltages, must employ a unique modulation scheme that cycles between the buck and boost modes of the chopper in that positive and negative $V_{DC}/2$ is applied to the coil with a resulting small average positive voltage.

One of the main design goals of the power stage hardware was to implement a 3-level IGBT based topology. This would basically allow better devices and in turn a higher switching frequency. This higher switching frequency resulted in a higher bandwidth and reduced DC link capacitance. The fast dynamics of the system eliminate

the need for large energy storage on the DC link, thus, capacitor selection is based only on ripple requirements. If mode transitions are not controlled properly the DC link voltage can fluctuate significantly and when the converter begins regulating the DC link again some unexpected transients can trigger protection circuits and shut down the controllers. Alleviating this type of operation demands a concise controller and proper controller initialization in mode transitions.

These control issues have caused problems during initial experiments. The DC link voltage falls to zero during mode transitions and unexpected and uncontrollable transients cause fault triggers. This thesis focuses on generating a comprehensive model of both the dc/dc bi-directional chopper and the voltage source converter so that a complete analysis of the system can be performed. This analysis looks at the charge/discharge transients and on improving the bandwidth of the boost rectifier and voltage source inverter control loops.

2.5 Integrated Controller

Both the VSC and the chopper have individual controllers that do not share any means of communication. It was therefore imperative that a system-level controller be developed that would integrate the controls of the chopper and VSC as well as configure the proper load/utility connections to the VSC. The overall demonstration setup (Digital controller with User Interface) with integrated controller is shown in Figure 2.8. The integrated controller allows a smooth, easy, user-friendly way to transition between different modes during the demonstration. The sequence and timing of switching loads and modes of operation can be quite complex; this integrated controller would eliminate

the possibility of human error in this regard.

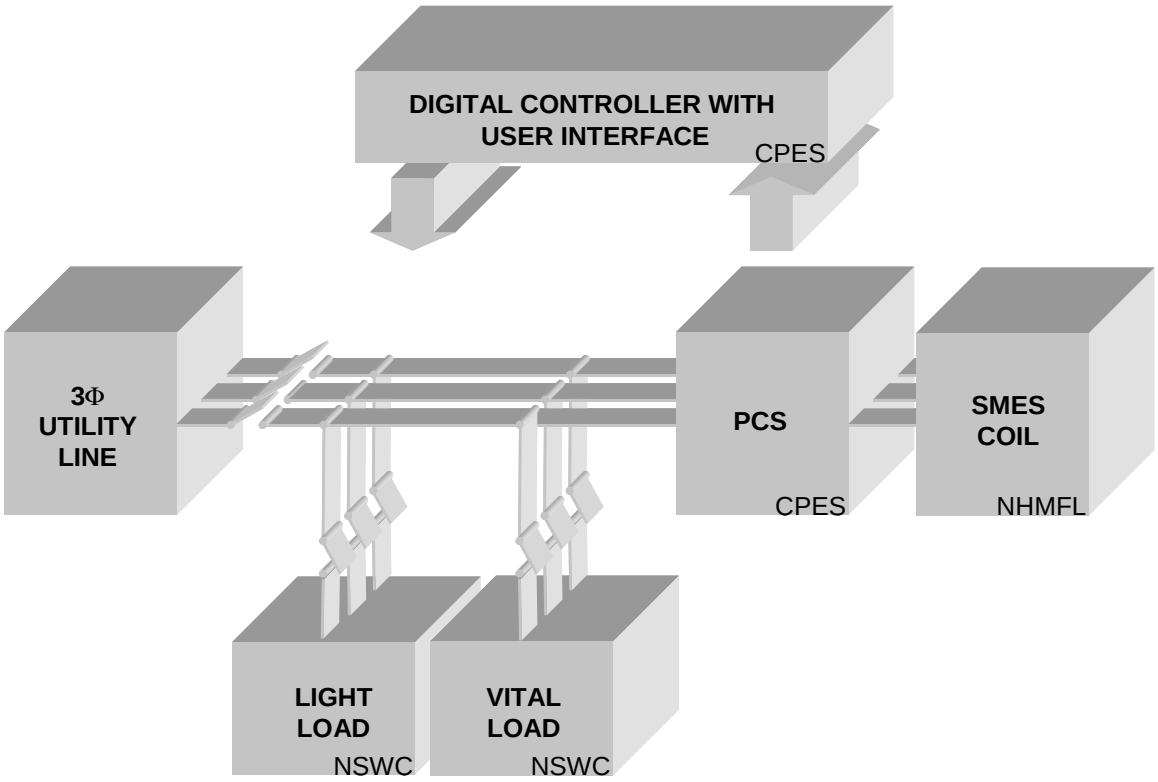


Figure 2.8 Overall demo setup

The integrated control concept is simple. There is a user interface board that consists of seven push button switches as shown in Figure 2.9. These seven switches toggle between the six different modes shown in Figure 2.7 as well as two alternative motor modes. The controller sends out a 3-bit signal to the chopper (and the chopper in turn forwards this to the VSC), via a fiber optic link, indicating which mode of operation to employ. The user interface board also indicates with a series of LEDs the 3-bit signal being transmitted to the PCS and the mode of operation in which the system is operating.

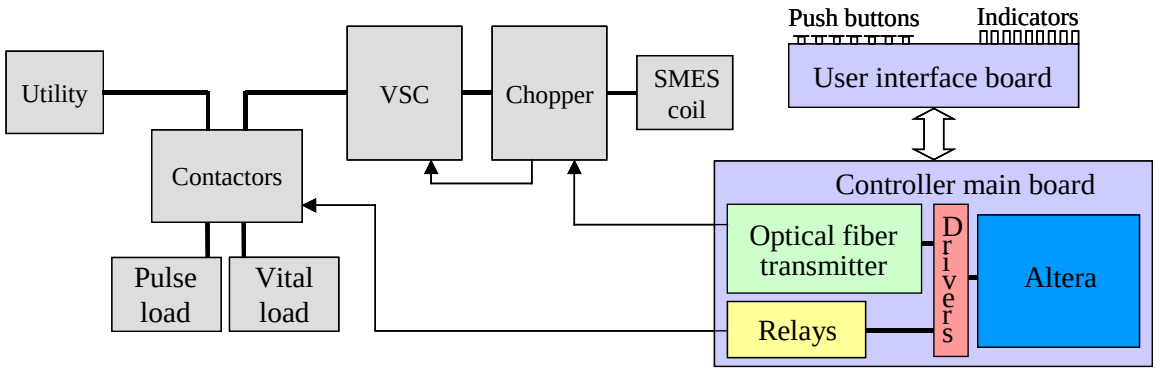


Figure 2.9 Functional block diagram of integrated controller

The user interface board is connected to the main processor board via shielded cable. A block diagram of the main processor board is shown in Figure 2.10. This board utilizes an Altera FLEX7084 Programmable Logic Device (PLD) for decision-making. The Altera receives the user input command from the interface board and outputs the corresponding 3-bit control signal to the PCS and indicates that signal on the user interface board. Table 2.1 provides the 3-bit codes and their corresponding modes. The main board also configures the proper connections to the VSC and indicates the mode of operations on the user interface board.

3-bit control signal	Corresponding mode
000	Hold
001	Discharge
010	Hold
011	Motor 1
100	Charge
101	Motor 2
110	Pulse
111	Motor 3

Table 2.1 3-bit codes and corresponding modes

Present State	Switch Combination	Next State
Hold	1010000 0110000 0000000 else	Charge Discharge Standby Hold
Standby	0010000 0001000 0000100 0000010 0000001 else	Hold Pulse Motor 1 Motor 2 Motor3 Standby
Charge	0010000 else	Hold Charge
Discharge	0010000 else	Hold Discharge
Pulse	0000000 else	Standby Pulse
Motor 1	0000000 else	Standby Motor 1
Motor 2	0000000 else	Standby Motor 2
Motor 3	0000000 else	Standby Motor 3

Table 2.2 State machine transtion conditions

A state machine consisting of eight different state, one for each mode, is implemented in the Altera device. A diagram of the state machine is given in Figure 2.10. The state machine dictates a particular sequence which the user must follow. This

provides a systematic disconnect of sources and loads and eliminates any possibility of the VSC and chopper both fighting to maintain the DC-link. A table detailing the state machine transition conditions is given in Table 2.2.

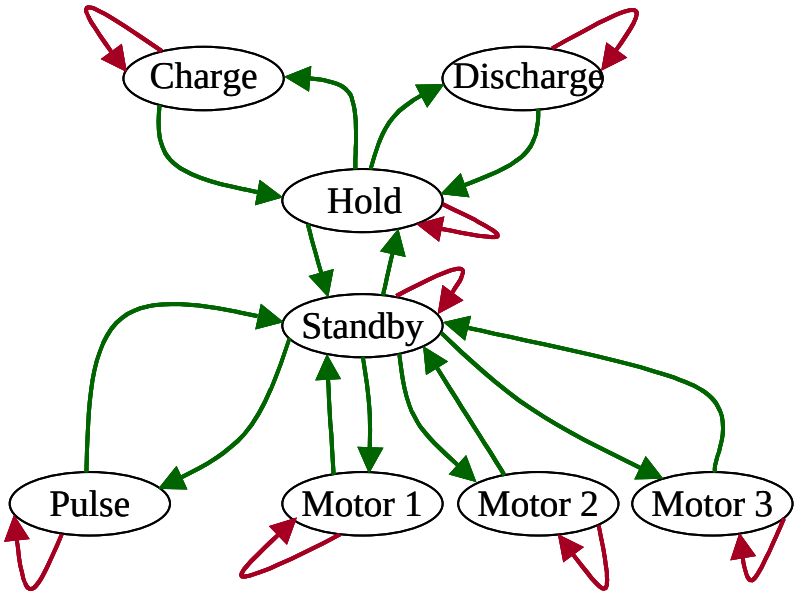


Figure 2.10 State machine implemented in the Altera device

The Altera drives three 4452 MOSFET drivers. They drive a logic level MOSFET, IR 3803, that in turn triggers the relays that engage and disengage the corresponding contactors. One contactor connects and disconnects the utility from the PCS while the other two contactors switch in and out the light and motor loads. A timer, configured in the PLD, is employed that induces time delays between sending new control signals to the PCS and switching in and out the utility and loads. This provides a dead time to ensure that loads are never directly connected to the utility and that the PCS does not begin to operate in a particular mode with an improper load connected. A detailed circuit schematic showing controller components and over all system connections is shown in Appendix A. Photos of the user interface and main proccessor

boards are also given in Appendix A.

The majority of the Altera is coded using the Altera Hardware Description Language (AHDL) with the remainder of the operations completed in the graphic design editor. The complete AHDL code, graphic design schematic and Altera chip pin out can be found in Appendix B.

3 3-Level Bi-Directional DC-DC Converter

The two-quadrant, bi-directional chopper controls power flow to and from the SMES coil. This is true regardless if a three-phase AC or DC system powers the PCS. In the case of a three-phase AC power system the VSC interfaces the three-phase load or source to the chopper and the chopper interfaces the VSC to the coil. When the power system is DC the VSC is eliminated and only the chopper is needed. Thus, the chopper is an intricate part of a SMES system regardless of the specific system in which it is connected.

The optimization of a SMES system tends to incorporate a high voltage DC link (1800 V for this system). In addition, to obtain the dynamic response needed, a high switching frequency, upwards of 20 kHz, must be achieved. While GTOs and SCRs can meet this high voltage requirement they cannot be operated at switching frequencies greater than several kilohertz. However, IGBTs can meet the switching requirements but do not have as high a voltage and current ratings as GTOs and SCRs. Therefore, a multi-level topology was used to achieve the desired converter voltage rating using IGBTs. The three-level chopper circuit diagram is shown in Figure 3.1 [16].

Conventional converter designs obtain higher voltage ratings by placing devices in series. However, proper voltage sharing of these devices is a major problem, especially during the turn off and turn on transitions. During these transitions one device can turn on more quickly leaving only one device to block a larger then expected voltage. Snubbers can be used in this case but this leads to higher losses and normally the devices still need to be heavily derated. The multi-level topology does not share these problems.

It ensures even voltage sharing by clamping the device voltage to Vdc/2 by way of the diodes Dc1 and Dc2 shown in Figure 3.1. The diodes D1 and D2 must be capable of blocking the full voltage, Vdc. However, diodes do not have the same voltage sharing

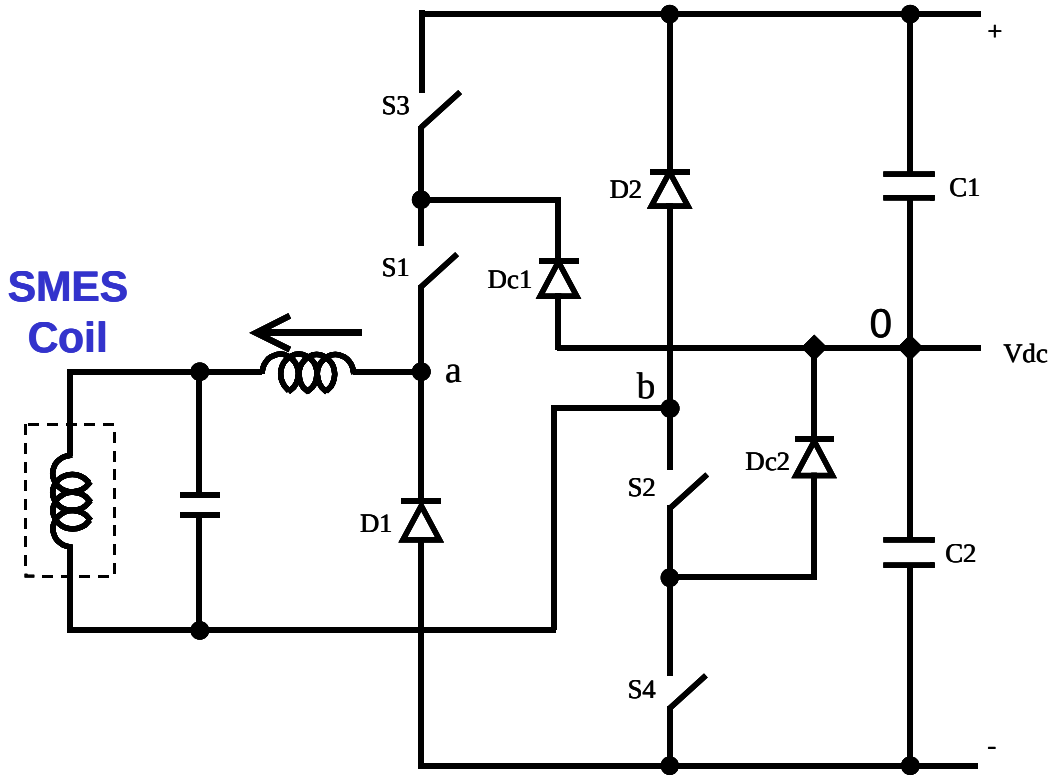


Figure 3.1 Three-level bi-directional chopper

problems as the active switches and can be placed in series to meet the voltage requirement. One issue that arises from the multi-level topology is maintaining the charge balance of the DC-link capacitance. Being able to maintain the charge balance of the DC-link capacitors is critical in order to provide even device stress and can be accomplished by selecting different subtopologies on alternate switching cycles [17].

The chopper incorporates two different control loops, one for the charge and one

for the discharge mode. Both loops employ an inner coil voltage loop while the charge mode has an outer current loop and the discharge mode with an outer voltage loop. The inner voltage loop is mainly to limit the voltage applied to the coil and consists of a zero and two poles for both charge and discharge. This control block diagram is shown in Figure 3.1a. The outer current loop in the charge mode regulates coil current. In the discharge mode the control objective is the Dc-link voltage, thus, the requirement of the outer voltage loop. Controller performance and analysis is discussed in Section 3.3.

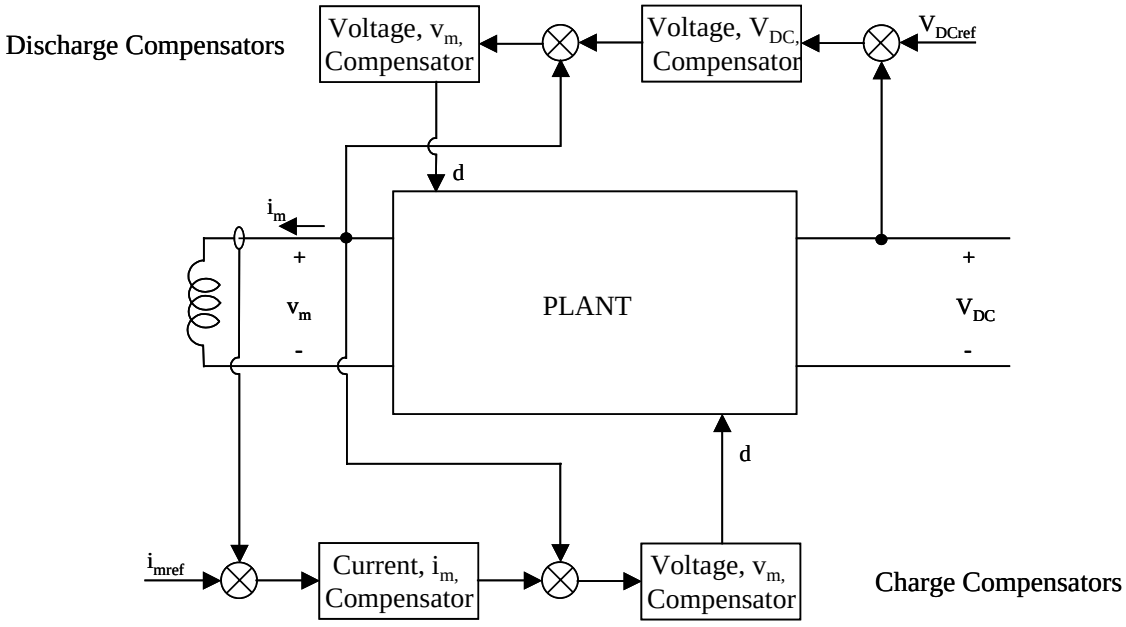


Figure 3.2. Charge and discharge mode control block diagram

3.1 Buck and Boost Modes of Operation

There are basically two modes of operation for the chopper; the charge mode and the discharge mode. During these two modes, the chopper is operating as a simple DC/DC buck or boost converter, respectively. Due to the three-level topology, the

chopper has a possibility of nine subtopologies, which are shown in Figure 3.2, while the two-level topology only offers four subtopologies. We see that multiple subtopologies exist for Vab equal to Vdc/2, -Vdc/2 and 0. By properly controlling the converter, these available states can be chosen so that switching losses and current ripple is reduced and that the charge balance of the DC-link capacitors is maintained.

When the chopper is in the buck, or charge, mode switches S1 and S2 are always on and switches S3 and S4 are modulated to obtain the proper voltage, Vab, across the coil. During this mode, subtopologies (1), (5), (6) and (7), from Figure 3.2, are utilized. When operating in the boost, or discharge, mode switches S3 and S4 are always off and switches S1 and S2 are modulated. This mode utilizes subtopologies (2), (5), (8) and (9).

Only the subtopologies closest to the reference voltage are used, this reduces the switching losses and reduces current ripple. In this manner only one device is switched per switching cycle and the devices only switch half of the DC-link voltage. Since only one device is switched each switching cycle, problems of voltage sharing are eliminated and switching losses are reduced by 50% compared to the two-level converter counterpart. In addition, by controlling which different redundant state is being employed, namely (6) or (7) for buck and (8) or (9) for boost, the charge balance of the DC-link capacitors can be maintained [16], [17].

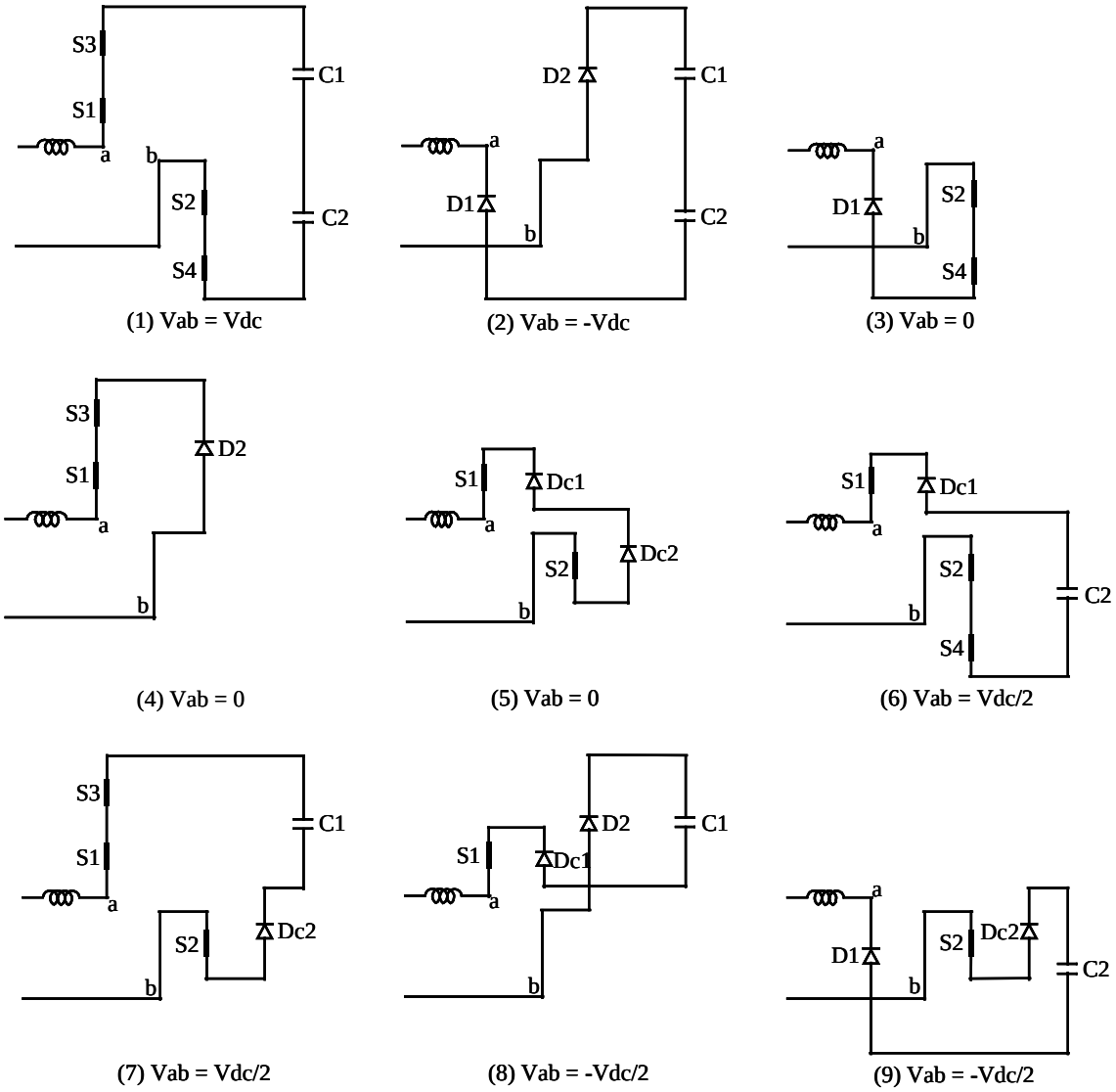


Figure 3.3 Subtopologies of the three-level, bi-directional chopper

Although three switch combinations are possible for Vab = 0, only one of these redundant states, (5), is utilized. Recall that in the buck mode S1 and S2 are always on and that only the sub topology nearest to the voltage reference will be used. Therefore, prior to switching to the zero vector the system is operating in either the (6) or (7) sub-topology. By examining these two states and the transition into the different zero states

we find that minimal switching action is obtained by always transitioning into the (5) sub-topology. The same examination can be done for the boost mode of operation. Since the capacitor does not play a part in these zero states, charge imbalance from using the sub topology is not an issue.

Due to duty cycle limitations the chopper cannot continue operation solely as a buck converter when trying to maintain a constant current in the magnet. The voltage necessary to maintain a hundred amps in the coil is approximately 5 volts. If the DC-link is operated at 400 V, as will be done in the demo, then the duty cycle required to produce 5 V output is,

$$D = \frac{Vo}{Vin} = \frac{400}{5} = 0.0125$$

Practical duty cycle limits are at approximately 0.9 and 0.1, thus, this is an unattainable duty cycle. To solve this problem the chopper begins to alter its modulations scheme. It applies both positive and negative voltage to the coil in order to obtain a small positive average voltage across the coil. Essentially, the chopper is alternating between charge and discharge in that it alternates positive and negative applications of voltage to the coil. Hysteresis control is implemented to detect when the required output voltage drops below a particular value. This value is set to correspond to the duty cycle limit of 0.1. When the threshold voltage is reached the converter alternates between the charging and discharging. This is shown in Figure 3.4. When the duty cycle crosses the threshold and the control scheme is initiated the duty cycle corresponding to the positive application of voltage changes from 0.1 to 0.2, S_1 and S_2 in Figure 3.4, and the duty cycle corresponding to the negative application of voltage, S_3 and S_4 in Figure 3.4, changes from 1 to 0.9, thus,

the average output voltage of the converter is the same as if the chopper operated only in the charging mode with a duty cycle of 0.1. As the required voltage continues to drop the charging duty cycle is decreased while the discharging duty cycle is maintained at 0.9, therefore, the resulting average duty cycle is less then 0.1. This control method also produces a discontinuity in the modulation scheme. A three level model of the chopper is developed later in this chapter that enables this discontinuity to be simulated and investigated.

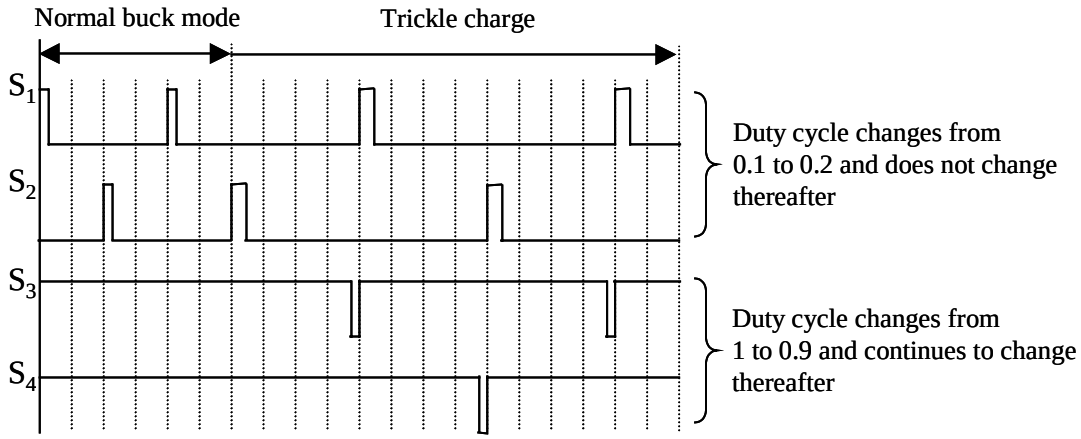


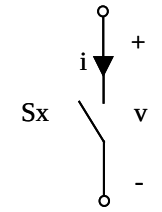
Figure 3.4 Modulation discontinuity from charge to hold (trickle charge)

3.2 Development of 3-Level Model

Before the introduction of SMES, very little work had been conducted in the area of two-quadrant bi-directional choppers [16]. This has left many research opportunities to advance or even develop soft-switching and multi-level technology for two-quadrant choppers. Previously, control designs and simulations where based on the standard average two-level model. A more complete average model that incorporates the three-

level topology is necessary to accurately detail the system's operation and observe transient behavior. Therefore, a three-level model was developed which averages each active switch in the converter.

The converter was broken down into the two operating modes, buck and boost. A table was developed, based on the circuit schematic shown in Figure 3.1, that listed possible switching combinations and the current path that corresponds to those combinations. The method used to model the switching function is as shown in Figure 3.2a.



$$Sx = \begin{cases} 1, & v = 0, \quad \textit{switch Sx is closed} \\ 0, & i = 0, \quad \textit{switch Sx is open} \end{cases}$$

where x = 1, 2, 3, 4

Figure 3.5. Definition of switching function for ideal switch

The buck mode is detailed in Table 3.1 and that of the discharge mode in Table 3.2.

Table 3.1 Model development for buck mode

Vab	S3	S4	Current Path
Vdc	1	1	C1-S3-S1-a-b-S2-S4-C2
Vdc/2	0	1	Dc1-S1-a-b-S2-S4-C2
Vdc/2	1	0	C1-S3-S1-a-b-S2-Dc2
0	0	0	Dc1-S1-a-b-S2-Dc2

S1 = S2 = 1

Table 3.2 Model development for boost mode

Vab	S1	S2	Current Path
0	1	1	a-b-S2-Dc2-Dc1-S1
-Vdc/2	0	1	a-b-S2-Dc2-C2-D1
-Vdc/2	1	0	a-b-D2-C1-Dc1-S1
-Vdc	0	0	a-b-D2-C1-C2-D1

S3 = S4 = 0

A circuit schematic for each mode was then developed based on the voltage Vab required at the output terminals and the corresponding current path outlined in the tables. Figures 3.5 and 3.6 are the switching models of the chopper while operating in the buck and boost mode, respectively. The complete average model of the bi-directional chopper was obtained by combining these two modes of operation and averaging the switching model. The final model is shown in Figure 3.7.

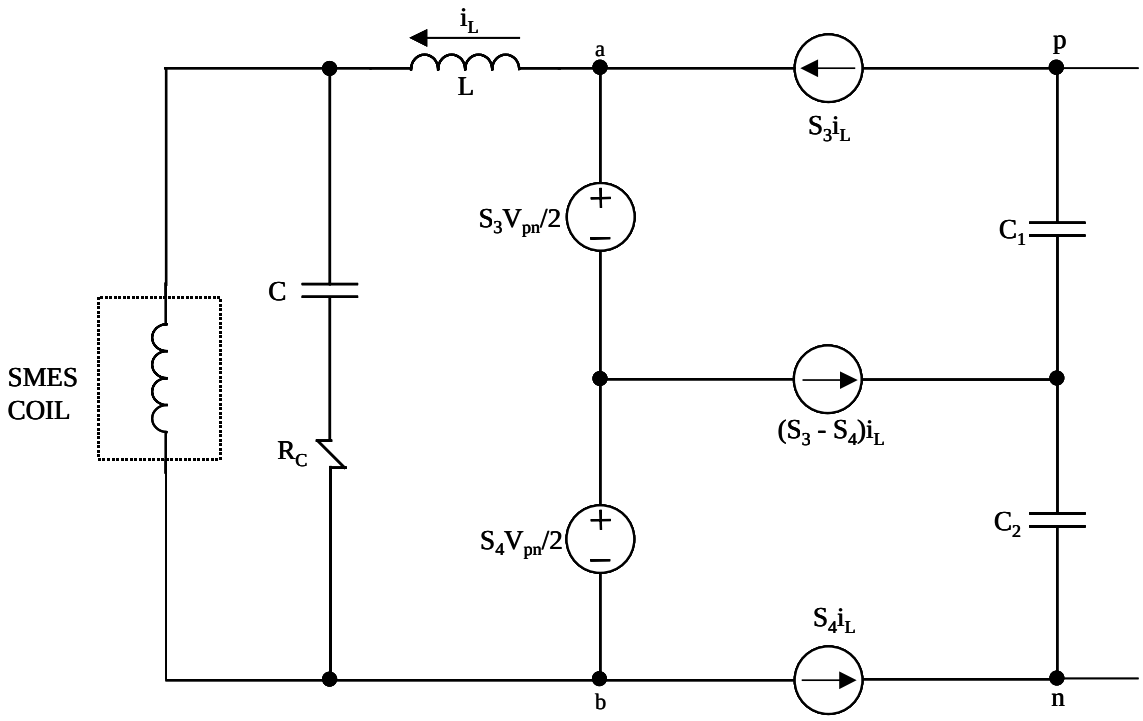


Figure 3.6 Switching model of chopper in charge mode

This model provides the opportunity to simulate the chopper working bi-directionally and the unique modulation techniques when operating with the SMES unit. For example, in SABER, mast code can be developed to incorporate the duty cycle limits and the hysteresis control during trickle charge. This can verify the modulation concepts and provide a simple way of testing new modulation ideas. In addition, this model provides a way to monitor and insure the charge balance of the DC-link capacitors.

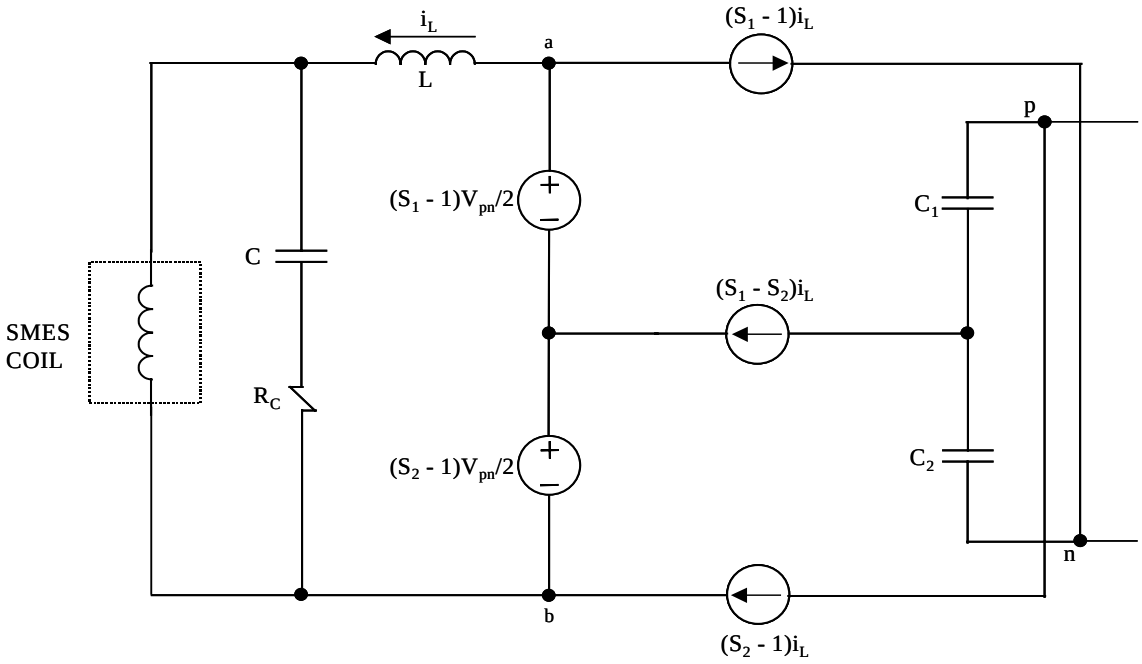


Figure 3.7 Switching model of chopper in boost mode

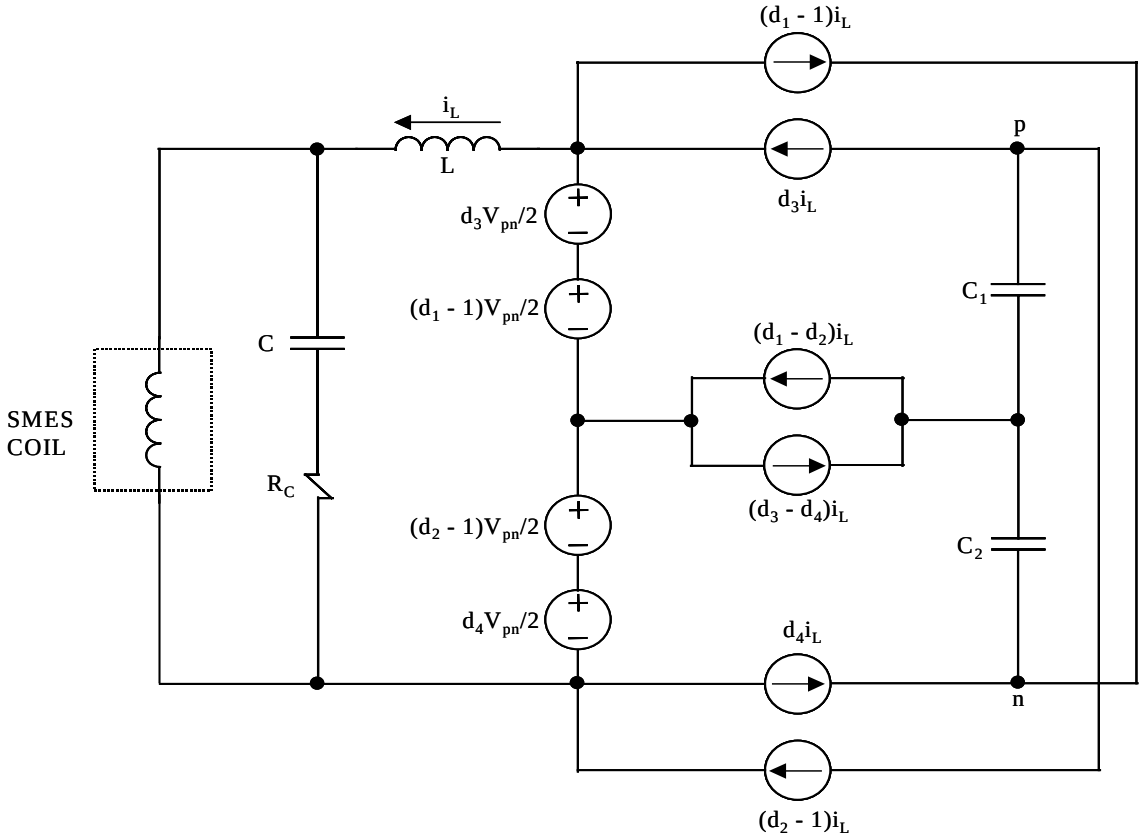


Figure 3.8 Complete average model of three-level bi-directional chopper

3.3 Simulation Result

The three-level chopper was simulated and results of its control loop transfer functions and transient behavior were obtained. With the chopper it is not possible to measure the transfer function at different operating points without reducing the order of the system by replacing the SMES inductor with a constant current source. During the charging process the current in the magnet is linearly increasing and there is a change in the duty cycle, therefore, there is no steady state condition around which to linearize.

3.3.1 Charge Mode

Transfer functions in the charge mode can only be obtained when the coil current has reached its reference value and the controller maintains the set value by applying a few volts across the magnet, in essence, providing a trickle charge. This operating condition is with a very low duty cycle and a coil current of 100 A. The simulation circuit schematics, with parameter values for the charge and discharge modes are provided in appendix C.

There are two loops that make up the controls for the charge mode. There is an inner voltage loop that regulates the coil voltage and an outer current loop to control coil current. The plant transfer function, buck duty cycle to coil voltage, around which this compensator was designed is shown in Figure 3.8. The resonant frequency is 1 kHz. This is due to the filter inductor and capacitor and is not affected by the coil inductance. This is a simple second order transfer function and the compensator design is straightforward. The effects of a high frequency ESR zero can be seen in the phase diagram. The compensator for the coil voltage loop consists of a lead-lag (pole and zero)

and an integrator. The transfer function for the compensator is shown in Figure 3.9. The integrator is used to obtain high DC gain and the pole and zero are placed to obtain the maximum bandwidth with proper gain and phase margins.

Trying to close above the resonant frequency proved to be very difficult. The peaking requires that the cross over be relatively far from the resonant frequency. However, at this point the digital delay becomes significant and meeting the phase requirements is not possible. Therefore, the crossover is before the resonant frequency at approximately 240 Hz. The plot of the loop gain is given in Figure 3.10. It can be seen from Figure 3.11 that the closed loop transfer function provides good regulation below 300 Hz.

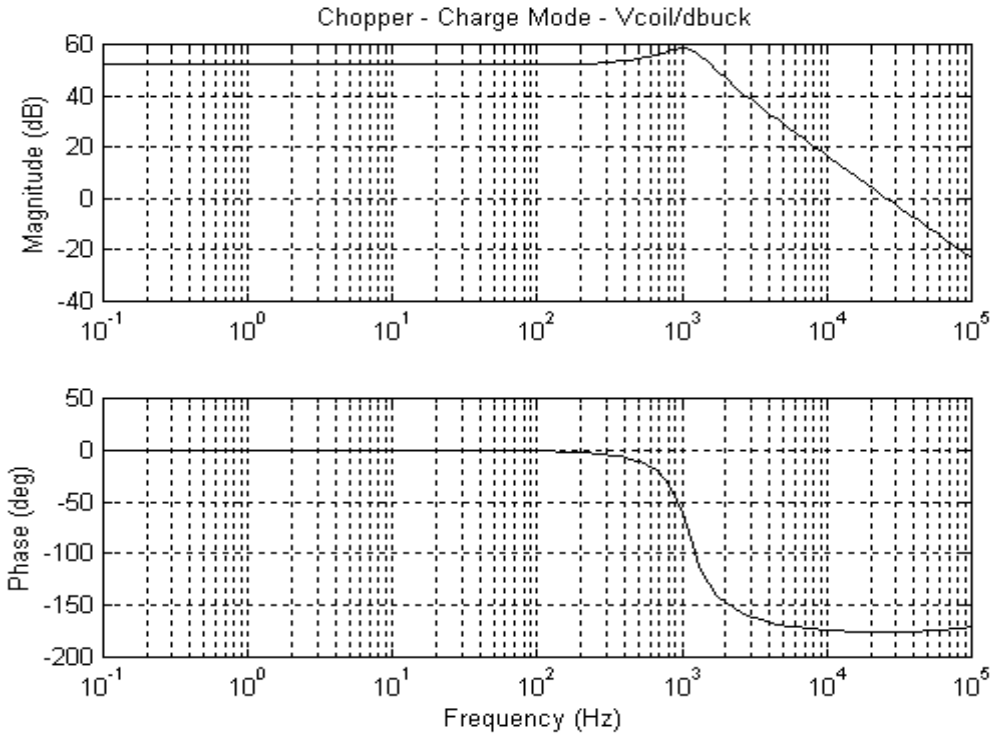


Figure 3.9. Buck duty cycle to coil voltage transfer function

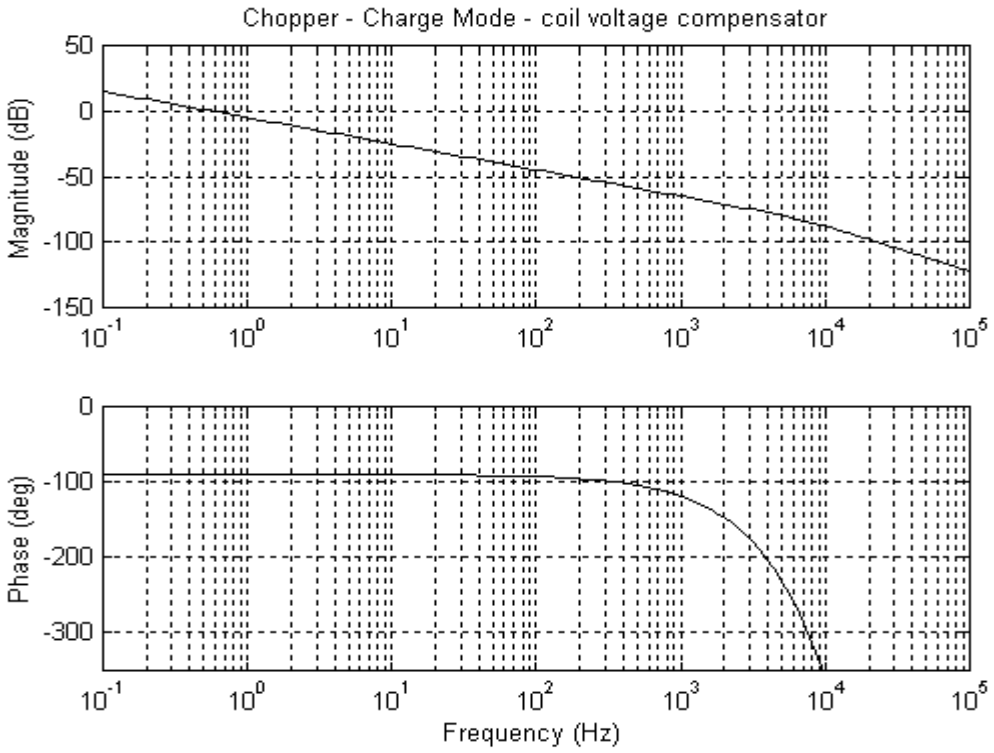


Figure 3.10. Transfer function of the coil voltage compensator

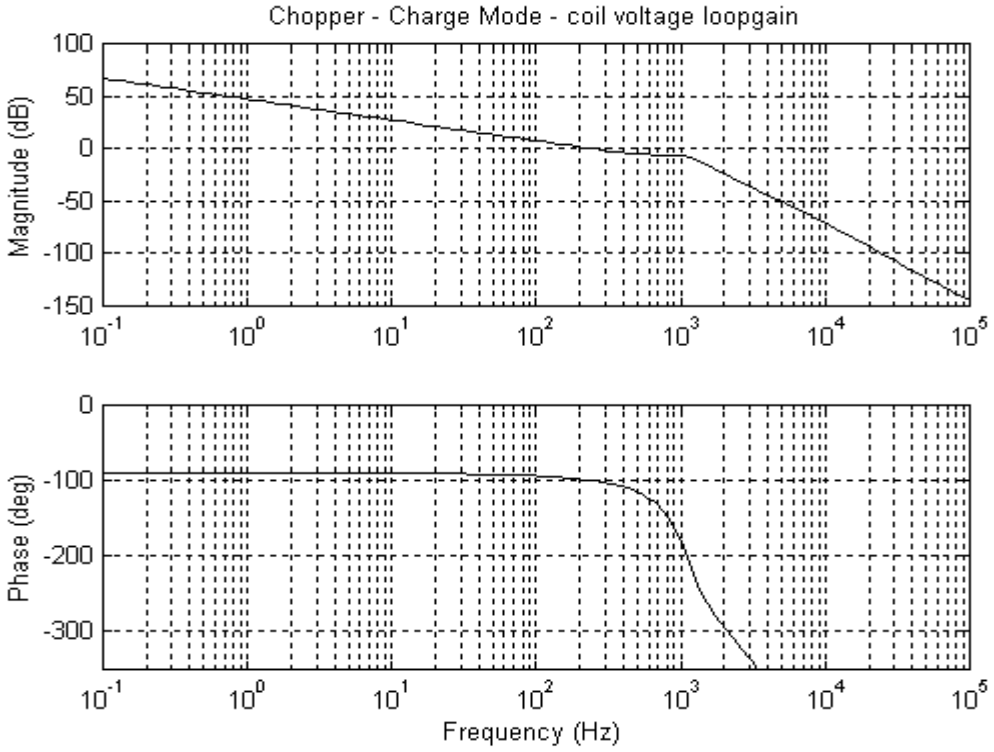


Figure 3.11 Transfer function of coil voltage loop-gain.

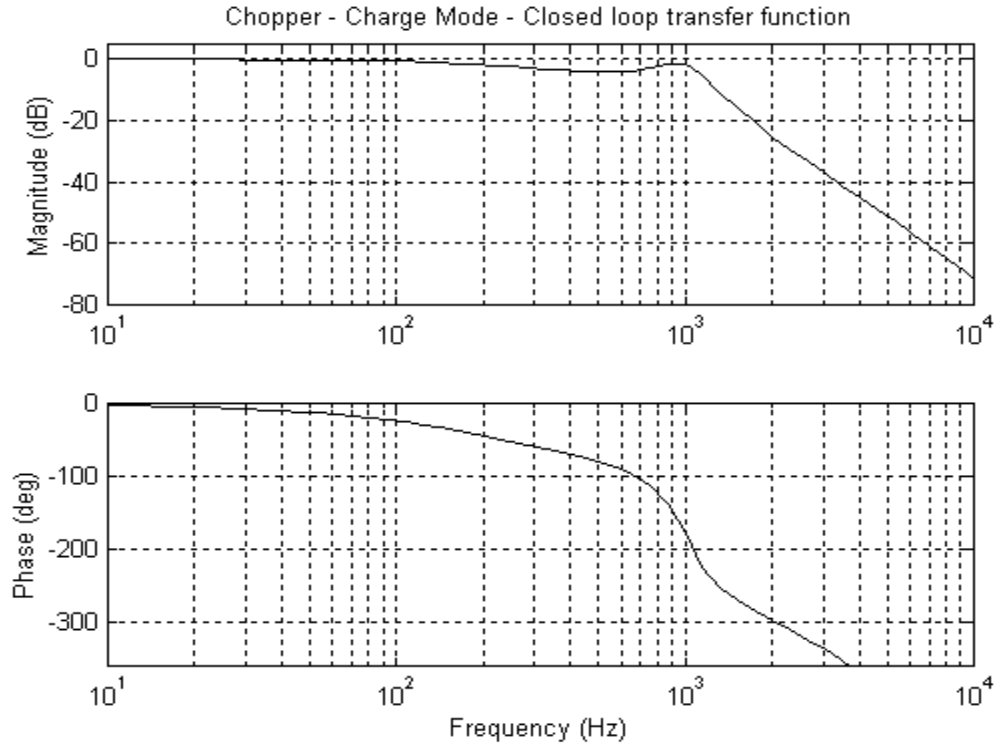


Figure 3.12 Closed loop transfer function – coil voltage reference to coil voltage

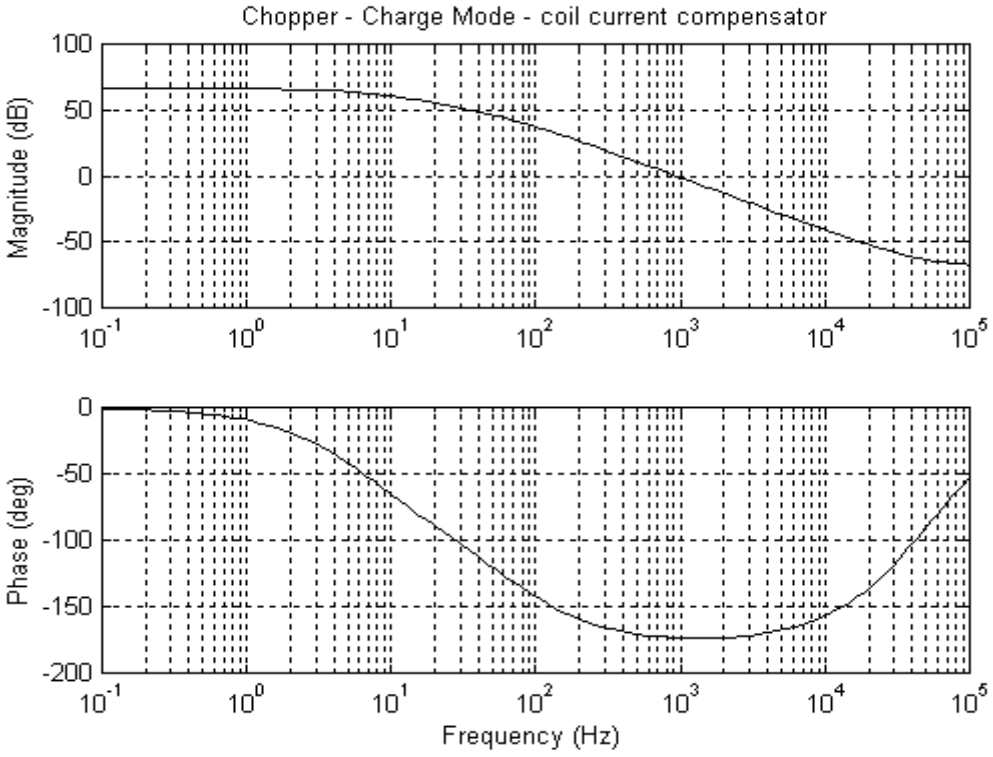


Figure 3.13 Transfer function of coil current compensator

The outer loop provides regulation of the SMES coil current. The compensator for this loop is given in Figure 3.12. It consists of two lead-lags and a limiter. The constraint of the limiter is set to the desired charging voltage. During the charge process, until the coil current approaches the coil current reference, the coil voltage is always hitting the limit, in effect opening the current loop. This is another reason that during the charge mode transfer functions at different operating points cannot be obtained. The coil current loop-gain transfer function obtained while the controller was maintaining 100 amps in the magnet is shown in Figure 3.13. The outer loop achieved a bandwidth of approximately 230 Hz.

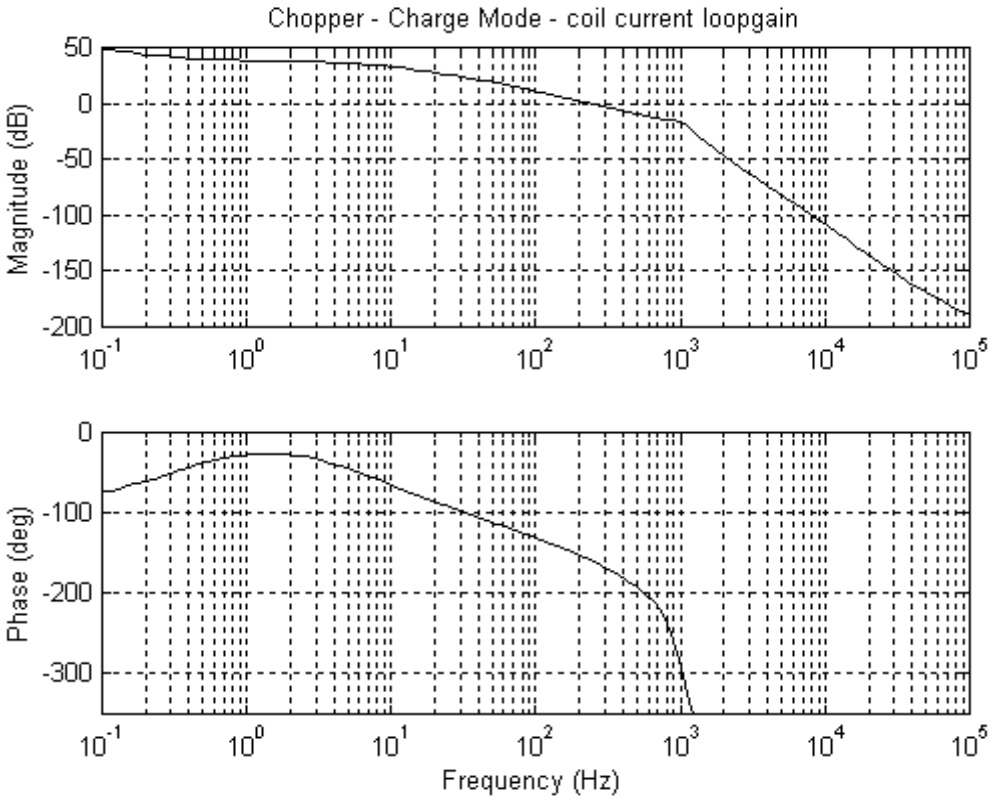


Figure 3.14 Transfer function of coil current loop-gain

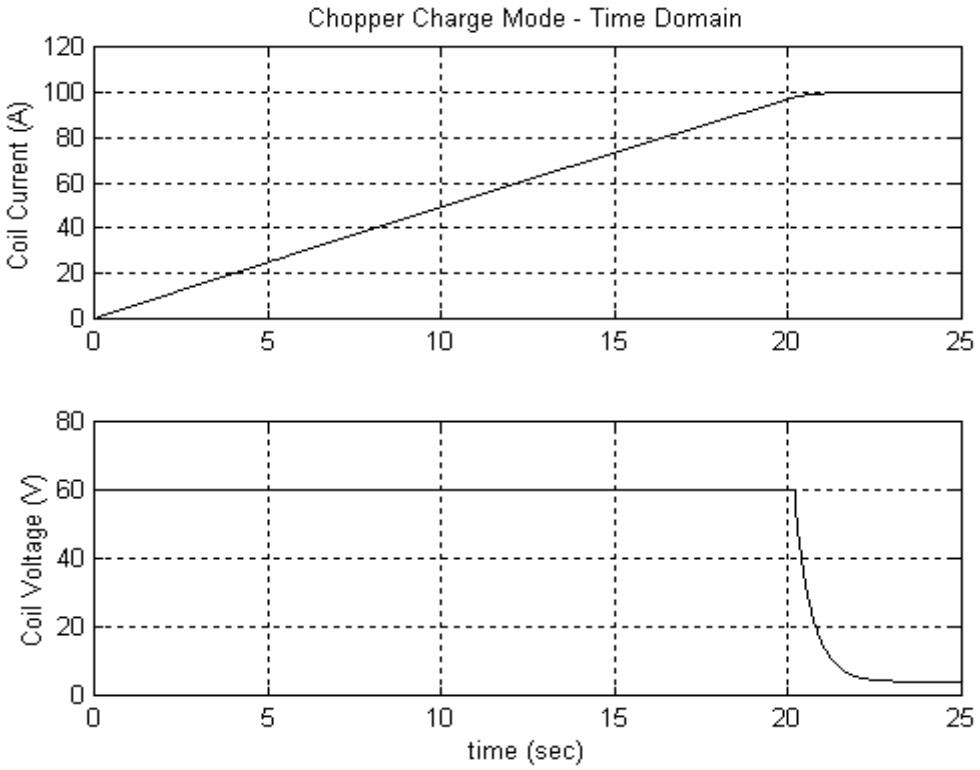


Figure 3.15 Time domain waveforms of coil voltage and current in charge mode.

The time domain waveforms of both the coil voltage and current are shown in Figure 3.14. It can be seen that the coil voltage hits a limit of 60 V during the majority of the charge mode. It is during this time that the outer loop is effectively opened. It is also shown that the coil current is continuously ramping until it reaches the reference value of 100 A, at which point it is linearized and transfer functions are obtained.

3.3.2 Discharge Mode

While the chopper is operating in the discharge mode parameters in the controller are constantly changing, thus, there is no operating point around which to linearize. In this respect the charge mode is slightly different from that of the discharge. In the

discharge mode there is no point at which coil current becomes constant. Therefore, in order to obtain any transfer function the order of the system must be reduced, the SMES coil must be replaced by a constant current source. This allows the controller to reach an operating point, designated by the magnitude of the current source. The controller was designed with this assumption and later simulated with the full order system to verify its stability. The simulated circuit schematic is provided in Appendix C.

Design of the controller for the discharge mode of the chopper follows the same procedure as for the charge mode. There is an inner voltage loop that controls the coil voltage. The plant transfer function, boost duty cycle to coil voltage, around which the coil voltage compensator was designed is shown in Figure 3.15. As is typical for a boost converter the phase delay starts out at –180 degrees. Thus, the first task of the

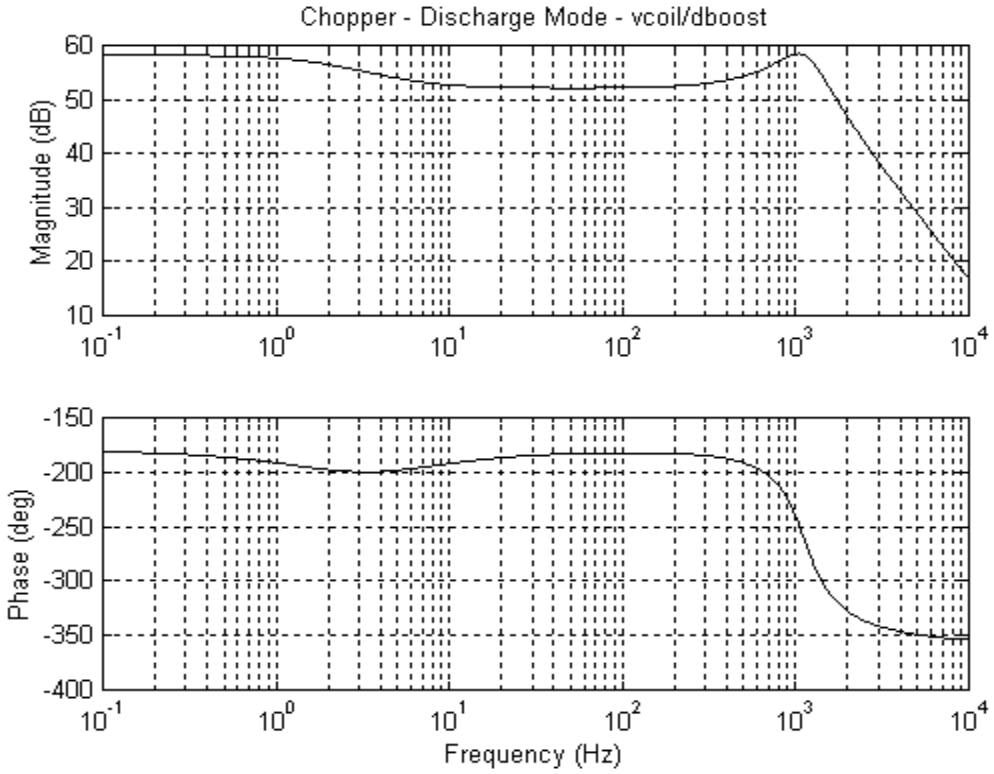


Figure 3.16 Transfer function of duty cycle to coil voltage in discharge mode.

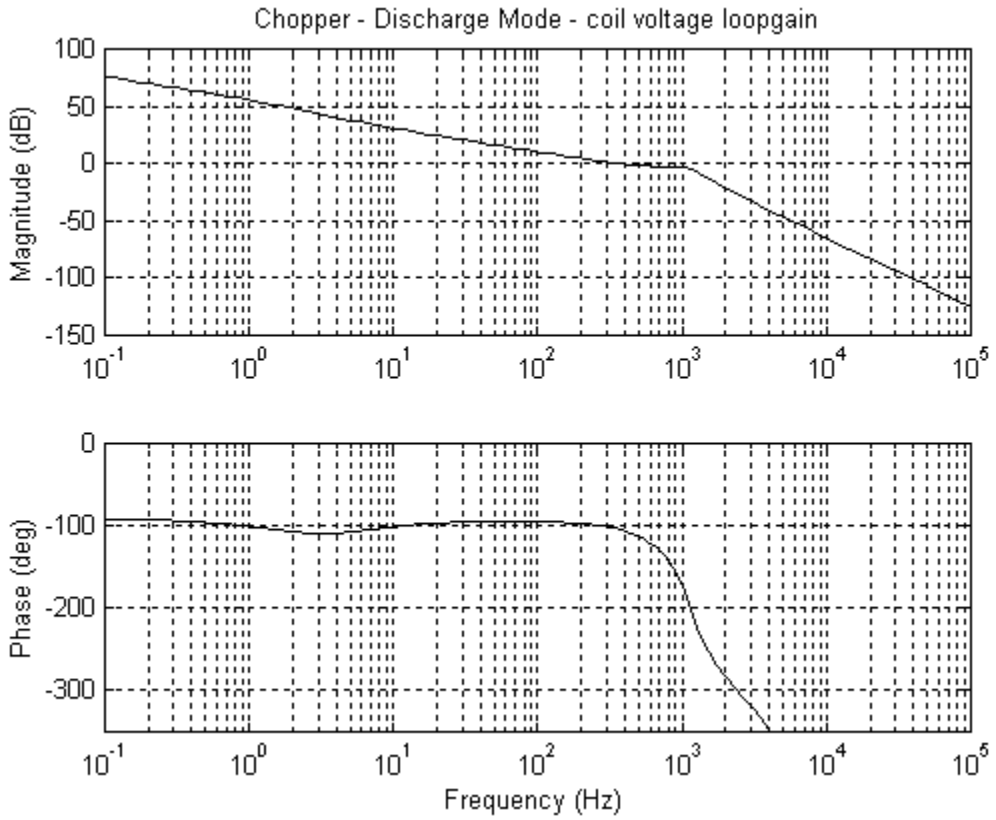


Figure 3.17 Transfer function of coil voltage loop gain in discharge mode.

compensator is to provide 180 degrees phase shift. In addition, an integrator is added to provide high DC gain. The transfer function of the coil voltage loop-gain in discharge mode with 50 A of coil current is shown in Figure 3.16. A bandwidth of approximately 400 Hz was achieved.

The outer loop of the controller regulates the DC-link voltage. This compensator design is based on the coil voltage to DC-link voltage transfer function, shown in Figure 3.17. A proportional-integral controller with a limiter was used in the compensator design. Again, the integrator was added to provide high DC gain and the zero was placed to compensate the pole at 1 Hz, thus, providing continuing –20 dB/dec role off and a

reduction in the phase delay. The limiter provides over voltage protection for the magnet. For this simulation the limiter was set at 150 V. This compensator transfer function is shown in Figure 3.18 and the DC-link voltage loop-gain transfer functions are shown in Figure 3.19. The overall bandwidth of the discharge controller is approximately 90 Hz.

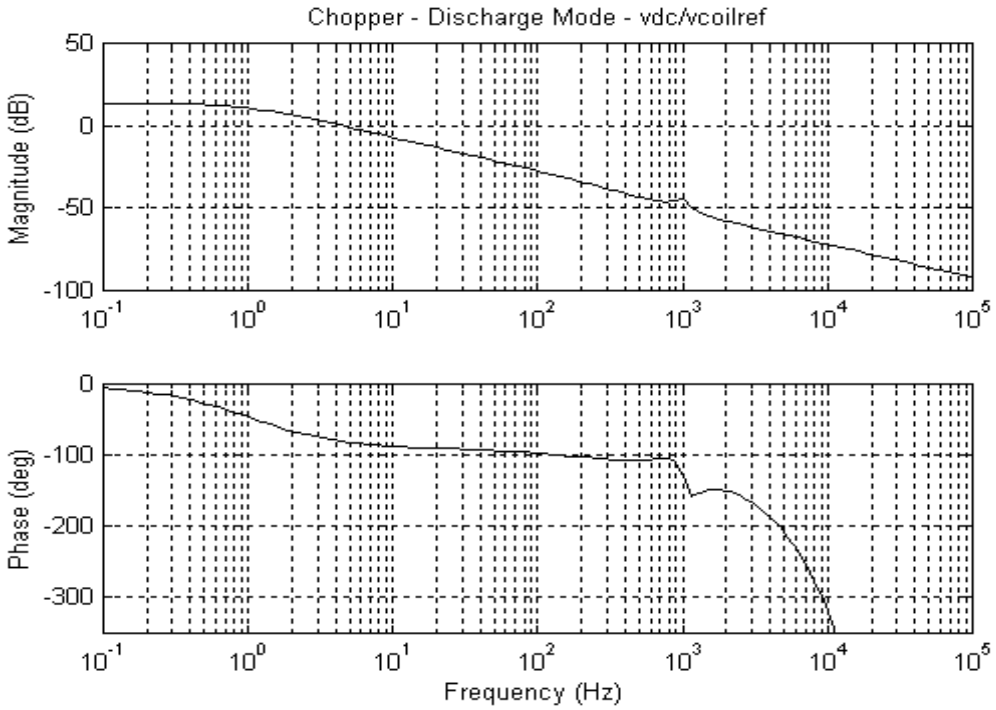


Figure 3.18 Coil voltage to DC-link voltage transfer function in discharge mode.

Time domain waveforms of the chopper in discharge mode are shown in Figures 3.20 and 3.21. They are of the coil voltage and current and DC-link voltage, respectively. A load resistance of 50 ohms was used in the simulation and a DC-link voltage reference of 400 V. The constant current source used to obtain the transfer functions results was replaced with a 12 H inductor with an initial condition of 100 A to simulate a previously charged SMES magnet. It can be seen from the graphs that as the current in the coil decreases that the negative voltage across the coil increases as to provide the needed

power on the DC-link. When the coil voltage hits its limit of 150 V the DC-link voltage begins to collapse as the magnet, at its specific current level and voltage limit, can no longer supply the needed power to the DC-link. This continues until the coil current has reached zero. It is obvious during this simulation that there is no operating point during the charge mode around which to linearize.

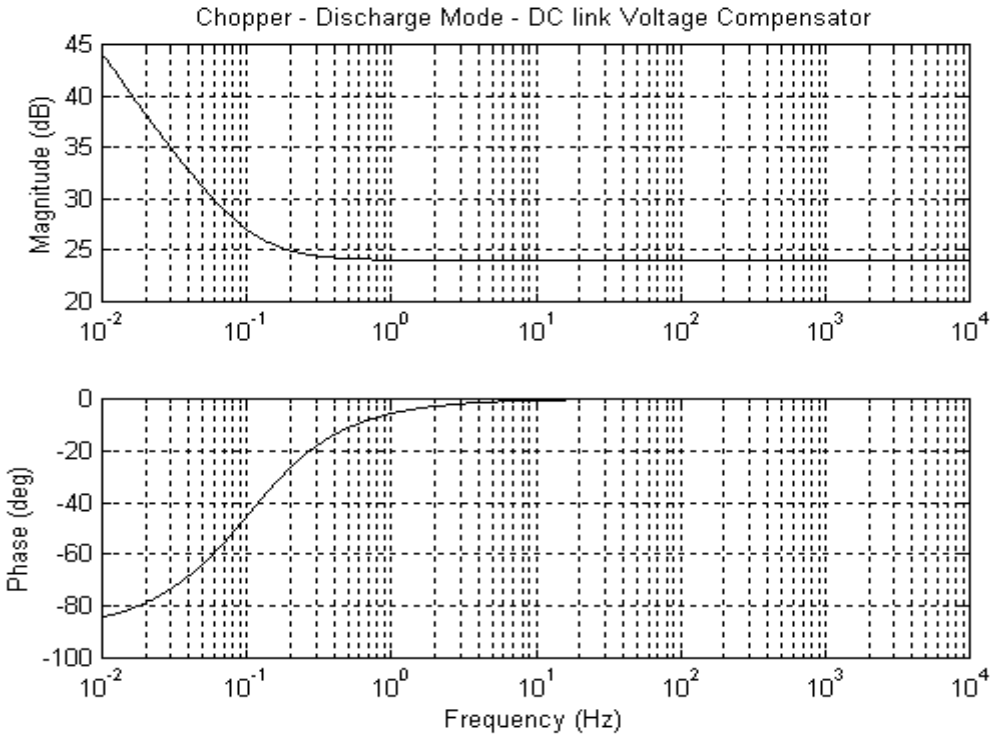


Figure 3.19 Dc-link voltage compensator transfer function in discharge mode.

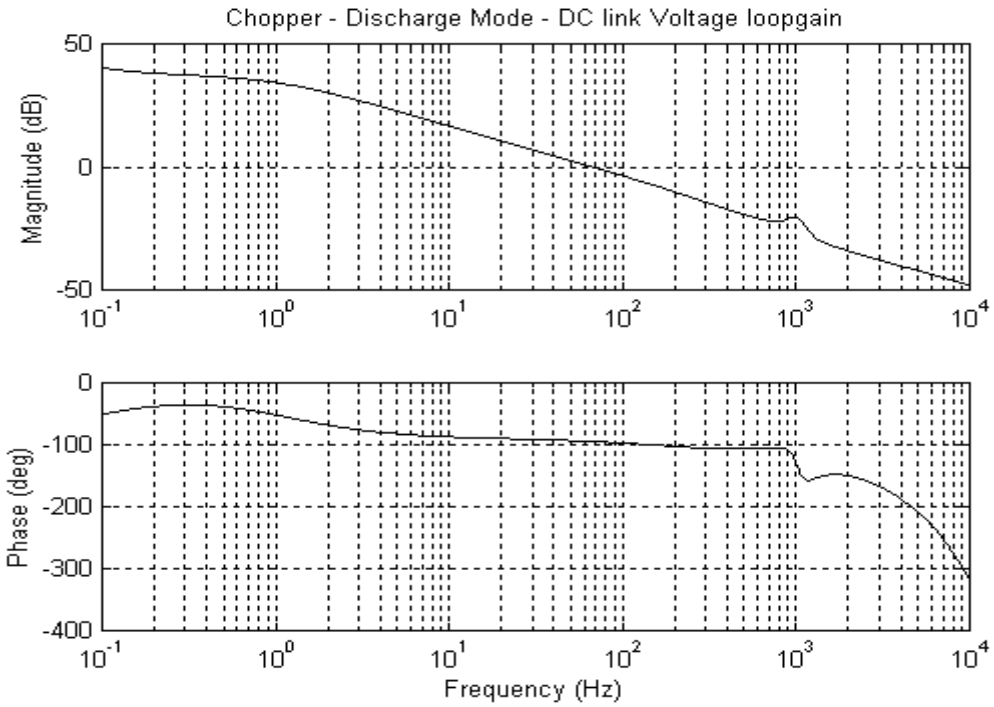


Figure 3.20 Transfer function of DC-link voltage loop-gain in discharge mode.

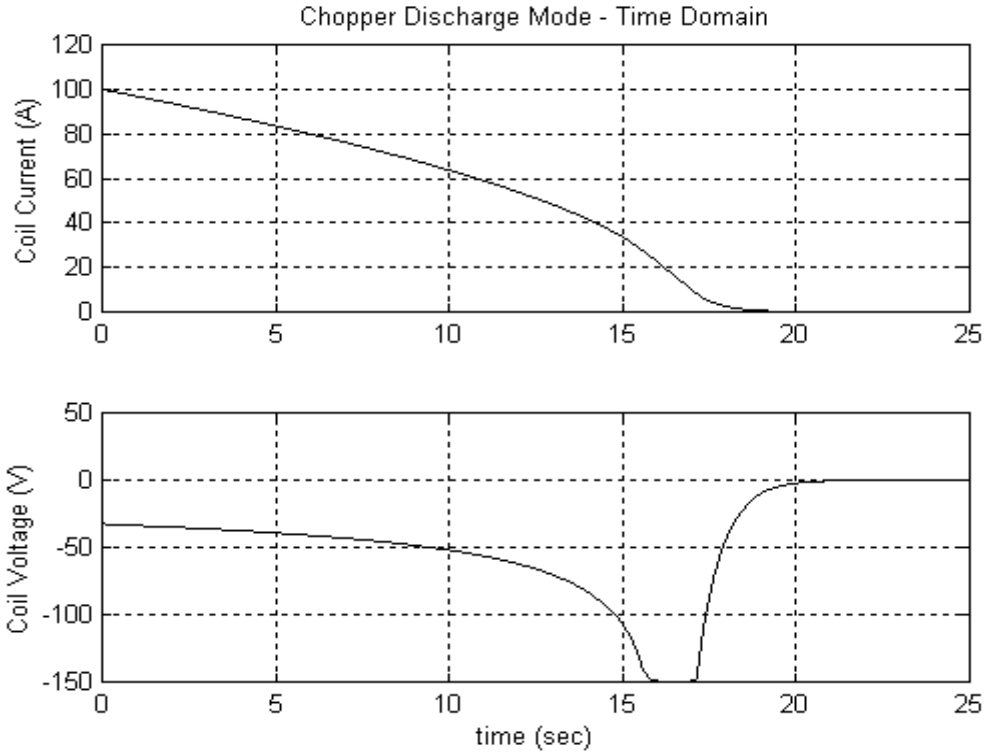


Figure 3.21 Time Domain waveform of the coil current and voltage

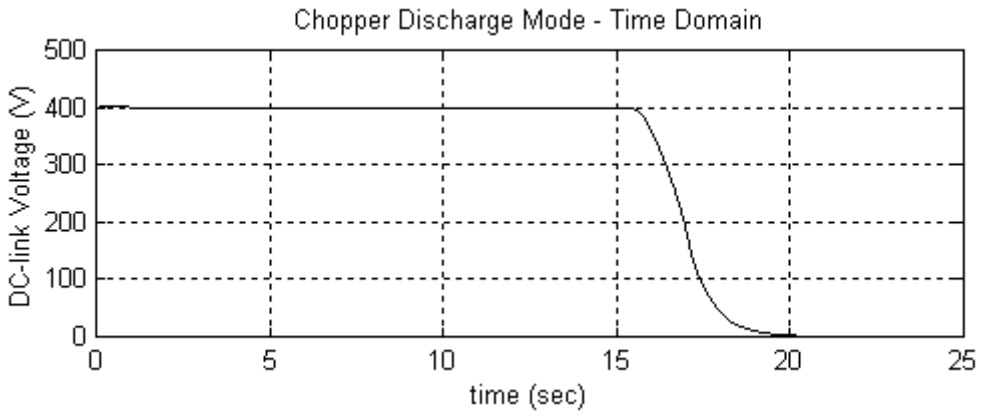


Figure 3.22 Time domain waveform of DC-link voltage

With the relatively fast dynamic response achieved with these controllers, passive component sizes and, hence, converter cost and weight can be minimized. The capacitors on the DC-link are mainly designed only for voltage ripple requirements and not for energy storage. This allows them to be greatly reduced in value and size.

3.4 Experimental Results

It should be noted that it was not possible to obtain experimental results to confirm the transfer functions presented in the previous section. Attempts to obtain these waveforms were made but results were fluctuating throughout the low frequency ranges and completely scattered in the upper frequency ranges. The cause of the inclusive results is the inability to linearize around a steady state operating point.

In the charge mode current is ramping linearly until it approaches the reference value. Theoretically at this point, during trickle-charge, a transfer function can be obtained. The chopper supplies and draws power to and from the magnet to maintain a small positive average voltage across the magnet. Essentially during this mode the

system is alternating between charge and discharge modes, in that instantaneous power flow alternates between positive and negative, but, the charge control loop is always used during this time and should allow a transfer function to be obtained. However, during this mode the voltage is very low and requires an even smaller perturbation to be injected. Difficulty in clearly measuring these low signal led to incomprehensible transfer function results.

When ever the system is in the discharge mode current is being extracted from the magnet. If this process is stopped the system immediately enters the hold mode and again is without a steady state operating point.

4 Analysis of the Voltage Source Converter

The role of the VSC is to interface the three phase AC utility lines or the three phase loads to the DC-link or chopper. As with the bi-directional chopper, the VSC also employs a three-level, ZCT topology that reduces the voltage stress, switching losses and inductor current ripple, which in turn reduces converter cost [16], [17]. Accepting these benefits, however, increases controller complexity, as the number of switching combinations increases and DC-link charge balance becomes a problem, and reduces reliability. It is controlled using a three level space vector modulation scheme. The three-level VSC circuit diagram is shown in Figure 4.1.

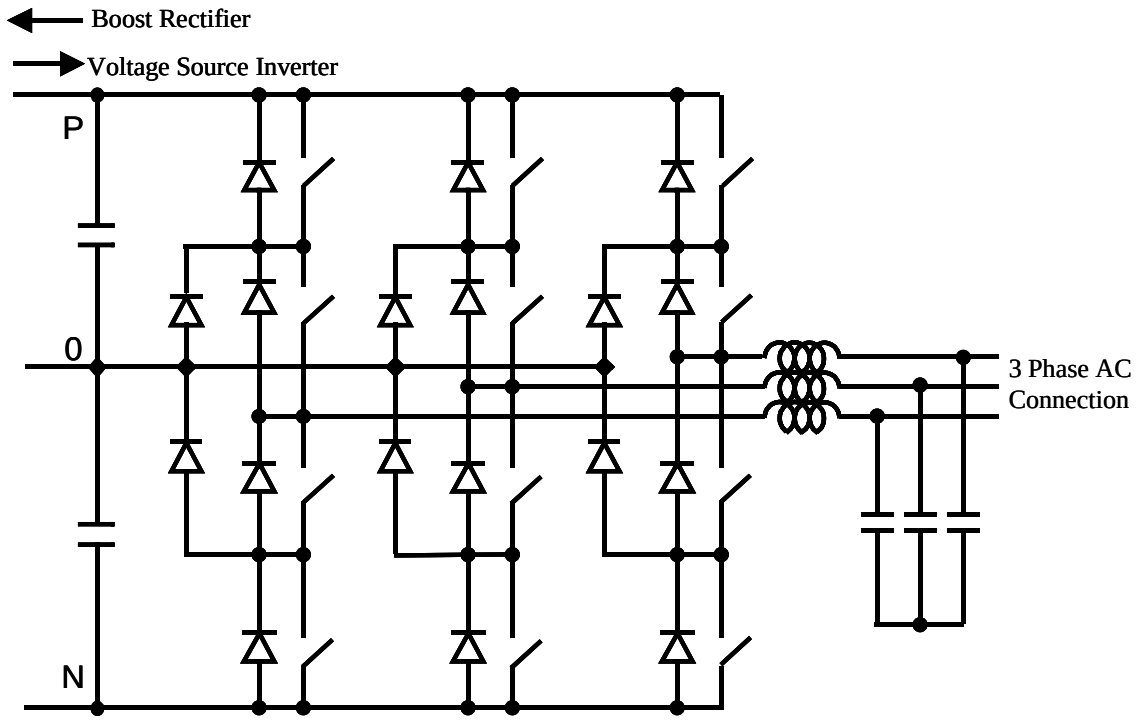


Figure 4.1 Voltage source converter

When modeling and designing the controls of this system it is desirable to work in a rotating coordinate system, thus eliminating the time varying sinusoidal functions. This rotating coordinate system is referred to as the *dqo* coordinate system. In a balanced system the '*o*' component of this coordinate system is always zero, thus, allowing it to be ignored. Conversion from *abc* coordinates to *dqo* is accomplished with a transformation matrix. This process is outlined in the following section. Eliminating the time-varying three-phase AC creates a system that is virtually DC. Therefore, working in the *dq* model simplifies modeling and control design as it is almost identical to that of a DC converter.

4.1 Boost Rectifier

When the magnet is being charged the VSC operates as a boost rectifier. It is connected to either a 208 or 480 V three-phase AC utility grid at the designated point in Figure 4.1 and maintains the required voltage on the DC-link. A system analysis and discussion of the control loops for the boost rectifier follows.

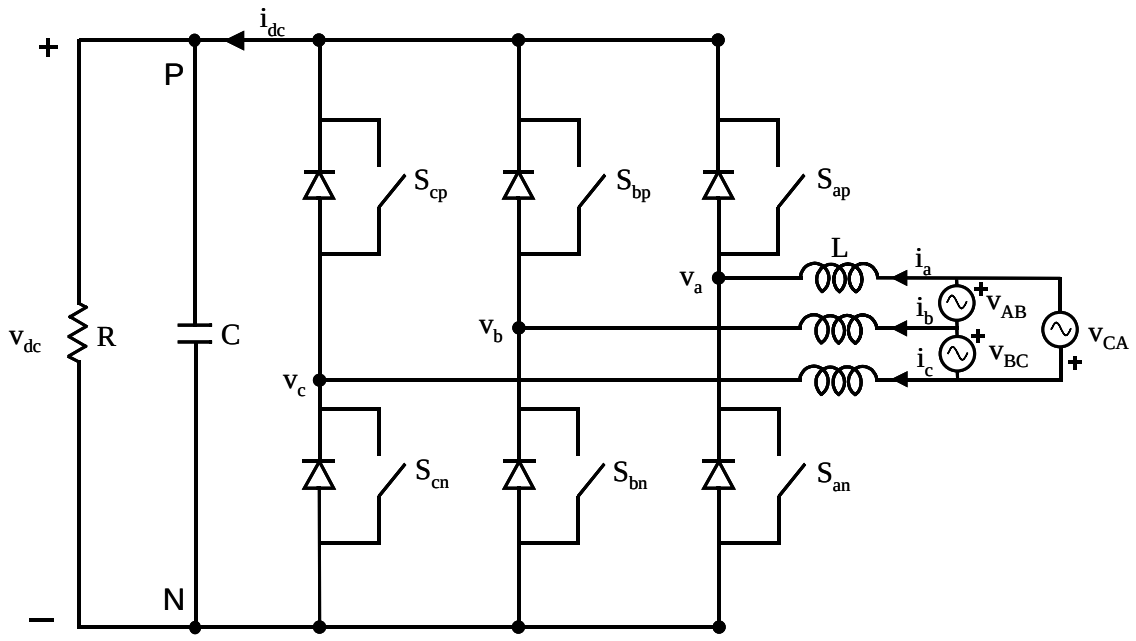


Figure 4.2 Two-level three-phase boost rectifier

4.1.1 System Analysis

The first step in the analysis of the boost rectifier is the derivation of state space equations. Figure 4.2 is a modified two-level version of Figure 4.1 to reflect the connections of the boost rectifier and voltage reference points. Average, system level operation is identical for both the three-level and two-level systems. Therefore, for simplicity derivations and models are based on the two-level converter. From Figure 4.2 the following equations are written as a representation of the circuit model,

$$\begin{bmatrix} v_{AB} \\ v_{BC} \\ v_{CA} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_a - i_b \\ i_b - i_c \\ i_c - i_a \end{bmatrix} + \begin{bmatrix} v_a - v_b \\ v_b - v_c \\ v_c - v_a \end{bmatrix}, \tag{4.1}$$

$$i_{dc} = C\frac{dv_{dc}}{dt} + \frac{v_{dc}}{R}. \tag{4.2}$$

The line-to-line currents and voltages are defined as follows in terms of phase variables,

$$\vec{i}_{l-l} = \frac{1}{3}\begin{bmatrix} i_a - i_b \\ i_b - i_c \\ i_c - i_a \end{bmatrix}, \qquad \vec{v}_{L-L} = \begin{bmatrix} v_A - v_B \\ v_B - v_C \\ v_C - v_A \end{bmatrix}, \qquad \vec{v}_{l-l} = \begin{bmatrix} v_a - v_b \\ v_b - v_c \\ v_c - v_a \end{bmatrix}.$$

Equations (4.1) and (4.2) can be rewritten using the above definitions as

$$\frac{d}{dt}\vec{i}_{l-l} = \frac{1}{3L}\vec{v}_{L-L} - \frac{1}{3L}\vec{v}_{l-l}, \tag{4.3}$$

$$\frac{dv_{dc}}{dt} = \frac{1}{C}i_{dc} - \frac{v_{dc}}{RC}. \tag{4.4}$$

Line-to-line voltages and dc current are related to the switching function, $s_{l\text{-}l,}$ v_{dc} and $i_{l\text{-}l}$ in the following manner,

$$\vec{v}_{l-l} = \vec{s}_{l-l} v_{dc},$$

$$i_{dc} = \vec{s}_{l-l}^{\,T} \vec{i}_{l-l},$$

$$\vec{s}_{l-l} = \begin{bmatrix} s_a - s_b \\ s_b - s_c \\ s_c - s_a \end{bmatrix}$$

These definitions of $v_{l\text{-}l}$ and i_{dc} are substituted into (4.3) and (4.4) to obtain

$$\frac{d}{dt}\vec{i}_{l-l} = \frac{1}{3L}\vec{v}_{L-L} - \frac{1}{3L}\vec{s}_{l-l} v_{dc}, \tag{4.5}$$

$$\frac{dv_{dc}}{dt} = \frac{1}{C}\vec{s}_{l-l}^{T}\vec{i}_{l-l} - \frac{v_{dc}}{RC}. \tag{4.6}$$

By applying an average operator to the switching model, (4.5) and (4.6), equations that represent the average model are obtained,

$$\frac{d}{dt}\bar{\vec{i}}_{l-l} = \frac{1}{3L}\bar{\vec{v}}_{L-L} - \frac{1}{3L}\vec{d}_{l-l}\bar{v}_{dc} \tag{4.7}$$

$$\frac{d\bar{v}_{dc}}{dt} = \frac{1}{C}\vec{d}_{l-l}^{T}\bar{\vec{i}}_{l-l} - \frac{\bar{v}_{dc}}{RC}. \tag{4.8}$$

Using (4.7) and (4.8), the *dq* model in phase variables is developed.

4.1.1.1 D-Q Model in Phase Variables

The *dq* models of three-phase systems are normally derived using the line-to-line variables. This is easier as the line-to-line voltage is directly related to the DC-link voltage and switching function. However, in the SMES PCS hardware, the controller performs all its calculations and manipulations using phase variables. Therefore, to insure an accurate simulation that represented proper gain and scaling factors, the *dq* model needed to be developed using phase variables.

The two equations that describe the boost rectifier, in *abc* line-to-line coordinates, are given in (4.7) and (4.8). Based on the earlier definition the relationship of phase variables to line-to-line variables can be written in the form,

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}$$

$$\begin{bmatrix} i_{ab} \\ i_{bc} \\ i_{ca} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$

$$\begin{bmatrix} d_{ab} \\ d_{bc} \\ d_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix}$$

We substitute the line-to-line variables in (4.7) and (4.8) by their respective phase equivalent to obtain the state equations in phase variables.

$$\frac{d}{dt} \frac{1}{3} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \frac{1}{3L} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} - \frac{1}{3L} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} v_{dc} \tag{4.9}$$

$$\frac{dv_{dc}}{dt} = \frac{1}{C} \left[\begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} \right]^T \frac{1}{3} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} - \frac{v_{dc}}{RC} \tag{4.10}$$

Equation (4.9) is considered first. It is simplified to obtain,

$$L \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} - \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} v_{dc}$$

This can then be separated into the *a*, *b* and *c* phase equations and multiplied by 1, $e^{j\frac{2\pi}{3}}$ and $e^{j\frac{4\pi}{3}}$, respectively, in order to transform the system from *abc* coordinates to $\alpha\beta$.

$$L\frac{di_a}{dt} = v_a - d_a v_{dc}$$
$$e^{j\frac{2\pi}{3}} L\frac{di_b}{dt} = e^{j\frac{2\pi}{3}} v_b - e^{j\frac{2\pi}{3}} d_b v_{dc}$$
$$e^{j\frac{4\pi}{3}} L\frac{di_c}{dt} = e^{j\frac{4\pi}{3}} v_c - e^{j\frac{4\pi}{3}} d_c v_{dc}$$

Combining these equations results in the following,

$$L\frac{d}{dt}\left[\frac{2}{3}\left(i_a + e^{j\frac{2\pi}{3}} i_b + e^{j\frac{4\pi}{3}} i_c\right)\right] = \frac{2}{3}\left(v_a + e^{j\frac{2\pi}{3}} v_b + e^{j\frac{4\pi}{3}} v_c\right) - \frac{2}{3}\left(d_a + e^{j\frac{2\pi}{3}} d_b + e^{j\frac{4\pi}{3}} d_c\right) v_{dc} \quad (4$$

Equation (4.11) is then written in stationary αβ coordinates.

$$L\frac{d}{dt}\left[i_\alpha + j i_\beta\right] = v_\alpha + j v_\beta - \left(d_\alpha + j d_\alpha\right) v_{dc}$$

To obtain the system model in rotating dq coordinates the above equation is rewritten as,

$$L\frac{d}{dt}\left[\left(i_d + j i_q\right) e^{j\omega t}\right] = \left(v_d + j v_q\right) e^{j\omega t} - \left(d_d + j d_q\right) e^{j\omega t} v_{dc}$$

$$L\frac{d}{dt}\left[\left(i_d + j i_q\right)\right] e^{j\omega t} + L\left(i_d + j i_q\right)\frac{d}{dt}\left(e^{j\omega t}\right) = \left(v_d + j v_q\right) e^{j\omega t} - \left(d_d + j d_q\right) e^{j\omega t} v_{dc}$$

$$L\frac{d}{dt}\left[\left(i_d + j i_q\right)\right] e^{j\omega t} + L\left(i_d + j i_q\right) j\omega e^{j\omega t} = \left(v_d + j v_q\right) e^{j\omega t} - \left(d_d + j d_q\right) e^{j\omega t} v_{dc}$$

$$L\frac{d}{dt}\left(i_d + ji_q\right) + L\left(i_d + ji_q\right)j\omega = \left(v_d + jv_q\right) - \left(d_d + jd_q\right)v_{dc}$$

The final equation is separated into its real and imaginary parts to obtain the d and q equations, respectively.

$$L\frac{di_d}{dt} = v_d - d_d v_{dc} + \omega L i_q \tag{4.12}$$

$$L\frac{di_q}{dt} = v_q - d_q v_{dc} - \omega L i_d \tag{4.13}$$

It should be noted that these equations are derived using complex notation. The actual transformation matrix implemented in the hardware is noninvertible. Therefore, it is easier to derive the equations using complex notation. The final outcome is the same regardless if derived using matrixes or complex notation

From the manipulation of the first state equation it can be seen that the only difference between the *dq* model derived with phase variables or line-to-line variables is the *3L* term. We now look at the second state equation, (4.10). The i_{dc} term is the only portion of the equation that is affected by the choice of phase or line-to-line variables. The DC current in phase variables is,

$$i_{dc} = \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix}^T \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}^T \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$

This equation is then simplified

$$i_{dc} = \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix}^T \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$

$$i_{dc} = \frac{1}{3} \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix}^T \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$

$$i_{dc} = \frac{1}{3} \left[T^{-1} \begin{bmatrix} d_d \\ d_q \\ d_o \end{bmatrix} \right]^T \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} T^{-1} \begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix}$$

$$i_{dc} = \frac{1}{3} \begin{bmatrix} d_d \\ d_q \\ d_o \end{bmatrix}^T \left[T^{-1} \right]^T \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} T^{-1} \begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix} \tag{4.14}$$

At this point the transformation matrix must be identified. The transformation matrix used in the actual controller software is

$$T = \frac{2}{3} \begin{bmatrix} \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ -\sin(\omega t) & -\sin\left(\omega t - \frac{2\pi}{3}\right) & -\sin\left(\omega t + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}$$

Using this transformation matrix 4.14 can further be simplified

$$i_{dc} = \begin{bmatrix} d_d \\ d_q \\ d_o \end{bmatrix}^T \begin{bmatrix} \frac{3}{2} & 0 & 0 \\ 0 & \frac{3}{2} & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_o \end{bmatrix}$$

$$i_{dc} = \frac{3}{2}\left(d_d i_d + d_q i_q\right) \tag{4.15}$$

Using equations (4.12), (4.13) and substituting equation (4.15) in equation (4.10) the final state equations of the average *dq* model in phase variables for the boost rectifier are,

$$L\frac{di_d}{dt} = v_d + \omega L i_q - d_d v_o$$

$$L\frac{di_q}{dt} = v_q - \omega L i_d - d_q v_o$$

$$C\frac{dv_c}{dt} = \frac{3}{2}\left(d_d i_d + d_q i_q\right) - \frac{v_o}{R} \tag{4.16}$$

The *dq* circuit model that corresponds to these state equations is shown in Figure 4.3.

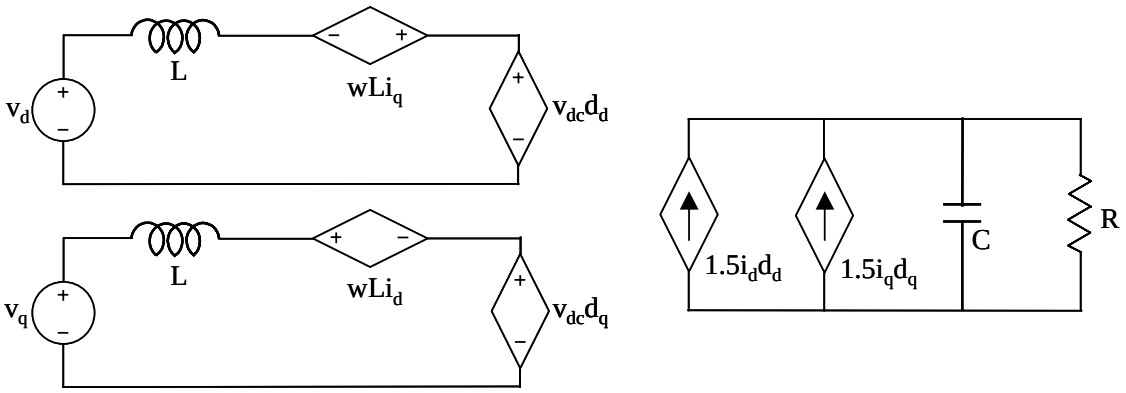


Figure 4.3 D-Q model of boost rectifier

4.1.2 Boost Rectifier Simulation Results and Control Design

The VSC has no particular control issues that are inherent to SMES applications. The VSC works between the three-phase utility or loads and the DC-link and is never directly connected to the magnet. Its control during charge and discharge transitions, however, must consider the overall state of the SMES system and the actions taken by the chopper.

The control design for the boost rectifier is based on the D-Q model developed in the prior section. The SABER schematic of this model and its control loops are given in Appendix D. There is a control loop for both the *d* channel and the *q* channel. The *d* channel control consists of two control loops, an inner current loop controlling the *d* channel current and an outer voltage loop, while the *q* channel control consists only of a current loop. If ideal power factor correction (PFC) is obtained then the current in the *q* channel is regulated to zero and the *q* channel voltage becomes whatever value is needed. A *q* channel voltage is only necessary to counter the voltage produced by the coupling term $\omega L i_d$. For nearly all converters the *q* and *d* channel control loops are the same,

although there is no voltage loop on the *q* channel.

The design process begins by looking at the plant transfer function, duty cycle to inductor current. It is this transfer function that the inner current loop design is based on. Because the *d* and *q* channels are very similar, the controller design is based only on the *d* channel and then verified in the *q* channel. The plant transfer function i_d/d_d is given in Figure 4.4. It can be seen in the three-phase boost rectifier that the initial phase angle is –180 degrees as it was in the boost mode of the DC/DC chopper. Therefore, the initial step in the design of the current compensator is the negating of the –180 degree phase shift so that the feedback loop initially provides 0 degree phase shift. In addition, the compensator incorporates an integrator to provide high DC gain and a lead-lag compensator. The zero is placed at 600 Hz, before the crossover, to reduce the phase delay while the pole is placed at 2400 Hz to provide adequate gain margin while having minimal effect of the phase delay. The transfer functions of the current compensator are shown in Figure 4.5. The inner current loop achieved a bandwidth of approximately 950 Hz. The current loop-gain transfer function can be seen in Figure 4.6.

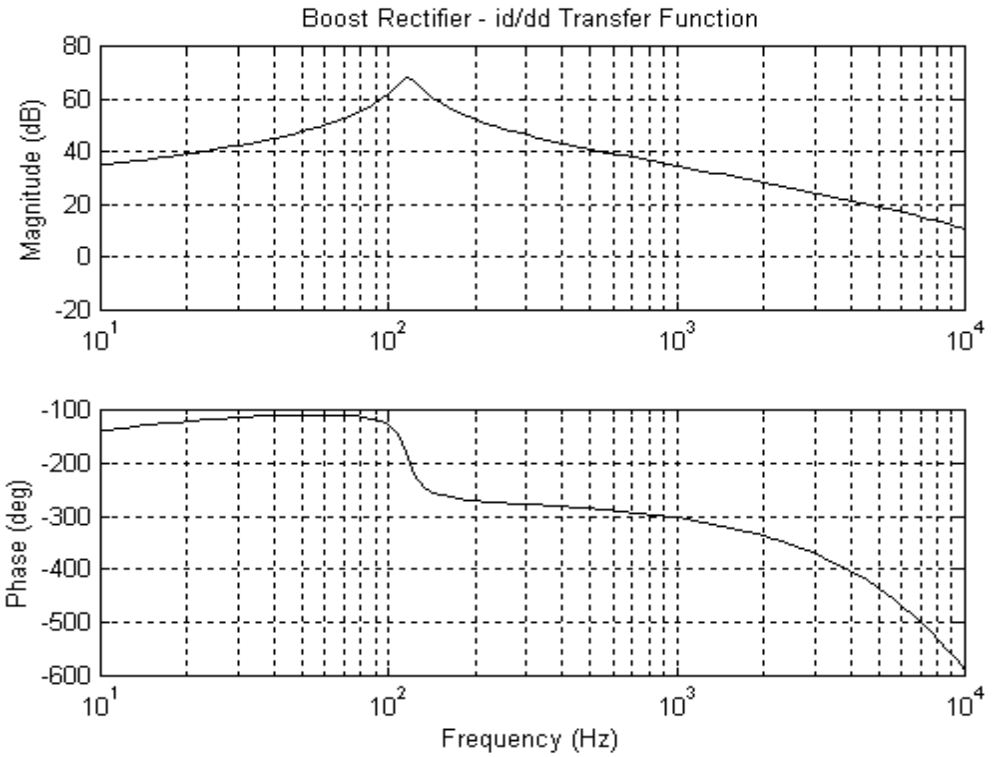


Figure 4.4 d channel duty cycle to d channel current transfer function

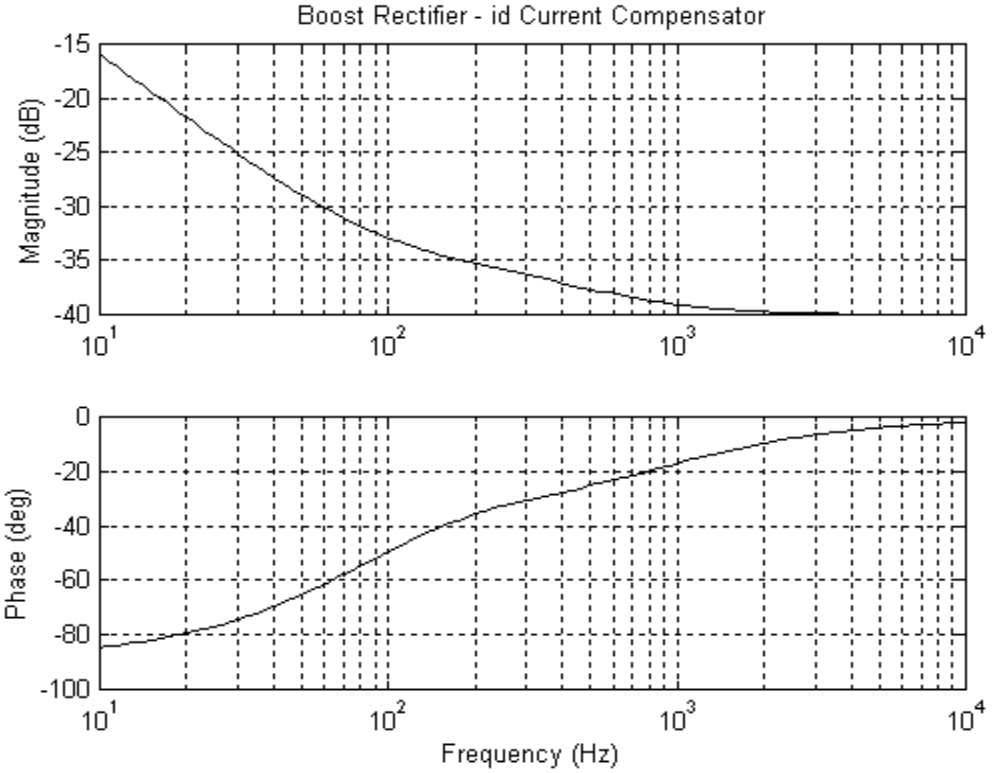


Figure 4.5 d and q channel current compensator

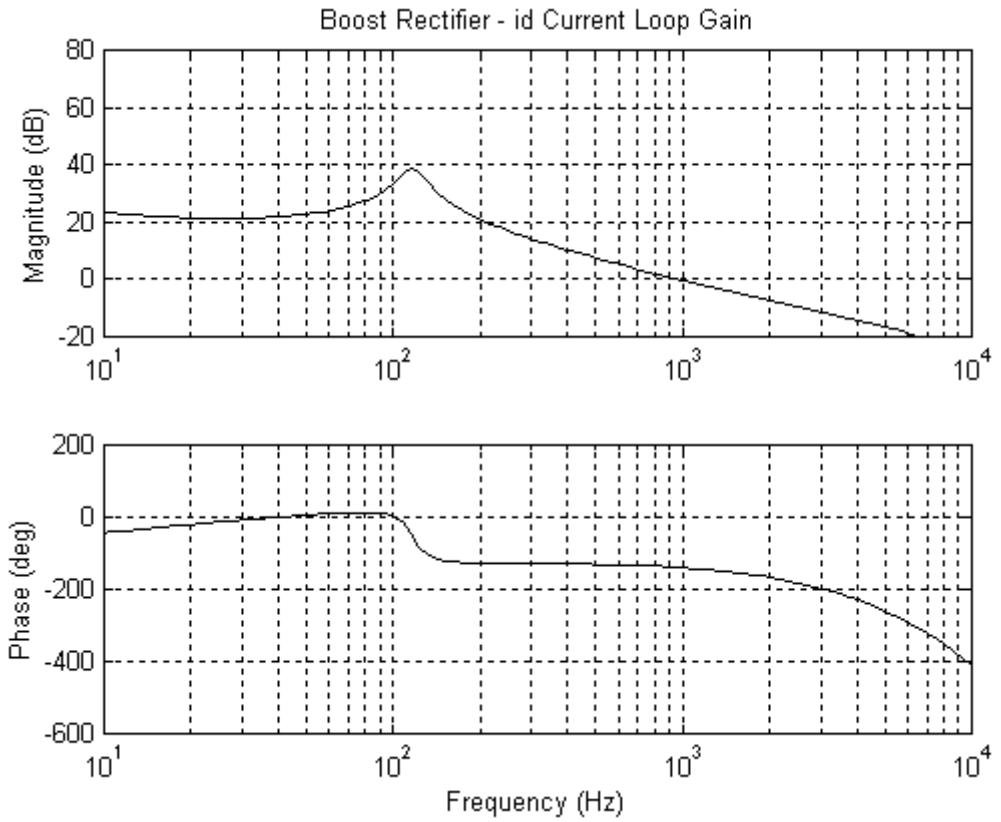


Figure 4.6 d channel current loop gain

The boost rectifier requires a voltage loop for the d channel. This voltage loop is to regulate the DC-link voltage to which the chopper is connected. The voltage loop compensator contains a proportional-integral, a lead-lag and a lag compensator. The compensator transfer function is shown in Figure 4.7. The transfer function of the overall loop-gain of the boost rectifier is given in Figure 4.8. The controller achieved a bandwidth of nearly 400 Hz.

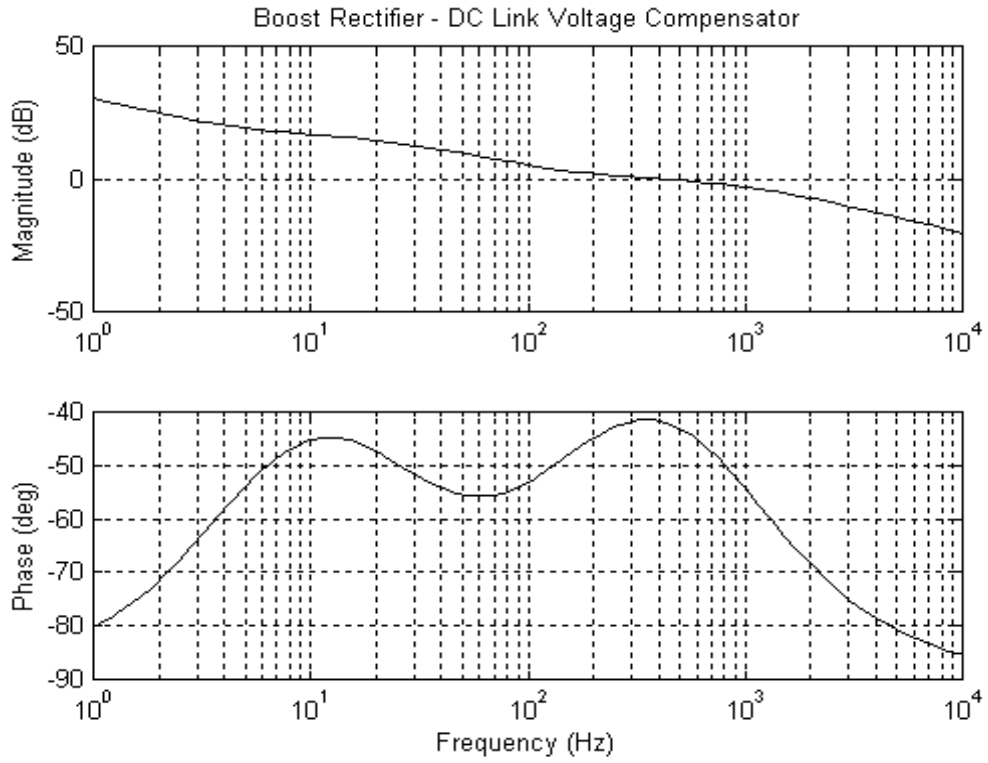


Figure 4.7 Boost rectifier DC-link voltage compensator

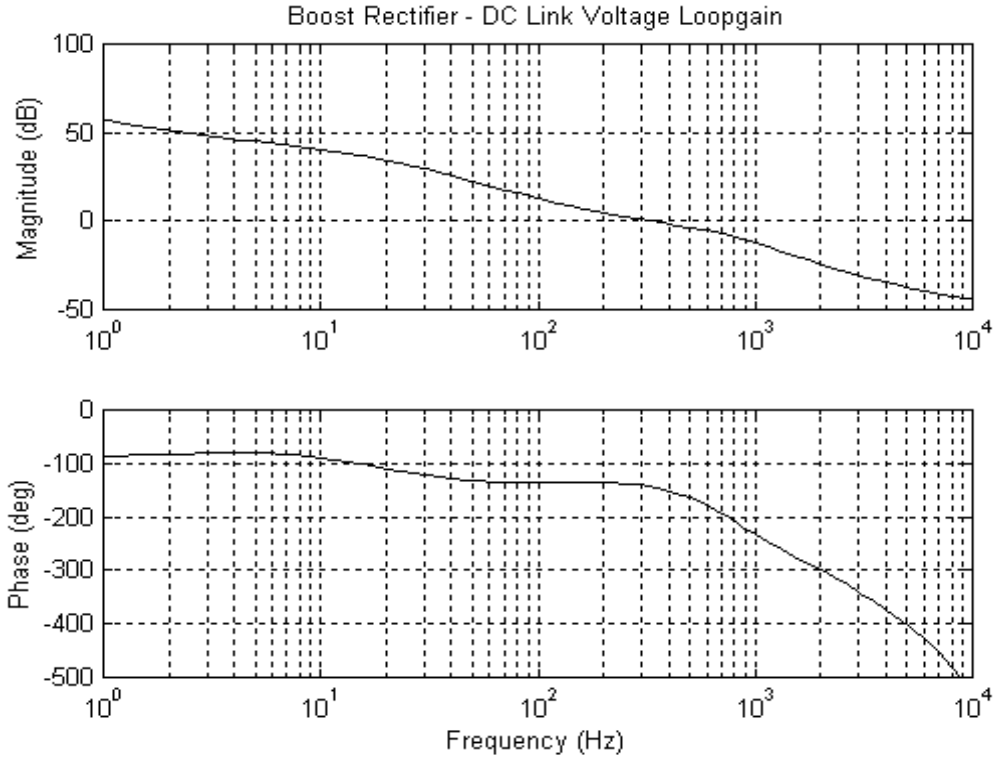


Figure 4.8 Boost rectifier DC-link voltage loop-gain

4.1.3 Boost Rectifier Experimental Results

In contrast to the chopper, transfer functions of the VSC are possible as steady state operating points can be obtained in any condition. Transfer function measurements were obtained experimentally to verify the accuracy of the model developed and simulated in the previous sections. Presented first is the plant transfer function, i_d/d_d, shown in Figure 4.9.

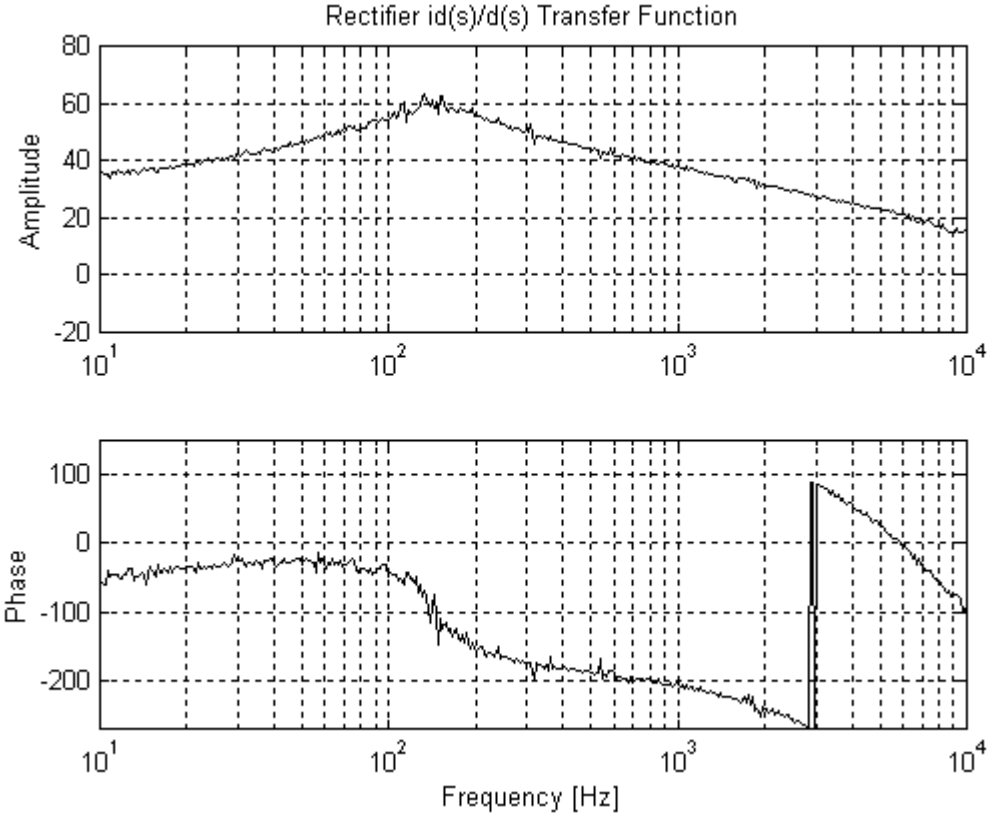


Figure 4.9 Experimental waveform of i_d/d_d transfer function.

By comparing the simulated transfer function in Figure 4.4 with the experimental transfer function in Figure 4.9 it is seen that the simulation is a very accurate prediction of the actual converter behavior. The overall shape of the transfer function is comparable. The

simulated transfer function has slightly higher peaking. This is understandable as the actual system would have parasitic resistances that add damping and are not accounted for in the simulation.

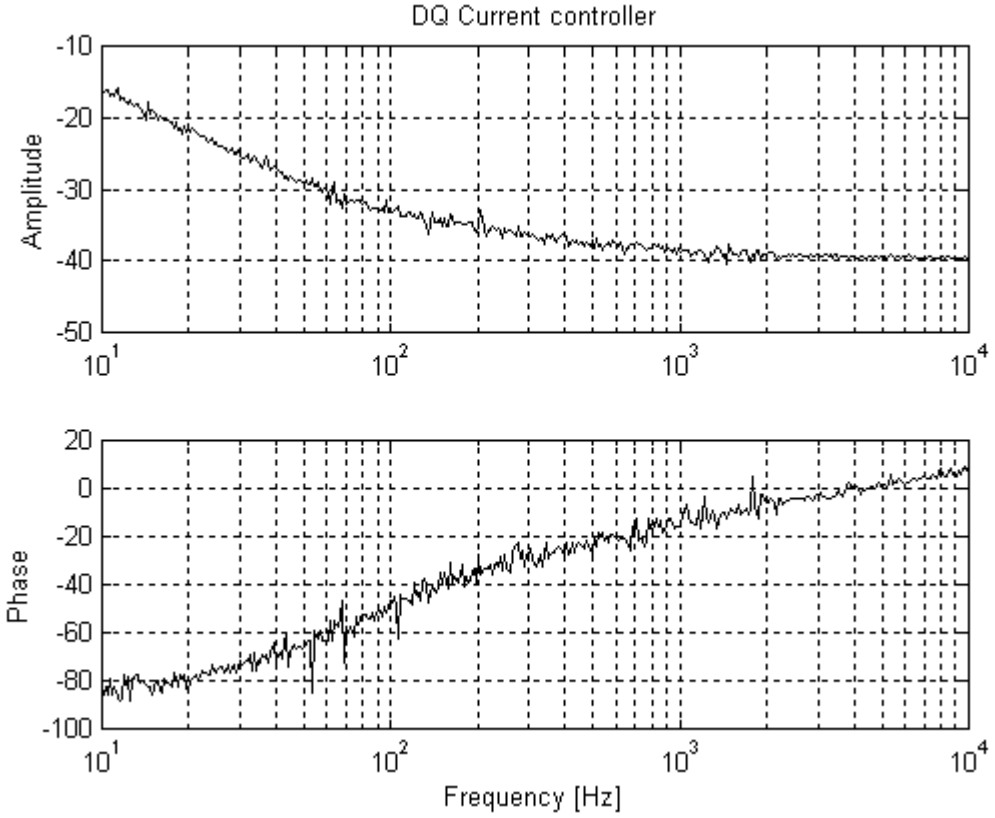


Figure 4.10 Current loop compensator

As is expected the experimental and simulated compensator transfer functions, given in Figures 4.5 and 4.10, respectively, are comparable. This is a basic control model and no discrepancy exists.

Given that the plant transfer function and the compensator transfer function are fairly accurate matches, it should follow that the simulated *d* channel loop-gain transfer functions also correctly predict that of the experimental waveforms. The experimental *d*

channel loop gain transfer function is given in Figure 4.11. Comparing this with the simulated results in Figure 4.6 this premise is confirmed.

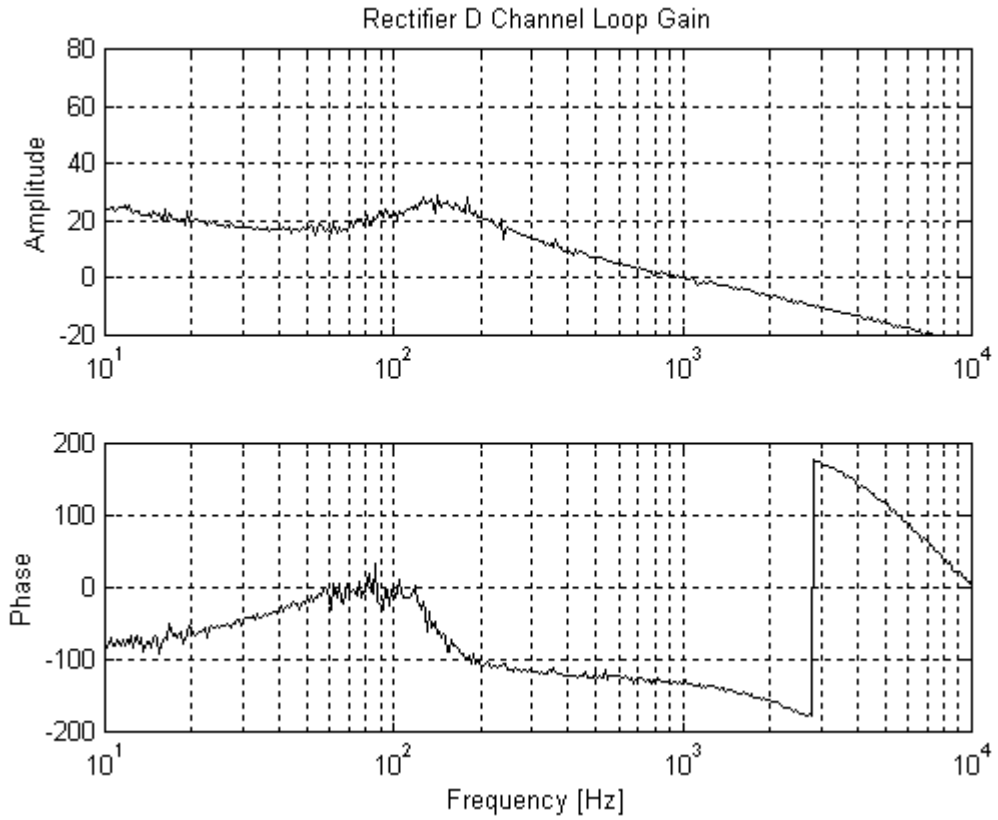


Figure 4.11 Boost rectifier D channel current loop gain.

An effort was undertaken to provide a detailed model of the SMES system and obtain simulations that accurately predicted system behavior. These detailed simulations confirm the validity of the model and provide a reliable and easy means of adjusting system parameters to optimize controller performance.

4.2 Voltage Source Inverter

When power is being drawn from the magnet the VSC is operating as a voltage source inverter (VSI). Figure 4.12 shows the VSC with specific connections to illustrate

the operation of the VSI. In this mode the chopper would be drawing power from the magnet and maintaining the voltage on the DC-link. The VSI would take power from the DC-link in order to power the three-phase load. In this particular schematic resistors are used as the load on the three-phase AC output.

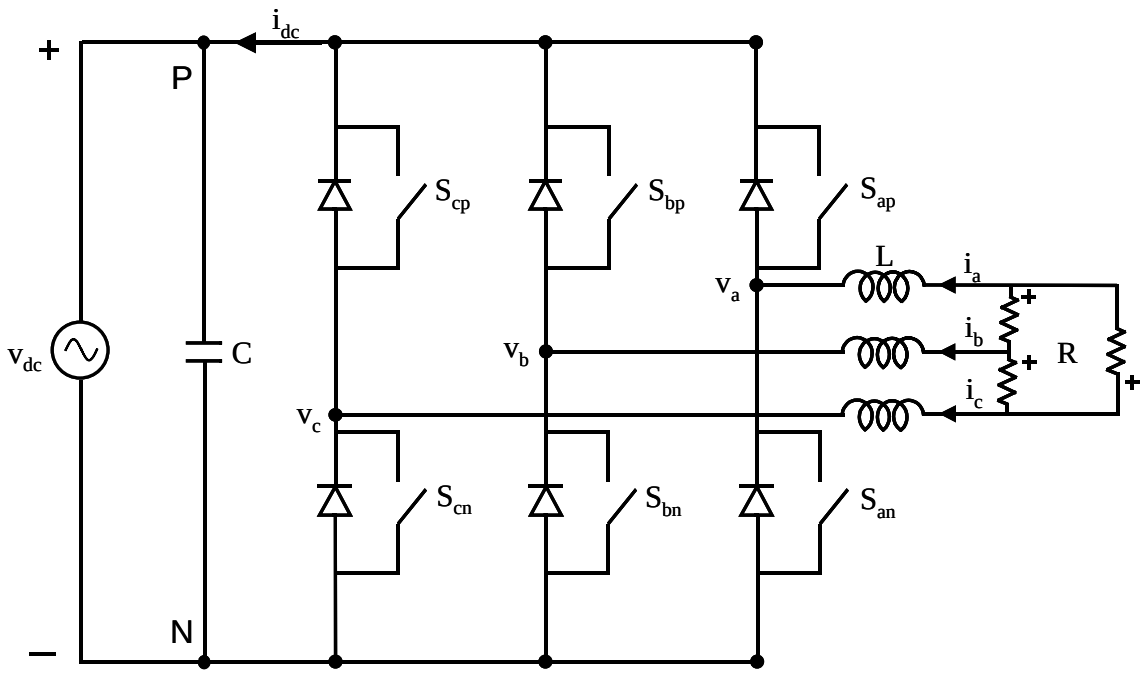


Figure 4.12 VSC configured as a voltage source inverter.

4.2.1 D-Q Model and System Analysis

The VSI has no output ac capacitors, therefore, the VSI model is practically the same as that of the boost rectifier. Namely, the *3L* inductor term and the *3ωL* cross-coupling term in the line-to-line model lose the factor of 3 in the phase-derived model. The difference is that the current in the DC equation and the cross coupling terms change sign. The D-Q model of the VSI is given in Figure 4.13. Note that the current direction change in the DC portion of the model and the polarity of the cross coupling terms are

reversed. In addition, the reference direction of the current i_d and i_q is changed. The SABER simulations were based on this model. A simulation schematic of the VSI and its corresponding control loops is given in Appendix D.

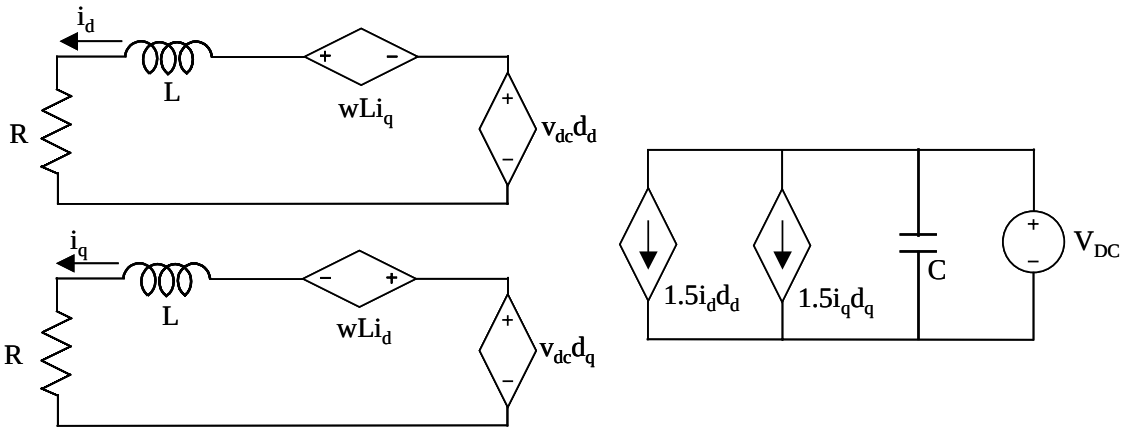


Figure 4.13 D-Q model of VSI based on phase variables

The governing state equations of the VSI are as follows,

$$L\frac{di_d}{dt} = -v_d + \omega L i_q + d_d v_o \tag{4.20}$$

$$L\frac{di_q}{dt} = -v_q - \omega L i_d + d_q v_o \tag{4.21}$$

$$i_{dc} = \frac{3}{2}\left(d_d i_d + d_q i_q\right) \tag{4.22}$$

Equation (4.22) is different from that of the boost rectifier. For the derivation of the model, a DC voltage source is placed on the DC-link. This in effect eliminates the effects of the capacitor and reduces the order of the system.

4.2.2 VSI Simulation Results and Control Design

It may be required that the VSC has separate *d* and *q* channel control loops for the boost rectifier and VSI modes of operation. However, for the system developed, the same control loops were possible. This allows a reduction in controller complexity and reduces the resources required by the controller hardware. One application of the VSI is to be capable of supplying power to the utility grid. This objective is accomplished by regulating the three-phase output current. Therefore, when the VSC moves from the boost rectifier mode to the VSI mode it drops the voltage loop on the d channel.

The current compensator for the VSI is the same compensator used in the boost rectifier current loop and its transfer function is provided in Figure 4.5. It consists of an integrator and lead-lag compensator. The i_d/d_d plant transfer function to be compensated is shown in Figure 4.15 and the overall current loop gain is shown in Figure 4.16.

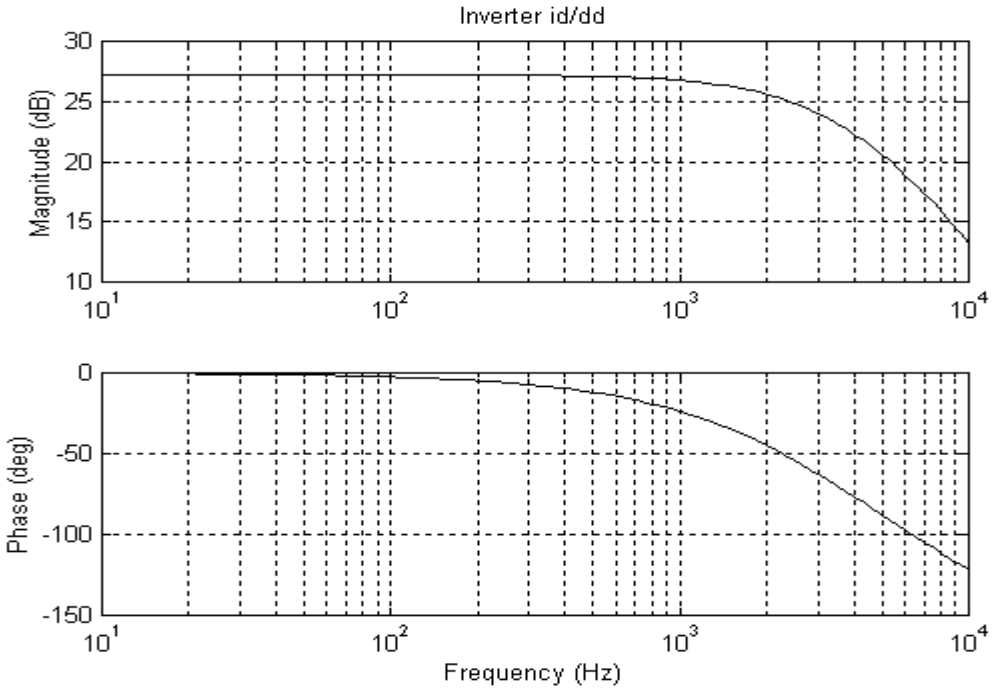


Figure 4.14 Voltage source inverter plant transfer function.

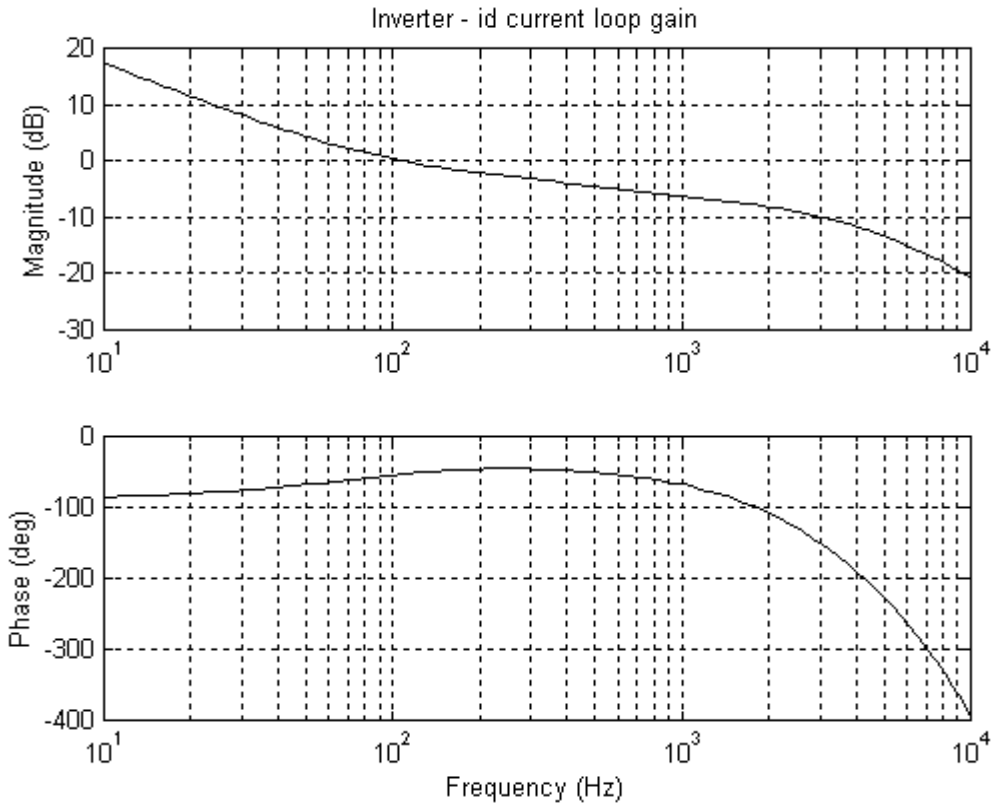


Figure 4.15 Voltage source inverter current loop gain.

4.2.3 VSI Experimental Results

Transfer functions of the real hardware were obtained so that the simulation model and waveforms could be verified. The current compensator is a straight forward design and little discrepancy was expected. Comparing Figures 4.14 and 4.17 this is proven to be the case. Figures 4.15 and 4.18, the plant transfer function i_d/d_d, also match very well. The initial magnitude value is the same with an insignificant difference, approximately 2 dB, in final magnitude. The current loop gain is the combined transfer function of the compensator and plant transfer functions. Therefore, the accuracy of the simulated loop-gain transfer function should follow that of the compensator and plant

transfer functions. The simulated and experimental id current loop gain transfer functions are given on Figures 4.16 and 4.19, respectively.

From these several experimental waveforms it is shown that the SABER model of the VSI accurately models the actual hardware setup. This model in conjunction with the three-level bi-directional chopper model will be used to detail system transitions.

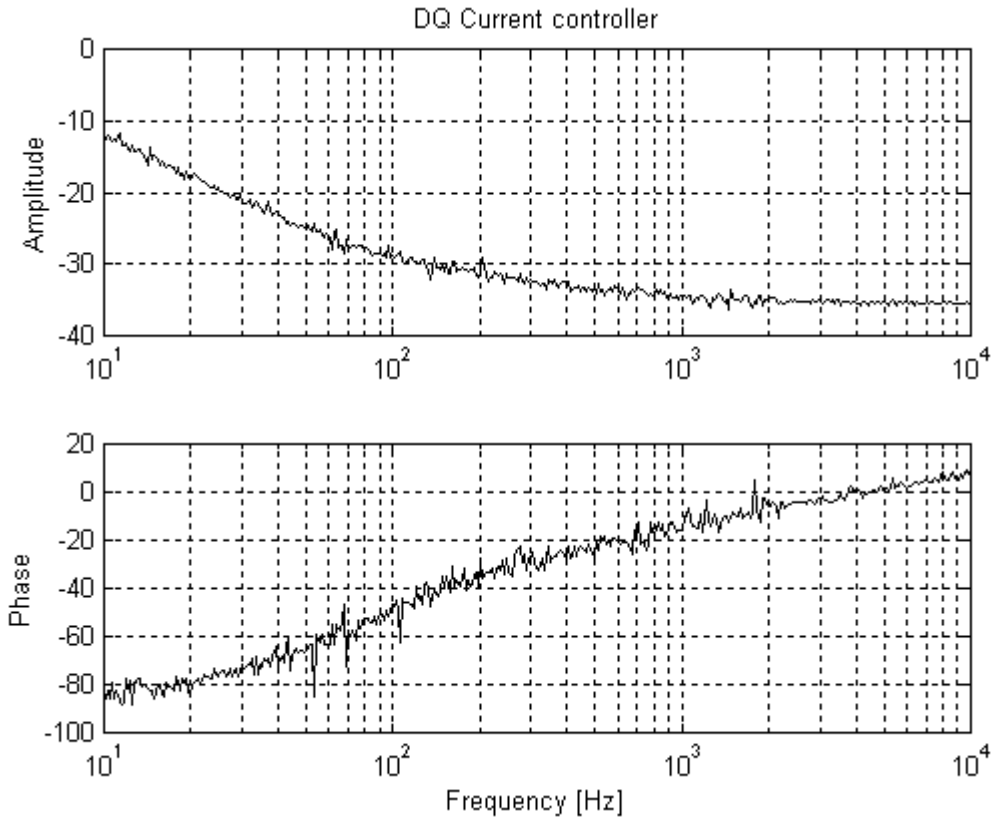


Figure 4.16 Utility inverter experimental current compensator

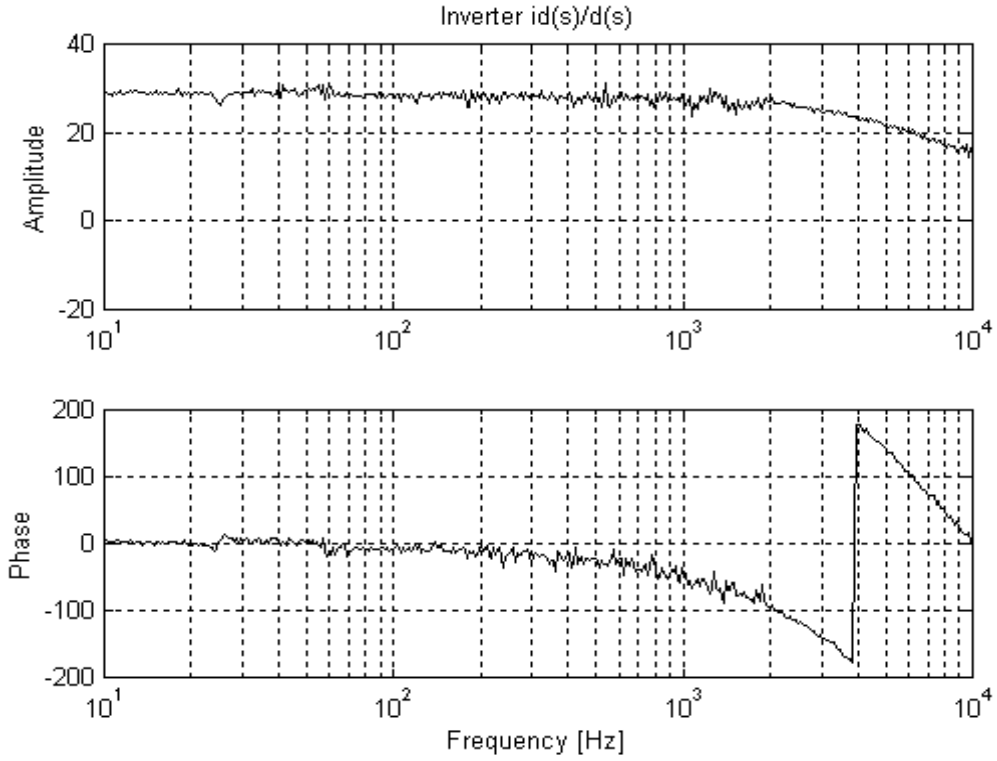


Figure 4.17 Utility inverter experimental plant transfer function

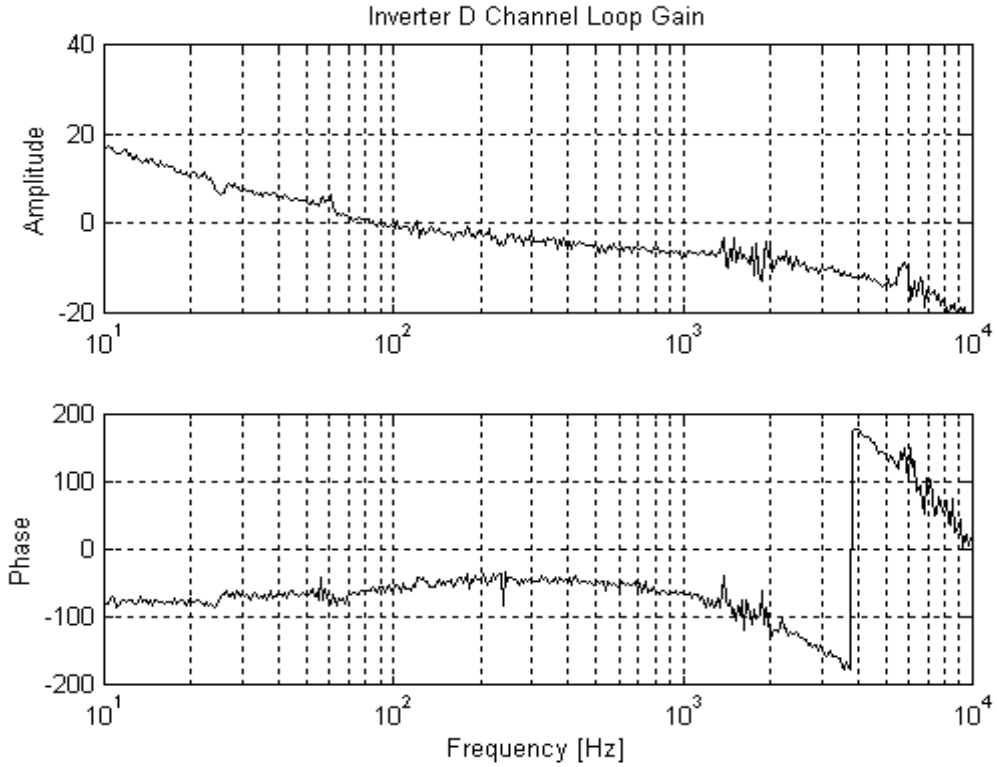


Figure 4.18 Utility inverter experimental d channel loop gain

5 SMES PCS System Transition Analysis

The inability to properly characterize and detail the system during mode transitions led to an effort to develop the models of the chopper and VSC discussed in the previous two chapters. The objective was to accurately simulate both the chopper and VSC so that analysis of the complete system, with the SMES coil, could be conducted and in turn accomplish seamless system transitions and operation.

5.1 Transition Issues

Initial tests with the SMES magnet revealed problems with several different charge/discharge mode transitions. Recall that in the charge mode the VSC is maintaining the DC link by drawing power from the utility. As the system transitions from hold (essentially a charge mode) to discharge, regulation of the DC link is dropped by the VSC and then picked up by the chopper. These types of transitions were not initially performed completely by the integrated system controller. It is this lack of system integration, hence, coordinated control, that would lead to significant drops in the DC-link and uncontrollable and unpredictable transient behavior.

5.2 Waveform Evaluation

Simulation results of an initial mode transition scenario are given in Figure 5.1 - 5.3. Coil current and coil voltage waveforms are given in Figure 5.1. The DC-link current and voltage are given in Figure 5.2 and the *d* channel load voltage in the VSI is shown in Figure 5.3. A detailed look at these waveforms reveals several problems during mode transitions. These following simulation and experimental results are based on a

tests completed with a 12 H LTS magnet provided by NSWC. Charging and discharging rates of 100V were obtained with current as high as 100A.

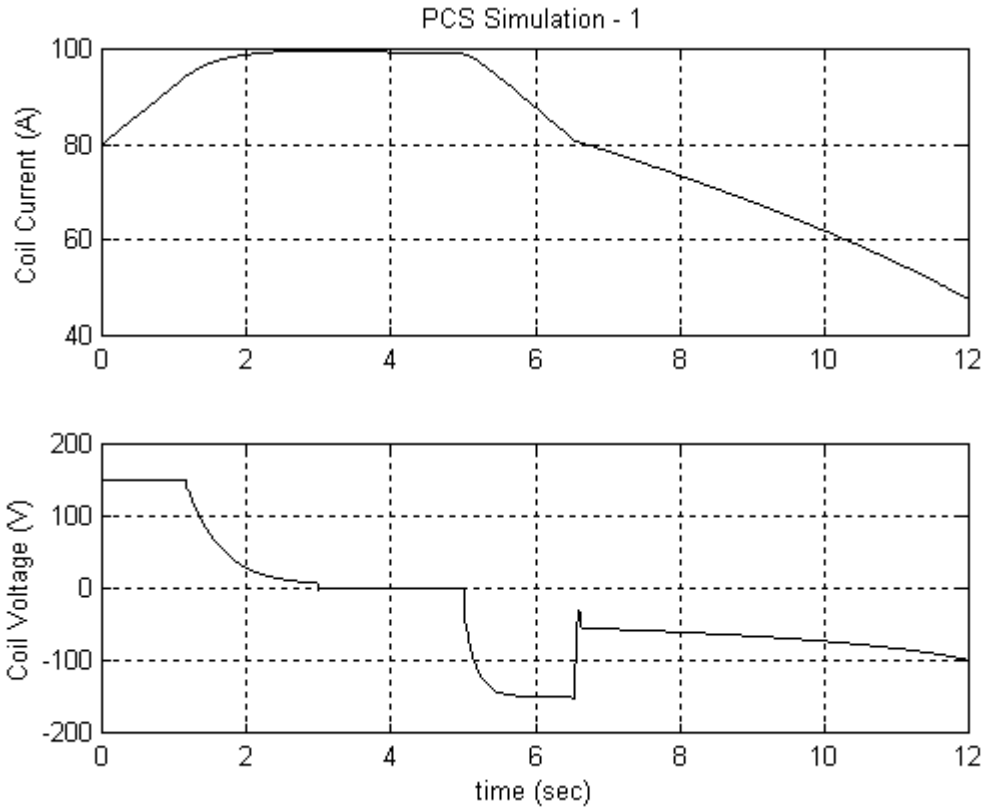


Figure 5.1 Coil current and voltage in a charge/discharge transition

In the first few seconds of the waveforms the system is in the charge mode. The VSC is operating as a boost rectifier, maintaining the DC-link and the chopper is in the buck mode charging the coil with a maximum voltage of 150 V. (Actual lab tests charged the coil with approximately 60 V. A 150 V limit was used in simulations to shorten simulation time.) Current in the coil rises linearly until it approaches 100 A at which point the voltage across the coil begins to tail off. In conjunction with this, the current through the DC-link decreases and falls to zero as the power required to maintain

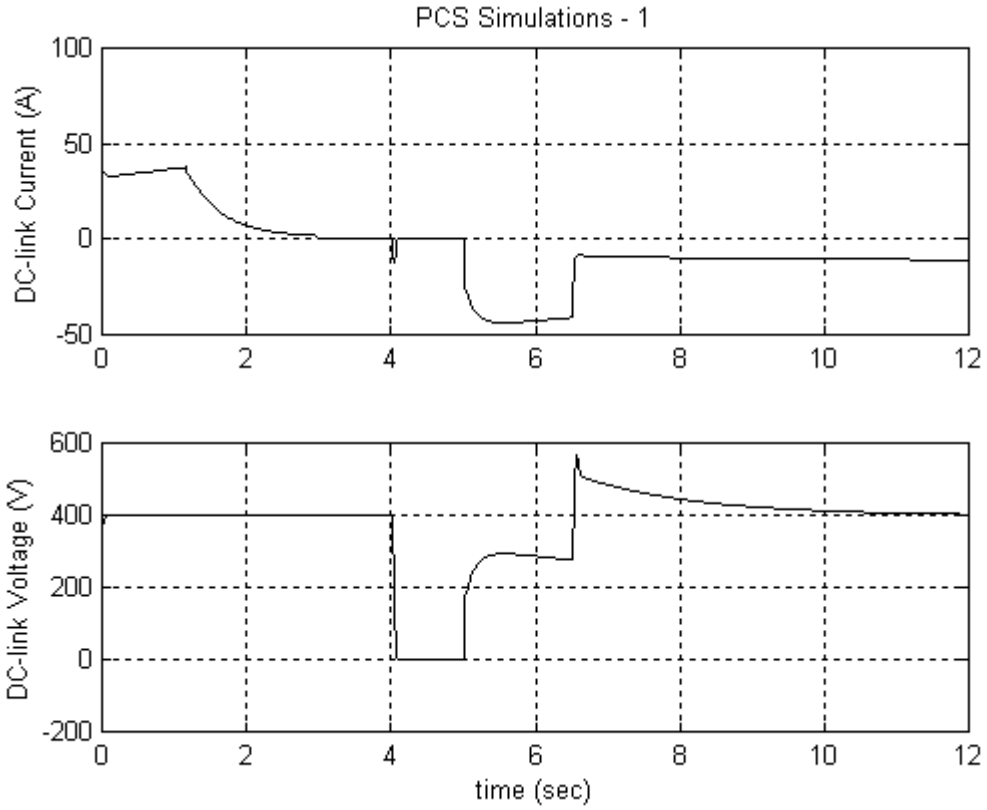


Figure 5.2 DC-link current and voltage in a charge/discharge transition

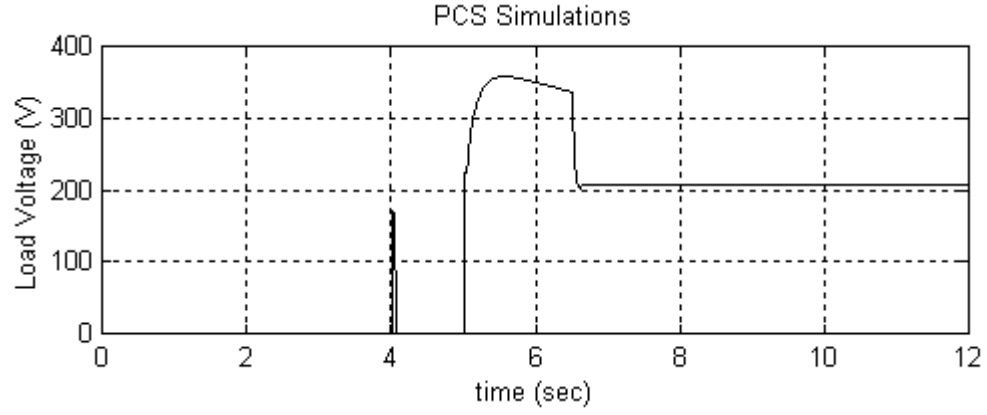


Figure 5.3 D channel load voltage in a charge/discharge transition

coil current, hold mode, is minimal. At 3 s the coil and DC-link voltage have a small but quick transient to zero. It is at this point that the VSC drops the DC-link voltage regulation and the controller for the chopper begins to freewheel the current. At 4 s the system controller sends the signal to the VSC to begin operation as an inverter. A small negative glitch in the DC-link current appears and the voltage drops to zero. This is because the VSC attempted to provide power to the load and consequently drained the DC-link capacitance of its energy. As a result, approximately 175 V is present across the d channel load resistor for a short duration.

The VSC is now attempting to provide the proper three-phase current to the load without any power being supplied by the chopper. This causes the VSC controller error signal to be positive and constant which continuously increases the output of the integrator in the controller. This continues for a period of until the chopper is switched to operation in the buck mode. Power is then supplied to the DC-link, the VSC drives current through the load and the integrator attempts to pull out of saturation. The period of time that the integrator is saturated can be seen in the waveforms. It is between 5 s and approximately 6.5 s. With the integrator in saturation the load current is regulated to a value much higher then its reference. During the saturation period the coil voltage is maximized and full power is being transferred to the DC-link. This in turn causes the DC-link voltage to drop as it is overloaded and it forces excessive current through the three-phase load. This creates both an over-voltage and over-current situation with the load. When the VSC controller recovers, it snaps back and causes an overshoot on the DC-link of nearly 200 V. It then takes several seconds until the chopper regulator returns

the DC-link to its reference value.

The above scenario not only causes severe and potentially damaging transients but it also results in a large amount of lost energy. While the controller is saturated, the current in the magnet rapidly decreases. Nearly half of the coil's stored energy is used during this time.

5.3 Transition Solutions

Figures 5.1 - 5.3 illustrate several problems with the mode transitions. First, timing is an important aspect and the sequence in which tasks are completed is of utmost importance. These waveforms also point to potential problems with setting initial conditions as the controllers attempt to start regulating after a mode transition.

The first step in correcting these issues was to link both the chopper and VSC controllers to the system controller. This enables precise and automatic timing of the commands sent to both controllers and eliminates the need for a computer to be connected to the chopper controller. The system controller sends the signal to the chopper and the chopper relays that signal to the VSC. This allows the two controllers to have a means of communicating and precisely controlling the timing of events. There was an effort to increase the bandwidth of the controllers so that they could respond more quickly to mode changes. However, for the demonstration, utility/load connection changes are accomplished with relatively slow mechanical contactors and dead times must be introduced in the controllers to account for this. Therefore, for this particular setup only, an increased bandwidth would have little effect on the transition waveforms.

Sending control signals to both the chopper and VSC helped eliminate some transition problems and made proper sequencing of events easier. However, these simulations point to a possible problem with "hard starting" the controllers, i.e. beginning the regulation after a transition without configuring the controller initial conditions to current system values. This is the reason the VSC, in Figure 5.3, over-drives the load. A similar "hard start" situation was present in other transition scenarios.

However, the transition from hold to standby still causes the DC-link voltage to drop and go through large transients that trigger protection and periodically cause the processor in either or both the chopper and VSC to shut down. The DC-link voltage experimental waveform with these circumstances can be seen in Figure 5.4. In the hold mode the VSC is operating as a boost rectifier and maintaining the DC-link while the chopper maintains the coil current. As the mode transitions to standby, the VSC first drops the DC-link voltage regulation and then the chopper attempts to regulate it by drawing a small amount of

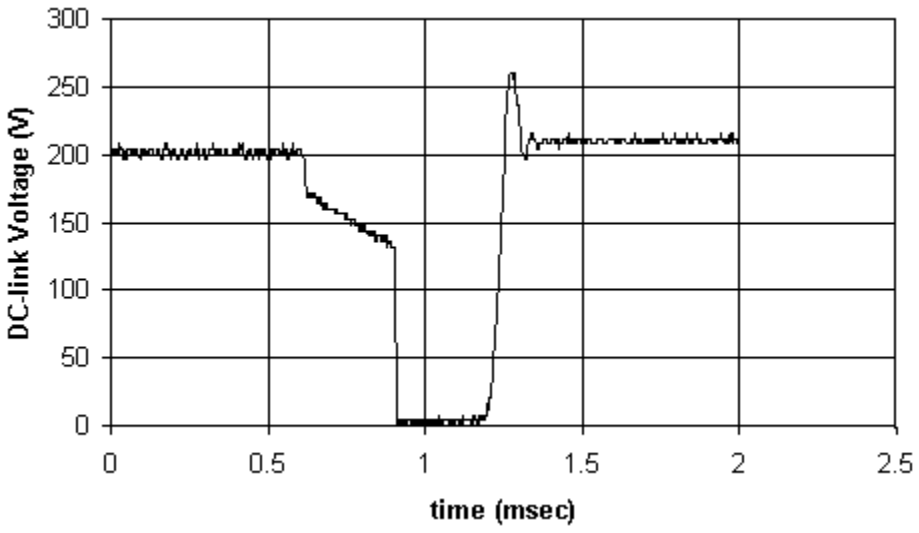


Figure 5.4 Experimental waveform of a hold – standby transition with incorrect initial condition

power from the magnet. However, when the chopper begins this regulation, the initial condition is zero. Hence, the chopper, for a short time, attempts to charge the magnet, but at this point, the only energy available is that stored in the DC-link capacitors. This error immediately discharges the DC-link before the controller corrects itself. The controller begins to regulate the DC-link and the voltage quickly returns to the reference with a substantial over-shoot. Disabling the bi-directional operation of the chopper during this time solved the problem, in turn preventing the chopper from being able to charge the magnet during the initial start in the standby mode. As a result of these tests, a soft-start operation was developed for both controllers. After each transition, the controller reference is linearly ramped to the final set value.

The simulated and experimental waveforms of a hold to standby transition of the coil voltage and DC-link voltage are shown in Figure 5.5 and 5.6, respectively. It can be seen that the simulated and experimental waveforms are basically identical. In Figure 5.5, the system starts in the hold mode and remains there until approximately 3.2 s. After this point the system controller was switched to the standby mode. At this time, the controller instructed the contactor, connecting the utility to the VSC, to be disconnected but did not send the control signal to the chopper and VSC until almost 300 ms later. The contactor disconnect occurs at approximately 200 ms. At this point the VSC continues to try and maintain the DC-link while the chopper draws power from the DC-link to maintain coil current. This is the reason for the drop in the DC-link voltage waveform between 3.2 s and 4.9 s. At 4.9 s the signal is sent to the VSC and chopper to switch modes from hold to standby. The VSC immediately transitions to standby and the

chopper adds a dead time before entering the standby mode. Initially the voltage across the magnet increases as the chopper reestablishes the DC-link. Once the DC-link voltage is restored the coil voltage resumes its steady state value.

The experimental waveforms, in Figure 5.6, basically follow the same sequence of events. The first 200 ms of the waveform, until point 1, is a result of the hold mode. At this point in the waveform a fairly large ripple is present. This ripple is approximately 40 Hz, thus ruling out switching frequency as a possible cause. It is possible that the point of discontinuity around which the chopper is transitioning between charge mode and the trickle charge causes this ripple. However, this was not investigated here in this research and explanation is not known.

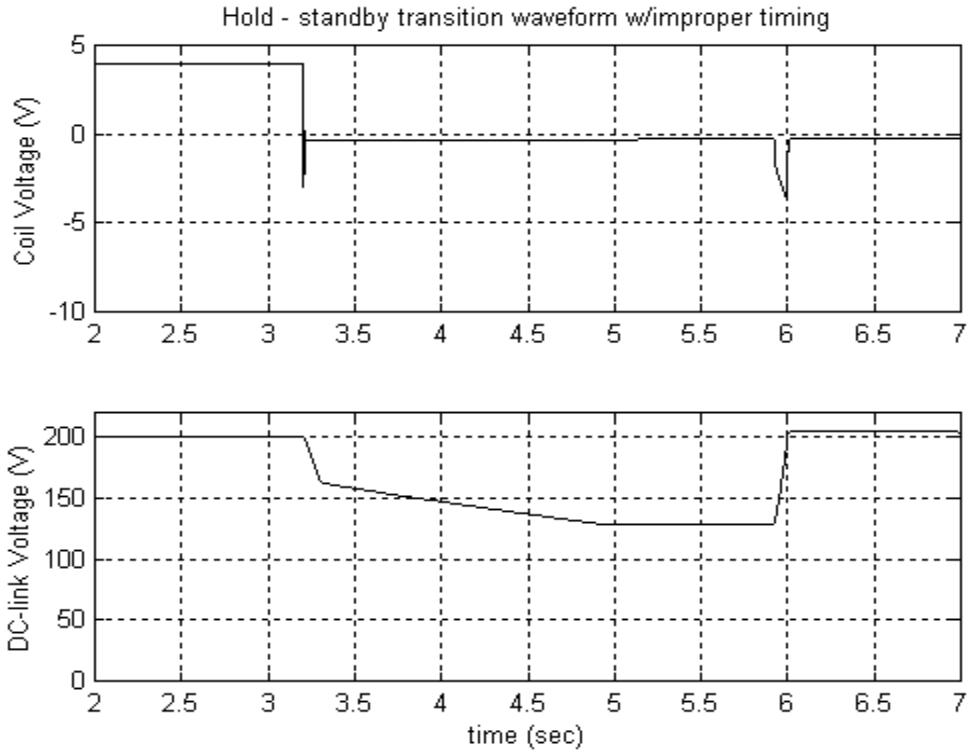


Figure 5.5 Simulated hold – standby transition waveform with improper timing

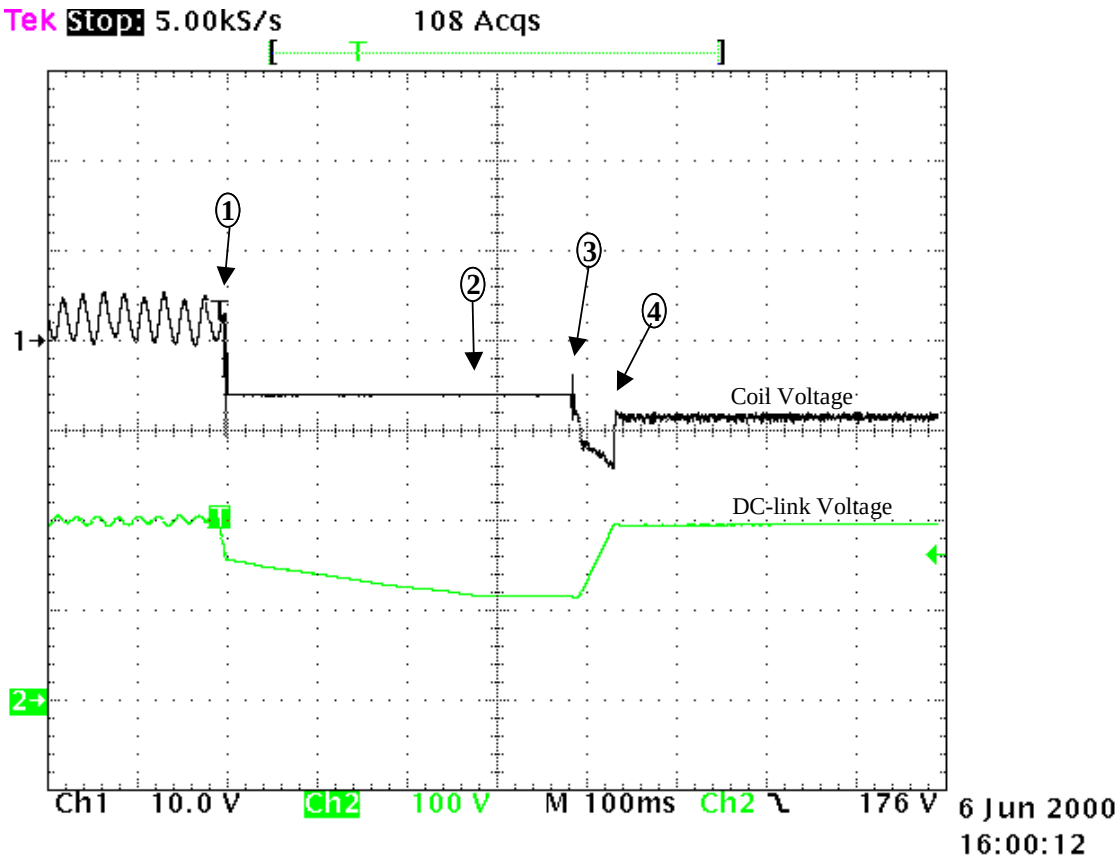


Figure 5.6 Hold – standby coil voltage and DC-link voltage transition waveforms with a drop in the DC-link voltage.

order to produce a small positive average voltage across the coil. In the experimental waveforms there is a slight discrepancy between the coil voltage before point 3 and after point 4. The coil voltage prior to the restored DC-link is due to the voltage across two diodes and two IGBTs while the current is simply freewheeling, thus compensating only

conduction losses. After the DC-link is established, the chopper is switching to maintain the DC-link voltage and the magnet must compensate for both the conduction losses and the switching losses.

Improper timing and sequence of the system controller and the contactor operation is responsible for the decrease in DC-link voltage in Figures 5.5 and 5.6. This error was corrected by sending out the standby signal to the VSC and chopper at the same time the utility contactor was disengaged. Tests were performed after this correction and the results are shown in Figure 5.7. These waveforms are of a hold – standby – discharge transition. The DC-link has no noticeable decline in voltage throughout this entire process. Until point 1 the system is in the hold mode, with an average voltage of approximately 4V, maintaining a constant coil current. At this point the command to enter the standby mode is received by the chopper and VSC and the utility contactor is enabled. Initially only the VSC transitions to standby and the chopper disables the bi-directional mode. The coil voltage drops to approximately –5 V as the coil current free-wheels. At point 2 the chopper enters the standby mode, maintaining the DC-link voltage and compensating for converter losses with the energy in the magnet. This consequently produces a voltage of approximately –8 V across the magnet. This continues for 2.4 s when the system enters the pulse mode and the coil voltage is increased to provide the needed power on the DC-link to power the lighting load. All of these transitions are accomplished with no noticeable change in DC-link voltage and no undesirable transients.

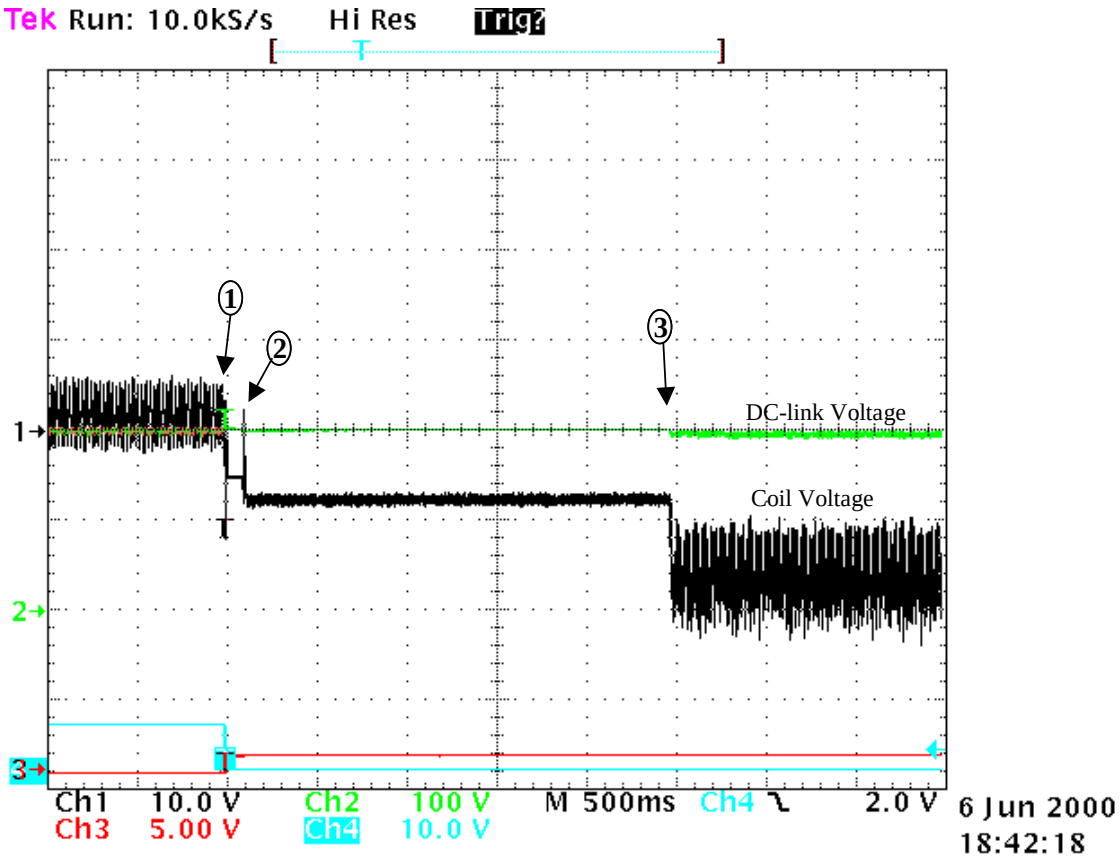


Figure 5.7 Hold – standby – discharge coil voltage and DC-link voltage transition waveforms with no drop in DC-link voltage

6 Conclusions

Successful integration of the PCS and magnet proved to be a difficult challenge. Many controller and transition details, initially not considered important, played a major roll in impeding this objective. Specifics of transition event sequencing, timing and controller initial conditions had to be carefully analyzed and implemented in the system controller.

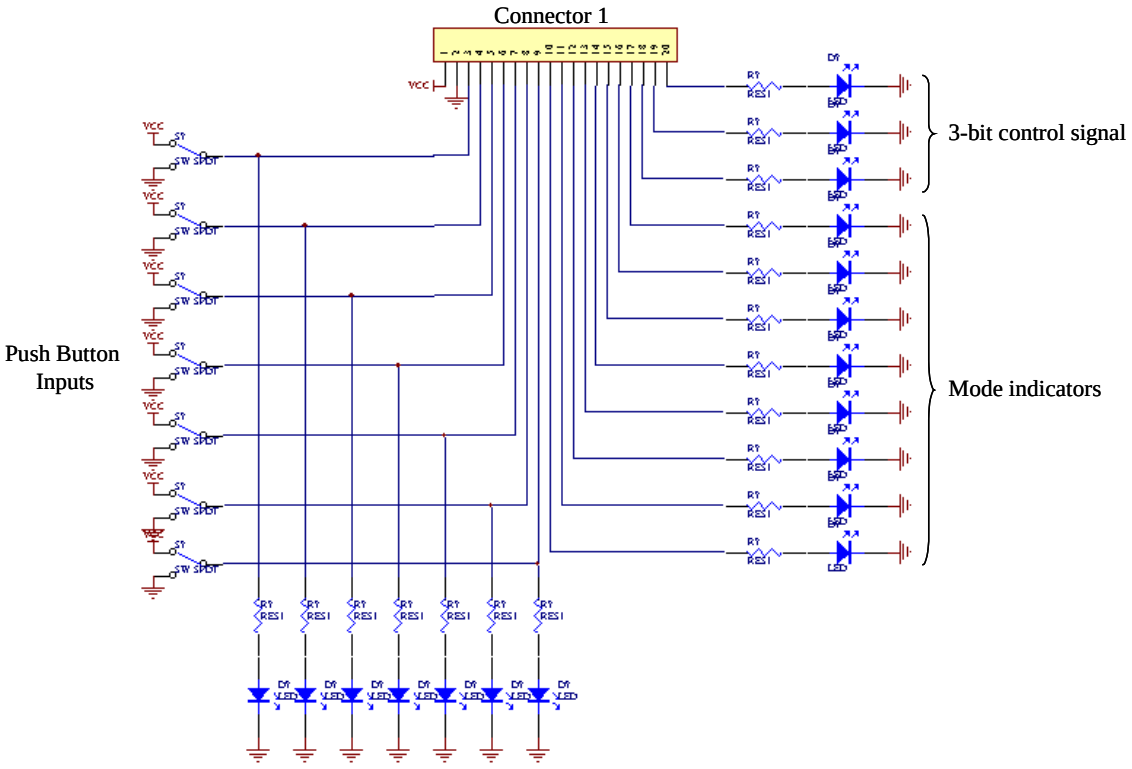
The average model of a three-level, two-quadrant bi-directional chopper was developed in order to produce a more realistic simulation in an effort to accurately account for transients in mode transitions. In addition, a more elaborate and precise simulation model of the VSC was also developed. The D-Q model was first derived using phase variables and the transformation matrix implemented in the actual hardware. Furthermore, a model of the current sensors, scaling factors and digital delay were included. These efforts produced a system model that could reasonably predict system behavior.

Initial system tests with the 12 H, 60 kJ LTS magnet produced somewhat disappointing but challenging results. Several of the transition mode transients caused controller faults and failure. This led to the investigation and development of the system simulations. Problems were identified, analyzed and solutions were produced. A sequence of problems and their solutions were outlined in the above chapter and simulations as well as experimental results verified these solutions.

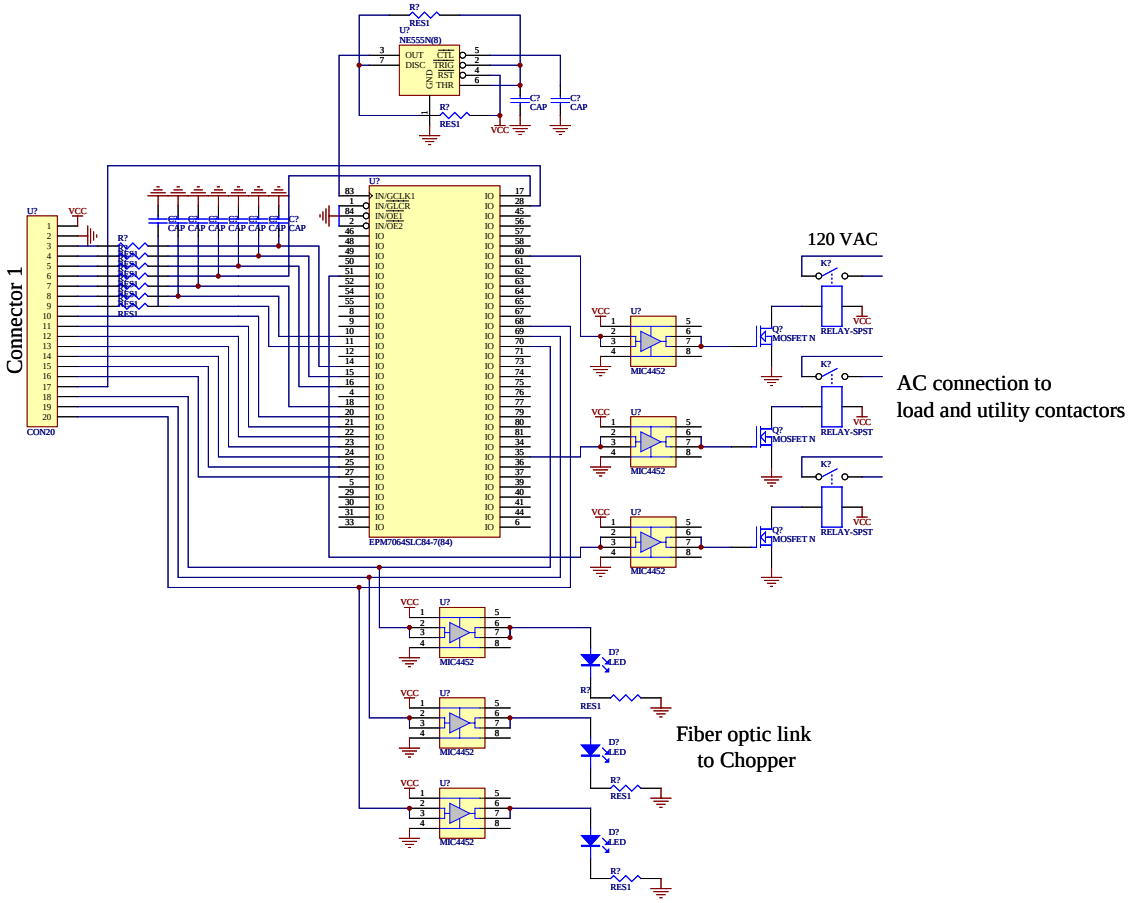
PCS and magnet operation was completed successfully and demonstration objectives were met both here at CPES with the 60 kJ LTS and at NRL with 60 kJ HTS magnet.

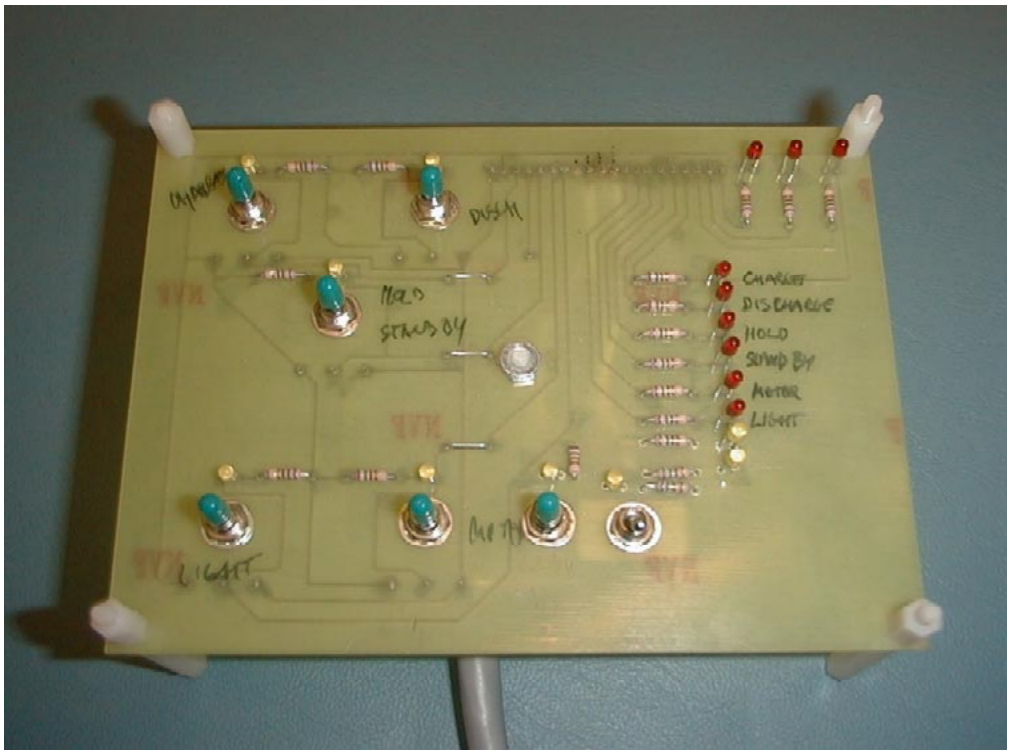
APPENDIX A

User interface Board

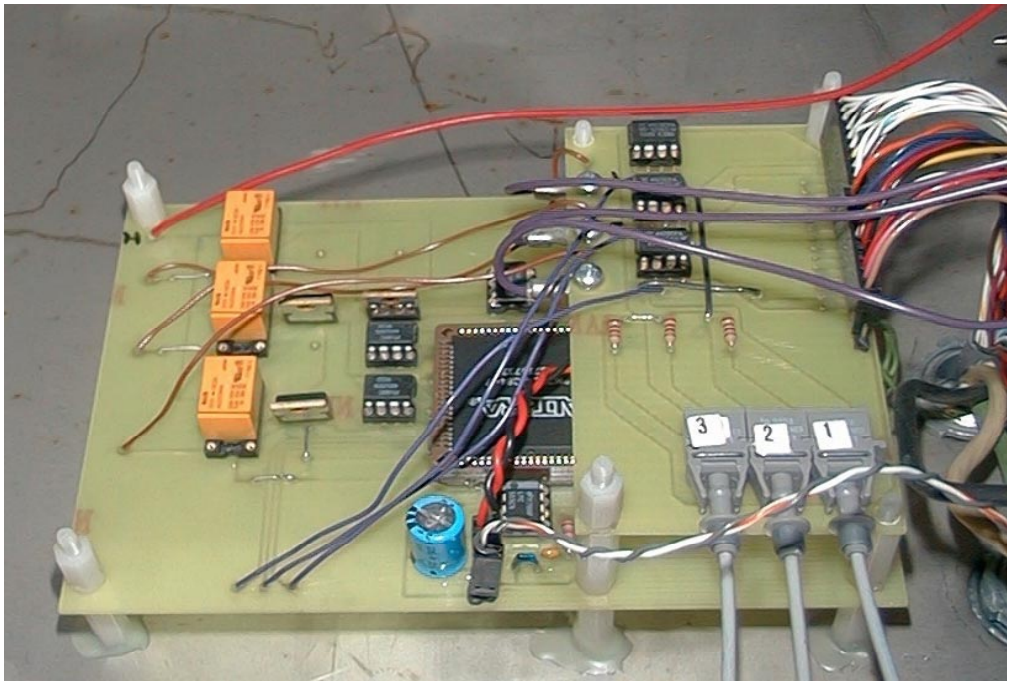


Main Processor board of integrated controller





Demo controller status and interface board



Main processor board of integrated controller

APPENDIX B

Altera AHDL code which dictates the operation of the counter6 sub-block in the graphic design schematic.

```
SUBDESIGN counter6

(
      switch[6..0]                                              :INPUT;
      clk, reset, clr                                           :INPUT;
      cntr1, cntr2, cntr3                                       :OUTPUT;
      out[2..0]                                                 :OUTPUT;
      ihold, istandby, icharge, imotor3, imotor_trans           :OUTPUT;
      idischarge, ipulse, imotor1, imotor2                      :OUTPUT;
)

VARIABLE
      ss: MACHINE WITH STATES
                  (standby, hold, holda, charge, discharge,
                        motor1, motor2, motor3, motor_trans, pulse,
pulsea);

      holdby[2..0]                  :DFF;
      count[14..0]                  :DFF;
      ipulsea                             :NODE;
      iholda                              :NODE;
      holdclk                             :NODE;
      holdclr                             :NODE;

BEGIN

      ss.clk           = clk;
      ss.reset     = reset;
      holdby[].clk   = holdclk;
      holdby[].clrn  = holdclr;
      count[].clk  = clk;
      count[].clrn = !clr;
      count[].clk = clk;

      CASE ss IS
            WHEN standby =>
                  count[].d = count[].q + 1;
                  cntr1 = B"0";
                  cntr3 = B"0";
                  holdclr = VCC;
                  out[] = holdby[].q;
                  CASE count[] IS
                        WHEN 16300 =>
                              holdby[].d = B"010";
                              holdclk = VCC;
                              out[] = holdby[].q;
                              CASE switch[] IS
                                    WHEN B"0000100" =>
                                          ss = holda;
```

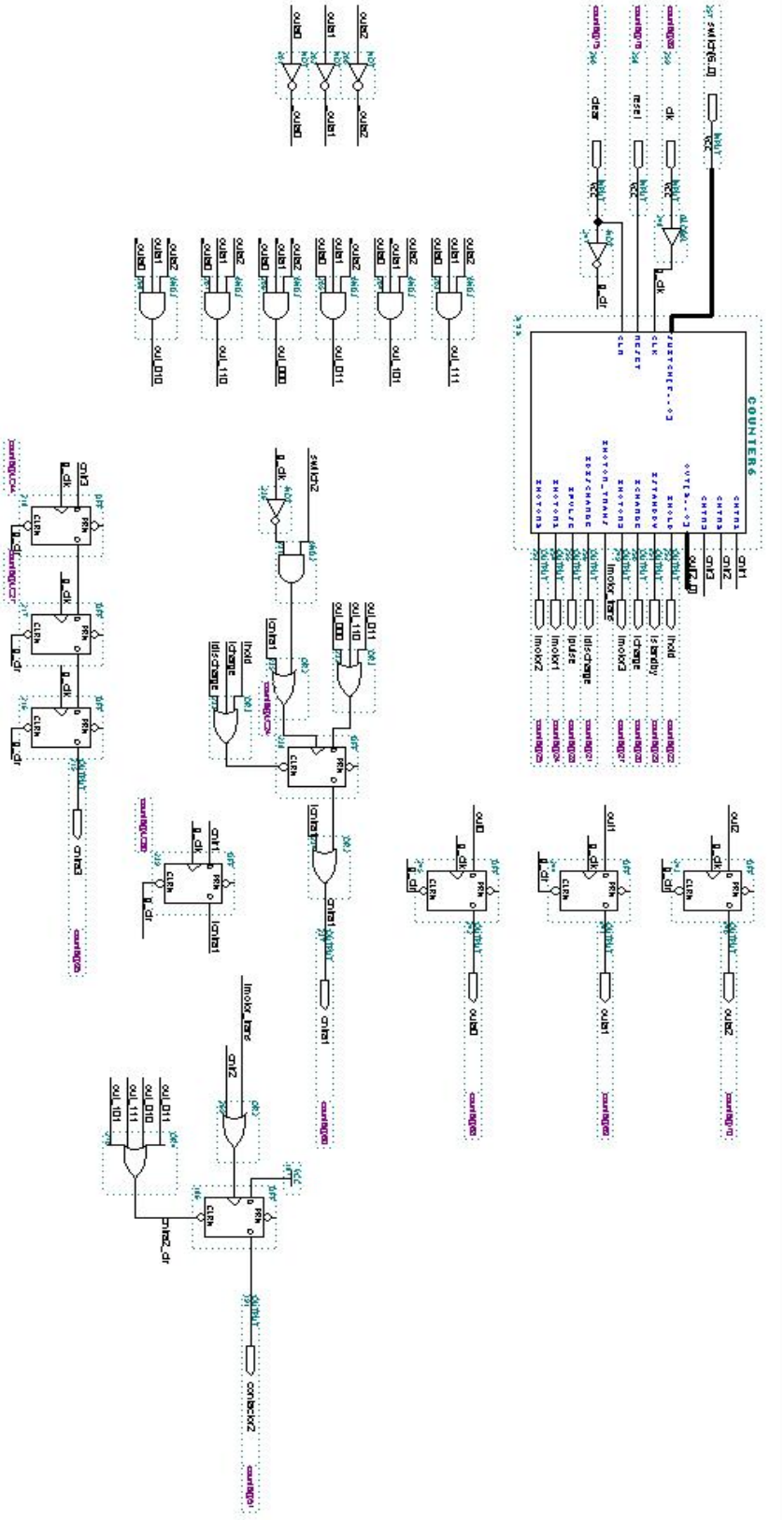
```
                              cntr2 = B"0";
                              count[].d = 0;
                        WHEN B"0001000" =>
                              ss = motor1;
                              count[].d = 0;
                        WHEN B"0100000" =>
                              ss = motor2;
                              count[].d = 0;
                        WHEN B"1000000" =>
                              ss = motor3;
                              count[].d = 0;
                        WHEN B"0010000" =>
                              ss = pulsea;
                              cntr2 = B"0";
                              count[].d = 0;
                  END CASE;
      END CASE;
WHEN holda =>
      count[].d = count[].q + 1;
      CASE count[] IS
            WHEN 16300 =>
                  ss = hold;
      END CASE;
WHEN hold =>
      count[].d = count[].q + 1;
      cntr2 = B"0";
      cntr3 = B"0";
      CASE count[] IS
            WHEN 16300 =>
                  CASE switch[] IS
                        WHEN B"0000000" =>
                              ss = standby;
                              cntr1 = B"0";
                              count[].d = 0;
                        WHEN B"0000101" =>
                              ss = charge;
                              out[] = B"100";
                              cntr1 = B"1";
                              count[].d = 0;
                        WHEN B"0000110" =>
                              ss = discharge;
                              out[] = B"001";
                              cntr1 = B"1";
                              count[].d = 0;
                        WHEN B"0000100" =>
                              cntr1 = B"1";
                  END CASE;
      END CASE;
WHEN charge =>
      count[].d = count[].q + 1;
      cntr2 = B"0";
      cntr3 = B"0";
      cntr1 = B"1";
      CASE count[] IS
            WHEN 16300 =>
                  CASE switch[] IS
                        WHEN B"0000100" =>
```

```
                              ss = hold;
                              out[] = B"000";
                              count[].d = 0;
                        WHEN B"0000101" =>
                              ss = charge;
                  END CASE;
      END CASE;
WHEN discharge =>
      count[].d = count[].q + 1;
      cntr2 = B"0";
      cntr3 = B"0";
      cntr1 = B"1";
      CASE count[] IS
            WHEN 16300 =>
                  CASE switch[] IS
                        WHEN B"0000100" =>
                              ss = hold;
                              out[] = B"000";
                              count[].d = 0;
                        WHEN B"0000110" =>
                              ss = discharge;
                  END CASE;
      END CASE;
WHEN motor_trans =>
      count[].d = count[].q + 1;
      cntr2 = B"1";
      out[] = B"010";
      CASE count[] IS
            WHEN 16300 =>
                  ss = standby;
      END CASE;
WHEN motor1 =>
      count[].d = count[].q + 1;
      cntr2 = B"1";
      cntr3 = B"0";
      cntr1 = B"0";
      holdclr = VCC;
      CASE count[] IS
            WHEN 16300 =>
                  CASE switch[] IS
                        WHEN B"0000000" =>
                              holdby[].d = B"010";
                              holdclk = VCC;
                              ss = motor_trans;
                              out[] = holdby[].q;
                              count[].d = 0;
                        WHEN B"0001000" =>
                              ss = motor1;
                  END CASE;
      END CASE;
WHEN motor2 =>
      count[].d = count[].q + 1;
      cntr2 = B"1";
      cntr3 = B"0";
      cntr1 = B"0";
      holdclr = VCC;
      CASE count[] IS
```

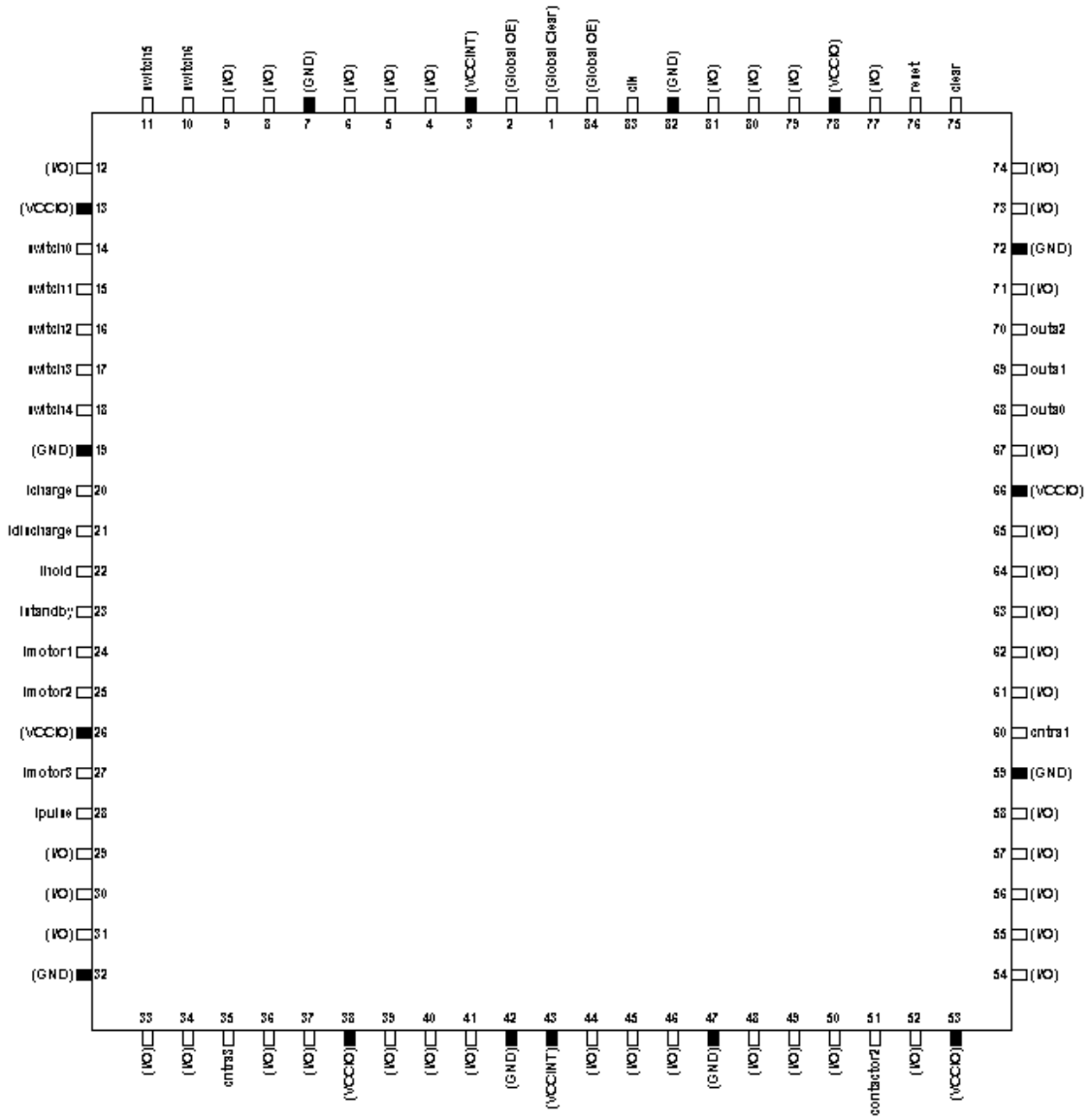
```
                  WHEN 16300 =>
                        CASE switch[] IS
                              WHEN B"0000000" =>
                                    holdby[].d = B"010";
                                    holdclk = VCC;
                                    ss = motor_trans;
                                    out[] = holdby[].q;
                                    count[].d = 0;
                              WHEN B"0100000" =>
                                    ss = motor2;
                        END CASE;
            END CASE;
      WHEN motor3 =>
            count[].d = count[].q + 1;
            cntr2 = B"1";
            cntr3 = B"0";
            cntr1 = B"0";
            out1 = B"1";
            CASE count[] IS
                  WHEN 16300 =>
                        CASE switch[] IS
                              WHEN B"0000000" =>
                                    holdby[].d = B"010";
                                    holdclk = VCC;
                                    ss = motor_trans;
                                    out[] = holdby[].q;
                                    count[].d = 0;
                              WHEN B"1000000" =>
                                    ss = motor3;
                        END CASE;
            END CASE;
      WHEN pulsea =>
            count[].d = count[].q + 1;
            cntr1 = B"0";
            CASE count[] IS
                  WHEN 16300 =>
                        ss = pulse;
            END CASE;
      WHEN pulse =>
            out[] = B"110";
            cntr3 = B"1";
            CASE switch[] IS
                  WHEN B"0000000" =>
                        ss = standby;
                        count[].d = 0;
                  WHEN B"0010000" =>
                        ss = pulse;
            END CASE;
END CASE;
CASE ss IS
      WHEN standby =>
            istandby = B"1";
            out1 = B"1";
      WHEN holda =>
            iholda = B"1";
            out[] = B"000";
      WHEN hold =>
```

```
                  out[] = B"000";
                  ihold = B"1";
            WHEN charge =>
                  out[] = B"100";
                  icharge = B"1";
            WHEN discharge =>
                  out[] = B"001";
                  idischarge = B"1";
            WHEN motor_trans =>
                  imotor_trans = B"1";
                  cntr2 = B"1";
                  out[] = B"010";
            WHEN motor1 =>
                  out[] = B"011";
                  imotor1 = B"1";
            WHEN motor2 =>
                  out[] = B"101";
                  imotor2 = B"1";
            WHEN motor3 =>
                  out[] = B"111";
                  imotor3 = B"1";
            WHEN pulsea =>
                  out[] = B"010";
                  ipulsea = B"1";
            WHEN pulse =>
                  ipulse = B"1";
      END CASE;
END;
```

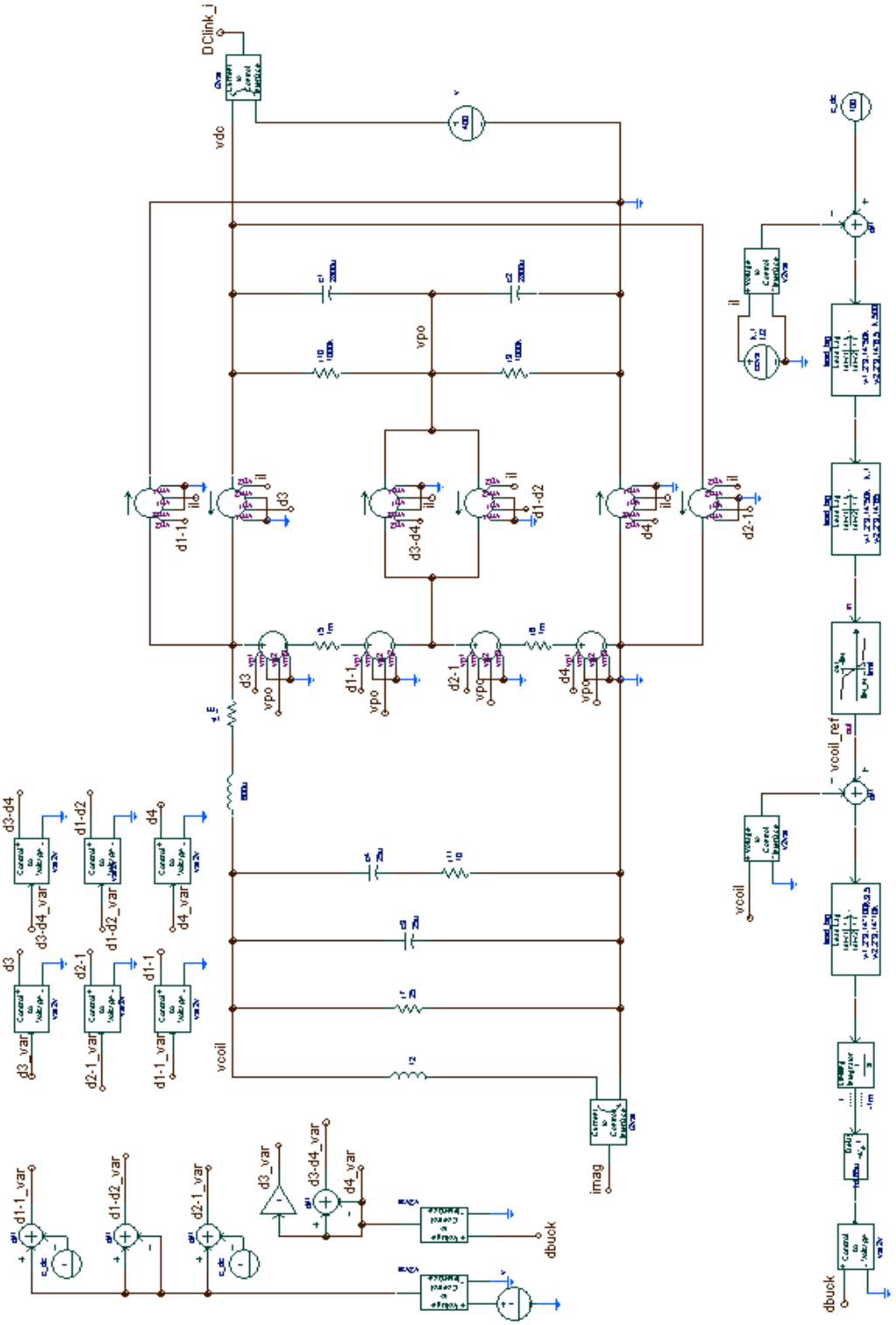
Graphic Design Schematic



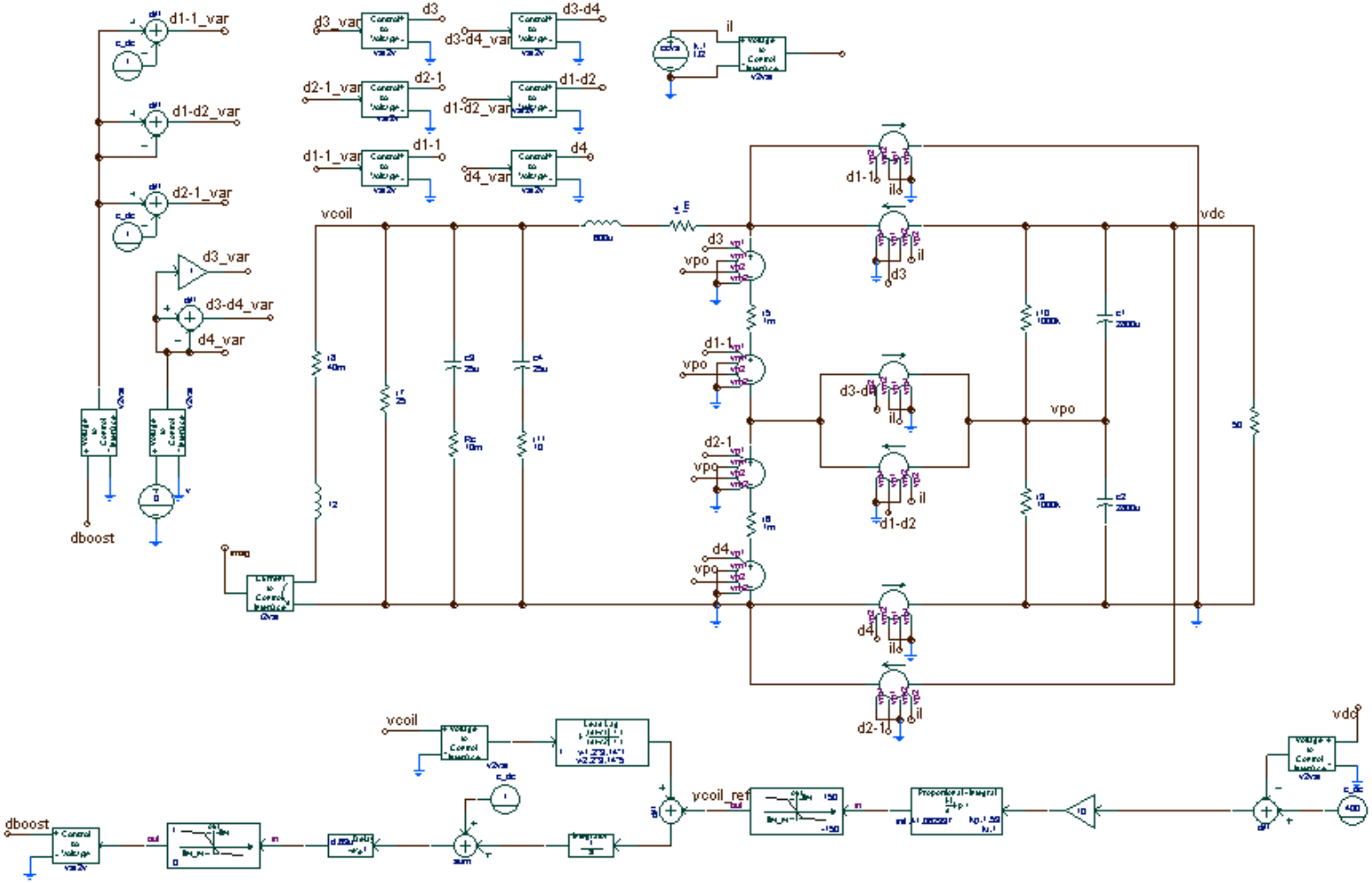
Altera Flex 7084 pinout



APPENDIX C

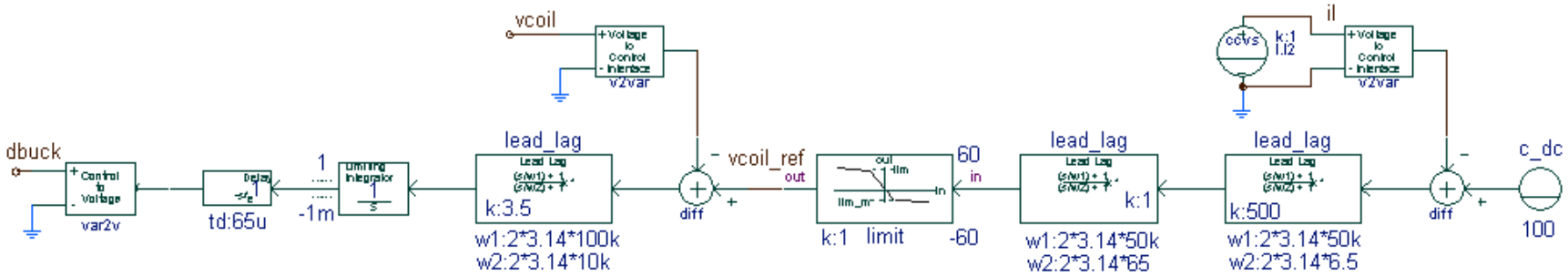


Chopper Buck Mode Simulation Schematic

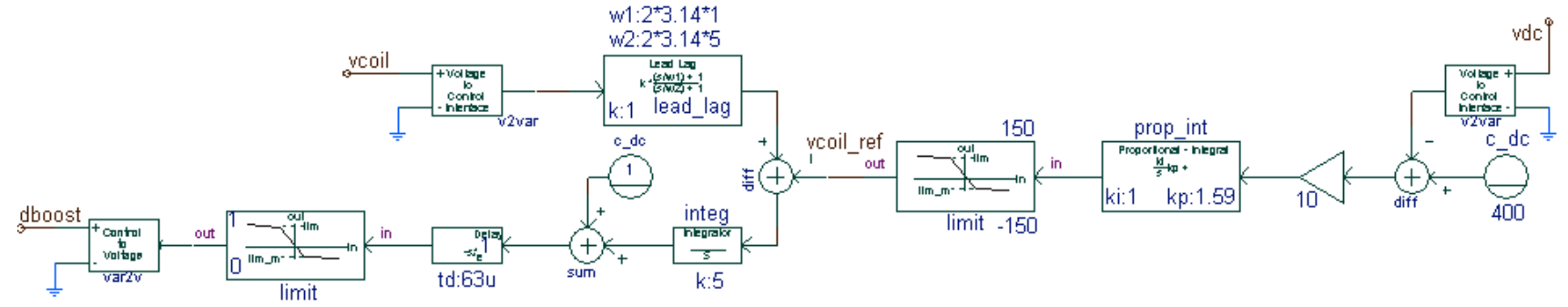


Chopper Boost Mode Simulation Schematic

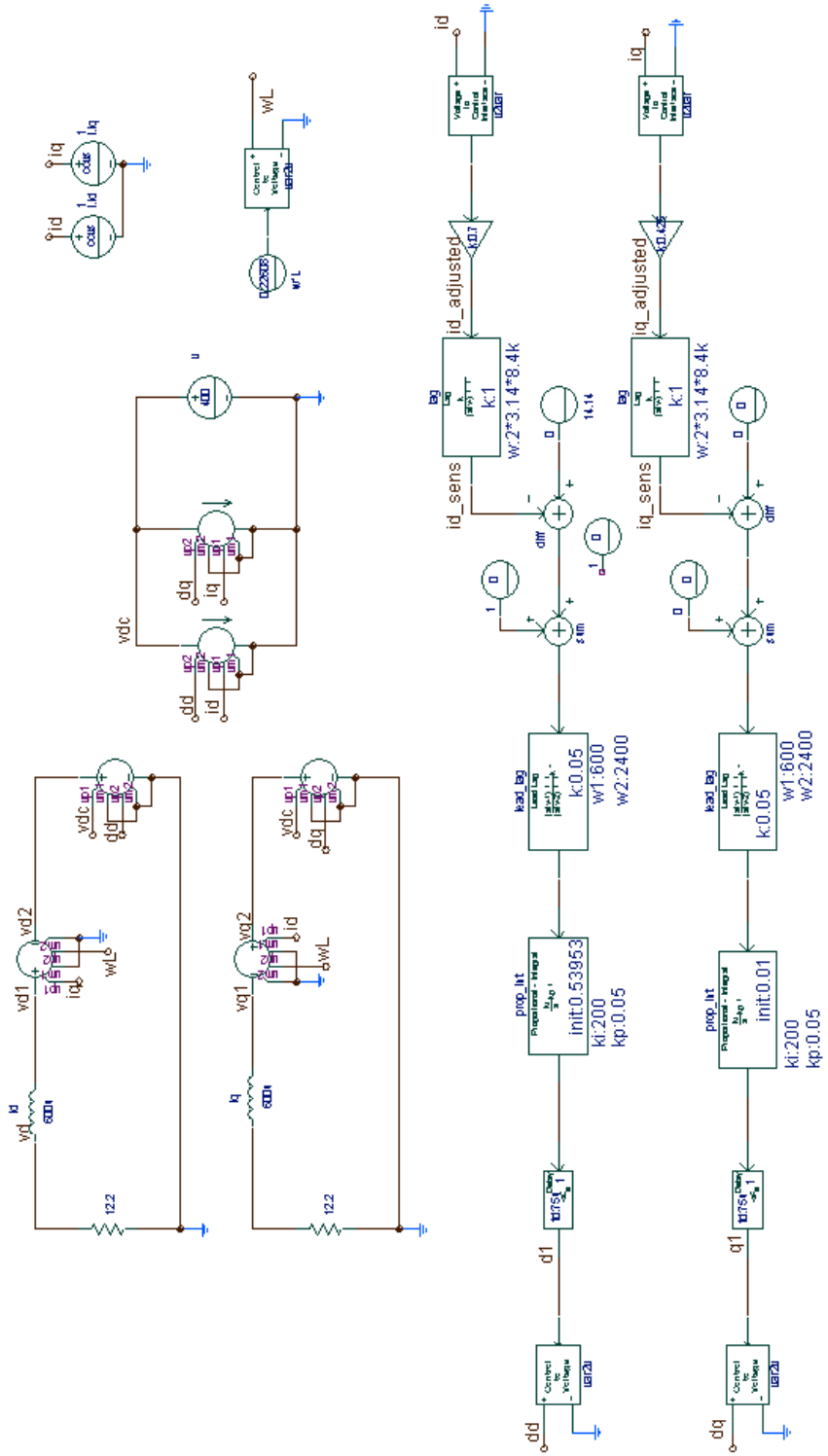
Chopper Buck Mode Control Loops



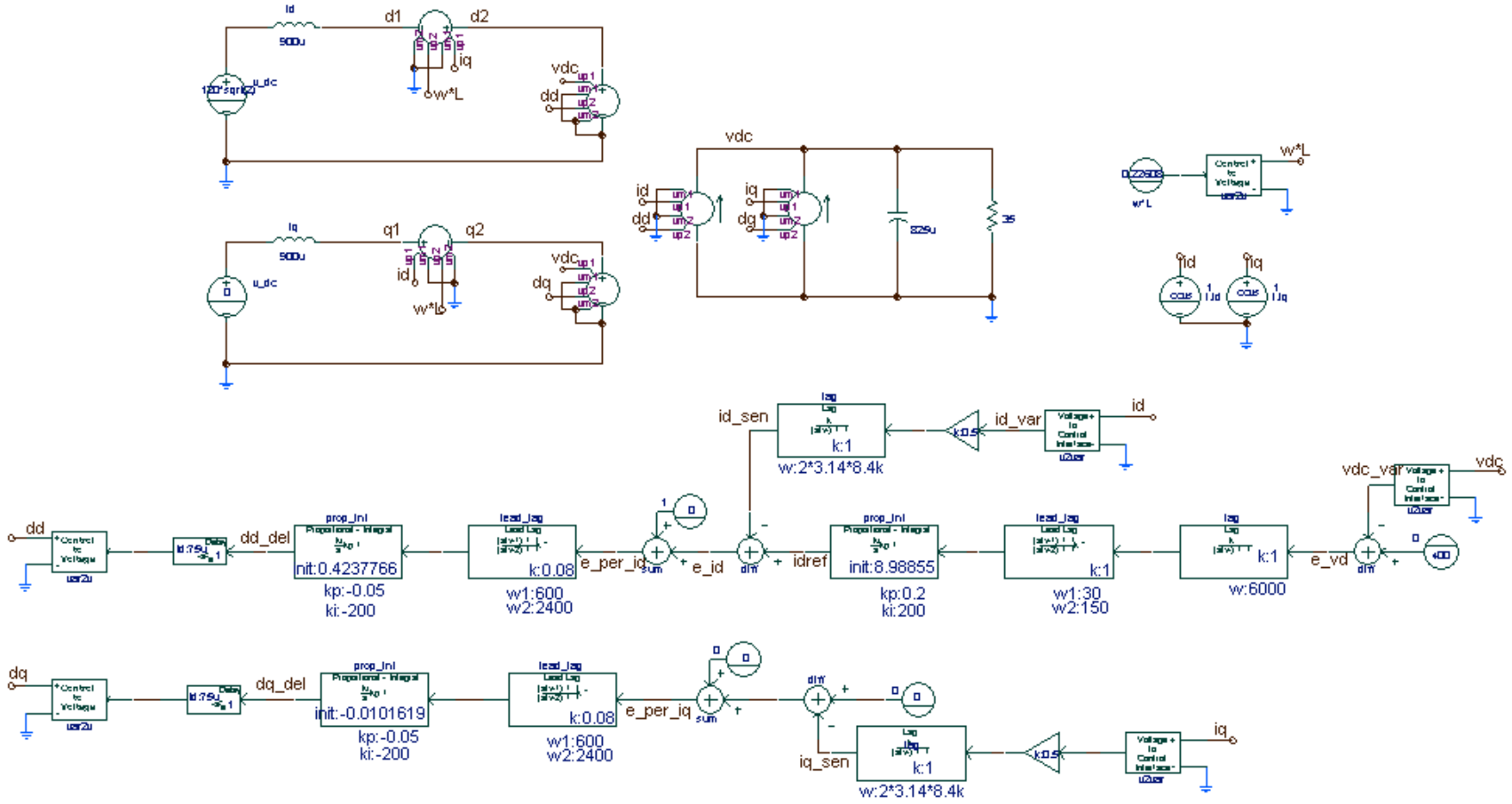
Chopper Boost Mode Control Loops



APPENDIX D

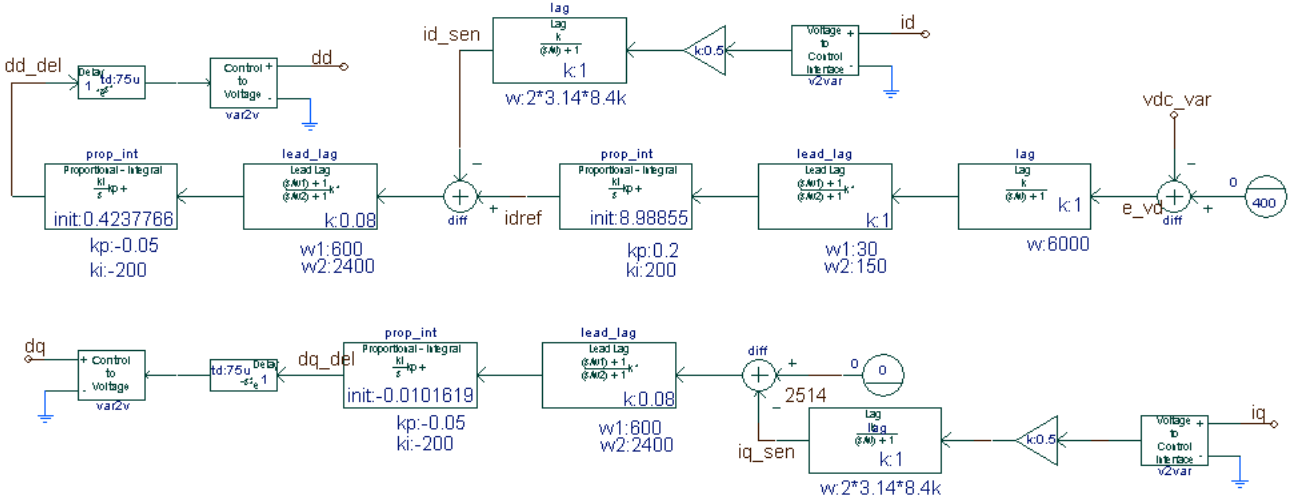


VSI Simulation Schematic

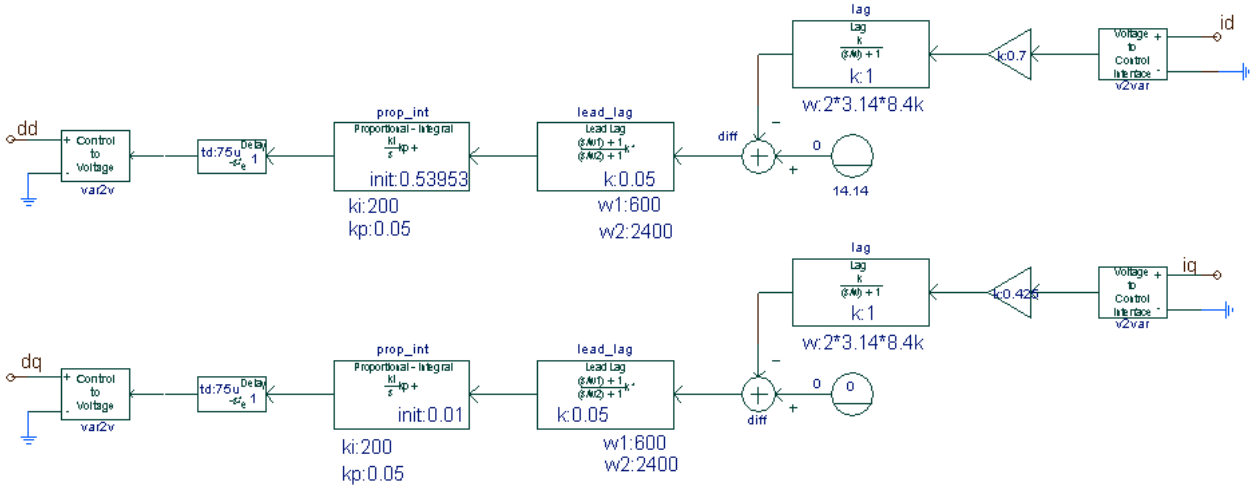


Boost Rectifier Simulation Schematic

VSC - Boost rectifier control loops



VSC - Inverter control loops



REFERENCES

[1] Paula Taylor, et al., "*A Summary of the State of the Art of Superconducting Magnetic Energy Storage, Flywheel Energy Storage, and Compressed Air Energy Storage*," Sandia Report SAND99-1854, Albuquerque, NM: Sandia National Labs, 1999.

[2] Cesar A. Luongo, "Superconducting Storage Systems: An Overview," *IEEE Trans. on Mag*., Vol. 32, No.4, pp. 2214-2223, 1996.

[3] Donald T. Hackworth, Henry E. Lokay and Kenneth B. Steinbruegge, "*Final Report: Superconducting Magnetic Energy Storage Development Program. SMES Applications Study Report*," Westinghouse Report 96-95M3-DSMEZ-R6, Pittsburg, PA: Westinghouse STC, 1996.

[4] C. Rehtanz, "Systemic Use of Multifunctional Superconducting Magnetic Energy Storage in Electric Power Systems," *IEEE Trans. on Power Systems*, Vol. 14, No. 4, pp. 1422-1427, 1999.

[5] Duangkamol Kamolyabutra, et al., "Experimental Study on Power System Stabilizing Control Scheme for the SMES with Solid-State Phase Shifter (SuperSMES)," *IEEE Trans. on Applied Superconductivity*, Vol. 9, No. 4, pp. 4715-4724, 1999.

[6] R. H. Lasseter, S. G. Jalali, "Dynamic Response of Power Conditioning Systems for Superconductive Magnetic Energy Storage," *IEEE Trans. on Energy Conversion*, Vol. 6, No. 3, pp. 388-393, 1991.

[7] A. K. Kalafala, et. al, "Micro Superconducting Magnetic Energy Storage (SMES) System for Protection of Critical Industrial and Military Loads," *IEEE Trans. on Mag*., Vol. 32, No. 4, 1996.

[8] D. Casadei, G. Grandi, U. Reggiani, G. Serra and A. Tani, "Behavior of a Power Conditioner for u-SMES Systems Under Unbalanced Supply Voltages and Unbalanced Loads," *IEEE*, pp. 539-544, 1999.

[9] Binad Kumar, "Magnetic Energy Storage Devices for Small Scale Applications," *IEEE AES Systems Magazine*, pp. 12-17, Nov. 1992.

[10] K. P. Juengt and H. Salbert, "Fast SMES for Generation of High Power Pulses," *IEEE Trans. on Mag*., Vol. 32, No. 4, pp.2272-2275, 1996.

[11] Ian R. McNab, "Pulsed Power for Electric Guns," *IEEE Trans on Mag*., Vol. 33, No. 1, pp.453-460, 1997.

[12] W. Weck, P. Ehrhart, A. Muller and G. Reiner, "Superconducting Inductive Pulsed Power Supply for Electromagnetic Launcher: Design Aspects and Experimental Investigation of Laboratory Set-up," *IEEE Trans. on Mag*., Vol. 33, No. 1, pp. 524-527, 1997.

[13] Werner Weck, Peter Ehrhart, Anton Muller, Hermann Scholderle and Evi Sturm, "Demonstration of a Superconducting Inductive Pulsed Power at Simulated Load Conditions," *IEEE Trans. on Mag*., Vol. 35, No. 1, pp. 383-387, 1999.

[14] Denis Netter, Jean Leveque, Abderrezak Rezzoug, "Theoretical Studies and

Experimental Results on a SMES Used in a Pulsed Current Supply," *IEEE Trans. on Applied Superconductivity*, Vol. 8, No. 1, pp. 7-13, 1998.

[15] F. Jarnet, V. Wegner and H. Peter, "Some Aspects of Future Military Requirements," *IEEE Trans. on Mag*., Vol. 29, No. 1, pp. 351-355, 1993.

[16] H.Mao, et. al, "*Advanced Power Electronics Techniques for Superconducting Magnetic Energy Storage Power Conditioning Systems*," First Phase Report, Blacksburg, VA: Virginia Power Electronics Center, 1996.

[17] D. Lee, et. al, "*Advanced Power Electronics Techniques for Superconducting Magnetic Energy Storage Power Conditioning Systems*," Third Phase Report, Blacksburg, VA: Virginia Power Electronics Center, 1999.

[18] "*High Field HTS Magnet System Operating Guide and Manual*", Boston, MA: American Superconductor, Revision date: July 7, 1998.

[19] Y. Li, A. Q., Haung and F. C. Lee, "Introduction the Emitter Turn-Off Thyristor (ETO)", *Conf. Rec. IEEE-IAS*, 1998, pp-860-864.

[20] P. K. Steimer, H. E. Grunning, J. Werninger, E. Carrol, S. Klaka, S. Linder, "IGCT – a new Emerging Technology for High Power, Low Cost Inverters", *Conf. Rec. IEEE-IAS*, 1997, pp. 1592-1599.

Vita

The author was born in Annapolis, Maryland on August 6, 1976. He received his B.S. degree in Electrical Engineering from the Virginia Polytechnic Institute and State University in 1998. He was involved in undergraduate research at the Virginia Power Electronics Center (VPEC) at Virginia Tech and following the completion of his B.S. degree began perusing a M.S. degree in power electronics at VPEC in August of 1998. He has worked for his family owned company, Chesapeake Cryogenics Inc., as an engineer in the area of cyrogenic refrigeration and will begin work with Northrop Grumman upon completion of his degree. His research interest include three-phase, high power converters, SMES and power electronics for military applications.