CHAPTER 3.
SINGLE-STAGE PFC TOPOLOGY GENERALIZATION AND VARIATIONS

3.1. INTRODUCTION

The original DCM S^2PFC topology offers a simple integration of the DCM boost rectifier and the PWM DC/DC converter. The front-end PFC quasi-stage contains a boost cell, which shares the boost switch with the DC/DC load converter. As shown in Fig. 3.1, the DCM boost cell has a boost inductor L_B, a charging path P_1 through diode D_1 to the switch S and a discharging path P_2 through diode D_2 to the boost output capacitor C_B.

Chapter 2 studies the ideal CCM boost PFC converter and derives the general understanding and necessary condition of the typical CCM S^2PFC techniques proposed in recent years. It is shown that, if the S^2PFC circuit in Fig. 3.1 is push into CCM mode, the input current has high distortion again because the average inductor node voltage $v_{y(ave)}$ is constant over a line cycle. To shape the CCM boost inductor current, the inductor node voltage v_y has to track the changes of instantaneous input voltage. This requirement is met in the CCM CS and VS S^2PFC by adding a modulation inductor [B6, B8, B9] in the DCM S^2PFC charging path P_1, or, by replacing P_1 with a modulation capacitor [B13].

Following the similar concepts, other CCM S^2PFC topologies can be also developed. To better understand the similarities and differences between different S^2PFC circuits as well as to develop new S^2PFC topologies, it is necessary to identify the general structure of the S^2PFC converter and discover the rules for implementation different CCM S^2PFC topologies, which will be presented and discussed in this chapter.

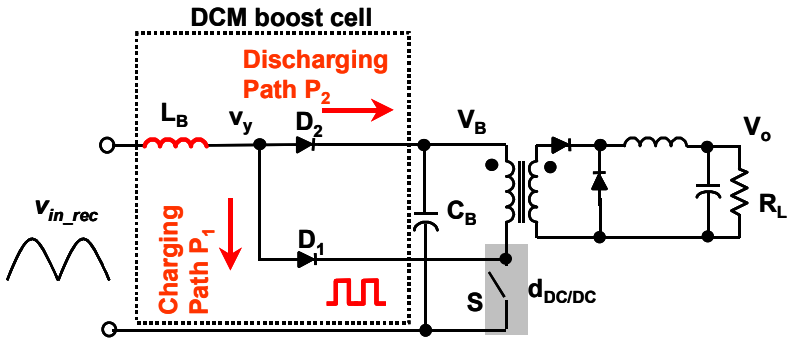
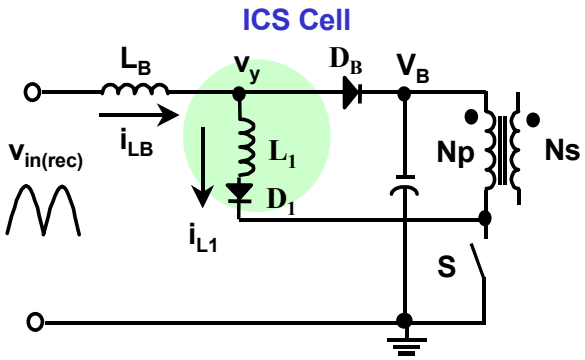
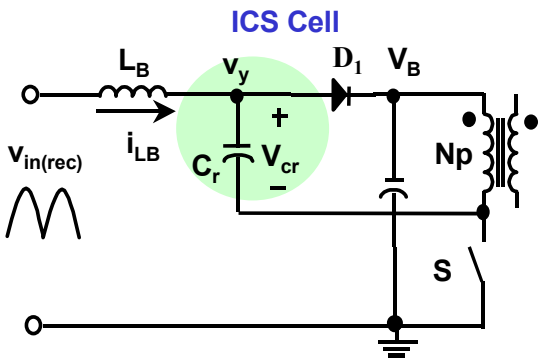


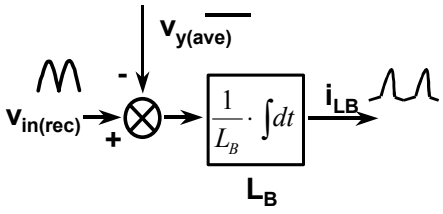
Figure 3.1 DCM boost cell in the basic DCM S²PFC converter



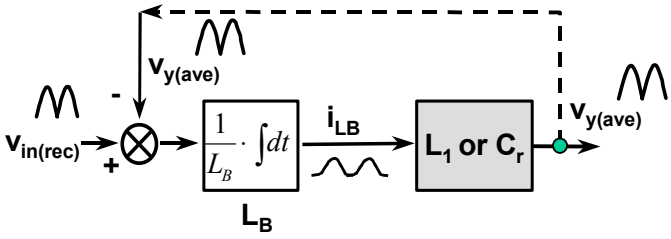
(a) CS S²PFC converter



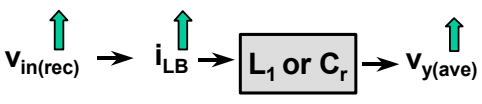
(b) VS S²PFC converter



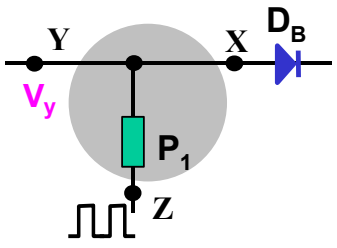
(c) Block diagram of the Circuit **without** L_1 or C_r in Fig. 3.1, while L_B is in CCM



(d) Conceptual block diagram of the Circuit **with** L_1 or C_r in Fig. 3.1, while L_B is in CCM



(e) Feed forward relationship from $v_{in(rec)}$ to $v_{y(ave)}$



(f) Feed forward cell

Figure 3.2 CCM S²PFC converters' feed-forward relationship between $v_{in(rec)}$ and $v_{y(ave)}$ and feed-forward cell

3.2. FEED-FORWARD PFC CELLS AND GENERALIZED THREE-TERMINAL S^{2}PFC STRUCTURE

3.2.1 Feed-forward cells in the CCM S^{2}PFC converters

Figure 3.2(a) and (b) show that two typical CCM S^{2}PFC topologies [B6, B8, B13] can be obtained by simply adding a modulation inductor L_1 into the DCM S^{2}PFC circuit charging path P_1 or replacing P_1 with a modulation capacitor C_r. The switching cycle waveforms in Fig. 2.15 and 2.18, and Eq. (2.13) and (2.17) show that the additional component L_1 or C_r provides v_y with the information of i_{LB}. Equation (2.12) and (2.17) can be re-written as Eq. (3.1) and (3.2), which mathematically shows the feed-forward effect introduced by L_1 or C_r. When the input instantaneous voltage $v_{in(rec)}(t)$ increases, the input inductor current $i_{LB}(t)$ naturally increases, and L_1 or C_r causes $v_{y(ave)}(t)$ to also increase and follow the movement of $v_{in(rec)}(t)$. Therefore, the CS and VS S^{2}PFC can be conceptually generalized as a feed-forward PFC cell, as shown in Fig. 3.2(f).

$$v_{y(ave)} \approx V_B \cdot (1-D) + i_{LB} \cdot \frac{L_1}{T_s} \propto (L_1 \cdot f_S) \cdot i_{LB} \propto v_{in(rec)} \tag{3.1}$$

$$v_{y(ave)} = V_B - \frac{C_r \cdot f_S}{2 \cdot i_{LB}} \cdot (\frac{V_B}{1-D})^2 = Const_1 - Const_2 \cdot \frac{C_r \cdot f_S}{i_{LB}} \propto v_{in(rec)} \tag{3.2}$$

Following a similar concept, other feed-forward PFC cells can be developed. For example, as shown in Fig. 3.3 (a) and (b), the feed-forward inductor L_1 can be added either in the charging path P_1 or in the discharging path P_2 in the basic PFC cell. With L_1 in the charging path, as shown in Fig. 3.3(a), the circuit is the previous CS S^{2}PFC circuit, which has modulation on the v_y waveform during the switch turn-on time interval. With L_1 in the discharging path, as shown in Fig. 3.3(b), the circuit is a new CS S^{2}PFC circuit, which has modulation on the v_y

waveform during the switch turn-off time interval. Figure 3.3(d) shows the new CS S^2PFC circuit's switching cycle waveform, in which the inductor L_1 introduces the additional area on to v_y, that is caused by the current commutation from D_1 to L_1 at the beginning of the switch turn-off time instant. With the similar feed-forward principle, this new CS S^2PFC can also shape the input current, as shown in Fig. 3.3 (f). Compared with the CS S^2PFC converter's inductor current waveform shown in Fig. 3.3(e), the new CS S^2PFC circuit has a comparable level of input current THD, but larger high-frequency inductor current ripples that occur due to its greater volt-second on its boost inductor in one switch period. Anyway, this new CS S^2PFC circuit shows just one possible way to implement the feed-forward PFC cell. There are several other possibilities to implement the PFC cells.

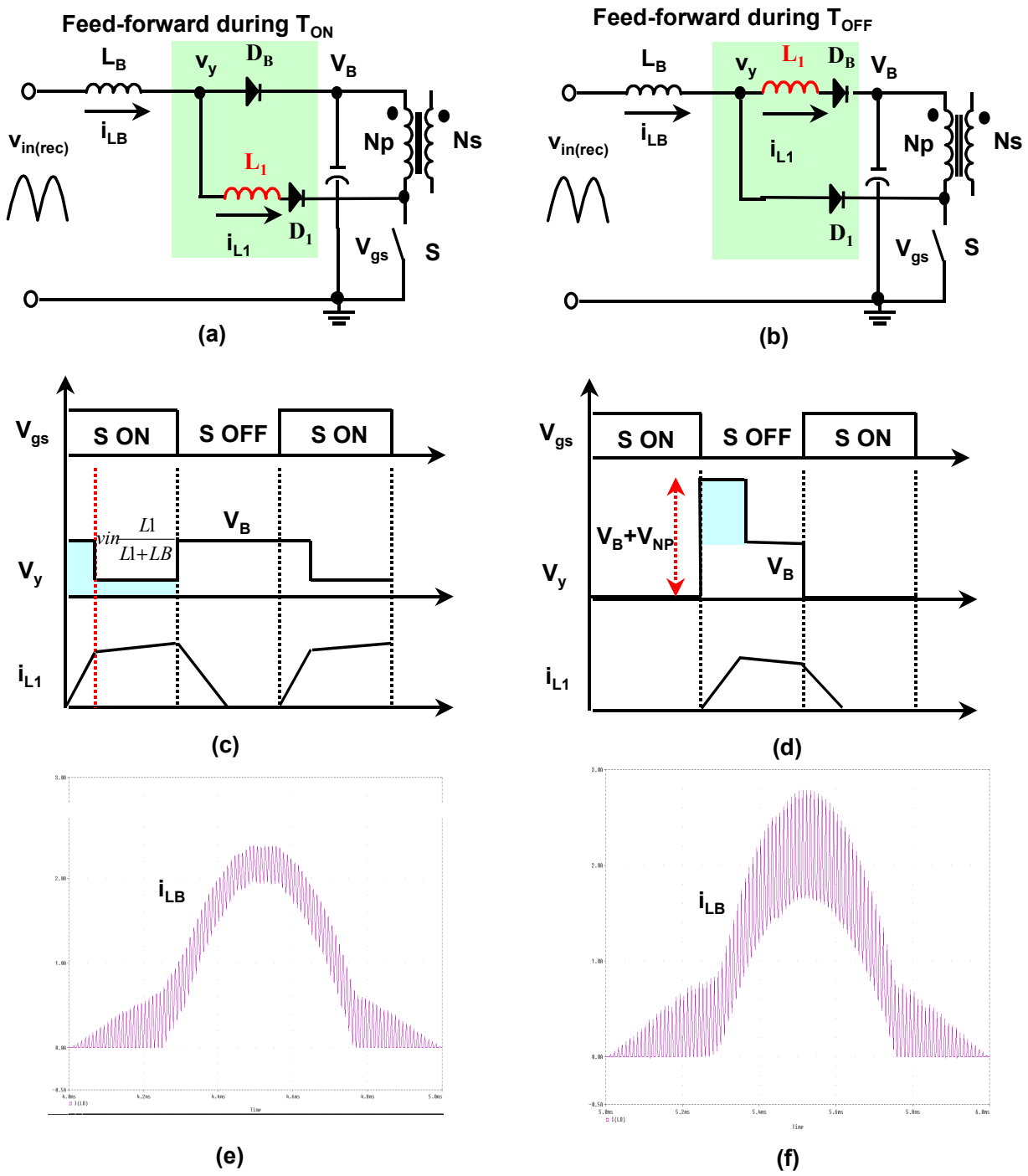


Figure 3.3 Different implementations of the feed-forward concept in the CCM CS S^2PFC

(a) (c) (e) Adding modulation inductor L_1 into the charging path

(b) (d) (f) Adding modulation inductor L_1 into the discharging path

3.2.2. The three-terminal general S^2PFC structure and rules for implementing of feed-forward cells

Before generating the different topologies of the CCM S^2PFC circuit, it is necessary to identify the general topology and the rules for implementing different feed-forward cells. Since the original integrated S^2PFC concept comes from the integration of boost rectifier with the DC/DC converter, the general PFC structure is defined as in Fig. 3.4, which has a 3-terminal cell with boost charging path P_1 and discharging path P_2. Moreover, to achieve CCM PFC, the charging path or discharging path of the integrated boost rectifier must contain feed-forward components to modulate v_y waveform or the effective duty-cycle of L_B. There are several basic rules for the implementation of P_1 and P_2:

1) Boost inductor charging path P_1 connects the high-frequency signal source at node Z to switch S, while the discharging path P_2 is connected to the energy-storage capacitor C_B through boost diode D_B at node X;
2) P_1 and/or P_2 should contain small energy-storage component L_i and/or C_i to provide feed-forward PFC modulation effects to node Y;
3) The energy of the high-frequency L_i or C_i should be reset in each switching cycle;
4) L_i cannot be in parallel with a diode, while C_i cannot be in series with a diode;
5) To minimize the circulating current or unwanted resonant current, it is desirable to put a diode in series with the modulation inductor L_i;
6) Finally, the bulk-capacitor voltage feedback winding can be added into P_1 and/or P_2 to limit the bus voltage stress and improve efficiency when needed. In this case, the feedback winding can be either inside P_1 or P_2, or nodes X and Z can be connected to the center tap of the DC/DC stage transformer windings.

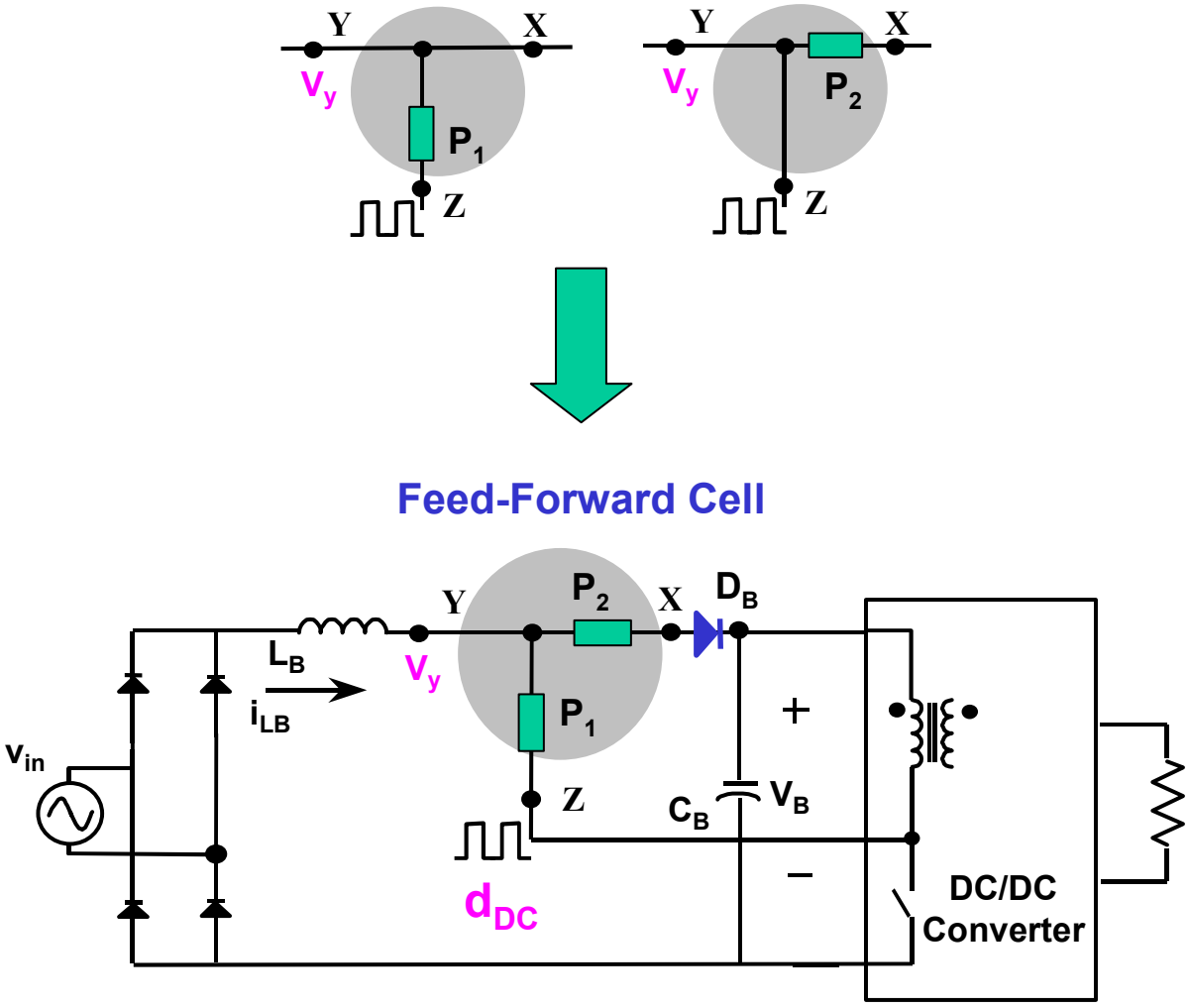


Figure 3.4 Generalized structure of the CCM S^2PFC with 3-terminal feed-forward PFC cell

Based on these rules, several 3-terminal feed-forward cells are implemented. To simplify the discussion, the feedback winding is not included in the cell structure. Figures 3.5 (a)-(c) show all the cells, each of which contains only one CCM PFC feed-forward component L_1 or C_r. In this case, there are only three different implementations of the feed-forward cells each with a single feed-forward component. These three circuits have been discussed in the previous sections. Among them, the existing CS and VS S^2PFC are the preferred topologies. Figure 3.5(d) also shows one example that the high-frequency capacitor C_r cannot be in the P_2 path, which has a boost diode D_B in series with the capacitor C_r. In this case, the capacitor can only be charged. Therefore, this circuit cannot work.

Figures 3.5(e)-(i) show all the possible feed-forward cells, each of which contains two feed-forward components. These two components can be two inductors L_1 and L_2, or one inductor L_1 plus one capacitor C_r. As shown in Fig. 3.5(e), the cell with two inductors L_1 and L_2 is the combination of the circuits in Fig. 3.3(a) and (b). The circuit implemented with the cell shown in Fig. 3.5(e) has been reported [B9], as has the circuits with the cells shown in Fig. 3.5 (h) and (f) [B6]. Figure 3.5 (g) and (i) show two new CCM S^2PFC cells.

In general, Fig. 3.5 also shows the relationship between the single-feed-forward-component cells and two-feed-forward-component cells. Further discussion of the performance of these cells will be given in Sections 3.5.2 and 3.5.3. As discussed in later section, the cell shown in Fig. 3.5(g) is a good combination of the CS and VS S^2PFC cells. With universal-line input, the CCM S^2PFC converter with this particular cell has an improved performance over the original CS and VS S^2PFC converters.

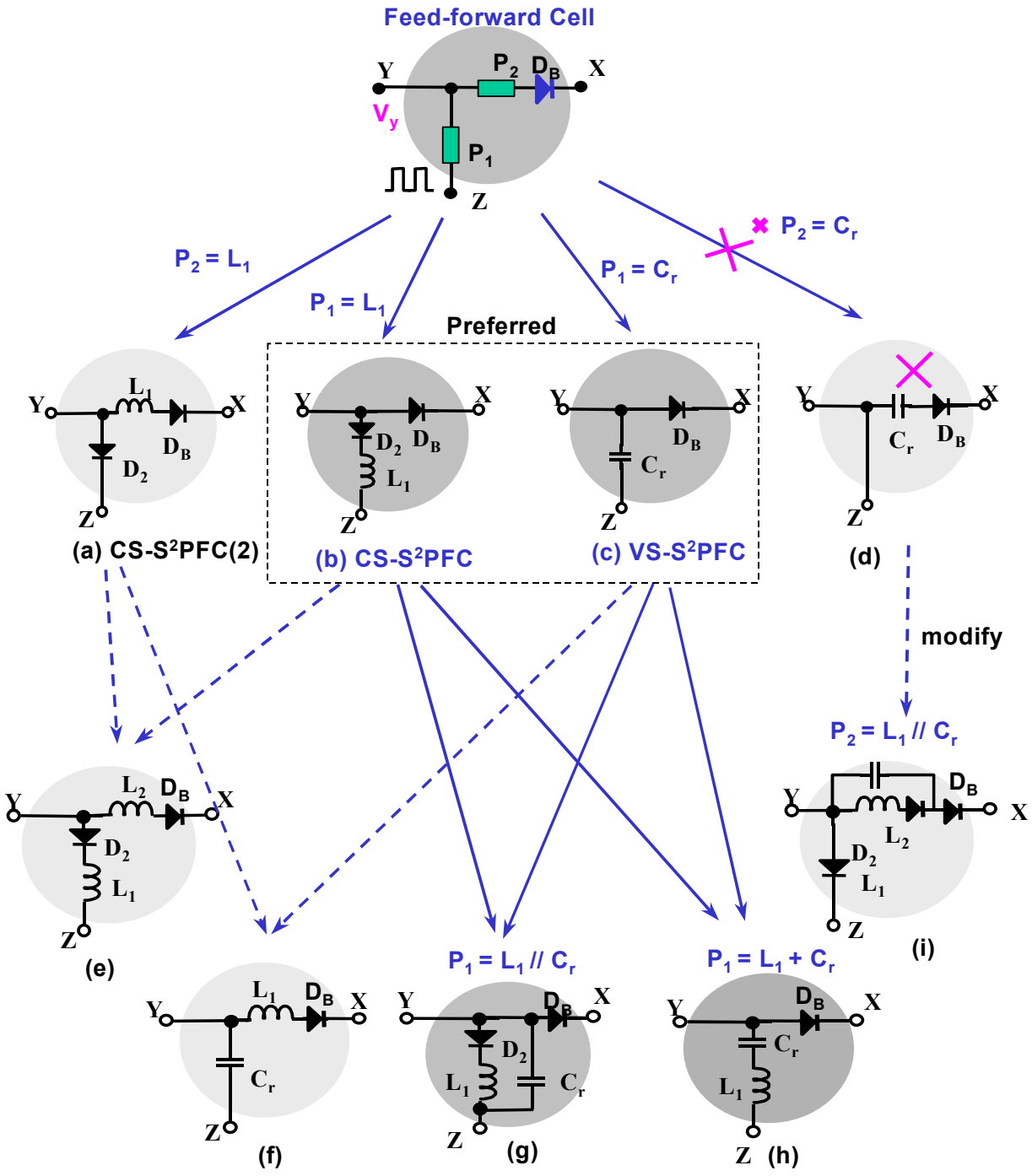


Figure 3.5 Implementations of feed-forward cells with one or two components (L or C).

Finally, it is necessary to point out that the "feedback" windings of the DCM S^2PFC circuits can also be added into the CCM S^2PFC boost charging/discharging paths P_1 or/and P_2, in order to further limit the bulk-capacitor voltage stress and improve the converter efficiency. Furthermore, the feedback windings can be implemented with coupled extra transformer windings or can utilize the center tap of the primary transformer winding, as shown in Fig. 3.6 or 3.7, respectively. As in the DCM S^2PFC converters, the penalty of the feedback windings is the dead conduction angle on the input current and the increased input current distortion. In general, with universal-line input, the feedback ratio (e.g., N_1/N_P) in the CCM S^2PFC converters is much less than that in the DCM S^2PFC converters.

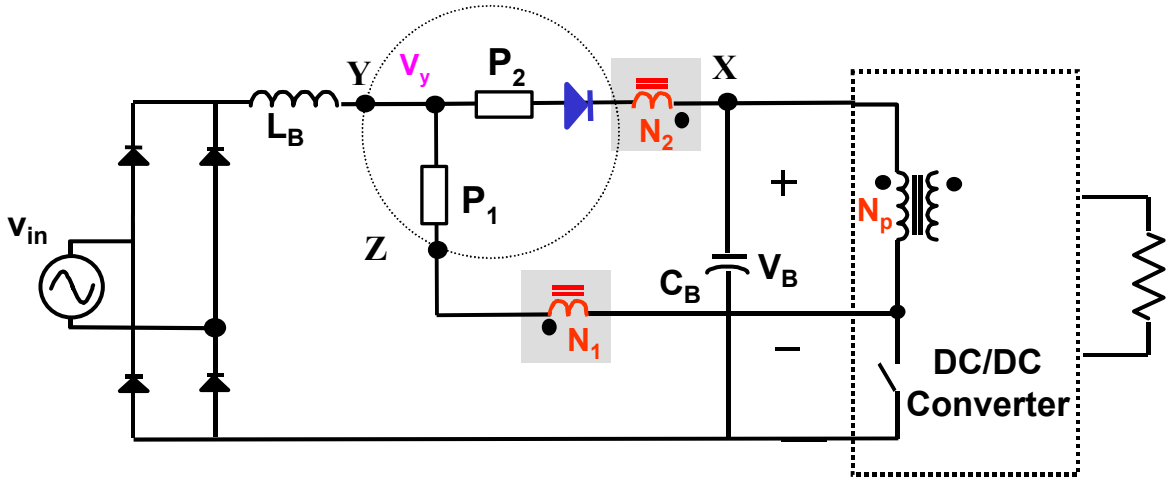


Figure 3.6 Modified generalized three-terminal S^2PFC topology with feedback windings N_1 and N_2

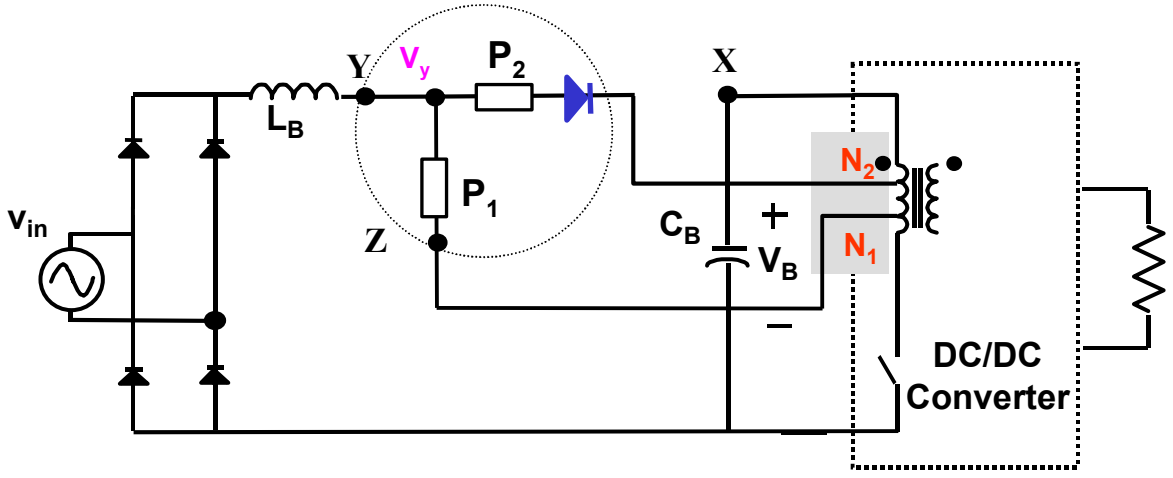


Figure 3.7 Feedback windings N_1 and N_2 also can be implemented by tapping the primary winding of the DC/DC transformer

3.3. GENERALIZED TWO-TERMINAL PFC STRUCTURE AND ITS FEED-FORWARD CELLS

3.3.1 Two-terminal DCM S^2PFC converters [B12, B21]

Besides the S^2PFC circuits with 3-terminal PFC cells, there are several other circuits that have modified boost-cells with a two-terminal structure. As introduced in Section 1.3.2.2, this kind of circuit was first named the "magnetic-switch" (MS) S^2PFC circuit in 1995 [B12]. In 1996, a DCM S^2PFC, which belongs to the MS S^2PFC family, was also proposed [B21].

As discussed in Section 1.3.2.2, in the DCM MS S^2PFC converter shown in Fig. 1.9(b), if the MS winding N_1 has the same turns number as does the DC/DC primary winding N_P, the CM S^2PFC circuits shown in Fig. 1.9(a) and (b) are equivalent with identical circuit waveforms and very close performances. The major difference between these circuits shown in Fig. 1.9(a) and (b) is their different way of implementation of the boost switch integration. The high-frequency switching signal on node Z is identical. To describe the MS S^2PFC in a more precise way and to extend its concept to a broader area, the DCM MS S^2PFC converter is renamed as the DCM "two-terminal" S^2PFC converter, while the original DCM S^2PFC circuit shown in Fig. 1.9(a) is renamed as DCM "three-terminal" S^2PFC converter.

3.3.2. Generalized structure of the two-terminal S^2PFC converters

Figure 3.8 shows how to extend the concept of the 2-terminal DCM S^2PFC converter to derive the generalized structure of the 2-terminal S^2PFC converters. As shown in Fig. 3.8, in the 3-terminal S^2PFC converters, the integrated boost-quasi-stage obtains the DC/DC switching duty-cycle signal by directly connecting the PFC cell node Z to the DC/DC stage switch S. In the

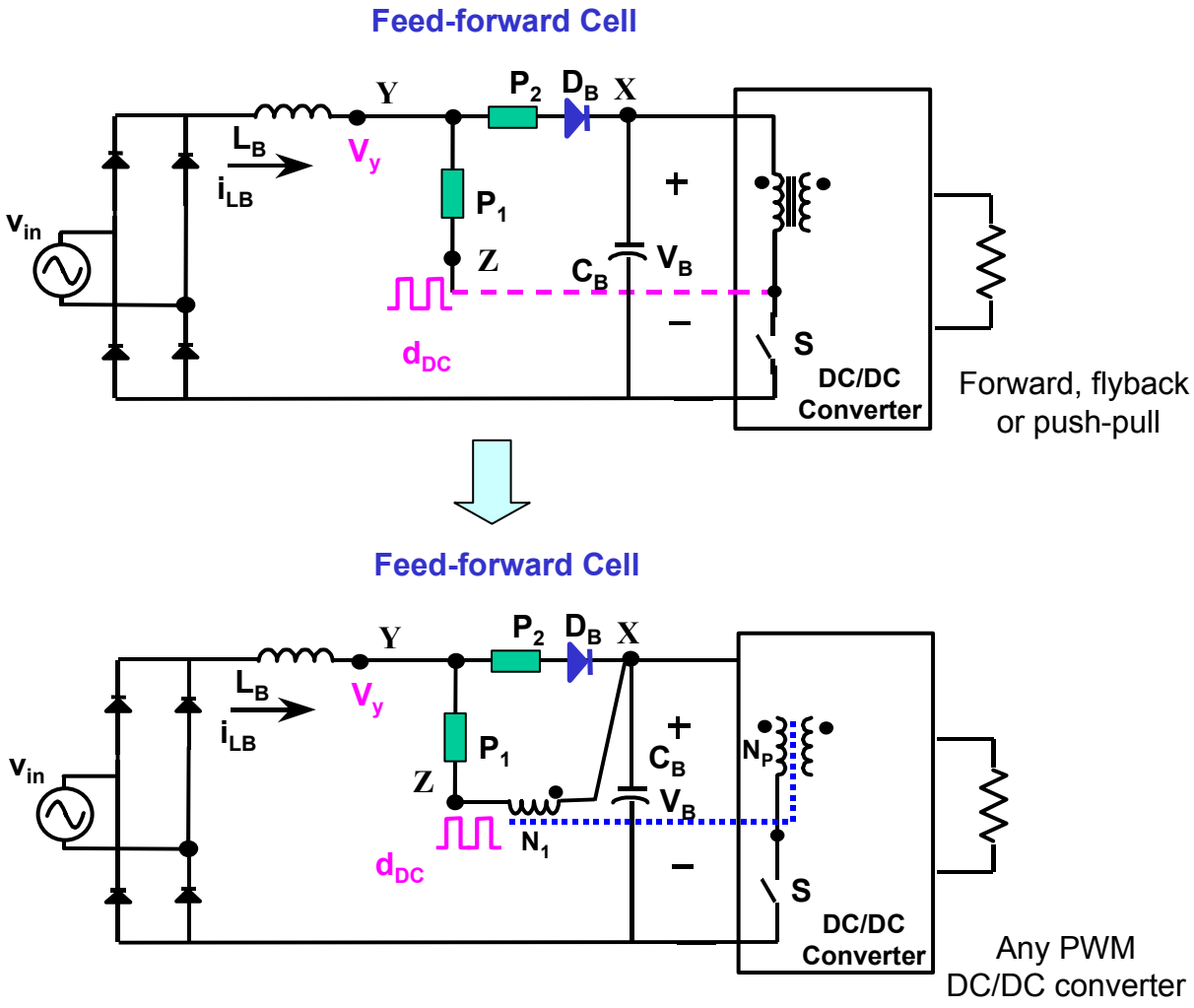


Figure 3.8 Deriving the general structure of the 2-terminal S^{2}PFC converter by change the implementation of high-frequency signal from node Z in the PFC cell.

2-termnial S^2PFC converters, the DC/DC duty-cycle signal is obtained through the additional transformer "magnetic-switch" winding N_1. If the MS winding N_1 turns number is properly chosen, the winding voltage v_{N1} will completely cancel the dc-bus voltage when switch S is turned on. As a result, N_1 brings node Z the same DC/DC duty cycle and these two circuits have identical waveforms and performance.

3.3.3. Topology variations of the 2-terminal S^2PFC converters

3.3.3.1 Topology variations

As shown in Fig. 3.8, the 2-terminal S^2PFC converter also has a feed-forward S^2PFC cell, which has the charging path P_1 and discharging path P_2. To implement the CCM S^2PFC circuits, similarly, the modulation component L_i and C_i can be placed in the charging path P_1 and discharging path P_2. Following the same rules for implementing the 3-terminal feed-forward cells, the same number of 2-terminal feed-forward cells can be developed.

Figure 3.9 shows the family of 2-terminal CCM S^2PFC circuits derived from their general structure in Fig. 3.8 and using the same feed-forward cell implementation rules. Based on the feed-forward components, these cells can be named 2-terminal VS, CS, or VS+CS S^2PFC, etc. Among them, the circuit with the cell shown in Fig. 3.9(d) was proposed as the CCM MS S^2PFC converter [B12]. The circuit with cell shown in Fig. 3.9(b) was proposed by the author of this dissertation in 1997 as a new CCM S^2PFC circuit, and was published in 1998 [C1], while Prof. J. Sebastian also published the same circuit in 1998 [B7]. Other circuits with cells shown in Fig. 3.9(a), (c), (e) and (f) were also published by the author of this dissertation in 1998 [C1] as new CCM S^2PFC circuits. Among them, the circuit with the cell shown in Fig. 3.9(a) seems to be an interesting circuit with good performance.

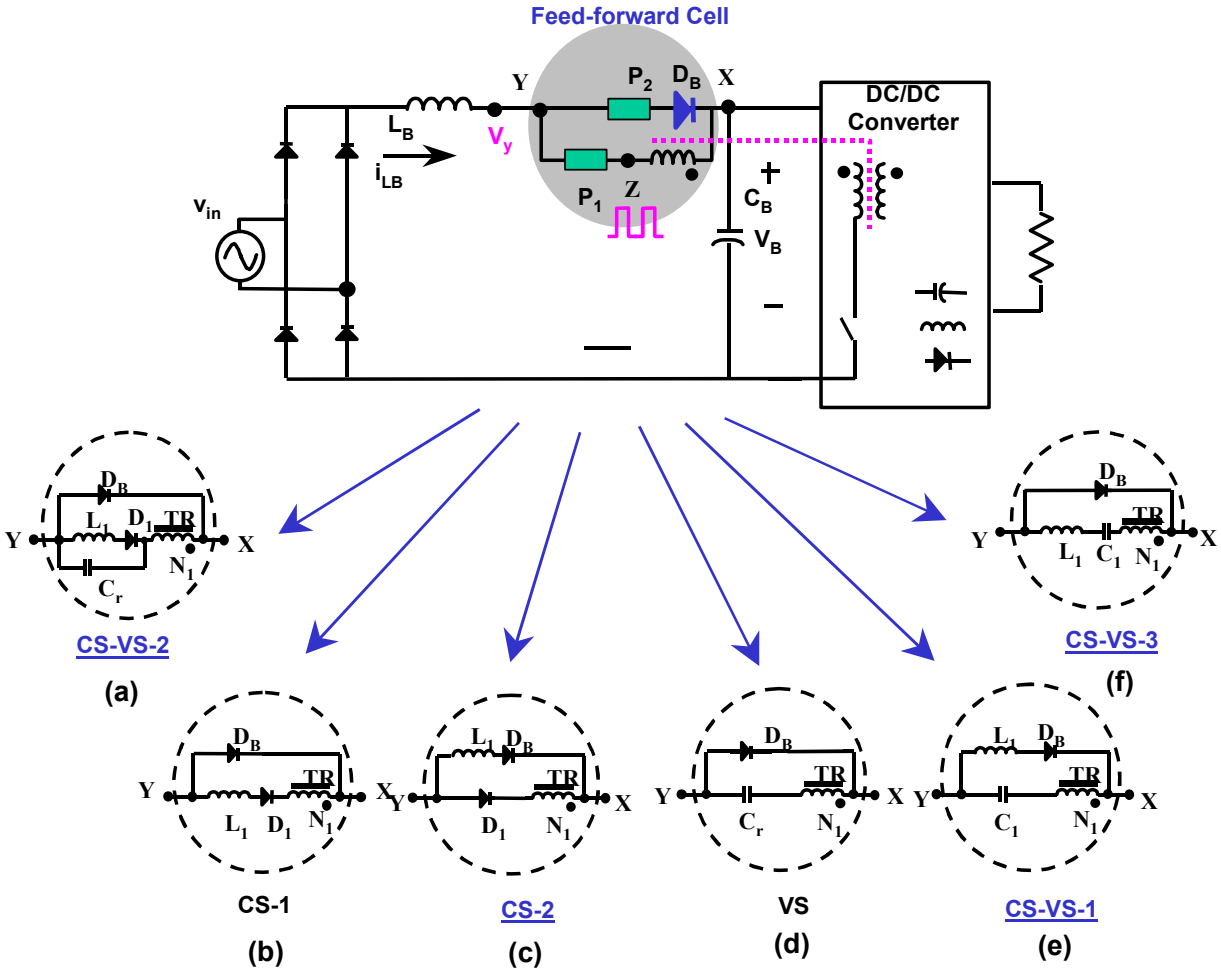


Figure 3.9 Two-terminal CCM S^{2}PFC converter topology variations

3.3.3.2 Bulk-capacitor feedback windings in the 2-terminal S^2PFC converters

Similar to the 3-terminal S^2PFC converters, the 2-terminal S^2PFC converters can also have the bulk-capacitor feedback windings to limit the voltage stress and improve the conversion efficiency. As shown in Fig. 3.10(a), the feedback winding N_1^* can be added into the charging path P_1, while the MS winding $N_1=N_P$ and the feedback winding $N_1^*<N_P$. The feedback ratio is defined as $k=N_1^*/N_P$. Every time when the switch S is turned on, the voltage on winding N_1^* has opposite polarity to the voltage on winding N_1. Thus, the feedback voltage is introduced by N_1^*. Since both windings N_1^* and N_1 are coupled to the DC/DC stage transformer, these two windings in Fig. 3.11(a) can be combined into one winding N_1 in Fig. 3.10(b). In this case, the equivalent feedback winding N_1^* should be defined as:

$$N_1^* = N_P - N_1 \tag{3.3}$$

Of course, in addition to inserting feedback windings in the charging path P_1, another feedback winding N_2 can also be placed in the discharging path P_2 to further improve the performance. Finally, the feedback-winding scheme in the 2-terminal S^2PFC converters has a tradeoff similar to that of the feedback winding in the 3-terminal S^2PFC converters.

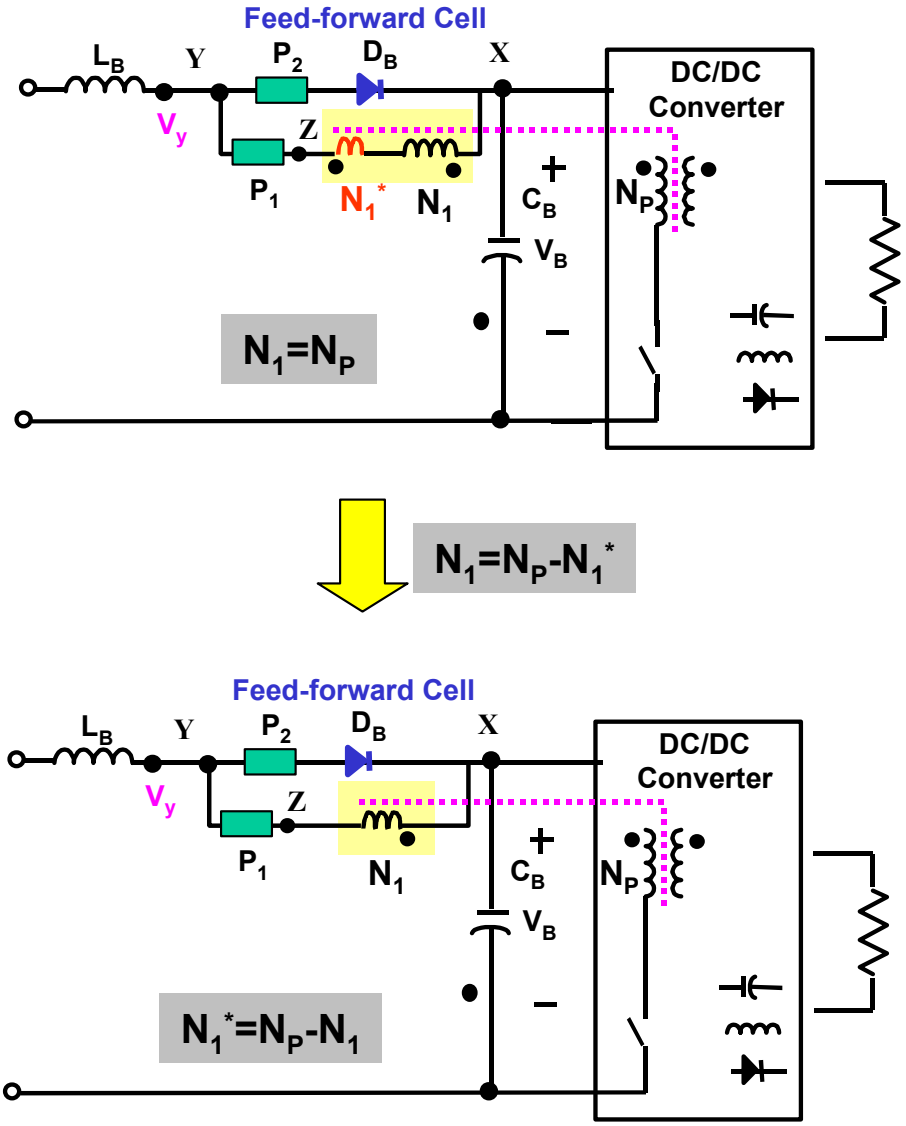


Figure 3.10 Implementing the capacitor-voltage feedback winding in the 2-terminal S^2PFC converter:

(a) Adding the feedback winding N_1^* ($N_1=N_p$, $N_1^*<N_p$),

(b) combining the feedback winding into N_1 ($N_1^*=N_p-N_1$).

3.4 EQUIVALENT RELATIONSHIP BETWEEN THE TWO-TERMINAL AND THREE-TERMINAL S^{2}PFC FEED-FORWARD CELLS

3.4.1 Equivalent two-terminal and three-terminal feed-forward cells

Since the difference between the generalized three-terminal and two-terminal S^{2}PFC converters in Fig. 3.9 is only in their implementations of the switching-frequency signal on the integrated boost rectifier, the 3-terminal and 2-terminal S^{2}PFC converters are equivalent. These families of corresponding feed-ward cells are also equivalent.

Figure 3.11 summarizes the equivalent relationship between the 3- and 2-terminal feed-forward cells. For each pair of equivalent cells, their feed-forward components in P_1 and P_2 are identical in order to achieve the identical performance in the corresponding 2-terminal and 3-terminal circuits. For example, Fig. 3.12 shows the identical switching-cycle waveforms of the 2-terminal and 3-terminal CCM S^{2}PFC converters with current-source cells. Figure 3.13 shows that these two circuits have identical inductor current waveforms during a line cycle.

3.4.2 Experimental verifications of the equivalent relationship

To experimentally verify the conclusion reached in Section 3.4.1, the CS S^{2}PFC converter pairs were selected, as shown in Fig. 3.12. Different from the circuit diagrams in Fig. 3.12, a forward output stage was used. The experimental S^{2}PFC circuits were designed for a 200 W (5-V/40-A), 180–265 V_{rms} line voltage power supply. The major components are as follows: $L_B = 408$ μH, $L_1 = 124$ μH, TR – EER35 core with $N_P = 49$ turns, $N_S = 3$ turns, $N_1 = 25$ turns, $N_1^* = 24$ turns, C_B – 220 μF/450 V, S - IXFH12N100, and secondary-side diodes - 81CNQ045. The reset of the forward transformer was achieved with a reset winding. The switching frequency was 70 kHz. The control circuit was implemented using the low-cost integrated controller UC3825A.

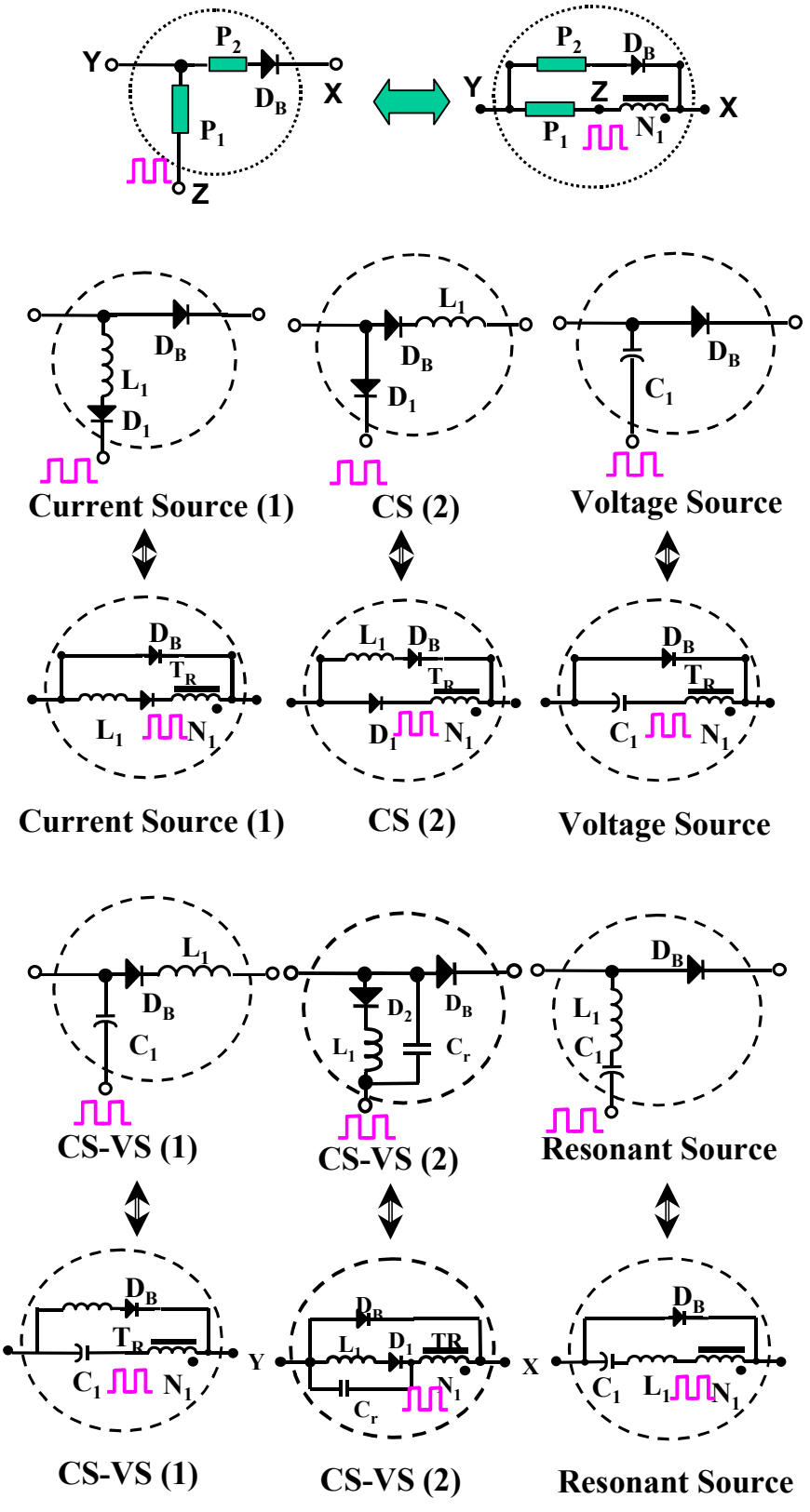


Figure 3.11 Equivalence between the 2-terminal and 3-terminal feed-forward cells.

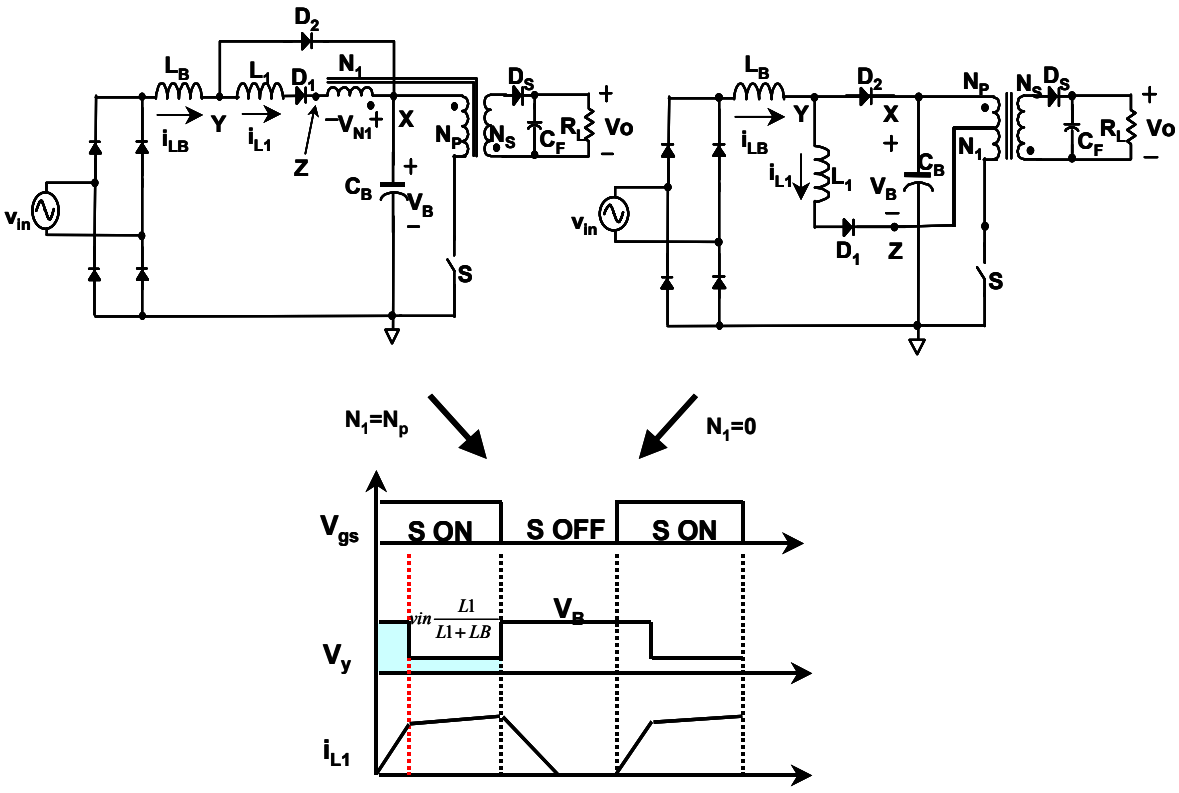


Figure 3.12 Equivalent CCM CS S^{2}PFC circuits and their switching cycle waveforms

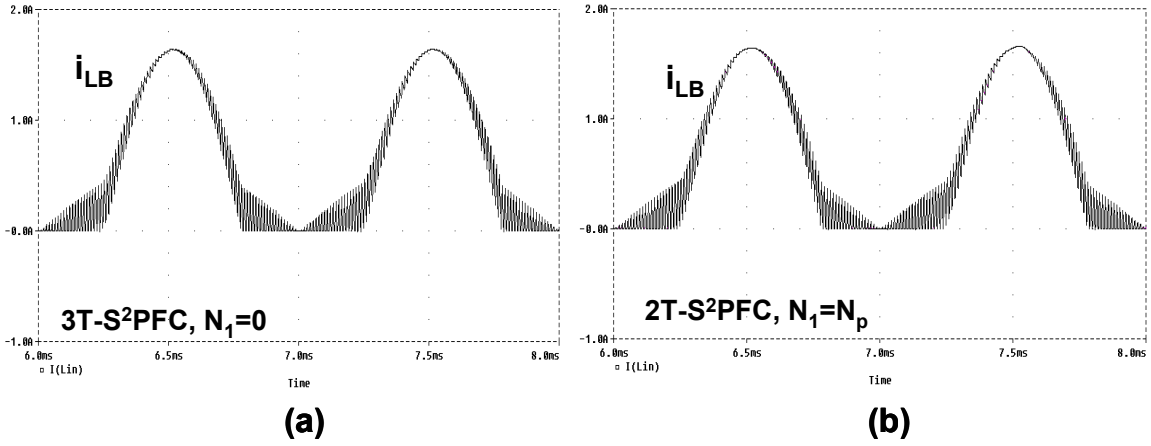
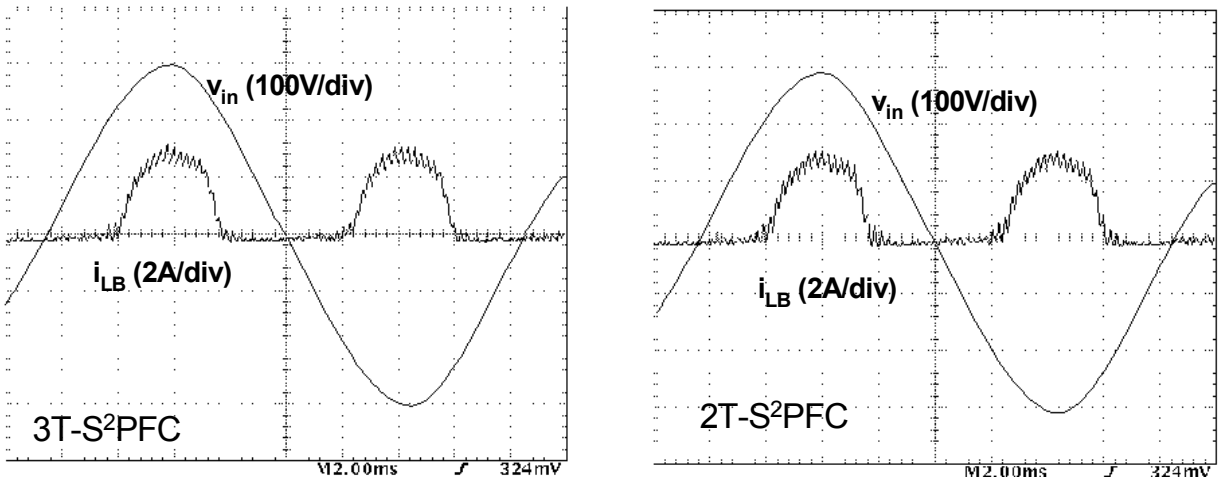


Figure 3.13 Simulated boost inductor current waveforms of:

(a) 3-terminal CS S^{2}PFC, (b) 2-terminal CS S^{2}PFC

Measured line-voltage and boost inductor current waveforms at nominal line ($V_{in} = 230V_{rms}$) and full load ($I_o = 40A$) for both implementations are shown in Fig. 3.14. As can be seen, the line-current waveforms are almost identical. The corresponding line-current harmonics are shown in Fig. 3.15. The harmonic limits for the IEC 1000-3-2 Class D standard are also given in Fig. 3.15. Both implementations satisfy the IEC 1000-3-2 Class D standard with sufficient margins. Comparative efficiency measurements at full load versus line voltage are presented in Fig. 3.16. The difference between the efficiencies of the two implementations is less than 0.5%. Finally, comparative bulk-voltage measurements at maximum line voltage ($V_{in} = 265V_{rms}$) versus load current are presented in Fig. 3.17. For both implementations, the maximum bulk voltage is around 410 V which was obtained at a load current slightly below 10 A.

All the experimental results in Figs. 3.14-17 verify that the two implementations of the selected S^2ICS circuit with 3-terminal and 2-terminal inductive CCM PFC cells exhibit only minor performance differences, which is the result of their slightly different transformer structure and, eventually, the measurement error as well.



(a) (b)

Figure 3.14 Experimental line-voltage and boost inductor current waveforms of the S^2PFC circuit with (a) 2-terminal and (b) 3-terminal ICS cell at nominal line (V_{in} = 230 V_{rms}) and full load (I_o = 40 A)

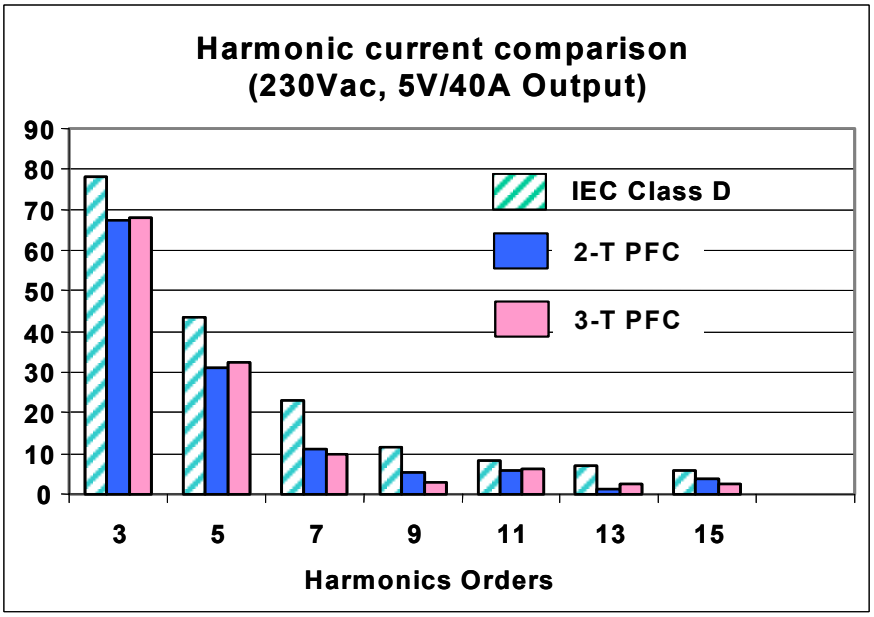


Figure 3.15 Experimental line-current harmonics at nominal line (V_{in} = 230 V_{rms}) and full load (I_o = 40 A)

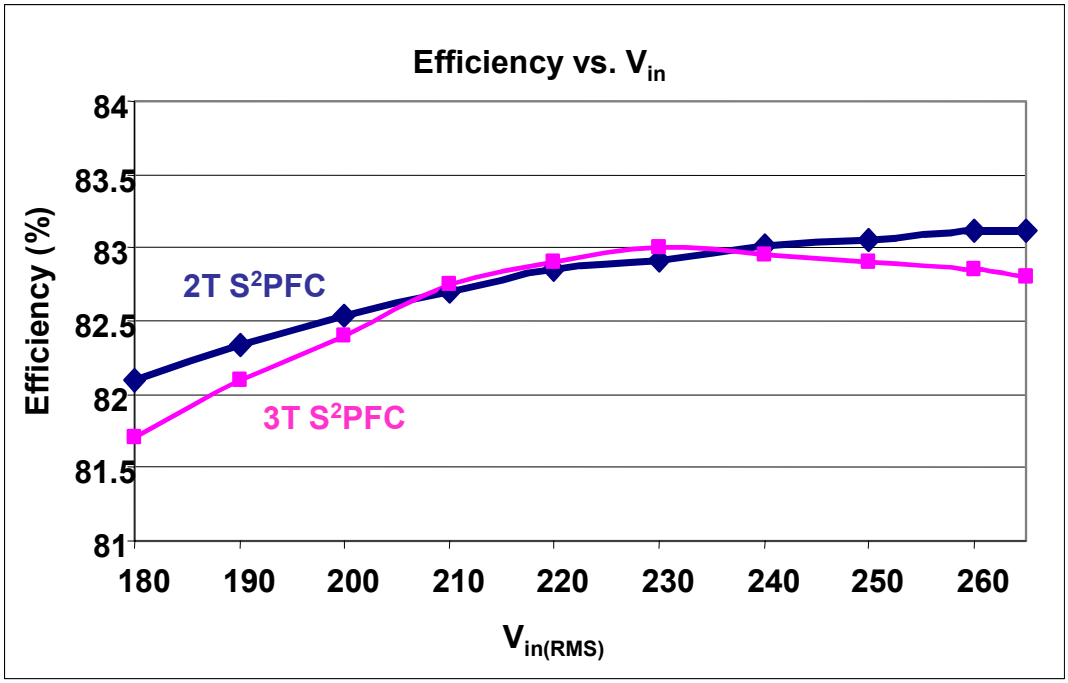


Figure 3.16 Efficiency measurement vs. line voltage at full load (5V/40A output)

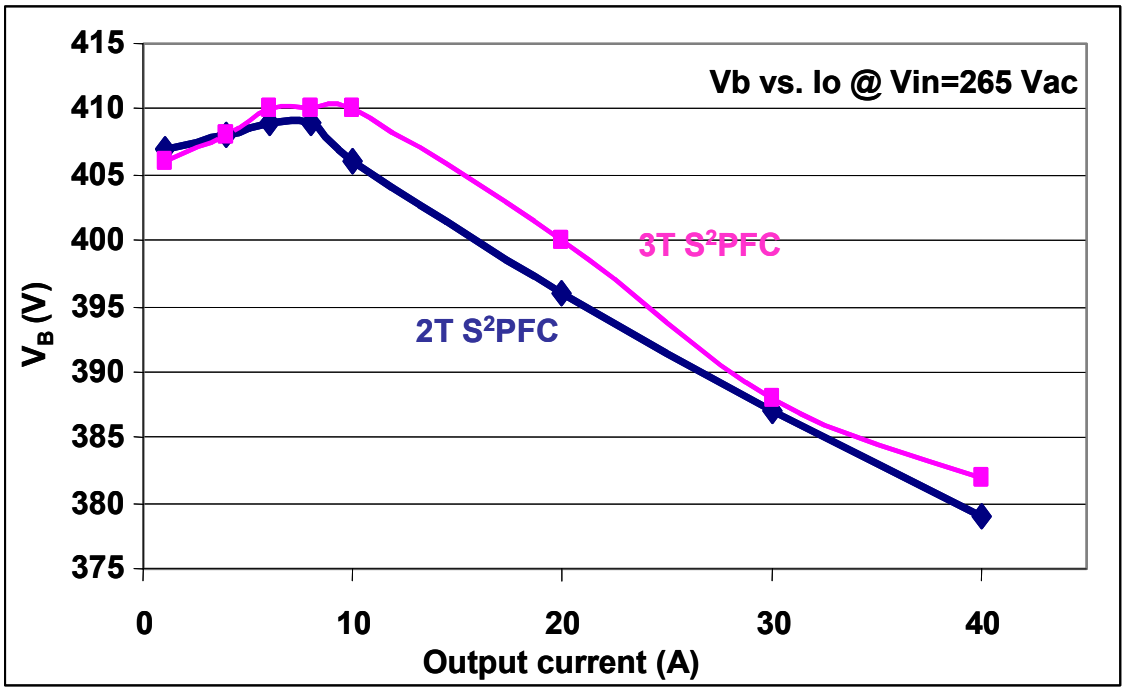


Figure 3.17 Bulk-voltage measurements versus load current at maximum line voltage (V_{in} = 265 V_{rms})

3.5 FURTHER DISCUSSIONS OF DIFFERENT CONVERTER TOPOLOGIES

3.5.1 Two-terminal vs. three-terminal S^{2}PFC converters

Section 3.4 shows that the S^{2}PFC circuits with 2-terminal and 3-terminal PFC cells are functionally equivalent and, hence, they exhibit similar performance. However, there are some differences between them, which will determine different choices of topology.

The major difference between them is related to the transformer design. A S^{2}PFC circuit with a 2-terminal PFC cell requires at least one additional transformer winding (magnetic-switch winding N_1 in Fig. 3.8) and, consequently, it may require a larger transformer than the corresponding S^{2}PFC circuit with a 3-terminal PFC cell if the feedback-winding N_1 is implemented by tapping the primary winding of the transformer.

On the other hand, it should be noted that the S^{2}PFC circuits with 3-terminal PFC cells are limited to single-ended topologies such as the single-switch forward and flyback converters, while the S^{2}PFC circuits with 2-terminal PFC cells can be implemented with any isolated dc/dc converter such as the 2-switch forward, half-bright and the full-bridge DC/DC converters. Therefore, when high output power is required and 2-switch or 4-switch DC/DC stages are necessary, the 2-terminal S^{2}PFC converter will be the only choice.

3.5.2 Current-source vs. voltage source CCM S^{2}PFC converters

3.5.2.1 General discussions

If only one feed-forward component can be used in the PFC cell, as shown in Fig. 3.5(a)-(c), there are only three different choices for the implementations of the charging path P_1 and discharging P_2 in the CCM S^{2}PFC converters. Two of these are CS S^{2}PFC converters, and one is

the VS S^2PFC converter. Figure 3.3 already showed that it is better to put the CS inductor L_1 in the charging path in order to achieve a low input current ripple. The remaining discussion compares the CS S^2PFC and VS S^2PFC converters.

Generally, the high-frequency capacitor C_r is cheaper than the high-frequency L_1, in terms of components and labor cost. However, according to the analysis of the operation principle of the VS S^2PFC in Chapter 2, in every switching cycle, the modulation capacitor C_r must be reset, while the DC/DC stage switch is off. When the flyback converter is used as the output stage, the transformer magnetizing current resets the capacitor voltage. However, if the forward-type DC/DC stage is used as the output, the forward transformer may not have enough magnetizing energy to reset capacitor C_r. As a result, the forward transformer may not have sufficient volt-second to be reset since it always "sees" the capacitor voltage. This could cause the transformer to be saturated and then the forward switch would burn out. This actually happened several times in the experiments. One solution to this problem is adding a large air-gap to the forward transformer to enlarge the magnetizing current in order to provide enough reset energy to C_r. However, this air gap will hurt the DC/DC stage efficiency. As a result, CS S^2PFC may be a better solution for high power applications when flyback converter is not suitable. (For example: $P_o > 100W$)

In terms of efficiency, both circuits have similar efficiency if the flyback converter is used as the DC/DC stage [B6][B13]. When the switching loss is of concern, the capacitor C_r in the VS S^2PFC circuit also works as a snubber to absorb the leakage inductor energy and clamp the switch voltage ringing when switch S is turned off. On the other hand, the inductor L_1 in the CS S^2PFC circuit also offers a good snubber to reduce the boost-diode di/dt and the related reverse-recovery loss when switch S is turned on. However, when the forward converter is used

as the DC/DC stage, the VS S^2PFC has lower efficiency, as shown in Section 3.5.2.2. This reduced efficiency is caused by the air gap in the power transformer in the VS S^2PFC converter.

3.5.2.2 Experimental comparison with narrow input line range

Figure 3.18 shows the 2-terminal CS and VS S^2PFC circuits used for the experimental comparison. Again, the experimental S^2PFC circuits were designed for a 200 W (5-V/40-A), 180–265 V_{rms} line-voltage power supply. The major components are as follows: L_B = 408 μH, L_1 = 124 μH, C_r=5.1 nF, *TR* – EER35 core with N_P = 49 turns, N_S = 3 turns, N_1^* = 24 turns, C_B – 220 μF/450 V, *S* - IXFH12N100, and secondary-side diodes - 81CNQ045. The reset of the forward transformer was achieved with a reset winding. The switching frequency was 70 kHz. In the CS S^2PFC power transformer TR, there is no air gap added, whereas there is a 10mil air-gap in the VS S^2PFC transformer.

Figure 3.19 (a) and (b) show the input voltage and boost inductor current waveforms, in the CS and VS S^2PFC converter, at nominal line voltage (V_{in}=230V) and full load (5V/40A-output). As shown in Fig. 3.19(a), the inductor current waveform of the CS S^2PFC converter has a clear dead-conduction angle caused by the feedback winding N_1^*, where Fig. 3.19(b) also shows the dead-conduction angle on the VS S^2PFC input current, although it is less clear. With the same boost inductance L_B = 408 μH, the VS S^2PFC has a greater inductor current ripple, which indicates that there is more circulating current in the VS S^2PFC converter because the capacitor C_r has bi-direction voltage. Based on the experimental waveform, the VS S^2PFC may need a larger EMI filter, which somewhat compensates for the cost saving of capacitor C_r vs. inductor L_1.

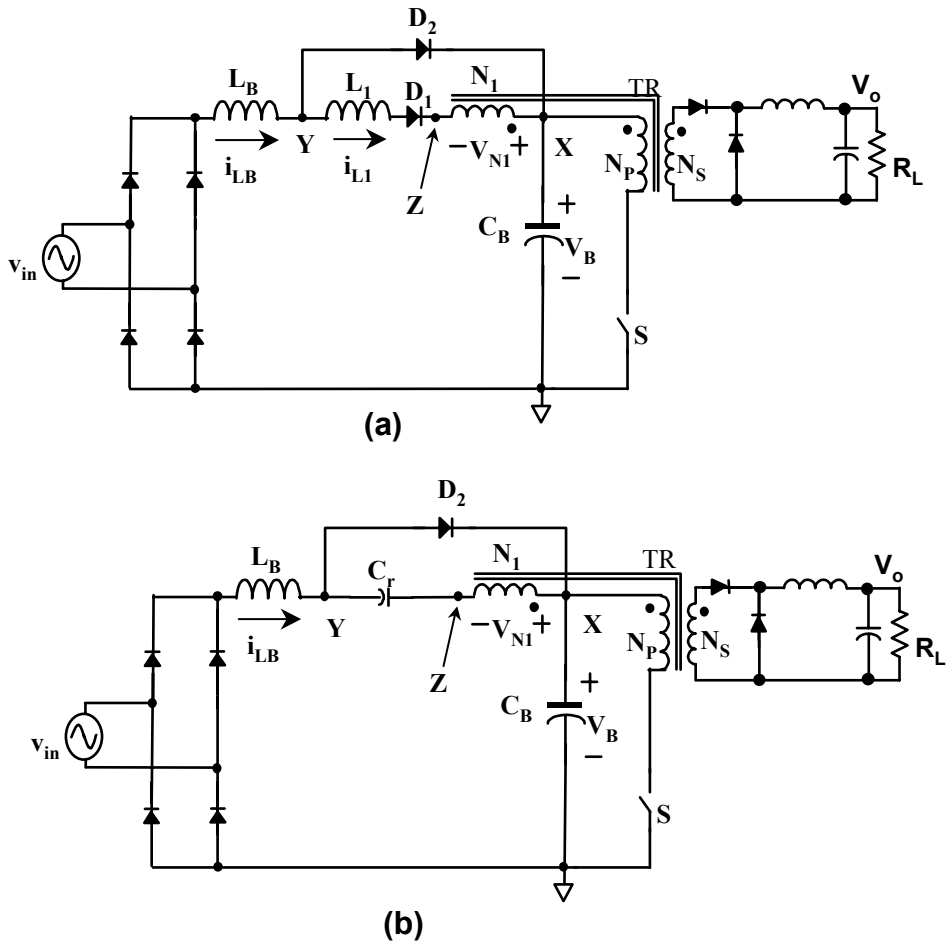


Figure 3.18 VS and CS S²PFC converter for experimental comparison

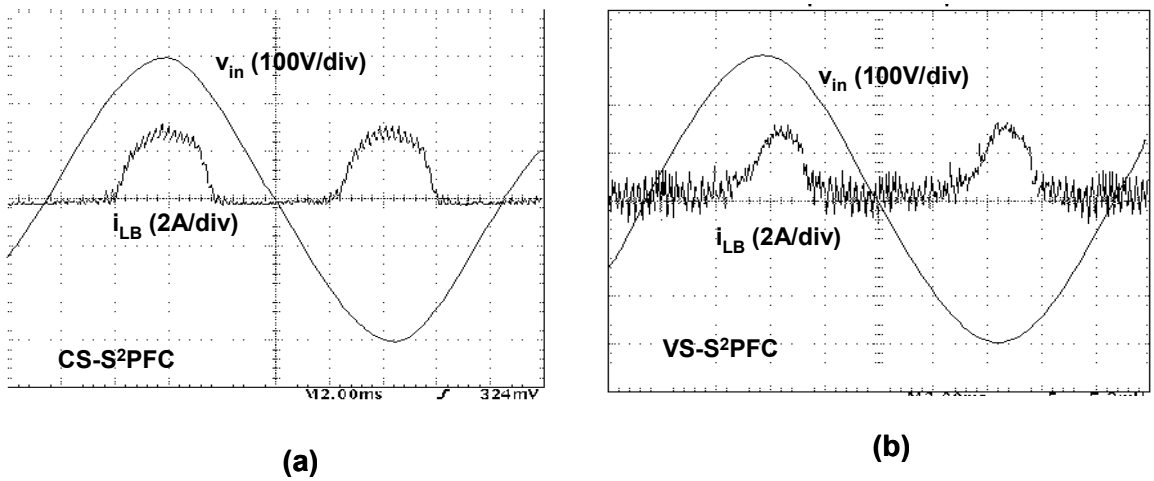


Figure 3.19 Input voltage and boost inductor current waveforms at V_{in}=230V, Po=200W:

(a) CS S²PFC converter, (b) CS S²PFC converter

Figure 3.20 shows the input current harmonics vs. the IEC61000-3-2 Class D standard at the nominal line and full load. Compared to the CS S^2PFC converter, the VS S^2PFC converter has lower 3^{rd} harmonics but higher 5^{th} and 7^{th} order harmonics. In general, these two circuits are designed with similar input current THD at nominal line voltage.

The full-load efficiency comparison shown in Fig. 3.21 indicates that the VS S^2PFC converter is 3-4% less efficient than the CS S^2PFC converter. As discussed, one major reason for the low efficiency of the VS S^2PFC converter is the large air gap in the DC/DC transformer on the forward stage.

Finally, Fig. 2.22 shows the bulk-capacitor voltage stress comparison, at the highest line voltage (V_{in}=265V). Although the VS S^2PFC has slightly higher capacitor voltage than does the CS S^2PFC converter, both circuits have the bulk-capacitor voltage stresses below 450V with sufficient margins for a 450 V-rated electrolytic capacitor to be used.

In summary, the experimental results prove the PFC functionality of both the CS and the VS S^2PFC converters. In addition, the test data shows that the CS S^2PFC converter is a better circuit if a forward converter is used in the DC/DC output stage.

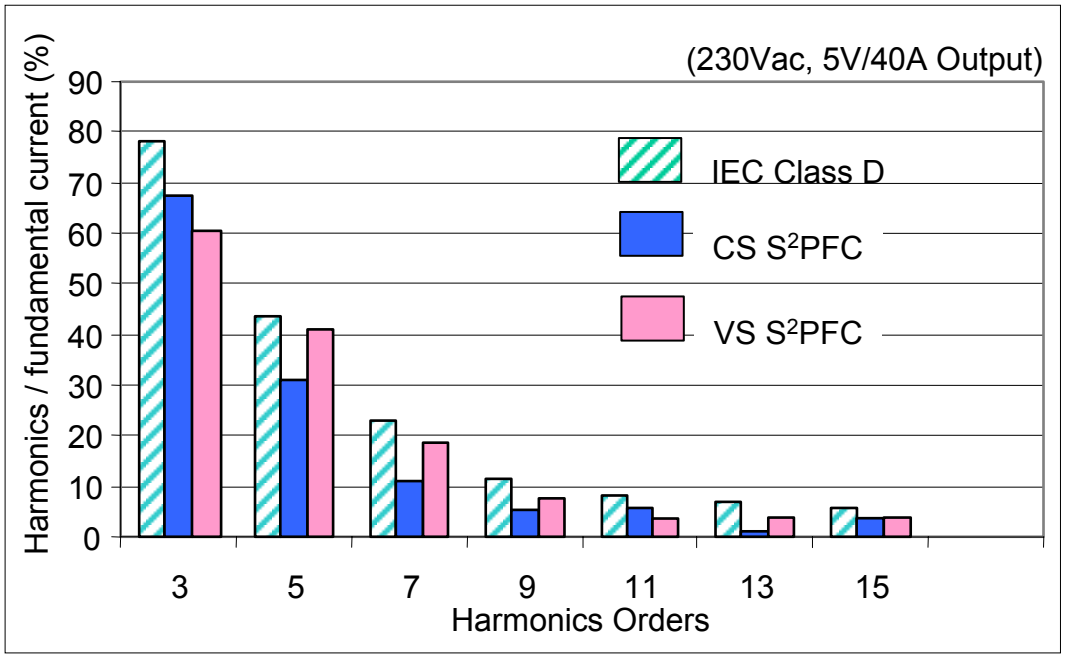


Figure 3.20 CS and VS S^2PFC input current harmonics comparison at V_{in}=230V, Po=200W

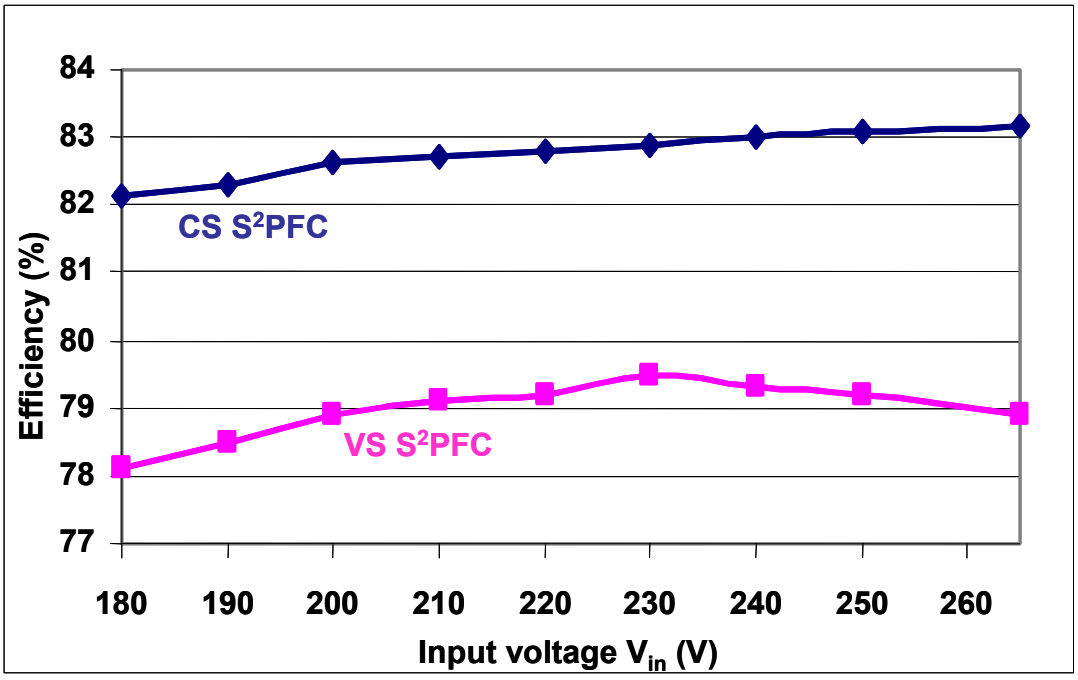


Figure 3.21 Efficiency comparison between CS and VS S^2PFC converters

(with forward output stage at 5V/40A full load)

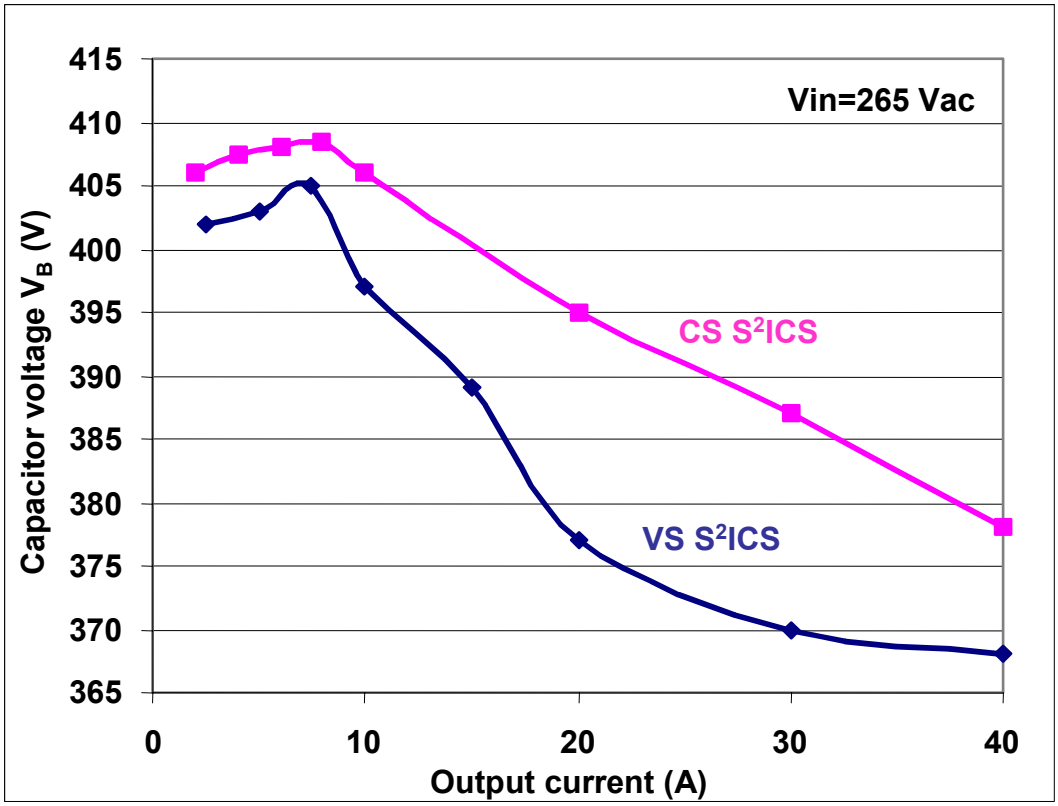


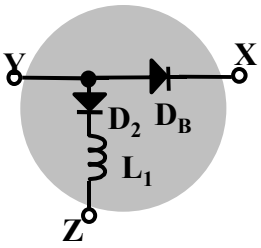
Figure 3.22 Bulk-capacitor voltage stress comparison (V_{in}=265V)

3.5.2.3 Further comparison with **universal-line** input range

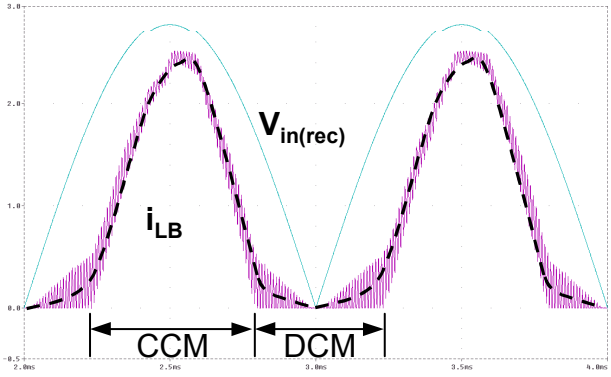
Universal-line input (V_{in} = 90-265 V_{ac}) is required in many applications. To compare the performance of the CCM CS and VS S^2PFC converters for universal-line applications, two circuits have been designed and simulated with the following specifications and parameters: input-V_{in} = 90-265 V_{ac}, output-5V/20A, switching frequency f_S = 100kHz, boost inductance L_B = 500 μH. In the CS S^2PFC converter, L_1 = 250 μH and the forward DC/DC stage with winding-reset scheme is used; while in the VS S^2PFC converter, C_r = 4.7 nF and the flyback DC/DC stage is used. No "feedback winding" scheme is used in either circuit. Both circuits have a closed voltage-loop to control the switch and regulate the output voltage.

Figure 3.23 shows the simulated boost inductor current i_{LB} waveforms of the CS S^2PFC converter with the nominal low- and high-line and full load. As shown in Fig. 3.23 (a) and (b), i_{LB} waveform has both DCM and CCM time intervals during a half-line cycle. With 100 V_{ac} input, i_{LB} has strong CCM current and wide CCM conduction angle, therefore, a nice waveform. However, with 230 V_{ac} input, the DCM angle of i_{LB} increases significantly. There is significant distortion on i_{LB} waveform caused by the imbalance between the CCM and DCM current at high line. As shown in Fig. 3.23(c), the input current harmonics are high at high-line (230 V_{ac}) input, where there are only very small margins for them to meet IEC limits. Furthermore, the input current distortion is even worse at higher input voltage, i.e., up to 265 V_{ac} input. On the other hand, in the designed CS S^2PFC converter, the maximum bulk-capacitor voltage is limited to be lower than 430 V for a 450 V-rated bulk-capacitor.

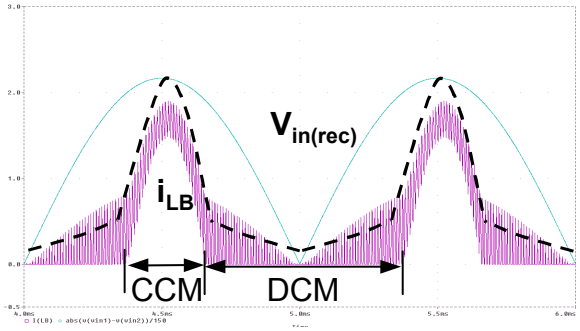
In conclusion, the simulation results show that the CS S^2PFC converter has difficulty meeting the input current harmonics specification at high-line.



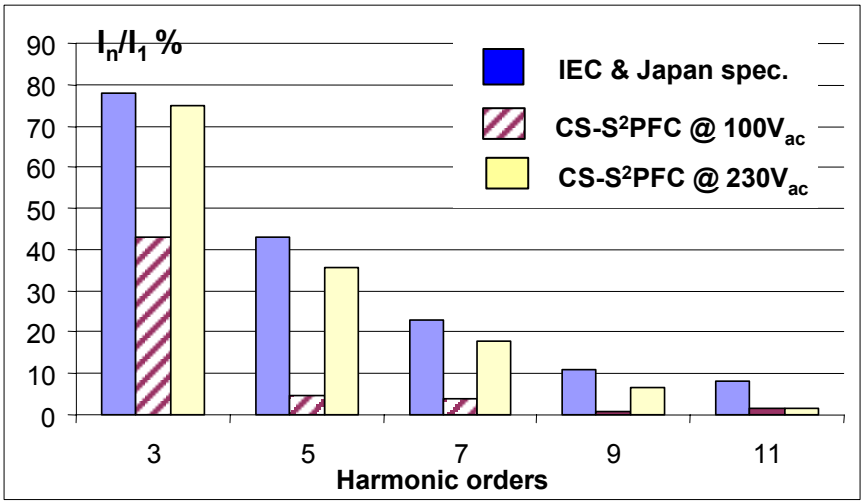
CS-S²PFC



(a) V_{in} = 100 V_{ac}, THD = 41%

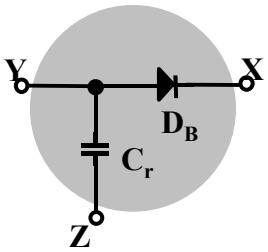


(b) V_{in} = 230V_{ac}, THD = 77 %

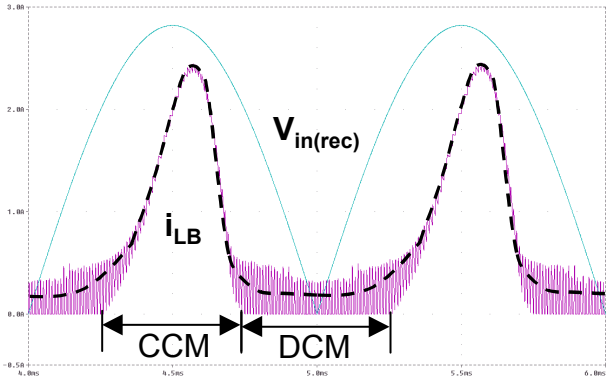


(c) Input current harmonics

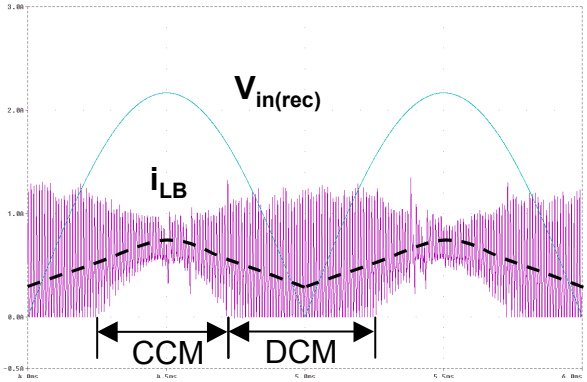
Figure 3.23 Simulated boost inductor current waveforms and harmonics of the CS S²PFC converter. (with universal-line input voltage, forward output stage at full load)



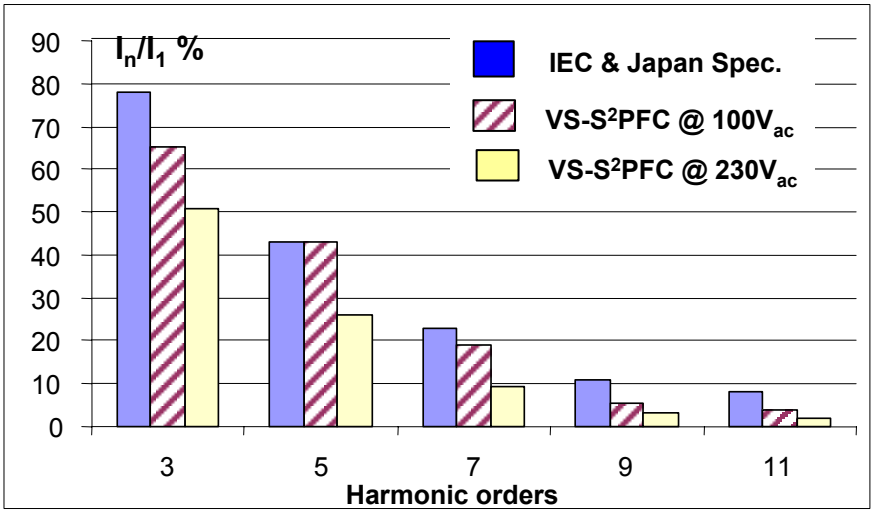
VS-S²PFC



(a) V_{in} = 100 V_{ac}, THD=62%



(b) V_{in}= 230 V_{ac}, THD=32%



(c) input current harmonics

Figure 3.24 Boost inductor current waveforms and harmonics of the VS S²PFC converter. (with universal-line input voltage, flyback output stage at full load)

Figure 3.24 shows the simulated boost inductor current i_{LB} waveforms of the VS S^2PFC converter, at the low and high nominal line voltage and full load. As shown in Fig. 3.24 (a) and (b), the current i_{LB} also has DCM and CCM time intervals with both low and high-line input voltages. However, the DCM angle is only slightly different between the two. Contrary to the CS S^2PFC converter, it is observed that the input current waveform of the VS S^2PFC converter has stronger distortion at low-line input (i.e. $100V_{ac}$) than it does at high-line input (i.e. 230 V_{ac}). In this design, the maximum bulk-capacitor voltage is less than 420 V.

In summary, it is observed from the simulation waveforms that the CCM CS and VS S^2PFC converters have difficulties meeting the input current harmonics specifications with universal line input. Specifically, the CCM CS S^2PFC converter has high distortion on the input current at high line, while the CCM VS S^2PFC converter has highly distorted input current at low line. Figure 3.25 shows the simulated input current THD of both circuits, which also verifies this observation.

3.5.3 Combined CS-VS S^2PFC converter with universal-line input

Inspiration from Fig. 3.25 leads naturally to considering a combination of the CS and VS S^2PFC cell in order to obtain a input current THD curve in between of the curves in Fig.3.25, and meet the harmonics specifications at both low- and high-line input. Figure 3.26 shows one combination of the CS and VS cells, which is also shown in Fig. 3.5(g). In this two-feed-forward-component cell, the CS inductor L_1 and its series diode D_1 are in parallel with the VS capacitor C_r. The following parameters and specifications have been used in the simulation: input 90-265 V_{ac}, output 5V/20A with forward DC/DC stage, L_B = 500 μH, L_1 = 250 μH, C_r = 2.7 nF, f_s = 100 kHz. To limit the bulk-capacitor voltage to below 440 V, a N_1/N_P = 0.23 feedback winding ratio is used.

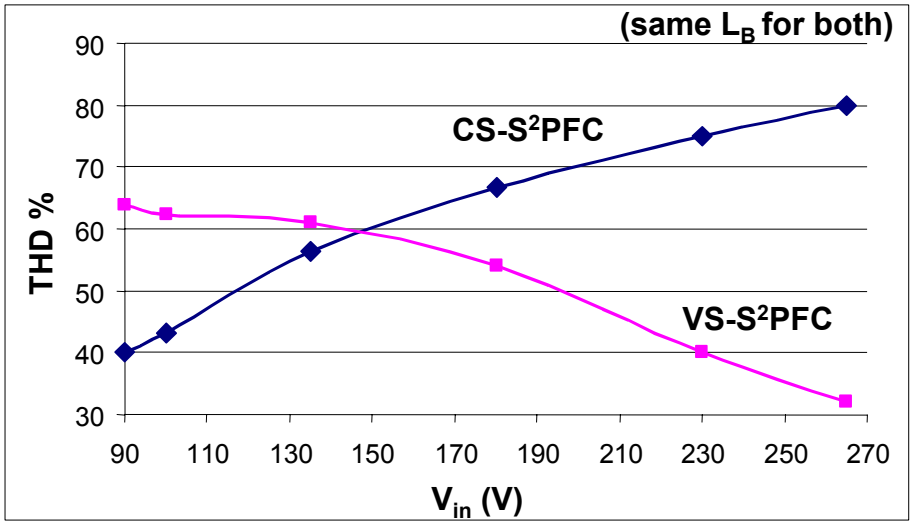


Figure 3.25 Input current THD vs. the input voltage of the CS and VS S²PFC converters.

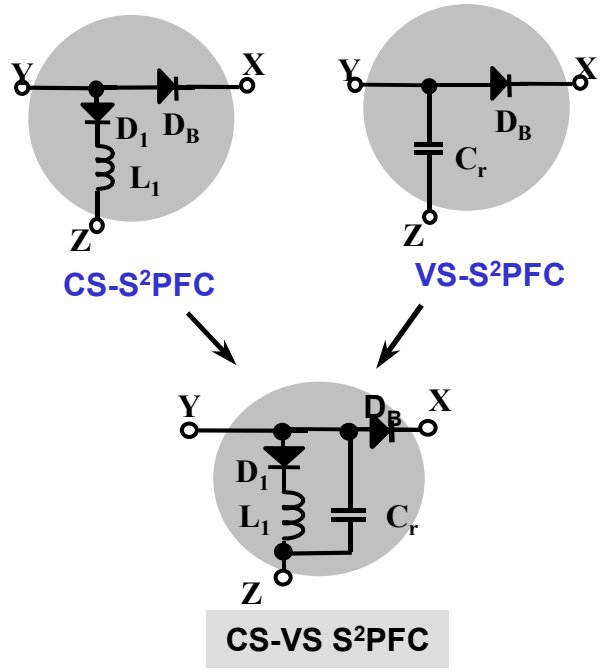
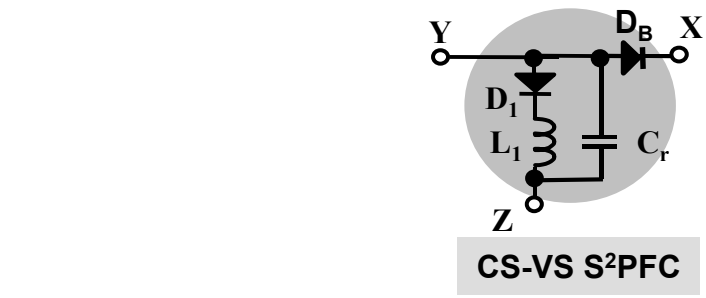
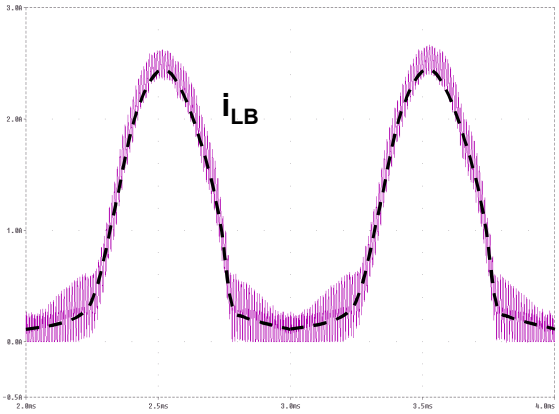


Figure 3.26. Combined CS-VS S²PFC feed-forward cell.

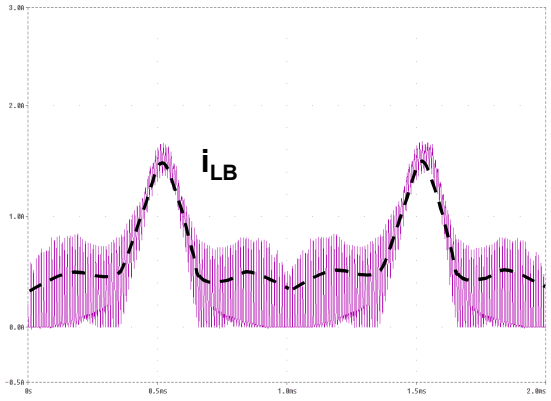
Figure 3.27 shows the simulated boost inductor current waveforms and the input current THD of the combined CS-VS S^2PFC converter. As shown in Fig. 3.27(a) and (b), with 100 V_{ac} input, the boost inductor current i_{LB} of the CS-VS S^2PFC converter has a waveform similar to that of Fig. 3.23(a) of the CS S^2PFC converter, while with 230 V_{ac} input, i_{LB} has a similar waveform as Fig. 3.24(b) of the VS S^2PFC converter. As a result, as shown in Fig. 3.27(c), the input current harmonics of the CS-VS S^2PFC converter have sufficient large margins to meet the IEC and its corresponding Japanese specifications at both the low and high line input. Figure 3.28 further shows that the input current THD curve of the combined CS-VS S^2PFC converter is between the THD curve of the CS and VS S^2PFC converters. On the other hand, the simulated maximum bulk-capacitor voltage is 436 V at 265 V_{ac} input, light load.

In conclusion, with the feed-forward cell shown in Fig. 3.26, the CS-VS S^2PFC converter combines the ICS features of both the CS and VS S^2PFC converters. It offers a better way to meet the harmonic specifications with universal-line input.

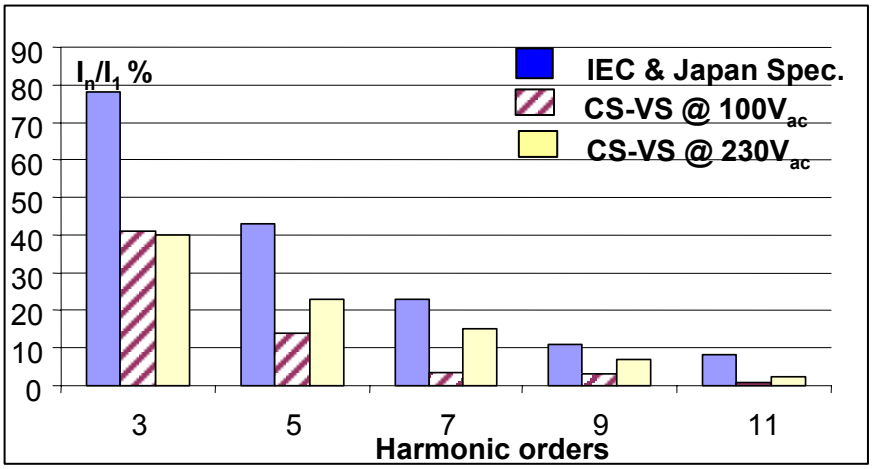




(a) V_{in}=100 V_{ac}, THD = 43%



(b) V_{in}= 230V_{ac}, THD = 60.5%



(c) Input current harmonics

Figure 3.27 Input current and its THD of the combined CS-VS-S²PFC converter

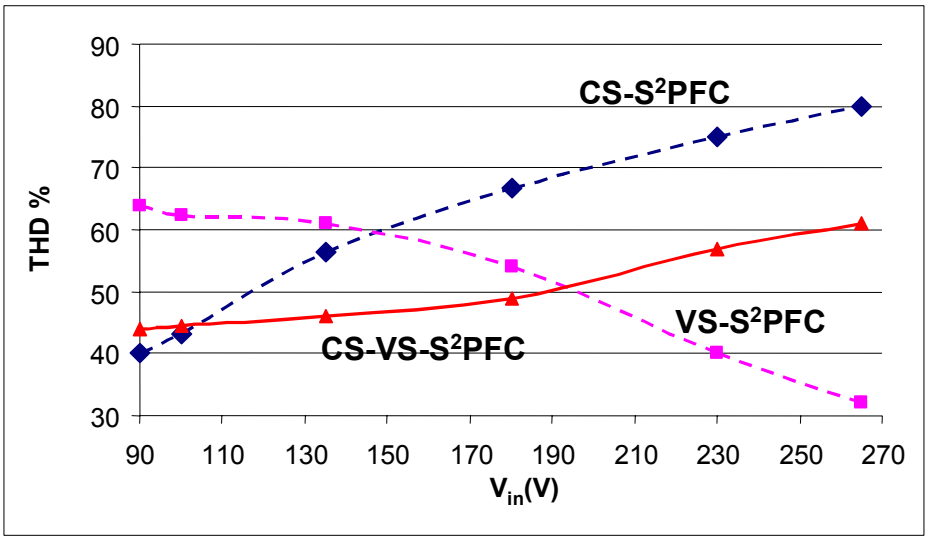


Figure 3.28 Simulated input current THD vs. input voltage of the CS, VS and CS-VS S^2PFC converters.

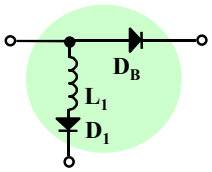
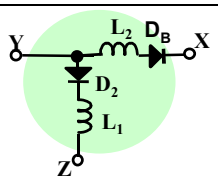
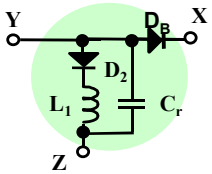
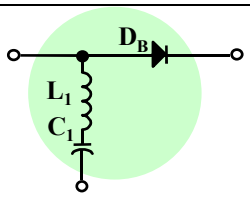
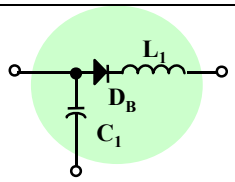
3.5.4. Further comparative study on the S^2PFC with other two-component feed-forward cells

Finally, as shown in Fig. 3.6, when two feed-forward components L_i or C_i can be used in the feed-forward PFC cells, there are several other possible implementations of the new PFC cells. Conceptually, compared to the original CS or VS S^2PFC converters with only one feed-forward component, these new circuits with two feed-forward components should have an improved performance.

Another simulation study on several different two-component S^2PFC has been done to compare the input current of different topologies. To limit the capacitor voltage stress, the bulk-capcitor voltage feedback winding is used. The simulation S^2PFC circuits were designed for a 200-W (5-V/40-A), 180–265-V_{rms} line-voltage power supply, with closed voltage-loop control. Forward DC/DC converter is used as the output stage. For the comparison purpose, some circuit parameters are same in all the cases: L_B = 400 μH, N_P = 49 turns, N_S = 3 turns, N_1 = 17 turns, C_B – 220 μF/450 V, switching frequency f_S=100 KHz.

Table 3.1 summarizes the 6 different cases in this simulation study. The 6 difference cases can be divided into two major groups. Group 1 contains case 1-3 and group 2 contains case 4-6. It is necessary to point out that, to limit the scope of this study, the simulated circuits are operated with narrow line input range, while further study needs to be done with universal-line input applications.

Table 3.1 Simulations circuit parameters and result of the CCM S^2PFC with different cells

Case #	Feed-forward cells	Cell Parameters	Input current THD (%)	Maximum C_B voltage (V)	Input current waveform
Case 1	 CCM CS S^2PFC	$P_1 = L_1$=**124** µH No P_2	**77.5**	**419**	Fig. 3.29(a)
Case 2	 CCM CS-CS S^2PFC	$P_1 = L_1$= **62** µH $P_2 = L_2$ = **62** µH	**75.8**	**424**	Fig. 3.29(b)
Case 3	 CCM CS-VS S^2PFC	$P_1 = L_1$ // C_r L_1=124 µH, C_r = 2 nF No P_2	**67.6**	**435**	Fig. 3.29(c)
Case 4	 CCM VS-CS S^2PFC	C_r = 4.7 nF, L_1= **2**uH (close to basic VS-S^2PFC)	**73.5**	**520**	Fig. 3.29(d)
Case 5	$P_1 = L_1$ series C_r, no P_2	C_r = 4.7 nF, L_1= **62**uH	**64.8**	**470**	Fig. 3.29(e)
Case 6	 CCM VS-CS S^2PFC	P_1 = C_r=4.7 nF $P_2 = L_1$= 62uH	**59.7**	**441**	Fig. 3.29(f)

Group 1 (case 1,2,3):

Case 1 show the CS S^2PFC and its modifications. As shown in Fig.3.29(a), the original CS S^2PFC input current has certain distortion and a dead conduction angle, which is caused by the bulk-capacitor voltage feedback winding. In Case 2, the modulation inductor is spitted into two inductors L_1 and L_2 on the charging and discharging paths, respectively. As a fair comparison, the total inductance of L_1+L_2 in Case 2 is same as the inductance L_1 in Case 1. Figure 3.29(b) shows the input current is close to the original CS S^2PFC input current. Table 3.1 also shows that Case 2 has slightly higher capacitor voltage stress than Case 1. However, in Case 3 if add a small capacitor Cr in parallel with the inductor L_1 and its series diode, the capacitor can provide some current during the previous dead angle, as shown in Fig. 3.29(c). Therefore, the input current distortion is reduced and its THD is also reduced, as shown in Fig. 3.1.

Figure 3.30(a) shows the harmonic comparisons between IEC class D limits and Case 1, 2, 3, at nominal input voltage and full load. It also shows that Case 1 and 2 has similar current harmonics but case 3 has reduced current harmonics. The penalty of adding C_r is the capacitor voltage stress V_B increases from 419 V to 435 V. It reduces the margin if a 450V-rated electrolytic capacitor is used as C_B. Finally, it is necessary to point out further study is needed to understand different circuit operating modes and design trade-off of the circuit in Case 3. This will be the future work of this dissertation research.

As a conclusion, adding a small capacitor C_r in parallel with the CS-inductor L_1 and its diode will improve the input current waveforms.

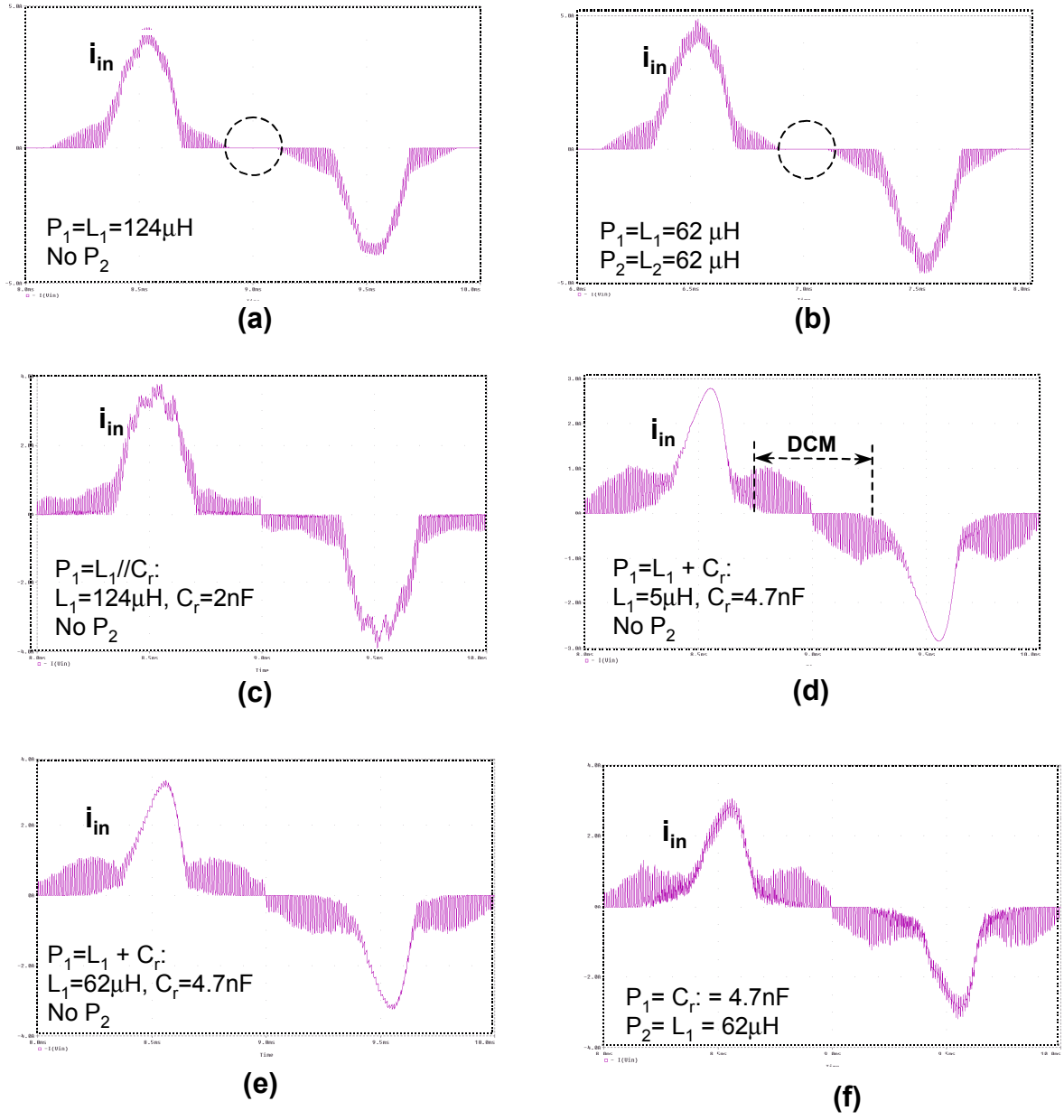
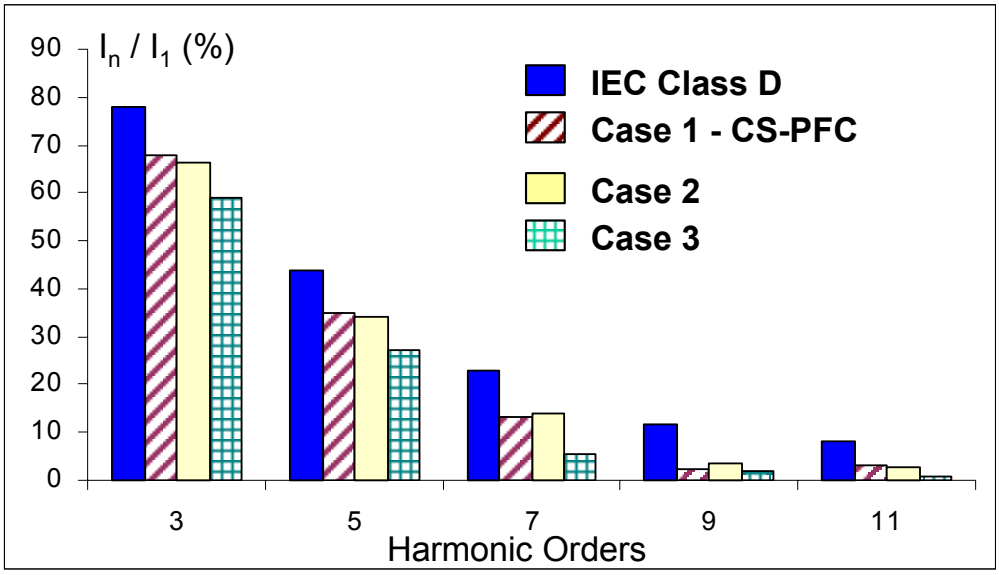
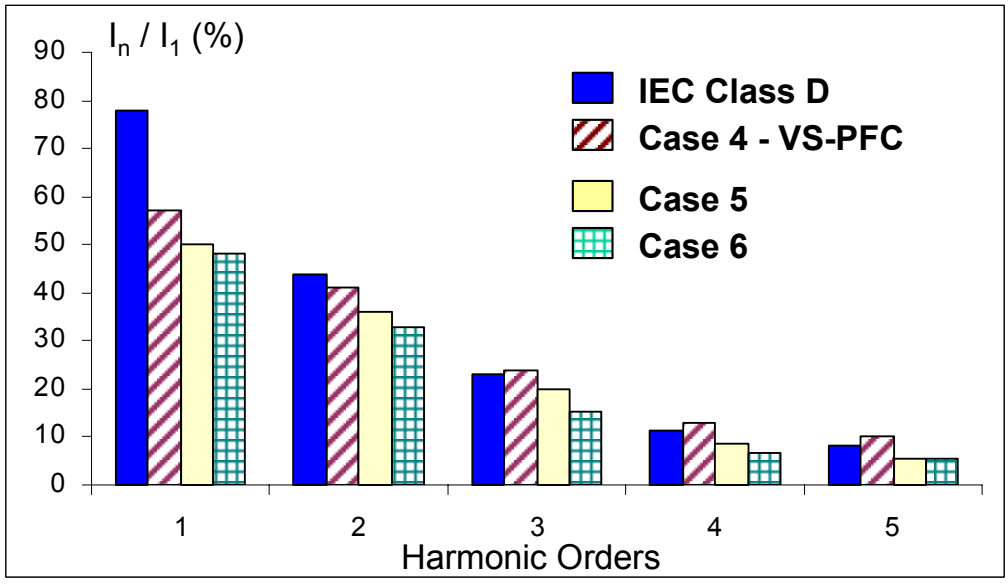


Figure 3.29 Simulated input current waveforms (W/O EMI filter) of different S^2PFC cells

(For study of two-component cells)



(a)



(b)

Figure 3.30 Input current harmonics comparisons of different CCM S^2PFC converters

(For study of two-component cells)

Group 2 (Case 4,5,6):

As discussed in Section 3.5.2, in the VS S^2PFC converter, if the forward converter is used as the output stage, the power transformer has to have an air-gap to provide sufficient current to reset the VS capacitor C_r. As a result, the converter efficiency is hurt due to the transformer air-gap. This problem can be solved by adding a small inductor L_1 in series with C_r, while the transformer does not need an air-gap. The additional inductor L_1 will "see" the voltage difference on the capacitor C_r and the transformer winding N_P, therefore, the transformer can have sufficient reset volt-second.

The modified circuit has a PFC cell, as shown in Case 4, in which the inductance of L_1 is very small. In this case, the performance of this circuit is close to the VS S^2PFC converter. Fig. 3.29(d) shows its current waveforms and Fig. 3.30(b) shows its current harmonics. Due to the VS capacitor Cr, the input current does not have a dead angle even with a feedback winding N_1*. Compared to the CS S^2PFC converter, the VS S^2PFC converter has a lower 3^{rd} order harmonics but higher 5^{th} , 7^{th}, 9^{th}, and 11^{th} order harmonics. In this design, the high order harmonics are higher than the IEC class D standard.

This problem of current harmonics can be solved by increasing the inductor L_1 in case 4 from a small value to a much large value, for example, from 2 μH in case 4 to 62 μH in case 5. By doing this, the input current distortion and harmonics can be reduced to lower than the IEC standard, as shown in Fig. 3.30(b). Case 6 and Fig. 3.30(b) also show that the inductor L_1 can be moved to the discharging path P_2, to further improve the input current without changing L_1 value.

As to the capacitor voltage stress, Table 3.1 shows that with the same boost inductance L_B and feedback winding numbers N_1^*, the VS-S^2PFC converter of Case 4 has the capacitor voltage

stress V_B as high as 520 V at high line (265 V_{ac}) , light load, when forward converter is used as the DC/DC stage. By increasing the inductance of L_r, the voltage stress can be reduced to 470 V, which is still higher than 450 V. V_B can be further reduced to 441 V, by moving Lr into the discharging path. In summary, the simulation results show that Case 6 is the preferred structure among Case 4-6.

Finally, it is necessary to point out that the analysis of the circuit in Case 5 and 6 are quite complicated and the principles are not clear at this time. It can be the future work of this dissertation research.

3.6 SUMMARY

Based on the necessary PFC condition derived in Chapter 2, this chapter further develops the concept of the feed-forward PFC cell and the generalized topologies of the CCM S^2PFC converters. The generalized topologies are represented in the two-terminal and three-terminal S^2PFC structures. Several new CCM S^2PFC cells are developed.

This chapter also presents the equivalent relationship between the two-terminal and three-terminal PFC cells. This equivalent relationship is experimentally verified with a pair of CS S^2PFC converters. After that, this chapter provides further discussions and comparisons among the CCM S^2PFC cells with different feed-forward components. To support the discussion, experimental or simulation results are provided. The simulation results show that one of the combined CS-VS S^2PFC converters have improved input current with universal-line input.