DESIGN AND ANALYSIS OF AN ACTIVE POWER FACTOR CORRECTION CIRCUIT

by

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(ABSTRACT)

The design of an active-unity power factor correction circuit with variable-hysteresis control for off-line dc-to-dc switching power supplies is described. Design equations relating the boost inductor current ripple to the circuit components selection and circuit performance are discussed. A computer-aided design program (CADO) is developed to give the optimal circuit components selection. A 500 watt, 300 volt experimental circuit is built to verify the simulation and analysis results.

The control-to-output response of the power factor circuit is verified with the experimental results. Design guidelines for the low-frequency feedback network are presented. Small-signal closed-loop responses are measured with an experimental power factor circuit.

Acknowledgements

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I. INTRODUCTION

1.1 General Background

Off-line, switch-mode power supplies require an ac-to-dc bridge rectifier, together with a bulk filter capacitor. This bulk filter capacitor is needed to give the specified voltage ripple before the dc-to-dc switching converter and to provide energy storage in case of a line failure. Since the capacitor draws the ac line current only when the capacitor voltage is below the rectified line voltage, the line current pulsates, as shown in Fig. 1.1. This pulsating current causes low power factor and high RMS line current. The harmonics it generates distort the ac line voltage, causing power disturbances in an office environment. Switching power supplies with this rectification process have less than a 0.65 power factor, resulting a low power utilization from the ac line. The high RMS line current places a tremendous stress on the bridge rectifier and the output capacitor, especially at low line.

With increasing demand for more power from a standard 110 - 220 V ac line, it is evident that something has to be done to improve the power usage. A common practice

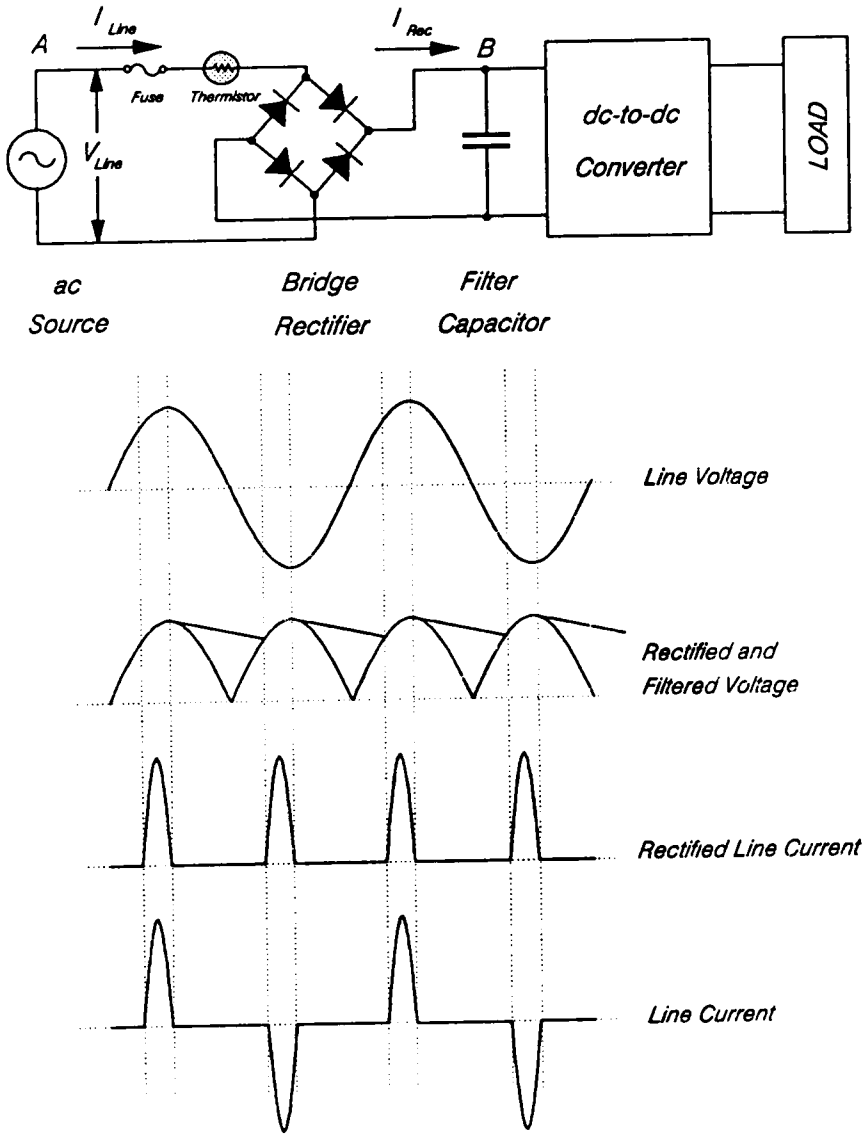


Figure 1.1 Conventional ac-to-dc Rectification and its Associated Waveforms

is to insert a power factor correction circuit between the bridge rectifier and the dc-to-dc converter, as shown in Fig. 1.2. Two types of power factor correction are available today, active power factor correction and passive power factor correction. Passive power factor correction requires one or more large line chokes, but that does not fit well with today's need for compact switching power supplies. The interest in active power factor correction has been growing rapidly in the power supply industry, recently. The primary function of the active power factor correction circuit is to shape the ac line current waveform to exactly match the sinusoidal shape of the ac line voltage. The power factor can be improved to between 0.95 and 0.99 with this process, and the line harmonics can be reduced to less than 3 percent. Other benefits [1][2][3] of the active power factor correction include:

- Full 90 V to 270 V ac line operation without using a voltage doubler.
- Regulated filter capacitor voltage. This results in reduced operating range of the dc-to-dc switching power supply, making it cost effective and more reliable.
- Smaller filter capacitor size.
- Reduced bridge rectifier and filter capacitor current stress.
- High power density.

The active power factor correction circuit discussed in this thesis uses the boost topology shown in Fig. 1.3. This topology is well suited for the power factor correction application, since the boost inductor is in series with the ac line. This minimizes the switching current ripple in the line and the requirements on the input filter. This topology generates a dc output voltage higher than the peak ac line voltage.

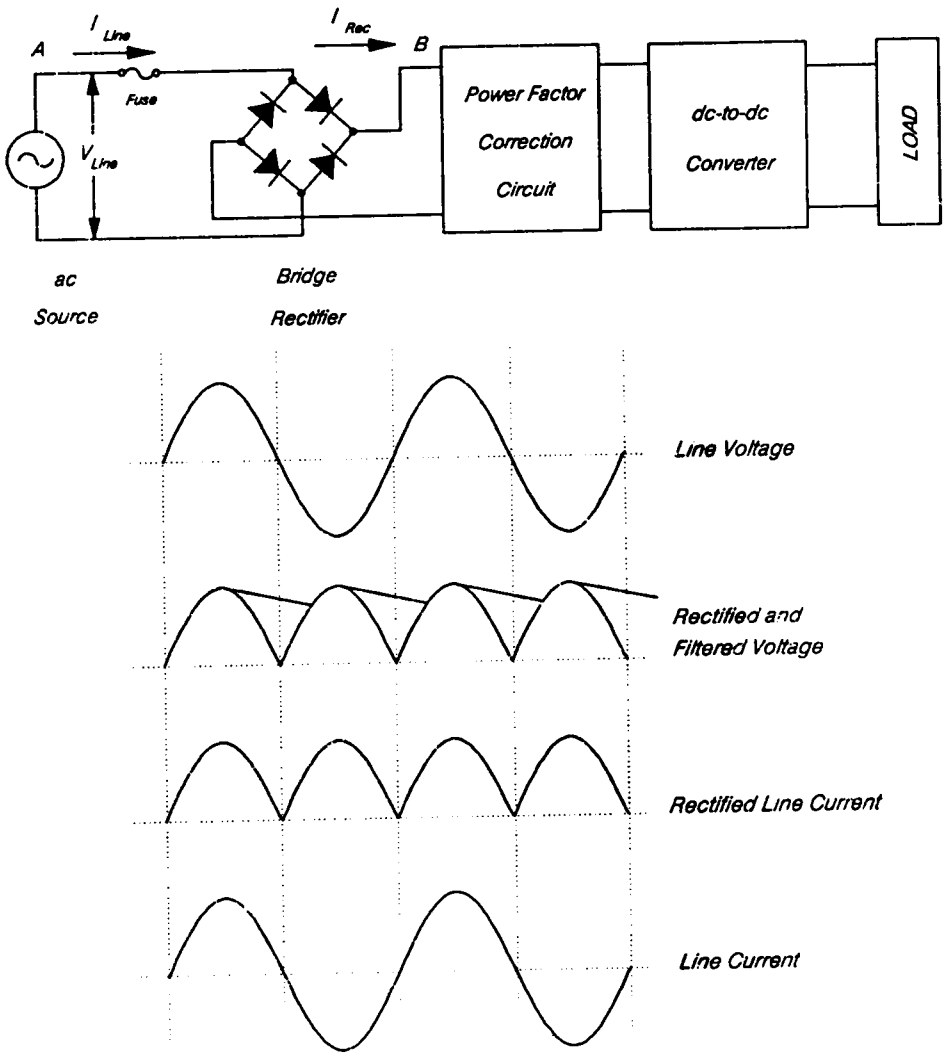


Figure 1.2 ac-to-dc Rectification with Active Power Factor Correction

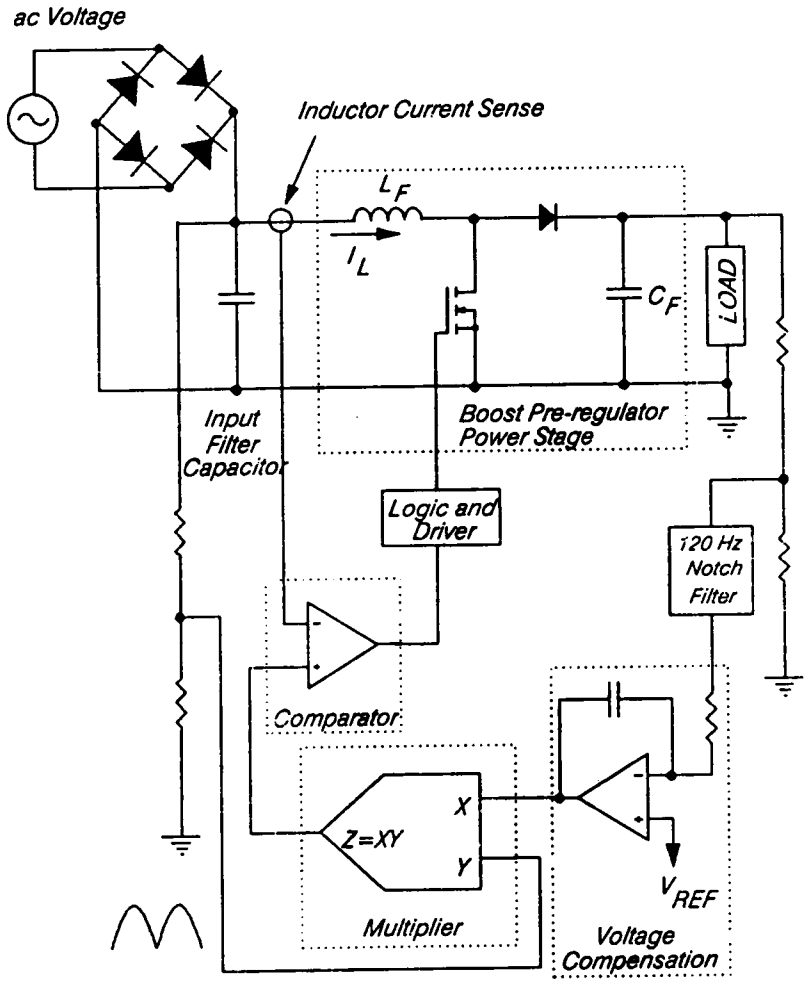


Figure 1.3 Functional Diagram of a Power Factor Correction Circuit

1.2 Operation of the Power Factor Circuit

The active power factor correction can be achieved using two different control methods: variable-hysteresis inductor-current control and constant-frequency inductor current-mode control [3][4][5]. Each has some advantages and disadvantages in terms of performance, complexity, and cost. The choice of control method primary depends upon power level, cost, and the designer's preferences. The variable-hysteresis control has the following advantages:

- Inductor current follows exactly the line voltage, achieving high power factor and minimal harmonic current at any line and load variations.
- Minimal current stress on the transistor when the inductor current operates in continuous conduction mode.
- No external ramp compensation required, as in the constant-frequency operation.

Some disadvantages of the variable-hysteresis control are:

- Current sense. A resistor is inserted in series with the boost inductor, since both the peak and valley inductor current information are required. Care must be applied to reduce noise in the sensed current.
- Circuit operates with variable-frequency, making the design of the input filter more complicated.

The constant-frequency inductor current-mode control is similar to its PWM counterpart. Its advantages are:

- Current sense. Only the peak inductor current information is required. A current transformer inserted in series with the transistor is sufficient.
- Constant-frequency operation.
- Minimal current stress on the transistor when operates in continuous conduction mode.

The disadvantages are:

- Only the peak inductor current exactly follows the line voltage. The average inductor current is distorted at the beginning and end of the half line cycle.
- External ramp compensation is difficult to implement, since the inductor current on-off slope is different at each switching cycle. The external ramp compensation is required for stability considerations for constant-frequency current-mode control with greater than 50 % duty cycle.

Fig. 1.4 shows a comparison of inductor current with variable-hysteresis control and constant-frequency control. It clearly shows that, for constant-frequency control, the inductor current has a higher ripple at the beginning and end of a rectified line cycle. This causes the filtered ac line current to be distorted from the line voltage, resulting a lower power factor and harmonic line currents.

In this thesis, the boost power factor correction circuit with variable-hysisteresis control is discussed. The variable-hysteresis control, as shown in Fig. 1.3 and Fig. 1.5, operates as follows: the inductor current is sensed via a small resistor in series with the inductor and the rectified ac line voltage is sensed with a set of resistive voltage dividers. The sensed rectified line voltage is scaled down to produce the upper and lower inductor current references. The gate-drive logic is designed such that the inductor current switches between these two references. The maximum inductor current ripple occurs at

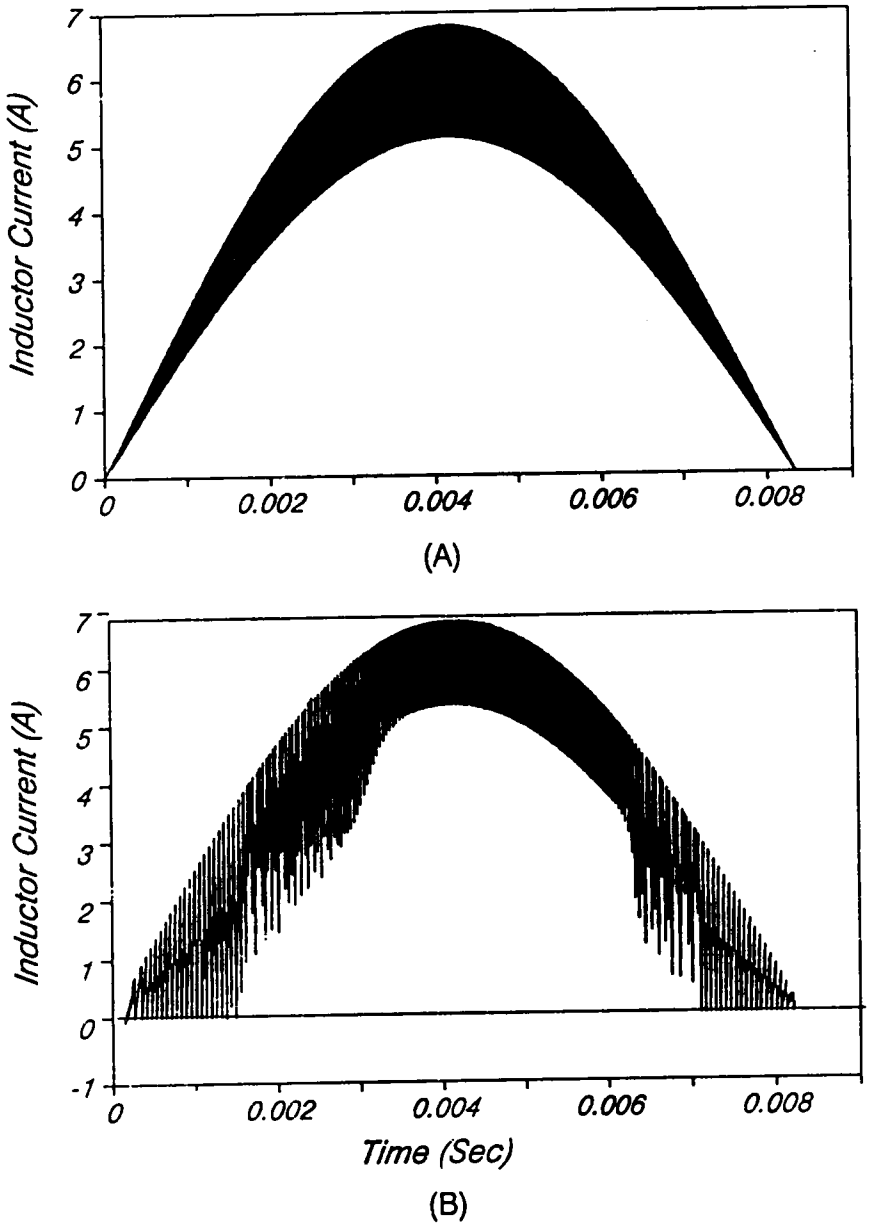


Figure 1.4 Inductor Current Waveforms for Variable-Hysteresis and Constant-Frequency Operations
(A) Variable-Hysteresis
(B) Constant-Frequency

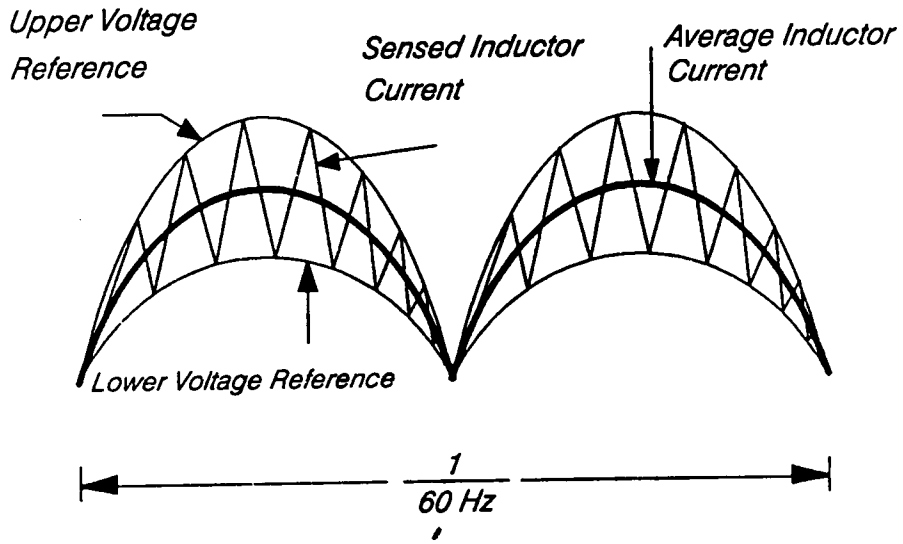


Figure 1.5 Inductor Current Waveform for Variable-Hysteresis Control

the peak rectified line voltage. The error amplifier produces the error signal between the fixed dc voltage reference and output voltage variations. This error voltage is multiplied with the sensed rectified line voltage to set the new upper and lower inductor current references. If the output voltage drops, the error voltage rises and the upper and lower inductor current references rise. This increases the inductor current and raises the output voltage. When the output voltage rises, the error voltage drops and the upper and lower current references also drop, forcing the output voltage to be regulated.

A typical boost power factor correction circuit was simulated on an IBM PC using the program COSMIR [6]. The circuit runs from a single-phase 120 volt RMS line, with an output voltage of 250 volt and an output power of 300 watt. The boost inductance used in the simulation is 3 mH and the output filter capacitor is 100 μF, giving 30 volt of output voltage ripple. The circuit was simulated at two different inductor current ripple percentages: 30 % and 200 %, where the inductor current ripple percentage is referred to as the ratio of the peak amplitude of the inductor current ripple to the peak amplitude of the average inductor current.

As can be seen in Fig. 1 6, the magnitude of the inductor current ripple determines the switching frequency of the correction circuit for a fixed inductor size; the higher the current ripple the lower the switching frequency. The output voltage, which has a 120 Hz ripple voltage, is independent of the speed at which the circuit switches. The output voltage ripple has a 90-degree phase shift with respect to the line voltage. The high-frequency switching voltage ripple at the output is negligible compared to the 120 Hz component. When the transistor is on, its drain-to-source voltage is zero. When the transistor is off, its drain-to-source voltage is the output voltage. At the beginning of a rectified line cycle, the transistor has to be on for a while for the inductor current to reach the upper current reference. The transistor drain-to-source voltage in that period is zero. This is why a white band appeared at the beginning of the second half-line cycle

in the transistor drain-to-source voltage plot in Fig. 1.6. The width of this band is directly related to the size of the current ripple. The upper current reference with 30 % ripple is lower than the one with 200 % ripple, resulting a smaller transistor on-time in that period.

Ripple [4] has derived expressions of transistor RMS current and power factor for constant-frequency inductor current-mode control. In this thesis, an analysis of the boost power factor correction circuit with variable-hysteresis control is performed. Equations for obtaining the duty cycle, transistor on-time, output filter capacitor, RMS inductor current, and RMS switch current are presented. This analysis relates the boost inductor current ripple to the selection of circuit components. The boost inductor current ripple also figures prominently in the expressions of the RMS inductor current, RMS transistor current, and power factor. Although the circuit operates with variable switching frequency, an approximated expression is derived to estimate the switching frequency of the circuit. All the equations results a computer-aided nonlinear design program that selects the optimal circuit components.

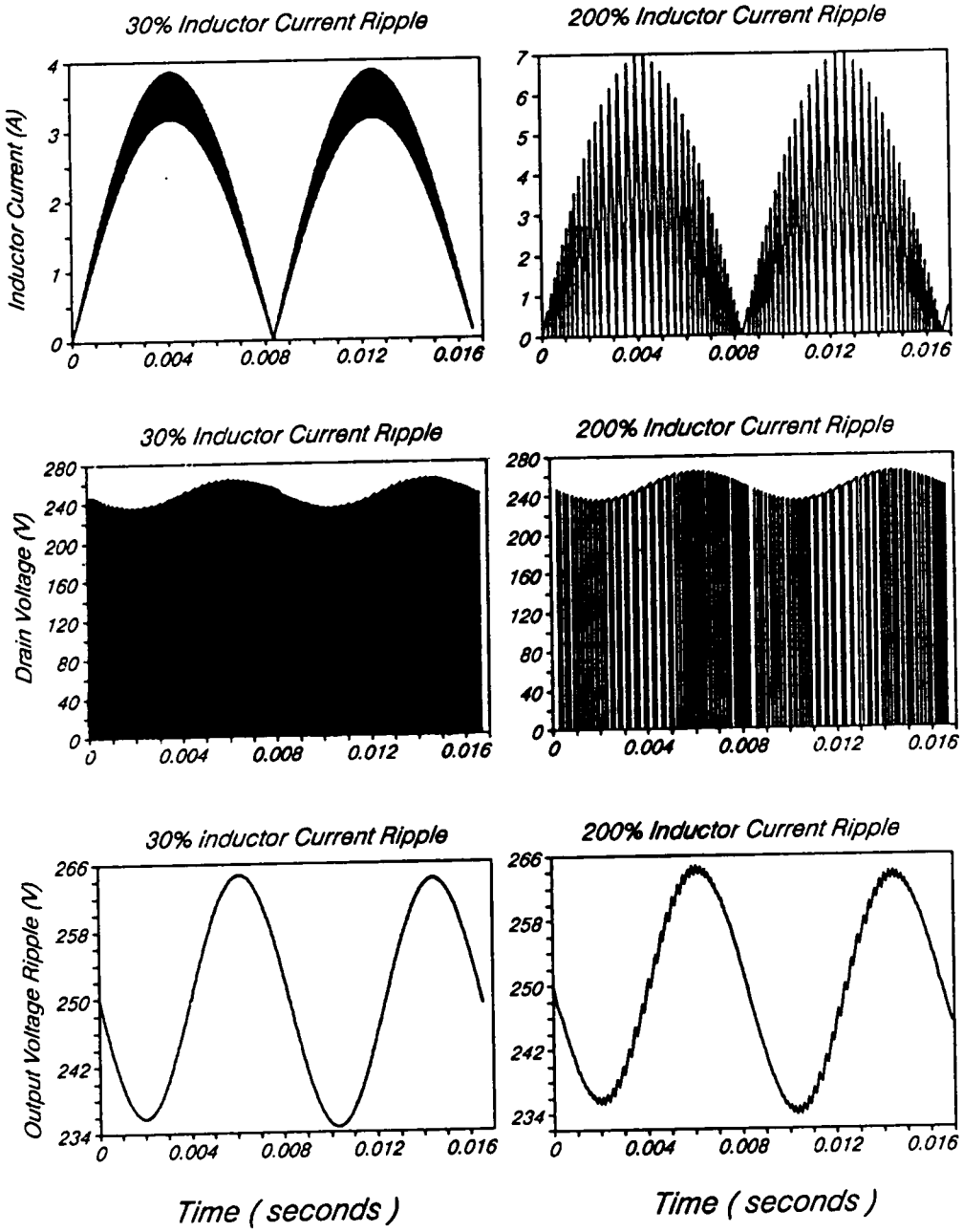


Figure 1.6 Simulation Waveforms of a 300 V, 250 W Power Factor Circuit

II. ANALYSIS OF THE BOOST POWER FACTOR CIRCUIT

2.1 Introduction

To design a boost power factor correction circuit, one must know how to select the boost inductor and output filter capacitor to satisfy a given input-output specification, efficiency and weight requirements. The following quantities will be analyzed for the boost power factor circuit with variable-hysteresis control:

- Duty cycle
- Transistor on-time and off-time
- Output voltage ripple
- RMS switch and inductor current
- Power factor
- Inductor current references

These analyzed results are then incorporated into the nonlinear design optimization program (CADO).

2.2 *Duty Cycle*

The boost inductor current reference waveform within a rectified ac line cycle is shown in Fig. 2.1. The upper and lower inductor current references are obtained from the rectified ac line voltage through a set of resistive voltage dividers. The upper inductor current reference is a half sinusoid, denoted $I_p \sin \omega t$, with a peak amplitude of I_p . The lower inductor current reference is a half sinusoid, denoted $I_c \sin \omega t$, with a peak amplitude of I_c . The average inductor current, which has only the 120 Hz component of an inductor current, is a half sinusoid, denoted $I_m \sin \omega t$. This current is also the line current drawn from the power line after sufficient input filtering. The inductor current ripple is $\delta \sin \omega t$, where δ is the peak current ripple. Since the circuit operates with a much higher frequency than the 120 Hz rectified line, the rectified line voltage is assumed to be constant in each switching cycles.

From Fig. 2.2, the boost power factor correction circuit power stage can be analyzed with two equivalent circuits. Throughout the analysis, two assumptions are made. First, the rectified line voltage, $V_p \sin \omega t$, is assumed constant in an arbitrary transistor switching cycle at time instant t. Second, the period of a transistor switching cycle, t_p, is much smaller than the period of the rectified line cycle.

From Fig. 2.3, in an arbitrary transistor switching cycle with its period, t_p, the inductor current rise within the transistor on-time, t_{on} , at time instant, t, is:

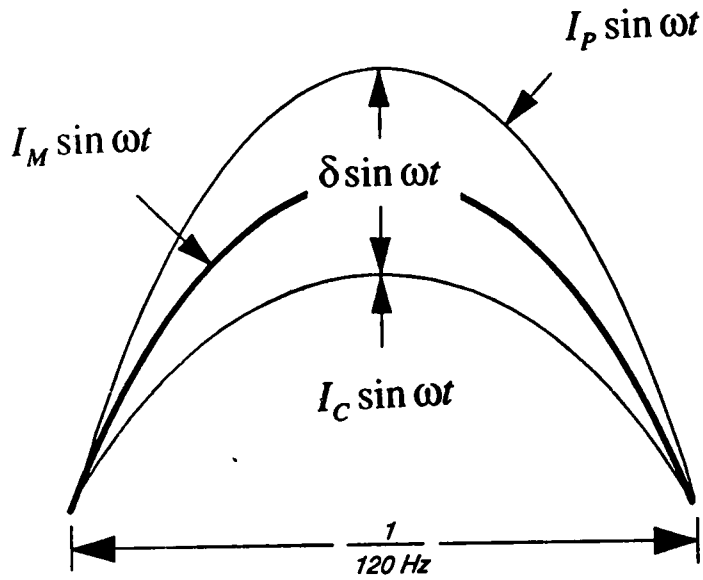


Figure 2.1 Inductor Current References and its Average Current

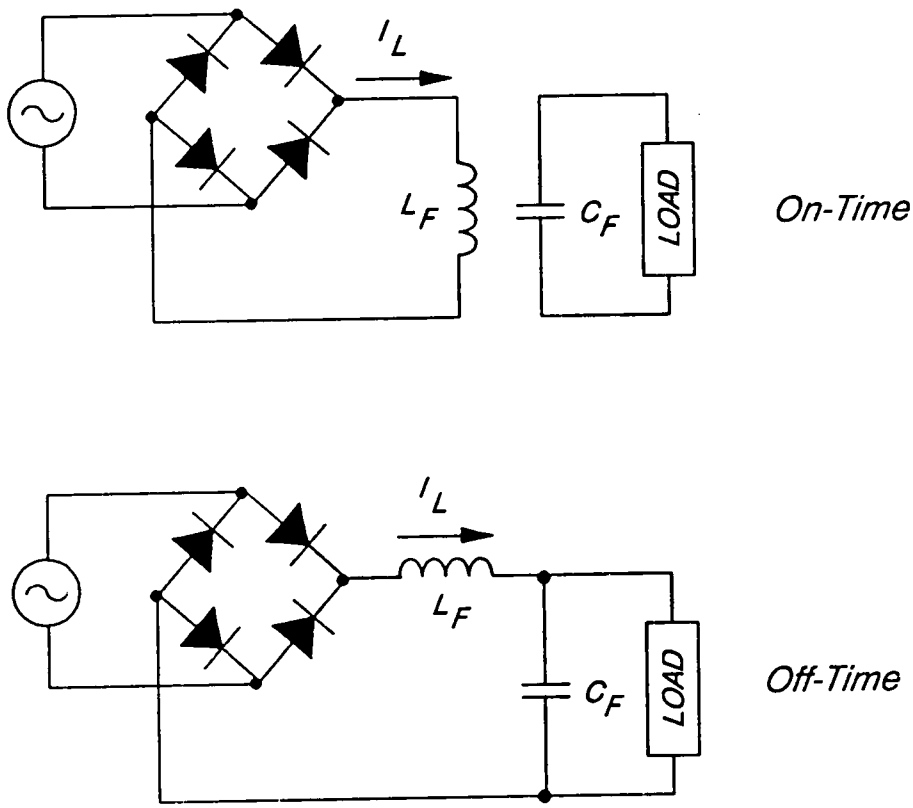


Figure 2.2 Equivalent Circuit of the Boost Power Factor Correction Circuit

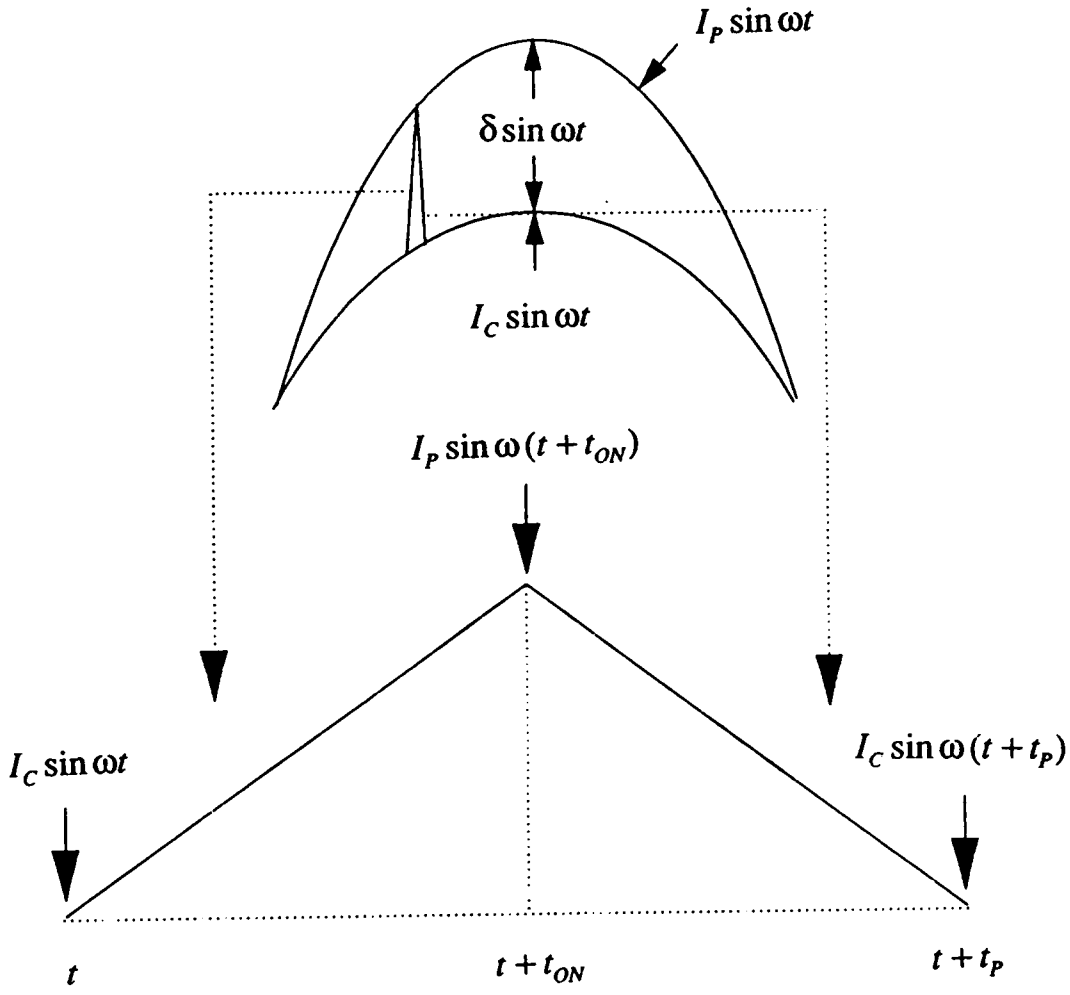


Figure 2.3 An Arbitrary Transistor Switching Cycle

$$\frac{1}{L_f}\int_{t}^{t+t_{on}} V_p \sin\omega\tau\, d\tau = I_p \sin(\omega t + \omega t_{on}) - I_c \sin\omega t \tag{2.2.1}$$

The inductor current drop during the transistor off-time, t_{off}, is:

$$\frac{1}{L_f}\int_{t+t_{on}}^{t+t_p} (V_p \sin\omega\tau - V_o)\, d\tau = I_c \sin(\omega t + t_p) - I_p \sin(\omega t + t_{on}) \tag{2.2.2}$$

By combining Eq.2.2.1 and Eq.2.2.2, and assume t_p is much smaller than the period of the half line cycle, the duty cycle , d, at time instant t , within the 120 Hz half line cycle is obtained

$$\therefore d = 1 - \frac{V_p \sin\omega t}{V_o} \tag{2.2.3}$$

$$\omega = 2\pi f_{line} = 120\pi \tag{2.2.4}$$

where V_p is the peak rectified ac line voltage and V_o is the dc output voltage of the boost power factor circuit. Eq. 2.2.3 shows that the transistor is fully on at the beginning and end of a rectified line cycle, to maintain the power flow from the line to the load.

2.3 Transistor On-Time and Off-Time

The inductor current ripple, δ, and current ripple percentage, Δ, are defined as follows:

$$\delta = I_p - I_c \tag{2.3.1}$$

$$\Delta = \frac{\delta}{I_m} \times 100\,\% \tag{2.3.2}$$

With a specified inductor current ripple, δ, the transistor on-time and off-time can be obtained from Appendix A, section A.1.

$$t_{on} = \frac{\delta L_f}{V_p - \omega L_f I_p \cot \omega t} \tag{2.3.3}$$

$$t_{off} = \frac{\delta L_f \sin \omega t}{V_o + \omega L_f I_c \cos \omega t - V_p \sin \omega t} \tag{2.3.4}$$

A plot of the transistor on-time, t_{on}, at different time instants within the rectified line cycle, is shown in Fig. 2.4. It shows that, at the beginning of a 120 Hz rectified line cycle, the transistor turn-on time has to be longer in order for the inductor current to reach the upper current reference, I_p. At the end of the rectified line cycle, the transistor switches very fast. In real circuit implementation, the transistor is turned off completely, so that the inductor current can pass through at the end of the half line cycle to avoid high-frequency switching. Transistor turn-on time, t_{on}, in the middle of the rectified line cycle, is approximately constant and is expressed by

$$t_{on} = \frac{\delta L_f}{V_p} \tag{2.3.5}$$

Eq. 2.3.5 is an important result, which tells us two things:

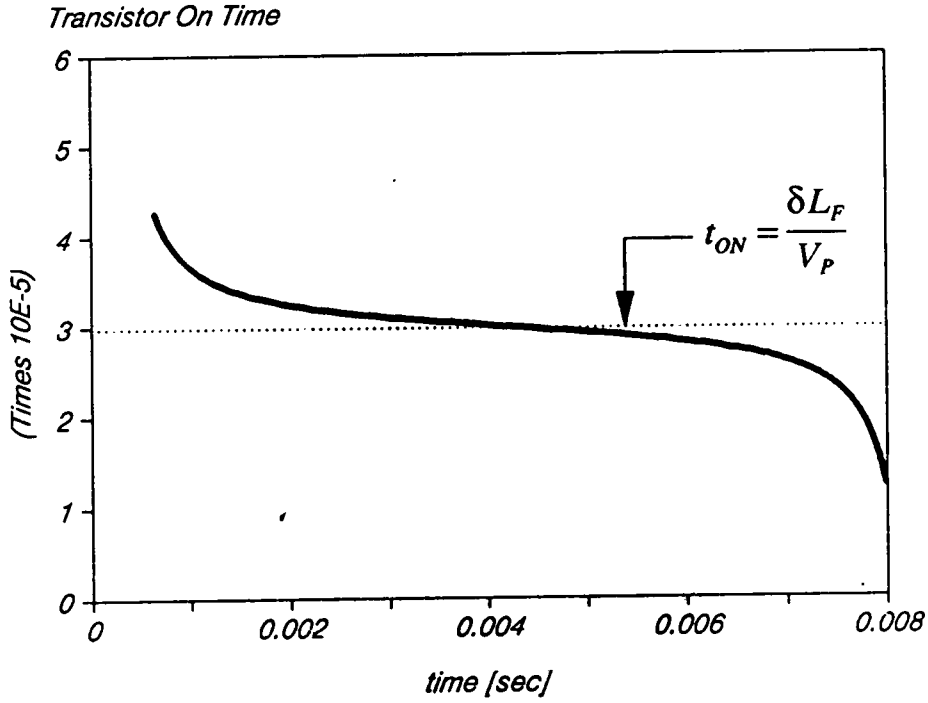


Figure 2.4 Transistor On-Time at Different Time Instants

(1) if the circuit is running at the constant on-time, t_{on} , the upper inductor current reference , I_p, is not required. The transistor is turned on again when the inductor current drops below the lower current reference, I_c.

(2) although the the inductor current is switching at variable frequency. due to the nature of this control, the total number of transistor switching cycles within the 120 Hz rectified line cycle can be approximately determined. This number of switching cycles is approximated by first calculating the total transistor on-time within the rectified line cycle, T_{on} :

$$T_{on} = \int_0^{T_s} (1 - \frac{V_p \sin \omega t}{V_o}) \, dt = T_s - \frac{2V_p}{\omega V_o} \tag{2.3.6}$$

where T_s is the period of the 120 Hz half-line cycle. The number of switching cycles can be approximated by dividing T_{on} and the constant transistor on-time, t_{on} . Thus, we obtain an equivalent switching frequency of the circuit:

$$F_{eq} = \frac{120 V_p}{\omega \delta L_f V_o} (\pi V_o - 2V_p) \tag{2.3.7}$$

F_{eq} is used in the calculation of the transistor switching loss and the magnetic core loss.

2.4 RMS Current

The values of the RMS inductor current and the RMS switch current are required when calculating transistor conduction loss and inductor copper loss. They are evalu-

ated by first calculating their RMS values in one switching cycle, then integrating them over the entire 120 Hz rectified line cycle.

From Appendix A, sections A.3 and A.4:

$$i_{rms}^{sw} = \sqrt{\left[I_m^2 + \frac{\delta^2}{12} \right]\left[\frac{1}{2} - \frac{4V_p}{3\pi V_o} \right]} \tag{2.4.1}$$

$$i_{rms}^{d} = \sqrt{\frac{4V_p}{3\pi V_o}\left(I_m^2 + \frac{\delta^2}{12}\right)} \tag{2.4.2}$$

$$i_{rms}^{ind} = \sqrt{\frac{1}{2}\left(I_m^2 + \frac{\delta^2}{12}\right)} \tag{2.4.3}$$

where i_{rms}^{sw} , i_{rms}^{d} , i_{rms}^{ind} are the RMS switch current, RMS diode current and RMS inductor current, respectively.

From the above equations, we see that both the RMS transistor current and RMS inductor current depend upon the inductor current ripple, δ. A power factor circuit operating in discontinuous conduction mode, i.e., with a 200 % ripple, has the highest RMS transistor and inductor current.

2.5 *Filter Capacitor*

The minimum filter capacitor size, for a given output voltage ripple, can be calculated by integrating the capacitor current $i_c(t)$. From Appendix A, section A.2:

$$\Delta V_o = \frac{1}{C_f}\int_0^{T_s} i_c(t)\,dt = \frac{1}{C_f}\frac{2V_p I_o}{\omega V_o} \tag{2.5.1}$$

$$\therefore C_{pf} = \frac{2V_p I_o}{\omega V_{ripple} V_o} \tag{2.5.2}$$

where V_{ripple} is the output voltage ripple. C_{pf} is the minimal filter capacitance with power factor correction. T_s is the period of the 120 Hz half line cycle.

For a convention ac-to-dc rectification without power factor correction, the exact expression for the filter capacitor is difficult to obtain. However, a simplified expression is:

$$C_{reg} = \frac{I_o T_s}{V_{ripple}} \tag{2.5.3}$$

where T_s is the period of the rectified line cycle. C_{reg} is the minimal filter capacitor without power factor correction.

By dividing Eq.2.5.2 and Eq.2.5.3, we obtain:

$$\frac{C_{pf}}{C_{reg}} = \frac{2V_p}{\pi V_o} \tag{2.5.4}$$

Eq.2.5.4 shows that, the boost power factor circuit filter capacitor, C_{pf}, is approximately 65 % smaller than C_{reg} for the same power level and voltage ripple. Since holdup-time is directly related to the capacitance and voltage, a relationship between C_{pf} and C_{reg} can be made. For the same holdup-time requirement

$$\frac{C_{pf}}{C_{reg}} = \frac{V_p}{V_o} \tag{2.5.5}$$

Having an output voltage V_o higher than the peak line voltage V_p, C_{pf} can be made much smaller than C_{reg} by increasing V_o.

2.6 Power Factor Analysis

From Appendix A, section A.5, the power factor is defined by the following equation:

$$pf = \frac{\frac{1}{T_s}\int_0^{T_s} i(t)\, v(t)\, dt}{V_{rms}\, I_{rms}} \tag{2.6.1}$$

where $i(t)$ and $v(t)$ are the instantaneous line current and voltage. I_{rms} and V_{rms} are the RMS values of the line current and voltage.

From Appendix A, section A.5, the actual power factor of the correction circuit, pf, is related to the inductor current ripple, δ, by the following expression:

$$pf = \sqrt{1 - \frac{\delta}{12 I_m^2 + \delta^2}} \tag{2.6.2}$$

The above equation shows that, the high-frequency switching ripple, $\delta \sin \omega t$, reduces the power factor of the boost power factor correction circuit. Unity power factor cannot be achieved without sufficient input filtering.

To simplify the gate-drive circuit implementation, the circuit is designed so that the transistor remains off at the beginning and end of a 120 Hz rectified line cycle. Keeping the transistor off at the end of the rectified line cycle avoids very high-frequency switching at that point. A certain delay at the beginning of the rectified line cycle also simplifies the circuit implementation. From Fig. 2.5, it can be seen that the power factor will decrease with the longer transistor off-time during that period. A simple expression

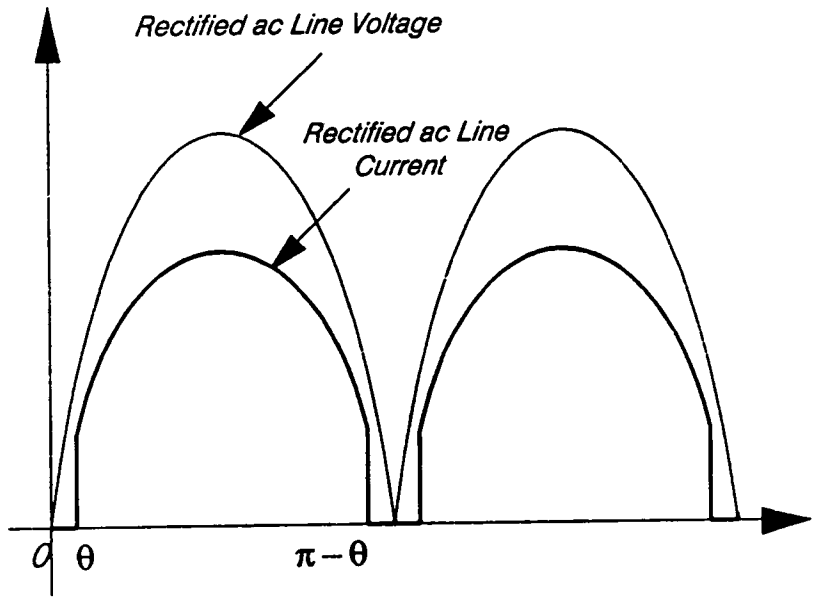


Figure 2.5 Rectified Line Voltage and Line Current with Phase Delay

that relates the power factor, pf, and the amount of phase delay, θ, at the beginning and end of the half-line cycle, from Appendix A.5, is:

$$pf = \sqrt{\frac{\pi - 2\theta + \sin 2\theta}{\pi}} \tag{2.6.3}$$

Fig. 2.6 shows a plot of power factor versus phase delay and current ripple. It shows that, as the inductor current ripple increases, the power factor gets worse. The lowest power factor is 0.86, when the correction circuit operates in discontinuous conduction mode with 200 % current ripple. Also, from the plot we can see that the power factor changed little when the phase delay is below 20 degrees. A 10-degree phase delay is sufficient to avoid high-frequency switching at the end of the rectified line cycle.

A commercial power supply usually has a L-C input filter in front of the power factor correction circuit to minimize inductor current switching noise back into the power line. The size of the L-C filter is directly proportional to the inductor current ripple, δ. A power factor circuit operating in discontinuous mode generates the most switching noise, thus requiring a bigger input filter. It is noted that even in the discontinuous mode, a small input capacitor alone will attenuate the inductor current ripple enough to improve the power factor from 0.86 to 0.99. However, a much bigger input filter is needed to satisfy the line RFI/EMI regulations.

2.7 Inductor Current References

Most of the equations obtained in the previous sections involve the upper inductor current reference, I_p , the lower inductor current reference, I_c , and the average inductor

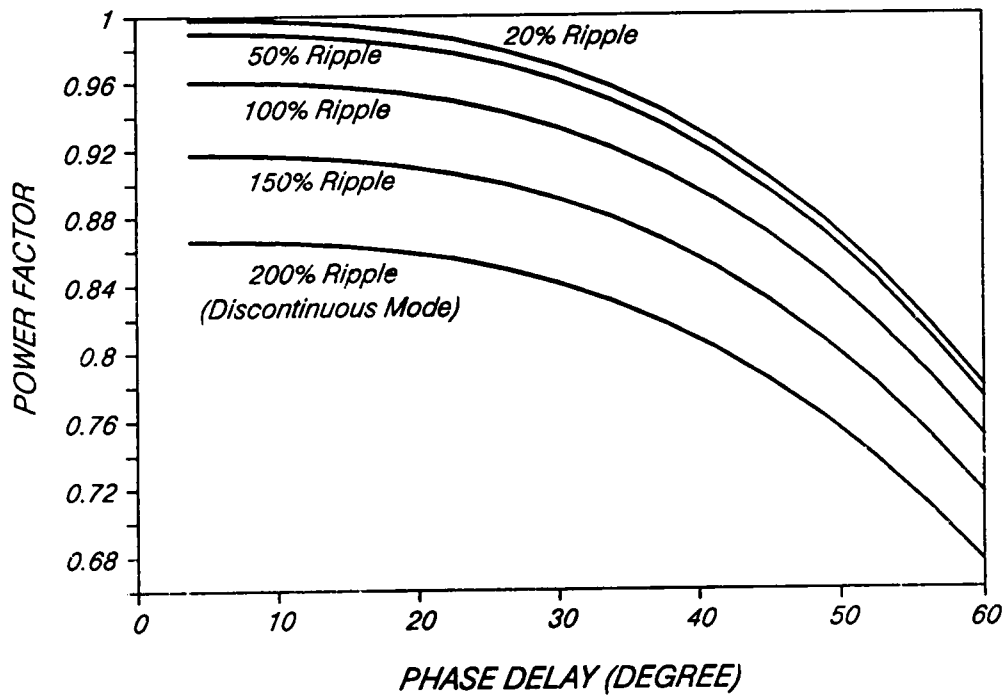


Figure 2.6 Power Factor versus Phase Delay at Different Inductor Current Ripple

current, I_m . This section deals with how to determine the correct I_p , I_c , and I_m for a given input and output specification.

Assume the active power factor correction circuit, through sufficient input filtering, has a unity power factor with an power stage efficiency of η. Then

$$P_{in} = \frac{1}{T_s}\int_0^{T_s} I_m \sin \omega t \; V_p \sin \omega t \, dt = \frac{I_m V_p}{2} \tag{2.7.1}$$

$$P_o = I_o V_o \tag{2.7.2}$$

where I_o and V_o are the dc load current and voltage. Applying power-balance principle

$$\eta P_{in} = P_o \tag{2.7.3}$$

An expression for I_m is obtained

$$I_m = \frac{2 I_o V_o}{\eta V_p} \tag{2.7.4}$$

The upper and lower inductor current references can be approximated as

$$I_p = I_m + \frac{\delta}{2} \tag{2.7.5}$$

$$I_c = I_m - \frac{\delta}{2} \tag{2.7.6}$$

Eq. 2.7.4 to Eq. 2.7.6 indicate that, with a given inductor current ripple, δ, the inductor current references can be easily obtained from the input and output specifications.

III. DESIGN OPTIMIZATION OF THE BOOST POWER STAGE

3.1 Introduction

To design a boost power factor correction circuit, a designer must know how to select the boost inductor, L_f, output capacitor, C_f, and the amount of inductor current ripple, δ, that can be tolerated. C_f is obtained from Eq. 2.5.2 for a specified output voltage ripple, V_{ripple}, but L_f and δ are not so easy to determine. The choice of the inductor size and the amount of inductor current ripple will affect the circuit efficiency and weight. The size of the input filter also increases as δ increases. The nonlinear design optimization routine (CADO) [7] is useful in this type of situation. The routine enables a designer to see the optimal circuit components selection, eliminating the trial-and-error design iterations. A computer-aided design program for power factor correction circuit utilizing this optimization routines will be developed to select the optimal boost inductor size and inductor current ripple.

There are several elements in the nonlinear design program: design variables and constants, design equations, design constraints, and objective function. The detailed description of how these elements work in the nonlinear design optimization routine is provided in reference [7]. In order to apply this nonlinear design routine to the power factor correction circuit, the design variables, design equations, and constraints must be identified and put into the program in their proper forms.

3.2 Design Variables

The design variables are the quantities that are unknown to a designer and have to be selected by the program. For the boost power factor correction circuit, the following elements have been identified as the design variables:

- Efficiency of the power stage, η
- Boost inductance, L_f
- Inductor turns, n
- Wire size, A_{cp}
- Core center-leg width, C_w
- Core window width, W_w
- Inductor current ripple, Δ

For the boost power factor correction circuit, the output filter capacitor, C_f, is determined once the output voltage ripple is given, and therefore it is not considered a design variable here. The majority of the work, therefore, is to optimize the boost

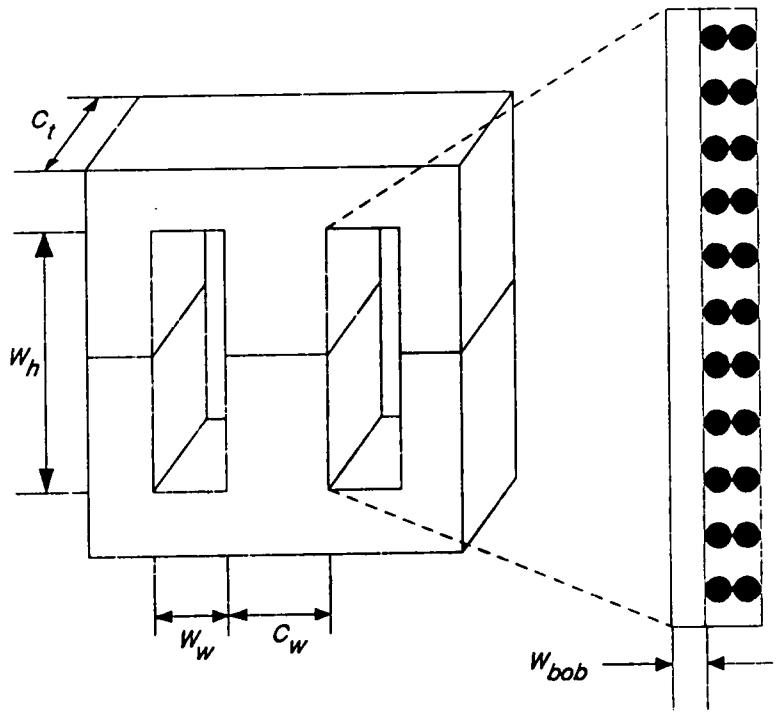
inductor. Fig. 3.1 shows the physical layout of an EE core used for the boost inductor. There are four dimensions to be determined in an EE core: the center-leg width, C_w, the center-leg thickness, C_t, the window width, W_w, and the window height, W_h. Only C_w and W_w are considered design variables, since the core thickness, C_t, is related to the center-leg width, C_w, by a constant, K_1. The core window height, W_h, is related to the window width, W_w, by a constant, K_2. (The value of K_1 and K_2 are usually between 1 and 3 for a given manufacturer's core.) The efficiency and inductor current ripple are also treated as design variables, thus enabling a designer to see the highest efficiency and proper current ripple percentage for a particular design.

3.3 Design Constants

Device characteristics of the active elements, design specifications, and core and wire material parameters are known as the design constants. These include transistor rise-time and fall-time, maximum flux density of the core, core window fill-factor, etc. A list of the design constants and design variables for a 500-watt, 300-volt power factor correction circuit is given in Table I.

3.4 Design Equations

The design equations are used to calculate circuit parameters. Examples of design equations are transistor switching loss calculations and inductor loss calculations. These



$$C_t = K_1 C_W, \; W_h = K_2 W_W$$

Figure 3.1 Core Geometry and Winding Layout of the Inductor

Table I

Boost Power Factor Circuit Power

Stage Variables and Constants

ELEMENT	SYMBOL	DESCRIPTION	VALUE
Transistor IRF740 (MOSFET)	T_r	Turn-on rise time	100 ns
	T_f	Turn-off fall time	150 ns
	R_{ds}	On resistance	0.5 Ω
	C_g	Gate capacitance	1300 pF
	V_g	Gate voltage	15 V
	C_{oss}	Output capacitance	210 pF
Diode	V_f	Forward drop	0.65 V
	T_{drr}	Reverse recovery	50 ns
	T_{dr}	Turn-on rise time	100 ns
	T_{df}	Turn-off fall time	100 ns
Inductor	L_f	Inductance	VARIABLE
	n	Turns	VARIABLE
	A_{cp}	Copper size	VARIABLE
	C_w	Center leg width	VARIABLE
	W_w	Window width	VARIABLE
	B_{sp}	Maximum flux density	0.2 T
	F_c	Winding pitch factor	1.9
	F_w	Window fill factor	0.4
	W_{bob}	Bobbin thickness	1.0 mm

Table I (cont.)

Inductor	K_1	Core leg aspect ratio	1.0
	K_2	window aspect ratio	3.0
	ρ	Copper resistivity	1.72×10^{-8}
	D_c	Copper density	8900 kg/m^3
	D_i	Core density	7800 kg/m^3
Efficiency	η	Specified efficiency	VARIABLE
Current Ripple	Δ	Current ripple	VARIABLE
AC input Voltage (RMS)	E_i	Nominal RMS voltage	120 V
	$E_i\,(min)$	Low-line RMS voltage	100 V
	$E_i\,(max)$	High-line RMS voltage	140 V
Output	V_O	Output voltage	300 V
	P_O	Output power	500 W
	V_{ripple}	Output ripple	20 V

design equations can be any functions of design variables and design constants. In this section, design equations are explained in detail. First, the peak amplitude of the average inductor current is given by

$$I_m = \frac{2P_o}{\eta V_p} \tag{3.4.1}$$

The peak inductor current ripple, δ, is obtained by multiplying the inductor current ripple percentage, Δ, and I_m .

$$\delta = \frac{I_m \Delta}{100} \tag{3.4.2}$$

The upper inductor current reference amplitude, I_p , can be estimated as

$$I_p = I_m + \frac{\delta}{2} \tag{3.4.3}$$

The lower inductor current reference amplitude, I_c , can be estimated as

$$I_c = I_m - \frac{\delta}{2} \tag{3.4.4}$$

The output filter capacitor, C_f , can be calculated as

$$C_f = \frac{2V_p I_o}{\omega V_{ripple} V_o} \tag{3.4.5}$$

Referring to Fig. 3.1, the available window area of the EE core is given by

$$WA = K_2 W_w^2 \tag{3.4.6}$$

The core cross-sectional area, A_p , is

$$A_p = K_1 C_w^2 \tag{3.4.7}$$

The mean-length turn, MLT, of the inductor is

$$MLT = 2(1 + K_1)F_c C_w \tag{3.4.8}$$

The mean magnetic-path length, Z_p , measured through the center leg and around one of the outer leg is

$$Z_p = 2(1 + K_2)W_w + \frac{\pi C_w}{2} \tag{3.4.9}$$

The effective permeability, μ_{eff} , is

$$\mu_{eff} = \frac{L_f Z_p}{\mu_o n^2 WA} \tag{3.4.10}$$

Inductor core air-gap, GAP, can be approximated as

$$GAP = \frac{Z_p}{\mu_{eff}} \tag{3.4.11}$$

The winding build-up, B_w , is given by

$$B_w = \frac{nA_{cp}}{K_2 F_w W_w} \tag{3.4.12}$$

The inductor dc resistance, R_l , is proportional to the mean-length of one turn, MLT , and the copper resistivity, ρ, by

$$R_l = \frac{n\,\rho MLT}{A_{cp}} \tag{3.4.13}$$

The maximum flux excursion in the inductor can be calculated from

$$\Delta B = \frac{\delta L_f}{n\,A_p} \tag{3.4.14}$$

The power factor of the boost power stage, *pf*, is related to the inductor current ripple, δ, by

$$pf = \sqrt{1 - \frac{\delta}{12 I_m^2 + \delta^2}} \tag{3.4.15}$$

The weight of the inductor core, Y_1, is related to ferrite core density, D_l, and its volume, $A_p\,Z_p$, by the following expression

$$Y_1 = D_l\,A_p\,Z_p \tag{3.4.16}$$

The weight of the inductor winding is

$$Y_2 = n\,D_c\,A_{cp}\,XMLT \tag{3.4.17}$$

The equivalent switching frequency of the circuit, F_{eq}, is approximated as

$$F_{eq} = \frac{120 V_p}{\omega \delta L_f V_o}(\pi V_o - 2V_p) \tag{3.4.18}$$

The MOSFET loss, P_q, is the sum of switching loss, conduction loss, gate-source capacitance loss and output capacitance loss. From Appendix A, section A.6

$$P_q = R_{ds}(i_{rms}^{sw})^2(1 - \frac{2V_p}{\pi V_o}) + \frac{1}{2} C_g V_g^2 F_{eq} + \frac{1}{2} C_{oss} V_o^2 F_{eq} + \frac{V_o F_{eq}}{3.6}(I_c t_r + I_p t_f) \quad (3.4.19)$$

The diode loss, P_d , is the sum of switching loss, conduction loss, and reverse recovery loss. From Appendix A, section A.6

$$P_d = \frac{2V_p}{\pi V_o} \frac{P_o V_d}{V_o} + V_o F_{eq} \frac{(I_p t_{dr} + I_c t_{df})}{7.2} + V_o F_{eq} \frac{(I_c t_{drr})}{2.4} \quad (3.4.20)$$

The inductor loss, P_f , includes core loss and copper loss. The core loss expression is derived from reference [7]

$$P_f = R_l (i_{rms}^{ind})^2 + 23.1 A_p Z_p \left[\frac{\Delta B}{3.6} \right]^{2.6} \left[\frac{F_{eq}}{2} \right]^{1.31} \quad (3.4.21)$$

The loss on the full-wave bridge rectifier, P_{db}, is related to the forward voltage drop of the rectifier, V_{db}, and the average line current by

$$P_{db} = \frac{4.0 I_M V_{db}}{\pi} \quad (3.4.22)$$

The efficiency of the boost power stage, η, is expressed by

$$\eta = \frac{P_o}{P_o + P_q + P_d + P_f + P_{db}} \quad (3.4.23)$$

3.5 Design Constraints

In the design of the boost power factor correction circuit, certain physical constraints should never be violated. For example, the magnetic core should never saturate. The design constraints in the CADO are represented by either equalities or inequalities. Some of the design constraints are listed below.

The first design constraint lists the efficiency requirement.

$$\eta \geq EFFUSER \tag{3.5.1}$$

where *EFFUSER* is the user-specified efficiency. This is particularly useful when the minimum efficiency requirement is given in the specification. The program will always give circuit components with this efficiency requirement satisfied. In some cases, if a user-specified efficiency is unrealistically high, the program will tend to select over-sized components.

The second constraint ensures that the winding and bobbin can fit into the available core window area.

$$WA > \frac{n A_{cp}}{F_w} + W_{bob} K_2 W_w \tag{3.5.2}$$

The third constraint prevents inductor core saturation.

$$B_{sp} > \frac{L_f I_p}{n A_p} \tag{3.5.3}$$

where B_{sp} is the maximum flux density of the ferrite core. The fourth constraint shows that the maximum inductor current ripple percentage can not exceed 200 percent, which is the discontinuous conduction mode.

$$\Delta \leq 2 \tag{3.5.4}$$

The fifth constraint limits the maximum efficiency that can be achieved.

$$\eta < 1 \tag{3.5.5}$$

The sixth constraint shows the minimum wire size.

$$A_{cp} > 7.29 \times 10^{-8} \quad (30AWG) \tag{3.5.6}$$

where all the units are MKS systems. The seventh and eighth constraints are related to practical core size considerations.

$$C_w > C_w^{\min} \tag{3.5.7}$$

$$W_w > W_w^{\min} \tag{3.5.8}$$

where $C_w^{\min}$ and $W_w^{\min}$ are the minimum core size for a given manufacturer's core. The minimum inductor current ripple cannot less than one percent.

$$\Delta > 0.01 \tag{3.5.9}$$

The minimum efficiency cannot lower than 50 percent.

$$\eta > 0.5 \tag{3.5.10}$$

the above two constraints avoid the unrealistic design iterations. It also facilitates numerical convergence in using CADO.

3.6 Objective Function

The objective of the boost power factor circuit optimization is to minimize its weight. Since the output capacitor is not a variable to be optimized, its weight is fixed as soon as its capacitance is determined. The only component that affects the weight of the circuit is the boost inductor. For this reason, the objective function is

$$F = Y_1 + Y_2 \tag{3.6.1}$$

where F is the objective function of the boost power factor circuit, Y_1 is the inductor core weight and Y_2 is the winding weight.

3.7 Design Output

The following quantities are printed after running the program. These include final values of the design variables and other useful design information. They are:

- Efficiency, η
- Boost inductance, L_f
- Inductor turns, n
- Wire size, A_{cp}
- Core center-leg width, C_w
- Core window width, W_w
- Output capacitance, C_f

- Inductor weight, F
- Inductor dc resistance, R_l
- Effective permeability and core gap, μ_{eff}, GAP
- Upper, lower, average inductor current amplitude, I_p , I_c , I_m
- Inductor current ripple, Δ
- Peak and RMS switch current, I_p , i_{rms}^{sw}
- Power factor, pf
- Transistor and diode loss, P_q , P_d
- Filter loss, P_f
- Equivalent switching frequency, F_{eq}

3.8 Boost Power Factor Circuit Design Results

The design results of the 500-watt, 300-volt boost power factor correction circuit are given in Table II. In the design, the user-specified efficiency is 95 %, including the diode bridge loss, and the inductor current ripple percentage, Δ, is 30 %. The CADO program was iterated several times until a suitable magnetic core was found. The diode bridge rectifier takes 4.5 watts of power loss. As can be seen from Table II, the MOSFET takes 65 % of the total power stage loss.

The power factor correction circuit can also be optimized over a wide range of inductor current ripples and desired efficiency. Fig. 3.2 shows a plot of boost inductance versus inductor current ripple at the 95 % efficiency. As the inductor current ripple increases, the inductance decreases. The smallest inductance occurs at the discontinuous conduction mode with a 200 % ripple. Running the inductor current in the discontinuous

Table II
Boost Power Factor Circuit
Power Stage Design Results

ELEMENT	SYMBOL	DESCRIPTION	VALUE
Efficiency	η	Efficiency	95%*
Current Ripple	Δ	Current ripple	30%*
Inductor L_f	L_f	Inductance	300 μH
	n	Turns	76
	A_{cp}	Copper size	$1.05 \times 10^{-6} m^2$
	C_w	Center leg width	1.2 cm
	W_w	Window width	1.0 cm
	K_1	Core leg aspect ratio	1.25
	K_2	Window aspect ratio	3.44
	l_g	Air gap	4.5 mm
	R_l	Inductor dc resistance	127 mΩ
C_f	C_f	Capacitor	295 μF
Current	I_p	Upper current reference	6.76 A
	I_c	Lower current reference	5.00 A
	$i_l(RMS)$	RMS inductor current	4.18 A
	$i_s(RMS)$	RMS switch current	3.24 A
	$i_s(PK)$	Peak switch current	8.21 A
Losses	P_q	MOSFET losses	17.1 W
	P_d	Diode losses	500 mW
	P_f	Inductor losses	2.65 W
	P_{Bridge}	Diode bridge losses	4.5 W

* Design variable fixed by the user.

conduction mode, therefore, results in the the smallest inductor size for the given power stage efficiency requirement. This also results in the smallest power stage weight. However, as the input filter required to filter the larger line current and voltage switching ripple increases, the overall weight may not be lighter. Experiments have shown that a small current ripple is much more suitable in high-power applications, when the noise generated by the inductor current is kept minimal.

Fig. 3.3 shows a plot of boost inductance versus efficiency at 30 % current ripple. It shows that the efficiency of the power stage increases when the inductor size increases. Since the transistor takes most of the loss in the boost power factor circuit, the bigger inductor size means a smaller transistor switching loss. Selecting a bigger inductor, therefore, reduces the large transistor loss and improves the power stage efficiency.

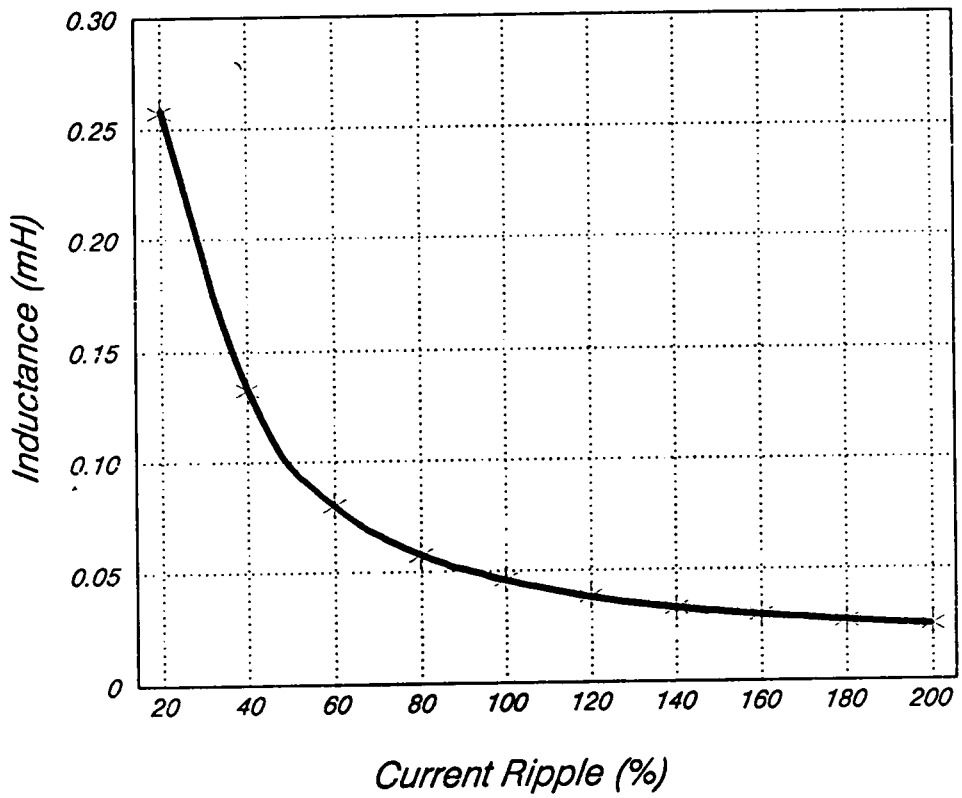


Figure 3.2 Boost Inductance versus Inductor Current Ripple at 95% Efficiency

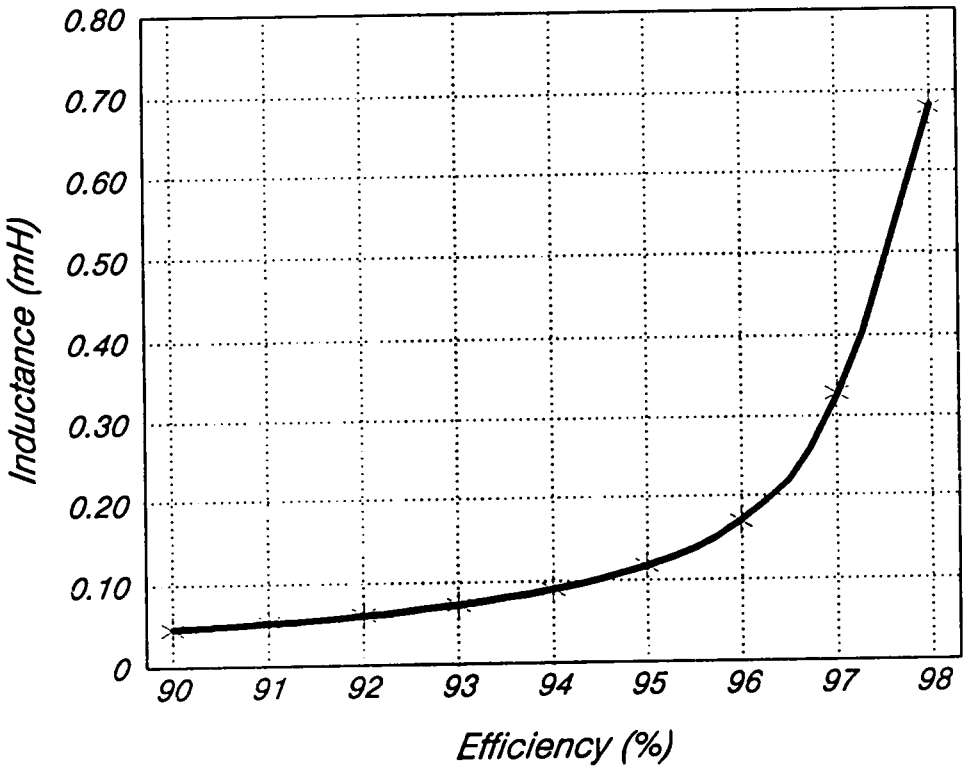


Figure 3.3 Boost Inductance versus Power Stage Efficiency at 30% Current Ripple

IV. DESIGN CONSIDERATIONS FOR A PRACTICAL POWER FACTOR CIRCUIT

4.1 Introduction

The design optimization results of the 500-watt, 300-volt active power factor correction circuit are listed in Table II in the previous chapter. In this chapter, the hardware implementation of the design is discussed in detail. Topics include:

- Inductor current-sense
- Control and gate-drive circuit
- Power stage experimental results

The open-loop and closed-loop small-signal responses will be discussed in the last sections of this chapter. A power factor switch model derived by Ridley [9] will be applied in the close-loop compensator design. Compensator design guidelines for a

50-watt, 50-volt active power factor correction under resistive load and regulator load will be discussed in detail.

4.2 *Inductor Current Sense*

As mentioned in chapter one, the variable-hysteresis controlled power factor correction circuit requires inductor current information. Both the peak and valley inductor current must be sensed. A resistive current sense method will be used here.

In selecting the current-sense resistor, two things must be kept in mind. First, the resistance should not be too high to lower the overall circuit efficiency. Second, a very small resistor causes a poorly-sensed inductor current signal-to-noise ratio, resulting in a very noisy signal. For the 500-watt power factor circuit, one watt loss on the resistor is acceptable. The loss in efficiency can easily be compensated by slightly increasing the inductor size in the original design.

From Table II, since the RMS inductor current is 4.18 A, the maximum resistance of the current sense resistor, R_{sense}, is:

$$R_{sense}(\max) = \frac{1.0}{4.18^2} = 0.06\Omega \tag{4.2.1}$$

The actual current sense resistor used is two 0.1 Ω resistors in parallel. This resistor, R_{sense}, can be placed in the circuit in two ways. Referring to Fig. 4.1(A), R_{sense} is placed next to the inductor; a differential operational amplifier is used to pick up the voltage across the resistor, $R_{sense}\, i_L$. An inverting op-amp then amplifies the sensed voltage, $R_{sense}\, i_L$, to an acceptable voltage level, V_{sense} (this can be anywhere from 0 to 10 volts).

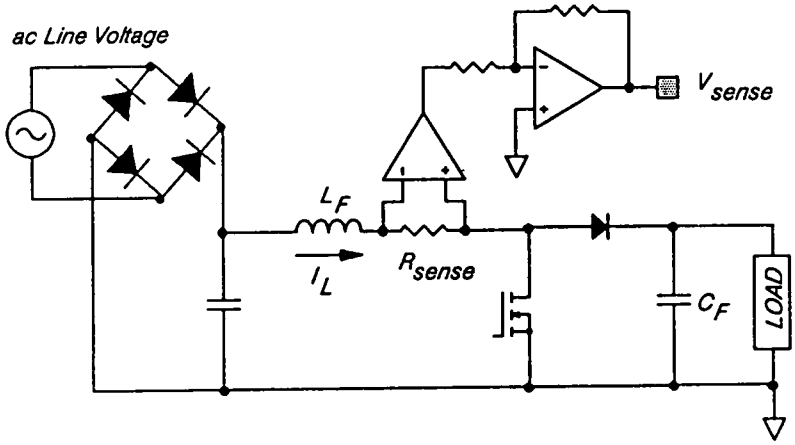


Figure 4.1 (A)

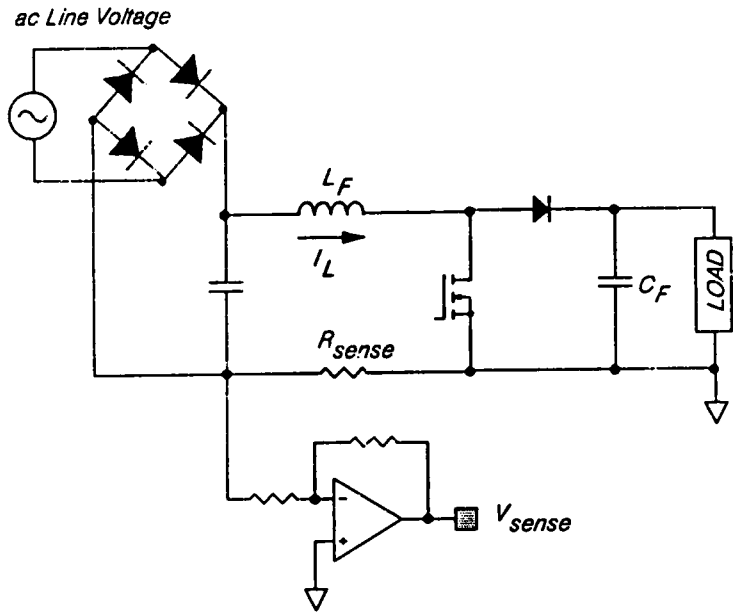


Figure 4.1 (B)

Figure 4.1 Two Methods of Inductor Current Sensing

Fig. 4.1(A) is not desirable ,since the individual terminals of the differential operational amplifier are subject to large voltage change: 0 volt when transistor is on, 300 volts when the transistor is off. A better choice is to place R_{sense} as shown in Fig. 4.1(B). The voltage at each terminals of the op-amp is always close to zero, thus eliminating the problem encountered in Fig. 4.1(A).

4.3 Control Logic Circuit

The complete control logic circuit for the open-loop test is shown in Fig. 4.2. It consists a window comparator formed with two LM311 ICs, a TTL latch 74LS00, a MOSFET driver DS0026, a multiplier AD532, and an active first-order low-pass filter. The window comparator and the TTL latch give the correct gate-drive signal. The MOSFET is turned off when the inductor current reaches the upper current reference. When the inductor current drops below the lower current reference, the MOSFET is switched back on. The small positive feed-back on the comparators prevents the false turn-on and off of the MOSFET due to the noise in the circuit. An optional comparator is used to force the MOSFET off at the beginning and end of a rectified line cycle. The first-order low-pass filter further attenuates the high-frequency noise on the rectified line voltage generated by the inductor current switching ripple. The analog multiplier IC, AD532, is a high-precision multiplier. It is used here only for demonstration purpose. In commercial production, an average-precision multiplier is sufficient.

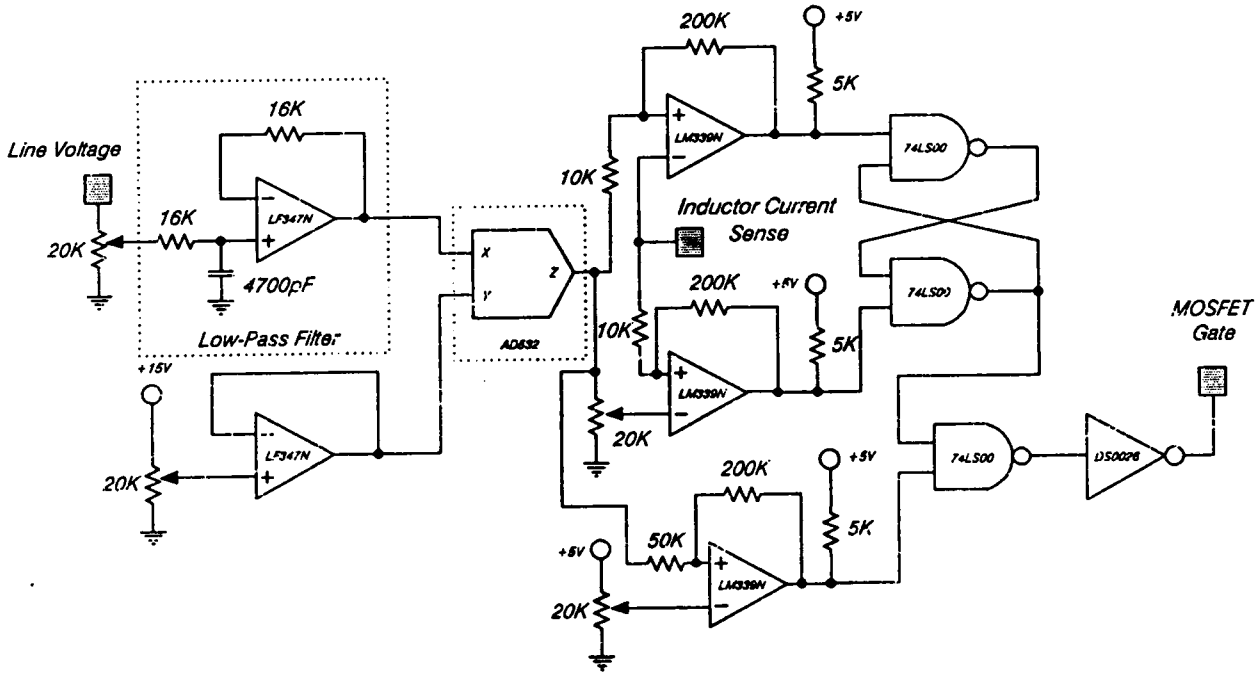


Figure 4.2 Control Logic Circuit for Open-Loop Test

4.4 Breadboard Performances

A breadboard of the 500-watt, 300-volt boost power factor correction circuit has been built. The circuit uses the resistive current sense method and the variable-hysteresis control logic circuit mentioned in sections 4.2 and 4.3. The inductor is built using the results obtained from Table II. It has 76 turns, and its actual inductance is 294 μH. A 300 μF-electrolytic capacitor is used for the output filter capacitor. The inductor current ripple can be adjusted from 10 % to 200 %.

Fig. 4.3 shows the inductor current with a 30 % current ripple. The peak inductor current, at the middle of the rectified line cycle, is about 6.8 A. A 20 μF-capacitor is inserted before the inductor to filter the high-frequency switching current ripple back into the ac power line. Fig. 4.4 shows the line voltage and current after such filtering. Fig. 4.5 shows the rectified line voltage, together with the output voltage ripple. It is clear that the output ripple voltage is approximately a sinusoid, with a frequency twice the line frequency and a 90-degree phase-lag.

Fig. 4.6 to Fig. 4.8 show the circuit waveforms for 100 % inductor current ripple. The peak inductor current is now increased to 9.0 A. A 40 μF-capacitor is inserted before the inductor. The output voltage ripple, however, remains the same.

Experimental results for the 30 % and 100 % inductor current ripple are shown in Table III. The apparent power is the product of the RMS line current and voltage. The real power draw from the ac line is measured using a wattmeter. The output power is the product of the dc voltage and load current. At 30 % current ripple, the measured circuit efficiency is 93.2 %. This is lower than the 95 % predicted by the CADO, partly due to the extra power losses in the snubber and current sense resistor which have not been taken into account in the analysis.

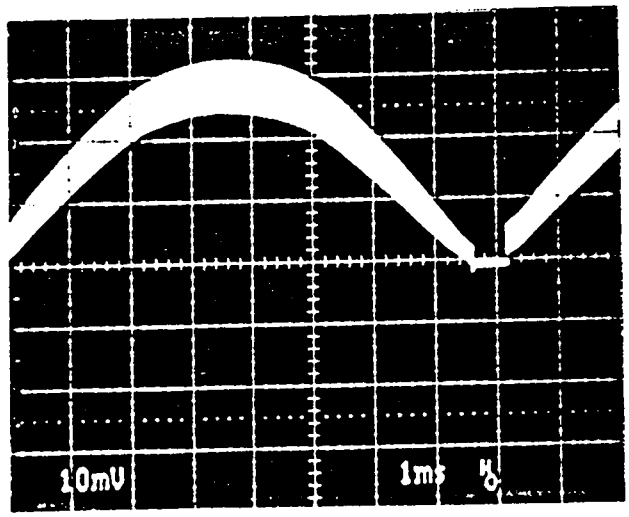


Figure 4.3 Boost Inductor Current at 30% Current Ripple (2 A/Division)

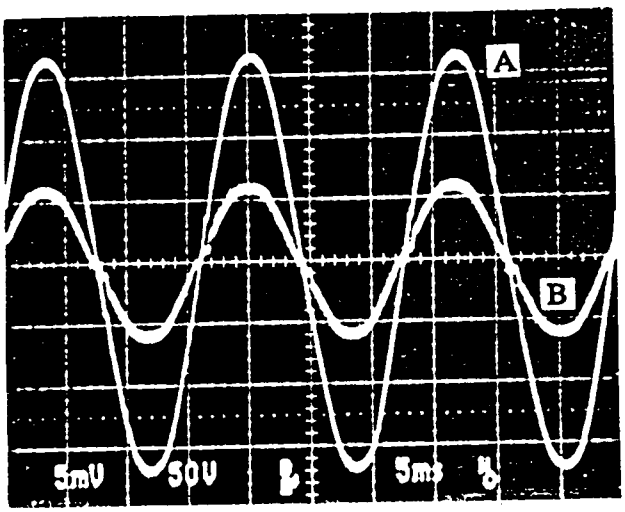


Figure 4.4 Line Voltage and Line Current at 30% Current Ripple
(A) Line Voltage (50 V/Division)
(B) Line Current (5 A/Division)

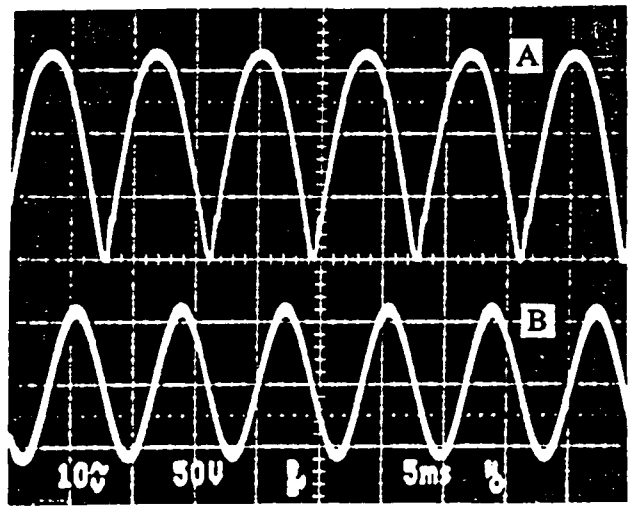


Figure 4.5 Rectified Line Voltage and Output Voltage Ripple at 30% Inductor Current Ripple
(A) Rectified Line Voltage (50 V/Division)
(B) Output Voltage Ripple (10 V/Division)

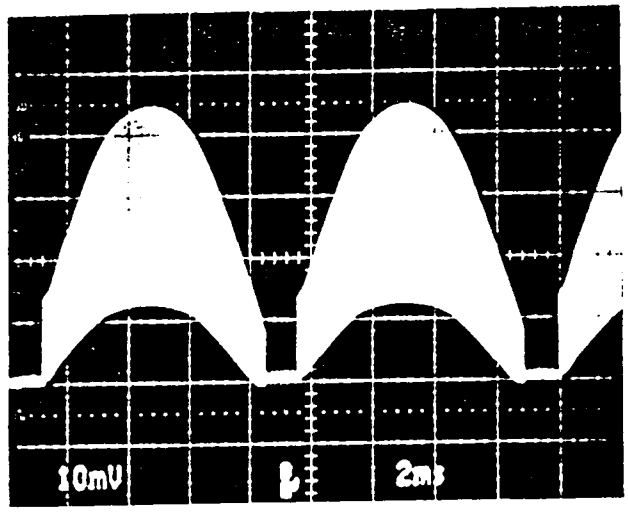


Figure 4.6 Boost Inductor Current at 100% Current Ripple (2 A/Division)

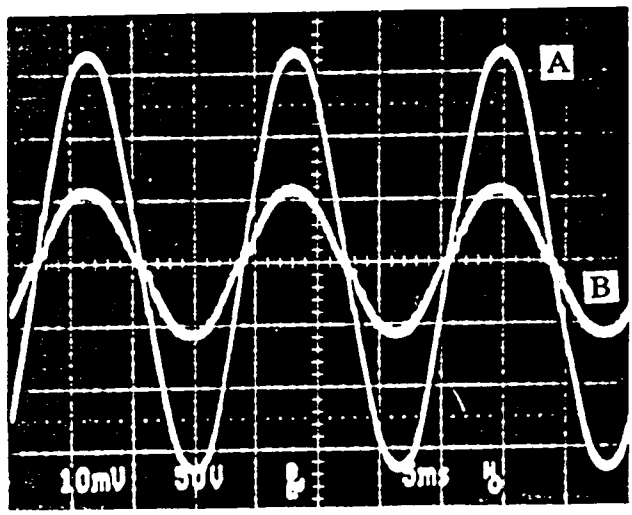


Figure 4.7 Line Voltage and Line Current at 100% Current Ripple
(A) Line Voltage (50 V/Division)
(B) Line Current (5 A/Division)

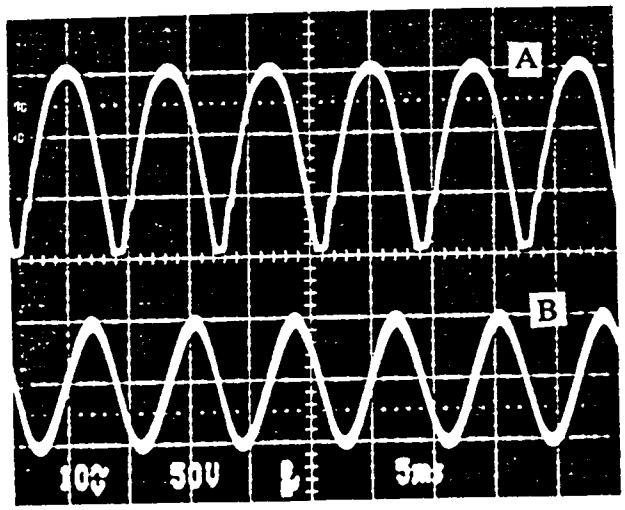


Figure 4.8 Rectified Line Voltage and Output Voltage Ripple at 100% Inductor Current Ripple
(A) Rectified Line Voltage (50 V/Division)
(B) Output Voltage Ripple (10 V/Division)

Table III
Boost Power Factor Circuit Power
Stage Experimental Results

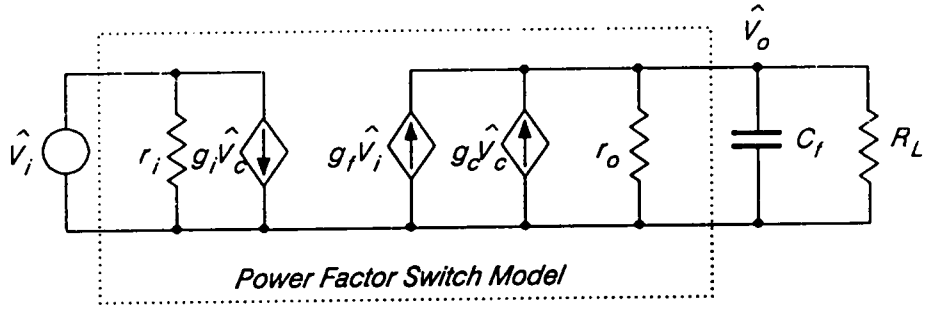
SYMBOL	DESCRIPTION	VALUE	VALUE
Δ	Current Ripple	30%	100%
V_{LINE}	RMS line voltage	119 V	120 V
I_{LINE}	RMS line current	4.40 A	4.15 A
P_{IN}	Real input power	515 W	490 W
V_O	Output voltage	300.0 V	296.5 V
I_O	Output current	1.60 A	1.58 A
P_O	Output power	480.0 W	468.5 W
pf	Power factor	0.983	0.984
EFF	Efficiency	93.2%	95.6%

4.5 Boost Power Factor Circuit Small-Signal Response

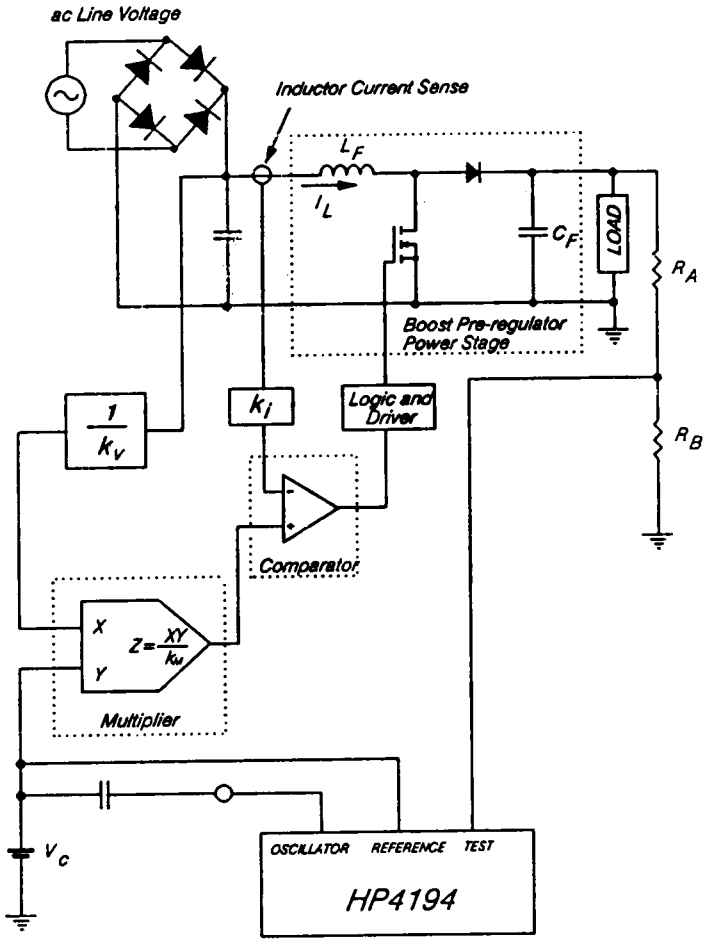
As mentioned in the previous chapters, the boost power factor correction generates a crudely-regulated dc output voltage. In order not to distort the line current and to draw a close to unity power factor from the line, the feedback circuit must be designed with a bandwidth compared to the 120 Hz line frequency. Ridley [9] has developed a power factor switch model and some design rules for the compensator selection. This switch model, however, has not been verified experimentally, and some modifications have to be made in consideration of the multiplier gain, output resistive divider gain, etc. The purpose of this section is to verify the model's open-loop control-to-output transfer function and to test the closed-loop circuit's performance at resistive load and regulator load for a 50-watt, 50-volt boost power factor circuit.

4.5.1 Resistive Load

The power factor switch model is shown in Fig. 4.9(A) with the filter capacitor and a resistive load connected. The parameters for the switch model is in Table IV, together with the circuit component values for the 50-watt, 50-volt experimental boost power factor circuit. Fig. 4.9(B) shows the open-loop test set up. A low-frequency ac signal is superimposed on the steady-state control voltage, V_c, thus perturbing the control voltage. The output of the multiplier generates a modulated inductor current reference , resulting modulated inductor current and output voltage. The quantity k_v relates the RMS rectified line voltage and the inductor current reference signal. The quantity k_i relates the sensed inductor current signal and the actual inductor current. The quantity M is the voltage conversion ratio of the power factor circuit, i.e.:



(A)



(B)

Figure 4.9 Power Factor Switch Model and Open Loop Test Setup

Table IV

(A) Component Values for the Power Factor Switch Model

M	k	r_i	g_i	r_O	g_f	g_C
$\frac{V_O}{V_i}$	$\frac{k_i k_v}{\eta}$	$\frac{r_O}{M^2}$	$\frac{V_i}{k}$	$\frac{V_O}{I_O}$	$\frac{2M}{r_O}$	$\frac{V_i}{kM}$

(B) Circuit Parameters for the Experimental Boost Power Factor Correction Circuit at 30% Ripple

$V_g(nom)$	V_g(max)	V_g(min)	L_F	C_F	V_O	P_O
25 V (RMS)	30 V (RMS)	20 V (RMS)	170 μH	320 μF	50 V (dc)	50 W

$$M = \frac{V_o}{V_l} \tag{4.5.1}$$

where V_o is the dc output voltage and V_l is the RMS value of the line voltage.

From the switch model, the control-to-output transfer function for a resistive load is:

$$\frac{\hat{v}_o}{\hat{v}_c} = \frac{g_c R_L}{2} \frac{1}{1 + s\frac{C_f R_L}{2}} \tag{4.5.2}$$

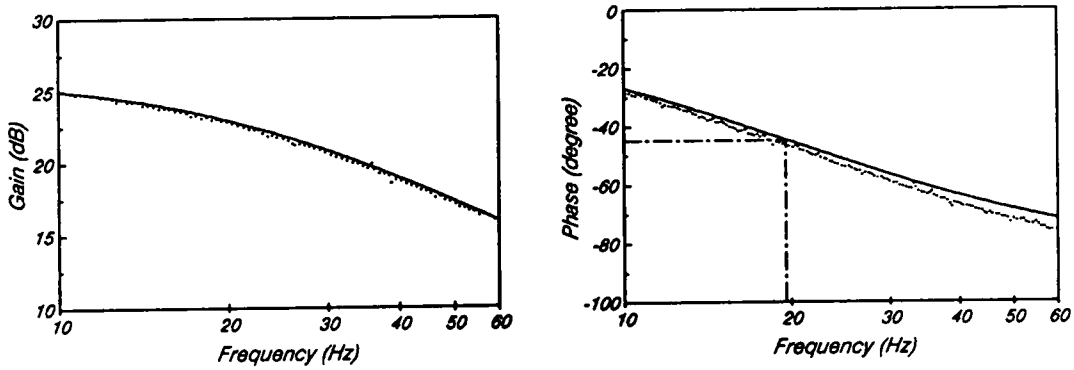
Note that the control-to-output transfer function has a dc gain, $\frac{g_c R_L}{2}$, and a pole at $\frac{2}{C_f R_L}$ rad/s. The right-hand plane zero of the boost topology and the filter capacitor ESR zero are ignored from the transfer function, since the rectified line frequency, 120 Hz, is much lower than the frequencies corresponding to the ESR zero and the right-hand plane zero.

Fig. 4.10 shows an overplot of theoretical control-to-output response, together with the experimental result. Note that, with the test setup in Fig. 4.9, the measured dc gain of the control-to-output response should multiply the reciprocal of the output resistive divider gain, $\frac{R_A + R_B}{R_B}$, and the reciprocal of the multiplier gain, $\frac{1}{k_M}$, to match the theoretical results. R_B and R_A are the resistive divider at the output and the quantity k_M is the multiplier gain. For the AD532 used in the experiment, k_M is 0.1, i.e.:

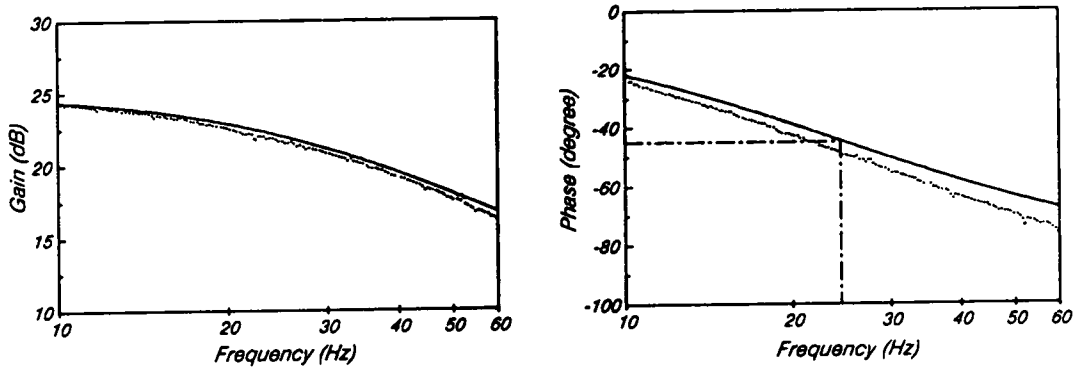
$$Z = \frac{XY}{10} \tag{4.5.3}$$

where X and Y are the two inputs of the AD532, Z is the output.

In the closed-loop compensator design, an integral and lead network is sufficient for both the resistive load and regulator load. Fig. 4.11 shows a simple integral and lead



(A) with a 50 ohm resistive load



(B) with a 40 ohm resistive load

——————— *Theoretical*

..... *Experimental*

Figure 4.10 Control-Output Response Experimental and Theoretical Plots

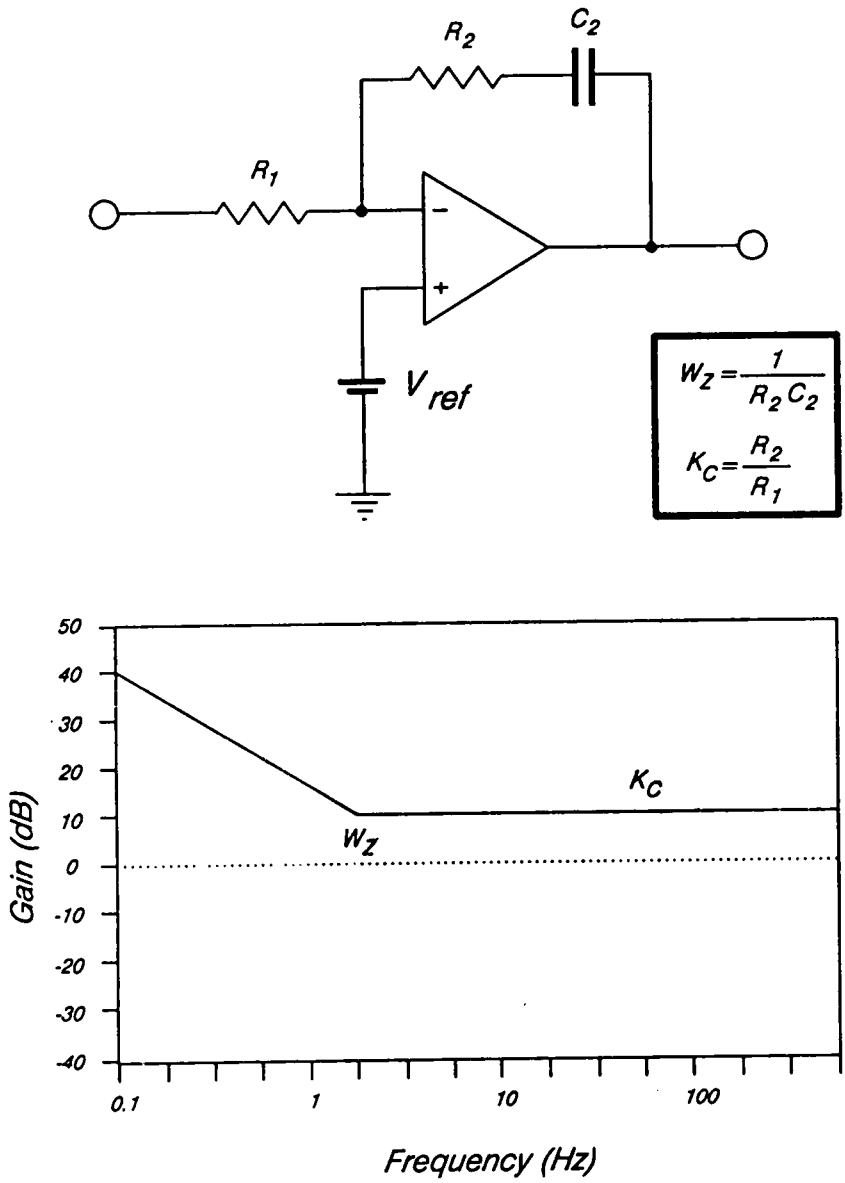


Figure 4.11 Integral and Lead Compensator and its Gain Asymptotes

compensator, together with its gain asymptotes. Two parameters have to be determined: the location of the zero, ω_z, and the high-frequency gain, k_c.

For a resistive load, the location of the zero, ω_z, is placed exactly at the pole presented in the control-to-output transfer function, $\frac{2}{C_f R_L}$. The high-frequency gain, k_c, is selected as follows:

$$k_c = 60\pi C_f \frac{k_v k_i M_{\min}}{\eta k_M V_i^{\max}} \frac{R_A + R_B}{R_B} \tag{4.5.4}$$

where $M_{\min}$ is the ratio of the dc output voltage and the RMS low line voltage, $V_i^{\max}$ is the RMS high line voltage, and η is the efficiency of the boost power stage.

The location of this zero, ω_z, theoretically ensures a 90 degree phase margin at all frequencies. Since the dc gain of the control-to-output transfer function is directly proportional to the RMS line voltage, the loop gain cross-over frequency will be lower at the low line A suitable cross-over frequency is at 1/2 of the line frequency, 30 Hz. Fig. 4.12 shows the test set up for the closed-loop measurements. Note that the signal transformer, T_1, has to be big enough to transfer a very low frequency ac signal, typically less than 60 Hz.

The compensator gain transfer function is:

$$\frac{\hat{v}_c}{\hat{v}_o} = \frac{k_c \omega_z}{s}\left(1 + \frac{s}{\omega_z}\right) \tag{4.5.5}$$

By combining Eq.4.5.2 and Eq.4.5.5, the closed-loop gain transfer function, T, can be obtained.

$$T = 60\pi \frac{V_i M_{\min}}{V_i^{\max} M} \frac{1}{s} \tag{4.5.6}$$

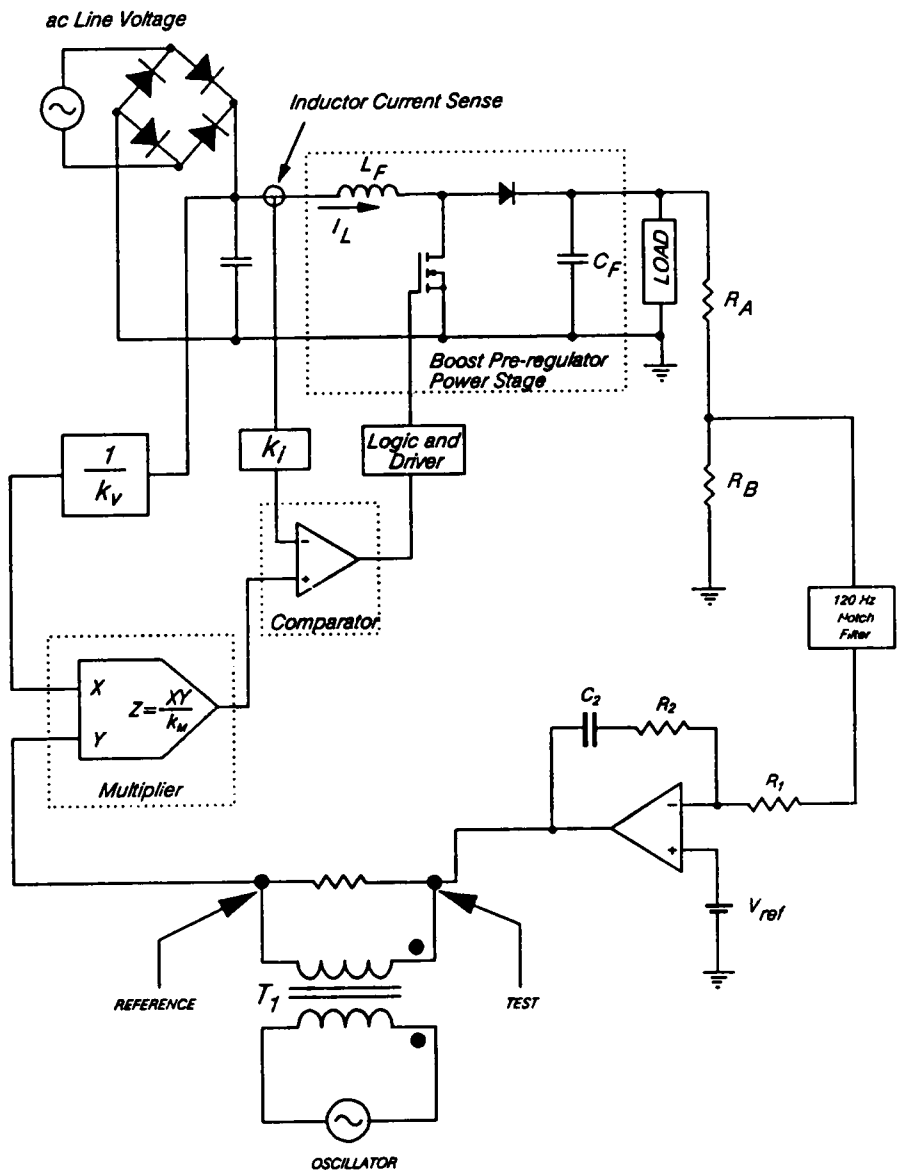


Figure 4.12 Closed-Loop Gain Response Test Setup

The loop gain crossover frequency, f_c, is:

$$f_c = 30 \frac{V_i}{V_i^{\max}}^2 \tag{4.5.7}$$

The closed-loop gain transfer function, T, is simply an integrator. Its maximum loop gain crossover frequency occurs at 30 Hz. T has a minus 90-degree phase at all frequencies.

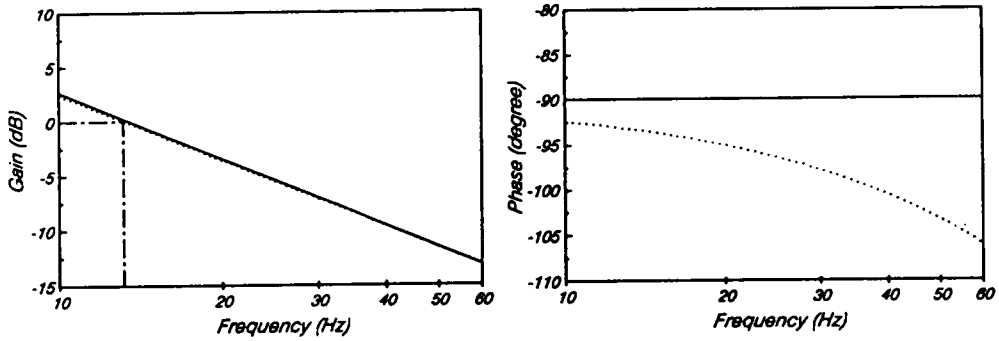
Fig. 4.13 shows the experimental and predicted loop gain responses at low line, nominal line, and high line for the 50 Ω resistive load. The closed-loop crossover frequency for the experimental boost power factor correction circuit at low line, nominal line, and high line are 13 Hz, 19 Hz, and 30 Hz, respectively.

4.5.2 Regulator Load

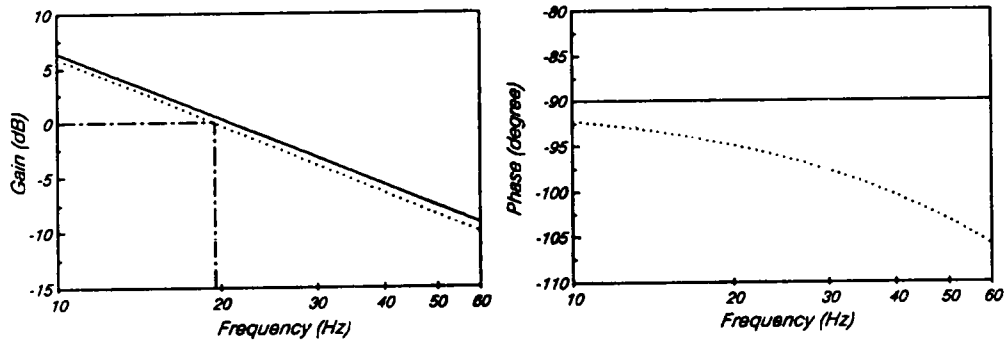
Since the boost power factor circuit is used also as a pre-regulator for the dc-to-dc switching power supply, a constant power load, the design of feedback network for it becomes very important. The constant power load exhibits a negative input resistance. The control-to-output transfer function is simply an integrator.

$$\frac{\hat{v}_o}{\hat{v}_c} = g_c \frac{1}{sC_f} \tag{4.5.8}$$

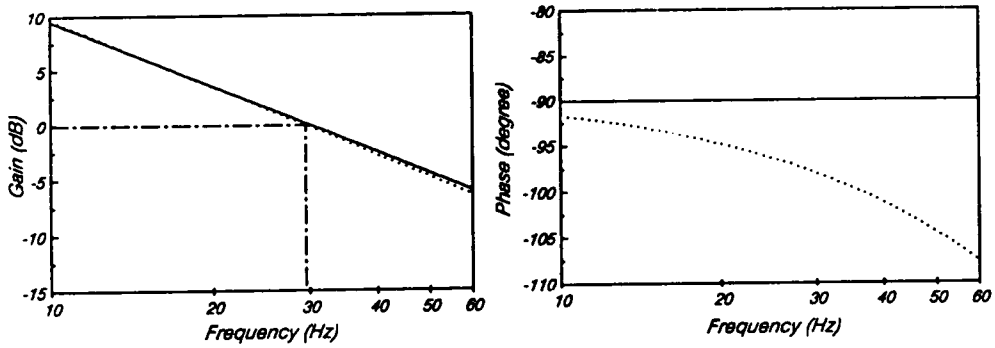
For the feedback compensator, the same integral and lead network can be used with the same high-frequency gain, k_c. The zero, however, has to be changed to ensure a 45 to 60 degree phase margin.



(A) at low line: V_g = 20 volt



(B) at nominal line: V_g = 25 volt



(C) at high line: V_g = 30 volt

Theoretical ———— *Experimental* .....

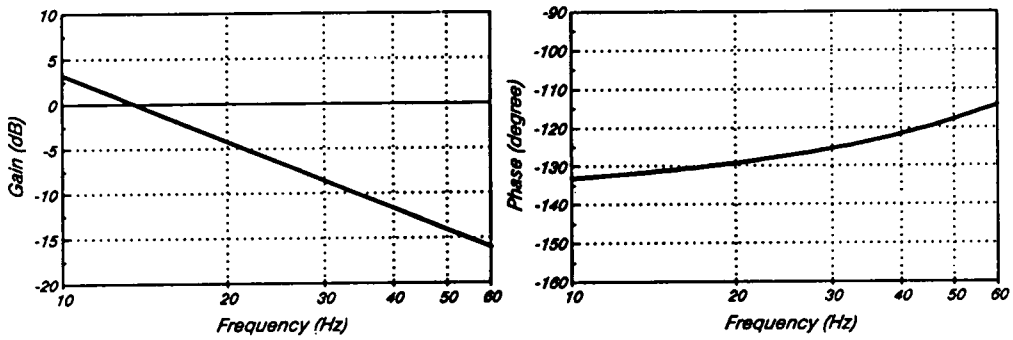
Figure 4.13 Closed-Loop Gain Theoretical and Experimental Response for the 50-ohm Resistive Load

$$\omega_z = \frac{120\pi}{\sqrt{3}} \left[\frac{V_i^{\min}}{V_i^{\max}} \right]^2 \tag{4.5.9}$$

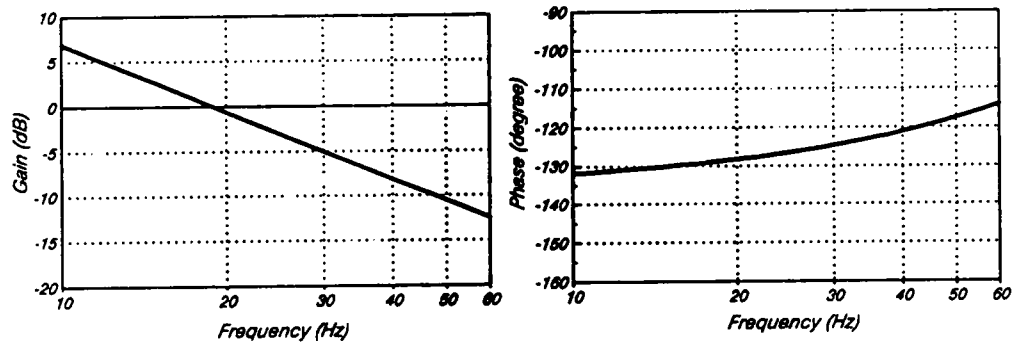
The closed-loop gain transfer function is:

$$T = 60\pi \frac{V_i M_{\min}}{V_i^{\max} M} \frac{\omega_z}{s^2} \left(1 + \frac{s}{\omega_z}\right) \tag{4.5.10}$$

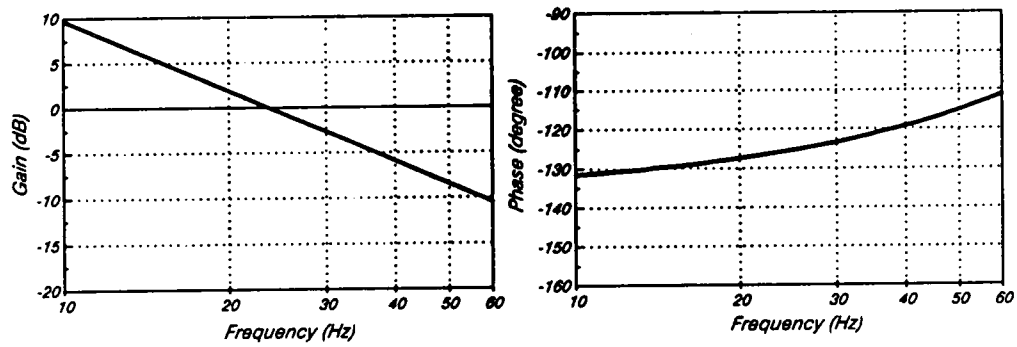
Fig. 4.14 shows a plot of loop gain measurement for the 50-volt, 50-watt regulator load. The loop gain response is similar to the gain response for the resistive load. The loop gain phase, due to the characteristics of the integrator of the control-to-output transfer function, has only around a 45-degree phase margin, compared to around a 90-degree phase margin for the resistive load.



(A) at low line: V_g = 20 volt



(B) at nominal line: V_g = 25 volt



(C) at high line: V_g = 30 volt

Figure 4.14 Experimental Closed-Loop Response for the Regulator Load

V. CONCLUSIONS

An analysis of the variable-hysteresis controlled boost power factor correction circuit power stage is performed. Design equations for output filter capacitor, RMS transistor and inductor current are derived. Approximated expressions for transistor loss, diode loss, inductor loss and equivalent switching frequency are obtained. These equations are incorporated into the nonlinear design optimization program.

The nonlinear design optimization routine (CADO) is proven to be very efficient in the design of active power factor correction circuits. By entering proper design constants and identifying design variables and constraints, a designer can achieve an optimal design using CADO. It is shown that the boost inductance and inductor current ripple play an important rule in the weight, size, and performance of the power factor circuit. The output filter capacitor size is directly related to the voltage ripple and holdup time requirements, and is insensitive to the boost inductor size and the switching frequency. This filter capacitor is at least three time smaller compared to the conventional ac-to-dc rectification process without power factor correction. By completely turning off the power transistor at the beginning and end of a rectified line cycle, the actual circuit implementation can be simplified without significantly compromises the power factor.

Minimal input filtering is required when the inductor current has a very small current ripple.

A low-frequency feedback network is employed in the power factor compensator design. It is shown that an integral and lead compensator is sufficient to ensure a 90-degree phase margin for a resistive load, and a 45-degree for the regulator load. The closed-loop gain crossover increases as the ac line voltage increases.

Suggestions for Future Work

The active power factor correction circuit improves the power factor and minimizes the line harmonics. Due to the nature of the active filtering, however, it generates high-frequency switching current ripple at the line. To satisfy the EMI/RFI requirements imposed by government agencies, an input filter is required. A detailed analysis on the single or even two-stage LC input filter is required. The interaction between this input filter and the low-frequency feedback loop is also a very important topic. By incorporating the input filter design into the CADO, the trade-offs the input filter size and inductor current ripple magnitude will be shown.

Appendix A. DERIVATIONS OF THE BOOST POWER FACTOR CIRCUIT

A.1 Transistor On-Time and Off-Time

From Fig. A.1, consider an inductor switching cycle with transistor on-time, t_{on}, and transistor off-time, t_{off}.

$$I_c \sin \omega t + \frac{1}{L_f} \int_t^{t+t_{on}} V_p \sin \omega\tau \, d\tau = I_p \sin(\omega t + \omega t_{on}) \qquad (A.1.1)$$

Then

$$\frac{V_p}{\omega L_f} [\cos \omega t - \cos(\omega t + \omega t_{on})] = I_p \sin(\omega t + \omega t_{on}) - I_c \sin \omega t \qquad (A.1.2)$$

$$\frac{V_p}{\omega L_f} \left[\frac{\cos \omega t - \cos(\omega t + \omega t_{on})}{\omega t_{on}} \right] = I_p \left[\frac{\sin(\omega t + \omega t_{on}) - \sin \omega t}{\omega t_{on}} \right] + \frac{\delta}{\omega t_{on}} \sin \omega t \, (A.1.3)$$

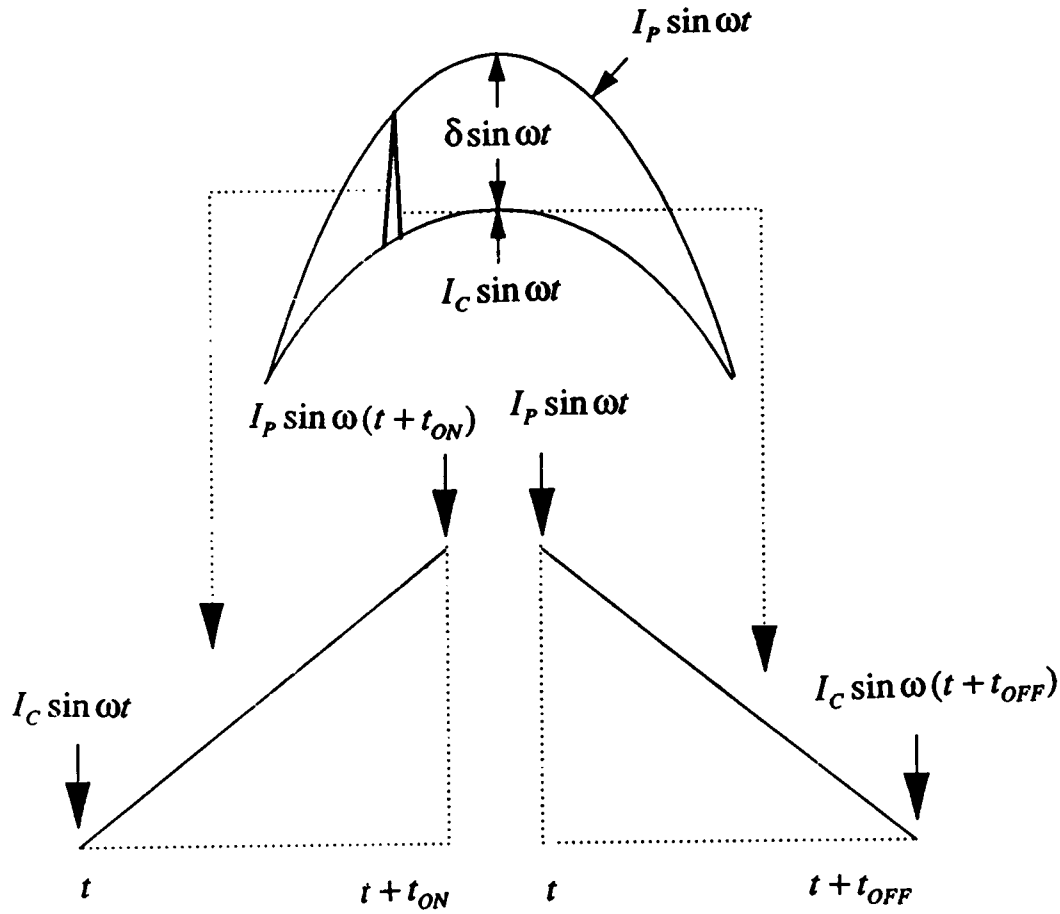


Figure A.1 Diagram for Calculating Transistor On-Time and Off-Time

Since t_{on} is much smaller compared to the period of the 120 Hz rectified line cycle, i.e., $\omega t_{on} \rightarrow 0$

$$\frac{V_p}{\omega L_f} \sin \omega t = I_p \cos \omega t + \frac{\delta}{\omega t_{on}} \sin \omega t \qquad (A.1.4)$$

$$\therefore t_{on} = \frac{\delta L_f}{V_p - \omega L_f I_p \cot \omega t} \qquad (A.1.5)$$

Similarly, for the transistor off-time, t_{off}

$$I_p \sin \omega t + \frac{1}{L_f} \int_t^{t+t_{off}} (V_p \sin \omega \tau - V_o)\, d\tau = I_c \sin(\omega t + \omega t_{off}) \qquad (A.1.6)$$

Then, with $\omega t_{off} \rightarrow 0$ for a 120 Hz rectified line cycle

$$\frac{V_p}{\omega L_f} \sin \omega t - \frac{V_o}{\omega L_f} = I_c \cos \omega t - \frac{\delta \sin \omega t}{\omega t_{off}} \qquad (A.1.7)$$

$$\therefore t_{off} = \frac{\delta L_f \sin \omega t}{V_o + \omega L_f I_c \cos \omega t - V_p \sin \omega t} \qquad (A.1.8)$$

A.2 Output Filter Capacitance

The output filter capacitance, C_f, for a given output voltage ripple, ΔV_o, is evaluated by integrating the current through the capacitor, $i_c(t)$. From Fig. A.2, we get

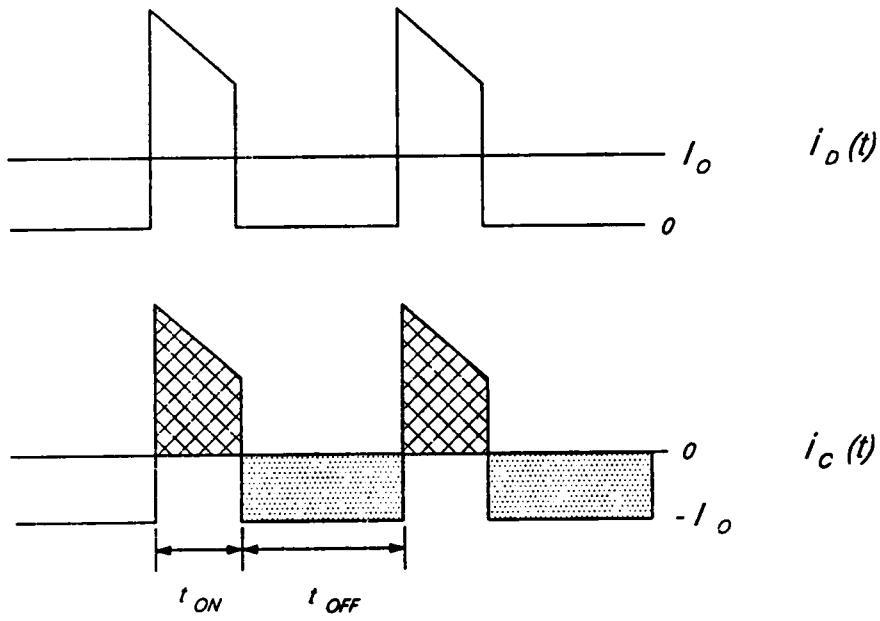


Figure A.2 Diagram for Calculating Output Filter Capacitance

$$\Delta V_o = \frac{1}{C_f} \int_0^{T_s} i_c(t)\, dt = \frac{1}{C_f} \int_0^{T_s} (\, I_d(t) - I_o \,)\, dt = \frac{1}{C_f} (I_o T_{off}) \qquad (A.2.1)$$

where $i_d(t)$ is the diode current, T_s is period of the 120 Hz rectified line cycle, and I_o is the dc load current. T_{off} is the total diode on-time in the entire 120 Hz rectified line cycle.

$$T_{off} = \int_0^{T_s} d'\, dt = \int_0^{T_s} \frac{V_p \sin \omega t}{V_o}\, dt = \frac{2V_p}{\omega V_o} \qquad (A.2.2)$$

where $d' = \frac{V_p \sin \omega t}{V_o}$. Since $\Delta V_o = V_{ripple}$ and $T_s = \frac{\pi}{\omega}$

$$C_{pf} = \frac{2V_p I_o}{\omega\, V_{ripple}\, V_o} \qquad (A.2.3)$$

A.3 RMS Transistor Current

The RMS switch current is evaluated by first calculating its RMS value in one arbitrary switching cycle, then summing it over the entire 120 Hz rectified line cycle. Since there are many high-frequency switching cycles within the 120 half-line cycle, the summation can be approximately by an integration. From Fig. A.3, in one arbitrary switching cycle, a , b, and c are constants, and the RMS switch current in one switching cycle is given by the following:

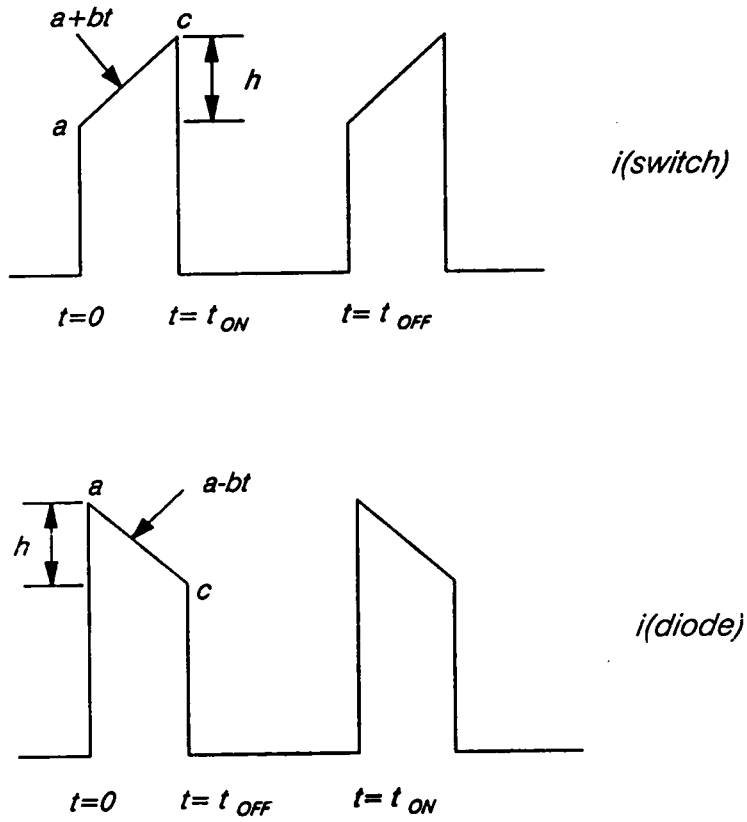


Figure A.3 Diagram for Calculating RMS Switch Current and Inductor Current

$$\frac{1}{t_{on}+t_{off}}\int_0^{t_{on}+t_{off}} i^2(t)\,dt = \frac{1}{t_{on}+t_{off}}\int_0^{t_{on}+t_{off}} (a+bt)^2\,dt$$

$$= \frac{1}{t_{on}+t_{off}}\int_0^{t_{on}} (a^2+2abt+b^2t^2)\,dt$$

$$= \frac{1}{t_{on}+t_{off}}\left(a^2t_{on}+abt_{on}^2+\frac{b^2t_{on}^3}{3}\right) \qquad (A.3.1)$$

$$= \frac{t_{on}}{t_{on}+t_{off}}\left(a^2+abt_{on}+\frac{b^2t_{on}^2}{3}\right)$$

$$= d\left(a^2+ah+\frac{h^2}{3}\right)$$

where $a = I_c \sin\omega t$, $c = I_p \sin\omega t$, $h = \delta \sin\omega t = bt_{on}$, $d = 1 - \dfrac{V_p \sin\omega t}{V_o}$, and $T_s = \dfrac{\pi}{\omega}$.

The RMS switch current, i_{rms}^{sw}, is

$$(i_{rms}^{sw})^2 = \frac{1}{T_s}\int_0^{T_s} d\left[(I_c \sin\omega t)^2 + (I_c \sin\omega t)(\delta \sin\omega t) + \frac{1}{3}(\delta \sin\omega t)^2\right]dt \qquad (A.3.2)$$

$$\therefore i_{rms}^{sw} = \sqrt{(I_c^2 + I_c\delta + \frac{1}{3}\delta^2)(\frac{1}{2} - \frac{4V_p}{3\pi V_o})} \qquad (A.3.3)$$

A.4 RMS Inductor Current

The RMS diode current is obtained in a similar way as the RMS switch current. Again, from Fig. A.3

$$\frac{1}{t_{on}+t_{off}}\int_0^{T_s}(a-bt)^2\,dt = d'\,(a^2-ah+\frac{h^2}{3}) \qquad (A.4.1)$$

where $a = I_p \sin\omega t$, $c = I_c \sin\omega t$, $h = bt_{off} = \delta \sin\omega t$, and $d' = \frac{V_p \sin\omega t}{V_o}$. The RMS diode current, i^d_{rms} is

$$(i^d_{rms})^2 = \frac{1}{T_s}\int_0^{T_s} d'\left[(I_p \sin\omega t)^2 - (I_p\delta \sin^2\omega t) + \frac{1}{3}(\delta \sin\omega t)^2\right]dt \qquad (A.4.2)$$

$$\therefore i^d_{rms} = \sqrt{\frac{4V_p}{3\pi V_o}(I_c^2 + I_c\delta + \frac{\delta^2}{3})} \qquad (A.4.3)$$

The RMS inductor current, i^{ind}_{rms}, can be obtained from the RMS switch current and RMS diode current

$$(i^{ind}_{rms})^2 = (i^{sw}_{rms})^2 + (i^d_{rms})^2 \qquad (A.4.4)$$

$$\therefore i^{ind}_{rms} = \sqrt{\frac{1}{2}(I_c^2 + I_c\delta + \frac{\delta^2}{3})} \qquad (A.4.5)$$

A.5 Power Factor

The power factor, *pf*, is defined by the following equation:

$$pf = \frac{\frac{1}{T_s}\int_0^{T_s} i(t)\,v(t)\,dt}{I_{rms}V_{rms}} \qquad (A.5.1)$$

where $i(t)$ and $v(t)$ are the instantaneous line current and voltage. I_{rms} and V_{rms} are the RMS values of the line current and voltage. T_s is the period of the rectified line cycle.

With a high-frequency current ripple, $\delta \sin \omega t$, the RMS line current will increase, while the average power drawn by the power factor circuit is approximately the same.

$$P_{in} \approx \frac{1}{T_s} \int_0^{T_s} V_p \sin \omega t \, I_m \sin \omega t \, dt = \frac{V_p I_m}{2} \tag{A.5.2}$$

$$V_{rms} = \frac{V_p}{\sqrt{2}} \tag{A.5.3}$$

$$I_{rms} = i_{rms}^{ind} = \sqrt{\frac{1}{2}(I_c^2 + I_c\delta + \frac{\delta^2}{3})} \tag{A.5.4}$$

With $I_c = I_m - \frac{\delta}{2}$

$$pf = \sqrt{1 - \frac{\delta}{12I_m^2 + \delta^2}} \tag{A.5.5}$$

The power factor with a phase delay, θ, at the beginning and end of a rectified line cycle can be calculated in a similar way.

$$P_{in} = \frac{1}{\pi} \int_\theta^{\pi-\theta} V_p \sin \omega x \, I_p \sin \omega x \, dx = \frac{V_p I_p}{\pi} \left[\frac{\pi - 2\theta}{2} + \sin \frac{2\theta}{2} \right] \tag{A.5.6}$$

$$V_{rms} = \frac{V_p}{\sqrt{2}} \tag{A.5.7}$$

$$I_{rms}^2 = \frac{1}{\pi} \int_\theta^{\pi-\theta} I_p^2 \sin^2 \omega t \, dx = \frac{I_p^2}{\pi} [\pi - 2\theta + 2 \sin \omega t] \tag{A.5.8}$$

$$\therefore pf = \sqrt{\frac{\pi - 2\theta + \sin 2\theta}{\pi}} \qquad (A.5.9)$$

If we want to know the power factor at certain phase delay, θ, and with current ripple, δ, just multiply Eq. A.5.5 and Eq. A.5.9.

$$pf = \sqrt{(1 - \frac{\delta}{12I_m^2})(\frac{\pi - 2\theta + \sin 2\theta}{2})} \qquad (A.5.10)$$

A.6 Switching Losses

The transistor and diode switching losses can be estimated by using the switching loss expression in reference [10]. For the transistor switching waveform in Fig. A.4, the switching loss when driving an inductive load is

$$Switching\ loss = \frac{V_{ds} f_s}{2} (I_{d1} t_{rise} + I_{d2} t_{fall}) \qquad (A.6.1)$$

where V_{ds} is the transistor drain-source voltage when it is off. f_s is the switching frequency of the circuit. t_{rise} and t_{fall} are the rise-time and fall-time of the switching waveform, respectively.

For the power factor correction circuit with variable-hysteresis control, V_{ds} is the dc output voltage, V_o. I_{d1} is $I_c \sin \omega t$. I_{d2} is $I_p \sin \omega(t + t_{on})$. f_s is approximated by the equivalent switching frequency, F_{eq}, found in chapter two. The transistor switching loss, P_q, is

$$P_q = \frac{V_o F_{eq}}{3.6} (I_c t_{rise} + I_p t_{fall}) \qquad (A.6.2)$$

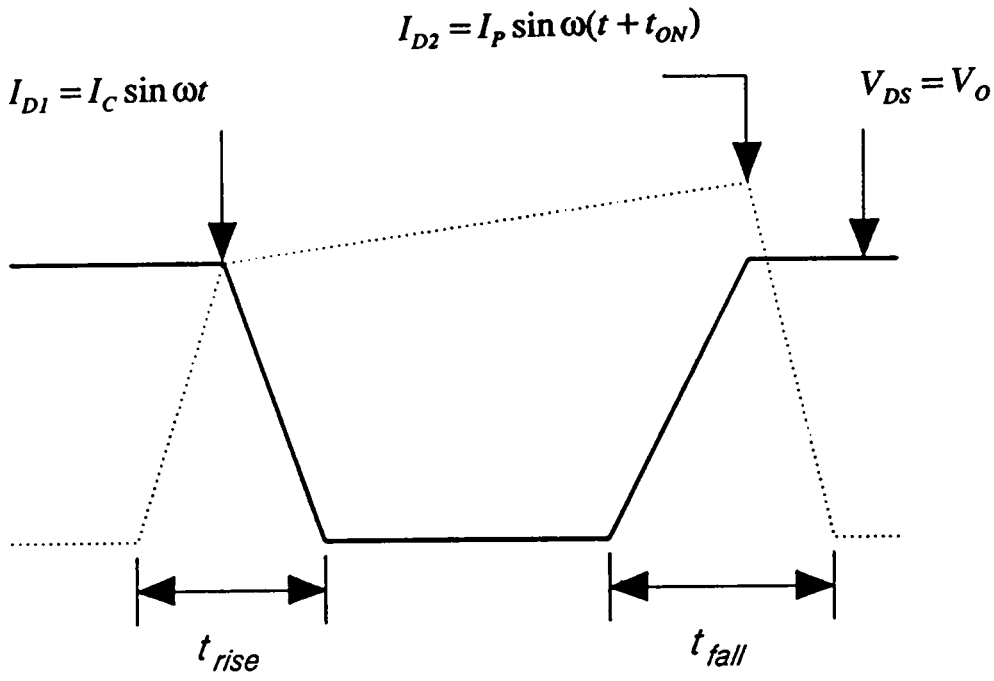


Figure A.4 Dragram for Calculating Transistor Switching Loss

The diode switching loss, P_d, can approximated in a similar way.

$$P_d = \frac{V_o F_{eq}}{7.2} (I_p t_{dr} + I_c t_{df}) \qquad (A.6.3)$$

where t_{dr} is the diode switching rise-time and t_{df} is the fall-time.

Appendix B. LIST OF COSMIR SIMULATION FILE

The computer simulation program COSMIR is used here not only to see the long-term circuit waveforms, but also to verify the analysis results. The open-loop and closed-loop hysteresis control can be very easily implemented by the program. The circuit nodal description of the 500-watt, 300-volt boost power stage, together with the sinusoidal source and full-bridge rectifier is shown in Fig. B.1. Two input data files are required to run the COSMIR; they are listed in Table B.1 and Table B.2.

Since the COSMIR does not have a built-in model for a sinusoidal voltage source, an LC resonant circuit is used to generate the ac line voltage. The frequency of the ac line voltage is determined by the values of L and C, and the amplitude the ac line voltage is based upon the initial conditions of the L and C. For a 60-Hz ac power line, the values of L and C are selected as follows:

$$L = C = \frac{1}{120\pi} = 2.65 \times 10^{-3} \qquad (B.1)$$

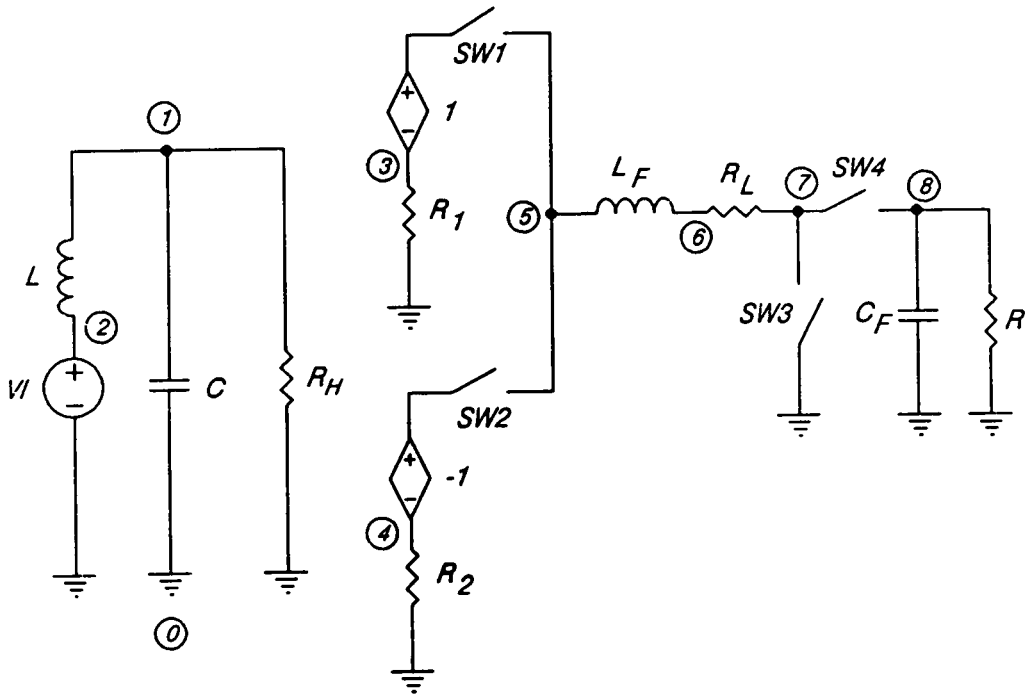


Figure B.1 Circuit Nodal Description for COSMIR Simulation

Table B1
INPUT1.DAT Listing

```
TITLE=POWER FACTOR CORRECTION CIRCUIT [ NEW VERSION ]

START=SW1 SW3

*** COMPONENT DESCRIPTION CARDS ***
*sinusoidal source
L=5.86D-3                B=1         N=(2,1)
C=1.04D-3                B=3         N=(0,1)
VI                       B=2         N=(0,2)
RH=20.0D+6               B=4         N=(1,0)
*bridge rectifier
R2=0.00001               B=6         N=(4,0)
VCVS=-1                  B=4,6
R1=0.00001               B=5         N=(3,0)
VCVS=1                   B=4,5
SWD=1                    B=7         N=(3,5)
SWD=2                    B=8         N=(4,5)
*boost power stage
LF=200.0D-6              B=9         N=(5,6)
RL=0.0001                B=10        N=(6,7)
SWD=3                    B=11        N=(7,0)
SWD=4                    B=12        N=(7,8)
CF=200.0D-6              B=13        N=(8,0)
R=180.0                  B=14        N=(8,0)

*** OUTPUT CARDS ***
*source voltage
Y1=VB(B4)
*upper current reference
*(4% of rectified line voltage)
Y2=VN(0.04*N5)
*lower current reference
*(3% of rectified line voltage)
Y3=VN(0.03*N5)
*inductor current
Y4=CB(B9)
*drain voltage
Y5=VN(N7)
*output voltage
Y6=VN(N8)

*** SWITCHING BOUNDARY CONDITIONS ***
*turn-on condition for switch #4
TON(4)=-Y4+Y2+0.002
*turn-on condition for switch #3
TON(3)=Y4-Y3-0.001
*turn-on condition for switch #2
TON(2)=Y1-1.0D-4
*turn-on condition for switch #1
TON(1)=-Y1+1.0D-4

END
```

Table B2
INPUT2.DAT Listing

```
2                   /(ONLY THE SWITCHING POINTS)
20                  /(NIT - MAX ITERATIONS USED IN NEWTON METHOD)
1                   /(MC - # OF STEP INPUTS)
1.0D-6              /(EPS - TOLERANCE FOR CALCULATING PHI & D)
1.7D-2              /(TF - FINAL SIMULATION TIME)
0.0
300.0
170.0
0.0                 /(INITIAL STATES)
1.0D+20
1.0D+20
1.0D+20
1.0D+20             /(UPPER LIMIT TO STATES)
-1.0D+20
-1.0D+20
-1.0D+20
-1.0D+20            /(LOWER LIMIT TO STATES)
5.0D-6
5.0D-6
5.0D-6
5.0D-6              /(FIXED TIME STEPS)
0.0
0.0                 /(STEP CHANGE)
1.0
1.0D-8
1.0D-8
1.0D-8
1.0D-8
1.0D-8
1.0D-8
1.0D-8
1.0D-8
```

Let the initial capacitor voltage, $v_c(0)$, be zero, then the initial inductor current, $i_L(0)$, is selected from

$$i_L(0) = A\omega C = A \tag{B.2}$$

where A is the amplitude of the ac line voltage. For the 120-volt RMS ac power line, the amplitude, A, is $120\sqrt{2}$.

The full-bridge rectifier is modelled by a set of voltage-controlled voltage sources, with gains of -1 and +1, and the switches $SW1$ and $SW2$. The voltage source VI is for the step-line simulation. The switch $SW3$ models the power factor circuit transistor and the switch $SW4$ models the diode in a similar way. The switch $SW3$ is turned off when the inductor current, $Y4$, reaches 4 % of the rectified line voltage, $Y2$. The switch $SW4$ is turned off when the inductor current, $Y4$, reaches 3 % of the rectified line voltage, $Y3$. The small numbers, such as +0.002, in the switching boundary conditions are used to prevent numerical problems during the simulation. The initial condition on the filter capacitor, C_f , is 300 volts, corresponding the the steady-state dc output voltage.

Appendix C. LIST OF CADO FILE

Boost Power Factor Correction Circuit Power Stage
Last Modified 4/20/1989

TITLE
Power Factor Correction Circuit Power Stage
END

DESIGN VARIABLES

0.95	E+00	EFF	X(1)	Efficiency
1.00	E-02	CW	X(2)	Core Centre Leg Width
5.00	E+01	TURNS	X(3)	Inductor Turns
1.00	E-06	ACP	X(4)	Copper Size
1.00	E-04	PINDUC	X(5)	Inductance
0.60	E+00	DEL	X(6)	Current Ripple Percentage
1.50	E-02	WW	X(7)	Core Window Width

DESIGN CONSTANTS

0.95	E+00	EFFUSER	User-specified efficiency
0.95	E+00	TEND	User-specified cut-off point
1.20	E+02	EI	Input RMS voltage (nominal)
1.00	E+02	EIMIN	Input RMS voltage (minimum)
1.40	E+02	EIMAX	Input RMS voltage (maximum)
3.00	E+02	EO	Output voltage
5.00	E+02	PO	Output power
2.00	E+01	VR	Output ripple specification. (actual value)
1.00	E+00	K1	Aspect ratio, centre leg depth to width
3.00	E+00	K2	Aspect ratio, window height to width
0.19	E+01	FC	Winding pitch factor
0.40	E+00	FW	Window fill factor
1.00	E-03	WBOB	Bobbin thickness
0.20	E+00	BSP	Maximum flux density
0.78	E+04	DI	Core density
0.89	E+04	DC	Copper density
1.72	E-08	RO	Copper resistivity

0.65	E+00	VD	Diode conduction drop
1.00	E-07	TND	Diode turn-on rise time
1.00	E-07	TFD	Diode turn-off fall time
0.50	E-07	TRE	Diode reverse recovery time
1.00	E-07	TSR	MOSFET turn-on rise time
1.50	E-07	TSF	MOSFET turn-off fall time
0.50	E+00	RDS	MOSFET on-resistance
1.30	E-09	CGS	MOSFET gate-source capacitance
2.10	E-10	COSS	MOSFET output capacitance
1.50	E+01	VGS	MOSFET gate-source voltage
0.70	E+00	VDB	Diode bridge conduction drop

END

DESIGN EQUATIONS

User-specified Problem Description

Part 1. Physical Constants:

PI=3.14159
XMU0=4.0E-07*PI
OMEGA=2.0*60.0*PI

Part 2. Physical Constants:
- WA - Core window area
- XMLT - Mean length of one turn
- AREA - Core cross-sectional area
- ZP - Magnetic path length

WA=K2*ABS(X(7)*X(7)
XMLT=2.0*(1+K1)*FC*X(2)
AREA=K1*ABS(X(2)*X(2))
ZP=2.0*(1.0+K2)*X(7)+(PI/2.0)*X(2)

Part 3. Winding Parameters:
- TURNS - Inductor turns
- WSIZE - Copper size
- BW - Winding build-up
- UEFF - Effective MU
- GAP - Core gap length
- RP - Inductor series resistance

TURNS=X(3)
WSIZE=X(4)
BW=TURNS*WSIZE/(FW*K2*X(7)
UEFF=X(5)*ZP/(XMU0*TURNS*TURNS*AREA)
GAP=ZP/UEFF
RP=XMLT*TURNS*RO/WSIZE

Part 4. Capacitance and Inductance Parameters:

EFF	-	Efficiency
CF	-	Capacitor capacitance
PINDUC	-	Inductance
DEL	-	Inductor current ripple percentage

```
EFF=X(1)
CF=PO/(OMEGA*VR*EO)
PINDUC=X(5)
DEL=X(6)
```

Part 5. Current Parameters:

XIM	-	Average inductor current amplitude
XDEL	-	Inductor current ripple (actual value)
XIP	-	Upper inductor current reference amplitude
XIC	-	Lower inductor current reference amplitude
XIMP	-	Peak average inductor current amplitude
XIPP	-	Peak transistor current

```
EI=SQRT(2.0)*EI
EIMIN=SQRT(2.0)*EIMIN
EIMAX=SQRT(2.0)*EIMAX
XIM=2.0*PO/(EI*EFF)
XDEL=XIM*DEL
XIP=XIM+XDEL/2.0
XIC=XIM-XDEL/2.0
XIMP=2.0*2.0*PO/(EIMIN*EFF)
XIPP=XIMP+XDEL/2.0
```

Part 6. RMS Current Parameters:

XIRMSL	-	RMS inductor current (squared)
XIRMST	-	RMS switch current (squared)
XIRMSD	-	RMS diode current (squared)

```
TEMP=(XIC*XIC+XIC*XDEL+XDEL*XDEL/3.0)
XIRMSL=TEMP/2.0
XIRMST=TEMP*(0.5-4.0*EIMIN/(3.0*PI*EO))
XIRMSD=TEMP*4.0*EIMAX/(3.0*PI*EO)
```

Part 7. Weight of the inductor:

Y1	-	EE core weight
Y2	-	Winding weight

```
Y1=ABS(DI*AREA*ZP)
Y2=ABS(XMLT*DC*WSIZE*TURNS)
```

Part 8. Other Parameters:

FREQ	-	Equivalent switching frequency used for calculating MOSFET switching loss and magnetic core loss
PF	-	Power factor (without input filter)
DELB	-	Inductor flux swing

```
FREQ=120.0*EI*(PI*EO-2.0*EI)/(OMEGA*XDEL*PINDUC*EO)
PF=SQRT(ABS(1.0-XDEL*XDEL/12.0/TEMP))
DELB=ABS(PINDUC*XDEL/(AREA*TURNS))
```

Part 9. Losses:

DD	-	Total MOSFET on time
PQ	-	Transistor losses
PD	-	Diode losses
POF	-	Filter losses
EFF	-	Efficiency of the boost power stage

```
DD=1.0-2.0*EI/(PI*EO)
PQ=RDS*XIRMST*DD+CGS*VGS*VGS*FREQ+EO*(XIC*TSR+XIP*TSF)*FREQ/3.6
$ +EO*(XIC*TRE)*FREQ/2.4
PD=PO*VD*(2.0*EI/(PI*EO))/EO+EO*FREQ*(XIP*TND+XIC*TNF)/7.2
$ +EO*FREQ*XIC*TRE/2.4
POF=XIRMSL*RP+23.1*(AREA*ZP)*(ABS(DELB/(2.0*SQRT(3.0))))**2.6*(ABS(FREQ/2))**1.31
EFF=PO/(PO+PQ+PD+POF)
```

Part 10. Cut-off Frequency:

T	-	User-specified cut-off point in terms of the seconds
TN	-	MOSFET on-time at the cut-off point
TF	-	MOSFET off-time at the cut-off point
FEND	-	Switching frequency at the cut-off point

```
T=TEND/120.0
TN=XDEL/(EI/PINDUC-OMEGA*XIP*COS(OMEGA*T)/SIN(OMEGA*T))
TF=XDEL*SIN(OMEGA*(T+TN))/(EO/PINDUC+OMEGA*XIC*SIN(OMEGA*(T+TN))
$ -EI*SIN(OMEGA*(T+TN))/PINDUC)
FEND=1.0/(TN+TF)
```

Part 11. Switching Frequency in the Middle of the Rectified Line Cycle:

TNMID	-	MOSFET on-time in the middle of the half line cycle
TFMID	-	MOSFET off-time in the middle of the half line cycle
FMID	-	Switching frequency in the middle of the half line cycle

```
T=0.5/120.0
TNMID=XDEL/(EI/PINDUC-OMEGA*XIP*COS(OMEGA*T)/SIN(OMEGA*T))
TFMID=XDEL*SIN(OMEGA*(T+TNMID))/(EO/PINDUC+OMEGA*XIC*SIN(OMEGA*(T+TNMID))
$ -EI*SIN(OMEGA*(T+TNMID))/PINDUC)
FMID=1.0/(TFMID+TNMID)
```

Part 12. Other terms:

WSIZECM	-	Inductor wire size in terms of circular mills
PDB	-	Bridge rectifier loss

```
WSIZECM=WSIZE*100.0*100.0*197238.66
PDB=VDB*XIM*4.0/PI

END

OBJECTIVE FUNCTION
```

F=Y1+Y2

END

CONSTRAINT EQUATIONS

User-specified Efficiency Constraint

C(1)=EFF-EFFUSER

Fill Window Constraint

C(2)=WA-TURNS*WSIZE/FW-WBOB*X(7)*K2

Maximum Inductor Ripple

C(3)=2.0-DEL

Core Saturation

C(4)=BSP-X(5)*XIPP/(AREA*TURNS)

Minimum Wise Size

C(5)=WSIZE-7.29E-8

Minimum Inductor Ripple

C(6)=DEL-0.01

C(7)=X(1)-0.50
C(8)=X(2)-0.001
C(9)=TURNS-1.0
C(10)=X(6)-0.01
C(11)=X(7)-0.001
C(12)=1.0-X(1)

END

OUTPUT

The efficiency is:
PRINT EFF

The inductance is:
PRINT X(5)

Number of inductor turns is:
PRINT TURNS

The wire size is:
PRINT WSIZE

The wire size in circular mills is:
PRINT WSIZECM

The inductor core centre leg width is:
PRINT X(2)

The inductor core window width is:
PRINT X(7)

The capacitor is:
PRINT CF

The core and copper weight are:
PRINT Y1, Y2

The weight of the inductor is:
PRINT F

The inductor series resistance is:
PRINT RP

The effective mu and core gap are:
PRINT UEFF, GAP

The upper, average, lower inductor current amplitudes are:
PRINT XIP, XIM, XIC

The inductor current ripple percentage is:
PRINT DEL

The peak and RMS switch current are:
PRINT XIPP, SQRT(XIRMST)

The power factor without input filter is:
PRINT PF

The transistor and diode losses are:
PRINT PQ, PD

The filter loss is:
PRINT POF

The diode bridge loss is:
PRINT PDB

The equivalent switching frequency is:
PRINT FREQ

The switching frequency in the middle of the rectified line cycle is:
PRINT FMID

The switching frequency at the cut-off point is:
PRINT FEND

END

VARIABLE SCALING

0.1	VSCAL(1)
0.001	VSCAL(2)
10.0	VSCAL(3)
0.0000001	VSCAL(4)

```
0.00001         VSCAL(5)
1.0             VSCAL(6)
0.001           VSCAL(7)

END

CONSTRAINT SCALING

1.0             CSCAL(1)
0.0001          CSCAL(2)
1.0             CSCAL(3)
0.3             CSCAL(4)
0.0000001       CSCAL(5)
1.0             CSCAL(6)
1.0             CSCAL(7)
0.001           CSCAL(8)
1.0             CSCAL(9)
1.0             CSCAL(10)
0.001           CSCAL(11)
1.0             CSCAL(12)
1.0             CSCAL(13)
0.001           CSCAL(14)
10.0            CSCAL(15)
0.0000001       CSCAL(16)
0.00001         CSCAL(17)
1.0             CSCAL(18)
0.001           CSCAL(19)

END

OBJECTIVE SCALING

1.0             FSCAL

END

CONTROL

1001          MAXFN  -  Number of inner iterations
1             IPR1   -  Print control variable
0             IPR2   -  Print control variable
2500          IW     -  Storage array size
1             MODE   -  1=Hessian estimate not available
0             DFN    -  Required change in objective
0.0005        CTOL   -  Constraint tolerance
0.0001        VTOL   -  Variable tolerance
0.01          DEL    -  Gradient delta X
```

Appendix D. REFERENCES

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