Development of Bidirectional Module using Wafer-Bonded Chips

by

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Abstract

This study focuses on the development of a bidirectional module (BD-module) using a wafer-bonded dice for high power/high frequency operating systems. A bidirectional switch can be used for applications that require bidirectional current conducting and blocking, such as matrix converters. Unlike conventional bidirectional switches that use two IGBTs and two diodes, this study employs a wafer-bonded bidirectional switch that has a symmetrical layout at the front and back. The chip can be illustrated as two unidirectional chips that are bonded back-to-back. This particular structure is advantageous in increasing power density by using less number of chips. The forward voltage drop is made lower than conventional BD-switches by eliminating the diode in series with the IGBT. It should be noted that a bond-line at n^- drift region has low mechanical strength, and thick wafer substrate increases conduction loss, which increases heat flux. In addition, gate pads at both the front and back require a stringent packaging process with precise alignment, low thermal resistance, and alleviated residual stress at the chip.

Packaging options were considered, including the conventional wire-bonding method, the flip-chip method, a planar-solder joint, the direct-lead-bonding, and the metal-post-interconnect-parallel-plate-structure (MPIPPS). Reference packages were

analyzed based on thermal/electrical characteristics, thermo-mechanical stress (reliability), and ease of process. To achieve high frequency operation with low temperature rise, a low thermal resistance and low parasitic inductance were the primary concerns for the package. For this reason, the planar joint was chosen as an interconnection layer, as it covers the entire pad area with solder, which minimizes thermal resistance. The planar joint enables the building of the module in a vertical structure, which minimizes the size of the power loop so that parasitic inductance can be reduced.

A preliminary module with the planar joint and indented lead frame was designed, and key parameters were analyzed by simulations. The dielectric performance was simulated by Maxwell, and it showed the maximum 9 kV/mm electric field at the gap between guard ring and lead frame that was much higher than the dielectric strength of air (3-kV/mm). Adding a spacer was considered in order to reduce the electric field intensity, but the addition of the spacer increased thermal resistance up to 35.8% with 0.8 mm height. Since increasing thermal resistance was the preferred option, a molding compound with high dielectric strength (19 kV/mm) was chosen to fill the gap in the modules. Parasitic inductance was analyzed by Q3D simulation and the result was 3 nH, which was 8 nH lower than a conventional module with similar power ratings (MMIX1G82N120A3V1).

The developed package showed superior electrical and thermal characteristics, but the double-sided structure introduced larger thermo-mechanical stress than a conventional

wire-bonded module. Symmetrical planar joints at both the top and bottom induced excessive thermo-mechanical stress to both chip and joints. To enhance the reliability of the interconnection layers, the hourglass-shaped joint for large chip attachment was designed. ANSYS simulation was used to analyze thermo-mechanical stress at the solder layer, and the hourglass joint showed 33.3% lower change of plastic-strain energy density (ΔW_{avg}) than the fillet joint. Moreover, the maximum stress point of the hourglass joint was the center of the curved surface, but the fillet joint's maximum stress point was at the interface between the chip and joint where the intermetallic compound (IMC) exists. For this reason, the planar-hourglass joint is expected to enhance the reliability of the interconnection layer, and thus enhance the lifetime of the module.

The mismatch of CTEs (coefficient of thermal expansion) among packaging materials builds up initial stress in the package after the reflow process. Conventional die that has solid silicon substrate can stand the initial stress, but the bonding interface of the wafer-bonded die is not strong enough to withstand the initial stress. As a result, the developed module using BD-IGBT showed chip delamination during a packaging process. As a solution for the peel stress reduction, the compressive post was developed and implemented into the double-sided module. The compressive posts were implemented during a vacuum reflow process using a high temperature solder ball ($Pb_{93.5}Sn_5Ag_{1.5}$) as core material and a solder preform ($Sn_{63}Pb_{37}$) as bonding material. During the heating phase of the reflow process, the solder preform melts and makes connections between the lead frame and DBC substrate. As the reflow process starts cooling, the solder post

shrinks more than the silicon chip to be protected, and pulls down the lead frame that result in compressive force to the chip. As an indicator of the compressive force to the chip, the surface curvature of the lead frame was monitored before and after packaging with different number of posts. Comparison of curvature changes revealed that the height displacement at the edge of the lead frame was changed from +13.5 um to –17.5 um, as the number of compressive posts was changed from none to six. ANSYS simulation results showed equivalent curvature changes as experiment results, and the simulated tensile stress at the chip with four compressive posts showed 0.6 MPa that was 3.52% of the non-post case. Another advantage of the compressive post was a reduction of the plastic strain at the die-attach layer. The influence of the distance between chip and post to the plastic strain at the die-attach layer was parametrically studied, and the simulation result with 1 mm gap with four posts turned out to be the right combination. The plastic strain at the die-attach layer with the right configuration showed 87% of strain compared with the non-post case, which implies the extended fatigue lifetime of the joint.

The forward voltage drop of the developed BD-module was measured as 2.85 V, whereas the conventional module with a forward diode showed 3.5 V. However, the reduced die-attach area limited the heat dissipation due to gate pads, and the thermal impedance was measured 17.24% higher than the conventional module. The package inductances was measured as 0.49 nH and 3.29 nH before and after encapsulation, and the blocking voltage was 800 V with 250 μA leakage current.

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Chapter 1. INTRODUCTION

1.1. Application Background

Over the past decades, energy production and consumption of renewable energy sources were significantly increased, and energy produced by renewable sources comprised 8% of the total energy consumption in the United States of America [1]-[4]. Figure 1-1 shows the trend of renewable energy sources from 1950 to 2012 [3]. Hydroelectric power and biofuel have been the dominant renewable sources, and wind, geothermal, and solar power have significantly increased over the last decade.

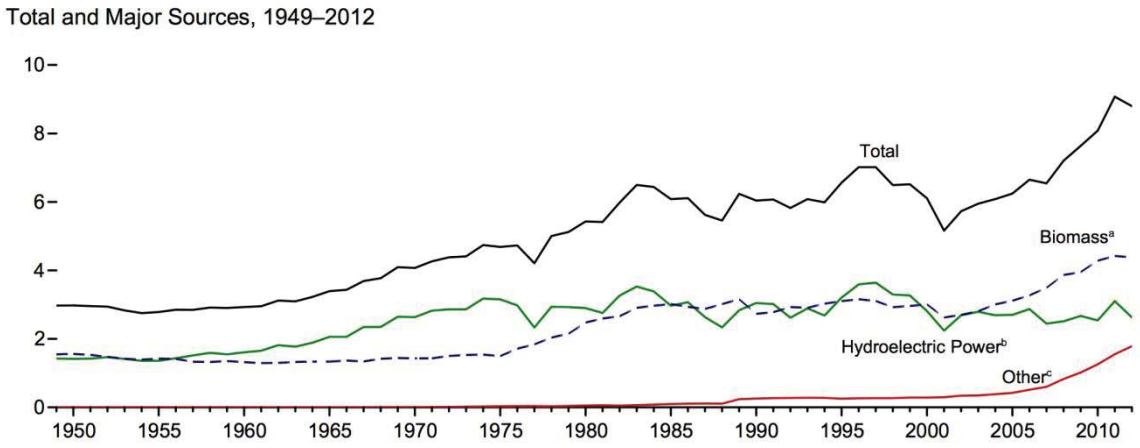


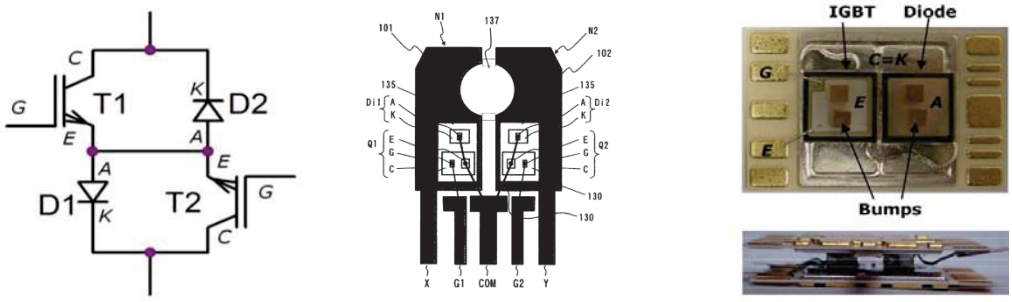
Figure 1-1. Trends in renewable energy production/consumption from 1950 through 2012 [3].

Renewable sources, such as hydroelectric, solar, and wind transfer, have produced energy in an electricity form. Generated electricity is either transmitted to a grid or stored in a battery, and this process requires switching converters. A traditional grid has unidirectional energy flow from plants, whereas a modern smart grid requires bidirectional energy flow due to numerous local energy sources. Numerous circuit topologies were developed for bidirectional energy

transmission, and a bidirectional switch plays an important role for this type of converters, which can include matrix converters, current-mode inverters, and bidirectional on-board chargers for electric vehicles.

1.2. Conventional Bidirectional Modules

A bidirectional module should be able to conduct and block currents in both forward and reverse directions. Using two IGBTs and two diodes is the conventional method used to realize a bidirectional switch, and Figure 1-2 shows the configuration of four chips [1], [6]. The bottom of the chip is normally attached to a substrate, and the top can be either connected by bond wire (Figure 1-2(b)) or directly connected to other chips by spacers (Figure 1-2(c)). Even though the vertical structure illustrated in Figure 1-2(c) helps to reduce parasitic inductance, large loop due to four discrete dice is an inevitable source of extra inductance. Since four dice require large substrate, this type of module is advantageous to dissipate heat flux. At the same time, however, large substrate and multiple dice increase the manufacture cost and weight. The diode in series with IGBT increases forward voltage drop, and results in additional conduction loss.



(a) (b) (c)

Figure 1-2. Schematic of conventional bidirectional switch with two IGBTs and two diodes (a), bidirectional module with bond wire for the top side (b), and the bidirectional module with four chips and copper posts (c).

To avoid using a pair of IGBTs and diode, industries have developed IGBTs with reverse-blocking capability. With a reverse-bias condition, p^+-n^- junction depletes within the chip, but the electric field at the edge of the chip results in a breakdown [7]. This problem can be overcome by using the technique called isolation diffusion, which permits folding up of the reverse-blocking IGBTs' lower p^+ layer at the chip edge as shown in Figure 1-3 [8]. Since the reverse-blocking diode is integrated into the IGBT die, it is especially useful for current source inverters and matrix converters that require bidirectional switches. Compared with the bidirectional module with four discrete chips, the bidirectional module with a reverse-blocking IGBT has lower conduction loss, lower parasitic inductance, and a smaller size.

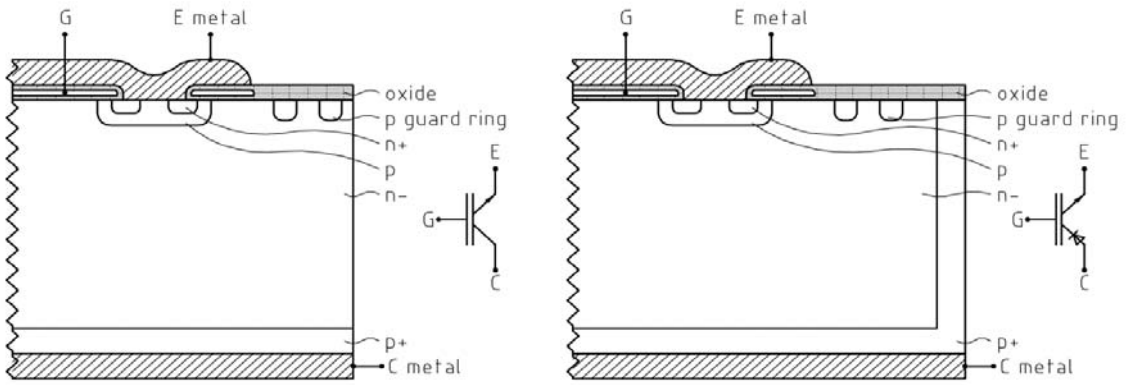


Figure 1-3. Cross-sections of conventional NPT IGBT (a), and reverse-blocking IGBT (b) [7].

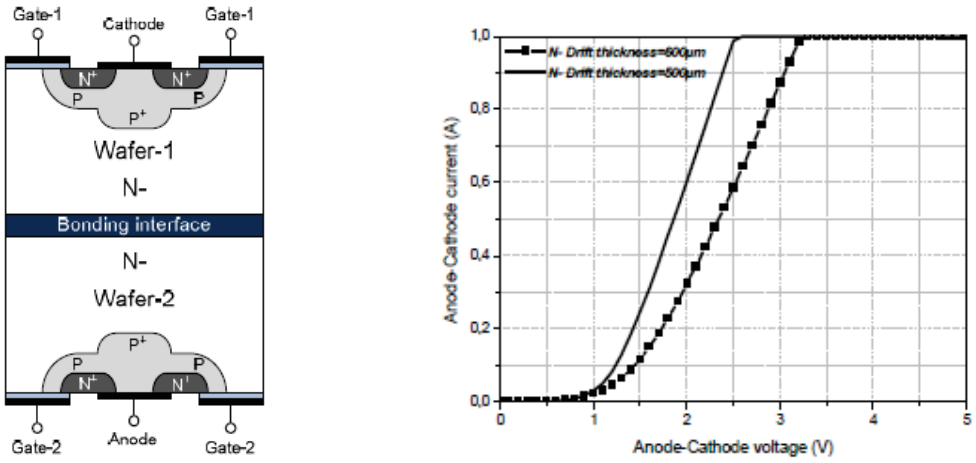
Another popular method for realizing a bidirectional switch is using a module with an IGBT and an anti-parallel diode. By connecting two modules back-to-back, current flows through the IGBT of one module and the diode of another module. However, this method has the same disadvantages as the four-chip module shown in Figure 1-2.

Another possible method to build a bidirectional module is using a double-sided IGBT that has gate and col/emitter pads at both the top and bottom. A double-sided IGBT is basically a four-quadrant switch that can conduct and block currents in both directions. More details about double-sided IGBT (bidirectional IGBT) are provided in the following section.

1.3. Introduction of Bidirectional IGBT

A bidirectional IGBT is a monolithically integrated switch that has MOS sections at both the front and back. A bidirectional IGBT can be fabricated by a wafer-bonding method or a double-sided photolithography method [9], [11]. The wafer-bonding method in Figure 1-4 polishes the bottoms of two unidirectional IGBTs, and bonds by high-temperature annealing

(400°C to 1100°C). Since the wafer-bonding method uses two identical dice, the bonded-die has symmetrical-MOS characteristics in both forward and reverse conditions. However, the bond-line is non-ideal and degrades conducting and blocking characteristics during its lifetime. The on-state voltage drop heavily depends on the thickness of n^- substrate that has to be precisely controlled during the polishing stage.

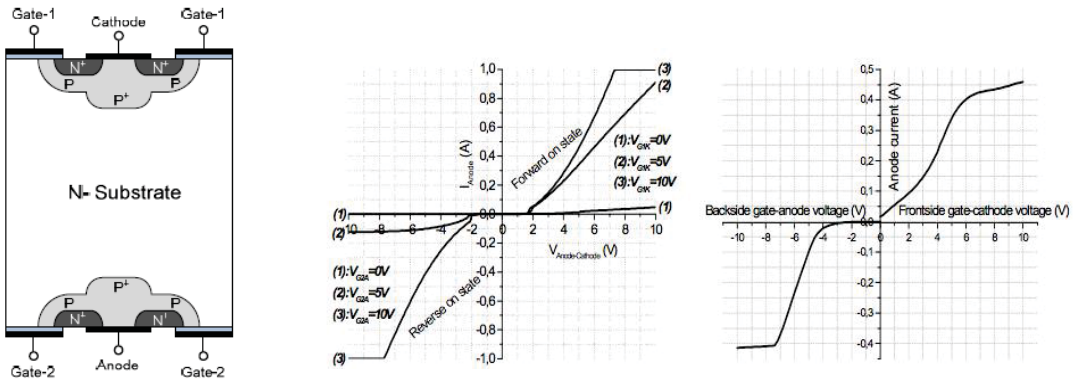


(a) (b)

Figure 1-4. Cross-section of wafer-bonded bidirectional IGBT (a), and influence of n^- substrate thickness to the I-V characteristics (b) [9].

The double-sided photolithography method in Figure 1-5 forms MOS regions at the top and bottom of a single wafer [9]. Since only one wafer is used in this process, the electrical characteristics are not influenced by the substrate thickness. Unlike the fusion-bonding process, the absence of bond-line provides better reliability for its lifetime. However, this process requires two steps to form MOS regions, and can result in asymmetric electrical characteristics in forward and reverse conductions. Figure 1-5 (b) shows I-V characteristics in both forward and reverse conduction, and they are fairly similar. However, the threshold voltage at the front and back

MOS show significant differences as a result of the two-step process that causes contamination during the process.



(a) (b) (c)

Figure 1-5. Cross-section of bidirectional IGBT by double-side photolithography process (a); I-V characteristics (b); and threshold voltage in forward and reverse conductions (c) [9].

1.4. Review of Existing Double-Sided Packages

1.4.1. Direct-lead-bonding

A direct-lead-bonding uses a copper lead for the top side connections as illustrated in Figure 1-6. This bonding method overcomes the limitations of the wire-bonding, which has high parasitic inductance and inferior heat dissipation. However, large bonding area to the copper lead frame creates residual thermo-mechanical stress after the packaging process. Both packaged chip and die-attach layer experience much higher thermo-mechanical stress than wire-bonding that results in reduced fatigue lifetime.

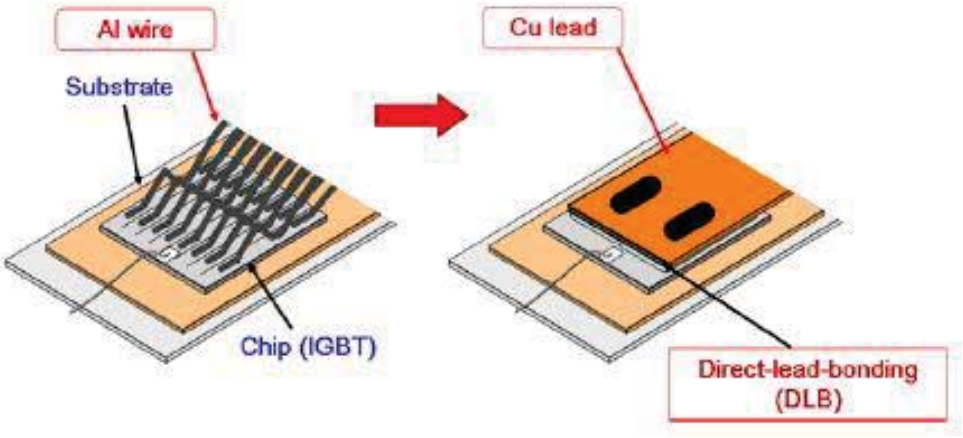


Figure 1-6. Illustration of the direct-lead-bonding from Mitsubishi [10].

1.4.2. Double-sided module

Symmetrical solder layers at the top and bottom is the most straightforward method used in realizing a planar joint (Figure 1-7). Since both top and bottom substrates are electrically isolated, double-sided cooling is available. Using this method, electrical/thermal resistance can be minimized and parasitic inductance can be also minimized. However, the symmetrical solder layers induce excessive tensile stress to the chip, and the degradation of the bond-line in the bidirectional IGBT can be accelerated or even broken during the packaging process.

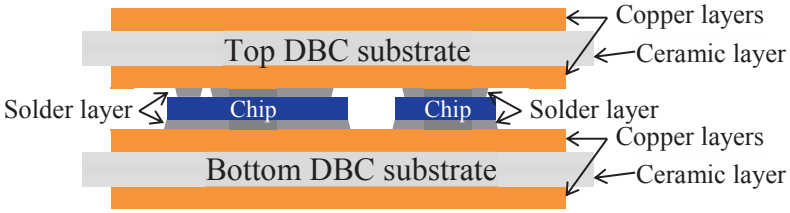


Figure 1-7. Illustration of the double-sided module using symmetrical substrates.

1.4.3. BGA interconnections

The flip-chip method in Figure 1-8 is a popular method for packaging of micro-controllers. Ball-grid-array (BGA) interconnections enable multiple connections in a vertical direction, and

minimize parasitic inductance. There were several attempts using the same concept to develop the package for power semiconductors. Solder bumps were used to make a direct connection from chip to substrate, and the shape of the solder bumps could be manipulated into an hourglass shape to increase reliability [16], [17]. However, the top of the chip with the solder bump has large thermal resistance, and the major thermal path becomes the bottom connection to the DBC substrate. Using multiple solder bumps distributes thermo-mechanical stress to a wide area, and the bidirectional IGBT will have less stress than if it has large solder layers.

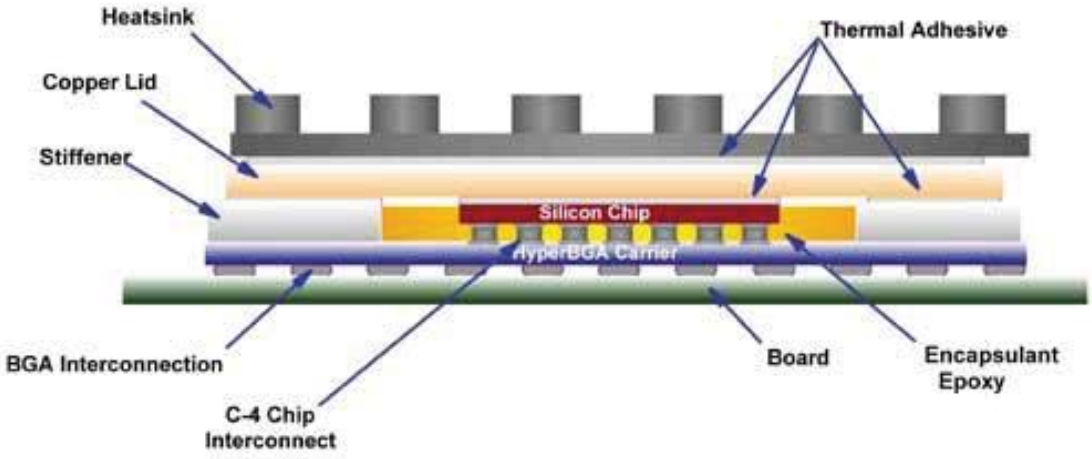


Figure 1-8. Illustration of the packaged chip by BGA interconnections.

1.4.4. Metal-post-interconnect-parallel-plate-structure (MPIPPS)

The metal-post-interconnect-parallel-plate-structure (MPIPPS) structure in Figure 1-9 uses several copper posts with different heights [13]. The purpose of the metal posts is to compensate for the height difference between chips and to increase dielectric strength. This structure dissipates some amount of heat to the top substrate, but the major thermal path is still to the

bottom substrate. Vertical structure gives less parasitic inductance, but the packaging process is rather complicated.

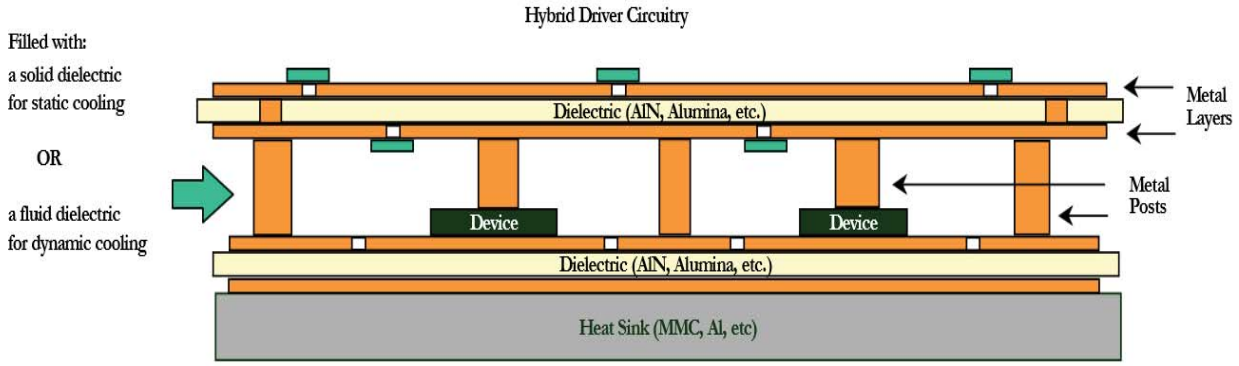
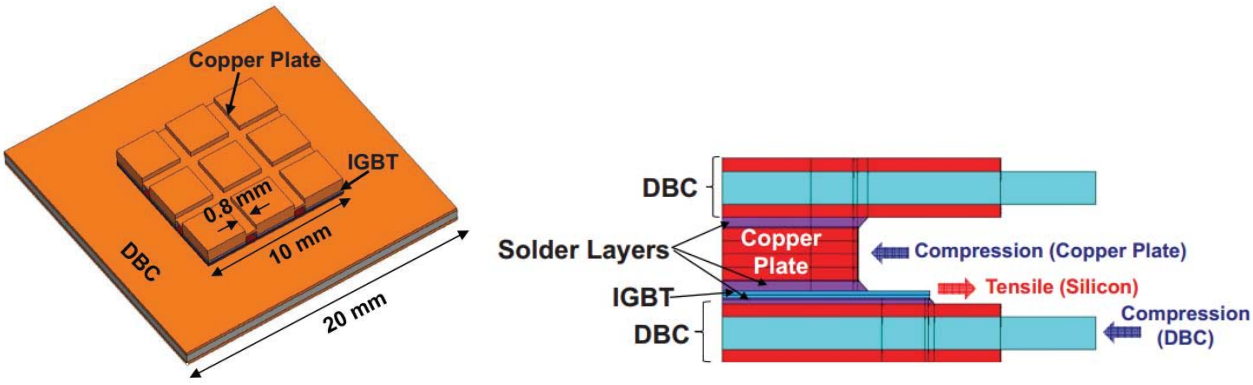


Figure 1-9. Illustration of the MPIPPS module [13].

1.4.5. Trenched copper plate

Trenched copper plate is similar to the plated-bonded module in Lexus, but this method focuses more on the reduction of thermo-mechanical stress at solder joints [12]. The copper plate between chip and substrate maximizes thermal, electrical, and dielectric performances. However, the copper plate increases thermo-mechanical stress induced by CTE mismatch between packaging materials. To distribute thermo-mechanical stress, the trenched copper plate was developed by dividing the copper plate into small pieces of matrix by a chemical etching process. By using trenched copper plate, the maximum plastic strain could be reduced by 53.7%, but thermal performance was also degraded by 9.04% [14], [15].



(a) (b)

Figure 1-10. Trenched copper plate (a) and side view of the double-sided module with trenched copper plate (b) [14].

1.5. Research Motivations and Objectives

Previous sections showed limitations of the conventional BD-module to support modern power electronics systems that require high power density and high switching frequency. To overcome the problem of a BD-module that uses multiple switches, the wafer-bonded bidirectional IGBT was used in this study. Smaller loop size is essential for high frequency switching, and using single chip (wafer-bonded IGBT) for realizing bidirectional switch can reduce loop size by a factor of four. However, the wafer-bonded IGBT has thicker substrate than the unidirectional IGBT, and it results in higher conduction loss that requires advanced thermal management. A planar joint is well-known for its superior thermal management compared to bond wire, and also enables double-sided cooling of the module. In addition to superior thermal performance, a planar joint also gives lower parasitic inductance and lower electrical resistance compared with bond wire. However, there is a trade-off between superior thermal/electrical performance and thermo-mechanical stress. In the past, increased thermo-mechanical stress by

double-sided structure did not fail the module during a reflow process because silicon is a rugged material compared with other packaging components. However, the wafer-bonded IGBT has a bond-line at the middle of the n^- drift region, and it is vulnerable to mechanical stress. Even though the planar joint has this drawback, its electrical/thermal performance is still useful in achieving high power density and switching frequency. Therefore, several packaging options for planar joints were reviewed in terms of thermal performance, electrical performance, reliability, and ease of process. A special bonding technique was developed to counteract planar-joint-induced thermo-mechanical stress so that stress at the chip can be alleviated. Figure 1-11 summarizes thermal and electrical performances of wire-bonded modules and double-sided modules in Section 1.4.

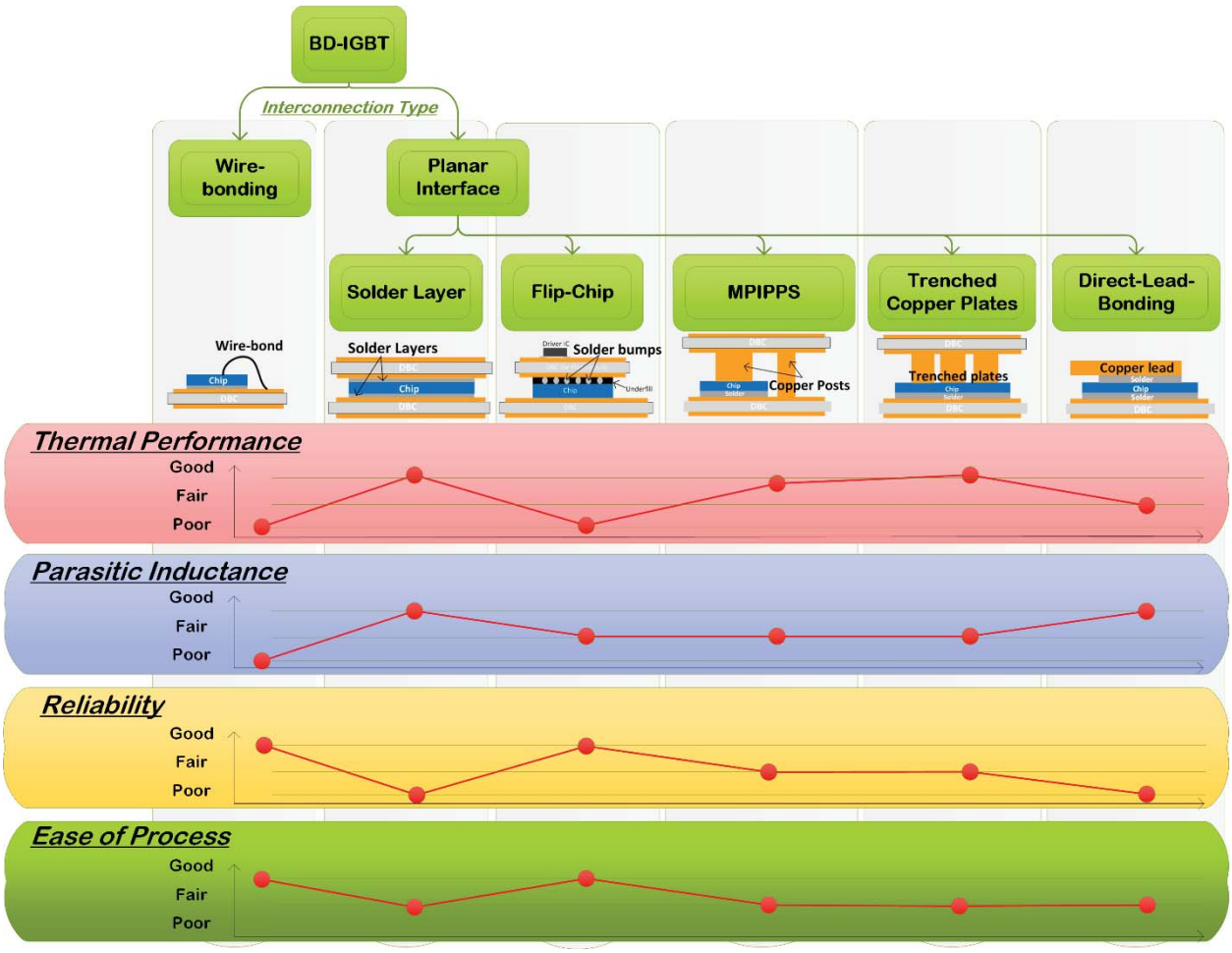


Figure 1-11. Categorized interconnection methods with thermal performance, parasitic inductance, reliability, and ease of process.

Because the expected application of the module is a high frequency/high power system, minimization of the parasitic inductance and thermal resistance are important. For this reason, the double-sided package with solder joints at the top and bottom is chosen as an interconnection method, because the entire pad area of the chip can be covered by a solder joint in order to minimize thermal resistance. However, the symmetrical structure of the double-sided module induces a large thermo-mechanical stress to chip and die-attach layer. Because of the stress, packaged chips warp or crack during a reflow process [18]. This can be a critical problem for

packaging the wafer-bonded IGBT. To solve this problem, the solder-posts-aided bonding method was developed. This method has all the advantages of a planar joint while reducing thermo-mechanical stress at the chip. This method can be used not only for the wafer-bonded IGBT, but also for conventional chips.

Another challenge of this study is the symmetrical layout of the chip. A normal unidirectional chip has a gate pad on the top side, and it can be electrically connected by a bond wire. However, the bidirectional chip has gate pads at both the front and the back, and they cannot be connected by a bond wire. The gate pad at the back has to be connected to the substrate, and it requires precise alignment during the packaging process. Multiple fixtures made of Cirlex are used for the alignment of each layer, such as bottom solder preform, chip, top solder preform, and lead frame.

To address these issues, the dissertation is organized as below.

Chapter 2 presents the synthesis and design of the package for the bidirectional chip. For the double-sided structure, the clearance between guard ring and top substrate is important to ensure the blocking voltage. In case of the BD-IGBT, the guard ring on top and bottom sides of the chip require clearances from substrates so that the electric field can be controlled. The developed packaging process that successfully controlled the height of the joint is introduced in this chapter. The indented lead frame was developed to enable single-step process and alleviate thermo-mechanical stress at the solder joint. The optimum parameter was found by parametric study, and the results are stated in this chapter. Since low parasitic inductance is important for

safe and fast switching, the structure of the module was optimized by FEA simulation. This chapter summarizes the design specifications for the packaging of the double-sided die, and introduces the packaged module.

Chapter 3 introduces the hourglass joint for large-chip attachment. The thermo-mechanical stress and thermal resistance of the hourglass joint was parametrically studied and compared with a conventional fillet joint. After the optimization of the structure, a packaging process that can control the height and shape of the die-attach layer was developed for the hourglass joint. For reliability assessment, samples were fabricated with an hourglass joint and a fillet joint, and power cycling was initiated with fabricated samples.

Chapter 4 presents the developed solder-posts-aided-bonding method that leaves residual-compression force to the packaged chip. This bonding method forms isolated solder posts around a chip that is made of solder ball as a core. Since solder has higher CTE than silicon, the solder post shrinks more during a cooling phase of reflow process. As a result, solder posts leave residual compression force to the chip, and help to alleviate tensile stress to the chip. To verify the concept, samples with different numbers of posts were fabricated, and the surface curvature of the lead frame was measured before and after packaging. After verifying the concept, the original layout of the module was modified with posts, and the module was fabricated. Measured parasitic inductance and thermal resistance were well matched with expected values, as shown by simulation and thermal cycling that were initiated with fabricated samples.

Chapter 5 presents the complete bidirectional module with the compressive posts. The developed module was encapsulated using molding compound, and the key parameters were experimentally measured. This chapter shows the test setup for the measurement of thermal impedance, parasitic inductance, blocking voltage, and on-state voltage drop. The measurement results are compared with the benchmark module, and the comparisons are discussed in this chapter.

Chapter 6 summarizes the research, and discusses future works.

1.6. Main Contributions

- A package for double-sided die was developed
- An indented lead frame has been developed and optimized by parametric study
- An hourglass joint for large-chip attachment was investigated and the packaging process was developed
- The compressive post was developed and experimentally verified
- The complete bidirectional module was characterized

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Chapter 2. SYNTHESIS AND DESIGN OF THE PACKAGE FOR DOUBLE-SIDED DIE

2.1. Introduction

In this research, a bidirectional surface-mount module was developed for the soft-switched AC-link photovoltaic inverter [1]. To support high power applications, the focus of the module development was to enable noise-free switching, high power density, and low temperature rise. Figure 2-1 shows the concept of the developed module in comparison with a conventional transfer-molded module from Mitsubishi. The two modules are somewhat similar, but the module developed in this research is more optimized for high frequency switching and a reliable packaging process for the bidirectional chip. Both modules use a lead frame along with a planar joint to make the connection from a top-side joint to outer circuitry. By using a planar joint with a lead frame rather than a bond wire, the electrical resistance, thermal resistance, and parasitic inductance can be significantly reduced. One main difference between the two modules is the substrate material. To enhance transient thermal performance, the Mitsubishi module uses a copper block as a substrate, but the combination of the double-sided structure and bulky copper substrate will introduce a large thermo-mechanical stress to both chip and joint. Conventional chips may able to stand the stress during the packaging process, but the stress will be too much for the bidirectional IGBT with the bond-line. For this reason, direct-bonded-copper (DBC) substrate is used for this study. Since DBC has an alumina layer, which is a dielectric material,

the module does not require an additional isolation layer for heat-sinking to minimize the junction-to-case thermal resistance. After the reflow process, the module is encapsulated with a molding compound to protect the module from moisture and mechanical stress.

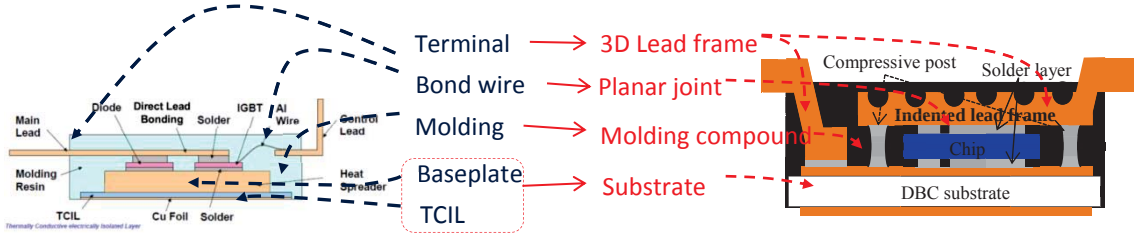


Figure 2-1. Comparison between Mitsubishi module with direct-bonded-lead (left) and developed module with the indented lead frame and compressive post (right) [10].

2.2. Designed Package for the Double-Sided Die

To increase its current capacity, two 50 A dice are paralleled in the module (Figure 2-2). The DBC has a silver coated surface to prevent oxidization, and both the DBC and the lead frame are prepared by a chemical etching process. A tin-lead solder preform was used for packaging, and gate pads were bonded with individual preforms. In the case of the packaged dice, the illustration in Figure 2-3 shows the module with a custom die that has a gate pad at the corner. The lead frame has a three-dimensional structure so that one side can be attached to the substrate, and the other side can be attached to the top of the chip. The indented lead frame plays an important role in minimizing parasitic inductance and thermo-mechanical stress, and more details on this will be discussed in Section 2.5.

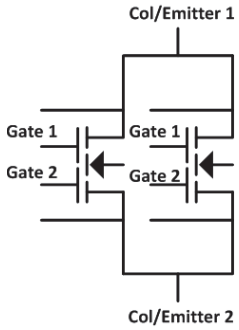
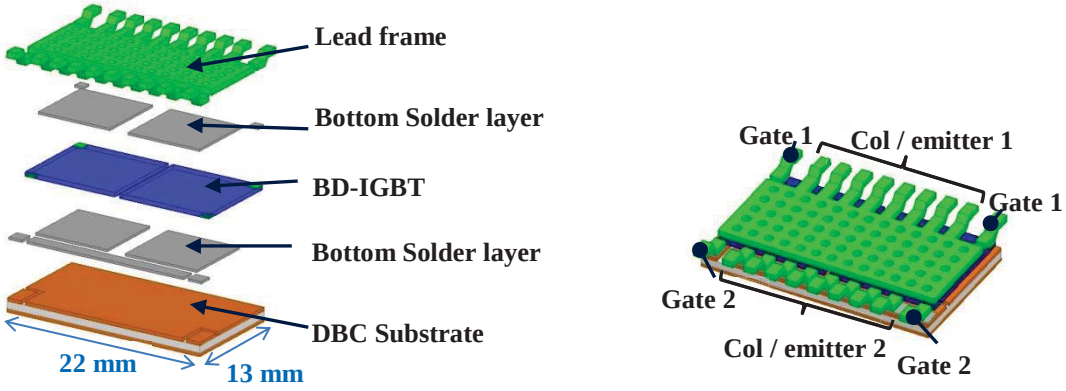


Figure 2-2. Schematic of the bidirectional module in Figure 2-3 with two bidirectional IGBTs in parallel.



(a) (b)

Figure 2-3. Lay-up of the developed module (a) and illustration of the packaged module (b) with two bidirectional IGBTs in Figure 2-2 with specifications in Table 3-1 (see Table B.(6) for 3D model).

2.3. Design for Dielectric Strength

A dielectric performance of the module is important for the safe operation of high power applications. To analyze the electric field in the module, Maxwell simulation model was built and analyzed. Figure 2-4 shows the simulation model with observation planes for monitoring the electric field in the module. The simulation model was built based on the actual dimensions of the packaging components, and a reverse-bias condition was simulated by applying high voltage to the DBC side, and ground condition at the lead frame side.

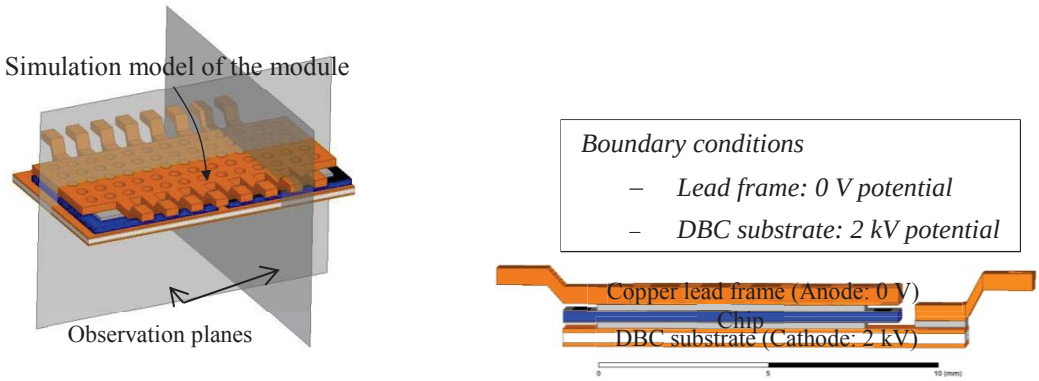
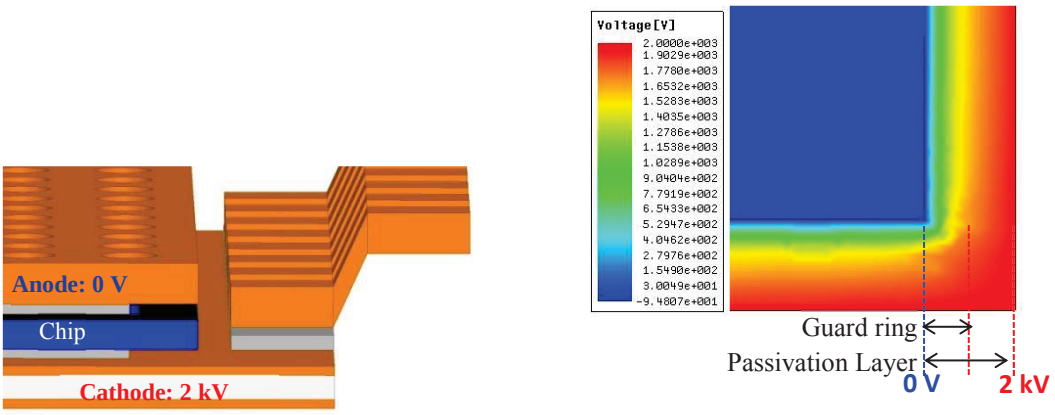


Figure 2-4. Maxwell simulation model for the analysis of electric field in the developed module in Figure 2-3; the model with electric-field observation planes (a), and the side view with polarity of the voltage excitation in Figure 2-5 (b) (find simulation setups in Appendix B.5 and original file in Table B.(7)).

Since the guard ring attenuates the electric field at the edge of the chip, the boundary condition with graduate voltage distribution in Figure 2-5(b) was used. There is a p-type guard ring under the passivation layer to reduce the electric field at the junction, and it results in gradient voltage distribution between the guard ring and pad area. Figure 2-5(b) shows the assigned voltage at the guard ring area. The edge of the chip has 2 kV voltage potential, and the pad area has 0 V potential.



(a) (b)

Figure 2-5. Boundary conditions of the simulation model in Figure 2-4; 2 kV at DBC substrate and 0 V at the lead frame (a), and gradient voltage excitation at guard-ring of the chip (b).

The maximum electric field was found at the gap between the lead frame and the chip as 9-kV/mm higher than the dielectric strength of air with 34% relative humidity at 25°C, which is about 3 kV/mm (Figure 2-6)[2]. There were two options to increase the dielectric performance while keeping the overall structure of the module. The first method was using spacers to increase the physical distance from chip to lead frame [3], [4]. By increasing the area between chip and substrate, the intensity of the electric field can be reduced, but the thermal resistance and parasitic inductance will be increased accordingly. Figure 2-7 shows how an additional copper layer can influence the maximum electric field and thermal resistance. Electric field decreases as the gap increases, and the electric field reduces to below 3 kV/mm after a height of 0.65 mm lower than dielectric strength of air. However, the thermal resistance also increases, and the thermal resistance with 0.8 mm is 35.8% higher than the thermal resistance with 0.2 mm height. Because low thermal resistance and low parasitic inductance were the main goal of this study,

the original structure remained the same, but a high dielectric strength material was used for the encapsulation.

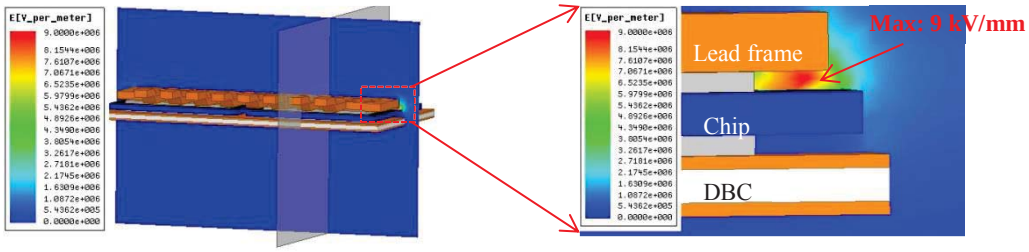
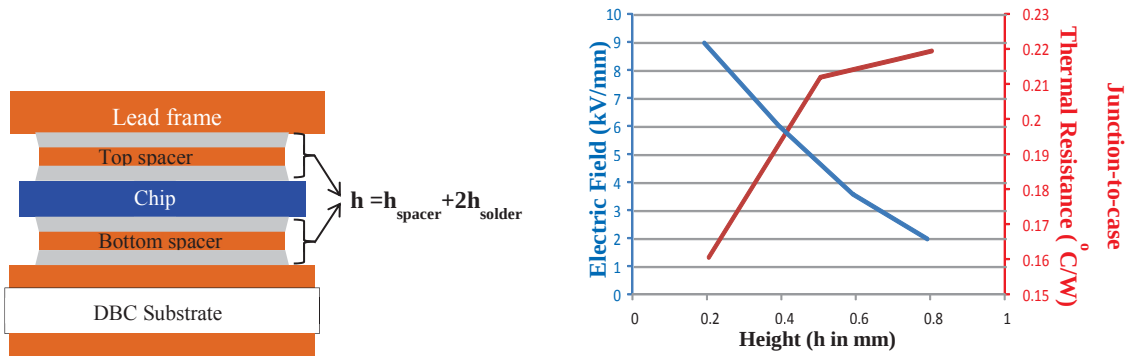


Figure 2-6. Simulated maximum electric field in the model in Figure 2-4 with boundary conditions in Figure 2-5 and simulation conditions in Appendix B.5.



(a) (b)

Figure 2-7. Addition of the spacer to the structure in Figure 2-4 to reduce the electric field (a), and the increase of thermal resistance due to the spacer (b).

2.4. Selection of the Encapsulation Material for Reduction of Viscoplastic Strain and Enhancement of Dielectric Strength

The selection of the encapsulation material was mainly focused on dielectric strength, CTE, and viscosity. The dielectric strength was desired to be more than 60% higher than the device rating with consideration of the transient voltage peak (2 kV), and the maximum electric field with this condition was 9 kV/mm. The encapsulation material was chosen that has higher

dielectric strength than 9 kV/mm, and viscosity was preferred to be below 15000 cps at room temperature due to lab facility limitations. Considering the maximum operating temperature of the module is 125^{o}C, the glass transition temperature is preferred to be higher than the maximum operating temperature. In terms of thermo-mechanical stress, the CTE around 20 ppm benefits from being joined with a solder so that the molding compound can damp down the thermo-mechanical stress at the joint. The simplified structure that consists of DBC substrate, solder joint, chip, and molding compound has simulated with different CTEs of the molding compound. Figure 2-9 shows the ANSYS simulation results with CTEs from 5 ppm/^{o}C to 40-ppm/^{o}C. When the CTE of the molding compound is around 20 ppm/^{o}C, the viscoplastic strain at solder joint is reduced to the minimum, which means the fatigue-lifetime of the joint can be extended. Therefore, it is recommended to select the molding compound that has similar CTE with solder to attenuate the thermo-mechanical stress.

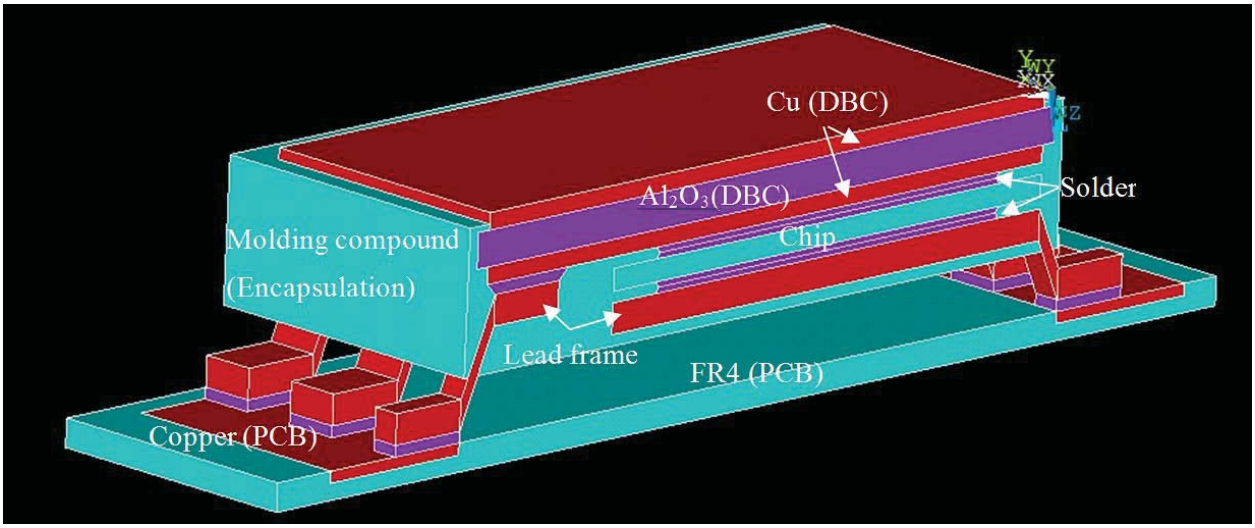


Figure 2-8. ANSYS simulation model of the encapsulated module in Figure 5-6 (see Appendix D for design process and Table B.(1) for simulation files).

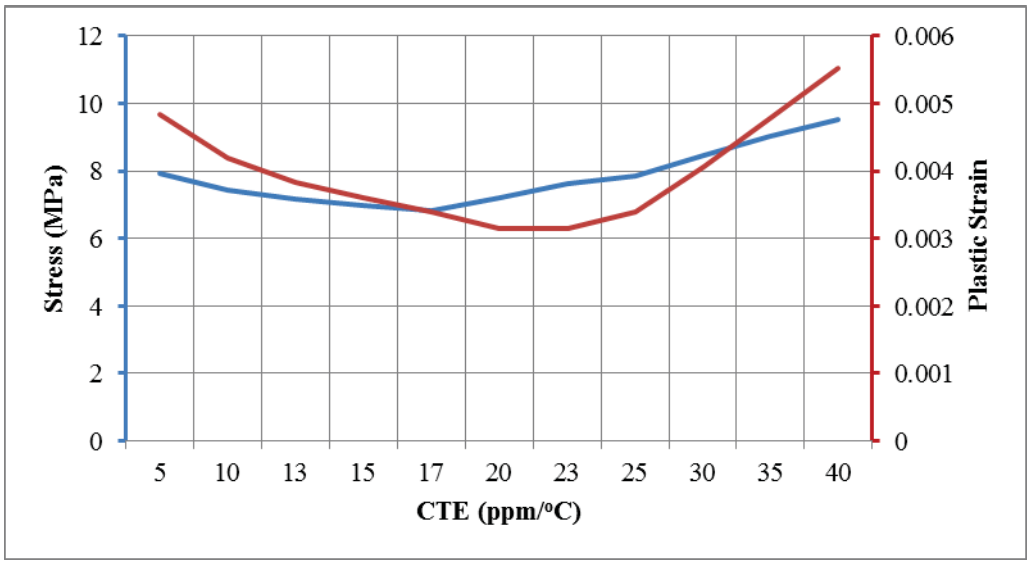


Figure 2-9. Simulated Von-Mises stress and plastic strain versus CTE of molding compound using simulation model in Figure 2-8 and material properties in Table 3-1 and Table 3-2.

The selected molding compound for encapsulation is UF1220 from United Adhesives, for which specifications are listed in Table 2-1.

Table 2-1. Specifications of the molding compound in Figure 2-12 [5]

Manufacture	United Adhesives
Part number	UF1220
Dielectric strength	>500 Volt/mil (19.69 kV/mm)
Glass transition temperature (T_g)	145°C
CTE (ppm)	48 ppm (@>T_g) and 10 ppm (@<T_g)
Viscosity at 25°C	12000 cps
Temperature range	-80°C to 200°C

Figure 2-10 shows the manufacturer-recommended curing profile from the datasheet. The molding compound first heated up to 75°C with low pressure so that it became less viscous and trapped air could be removed. After removing trapped air bubbles, the chamber pressure goes

back to 1 atm, the temperature increases to 125°C and stays for 30 minutes, and the molding compound completely cures during this transition.

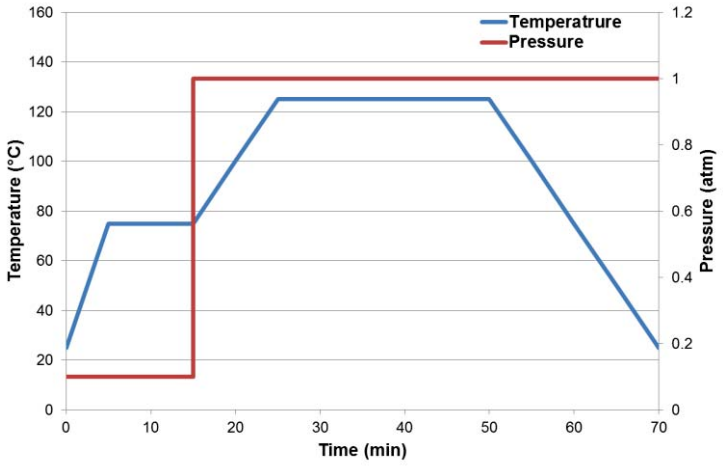


Figure 2-10. Curing profile for UF1220 molding compound in Table 2-1 [5].

Even though the CTE of UF1220 is listed in the datasheet, this was considered a rough number at below and above the glass transition temperature. To have a more accurate CTE over the operating temperature range, a dilatometer (Orton Dilatometer 1600R) in Figure 2-11 was used to measure the actual CTE of the molding compound.

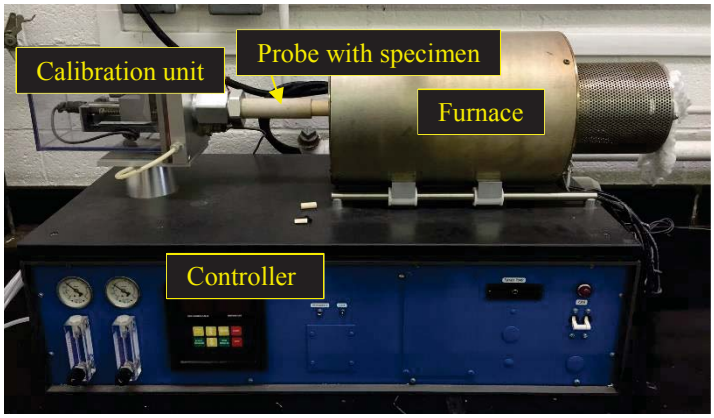


Figure 2-11. Dilatometer from the Edward Orton Jr. Ceramic Foundation for the measurement in Figure 2-13.

The block diagram in Figure 2-12 introduces the measurement process. The molding compound was cured in a cylinder shape, and it was inserted in the measurement bar as shown in

Figure 2-13(a). The measurement probe went into the furnace, and the probe measured how much sample expanded as the temperature swept from 30°C to 200°C. Two samples were fabricated, and each sample was measured twice to make sure there were consistent results. Figure 2-13(b) is one of the measurement results showing the length of change over the range of temperatures. Linear lines are drawn at flat ranges of low and high temperature measurements. The crossing of two lines was measured as the glass-transition temperature (T_g), and the CTEs before and after glass-transition temperature were calculated by taking two measurement points in the flat ranges.

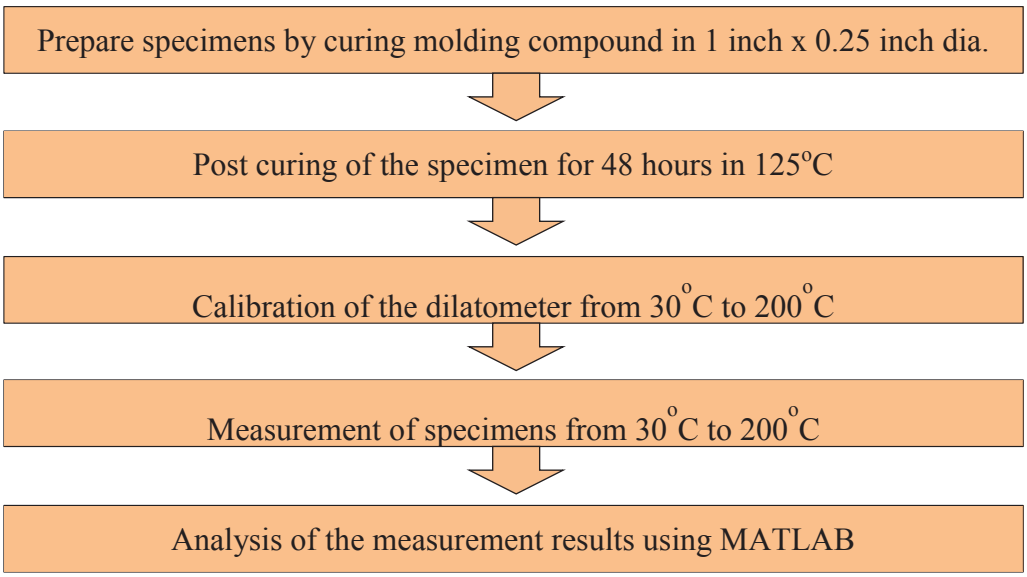
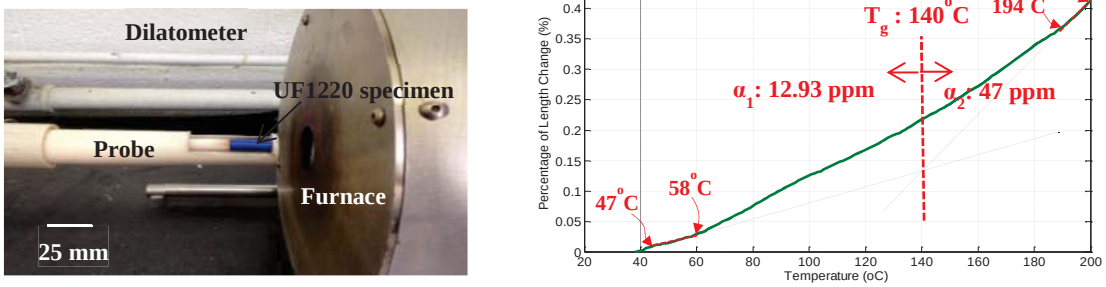


Figure 2-12. CTE measurement process using dilatometer.



(a) (b)

Figure 2-13. Dilatometer for the CTE measurement with the procedures in Figure 2-12 (a) and measured change of length by temperature (b).

The measurement result in Figure 2-13(b) can be analyzed as:

$$\begin{aligned}\alpha_1 &= \left[\left(L_2/100 - L_1/100\right)\cdot 10^6\right]/\left(T_2 - T_1\right)\\ &= \left[\left(0.02497\%/100 - 0.01185\%/100\right)\cdot 10^6\right]/\left(58^oC - 47^oC\right) = 12.93\\ \alpha_2 &= \left[\left(0.4133\%/100 - 0.3851\%/100\right)\cdot 10^6\right]/\left(200^oC - 194^oC\right) = 47.00\end{aligned} \quad (1)$$

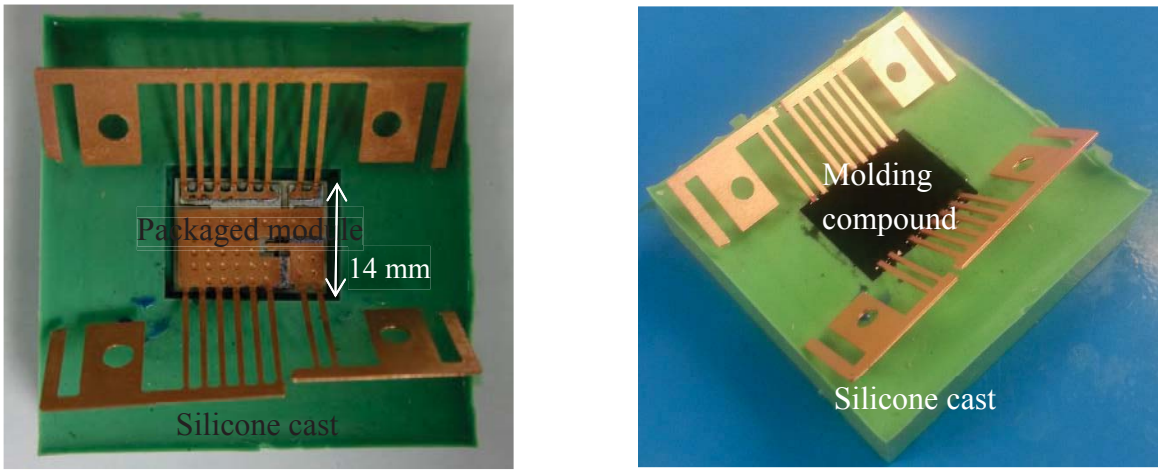
Using the same method, four measurements were analyzed, and all four measurements showed consistent results as shown in Table 2-2.

Table 2-2. Measured CTE of UF1220 molding compound using the dilatometer in Figure 2-11

	Sample 1_1st	**Sample 1_2nd**	**Sample 2_1st**	**Sample 2_2nd**
T_g (^oC)	140	142	140	141
α_1 (ppm)	12.93	13.5	13.54	12.29
α_2 (ppm)	47.00	48.57	51.5	50.91

The assembled module was encapsulated to enhance dielectric strength and protect the packaging components from mechanical stress and humidity. Since the transfer molding equipment was not available in the lab, the molding compound was applied by potting into the

case as shown in Figure 2-14. Detailed encapsulation process is described in Appendix B.3.D. The silicone gel was cured to make a cast, as it was easy to make and detach after the molding compound was cured. The molding compound was heated to 75^{o}C to make it less viscous, then placed in a vacuum chamber in Figure B-9 to get rid of trapped air bubbles.



(a) (b)

Figure 2-14. Encapsulation of the module using the process in Appendix B.3.D; packaged module in a silicon cast (a), and the cast filled with molding compound (b).

Since filling the maximum electric field region (gap between chip and DBC substrate) by molding compound was crucial, the sample in Figure 2-15 was fabricated. The developed sample showed no voids in the encapsulant, and the 0.2 mm height gap between chip and DBC substrate was successfully filled.

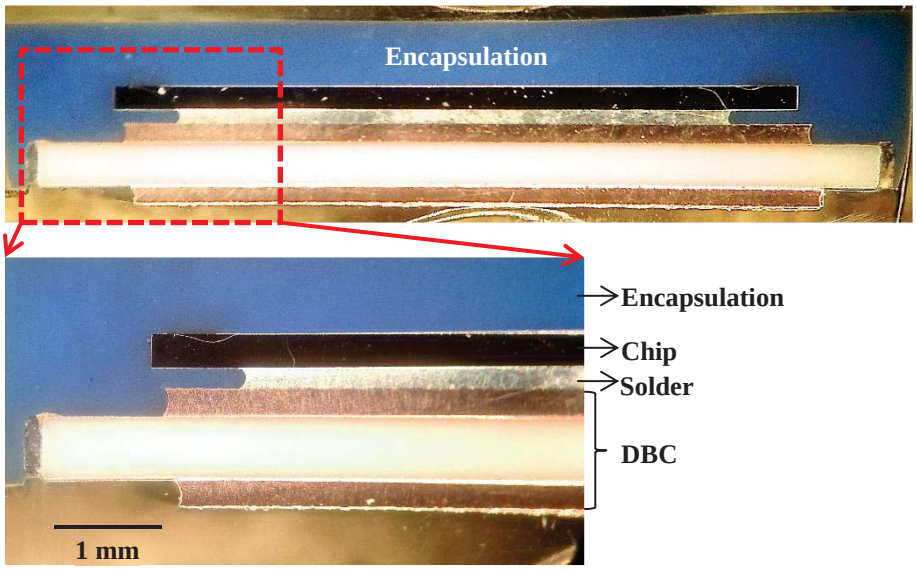


Figure 2-15. Cross-section of the encapsulated sample using UF1220 in Table 2-1.

2.5. Design for Parasitic-Inductance Reduction

The parasitic inductance was analyzed by Q3D simulation with simulation conditions in Appendix B.5. The simulation model in Figure 2-16(a) was used for the parasitic extraction, and ac inductance was simulated with 200 kHz switching frequency. For comparison, a simulation model of a commercial module from IXYS was built (Figure 2-16(b)). The IXYS module was chosen because it has similar voltage and current ratings, and the lead frame for surface mounting is somewhat similar to the developed module.

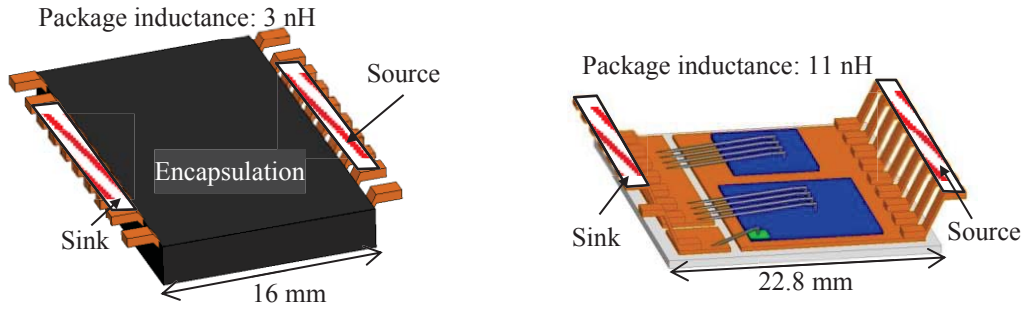


Figure 2-16. Simulation models of Q3D Extractor for the parasitic inductance extractions; encapsulated module in Figure 2-3 (a) and benchmark module from IXYS (MMIX1G82N120A3V1) (b) (see Table B.(8) for simulation files).

Table 2-3. Simulation setup for the parasitic-inductance extraction of models in Figure 2-16

Simulation tool	Q3D Extractor
Frequency	200 kHz
Mesh	Adaptive-mesh control (50 μm mesh length)
Number of sub-steps	10
Source and sink excitation	Indicated with dashed box

Figure 2-17 compares simulated parasitic inductance with other types of packages [6], [7]. The Powerex U-series package is common for high power modules, and the total parasitic inductance is about 50 nH, which is mainly caused by U-shaped terminal and bond wire. The IXYS module, which is similar to the developed module, has about 11 nH inductance, which is 8-nH higher than the developed module (3 nH), with the difference mainly caused by the bond wire. Based on the simulation results, the parasitic inductance of the module is much lower than conventional modules, and it will be even more advantageous for realizing a bidirectional switch. For example, the IXYS module has an IGBT with an anti-parallel diode, and two modules are

required to realize a bidirectional switch. Therefore, the developed module will enable a minimized power loop in the system.

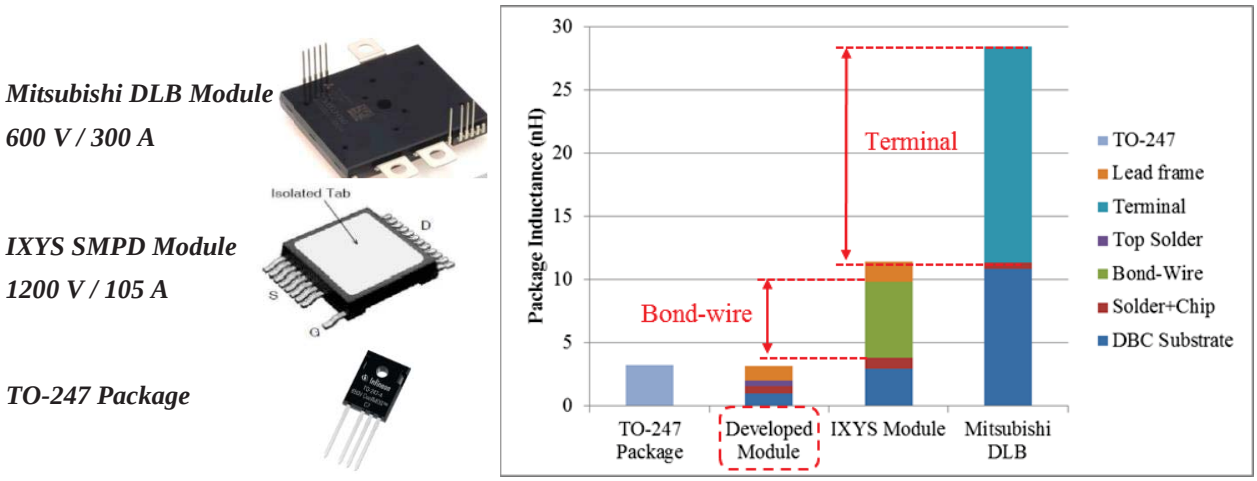


Figure 2-17. Comparison of simulated parasitic inductances of the models in Figure 2-16 and other types of packages [6],[7].

2.6. *Parametric Study of the Indented Lead Frame for Thermo-Mechanical Stress Reduction*

The lead frame in the module was designed to make direct connections from the front side of the chip to the DBC substrate. Because the front side of the chip and the DBC substrate had height differences, the lead frame was fabricated to be able to bond to two points at the same time. As shown in Figure 2-18, the required height to be compensated for was 0.7 mm, and a fabrication process for the lead frame was developed.

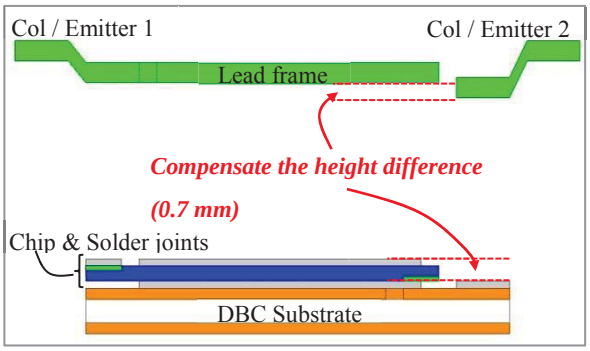


Figure 2-18. Required height compensation by the lead frame (side view of the model in Figure 2-3).

On a copper plane, a laser router masked the outline of the lead frame, and the chemically etched lead frame was placed on the press mold as addressed in Appendix B.1. The press mold was specially designed to be able to compensate for the height difference via a single-step process. Air-hardened steel was used for making the press mold, and there were four alignment pins to keep the lead frame in position during the pressing process (Figure 2-19). After putting on the top-side mold, 50000 psi pressure was applied from the top so that the lead frame could be bent (Figure 2-19(b)). After bending the lead frame, it could simply be removed from the mold, and the height compensation could be achieved as designed.

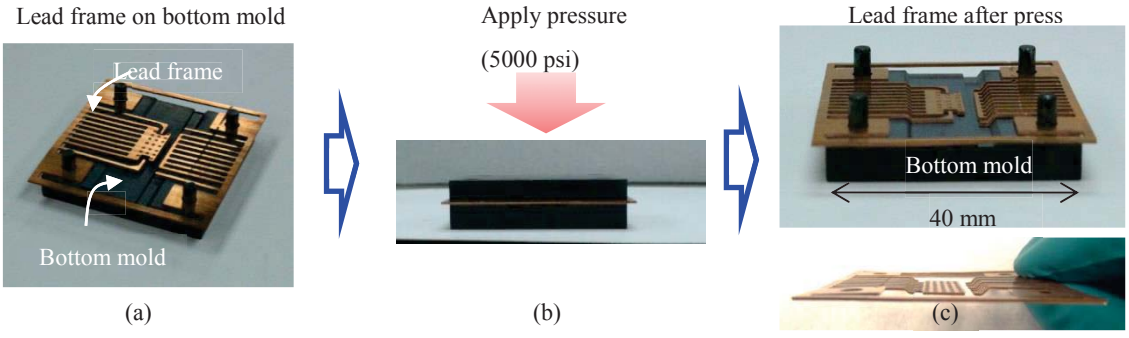
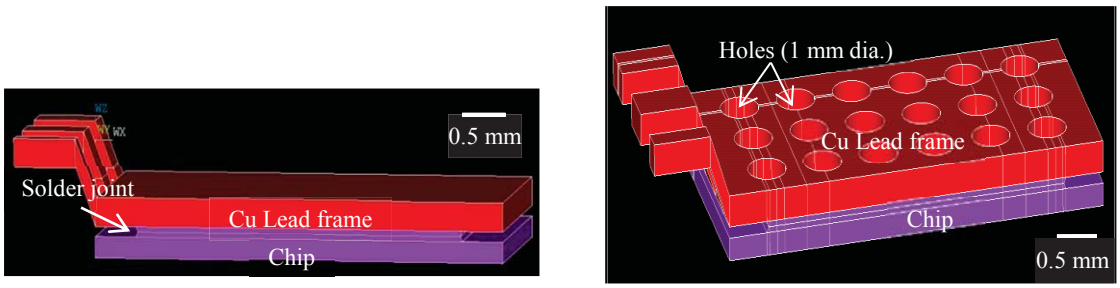


Figure 2-19. Lead frame shape process using the layouts of lead frame and press mold in Appendix B.1 (see Table B. for AutoCAD layout of the press molds).

The CTE mismatch between the solder and the copper lead frame is expected to result in excessive thermo-mechanical stress in the solder joint. Because the lead frame plays an important role in achieving superior thermal and electrical performance, it was preferable to make minimum changes from the original design. For this reason, the indented lead frame was developed by adding an array of indentations on the lead frame. ANSYS simulation models in Figure 2-20 were built to analyze the influence of the newly-developed lead frame. Both models were simulated and plastic strains at the solder joints were analyzed. In the original lead frame case, the maximum plastic strain was found at the edge of the joint, and there was a gradient decrease to the center of the joint. The strain distribution with the indented lead frame showed more evenly distributed plastic strain. The maximum strain was reduced by 58.70% compared to the original lead frame. Therefore, the three-dimensional indented lead frame was used for the module fabrication.



(a) (b)

Figure 2-20. ANSYS simulation models of the lead frame without indentation (a) and with indentation (b) (see Table B.(2) for simulation files).

The effectiveness of the indented lead frame for thermo-mechanical stress reduction at the die-attach layer is shown in Figure 2-20. However, the lost volume of copper at the lead frame

increases the electrical and thermal resistances. To analyze the trade-off among thermo-mechanical stress, electrican resistance, and thermal resistance, five parameters in Figure 2-21 were defined. The total volume of the lead frame without indentation is defined as V_{total}; the lost volume of copper due to the indentation is defined as $V_{indentation}$; and *diameter*, *depth*, and *pitch* of the indentations are defined. Q3D Parasitic Extractor was used for electrical-resistance simulations, and the same simulation model was used for thermal simulation using ePhysics. Appendix B and Appendix D show the details of ePhysics thermal simulation, Q3D parasitic extraction, and ANSYS thermo-mechanical stress simulations. Von-Mises plastic strain at the die-attach layer was simulated by ANSYS Mechanical. The simulated data are shown from Table 2-5 to Table 2-7.

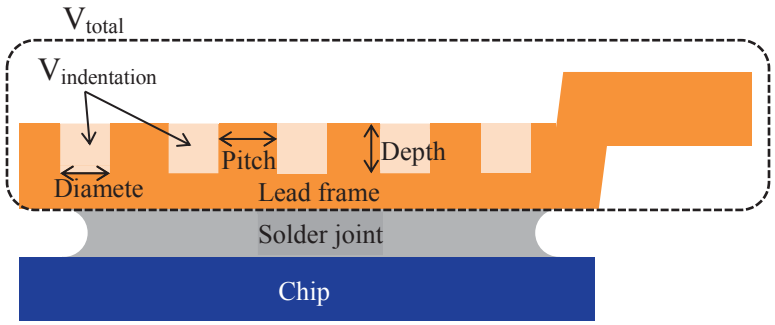


Figure 2-21. Illustration of the defined parameters for parametric study of the indented lead frame in Figure 2-20.

Table 2-4. Simulation results of the depth-controlled indentation (see Table B.(2, 6, and 8) for simulation files)

$V_{indentation}$ / V_{total} (%)	0	3.7423	7.4846	11.2269	14.9692
Diameter (mm)	0	0.750	0.750	0.750	0.750
Pitch (mm)	0	1.5	1.5	1.5	1.5

Depth (mm)	0	0.125	0.250	0.375	0.500
Resistance (μΩ)	23.8131	24.5272	25.4927	26.7955	29.2069
Thermal resistance (^{o}C/W)	3.2543	3.3964	3.5386	3.7110	4.0453
Von-Mises plastic strain	0.01197	0.010132	0.009716	0.009579	0.008979

Table 2-5. Simulation results of the diameter-controlled indentation (see Table B.(2, 6, and 8) for simulation files)

$V_{indentation}$ / V_{total} (%)	5.6701	11.2269	18.6634	23.1082	27.9797	39.1197
Diameter (mm)	0.533	0.750	0.967	1.0760	1.184	1.400
Pitch (mm)	1.5	1.5	1.5	1.5	1.5	1.5
Depth (mm)	0.3750	0.3750	0.3750	0.3750	0.3750	0.3750
Resistance (μΩ)	25.2943	26.7955	29.0366	30.7411	32.4456	38.0327
Thermal resistance (^{o}C/W)	3.5034	3.7110	4.0678	8.3867	4.5700	5.3883
Von-Mises plastic strain	0.010032	0.009579	0.009579	0.009006	0.008682	0.008521

Table 2-6. Simulation results of the pitch-controlled indentation (see Table B.(2, 6, and 8) for simulation files)

$V_{indentation}$ / V_{total} (%)	57.1273	33.7037	22.9459	17.0178	15.0598
Diameter (mm)	0.967	0.967	0.967	0.967	0.967
Pitch (mm)	1.1	1.3	1.5	1.7	1.9
Depth (mm)	0.375	0.375	0.375	0.375	0.375
Resistance (μΩ)	36.9323	31.5514	29.0366	27.1260	27.1260

Thermal resistance (^{o}C/W)	5.0918	4.4176	4.0678	3.8417	3.7900
Von-Mises plastic strain	0.008821	0.009396	0.009579	0.00944	0.009804

The x-axis in Figure 2-22 is calculated as $V_{indentation}/V_{total}$, which means the fraction of the indentation over the original lead frame. The primary y-axis shows the normalized electrical and thermal resistances that have increasing trend as the portion of indentation increases. On the contrary, Von-Mises plastic strain decreases as the indentations are increased. The change of electrical/thermal resistances and Von-Mises plastic strain for different parameter-controlled conditions are summarized in Table 2-7. The summary reveals that the depth controlled method is the most effective way to reduce the thermo-mechanical stress while minimizing the increase of electrical/thermal resistances.

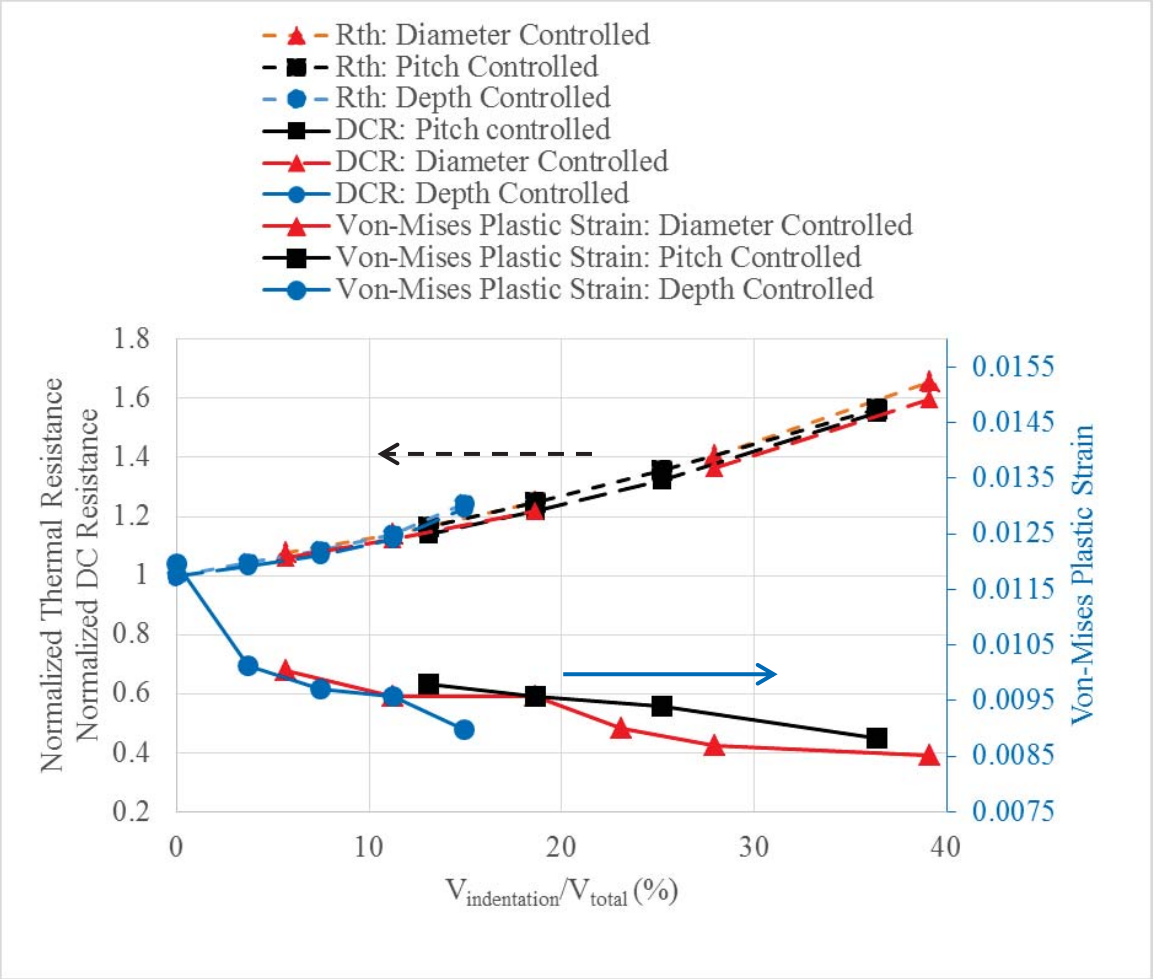


Figure 2-22. Comparison of junction-to-lead thermal resistance, dc resistance, and Von-Mises plastic strain at solder joint based on simulation results from Table 2-4 to Table 2-6.

Table 2-7. Summary of the parametric study in Figure 2-22 using depth, diameter, and pitch of the indented lead frame

	Thermal resistance	**Electrical resistance**	**Von-Mises Plastic strain**
Depth controlled	24% ↑	23% ↑	32% ↓
Diameter controlled	54% ↑	50% ↑	21%↓
Pitch controlled	34% ↑	36% ↑	16% ↓

2.7. Fabricated Bidirectional Module

A DBC substrate was prepared by a chemical etching process, and the surface was coated with silver to prevent oxidation and for better wettability with solder. Dummy bidirectional IGBTs were used for the process development, but had the same pattern as real dice. Both the top and bottom sides had the same layout, and had a gold metallization. $Sn_{63}Pb_{37}$ solder perform was used, and high temperature solder balls were placed at the perforated holes in the preform. The high temperature solder balls had a 0.2 mm diameter, and they were used to control the height of the joint. Figure 2-23 shows prepared packaging materials, and Table 2-8 shows the material properties and dimensions of each layer.

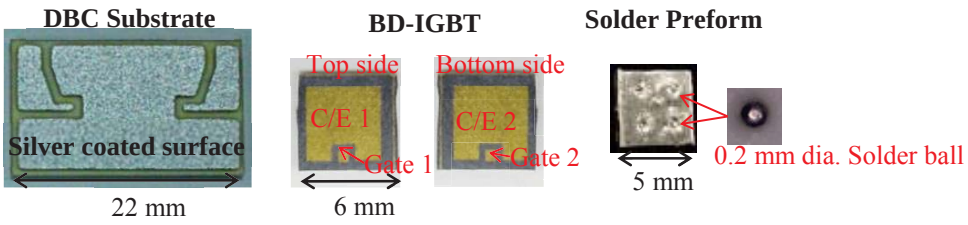


Figure 2-23. Prepared packaging materials using the layout and process in Appendix B.1.

Table 2-8. Dimensions and specifications of the packaging materials in Figure 2-23

Layer	Material	Thickness (mm)
DBC	Copper	0.305
	Al2O3	0.635
Solder	Sn63Pb37	0.2
Chip	Silicon	0.5
Lead frame	Copper	0.5

Using prepared packaging materials, the module was assembled and vacuum reflowed to minimize voids at the solder joint. Since the quality of the die-attach layer was important for heat propagation and dissipation, the module was processed in a vacuum reflow chamber (SSV-MV2200). The forming gas (10% H_2 + 90% N_2) was used as flux, and the temperature and pressure were controlled as illustrated in Figure 2-24.

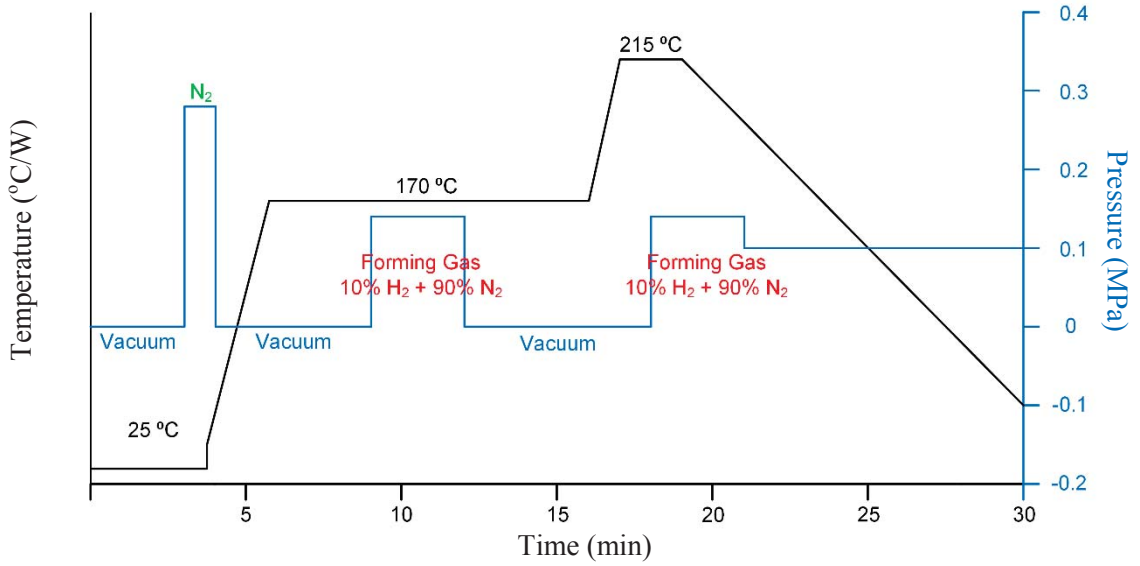
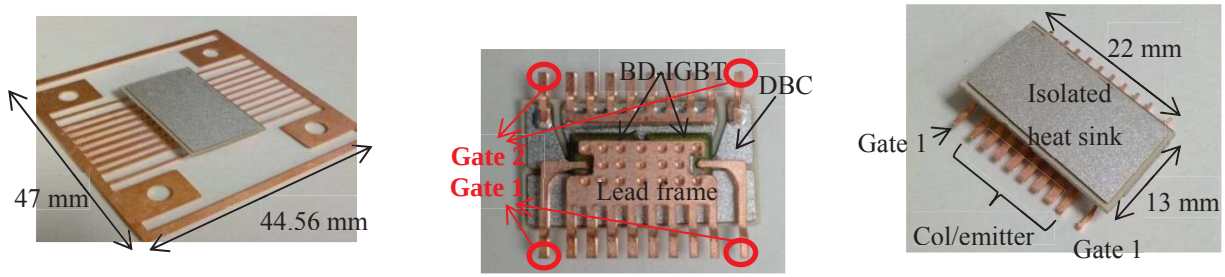


Figure 2-24. Vacuum reflow profile for tin-lead ($Sn_{63}Pb_{37}$) solder preform in Figure 2-23.

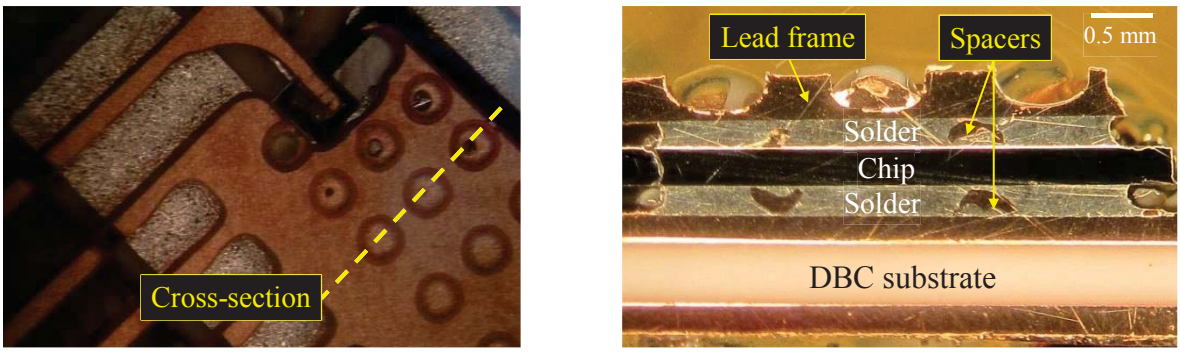
Figure 2-25(a) shows the packaged module after the vacuum reflow process. Figure 2-25(b), (c) shows the top and bottom sides of the module after the lead frame trimming. The gate pads' alignment was the biggest obstacle for the bidirectional chip packaging, and all gate pads showed precise alignment with the lead frame and the DBC substrate. Therefore, the developed packaging process was verified and the bare module was encapsulated to provide mechanical strength and enhance the reliability of the joint.



(a) (b) (c)

Figure 2-25. Module after the vacuum-reflow process using the reflow profile in Figure 2-24 (a), bottom side of the module (b), and top side of the module (c) after lead frame trimming.

The fabricated module has cross-sectioned along the line in Figure 2-26(a), and Figure 2-26(b) shows the cross-sectioned module. The inserted spacer successfully controlled the height of the solder layers, and the five-layer structure was successfully fabricated without tilting, void, or crack.



(a) (b)

Figure 2-26. Cross-section of the packaged module in Figure 2-25.

2.8. References

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Chapter 3. LARGE-CHIP ATTACHMENT BY HOURGLASS JOINT

3.1. Introduction

The die attach layer of a high-power module is the predominant thermal path for heat generated from the power chip. For that reason, the reliability of a die attach layer is important to enhance life time of a power module. A conventional die attach layer has a fillet-shape joint that naturally forms during a solder reflow process. A fillet-shape joint shows the maximum thermo-mechanical stress at the interface between solder and chip where intermetallic compounds (IMC) exist [1]-[6]. Due to a brittleness of an IMC, a crack initiates and propagates along the interface [7]-[9]. To avoid high thermo-mechanical stress at the interface, an hourglass joint was proposed for a ball grid array (BGA) interconnection [14], [16]. An hourglass joint was compared with a barrel shape joint, and it was shown that an hourglass joint delayed crack initiation time and extended crack propagation time [13]-[16].

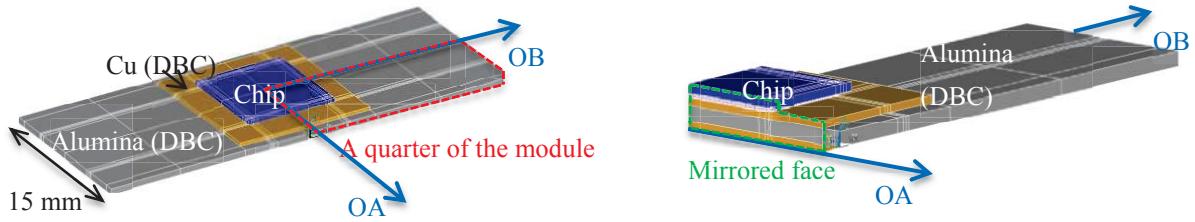
To take advantage of the extended reliability of an hourglass joint to a large-sized (100 mm^2) chip, the packaging process was developed and verified by experiments. In case of BGA joints in hourglass shape, the reliability can be enhanced, but the thermal performance is degraded due to the reduced die-attach area. In case of fillet joints, the thermal performance is superior by having a large die-attach area, but the reliability is less than an hourglass joint. By applying the concept of hourglass-shaped joint to a large-chip attachment, a power module can have the superior thermal-characteristic as well as the enhanced reliability. For the optimum design, a shape of

hourglass joint was studied based on the finite-element analysis (FEA) of thermo-mechanical simulation and static-thermal simulation. Section 3.2 shows the simulation models of hourglass joint and fillet joint that compare Von-mises stress and plastic strain. Since FEA solution has been commonly used for the lifetime prediction, the simulation-based design focused on the reduction of thermo-mechanical stress. The die-attach layer of hourglass joint has smaller area by the nature of the developed process. To see the influence of the area reduction on the thermal characteristics, the static-thermal simulation was performed by ePhysics. Section 3.3 shows the developed packaging process that can shape the designed hourglass joint. The developed process was able to obtain a consistent packaging result by controlling the height of spacer and applied pressure during a reflow process. Using the developed process, samples for power-cycling were fabricated for both hourglass joint and fillet joint that have the same volume of solder joint for fair comparison. Section 3.4 shows the experiment setup and the analysis of the test results. The diode was packaged on a substrate, and the change of forward-voltage drop over power-cycling was used as the failure criteria. To have a fair comparison with power-cycling results of other literature, packaged samples have been cycled by JEDEC standard power-cycling profile. Since the forward voltage drop of a diode is a temperature-sensitive parameter, the control circuit for the power-cycling was designed based on this parameter. The control circuit samples forward-voltage of diode, and a window comparator determines the cycling temperature range based on the sampled forward-voltage. Power-cycling was continued until the dramatic change of forward-voltage was observed. Analysis of the experiment result will be added later.

3.2. Methodology for Shape Optimization

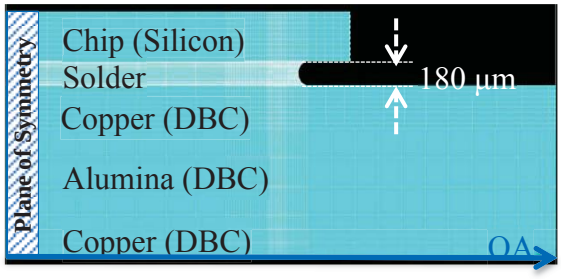
3.2.1. Analysis of Thermo-Mechanical Stress

The mismatch of coefficient of thermal expansion (CTE) among materials induces high thermo-mechanical stress, and the accumulated stress results in a failure of the joint. Thermo-mechanical stress has been analyzed by either numerical calculation or simulation of ANSYS 13 [1], [15]. Since plastic strain is known as the dominant parameter that influences on the lifetime of joint [25], the maximum plastic strain of different types of solder joints was compared. By virtue of the symmetric structure, a quarter of the entire structure in red-dashed box in Figure 3-1 was simulated with zero-displacement-boundary condition. Figure 3-2 shows meshed models that have refined mesh at the edges. Since the maximum stress was expected at the corner of joint, the volume of mesh at this location had 8.13E-16 m^3, and inner-side mesh had 6.32E-13 m^3 volume. 8-Node VISCO107 element was used for solder and SOLID185 for other materials. Detailed ANSYS simulation setup and codes are introduced in Appendix D

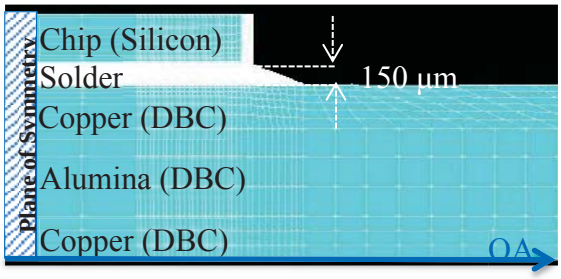


(a) (b)

Figure 3-1. Model of the cycling sample in Figure 3-13 (a), and actual simulation model in red-dashed box. (b) A quarter of the module with mirrored face (see Table B.(9) for simulation files).



(a)



(b)

Figure 3-2. Meshed simulation models at mirrored face in Figure 3-1; (a) Hourglass joint. (b) Fillet joint.

Table 3-1. Material properties and dimensions of model for ANSYS simulation in Figure 3-2

Material	**Dimension**	**CTE (ppm/°C)**	**Elastic modulus (Pa)**	**Poisson's ratio**
Copper (DBC)	15 mm x 15 mm x 0.305 mm	1.64E-5 (-40°C) 1.70E-5 (105°C)	1.23E11	0.34
Al_2O_3 (DBC)	46 mm x 17 mm x 0.625 mm	8.1E-6	3E11	0.21
Solder	8.66 mm x 8.66 mm x 0.2 mm (Hourglass Joint) 10.5 mm x 10.5 mm x 0.15 mm (Fillet Joint)	1.87E-5 (-40°C) 2.28E-5 (105°C)	5.64E10 (-40°C) 4.57E10 (105°C)	0.336 (-40°C) 0.363 (105°C)
Silicon	10 mm x 10 mm x 0.35 mm	2.25E-6 (-40°C) 2.82E-6 (105°C)	1.64E11 (-40°C) 1.62E11 (105°C)	0.22 (-40°C) 0.23 (105°C)

Molding Compound	Over-molded	10E-6 (-40°C) 48E-6 (200°C)	8.8E9	0.49

Anand model has been widely used to analyze non-linear behavior of solder, and VISCO107 is the ANSYS-provided element that can import Anand model. Parameters of Anand model are listed in Table 3-2 [19].Anand model employs the functional form to define the flow equation as:

$$\dot{\varepsilon}_p = Ae^{-\frac{Q}{RT}} \cdot \left[\sinh\left(\xi \frac{\sigma}{s} \right) \right]^{1/m} \tag{2}$$

where

$$s^* = \hat{s} \left[\frac{\dot{\varepsilon}_p}{A} e^{(Q/RT)} \right]^n \tag{3}$$

Table 3-2. Parameters of lead-free solder for thermo-mechanical stress simulations from Figure 3-5 to Figure 3-7 (input code to ANSYS is shown in Appendix D) [1]

Parameters	Definition	Value
A (s^{-1})	Pre-exponential factor	717.260
Q (J/mol)	Activation energy	50446
R ($JK^{-1}mol^{-1}$)	Universal gas constant	8.3145
S_0 (MPa)	Initial value of deformation resistance	2.45
T (K)	Temperature	-
a	Strain rate sensitivity of hardening/softening	2.22
h_0 (MPa)	Hardening/softening constant	14560
m	Strain rate sensitivity	0.130
n	Strain rate sensitivity of the saturation value of deformation resistance	0.0436
s (MPa)	Deformation resistance	-
$\hat{s}$ (MPa)	Coefficient for deformation resistance saturation value	29.0
ε_p	Plastic strain	-
ξ	Multiplier of stress	2

Prior to thermo-mechanical stress comparison between the hourglass joint and the fillet joint, the shape of the hourglass joint was optimized by ANSYS simulations. The parameters of the

hourglass joints are defined as shown in Figure 3-3, and plastic strain is observed at the interface between joint and substrate, joint and chip, and the center of the curved surface which are defined as point 1 to 3. The solder joint in Figure 3-2(b) was replaced with the hourglass joints in Figure 3-4 that have different geometry factors.

Figure 3-3. Illustration of the hourglass joint with defined geometry factor (GF=h/a).

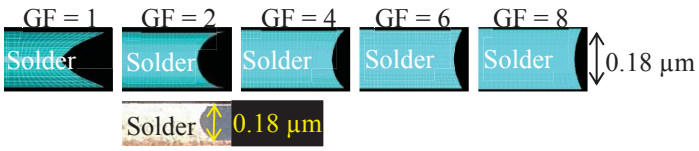


Figure 3-4. Edge of hourglass joints (red-dashed box in Figure 3-3) with different geometry factors (GF) for ANSYS simulations in Figure 3-5 (GF=h/a).

Simulation results are plotted in Figure 3-5, and plastic strain at each point is observed. Because the purpose of the hourglass joint is the migration of the maximum stress from the interface (point 3) to the center of the curved surface (point 2), the geometry factor above 5 can be excluded from the design range. When the geometry factor is 2, the point 1 and 3 have the minimum plastic strain, and the point 2 has moderate plastic strain. Another dependent parameter to geometry factor is the thermal resistance. The shape of the edge termination influences the heat propagation from junction to case of the substrate, and simulation results show that the thermal resistances have up to 23% difference by the geometry factor as shown in Figure 3-5. Compared to the geometry factor 1, when geometry factor is 2 the thermal resistance shows 10%

and Von-Mises plastic strain shows 45% reductions while increasing Von-Mises plastic strain at other points less than 1%. Therefore, the optimum design point was determined as geometry factor of 2, and all simulation models and hardware were fabricated with this criterion.

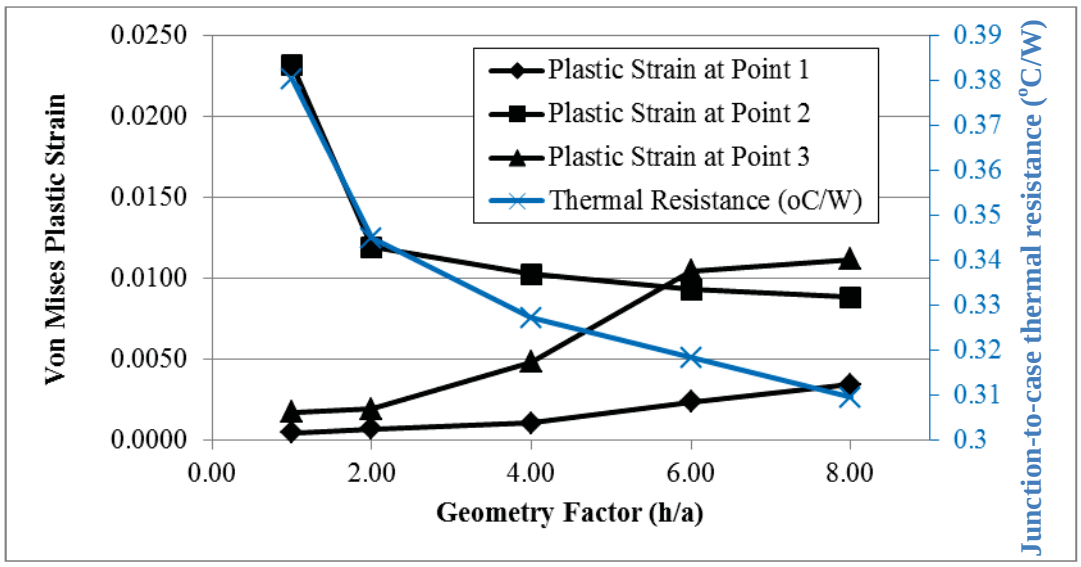
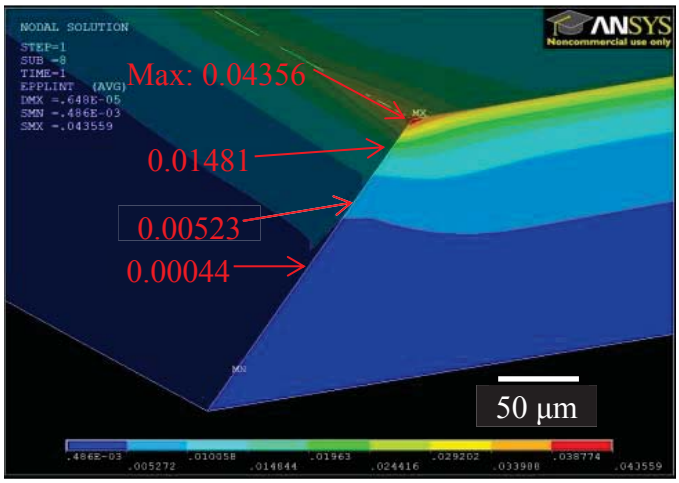
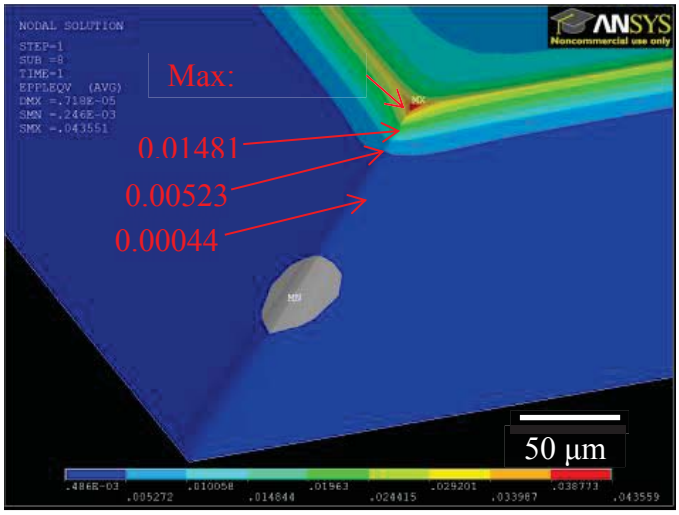


Figure 3-5. Simulated plastic strain and junction-to-case thermal resistance versus geometry factor using different GFs in Figure 3-4 (refer to Appendix D for thermo-mechanical analysis and Appendix B.5 for thermal simulation).

The model was simulated using 25°C as reference temperature, and 105°C as load temperature to have comparable results with previous studies [1]-[3]. For fair comparison between hourglass and fillet joint, the volumes of two joints were preferred to be the same (15-mm^3), but the sample-fabrication process of fillet joint showed that more consistently shaped joint could be obtained with 10% larger volume (16.54 mm^3). ANSYS simulations were used to see the influence of the volume difference, and the maximum plastic strains of two joints were found at below of interface between chip and solder with 0.02% difference (Figure 3-6). Therefore, both models were expected to have similar cycling results, and the actual cycling samples of fillet joint were fabricated with 10% larger volume.



(a)

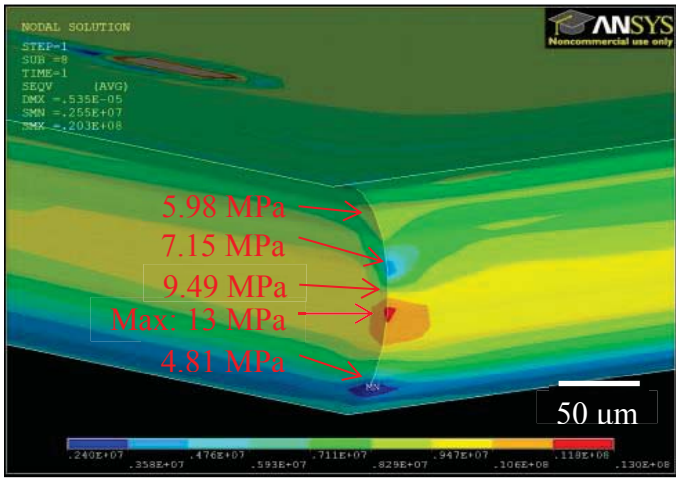


(b)

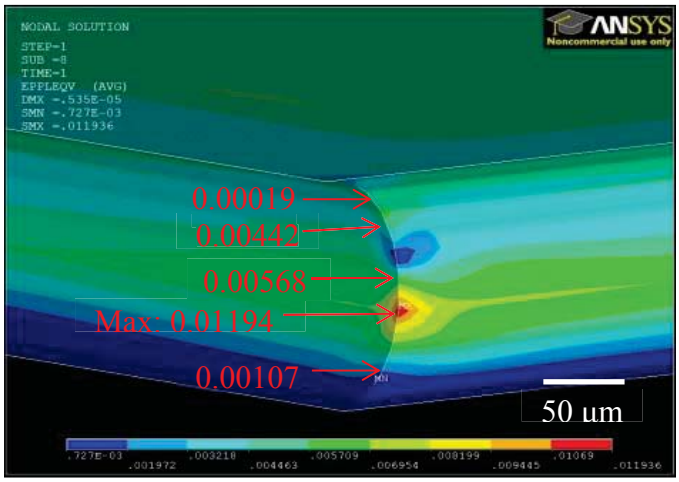
Figure 3-6. Strain distribution of 15 mm^3 fillet joint (a), and 16.54 mm3 fillet joint (b) in Figure 3-2(b).

Figure 3-7 shows normalized Von-Mises stress and strain of hourglass joints. Unlike a fillet joint in Figure 3-6, the maximum strain was found at the center of corner with 27.42% reduction. Compared with the interface between solder and chip, the middle of solder joint is less vurnerable to thermo-mechanical stress, and this result explains how previous literature could get the extended lifetime with hourglass-shaped BGA joints [10]-[13]. The same effect was expected

with large-joint with hourglass shape, and the packaging process for large-chip attachment (10-mm^2) was developed.



(a)



(b)

Figure 3-7. Von-Mises stress (a) and Von-Mises plastic strain (b) of hourglass joint in Figure 3-2(a).

Prior to the fabrication of samples for power-cycling, lifetimes of two types of joints were analyzed by energy-based prediction model. Unlike strain-based prediction models, such as Coffin-Manson model, energy-based models consider the energy density from the stress-strain

hysteresis loop. Energy-based models couple the crack-initiation time and propagation-time with energy density, and results in more accurate prediction than strain-based models. Gustafsson fatigue model in (4) is one of the popular model that originated from Darveaux energy-based prediction model [19]-[22]:

$$N_{\alpha w} = N_{0s} + \frac{a - (N_{0s} - N_{0p})\left(\frac{da_p}{dN}\right)}{\frac{da_s}{dN} + \frac{da_p}{dN}} \tag{4}$$

where $N_{\alpha w}$ is the number of cycles to failure; a is total possible crack length; N_{0p} and N_{0s} are the primary and secondary energy-based-crack-initiation terms; and da_s / dN and da_p / dN are the crack-propagation terms. The influence of the energy density to the crack initiation and propagation terms are:

$$N_{0p} = N_{0s} = \frac{54.2}{\Delta W_{avg}} \tag{5}$$

$$\frac{da}{dN} = \left(3.49 \times 10^{-7}\right)\left(\Delta W_{avg}{}^{1.13}\right) \tag{6}$$

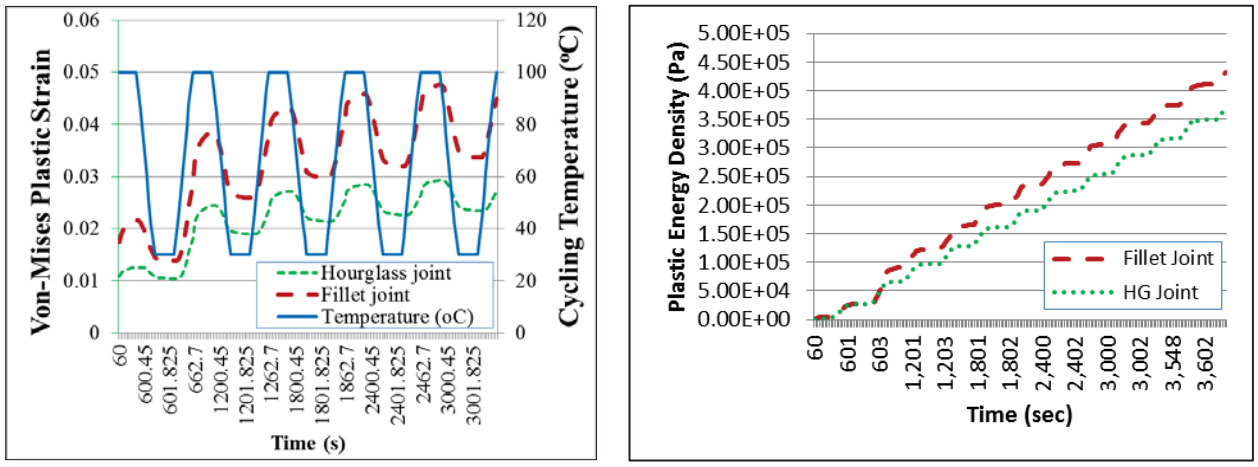
where ΔW_{avg} is the energy-density term that calculated from the stress-strain hysteresis loop and can be derived by ANSYS. This model cannot be directly used for the lifetime prediction of samples for power-cycling in this study because the constants in this model were found by correlation of specimen-degradataion and simulation result. However, this model implies the significance of the strain-energy to the lifetime prediction, and the comparison of strain-energy between fillet joint and hourglass joint will give good approximation of reliability difference.

To calculate the strain energy, two models were analyzed with transient-load conditions using codes in Appendix D and B. The temperature profile for simulation was determined based on the JEDEC power-cycling standard (JESD22-A122). The solid-curve in Figure 3-8(a) represents the monitored temperature at the solder joint that has range between 30^{o}C and 100^{o}C with 10 minutes per cycle. The accumulated-strain energy reached steady-state after three cycles, and the strain energy at the interface of hourglass joint showed negligible accumulation of plastic-strain compared with the middle of hourglass joint. This result means that the most of plastic strain have accumulated at the bulk-solder region, whereas a fillet joint has accumulated-strain energy at the interface with chip. The dash-curve in Figure 3-8(a) represents accumulated-strain energy at below of the interface in fillet joint, and the dot-curve represents accumulated-strain energy at the center of hourglass joint. The volume-averaging technique in (8) was used to calculate the strain-energy density. This method was proposed in Darveaux model to effectively calculate the strain-energy density [19]:

$$\Delta W_{avg} = \frac{\sum \Delta W \cdot V}{\sum V} \tag{7}$$

where ΔW_{avg} is the average plastic strain energy density accumulated per cycle for the critical elements; ΔW is the plastic strain energy density accumulated per cycle of each element; and V is the volume of each element. To have a fair comparison of strain-energy density, the element-volumes of two models were kept the same as 8.13E-16 m^3, and two layers of elements at critical area were used to calculate average-strain-energy density. After reaching the

steady-state, the change of strain-energy density of hourglass joint was 33% lower than fillet joint (Table 3-3). The simulation result implies the extended lifetime of hourglass joint in three reasons. The first is a negligible strain-energy accumulation at below of interface between chip and solder, the second reason is the migration of the maximum strain-energy to the center of the chip, and the third reason is the reduced strain-energy density compared with a fillet joint.



(a) (b)

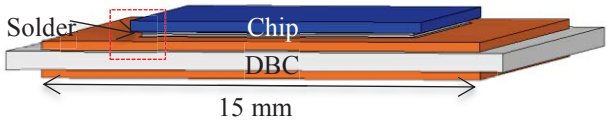
Figure 3-8. Accumulated strain energies (a) and plastic-strain-energy densities (b) of hourglass and fillet joints in Figure 3-2.

Table 3-3. Change of plastic strain and strain-energy density of fillet and hourglass joints from simulation results from Figure 3-6 to Figure 3-8

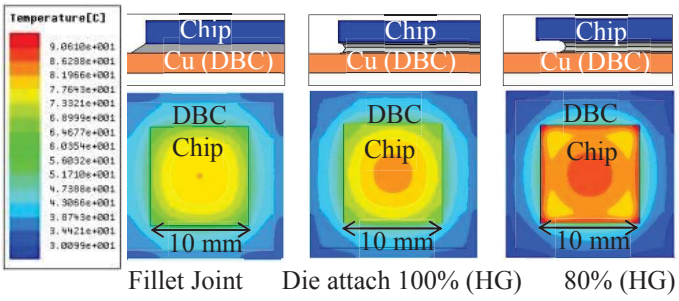
	Fillet Joint	**Hourglass Joint**
$\Delta\varepsilon_p$	0.18E-2	0.082E-2
ΔW	39995	26667

3.2.2. Analysis of Thermal Characteristics

A solder joint in a power module is not only a bonding layer, but also a major thermal path to dissipate heat generated in chips. By the nature of the packaging process of hourglass joint, however, the die-attach area is smaller than the solderable area of the die. Because of this reason, an hourglass joint is expected to degrade the thermal performance of the module. To analyze the influence of the reduced die-attach area on the thermal characteristics, the simulation model with DBC substrate, chip, and solder layer (Figure 3-9(a)) with different areas was simulated. The power dissipation (200 W) was applied to the chip, and forced-convection-boundary condition ($20000\ (W/m^2)/^oC$) was applied to the bottom copper on DBC. The temperature distribution was analyzed with the die-attach area from 60% to 100%, and the calculated thermal resistance was plotted in Figure 3-9. In case of fillet joint, generated heat in the chip was naturally dissipated to the substrate, through the solder joint. However, the reduced die-attach area and the hourglass-shaped joint hindered the heat dissipation, and resulted in residual-heat along the edge of the die. This problem was worsened as the die-attach area was reduced below 80% of the entire area, but the thermal resistance did not changed significantly after this point. Therefore, the developed packaging process had 80% die-attach area to have acceptable tradeoff between successful packaging and thermal performance.



(a)



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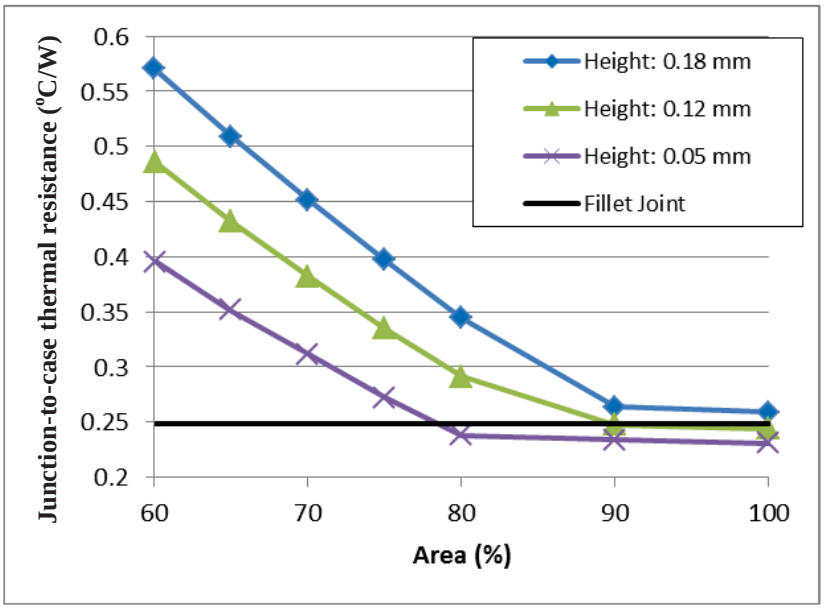


(c)

Figure 3-9. ePhysics simulation model (a); temperature distribution of fillet joint and hourglass joints (b); and the plot of junction-to-case thermal resistance versus die-attachment area and height of hourglass joint (c).

3.3. Developed Packaging Process

3.3.1. Verification of the Developed Process

The developed process was focused to achieve cosistent packaging result with hourglass joint. To be able to control the shape of joint, various parameters of copper spacer, solder mask, and pressure were tested, and the optimum parameters were found. Figure 3-10 illustrates how these paramers control the joint to be hourglass shape. The copper spacer was placed in the cavity of perporated solder preform. The thickness of solder preform was 200 μm and the height of copper spacer was 180 μm so that the height of the solder could be reduced by applied weight during a reflow process. The spread-out solder will stop at the boundary of solder mask that was attached at the edge of chip. The pressure to the solder joint was controlled by the applied weight. The optimum weight was found as 0.8 g that spreads-out the melted solder to the edge of solder mask and prevents die-tilting. The dimension of the solder mask, that helps hourglass joint formation, could be calculated by the volume of solder joint. Based on the initial dimensions, the volume of solder preform can be calculated as:

$$8.66\ mm \times 8.66\ mm \times 0.2\ mm = 15\ mm^3 \tag{8}$$

Since the volume of joint will be the same before and after reflow, the length of gap between solder perform and mask can be calculated as:

$$x^2 \times 0.18\ \text{mm} - 2\pi\left(0.18\ \text{mm}/2\right)^2 x = 15\ mm^3 \tag{9}$$

Therefore, the inner width of the solder mask can be calculated as x = 9.27 mm, and the gap can be calculated as 9.77 mm – 8.66 mm = 1.11 mm.

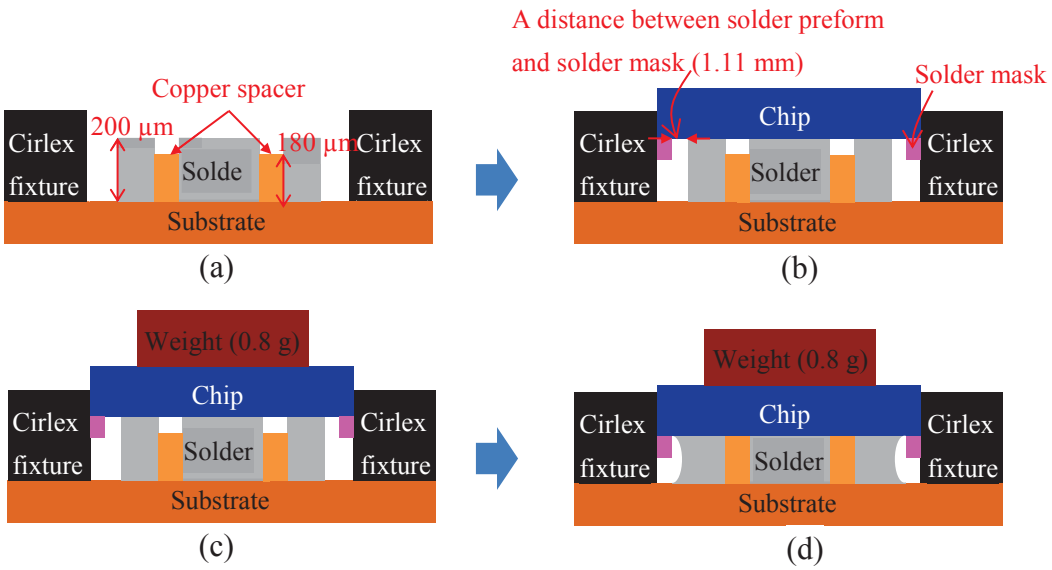


Figure 3-10. Developed packaging process for hourglass joint in Figure 3-2 (not to scale). Place solder preform, spacers, and Cirlex fixtures on the substrate (a); place chip with solder mask with the dimension in (9)(b); apply 0.8-g weight on the chip (c); and reflow using a vacuum chamber in Figure B-8 (d).

Figure 2-15 shows the cross-section of the preliminary sample with hourglass joint in which a silicon chip is attached to a DBC substrate using the developed method. The packaging result showed that the solder joint had no noticeable voids, no die-tilting, and hourglass shape at the edges.

After the verification of the method, the samples for power-cycling were fabricated. Diode was used for the test samples for their ease for electrical characterization. 5SLY 12J1200 by ABB was chosen that had the dimensions of 10×10×0.35 mm^3. The backside metallization was Ag finished, and the alloy of the solder preforms was SN100C.

The fabrication process of fillet joint samples is shown in Figure 3-11. As mentioned earlier, the volume of fillet joint (16.54 mm^3) was larger than hourglass joint in order to facilitate the

formation of the fillet joint. A silicon chip was packaged in this method, and showed consistent packaging results (Figure 3-12).

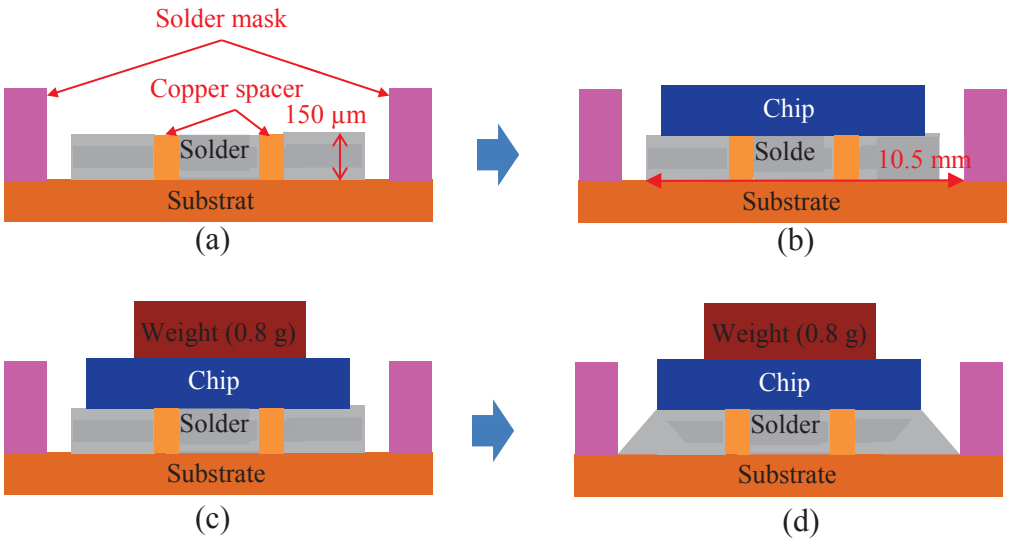


Figure 3-11. Developed packaging process for hourglass joint in Figure 3-2 (not to scale). Place solder preform, spacers, and solder mask on the substrate (a); place chip with (b); apply 0.8 g weight on the chip (c); and reflow using a vacuum chamber in Figure B-8 (d).

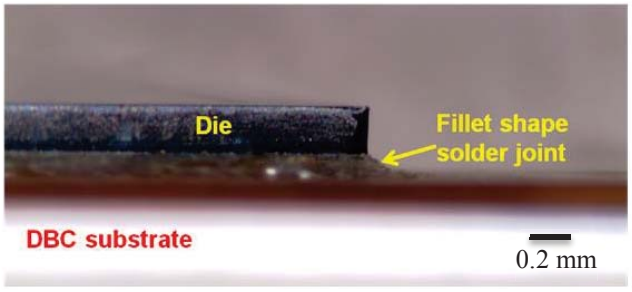


Figure 3-12. Packaged sample with fillet joint using the process in Figure 3-11.

3.3.2. Sample Fabrication for the Power-Cycling

The bottom side of diode with silver finish was attached to the silver-plated DBC so that similar wettability could help the symmetrical formation of hourglass joint. The substrate was patterned to have 15 mm ×15 mm area for the attachment of diode, and two BNC connectors

were used for each sample for the four-point measurement. This connection is expected to be advantageous to keep the consistent measurement as power-cycing continues. The top side of the die was wire-bonded, and the bottom side was attached with hourglass and fillet joints. Five samples were fabricated for each type of joint (Figure 3-13), and X-ray pictures were taken to observe the baseline-condition of solder joint. Both types of joint showed no significance voids in Figure 3-14, and power-cycling was initiated with these samples.

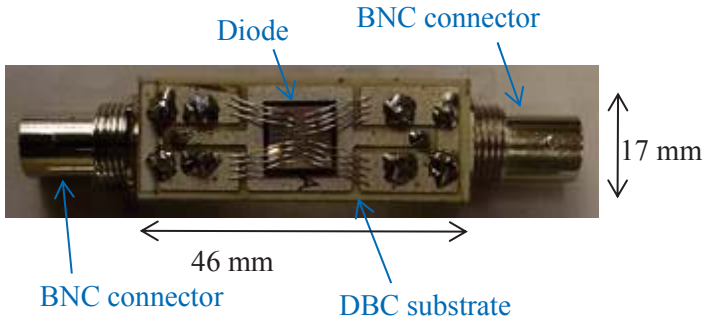
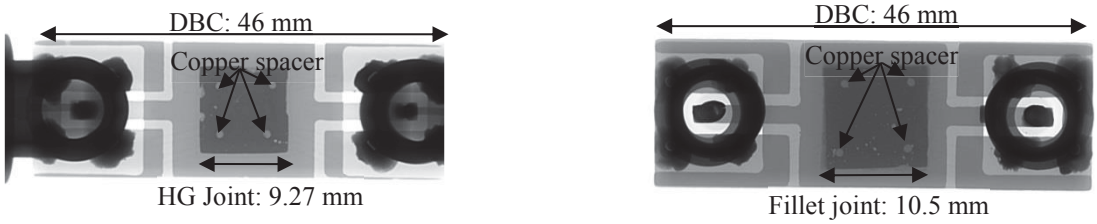


Figure 3-13. Fabricated module using processes in Figure 3-10 and Figure 3-11 for power cycling in Figure 3-16.



(a) (b)

Figure 3-14. X-ray image of fabricated samples of HG joint (a) and fillet joint (b) with the package in Figure 3-13.

3.4. Experiment Results

3.4.1. Power-Cycling Setup (see Appendix C for more information)

To test the reliability of the module, the power-cycling system in Figure 3-16 was configured that controls the junction temperature within predetermined range. Two resistors R_{s1} and R_{s2} were used to control the current flow in IGBT and diode. The resistor Rs_2 was connected in series with MOSFET, and Rs_2 was 5000 times smaller than Rs_1 so that when the switch is on, the high current can increase the junction temperature of the diode and IGBT. Since forward voltage is a temperature-sensitive parameter, the forward-voltage drop of reference sample was sampled by sample and hold IC. According to the K-factor measurement of diode in Figure 3-19 with process in 5.3.2, the forward-voltage change by temperature was found as 2.18 mV/^{o}C. The sampled forward-voltage was used as an input to the window comparator that determines the cycling-temperature range. Detailed operating principle is explained in Appendix C. The cycling profile was determined based on the JEDEC standard JESD22-A122.

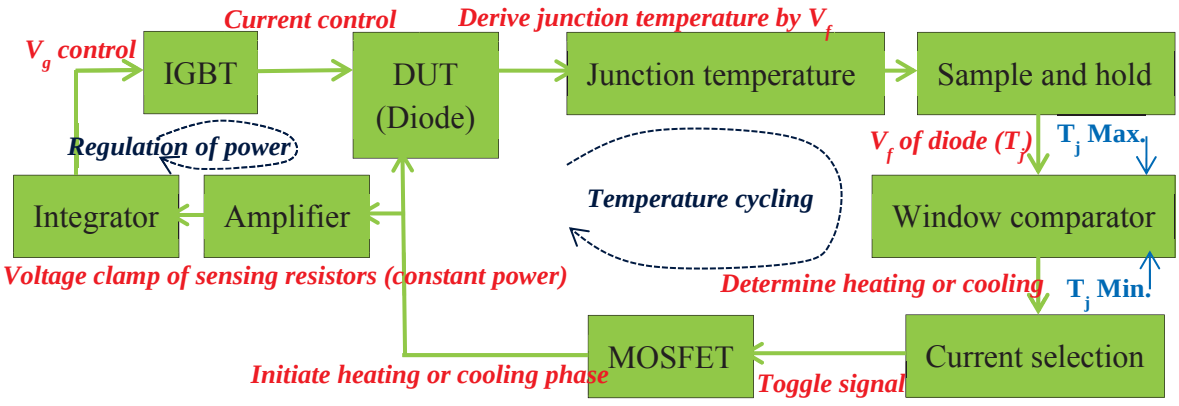


Figure 3-15. Block diagram of the power-cycling system in Figure 3-16.

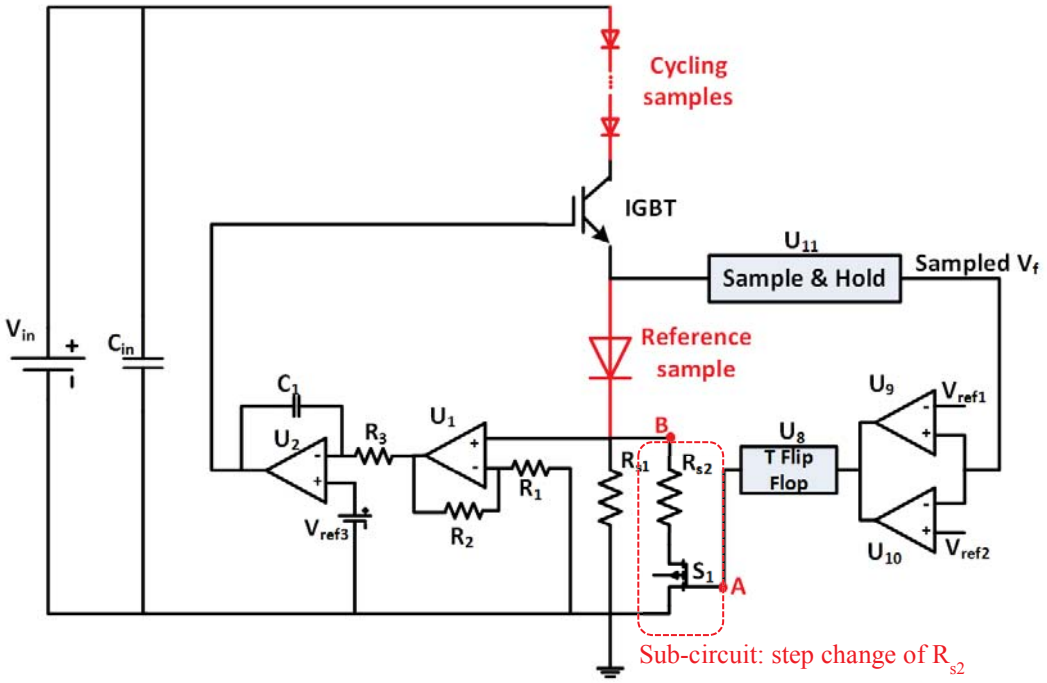


Figure 3-16. Simplified schematic of the power-cycling system for the samples in Figure 3-14 (see Appendix C for the complete layout).

Table 3-4. Bill-of-material of the power-cycling system in Figure 3-16 (complete BOM is in Table B.(3))

Component	Part number	Description
C1	399-1221-1-ND	CAP CER 1000PF 50V 10% X7R 1206
C13,C14	445-4020-1-ND	CAP CER 0.47UF 25V 10% X7R 1206
Cin	490-1775-1-ND	CAP CER 0.1UF 50V 10% X7R 1206
R1,Rs1	P10ECT-ND	RES 10 OHM 1/4W 5% 1206 SMD
R15,R16	311-4.99FRCT-ND	RES 4.99 OHM 1/4W 1% 1206 SMD
R2	P1.0KECT-ND	RES 1K OHM 1/4W 5% 1206 SMD
R3	RHM10.0KFCT-ND	RES 10K OHM 1/4W 1% 1206 SMD

R5	696-1369-1-ND	RES 0.001 OHM 1W 1% 1206
R6	RHM.009AMCT-ND	RES 0.009 OHM 3/4W 5% 1206 SMD
R7	P50NPCT-ND	RES 0.05 OHM 1/3W 5% 1206 SMD
S1 (Q1,Q2,Q3)	IPB009N03L GCT-ND	MOSFET N-CH 30V 180A TO263-7
U1,U2	LT1806CS6#TRMPBFCT-ND	IC OPAMP R-R IN/OUT SGL SOT23-6
U11	SMP04EPZ-ND	IC AMP SAMPLE HOLD CMOS 16DIP
U7	296-1189-1-ND	IC HEX INVERTER 14-SOIC
U8	296-2050-5-ND	IC NOR R/S LATCH 3ST QUAD 16-DIP
U9,U10	LTC1540CS8#PBF-ND	IC COMP NANOPOWER W/REF 8-SOIC

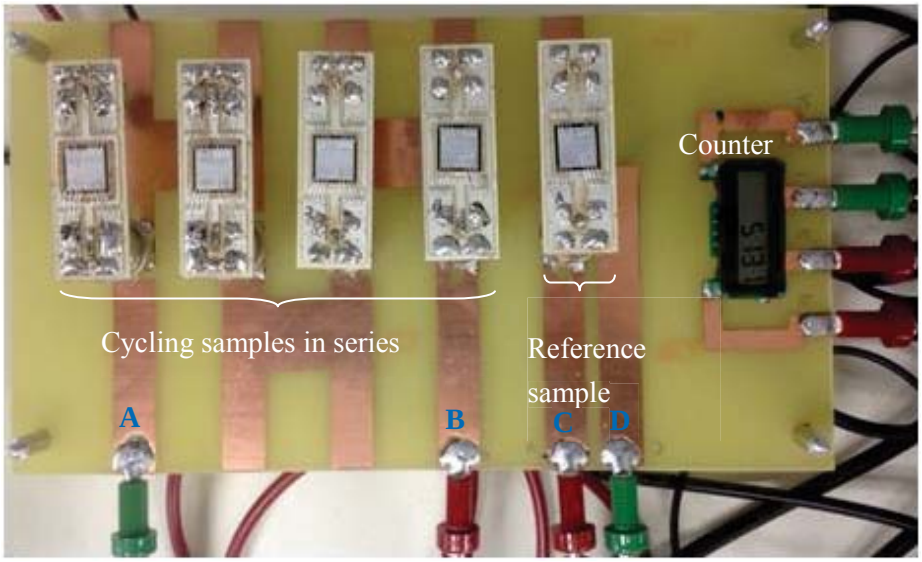


Figure 3-17. Five cycling samples in the red-dashed box of Figure 3-16 (see Appendix C for hardware setup).

Figure 3-18 shows the calibrated temperature profile and measured forward-voltage during cycling. The calibrated temperature range was from 30°C to 100°C and one cycle took 10

minutes. The sampled forward-voltage of diode was measured to make sure the junction temperature of diode was cycling as designed. The dashed line represents the measured temperature by thermocouple, and the solid line represents the measured forward-voltage. It can be seen that the junction temperature of diode is being controlled based on the sampled forward voltage. As joint degrades over cycling, the cycling time for one period can be changed, but the temperature range will remain the same.

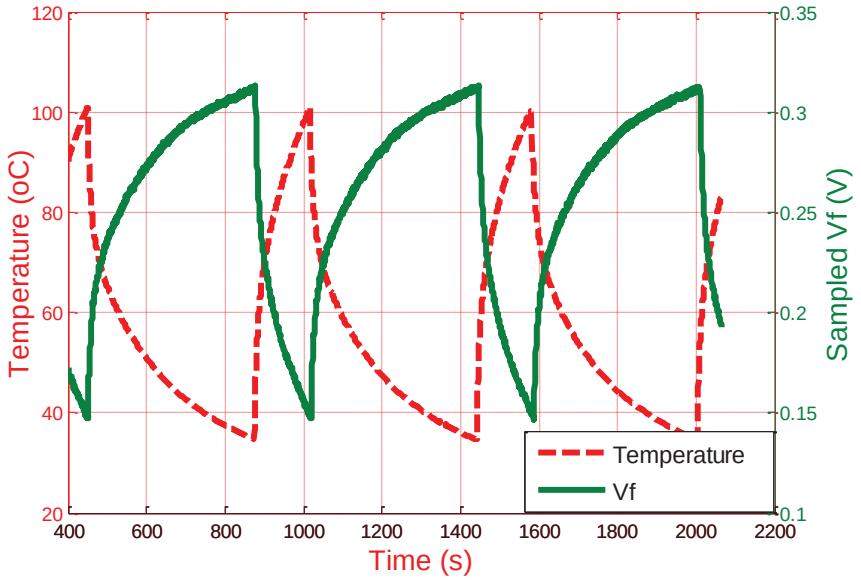


Figure 3-18. Temperature profile and sampled forward voltage using the developed circuit in Figure 3-16.

3.4.2. Method for the Failure Detection

Degradation of the joint can be tested by X-ray scan, scanning acoustic microscopy (SAM), or measurement of thermal impedance. In this paper, the steady-state thermal method is used that applies heating-current to the sample, and measures change of forward-voltage. A forward

voltage of diode is influenced by a junction temperature which is defined as K-factor and measured as 2.13 mV/^{o}C (Figure 3-19). As power cycling continues, a crack in the joint propagates, and reduces the effective-die-attach area. As a result, the heating current congests in a narrower area, and results in higher temperature with a defective joint.

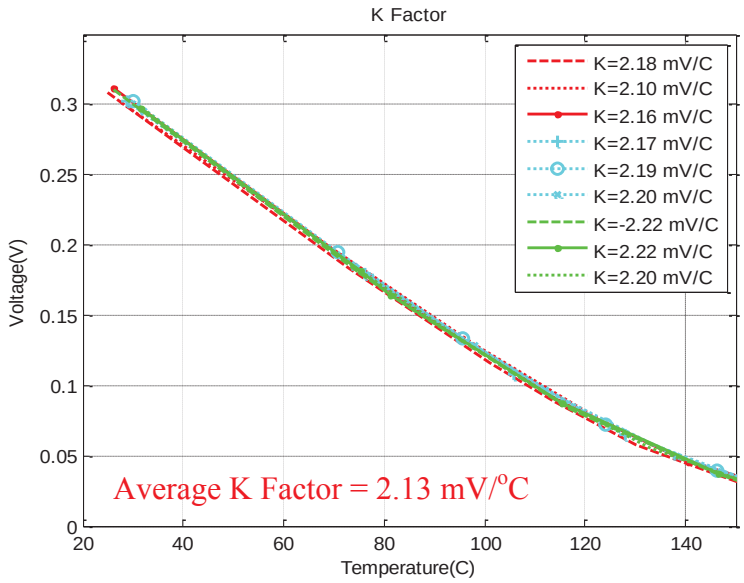


Figure 3-19. Measured K-factor of the diode in Figure 3-13 with specifications in Table 4-4.

To verify the concept, the heating current (10 Adc) was applied for an hour, and forward voltage was measured by oscilloscope (Figure 3-20). After reaching to the steady state, measured forward voltage was dropped by 0.28 V, and temperature increased from 30^{o}C to 132^{o}C (Figure 3-21). To ensure the consistent measurement, each sample was measured three times, and the maximum measurement error was found as 0.65%. To monitor degadation, forward voltage was measured in every 1000 cycles.

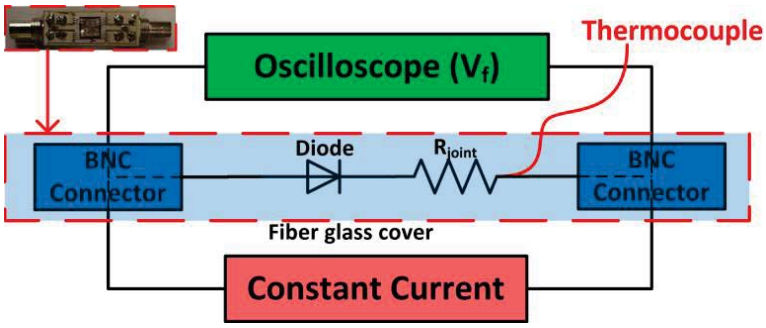


Figure 3-20. Schematic of the measurement setup for the cycling sample in Figure 3-13 using equipment in Table 3-5.

Table 3-5. List of equipment for the measurement in Figure 3-20 and Figure 3-21

	Oscilloscope	**Constant current**	**Thermocouple**	**BNC connector**
Part number	MDO3012	UP6-132	T-type	BNC female
Function	Measure V_f	Apply heating current	Measure temperature	Kelvin connection

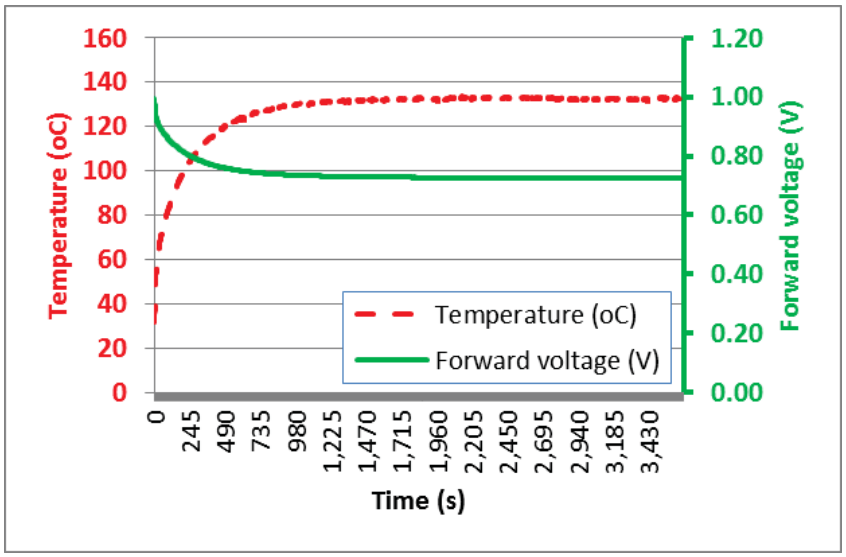


Figure 3-21. Measured junction temperature and forward voltage of cycling sample in Figure 3-17.

3.4.3. Analysis of Power-Cycling Results

Five samples for each type of joint are being cycled, and Figure 3-22 shows power-cycling progress. In case of the fillet samples, the failure mechanism entered the catastrophic failure from 14000 cycles, and the forward voltage of diode was increased to 14% after 16000 cycles. The power cycling for fillet joint will be continued until it reaches 20% change from the initial point. In case of the hourglass samples, the forward voltage decreased for initial 1500 cycles, and then entered the crack propagation phase. As of paper submission date, hourglass samples have finished 5500 cycles, and it will be continued until it reaches 20% of initial measurement. Even though two types of samples do not have same number of cycles so far, the hourglass samples show lower change of forward voltage. Overall, thermo-mechanical stress analysis by ANSYS and cycling status imply superior reliability of hourglass joint than fillet joint.

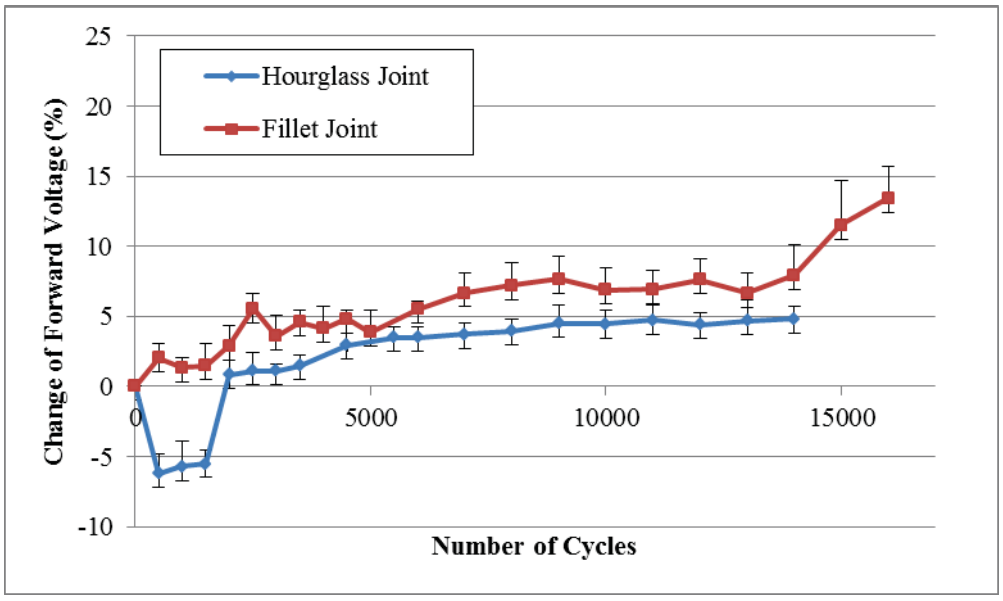


Figure 3-22. Measured forward-voltage changes of the samples in Figure 3-13.

3.5. Summary

In this study, the hourglass joint for a large chip attachment was developed, and thermo-mechanical stress and thermal characteristic of the hourglass joint were parametrically studied. ANSYS simulation showed that the conventional fillet joint had the maximum stress at the interface between chip and solder. However, the hourglass joint showed the maximum stress at the center of curved-surface, and the maximum plastic strain was 0.045 times of the maximum strain in the fillet joint. In case of plastic strain at the interface, where IMC exists, the plastic strain of the hourglass joint was 0.13 of the fillet joint.

Strain-energy-based fatigue prediction models are well-known for its accurate prediction than strain based models. For this reason, the change of average plastic strain energy density (ΔW_{avg}) was simulated by ANSYS. The transient load that was the same with the actual power-cycling profile was used, and ΔW_{avg} was calculated after ΔW_{avg} reached the stead state. After reaching the steady-state, ΔW_{avg} of the hourglass joint was 0.67 of the fillet joint that implies the extended reliability.

One of the drawbacks of the hourglass joint is the reduced die-attach area than the fillet joint. The necessity of the solder mask at the edges of chip limits the size of the joint. Larger solder mask makes the process easier, but reduces the die-attach area. For this reason, the junction-to-case thermal resistance was simulated by changing the die attach area from 60% to 100% of the chip size. The simulation results showed that the thermal resistance was increased

by 9% than the fillet joint with 90% area and 0.18 mm height that is a fair trade-off for the 0.67 times less thermo-mechanical stress reduction.

A packaging process was developed to control the height and shape of the joint, and the optimum parameters for shaping the hourglass joint were empirically found. Samples for power cycling were fabricated, and the conditions of the joints were verified by taking X-ray pictures. Fabricated samples are cycled with JEDEC standard profile that has temperature range from 30^{o}C to 125^{o}C.

The optimized structure and developed packaging process will provide a guideline for replacing a conventional die-attach layer. The developed hourglass joint will be useful for developing a planar module that has higher thermo-mechanical stress than wire-bonded module due to its symmetrical joints.

3.6. References

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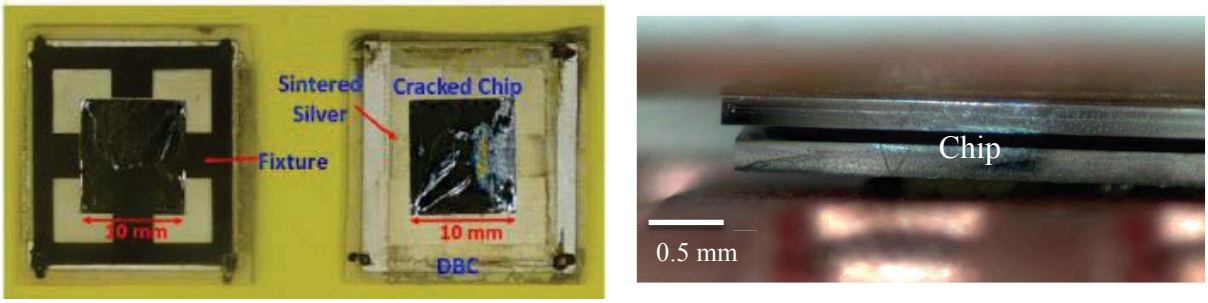
Chapter 4. COMPRESSIVE-POST PACKAGING OF FUSION-BONDED DIE

4.1. Introduction

Chip-stack and double-sided packaging processes often encounter chip warping or cracking during solder reflow owing to mismatches among coefficients of thermal expansion (CTE) as shown in Figure 4-1 [1], [2]. Die damage becomes more severe as semiconductor roadmaps call for thinner dice.

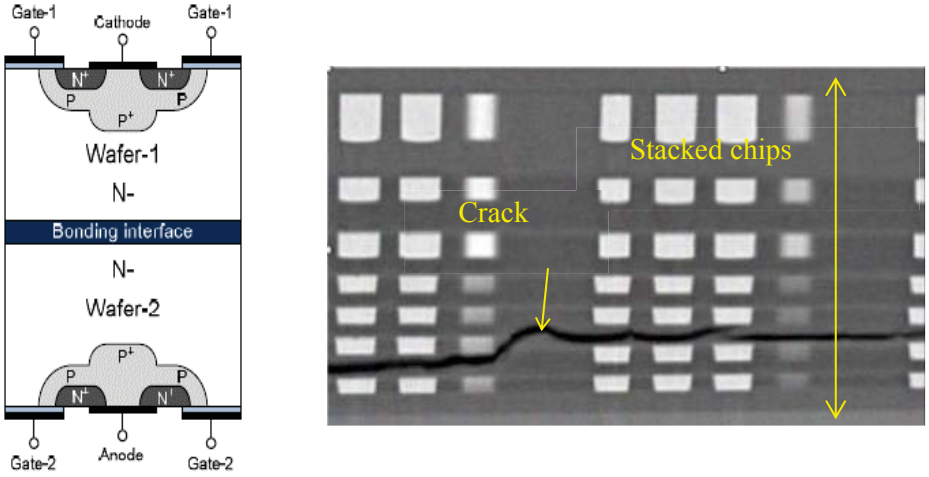


(a) (b)

Figure 4-1. Cracked unidirectional chip during packaging [3](a) and delaminated bidirectional chip during the packaging of the module in Figure 2-25 (b).

A packaging method using compressive posts is discussed herein as a means to reduce thermo-mechanical stress on the die. The packaging of bidirectional IGBT (BD-IGBT) (Figure 4-2(a) [7]) with planar joints is used for process development and verification. Unlike conventional BD-module with two IGBTs and two diodes, the BD-IGBT chip can conduct and block currents in both forward and reverse directions [4]-[11]. The BD-IGBT can be fabricated by either a double-sided process or hydrophobic wafer bonding process (Figure 4-2); previous studies showed that the latter had more symmetrical I-V characteristics in both directions [6]-[8].

The ultimate strength of the bonding interface is only 0.7 MPa, rendering this stress-sensitive chip a suitable candidate to test the effectiveness of the compressive-post idea.



(a) (b)

Figure 4-2. Bidirectional switch developed with a double-sided process (a) and stacked chips with crack due to thermo-mechanical stress during a packaging process [2], [7] (b).

In general, thermo-mechanical stress due to CTE mismatch is avoided in electronic packaging. However, the developed compressive posts take advantage of the CTE mismatch to counterbalance asymmetric expansion in the package. The compressive posts are formed around the die using solder balls that have higher CTE than silicon. During the cooling phase of the reflow process, the posts shrink more than the chip, compressing the chip and alleviating the tensile stress.

4.2. Thermo-Mechanical Stress in a Multi-Layer Structure

4.2.1. Layout of the Module

To reduce electrical and thermal impedances, an indented lead frame was developed to connect the chip's terminals to the package pins as shown in Figure 4-3. The measured package inductance was 70% of wire-bonded inductance. The simulated maximum Von-Mises plastic strain at the die-attach layer was reduced to 54% of the strain in a solid copper lead frame. Thus, thermo-mechanical stress was mitigated without compromising the electrical and thermal advantages of the double-sided package.

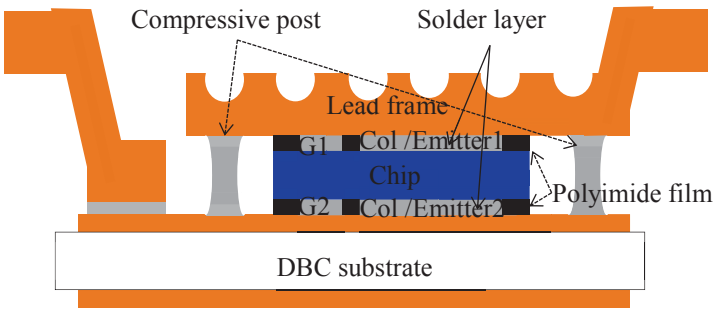


Figure 4-3. Lay-up of the developed module in Figure 2-3 with compressive posts (not to scale).

4.2.2. Peel Stress of the Double-Sided Package

A solder layer between two materials experiences high thermo-mechanical stress due to differences in CTE [9], [12]. The interfacial shear and peel stresses were modeled in [13], [14] for the geometry illustrated in Figure 4-4. The line AA represents the center of the model.

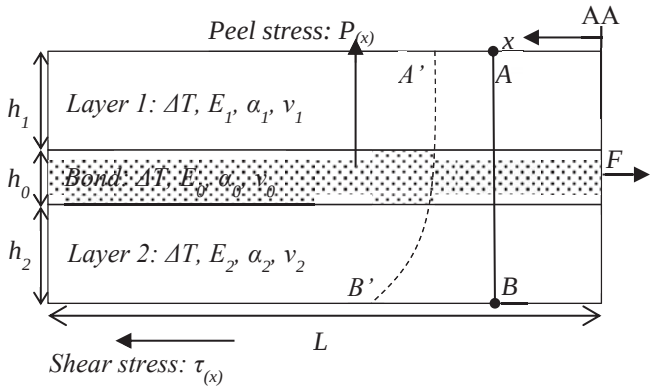


Figure 4-4. 2D presentation of shear stress and displacement [13].

The peel stress in Figure 4-4 was derived from considerations of moment of equilibrium of the applied forces combined with shear stress:

$$P(x) = \frac{(h_1 D_2 - h_2 D_1)}{2D} \frac{(\alpha_1 \Delta T - \alpha_2 \Delta T)}{K \cosh(\kappa L)} \cosh(\kappa x) \tag{10}$$

where α_i is coefficient of thermal expansion of ith material; ΔT is the change of temperature; L is length of the layer; and D_i is the flexural rigidity;

$$\kappa = \sqrt{\lambda \cdot K^{-1}} \tag{11}$$

where λ is axial compliance; K is stress compliance; and D is the flexural rigidity given by

$$K = K_0 + \sum_{i=1}^{2} K_i = h_i / G_i + \sum_{i=1}^{2} h_i / 3G_i \tag{12}$$

$$\lambda = \sum_{i=0}^{3} \left(1 - \nu_i^2\right) / E_i h_i \tag{13}$$

$$D = \sum_{i=0}^{2} E_i h_i^3 / 12\left(1 - \nu_i^2\right) \tag{14}$$

where h is the height of the layer; G is shear modulus; E is elastic modulus; and ν is Poisson's ratio.

Material properties in Table 4-1 were used in (10) - (14) to estimate the peel stress. Since the bonding interface has much weaker strength than the adhesion strength of the solder layer, the

five-layer structure was divided into two parts along the bonding interface: the top side with lead frame, solder, and top half of the chip; the bottom side with bottom half of the chip, solder, and DBC substrate. Figure 4-4 shows the calculated peel stress at top and bottom joints resulting from 150^{o}C change. The peel stress increases from the center to the edge of the module. The top side experiences 2.48 times the peel stress of the bottom side. The peel stresses are induced in opposite directions, implying higher stress to the chip than single-side die attachment. Even though the peel stresses were calculated with simplified five-layer structure, the result showed the possibility of the die cracking with the double-sided package. In addition, the calculated peel stresses with different heights (h_0) in Figure 4-6 shows that the thinner joint results in the higher peel stress. Therefore, it is advisory to avoid using thin (< 0.2mm) die-attach layer for the double-sided module.

Table 4-1. Material properties for the peel stress calculations in Figure 4-5 and Figure 4-6

Material	**E (GPa)**	**G (GPa)**	**Poisson's Ratio**
Copper	32	40.95	0.343
Silicon	112.4	43.91	0.28
Al_2O_3	303	125.21	0.21
Solder ($Sn_{63}Pb_{37}$)	110	11.59	0.38

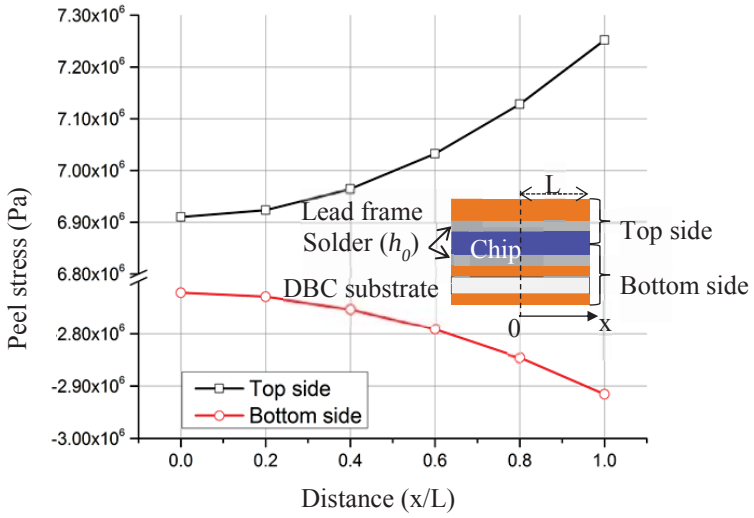


Figure 4-5. Calculated peel stresses of the top and bottom joints (h_0 = 0.2 mm) using the model in Figure 4-4 and material properties in Table 4-1.

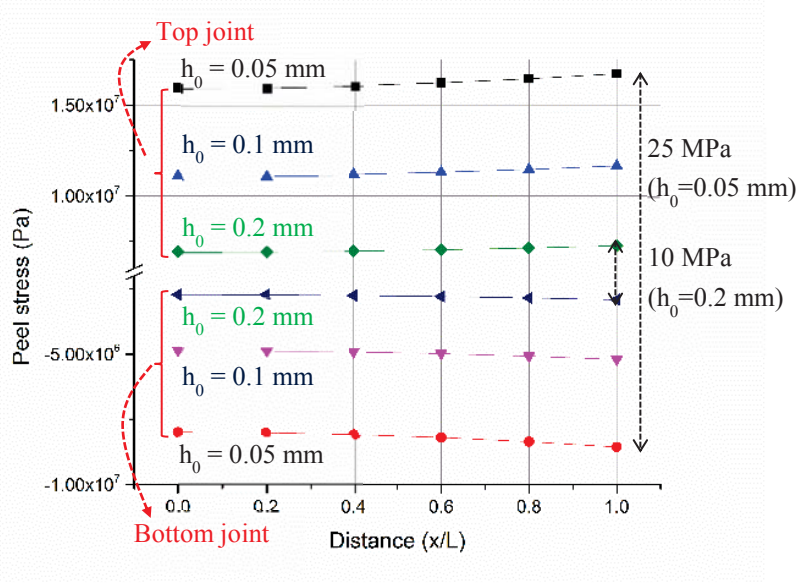


Figure 4-6. Calculated peel stresses with different heights of solder layers (h_0) in Figure 4-5.

4.3. Compressive Post

4.3.1. Material Deformation in Double-Sided Package

Due to the asymmetrical deformation of packaging materials, an electronic package experiences residual stress. Figure 4-7(a) illustrates the deformation of the double-sided module with a DBC substrate at the bottom and a copper lead frame on the top. As temperature of the chamber cools down from the stress-free temperature, the DBC substrate and copper lead frame shrinks at a higher rate than silicon chip. Both DBC substrate and lead frame bend away from the chip, inducing tensile stress on the die and solder joints. As analyzed in Figure 4-5, the tensile stress detaches the bonded chips if it is higher than the bond strength. Compress posts were integrated into the package as shown in Figure 4-7(b) to counteract the tensile stress.

High-temperature solder balls ($Pb_{93.5}Sn_5Ag_{1.5}$) were placed around the chip, and solder preforms ($Sn_{63}Pb_{37}$) were used as joining material. Representative packaging materials are listed in Table 4-1. As temperature of reflow chamber increases, both copper lead frame and DBC substrate starts expanding as indicated by dashed lines. Because the solder ball has higher melting temperature ($T_m = 301^oC$) than solder preform ($T_m = 183^oC$), it keeps the shape at the reflow temperature and forms a post. As the chamber temperature cools down below the liquidus temperature, solidified solder posts shrink more than silicon chip due to its higher CTE. The compressive posts pull down the lead frame and provide residual compressive force to the chip.

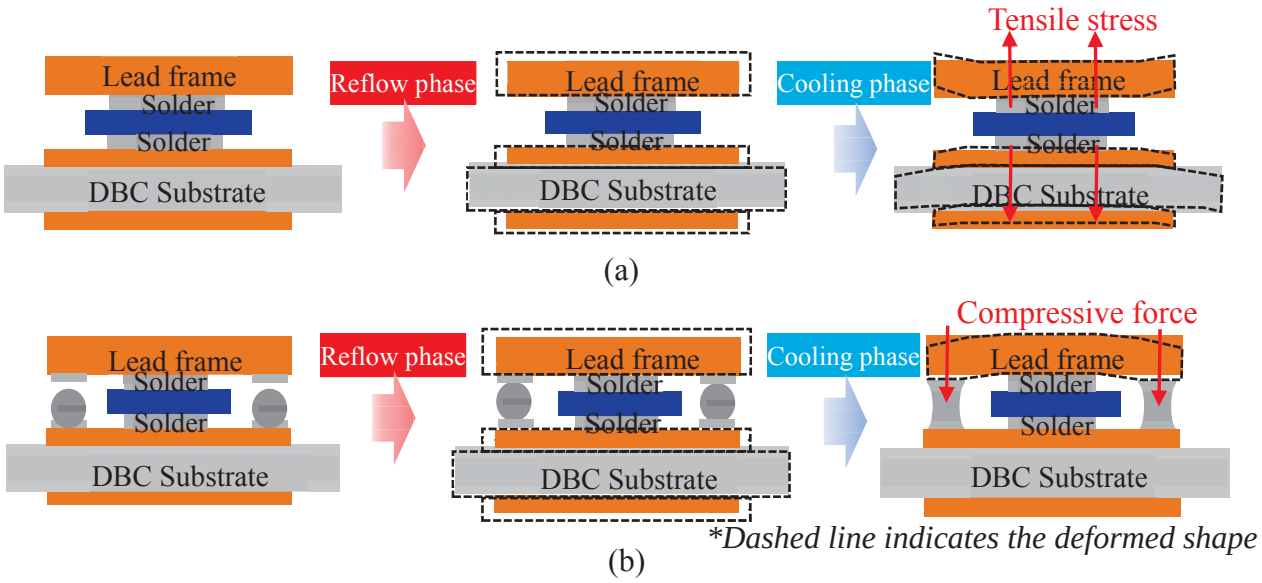


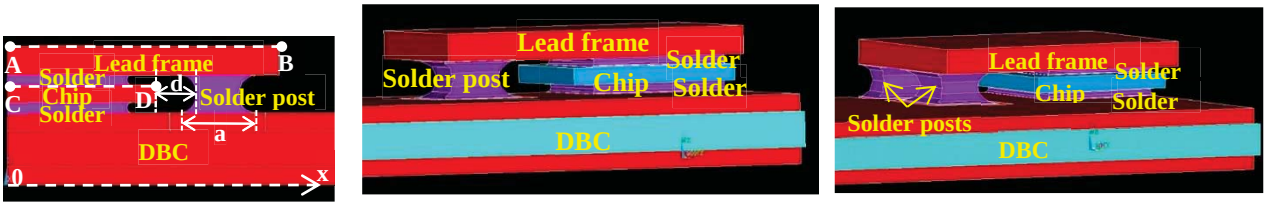
Figure 4-7. Deformation (dashed line) in double-sided module during a reflow process without (a) and with compressive posts (b).

4.3.2. Parametric Study of Compressive Posts

To verify and optimize the concept in Figure 4-7, the structure in Figure 4-3 was modeled by ANSYS 13 as shown in Figure 4-8. The model consists of the DBC substrate, solder layers, die, copper lead frame, and the solder posts. Material specifications and dimensions are in Table 4-2, and simulation setups are described in Appendix D. The distance between the post and chip is defined as *d*, and the displacements of the lead frame and chip were monitored along lines AB and CD, respectively. The number of posts was varied from zero to six, and Figure 4-8(b) shows the simulation model for a quarter of a module with four posts.

To analyze the influence of the gap between chip and post, distance (*d*) was swept from 0.5 mm to 2 mm with four and six posts. The Von-Mises plastic strains were monitored at the top solder layer and the compressive post (Figure 4-9); the dashed line is for the case without post.

When the distance (d) increases with four posts, the plastic strain decreases at the solder and increases at the compressive post. Four posts yield lower strains than six posts between 0.5 mm and 1.5 mm. Therefore, the best design is four posts separated by 0.75 mm to 1 mm from the die. The maximum Von-Mises plastic strain at the top solder layer decreases to 87.7% of the no-post value. The simulation suggests that the compressive posts yield reliable packaging process for the bonded chips and reduce stress on the die-attach layer.



(a) (b) (c)

Figure 4-8. Side view of the ANSYS models (a); the simulation model with four posts (b); and six posts (b) with dimensions in Table 4-2 (see Appendix D for modeling procedures, and Table B.(13) for simulation files).

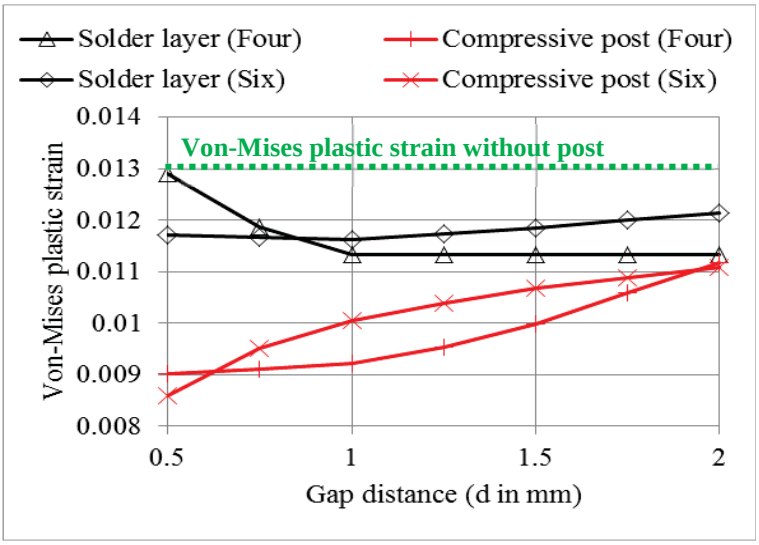


Figure 4-9. Simulated Von-Mises plastic strains at the compressive post and the solder layer between lead frame and chip in Figure 4-8(a).

Because the substrate and lead frame cover the die, the packaged chip is invisible after packaging. The height displacement of the copper lead frame was used to gauge the residual

thermo-mechanical stress in simulation and experiment. The simulation followed the demonstration and material properties in Appendix D Figure 4-10 shows the simulated displacement along line AB in Figure 4-8(a) when the temperature is stepped from 180^{o}C to 30^{o}C to emulate a cooling phase of the reflow profile. The measured displacement is plotted from the center to the edge of the module. When there is no post, the edge of the lead frame curves up by 3.25 μm as suggested by Figure 4-7(a). The edge curves up by 0.70 μm and curves down by 3.70 μm as the number posts increases to four and six, respectively. Four posts are the safe choice because the high compression force from six posts might damage the chip. The change of post quantity coarsely controls the compressive force, but the area control of each post enables fine tune of the compressive force. The blue curves in Figure 4-10 show the curvature changes with three different cross-sectional areas of the compressive post. The larger area induced more compressive force, and the length a (defined in Figure 4-8(a)) between 1.5 mm and 2mm crossed the zero displacement line. Therefore, four posts with 1.5 mm width are expected to attenuate the tensile stress to near-zero.

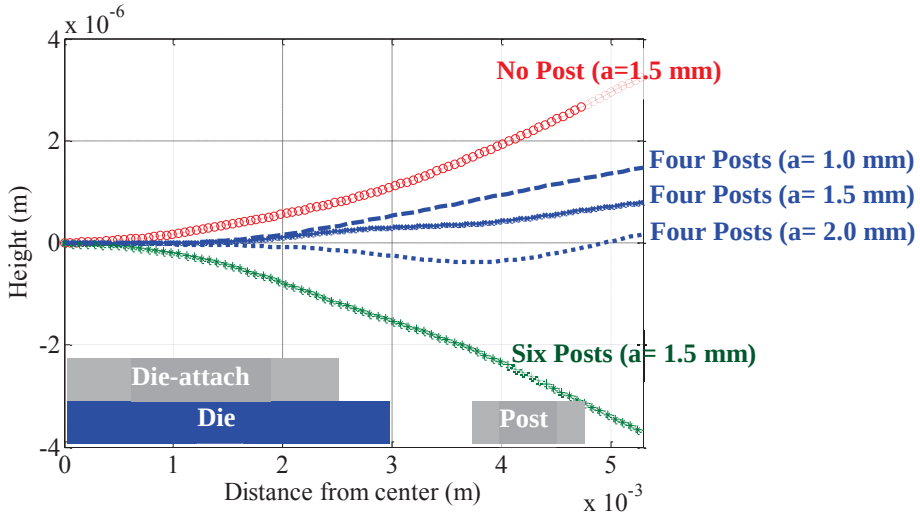
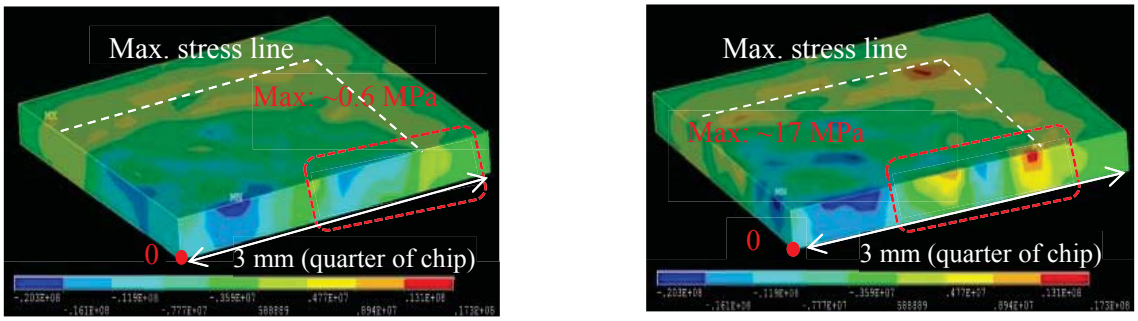


Figure 4-10. Simulated vertical displacement of the copper lead frame along the line $\overline{AB}$ in Figure 4-8(a) $(d = 0.75\ mm)$.

The Von-Mises stress on the chip is analyzed in Figure 4-11(a) and Figure 4-11(b) with conditions of no post and four posts, respectively. The maximum z-directional stress is found at the side of the chip attached to the copper lead frame; the terminating edge of the solder layer (bordered by the dashed line) experiences the highest stress. The maximum stress without the compressive posts was about 17 MPa, much higher than the expected strength of the bonding interface (~ 0.7 MPa).



(a) (b)

Figure 4-11. Z-directional stress in the silicon chips (Figure 4-8) without post (a) and with four posts (b).

The photograph in Figure 4-13 confirms the detachment of the bonded chips in the absence of the compressive posts; the cracked interface is consistent with the maximum-stress line in Figure 4-12(a).

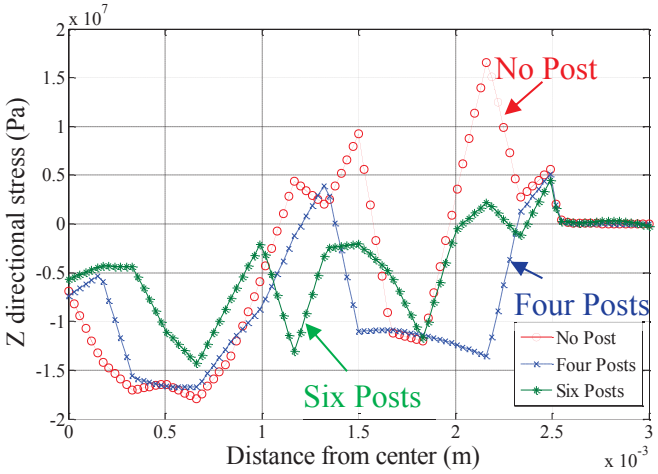


Figure 4-12. Simulated z-directional stress in the chip along the line $\overline{CD}$ in Figure 4-8(a).

The integration of four posts (Figure 4-8(b)) reduces the maximum z-directional stress to 0.6 MPa; the line of maximum stress remains the same. The photograph in Figure 4-14 confirms the integrity of the package after the addition of four compressive posts. The current-voltage characteristic and the breakdown voltage of the complete module are detailed in Chapter 5.

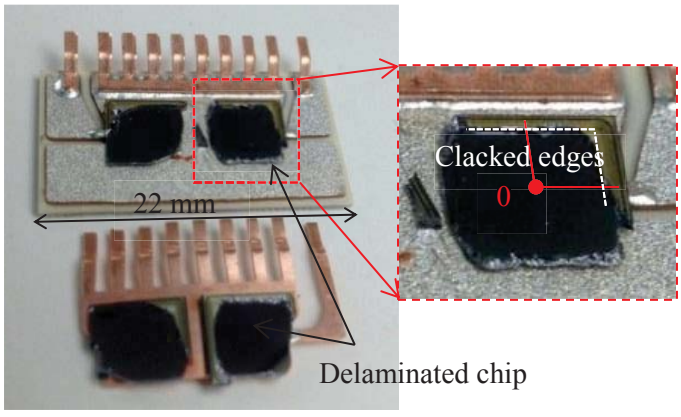


Figure 4-13. Delaminated bidirectional dies without post (refer to the simulation result in Figure 4-11(a)).

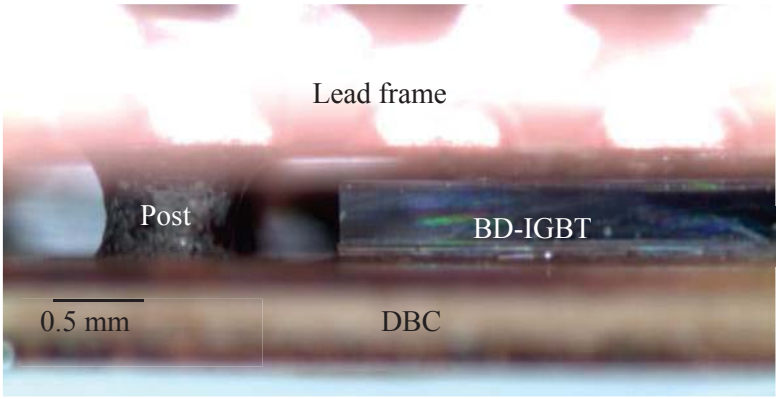


Figure 4-14. Packaged bidirectional dies without delamination by integrating four posts as modeled in Figure 4-8 (refer to the simulation result in Figure 4-11(b)).

4.4. Experimental Verification

Test samples with dummy dice and different numbers of posts were fabricated to verify the concept. Figure 4-15 shows the fabrication steps. Silver-coated DBC substrates were prepared by wet-etching, and Cirlex fixtures were designed by for alignment of posts and chip. Solder preforms ($Sn_{63}Pb_{37}$) for attachment of die and solder balls were perforated to keep the solder balls in position. The surfaces of the copper lead frame were plated by Ni-Au to protect the surface from oxidization, and to keep the surface reflective for the curvature measurement by three-dimensional optical surface profiler (Zygo NewView™ 7300).

Table 4-2. Specifications of the packaging materials for the module development in Figure 4-18 and Figure 5-2 [16]

Layer	Material	Dimensions (mm^3)	CTE (ppm/^oC)
DBC substrate	Al_2O_3	24 x 14 x 0.32	8.1
	Copper	23 x 13 x 0.127	16.4 to 17

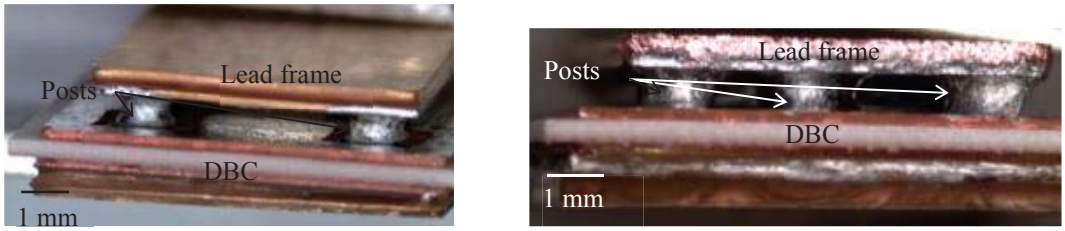
Die attach	$Sn_{63}Pb_{37}$	5 x 5 x 0.2	18.7 to 22.8
Chip	Silicon	6 x 6 x 0.4	2.25 to 2.82
Lead frame	Copper	23 x 13 x 0.5	16.4 to 17
Compressive post	$Pb_{93.5}Sn_5Ag_{1.5}$	0.72 mm diameter	~23

Figure 4-16 shows the packaged samples with four and six posts. The surface curvature was measured before and after packaging along the line indicated in Figure 4-15(d). The measurement results of three samples are shown in Figure 4-17.

Since the curvature measurement shows the relative height differences on the surface, the differences between the minimum height and the maximum height were monitored. In the sample without post, the edge of the lead frame was bent up by 13.5 μm, implying residual tensile stress to the chip. The sample with four posts was still bent up at the edge, but the height difference was 5 μm, 37% of the no-post condition. When six posts were packaged with die, the edge was bent down by 17.5 μm. Even though experimental numbers are larger than the simulated values in Figure 4-12, the impact of the number of posts on strain magnitude and polarity has been affirmed.

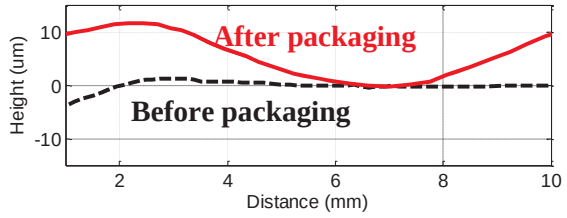
(a) (b) (c) (d)

Figure 4-15. Fabrication process of the samples for curvature measurement (the same dimensions in Table 4-2): (a) DBC substrate with fixtures; (b) solder balls and preforms; (c) Ni-Au-coated copper lead frame; and (d) packaged module after solder reflow (see Appendix B.3 for the material fabrications).

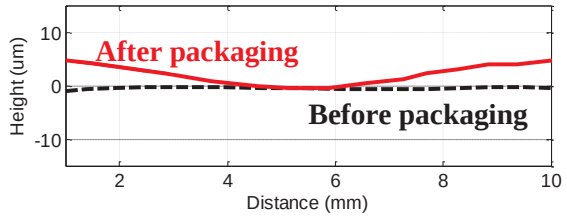


(a) (b)

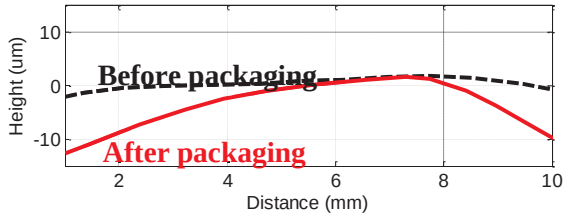
Figure 4-16. Packaged samples for curvature measurement with four posts (a) and six posts (b) after the fabrication steps in Figure 4-15.



(a)



(b)



(c)

Figure 4-17. Measured curvature changes of the samples in Figure 4-16 along the dashed line in Figure 4-15(d): (a) no post, (b) four posts, and (c) six posts.

Table 4-3. Summary of the curvature-measurement results in Figure 4-17

	Cu base plate	# of Solder post	Result (Δh)
Case 1	Without	0	↑13.5 μm
Case 2	With	4	↑5 μm
Case 3	With	6	↓17.5 μm

4.5. Fabricated Samples with Solder Posts for Cycling

ANSYS simulation results in Figure 4-9 revealed that the implementation of the compressive post helps to mitigate the plastic strain at the die-attach layer. Also the simulation result in Figure 2-9 implied the impact of CTE of encapsulation material to the reliability of die-attach layer. As a verification purpose of two assumptions, thermal cycling samples in Figure 4-18 were fabricated. The packaging components such as DBC substrate, lead frame, and fixture were fabricated using the process in Appendix B.3. Since the verification of the package was the purpose of the cycling, conventional diode in Table 4-4 with top side metallization using Cr/Ni/Ag was used for sample fabrication.

Table 4-4. Specifications of the diode for sample fabrication in Figure 4-18

Manufacturer	ABB
Part number	5SLY 12J1200 (Diode)
Dimension	10 mm x 10 mm x 0.35 mm
Front Metallization	Cr (150 nm) / Ni (200 nm) / Ag (250 nm)
Back Metallization	Al/Ti/Ni/Ag (1.2 μm)

Table 4-5. Classification of thermal cycling samples in Figure 4-18 with four conditions

	Compressive post	Encapsulation
Group 1	No	No
Group 2	Yes	No
Group 3	No	Yes
Group 4	Yes	Yes

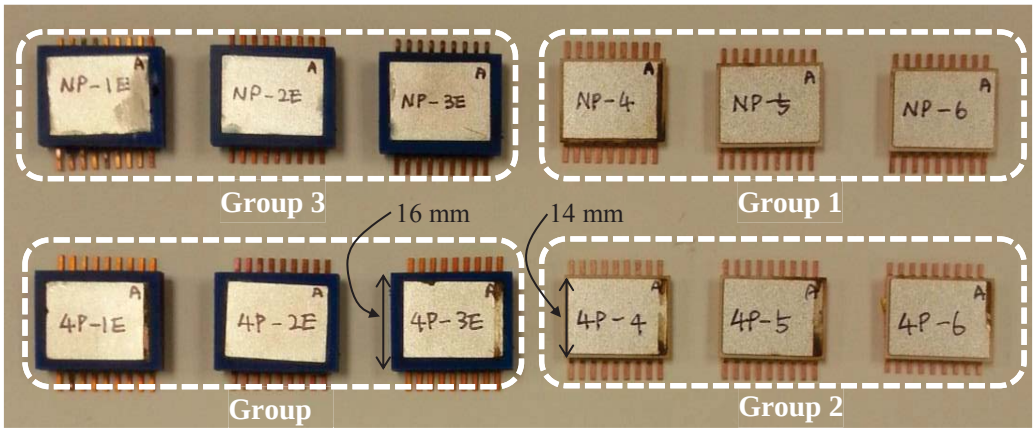


Figure 4-18. Fabricated samples for thermal cycling with four groups as specified in Table 4-5.

The thermal cycling profile in Figure 4-19 follows the JEDEC standard (JESD22-A104D) that has temperature range from -40°C to 125°C and 10 minutes soaking time. The blue and red curve in Figure 4-19 are showing programmed and measured temperature of the chamber, respectively. The temperature was measured by K-type thermocouple that was attached on the DBC substrate. Even though there was delay to reach the peak temperature, the soaking time was long enough to achieve homogeneous temperature distribution of the entire chamber and samples.

Table 4-6. Specifications of the JEDEC thermal cycling profile in Figure 4-19

JEDEC JESD22-A104D	Recommended profile for solder layer
Period	< 2 Hours (calibrated time: 90 minutes)
Soaking time	10 minutes
Temperature range	-40°C to 125°C

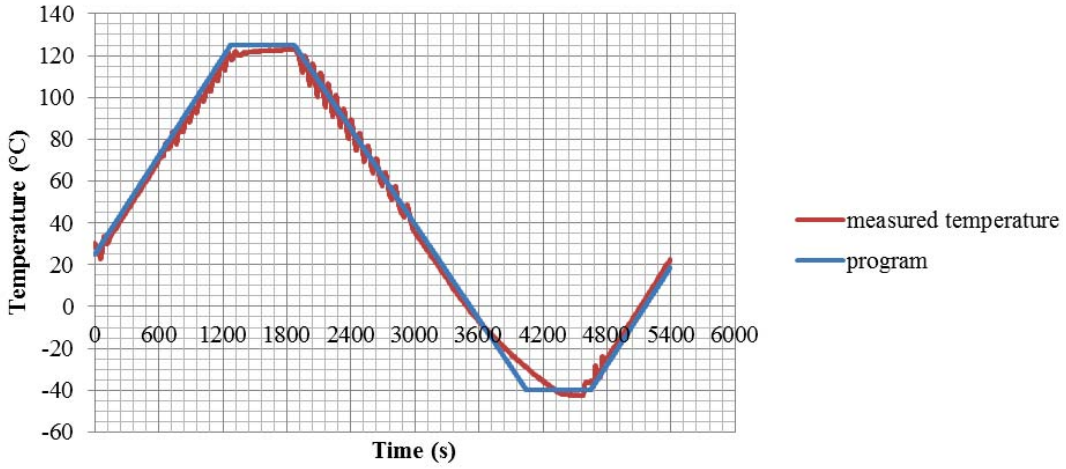


Figure 4-19. Thermal cycling profile based on the JEDEC standard (JESD22-A104D) with specifications in Table 4-6.

Thermal impedances of the samples were measured with 40 ms heating pulse in every 200 cycles using the measurement method in Appendix C.3. Figure 4-20 shows the change of thermal impedances after 1200 thermal cycles. All samples showed minor changes by 400 cycles, but the increase rates were rather drastic after 600 cycles. The sample without post and encapsulation showed the highest change, and the cross-section of the sample is shown in Figure 4-21(a). The sample shows cracks at both top and bottom joints where the IMC exists between solder and chip. In case of the sample with four posts without encapsulation, the increase rate was much lower than the sample without post. The cross-section of the sample shows that the top joint delaminates like the sample without post, but the bottom joint showed much healthier condition. The thermo-mechanical simulation results showed much higher Von-Mises plastic strain at the top joint, and the cycling results showed the consistent result as simulation results. In case of the encapsulated samples with/without compressive posts, the increase of thermal impedances were less than 20%, and the cross-sectioned samples showed healthy solder joints. The encapsulated

sample without post shows the sign of delamination at the interface between top joint and chip, but the overall conditions are similar to the sample with compressive posts. The thermal cycling shows give three important conclusions in terms of reliability. The compressive post helps to reduce the residual stress at the die-attach layer; the over-molded structure by molding compound keeps the residual-compressive force during cycling; and the molding compound cancels the asymmetric expansions of materials due to CTE mismatches.

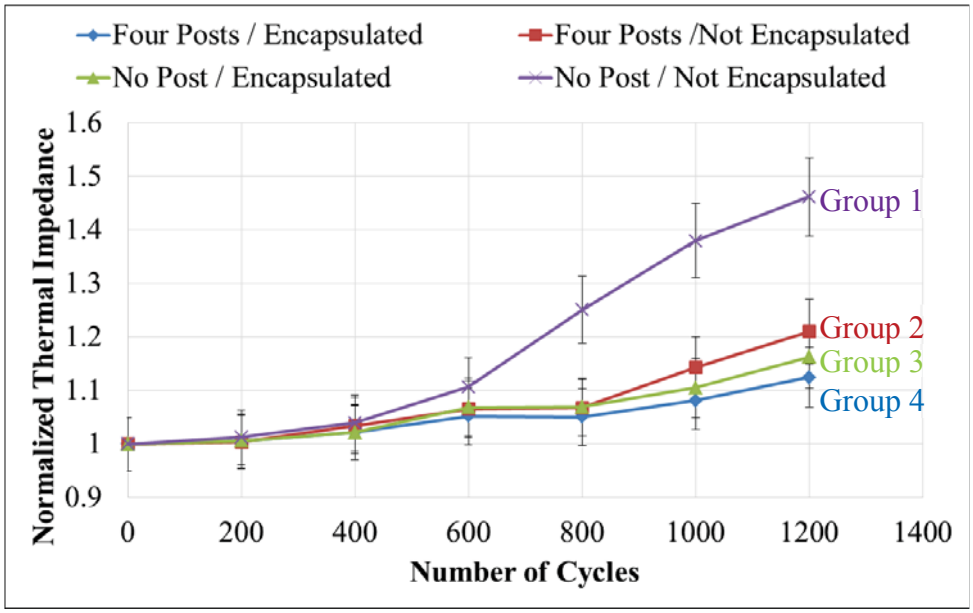


Figure 4-20. Measured thermal-impedance change of the cycling samples in Figure 4-18 using the measurement method in Appendix C.3.

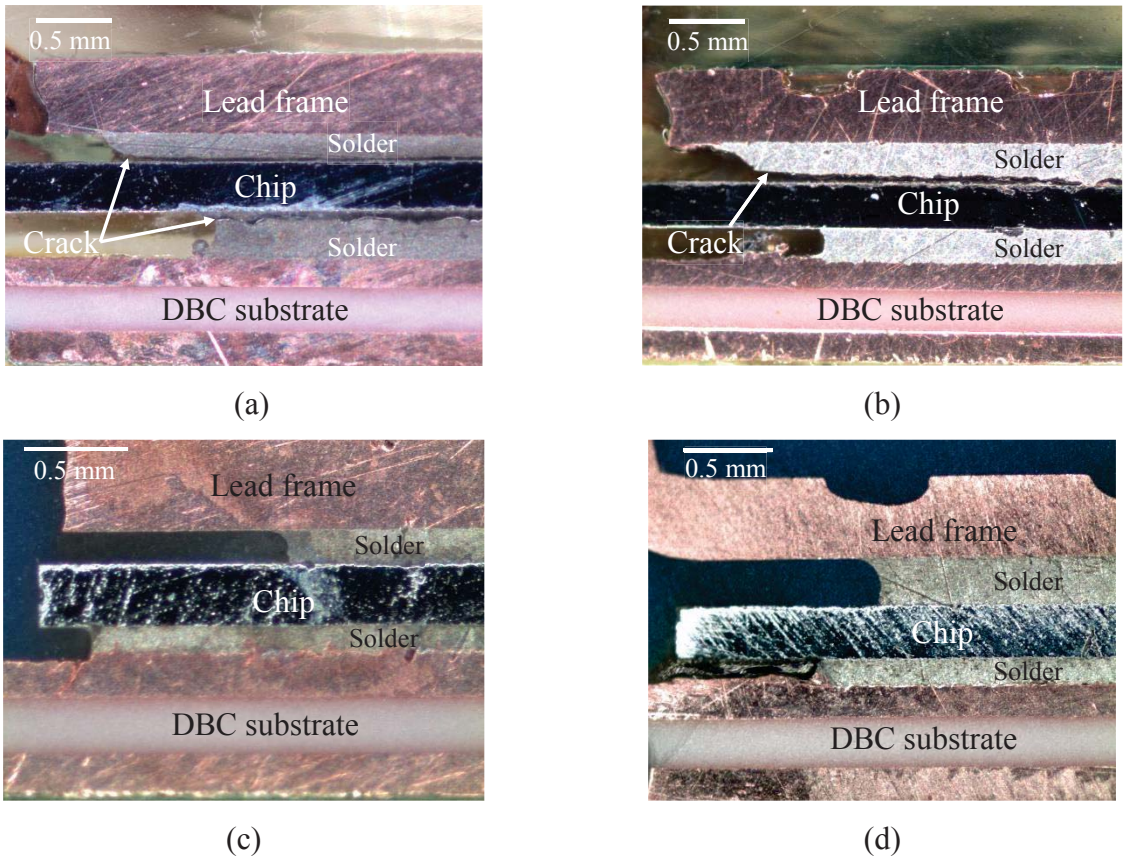


Figure 4-21. Cross-section of the thermal-cycling samples in Figure 4-18 after 1200 cycles; (a) no post without encapsulation (group 1), (b) four posts without encapsulation (group 2), (c) no post with encapsulation (group 3), and (d) four posts with encapsulation (group 4).

4.6. Summary

Compressive post has been investigated as a means to reduce residual thermo-mechanical stress in a power-electronic module. Because the mismatch among CTE's result in asymmetrical shrinkage during cooling phase, especially in double-sided packaging process, a chip could warp or crack due to residual stress.

For the 6.6 mm x 6.6 mm die studied, the optimal arrangement would place four posts symmetrically around the chip, each post at a distance between 0.75 mm and 1 mm from the

chip's edges. The bonded chips no longer detached and the module fully functioned after being sandwiched between a DBC substrate and a copper lead frame. The Von-Mises plastic strain at the die-attach layer was reduced to 87.69% of the strain without compressive posts, implying enhanced fatigue lifetime of the joint.

To verify the compressive force by the posts, curvature change of the lead frame was measured as an indicator of the thermo-mechanical stress at the chip. As the number of posts increased, the curvature at the edge changed from upward to downward, as tensile stress became compressive stress.

The influence of the compressive post and the molding compound to the reliability of the die-attach layer was verified by thermal cycling. The module without compressive post that represents a conventional double-sided module showed the earliest failure, but the module with compressive post showed much more extended lifetime and healthier joint conditions after the same amount of thermal cycles.

Both simulation and experimental results prove that the compressive posts alleviate the tensile stress in a package and enhance the reliability of the module.

4.7. Reference

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Chapter 5. FABRICATION AND CHARACTERIZATION OF THE COMPLETE BIDIRECTIONAL MODULE

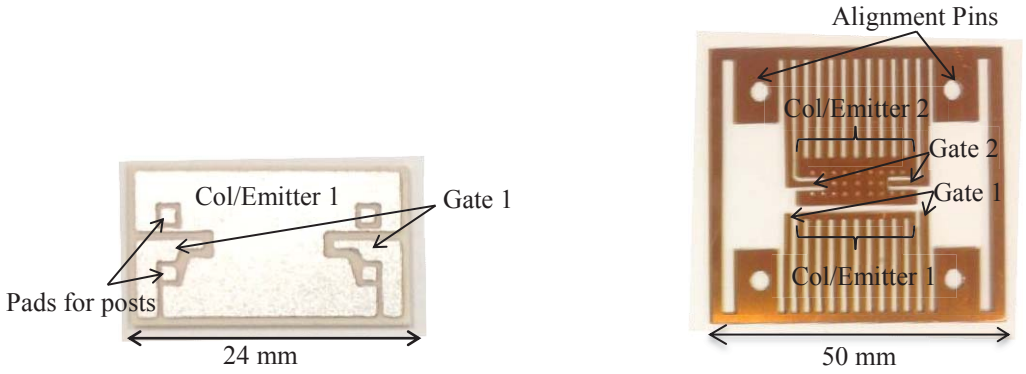
5.1. Introduction

The bidirectional IGBT was packaged based on optimized parameters, including an indented lead frame, particular shape of the die-attach layer, and use of compressive posts. Two bidirectional modules were developed; the first module had two chips in parallel to increase the current capacity, and the second module was packaged with a single die. As a comparison to the developed module, a unidirectional die that was used for the wafer-bonding process was packaged with diodes as the BD-module. The electrical characteristics and thermal characteristics of these two modules were compared to assess pros and cons of the developed module. Detailed packaging steps and equipment for hardware design and fabrication are described in Appendix B.

5.2. Packaged BD-Module with Compressive Posts

5.2.1. Multi-Chip Module (1.2 kV / 50 A)

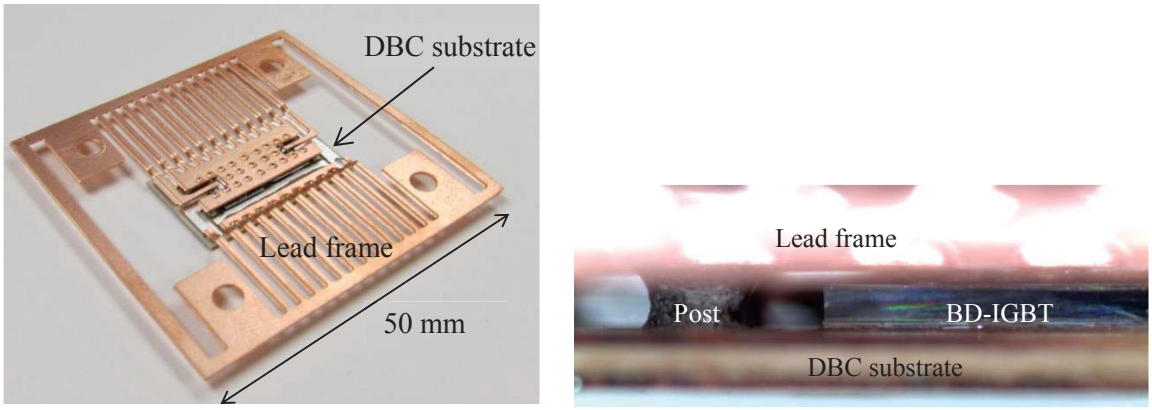
The DBC substrate and lead frame were designed to accommodate two chips in parallel. The packaged module was a six-terminal device that had four gate pins and two col/emitter pins. Figure 5-1 shows the prepared DBC substrate and copper lead frame. Both substrates were prepared by laser routing and a chemical etching processes.



(a) (b)

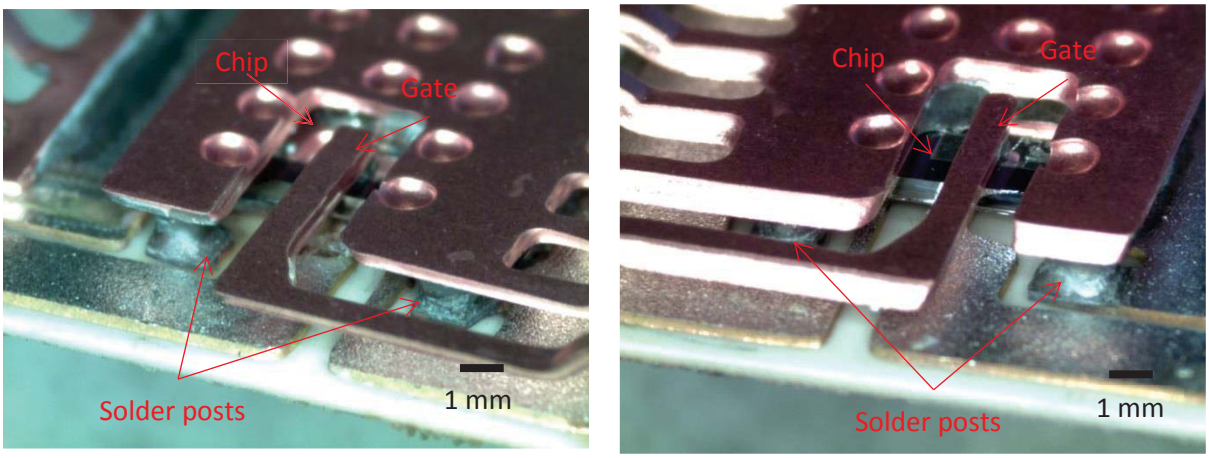
Figure 5-1. DBC substrate (a) and copper lead frame (b) for the fabrication of BD-module with two chips in parallel (see Table B.(18) for the AutoCAD layout).

The packaged module is shown in Figure 5-2(a) and Figure 5-3. The alignments among packaging components were precisely kept with the aid of Cirlex fixtures. The compressive posts were naturally formed in an hourglass shape due to the smaller diameter of the solder ball compared with the pad sizes on the DBC substrate. The chip delamination phenomenon was no longer observed with compressive posts (Figure 5-2(b)), and the functionality of the packaged module was verified in Chapter 5.3.



(a) (b)

Figure 5-2. Fabricated module with four solder posts (a) and side view of the packaged module (b) using the same packaging steps in Figure 5-5.

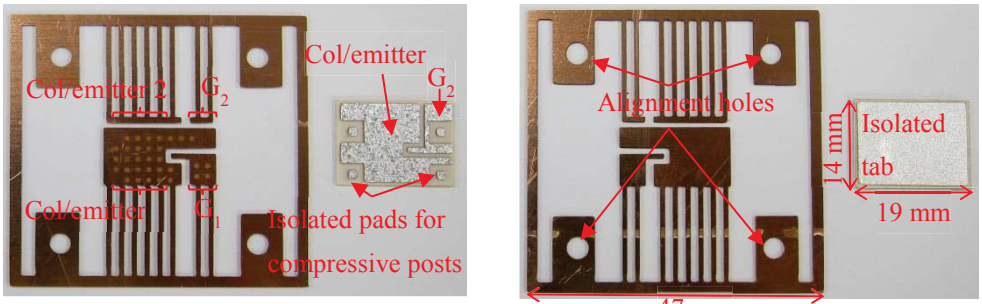


(a) (b)

Figure 5-3. Side view of the packaged module in Figure 5-2.

5.2.2. Single-Chip Module (1.2 kV / 25 A)

The single-chip module was developed with a reduced current and footprint area. The overall structure of the module was similar to the multi-chip module. Figure 5-4 shows the prepared DBC substrate and lead frame using the layouts in Appendix B.1 and fabrication processes in Appendix B.3.



(a) (b)

Figure 5-4. Prepared lead frame and DBC substrate for the packaging of single chip module (see Appendix B for the layout and fabrication process, and Table B.(19) for AutoCAD layouts).

Figure 5-5 shows the packaging procedures. The lead frame was prepared by a chemical etching process, and shaped using the same molds as in Figure 2-19. The Cirlex fixture in (c)

was prepared to align chip and solder preforms for the post. Sn63Pb37 solder preforms were used, and a solder mask was applied around the gate pad to prevent solder overflow from col/emitter to gate. The module after vacuum reflow process is shown in (f), and (g) shows the module after lead-frame trimming.

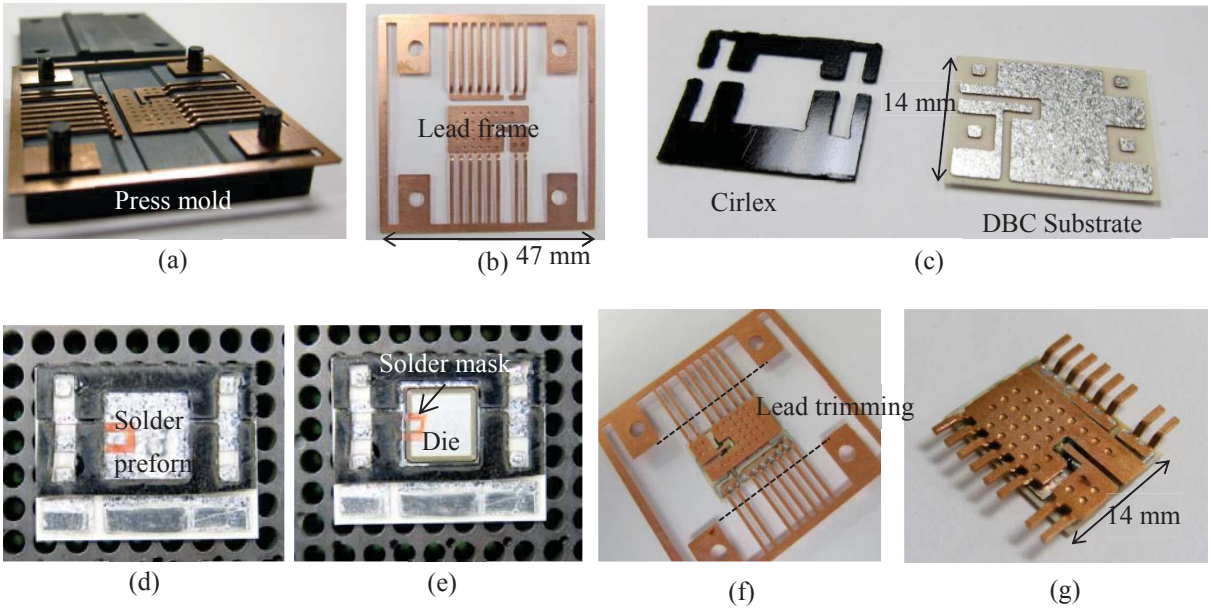


Figure 5-5. Packaging process of the single chip module using components in Figure 5-5: (a)(b) lead frame shaping; (c) Cirlex fixture and DBC substrate; (d) place solder preform; (e) place die with mask; (f) after vacuum reflow process; and (g) lead frame trimming.

Figure 5-6 shows the encapsulated module next to a U.S. Quarter coin. The device has four terminals as designed, and the bottom side copper of the DBC substrate was exposed for heat management.

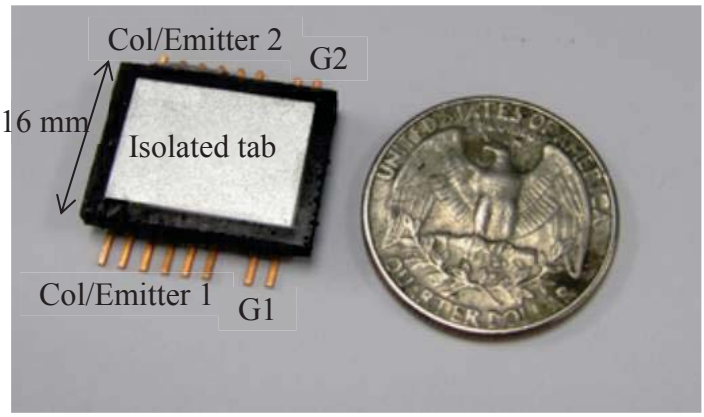


Figure 5-6. Encapsulated single chip module in Figure 5-5 using the encapsulation process in Figure 2-14.

5.3. Comparison of Characteristics between the Developed Module and a Conventional Layout

The developed BD-module was successfully packaged using a wafer-bonded chip to replace the conventional BD-module with two IGBTs and two diodes. As a comparison with the developed BD-module, another BD-module with a conventional layout was fabricated. This module had a lateral layout with four dice as shown in Figure 5-7, and the unidirectional die that was used for the BD-IGBT was used for fair comparison. A 1.2 kV rated diode is recommended for use in order to fully utilize blocking voltage of IGBT, but the 650 V SiC SBD (Schottky Barrier Diode) was used here due to limited availability. A commercially available benchmark module (MMIX1G82N120A3V1) was also selected to consider the option of using two discrete modules. The selected benchmark module has one IGBT and an anti-parallel diode, and the power rating is 1.2 kV / 66 A.

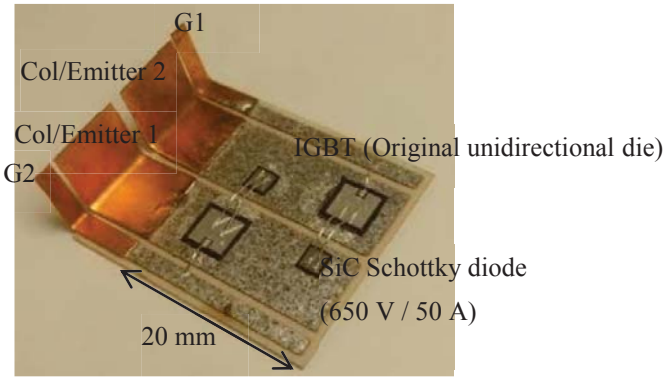
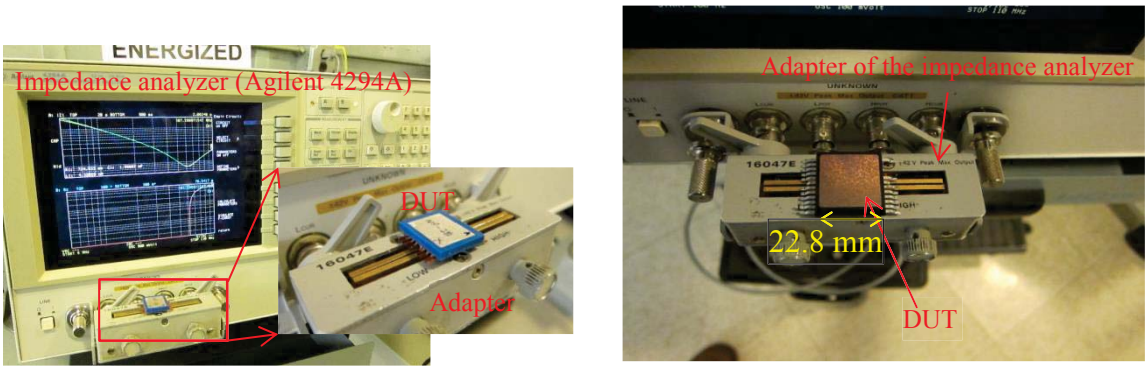


Figure 5-7. Benchmark bidirectional module with two IGBTs and two diodes as described in Figure 1-2(a) (see Table B.(20) for the AutoCAD layout).

5.3.1. Package Inductance

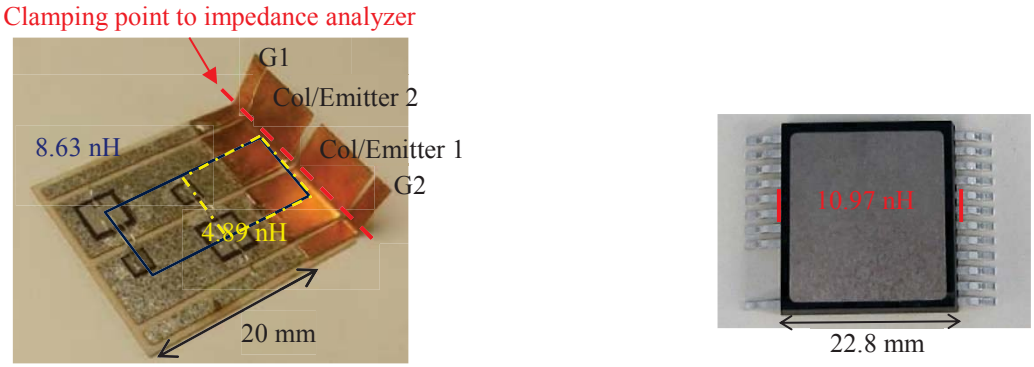
A package inductance is not adjustable once a module is packaged. Thus, it was attempted to minimize the package inductance to acquire fast switching speed and low ringing. An impedance analyzer was used to measure package inductance (Agilent 4294A). The lead frame of the module was directly clamped at the adapter of the test equipment, and five measurements were averaged to reduce measurement error.



(a) (b)

Figure 5-8. Parasitic inductance measurement of the developed module (Figure 5-6) (a) and benchmark module (MMIX1G82N120A3V1) (b) by impedance analyzer (Agilent 4294A).

The benchmark module with a conventional layout had two power loops as indicated in dashed and solid lines in Figure 5-9. The inner loop (dashed line) showed 4.89 nH and the outer loop (solid line) showed 8.63 nH. Another benchmark module from IXYS was measured at center leads as indicated in the red line in Figure 5-9(b), and the measured package inductance was 10.97 nH.



(a) (b)

Figure 5-9. Measured package inductances of the benchmark modules; (a) BD-module with four discrete dice (Figure 5-7), and (b) IGBT module with anti-parallel diode (MMIX1G82N120A3V1).

The developed module was measured using the same method, and the inductances measured at center leads were 0.49 nH and 3.29 nH before and after encapsulation, respectively, which was up to 10% lower than that of the module with a conventional layout. Since the bond wires on the

emitter side of the die mainly introduce parasitic inductances, the implementation of the indented lead frame helped to significantly reduce the parasitic inductance.

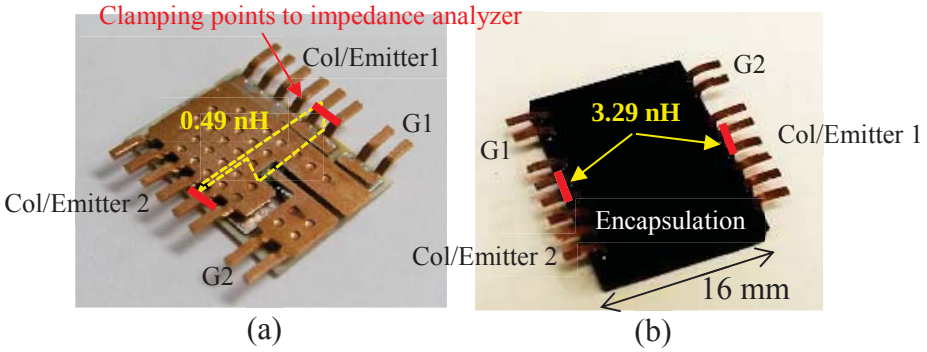


Figure 5-10. Measured package inductance of the developed BD-modules using impedance analyzer in Figure 5-8; before (a) and after (b) encapsulation.

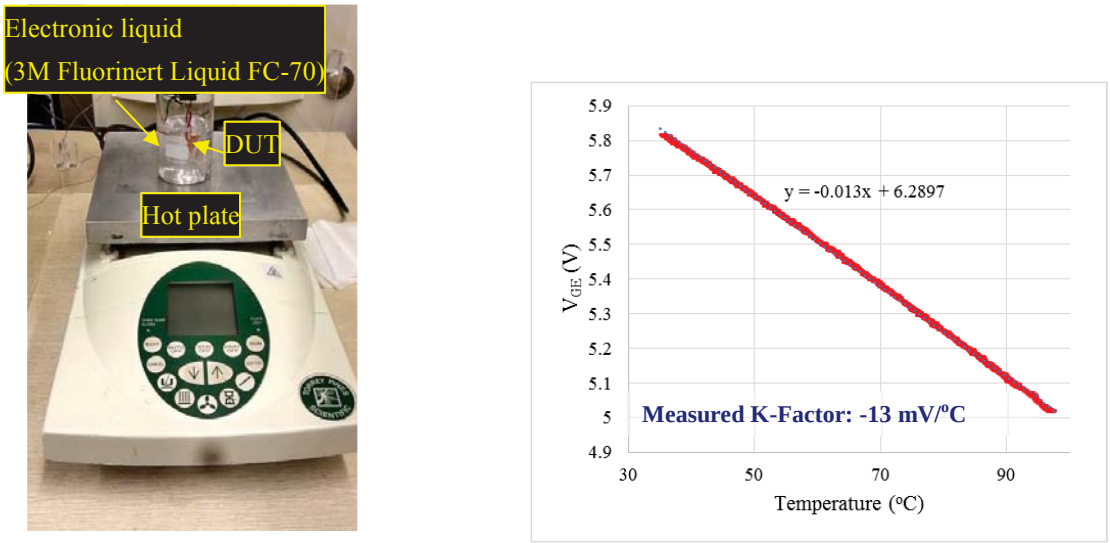
5.3.2. Thermal Characteristics

The use of the double-sided die is advantageous in terms of parasitic inductance and footprint area, but it is less desirable for heat dissipation. The BD-IGBT has two junctions, unlike the unidirectional dice, which can be considered as two heat sources in one die. Also a gate pad at the back reduces the die-attach area for heat dissipation, while the entire back of the conventional die is being used for heat sinking. Thermal impedances of fabricated modules in Figure 5-9(a) and Figure 5-10 were measured to analyze the impact of a reduced die-attach area. A temperature sensitive parameter -- gate-emitter voltage -- was used to sense the junction temperature for accurate measurement. The temperature sensing method using V_{GE} requires a calibration process, namely K-factor measurement, which characterizes V_{GE} response to the temperature change. A bare die was damped in the electronic liquid (3M FC-70) for accurate measurement. The

electronic liquid, with specifications in Table 5-1 has a very high density and specific heat with low thermal conductivity, which helps to keep the temperature steady during a measurement. The hot plate was initially set to 100°C and slowly cooled down to 30°C at a -0.3°C/min rate. Figure 5-11(b) shows the measured V_{GE}, and the K-factor is calculated to be -13 mV/°C.

Table 5-1. Specifications of the electronic liquid in Figure 5-11(a) for K-factor measurement

Part number	FC-70
Boiling temperature	215°C
Liquid density	1940 kg/m^3
Specific heat	1100 J/kg-°C
Thermal conductivity	0.070 W/m-°C
Dielectric strength	400 V/mil



(a) (b)

Figure 5-11. Test setup for the K-factor measurement of BD-IGBT in Figure 2-23 (a), and the measurement result (b).

The procedure for the thermal impedance measurement is illustrated in Figure 5-12. The device under test was placed on a liquid-cooled heat sink, and thermal grease was applied in

between to compensate for surface roughness. Clamping force was applied on top of the module to ensure good contact, and the force was controlled as 10 N/cm^2 for all measurements (JESD51-14). Heating pulses from 20 ms to 200 ms were applied, and thermal impedances were calculated using measured V_{GE} and applied power. Five measurements were averaged for each condition, and the maximum measurements error was 1%. The specific thermal resistances were calculated for both modules, and are compared in Figure 5-13. The developed module shows up to a 32% reduction in specific thermal resistance compared to the conventional module with a bond wire on top. Thanks to the bidirectional IGBT and double-sided structure, the developed module has a 266-mm^2 footprint area, which is 66.5% less than the conventional module (400-mm^2). Therefore, even though the developed module loses die-attach area due to a back-side gate, it shows less specific thermal resistance than the conventional four-chip module.

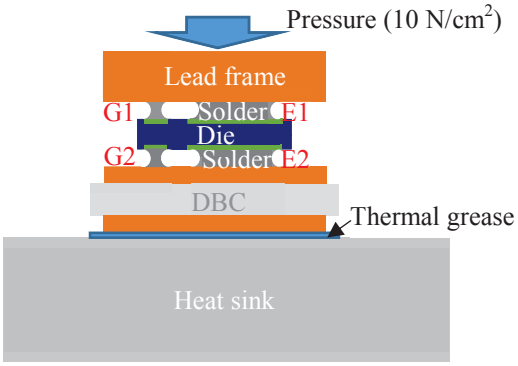


Figure 5-12. Illustration of the thermal-impedance measurement.

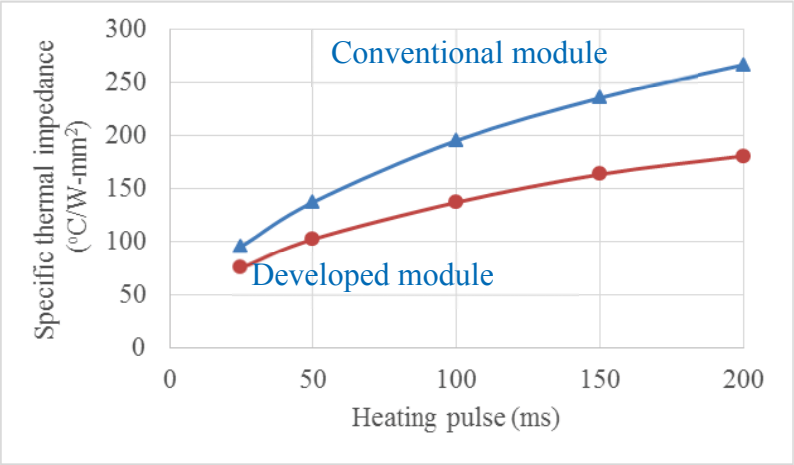


Figure 5-13. Measured specific thermal impedance using test condition in Figure 5-12 with 20 ms to 200 ms heating pulse (modules in Figure 5-7 and Figure 5-10).

Table 5-2. Summary of the module characterizations

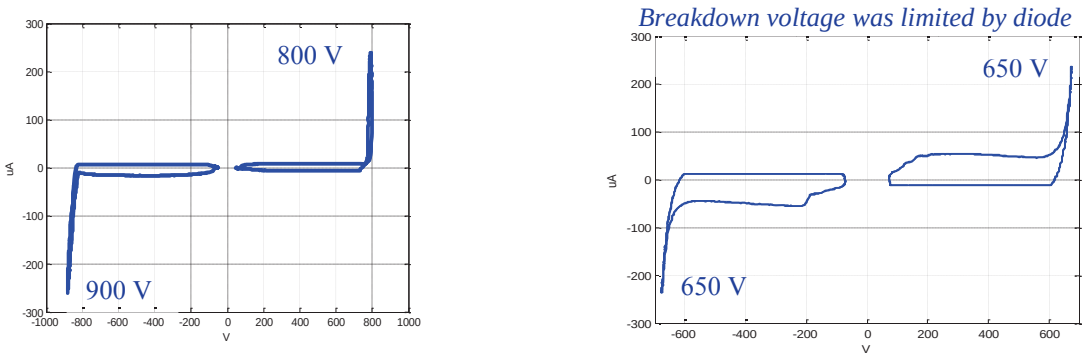
	Developed module (bidirectional module)	Benchmark module from IXYS	Benchmark module with 2 IGBTs and 2 Diodes (Figure 5-7)
Parasitic inductance (nH)	3.29	10.97	4.89 (shorter loop) 8.63 (longer loop)
Specific thermal impedance (^{o}C/W-mm^{2})	180.01	146.77	265.71

5.3.3. Dielectric Strength

A curve tracer (Tektronix 371A) in Figure 5-14 was used to measure blocking voltage of the developed module. The benchmark module from IXYS (MMIX1G82N120A3V1) showed 1.2-kV blocking voltage as listed in a datasheet, so the measurement result is not added here. The BD-modules with wafer-bonded die and unidirectional die were measured in both directions, and the results are shown in Figure 5-15.

Figure 5-14. Curve tracer (Tektronix 371A) for the breakdown voltage and I-V curve measurement.

The voltage was increased until the leakage current reached 250 μA. The module with the BD-IGBT showed 800 V and 900 V blocking voltages, and the module with a diode showed 650-V blocking voltages in both directions. Since the packaged diode had a blocking voltage of 650-V, the maximum blocking voltage was limited by diode for the conventional module. The reason the blocking voltage was unbalanced in the developed module could be the result of two cases. The first case involves voids in the molding compound. Even though the molding compound was filled in a vacuum chamber, air bubbles still can be trapped inside the module. In practice, the transfer molding process will help to deal with this problem. The die characteristic unbalance could also be for another reason. The characteristic unbalance has been reported in several literatures [4]-[6], and it cannot be dealt with through the packaging method. The height variation of the solder joint could be a reason, but the spacer in the solder preform (Figure 3-10) controls the height. Thus height variation is not the likely reason for the unbalanced breakdown voltage.

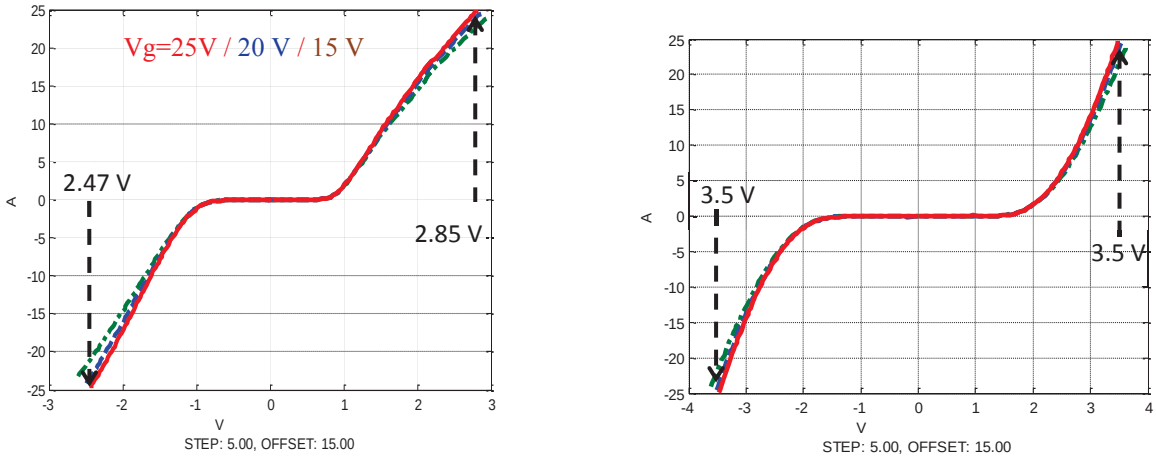


(a) (b)

Figure 5-15. Measured breakdown voltage of the developed BD-module (a) and conventional module (b) at 250 μA leakage current (modules in Figure 5-7 and Figure 5-10).

5.3.4. I-V Characteristics

On-state voltages were measured using the curve tracer, as shown in Figure 5-14. Figure 5-16(a) shows the forward and reverse conductions of the BD-module using the wafer-bonded die, and (b) shows the result of the module with four discrete dice. In compared measurement results in (a) and (b), the developed BD-module showed less forward-voltage drop than the one with a diode, but the on-state voltage at 25 A showed a 14.29% difference in forward and reverse conductions. Again, the variations in bidirectional conduction have been reported in literature, and this will have to be dealt with in the die-fabrication process.



(a) (b)

Figure 5-16. Measured bidirectional I-V characteristics of the developed BD-module (a) and conventional module (b) (modules in Figure 5-7 and Figure 5-10).

5.4. Summary

The functionality and characteristics of the developed module were experimentally verified in this chapter. The package inductance is reduced to 10% that of the package with a conventional layout of two IGBTs and two diodes. The use of a single die (wafer-bonded die) and a three-dimensional layout with an indented lead frame played a major part in the package inductance reduction. However, the thermal resistance had to be sacrificed due to reduced die-attach area at the back of the chip. Compared with the conventional BD-module, the developed module using a wafer-bonded die showed up to 17.24% larger thermal impedance. Both blocking voltage and on-state voltage was unbalanced in forward and reverse conditions, but these unbalances had to be dealt with in the die-fabrication process. Overall, the process with the compressive post successfully packaged the wafer-bonded chip without delamination.

5.5. Reference

[1]. Jia Woei Wu, Sauvik Chowdhury, Nga C Lee, Collin Hitchcock, James J.-Q. Lu, and T. Paul Chow, "1200V, 25A Bidirectional Si DMOS IGBT fabricated with fusion wafer bonding," *in Proc. International symposium on power semiconductor device and ICs*, June. 2014.

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[7]. K.D. Hobart, F.J. Kub, G. Dolny, M. Zafrani, J.M. Neilson, J. Gladish, and C. McLachlan, "Fabrication of a double-side IGBT by very low temperature wafer bonding," *in Proc. Power Semiconductor Devices and ICs (ISPSD)*, 1999, pp. 45-48.

Chapter 6. CONCLUSION AND FUTURE WORK

6.1. Introduction

This dissertation focuses on the development of a bidirectional module using wafer-bonded bidirectional IGBTs (BD-IGBT). Since the strength of the bonding interface in the BD-IGBT is much weaker than the residual thermo-mechanical stress of the module, the die easily delaminates during the packaging process. The compressive-post packaging method, with the aid of the indented lead frame is discussed as a way to deal with chip delamination during packaging process.

ANSYS simulation verified that the induced tensile and shear stresses at the die are larger than the bonding strength of the die-interface. The simulated curvature change of the lead frame supported the assumption that both top and bottom substrates (lead frame and DBC) bow outside of the package. The compressive-post was developed to constrain the substrate bending that induces compressive force to the die.

It is well known that a three-dimensional structure helps to reduce the parasitic inductance of the module. At the same time, however, the double-sided structure increases viscoplastic strain at the solder joint, which leads to early failure. The indented lead frame is introduced in this paper in order to lessen thermo-mechanical stress while still keeping the advantages of a three-dimensional structure.

6.2. Main Contributions and Conclusions

1. The package for wafer-bonded die was developed.

Previous studies introduced the fabrication of the BD-IGBT. However, the packaging of double-sided die in a three-dimensional package was a new attempt. The bonding interface of the die has only 0.7 MPa bonding strength, and it is much lower than the initial stress in a package after the reflow process. This dissertation found solutions to alleviate the initial stress while keeping advantages of the three-dimensional package.

2. An indented lead frame has been developed and optimized by parametric study.

The module has been developed as a surface-mount device using copper lead frame. Unlike a conventional lead frame that has a lateral layout, the developed lead frame has been shaped to make multiple contacts to both the front of the die and the bottom DBC substrate. The height difference between chip and DBC substrate was precisely compensated for using the designed press mold. Nitric acid (10% HNO_3) was used to etch away the oxidization layer of the copper lead frame. The die-attach layer between lead frame and die showed larger viscoplastic strain than the other joint due to the high CTE of copper (17 ppm/^{o}C). The indented lead frame helps to distribute thermo-mechanical stress to a wide area by not having the maximum stress point at the corner. However, the indentation on the lead frame reduces the copper volume, which increases electrical and thermal resistances of the lead frame. The impact of indentation geometry to viscoplastic strain, electrical resistance, and thermal resistance were parametrically studied. The diameter, pitch, and depth of the indentation have

been controlled, and ANSYS was used for simulation. The simulation results revealed that the depth-controlled method most effectively reduces the viscoplastic strain (28.56% reduction) while minimizing the electrical and thermal resistance degradations (20.35% and 21.67%, respectively).

3. An hourglass joint for large-chip attachment was investigated and the packaging process was developed.

The thermo-mechanical stress and thermal characteristic of the hourglass joint were parametrically studied. The hourglass joint showed the maximum stress at the center of the curved-surface, and the maximum plastic strain was 4.5% of the maximum strain in the fillet joint. In the case of plastic strain at the interface, where IMC exists, the plastic strain of the hourglass joint was 13% of the fillet joint. One of the drawbacks of the hourglass joint is the reduced die-attach area when compared to the fillet joint. The junction-to-case thermal resistance was simulated by changing the die attach area from 60% to 100% of the chip size. The simulation results showed that the thermal resistance was increased by 9% compared to that of the fillet joint with 90% area and 0.18 mm height that is a fair trade-off for the 23% reduction in thermo-mechanical stress. A packaging process was developed to control the height and shape of the joint, and the optimum parameters for shaping the hourglass joint were empirically found.

4. The compressive post was developed and experimentally verified.

The compressive post has been studied to reduce residual stress in a power module. The combination of the double-sided package and wafer-bonded die made the packaging process vulnerable to thermo-mechanical stress. The optimum layout of the posts was found using ANSYS simulation, and the best design was found to be four posts separated by 0.75 mm to 1 mm from the die. The maximum Von-Mises plastic strain at the top solder layer decreases to 87.7% of the no-post value. The z-directional stress at the die is the key parameter that induces chip delamination. The four posts with 0.75 mm separation from die reduced the maximum stress at die from 17 MPa to 0.6 MPa. Since the strength of the bonding interface was about 0.7 MPa, the wafer-bonded die could be securely packaged. The curvature change of the lead frame was monitored as an indicator of compressive force. Fabricated samples with no post, four posts, and six posts showed 13.5 μm upward, 5 μm upward, and 17.5 μm downward, respectively, which verifies the attenuation of the residual stress.

5. Integrated packaging process of the BD-module.

Packaging processes for one-chip and two-chip modules were developed. The developed module was compared with a benchmark module that had two IGBTs and two diodes. Thanks to the double-sided package with the indented lead frame, the package inductance was reduced to 10% that of the benchmark module. Thanks to the reduced footprint area, the specific thermal resistance of the module was also reduced by 32% of the conventional four-chip module. Both blocking voltage and on-state voltage was unbalanced in forward and reverse conditions, but these unbalances had to be dealt with in the die-fabrication process.

Overall, the developed packaging process securely packaged the wafer-bonded chip without any delamination problem.

6.3. Future Work

The work presented the topics of future work:

1. Study of thermo-mechanical stress control using encapsulation material
2. Impact of substrate material to the reliability of the module
3. Enhancement of heat dissipation in the developed BD-module

LIST OF PUBLICATIONS

JOURNAL PAPERS

[1] **Woochan Kim**, Jongwon Shin, and Khai D.T. Ngo, "DBC switch module for management of temperature and noise in 220-W/in^3 power assembly", *Journal of Microelectronics and Electronic Packaging*, Dec. 2014.

[2] **Woochan Kim**, Jia-Woei Wu, Bill Alexander, Sauvik Chowdhury, Collin Hitchcock, Nga C. Lee, James J.Q. Lu, T. Paul Chow, and Khai D.T. Ngo, "Compressive-post packaging of double-sided dies", *Journal of Microelectronics and Electronic Packaging*, 2015.

[3] Jongwon Shin, **Woochan Kim**, and Khai D.T. Ngo, "DBC switch module for management of temperature and noise in 220-W/in^3 power assembly", *IEEE Trans. Power Electronics*, Sep. 2014.

CONFERENCE PAPERS

[1] **Woochan Kim**, Jongwon Shin, and Khai D.T. Ngo, "DBC switch module for management of temperature and noise in 220-W/in^3 power assembly", *in Proc. International Microelectronics Assembly and Packaging Society (IMAPS),* 2014, Oct.

[2] **Woochan Kim**, Jia-Woei Wu, Bill Alexander, Sauvik Chowdhury, Collin Hitchcock, Nga C. Lee, James J.Q. Lu, T. Paul Chow, and Khai D.T. Ngo, "Compressive-post packaging of double-sided dies", *in Proc. International Microelectronics Assembly and Packaging Society (IMAPS)*, 2014, Oct.

[3] **Woochan Kim**, S. Luo, Guo-Quan Lu, and K.D.T. Ngo "Integrated current sensor using giant magneto resistive (GMR) field detector for planar power module," *in Proc. Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, pp. 2498 - 2505, 2013, March.

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[5] Jongwon Shin, **Woochan Kim**, and Khai D.T. Ngo, "DBC switch module for management of temperature and noise in 220-W/in3 power assembly", *in Proc. Applied Power Electronics Conference and Exposition (APEC),* 2015 (accepted).

[6] Jia Woei Wu, Sauvik Chowdhury, Nga C Lee, Collin Hitchcock, James J.-Q. Lu, **Woochan Kim**, Khai D. T. Ngo, and T. Paul Chow, "1200V, 25A bi-directional Si DMOS IGBT fabricated with fusion wafer bonding", *in Proc. Power Semiconductor Devices & IC's (ISPSD),* June, 2014, pp. 95 – 98.

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[1] Khai D.T. Ngo, Woochan Kim, and Tao Tao, "Packaging Method for Semiconductor Dice with Multiple Contacts on Both Front and Back Sides", VTIP NO.: 13-029, Apr, 2013.

Appendix A. Fabrication of Test Fixture for Double-Side Die

1. *Test fixture for high current measurement*

A test fixture for die was developed for characterization. Conventional curve tracer has a probe station with needle tips. However, this type of probe is easy to scratch the surface of die and not suitable for high current testing. A solid contact to die was required, and the copper strip in Figure A-1 was used to make contacts to gate and emitter pads.

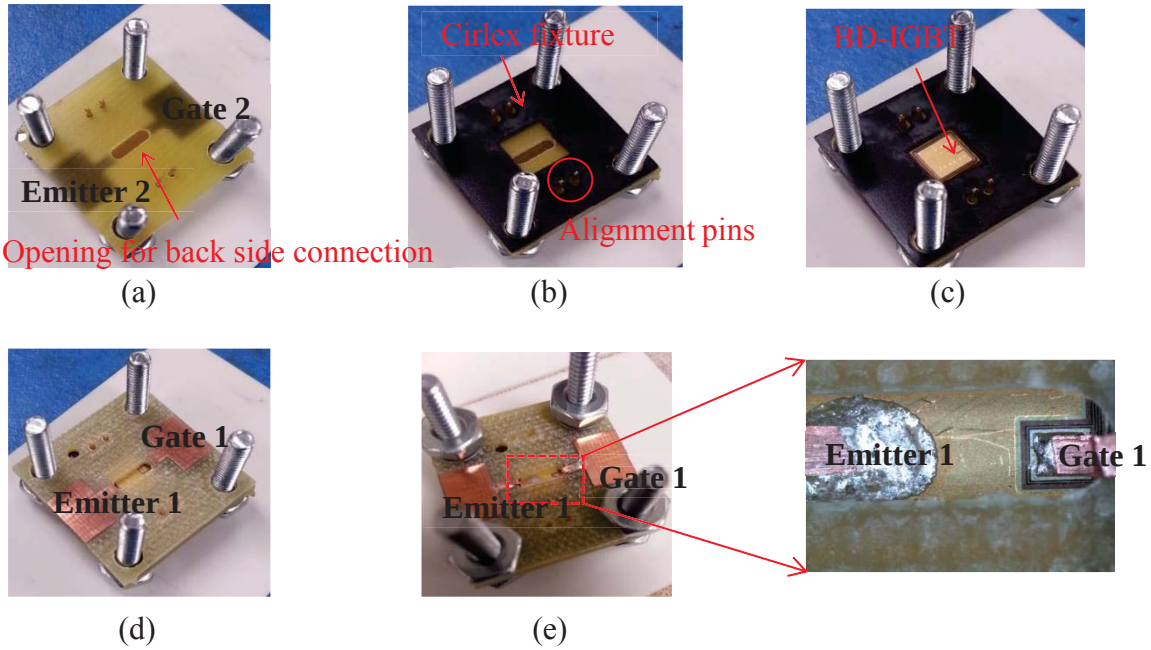


Figure A-1. Test fixture of the bidirectional die in Figure 2-23 for high current characterization.

The fixture consists of top and bottom PCBs and fixture layer in between. Figure A-1(a) shows the bottom PCB with four screws for alignment, and the center of the PCB has opening to exposure back side of die. The BD-IGBT is placed in the cavity of Cirlex fixture in (b), (c), and the top PCB is placed. Three-layer structure is clamped, and 0.7 mm width copper strips are

soldered to emitter and gate pads. Since top and bottom PCBs pressed the die and copper strips minimized thermo-mechanical stress, the chip could be characterized without delamination.

2. Test fixture for low current measurement

The test method in Appendix A.1 is suitable for high current die characterization, but the soldered strip makes the die unusable for module development. The test fixture in Figure A-3 was developed using components in Figure A-2 to test the die with pressure contact. The back side of the die makes contact to the bumps on the DBC substrate, and the extended copper patter makes contact to the measurement instruments. The top lid presses down the device for firm contact, and the cavity at the lid exposes the front side of the die for the measurement.

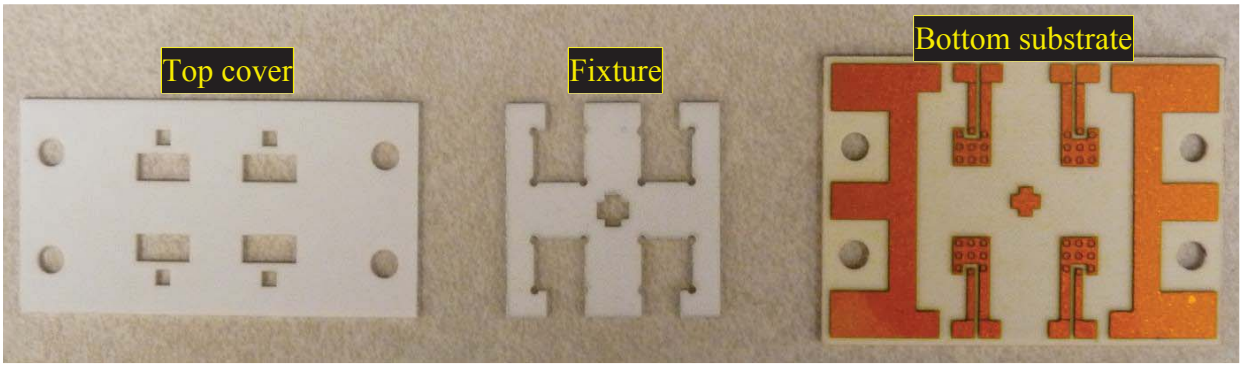


Figure A-2. Fabricated components for the test fixture in Figure A-3

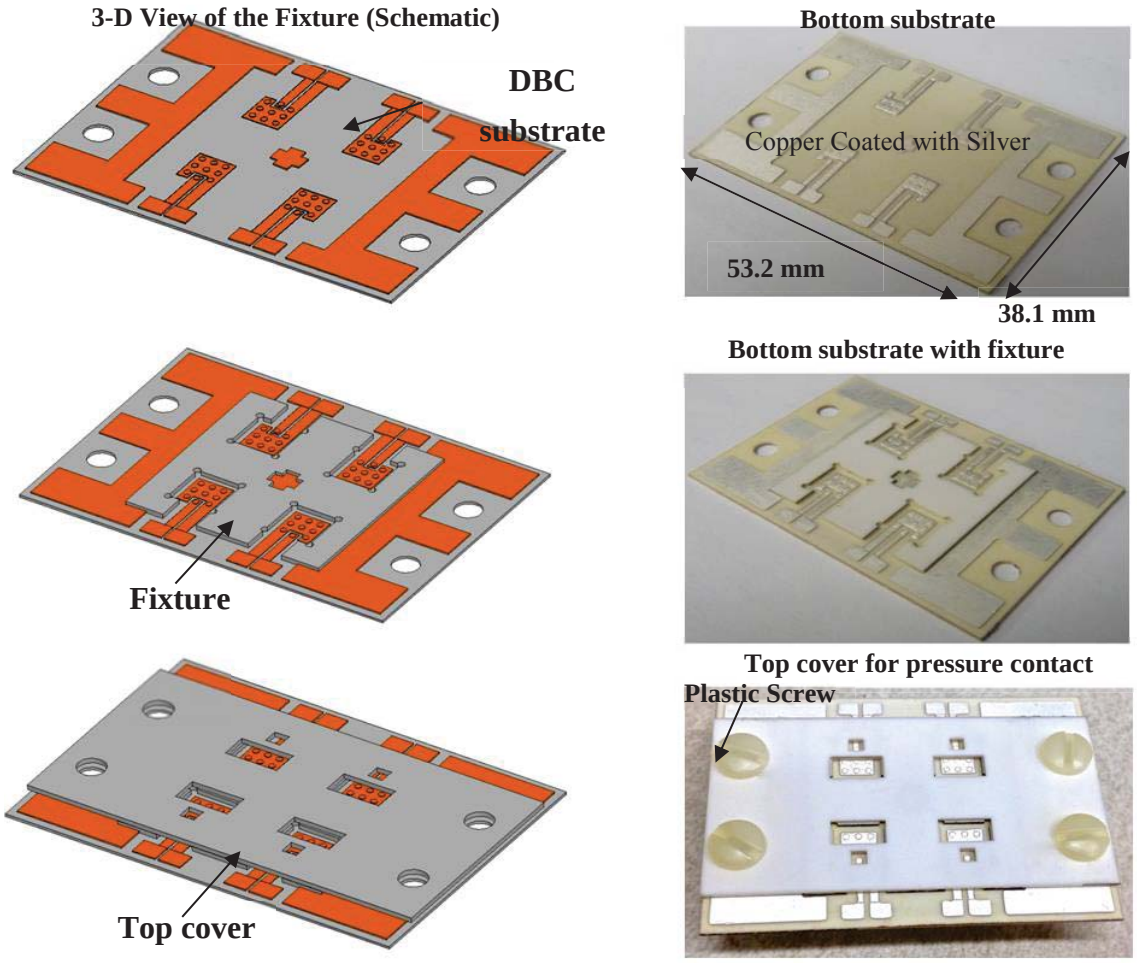


Figure A-3. Test fixture for the bidirectional IGBT for low current characterization.

Appendix B. SOFTWARE AND EQUIPMENT FOR THE MODULE FABRICATION

1. Design of the packaging components using AutoCAD

All packaging components such as DBC substrate, lead frame, and fixture can be fabricated using equipment in the packaging lab in CPES. Layouts in Figure B-1 to Figure B-5 are drawn in inch because the laser router in Figure B-6 uses inch as default unit. AutoCAD 2013 was used for all drawings, but the actual file was saved as 2004 version DWG format due to the compatibility with the Resonetics laser router. Figure B-1 shows the layout of the DBC substrate in Figure B-5 that contains one bidirectional IGBT and four posts. The minimum clearance between copper traces is kept above 0.5 mm to prevent solder overflow and ensure filling of the gap by molding compound.

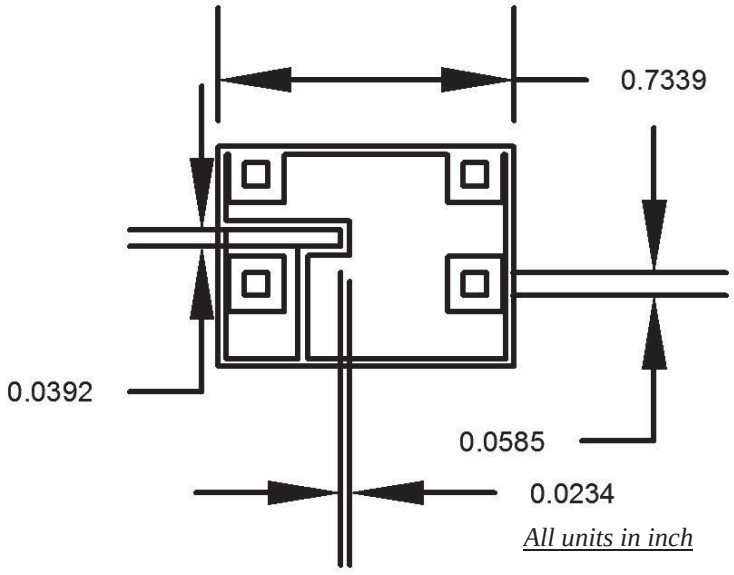
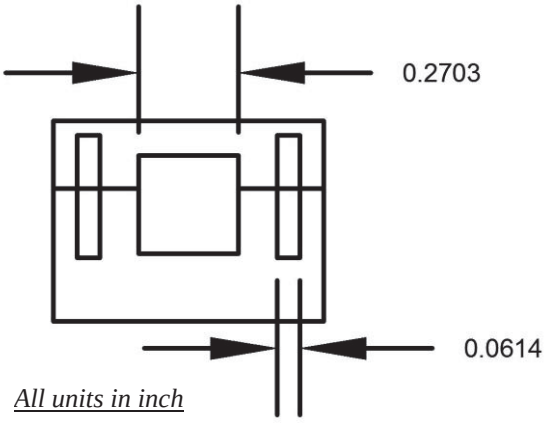
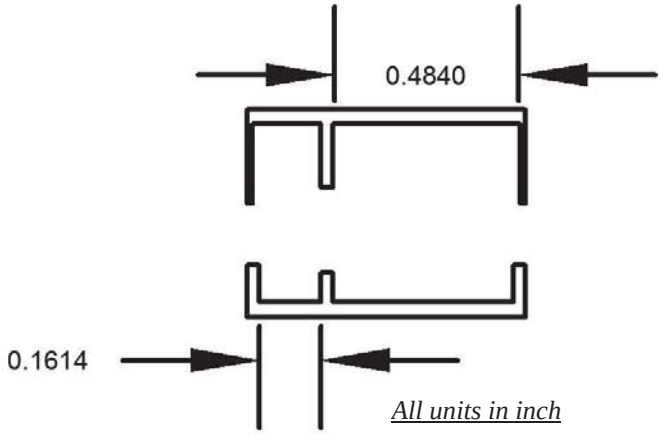


Figure B-1. DBC layout of the single-chip module in Figure 5-4 (see Table B.(19) for the original file).

Two layers of the Cirlex fixtures in Figure B-2 were designed to stabilize the packaging components during a reflow process. Since the fixture had to be removed after the reflow process, all fixtures were divided into two parts. The first fixture in Figure B-2(a) keeps the chip and solder preforms in position, and the fixture in (b) keeps the lead frame in position. Since the thickness of the solder preform was 0.2 mm and the chip thickness was 0.4 mm, 0.5 mm thick Cirlex was used to make fixtures.



(a)



(b)

Figure B-2. Layouts of the Cirlex fixtures for chip and solder preforms (a) and lead frame (b) (see Table B.(19) for the original files).

Figure B-3 shows the layout of the indented lead frame. At the design step of the lead frame, the folding of the leads had to be considered to get the precise alignment with DBC substrate and chip. The dashed boxes in Figure B-3 indicate the folding areas for the height compensation between DBC substrate and the top of the chip. In this case the length of lead was extended to compensate 0.8 mm height differences. The width and pitch of the lead were kept as 1 mm (0.0378 inch).

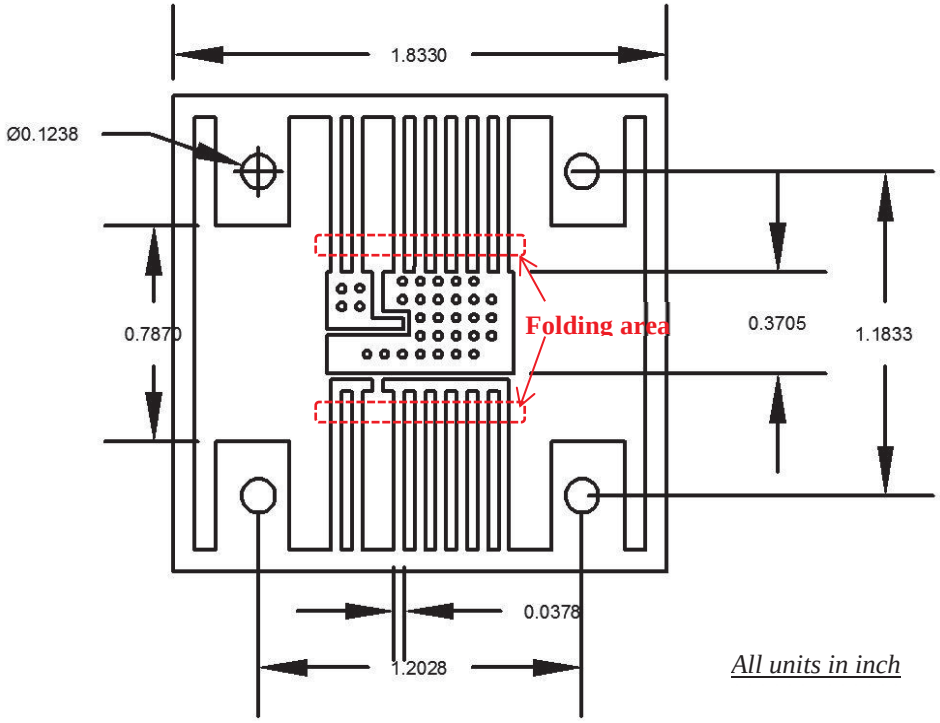


Figure B-3. Layout of the indented lead frame in Figure 5-4 (see Table B.(19) for the original file).

Finding consistent and repeatable process for the indented lead frame was important. The press mold in Figure 5-5(a) was developed using air-hardened steel to shape the lead frame. The press mold consists of top and bottom sides, and Figure B-4 and Figure B-5 show the layouts. Four pins are added for alignment with the copper lead frame, and patterns are designed to make multiple connections at the same time.

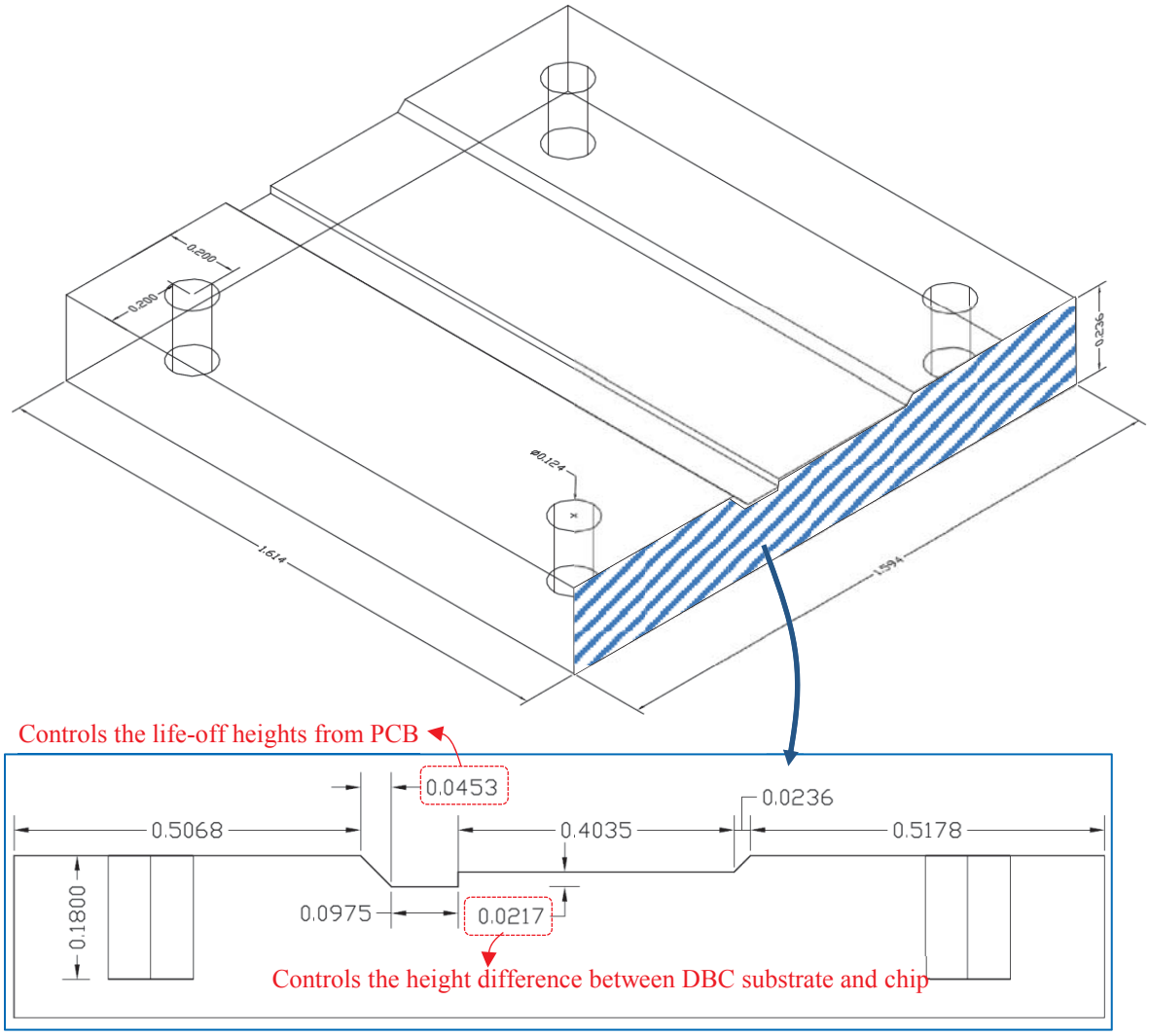


Figure B-4. Layout of the bottom mold in Figure 2-19.

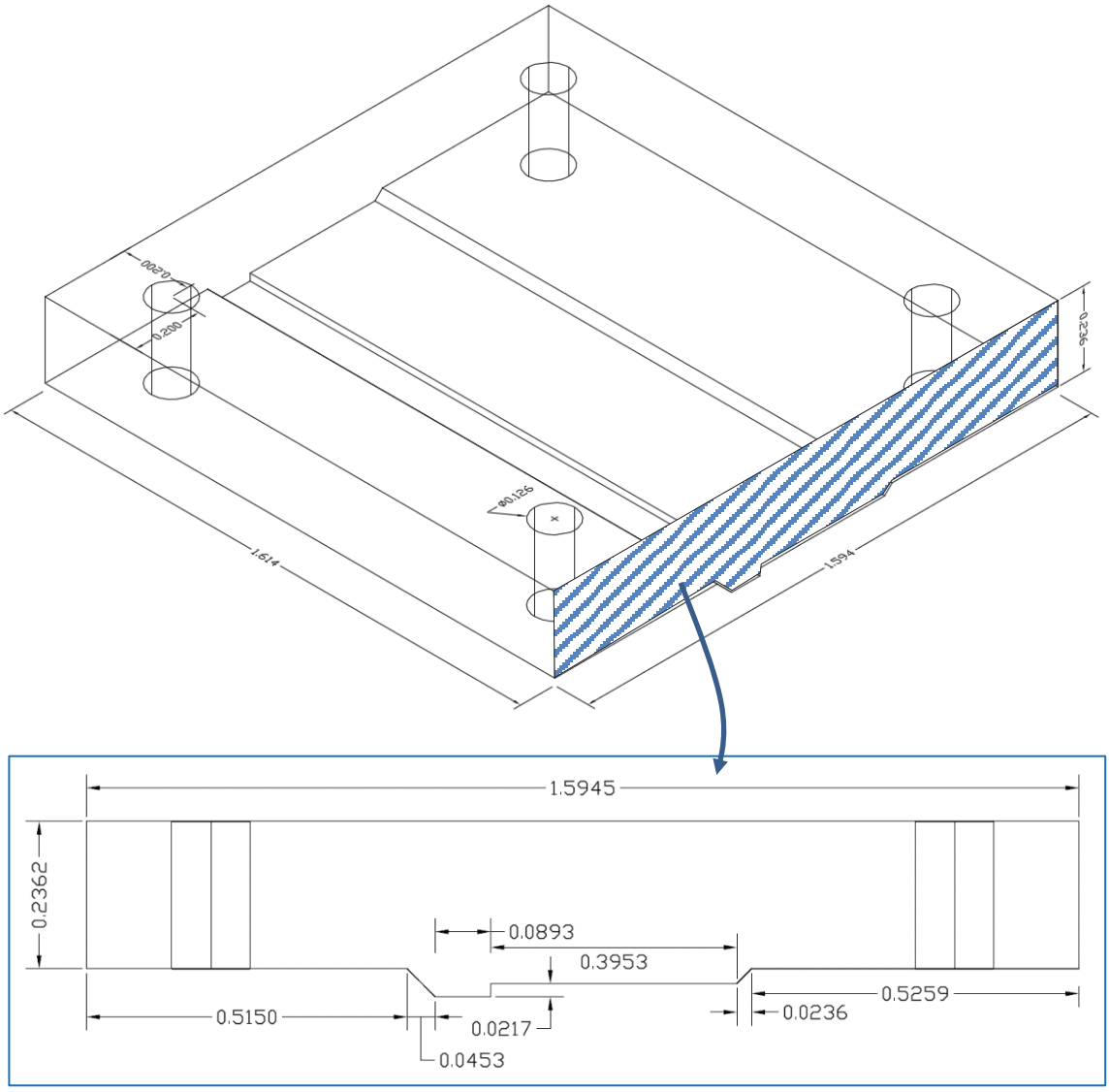


Figure B-5. Layout of the top mold in Figure 2-19.

2. Equipment for the module fabrication

The layouts of the DBC substrate, lead frame, and fixtures were processed using the laser router from Resonetics Micromachining in Figure B-6. Since each packaging material has different material and thicknesses, input parameter for each material has shown in Table B.1.

The given parameters are optimized to process the packaging materials in Table 4-2, and these parameters can be adjusted to process other materials.

Table B.1. Input parameters to route packaging components from Figure B-1 to Figure B-5

Input parameters	Kapton	Alumina (0.32 mm)	Cirlex (0.5 mm)	Cirlex (0.2 mm)
Stage lasing velocity (inch/s)	0.6	0.1	0.2	0.2
Stage slewing velocity (inch/s)	1	1	1	1
Pulse spacing (inch)	0.2	0.0006	0.0006	0.0006
Laser power (W)	6	150	40	20
Pulse number	15	300	150	70

Figure B-6. Laser routing system from Resonetics Micromachining.

A chemical etcher in Figure B-7 was used to pattern copper on DBC substrate and lead frame. To prevent partial etching, the substrate was 90^{o} rotated in every 5 minutes.

Figure B-7. Bench-top etching system from Kepro Circuit Systems (BTD-201B).

The prepared packaging components are assembled on a graphite boat for the vacuum reflow process. The vacuum reflow chamber in Figure B-8 applies current to the graphite boat to increase temperature, and the attached thermocouple at the side of graphite boat gives temperature signal to the controller so that the temperature of the graphite boat can be controlled as programmed. The soldering technique takes advantage of the pressure differential to eliminate voids. This method showed less than 5% voids for large-chip attachment (10 mm x 10 mm). This method can be explained by the Ideal Gas Law:

$$P_1V_1 = P_2V_2$$

P_1 and V_1 are initial pressure and volume of void, and P_2 and V_2 are final pressure and volume of final void. Solving the equation for final void volume, $V_2 = V_1 (P_1/P_2)$. Therefore, the greater is P2 in relation to P1, the more effective is the method.

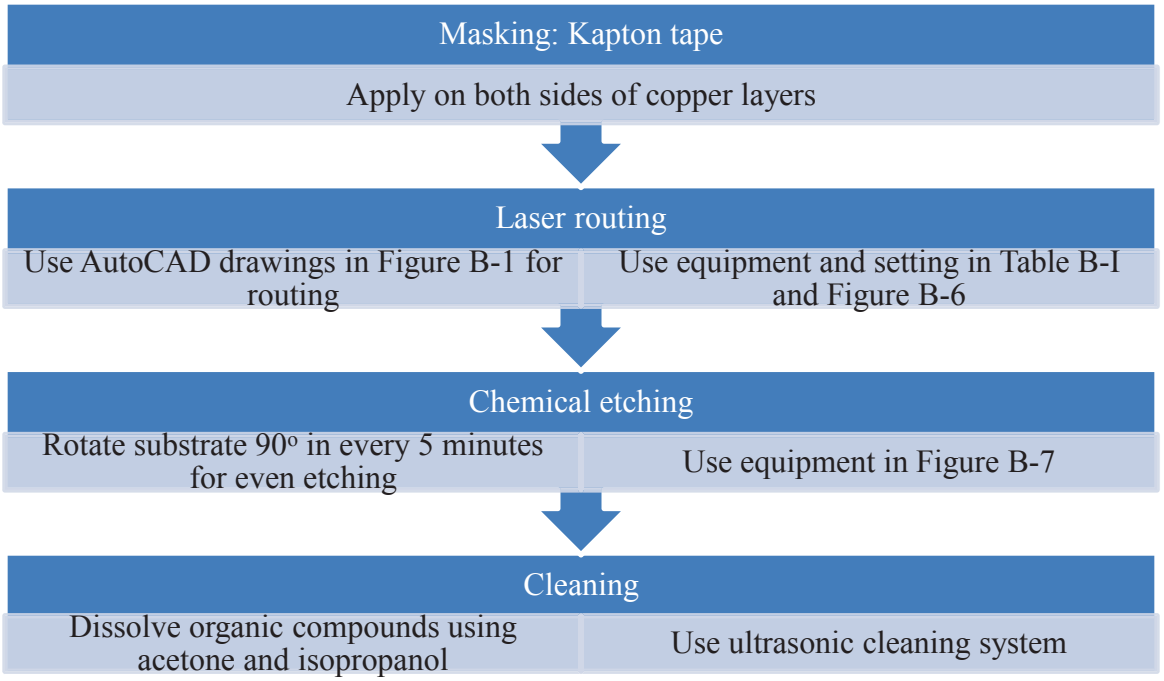
Figure B-8. Vacuum reflow chamber from SST (MV2200).

The assembled module after a vacuum reflow process should be encapsulated to protect module from mechanical loading, humidity, high electric field, etc. The pressure-controlled oven in Figure B-9 was used in this research. The low pressure in the chamber helps to remove trapped airs in the molding compound, and controlled temperature accelerates the curing of the material.

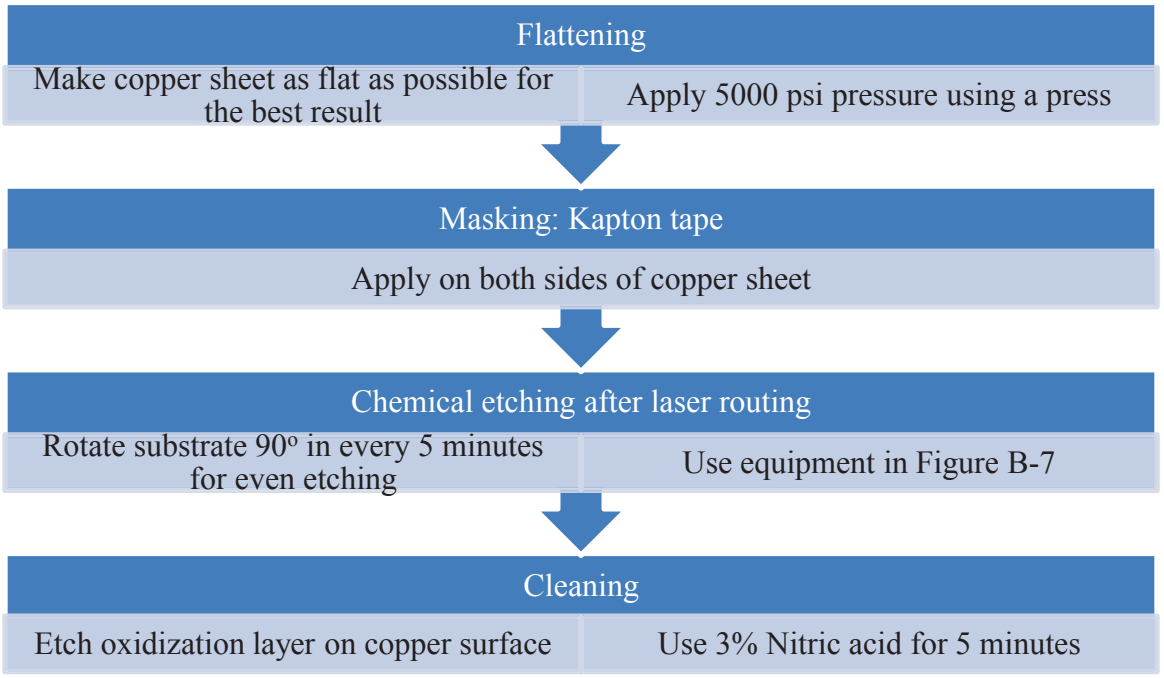
Figure B-9. Pressure-controlled environment chamber from Tenney for curing molding compounds.

3. *Steps for the fabrication of packaging components*

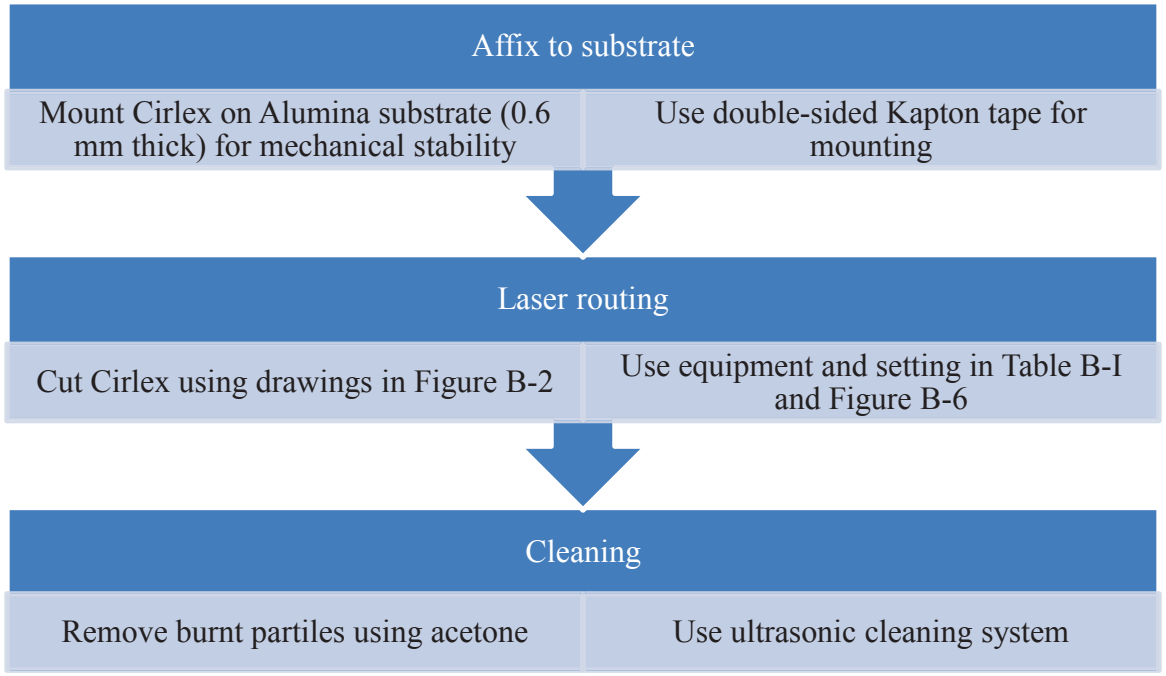
A. DBC substrate



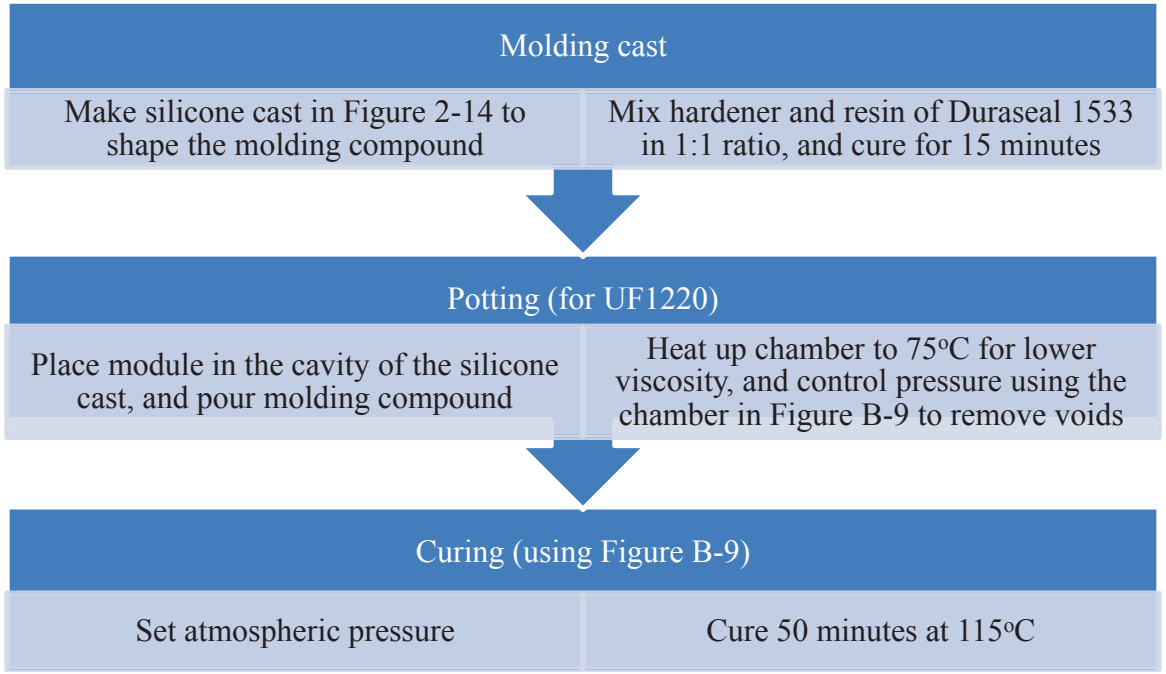
B. Lead frame



C. Cirlex fixture



D. Encapsulation using UF1220 (Curing profile varies for different materials)

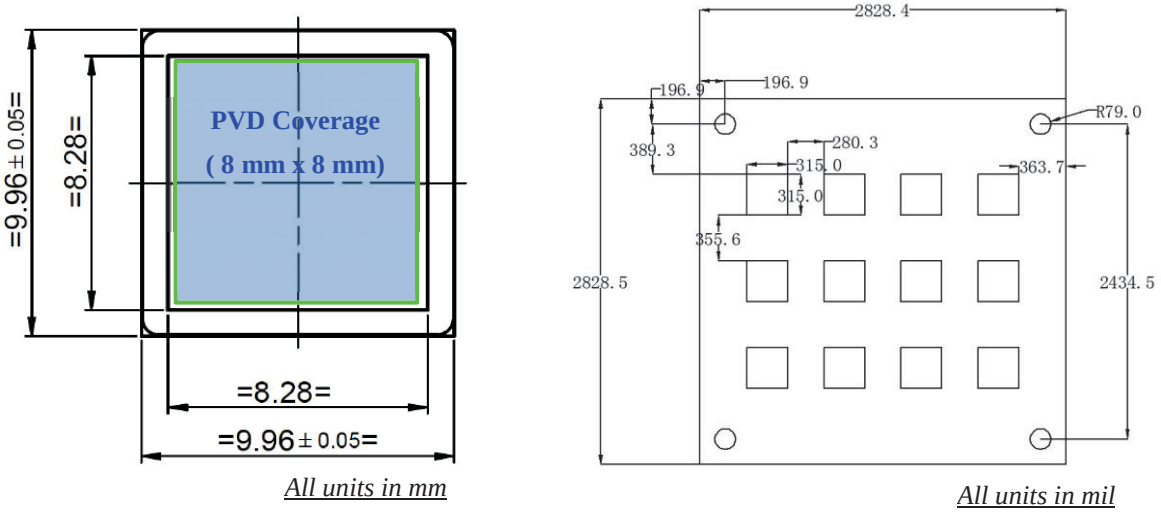


4. Physical-Vapor-Deposition (PVD) process for diode

The conventional power semiconductor such as the diode in Table 4-4 has Al metallization on top side which does not wet to solder. The applications such as the double-sided modules in Section 1.4 require the solderable layers for both front and back of the die. The fixture fabrication for PVD process and deposition steps are explained in this section.

A. Layout of the fixture

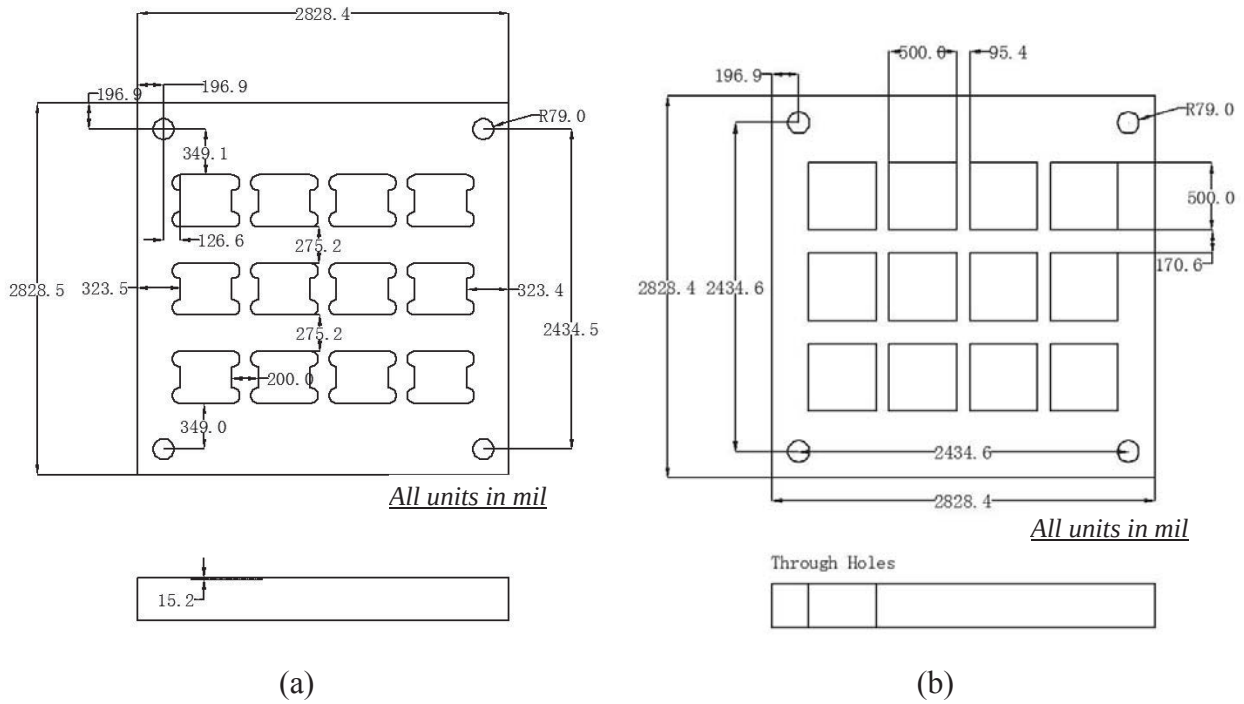
The thermal cycling samples in Figure 4-18 were fabricated using the diode in Table 4-4 that has Al layer at the front. Since then exposed metal area was 8.28 mm x 8.28 mm (Figure B-10(a)), the area for the metal deposition was controlled to be 8 mm x 8 mm. The stencil mask made of stainless steel in Figure B-10(b) has 8 mm x 8 mm (315 mil x 315 mil) openings.



(a) (b)

Figure B-10. Layout and mark of PVD area on the diode in Figure 4-18 (a); and the layout of the stencil mask with openings for the metal deposition (b) (see Table B.(22) for AutoCAD file).

In addition to the stencil mask in Figure B-10, top and bottom fixtures in Figure B-11 were designed to provide mechanical stability and alignment.



(a) (b)

Figure B-11. Layout of the bottom (a) and top (b) fixtures (see Table B.(22) for AutoCAD file).

The bottom fixture has 15.2 mil depth indentations to hold the devices under PVD, and the top fixture has through-hole openings for the front side of dice. The depth of indentation is determined to be 17% deeper than the thickness of die so that the die does not crack due to pressure of the top fixture.

B. PVD process with the fixture

Three metallization layers were deposited at the front side of die. Chromium (Cr) first deposited on the die which functions as barrier layer between Silicon (or Aluminum) and Nickel (Ni). The second layer was Ni that serves as actual soldering layer, and the third layer was Silver (Ag) layer that provides protection to Ni from the oxidization. The deposition rate was determined based on Langmuire-Knudsen Relation:

$$R_m = C_m \left(\frac{M}{T} \right)^{1/2} \cos\theta \cos\varphi \frac{1}{r} \left(P_e(T) - P \right) \tag{15}$$

where C_m is 1.85E-2; r is substrate-source distance (cm); T is source temperature (K); P_e is evaporant vapor pressure (torr); P is chamber pressure (torr); and M is evaporant gram-molecular mass (g). Table B. shows the parameters of deposition rates and final thicknesses.

Table B.2. PVD conditions for the deposition of Cr/Ni/Ag on the diode in Table 4-4

Layer	**Deposition order**	**Deposition rate**	**Final thickness**	**Function**
Cr	1	3 Å/s	150 nm	Barrier
Ni	2	5 Å/s	200 nm	Soldering
Ag	3	5 Å/s	250 nm	Protection

Figure B-12 shows the assembly steps of the PVD fixture. Prior to the assembly, diodes were cleaned using isopropanol and acetone to dissolve organic compounds. The cleaned diodes were placed in the cavities of the bottom fixture (b), and the stencil was placed on top of it with aid of alignment pins (c). The top fixture through hole was fixed on the stencil mask using screws (d), and placed on the PVD substrate (e). The PVD substrate is placed in the evaporation chamber, and processed using the profile in Table B..

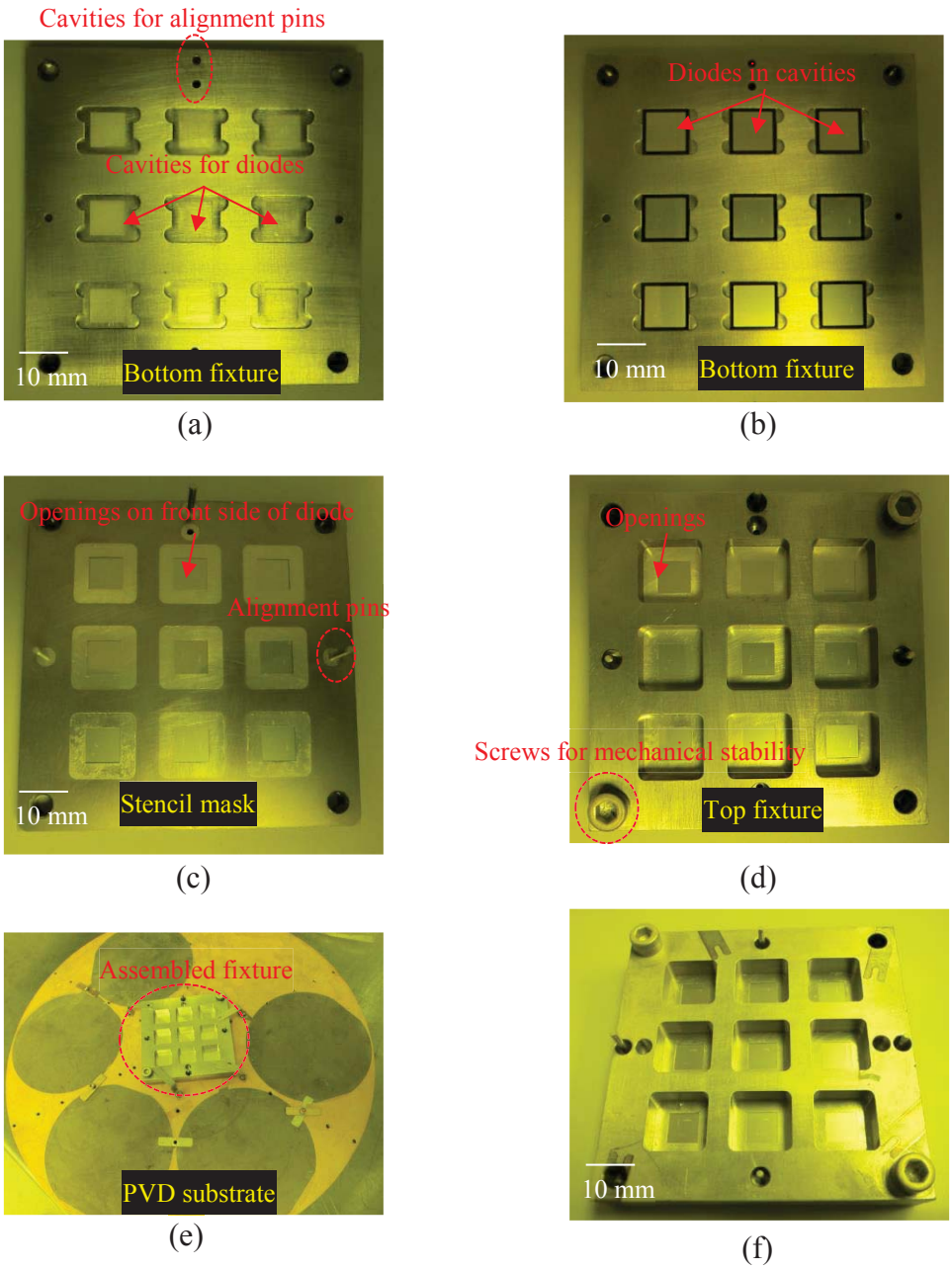


Figure B-12. Demonstration of PVD fabrication steps using the fixture made of stainless steel with layouts in Figure B-10 and Figure B-11. Bottom fixture with cavities for diodes in Table 4-4 (a); placed diodes in cavities (b); stencil mask to provide openings for PVD (c); top fixture with screws for mechanical stability (d); assembled fixture on the PVD substrate (e); and after PVD process (f).

Figure B- 13 shows the corner of the diode after the metal deposition. The yellow-dashed line indicates the edge of the deposition layer, and it can be seen that the passivation layer at the edge is not influenced by PVD process.

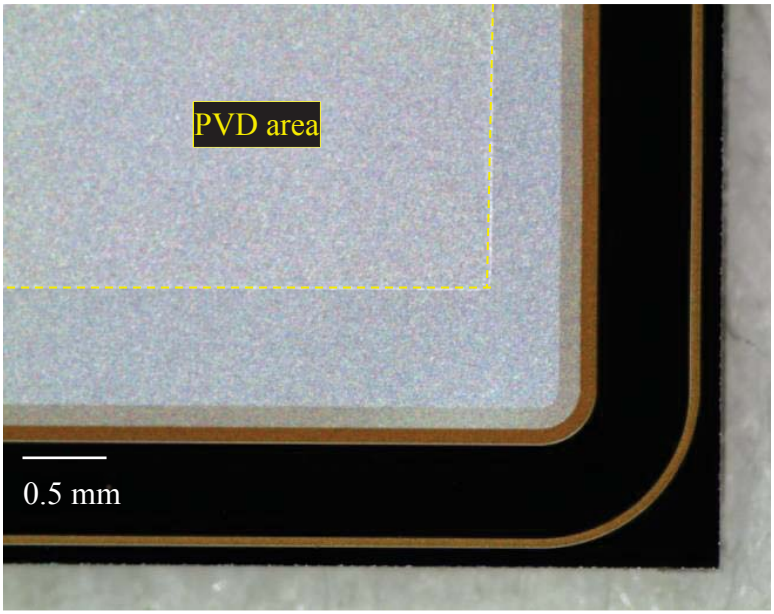


Figure B- 13. Zoomed in image of the PVD area after the process in Figure B-12.

5. Simulation tools and conditions

A. Directory of raw files for simulation or drawing of each figure

The original simulation files, AutoCAD layout, and BOM in this dissertation can be found at the //ADFS directories in Figure B-3.

Table B.3. Directory of raw files for each figure

List	Chapter	Type	Figure	Directory
1	2	ANSYS Mechanical	Figure 2-8	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\ANSYS\Chapter 2\Encapsulation

2	2	ANSYS Mechanical	Figure 2-20	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\ANSYS\Chapter 2\Indented lead frame
3	2	AutoCAD	Figure 2-23	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\AutoCAD\DBC substrate\Bidirectional module\Two chip module
4	2	AutoCAD	Figure 2-19	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\AutoCAD\Lead frame
5	2	BOM	Figure 2-23	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\BOM\Chapter 2 to 5_Module fabrication
6	2	ePhysics	Figure 2-18 Figure 2-22	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\ePhysics\Chapter 2_thermal resistance simulation
7	2	Maxwell	Figure 2-4 Figure 2-6 Figure 2-7	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\Maxwell\Chapter 2_electric field simulation
8	2	Q3D	Figure 2-16	\\adfs\projects\Khai

			Figure 2-17	Ngo\woochanKim\Dissertation_Files\Q3D\Chapter 2 and 5_package inductance
9	3	ANSYS Mechanical	Figure 3-2 Figure 3-4	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\ANSYS\Chapter 3
10	3	AutoCAD	Figure 3-13	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\AutoCAD\DBC substrate\Power cycling samples
11	3	BOM	Figure 3-16	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\BOM\Chapter 3_Power Cycling Board
12	3	ePhysics	Figure 3-9	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\ePhysics\Chapter 3_heat dissipation of hourglass joint
13	4	ANSYS Mechanical	Figure 4-8	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\ANSYS\Chapter 4
14	4	AutoCAD	Figure 4-15 Figure 4-16	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\AutoCAD\DBC substrate\Samples for curvature measurement
15	4	AutoCAD	Figure 4-18	\\adfs\projects\Khai

				Ngo\woochanKim\Dissertation_Files\AutoCAD\Power cycling samples
16	4	AutoCAD	Figure 4-18 Diode PVD stencil	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\AutoCAD\PVD fixture for diode
17	4	BOM	Figure 4-16 Figure 4-18 Figure 5-1	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\BOM\Chapter 2 to 5_Module fabrication
18	5	AutoCAD	Figure 5-1	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\AutoCAD\DBC substrate\Bidirectional module\Two chip module
19	5	AutoCAD	Figure 5-4	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\AutoCAD\DBC substrate\Bidirectional module\One chip module
20	5	AutoCAD	Figure 5-7	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\AutoCAD\DBC substrate\Benchmark module with 2IGBTs 2Diodes
21	3&4	Labview	Figure 3-16	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\Labview

22	B	AutoCAD	Figure B-10 Figure B-12	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\AutoCAD\PVD fixture for diode
23	C	Altium Designer	Figure C- 9 Figure C-10	\\adfs\projects\Khai Ngo\woochanKim\Dissertation_Files\Altium PCB Designer\Chapter 3_Power cycling board

B. Q3D Extractor and Maxwell

Q3D Extractor uses finite-element-method (FEM) to compute capacitance, inductance, and resistance matrices. The simulation models in 2.5 and 2.6 were analyzed to compute parasitic inductance and resistance of the designed module with solution setups in Figure B-14. Q3D provides selective solution such as capacitance and dc and ac resistance and inductance for circuit frequency range. In this study, the solution frequency was selected as 200 kHz, and dc resistance and ac inductance were analyzed as selected in Figure B-14.

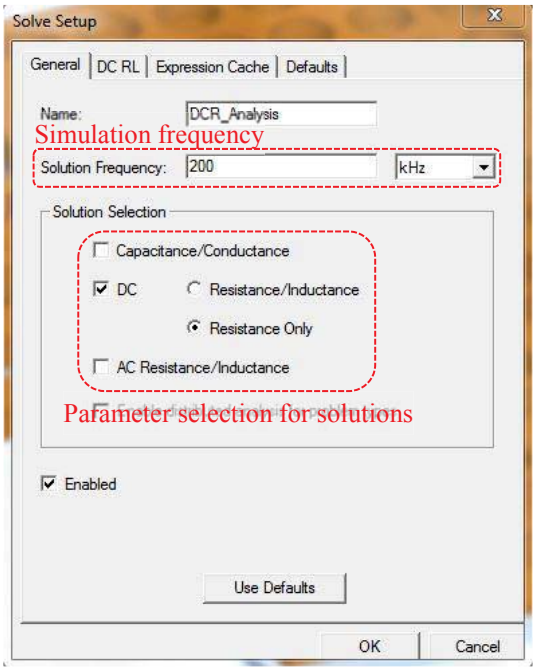
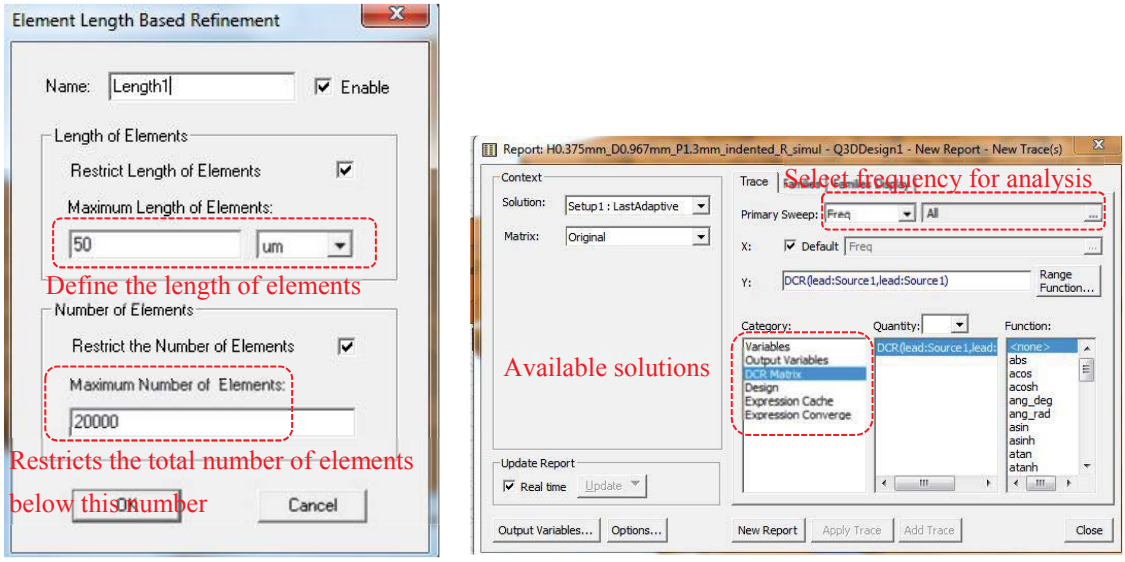


Figure B-14. Simulation setup for analysis of parasitic resistance and inductance.

It is important to assign proper mesh for the accurate simulation results. The adaptive meshing technique of ANSYS products uses a highly robust volumetric meshing and includes a multithreading capability that reduces the amount of memory used and speeds the simulation time. The element-length based mesh operation was used for this study (Figure B- 15(a)). Considering the thinnest layer was the solder layer (200 μm), the maximum length of the element was selected as 50 μm so that four layers of meshing elements could be generated. When the simulation is complete, the result can be either plotted or shown in matrix. In this study, the matrices were used to see the results (Figure B- 15(b)).



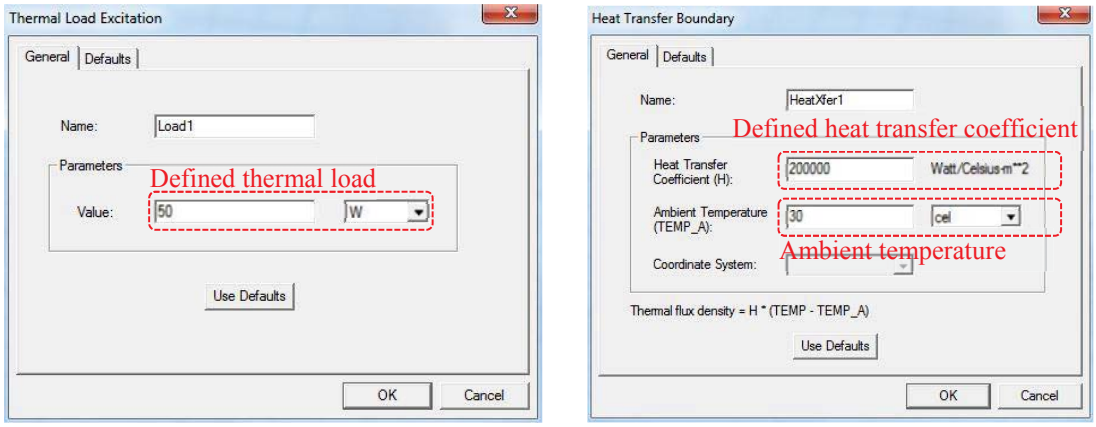
(a) (b)

Figure B- 15. Assigned mesh operation (a), and analysis of simulation results (b).

C. ePhysics thermal simulation

Thermal simulation is important to estimate and optimize the thermal characteristic of the module. Since ePhysics is one of the ANSYS products, the same simulation model for Q3D Extractor or Maxwell can be used for thermal simulation. The thermal load is determined based on the switching and conduction losses of the switch, and Figure B- 16(a) shows the thermal-load assignment for the simulation. Another important parameter is the boundary condition. The heat transfer coefficient was selected considering the convention thermal resistance (R_{th}=1/hA) in Figure B- 16(b). The heat transfer coefficient (h) used in this simulation was higher than conventional air or liquid cooling systems'. It is necessary to add the heat sink in the simulation to increase the area (A) so that the convection thermal resistance can be reduced. However, the addition of the heat sink significantly increases the simulation time.

Therefore, high heat transfer coefficient (h) was used to achieve the junction temperature below limit. The convection thermal resistance in this simulation can be used for the design of heat sink of the developed module.



(a) (b)

Figure B- 16. Assigned thermal load (a), and boundary condition (b) for the analysis.

Appendix C. DESIGN OF THE POWER-CYCLING SYSTEM

1. Relationship between gate-emitter voltage and junction temperature

Several properties of the IGBT are a function of the junction temperature [1]-[3]. As mentioned in [3], the gate-emitter voltage (V_{ge}) of silicon IGBT or the forward voltage (V_f) of diode are reliable temperature-sensitive parameters. The power cycling samples in this study (Figure 3-13 and Figure 4-18) packaged diodes. Thus, the forward voltage of the diode was used as a temperature sensitive parameter. Even though the power-cycling system in this chapter uses IGBT for cycling samples, the operating principles are the same for both devices.

The setup developed for power cycling uses the relationship between V_{ge} and junction temperature (T_j) to measure the junction temperature during the heating transients. The IGBT IRG4CH30K from International Rectifiers was characterized to obtain the relationship between V_{ge} and T_j at the collector current of 2 mA. The low collector current prevents the IGBT from self-heating.

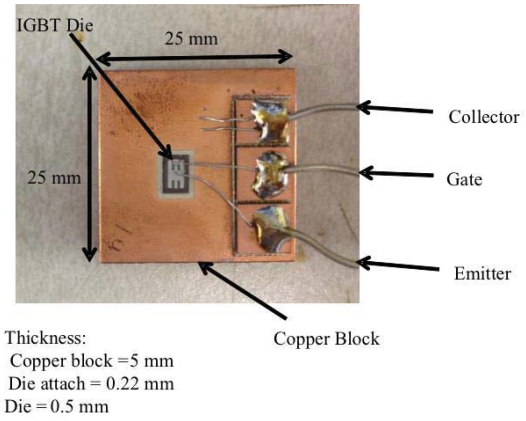


Figure C-1. IGBT die mounted on a copper block.

The IGBT die IRG4CH30K (3.5 mm x 5.5 mm x 0.5 mm) was mounted on a copper block (25 mm x 25 mm x 5 mm) using SN100C solder paste (0.22 mm thickness and 3.5 mm x 5.5 mm footprint area) for die- attach as seen in Figure C-1. The module was placed on a heating plate (SA-750 from OK Industries). A thermocouple (K-type) was attached to the copper block using Kapton tape very close (< 2 mm) to the IGBT to measure the junction temperature. A voltage source (Agilent E3631A) was connected between the collector and the emitter of the IGBT, and another voltage source was connected between the gate and the emitter terminals. The voltage source connected between the collector and the emitter terminals was set to 5 V. An ammeter was connected in series with the collector to measure the IGBT collector current. A voltmeter was connected between the gate and the emitter of the IGBT to measure V_{ge}. The schematic of the setup is shown in Figure C-2.

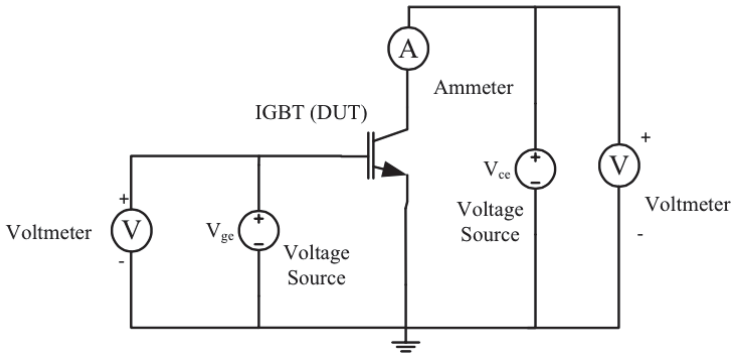


Figure C-2. Set-up for characterization of relationship between V_{ge} and T_j.

The voltage V_{ge} was gradually increased in steps such that the collector current is 2 mA. The temperature of the die was controlled by controlling the temperature of the hot plate. As the temperature of the IGBT die was increased, the collector current increased. To keep the collector current at 2 mA, V_{ge} had to be decreased accordingly. The temperature and the corresponding

gate-emitter voltage were recorded in steps, from 25°C to 100°C. Each measurement was taken after sufficiently long time (5-7 minutes) so that the temperature and V_{ge} have reached steady state.

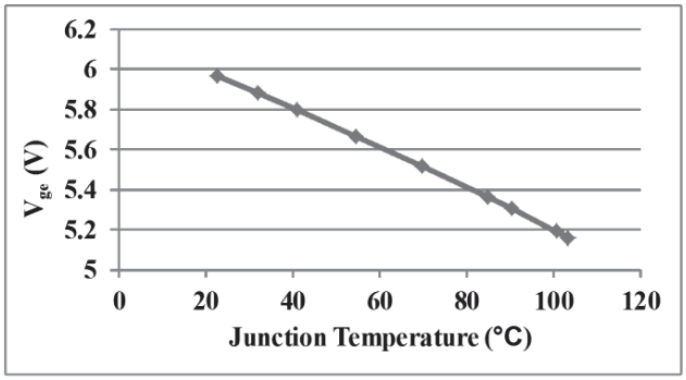


Figure C-3. Plot of relationship between V_{ge} and T_j for the IGBT die IRG4CH30K at I_{CE}=2 mA and V_{CE} =5 V (using setup in Figure C-2).

The measured relationship between V_{ge} and T_j is shown in Figure C-3. By linear curve fitting:

$$V_{ge} = -0.01 \cdot T_j + 6.2007 \cdot V \tag{16}$$

The preceding equation is employed in the setup for power cycling shown in Figure C-4 to determine T_j from measured V_{ge}.

2. Circuit and operation

The circuit for power cycling the IGBT consists of two control loops. The first control loop is for regulating the power. The power dissipated in the IGBT during heating is used to calculate Z_{th}. As seen in Figure C-4, there is a combination of resistances between the emitter terminal and ground. The equivalent resistance between the emitter terminal and ground is used for current-sensing and called R_{sense}.

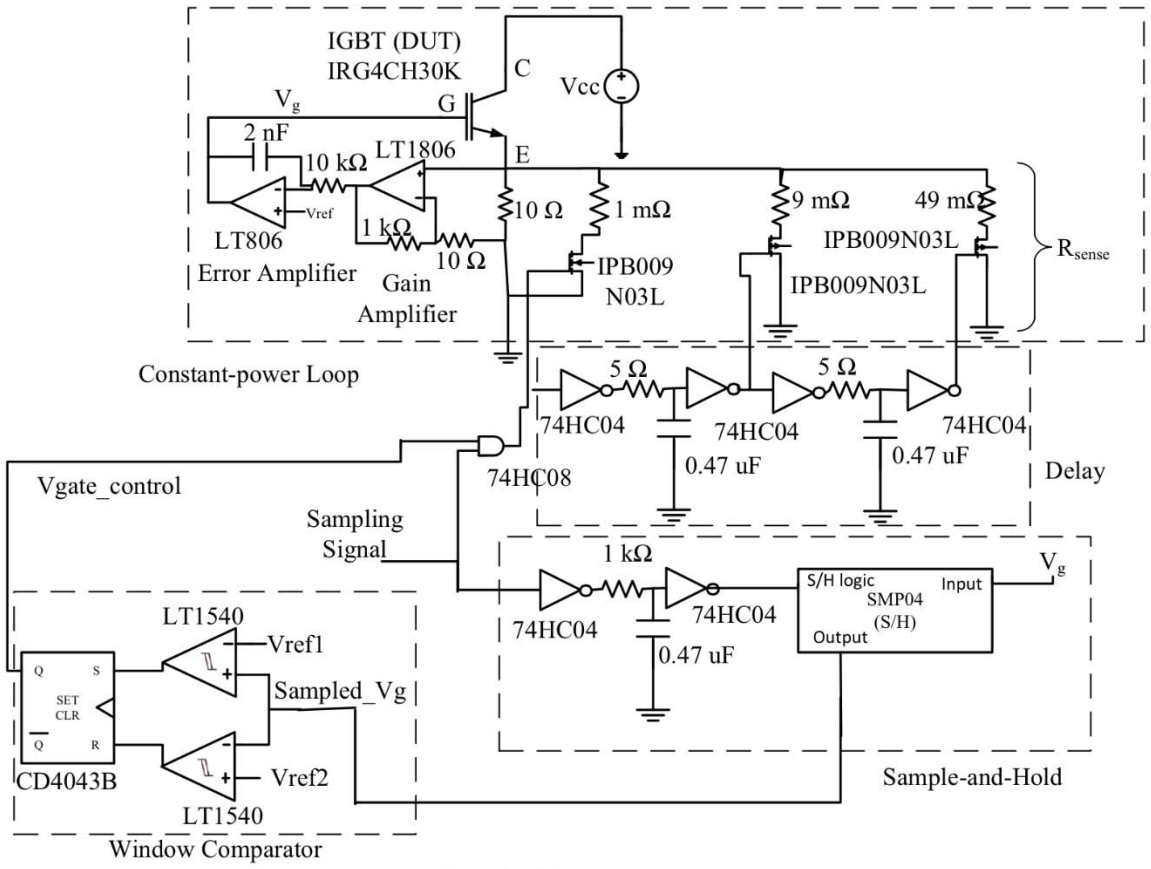


Figure C-4. Schematic of the power-cycling system.

The voltage sensed across R_{sense} is amplified by a gain amplifier providing a high gain ($G = 1+R_f / R_i = 101$), which is further given as an input to an operational amplifier in integrator configuration. The output of the integrator controls the gate voltage of the IGBT. The other input of the integrator comes from a fixed reference voltage of 2 V. The integrator acts as an error amplifier in the control loop. It compares the output of the gain amplifier with a 2 V reference voltage connected to its non-inverting terminal. The reference voltage is generated using a voltage reference IC LM4128. The closed loop works in such a way that the output of the gain amplifier is regulated at 2 V; which in turn regulates the voltage across the current-sense resistor R_{sense} to $2V / 101 \approx 20$ mV. Thus, the control loop works to keep the current through R_{sense} (and

hence, the current through IGBT (I_{CE})), constant. The voltage across the collector-emitter of the IGBT (V_{CE}) is maintained constant by the DC voltage source, connected to the collector of the IGBT. Since both V_{CE} and I_{CE} are constant (during heating phase, and during cooling phase separately), the power dissipated in the IGBT is constant during any particular phase, and is given by:

$$P_{IGBT} = V_{CE} I_{CE} \tag{17}$$

The current through the IGBT (I_{CE}) can be controlled by the resistance R_{sense}. The resistance R_{sense} is used to set the phase (heating or cooling) during power cycling. During the cooling phase, R_{sense} is set to 10 Ω to realize I_{CE} = 2 mA. During the heating phase, R_{sense} is set to 2 mΩ to realize I_{CE} = 10 A (heating power = 50W), sufficient enough to heat the die. Since I_{CE} needs to change between the high and the low value dynamically, R_{sense} is synthesized by paralleling a 10-Ω and a 2-mΩ resistor. The 2-mΩ resistance is realized by the series combination of a 1-mΩ resistor and the MOSFET IPB009N03L from Infineon with on-resistance 1 mΩ as shown in Figure C-4. Thus, whenever the MOSFET is on, the effective R_{sense} is 2 mΩ resulting in I_{CE} = 10 A. The 10-Ω resistor can be neglected when the MOSFET is on. Thus, the switching state of the MOSFET (on or off) controls the state of the IGBT (heating or cooling). As explained next, the state of the MOSFET is established by the second control loop.

The second control loop is the temperature cycling loop. The voltage V_{ge} is used as a parameter to sense the junction temperature (T_j) of the IGBT, and to set the temperature limits for power cycling. Since the emitter of the IGBT is maintained at a voltage of 20 mV, the gate

voltage V_g is used to represent the junction temperature, and the emitter voltage offset can be compensated by adding the 20 mV later. The gate voltage V_g is given as input to the window comparator circuit as observed in Figure C-4.

The externally controlled voltages V_{ref1} and V_{ref2} are used to control the temperature limits. They define the range for variation in Vge. For example, for the maximum temperature limit to be 100^{o}C, V_{ge} should be 5.200 V. Similarly, for the minimum junction temperature limit to be 25^{o}C, the corresponding V_{ge} can be calculated to be 5.950 V. If V_e is the emitter voltage, the voltage V_g is calculated from V_{ge} by:

$$V_g = V_{ge} + V_e \tag{18}$$

Thus, the limits for V_g are calculated, and are used as the threshold voltages V_{ref1} and V_{ref2}. Hence, V_{ref1} and V_{ref2} are set to 5.970 V and 5.220 V, respectively. The device CD4043B is used as a Set-Reset (SR) flip-flop. The output of the SR flip-flop remains in its last state (either high or low) until $V_{ref2} < V_g < V_{ref1}$. If the voltage V_g crosses the upper threshold (V_{ref1}), this indicates an "under-temperature" condition and the SR flip-flop output goes high so that heating phase begins. On the other hand, if the voltage V_g crosses the lower threshold (V_{ref2}) (over-temperature condition), the output of the SR flip-flop turns low so that cooling phase begins. The window comparator and the related logic circuit can be better understood by the sample waveforms for this sub-circuit shown in Figure C-5.

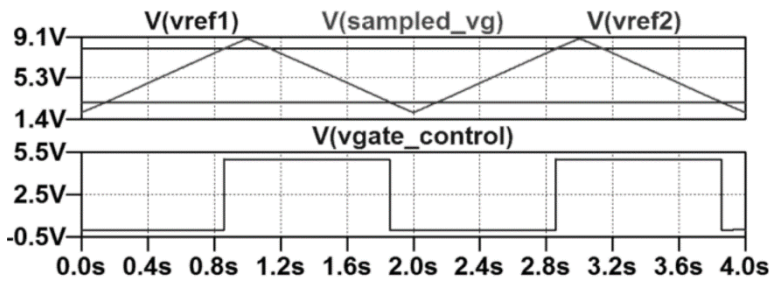


Figure C-5. Example of the window-comparator operation.

Since the relationship between V_{ge} and T_j is characterized for very low current (2 mA), (16) is valid only when the collector current is 2 mA. Thus, V_{ge} is an indication of the junction temperature only during the cooling phase. During the heating phase, V_{ge} is not related to T_j by (16). Hence, in order to sense the junction temperature correctly even during the heating phase, the IGBT current is periodically lowered to 2 mA for about 100 μs. The gate voltage is sampled during this time interval, stored in a "sample-and-hold" circuit, and employed by the window comparator in the temperature-cycling loop. A sampling signal is given to the sample-and-hold circuit. The sampling frequency is chosen based on the heating interval. It is important that the voltage V_{ge} is sampled sufficient number of times during the heating phase (or cooling phase) so that the phase change takes place at the specified temperature limits. The lower the sampling frequency, the higher is the probability of error in the sensed junction temperature during switching. We choose the sampling to take place every 6 ms, and hence, our sampling frequency is 166 Hz.

When the IGBT goes from high-current mode to low-current mode, the voltage V_{ge} is lowered, and is sampled by the sample-and-hold IC SMP04. The drop in the collector current causes a drop in the gate emitter voltage which results in undershoot at the gate voltage for a

small duration. This may introduce error in the recorded voltage V_g if sampled at that instant. The undershoot can be seen in Figure C-6 after time t = 0 ms. In order to avoid sampling of the ringing, a small delay is given to the logic signal for "sample-and- hold" IC such that it starts sampling the gate voltage at 300 μs after the cooling phase has started.

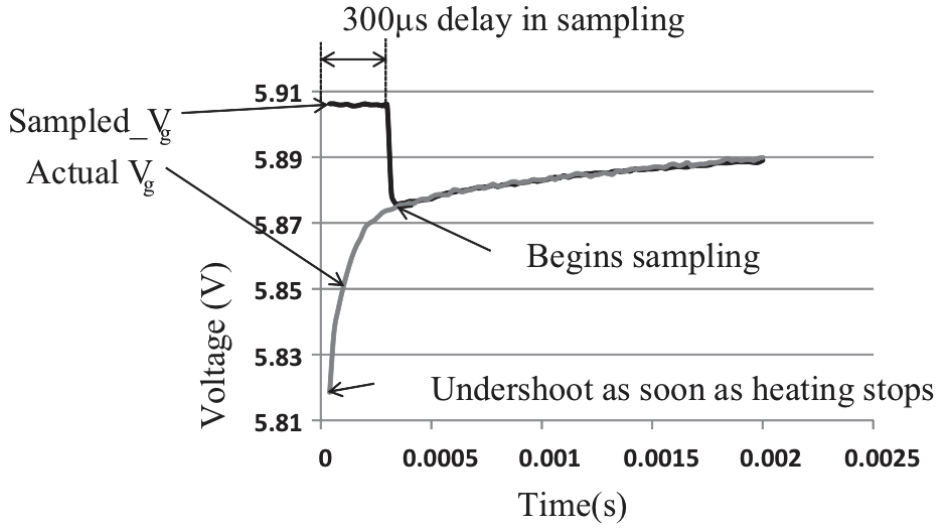


Figure C-6. Sampled V_g with the necessary delay (from the beginning of the cooling phase) to avoid sampling the undershoot.

Also, during the transition from heating phase to cooling phase, i.e., 10 A current to 2 mA current, there is an increase in the equivalent R_{sense} by 5000 times which can cause a voltage spike at the operational amplifier input terminal connected to R_{sense}. In order to assist the constant-current control loop to respond smoothly to the change, the resistance/current is increased/lowered in three steps, i.e., from 2 mΩ to 10 mΩ, 10 mΩ to 51 mΩ, and 51 mΩ to 10 Ω. The stepwise fall of current helps the control loop to respond smoothly during the transition from heating to cooling. The effective resistance R_{sense} controls the collector current through IGBT. The stepwise drop in the IGBT current is achieved by multiple sense resistors connected

in parallel with the 10-Ω resistor, and enabling them in the increasing order. Here, enabling the resistor means turning on the MOSFET in series with that resistor. The gate signals to these MOSFETs are connected in a daisy chain configuration with an RC circuit providing the necessary delay between each current step as observed in the schematic in Figure C-4.

3. Thermal impedance measurement

When power P dissipated in a layer of a specific material causes a temperature rise of ΔT, the thermal impedance of the layer is given by

$$Z_{th} = \frac{\Delta T_j}{P} \tag{19}$$

Since the relationship between the junction temperature and temperature sensitive parameter (K-factor in Figure 3-19), the change in junction temperature can be written as $\Delta T_j = \Delta V_{ge} / k$. Thus, (19) can be rewritten as

$$Z_{th} = \frac{\Delta V_{ge}}{kP} \tag{20}$$

When the diode die in a sample is heated, the heat transmits through the various layers of the module. Based on the amount of time the heat takes to travel through the different material layers, the plot of Z_{th} and different heating time intervals will indicate the thermal impedance of each layer.

In the power cycling setup mentioned in Appendix C.1, the heating phase is the period for which high current (10 A) flows through the IGBT. However, as explained, during the heating

phase, the collector current is periodically lowered (to 2 mA) for sensing the V_g. Since the heating is not continuous, there is a possibility of error in the Z_{th} measurement if there is any sensing during the heating pulse. Hence, the heating time without any interruption (sensing) is considered for the Z_{th} measurement. The time interval begins from the start of heating phase until the first time the collector current is lowered for sampling. The time interval can be easily controlled by controlling the frequency of the logic signal given to the "sample- and-hold" circuit. The sampling frequency is set to obtain the necessary heating duration. As an example, Figure C-7 shows the sampled V_g of the IGBT before heating and after the heating interval. The sampled V_g before heating and after the heating interval is captured and it appears as seen in Figure C-7.

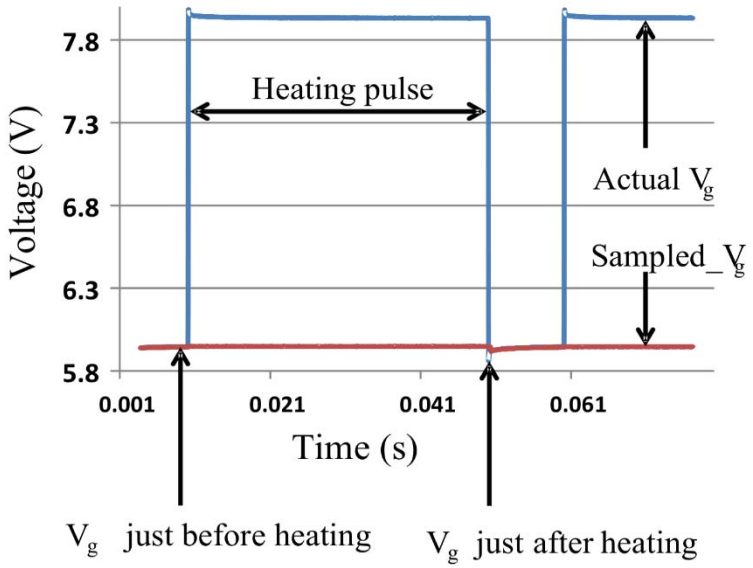


Figure C-7. Waveform of the gate voltage used for Z_{th} calculation.

Before starting the heating phase, the voltage V_g is maintained constant by the sample-and-hold IC in "hold" mode, during heating. It can be observed in Figure C-7 that before

time t = 0 s, the voltage V_g is constant. Average of the voltage V_g before t = 0 s over an interval of 10 ms is calculated and is called V_{g_i} or initial gate voltage. The point labeled as "V_g just after heating" in Figure C-7 is the voltage V_g immediately after the heating pulse ends. However, due to steep drop in V_g from the higher voltage, there could be an undershoot causing some ringing for a short duration. The ringing could cause error in the sensed "V_g just after heating". Hence, in order to avoid the error, the voltage V_g at t = 0 s shown in Figure C-7 needs to be extrapolated from the curve of the V_g after the heating pulse ends. A plot of V_g and $t^{1/2}$ is shown in Figure C-8, and is linear as expected in [1] and [4].

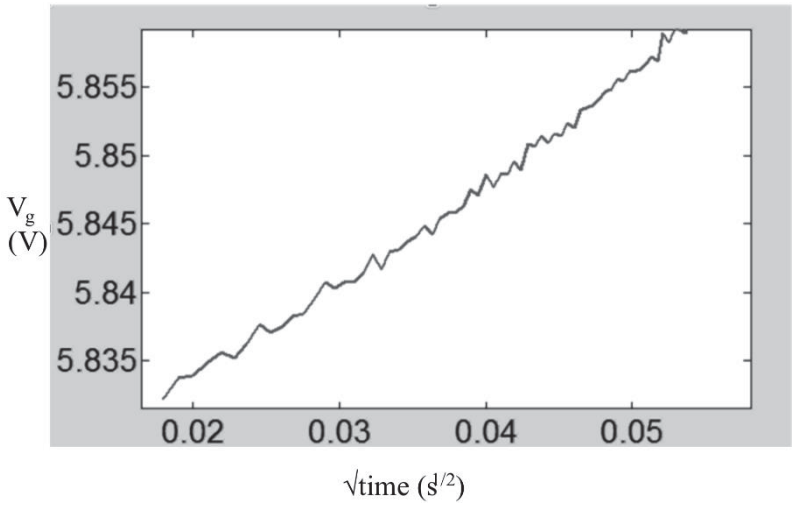


Figure C-8. Plot of V_g with $time^{1/2}$.

The relationship between V_g and t is extrapolated backwards using linear curve fitting to find the voltage V_g at t = 0 s (i.e., when the heating pulse is stopped), and is called V_{g_f} or the final gate voltage. Since the emitter of the IGBT is always regulated at 20 mV by the constant-current control loop, it can be stated that $\Delta V_{ge} = \Delta V_g$. Thus, (20) can be further simplified as:

$$Z_{th} = \frac{\Delta V_g}{kP} \tag{21}$$

Based on the method described in [5], the heat propagation times in the silicon die and in the copper block are around 2 ms and 280 ms, respectively. Therefore, for a module consisting of an IGBT die attached to a copper block by solder as die-attach, the maximum width of the heating pulse should be less than 280 ms to minimize the interference from any other materials exterior to the module. Also, the width of the heating pulse should be considerably higher than 2 ms to ensure that the heat has passed through the die-attach layer completely. For consistency of experimental conditions and in order to be able to compare the test results, 40 ms is chosen as duration of the heating pulse. This is same as the heating interval chosen in [5].

4. Layout of the power-cycling board

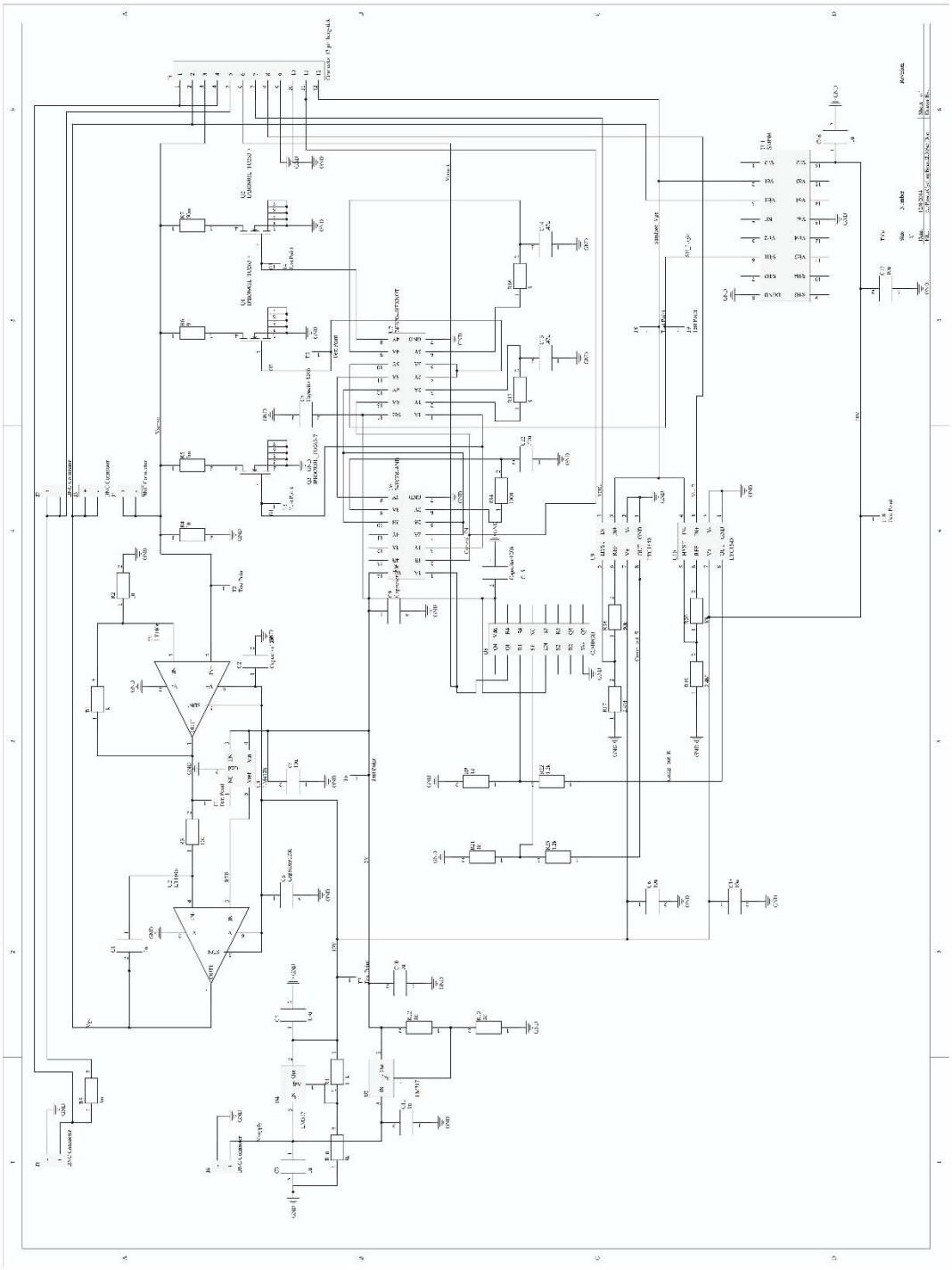
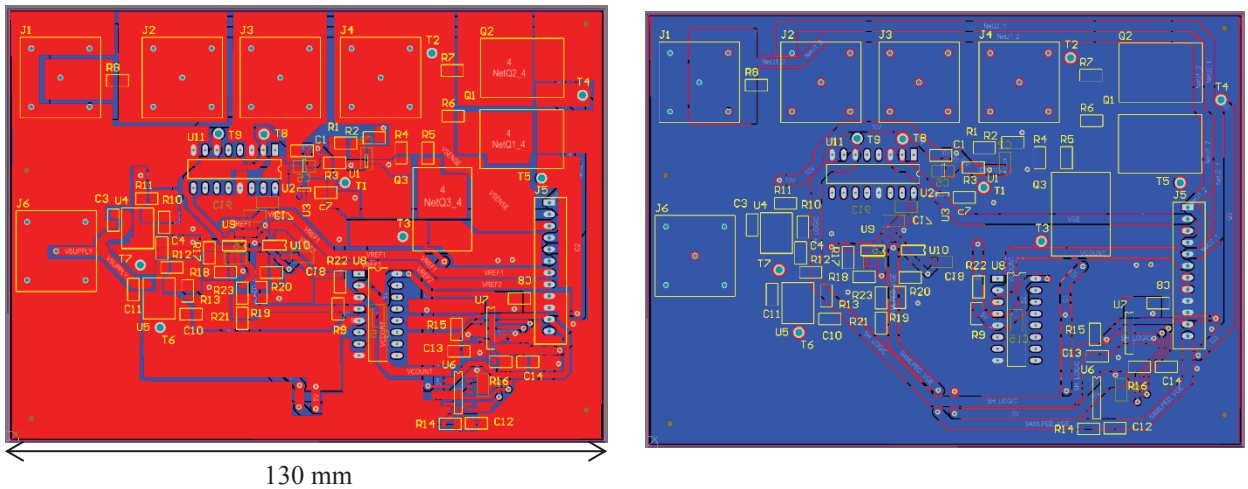


Figure C- 9. Complete schematic of the power-cycling system in Figure 3-16 for PCB design (see Table B.(23) for the original file).

Altium PCB designer was used for the schematic and PCB layout in Figure C- 9 and Figure C-10. The original design projects are saved at the directory in Table B.(23).



(a) (b)

Figure C-10. Layout of the power-cycling board; top layer (a) and bottom layer (b) (see Table B.(23) for the original file).

5. Experiment conditions for diode

The power cycling board in Figure C-4 was designed for the IGBT sample, but it can be used for diode as well using the forward voltage of diode as temperature-sensitive parameter. As shown in the Figure 3-16, the diode can be connected to the emitter of the IGBT, and the forward voltage (V_f) of diode can be sampled instead of V_g. By connecting additional diode samples in series with IGBT at the collector side, these diodes can see the same heating and cooling current as IGBT and reference diode at the emitter side of IGBT. As long as the power supply for V_{in} provides a sufficient power to IGBT, sensing resistors, and diodes in series, multiple diode samples can be cycled at the same time. The minimum V_{in} can be calculated as:

$$V_{in} = a \cdot V_f + V_{CE} + V_{R,sense} \tag{22}$$

where V_{in} is input voltage of power supply; V_f is on-state voltage drop of diode; V_{CE} is on-state voltage drop of IGBT; and $V_{R,sense}$ is voltage drop across the sensing resistor. The input voltage was calculated based on the voltage drops of each component. IGBT IRG4CH30K had 3.1 V drop; the diode in Table 4-4 had 1.3 V drop; and the sensing resistor had 20 mV drop. Therefore calculated V_{in} with the conditions is:

$$V_{in} = a \cdot V_f + V_{CE} + V_{R,sense} = 5 \cdot 0.32 \text{ V} + 3.1 \text{ V} + 0.02 \text{ V} = 4.72 \text{ V} \tag{23}$$

The complete list and condition of equipment are shown Table C.. To supply sufficient power, the input voltage was set to 5V, and current limit was set to 12 A. Another power supply for control ICs was set to 15 V input with 1 A current limit. Labview 2012 was used to set reference voltages for the window comparator in Figure C-4, and save sampled waveforms to a computer. The directory of Labview codes for the acquisition of sampled waveform, Zth analysis, and K-factor measurement are saved in Table B..

Table C.1. List of equipment and test conditions for the power-cycling system in Figure C-4

Equipment	**Part number**	**Function**	**Condition**
Power supply	Lambda UP6-132	Power supply for cycling devices	V_{in} = 5 V / I_{limit} = 12 A
Power supply	Agilent E3631A	Power supply for control ICs	V_{in} = 15 V/ I_{limit} = 1 A
DAQ	NI USB-6211	Connection between power-cycling board and computer	
Labview	Labview 2012	Sets reference voltages	V_{ref1} = 0.32 V / V_{ref2} = 0.15 V

6. References

[1]. Z. Jakopovic, Z. Bencic, and F. Kolonic, "Important properties of transient thermal impedance for MOS-gated power semiconductors," *in Proc. IEEE Int. Symp. Ind. Electron.*, Jul. 1999, vol. 2, pp. 574-578.

[2]. B. J. Baliga, "Fundamentals of Power Semiconductor Devices," New York: Springer-Verlag, 2008.

[3]. Xiao Cao, Tao Wang, Khai D T Ngo, and Guo-Quan Lu, "Characterization of lead-free solder and sintered nano-silver die-attach layers using thermal impedance", *IEEE Trans. Compon. Packag. and Manuf. Technol.*, vol. 1, no. 4, pp. 495-501, Apr. 2011.

[4]. H. Pappe, D. Schweitzer, J. H. Janssen, A. Morelli, and C. M. Villa, "Thermal transient modeling and experimental validation in the european project PROFIT," *IEEE Trans. Compo., Packag. and Manuf. Technol.,* vol. 27, no. 3, pp. 530-538, Sep. 2004.

[5]. X. Cao, K. D. T. Ngo, and G.-Q. Lu, "Thermal design of power module to minimize peak transient temperature," *in Proc. IEEE Int. Conf. Electron. Packag. Technol. and High Density Packag.,* Beijing,China, Aug. 2009, pp. 248-254.

Appendix D. TRANSIENT THERMO-MECHANICAL STRESS SIMULATION USING ANSYS 13

Solder joint fatigue models can be categorized into five categories: stress based, plastic-strain based, creep-strain based, energy based, and damage based. Among these empirical fatigue models, the energy-based model showed the highest accuracy than others. Since the accumulated plastic strain energy density is time-dependent parameter, the transient analysis of the model is required. This chapter introduces the step-by-step simulation procedure for the transient analysis. The simple structure consists of copper substrate, solder, and chip is used for the demonstration.

1. Drawing of the simulation model

It is recommended to define dimensions with parameters for the ease of structure modification. Figure D-1 shows the modeled structure using the code below:

```
/UNITS, SI    Change to SI unit
!DBC DIMENSION
CU_W=5E-3
CU_H=4.5E-3
CU_T=1.5E-3
!SOLDER DIMENSION
SOLDER_W=2E-3
SOLDER_T=0.05E-3
!CHIP
CHIP_W=2E-3
CHIP_T=0.29E-3
/PREP7      Go to pre-processor
!SUBSTRATE  Draw packaging components
BLOCK, 0, CU_W, 0, CU_H, 0, CU_T
BLOCK, 0, SOLDER_W, 0, SOLDER_W, CU_T, CU_T+SOLDER_T
BLOCK, 0, CHIP_W, 0, CHIP_W, CU_T+SOLDER_T,CU_T+SOLDER_T+CHIP_T
```

Define parameter and dimension

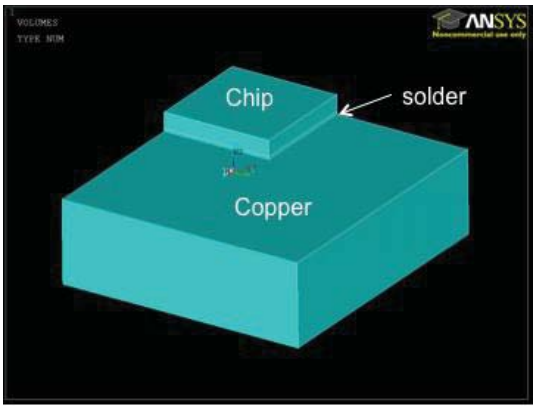


Figure D-1. Simulation model for the process demonstration.

2. Partition for the localized meshing

The partition of the simulation model is important to enhance the accuracy while keeping the reasonable simulation time. If the maximum stress region is known, the location can be partitioned into small segments that help to achieve finer meshes. Simulation models in Figure 3-2 are partitioned models for more accurate analysis at the edge of the joint. Figure D-2 shows the partitioned object of Figure D-1 using the code:

```
!PARTITION
WPOFF, SOLDER_W, SOLDER_W, CU_T
CSWPLA, 11, 0,1,1
WPROTA, 0, 90, 0
VSBW, ALL
WPOFF, 0,0, SOLDER_T/2
VSBW, ALL
WPOFF, 0,0, SOLDER_T
VSBW, ALL
WPOFF, 0,0, SOLDER_T
VSBW, ALL
WPOFF, 0,0, 2*SOLDER_T
VSBW, ALL
WPCSYS, -1
WPROTA, 0,0,-90
VSBW, ALL
WPOFF, 0,0, SOLDER_T/2
VSBW, ALL
WPOFF, 0,0, SOLDER_T
VSBW, ALL
WPOFF, 0,0, SOLDER_T
VSBW, ALL
WPOFF, 0,0, 2*SOLDER_T
VSBW, ALL
VGLUE, ALL
```

Define new coordinate

Partition process along xy plane

Glue all drawings

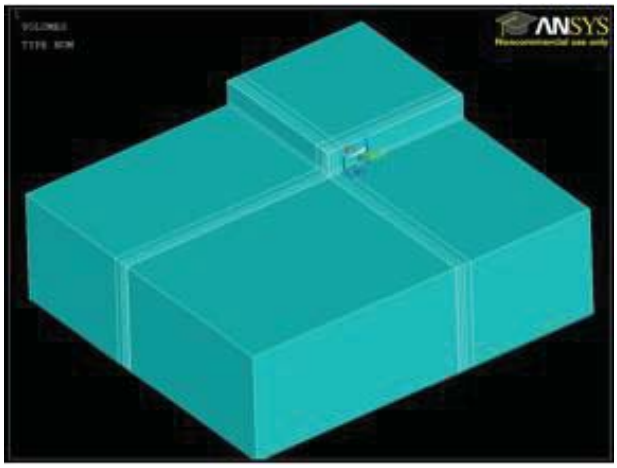


Figure D-2. Partitioned model of the structure in Figure D-1.

3. Assign material properties

The ductile materials, such as solder and copper, show plastic deformation under thermal loads. Anand model was used for the analysis of thermo-mechanical stress at solder layer. More details about theory are explained in 3.2.1. The element for each material was selected based on the degree-of-freedom, material properties, and special features. For example, SOLID 187 is defined by 10 nodes having three degrees of freedom at each node. According to the manual of ANSYS, the element has plasticity hyper-elasticity, creep, stress stiffening, large deflection, and large strain capabilities. According to these specifications, the element was used for the modeling of copper. In the same manner, VISCO 107 is used for solder because it can import Anand constitution model that emulates plastic behavior of the solder. Figure D-3 shows the model after material assignments using code:

```
!MATERIAL PROPERTIES

!ASSIGN ELEMENTS AND MATERIALS PROPERTIES
!ADD ELEMENT

ET,1,SOLID187
ET,2,VISCO107
ET,3,SOLID185

!MATERIALS

!MATERIAL 1: AL2O3
!MATERIAL 2: SOLDER
!MATERIAL 3: CU
!MATERIAL 4: SILICON
!MATERIAL 5: EPOXY

!MATERIAL 1: AL2O3
MPTEMP,R5.0, 1, 1,    0.00000000       ,
MPDATA,R5.0, 1,EX    ,1      , 1, 3.00000000E+11,
MPTEMP,R5.0, 1, 1,    0.00000000       ,
MPDATA,R5.0, 1,DENS,1      , 1,    3690.00000       ,
MPTEMP,R5.0, 1, 1,    0.00000000       ,
MPDATA,R5.0, 1,KXX ,1      , 1,    30.000000        ,
MPTEMP,R5.0, 1, 1,    0.00000000       ,
MPDATA,R5.0, 1,PRXY,1      , 1, 0.210000000       ,
MPTEMP,R5.0, 1, 1,    0.00000000       ,
MPDATA,R5.0, 1,REFT,1      , 1,    25.0000000       ,
MPTEMP,R5.0, 1, 1,    0.00000000       ,
MPDATA,R5.0, 1,CTEX,1      , 1, 8.100000000E-06,
```

Define element types for simulation

Assign number for each material

Define material properties of alumina

```
!MATERIAL 2 SOLDER
MPTEMP,R5.0, 2, 1, -40.0000000      ,    105.000000      ,
MPDATA,R5.0, 2,EX    ,2     , 1, 5.640000000E+10, 4.570000000E+10,
MPTEMP,R5.0, 2, 1, -40.0000000      ,    105.000000      ,
MPDATA,R5.0, 2,NUXY,2     , 1, 0.336000000      , 0.363000000      ,
MPTEMP,R5.0, 3, 1, -40.0000000      ,    25.0000000      ,    105.000000
MPDATA,R5.0, 3,ALPX,2     , 1, 1.961896552E-05, 2.053793103E-05, 2.166896552E-05
MPTEMP,R5.0, 1, 1,    0.00000000      ,
MPDATA,R5.0, 1,DENS,2     , 1,    7400.00000      ,
MPTEMP,R5.0, 1, 1,    0.00000000      ,
MPDATA,R5.0, 1,KXX ,2     , 1,    64.0000000      ,
MPTEMP,R5.0, 2, 1, -40.0000000      ,    105.000000      ,
MPDATA,R5.0, 2,PRXY,2     , 1, 0.336000000      , 0.363000000      ,
MPTEMP,R5.0, 2, 1, -40.0000000      ,    105.000000      ,
MPDATA,R5.0, 2,CTEX,2     , 1, 1.870000000E-05, 2.280000000E-05,
TB,ANAN,2
TBDAT,     1,    2450000.00      ,    6067.25238      ,    717.260000
TBDAT,     4,    2.00000000      , 0.130000000      , 1.456000000E+10
TBDAT,     7,    29000000.0      , 4.360000000E-02,    2.22000000
```

Define material properties of solder

Define ANAND model

```
!MATERIAL 3: COPPER
MPTEMP,R5.0, 1, 1,  0.00000000      ,
MPDATA,R5.0, 1,EX   ,3     , 1, 1.230000000E+11,
MPTEMP,R5.0, 1, 1,  0.00000000      ,
MPDATA,R5.0, 1,NUXY,3      , 1, 0.340000000      ,
MPTEMP,R5.0, 3, 1, -40.0000000      ,  25.0000000      ,  105.000000
MPDATA,R5.0, 3,ALPX,3      , 1, 1.653448276E-05, 1.666896552E-05, 1.683448276E-05
MPTEMP,R5.0, 1, 1,  0.00000000      ,
MPDATA,R5.0, 1,DENS,3      , 1,  8960.00000      ,
MPTEMP,R5.0, 1, 1,  0.00000000      ,
MPDATA,R5.0, 1,KXX ,3      , 1,  385.000000      ,
MPTEMP,R5.0, 1, 1,  0.00000000      ,
MPDATA,R5.0, 1,C    ,3     , 1,  380.000000      ,
MPTEMP,R5.0, 1, 1,  0.00000000      ,
MPDATA,R5.0, 1,PRXY,3      , 1, 0.340000000      ,
MPTEMP,R5.0, 2, 1, -40.0000000      ,  105.000000      ,
MPDATA,R5.0, 2,CTEX,3      , 1, 1.640000000E-05, 1.700000000E-05,
TB,MISO,3     ,     1,  30
TBTEM,  0.00000000      ,     1
TBPT,, 3.571000000E-04,  43891000.0
TBPT,, 4.001000000E-04,  45185000.0
TBPT,, 5.001000000E-04,  47837000.0
TBPT,, 6.002000000E-04,  50118000.0
TBPT,, 7.002000000E-04,  52130000.0
TBPT,, 8.003000000E-04,  53937000.0
TBPT,, 9.004000000E-04,  55583000.0
TBPT,, 1.001000000E-03,  57097000.0
TBPT,, 2.061000000E-03,  68619000.0
TBPT,, 3.005000000E-03,  75489000.0
TBPT,, 4.008000000E-03,  81177000.0
TBPT,, 5.013000000E-03,  85864000.0
TBPT,, 6.018000000E-03,  89876000.0
…
TBPT,, 0.105200000      ,  168120000.
TBPT,, 0.221400000      ,  181660000.
TBPT,, 0.349900000      ,  182350000.
TBPT,, 0.491800000      ,  185610000.
TBPT,, 0.648700000      ,  187150000.
```

Define material properties of copper

Define stress vs. strain curve

```
!MATERIAL 4: SILICON
MPTEMP,R5.0, 2, 1, -40.0000000      ,   105.000000      ,
MPDATA,R5.0, 2,EX    ,4     , 1, 1.640000000E+11, 1.620000000E+11,
MPTEMP,R5.0, 1, 1,   0.00000000     ,
MPDATA,R5.0, 1,DENS,4     , 1,   2330.00000      ,
MPTEMP,R5.0, 1, 1,   0.00000000     ,
MPDATA,R5.0, 1,KXX ,4     , 1,   149.000000      ,
MPTEMP,R5.0, 2, 1, -40.0000000      ,   105.000000      ,
MPDATA,R5.0, 2,PRXY,4     , 1, 0.220000000      , 0.220000000      ,
MPTEMP,R5.0, 2, 1, -40.0000000      ,   105.000000      ,
MPDATA,R5.0, 2,CTEX,4     , 1, 2.250000000E-06, 2.820000000E-06,
```

Define material properties of silicon

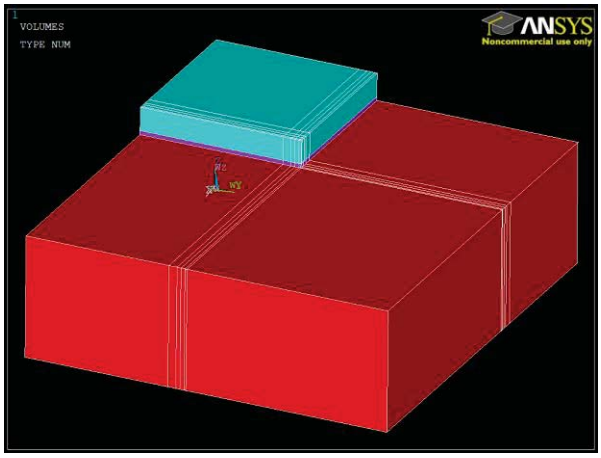
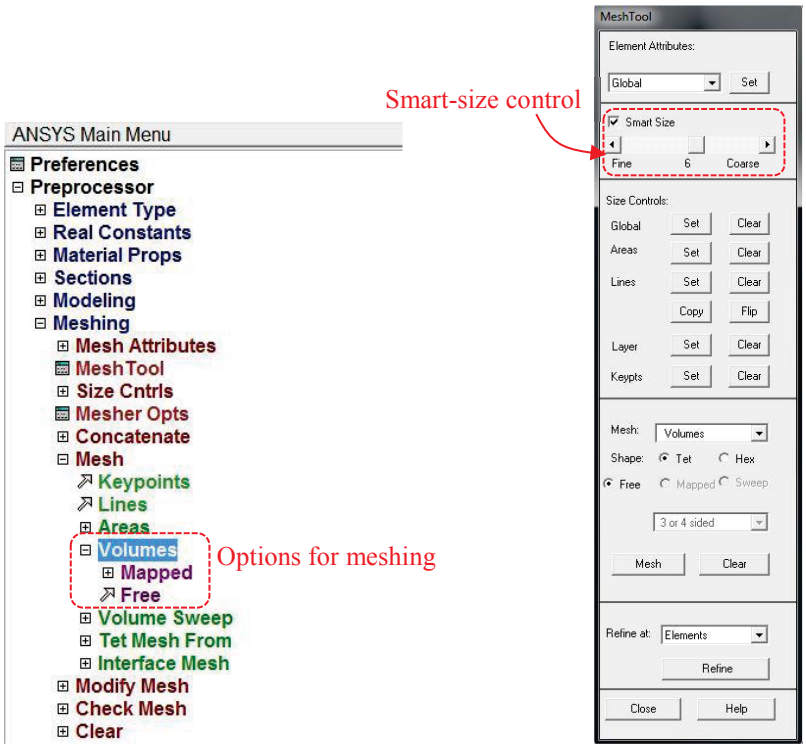


Figure D-3. Simulation model after material assignment.

3. Meshing

ANSYS provides free and mapped meshing tools. A free mesh does not restrict the shape of the element and pattern is also random. The structure in Figure D-5 shows the example of the free mesh. This method is easy and flexible to many different shapes of the model. However, the internal angle of the element tends to be shaped smaller than the tolerance, which results in

inaccurate simulation result. To prevent this problem, it is recommended to use smart-sizing tool in Figure D-4(b) that controls the shape of each element within the tolerance. A mapped-volume-mesh constrains the shape of the element as hexahedron only. For this reason, a mapped mesh has regular mesh distributions that give more accurate simulation results than free mesh. However, this method is highly influenced by the shape of the simulation model that requires regular volumes and connections among them. Meshed simulation models in Figure 3-2 shows the example of the mapped mesh.



(a) (b)

Figure D-4. ANSYS menu for volumetric meshing (a) and the window of the smart meshing tool (b).

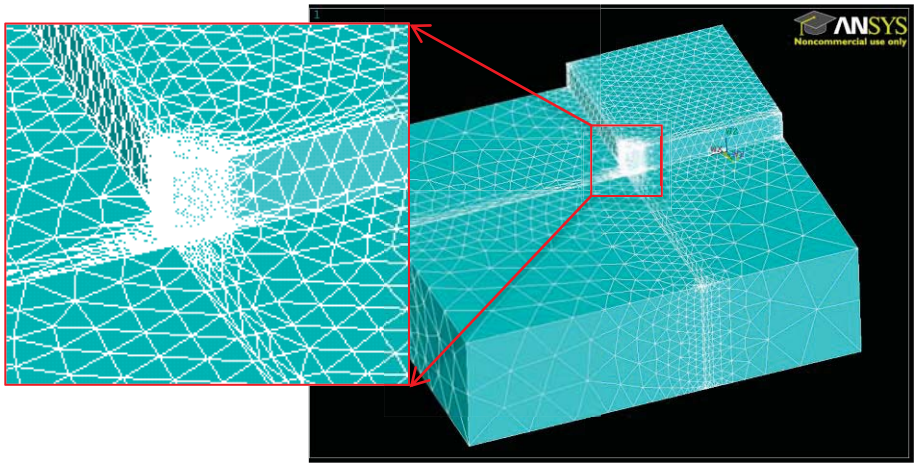


Figure D-5. Generated meshes by ANSYS smart meshing tool.

4. Assign boundary conditions

If the simulation model has the symmetrical structure, half or quarter of the entire structure can be simulated to save the simulation time. Figure D-6 shows the quarter of the entire structure with boundary conditions of zero-displacements at the plane of symmetry.

```
!APPLY BOUNDARY CONDITIONS
CSYS,0,
WPCSYS,-1
ALLSEL,ALL
ASEL,S,LOC,X,-0.001E-3,0.001E-3
DA,ALL,UX,0
CSYS,0,
WPCSYS,-1
ALLSEL,ALL
ASEL,S,LOC,Y,-0.001E-3,0.001E-3
DA,ALL,UY,0
CSYS,0,
WPCSYS,-1
ALLSEL,ALL
KSEL,S, , ,            2
DK,ALL, ,0, ,0,ALL, , , , , ,
ALLSEL,ALL
```

Displacement along xz plane is zero

Displacement along yz plane is zero

Fix key point

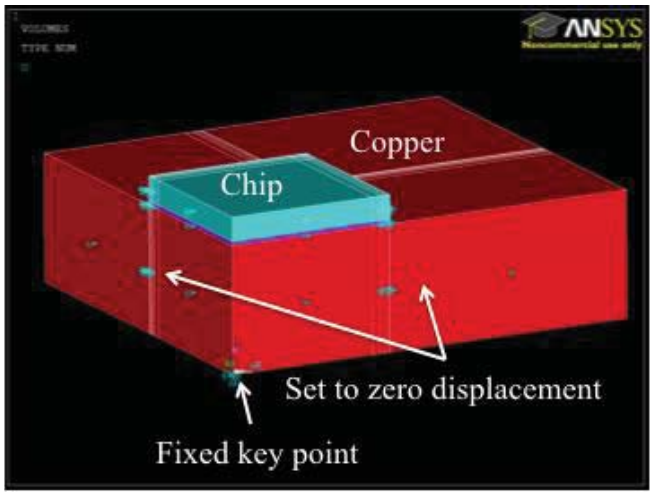


Figure D-6. Demonstration of the boundary condition.

5. Simulation setup for transient analysis

The previous steps finalized the modeling of the simulation object, and the model can be used for either static or transient simulation. Appendix D.A shows the setup for the single load step (static) simulation. Reference temperature, load temperature, and the number of sub-steps should be defined. For the transient simulation, the assigned thermal load has to emulate the temperature variation seen by the module. A thermal cycling of the module is emulated in the example in Appendix D.B. The codes define temperature range, ramp time, and soak time as thermal cycling profile. Then Do-Loop executes each load step until the defined number cycles are reached.

A. Code for static analysis

```
!SINGLE LOAD STEP
!APPLY TEMPERATURE LOAD
TREF,25,      Reference temperature
TUNIF,105,    Load temperature
!SIMULATION SETTINGS
/SOLU
NSUBST,8,8,8   Number of
LNSRCH,1
PRED,ON
ANTYPE,0
NLGEOM,1    Enable large displacement analysis
```

B. Code for transient analysis

```
! THERMAL CYCLING
/SOLU
EQSLV, PCG, 1.0E-8
ANTYPE, STATIC, NEW     Define analysis type
NLGEOM, ON              Enable large displacement analysis
NROPT, AUTO,,OFF
OUTRES, ALL, ALL
HIGHDWEL=600
LOWRAMP=2100
HIGHRAMP=2100           Define load temperature, ramp time, and dwel time
LOWDWEL=600
HIGHTEMP=105
LOWTEMP=-40
DELTA=HIGHTEMP-LOWTEMP
RMPSTP=DELTA/10
TREF, HIGHTEMP
TCYC=HIGHDWEL+LOWRAMP+LOWDWEL+HIGHRAMP
NTC=4   Set number of cycles
RAMPSTEP=2
```

```
*DO,CNT,1,NTC,1 Start Do loop
! LOAD STEP 1
AUTOTS, ON The first load step
NSUBST, 10,15,8
BF, ALL, TEMP, LOWTEMP
KBC,0
TIME, LOWRAMP+(CNT-1)*TCYC
SOLVE
! LOAD STEP 2 The second load step
AUTOTS, ON
NSUBST, 10,15,8
BF, ALL, TEMP, LOWTEMP
KBC,1
TIME, LOWRAMP+LOWDWEL+(CNT-1)*TCYC
SOLVE
… Define remaining load steps
*ENDDO End Do loop
FINISH
```

6. Post processing

The example code shows the calculation of the plastic strain energy of the certain element. In this example, only one element is selected for the process demonstration, but predefined volume has to be analyzed in the actual strain energy analysis.

```
ELE=3128      Select element
!DATA ACQUISITION
ESOL, 34, ELE, , NL, PLWK    Recall transient solutions
! X,Y,Z COMPONENTS OF PLASATIC STRAIN
ESOL, 35, ELE, ,EPPL, X
ESOL, 36, ELE, ,EPPL, Y      Retrieve plastic strains in x,y,z directions
ESOL, 37, ELE, ,EPPL, Z
! SHEAR PLASTIC STRAIN
ESOL, 38, ELE, ,EPPL,XY
ESOL, 39, ELE, ,EPPL,YZ      Retrieve shear strains in x,y,z directions
ESOL, 40, ELE, ,EPPL,XZ
! X,Y,Z COMPONENTS OF STRESS
ESOL, 41, ELE, ,S,X
ESOL, 42, ELE, ,S,Y          Retrieve stresses in x,y,z directions
ESOL, 43, ELE, ,S,Z
! SHEAR STRESS
ESOL, 44, ELE, ,S, XY
ESOL, 45, ELE, ,S, YZ        Retrieve shear stresses in x,y,z directions
ESOL, 46, ELE, ,S, XZ
```

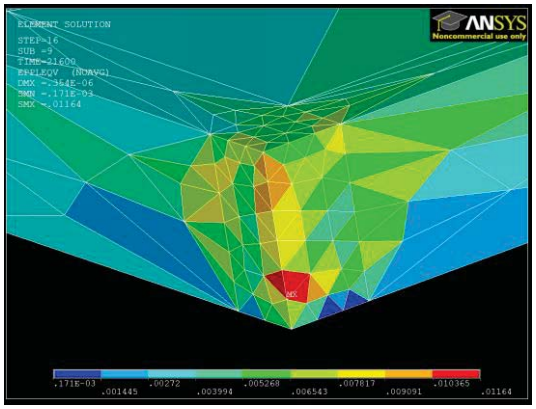
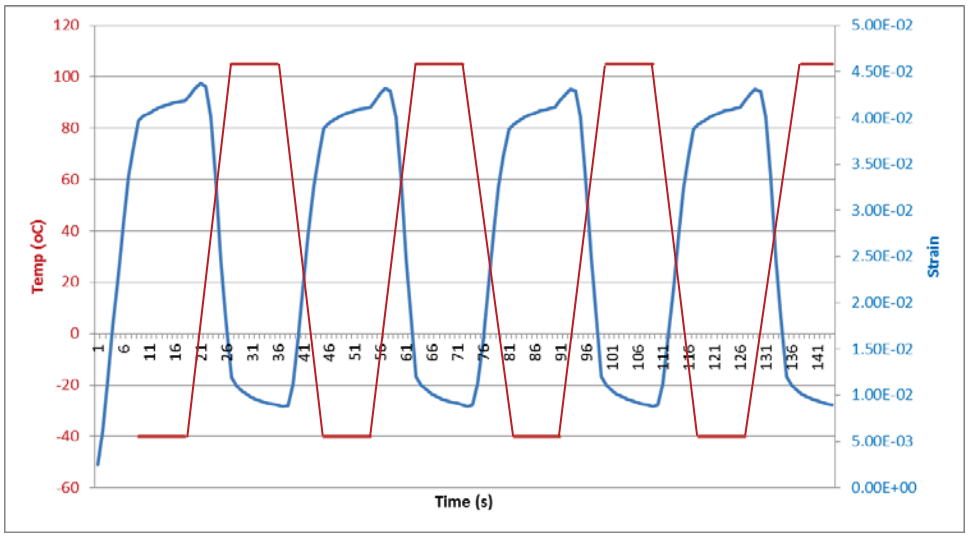


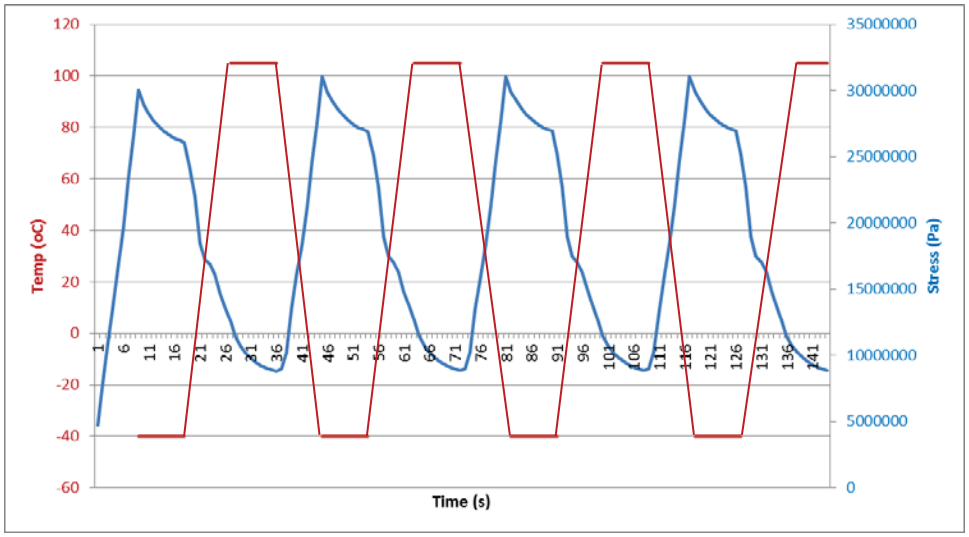
Figure D-7. Plot of the plastic strain by elements.

Figure D-8 shows the simulated Von-Mises plastic strain and stress at the selected element in Figure D-7. The red curve shows the applied thermal load that emulates four thermal cycles, and the blue curves mean the monitored strain and stress. By drawing hysteresis loop of stress and

strain, the accumulated energy per cycle can be calculated, and it can be used for the lifetime prediction of the solder joint.



(a)



(b)

Figure D-8. Simulated Von-Mises plastic strain (a) and stress (b) with temperature cycling condition.

Appendix E . DESIGN PRINCIPLES OF HIGH TEMPERATURE AND HIGH FREQUENCY MODULE

1. Introduction

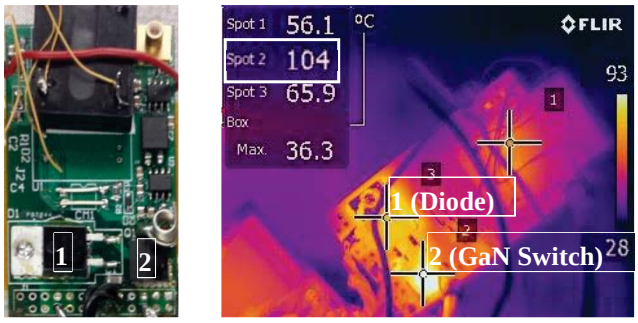
Effort to increase power density beyond 150-W/in^3 while keeping junction temperature rise below 75^{o}C for a 2-kW power converter was confronted by thermal, noise, and integration barriers. Table E.1 shows the power densities of on-board chargers from literature and commercial products. The commercial products have about 4-W/in^3 power densities including liquid-cooling plates, and the recent technology from APEI has 82-W/in^3. Thus, it can be seen that 150-W/in3 power density with low junction temperature rise is challenging goal. Both silicon-carbide and gallium-nitride power semiconductor switches were investigated to permit operation in the 0.5 to 1 MHz range to achieve high power density [1].

Table E.1. State-of-the-art of the on-board charger for electric vehicle [1]-[4]

	Toyota Prius	Chevrolet Volt	J. Kim	J. Lee	APEI
Power Density (W/in^3)	3.6	4.0	9.3	13	82

The low threshold voltages in wide-band-gap switches lead to low noise immunity. Fast turn-off of drain current (or high di/dt) through the common-source layout inductance would induce voltage spike on the gate terminal, turning on the switch again, a phenomenon referred to herein as “self-turn-on” [6]. Switching loss would increase, leading to failure due to excessive heating. Following conventional practice, a power module had been built on printed-circuit board (PCB – Fig. 1) using discrete GaN components in PQFN packages. The parasitic inductances of

the switches and the layouts, however, were found unacceptable. Unstable operation owing to self-turn-on halted testing at about 1 kW.



(a) (b)

Figure E-1. Developed PCB module (a) and thermal image at 650-W operation (b).

The high-density requirement limits the size of heat sink or fan. Thermal management then relies on reduction of resistance along the thermal path. Conventional assembly approaches based on discrete SiC or GaN components, PCB, thermal vias, and thermally conductive insulators in PCB version of the prototype were found inadequate [7]. At only 650 W output power, the temperature at the GaN junction already reached 104^{o}C.

A modern PCB with copper inlay can be a solution for a better thermal management than thermal vias. The method replaces thermal vias to copper coin so that heat flux can be better dissipated to the cooling system. However, the PCB area filled with the copper coin has to be isolated from other patterns and increases the loop size that contains the switching device.

A hybrid approach (similar to that demonstrated in [8] for low power) involving power dice, DBC (direct-bond-copper) substrate, and hybrid assembly turned out to be the right combination. Although the heat sinks dominate the thermal path in both cases, the thermal resistance of the PCB structure is 1.67 times larger than that of the DBC counterpart owing to the thermal vias.

Since the temperature rise is proportional to the junction-to-ambient thermal resistance, this improvement permits the requirement of 75°C temperature rise to be met.

To optimize the common-source inductance, a switch module consisting of three SiC dice was laid out and analyzed in ANSYS Q3D Extraction. The parasitic inductances were limited to 2.89 nH to suppress self-turn-on. Current fall-rate of up to 500 A/μs can be robustly commutated. Noise-free waveforms were observed at all nodes in the power assembly.

Since the quality of the die-attach layer was crucial for heat propagation and dissipation, a vacuum chamber was used to fabricate the module. The DBC switching cell was then assembled with the main PCB board and copper heat sink. The DBC version met the thermal and noise requirements in a 220 W/in^3 assembly.

2. Design Process

A zero-voltage-switched (ZVS) boost converter in Figure E-1 with specifications in Table E.2 was developed in this study. It is half of the topology in [9] and operates with variable switching frequency to simplify the switch connected to the output. Auxiliary inductor L_a and capacitor C_a enable ZVS of M_1 and M_2 and mitigate the peak current stress of boost inductor L_b. Key voltages and currents with their reference directions are marked in Table E.2. The components for power loop in the dashed box are packaged on the DBC module, and remaining components are placed on the PCB board. Gate and power loops which require a carefully designed layout are identified by dotted arrows in red.

Table E.2. Specifications of Converter in Table E.2

Parameter	Description
Input voltage v_{in}	150 – 350 Vdc
Output voltage v_o	390 Vdc
Nominal output power	1.5 kW
Targeted power density	150 W/in^3
Cooling method	Forced-air cooling
Maximum temperature rise at dice	75^{o}C

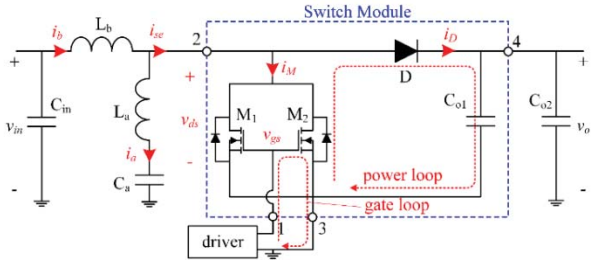


Figure E-2. Circuit diagram of the ZVS boost converter. Components M1, M2, D, and Co1 were modularized to mitigate temperature rise and noise-induced self-turn-on.

Thermal resistances of the PCB and DBC modules were calculated and compared in Figure E-3. Since the thermal pad on PQFN package has high voltage at the drain [10], a thermal-interface-material (TIM) is needed to isolate the thermal pad from heat sink. The thermal resistance of thermal vias is calculated based on the PCB dimension in Figure E-1(a) that has 15 vias with 0.45 mm diameter and 1.6 mm height. A thermal pad and aluminum oxide (Al_2O_3) of DBC substrate were considered as TIM to minimize thermal resistance increase by isolation layer. Although the thermal resistance of heat sink is dominant for all cases, the PCB structure with thermal vias shows 1.7 times, and the structure with copper inlay shows 1.15 times larger thermal resistance than the DBC structure. Considering the integration of switching devices into a small footprint for low parasitic inductance, the DBC structure is more advantageous because bare dice can be packaged to minimize the loop size.

Figure E-4(a) shows the developed DBC module using SiC MOSFETs, diode, and capacitor as explained in Figure E-2. The module was modeled using ePhysics, and the boundary condition was set as 800-LFM forced-air convection at the attached heat sink. The applied thermal load was 3.75 W based on SPICE simulation.

The simulation result in Figure E-5(b) shows that the maximum junction temperature is 65.1°C and the heat sink temperature is 55.7°C. The total thermal resistance from junction to heat sink is calculated as 2.50°C/W.

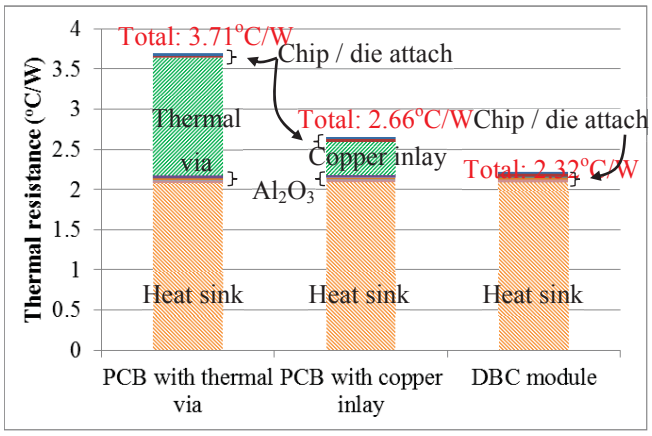


Figure E-3. Calculated thermal resistances of the DBC and PCB module with thermal vias and copper inlay with Alumina (30 W/m-C) as isolation layers.

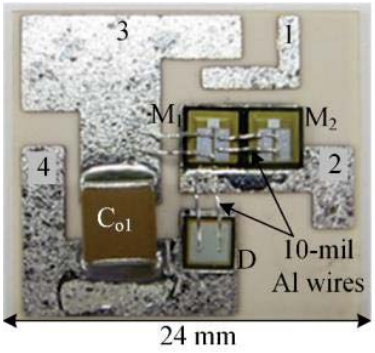
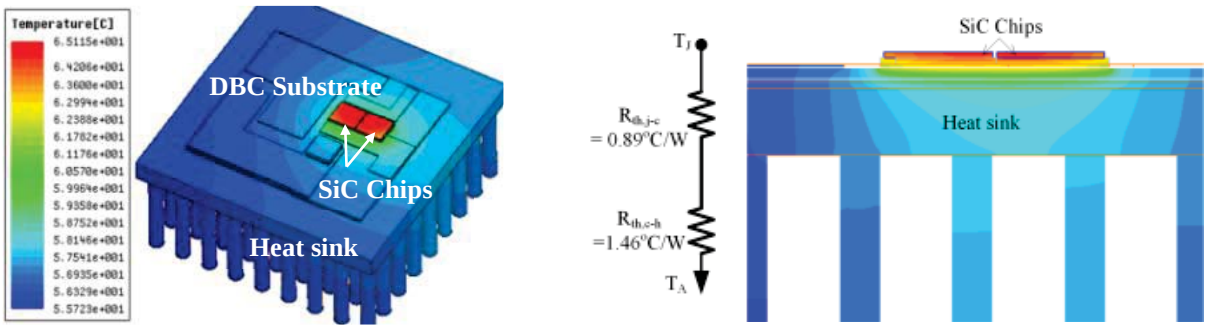


Figure E-4. Layout of the DBC switch module for the thermal simulation in Figure E-5.



(a) (b)

Figure E-5. Simulated junction temperature of the SiC MOSFETs on the DBC module with 3.75-W thermal load for each chip and 800 LFM forced air convection (2-kW operation).

Availability of multilayers in PCB is advantageous to minimize the critical loops. However, the lower thermal conductivity of PCB would necessitate large heat sink and fan to meet thermal specifications. While the DBC substrate enjoys higher thermal conductivity than PCB, it is limited to a small number of metal layers and vias. The developed DBC module contains the power-loop components on the top side and heat sink at the bottom side. Since the wide-band-gap (WBG) switches have lower threshold voltage and higher *di/dt* than silicon counterpart, the layout of the DBC module was designed to minimize the common-source inductance. SiC dice were used to eliminate the package inductances of the switches.

Figure E-6 shows the simulation models for parasitic extractions using ANSYS Q3D. Source and sink currents were applied as indicated in the figure, and the matrix of parasitic inductances were found as

$$\begin{bmatrix} L_{gg} & L_{gd} & L_{gs} & L_{go} \\ L_{dg} & L_{dd} & L_{ds} & L_{do} \\ L_{sg} & L_{sd} & L_{ss} & L_{so} \\ L_{og} & L_{od} & L_{os} & L_{oo} \end{bmatrix} = \begin{bmatrix} 9.58 & 0.26 & -0.41 & 0.46 \\ 0.26 & 2.40 & -0.60 & 0.51 \\ -0.41 & -0.60 & 2.89 & -0.70 \\ 0.46 & 0.51 & -0.70 & 3.39 \end{bmatrix} nH \quad (24)$$

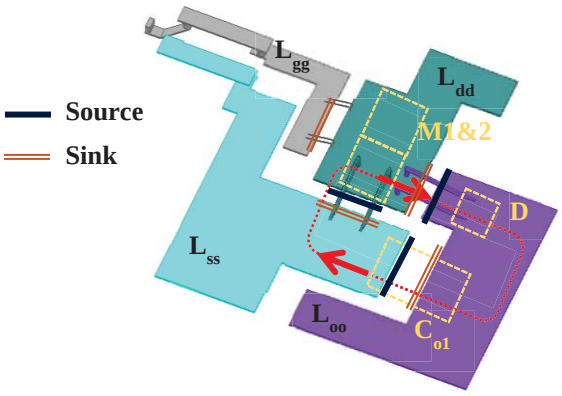


Figure E-6. Q3D simulation model for the parasitic extraction of the DBC module.

The major determinants of turn-off noise are source inductance (L_{ss}) and mutual inductance between drain and source conductors (L_{ds}). As illustrated in Figure E-7(a), the source inductance, L_{ss}, is in a shared path between power and gate loop, and the induced voltage due to high *di/dt* is reflected to gate signal that induces noise during switching transient. Therefore, it is important to suppress the induced voltage at source inductance defined as

$$v_{sn} = L_{ss} \, di_M/dt + L_{ds} \, di_M/dt + L_{os} \, di_D/dt \qquad (25)$$

The first term in (2) is induced voltage by self-inductance, and remaining terms represent the influence of mutual inductances. Thus, it is advantages to suppress L_{ss}, and have negative coupling for L_{ds} and L_{os}.

The source inductance of the optimized DBC module was 2.89 nH, and the calculated coupling coefficient between drain and source using mutual inductance between two paths was found as -0.23. The negative coupling in Table E.3 helps to cancel out the generated magnetic fluxes at these two conductors that eventually mitigate the turn-off noise.

Table E.3. Simulated coupling coefficients among parasitic inductances in Figure E-6

	k_{gd}	k_{gs}	k_{go}	k_{ds}	k_{do}	k_{so}
Coupling coefficient	0.054	-0.077	0.080	-0.23	0.18	-0.22

The circuit in Figure E-6(a) was simulated by LTspice with the extracted parasitic inductances to evaluate the optimized layout. The simulated waveform of DBC module is compared with the measured one as shown in Figure E-7(b). A parameter R_d represents a parallel resistance of the gate conductor induced by the skin effect, and R_s represents resistances of gate driver and conductors. The simulation parameters were tuned to match the measured peaks and frequency so that the circuit model is useful for prediction of self-turn-on. Considering the output resistance of the gate driver is 1 Ω, the total series resistance with copper trace and wire-bond is tuned as 1.08 Ω. The simulated peak voltage at turn-off transient was -0.12 V with 200 V input voltage that was well below the threshold voltage (1.7 V).

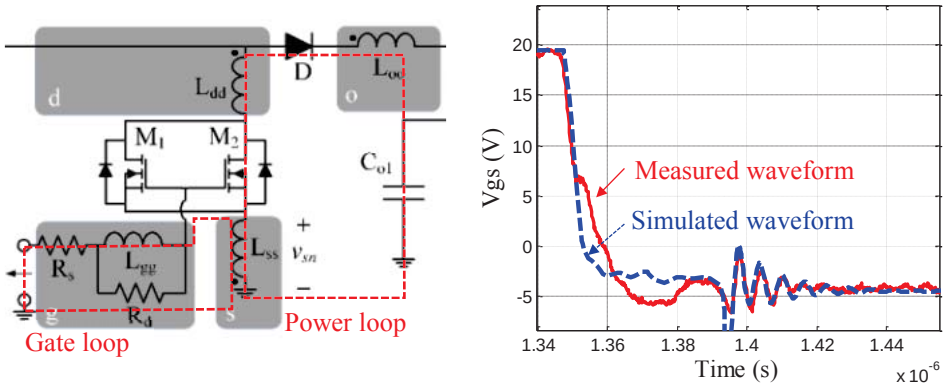


Figure E-7. Schematic of the power loop with parasitic inductances (a), and simulated turn-off noise compared with measurement result (R_d=50 Ω and R_s=1.08 Ω) (b).

3. Developed DBC Module

Packaging materials for the fabrication of DBC module are listed in Table E.4. The materials are selected for two-step reflow process: the first step for the DBC module fabrication; the second step for the assembly of PCB board, DBC module, and heat sink. The die attach material was chosen accordingly as $Sn_{63}Pb_{37}$ solder (T_m=183^{o}C) and Bi58Sn42 solder (T_m=138^{o}C). Detailed packaging steps are explained in the next section.

Table E.4. Specifications of the Packaging Materials of the DBC Module

Layer	Material	Dimension (mm x mm x mm)	Thermal Conductivity (W/m-^{o}C)
Die	SiC	4.08 × 4.08 × 0.36	125
Die solder	$Sn_{63}Pb_{37}$	0.2 mm thick (T_m=183^{o}C)	40.9
PCB solder	$Bi_{58}Sn_{42}$	0.2 mm thick (T_m=138^{o}C)	
Copper top / bottom (DBC)	Copper	23.5 × 20.9 × 0.127	400
Alumina (DBC)	Al_2O_3 (96%)	24 × 21.4 × 0.32	40
Heat sink	Copper	31.2 × 31.2 × 10.2	400
Bond wire	Al	10 mil (source) / 2 mil (gate)	205

Since the quality of the die-attach layer is crucial for heat propagation and dissipation, the assembly process was divided in two steps. The first step was using a vacuum chamber to fabricate the DBC module (Figure E-8), and the second step was using convection oven with lower temperature solder to attach motherboard and heat sink to the DBC module (Figure E-8). The DBC substrate was chemically etched to pattern the interconnections (Figure E-8(a)). Cirlex fixture was laser-machined with cavities to align components with DBC substrate (Figure

E-8(b)). The DBC with the fixture was embedded in a graphite boat for the vacuum-reflow, and components were placed with tin-lead solder preforms of which melting temperature is 183°C (Figure E-8(d)). The source pads of SiC MOSFET and diode were then wire-bonded by 10-mil aluminum wires, and gate pads by 2-mil aluminum wires (Figure E-8(e)).

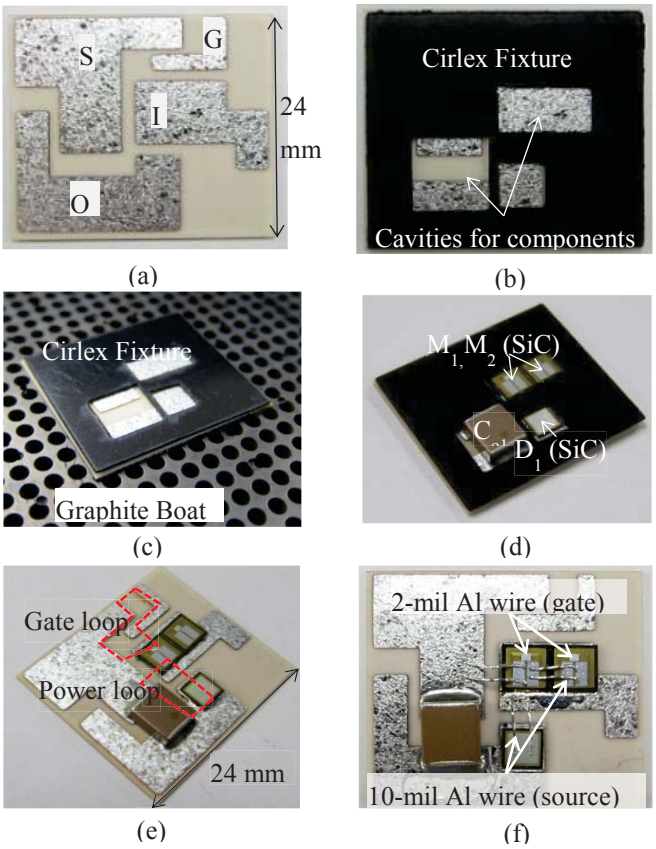


Figure E-8. Fabrication process of the DBC module: (a) chemical etching, (b) fixture design, (c) masking, (d) assembly, (e) vacuum reflow, and (f) wire-bonding.

Since the solder layers of SiC dice and capacitor on DBC module should not be influenced during the assembly process with the PCB motherboard, $Bi_{58}Sn_{42}$ solder paste with melting temperature 138°C was applied to the edges of the DBC substrate and the bottom side of DBC

substrate as illustrated in Figure E-9. By soldering DBC module to the mother board and to the heat sink, reliable mechanical support and low thermal resistance were achieved.

After attaching the DBC module to the PCB, remaining components on the top side of the PCB were soldered as exhibited in Figure E-9. The input and output capacitors, gate driver, and common-mode choke were placed on the top side, and magnetic components L_a and L_b on the bottom side of the PCB. The area used for electric operation was 57 mm × 61 mm, or 3477 mm^2 with 43 mm height. The volumetric power density (P_d) of the converter with 2-kW output power is calculated as

$$P_d = \frac{2000\ W}{3477\ mm^2 \times 43\ mm} = 219\ W / in^3 \qquad (26)$$

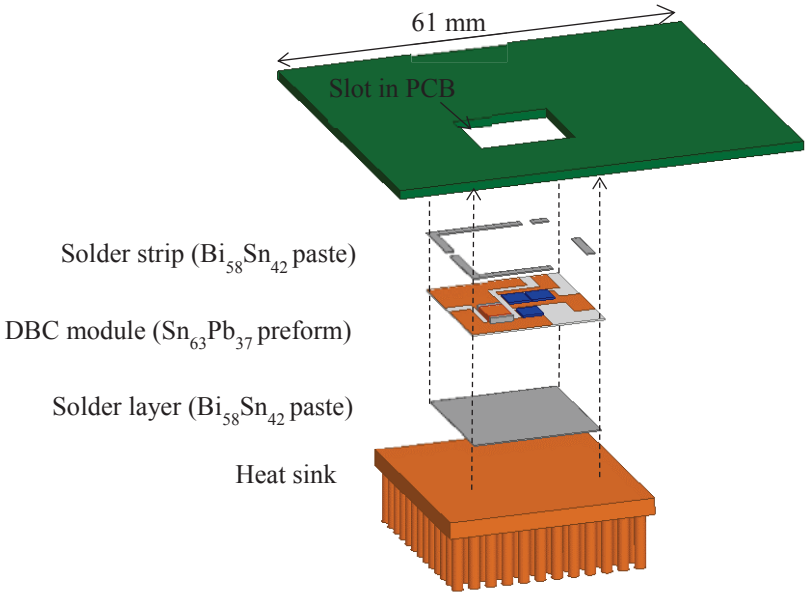
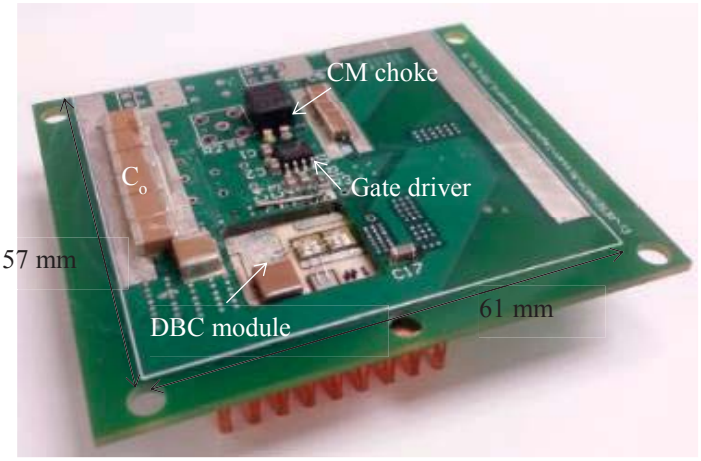
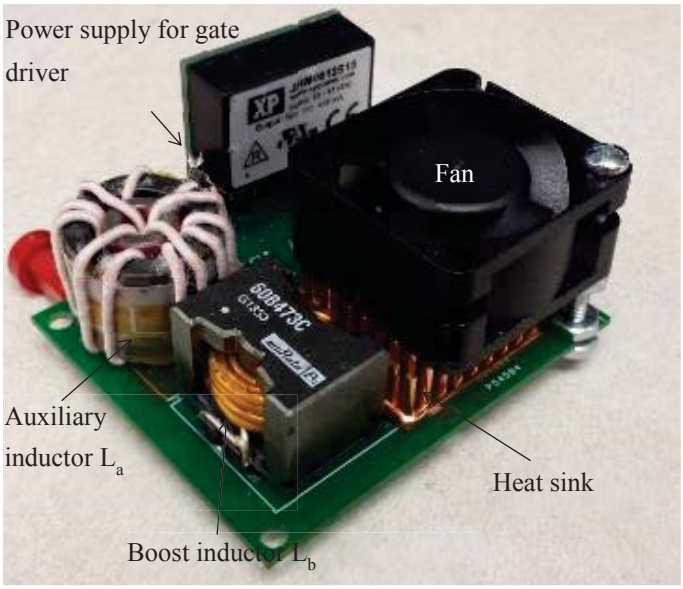


Figure E-9. Assembly of packaged DBC substrate (Figure E-8) with PCB and heat sink.



(a)



(b)

Figure E-10. (a) Top side of the PCB mother board with the switch module integrated. (b) Bottom side of the mother board with magnetic and cooling components.

4. Experiment Results

All experimental waveforms were captured by a 5-gigasample-per-second oscilloscope, Tektronix MSO5104. Channels from 1 to 4 represents v_{gs}, v_{ds}, i_b, and i_a, respectively, and the channel 3 and 4 have the same zero level. Semiconductor current i_{se} is calculated by subtracting i_a (channel 4) from i_b (channel 3) using the math function of the scope. Specifications and list of

components for the boost converter development are listed in Table E.5. Figure E-11 shows converter operation when v_{in} = 250 V; switching frequency = 690 kHz; output power = 1.5 kW. The bandwidth of channel 1 is 500 MHz to check the existence of the noise in vgs waveform. MOSFET's M1 and M2 turned on when vds was 104 V to minimize the turn-on switching loss.

Table E.5. Configuration of Boost Converter with DBC Module

Parameter	Description
Input Voltage v_{in}	150 – 350 Vdc, (Sorensen™ SGI 160/63 for 150 V; TDK-Lambda™ GEN600-8.5 for higher voltages)
Output Voltage v_o	390 Vdc
Maximum Output Power	2 kW (consumed by TDI Power™ MCL488)
L_b	47 μH (60B473C from Murata Power Solution™)
L_a	9.7 μH (customized constant flux inductor [25])
C_a	1 μF (ten 0.1 μF/630 V ceramic capacitors in parallel)
M_1, M_2	CPM2-1200-0080B from Cree™ (SiC, 1200 V-31.6 A, 80 mΩ on-resistance)
Switching Frequency	400 kHz – 1 MHz
D	CPW5-0650-Z050B from Cree™ (SiC, 650 V-50 A)
Gate Driver	IXDD609SI from IXYS™ (60-ns maximum propagation delay)
Gate Driver Output Voltage v_{gs}	+21.5 V (turn-on) and -2.5 V (turn-off)
Power Supply for Gate Driver	JCD0412S24 from XP Power™ (24 V-166 mA output, 500-pF isolation capacitance)
C_{o1}	0.47 μF/630 V ceramic capacitor
C_{o2}	2.7 μF (ten 0.27 μF/630 V ceramic capacitors in parallel)
Heat Sink	4-121204U from Cool Innovations™ (31.2 × 31.2 × 10.2 mm)
Fan	PMD1238PKB1-A from Sunon™

(38 mm × 38 mm × 20 mm)

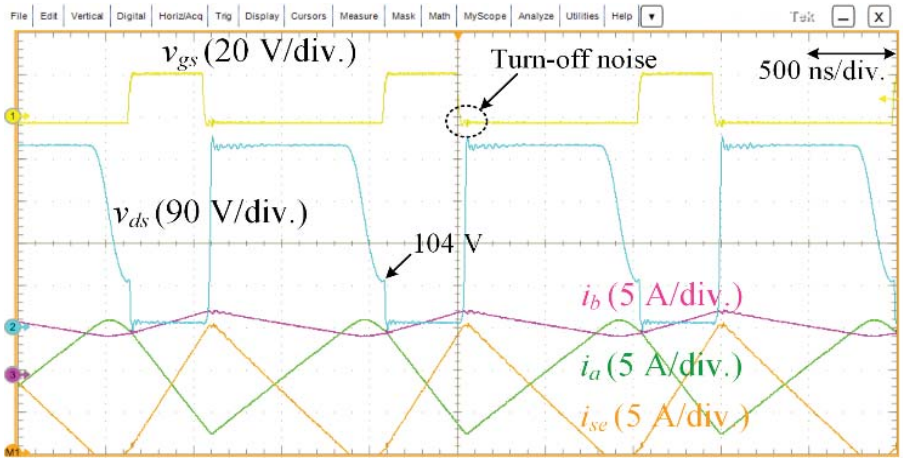
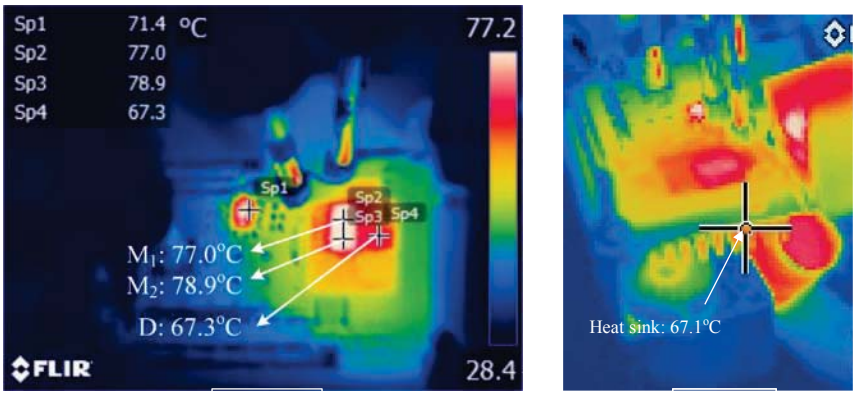


Figure E-11. Experimental waveforms of the boost converter with Version-3 switch module when the input voltage is 250 V and output power is 1.5 kW.

Thermal image in Figure E-12(a) was taken by infrared thermal camera FLIR-E40 after the switch module surface had been dyed in black for calibrated measurement. Spot Sp2 and Sp3 show the highest temperature of M_1 and M_2 as 77°C and 78.9°C with forced-air cooling when v_{in} = 350 V; switching frequency = 435 kHz; output power = 1.5 kW. The temperature rise was limited to 48.9°C considering the ambient temperature was 30°C. Figure E-12(b) shows the measured temperature of the heat sink. Since the bottom side of the heat sink was covered by fan, the temperature of fin at the edge was measured, and the measured temperature was 62.1°C. The expected temperature change from die to edge of heat sink was 9.38°C, but the measured temperature change was 11.8°C. The error could be induced by the thermal resistance variation of the heat sink according to the applied wind speed. The simulation condition in Figure E-5 was conducted with estimated wind speed, 800 LFM, but the actual wind speed in the experiment could be lower. Considering the thermal resistance of heat sink varies from 1.66°C/W to

3.05°C/W with wind speed from 600 LFM to 200 LFM, this can be a reason of mismatch between simulated and experimented thermal resistances.



(a) (b)

Figure E-12. Thermal image of the switch module (a) and heat sink (b) when the die temperature was the maximum in 350-V vin and 1.5-kW output operation.

Figure E-13 plots the measured efficiency, simulated efficiency, and switch die temperature for various input voltage. The maximum efficiency is 98.3% when v_{in} = 250 V; output power = 1.5 kW. The temperatures of the MOSFET show opposite trends with the efficiency. The lowest temperature of the MOSFET is 54.1°C when v_{in} is 200 V or 250 V, and the highest is 78.9°C when vin = 350 V as shown in Figure E-12. The simulated efficiency was obtained by LTspice. The losses in the components are calculated during the 200-ns steady-state operation (from 1.3 µs to 1.5 µs) with 15-ns maximum time step. The converter is tested with the higher output power by increasing v_{in} to 250 V. The output power is limited to 2 kW by the maximum current that the power supply TDK-Lambda GEN600-8.5 could provide.

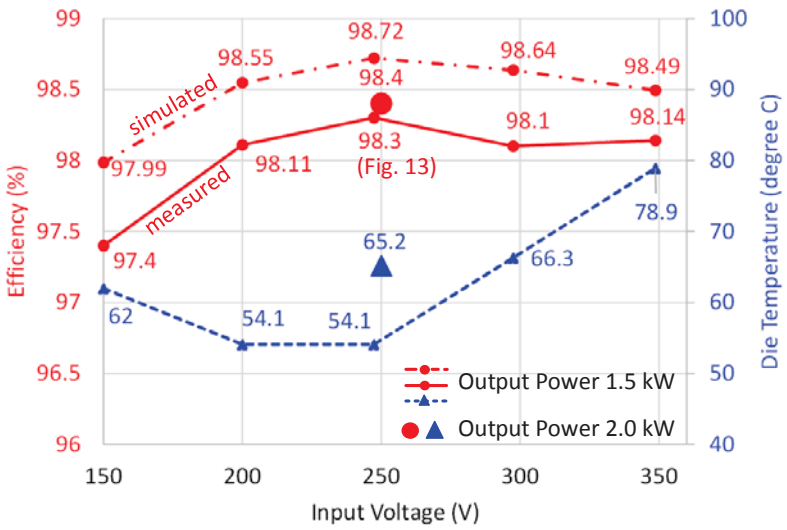


Figure E-13. (a) Efficiency (with y-axis in left-hand side) and MOSFET chip temperature (with y-axis in right-hand side) for various v_{in}.

Figure E-14 shows the loss breakdown in the simulation when v_{in} was 250 V; output power was 1.5 kW; efficiency was 98.72%; total loss was 19.11 W. The core and winding losses of L_a was simulated using Maxwell with the current excitation from the circuit simulation, and the simulated losses were 2.47 W and 2.3 W, respectively.

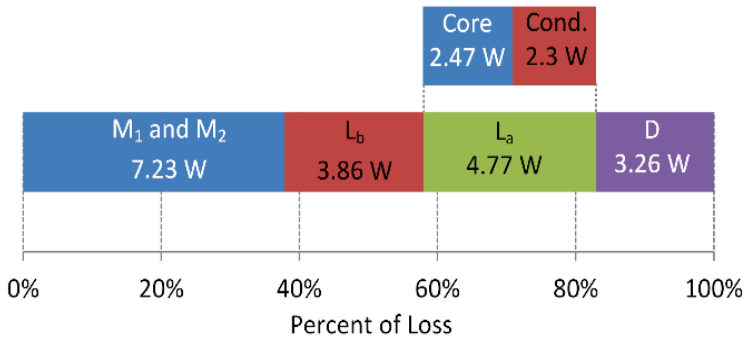


Figure E-14. Loss breakdown in the simulation when vin = 250 V; output power = 1.5 kW.

5. Conclusion

Designing a high power-density converter is challenging when high output power and limited semiconductor temperature are required. A switch module integrated the semiconductor dice on the DBC to lower thermal resistance to 2.35^{o}C/W from the surface-mounted chip to ambient air. The small thermal resistance lowered the chip temperature and increased the power density by shrinking the size of cooling components. Compact layout of the power loop with 2.89-nH common-source inductance and negatively coupled source and drain conductor reduced the noise in v_{gs} waveform to void self-turn-on. Vacuum reflow is used to integrate the semiconductor dice and DBC with $Sn_{63}Pb_{37}$ solder preform. $Bi_{58}Sn_{42}$ solder paste and hot plate are utilized to attach the module to PCB. The 2-kW boost converter realized by the fabricated module recorded 220-W/in^3 power density. Its maximum efficiency and temperature rise of the semiconductor were 98.4% and 48.9^{o}C, respectively. The junction temperature rise can be even further decreased by using aluminum nitride (AlN) substrate that has seven times higher thermal conductivity than aluminum oxide (Al_2O_3). The maximum switching frequency was 1 MHz when output power was equal to 770 W.

6. Acknowledgement

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