SOME DESIGN CONSIDERATION OF SWITCHING REGULATOR USING CURRENT-INJECTED CONTROL

by

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Thesis submitted to the Faculty of the

Virginia Polytechnic Institute and State University

in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

in

Electrical Engineering

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June, 1982
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ACKNOWLEDGEMENTS

I wish to express my gratitude to Dr. Fred C. Lee for providing the opportunity to analyze and research the topic discussed in this thesis. The continued encouragement, positive attitude and technical expertise Dr. Lee has provided throughout the duration of this thesis is greatly appreciated.

I wish to express my appreciation to my committee members Dr. D. D. Chen and Dr. C. E. Nunnally for sharing their knowledge of control theory and converter design with me and their continuous support and leadership.

I would also like to acknowledge XEROX COMPANY for their financial support .

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CHAPTER I

INTRODUCTION

In recent years, various multi-loop sensing schemes have been proposed for switching regulator control. These schemes have vastly improved the switching regulator stability and dynamic performance. Among these multi-loop control schemes, two of them are particularly noteworthy. One, often referred to as standardized control module[1,2] employs a loop that indirectly senses the ac component of the inductor current in addition to the conventional dc sensing loop. The second scheme, often referred to as current-injected control or current programmable control[4,5,6], employs an ac loop that senses either the switch current or the total inductor current (with both dc and ac component). Due to their derived superior dynamic performance characteristics, the above mentioned control schemes, have been widely used for high performance regulator designs for aerospace and industry applications.

The analysis of multi-loop DC-DC converter has been performed thoroughly for SCM control, where the designer following the design procedure can pinpoint the control circuit parameters that optimize the converter performances. Although the current-injected control is similar to the SCM control in some aspects, the differences concerning various small-signal control-dependent characteristics of the two controls are quite noticeable. Due to the lack of efforts of modeling and analysis, the complex interaction among various control parameters of the current-injected control is not well understood. The objective of the present study is to pinpoint the effects of

various critical control circuit parameters and to establish analysis-based design guidelines in order to optimize the switching regulator performances.

1.1 Circuit Descriptions

Illustrated in Fig. 1.1 is a two-winding buck/boost converter employing current-injected control that will be discussed in this thesis.

During the switch (HEXFET) ON time input current flows through current sensing transformer T_2 and power inductor/transformer T_1. Because of the polarity of the diode no energy is transferred to output and energy is stored in the magnetic core of T_1; therefore T_1 acts as an inductor rather than a transformer. During this ON period, two signals are sensed, which will be used to generate the duty-cycle control signal applied to the switch. First signal, any voltage fluctuation at the output will be sensed by the DC error sensing loop and amplified. Second signal, the switching current i_p ramp is sensed by the AC loop (current injected loop). These two signals add together, as shown in Fig. 1.1 and compare with a reference voltage, which is imbeded in the NE555 chip. For the constant frequency control a clock signal is used to turn-on the switch. As the combined dc and ac signal, V_T, intersects the reference voltage as shown in Fig. 1.2, it terminates the ON time.

During the OFF time the stored energy in T_1 is released to the output and charges the output capacitor C_{01}. After certain period, determined by the digital signal processor (DSP), a signal is generated by the DSP to initiate the next ON time.

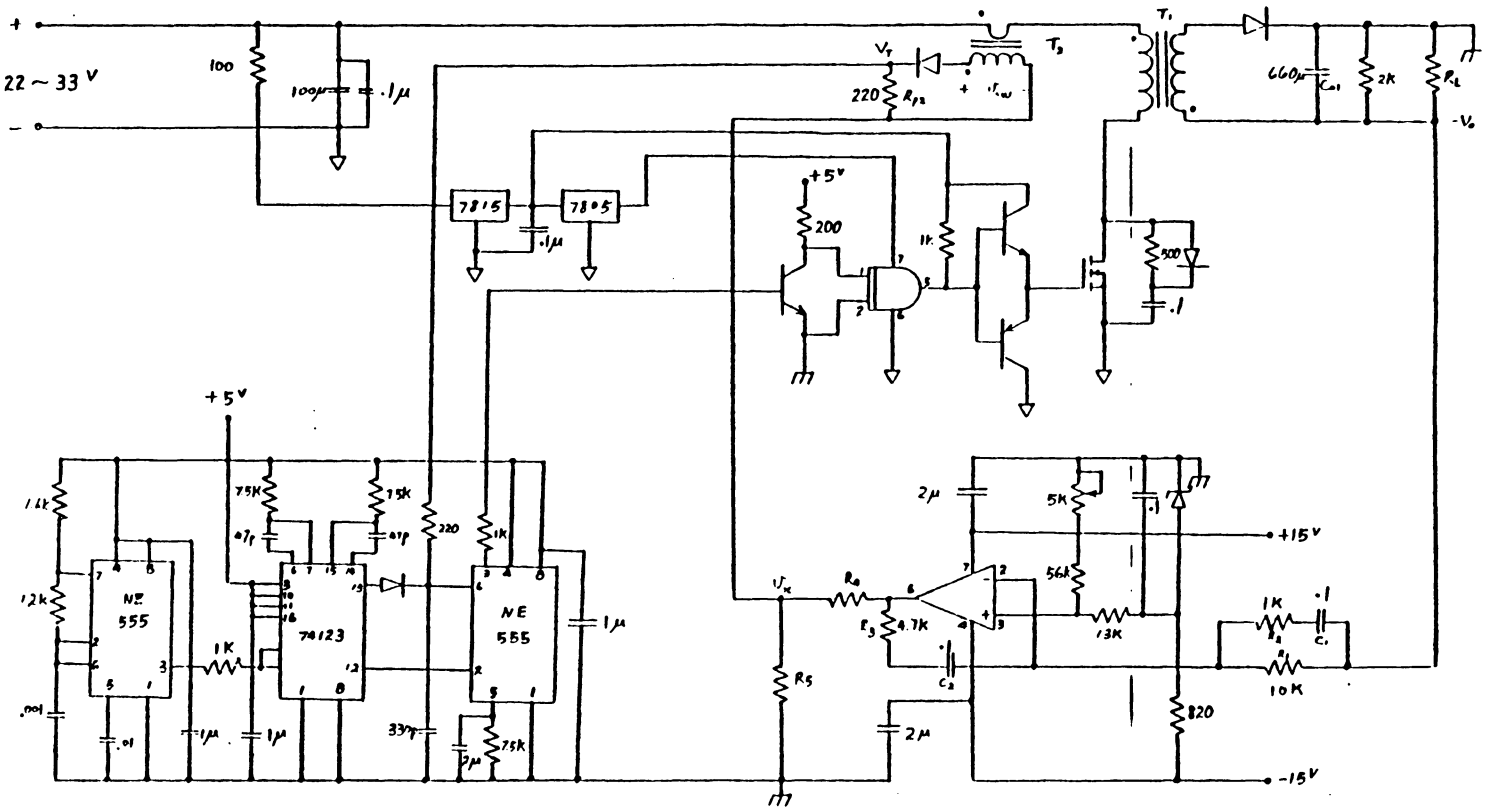
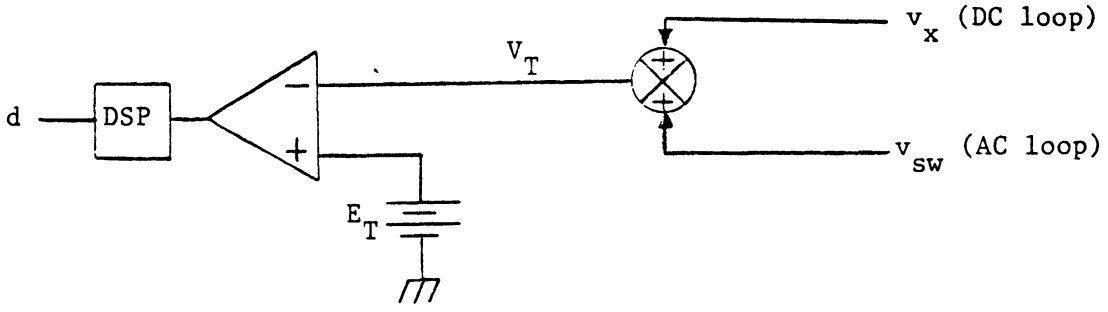
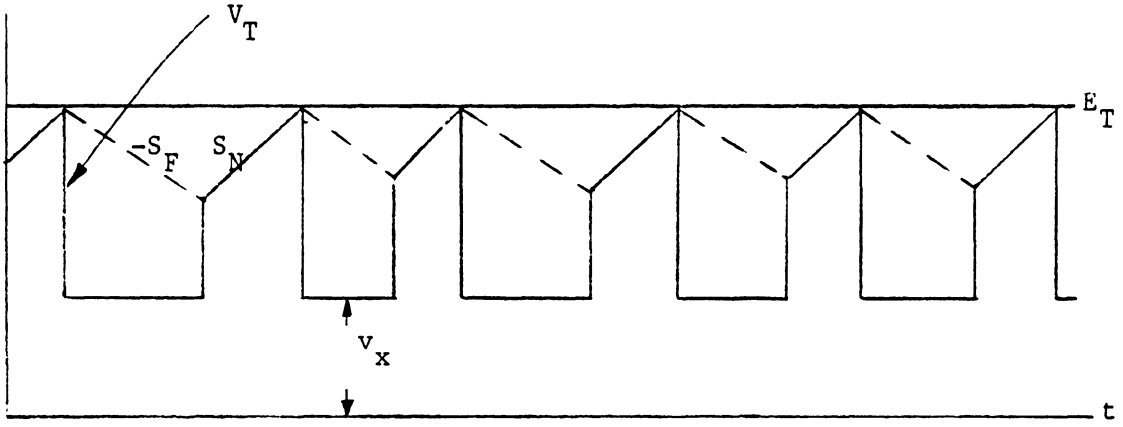


Fig. 1.1 DC-DC Switching Regulator Employing Current-Injected Control



(a)



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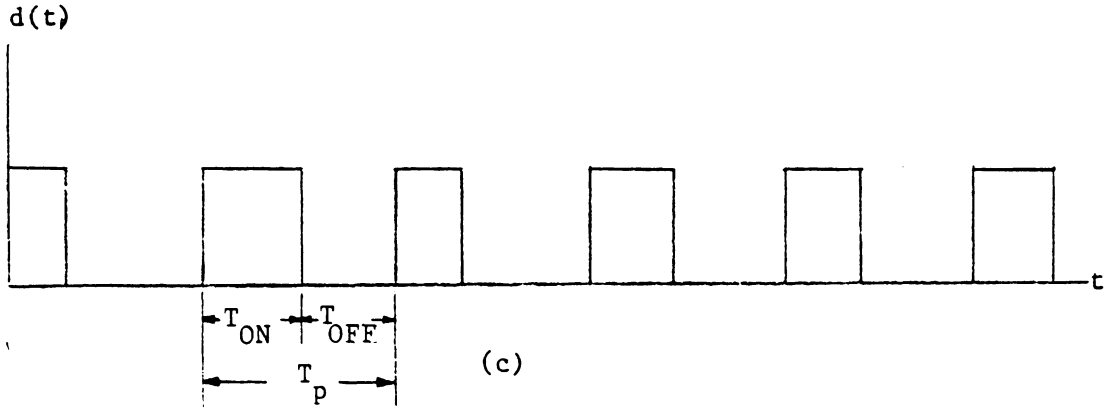


(c)

Fig. 1.2 Waveforms in Pulse Modulator

Current-injected control offers many desirable features that are unique.

1. Inherent peak current protection of the power switch. Since the peak switching current is limited by the control voltage from the DC loop so protection for the power switch is inherent. In addition, the peak magnitude of the inductor current (or switch current) is controlled. The converter is sometimes referred to as a current source converter instead of a voltage source converter.
2. Improved dynamic performances. Besides sensing output voltage variation the inductor current or the switch current modulation signal is also sensed to provide a total-state control. Improvement of regulator dynamic performances are therefore expected.
3. Parallel-Power module operation. The current sharing problem exists in many types of power supply where several converters are parallelly connected to get higher power output. Employing the current-injected control for each power module, while sharing a common DC error voltage, the output current of each module will be equally shared.

In this thesis, the small-signal model for power stage, error processor and duty cycle pulse modulator are presented in Chapter II. The analysis of current-injected converter employing gain compensation, lag compensation and lead-lag compensation are discussed in Chapter III, IV and V, respectively, and key control parameters are pinpointed.

In Chapter VI, the effects of duty cycle pulse modulator operating under different control laws are discussed.

Design considerations and guidelines for selecting control circuit parameters are provided in Chapter VII. Finally, conclusions and future works are given in Chapter VIII.

The performances of switching regulator can be characterized in the following five categories [1]:

.stability; from the phase margin to justify the stable operation of the switching regulator.

.audiosusceptibility; input noise rejection rate to be high so that the ouput (V_o) is immune to the disturbance from input (V_i).

.output impedance; output impedance to be low so that the output (V_o) is unaffected by the change of the load (i_o).

.transient response; the settling time and transient peaking due to a step load change to be small.

.DC regulation; the output of the converter to be regulated.

A tool to evaluate these performances is the open loop gain and phase, which is the criterion we used in this thesis. From the previous work [1,3] we know a higher open-loopgain, especially within frequency range lower than resonant frequency, under stable condition will result in better performances mentioned above. Therefore, our goal is to obtain a set of control loop parameters values such that the open loop gain is as high as possible with ample phase margin.

CHAPTER II

MODELING OF CURRENT-INJECTED CONVERTER

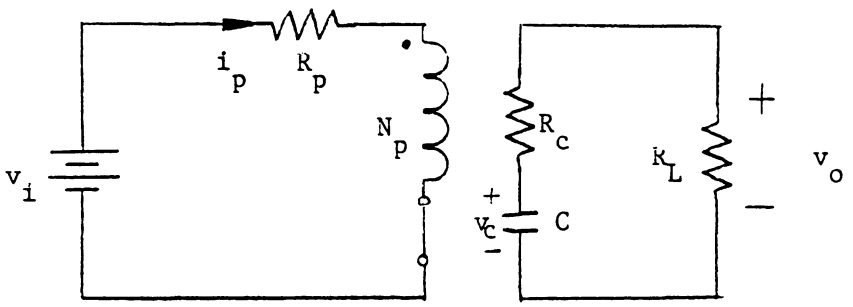
The converter is a nonlinear, discrete, time varying system [1] due to: 1) the discrete nonlinearity originated from the operation of power switch, and 2) the nonlinearity in the digital signal processor (DSP), the analog error signal is converted into the duty cycle signal. A small signal model is derived in this chapter for the purpose of frequency-dependent performance analysis and control design. State space averaging technique is used to derive the small signal model for power stage [7,8,9].

In section 2.2, the power stage transfer function is derived from this model. Error processor model and DSP model [1,4] are derived in sections 2.3 and 2.4, respectively. The small signal block diagram representing the whole system is established in section 2.5.

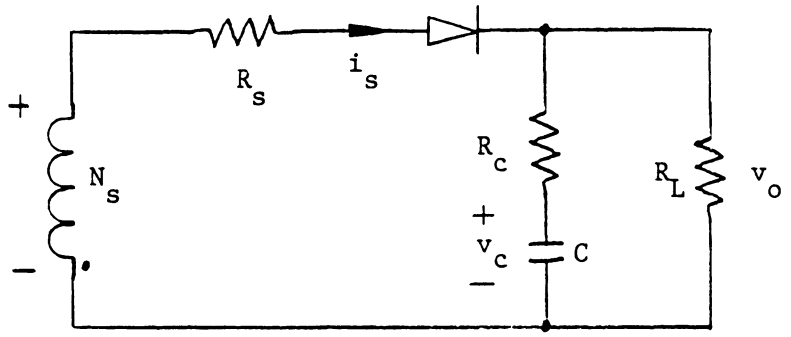
2.1 Power Stage Model

The nonlinear power stage can be modeled by two linear circuits for continuous inductor current operation, according to the switch ON-OFF, which are shown in Fig. 2.1. The magnetic flux, ϕ, and the output capacitor voltage, V_c, are chosen as the state variables and V_o and i_p as output variables. Perform mesh analysis on the two circuits in Fig. 2.1, we can write down two sets of state equations.

For switch ON:
$$\frac{d\phi}{dt} = -\frac{R_p}{L_p}\phi + \frac{1}{N_p}v_i$$
$$\frac{dv_c}{dt} = \frac{-v_c}{(R_L + R_c)C} \qquad (2.1)$$



T_{ON}



T_{OFF}

Fig. 2.1 Power Stage Equivalent Circuit During Power Switch ON and OFF

$$v_o = \frac{R_L}{R_L + R_c} v_c \qquad i_p = \frac{N_p}{L_p} \phi$$

For switch OFF (Fig. 2.1(b)):

$$\frac{d\phi}{dt} = -\frac{R_s + R_c \,//\, R_L}{L_s} \phi - \frac{R_L}{N_s(R_L + R_c)} v_c$$

$$\frac{dv_c}{dt} = \frac{N_s R_L}{L_s C(R_L + R_c)} \phi - \frac{1}{(R_L + R_c)C} v_c \qquad (2.2)$$

$$v_o = \frac{N_s}{L_s} \cdot (R_c \,//\, R_L)\phi + \frac{R_L}{R_L + R_c} v_c$$

$$i_p = 0$$

Assemble them into matrix form, we have:

$$\left.\begin{aligned} \dot{\underline{x}} &= A_1\underline{x} + B_1\underline{u} \\ \underline{y} &= C_1\underline{x} \end{aligned}\right\} \; T_{ON} \qquad (2.2)$$

$$\left.\begin{aligned} \dot{\underline{x}} &= A_2\underline{x} + B_2\underline{u} \\ \underline{y} &= C_2\underline{x} \end{aligned}\right\} \; T_{OFF} \qquad (2.3)$$

where

$$\underline{x} = \begin{bmatrix} \phi \\ v_c \end{bmatrix}, \quad \underline{u} = \begin{bmatrix} v_I \end{bmatrix}, \quad \underline{y} = \begin{bmatrix} v_o \\ i_p \end{bmatrix}$$

$$A_1 = \begin{bmatrix} -\frac{R_p}{L_p} & 0 \\ 0 & \frac{-1}{(R_L + R_c)C} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} \frac{1}{N_p} \\ 0 \end{bmatrix}$$

$$C_1 = \begin{bmatrix} 0 & \frac{R_L}{R_L + R_c} \\ \frac{N_p}{L_p} & 0 \end{bmatrix}$$

$$A_2 = \begin{bmatrix} -\frac{R_s + R_c \,//\, R_L}{L_s} & -\frac{R_L}{N_s(R_L + R_c)} \\ \frac{N_s R_L}{L_s C(R_L + R_c)} & \frac{-1}{(R_L + R_c)C} \end{bmatrix}$$

$$B_2 = \underline{0}$$

$$C_2 = \begin{bmatrix} \frac{N_s}{L_s}(R_c \,//\, R_L) & \frac{R_L}{R_L + R_c} \\ 0 & 0 \end{bmatrix}$$

After averaging over a single period T_p:

$$\dot{\underline{x}} = A\underline{x} + B\underline{u}$$
$$y = C\underline{x} \qquad (2.4)$$

where

$$A = dA_1 + d'A_2 = \begin{bmatrix} -d\frac{R_p}{L_p} - d'\frac{R_s + R_c \,//\, R_L}{L_s} & -d'\frac{R_L}{N_s(R_L + R_c)} \\ \frac{d'N_s R_L}{L_s C(R_L + R_c)} & \frac{-1}{(R_L + R_c)C} \end{bmatrix}$$

$$B = dB_1 + d'B_2 = \begin{bmatrix} \frac{d}{N_p} \\ \\ 0 \end{bmatrix}$$

$$C = dC_1 + d'C_2 = \begin{bmatrix} d' \frac{N_s}{L_s} (R_c \,//\, R_L) & \frac{R_L}{R_L + R_c} \\ \\ d \frac{N_p}{L_p} & 0 \end{bmatrix}$$

assume $R_c << R_L$ and $\frac{R_p}{L_p} = \frac{R_s}{L_s}$, the expressions can be simplified as:

$$A = \begin{bmatrix} \frac{-R_s - d'R_c}{L_s} & -d' \frac{1}{N_s} \\ \\ d' \frac{N_s}{L_s c} & -\frac{1}{R_L c} \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{d}{N_p} \\ \\ 0 \end{bmatrix}$$

$$C' = \begin{bmatrix} d' \frac{N_s}{L_s} R_c & 1 \\ \\ d \frac{N_p}{L_p} & 0 \end{bmatrix}$$

Perturbation

Introduce the input voltage variation and duty cycle variation in the following form:

$$v_i = V_I + \hat{v}_i$$

$$d = D + \hat{d}$$

$$d' = D' - \hat{d}$$

where V_I is the DC input voltage, $\hat{v}_i$ is the variation, D is the steady state duty ratio, $\hat{d}$ is the variation. This causes a perturbation in state variables and output:

$$\underline{x} = X + \hat{\underline{x}}$$

$$y = Y + \hat{\underline{y}}$$

where $\underline{X}$ is the DC value of the state vector,

$\hat{\underline{x}}$ is the AC variation riding on the DC value,

$\underline{Y}$ is the DC value output,

$\hat{\underline{y}}$ is the AC variation riding on the DC value.

Substitute these variations into eq. (2.4) results in:

$$\dot{\underline{x}} = \underline{0}$$

$$\begin{aligned}
\dot{\hat{\underline{x}}} = {} & [DA_1 + D'A_2]\underline{X} + [DB_1 + D'B_2]\underline{U} && \text{(DC term)} \\
& + [DA_1 + D'A_2]\hat{\underline{x}} + [DB_1 + D'B_2]\hat{\underline{u}} && \text{(AC variation} \\
& + \{[A_1 - A_2]\underline{X} + [B_1 - B_2]\underline{U}\}\hat{d} && \text{(duty cycle variation)} \\
& + \{[A_1 - A_2]\hat{\underline{x}} + [B_1 - B_2]\hat{\underline{u}}\}\hat{d} && \text{(second order term)}
\end{aligned} \qquad (2.5)$$

$$\begin{aligned}
Y + y = {} & [DC_1 + D'C_2]\underline{X} && \text{(DC term)} \\
& + [DC_1 + D'C_2]\hat{\underline{x}} && \text{(AC variation)} \\
& + [C_1 - C_2]\underline{x}\ \hat{d} && \text{(duty cycle variation)} \\
& + [C_1 - C_2]\underline{x}\ \hat{d} && \text{(second order term)}
\end{aligned} \qquad (2.6)$$

The perturbed state equation is nonlinear due to the second order term.

Linearization

Under small signal approximation, the variation part is small compared to the steady state value, i.e.:

$$\frac{\hat{v}_i}{V_I} << 1 , \quad \frac{\hat{d}}{D} << 1 , \quad \frac{\hat{\phi}}{\Phi} << 1 , \quad \frac{\hat{v}_c}{V_c} << 1 , \quad \frac{\hat{v}_o}{V_o} << 1 , \quad \frac{\hat{i}_p}{I_p} << 1$$

and neglect the second order term, we have:

$$[DA_1 + D'A_2]\underline{X} + [DB_1 + D'B_2]\underline{U} = 0 \tag{2.7}$$

$$\dot{\hat{\underline{x}}} = [DA_1 + DA_2]\hat{\underline{x}} + [DB_1 + D'B_2]\hat{\underline{u}} + \{[A_1 - A_2]\underline{X} + [B_1 - B_2]\underline{U}\}\hat{d} \tag{2.8}$$

$$\underline{Y} = [DC_1 + D'C_2]\underline{X} \tag{2.9}$$

$$\hat{\underline{Y}} = [DC_1 + D'C_2]\hat{\underline{x}} + [C_1 - C_2]\underline{x}\,\hat{d} \tag{2.10}$$

where

$$DA_1 + D'A_2 = \begin{bmatrix} -\frac{R_s\ tD'R_c}{L_s} & -\frac{D'}{N_s} \\ \frac{D'N_s}{L_sC} & \frac{-1}{R_LC} \end{bmatrix}$$

$$DB_1 + D'B_2 = \begin{bmatrix} \frac{D}{N_p} \\ 0 \end{bmatrix}$$

$$A_1 - A_2 = \begin{bmatrix} \frac{R_c}{L_s} & \frac{1}{N_s} \\ -\frac{N_s}{L_sC} & 0 \end{bmatrix}$$

$$B_1 - B_2 = \begin{bmatrix} \frac{1}{N_p} \\ 0 \end{bmatrix}$$

$$DC_1 + D'C_2 = \begin{bmatrix} D' \frac{N_s}{L_s} R_c & 1 \\ D \frac{N_p}{L_p} & 0 \end{bmatrix}$$

$$C_1 - C_2 = \begin{bmatrix} -\frac{N_s}{L_s} (R_c \,//\, R_L) & 0 \\ \frac{N_p}{L_p} & 0 \end{bmatrix}$$

Equivalent Circuit Realization

In order to realize the model into circuit form we need to express the state variables in terms of input and output variables. To do so we need to go back to the perturbed matrix form:

$$y = [dC_1 + d'C_2]\underline{x}$$

soving for v_c:

$$v_c = -d' \frac{N_s}{L_s} R_c \phi + v_o \tag{2.11}$$

$$(V_c + \hat{v}_c) = -(D' - \hat{d}) \frac{N_s}{L_s} R_c (\phi + \hat{\phi}) + (V_o + \hat{v}_o) \tag{2.12}$$

The expression of $\hat{V}_c$ in terms of $\hat{V}_o$ can be derived from eq. (2.12):

$$\hat{V}_c = -D' \frac{N_s}{L_s} R_c \hat{\phi} + \Phi \frac{N_s}{L_s} R_c \hat{d} + \hat{V}_o \tag{2.13}$$

The expression for $\hat{\phi}$ is:

$$\hat{\phi} = \frac{L_s}{N_s} \hat{i} \tag{2.14}$$

Substitute eqs. (2.13) and (2.14) into eq. (2.8), we have:

$$(R_s + DD'R_c)\hat{i} = V_{LS} + \left[\frac{N_s}{N_p} V_I + V_o + I(D - D')R_c\right] \hat{d} + D \frac{N_s}{N_p} \hat{V}_i \tag{2.15}$$

$$\hat{i}_c = D'\hat{i} - I\hat{d} - \frac{1}{R_L} \hat{V}_o \tag{2.16}$$

One of the output, i_p, can be derived from eqs. (2.9) and (2.10):

$$\hat{i}_p = D \frac{N_s}{N_p} \hat{i} + I \frac{N_s}{N_p} \hat{d} \tag{2.17}$$

From eqs. (2.15), (2.16), and (2.17), we can realize the equivalent as illustrated in Fig. 2.2, which is a small signal linear model.

2.2 Power Stage Transfer Function

To derive the transfer function of power stage perform KVL and KCL on fig. 2.2 and write the equations for the two outputs, $\hat{V}_o$ and $\hat{i}_p$, in terms of the two inputs, $\hat{V}_i$ and $\hat{d}$:

$$\hat{V}_o = \frac{R_L(SR_cC + 1) \cdot \frac{D'}{D} V_o[1 - \frac{D}{R_L}(R_e + R_c + sL_e)]}{s^2L_sC(R_L + R_C) + s[L_s + RC(R_L + R_c) + (D')^2 R_LR_cC] + (D')^2 K_L + R} \hat{d}$$

$$+ \frac{DD'\frac{N_s}{N_p} R_L(SR_cC + 1)}{s^2L_sC(R_L + R_c) + S[L_s + RC(R_L + R_c) + (D')^2 R_LR_cC] + (D')^2 R_L + R} \hat{V}_i \tag{2.18}$$

$$\hat{i}_p = \frac{N_s V_o}{(D')^2 R_L N_p} \hat{d} + \frac{DN_s}{D'N_p} \cdot \frac{SR_LC + 1}{R_L(SR_cC + 1)} \hat{v}_o \tag{2.19}$$

where

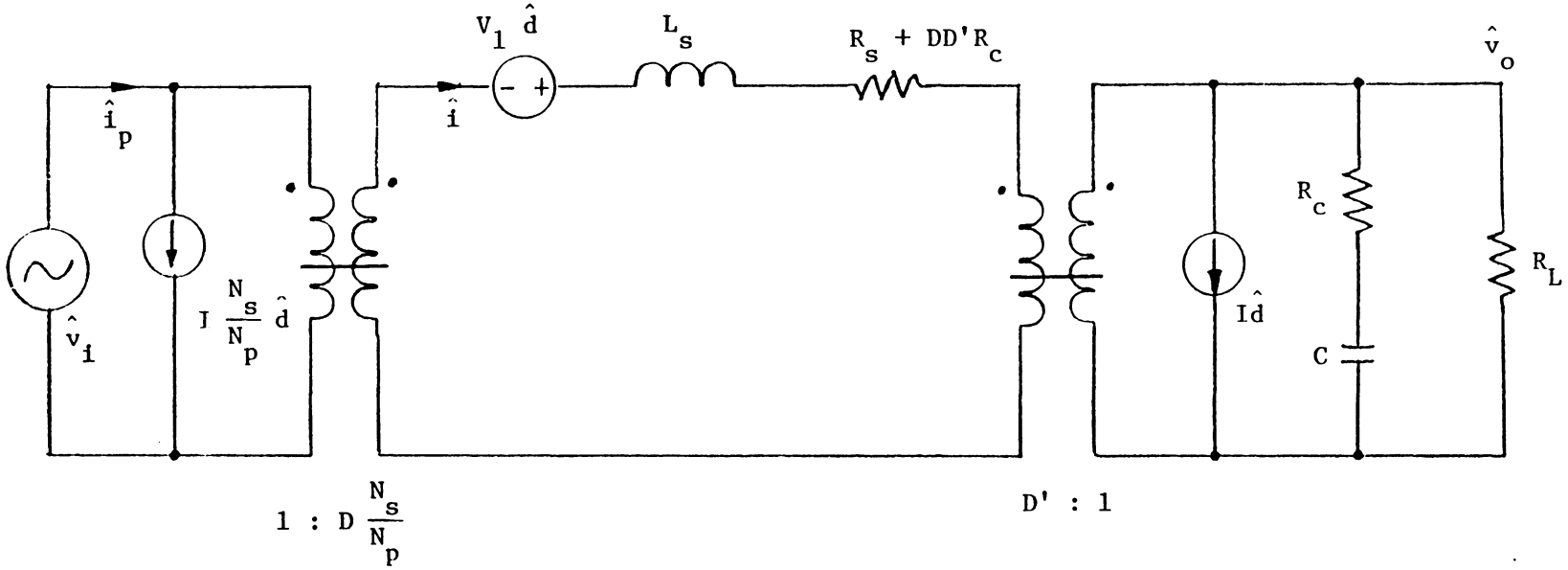


Fig. 2.2 State Space Averaged Power Stage Model

$$(V_1 = \frac{N_s}{N_p} V_I + V_o + I(D - D')R_c)$$

$$R_e = \frac{R_s}{(D')^2} \quad , \quad L_e = \frac{L_s}{(D')^2}$$

and let $\omega_o \triangleq \frac{1}{\sqrt{L_e C}}$ (2.20)

$$y \triangleq \frac{\omega_o}{2} \left[\frac{L_e}{R_L} + (R_e + \frac{R_c}{D'})C \right] \tag{2.21}$$

$$\Delta \triangleq \frac{s^2 + 2y\omega_o s + \omega_o^2}{\omega_o^2} \tag{2.22}$$

Assume $R_c << R_L$, $R_s << R_L$ and $\frac{D}{R_L}(R_e + R_c) << 1$, eqs. (2.18) and (2.19) can be simplified:

$$\hat{V}_o = \frac{V_o}{DD'}(SR_cC + 1)(1 - \frac{DL_e}{R_L}S)\frac{1}{\Delta}\hat{d}$$

$$+ \frac{DN_s}{D'N_p}(SR_cC + 1) \cdot \frac{1}{\Delta}\hat{v}_i \tag{2.23}$$

$$\hat{i}_p = \frac{V_o N_s}{(D')^2 R_L N_p}[\Delta + (SR_cC + 1)(1 - \frac{DL_e}{R_L}S)] \cdot \frac{1}{\Delta}\hat{d}$$

$$+ \left(\frac{DN_s}{D'N_p}\right)^2 \cdot \frac{1}{R_L}(SR_LC + 1) \cdot \frac{1}{\Delta}\hat{V}_i \tag{2.24}$$

Define the following transfer functions:

$$F_{D1} = \frac{V_o}{DD'}(SR_cC + 1) \cdot (1 - \frac{DL_e}{R_L}S) \tag{2.25}$$

$$F_{V1} = \frac{DN_s}{D'N_p}(SR_cC + 1) \tag{2.26}$$

$$F_{p1} = \frac{1}{\Delta} = \frac{\omega_o^2}{s^2 + 2y\omega_o S + \omega_o^2} \tag{2.27}$$

$$F_{D2} = \frac{V_o N_S}{(D')^2 R_L N_P^2} (D'\Delta + SR_L C_{o1} + D + 1)$$

$$F_{V2} = \left(\frac{DN_s}{D'N_p} \right) \cdot \frac{1}{R_L} (SR_L C + 1) \tag{2.29}$$

$$F_{p2} = \frac{1}{\Delta}$$

The block diagram for the power stage is shown in Fig. 2.3.

2.3 Error Processor Model

The error processor, or the analog signal processor (ASP), is a feedback compensation network. It senses the analog signals from output voltage and switching current and provides a compensated error signal to the digital signal processor (DSP).

There are two loops in the ASP: a DC loop, and AC loop. DC loop senses the variation of output voltage, V_o, after compensation and amplification, this error signal, V_x, is to be served as a control voltage in the ASP output error signal when compares to the threshold voltage, E_T. The AC loop senses the switching current and transform the current signal into a proportional voltage signal V_{sw}. This voltage signal combines with V_x generated from DC loop then compares to the threshold voltage, E_T, within the DSP.

Fig. 2.4 shows the two-loop error processor. The transfer function for the DC loop is derived as follows:

The current flows through R1 and R2-C1 branches is equal to the current flows through R3-C2 branch:

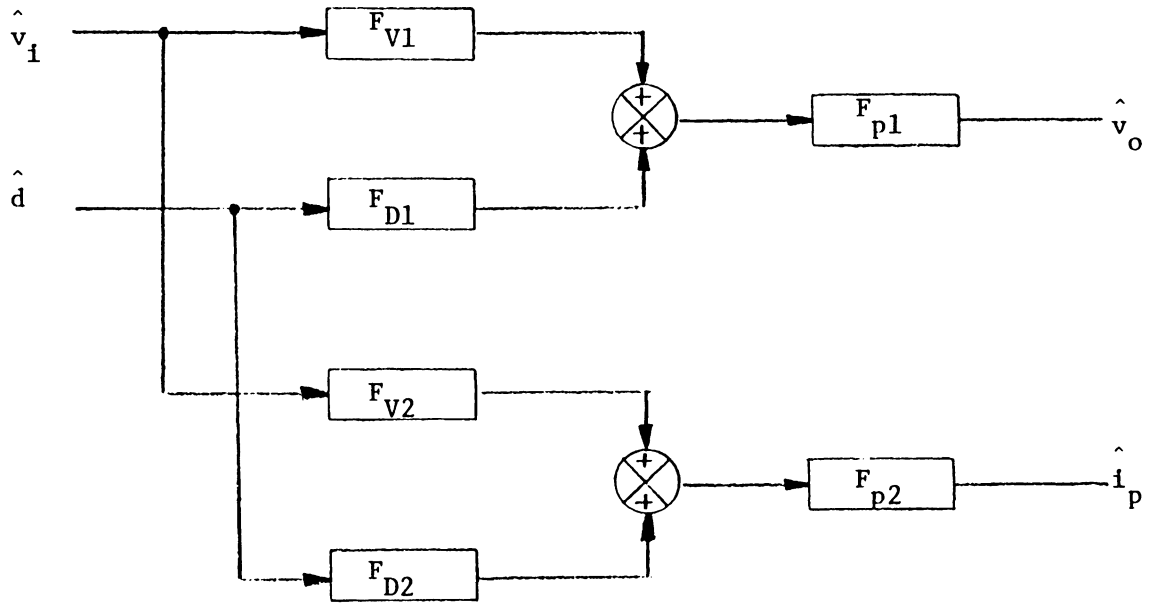


Fig. 2.3 Power Stage Small Signal Block Diagram

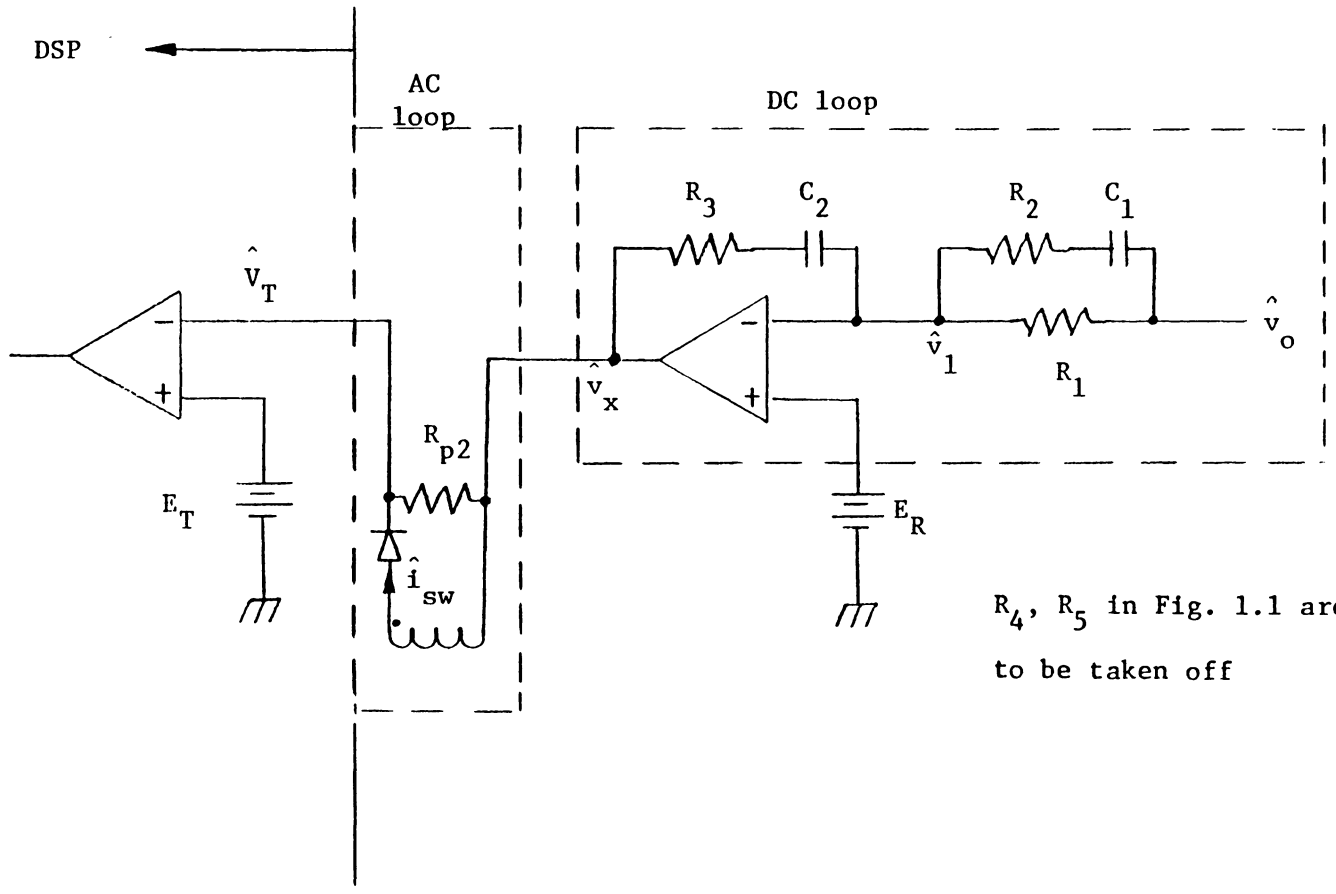


Fig. 2.4 Error Processor

$$\frac{-\hat{v}_o - \hat{v}_1}{R_2 + \frac{1}{SC_1}} + \frac{-\hat{v}_o - \hat{v}_1}{R_1} = \frac{\hat{v}_1 - \hat{v}_x}{R_3 + \frac{1}{SC_2}} \tag{2.31}$$

$\hat{v}_x \simeq -K\hat{v}_1$, where K is the amplification factor of the operational amplifier. (2.32)

Solving for $\hat{v}_x/\hat{v}_o$, assume $\hat{v}_x >> \hat{v}_1$, we obtain:

$$\frac{\hat{v}_x}{\hat{v}_o} = \frac{(SR_3C_2 + 1)[S(R_1 + R_2)C_1 + 1]}{SR_1C_2(SR_2C_1 + 1)} \tag{2.33}$$

Define the DC loop gain for the EP by the following equation:

$$F_{DC} = \frac{(SR_3C_2 + 1)[S(R_1 + R_2)C_1 + 1]}{SR_1C_2(SR_2C_1 + 1)} \tag{2.34}$$

The AC loop transfer function is derived as follows:

$$\hat{v}_{sw} = \hat{i}_{sw} \cdot R_{p2} \tag{2.35}$$

$$\hat{i}_{sw} = \frac{\hat{i}_p}{n} \tag{2.36}$$

$$\frac{v_{sw}}{i_p} = \frac{R_{p2}}{n} \tag{2.37}$$

Define the AC loop gain for the EP by the following equation:

$$F_{AC} = \frac{R_{p2}}{n} \tag{2.38}$$

Fig. 2.5 illustrates the error processor block diagram.

2.4 Duty-Cycle Pulse Modulator Model

The digital signal processor (DSP) converts the analog signal from error processor into a duty cycle pulse train to control the ON-OFF of the power switch. Three kinds of signal are contained in the analog

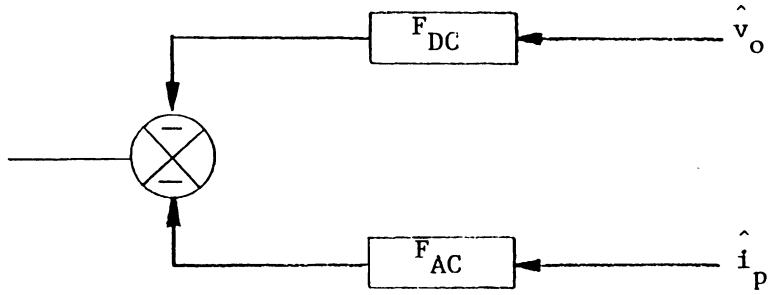


Fig. 2.5 Error Processor Small Signal Block Diagram

output a EP, a DC error signal from converter output, V_x, an AC small amplitude error signal embedded in V_x, V_s and the large-amplitude switching waveform, V_{sw}. As shown in Fig. 2.6, when this combined signal, V_T, intersects a threshold voltage, E_T, T_{OFF} commences. T_{ON} is initiated by a clock, before V_T reaches E_T the duty cycle signal stays high.

As one can see from Fig. 2.6, d(t) is modulated by the small AC disturbance signal. In order to characterize the small signal behavior of pulse modulator we add, externally, a low amplitude sine wave and a DC bias voltage, as illustrated in Fig. 2.7, to simulate the output voltage of DC loop and disconnect the DC loop. By so doing, we can calculate the effects of this simulated disturbance to the duty cycle signal modulation. It should be noted that, after injection of the disturbance signal, not only the duty cycle is modulated so are the two slopes, S_N and S_F, as can be seen in Fig. 2.8.

Let

$$v_s = A \sin \omega t \tag{2.39}$$

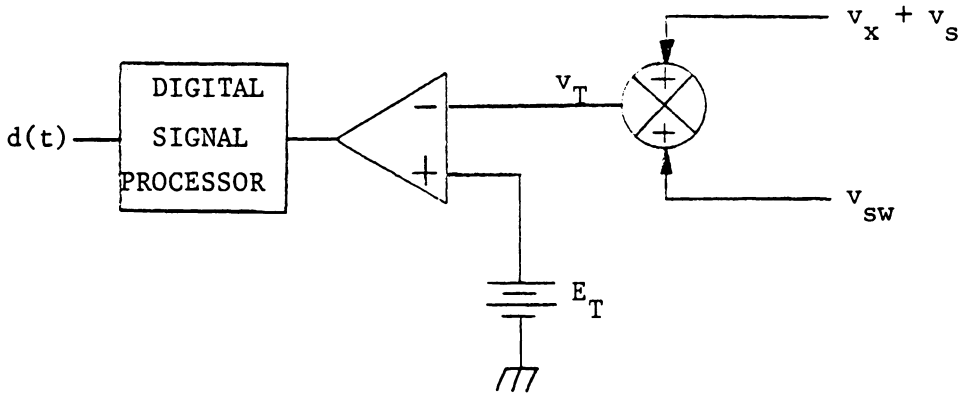
and

$$v_T = v_x + v_s + v_{sw} \tag{2.40}$$

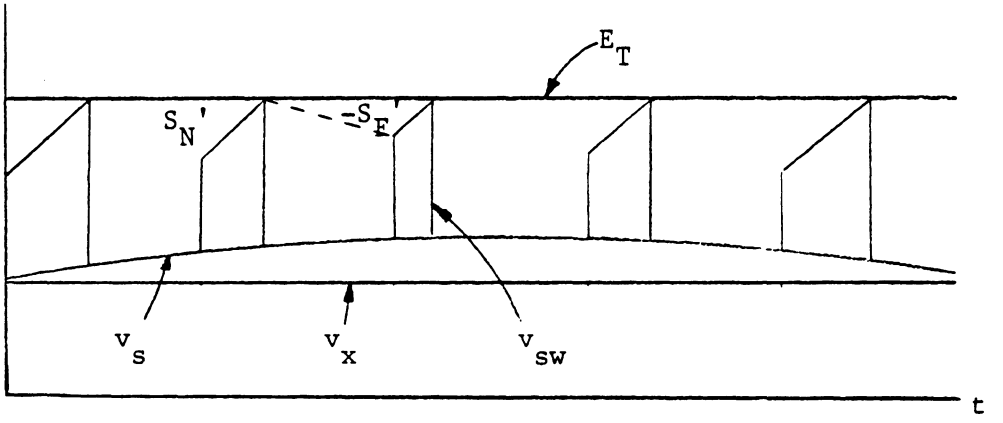
The Fourier series expansions of d(t) and are as follows:

$$\begin{aligned} d(t) &= D + a_1 \sin \omega t + b_1 \cos \omega t + \ldots \\ v_T &= v_T + c_1 \sin \omega t + d_1 \cos \omega t + \ldots \end{aligned} \tag{2.41}$$

The describing function F_M of the pulse modulator is defined as:



(a)



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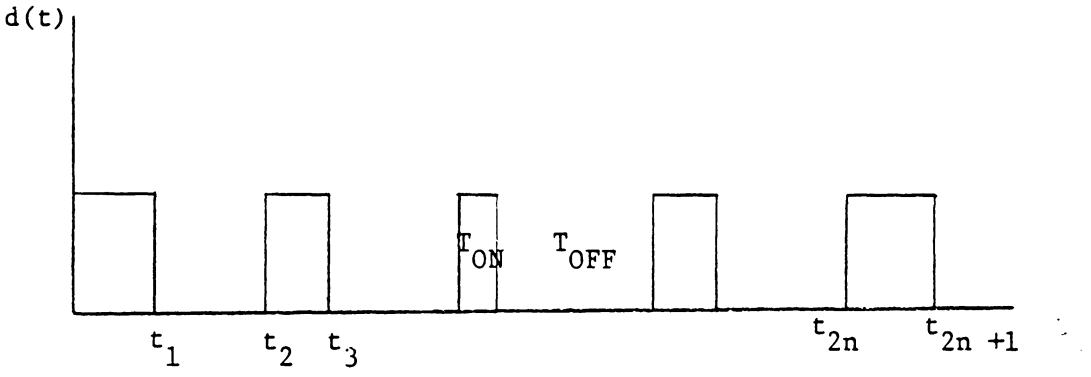


Fig. 2.6 Pulse Modulator

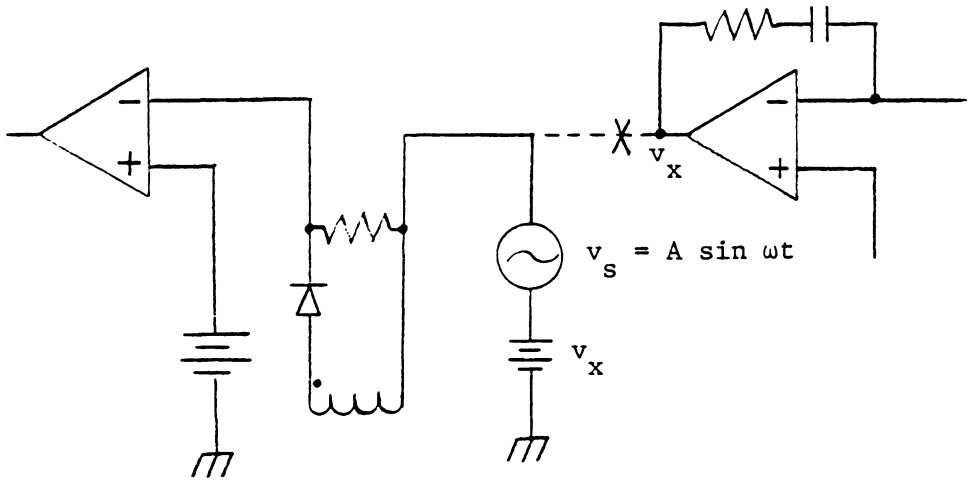
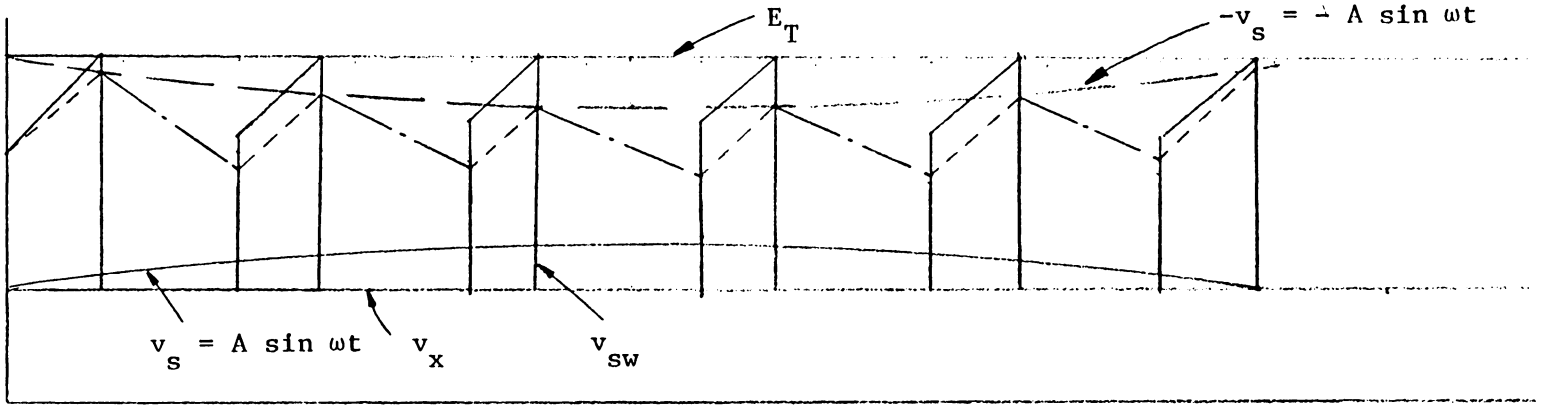
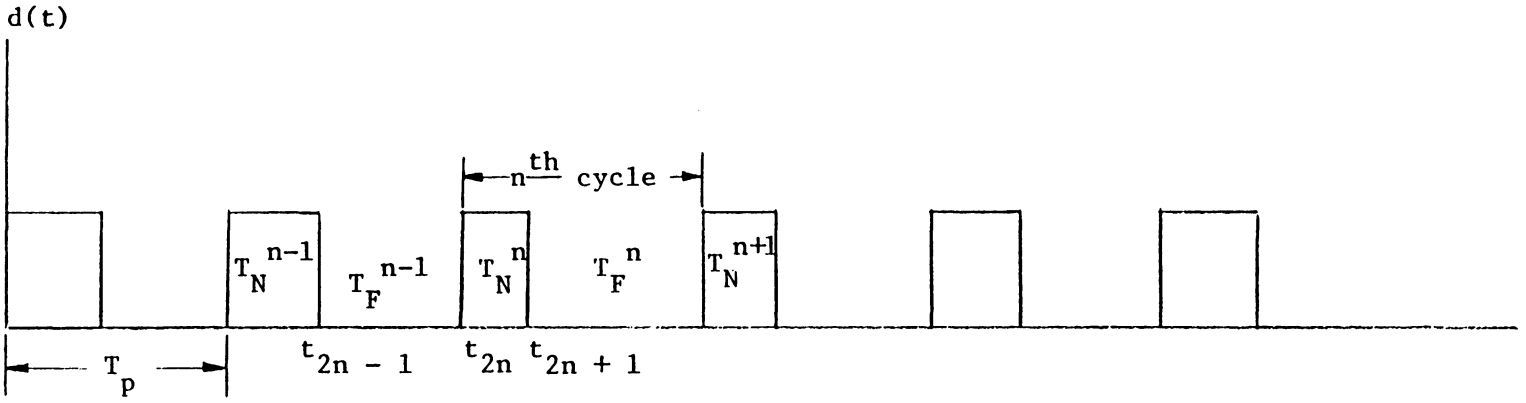


Fig. 2.7 Substitute A New Branch ($v_x + v_s$) To Simulate DC Loop output



(a)



(b)

Fig. 2.8 Perturbed PWM Waveforms

$$F_M \triangleq \frac{\hat{d}}{\hat{V}_t} = \frac{(a_1^2 + b_1^2)^{1/2}}{(c_1^2 + d_1^2)^{1/2}} e^{j\left[\tan^{-1}\frac{b_1}{a_1} - \tan^{-1}\frac{d_1}{c_1}\right]} \tag{2.42}$$

which is derived for constant frequency law without external ramp. The detailed derivation of the coefficients a_1, b_1, c_1 and d_1 will be given Appendix A, after these calculations. F_M can be written as:

$$F_M = \frac{1}{\frac{T_p}{2}(S_N - S_F)} \tag{2.43}$$

where

$$S_N = V_I \frac{R_{p2}}{nL_p}$$

$$S_F = V_I \frac{T_{ON}}{T_{OFF}} \cdot \frac{R_{p2}}{nL_p}$$

or in another form:

$$F_M = \frac{2nL_p}{T_p V_I R_{p2}} \cdot \frac{D'}{D' - D} \tag{2.44}$$

From eq. (2.43) it is noticed that F_M can be negative if

$$S_N < S_F$$

or

$$D > D'$$

which is the inherent limitation of constant frequency control law [10]. The negative F_M together with a negative feedback control will result to an unstable positive feedback system.

To eliminate this situation we can either drive the converter into discontinuous mode or add an external ramp [1, 5] during on time such the new ON-time slope is always greater than the OFF-time slope. The

first remedy is out of this thesis' scope and will not be discussed here.

As for the second method, the derivative procedure of F_M is the same as the without-ramp case [1], the result is:

$$|F_M| = \frac{2}{T_p} \cdot \frac{1}{2S_E + S_N - S_F} \quad \text{(for constant } T_p \text{ with ramp)} \tag{2.45}$$

The effect of the addition of S_E is illustrated in Fig. 2.9. The criteria for adding S_E is to let

$$2S_E + S_N - S_F > 0 \tag{2.46}$$

In other words, for certain duty cycle operating range S_E has to be:

$$S_E > \frac{1}{2}(S_F - S_N)$$

$$= \frac{1}{2} S_N \left(\frac{D_{max}}{D'_{min}} - 1 \right) \tag{2.47}$$

where D_{max} is the maximum duty ratio the converter can run into under certain conditions,

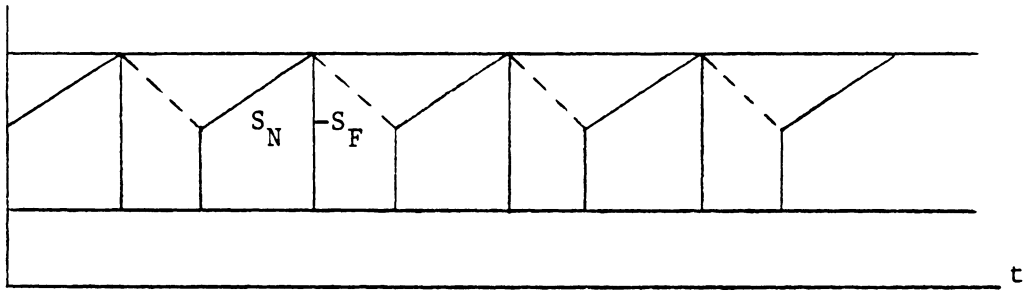
$$D'_{min} = 1 - D_{max}$$

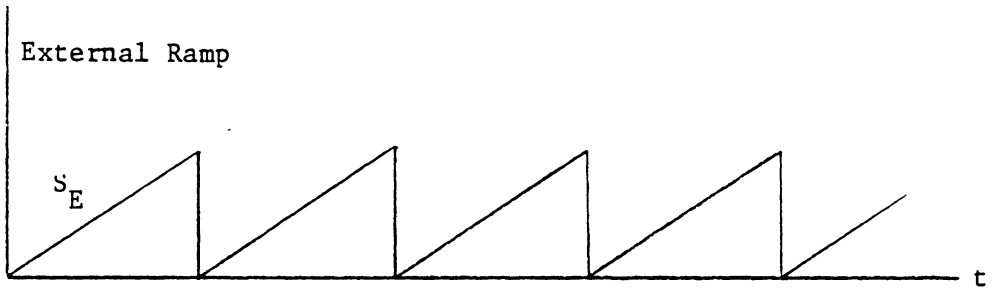
Besides constant frequency, constant T_{OFF} is another control law that can be applied to current-injected control. The describing function for constant T_{OFF} control has been derived in a similar manner in [4] and is given below:

$$F_M = \frac{2}{T_{OFF}} \cdot \frac{1}{S_N + S_F} \quad \text{(for constant } T_{OFF}) \tag{2.48}$$

It is shown in eq. (2.48) that there will be no duty cycle related instability when constant T_{OFF} control law is used.

The describing function for the DSP is illustrated by one block as shown in Fig. 2.10





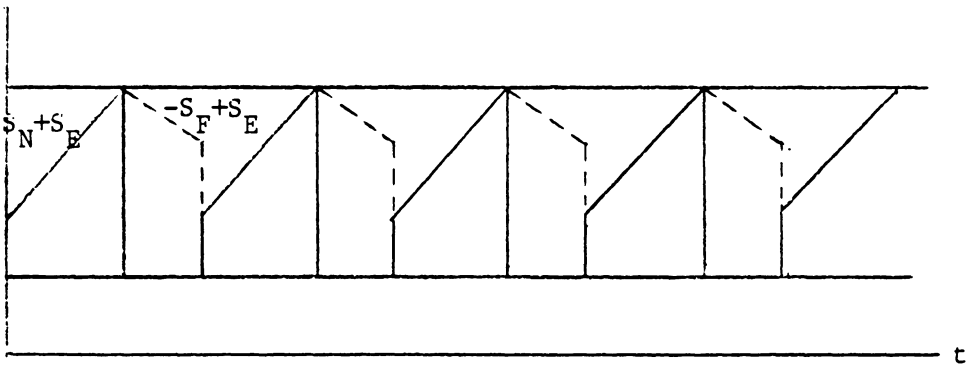


Fig. 2.9 Adding an External Ramp to Prevent Negative F_M

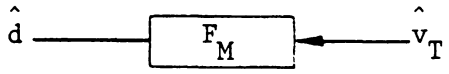


Fig. 2.10 Digital Signal Processor Small Signal Block Diagram

2.5 Small Signal Block Diagram Representative

Sections 2.2, 2.3, and 2.4 have provide the low frequency small signal characterizations of the current-injec controlled switching regulator three functional blocks: the power stage, the error processor and the duty cycle pulse modulator. Based on the power stage block diagram of Fig. 2.3, the error processor block diagram of Fig. 2.5 and the pulse modulator block diagram of Fig. 2.10, a complete system block diagram operating under constant frequency or constant T_{OFF} duty cycle control law can be shown in Fig. 2.11.

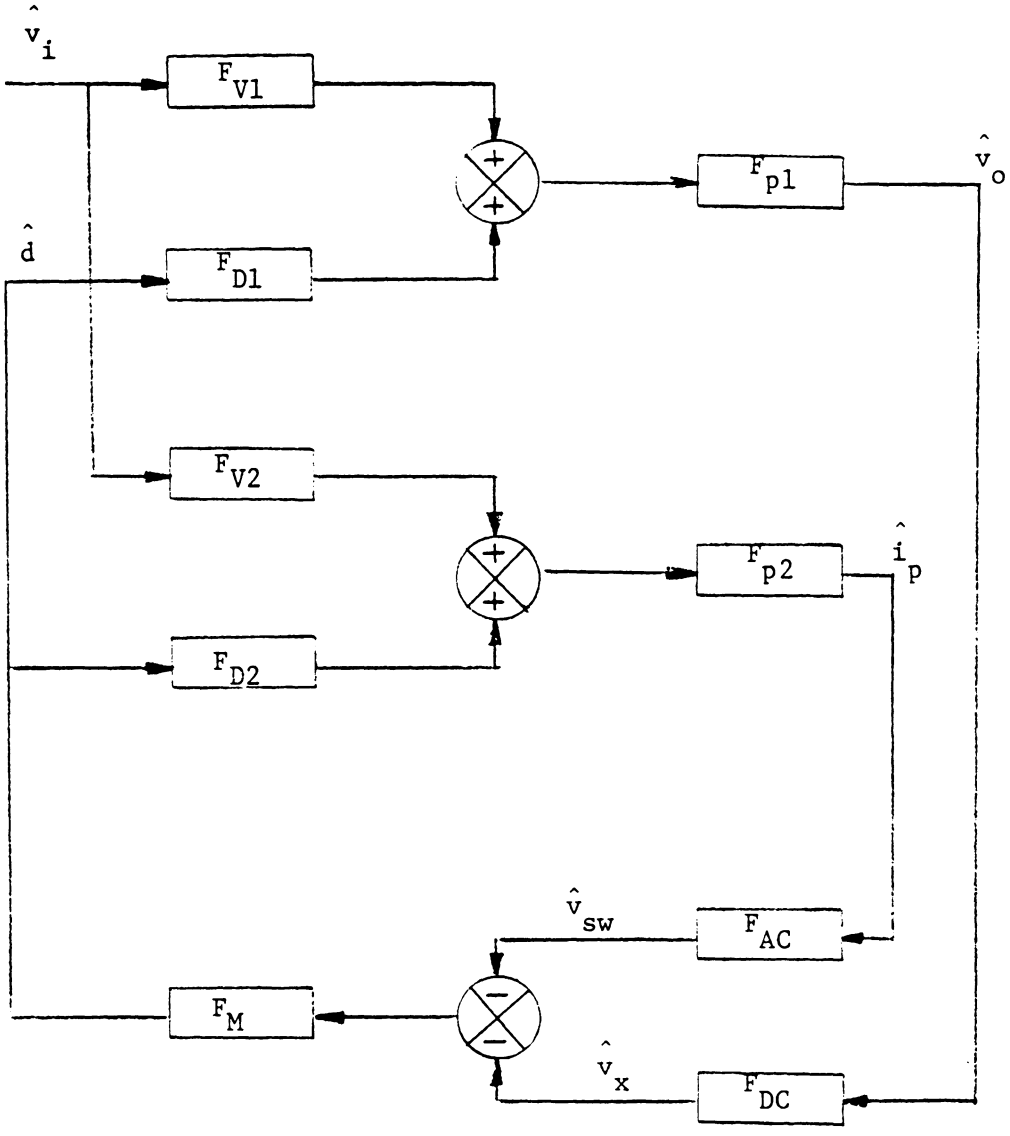


Fig. 2.11 System Small Signal Block Diagram

CHAPTER III

ANALYSIS OF CURRENT-INJECTED CONTROL EMPLOYING SIMPLE GAIN COMPENSATIONS

Due to the complex interdependency of various parameters in the control loops, it is often difficult to pinpoint the exact function and property of each critical control circuit parameter without considering its interaction with other circuit parameters. It is found, in general, that the improvement of one regulator performance characteristic by changing specific control parameters often accompanies with severe degradation of other performance characteristics. Due to the complex interaction of control parameters, bench design with trial and error techniques seldom results in an optimal design. An understanding of the basic characteristics of the current-injected control has to be reached before any control optimization is attempted.

In this chapter, we shall analyze the control starting from the simplest case -- the basic current-injected control with only gain compensation and no lead-lag compensation network. After the basic nature and deficiency of such a control scheme is understood, additional compensation network is added to the basic control loops. Improvements of regulator performances can then be singled out with the added control parameters.

Fig. 3.1 illustrates the simple gain compensation. In this chapter and the following two chapters, Bode analysis technique is employed to investigate the open-loop gain and phase.

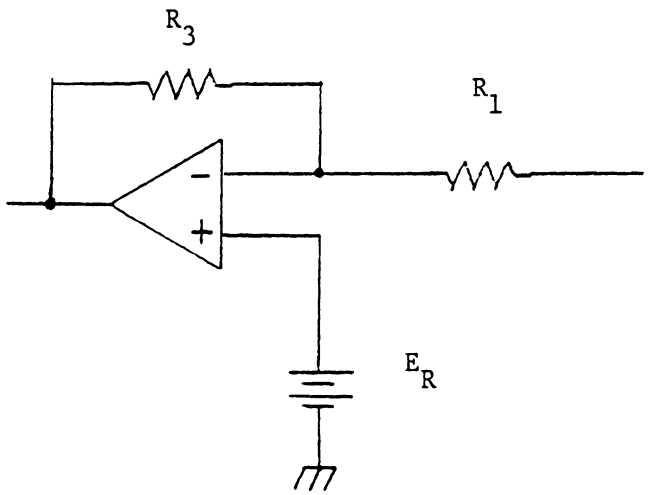


Fig. 3.1 SIMPLE GAIN COMPENSATION

3.1 Open-Loop Characteristics

System stability is characterized by the system open loop performance. For a multi-loop control system, the loop should be opened at a place common to all feedback paths.[1] By opening the loop at the place shown in Fig. 3.2, the open-loop transfer function can be derived:

$$G_T = \frac{F_M}{\Delta}\left[F_{DC}\,F_{D1} + F_{AC}\,F_{D2}\right] \tag{3.1}$$

Note that F_{DC} would be different from eq. (2.34) in this case, the new F_{DC} is:

$$F_{DC} = R_3/R_1 \tag{3.2}$$

Substitute eqs. (2.22), (2.25), (2.28) and (3.2) into the above expression, the following formulation results:

$$G_T = F_M \cdot \omega_0^{\,2} \cdot \frac{V_0}{D'} \cdot \frac{S^2 K_1 + SK_2 + K_3}{S^2 + 2\zeta\omega_0 S + \omega_0^{\,2}} \tag{3.3}$$

where

$$K_1 = \frac{1}{R_L \omega_0^{\,2}}\left(F_{AC}\frac{N_S}{N_P} - \frac{R_3 R_c}{R_1}\right)$$

$$K_2 \cong \frac{R_3}{D\,R_1}\left(R_c C - \frac{D\,L_e}{R_L}\right) + \frac{F_{AC} N_S}{D' N_P} C, \text{ assume } R_L C >> \frac{2\zeta D'}{\omega_0}$$

$$K_3 = \frac{R_3}{DR_1} + \frac{2F_{AC}N_S}{D'R_L N_P}\,.$$

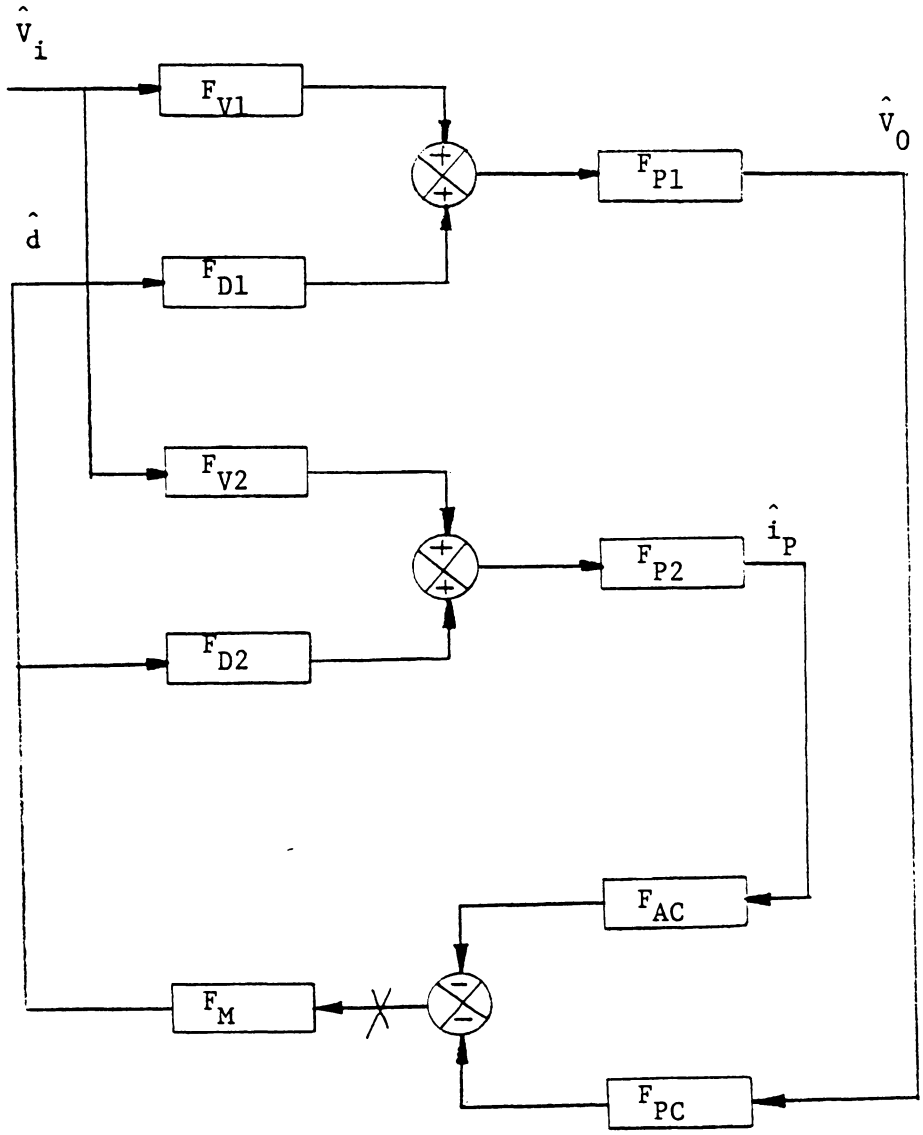


Fig. 3.2 LOOP-OPENING FOR DERIVATION OF OPEN-LOOP TRANSFER FUNCTION

The numerator of eq. (3.3) can be expressed in terms of two zeros, S_{01} and S_{02}:

$$G_T = F_M \cdot \omega_0^2 \cdot \frac{V_0}{D'} \cdot K_3 \cdot \frac{(S/S_{01} + 1)(S/S_{02} + 1)}{S^2 + 2\zeta\omega_0 S + \omega_0^2} \tag{3.4}$$

and $$\frac{1}{S_{01} \cdot S_{02}} = \frac{K_1}{K_3}$$

$$\frac{1}{S_{01}} + \frac{1}{S_{02}} = \frac{K_2}{K_3}$$

If S_{01} and S_{02} are sufficiently apart, i.e. $1/S_{01} >> 1/S_{02}$ (choose S_{01} to be the smaller zero), the following approximations hold true:

$$1/S_{01} \simeq K_2/K_3 \tag{3.5}$$

$$1/S_{02} \simeq K_1/K_2 \tag{3.6}$$

Substitute the expressions of K_1, K_2 and K_3 into eqs. (3.5), (3.6) then S_{01} and S_{02} can be expressed in terms of circuit parameters:

$$S_{01} \simeq \frac{\frac{R_3}{DR_1} + \frac{2F_{AC}N_S}{D'R_L N_P}}{\frac{R_3}{DR_1}(R_c C - \frac{DL_e}{R_L}) + \frac{F_{AC} N_S}{D'N_P} C} \tag{3.7}$$

$$S_{02} \simeq R_L\omega_0^2 \cdot \frac{\frac{R_3}{DR_1}(R_c C - \frac{DL_e}{R_L}) + \frac{F_{AC}N_S}{D'N_P} C}{F_{AC}\frac{N_S}{N_P} - \frac{R_3 R_c}{R_1}} \tag{3.8}$$

Which are two rather complicated equations. However, there exists only two key control related parameters in these equations. One is the DC gain, R_3/R_1, the other one is AC gain, F_{AC}. The rest of the terms in (3.7) and (3.8) are related to power stage parameters that are assumed to be given before our analysis on the control loop.

The characteristic of open-loop gain can now be illustrated by the asymptotic curve as shown in Fig. 3.3.

The open-loop gain in each frequency range is approximated by the following equations if all corner frequencied are sufficiently apart:

$$S < \omega_0 \qquad G_T \simeq F_M \cdot \omega_0^2 \cdot \frac{V_0}{D'} \cdot K_3 \cdot \frac{1}{\omega_0^2}$$

$$= F_M \cdot \frac{V_0}{D'} \cdot \left(\frac{R_3}{DR_1} + \frac{2F_{AC}N_S}{D'R_LN_P} \right) \tag{3.9}$$

$$\omega_0 < S < S_{01} \quad G_T \simeq F_M \cdot \omega_0^2 \cdot \frac{V_0}{D'} \cdot K_3 \cdot \frac{1}{S^2 + 2\zeta\omega_0 S + \omega_0^2}$$

$$= F_M \cdot \frac{V_0}{D'} \cdot \left(\frac{R_3}{DR_1} + \frac{2F_{AC}N_S}{D'R_LN_P} \right) \cdot \frac{\omega_0^2}{S^2 + 2\zeta\omega_0 S + \omega_0^2} \tag{3.10}$$

$$S_{01} < S < S_{02} \quad G_T \simeq F_M \cdot \omega_0^2 \cdot \frac{V_0}{D'} \cdot K_3 \cdot \frac{S/S_{01}}{S^2 + 2\zeta\omega_0 S + \omega_0^2}$$

$$= F_M \cdot \frac{V_0}{D'} \cdot \left[\frac{R_3}{DR_1} \left(R_c C - \frac{DL_e}{R_L} \right) + \frac{F_{AC}N_S}{D'N_P} C \right] \cdot \frac{S\,\omega_0^2}{S^2 + 2\zeta\omega_0 S + \omega_0^2}$$

(3.11)

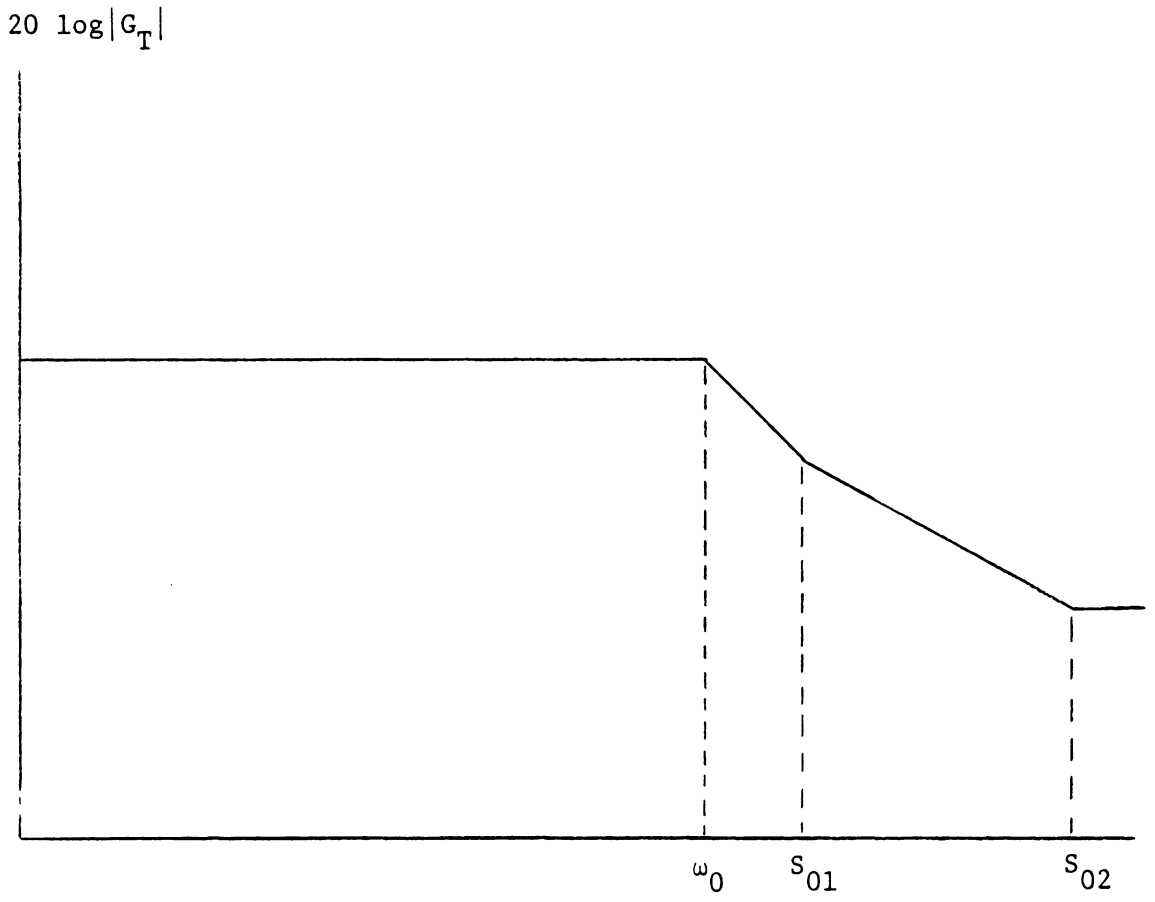


Fig. 3.3 ASYMPTOTIC CURVE OF G_T

$$S > S_{02} \qquad G_T \simeq F_M \cdot \omega_0^2 \cdot \frac{V_0}{D'} \cdot K_3 \cdot \frac{S/S_{01} \cdot S/S_{02}}{S^2}$$

$$= F_M \cdot \frac{V_0}{D'R_L} \cdot \left(F_{AC} \frac{N_S}{N_P} - \frac{R_3 R_c}{R_1}\right) \tag{3.12}$$

Substitute the actual circuit parameter values, Table 3.1, into eq. (3.3), we obtain the computer plot of open-loop gain and phase shown in Fig. 3.4(a) and (b). The computer program is listed in Appendix B.

3.2 Stability Criteria and Constraints

Examining eqs. (3.7) and (3.8), we notice that both equations consist of negative terms in their denominators which can be crucial to the stability of the system. For example, if the negative term in S_{01} becom predominant such that the denominator is negative under this condition, S_{01} will be a positive zero. Likewise, S_{02} can be a positive zero. Each positive zero will give 90° phase delay compared to a negative zero which boosts the phase by 90°. Hence the system can be greatly degraded due to the existence of a positive zero. To ensure the non-existance of a positive zero the following two constraints must be satisfied.

$$F_{AC} \frac{N_S}{N_P} - \frac{R_3 R_c}{R_1} > 0,$$

$$\frac{R_3}{DR_1}\left(R_c C - \frac{DL_e}{R_L}\right) + \frac{F_{AC} N_S C}{D'N_P} > 0$$

The above two constraints can be rewritten as:

$$\text{first constraint:} \quad F_{AC} \frac{N_S}{N_P} > \frac{R_3 R_c}{R_1} \tag{3.13}$$

$$\text{second constraint:} \quad F_{AC} \frac{N_S}{N_P} > \frac{R_3 R_c}{R_1} \left(\frac{D'L_e}{R_L R_c C} - \frac{D'}{D}\right) \tag{3.14}$$

TABLE 3.1

CIRCUIT PARAMETER VALUES USED

$V_I = 23$ V

$V_0 = 5.2$ V

$N_P = 22$ turns

$N_S = 10$ turns

$T_P = 2 \times 10^{-5}$ sec

$L_P = 40$ μH

$L_S = L_P \times (N_S/N_P)^2$ μH

n = 300 turns

$R_S = 0.013$ Ω

$R_c = 0.07$ Ω

$R_L = 1.69$ Ω

$R_1 = 10.5$ KΩ

$R_2 = 1$ KΩ

$R_3 = 4.42$ KΩ

$C_1 = 0.1$ μF

$$D = \frac{V_0 N_P}{V_I N_S + V_0 N_P}$$

$D' = 1-D$

$R_e = R_S/(D')^2$

$L_e = L_S/(D')^2$

C = 660μF

$C_2 = 0.1$ μF

$R_{P2} = 53.6$ Ω

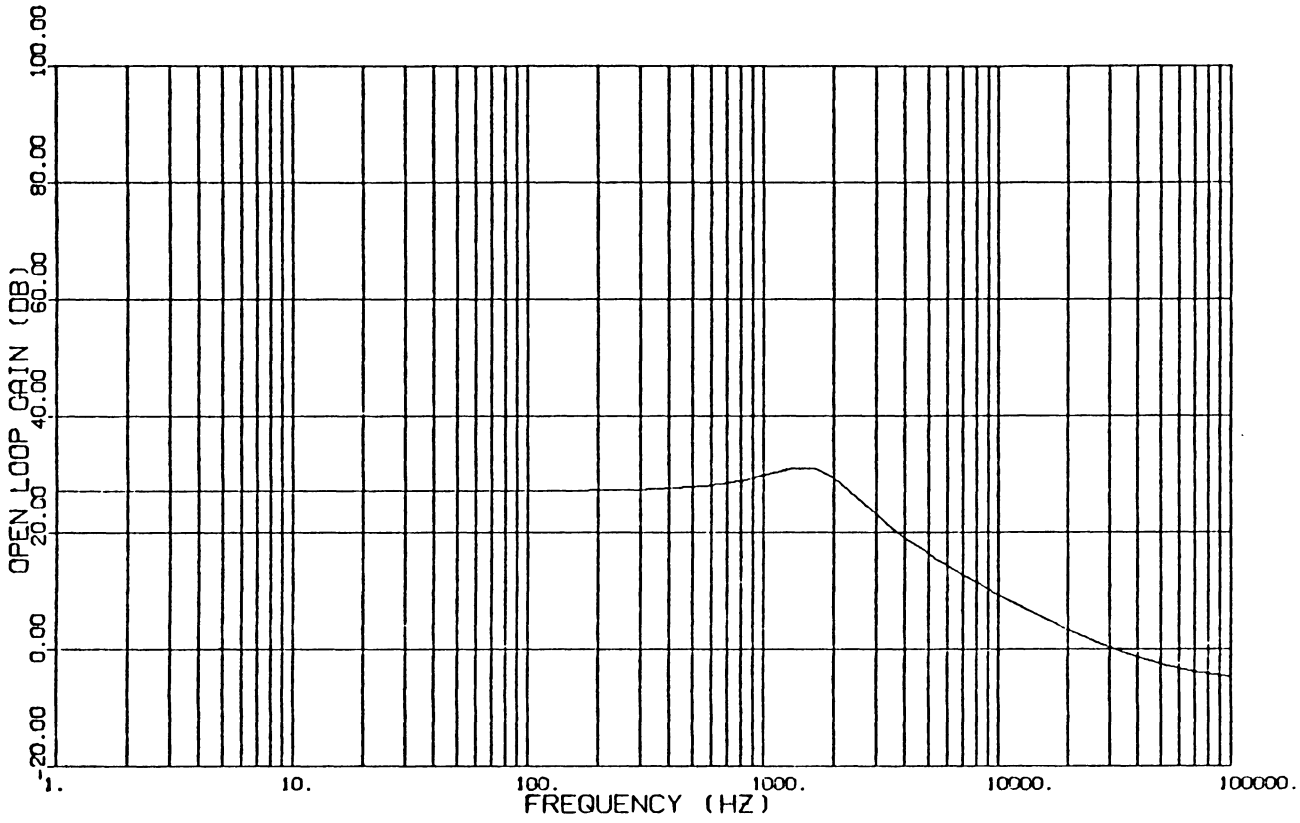


Fig. 3.4(a) OPEN-LOOP GAIN USING GAIN COMPENSATION

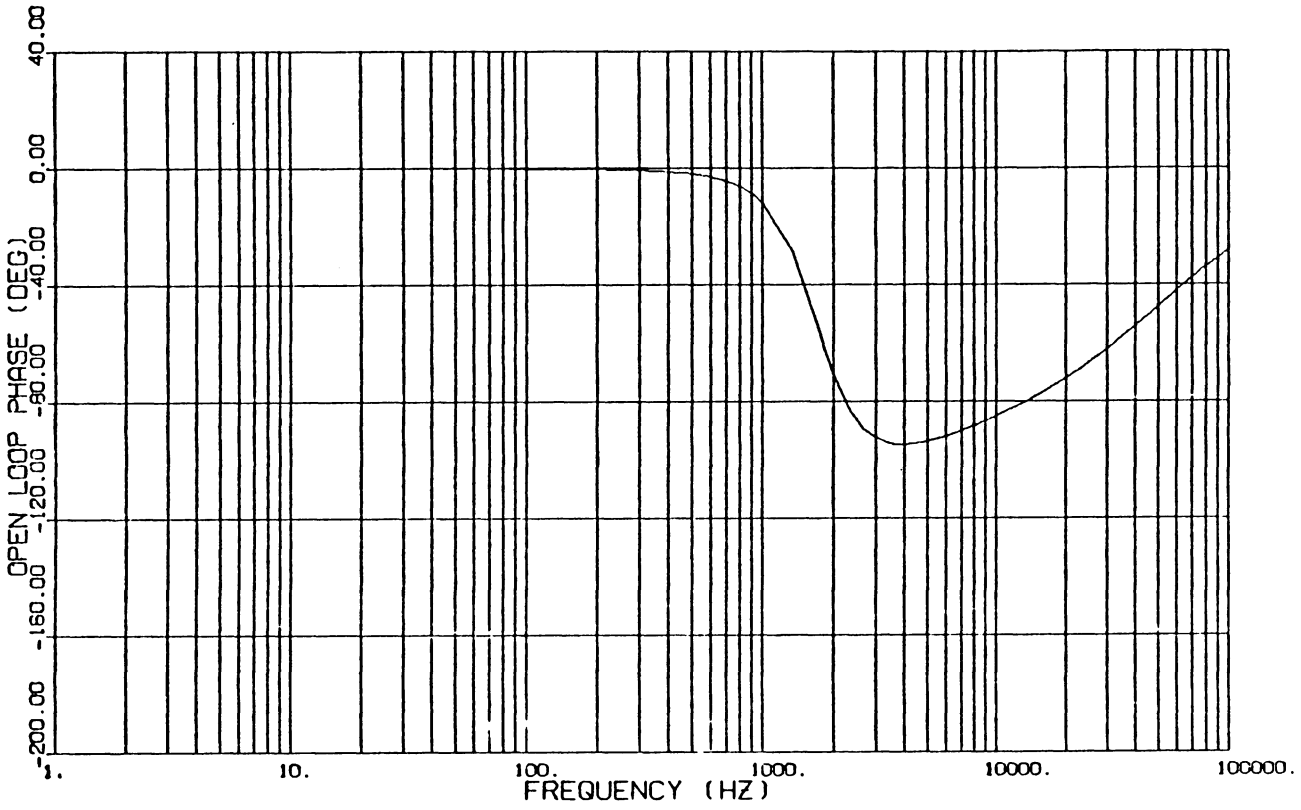


Fig. 3.4(b) OPEN-LOOP PHASE USING GAIN COMPENSATION

The relation between these two constraints depends on the terms in the parentheses of eq. (3.14). The first constraint is not necessarily tighter than the second one or vice versa.

To illustrate this point, we can draw a root locus diagram to show how the two zeros are affected by the constraint. Choose F_{AC} as variabl and substitute parameter values into eqs. (3.13) and (3.14), then F_{AC} has to be greater than 0.065 to satisfy (3.13). (First constraint is now tighter than the second one.) Fig. 3.5(a) shows as F_{AC} decreases from 0.08 to 0.06 S_{02} moves from left half S-plane (negative zero) to right half plane (positive zero). The motion of S_{01} is relatively Fig. 3.5(b) shows an enlarged picture to illustrate the movement of S_{01}.

It is interesting to note that the above two constraints in fact states the necessary relation between the dc loop gain ($F_{DC}F_{D1}/\Delta$) and the ac loop gain ($F_{AC}F_{D2}/\Delta$) at high frequencies. Upon examination of the following relations.

$$\text{AC loop gain } G_{AC} = F_{AC} \cdot F_{D2}/\Delta$$

$$= F_{AC} \cdot \frac{V_0 N_S \cdot \omega_0^2}{(D')^2 F_L N_P} \cdot \frac{s^2 \frac{D'}{\omega_0^2} + (R_L C + \frac{2\zeta D'}{\omega_0})s + 2}{s^2 + 2\zeta\omega_0 s + \omega_0^2}$$

The gain at high frequencies when $S >> S_{02}$

$$G_{AC}\Big|_{S >> S_{02}} \simeq F_{AC} \cdot \frac{V_0 N_S}{D' R_L N_P}$$

$$\text{DC loop gain } G_{DC} = F_{DC} \cdot F_{D1}/\Delta$$

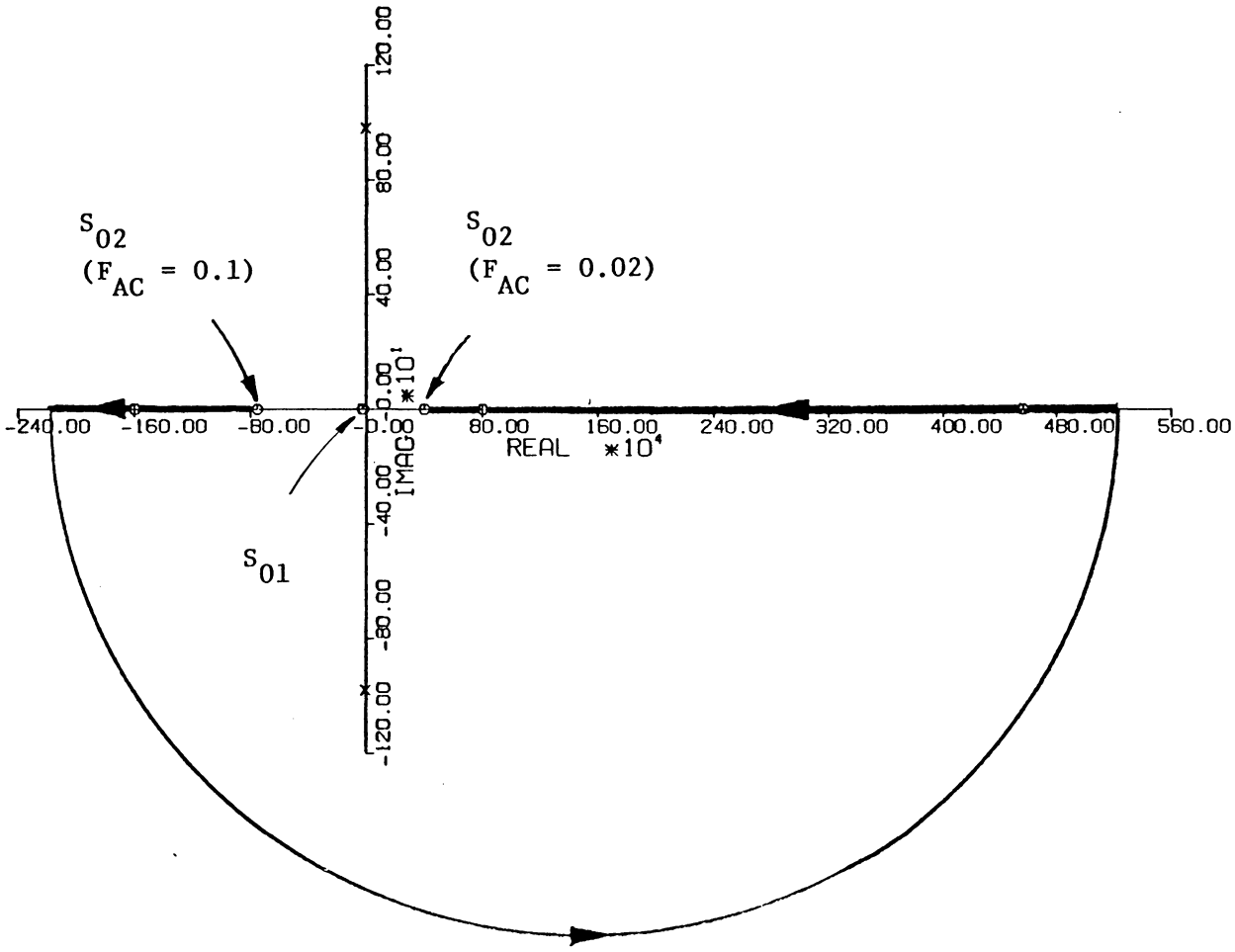


Fig. 3.5(a) MOVEMENT OF S_{02} CORRESPONDING TO F_{AC} CHANGE
(F_{AC} = 0.1, 0.08, 0.06, 0.04, 0.02)

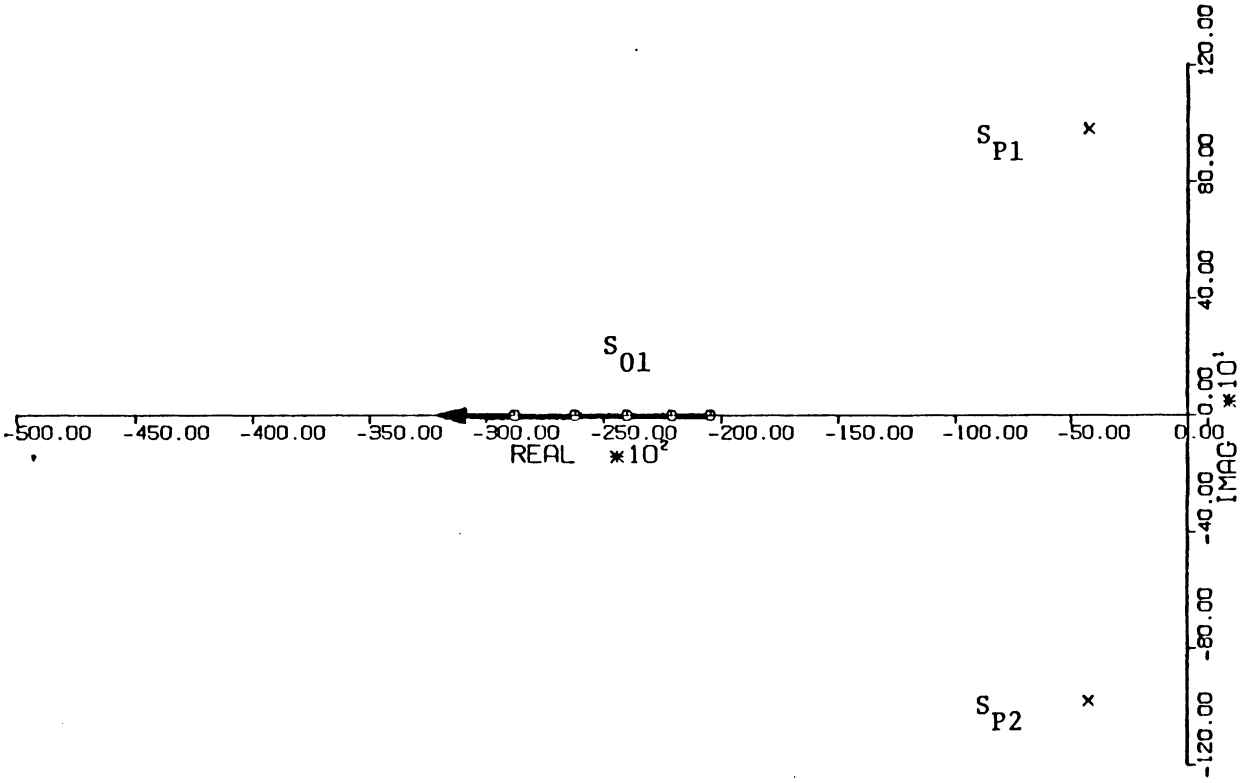


Fig. 3.5(b) MOVEMENT OF S_{01} CORRESPONDING TO F_{AC} CHANGE

$$= \frac{SR_3C_2 + 1}{SR_1C_2} \cdot \frac{V_0\omega^2}{DD'} \cdot \frac{\left|(SR_cC + 1) \cdot (1 - \frac{DL_e}{R_L} \cdot S)\right|}{S^2 + 2\zeta\omega_n S + \omega_0^2}$$

$$G_{DC}\Big|_{S >> S_{02}} \simeq \frac{V_0}{D'R_L} \cdot \frac{R_3R_c}{R_1}$$

and let AC loop gain be greater than DC loop gain:

$$G_{AC}\Big|_{S >> S_{02}} > G_{DC}\Big|_{S >> S_{02}}$$

i.e. $$F_{AC} \frac{V_0N_S}{D'R_LN_P} > \frac{V_0}{D'R_L} \cdot \frac{R_3R_c}{R_1}$$

or

$$F_{AC} \frac{N_S}{N_P} > \frac{R_3R_c}{R_1} .$$

This inequality relation is identical to that of equation (3.13). This is exactly what Fig. 3.6 shows, which is the explaination of the constraint from the Bode analysis viewpoint. Fig. 3.6(a) shows the AC loop gain intersects DC loop gain at high frequency when F_{AC} increases from 0.06 to 0.08.

3.3 Effects of DC-Loop Gain

Examining Fig. 3.4, we note that there are severe drawbacks in the system, primarily due to the low-frequency loop gain. A high gain in DC to low frequency range is necessary to provide good DC regulation and attenuate low-frequency audio noise from both input and output.

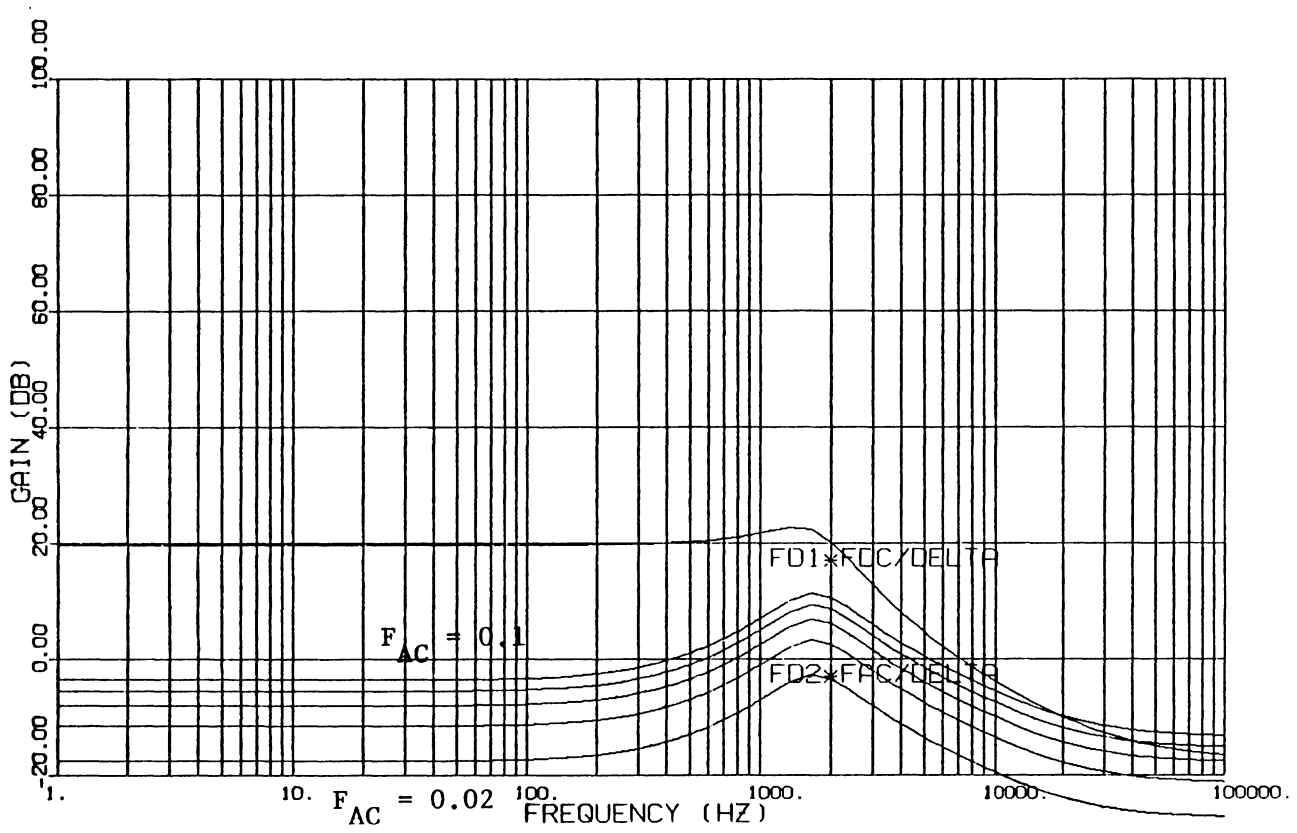


Fig. 3.6(a) AC LOOP GAIN AND DC LOOP GAIN

(F_{AC} = 0.1, 0.08, 0.06, 0.04, 0.02)

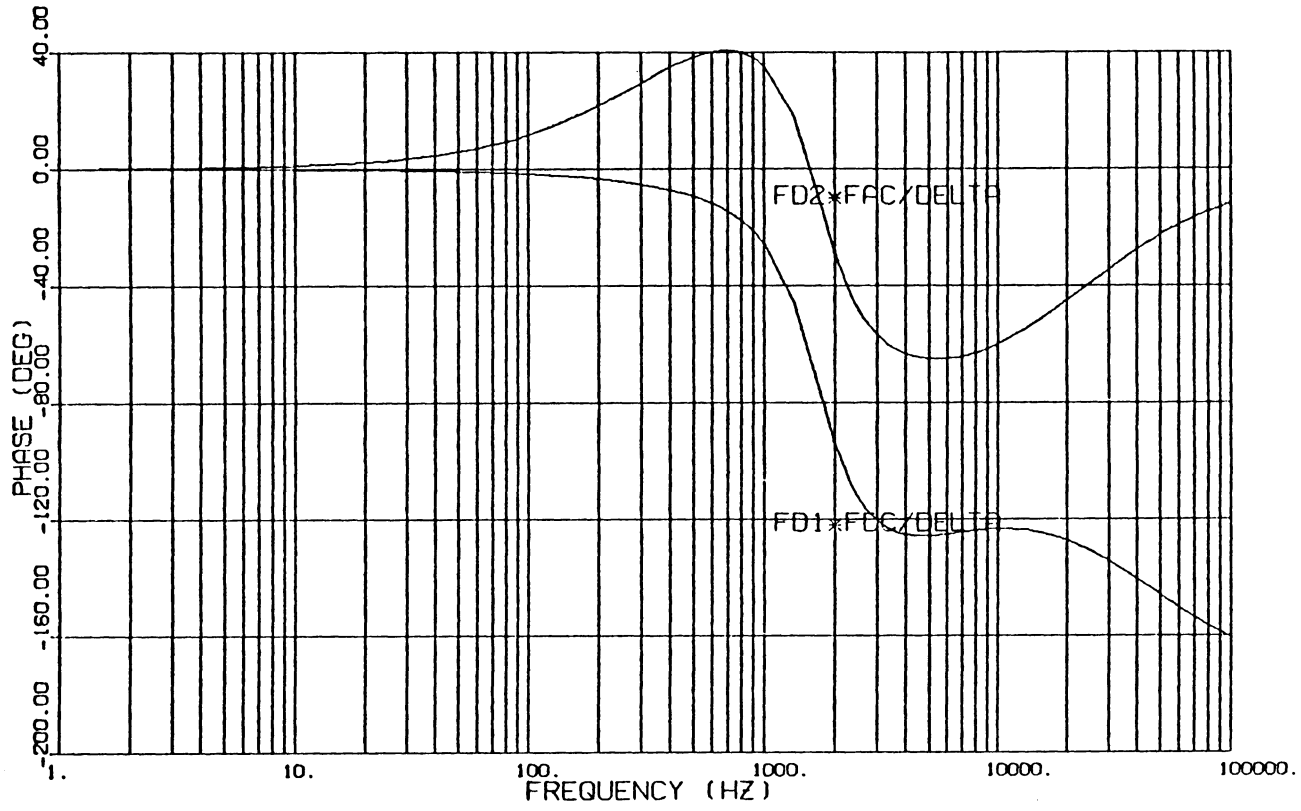


Fig. 3.6(b) AC LOOP PHASE AND DC LOOP PHASE

High DC to low frequency gain can be easily achieved by increasing the gain of the DC feedback loop. Second, the phase drops sharply after the output filter resonant frequency. This could result to inadequate phase margin. If S_{01} moves further to the right the system could be oscillatory due to excessive phase delay.

At this point we wish to note two desirable performance characteristics to be achieved for control loop design:

- low-frequency gain as high as possible so that DC regulation, audiosusceptibility and output impedance can be better,
- S_{01} to be sufficiently low so that phase lag is as small as possible.

To achieve high loop gain, it is obvious from eq. (3.9) that high DC loop gain (R_3/R_1) and/or high AC loop gain (F_{AC}) are necessary. In practice, the magnitude of second term of (3.9) contributed by AC loop is much smaller than the first term. Therefore the low-frequency gain is predominantly determined by DC loop gain.

Increase of DC loop gain by increasing R_3/R_1 has the following consequencies:

- increase of the open-loop gain G_T at frequencies below S_{02},
- decrease of the open-loop gain at frequencies higher than S_{02},
- increase of S_{01},
- increase of S_{02}.

Note that the second and fourth results are correct only if (3.13) and (3.14) are not violated. As R_3/R_1 increases to the extent that the constraints are violated, S_{02} and G_T at high frequencies as shown in (3.12) become negative . These phenomena

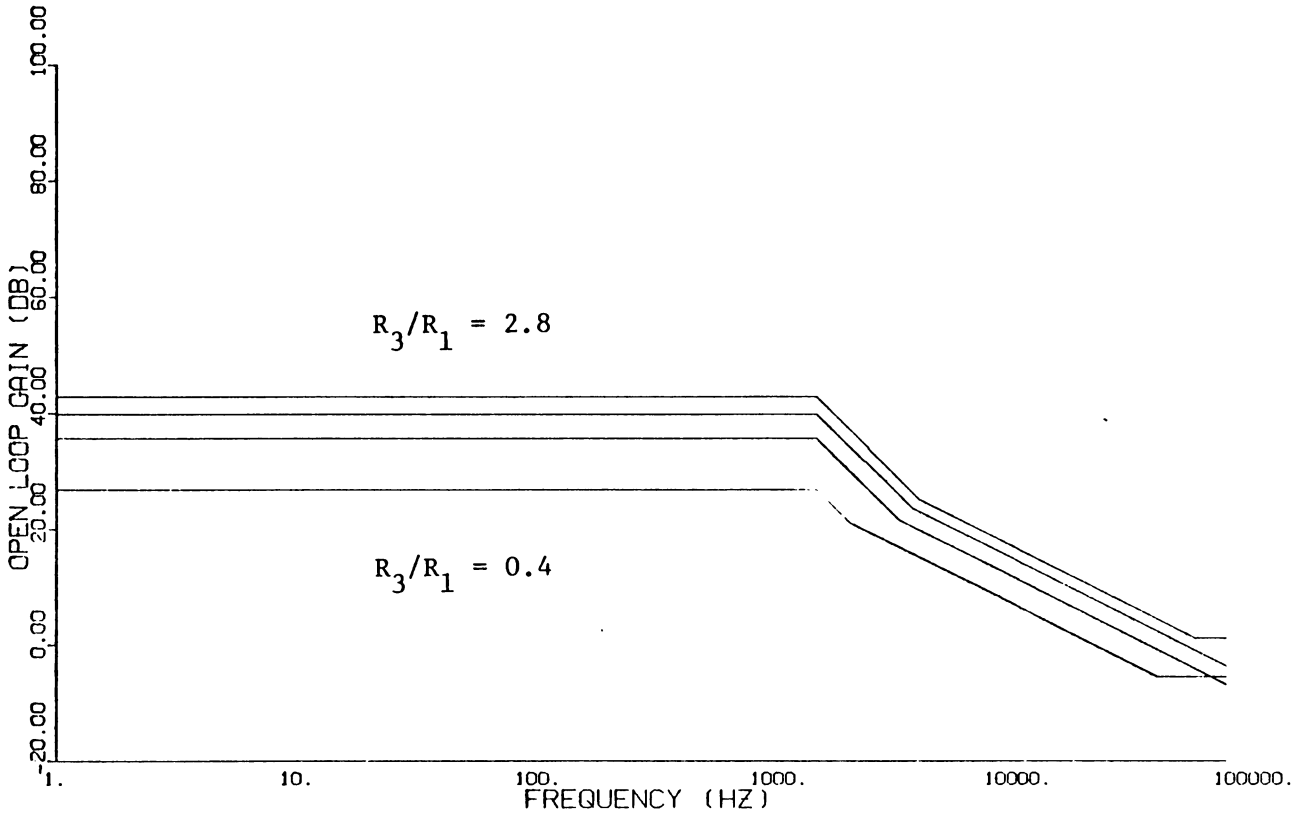


Fig. 3.7 ASYMPTOTIC CURVES SHOWING EFFECTS OF DC-LOOP GAIN (R_3/R_1 = 2.8, 2.0, 1.2, 0.4)

can be illustrated in Fig. 3.7, the asymptotic curves of G_T, and in Fig. 3.8, the gain and phase plots of G_T. Fig. 3.8 (b) shows as DC loop gain exceeds AC loop gain at high frequencies S_{02} becomes positive zero and phase starts to drop to -180° instead of rising up to 0°.

From the previous discussion, increase DC loop gain will boost low frequency gain and expand system bandwidth to a small extent and beyond that further increase of DC loop gain can result to excessive phase delay due to a positive zero.

3.4 Effects of AC Loop gain

It may appear that one could simultaneously increase F_{AC} and R_3/R_1 in order to satisfy the constraints (3.13) and (3.14). A closer examination would indicate that the duty cycle modulator gain F_M is inversely proportional to F_{AC}. An increase of F_{ac} will invariably result in a reduction of F_M and thus a reduction of the overall loop gain.

In addition, an increase in AC loop gain F_{AC} will cause both S_{01} and S_{02} to decrease. Figs. 3.9 and 3.10 illustrate the effects of increasing F_{AC}. From the point of view of system stability, the AC loop serve an important function. If the AC loop gain is sufficiently large that both constraints (3.13) and (3.14) are satisfied, it can shift the positive zero, originated from the power stage, to the left half s-plane. The above described important observation can be verified in three ways: 1) comparing Fig. 3.6 (b) to Fig. 3.4 (b), the AC loop gain dominates DC loop gain at high frequencies.

As a result, it causes the system open loop phase to follow that of the AC loop shown in Fig. 3.6 (b) rather than to follow the down-going phase of DC loop. 2) In Fig. 3.5 (a), as F_{AC} is increased, S_{02} moved from right half s-plane to the left.

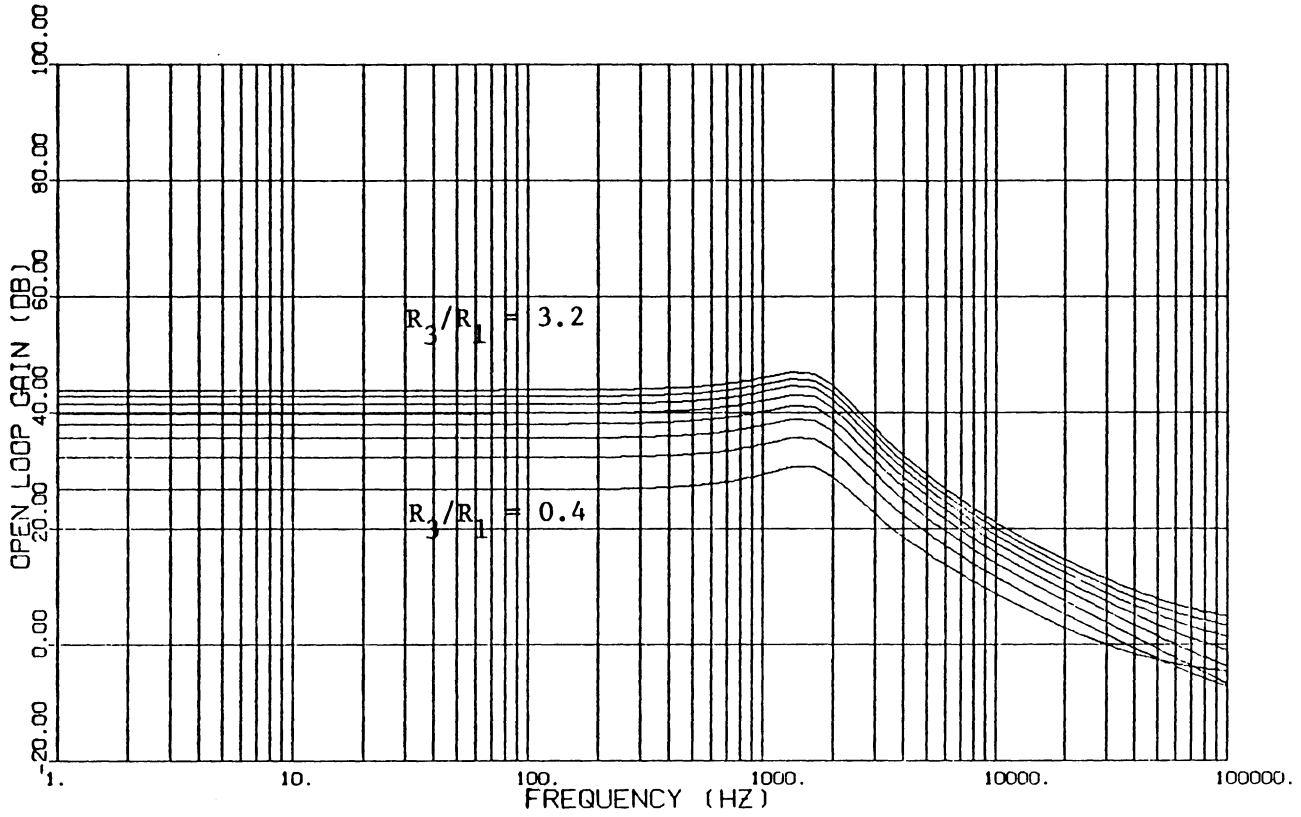


Fig. 3.8(a) OPEN-LOOP GAIN AFFECTED BY DC-LOOP GAIN VARIATION (R_3/R_1 = 3.2, 2.8, 2.4, 2.0, 1.6, 1.2, 0.8, 0.4)

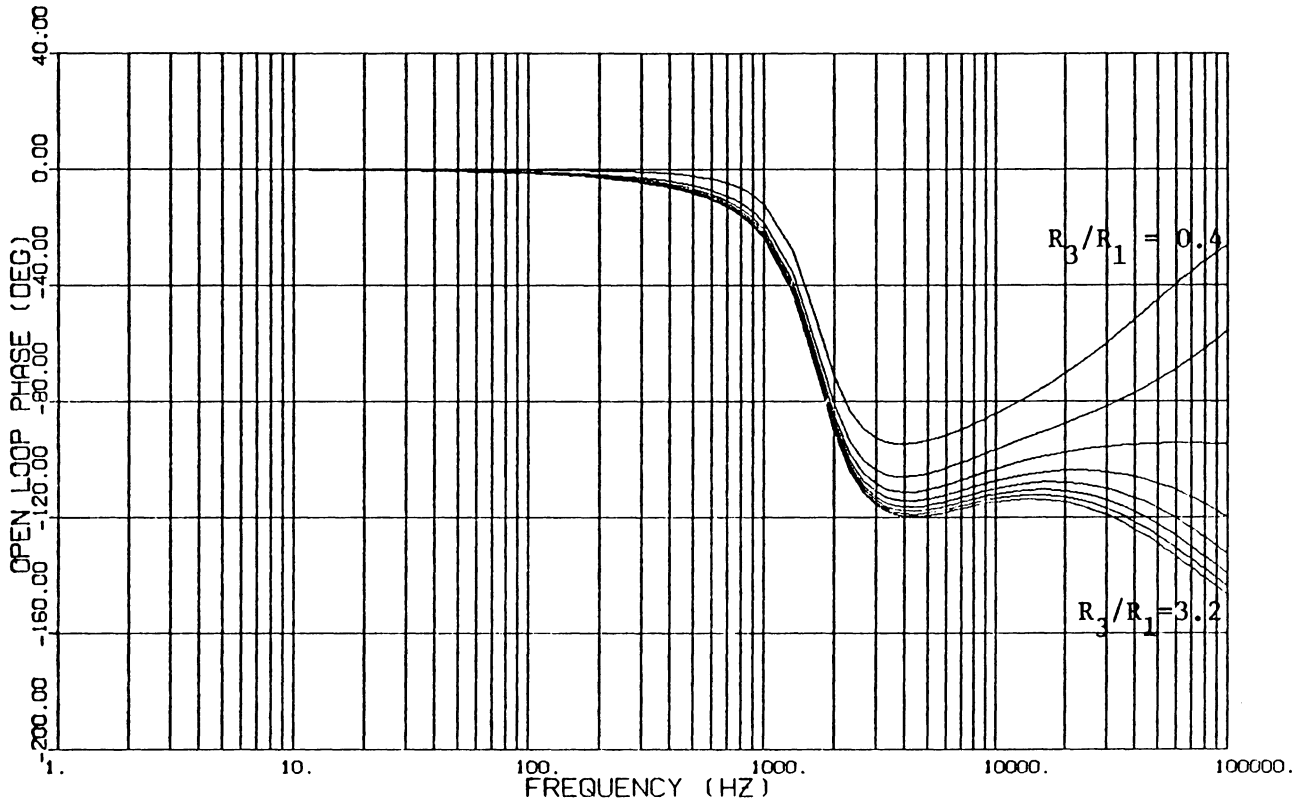


Fig. 3.8(b) OPEN-LOOP PHASE AFFECTED BY DC-LOOP GAIN VARIATION

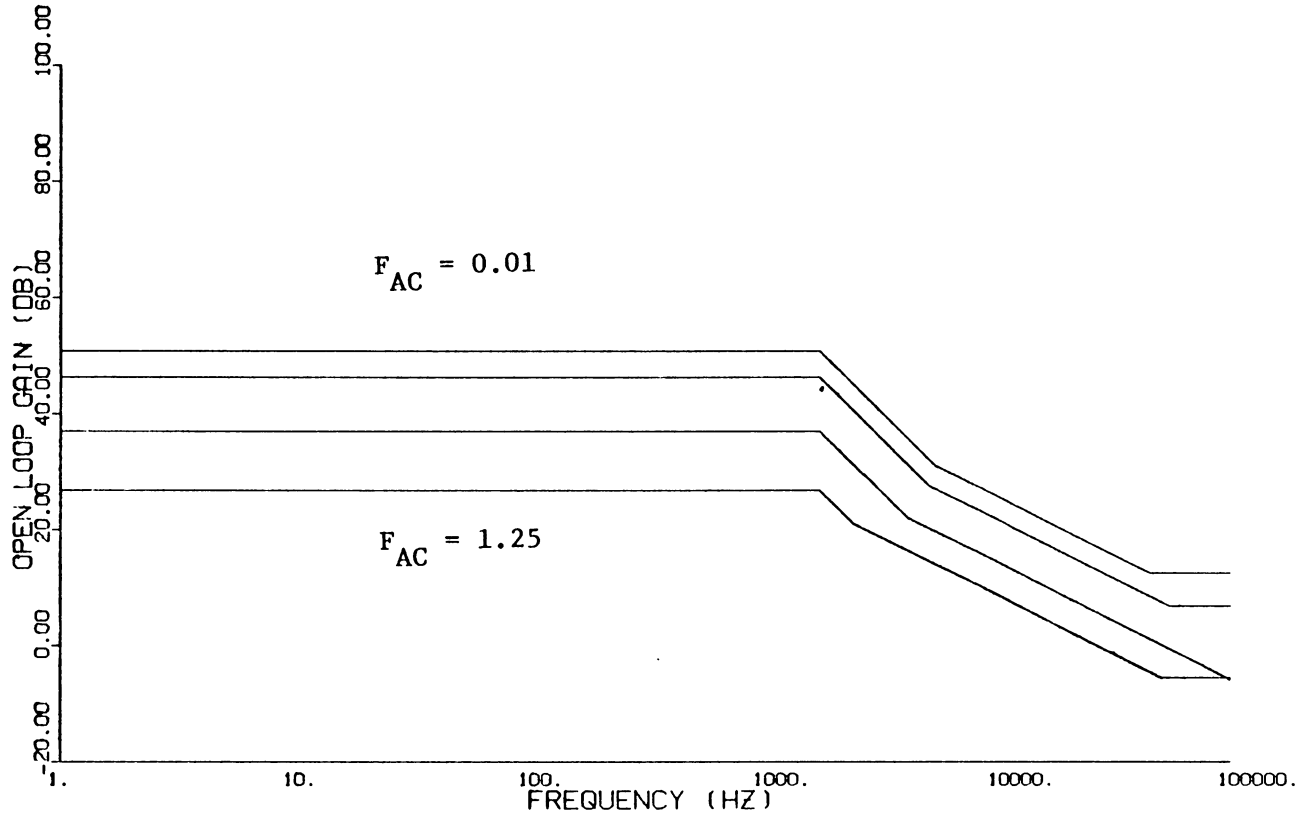


Fig. 3.9 ASYMPTOTIC CURVES SHOWING EFFECTS OF AC-LOOP GAIN

(F_{AC} = 0.01, 0.05, 0.25, 1.25)

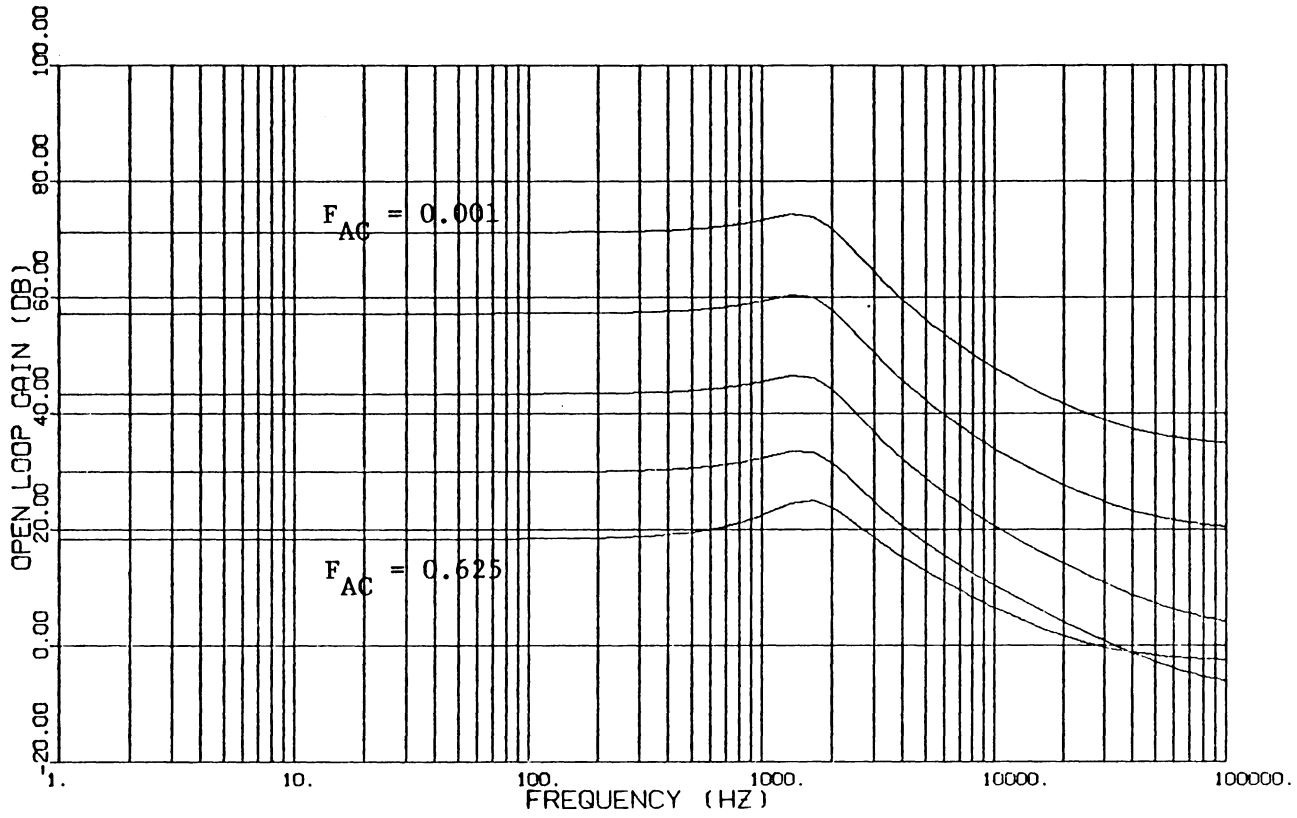


Fig. 3.10(a) OPEN-LOOP GAIN AFFECTED BY AC-LOOP GAIN VARIATION (F_{AC} = 0.001, 0.005, 0.025, 0.125, 0.625)

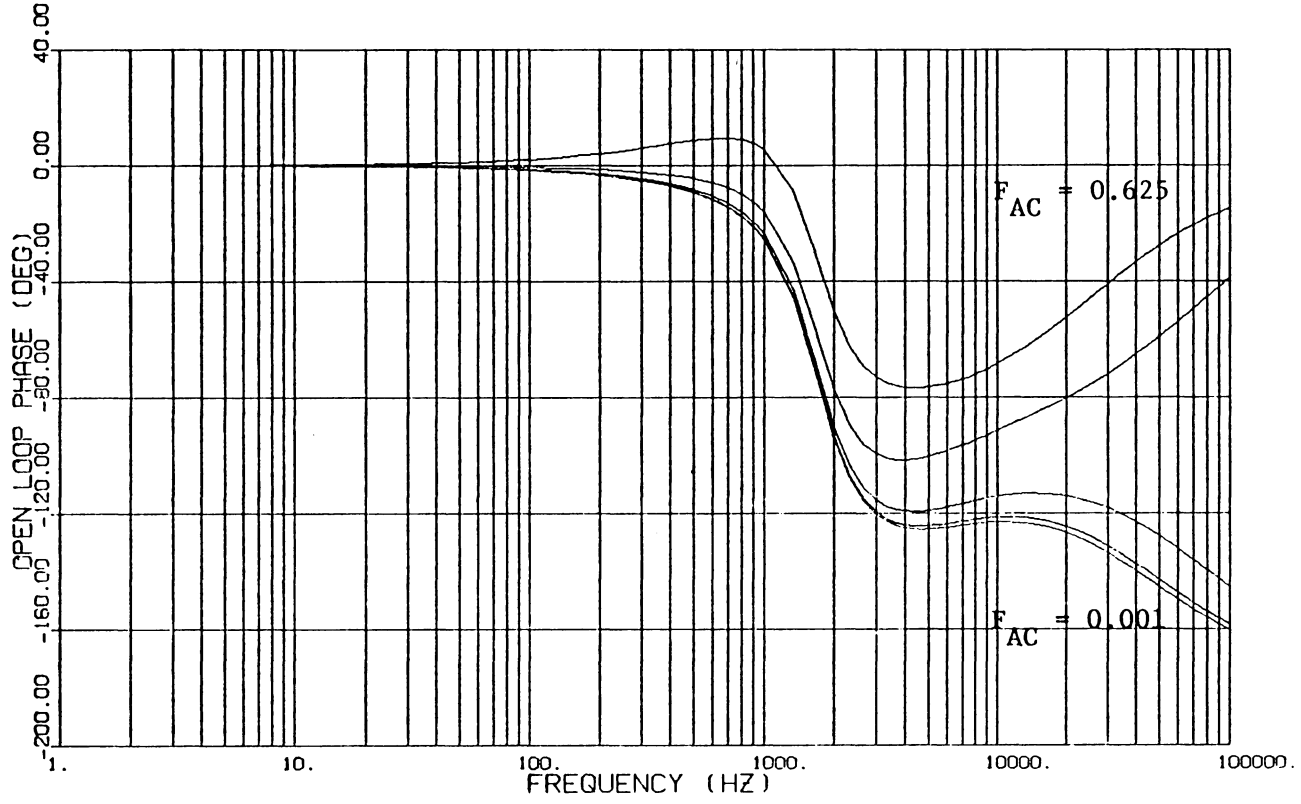


Fig. 3.10(b) OPEN-LOOP PHASE AFFECTED BY AC-LOOP GAIN VARIATION

3) If one disconnects the AC loop and externally injects a ramp to imitate the switching waveform sensed by the current injected loop, he can compare the open-loop system pole-zero locations.

Fig. 3.11(a) shows the locations of poles and zeros without current sensing loop. The two zeros comes from F_{D1}, since the open-loop characteristic equation now becomes:

$$G_T = \frac{F_M}{\Delta} \cdot F_{D1} F_{DC} \quad ,$$

Fig. 3.11(b) is the case with AC loop, here both zeros are in the left half S-plane.

3.5 Discussion

In this chapter we analyzed the simple case employing only gain compensation for both DC loop and current-injected loop. First, in section 3.1, the open-loop characteristic equation is derived and the gain expression in each frequency range and the two zeros are expressed in terms of circuit parameters to enable us to understand some basic characteristics of the system. In section 3.2, two important constraints concerning system stability are brought up. These two constraints must not be violated in order to maintain the system stability. Also pointed out in this section is that these two contraints dictate certain important relations between AC loop gain and DC loop gain which must be satisfied. In sections 3.3 and 3.4, the effects of DC loop gain and AC loop gain on the system characteristics are discussed in details. Here we point out some strong interactions between these two loops. As a result, a system with high loop gain and stable operations can not be achieved consurrently. Since the constraints indi cate some fundamental relation between AC loop and DC loop, it is pre-

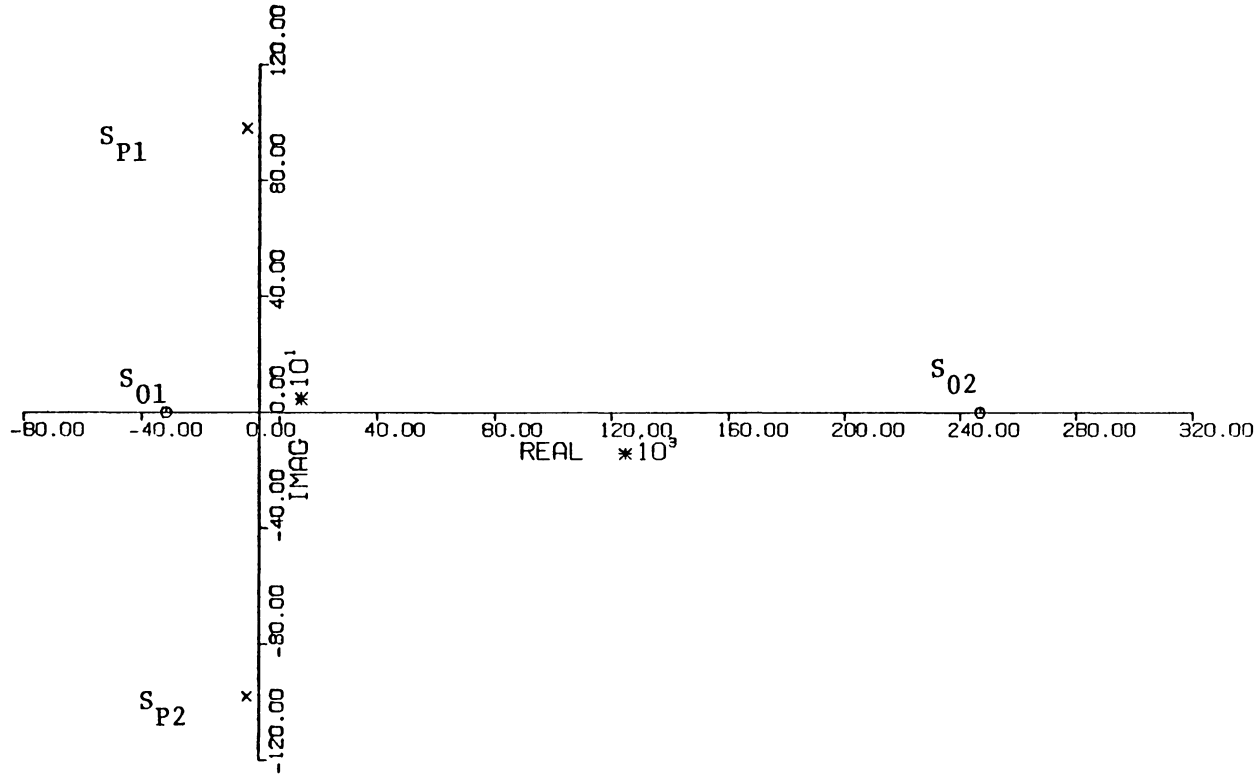


Fig. 3.11(a) OPEN-LOOP POLE-ZERO WITHOUT AC-LOOP

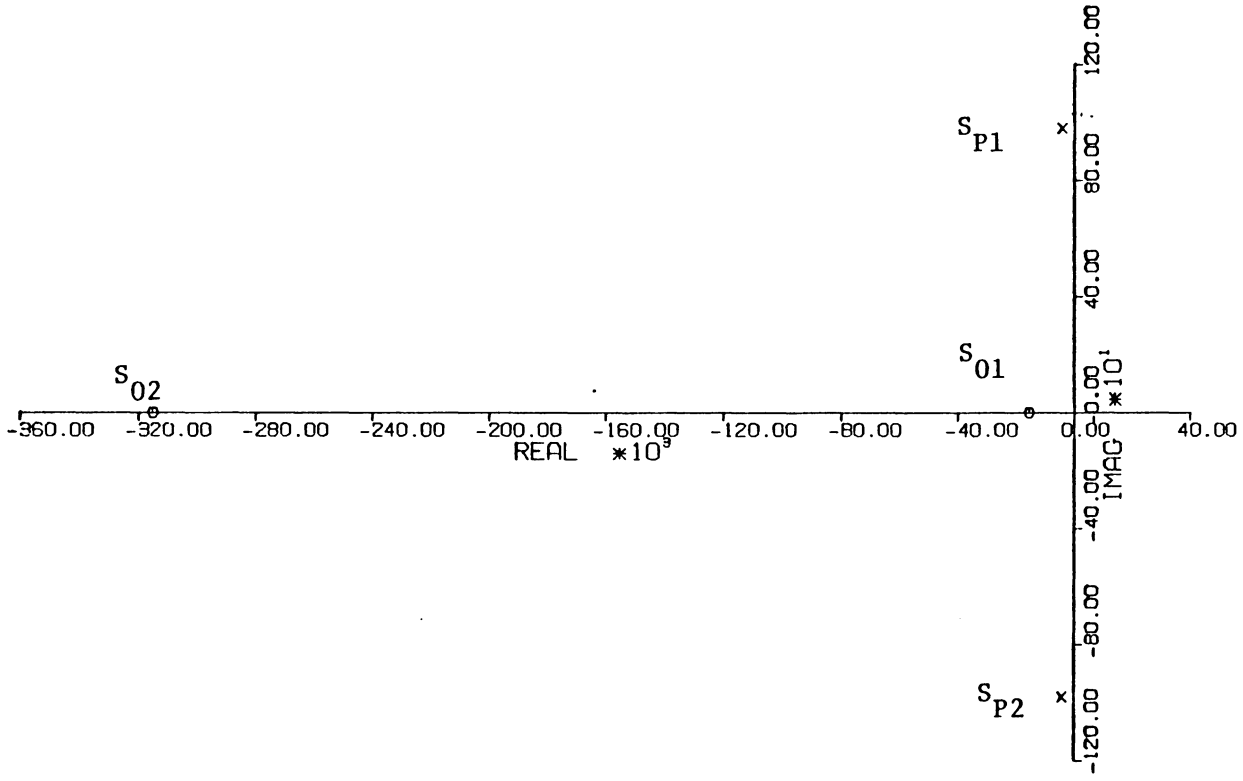


Fig. 3.11(b) OPEN-LOOP POLE-ZERO WITH AC-LOOP

dictable that these two contraints also exist in a more complex case where some form of lead-lag compensation networks are used as will be studied in the following chapters.

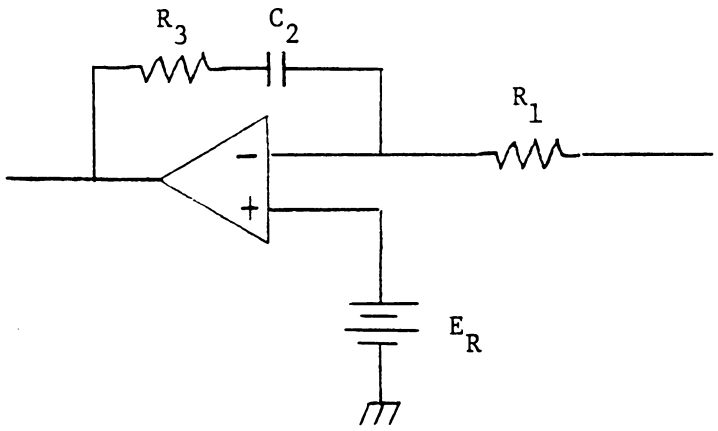
CHAPTER IV

ANALYSIS OF CURRENT-INJECTED CONTROL EMPLOYING A LAG COMPENSATION NETWORK

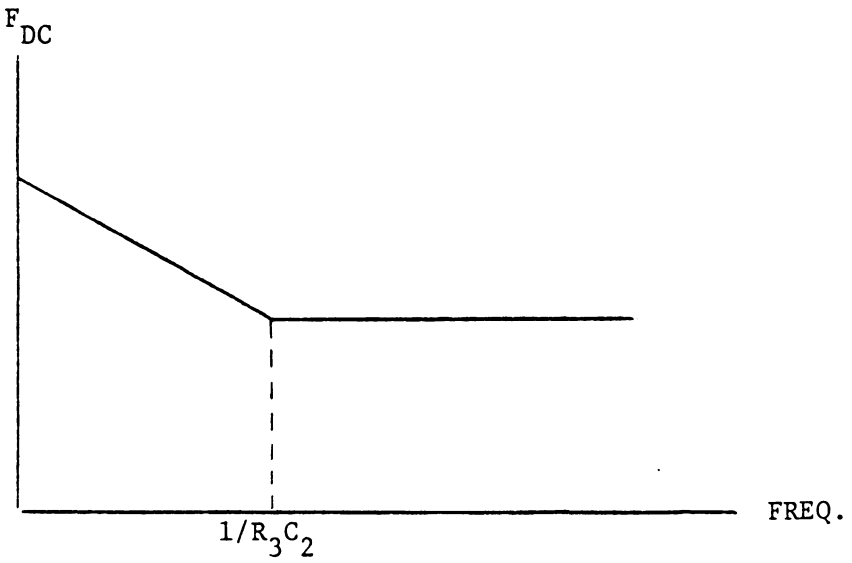
The analysis of current-injected control employing simple gain compensation as was discussed in the previous chapter has revealed certain control characteristic of fundamental importance. The design constraints as shown in equations (3.13) and (3.14) provide the relation between AC and DC loop gains at high frequency. Qualitatively speaking, if DC-loop gain dominates AC-loop gain at high frequencies, positive zero(s) can exist in the system open loop characteristic. In low modulation frequen cies, dc loop gain is sufficiently high that dc loop is always a predomi nant loop in relation to the ac loop.

A high dc loop gain at low frequencies is desirable to attenuatelow frequency noise and to improve regulation. Likewise, low ac loop gainis desirable due to the inverse relationship between F_{AC} and F_M.In summary, the following design guidelines should be observed 1) The dc loop gain should be high and the ac loop gain should be low at low frequencies, 2) The dc loop gain should be sufficiently attenuated at high frequencies, in particular near the loop crossover frequency, such that the ac loop is greater than the dc loop gain. To implement such a control characteristic, we examine the use of a lag compensation in the dc loop, because a lag compensation network will give high gain at low frequency and lower gain at high frequency. In the next chapter, a commonly used lead-lag compensation network will be investigated.

The lag compensation network to be discussed in this chapter is shown in Fig. 4.1. This network gives a transfer function as below:



(a)



(b)

Fig. 4.1 (a) Lag Compensation Network
(b) Its Characteristic Curve

$$F_{DC} = (R_3 + \frac{1}{SC_2}) \cdot \frac{1}{R_1}$$

$$= \frac{SR_3C_2 + 1}{SR_1C_2} \qquad (4.1)$$

4.1 Open-Loop Characteristics

Substitute eq.s (2.22), (2.25), (2.28), and (4.1) into eq. (3.1), the open-loop gain results:

$$G_T = F_M \cdot \omega_o^2 \cdot \frac{V_o}{DD'R_1C_2} \cdot \frac{S^3K_1 + S^2K_2 + SK_3 + K_4}{S(S^2 + 2\zeta\omega_o S + \omega_o^2)} \qquad (4.2)$$

where

$$K_1 = \frac{DR_1C_2}{R_L\omega_o^2}\left(F_{AC}\frac{N_s}{N_p} - \frac{R_3R_c}{R_1}\right)$$

$$K_2 = \frac{F_{AC}N_sC}{D'N_p}\,DR_1C_2 + R_3C_2\left(R_cC - \frac{DL_e}{R_L}\right) - \frac{DL_e}{R_L}R_cC$$

$$K_3 = \frac{2F_{AC}N_s}{D'R_LN_p}\,DR_1C_2 + R_cC - \frac{DL_e}{R_L} + R_3C_2$$

$$K_4 = 1$$

The numerator of eq. (4.2) can be expressed in terms of three zeros, S_{o1}, S_{o2}, and S_{o3}:

$$G_T = F_M \cdot \omega_o^2 \cdot \frac{V_o}{DD'R_1C_2} \cdot \frac{(S/S_{o1} + 1)(S/S_{o2} + 1)(S/S_{o3} + 1)}{S(S^2 + 2\zeta\omega_o S + \omega_o^2)} \qquad (4.3)$$

and

and $$K_1 = \frac{1}{S_{o1} \cdot S_{o2} \cdot S_{o3}}$$

$$K_1 = \frac{1}{S_{o1} \cdot S_{o2} \cdot S_{o3}}$$

$$K_2 = \frac{1}{S_{o1} \cdot S_{o2}} + \frac{1}{S_{o1} \cdot S_{o3}} + \frac{1}{S_{o2} \cdot S_{o3}}$$

$$K_3 = \frac{1}{S_{o1}} + \frac{1}{S_{o2}} + \frac{1}{S_{o3}}$$

Assuming the three zeros are sufficiently apart, i.e. $1/S_{o1} >> 1/S_{o2} >> 1/S_{o3}$, the following approximations hold true:

$$K_3 \simeq 1/S_{o1}$$

$$K_2 \simeq \frac{1}{S_{o1} \cdot S_{o2}}$$

therefore,

$$1/S_{o1} \simeq K_3$$

$$1/S_{o2} \simeq K_2/K_3$$

$$1/S_{o3} \simeq K_1/K_2$$

Compare eq. (4.3) and eq. (3.4), a zero and a pole have been added tothe aystem because of the DC loop compensation network. And since the open-loop characteristic at low frequency is predominantly determined by DC loop, therefore it is reasonable to assume the new zero and new pole are the zero and pole of F_{DC}, which are $-1/R_3C_2$ for the zero and 0.0 for the pole.

Now, we can express the three approximated zeros as follows:

$$S_{o1} \simeq 1/R_3C_2 \qquad \frac{R_3}{DR_1} \tag{4.4}$$

$$S_{o2} \simeq K_2/K_3 \simeq \frac{\frac{R_3}{DR_1}}{\frac{F_{AC}N_sC}{D'N_p} + \frac{R_3}{DR_1}\left(R_cC - \frac{DL_e}{R_L}\right)} \tag{4.5}$$

$$S_{o3} \simeq K_2/K_1 \simeq R_L\omega_o^2 \frac{\frac{F_{AC}N_sC}{D'N_p} + \frac{R_3}{DR_1}\left(R_cC - \frac{DL_e}{R_L}\right)}{F_{AC}\frac{N_s}{N_p} - \frac{R_3R_c}{R_1}} \tag{4.6}$$

The two high frequency zeros, S_{02} and S_{03}, share the very similar forms as the two in the previous chapter, eqs. (3.7) and (3.8). The only difference after we add a lag compensation network is the addition of a low frequency zero and pole which provides a higher low-frequency gain. Fig. 4.2 shows the asymptotic curves for $G_T(s)$. The open-loop gain in each frequency range is approximated by the following equations:

$$S < S_{o1} \qquad G_T \simeq F_M \cdot \omega_o^2 \frac{V_o}{DD'R_1C_2} \cdot \frac{1}{s \cdot \omega_o^2}$$

$$= F_M \cdot \frac{V_o}{DD'R_1C_2} \cdot \frac{1}{S} \tag{4.7}$$

$$S_{o1} < S < \omega_o \qquad G_T \simeq F_M \cdot \omega_o^2 \frac{V_o}{DD'R_1C_2} \cdot \frac{S/S_{o1}}{s \cdot \omega_o^2}$$

$$= F_M \cdot \frac{V_oR_3}{DD'R_1} \tag{4.8}$$

$$\omega_o < S < S_{o2} \qquad G_T \simeq F_M \cdot \omega_o^2 \cdot \frac{V_o}{DD'R_1C_2} \cdot \frac{S/S_{o1}}{S(S^2 + 2\zeta\omega_oS + \omega_o^2)}$$

$$= F_M \cdot \frac{V_oR_3}{DD'R_1} \cdot \frac{\omega_o^2}{S^2 + 2\zeta\omega_oS + \omega_o^2} \tag{4.9}$$

$$S_{o2} < S < S_{o3} \qquad G_T \simeq F_M \cdot \omega_o^2 \cdot \frac{V_o}{DD'R_1C_2} \cdot \frac{S/S_{o1} \cdot S/S_{o2}}{S(S^2 + 2\zeta\omega_oS + \omega_o^2)}$$

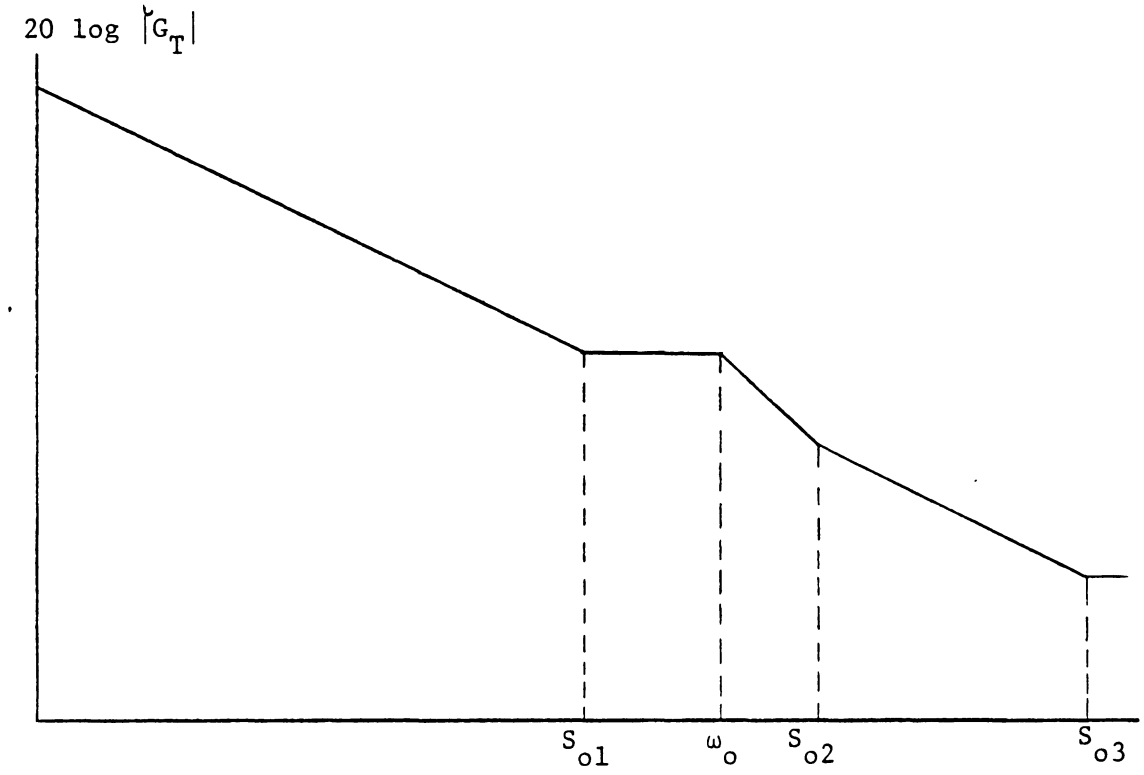


Fig. 4.2 Open Loop Asymptotic Curve
Under Lag Compensation

$$= F_M \cdot \frac{V_o}{D'} \cdot \left[\frac{F_{AC} N_s C}{D' N_p} + \frac{R_3}{D R_1} \left(R_c C - \frac{D L_e}{R_L} \right) \right]$$

$$\cdot \frac{S\omega_o^2}{S^2 + 2\zeta\omega_o S + \omega_o^2} \qquad (4.10)$$

$S > S_{o3}$

$$G_T \simeq F_M \cdot \omega_o^2 \cdot \frac{V_o}{DD' R_1 C_2} \cdot \frac{S/S_{o1} \cdot S/S_{o2} \cdot S/S_{o3}}{S \cdot S^2}$$

$$= F_M \cdot \frac{V_o}{D' R_L} \cdot \left(F_{AC} \frac{N_s}{N_p} - \frac{R_3 R_c}{R_1} \right) \qquad (4.11)$$

The computer plots of the open-loop gain and phase using lag compensatio network are shown in Fig. 4.3 (a), (b).

4.2 Stability Criteria and Constraints

The negative terms in eq.s (4.5) and (4.6), if is sufficientlylarge can produce positive zero(s). Therefore, the following two constraints have to be satisfied for stable operation.

first constraint: $$F_{AC} \frac{N_s}{N_p} > \frac{R_3 R_c}{R_1} \qquad (4.12)$$

second constraint: $$F_{AC} \frac{N_s}{N_p} > \frac{R_3 R_c}{R_1} \left(\frac{D' L_e}{R_L R_c C} - \frac{D'}{D} \right) \qquad (4.13)$$

Note that, these two constraints are identical to those eq.s (3.13) and (3.14) of the simple gain compensation.This is because the two constrain deal with dc and ac loop gain relation at high frequencies. The dc loop at high frequencies is:

$$F_{DC} \Big|_{s \to \infty} = \frac{R_3}{R_1}$$

and is the same as before.

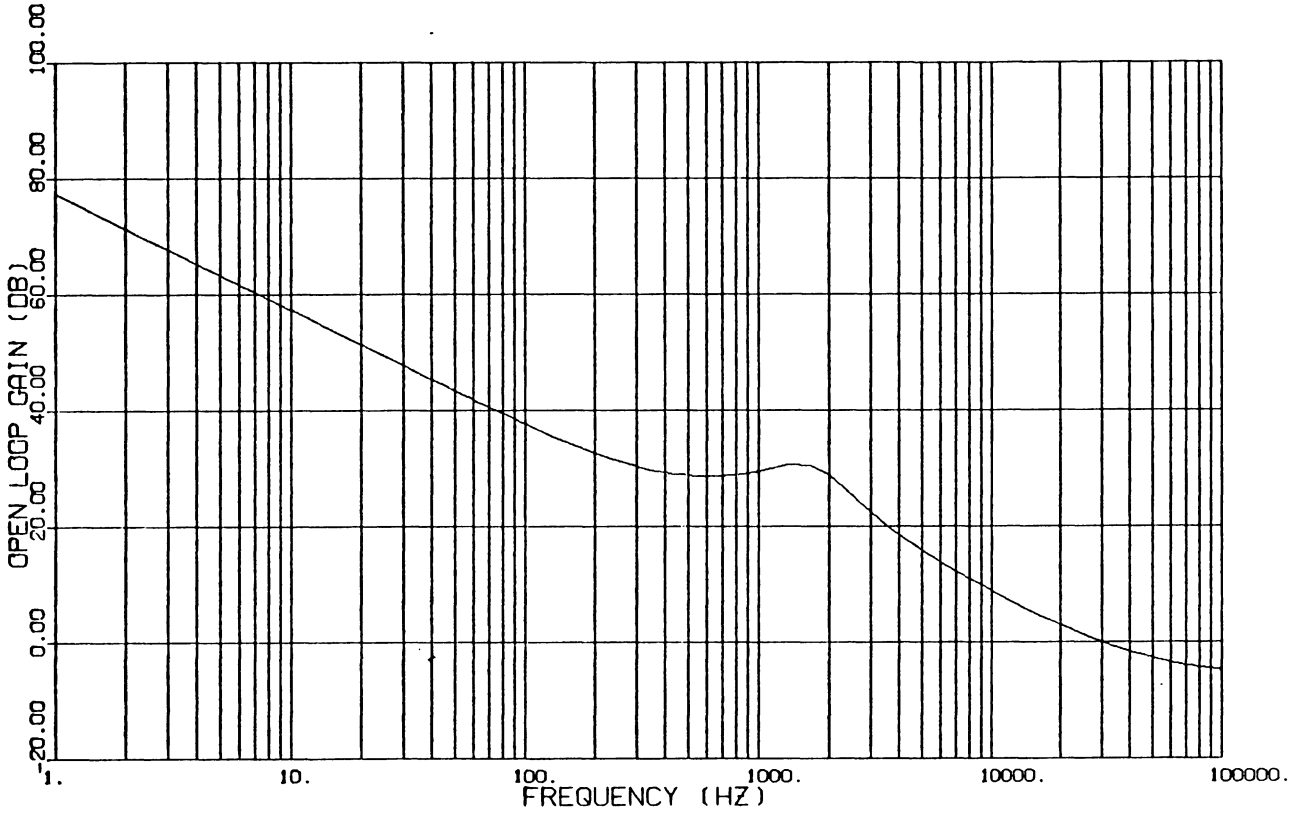


Fig. 4.3 (a) Open-Loop Gain Under Lag Compensation

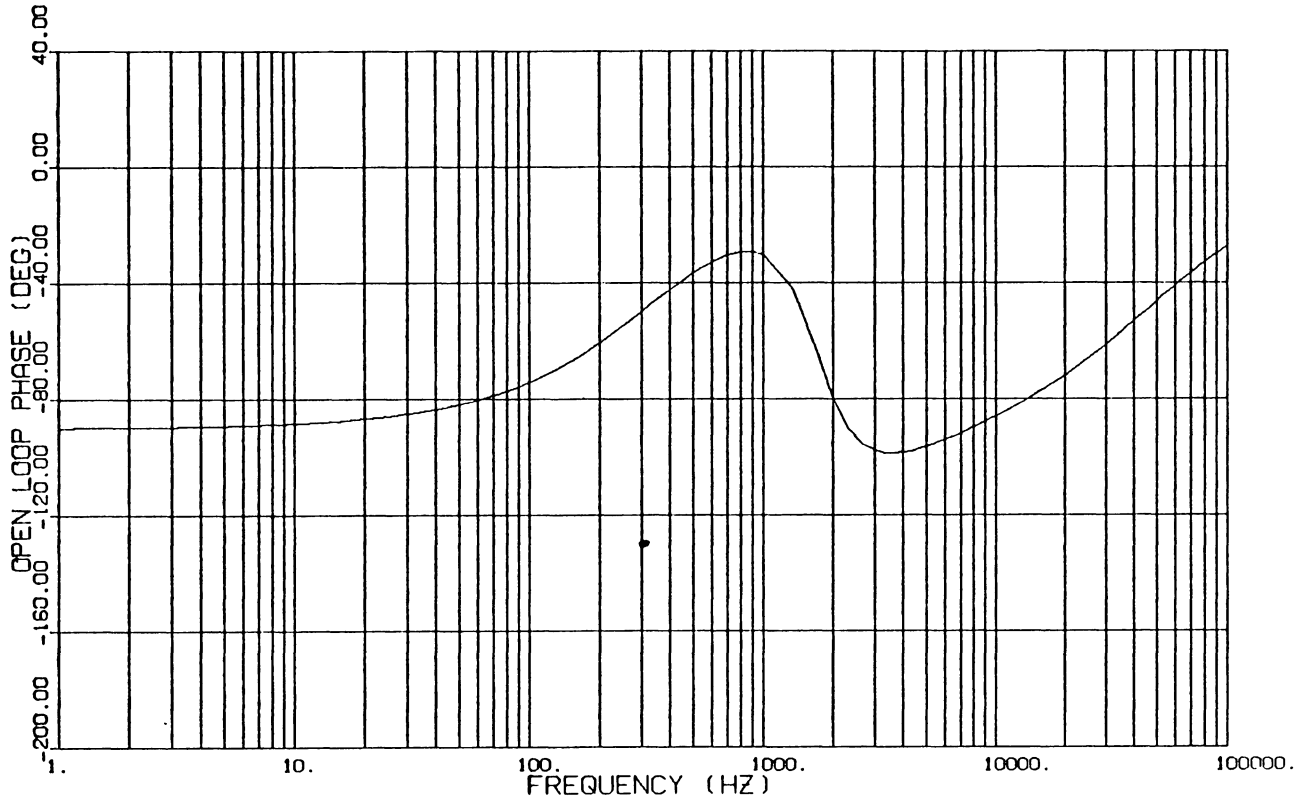


Fig. 4.3 (b) Open-Loop Phase Under Lag Compensation

4.3 Effects of DC Compensation Parameters

After adding a lag compensation network to DC loop, we already have some idea about how this network has affected the open-loop characteristic. But questions like what type of change can these parameters bring to this new system or which parameter can be changed to what extent such that we can obtain a better open-loop performance are still remained to be answered. Prior to the investigation of various effects of certain key control loop parameters to regulator performances it should be noted that the following loop characteristics are desirable:

(1) high loop gain and wide bandwidth for better DC regulation, audiosusceptibility, output impedance and transient response,

(2) sufficiently phase margin to ensure stable operation

A. Effects of R1

Examining eqs. (4.7)-(4.11), it is clearly indicated that the open-loop gain is controlled by the factor R3/R1 at frequencies higher than S_{01}. Decrease R1 or increase R3 has the similar effects on the open-loop characteristic at frequencies higher than S_{01}.

Fig. 4.4 shows the asymoptotic curves of $G_T(s)$ as R1 is varied. In general, decrease of R1 will cause the loop gain to increase accompanying with an increase of phase delay at high frequency. Further decreasing of R1 will result to violation of the first constraint, eq. (4.12). If the constraint is violated S_{03} becomes a positive zero

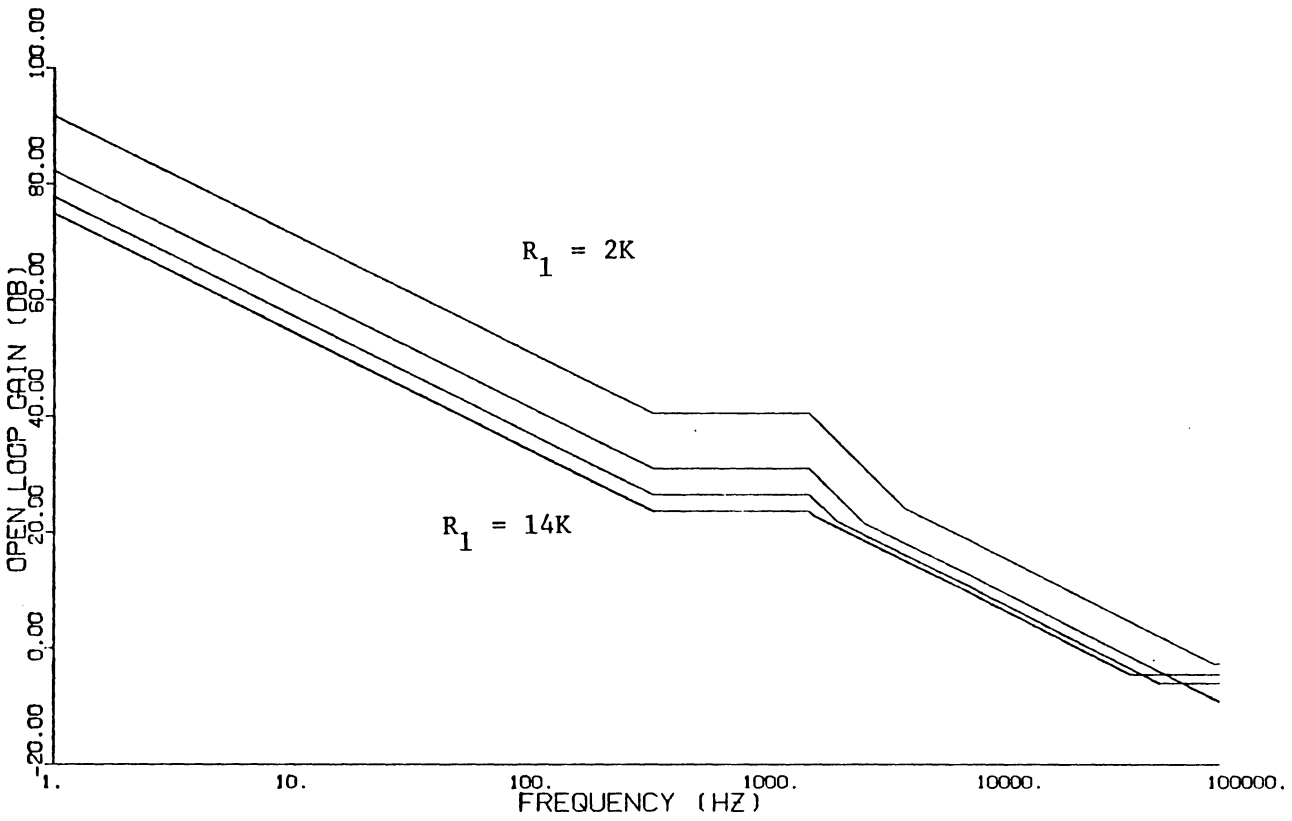


Fig. 4.4 Asymptotic Curve Showing the Effects of R_1

(R_1 = 2K, 6K, 10K, 14K)

and the magnitude of S_{o3} starts to decrease as R_1 is further reduced, at the same time, the magnitude of the loop gain at frequencies higher than S_{o3} starts to increase. What appears in the phase plot, Fig. 4.5(b), is an increasing of phase towards -180° at high frequencies as R_1 is decreased.

(b) Effects of R_3

Fig. 4.6 illustrates the asymptotic curves of $G_T(s)$ as R_3 is increased. Fig. 4.7 (a), (b) are the open-loop characteristics of gain and phase. Comparing 4.7 (a) and (b) with Fig. 4.5 (a) and (b), we note that the similar effects are observed at high frequencies. This is because in eq.s (4.5), (4.6), and (4.7), R_3/R_1 acts as a single factor at frequencies higher than S_{o1}.

For signal frequency lower than S_{o1}, R_3 can be neglected due to the much smaller impedance, and the DC loop gain is now dictated by the op-amp integrator and R_1C_2.

(c) Effects of C_2

Decrease of C_2 will cause:

- S_{o1} to increase,
- System gain at frequencies higher than S_{o1} to remain constant

The asymptotic curve of $G_T(s)$ in Fig. 4.8 and computer plots for gain and phase in Fig. 4.9 (a), (b) illustrate these results. It is noted in Fig. 4.9 (b) that, at

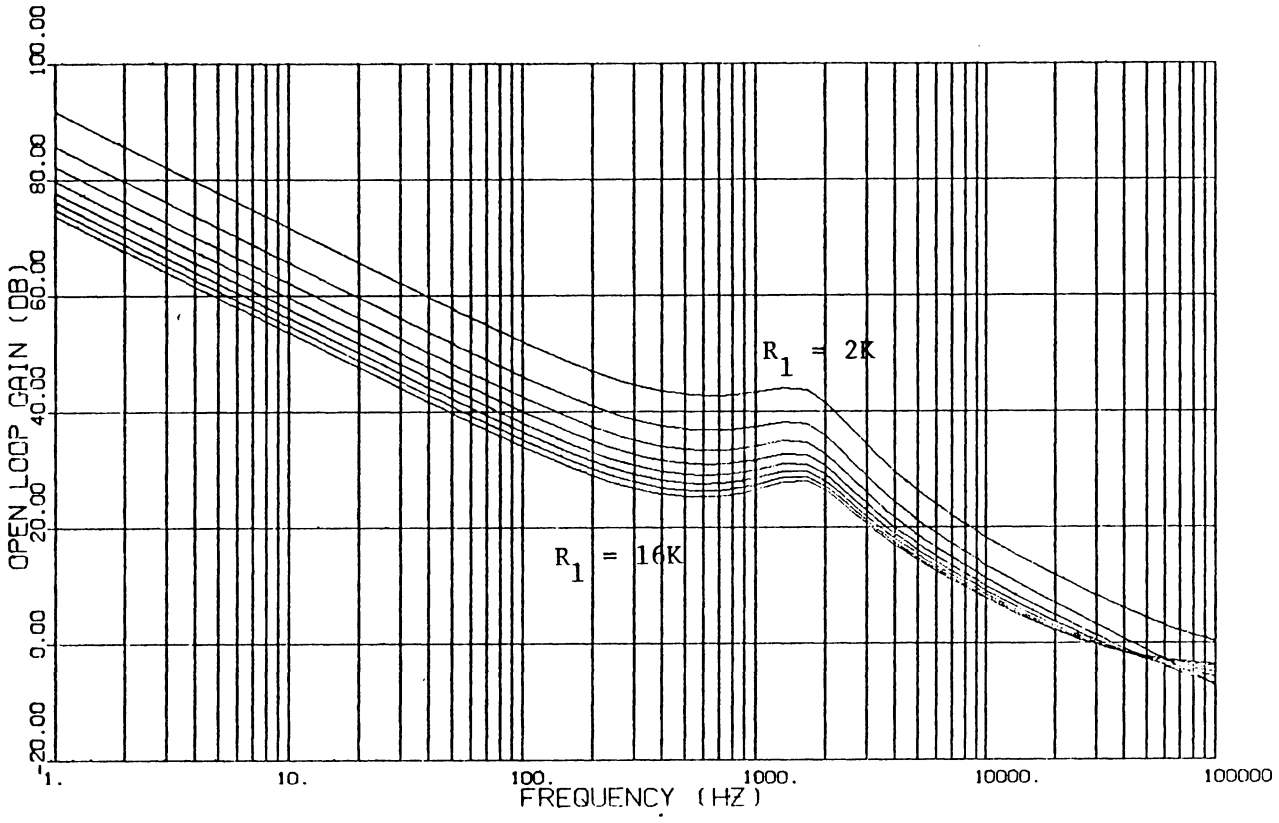


Fig. 4.5 (a) Open-Loop Gain by Changing R_1

(R_1 = 2K, 4K, 6K, 8K, 10K, 12K, 14K, 16K)

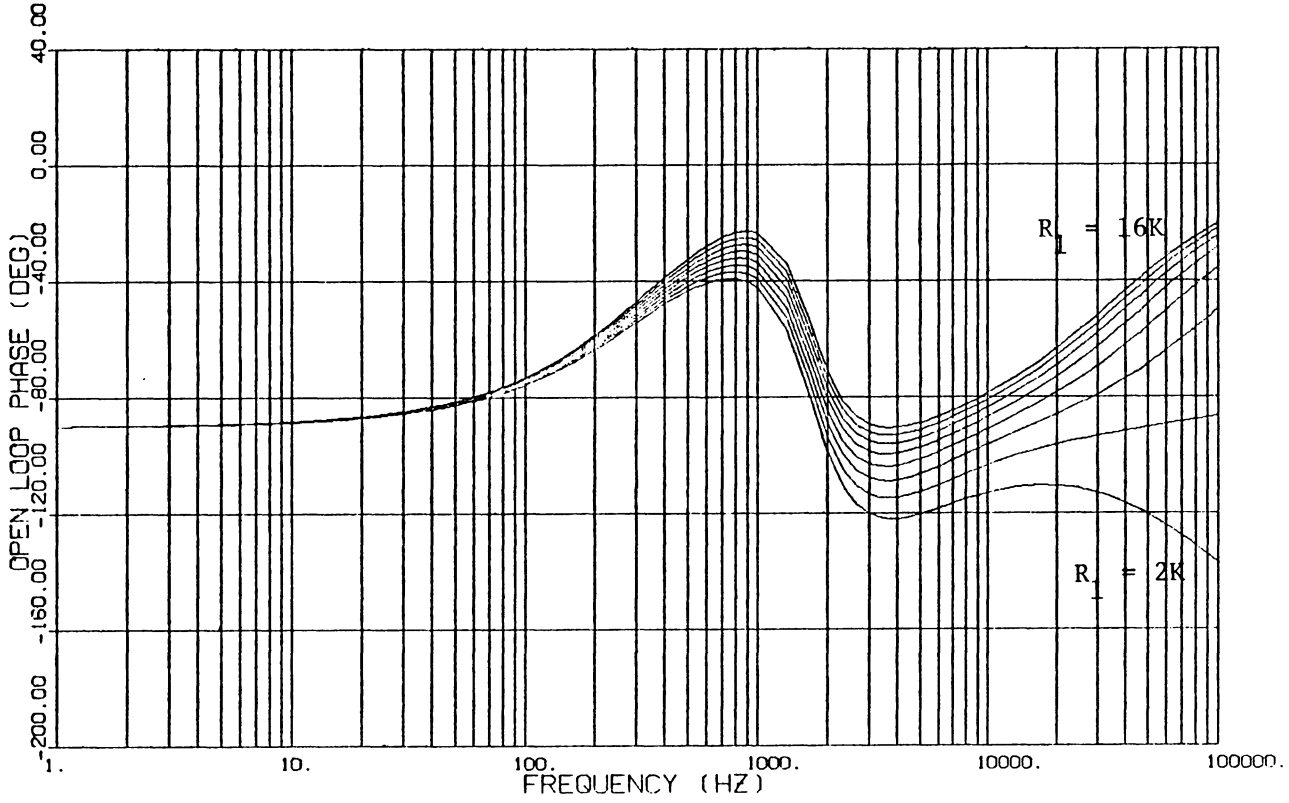


Fig. 4.5 (b) Open-Loop Phase by Changing R_1

(R_1 = 2K, 4K, 6K, 8K, 10K, 12K, 14K, 16K)

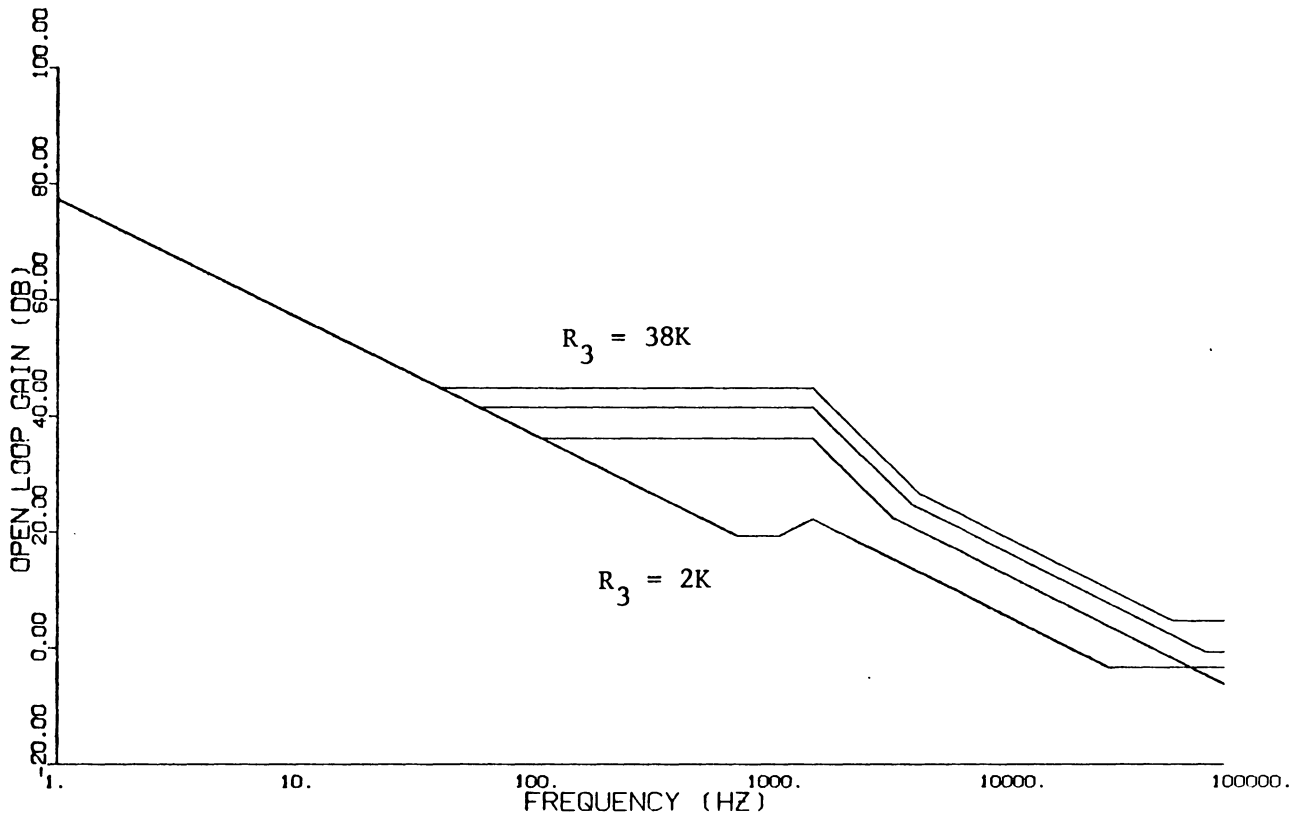


Fig. 4.6 Asymptotic Curve Showing the Effects of R_3

(R_3 = 2K, 14K, 26K, 38K)

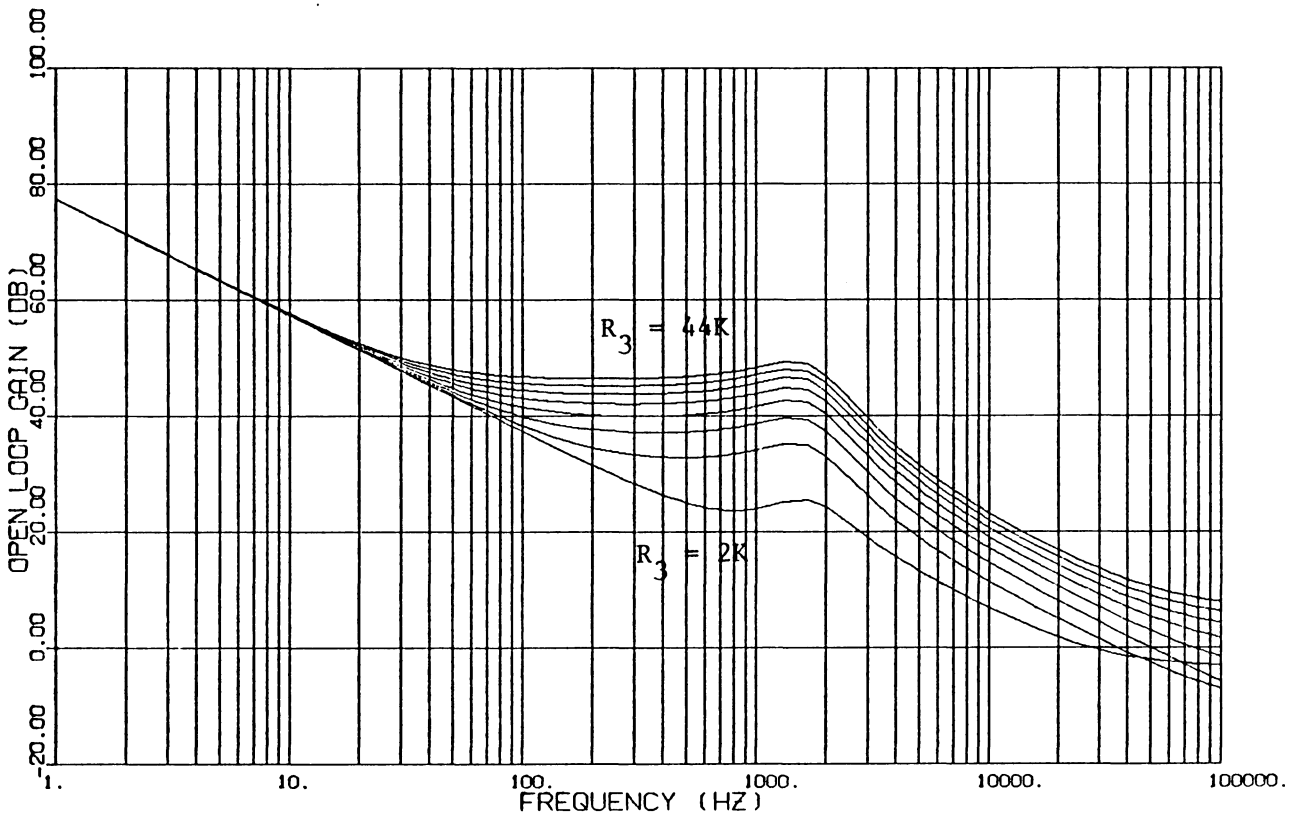


Fig. 4.7 (a) Open-Loop Gain by Changing R_3

(R_3 = 2K, 8K, 14K, 20K, 26K, 32K, 38K, 44K)

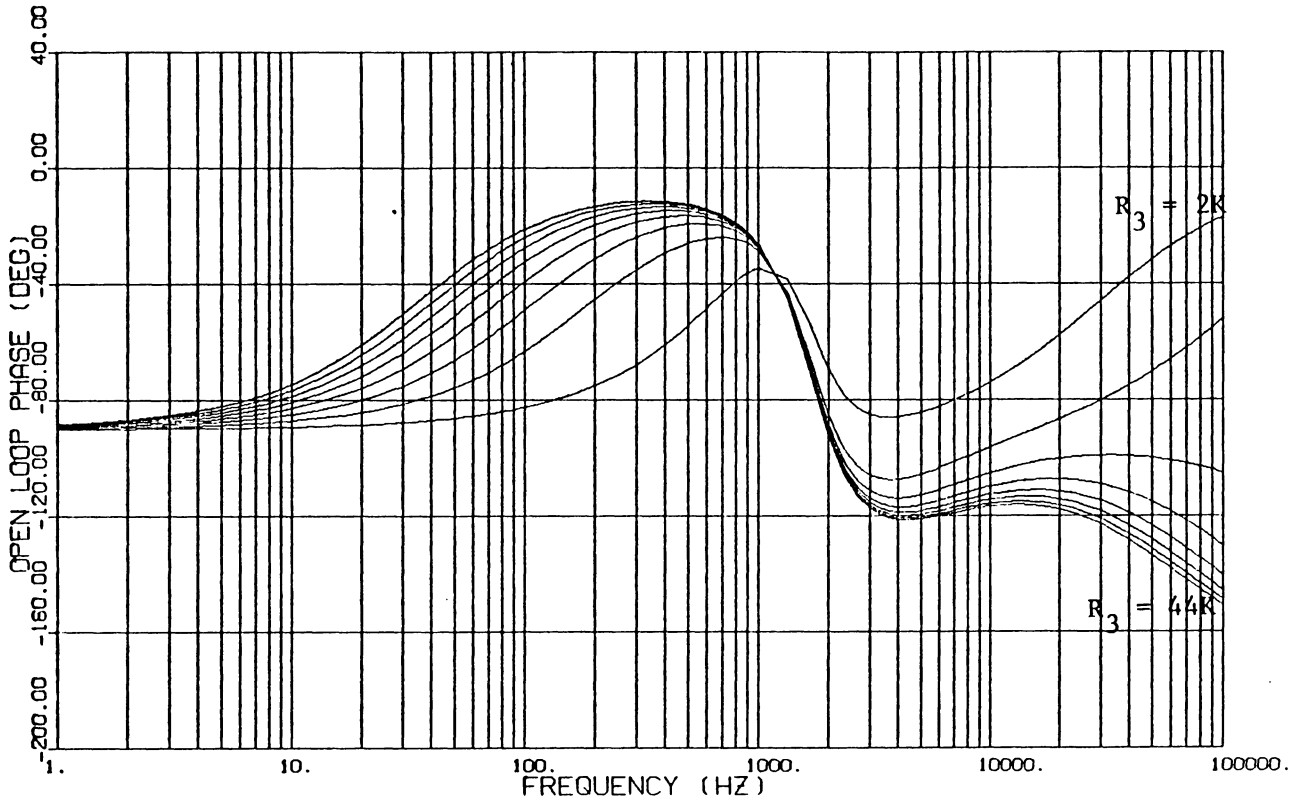


Fig. 4.7 (b) Open-Loop Phase by Changing R_3

(R_3 = 2K, 8K, 14K, 20K, 26K, 32K, 38K, 44K)

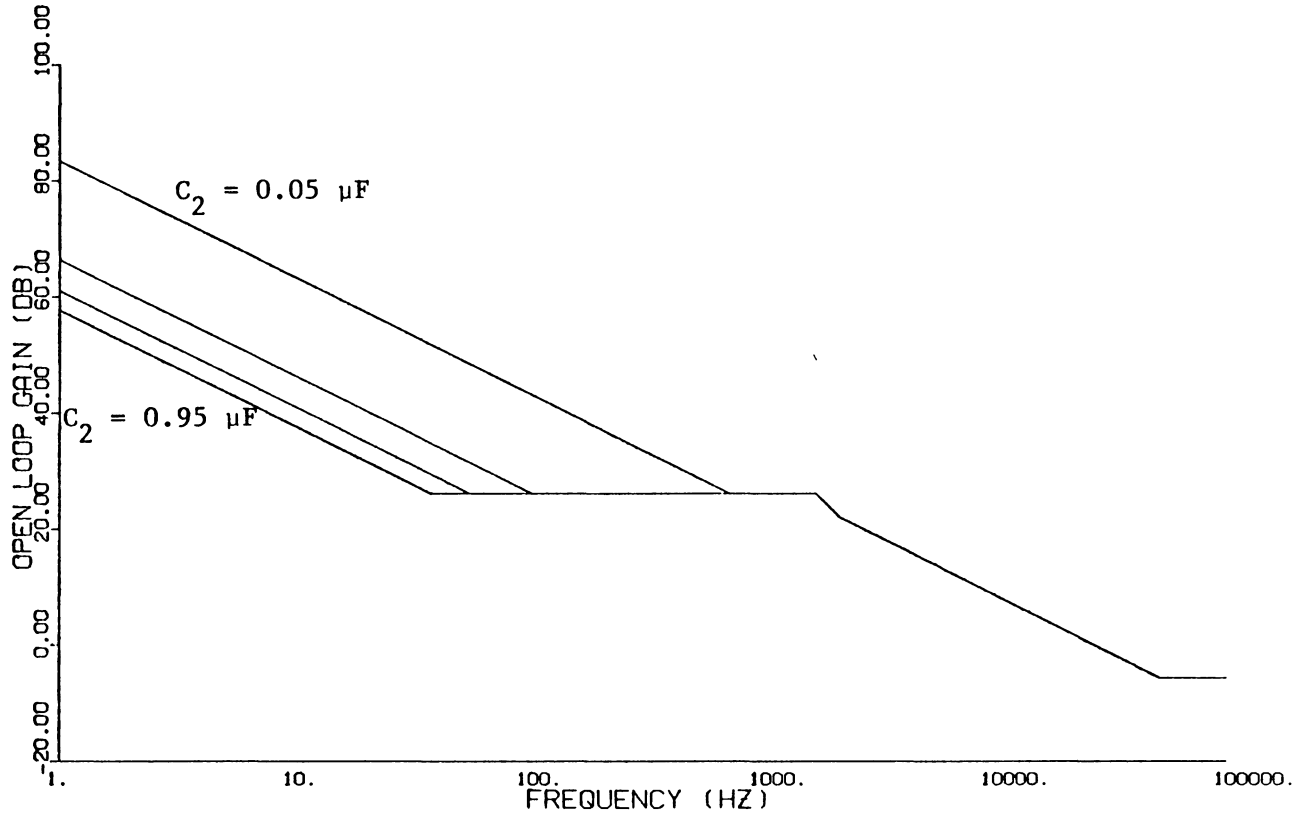


Fig. 4.8 Asymptotic Curve Showing the Effects of C_2

(C_2 = .05 μF, 0.35 μF, 0.65 μF, 0.95 μF)

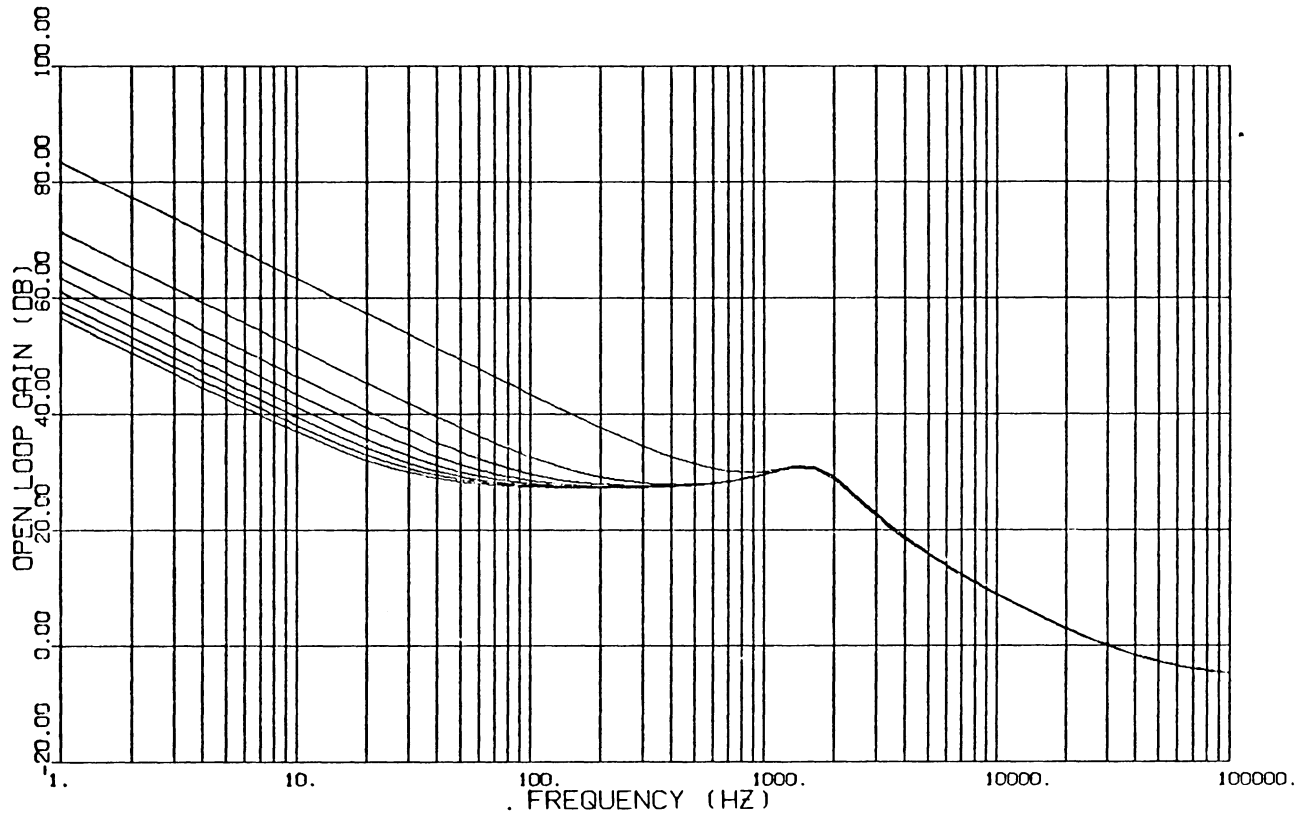


Fig. 4.9 (a) Open-Loop Gain by Changing C_2
(C_2 = .05 μF, 0.2 μF, .35 μF,
0.5 μF, 0.65 μF, 0.8 μF,
0.95 μF, 1.1 μF)

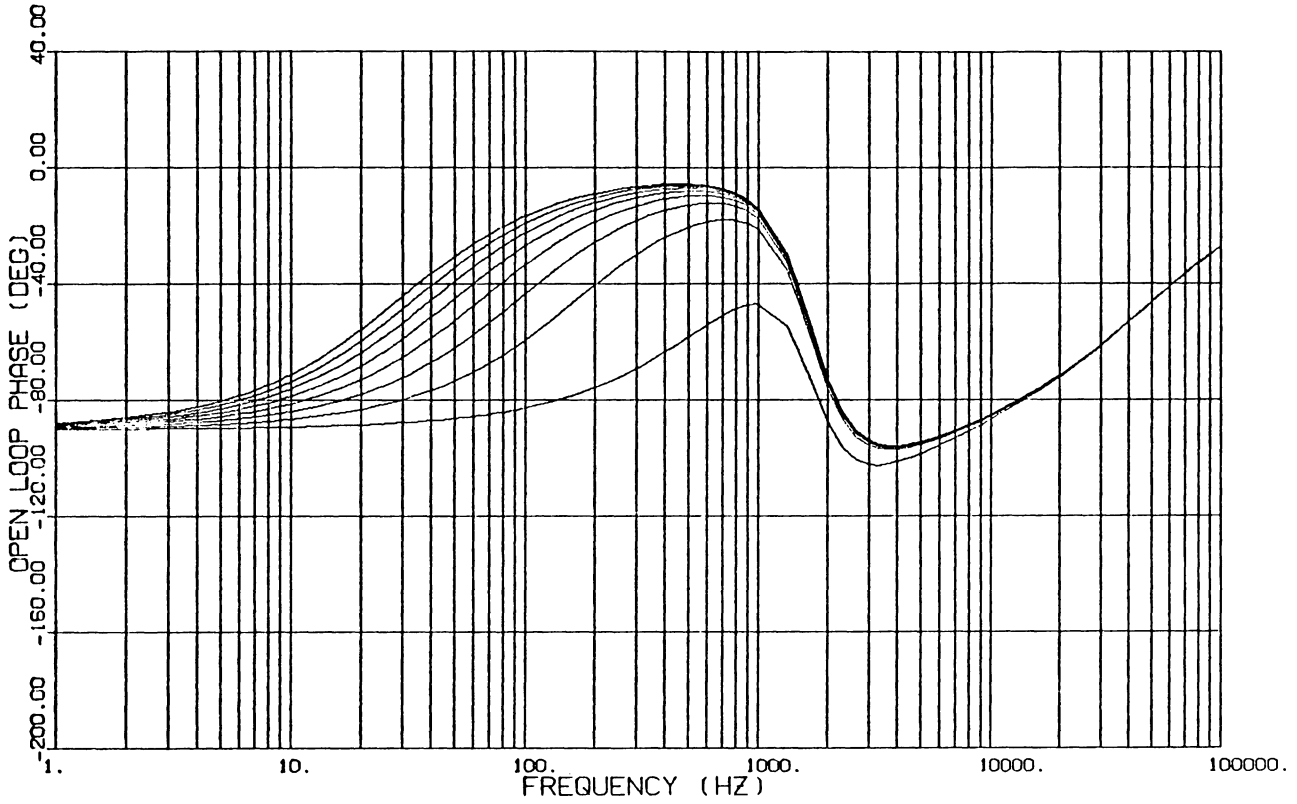


Fig. 4.9 (b) Open-Loop Phase by Changing C_2

(C_2 = 0.5 μF, 0.2 μF, .35 μF, .5 μF,
.65 μF, 0.8 μF, .95 μF, 1.1 μF)

high frequencies, the phase delay of the loop vanishes.

4.4 Effects of AC Loop Gain

It is demonstrated in the previous section that in order to increas the loop gain, one can only adjust the DC compensation parameters (R_1 and R_3) in somewhat limited ranges set by the constraints (4.12) . The effort of varying the AC loop gain is examined in this section. It appears from (4.12) and (4.13) that an increase of the AC loop gain F_{AC} is a possible way to relax these two constraints. Nevertheless, the PWM gain F_M is inversely proportional to F_{AC}. Increase of F_{AC} will decrease F_M and thus the loop gain.

The asymptotic curves are illustrated in Fig. 4.10 for different R_{p2}, where all other parameter values are the same as in Table I. As F_{AC} is reduced to a sufficiently small magnitude ($F_{AC} < 0.065$ or $R_{p2} < 19.45$), the inequality constraint (4.12) is violated and S_{o3} becomes a positive zero. Fig. 4.11 (a), (b) illustrate the open-loop gain and phase.

4.5 Discussion

In section 4.1, the open-loop characteristic equation was derived and loop gain in each frequency range was approximated in terms of control loop parameters to serve as the basis for the discussions. When we derived the constraints for this new case in section 4.2, we found they were exactly the same constraints we had in Chapter III because the high-frequency DC loop gains were the same. In sections 4.3 and 4.4, each control loop parameter's effects on the open-loop characteristic was discussed. Since the constraints were the same, the

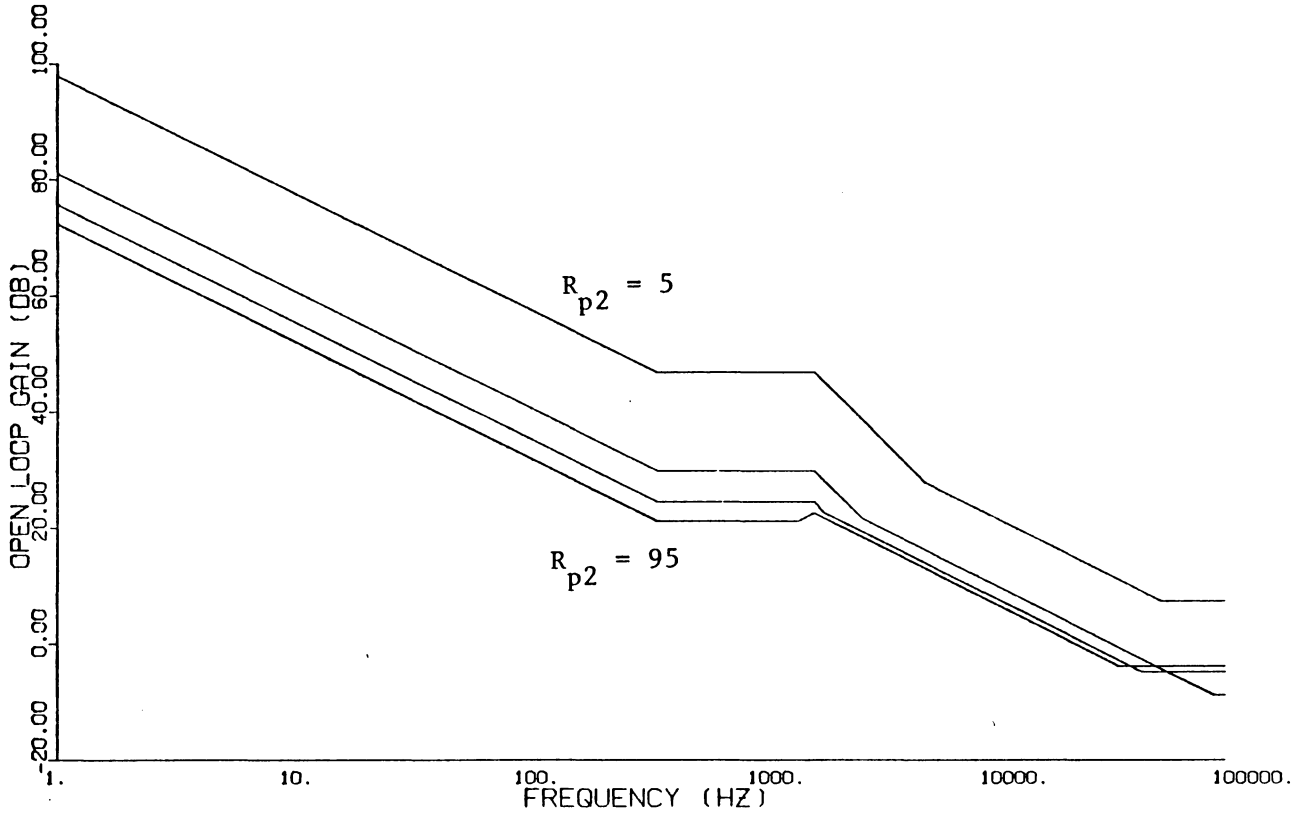


Fig. 4.10 Asymptotic Curve Showing the Effects of F_{AC} (R_{p2} = 5, 35, 65, 95)

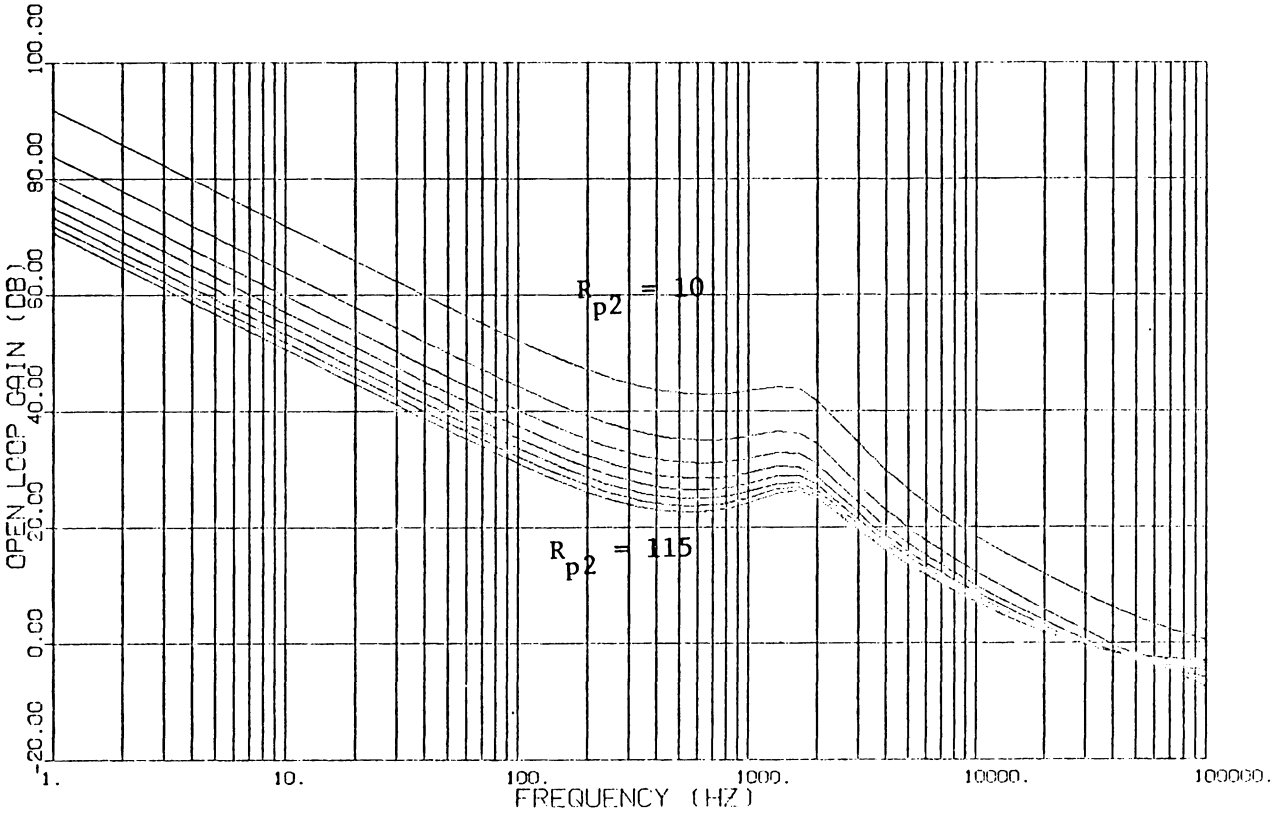


Fig. 4.11 (a) Open-Loop Gain by Changing R_{p2}

(R_{p2} = 10, 25, 40, 55, 70, 85, 100, 115)

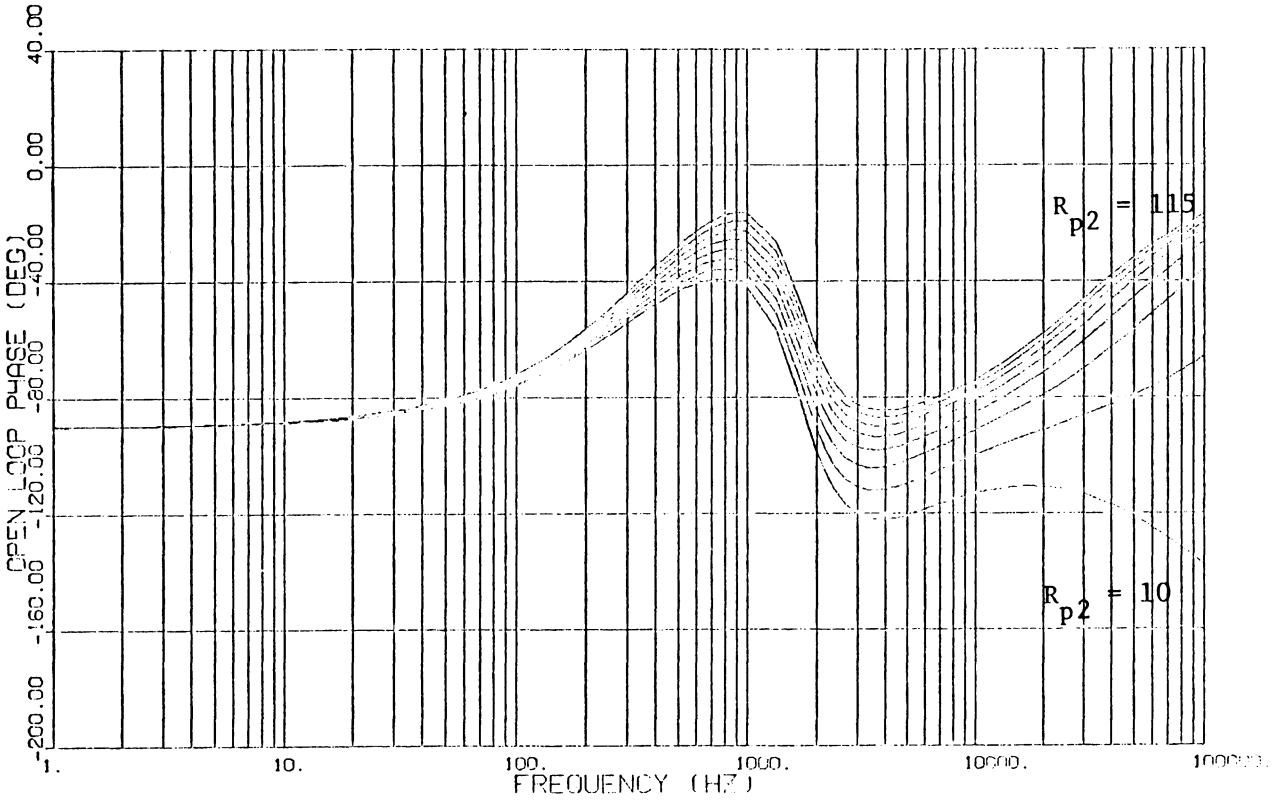


Fig. 4.11 (b) Open-Loop Phase by Changing R_{p2}

(R_{p2} = 10, 25, 40, 55, 70, 85, 100, 115)

performances didn't improve very much except for low-frequency.

Since the change of C_2 will not affect the performance at frequencies higher than S_{o1}, C_2 can be used to improve low-frequency gain independently without degrading the performance in the rest part of frequency spectrum. In the next chapter, we shall add a lead network to the system to form a lead-lag compensation network and discuss its effects.

CHAPTER V

ANALYSIS OF CURRENT-INJECTED CONTROL EMPLOYING A LEAD-LOG COMPENSATION NETWORK

Perhaps a most commonly used compensation network in achieving switching regulator control is in a corm of a lead-lag network as shown in Fig. 5.1. While in the previous chapter a lag compensation network in conjunction with the current injected loop was analyzed in considerable detail and its constraints and limitations were understood, a lead-lag compensation scheme is the subject of discussion in the present chapter to explore any possible benefit and/or additional control freedom.

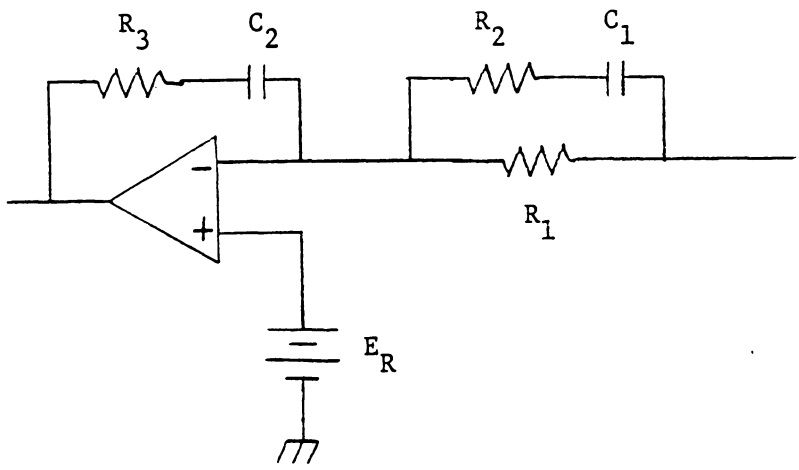
The transfer function of the lead-lag compensation network as shown in Fig. 5.1 (a) can be expressed as follows:

$$F_{DC} = \frac{(SR_3C_2 + 1)[S(R_1 + R_2)C_1 + 1]}{SR_1C_2\ (SR_2C_1 + 1)} \qquad (5.1)$$

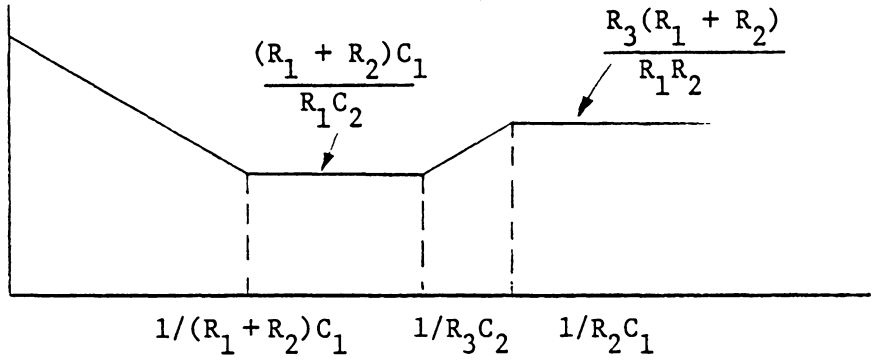
The characteristic of this network can be either the one shown in Fig. 5.1 (b) or the one shown in Fig. 5.1 (c), depending on the positions of the pole, -1/R2C1, and the zero, -1/R3C2.

Examining Fig. 5.1 (b) and (c), it appears that the characteristic curve shown in Fig. 5.1 (c) is more desirable than that of Fig. 5.1 (b).

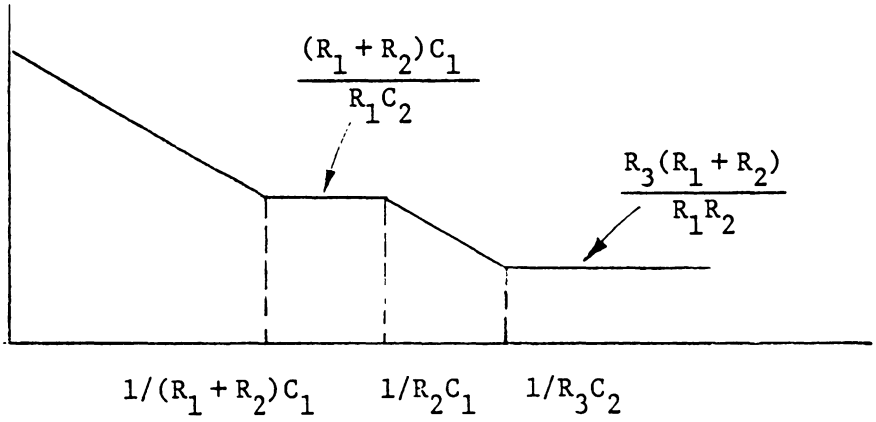
This is because the low-frequency gain and mid-frequency gain of Fig. 5.1 (c) are higher than the corresponding gains shown in Fig. 5.1 (b). Higher DC loop gain, in term, will boost the gain of the regular open-loop characteristic.



(a)



(b)



(c)

Fig. 5.1 LEAD-LAG COMPENSATION NETWORK AND ITS CHRACTERISTIC CURVE

5.1 Open-Loop Characteristic

Substitute eqs. (2.22), (2.25), (2.28) and (5.1) into eq. (3.1), the following formulation results:

$$G_T = F_M \cdot \omega_0^2 \cdot \frac{V_0}{DD'R_1C_2} \cdot \frac{S^4K_1 + S^3K_2 + S^2K_3 + SK_4 + K_5}{S(SR_2C_1 + 1)\ (S^2 + 2\zeta\omega_0\ S + \omega_0^2)} \qquad (5.2)$$

where

$$K_1 = \frac{DR_1C_2R_2C_1}{R_L\ \omega_0^2} \cdot \left[F_{AC}\frac{N_S}{N_P} - \frac{R_3\ R_c}{R_1 /\!/\ R_2}\right]$$

$$K_2 = \frac{1}{R_L\omega_0^2}\left[F_{AC}\ \frac{N_S}{N_P}\ DR_1C_2 - DR_cR_3C_2 - DR_c\ (R_1 + R_2)C_1\right]$$

$$+ R_3C_2\ (R_1 + R_2)\ C_1\left[R_cC - \frac{DL_e}{R_L}\right] + \frac{F_{AC}N_SC}{D'N_P}\ DR_1C_2R_2C_1$$

$$K_3 = R_3C_2(R_1 + R_2)C_1 + \left[R_3C_2 + (R_1 + R_2)C_1\right] \cdot \left[R_cC - \frac{DL_e}{R_L}\right] - \frac{DR_c}{R_L\omega_0^2}$$

$$+ \frac{F_{AC}N_SC}{D'N_P}\ DR_1C_2 + \frac{2F_{AC}N_S}{D'R_LN_P}\ DR_1C_2R_2C_1$$

$$K_4 = (R_1 + R_2)\ C_1 + R_3C_2 + R_cC - \frac{DL_e}{R_L} + \frac{2F_{AC}N_S}{D'R_LN_P}\ DR_1C_2$$

$$K_5 = 1$$

The numerator of eq. (5.2) can be expressed in terms of four zeros, S_{01}, S_{02}, S_{03} and S_{04}:

$$G_T = F_M \cdot \omega_0^2 \cdot \frac{V_0}{DD'R_1C_2} \cdot \frac{(S/S_{01}+1)(S/S_{02}+1)(S/S_{03}+1)(S/S_{04}+1)}{S(SR_2C_1+1)(S^2+2\zeta\omega_0 S+\omega_0^2)} \quad (5.3)$$

and

$$K_1 = \frac{1}{S_{01} \cdot S_{02} \cdot S_{03} \cdot S_{04}}$$

$$K_2 = \frac{1}{S_{01} \cdot S_{02} \cdot S_{03}} + \frac{1}{S_{01} \cdot S_{02} \cdot S_{04}} + \frac{1}{S_{01} \cdot S_{03} \cdot S_{04}} + \frac{1}{S_{02} \cdot S_{03} \cdot S_{04}}$$

$$K_3 = \frac{1}{S_{01} \cdot S_{02}} + \left(\frac{1}{S_{01}}+\frac{1}{S_{02}}\right) \cdot \left(\frac{1}{S_{03}}+\frac{1}{S_{04}}\right) + \frac{1}{S_{03} \cdot S_{04}}$$

$$K_4 = \frac{1}{S_{01}} + \frac{1}{S_{02}} + \frac{1}{S_{03}} + \frac{1}{S_{04}}$$

If the four zeros are sufficiently apart, i.e. $1/S_{01} >> 1/S_{02} >> 1/S_{03} >> 1/S_{04}$, the following approximations hold true:

$$K_4 \simeq \frac{1}{S_{01}}$$

$$K_3 \simeq \frac{1}{S_{01} \cdot S_{02}}$$

$$K_2 \simeq \frac{1}{S_{01} \cdot S_{02} \cdot S_{03}}$$

therefore,

$$1/S_{01} \simeq K_4$$

$$1/S_{02} \simeq K_3/K_4$$

$$1/S_{03} \simeq K_2/K_3$$

$$1/S_{04} \simeq K_1/K_2$$

The new system now has one more low-frequency zero than the previous system (with lag compesnator). Following the same statement as in 4.1, it is reasonable to assume the two low-frequency zeros are the zeros of F_{DC}, hence

$$S_{01} \simeq 1/(R_1 + R_2)C_1 \tag{5.4}$$

$$S_{02} \simeq 1/R_3C_2 \tag{5.5}$$

$$S_{03} \simeq K_3/K_2 \simeq \frac{1}{K_2 \cdot S_{01} \cdot S_{02}} \simeq \frac{\dfrac{R_3}{D(R_1//R_2)}}{\dfrac{F_{AC}N_SC}{D'N_P} + \dfrac{R_3}{D(R_1//R_2)}\left(R_cC - \dfrac{DL_e}{R_L}\right)} \tag{5.6}$$

$$S_{04} \simeq K_1/K_2 \simeq R_L\,\omega_0^2 \cdot \frac{\dfrac{F_{AC}N_SC}{D'N_P} + \dfrac{R_3}{D(R_1//R_2)}\left(R_cC - \dfrac{DL_e}{R_L}\right)}{F_{AC}\dfrac{N_S}{N_P} - \dfrac{R_3R_c}{R_1//R_2}} \tag{5.7}$$

and let $S_{P2} = 1/R_2C_1$ (5.8)

Similarities are found between the two high frequency zeros in this case and the two high-frequency zeros in the case of lag compensation network as discussed in the previous chapter with the exception that R_1 in eqs. (4.6) is replaced by $R_1//R_2$ in eqs. (5.7). One of the low-frequency zero, S_{02}, is the same as S_{01} in previous case. The only noticable difference in the open-loop characteristic is the low-frequency zero S_{01} and the low-frequency pole S_{P2}, which alter the low-frequency characteristic somewhat, as illustrated in Fig. 5.2.

The open-loop gain in each frequency range is approximated by the following equations if all corner frequencies are sufficiently apart:

$$S < S_{01} \qquad G_T \simeq F_M \cdot \omega_0^2 \cdot \frac{V_0}{DD'R_1C_2} \cdot \frac{1}{S \cdot \omega_0^2}$$

$$= F_M \cdot \frac{V_0}{DD'R_1C_2} \cdot \frac{1}{S} \tag{5.9}$$

$$S_{01} < S < S_{P2} \qquad G_T \simeq F_M \cdot \omega_0^2 \cdot \frac{V_0}{DD'R_1C_2} \cdot \frac{S/S_{01}}{S \cdot \omega_0^2}$$

$$= F_M \cdot \frac{V_0}{DD'} \cdot \frac{(R_1 + R_2)C_1}{R_1C_2} \tag{5.10}$$

$$S_{P2} < S < S_{02} \qquad G_T \simeq F_M \cdot \omega_0^2 \cdot \frac{V_0}{DD'R_1C_2} \cdot \frac{S/S_{01}}{S \cdot SR_2C_1 \cdot \omega_0^2}$$

$$= F_M \cdot \frac{V_0}{DD'} \cdot \frac{1}{(R_1//R_2)C_2} \cdot \frac{1}{S} \tag{5.11}$$

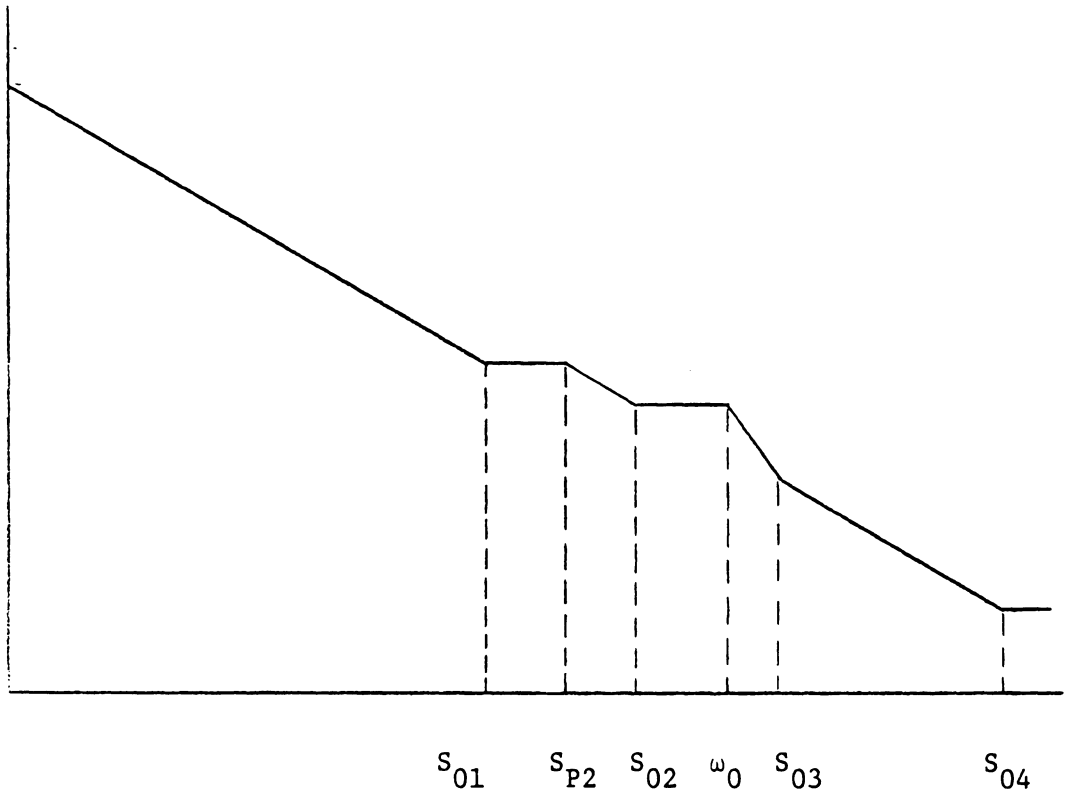


FIG. 5.2 OPEN-LOOP ASYMPTOTIC CURVE

$$S_{02} < S < \omega_0 \qquad G_T \simeq F_M \cdot \omega_0^2 \cdot \frac{V_0}{DD'R_1C_2} \cdot \frac{S/S_{01} \cdot S/S_{02}}{S \cdot SR_2C_1 \cdot \omega_0^2}$$

$$= F_M \cdot \frac{V_0}{DD'} \cdot \frac{R_3}{R_1//R_2} \tag{5.12}$$

$$\omega_0 < S < S_{03} \qquad G_T \simeq F_M \cdot \omega_0^2 \cdot \frac{V_0}{DD'R_1C_2} \cdot \frac{S/S_{01} \cdot S/S_{02}}{S \cdot SR_2C_1 \cdot (S^2 + 2\zeta\omega_0 S + \omega_0^2)}$$

$$= F_M \cdot \frac{V_0}{DD'} \cdot \frac{R_3}{R_1//R_2} \cdot \frac{\omega_0^2}{S^2 + 2\zeta\omega_0 S + \omega_0^2} \tag{5.13}$$

$$S_{03} < S < S_{04} \qquad G_T \simeq F_M \cdot \omega_0^2 \cdot \frac{V_0}{DD'R_1C_2} \cdot \frac{S/S_{01} \cdot S/S_{02} \cdot S/S_{03}}{S \cdot SR_2C_1 \cdot (S^2 + 2\zeta\omega_0 S + \omega_0^2)}$$

$$= F_M \cdot \frac{V_0}{D'} \cdot \left[\frac{R_3}{D(R_1//R_2)}\left(R_cC - \frac{DL_e}{R_L}\right) + \frac{F_{AC}N_SC}{D'N_P} \right] \cdot \frac{S \cdot \omega_0^2}{S^2 + 2\zeta\omega_0 S + \omega_0^2} \tag{5.14}$$

$$S > S_{04} \qquad G_T \simeq F_M \cdot \omega_0^2 \cdot \frac{V_0}{DD'R_1C_2} \cdot \frac{S/S_{01} \cdot S/S_{02} \cdot S/S_{03} \cdot S/S_{04}}{S \cdot SR_2C_1 \cdot S^2}$$

$$= F_M \cdot \frac{V_0}{D'R_L} \cdot \left(F_{AC} \frac{N_S}{N_P} - \frac{R_3R_c}{R_1//R_2} \right) \tag{5.15}$$

The computer plots of the open-loop gain and phase are shown in Fig. 5.3 (a) & (b), where R2 and R3 are arbitrarily chosen to be 5 KΩ and 1 KΩ.

5.2 Stability Criteria and Constraints

If the negative terms in eqs. (5.6), (5.7) become predominant S_{04} and/or S_{03} can be positive zero(s), which can degrade system performance drastically. To avoid positive zero, two constraints derived from eqs. (5.6) and (5.7) must not be violated:

$$\text{first constraint: } F_{AC}\frac{N_S}{N_P} > \frac{R_3 R_c}{R_1 // R_2} \tag{5.16}$$

$$\text{second constraint: } F_{AC}\frac{N_S}{N_P} > \frac{R_3 R_c}{R_1 // R_2}\left(\frac{D' L_e}{R_L R_c C} - \frac{D'}{D}\right) \tag{5.17}$$

Basically, these are the same constraints as shown in previous cases except now R1 is replaced by R1//R2. Because at high frequency, the gain of F_{DC} can be approximated by R3/(R1//R2) rather than R3/R1 as in previous cases. Since these constraints are basically very similar to those constraints as established in the previous cases, it is not surprising that adding one more compensation network, R2C1, will not improve open-loop gain and phase significantly.

5.3 Effects of Compensation Network Parameters

Examining eqs. (5.12)-(5.15), one can find that these equations are of the same forms as comparing to the previous case for frequency higher than S_{02}. The following parametric study is performed to investigate any added benefit with the additional R2C1 compensation network.

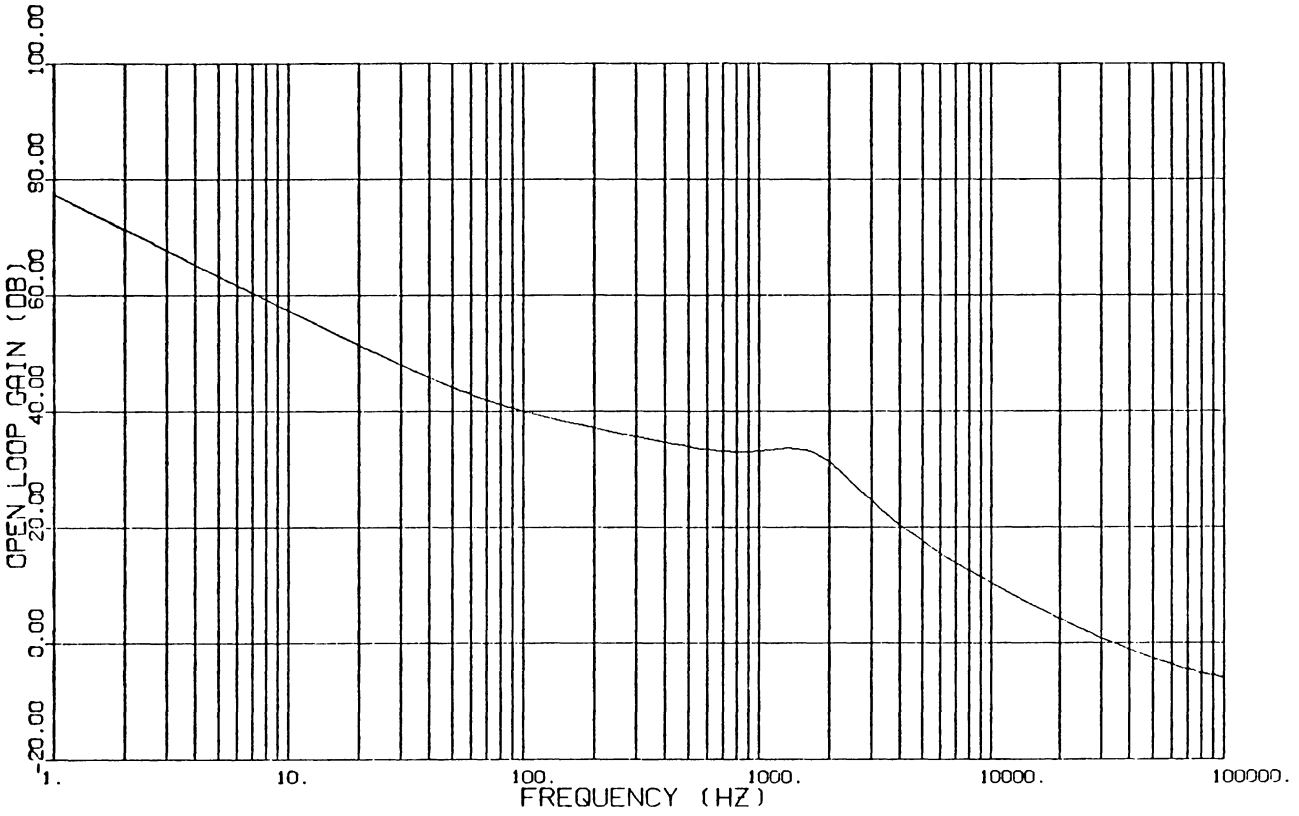


FIG. 5.3(a) OPEN-LOOP GAIN USING LEAD-LAG COMPENSATION NETWORK

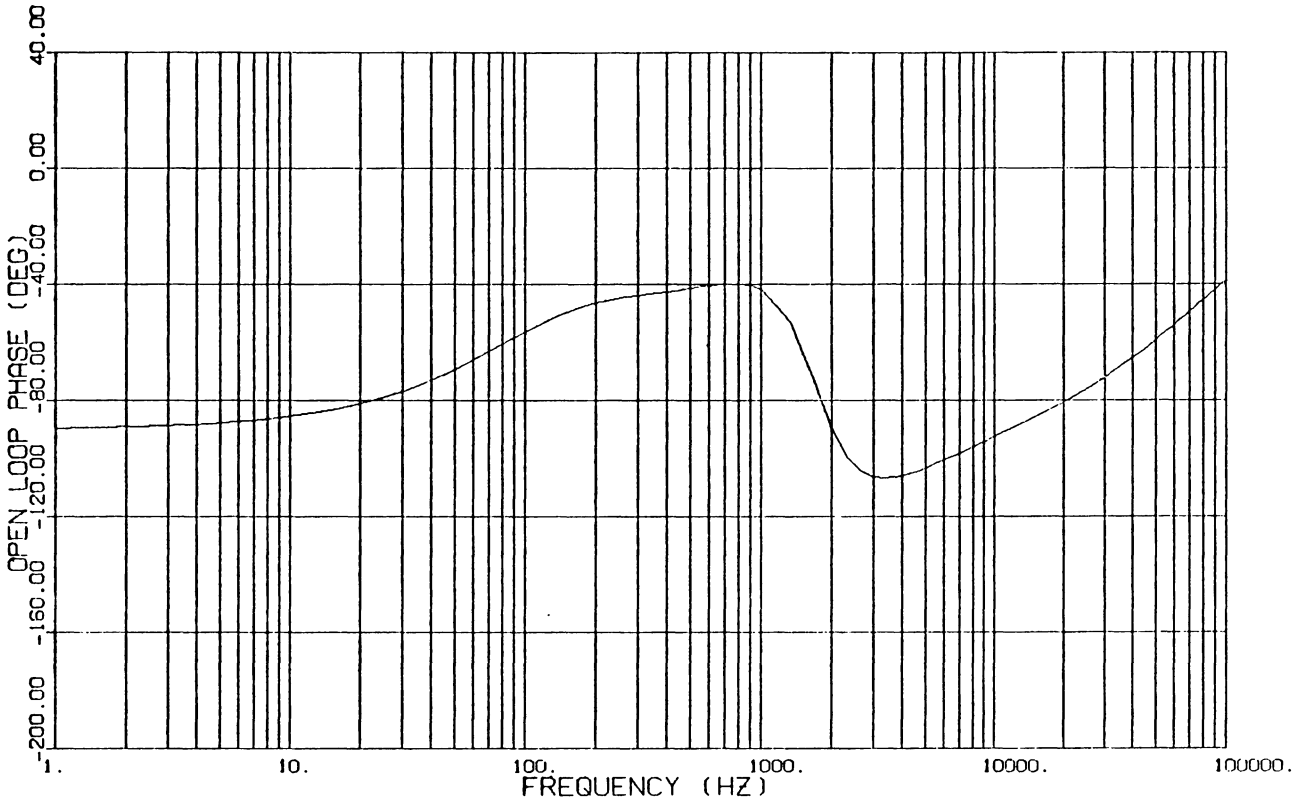


FIG. 5.3(b) OPEN-LOOP PHASE USING LEAD-LAG COMPENSATION NETWORK

Case 1: Variation of R1

Usually, in the actual circuit design R1 is much greater than R2. With this assumption only loop gain below S_{01} and the zero S_{01} will be changed accordingly. The effect of varying R1 to the higher frequency gain and phase are negligible. Fig. 5.4 illustrates the asymptotic curve as R1 changes. Fig. 5.5 (a), (b) show the open-loop gain and phase.

Case 2: Variation of R2

An increase of R2 primarily will cause S_{p2} to reduce, and consequently, a reduction of loop gain at frequencies above S_{p2}. As a secondary effect, an increase of R2 will result to reductions of S_{01}, S_{03}, S_{04}. Fig. 5.6 illustrates the asymptotic curve by changing R2, Fig. 5.7 (a), (b) are the gain and phase plots. Since R3/(R1//R2) acts as a single factor at frequencies higher than , gain variations at frequencies higher than S_{02} are the same in this case as of the previous case by changing R1. Changing R2 will not affect loop gain at frequencies below S_{02}. Therefore, variation of R2 only provides limited amounts of adjustment to the loop characteristics.

Case 3: Variation of R3

An increase of R3 will cause primarily a decrease of S_{02} and an increase of the corresponding loop gain at frequencies higher than S_{02}. Fig. 5.8 illustrates the asymptotic curve by changing R3, Fig. 5.9 shows the gain and phase plots. Change R3 will not affect system characteristic at frequencies lower than S_{02}. But as R3 increases such that the loop gain is increased, the design constraints (5.16), (5.17) are soon violated.

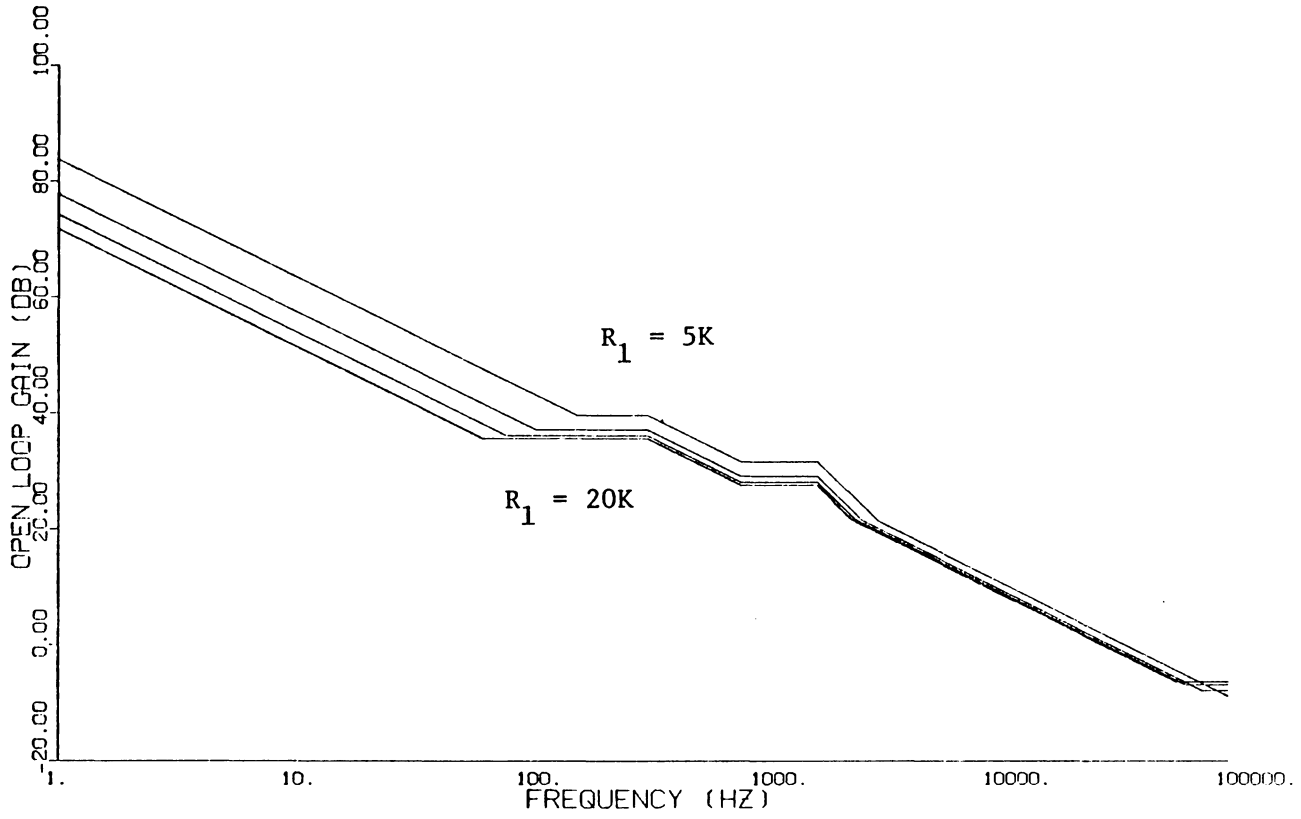


Fig. 5.4 ASSYMPTOTIC CURVE SHOWING THE EFFECTS OF R_1 (R_1 = 5K, 10K, 15K, 20K)

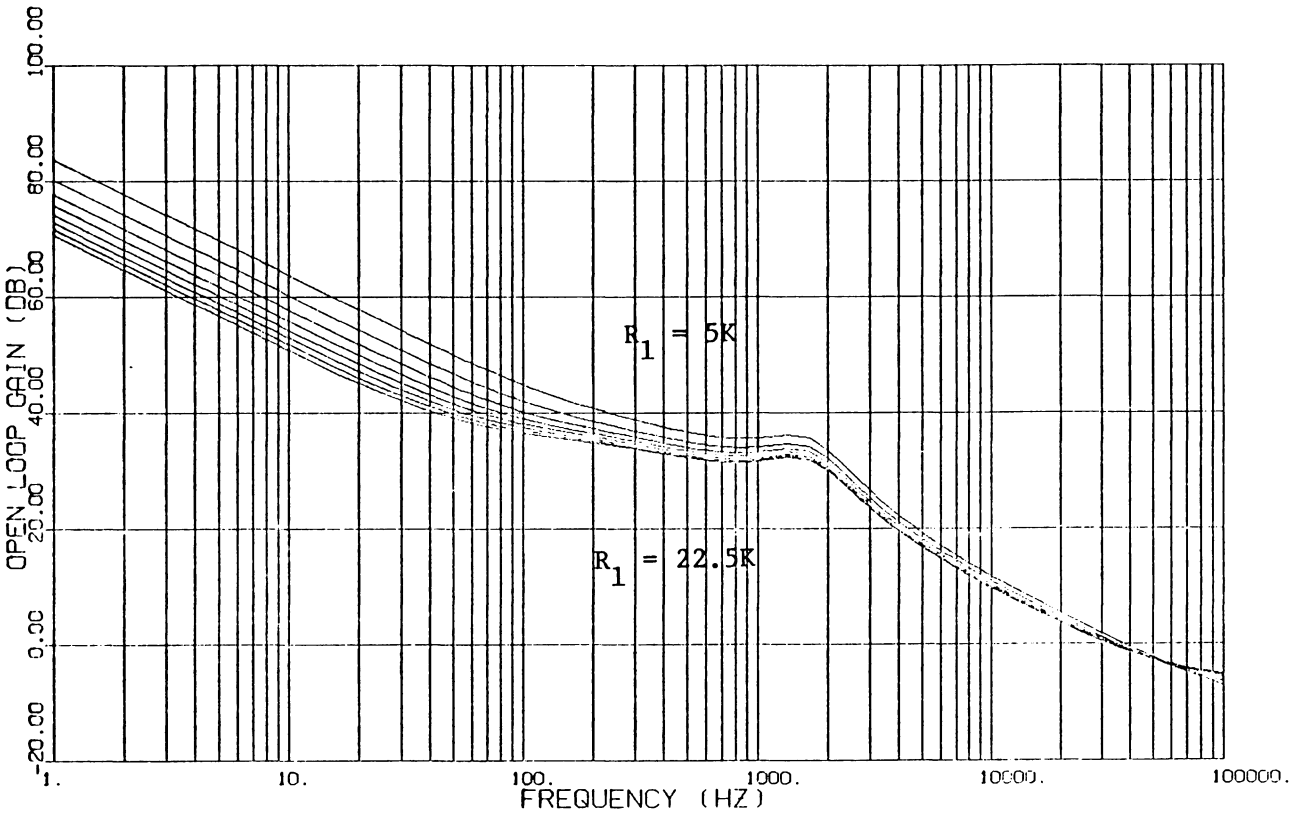


FIG. 5.5(a) OPEN-LOOP GAIN BY CHANGING R_1 (R_1 = 5K, 7.5K, 10K, 12.5K, 15K, 17.5K, 20K, 22.5K)

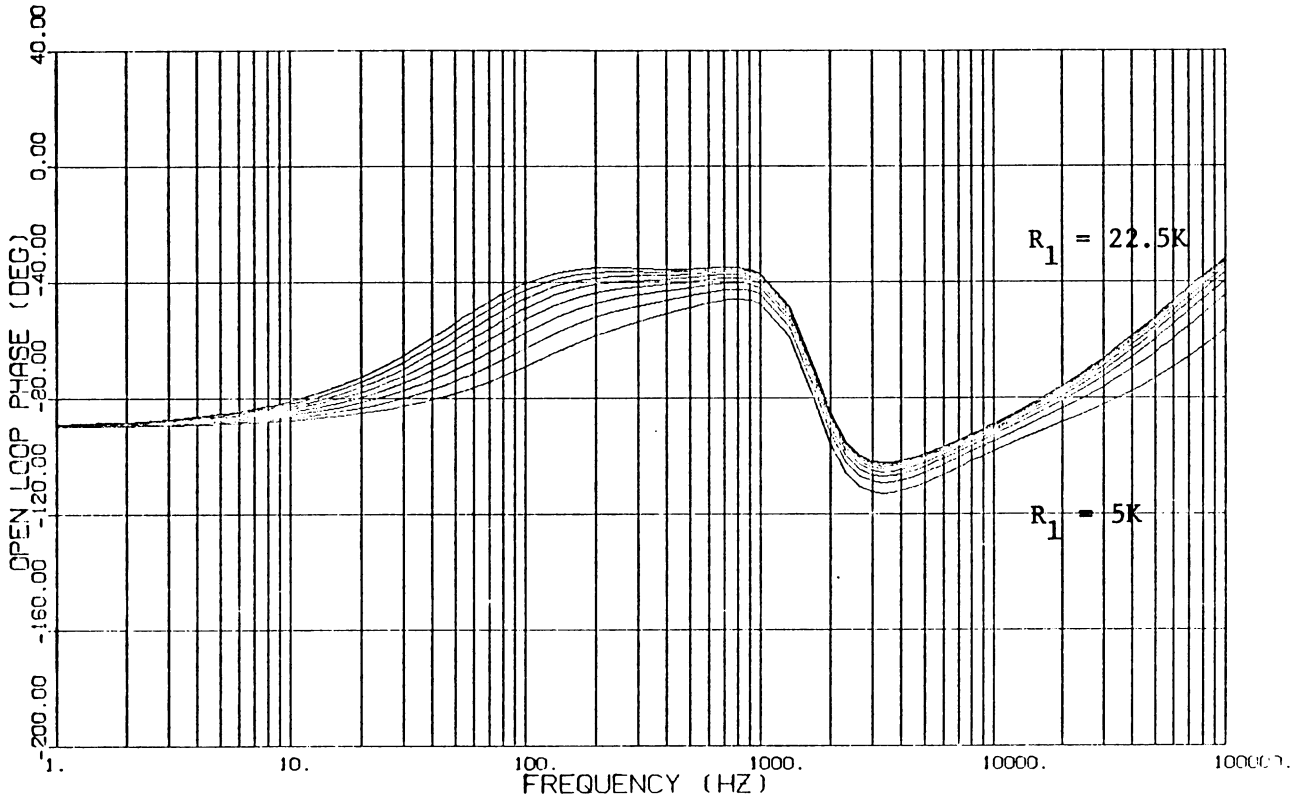


FIG. 5.5(b) OPEN-LOOP PHASE BY CHANGING R_1

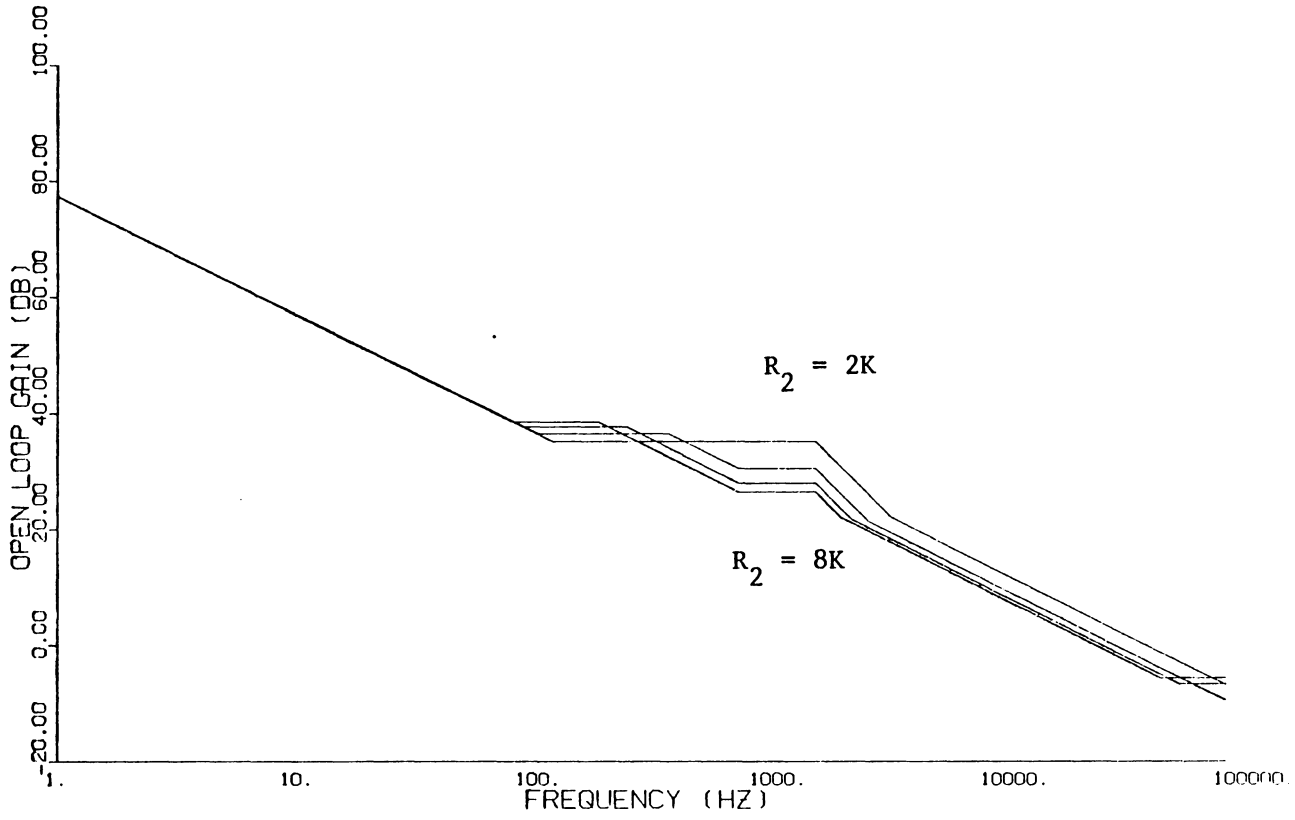


FIG. 5.6 ASYMPTOTIC CURVE SHOWING THE EFFECTS OF R_1(R_1 = 2K, 4K, 6K, 8K)

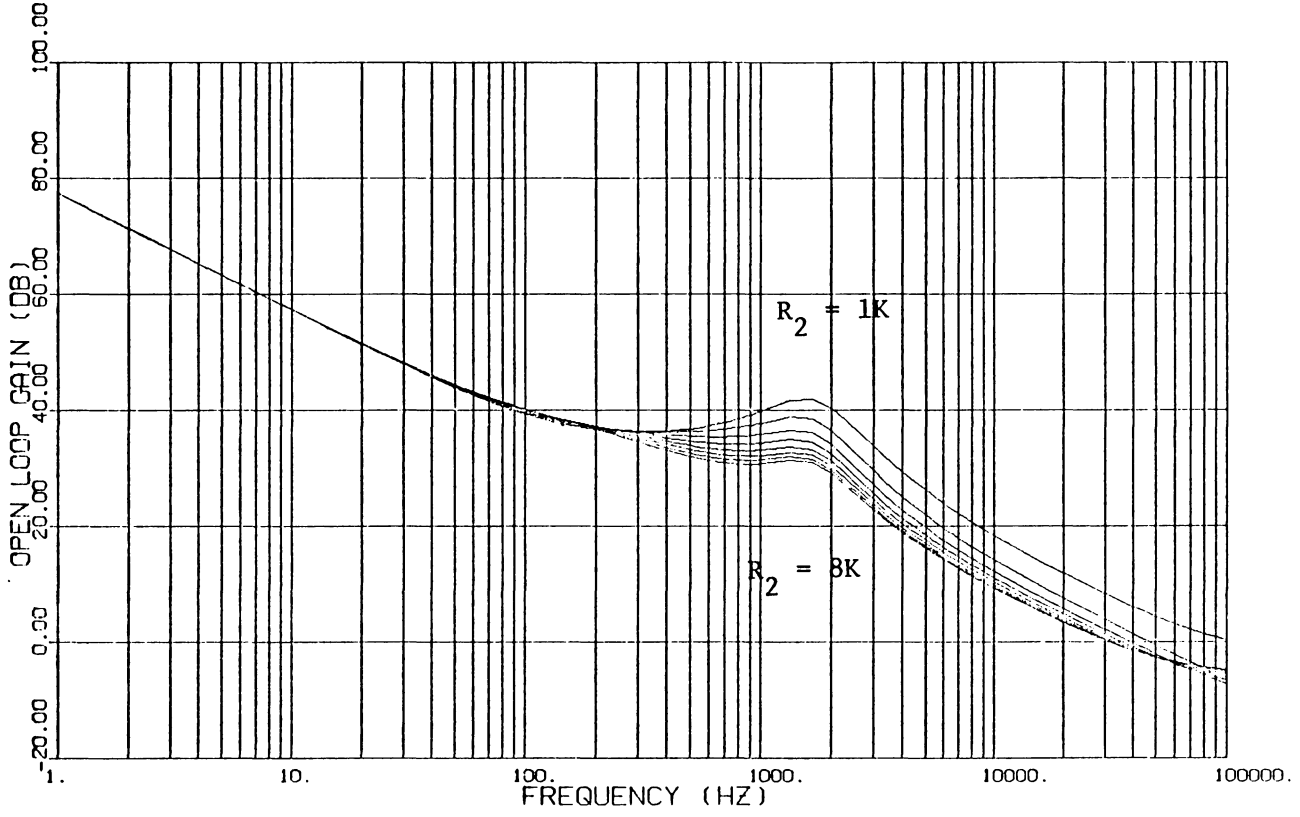


FIG. 5.7(a) OPEN-LOOP GAIN BY CHANGING R_2

(R_2 = 1K, 2K, 3K, 4K, 5K, 6K, 7K, 8K)

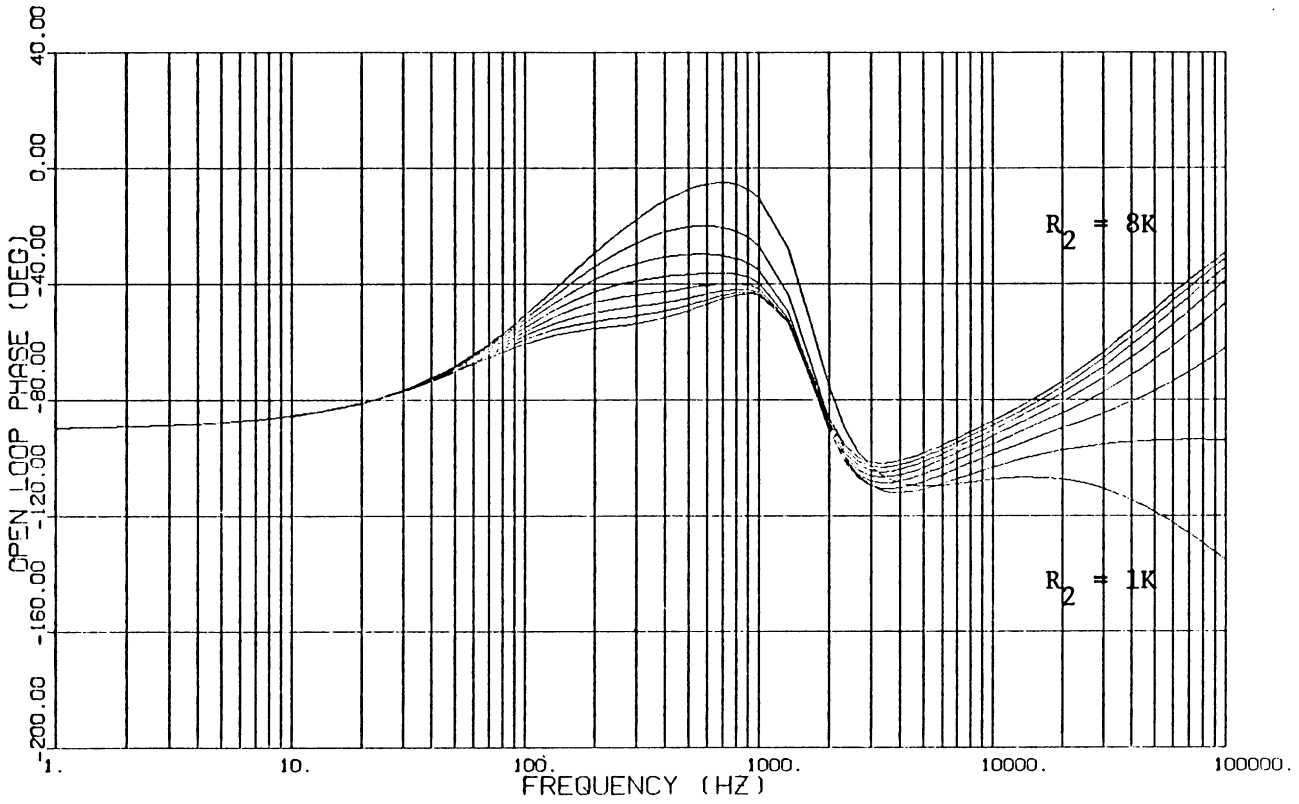


FIG. 5.7(b) OPEN-LOOP PHASE BY CHANGING R_2

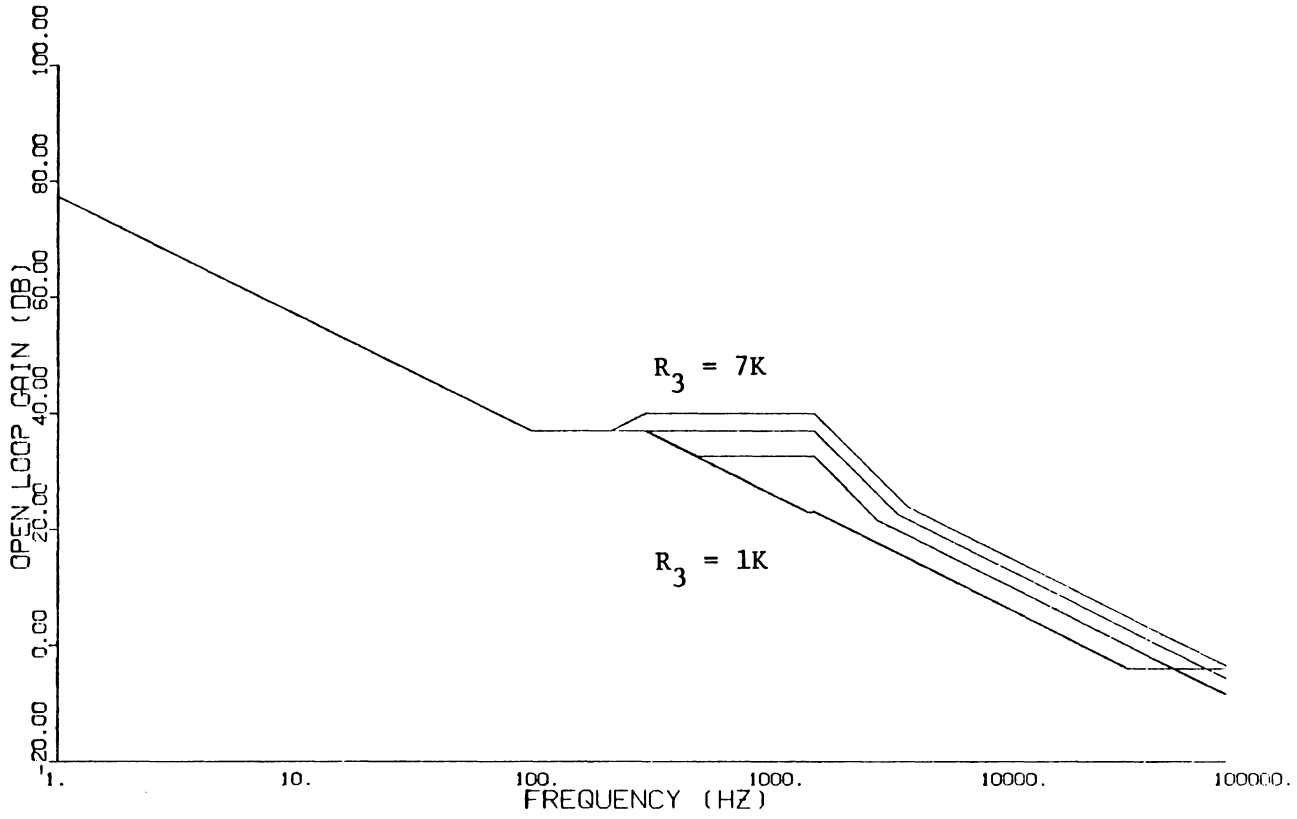


FIG. 5.8 ASYMPTOTIC CURVE SHOWING THE EFFECTS OF R_3(R_3 = 7K, 5K, 3K, 1K)

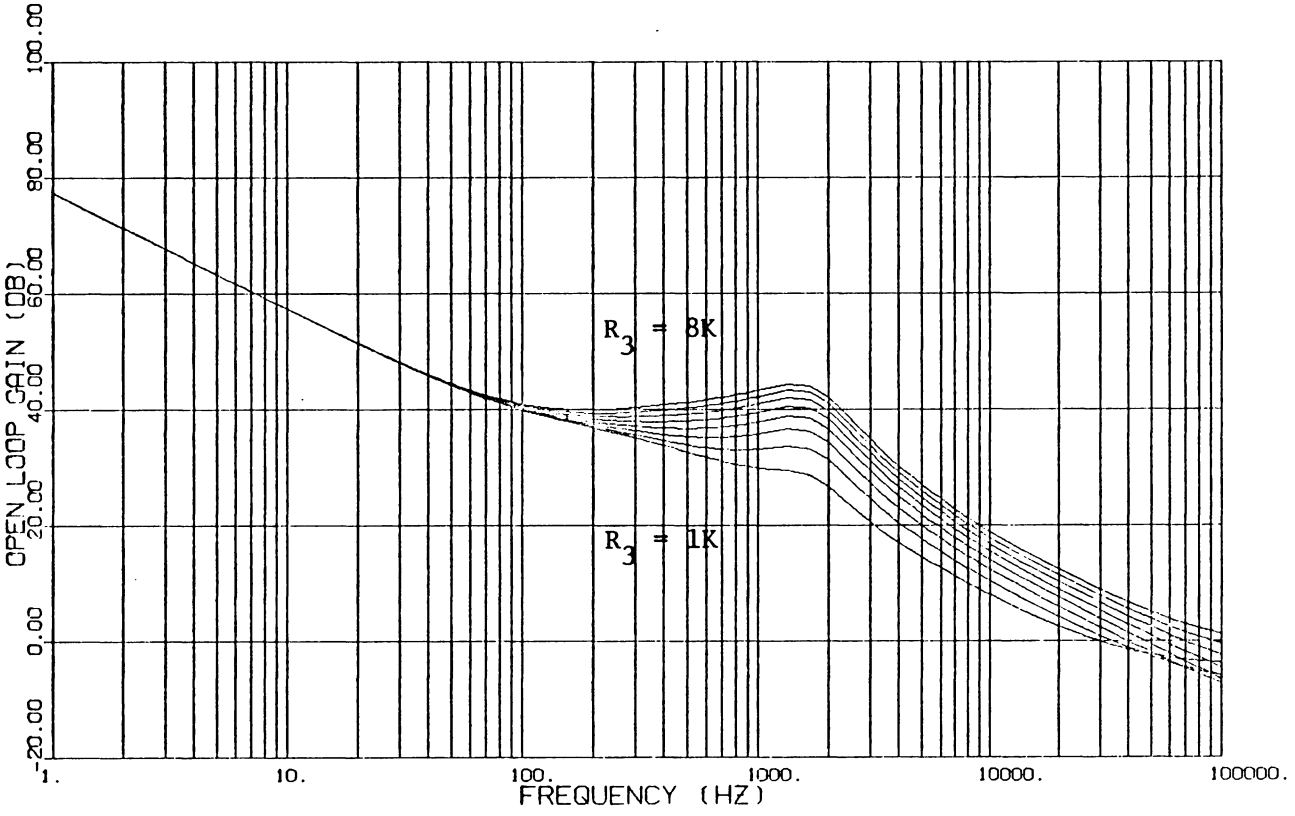


FIG. 5.9(a) OPEN-LOOP GAIN BY CHANGING R_3

(R_3 = 8K, 7K, 5K, 5K, 4K, 3K, 2K, 1K)

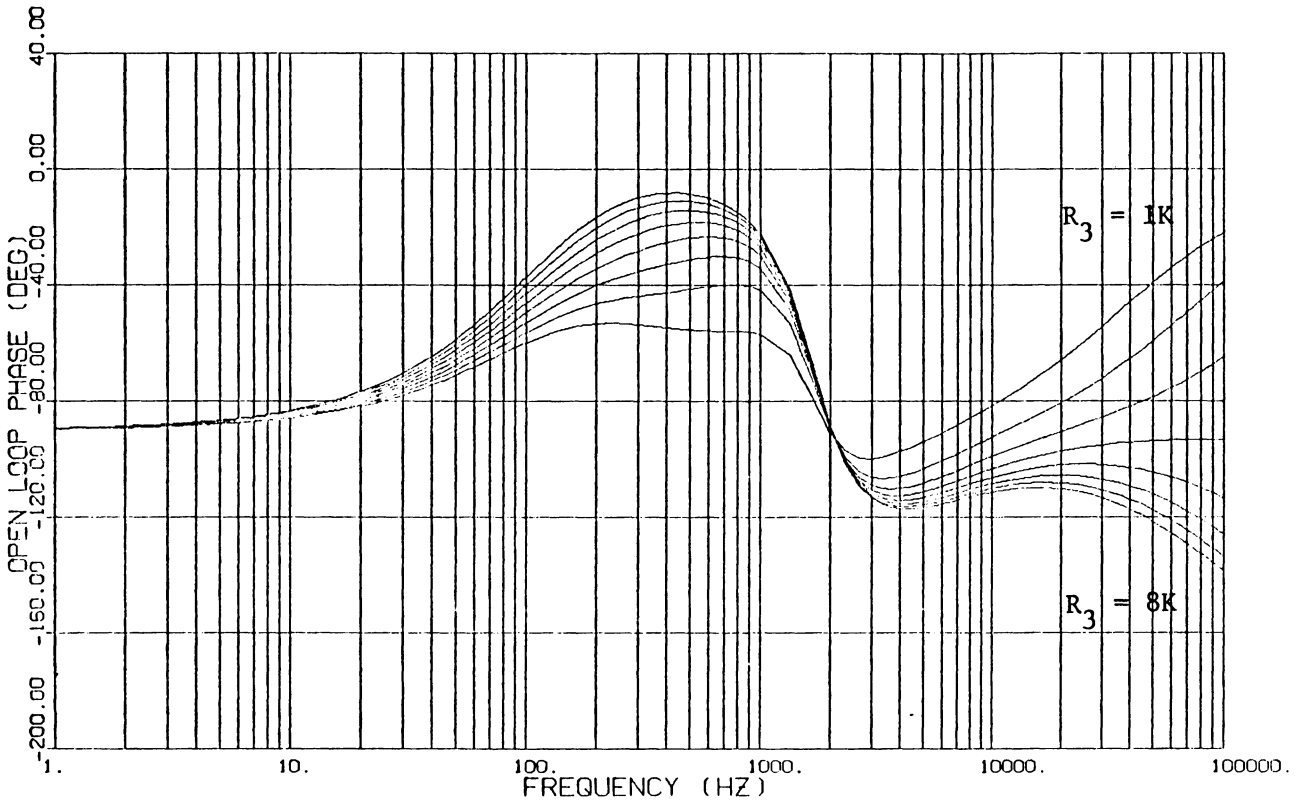


FIG. 5.9(b) OPEN-LOOP PHASE BY CHANGING R_3

Consequently a positive zero is generated and the phase delay of the open-loop is rapidly degenerated as shown in Fig. 5.9 (b).

Case 4: Variations of C1 and C2

Increase C1 will cause:

.S_{01} to decrease,

.S_{p2} to decrease,

.S_{02}, S_{03} and S_{04} to remain constant,

.system gain at frequencies between S_{01} and S_{p2} to increase,

.system gain at other frequencies to remain constant.

Fig. 5.10 illustrates the asymptotic curve and Fig. 5.11 shows the gain and phase plots by changing C1. Consequently it provides very limited control.

Fig. 5.12 and Fig. 5.13 show the gain and phase plots. Using C2 as a parameter. Decrease C2 will increase low frequency gain but system characteristic is not affected at frequencies higher than S_{02}.

5.4 Discussion

As stated earlier, the two design constraints that eliminate positive zeros exist not only in the case of a simple gain compensation and the compensation employing a lag network but also in the more complex case, lead-lag compensation. The two constraints state a basic relation that must be satisfied between AC loop and DC loop at high frequencies. These two constraints, in general, are independent of the three different forms of compensation that has been analyzed up to now.

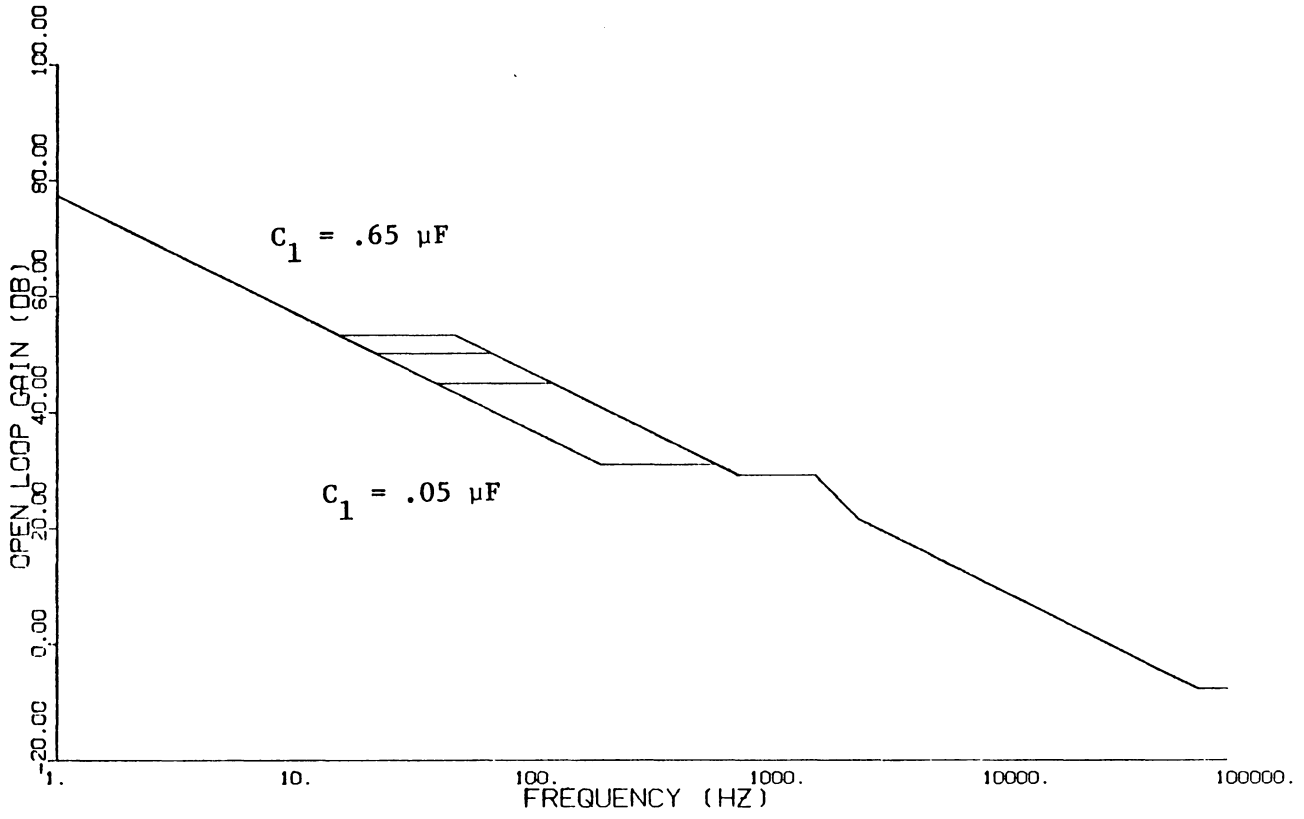


FIG. 5.10 ASYMPTOTIC CURVE SHOWING THE EFFECTS OF C_1

(C_1 = .65 μF, .45 μF, .25 μF, .05 μF)

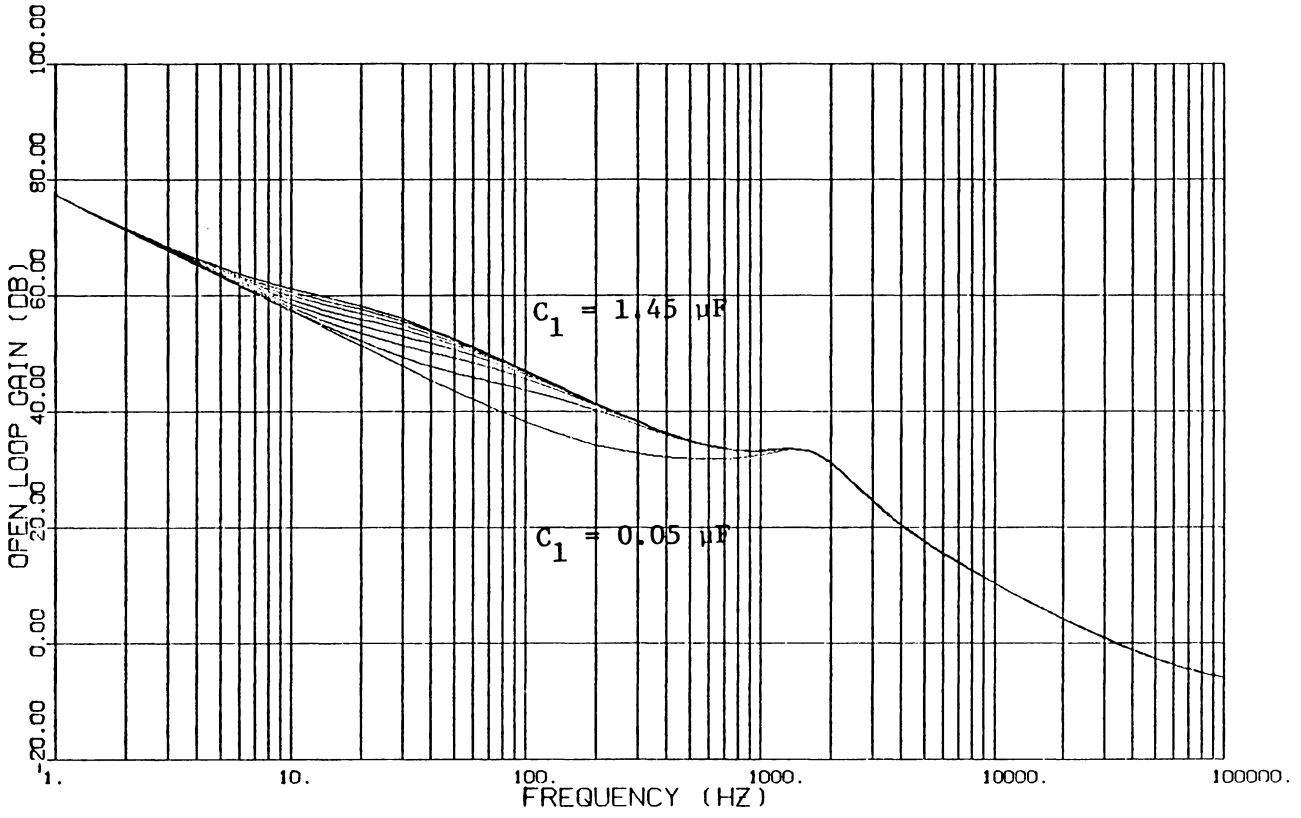


FIG. 5.11(a) OPEN-LOOP GAIN BY CHANGING C_1

(C_1 = 1.45 μF, 1.25 μF, 1.05 μF, .85 μF, .65 μF,

.45 μF, .24 μF, .05 μF)

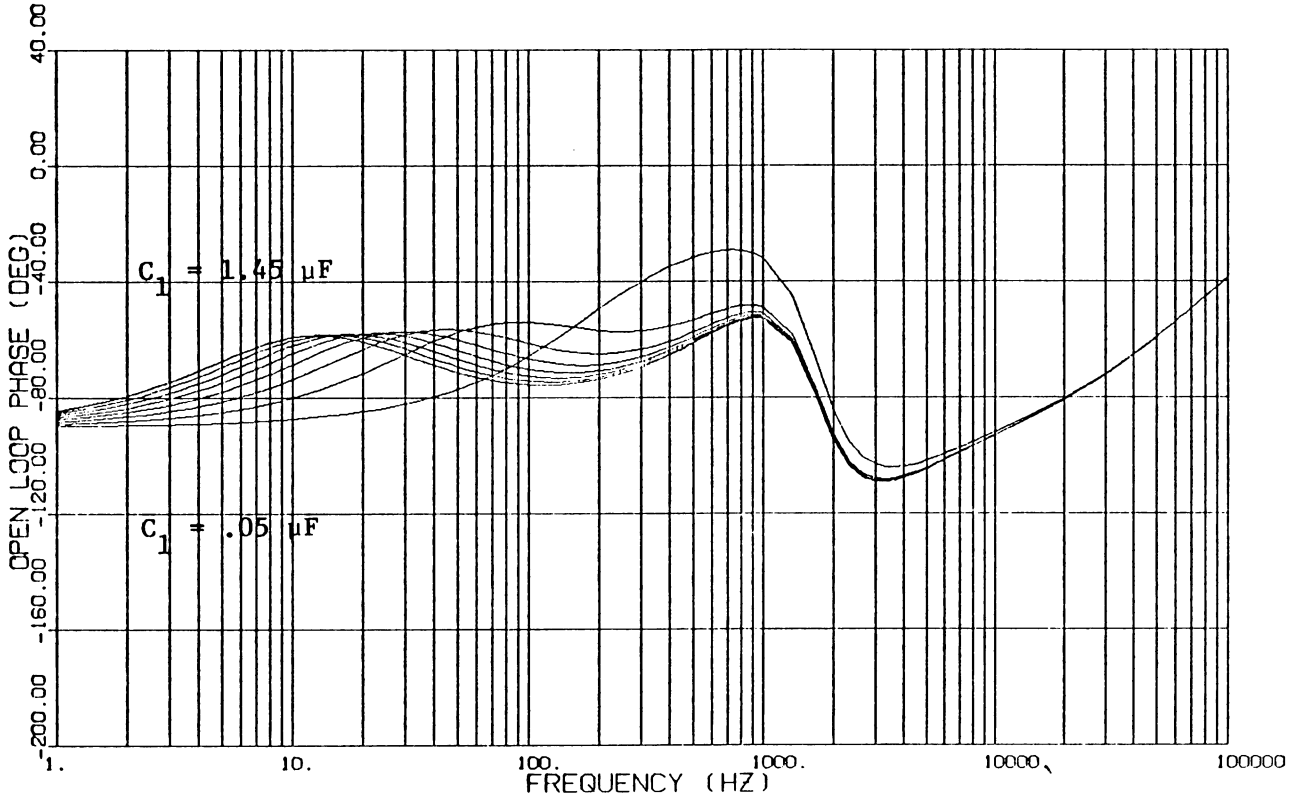


FIG. 5.11(b) OPEN-LOOP PHASE BY CHANGING C_1

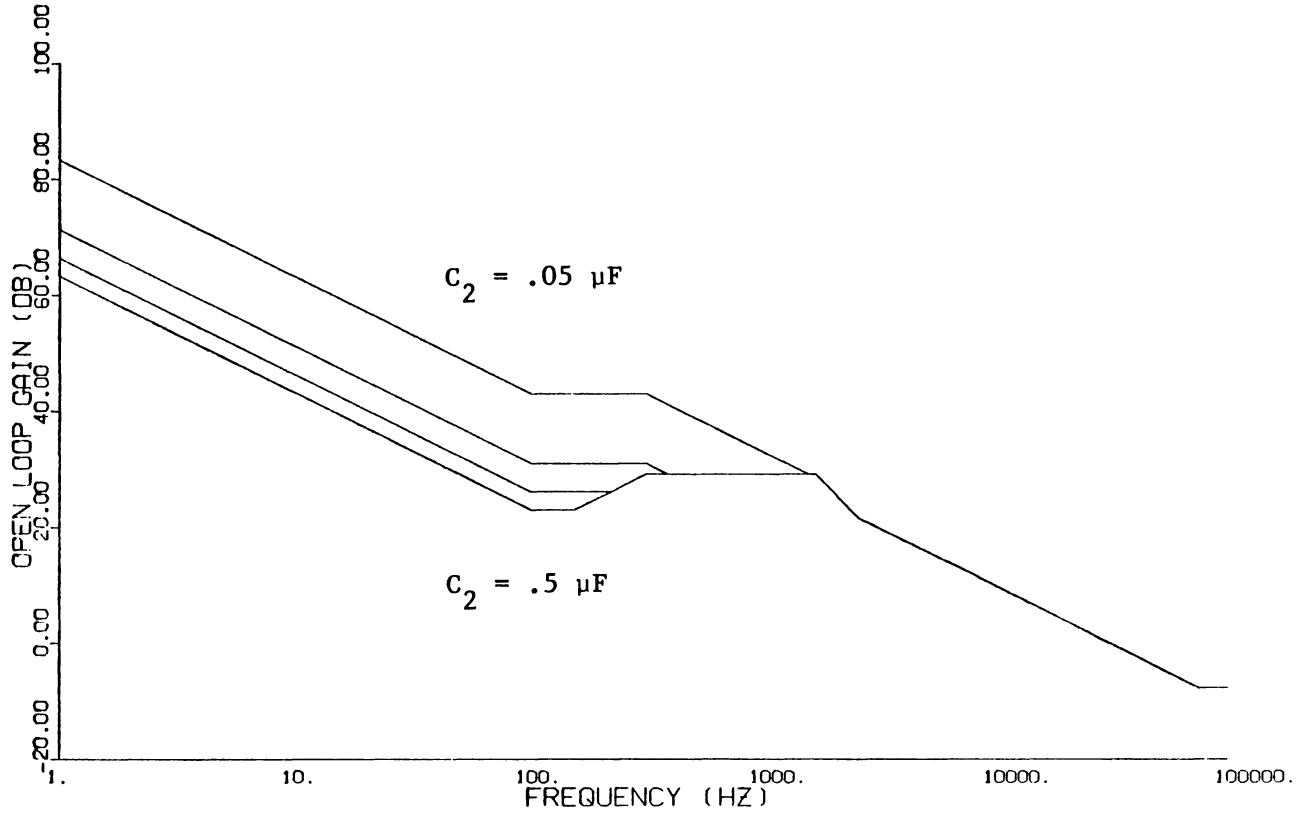


FIG. 5.12 ASYMPTOTIC CURVE SHOWING THE EFFECTS OF C_2

(C_2 = .05 μF, .2 μF, .35 μF, .5 μF)

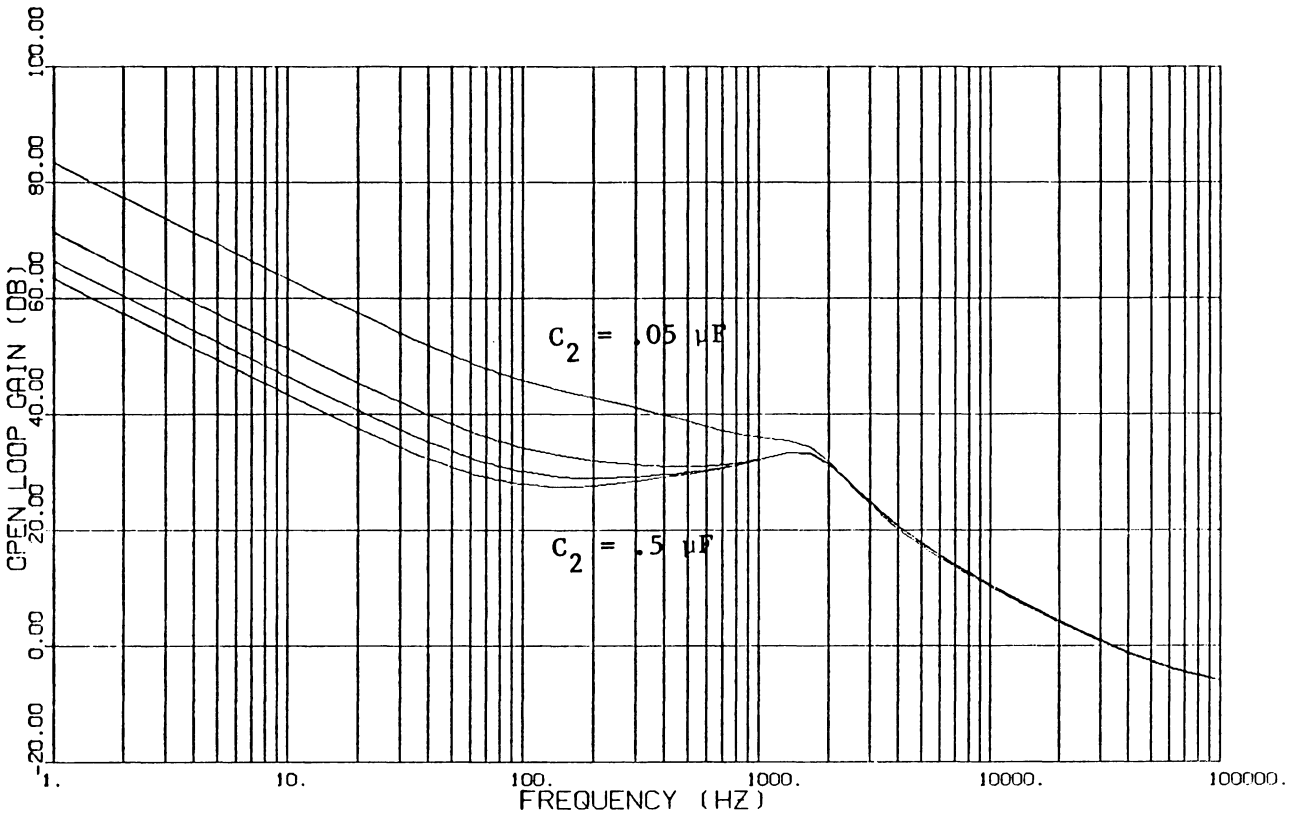


FIG. 5.13 (a) OPEN-LOOP GAIN BY CHANGING C_2

(C_2 = .05 μF, .2 μF, .35 μF, .5 μF)

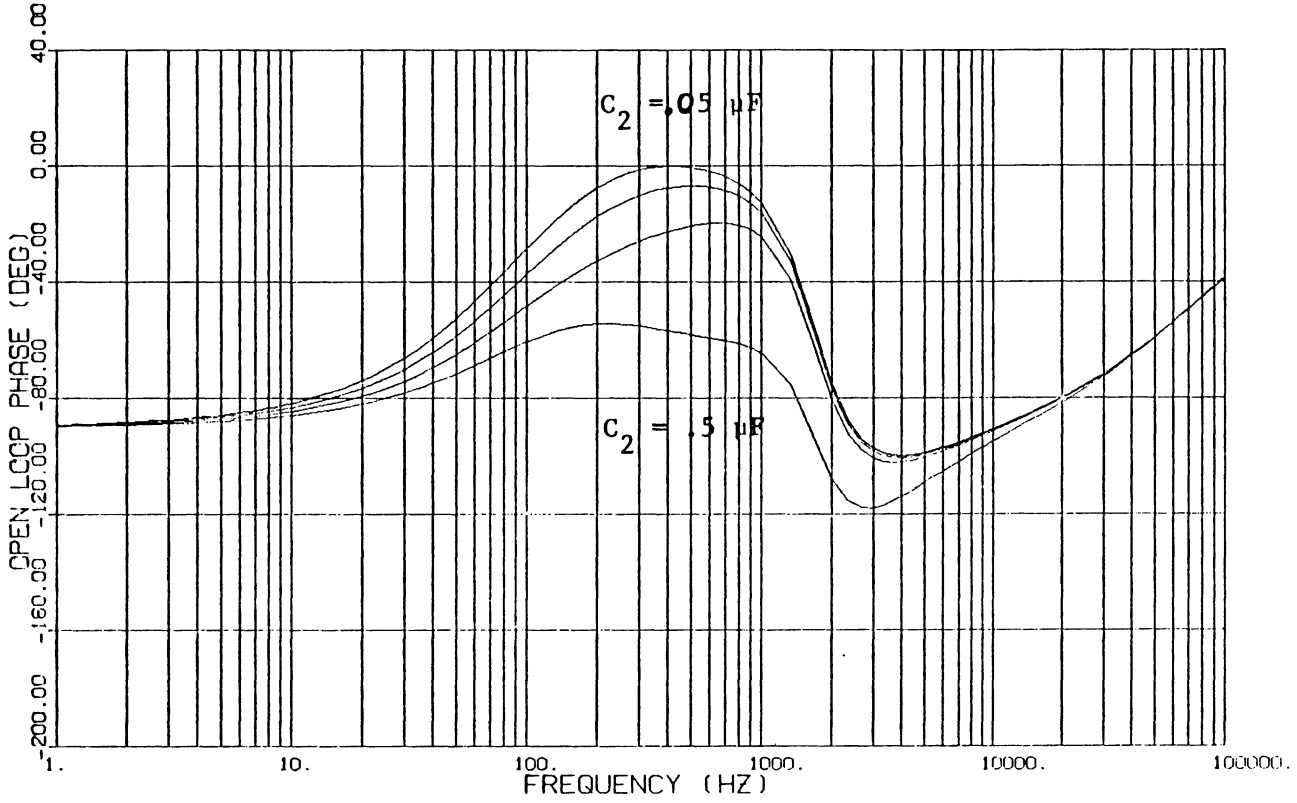


FIG. 5.13(b) OPEN-LOOP PHASE BY CHANGING C_2

Besides the two constraints, there are several inherent limitations that forbid us to manipulate the system characteristic so as to obtain satisfactory performance characteristics. First, S_{03} and S_{04} are both functions of R3/(R1//R2), they can not be independently adjusted. Second, an increase of mid-frequency gain in an attempt to improve audiosusceptibility, output impedance often result in a severe reduction of phase margin at a frequency higher than W_0 due to the increase of S_{03}. Sufficient loop gain and phase margin are difficult to achieve simultaneously in a design practice.

Based on the study presented in this chapter no apparent benefit is observed using the lead-lag compensation in comparison with the simple lag compensation scheme. Since the basic limitation is set by the maximum value of R3/(R1//R2) such that the constraints will not be violated, it appears that the best achievable design is by letting $S_{p2}=S_{01}$ or $R2=\infty$. Such a characteristic can be achieved by simply using the lag compensation network alone. The conclusion is quite surprising, since it is generally recognized that a lead-lag compensation is usually more desirable than lag network for switching regulator control.

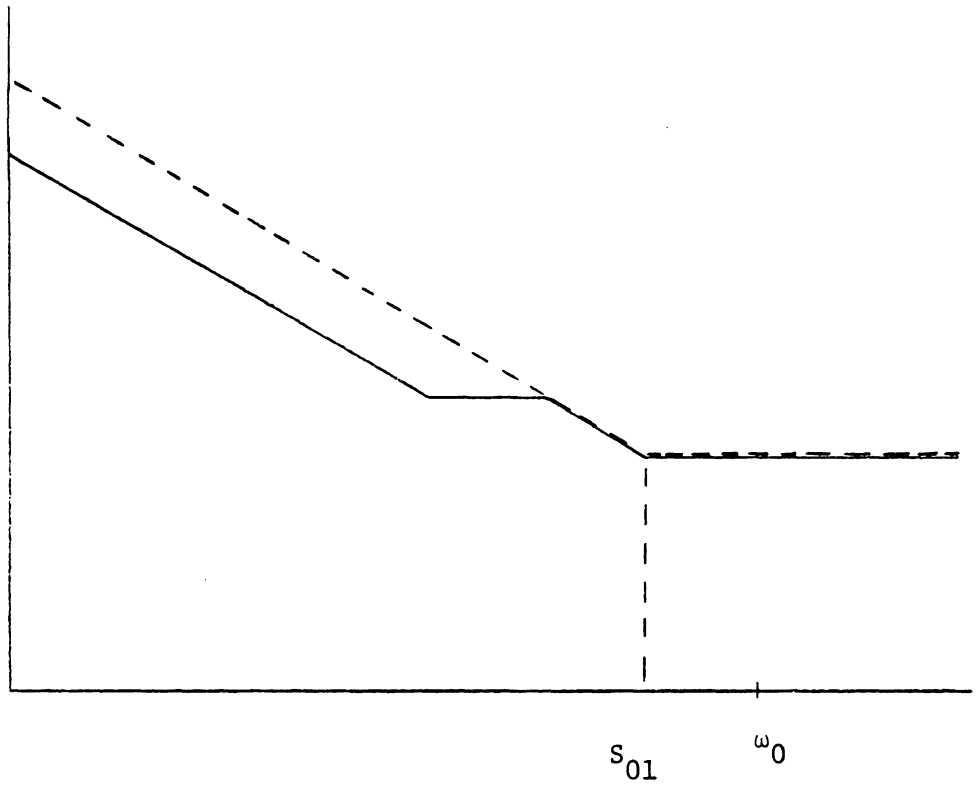


FIG. 5.14 LEAD-LAG COMPENSATION CHARACTERISTIC AS COMPARED TO LAG COMPENSATION

CHAPTER VI

EFFECTS OF DUTY CYCLE PULSE MODULATOR

We have employed constant frequency control law for duty cycle pulse modulator in earlier discussions. In general, there are several different types of control laws that are used in different switching regulator control, e.g. constant ON time control, constant volt-sec control, constant OFF time control and constant frequency control. Among these control schemes, only the last two are applicable to current-injected control. Since constant ON time and constant volt-sec both designate a constant ON period in the switching cycle; the former designates a constant ON time regardless of converter input voltage and the latter designates a constant ON time for a given converter input voltage with $V_I T_{ON}$ being kept constant. Under such control law, both the initiation and termination of ON period have to be generated by a clock signal, then the ascending switching current signal can be terminated before or after it intersects the threshold voltage. This means the peak amplitude of inductor current or switch current can no longer be kept constant, which is in contradiction to the current-injected (or current programmable) control principle.

Employing constant OFF time and constant frequency control, the peak inductor current or switch current can be limited during each switching cycle by adjusting the on-time interval.

In this chapter we will investigate the types of external ramp and its

magnitude in order to resolve the 50% instability problem,

The criteria we used to evaluate duty cycle control schemes and determine an optimal external ramp for constant frequency control for duty cycle range greater than 50% is as follows

- range of regulator performance variation with respect to input voltage change,
- open-loop gain bandwidth and phase margin,
- easiness of implementation

6.1 Constant T_{OFF} Duty Cycle Control

Eq. (2.48) shows the transfer function of pulse modulator under constant OFF time control:

$$F_M = \frac{2}{T_F} \cdot \frac{1}{S_N + S_F} \tag{6.1}$$

where $$S_N = V_I \frac{R_{p2}}{nL_p} = V_o \frac{D'N_p}{DN_s} \cdot \frac{R_{p2}}{nL_p} \tag{6.2}$$

$$S_F = V_I \frac{T_{ON}}{T_{OFF}} \cdot \frac{R_{p2}}{nL_p} = V_o \frac{N_p}{N_S} \cdot \frac{R_{p2}}{nL_p} \tag{6.3}$$

It is shown in (6.1) that F_M always remain positive,and there is no duty-cycle related instability problem.

As we stated in Chapter V, the converter using lag compensation will be based on for further analysis. The characteristic equation is:

$$G_T = F_M \cdot \omega_o^2 \cdot \frac{V_o}{DD'R_1C_2} \cdot \frac{(S/S_{01} + 1)(S/S_{02} + 1)(S/S_{03} + 1)}{S(S^2 + 2\zeta\omega_o S + \omega_o^2)} \tag{6.4}$$

Substitute eq.s (6.1), (6.2), (6.3) into (6.4), we have:

$$G_T = M \cdot \frac{2}{T_F} D' \cdot \frac{(S/S_{01} + 1)(S/S_{02} + 1)(S/S_{03} + 1)}{S(S^2 + 2\zeta\omega_o S + \omega_o^2)} \tag{6.5}$$

where $$M = \frac{N_p}{N_S} \cdot \frac{n}{R_{p2}} \cdot \frac{1}{R_1C_2C}$$

and D' is a function of input voltage:

$$D = \frac{V_O N_P}{V_O N_P + V_I N_S}$$

$$D' = 1 - D$$

When V_I increases it will cause:

- D to decrease, D' to increase,
- ω_o to increase, since

$$\omega_o = \frac{(D')^2}{L_S C}$$

Figure 6.1 (a), (b) show the open-loop gain and phase affected by changes of input voltage from 10^V to 50^V. The lower the input voltageis the higher the gain-bandwidth will be. The phase margin improves asgain increases.

It is also indicated from eq. (6.5) that one can increase the open-loop gain by reducing T_F and thus reducing the period of one switching cycle. This aspect is quite different from the conventional single loop control of which the duty cycle gain is independent of the switching fre quency.

6.2 Constant T_p Without Ramp

Eq. (2.43) shows the transfer function of the pulse modulator under constant frequency without ramp control law:

$$F_M = \frac{2}{T_p} \cdot \frac{1}{S_N - S_F} = \frac{2nL_p}{T_p V_I R_{p2}} \cdot \frac{D'}{D' - D} \tag{6.6}$$

F_M can be negative for $S_N < S_F$ or $D > D'$ and produces a positivefeedback that causes the system to be unstable [1].

Substitute eq.s (6.6), (6.2) and (6.3) into eq. (6.4), we have:

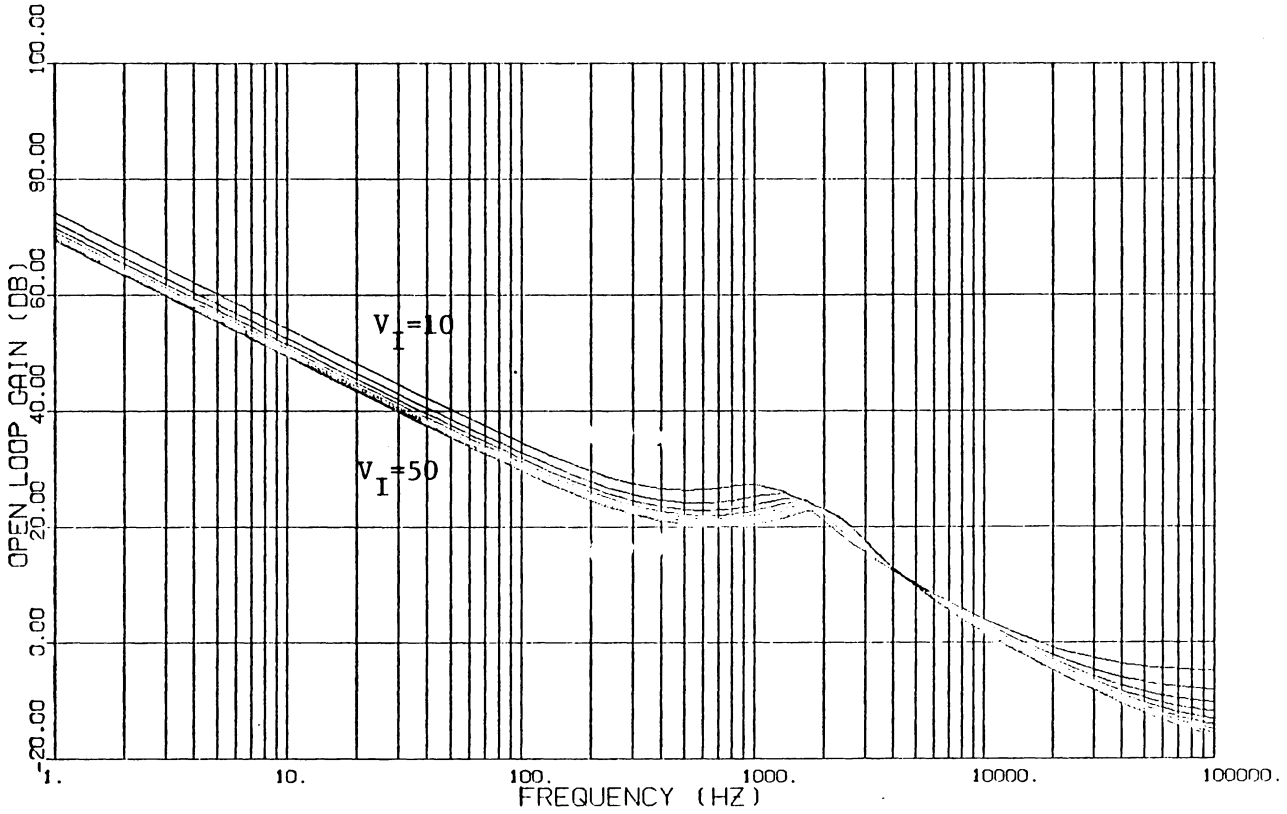


Fig. 6.1 (a) Open-Loop Gain Using Constant T_{OFF} Control

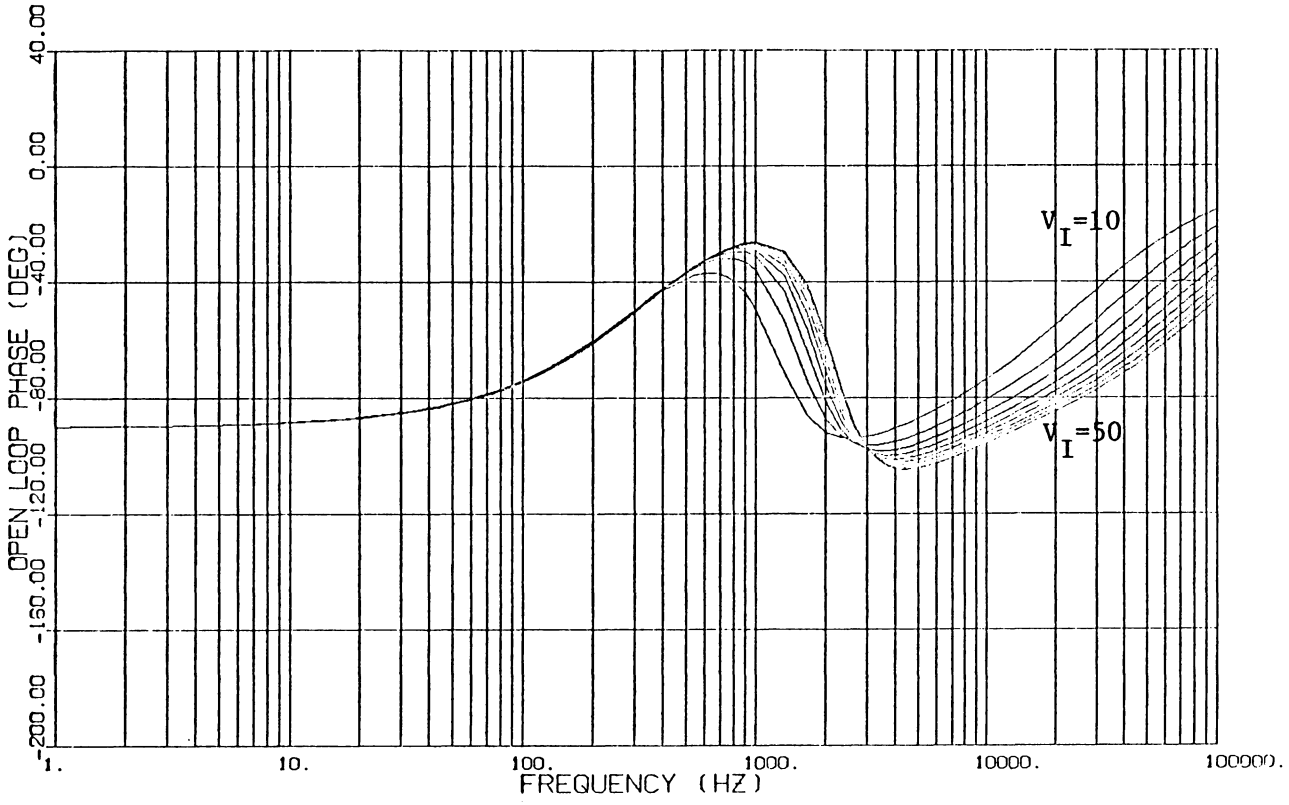


Fig. 6.1 (b) Open-Loop Phase Using Constant T_{OFF} Control

$$G_T = M \cdot \frac{2}{T_p} \cdot \frac{D'}{D' - D} \cdot \frac{(S/S_{o1} + 1)(S/S_{o2} + 1)(S/S_{o3} + 1)}{S(S^2 + 2\zeta\omega_o S + \omega_o^2)} \tag{6.7}$$

For positive F_M, D has to be less than 0.5, or V_I has to be larger than 11.44V. Fig. 6.2 (a), (b) illustrates the open-loop gain and phase as a function of input voltage. As V_I is reduced to less than 11.44V the phase becomes positive which implies an unstable operation.

6.3 Constant T_p With Ramp

A remedy for the 50% duty cycle instability is to add an external ramp to the sensed switch current waveform as shown in Fig. 6.3. After adding S_E, the transfer function now becomes (eq. (2.45)):

$$F_M = \frac{2}{T_p} \cdot \frac{1}{2S_E + S_N - S_F} \tag{6.8}$$

F_M can still be negative at a duty cycle higher than 50% if the additional S_E is not large enough. To guarantee a positive F_M.

$$2S_E + S_N - S_F > 0 \tag{6.9}$$

$$S_E > \tfrac{1}{2}(S_F - S_N)$$

$$= \frac{V_o N_p R_{p2}}{2N_S nL_p}\left(1 - \frac{D'_{min}}{D_{max}}\right) \tag{6.10}$$

D_{max} is the maximum prescribed duty cycle ratio.

$D'_{min} = 1 - D_{max}$

Substitute eq.s (6.9), (6.2) and (6.3) into eq. (6.4), we have:

$$G_T = M \cdot \frac{2}{T_P} \cdot \frac{V_o D'}{V_o(D' - D) + 2S_E \frac{nL_P}{R_{P2}} \frac{N_S}{N_P} D} \cdot \frac{(S/S_{01} + 1)(S/S_{02} + 1)(S/S_{03} + 1)}{S(S^2 + 2\zeta\omega_o S + \omega_o^2)} \tag{6.11}$$

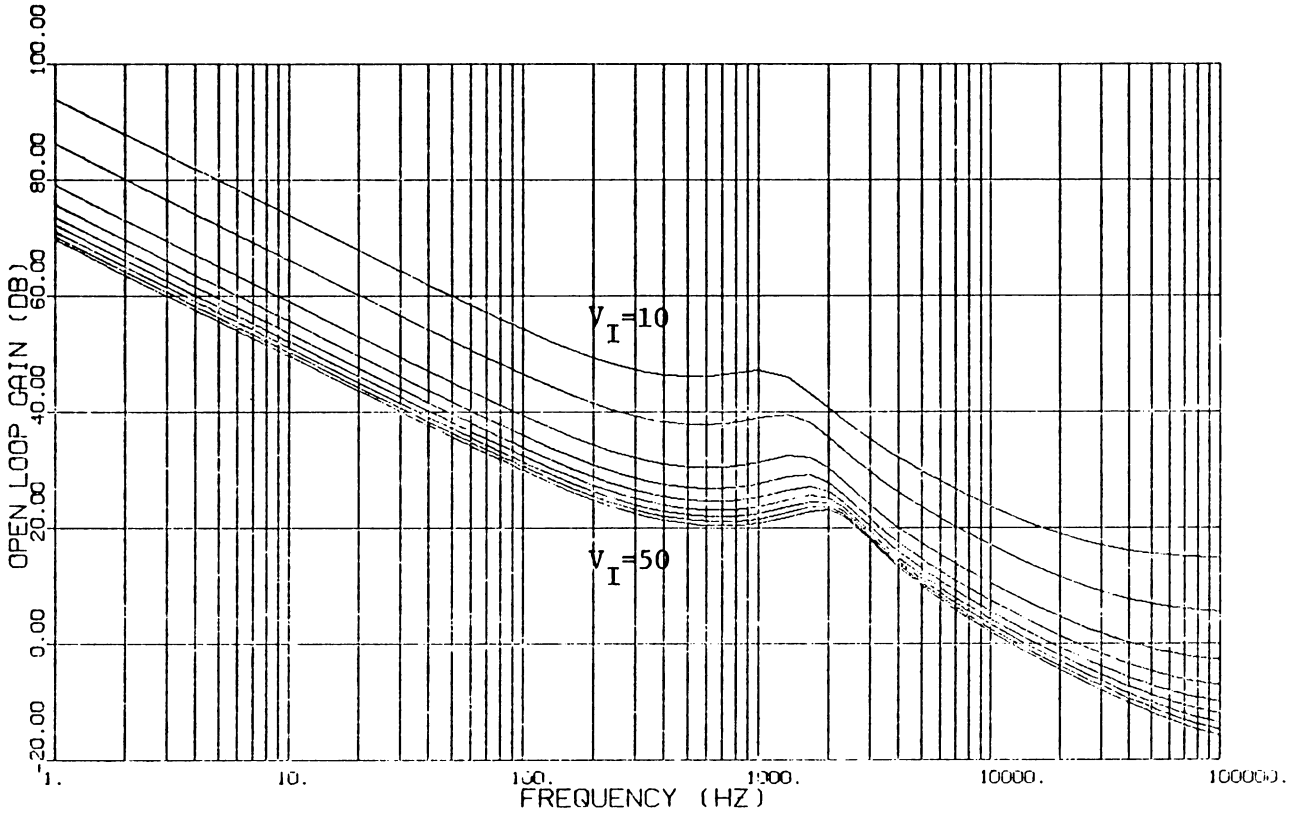


Fig. 6.2 (a) Open-Loop Gain Using Constant Frequency Without Ramp Control

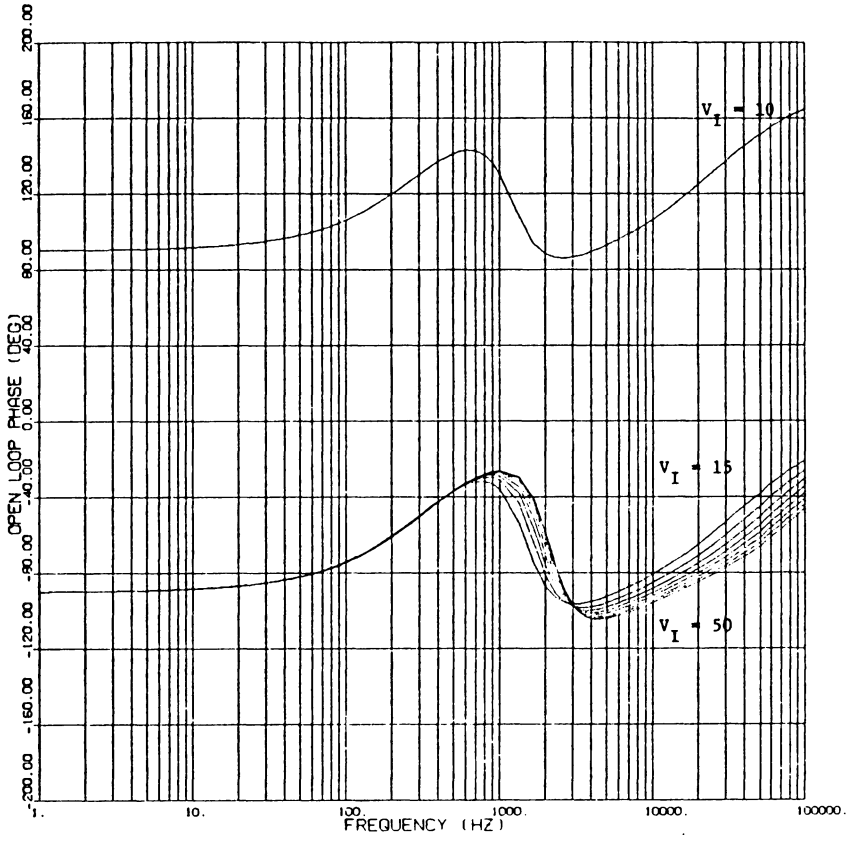


FIG. 6.2(b) OPEN-LOOP PHASE USING CONSTANT FREQUENCY WITHOUT RAMP CONTROL SHOWING THE INSTABILITY PROBLEM

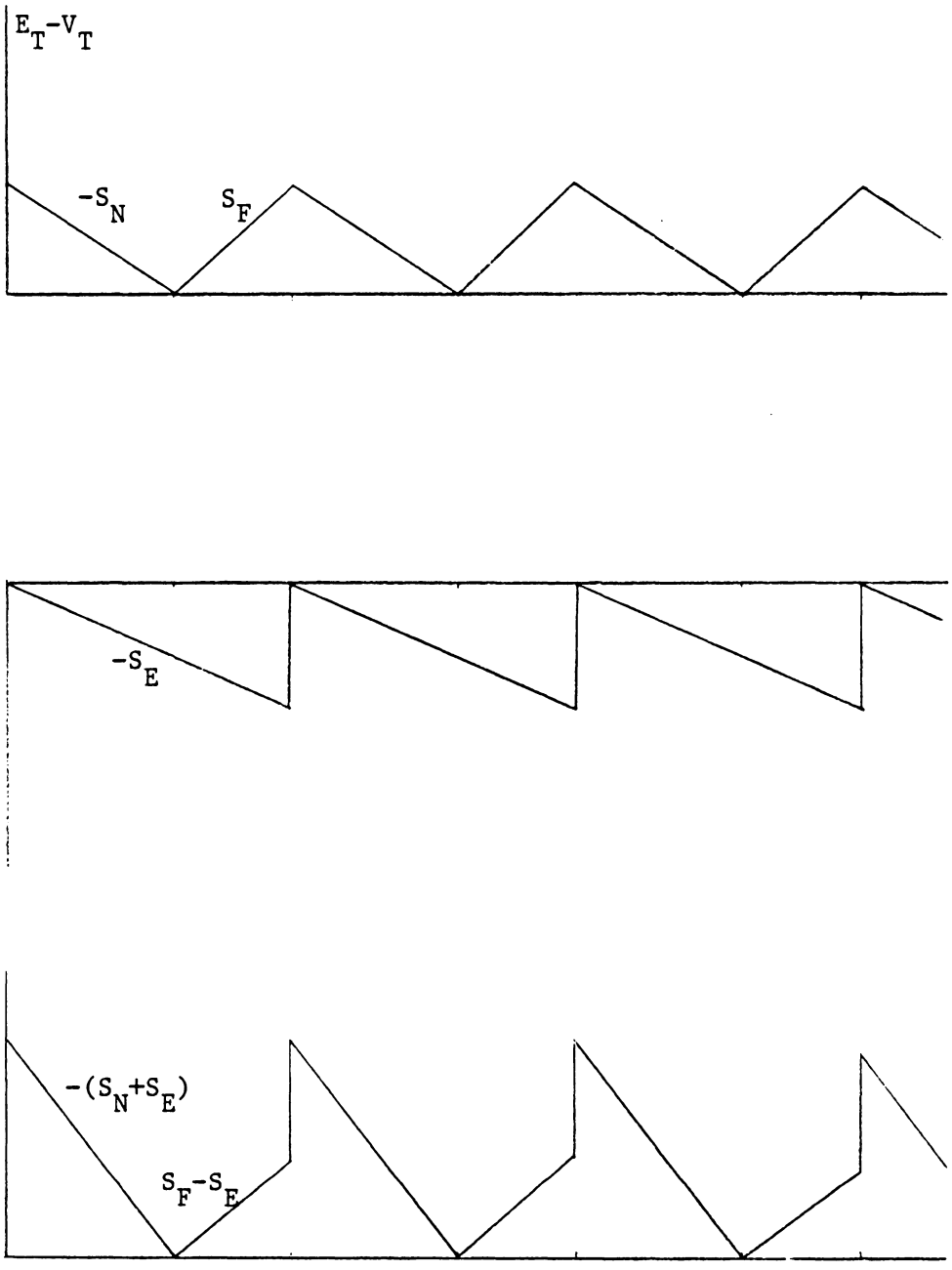


Fig. 6.3 Adding An External Ramp To Eliminate The Duty Cycle Instability

To extend the duty cycle range up to its theoretical limit 100%, one let $S_E = \frac{1}{2}S_F$. Under this condition, eq. (6.8) becomes:

$$F_M = \frac{2}{T_p} \cdot \frac{1}{S_N}$$

Figure 6.4 (a) and (b) illustrate the gain and phase plots.

6.4 Optimizing the Ramp Slope

While an artificial external ramp will eliminate the potential instability when using the constant frequency control law the ramp slope that can stablize the system as well as give a better performance is what we seek for.

As discussed in [5], when this slope is equal to the OFF-time slope, the duty cycle range can be extended to 100%. In addition, a one-cycle response can be obtained to reach a new steady state when the system is subjected to a step input transient This is illustrated in Figure 6.5 when $S_E = S_F$ eq. (6.8) becomes:

$$F_M = \frac{2}{T_p} \cdot \frac{1}{S_N + S_F} \quad \text{with } S_E = S_F \tag{6.12}$$

and an error signal, illustrated by dotted line, will not propagate after on switching cycle. Open-loop characteristics by letting S_E equal to S_F are shown in Figure 6.6 (a), (b). Although the instability problem is solved, the open-loop gain suffers a substantial set back. Consequently, this degreades the audiosusceptibility and output impedance as well as transient response of the regulator. In fact, eq. (6.12) is exactly the expression for constant OFF-time control law except T_F in eq. (6.1) is substituted by T_p in eq. (6.12), we can see the resemblance of these two controls by comparing Figure 6.1 (a) and Figure 6.6 (a).

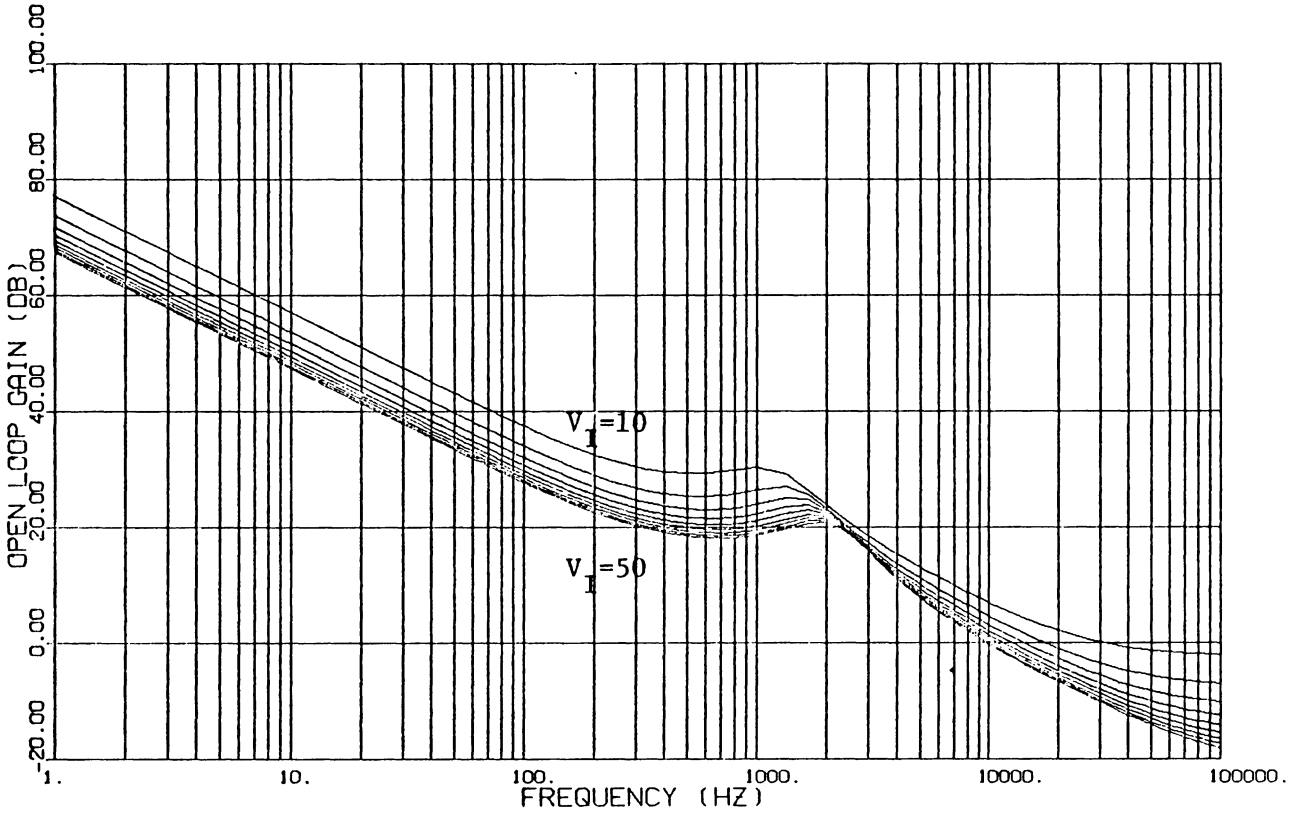


Fig. 6.4 (a) Open-Loop Gain Using Constant Frequency With Ramp $S_E=S_{F/2}$

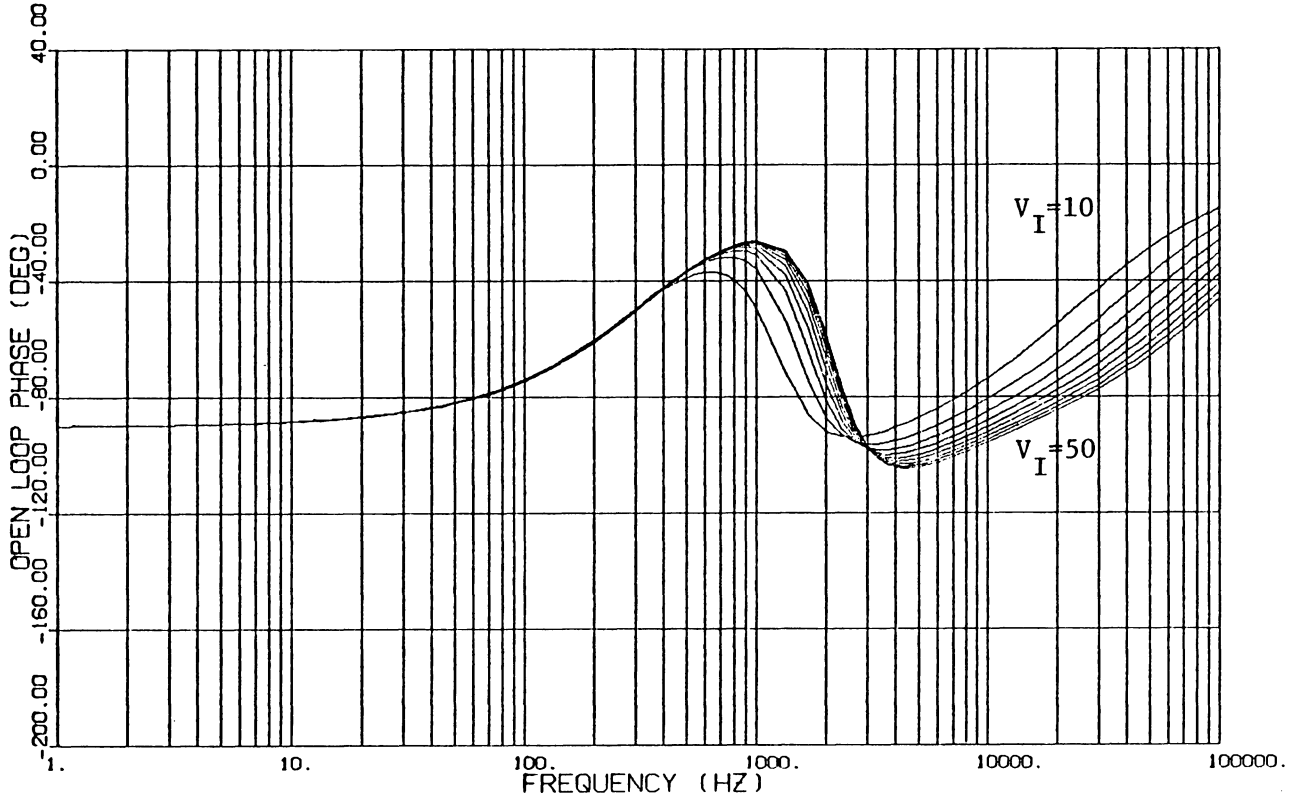


Fig. 6.4 (b) Open-Loop Phase Using Constant Frequency With Ramp $S_E=S_{F/2}$

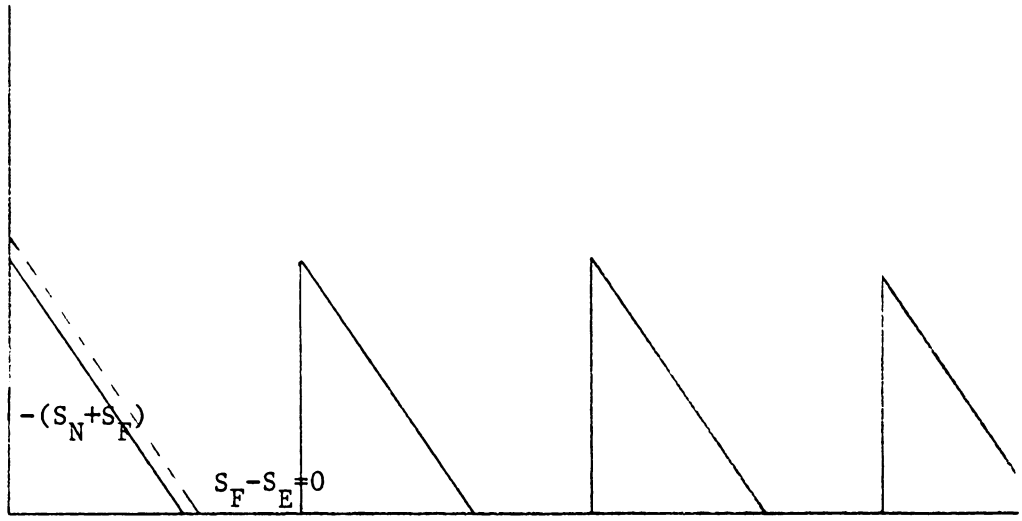


Fig. 6.5 With An External Ramp $S_E=S_F$ To Eliminate Disturbance Within One Cycle

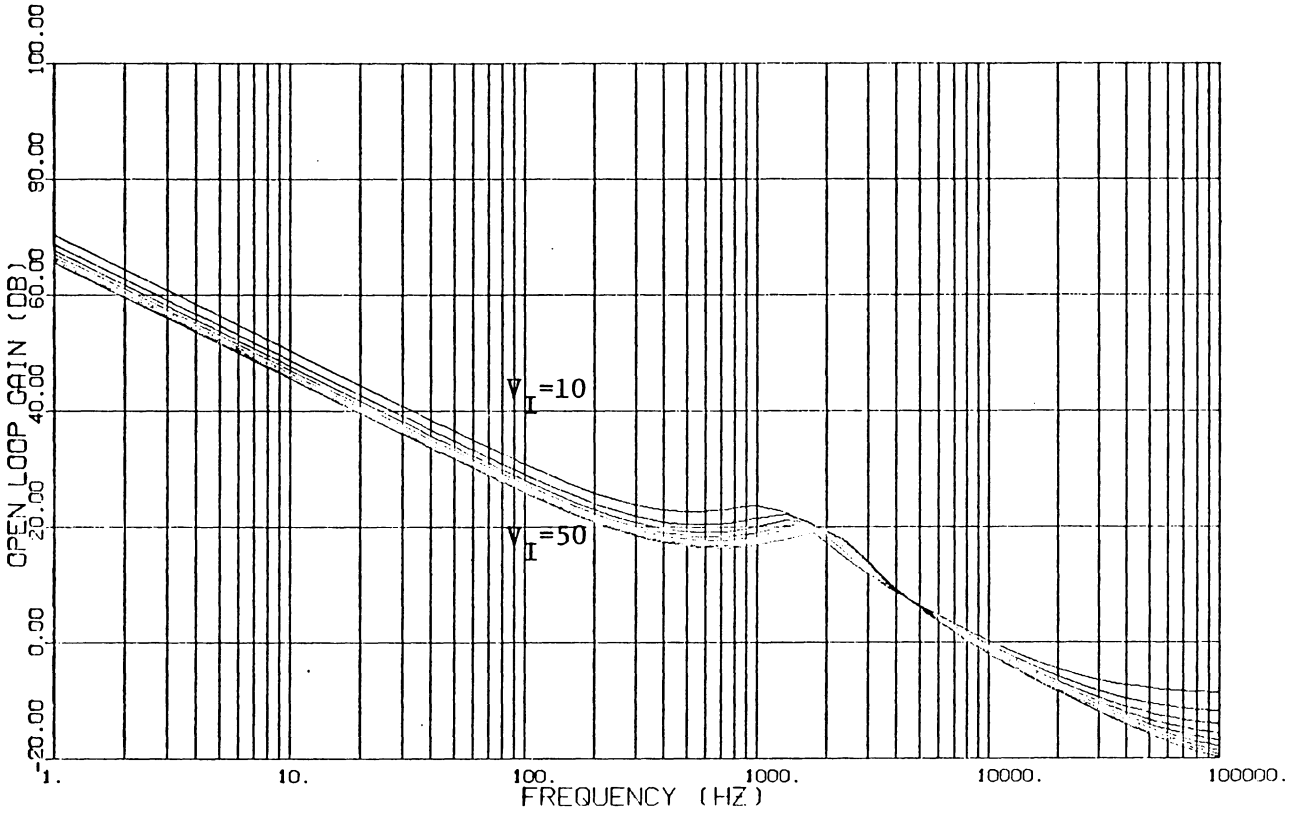


Fig. 6.6 (a) Open-Loop Gain Using Constant Frequency With Ramp $S_E=S_F$

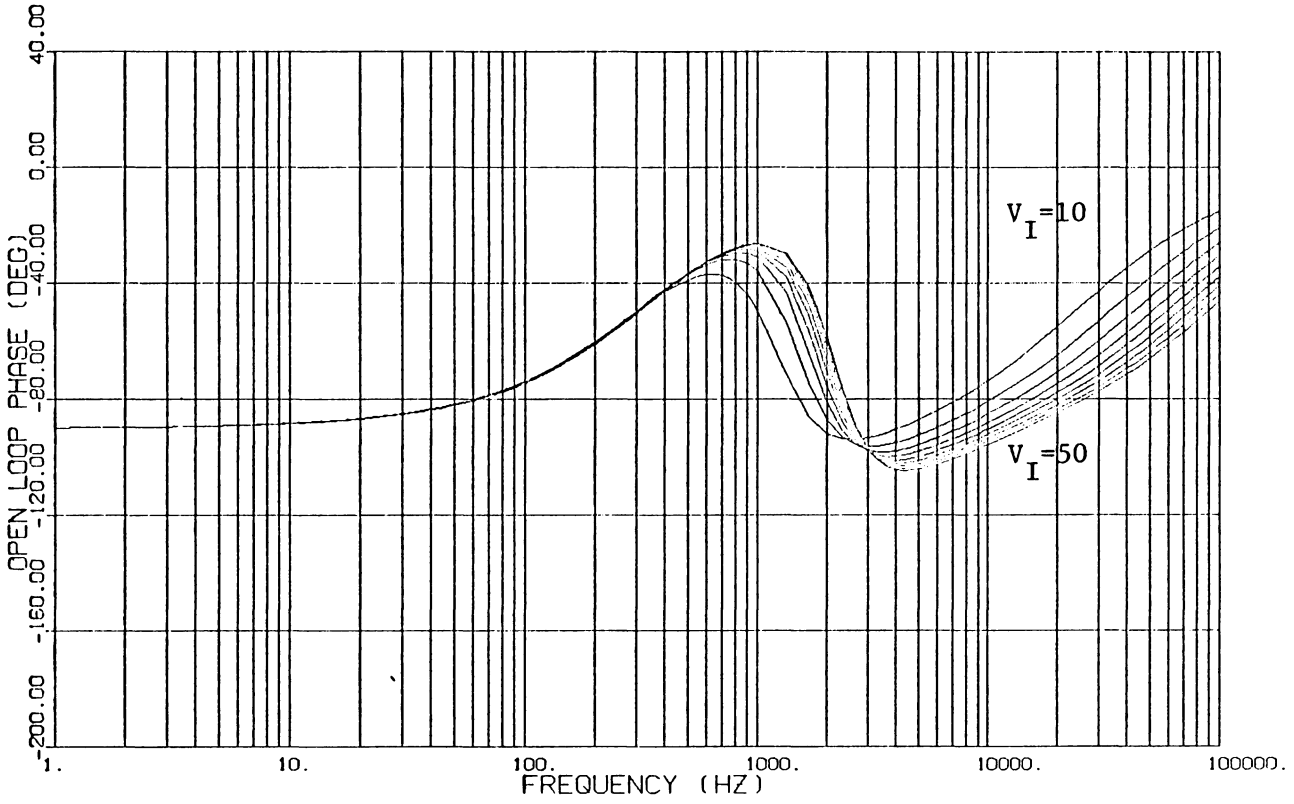


Fig. 6.6 (b) Open-Loop Phase Using Constant Frequency With Ramp S_E=S_F

Further examining eq.s (6.2), (6.3) (6.8), it reveals that S_F is a constant and

$S_N > S_F$ for $D < D'$

$S_N < S_F$ for $D > D'$

The external ramp S_E is needed only when $D > D'$, while it is to extend the duty cycle range. Adding a fixed external ramp, however, lowers the overall loop gain of the system and thus over compensates the system in the lower duty cycle operating range while no external ramp is needed.

According to the above argument, it is desirable to design an external ramp such that

$$S_E = K\ (11.44 - V_I)$$

where 11.44V is the input voltage value at which the duty cycle is 0.5. Using the above expression for S_E is positive when $D > D'$ to help stabil izing the system and is negative when $D < D'$ to boost the F_M gain. There is one problem with this implementation, as V_I equals to 11.44V, F_M will be infinite. To resolve this difficulty, one can choose a somewhat larger bias voltage. Concerning the selection of K, it must be such that F_M is positive. The following example illustrates the effects of such an external ramp and the selection of K.

When input voltage changes, the value of $S_N - S_F$ will change. For each operating input voltage there is a minimum or maximum value for K that will guarantee a positive F_M.

$$K > K_{min} \triangleq \frac{1}{2(V_B - V_{Imin})} \frac{R_{p2}}{nL_p} \left(V_o \frac{N_p}{N_S} - V_{Imin}\right) \tag{6.13}$$

$$K < K_{max} \triangleq \frac{1}{2(V_B - V_{Imax})} \quad \frac{R_{p2}}{nL_p} \quad (V_o \frac{N_p}{N_S} - V_{Imax}) \qquad (6.14)$$

where $V_{Imin} < V_B < V_{Imax}$.

For input voltage range from 10^V to 50^V and a bias voltage $V_B = 15^V$, the range of K can be determined from Table 6.1

$$6.432 \times 10^2 < K < 2.46 \times 10^3$$

Letting K to be 2.15×10^3 and a bias voltage of 15V, Figure 6.7 (a), (b) shows the open-loop gain and phase using the above discussed ramp. By comparing Figure 6.7 to Figure 6.6 we can see the loop gain is improved under stable operating condition and almost remains unchanged as input voltage varies.

The optimization of the ramp slope can be illustrated by the F_M vs. duty ratio diagram. Figure 6.8 shows the absolute value of F_M (w/o external ramp) operated at different duty ratio. A horizontal line in figure means the F_M gain is unchanged for all duty ratio.

Figure 6.8 shows a drastically change in F_M gain when duty ratio approaches 0.5. Figure 6.9 shows the F_M gain using eq. (6.13) with $V_b = 15$ and a set of K values. Comparing with Figure 6.8, the additional external ramp eliminate the duty cycle instability with a more unified and also higher gain within a wide range of duty ratio variation. Figure 6.10 (a), (b) show the DC gain of the system open loop under different bias voltage and K values. The DC gain can be expressed as:

$$G_{DC}\Big|_{\omega \to o} \simeq F_M \cdot \frac{V_o}{DD'} \qquad (6.14)$$

Figure 6.10 (a) is the DC gain with a bias voltage of 15^V and K ranges 2000 to 2250. Figure 6.10 (b) has a bias voltage of 17^V and K ranges

Table 6.1

VI	SN-SF	K
0.0	-51098.6875	K>0.1703290E+04
5.00	-28765.3477	K>0.1438267E+04
10.00	-6432.00000	K>0.6432000E+03
11.44	-0.00000	----------
15.00	15901.2500	ANY NUMBER
20.00	38234.5625	K<.3823456E+04
30.00	82901.2500	K<.2763375E+04
40.00	127568.000	K<.2551360E+04
50.00	172234.625	K<.2460495E+04

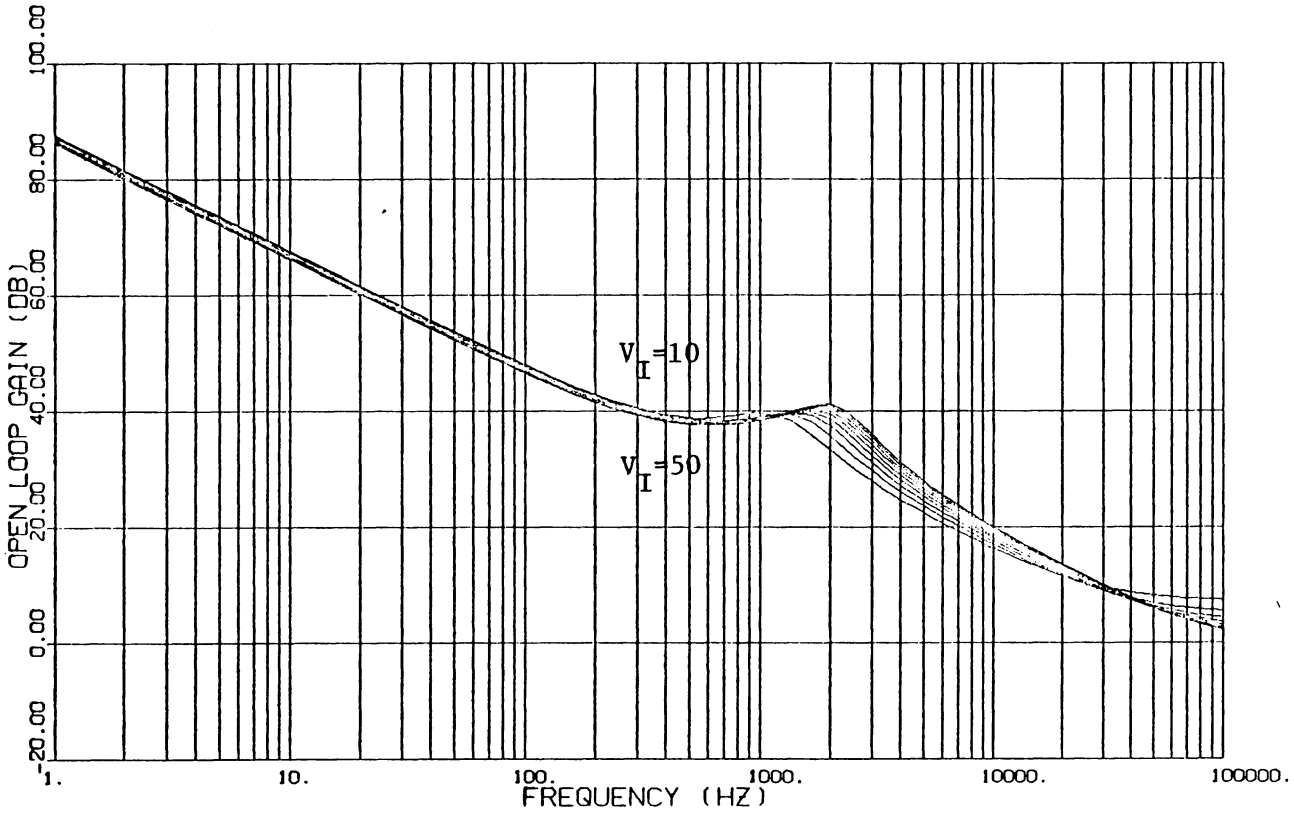


Fig. 6.7 (a) Open-Loop Gain Using Constant Frequency With Ramp $S_E=K\ (V_{bias}-V_I)$

$K=2.15 \times 10^3$, $V_{bias}=15$

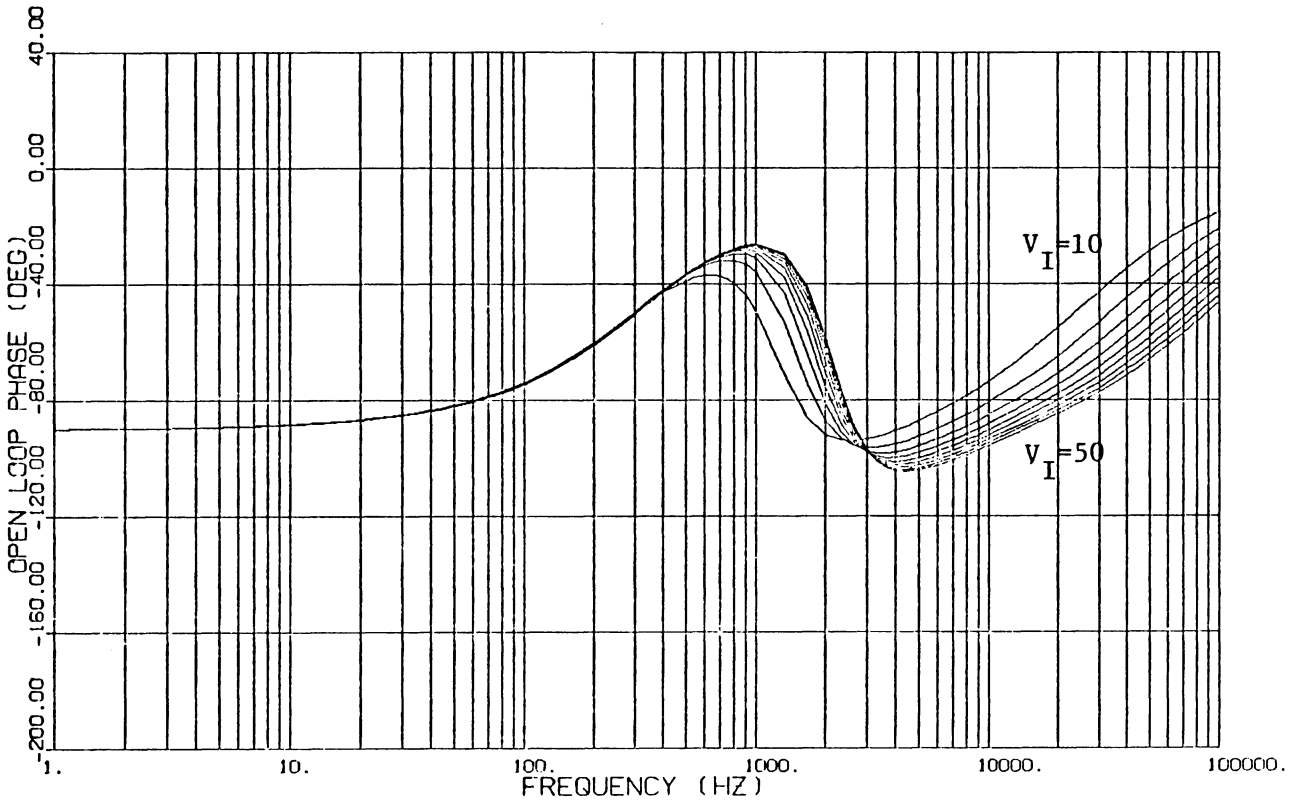


Fig. 6.7 (b) Open-Loop Phase Using Constant Frequency With Ramp $S_E=K\ (V_{bias}-V_I)$

$K=2.15 \times 10^3$, $V_{bias}=15$

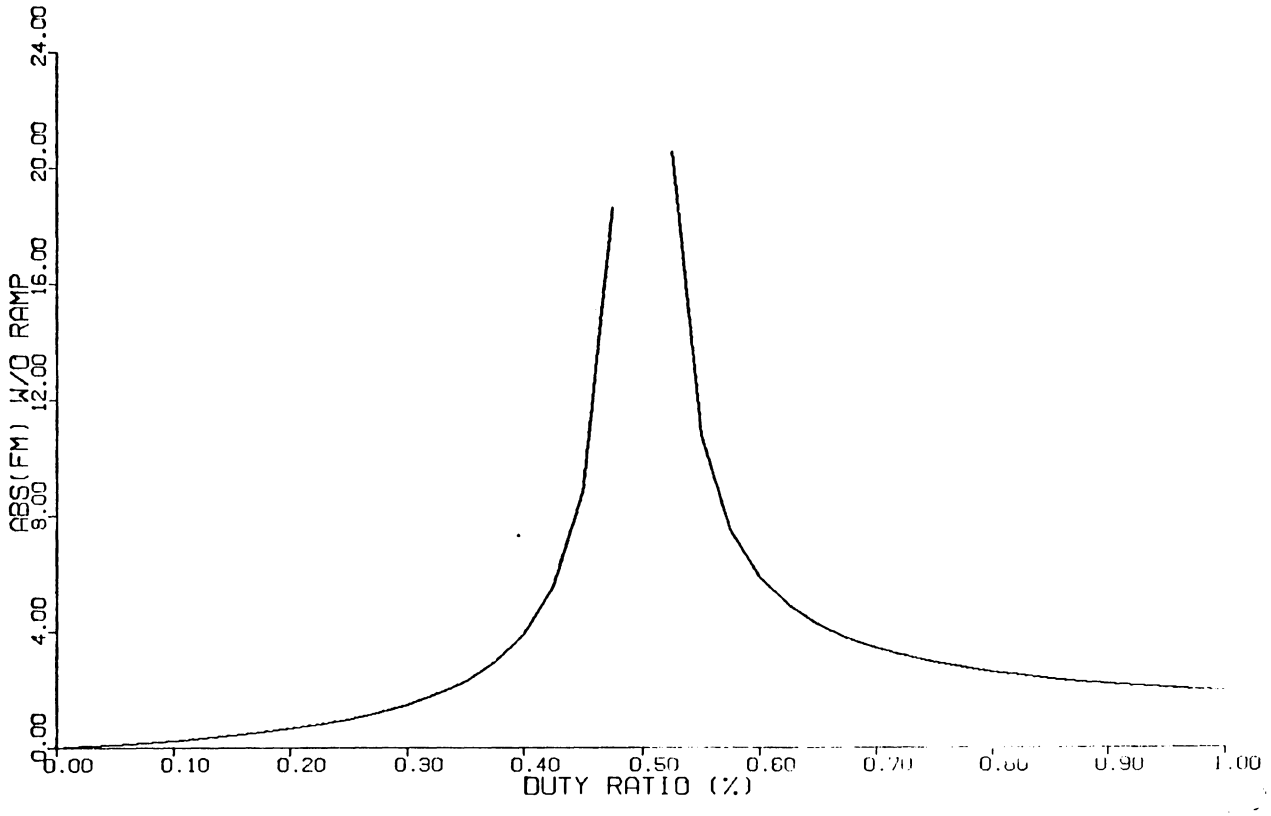


Fig. 6.8 F_M Gain VS. D Using Constant Frequency Without Ramp

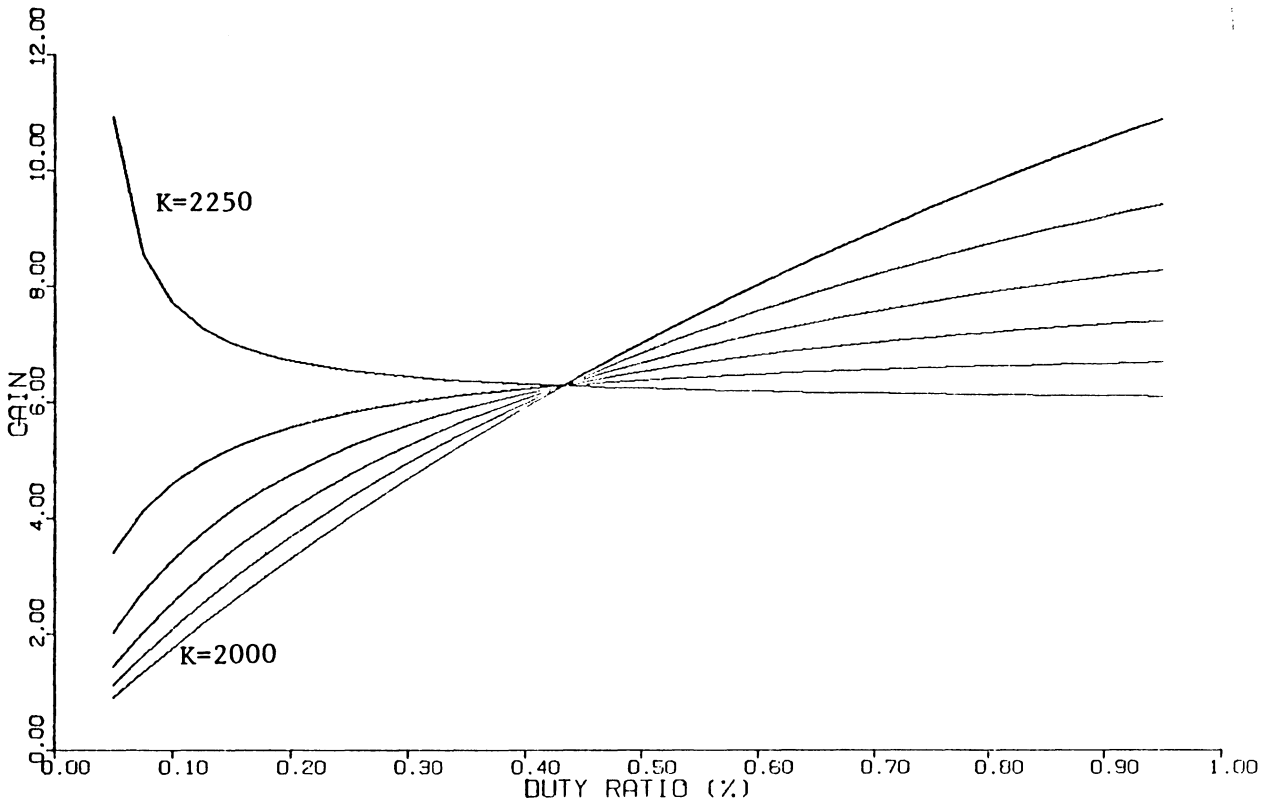


Fig. 6.9 F_M Gain VS. D Using Constant Frequency With Ramp $S_E=K(15-V_I)$

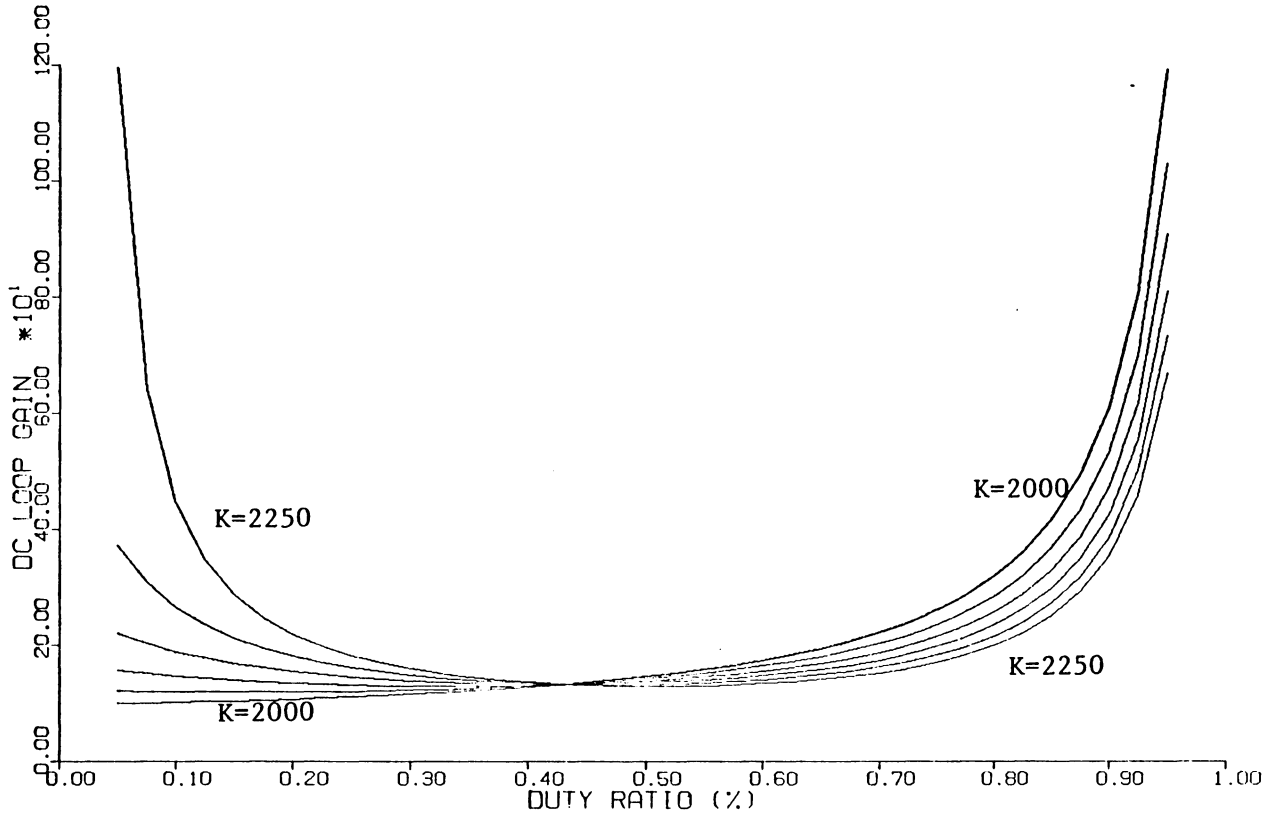


Fig. 6.10 (a) DC Loop Gain VS. D Using Constant Frequency With Ramp $S_E=K\ (15-V_I)$

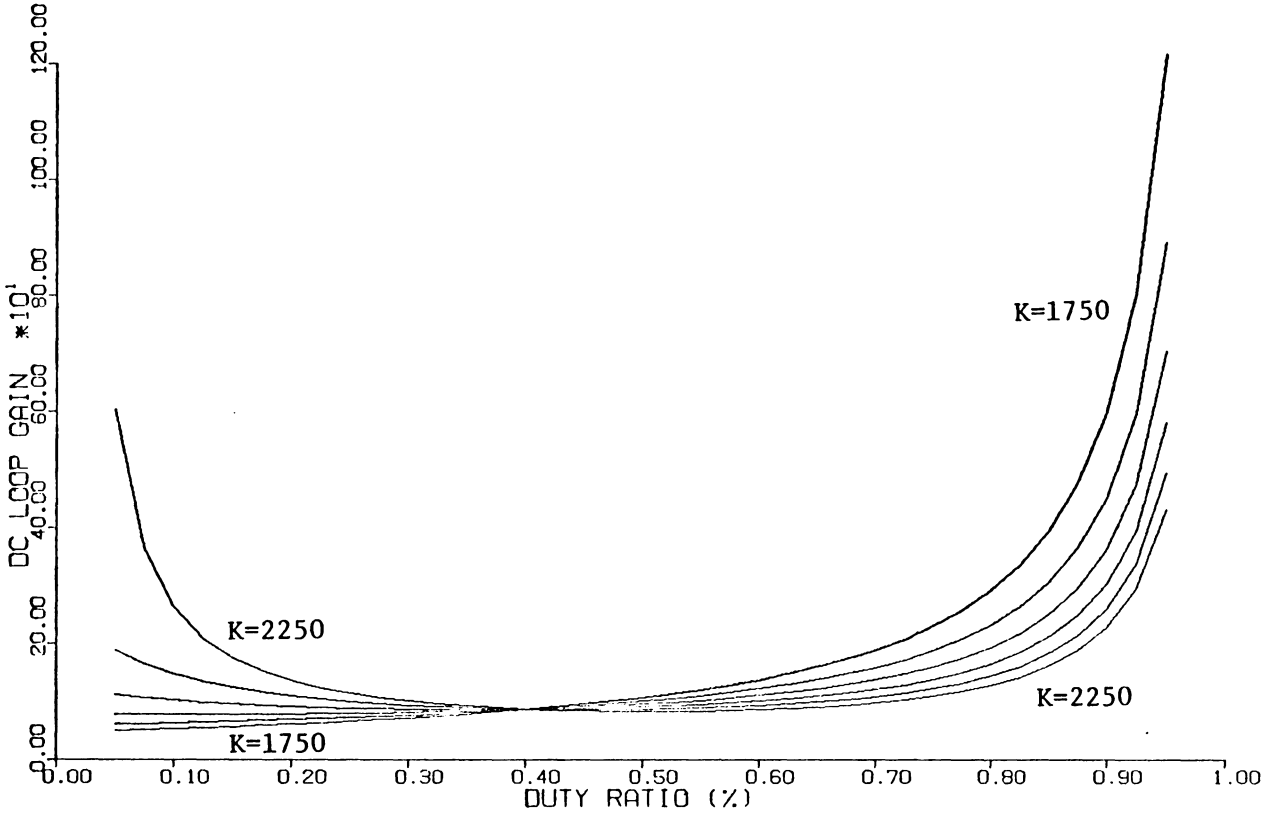


Fig. 6.10 (b) DC Loop Gain VS. D Using Constant Frequency With Ramp $S_E=K\ (17-V_I)$

1750 to 2250. Thus, a smaller bias voltage V_B produces a higher loop gain but with smaller range of K for stable operation.

To solve for the 50% duty cycle instability, it is commonly done by adding a sufficiently large constant external ramp. Although, it is easy to implement, it is not a very efficient method. The effects of adding such an external ramp is simply to extend the duty cycle operation range and it will lower the loop gain. Fig. 6.11 illustrates the DC gain for different slopes (K) of an external ramp. Fig. 6.11 tells us the larger the K is, the wider the duty cycle range for stable operation with the penalty of a lower loop gain. The overall loop gain by using the constant external ramp is much lower than the one using the proposed external ramp as can be seen by comparing Fig. 6.11 to Fig. 6.10.

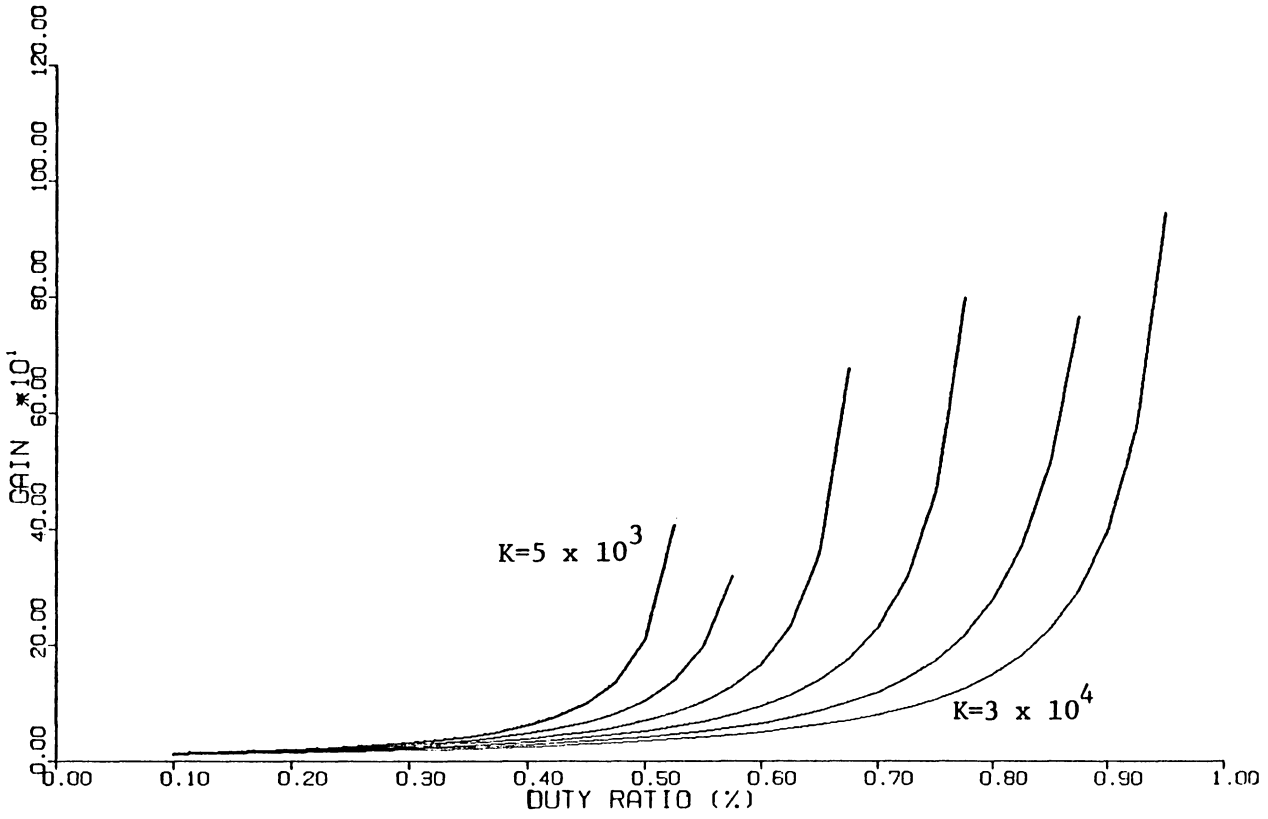


Fig. 6.11 DC Loop Gain VS. D Using Constant Frequency With Ramp S_E=K

Chapter VII

SOME DESIGN CONSIDERATIONS

From Chapter III to Chapter V, we have analyzed the current-injecte control employing gain compensation, lag compensation, and lead-lag compensation. The objective there is to understand how the control loop interacts with power stage and the effects of various control loop parameters on the system characteristics. From these analyses, we have pin pointed the key control loop parameters regarding to dc loop compensatio and the current injected loop.

It has also been shown that the three types of compensation share similar loop characteristics which confine the feedback control design to follow two basic design constraints governing the stability of the regulator. These limitations appear in all three cases. Consequently, compromises between loop gain and phase margin have to be carefully exercised in the control design.

Since no obvious benefit is observed using the lead-lag compensatio over that of the lag compensation scheme, the system employing lag compensation network is used as the basic control upon which some design guidelines are to be established.

7.1 Key Design Parameters

The following aspects are key to current-injected control design: the design constraints (4.12) and (4.13), the position of the open-loop zeros (4.4 - 4.6) and the loop-gain expressions in each frequency (4.7 - (4.11) range. These are the determinant factors when we compare two loop gains and phase margins.

As we discussed in Chapter IV, the two design constraints, eqs. (4.12) and (4.13), indicate the necessary conditions that must exist between DC loop gain and AC loop gain at high frequencies. If DC loop gain dominates AC loop gain at high frequencies a positive zero invariably will be present and the open-loop phase delay will approach -180°. This phenomenon is shown in Fig. 7.1 (a), (b). Figure 7.2 illustrates the DC loop gain, G_{DC}, and AC loop gain, G_{AC}, as F_{AC} varies. Where

$$G_{DC} = F_{D1} \cdot F_{DC}/\Delta$$

$$G_{AC} = F_{D2} \cdot F_{AC}/\Delta$$

When F_{AC} reduces to a value smaller than 0.0648, G_{AC} becomes smaller than G_{DC} at high frequency (Fig. 7.2(a)). Consequently, then system open-loop phase starts to drop at high frequency (Fig. 7.1 (b)) because the presence of a positive zero.

As discussed in the previous chapters, there exist three key control loop parameters namely F_{AC}, R_3/R_1, and C_2. F_{AC} comes from the AC loop, R_3/R_1 and C_2 come from the DC compensation loop. Since F_{AC} is related to F_M and the effect of F_{AC} was discussed in the previous chapte the design guidelines for dc loop parameters will be emphasized in the present chapter.

7.2 Selections of DC Compensation Network Parameters

From a design point of view, it is desirable to have independent adjustment of the positions of zeros such that an optimal loop gain shapping can be obtained. However, independent adjustment of open-loop

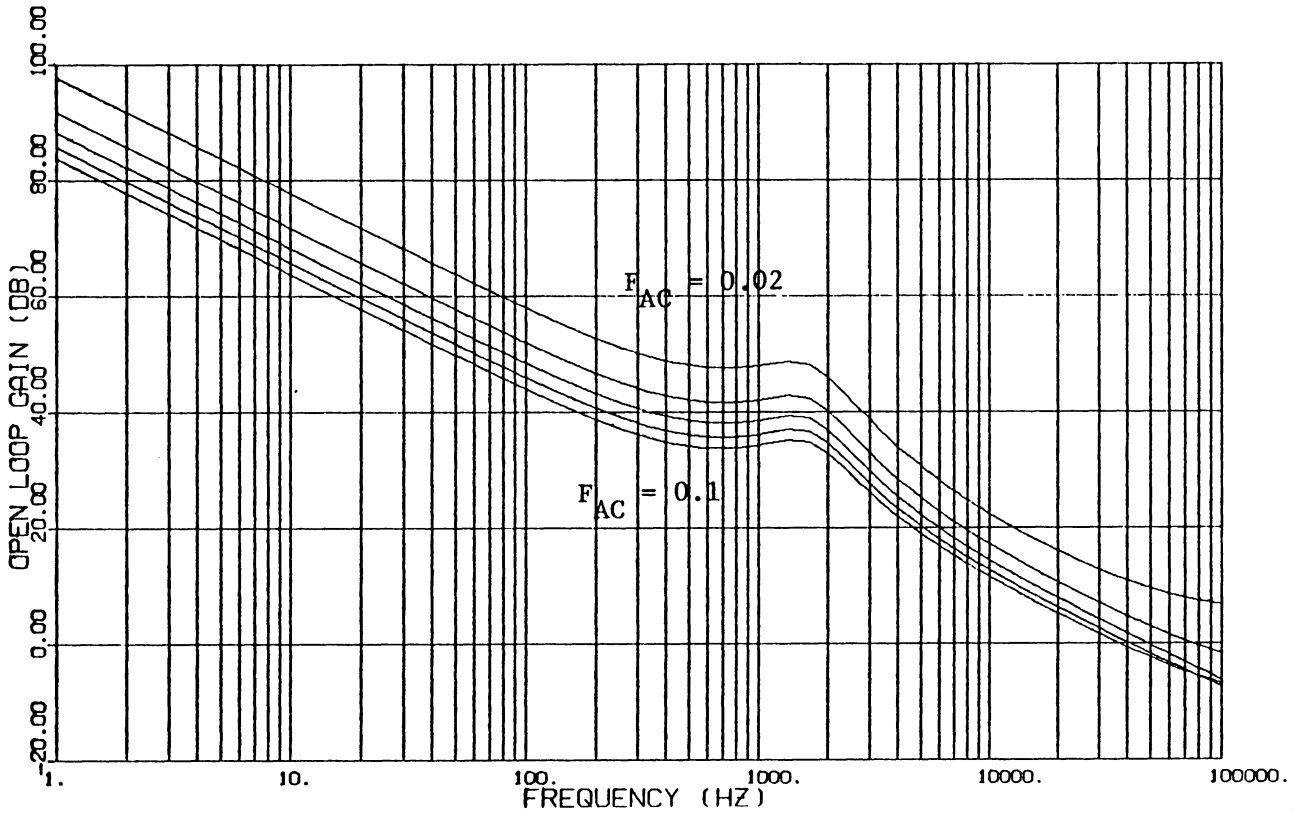


Fig. 7.1 (a) Open-Loop Gain by Changing F_{AC}

(F_{AC} = 0.02, 0.04, 0.06, 0.08, 0.1)

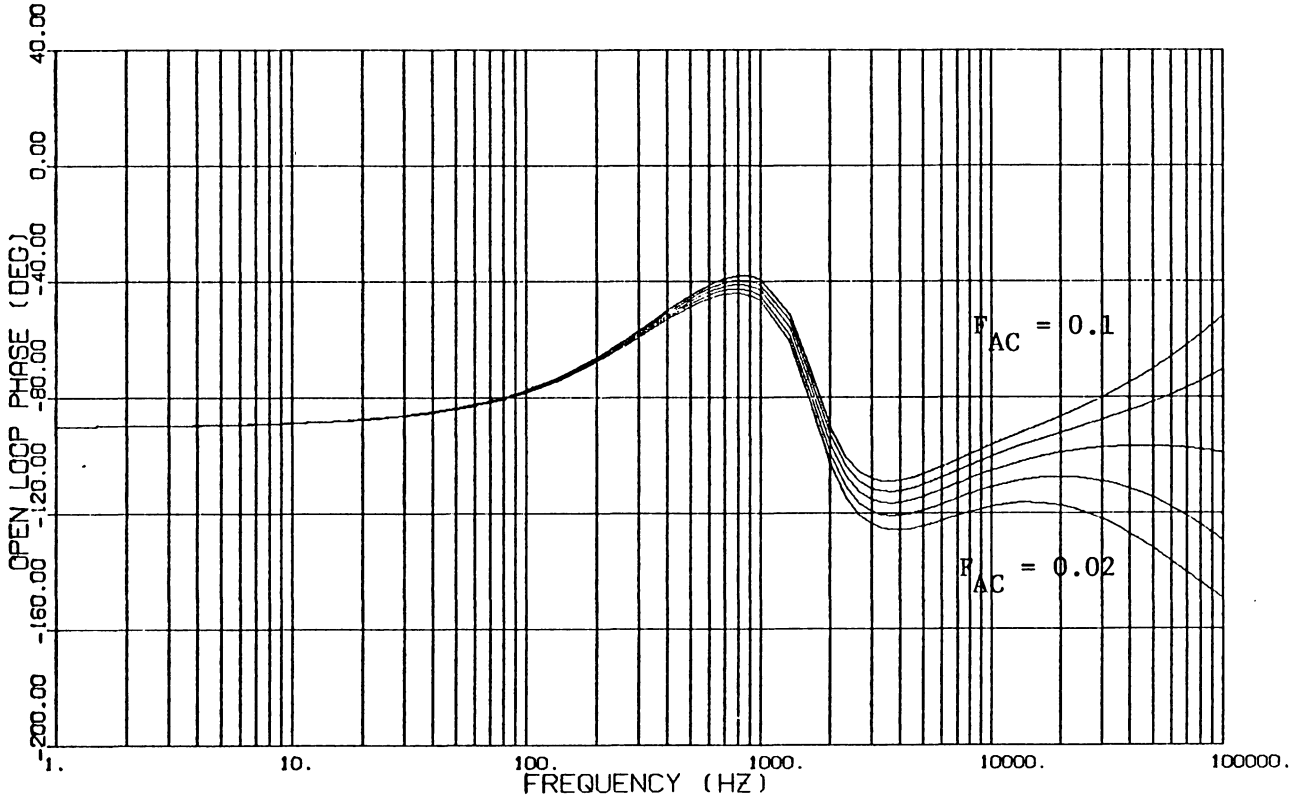


Fig. 7.1 (b) Open-Loop Phase by Changing F_{AC}

(F_{AC} = 0.02, 0.04, 0.06, 0.08, 0.1)

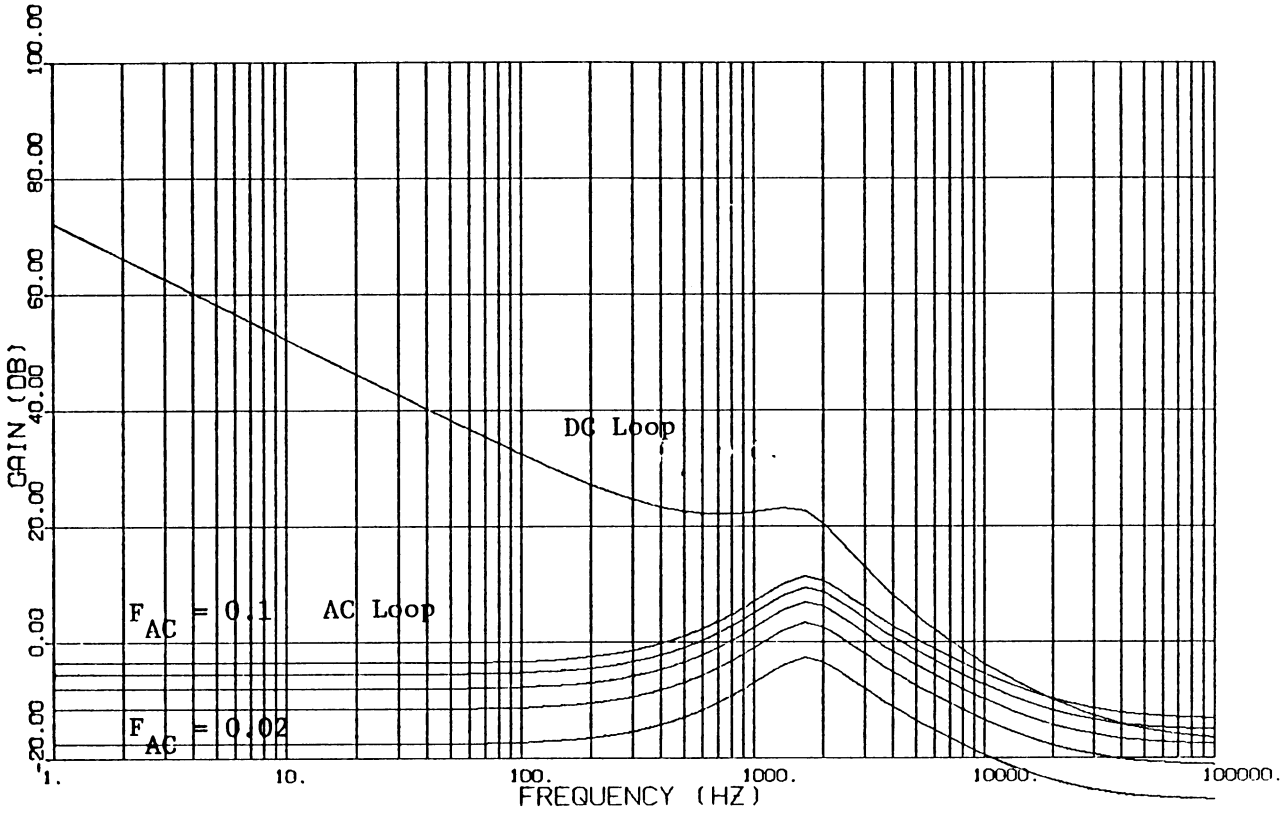


Fig. 7.2 (a) DC Loop and AC Loop Gain By Changing F_{AC} (F_{AC} = 0.02, 0.04, 0.06, 0.08, 0.1)

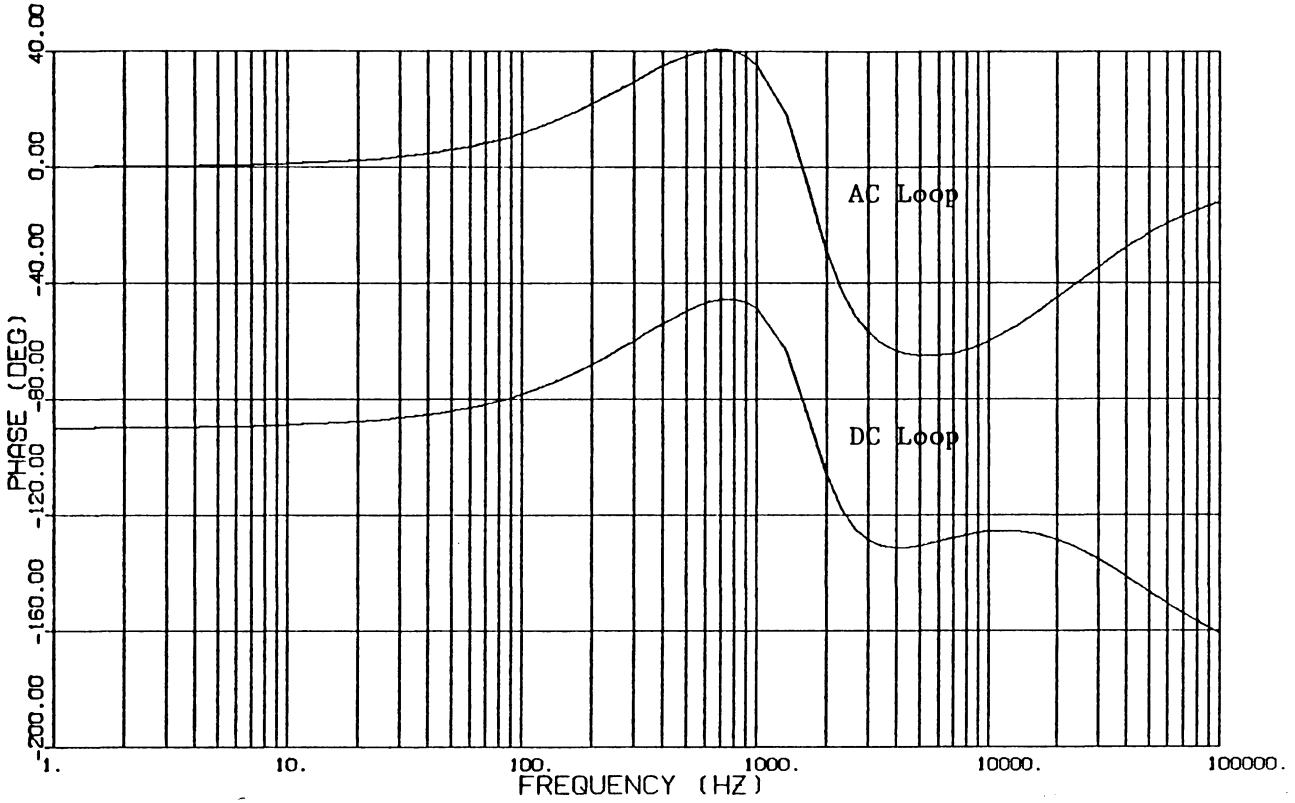


Fig. 7.2 (b) DC Loop and AC Loop Phase By Changing F_{AC} (F_{AC} = 0.02, 0.04, 0.06, 0.08, 0.1)

poles and zeros cannot be achieved. The control loop dependent poles and zeros are interrelated through the parameters R_3, R_1, and C_2.

If on increase the loop gain by adjusting these parameters the phase margin likely will be decreased. The selections of these parameters are basically design compromises between loop gain and phase margin.

One design parameter, C_2, appears in S_{o1} but not in S_{o2} and S_{o3}, therefore it can be used to adjust the position of S_{o1} which dominates the low frequency loop gain and settling time of the transient response [I]. Another design parameter R_3/R_1, determines the loop gain at frequencies between S_{o1} and ω_o. The loop gain is critical in this frequenc range, since the worst case audiosusceptibility and output impedance usually occur in this frequency range, and the peak amplitude of transient response is also determined by the loop gain in this frequency rang [3].

A simple design procedure is devised to assist the selection of control parameters.

1. First, select S_{o1} for transient settling time for design tradeoff.
2. Adjust R_3/R_1 and generate a family of open-loop curves. The range for R_3/R_1 has to be such that the design constraints, (4.12) and (4.13) are satisfied.
3. From these curves, select a value for R_3/R_1 such that within an acceptable range of phase margin the loop gain is highest.

Fig. 7.3 through Fig. 7.5 illustrate a series of open-loop characteristics with different value of S_{o1} and R_3/R_1. As we can see in

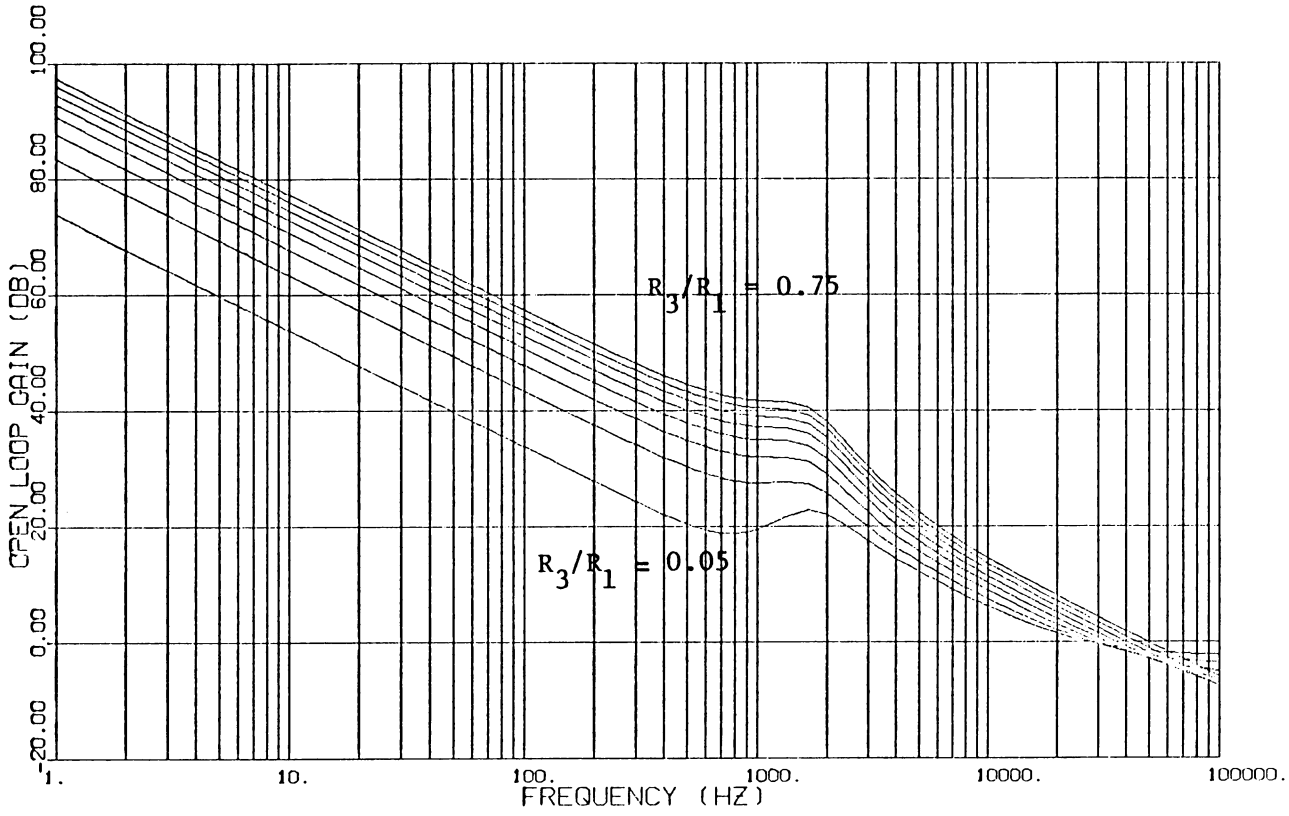


Fig. 7.3 (a) Open-Loop Gain with $S_{o1} = \frac{2}{3}\omega_o$, $R_{p2} = 30$

R_3/R_1 = 0.05, 0.15, 0.25, 0.35, 0.45, 0.55, 0.65, 0.75

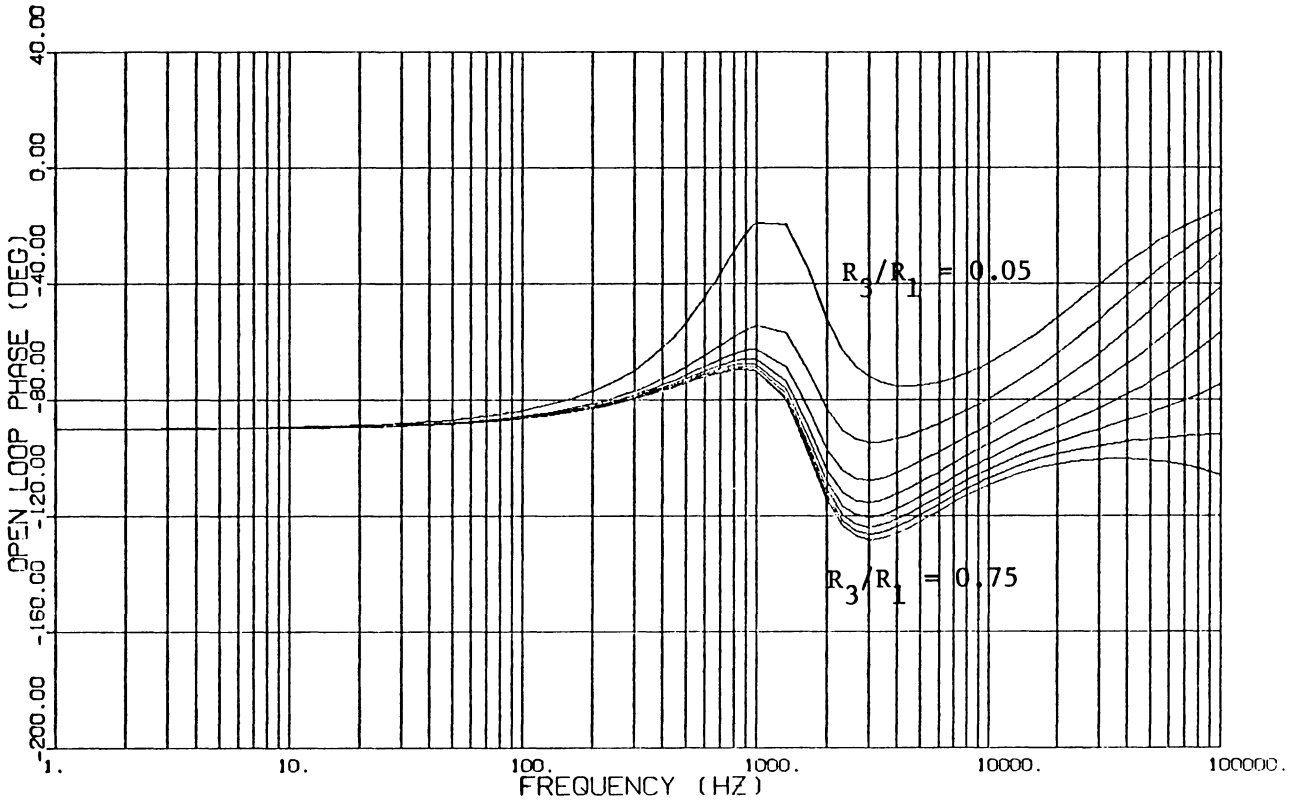


Fig. 7.3 (b) Open-Loop Phase with $S_{o1} = \frac{2}{3}\omega_o$, $R_{p2} = 30$

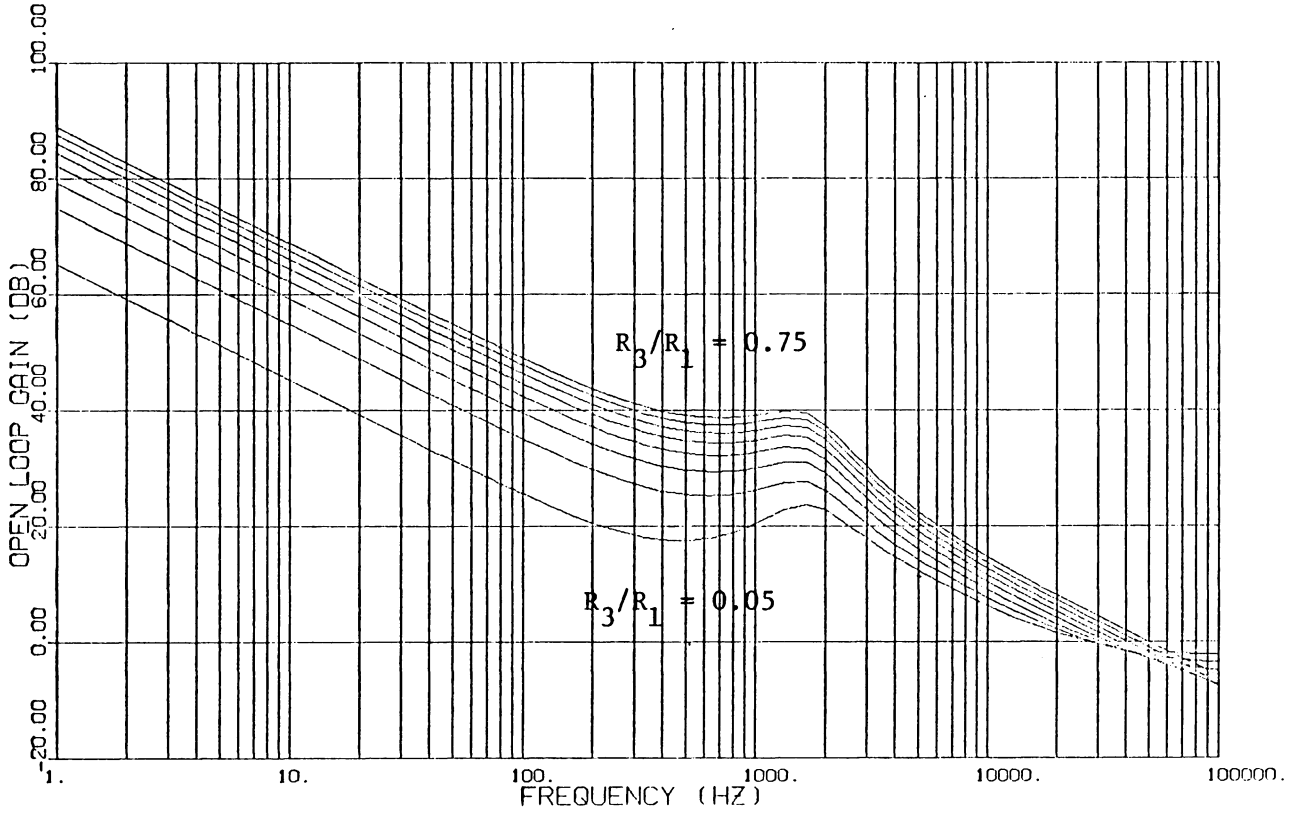


Fig. 7.4 (a) Open-Loop Gain with $S_{o1} = \frac{1}{4}\omega_o$, $R_{p2} = 30$

R_3/R_1 = 0.05, 0.15, 0.25, 0.35, 0.45, 0.55,

0.65, 0.75

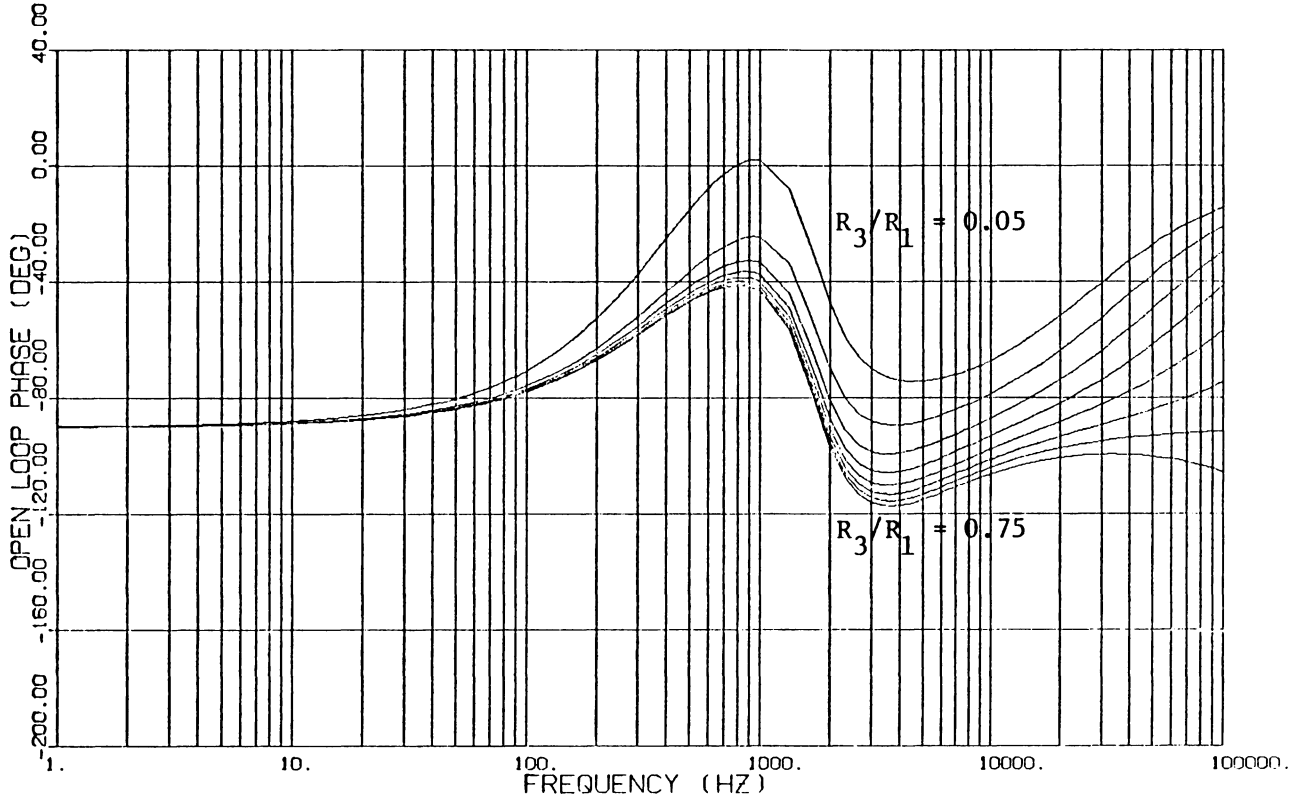


Fig. 7.4 (b) Open-Loop Phase with $S_{o1} = \frac{1}{4}\omega_o$, $R_{p2} = 30$

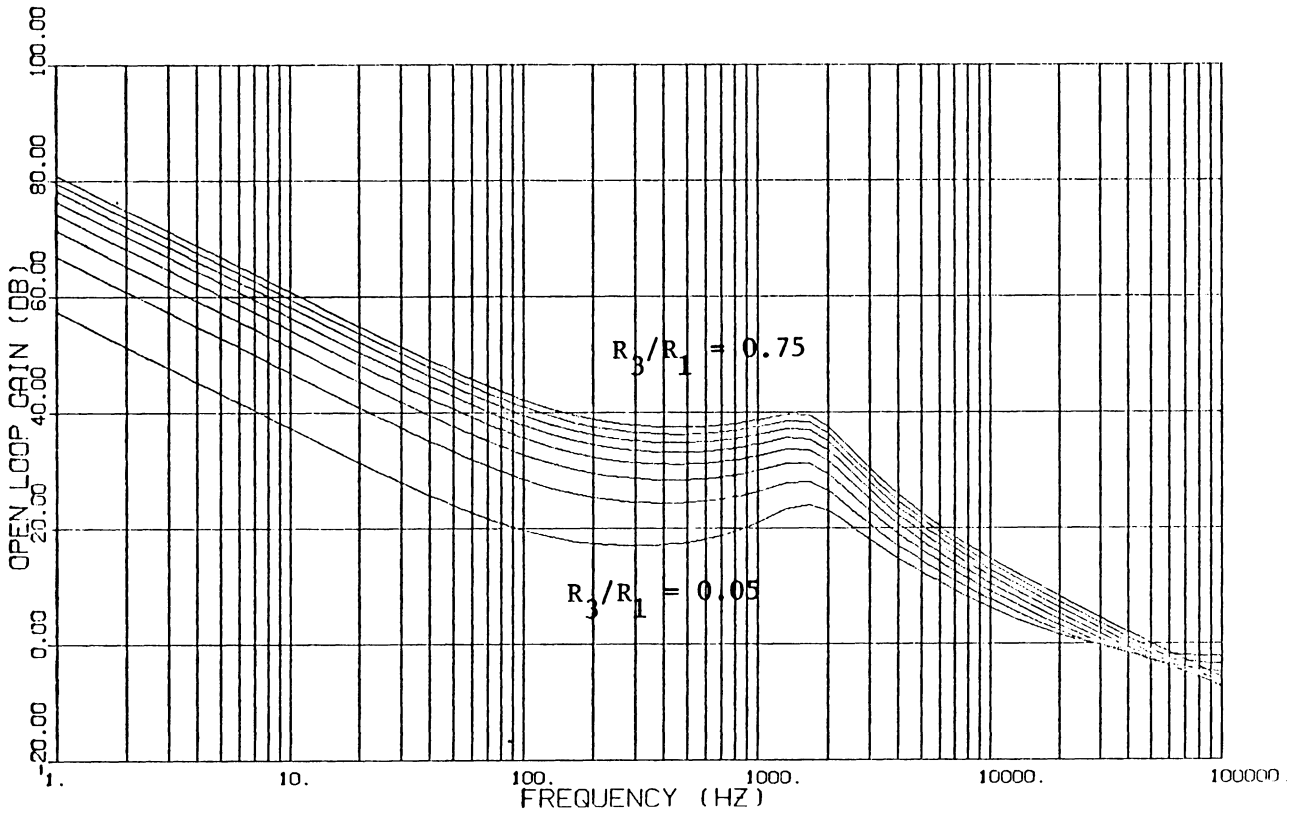


Fig. 7.5 (a) Open-Loop Gain with $S_{o1} = \frac{1}{10}\omega_o$, $R_{p2} = 30$

R_3/R_1 = 0.05, 0.15, 0.25, 0.35, 0.45, 0.55,

0.65, 0.75

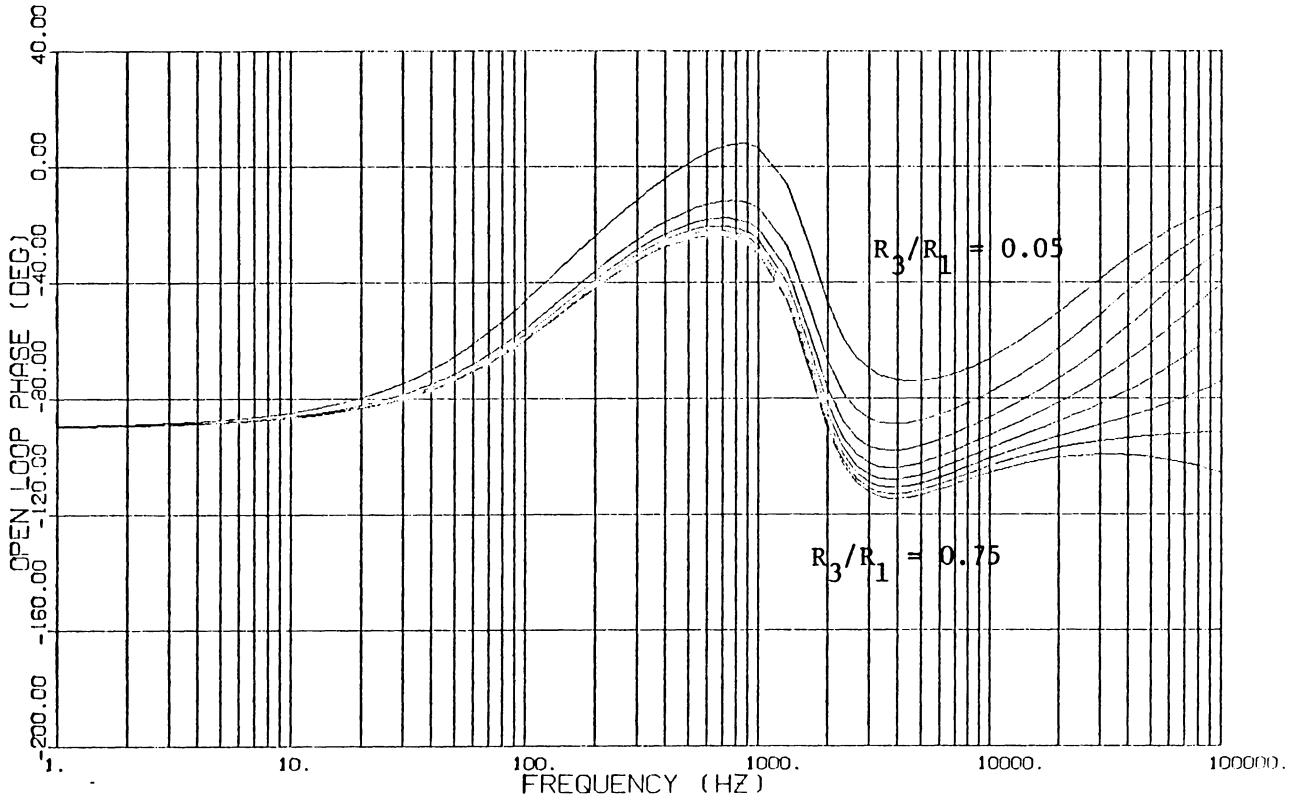


Fig. 7.5 (b) Open-Loop Phase with $S_{o1} = \frac{1}{10}\omega_o$, $R_{p2} = 30$

these figures, a) the larger the S_{o1} is, the higher low-frequency gain ($S < S_{o1}$) and mid-frequency gain ($S_{o1} < S < \omega_o$) can be obtained b) a smaller S_{o1} will give more boost in phase at frequencies between S_{o1} and ω_o, but the phase margin will not be affected by it, c) in general, it follows that the higher loop gain, the smaller phase margin, d) in each set of curves, as R_3/R_1 is increased, the phase at high frequencies degenerates. This is because the particular value we chose for F_{AC} and R_3/R_1 can not satisfy the design constraint.

As for the selection of F_{ac}, Fig. 7.6 illustrates the effects of different R_{p2} value by fixing S_{o1} and R_3/R_1. A smaller R_{p2}, or a smaller F_{AC}, will reduce the design margin that satisfies the constraints (4.12) and (4.13). Fig. 7.6 (b) shows as F_{AC} decreases the phase margin also decreases and eventually drops towards -180°.

7.3 Effects of the 2nd Stage Output Filter

one of the drawbacks of buck-boost converter is that both the input and output currents are of pulsating type, which produces a high ripple in the output current.

In order to provide a good output voltage regulation, a second stage output filter is usually employed. While the first stage output filter takes most of the pulsating current, the second stage output filter provides a low-ripple output current to the load.

While the DC regulation performance is improved, a brief analysis of the effects of the second stage output filter is given in this section.

The output stage with the second stage output filter is shown in Fig. 7.7. After employing the second stage output filter, the power

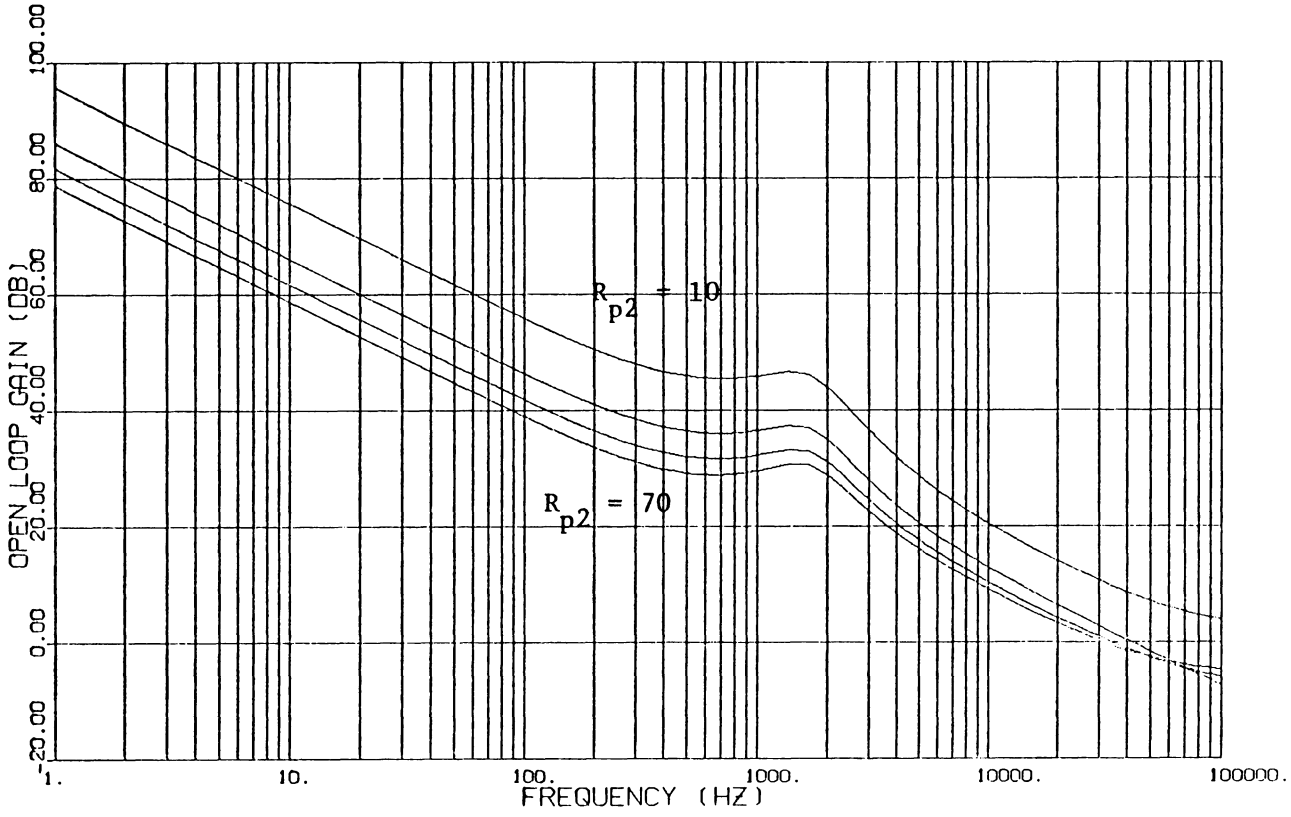


Fig. 7.6 (a) Open-Loop Gain with $S_{o1} = \frac{1}{4}\omega_o$,

$R_3/R_1 = 0.55$, $R_{p2} = 10, 30, 50, 70$

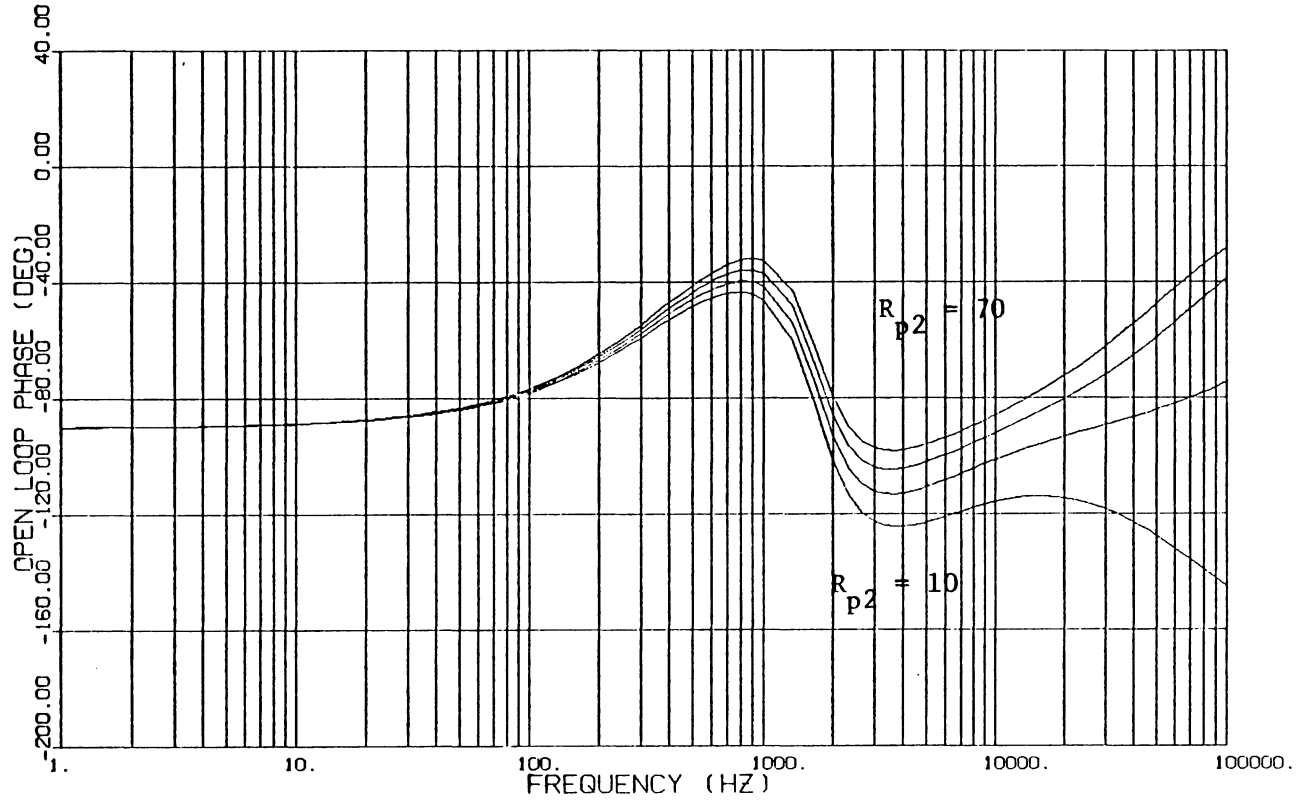


Fig. 7.6 (b) Open-Loop Phase with $S_{o1} = \frac{1}{4}\omega_o$, $R_3/R_1 = 0.55$

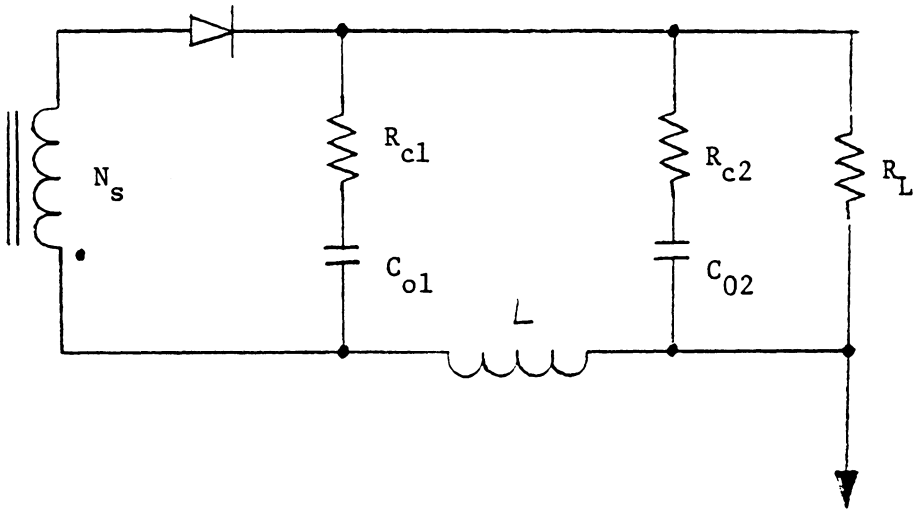


Fig. 7.7 Output Stage to DC Loop with Two Stage Output Filter

stage transfer functions would be modified. Without going through detailed derivations, the transfer functions in the open-loop characteristic equation that had been changed are given below:

$$\omega_1 = \frac{1}{\sqrt{L_e C_{o1}}} \tag{7.1}$$

$$\omega_2 = \frac{1}{\sqrt{LC_{o2}}} \tag{7.2}$$

$$\zeta_1 = \frac{\omega_1}{2} \cdot \left(R_e + \frac{R_{c1}}{D'} \right) C_{o1} \tag{7.3}$$

$$\zeta_2 = \frac{\omega_2}{2} \cdot \left(\frac{L}{R_L} + R_{c1}C_{o2} + R_{c2}C_{o2} \right) \tag{7.4}$$

$$\Delta_1 = \frac{s^2 + 2\zeta_1\omega_1 S + \omega_1^2}{\omega_1^2} \tag{7.5}$$

$$\Delta_2 = \frac{s^2 + 2\zeta_2\omega_2 S + \omega_2^2}{\omega_2^2} \tag{7.6}$$

$$F_{D1} = \frac{V_o}{DD'} \left(SR_{c1}C_{o1} + 1 \right) \left(SR_{c2}C_{o2} + 1 \right) \left(1 - \frac{DL_e}{R_L} S \right) \tag{7.7}$$

$$F_{D2} = \frac{V_o N_s}{(D')^2 R_L N_p} \cdot \left[D'\Delta_1\Delta_2 + (SR_L C_{o1} + 1)(\Delta_2 + D) \right] \tag{7.8}$$

$$G_T = \frac{F_M}{\Delta_1\Delta_2} (F_{D1} \cdot F_{DC} + F_{D2} \cdot F_{AC}) \tag{7.9}$$

where

$$R_{c1} = R_c$$

$$C_{o1} = C$$

$$\omega_1 = \omega_o$$

Since the main function of the second-stage output filter is tcattenuate high frequency noise, low frequency characteristic should not beaffected. Eq.s (7.7), (7.8) and (7.9) have the similar forms as with single-stage output filter case. To illustrate the effects of the second stage output filter we choose F_{AC} as variable and generate a family of curves of open-loop gain and phase as shown in Fig. 7.8 (a), (b). In Fig. 7.8 (a) we see the possibility of complex zeros at high frequency and Fig. 7.8 (b) reveals that as F_{AC} is larger than 0.016 the complex zeros become positive.

When F_{AC} is smaller than 0.016, the phase approaches -360°, the locus of open-loop zero as F_{AC} varies are shown in Fig. 7.9. As F_{AC} increases the complex zeros (S_{o4}, S_{o5}) move from right half s-plane to left half s-plane, S_{o3} increases, S_{o2} decreases and S_{o1} almost stays still. Compare to Fig. 7.10 (a), (b), the open-loop gain and phase with only one stage output filter, the effects of the second stage filter is clearly illustrated.

The locus of the complex zeros as a function of AC loop gain can be illustrated using Fig. 7.9, Fig. 7.11 and Fig. 7.12. In Fig. 7.9, the complex zeros migrate from the right-half S-plane to the left-half S-plane as F_{AC} is increased, and as F_{AC} is sufficiently large AC loop

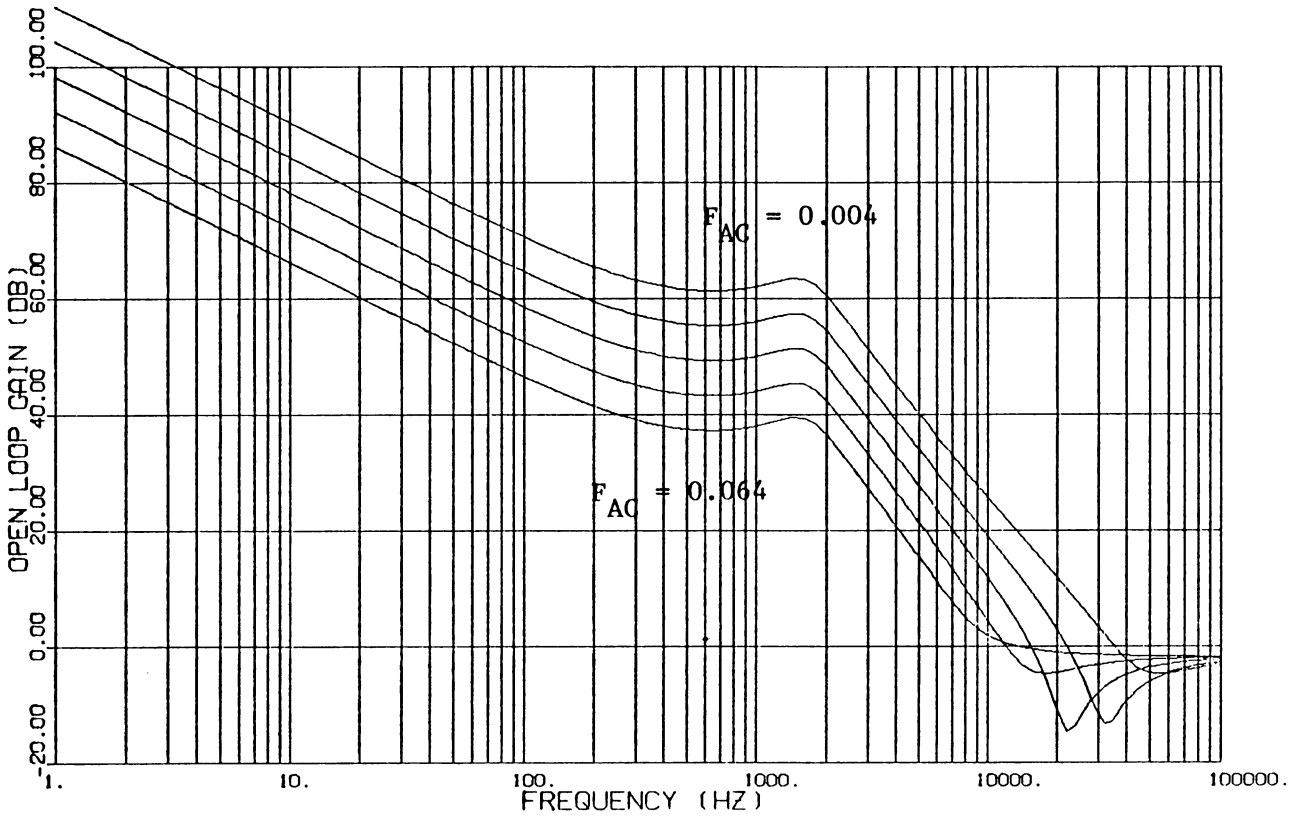


Fig. 7.8 (a) Open-Loop Gain with Second Stage Output Filter

F_{AC} = 0.004, 0.008, 0.16, 0.032, 0.064

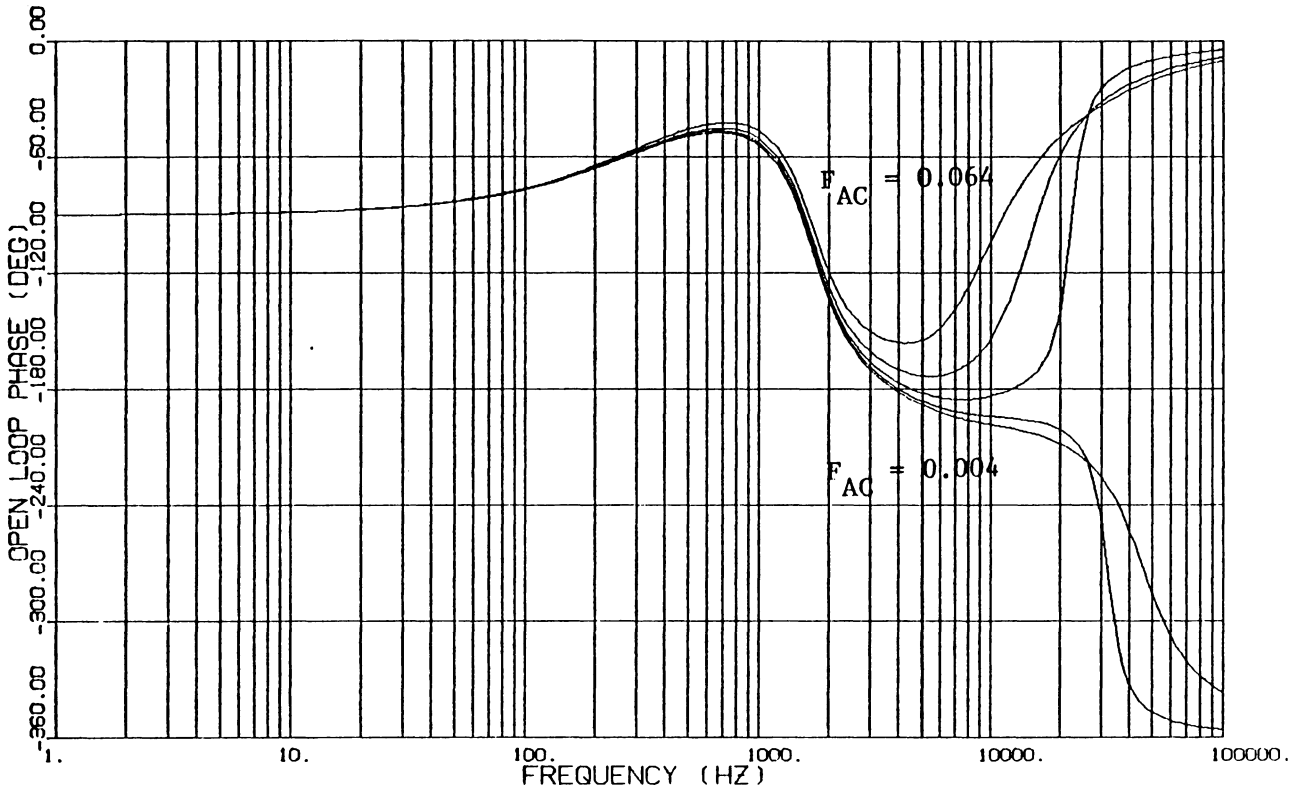


Fig. 7.8 (b) Open-Loop Phase with Second Stage Output Filter

F_{AC} = 0.004, 0.008, 0.016, 0.032, 0.064

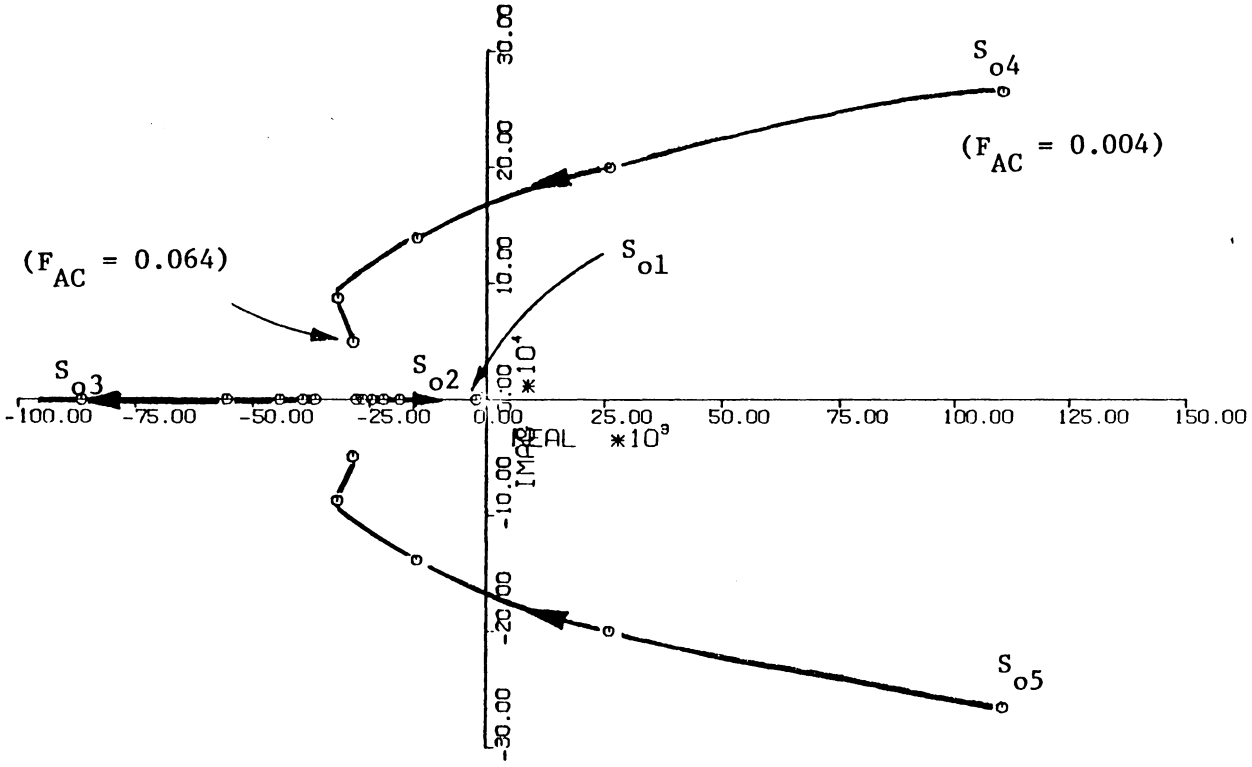


Fig. 7.9 Open-Loop Zeros by Changing F_{AC}

F_{AC} = 0.004, 0.008, 0.016, 0.032, 0.064

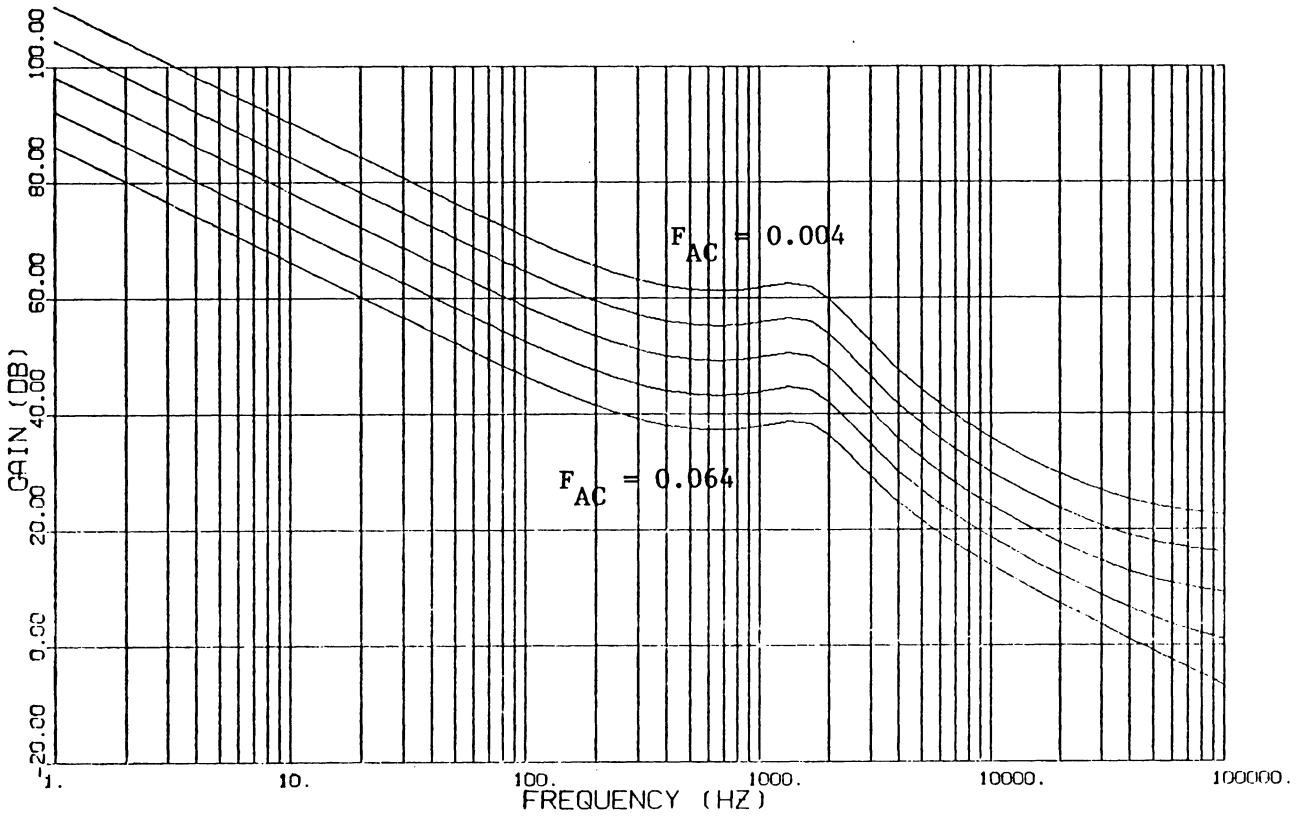


Fig. 7.10 (a) Open-Loop Gain with One Stage Output Filter

F_{AC} = 0.004, 0.008, 0.016, 0.032, 0.064

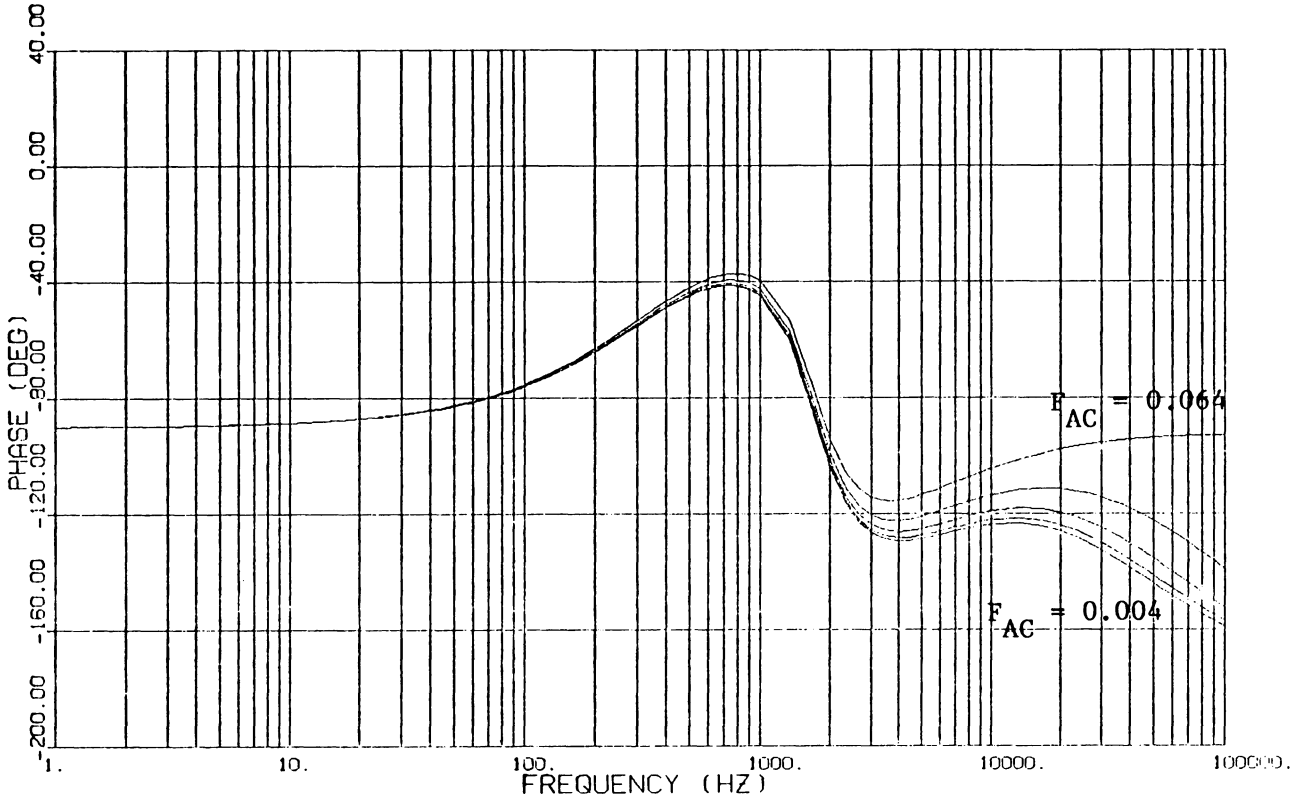


Fig. 7.10 (b) Open-Loop Phase with One Stage Output Filter

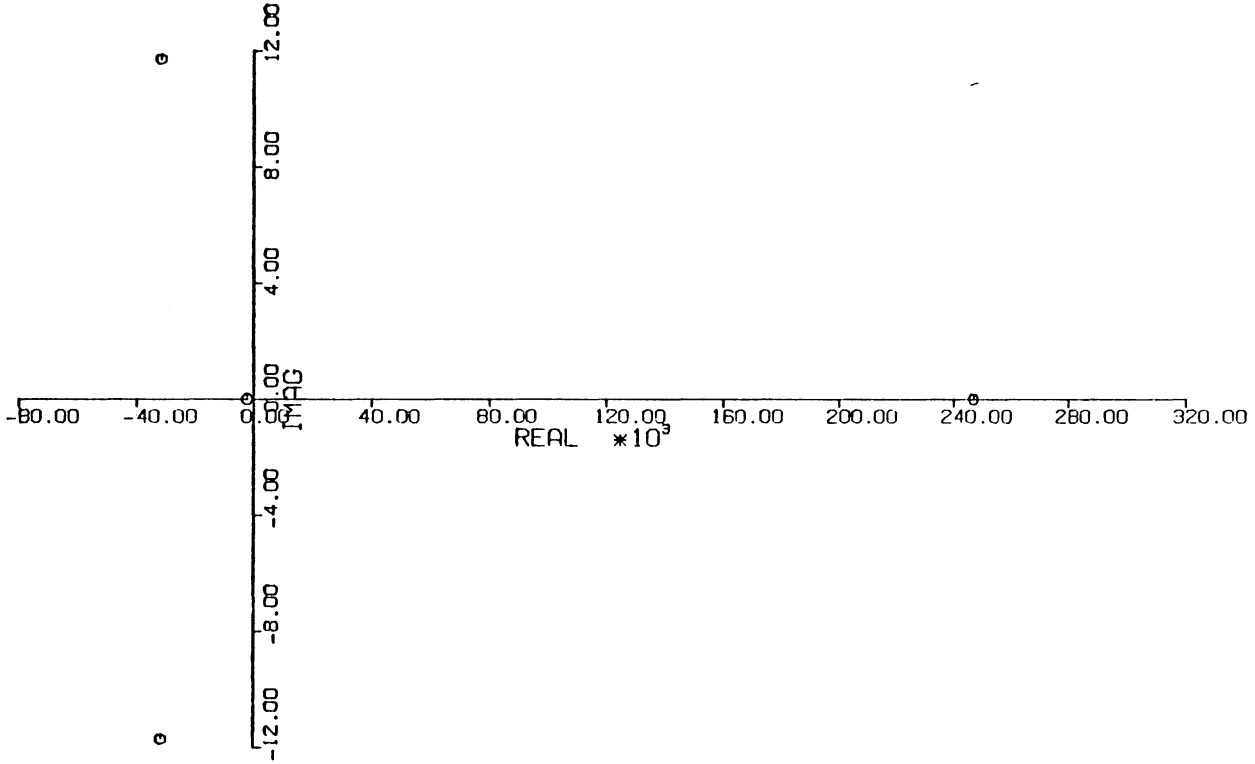


Fig. 7.11 (a) Zeros of $F_{D1}F_{DC}$

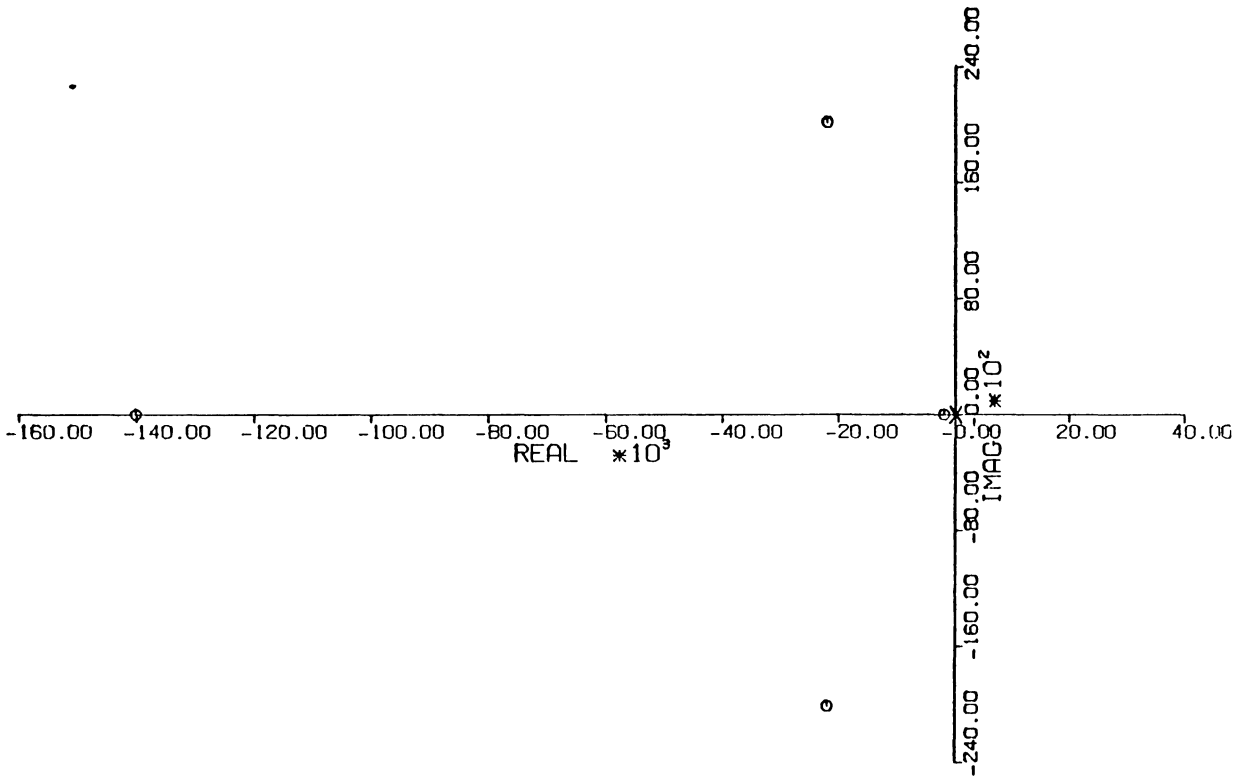


Fig. 7.11 (b) Zeros of $F_{D2}F_{AC}$

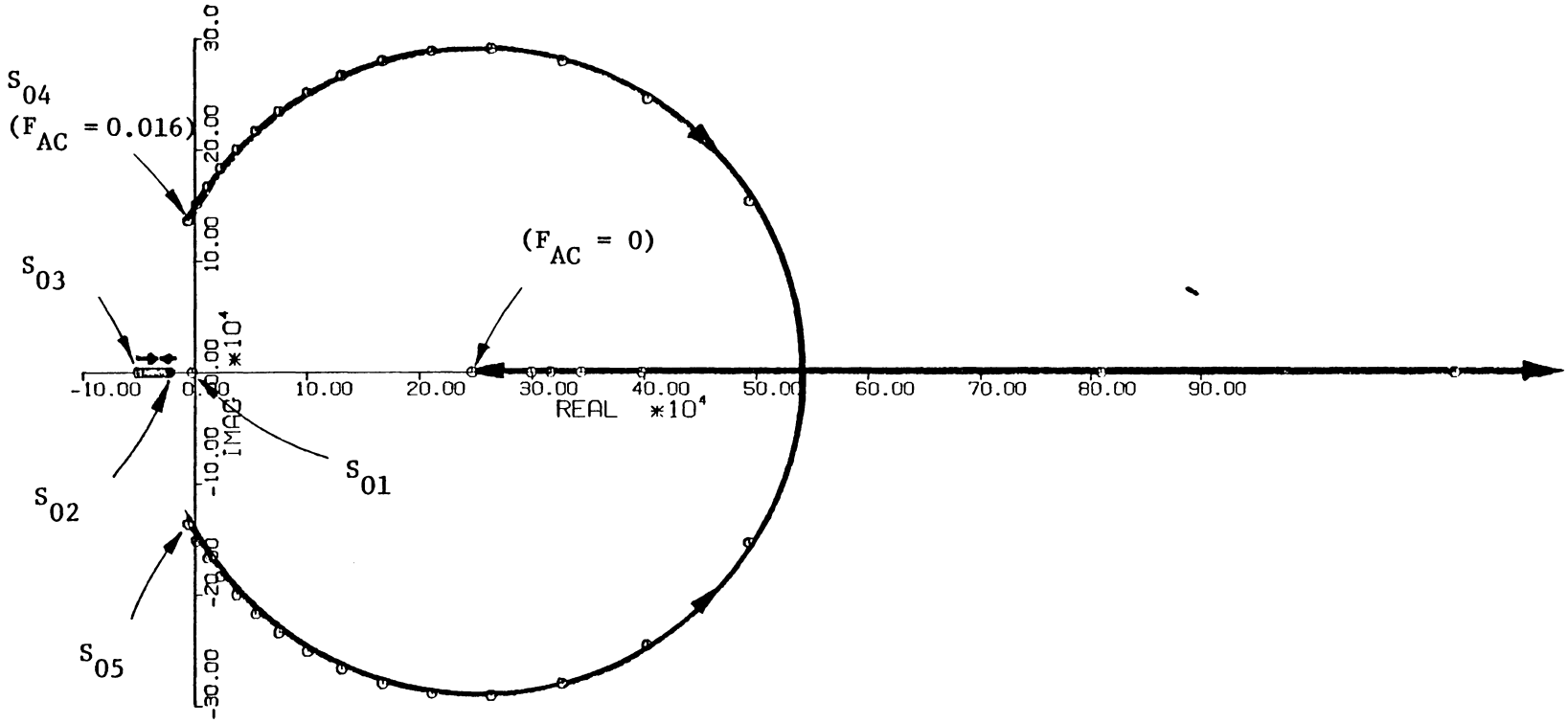


FIG. 7.12 OPEN-LOOP COMPLEX ZEROS LOCK CORRESPONDING TO A DECREASING F_{AC}

gain dominates DC loop gain and open loop zeros becomes the zeros of AC loop as shown in Fig. 7.11(b). By comparing Fig. 7.9 with Fig. 7.11(b), the two complex zeros, S_{04} and S_{05}, end at the AC loop complex zeros; S_{03} becomes increasingly more negative and ends at the larger negative zero in Fig. 7.11(b); S_{02} and S_{01} merge together and form another pair of complex zeros then become two real zeros and separate apart, one terminates at the smaller negative zero in Fig. 7.11(b) and the other ends at origin, which is cancelled by the open loop pole at origin.

On the other hand, as F_{AC} is decreased, the two complex zeros shown in Fig. 7.12 become positive. If F_{AC} is sufficiently small, the open loop zeros become the zeros of DC loop as shown in Fig. 7.11 (a). By comparing Fig. 7.12 with Fig. 7.11(a), the two complex zeros, S_{04} and S_{05}, merge together then separate apart along the real axis; one goes to infinity and the other one ends at the positive zero of the DC loop gain as shown in Fig. 7.11(a). S_{02} and S_{03} merge together to form the complex zeros of the DC loop gain as shown in Fig. 7.11(a). S_{01} hardly moves due to the scale we used.

Within the normal range of F_{AC}, the complex zeros always exhibit in the open loop. The designer should avoid positive complex zeros by increasing F_{AC}. However, increasing F_{AC} will cause the overall loop gain to reduce as can be seen from Fig. 7.8(a). The critical value of F_{AC} to ensure negative complex zeros is 0.01383.

7.4 Test Verification

A test circuit has been built to verify the existing theory. The actual parameters values are listed in Table 7.1. According to the design guideline given in 7.2, choose S_{01} to be (1/4)WO and R3/R1=1. Since the true open loop gain and phase cannot be measured by injecting an AC signal [4], only analytical characteristic curves are plotted for open loop. Which are illustrated in Fig. 7.13.

With DC loop opened, the system transfer function can be derived as:

$$GDC = \frac{F_M F_{DC} F_{D1}}{\Delta + F_M F_{AC} F_{D2}} \qquad (7,10)$$

Test verification is given in Fig. 7.14 for both the gain and phase.

The transfer function for control-to-output is derived as:

$$V_o/V_x = \frac{F_M F_{D1}}{\Delta + F_M F_{AC} F_{D2}} \qquad (7,11)$$

and the verification is demonstrated in Fig. 7.15.

The transfer function for audiosusceptibility is derived as:

$$GA = \frac{F_{V1}(\Delta + F_M F_{AC} F_{D2}) - F_M F_{AC} F_{D1} F_{V2}}{\Delta^2 (1 + G_T)} \qquad (7,12)$$

the verification is demonstrated in Fig. 7.16.

Table 7.1

Test Circuit Parameters

Vi=23V	R1=4.3 KΩ
Vo=5.05V	R3=4.3 KΩ
Np=24 turns	C2=0.1 μF
Ns=10 turns	R4=9.1 KΩ
Tp=18.5 μS	R5=7.5 KΩ
Lp=43.2 μH	Rp2=11 Ω

$Ls=Lp\ (Ns/Np)^2$ μH

$n=125/2$

Rs=.013 Ω

Rc=.07 Ω

RL=3 Ω

C=660 μF

$Re=Rs/(D')^2$

$Le=Ls/(D')^2$

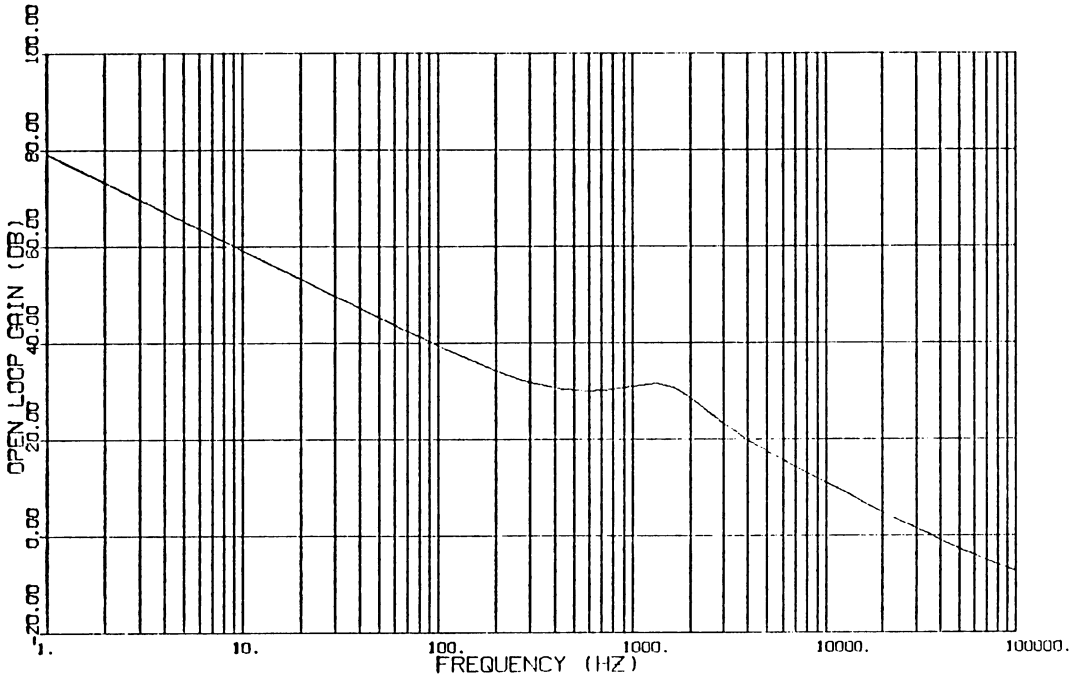


Fig. 7.13 (a) OPEN LOOP GAIN WITH So1=(1/4)Wo,
R3/R1=1, Fac=0.176

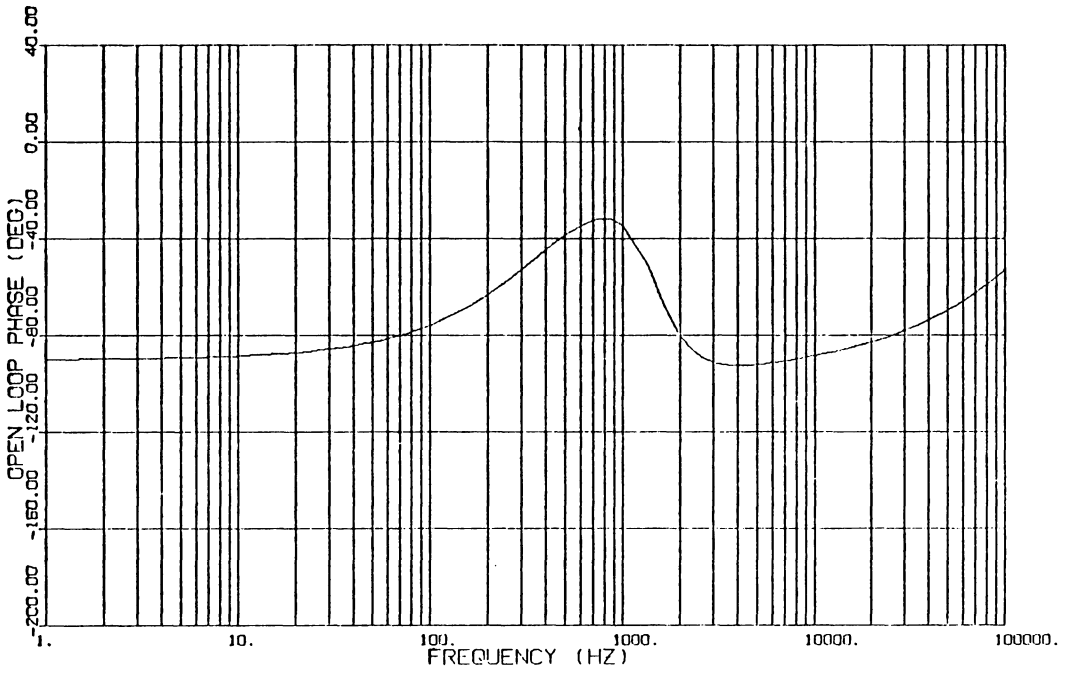


Fig. 7.13 (b) OPEN LOOP PHASE WITH So1=(1/4)Wo,
R3/R1=1, Fac=0.176

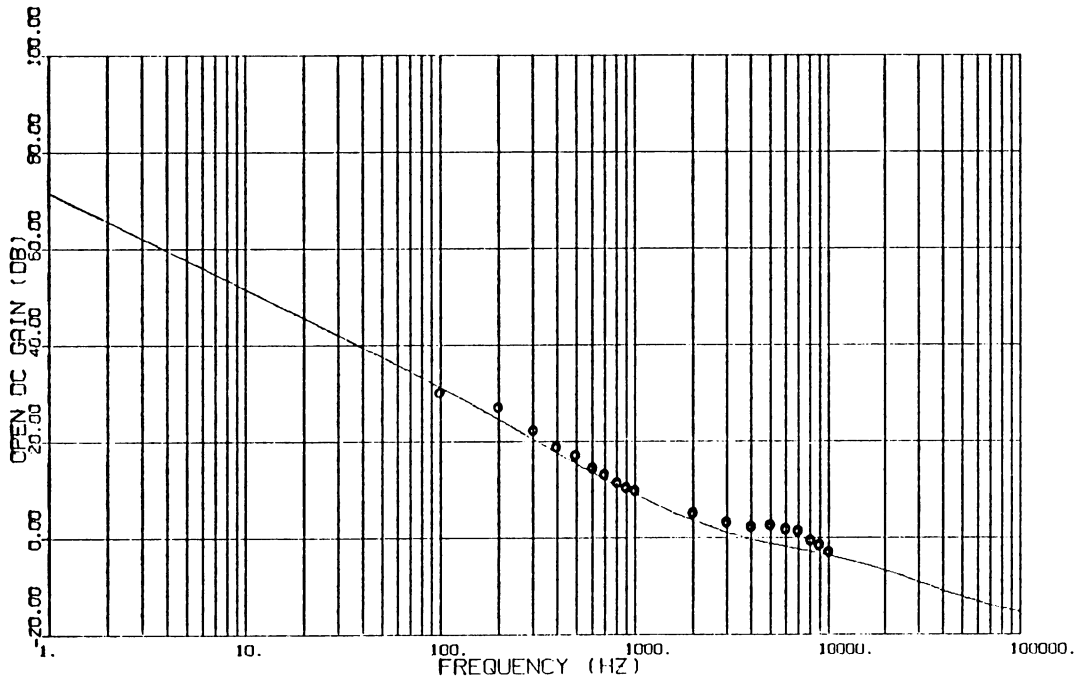


Fig. 7.14 (a) THEORY AND MEASUREMENT OF OPEN DC LOOP GAIN

——— THEORY ∘ MEASUREMENT

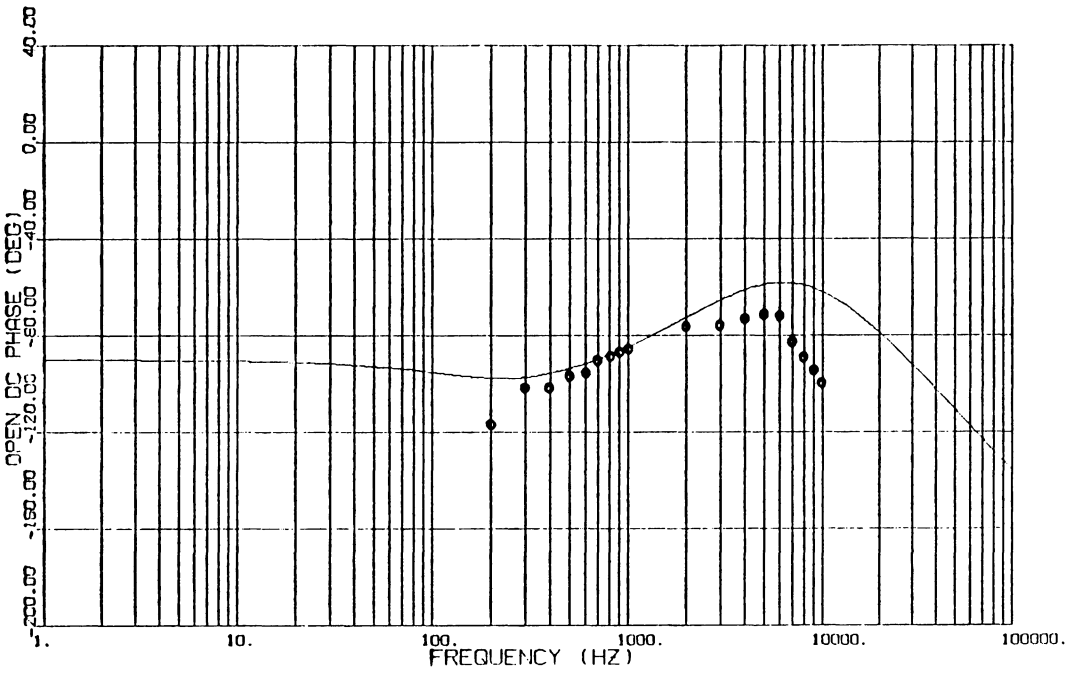


Fig. 7.14 (b) THEORY AND MEASUREMENT OF OPEN DC LOOP PHASE

——— THEORY ∘ MEASUREMENT

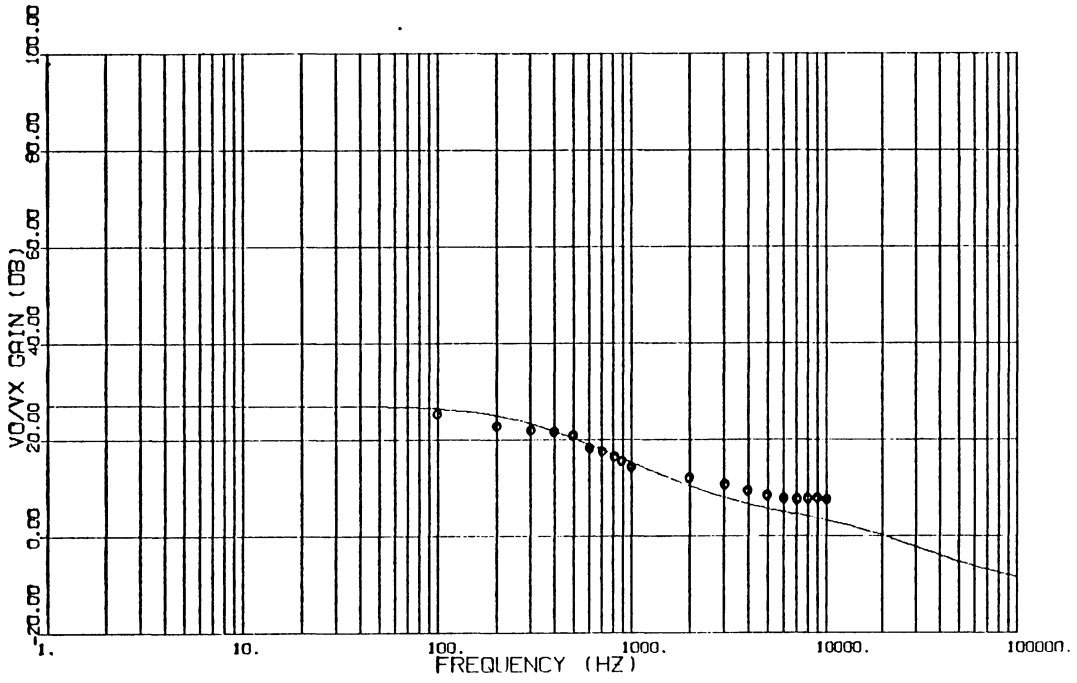


Fig. 7.15 (a) THEORY AND MEASUREMENT OF CONTROL TO OUTPUT GAIN

——— THEORY o MEASUREMENT

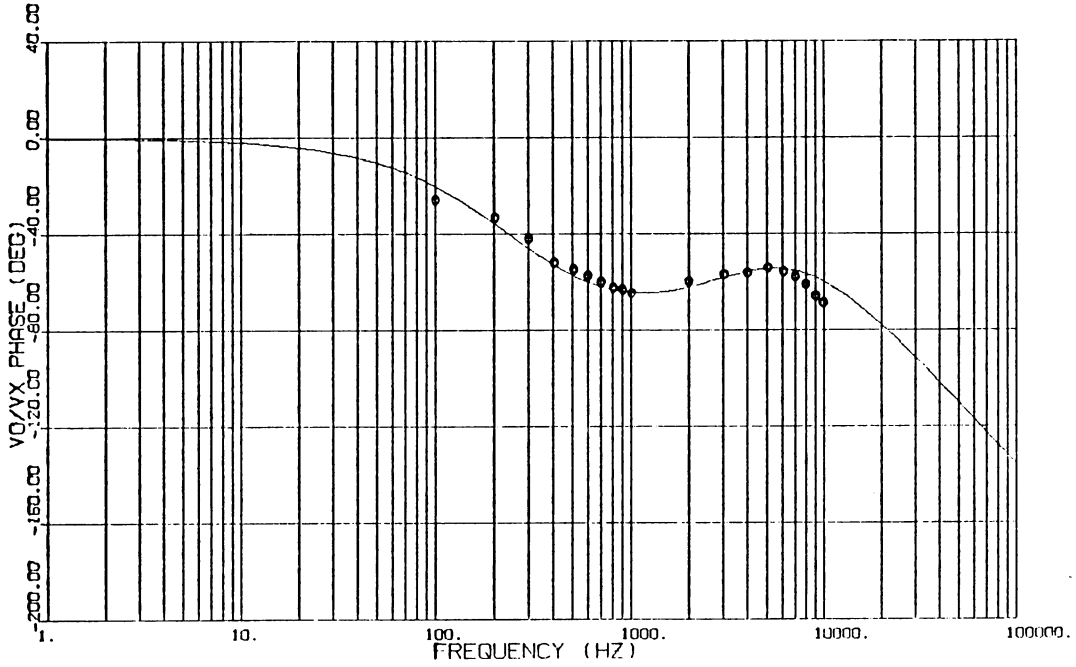


Fig. 7.15 (b) THEORY AND MEASUREMENT OF CONTROL TO OUTPUT PHASE

——— THEORY ∘ MEASUREMENT

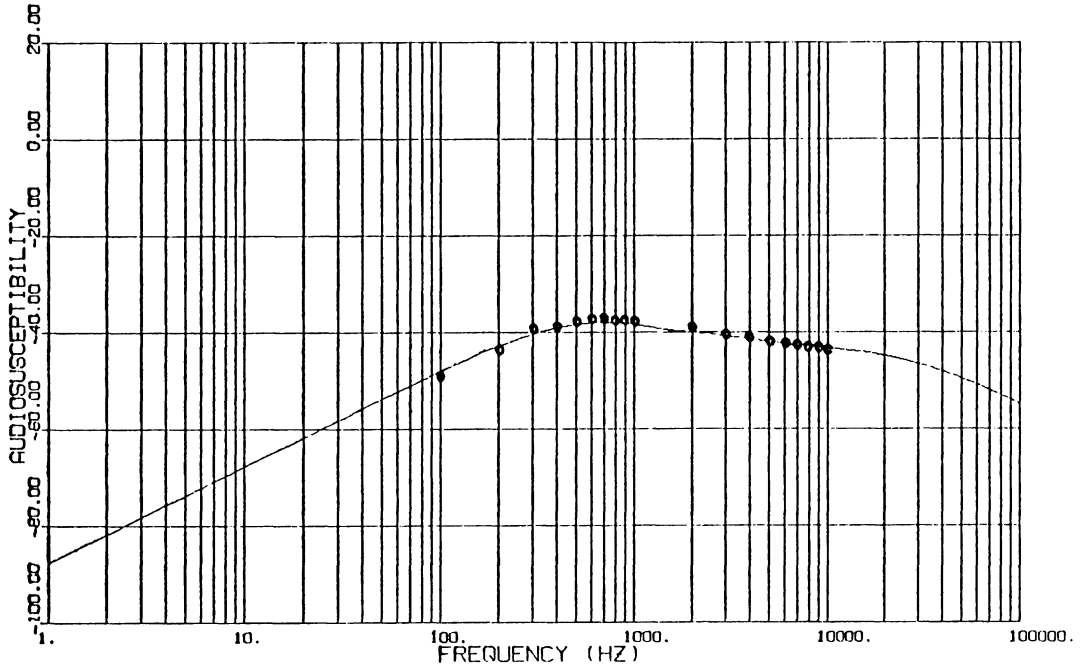


Fig. 7.16 THEORY AND MEASUREMENT OF AUDIOSUSCEPTIBILITY

—— THEORY ∘ MEASUREMENT

CHAPTER VIII

CONCLUSIONS AND FUTURE WORK

A buck-boost DC-DC converter employing current-injected control scheme is analyzed in this thesis. The advantages of using current-injected control over the other types of control scheme are: inherent peak current protection of the power switch, improved dynamic performances and balanced parallel module operation. A switching regulator using this type of control scheme not only achieves a constant voltage source but also provides, to some extent, current control which limits the peak switch current or peak inductor current.

In Chapter II, the modeling of current-injected converter is provided. The model consists of three transfer functions, characterizing the power stage, the analog processor (ASP), and the digital signal processor (DSP). The power stage incorporating two possible forms of small digital disturbances from line and control loops was derived using state space averaging techniques and transformed to an equivalent circuit. The ASP model consists of two feedback loops: DC loop and current injected. These two feedback loops sense and process the output voltage and the switch current to provide the necessary feedback information to DSP. The DSP then processes the input analog signal into a digitized output signal to control the duty cycle of the power switch. Finally, the model is characterized by a small signal block diagram.

In Chapter III, the simple gain compensation was employed in both DC and AC loop. Two basic design constraints were derived. These two constraints dictate the fundamental relationship between

DC loop and AC loop gain. If the design constraints are violated, positive zeros will be observed in the open-loop characteristic.

Chapter IV and V further examine the open-loop characteristics with lag compensation and lead-lag compensation network in the DC loop, respectively. Some design constraints and limitations as derived in Chapter III are also exhibited in these two cases. After a thorough study, it is concluded that no obvious benefit can be achieved by using lead-lag compensation over that of a simple lag compensation.

Chapter VI examines the effects of different duty cycle control modes. Means of stabilizing the constant frequency operation with duty cycle greater than 50% were discussed. An optimal external ramp was suggested which offers higher loop gain and more unified performance.

In Chapter VII, the key design parameters were identified and design guidelines were given based on the lag compensation scheme. The design objective is to identify a set of control parameters such that a high gain and stable loop characteristics can be achieved within the confinement of the two previously established design constraints. In this chapter, the effects of adding second stage output filter to the converter is also discussed. For insufficient AC loop gain, a sharp reduction in the open-loop gain and drastically change in phase due to a pair of complex zeros are observed.

Through the course of investigation, several limitations associate with the current-injected control scheme are observed. First, two

design constraints, dictating basic relations between DC loop and AC loop must be satisfied to avoid the presence of positive zeros. Second, the interaction among the open-loop pole-zero forbids the independent adjustment of them. Whereas compare to the SCM switching regulator [1,3] the open-loop poles and zeros can be adjusted independently. The implementations of current-injected control and SCM share many similarities. Nevertheless, the current-injected control senses the switch current, while the SCM control senses the flux of the energy storage inductor/transformer. Consequently, the current-injected control fails to provide an AC signal during T_{OFF} interval; SCM, although provides total flux (a state variable) feedback, fails to relate its DC portion of the flux waveform. What seems to be most desirable is a control loop that provides a total state feedback by sensing either the magnetic flux (both DC and AC components) or both primary current and secondary currents. If the suggested control could be easily implemented without resort to complicated electronic circuitry, the control will combine the merits from both SCM and current-injected control.

Another interesting extension of the present work is to investigate the adaptibility of the current-injected control to output filter parameters and possible reactive loading effect. In our analysis, only a resistive load is assumed. In practical applications, the load is often reactive and consequently the load could interact with the switching regulator in a complicated and dynamic fashion.

APPENDIX A

DUTY CYCLE PULSE-WIDTH-MODULATOR MODEL

The Fourier series expansion of d(t), which is equated as eq. (2.45), is given below:

$$d(t) = D + a_1 \sin\omega t + b_1 \cos\omega t + \ldots . \qquad (A.1)$$

In characterizing the small signal model we are only interested in the fundamental component of the Fourier series. The coefficient a_1 of eq. (A.1) can be derived as:

$$a_1 = \frac{\omega}{\pi}\left(\int_{t_0}^{t_1} \sin\omega t\, dt + \int_{t_2}^{t_3} \sin\omega t\, dt + \ldots + \int_{t_{2n}}^{t_{2n+1}} \sin\omega t\, dt \right)$$

$$= \frac{\omega}{\pi} \sum_{n=1}^{N} A_{2n} \qquad \text{, N is the ratio between switching frequency and modulation frequency.} \qquad (A.2)$$

where $A_{2n} \triangleq \int_{t_{2n}}^{t_{2n+1}} \sin\omega t\, dt$

$$= \frac{2}{\omega} \sin\frac{\omega}{2}(t_{2n+1} + t_{2n}) \sin\frac{\omega}{2}(t_{2n+1} - t_{2n})$$

$$= \frac{2}{\omega} \sin\frac{\omega}{2}(2t_{2n} + T_N^n) \sin\frac{\omega}{2} T_N^n \qquad (A.3)$$

where T_N^n is the on time interval of the nth cycle shown in Fig. 2.8. T_N^n can be derived as follows.

In Fig. 2.8 it can be shown that during T_r^{n-1}:

$$V_T(t_{2n}) = S_F(t_{2n} - t_{2n-1}) + A\sin\omega t_{2n} - A\sin\omega t_{2n-1} \quad (A.4)$$

, without considering the two DC levels, V_x and E_T, and during T_N^n:

$$V_T(t_{2n}) = S_N(t_{2n+1} - t_{2n}) + A\sin\omega t_{2n} - A\sin\omega t_{2n+1} \quad (A.5)$$

Eqs. (A.4) and (A.5) have to be equal,

$$A\sin\omega t_{2n+1} - A\sin\omega t_{2n-1} + S_F(t_{2n} - t_{2n-1}) - S_N(t_{2n+1} - t_{2n}) = 0$$

Since

$$t_{2n+1} - t_{2n-1} = T_N^n + T_F^{n-1} \quad (A.6)$$

$$t_{2n+1} + t_{2n-1} = 2t_{2n-1} + T_N^n + T_F^{n-1}$$

eq. (A.6) can be rewritten as:

$$S_F T_F^{n-1} - S_N T_N^n + 2A\cos\frac{\omega}{2}(2t_{2n-1} + T_N^n + T_F^{n-1})\sin\frac{\omega}{2}(T_N^n + T_F^{n-1}) = 0$$

Substitute the following equations into the above equation: (A.7)

$$T_F^{n-1} = T_P - T_N^{n-1}$$

$$T_F^n = T_P - T_N^n$$

then

$$S_F(T_P - T_N^{n-1}) - S_N T_N^n + 2A\cos\omega\left(t_{2n-1} + \frac{T_N^n - T_N^{n-1} + T_P}{2}\right).$$

$$\sin\frac{\omega}{2}(T_N^n - T_N^{n-1} + T_P) = 0 \quad (A.8)$$

Assume $T_N^n - T_N^{n-1} \ll T_P$ and because modulation frequency is much lower than the switching frequency, the following approximation stays true:

$$T_N^{n-1} \simeq T_N^n$$

with these two assumptions, eq. (A.8) becomes

$$S_F(T_P - T_N^n) - S_N T_N^n + 2A \cos\omega(t_{2n-1} + \frac{T_P}{2}) \sin\frac{\omega T_P}{2} = 0 \qquad (A.9)$$

Solving for T_N^n:

$$T_N^n = \frac{1}{S_N + S_F}\left[2A\sin\frac{\omega T_P}{2}\cos\omega(t_{2n-1} + \frac{T_P}{2}) + S_F T_P\right] \qquad (A.10)$$

At steady state

$$T_N = \frac{S_F}{S_N + S_F} T_P \qquad (A.11)$$

Substitute eq. (A.10) into eq.(A.3):

$$A_{2n} \simeq \frac{1}{S_F + S_N}\left[2A\sin\frac{\omega T_P}{2}\cos\omega(t_{2n-1} + \frac{T_P}{2}) + S_F T_P\right] \cdot$$

$$\sin\omega\left\{t_{2n} + \frac{1}{2}\frac{1}{S_N + S_F}\left[2A\sin\frac{\omega T_P}{2}\cos\omega(t_{2n-1} + \frac{T_P}{2}) + S_F T_P\right]\right.$$

$$\simeq \frac{2A}{S_N + S_F}\sin\frac{\omega T_P}{2}\cos\omega(t_{2n-1} + \frac{T_P}{2})\sin\omega(t_{2n} + \frac{S_F}{S_N + S_F}\frac{T_P}{2})$$

$$+ \frac{S_F\, T_P}{S_N + S_F}\sin\omega(t_{2n} + \frac{S_F}{S_N + S_F}\frac{T_P}{2})$$

Assume

$$t_{2n-1} = t_{2n} - T_F^{n-1} = t_{2n} - T_P + T_N^{n-1} \simeq t_{2n} - T_P + T_N^n$$

$$A_{2n} \simeq \frac{2A}{S_N + S_F}\sin\frac{\omega T_P}{2}\cos\omega(t_{2n} - \frac{T_P}{2} + \frac{S_F}{S_N + S_F}T_P)\sin\omega(t_{2n} + \frac{S_F}{S_N + S_F}\frac{T_P}{2})$$

$$+ \frac{S_F\, T_P}{S_N + S_F}\sin\omega(t_{2n} + \frac{S_F}{S_N + S_F}\frac{T_P}{2})$$

$$A_{2n} \simeq \frac{A}{S_N + S_F} \sin\frac{\omega T_P}{2} \left[\sin\omega\left(2t_{2n} + \frac{S_F}{S_N + S_F}\cdot\frac{3T_P}{2} - \frac{T_P}{2}\right) + \sin\omega\left(\frac{S_N}{S_N + S_F}\frac{T_P}{2}\right)\right]$$

$$+ \frac{S_F \; T_P}{S_N + S_F} \sin\omega\left(t_{2n} + \frac{S_F}{S_N + S_F} \; \frac{T_P}{2}\right) \qquad \text{(A.12)}$$

If N is very large, eq. (A.2) can be approximated by the following integration

$$a_1 \simeq \frac{\omega}{\pi T_P} \int_0^{\frac{2\pi}{\omega}} A_{2n} dt \qquad \text{(A.13)}$$

Making (A.12) to be more general, let $t_{2n}=t$, and using the fact that ωT_P is very small,

$$\sin\frac{\omega T_P}{2} \simeq \frac{\omega}{2} T_P$$

$$\sin\omega\left(\frac{S_N}{S_N + S_F} \; \frac{T_P}{2}\right) \simeq \frac{\omega T_P}{2} \frac{S_N}{S_N + S_F}$$

then substitute eq. (A.12) into eq.(A.13), we have:

$$a_1 \simeq \frac{\omega}{\pi T_P} \cdot \frac{A}{S_N + S_F} \frac{\omega T_P}{2} \cdot \frac{\omega T_P}{2} \cdot \frac{S_N}{S_N + S_F} \cdot \frac{2\pi}{\omega}$$

$$\simeq \frac{\omega T_P}{2} \cdot \frac{A \; S_N}{(S_N + S_F)^2} \qquad \text{(A.14)}$$

The coefficient b_1 can be calculated following the same procedure as the calculation of a_1.

$$b_1 = \frac{\omega}{\pi}\left[\int_{t_0}^{t_1} \cos\omega t \; dt + \cdots + \int_{t_{2n}}^{t_{2n+1}} \cos\omega t \; dt\right] \triangleq \frac{\omega}{\pi} \sum_{n=1}^{N} B_{2n}$$

where

$$B_{2n} \triangleq \int_{t_{2n}}^{t_{2n+1}} \cos\omega t \, dt = \frac{1}{\omega} \sin\omega t \Big|_{t_{2n}}^{t_{2n+1}}$$

$$= \frac{2}{\omega} \cos \frac{\omega}{2} (t_{2n+1} + t_{2n}) \sin \frac{\omega}{2} (t_{2n+1} - t_{2n})$$

$$B_{2n} = \frac{2}{\omega} \cos \frac{\omega}{2} (2t_{2n} + T_N{}^n) \sin \frac{\omega}{2} T_N{}^n$$

$$= T_N{}^n \cos\omega \left(t_{2n} + \frac{T_N{}^n}{2}\right)$$

substitute $T_N{}^n$ of eq. (A.10) into B_{2n}, the following simplified solution can be obtained:

$$B_{2n} \simeq \frac{1}{S_N + S_F} \left[2A \sin \frac{\omega T_P}{2} \cos\omega \left(t_{2n-1} + \frac{T_P}{2}\right) + S_F T_P \right] \cdot$$

$$\cos\omega \left(t_{2n} + \frac{S_F}{S_N + S_F} \cdot \frac{T_P}{2}\right)$$

$$b_1 \triangleq \frac{\omega}{\pi} \sum_{n=1}^{N} B_{2n}$$

$$\simeq \frac{\omega}{\pi T_P} \cdot \frac{1}{S_N + S_F} \int_0^{2\pi/\omega} \left[2A\sin \frac{\omega T_P}{2} \cos\omega \left(t_{2n} - \frac{T_P}{2} + \frac{S_F T_P}{S_N + S_F}\right) + S_F T_P \right] \cdot$$

$$\cos\omega \left(t_{2n} + \frac{S_F}{S_N + S_F} \frac{T_P}{2}\right) dt$$

$$\simeq \frac{\omega}{\pi T_P} \frac{1}{S_N + S_F} \left[A \sin \frac{\omega T_P}{2} \cos \frac{\omega T_P}{2} \left(\frac{S_F}{S_N + S_F} - 1\right) \cdot \frac{2\pi}{\omega} \right]$$

$$\simeq \frac{\omega}{\pi T_P} \cdot \frac{1}{S_N + S_F} \left[A\, \pi T_P \cdot \cos\omega \left(\frac{S_N}{S_N + S_F} \cdot \frac{T_P}{2} \right) \right]$$

Assume

$$\cos\omega \left(\frac{S_N}{S_N + S_F} \cdot \frac{T_P}{2} \right) \simeq 1$$

$$b_1 \simeq \frac{A\omega}{S_N + S_F} \tag{A.15}$$

The coefficients c_1 and d_1 are derived in the following. The instantaneous error signal can be expressed, without considering the two DC voltage E_T and V_x, as:

$$V_T(t_{2n}) \triangleq V_{2n} = S_N(t_{2n+1} - t_{2n}) + A \sin\omega t_{2n} - A \sin\omega t_{2n+1}$$

$$= S_N T_N{}^n - 2A \cos \frac{\omega}{2} \left(t_{2n+1} + t_{2n} \right) \sin \frac{\omega}{2} T_N{}^n$$

Substitute eq. (A.10) into the above equation:

$$V_{2n} = \frac{1}{S_N + S_F} \left\{ 2A \sin \frac{\omega T_P}{2} \cos \omega \left[t_{2n} + T_P \left(\frac{S_F}{S_N + S_F} - \frac{1}{2} \right) \right] + S_F T_P \right\} \cdot$$

$$\left[S_N - A\omega \cos\omega \left(t_{2n} + \frac{S_F}{S_N + S_F} \frac{T_P}{2} \right) \right]$$

We are only interested in fundamental component of V_{2n}.

$$V_{2n}\Big|_{\pm\omega} = \left\{ \frac{S_N}{S_N + S_F} 2A \sin \frac{\omega T_P}{2} \cos \omega T_P \left(\frac{S_F}{S_N + S_F} - \frac{1}{2} \right) \right.$$

$$\left. - \frac{S_F}{S_N + S_F} A\omega T_P \cos \left(\frac{\omega T_P}{2} \cdot \frac{S_F}{S_N + S_F} \right) \right\} \cdot \cos\omega t_{2n} +$$

$$\left\{\frac{-S_N}{S_N + S_F}\, 2A \sin\frac{\omega T_P}{2} \sin\omega T_P \left(\frac{S_F}{S_N + S_F} - \frac{1}{2}\right)\right.$$

$$\left. + \frac{S_F}{S_N + S_F} A\omega T_P \sin\frac{\omega T_P}{2}\right\} \cdot \sin\omega t_{2n}$$

The above equation can be simplified as:

$$V_{2n}\Big|_{\pm\omega} \simeq \frac{S_N - S_F}{S_N + S_F} A\omega T_P \cdot \cos\omega t_{2n}$$

The average effect of the above derived instantaneous waveform is calculated as follows:

$$\text{Average } V_{2n}\Big|_{\pm\omega} \triangleq \hat{V}_{2n}$$

$$\hat{V}_{2n} = \frac{1}{T_P}\left\{\frac{S_N - S_F}{S_N + S_F} A\omega T_P \cos\omega t_{2n} \cdot \frac{T_N{}^n}{2}\right.$$

$$\left. + \left[\frac{S_N - S_F}{S_N + S_F} A\omega T_P \cos\omega t_{2n+2} + ST_N{}^n\right] \cdot \frac{T_P - T_N{}^n}{2}\right\}$$

Detailed derivations is neglected. The fundamental component of $\hat{V}_{2n}$ is obtained.

$$\hat{V}_{2n} \simeq \frac{1}{2} \cdot \frac{S_N - S_F}{S_N + S_F} A\omega T_P \cos\omega t_{2n} \qquad \text{(A.16)}$$

The previously derived results are summarized as follows:

$$\text{Let } V_{2n}\Big|_{\pm\omega} = C_1 \sin\omega t_{2n} + d_1 \cos\omega t_{2n}$$

$$C_1 \approx 0$$

$$d_1 \approx \frac{1}{2} \frac{S_N - S_F}{S_N + S_F} A\omega T_P$$

$$C_T = (C_1^2 + d_1^2)^{\frac{1}{2}} = d_1$$

$$d(t) = a_1 \sin\omega t + b_1 \cos\omega t$$

where

$$a_1 \approx 0$$

$$b_1 \approx \frac{A\omega}{S_N + S_F}$$

$$A_T = (a_1^2 + b_1^2)^{\frac{1}{2}} = b_1$$

The phase of F_M is as following:

$$\exp j \left[\tan^{-1} \frac{b_1}{a_1} - \tan^{-1} \frac{d_1}{c_1}\right] = \exp j (\theta_1 - \theta_2)$$

$$\theta_1 = \tan^{-1} \infty = 90°$$

$$\theta_2 = \tan^{-1} \infty = 90°$$

$$\exp j(\theta_1 - \theta_2) = 1$$

Therefore,

$$F_M \triangleq \frac{\hat{d}}{\hat{V}_T} = \frac{A_T}{C_T} \exp j(\tan^{-1} \frac{b_1}{a_1} - \tan^{-1} \frac{d_1}{c_1})$$

$$= \frac{T_P}{2} \frac{1}{S_N - S_F} \qquad \text{(A.17)}$$

APPENDIX B

COMPUTER PROGRAMS

```
C  PROGRAM I
C  COMPUTER PROGRAM FOR OPEN-LOOP GAIN AND PHASE :

      COMPLEX S,FD1,FD2,FDC,G,DELTA
      REAL X(138),Y1(138),Y2(138),V1(138),V2(138)
      REAL XX(94),YY(94),XXX(94),YYY(94),XG(16),YG(16),XXG
      REAL LP,LS,LE,NP,NS,N,L

C  PLOT OF VERTICAL LINES :

      GMIN=0.
      GMAX=6.
      J=1
      I=1
      XSTEP=1.
      M=1
      XX(1)=0.
      DO 10 M=1,92
      MTEST=IFIX(M/2.)
      TM=FLOAT(MTEST)-M/2.
      IF(TM .EQ. 0.) GO TO 2
      YY(M)=GMIN
      XSTEP=10.**(J-1)
      XX(M)=ALOG10(XSTEP*I)*10./5.
      I=I+1
      IF(I .EQ. 10) GO TO 3
      GO TO 10
    3 J=J+1
      I=1
      GO TO 10
    2 YY(M)=GMAX
      XX(M)=XX(M-1)
   10 CONTINUE
      DO 20 I=1,92
      YYY(I)=YY(I)
   20 XXX(I)=XX(I)
      M=3
      DO 30 I=1,23
      XXX(M)=XX(M+1)
      XXX(M+1)=XX(M)
      YYY(M)=YY(M+1)
      YYY(M+1)=YY(M)
   30 M=M+4
```

```
C  PLOT OF HORIZONTAL LINES :

      KA=1
      DO 60 I=1,7
      XG(KA)=0.
      XG(KA+1)=10.
   60 KA=KA+2
      DO 70 I=1,14
   70 XXG(I)=XG(I)
      MA=3
      DO 80 I=1,3
      XXG(MA)=XG(MA+1)
      XXG(MA+1)=XG(MA)
   80 MA=MA+4
      YSTEP=(GMAX-GMIN)/6.
      IA=1
      DO 90 I=1,7
      YG(IA)=GMIN+YSTEP*FLOAT(IA-1)
      YG(IA+1)=YG(IA)
   90 IA=IA+2

      CALL PLOTS(0,0,92)
      CALL FACTOR(.5)
      CALL PLOT(.5,.5,-3)
      CALL SCALE(XXX,10.,92,1)
      CALL SCALE(YYY,6.,92,1)
      CALL LINE(XXX,YYY,92,1,0,14)
      CALL SCALE(XXG,10.,14,1)
      CALL SCALE(YG,6.,14,1)
      CALL LINE(XXG,YG,14,1,0,14)
      XI=-0.1
      F=1.
      DO 50 I=1,6
      CALL NUMBER(XI,-.2,.1,F,0.,0)
      XI=XI+10./5.
   50 F=F*10.
      CALL SYMBOL(4.,-.4,.15,'FREQUENCY (HZ)',0.,14)
      CALL SYMBOL(0.,7.40,.15,'LAG COMP.',0.,9)
      CALL SYMBOL(0.,7.20,.15,'CHANGE FAC',0.,10)
      CALL SYMBOL(0.,7.00,.15,'FAC=.004--.064',0.,14)

C  POWER STAGE PARAMETERS :

      NP=22.
      NS=10.
      LP=40.E-06
      LS=LP*NS**2/NP**2
      N=300.
      VI=23.
```

```
      VO=5.2
      RC1=.07
      CO1=450.E-06
      RL=1.69
      RS=.013
C     DO 300 II=1,2
      DO 200 IT=1,5
      D=0.35
      DP=1.-D
      T=1./5.E+04
      RE=RS/DP**2
      LE=LS/DP**2
      W1=SQRT(1./(LE*CO1))
      ZE=(W1/2.)*(LE/RL+(RE+RC1/DP)*CO1)

C  CONTROL LOOP PARAMETERS :

      R1=10.5E+03
      R2=1.E+03
      C1=1.E-07
      R3=4.42E+03
      C2=1.E-07
      RP2=53.6

      K=0
      M=0
      DO 100 J=1,6
      WINC=1.*10.**(J-1)
      DO 100 I=1,27
      K=K+1
      P=(2.+FLOAT(I))/3.
      W=P*WINC*2.*3.14159
      S=CMPLX(0.,W)
      DELTA=(S**2+2.*ZE*W1*S+W1**2)/W1**2

C  TRANSFER FUNCTIONS :

      FD1=VO*(-S**2*D*RC1/(RL*W1**2)+S*(RC1*CO1-D*LE/RL)+1.)/
     *(D*DP)
      FD2=VO*NS*(S**2*DP/W1**2+S*(2.*ZE*DP/W1+RL*CO1)+2.)/
     *(DP**2*RL*NP)
      FDC=(S*R3*C2+1.)/(S*R1*C2)
      FAC=RP2/N
      FAC=.004*2.**(IT-1)
      FM=2.*LP*DP/(T*VI*FAC*(DP-D))

C  SYSTEM OPEN LOOP :
      G=FM*(FD1*FDC+FD2*FAC)/DELTA
```

```
      V1(K)=20.*ALOG10(CABS(G))
      THETA=ATAN2(AIMAG(G),REAL(G))*57.3
      V2(K)=THETA
      X(K)=ALOG10(W/(2.*3.14159))*10./5.
      IF(K .EQ. 1) GO TO 5
      V=V2(K)-V2(K-1)
      V=ABS(V)
      IF(V .LT. 330.) GO TO 5
      IF(V2(K) .GT. 0.) GO TO 4
      V2(K)=V2(K)+360.
      GO TO 5
    4 V2(K)=V2(K)-360.
    5 Y1(K)=V1(K)
      Y2(K)=V2(K)
      IF(K .EQ. 136) GO TO 101
  100 CONTINUE

  101 CALL PLOT(0.,0.,-3)
      IF(IT .NE. 1) GO TO 102
C     CALL SCALE(X,10.,136,1)
C     CALL SCALE(Y1,6.,136,1)
C     Y1(137)=-20.
C     Y1(138)=20.
C     CALL AXIS(0.,0.,19HOPEN LOOP GAIN (DB),19,6.,90.,Y1
C    *Y1(138))
C 102 CALL LINE(X,Y1,136,1,0,14)
      CALL SCALE(X,10.,136,1)
      CALL SCALE(Y2,6.,136,1)
      Y2(137)=-200.
      Y2(138)=40.
      CALL AXIS(0.,0.,21HOPEN LOOP PHASE (DEG),21,6.,90.,Y2
     *Y2(138))
  102 CALL LINE(X,Y2,136,1,0,14)
  200 CONTINUE
C 300 CONTINUE
      CALL PLOT(0.,0.,999)
      STOP
      END
```

```
C  PROGRAM II
C  COMPUTER PROGRAM FOR ROOT LOCUS : .

      REAL X(5),Y(5),AR(100),MK1,MK2,MK3,MK4,MK5
      REAL LP,LS,NP,NS,N,L,LE
      COMPLEX Z(3)

C  POWER STAGE PARAMETERS :

      NP=22.
      NS=10.
      LP=40.E-06
      LS=LP*NS**2/NP**2
      N=300.
      VI=23.
      VO=5.2
      RC1=.07
      CO1=450.E-06
      RC2=.21
      RL=1.69
      RS=.013
      D=0.35
      DP=1.-D
      T=.2E-04
      RE=RS/DP**2
      LE=LS/DP**2
      W1=1./SQRT(LE*CO1)
      ZE=(W1/2.)*(LE/RL+(RE+RC1/DP)*CO1)

C  CONTROL LOOP PARAMETERS :

      R1=10.5E+03
      R2=1.E+03
      C1=.1E-06
      R3=4.42E+03
      C2=.1E-06
      RP2=53.6

      K=0
      DO 100 I=1,5
      FAC=RP2/N
      FAC=.004*2.**(I-1)

      NDEG=3
      MK1=(1./(RL*W1**2))*(FAC*NS/NP-R3*RC1/R1)
      MK2=CO1*(FAC*NS/(DP*NP)+(R3/(D*R1))*(RC1-D*LE/(RL*CO1)-
     *D*LE*RC1/(RL*R3*C2)))
      MK3=2.*FAC*NS/(DP*RL*NP)+(1./(D*R1*C2))*(RC1*CO1-D*LE/R
     *+R3*C2)
```

```
      MK4=1./(D*R1*C2)

      AR(1)=MK1
      AR(2)=MK2
      AR(3)=MK3
      AR(4)=MK4
      AR(5)=MK5
      CALL ZPOLR(AR,NDEG,Z,IER)
      DO 60 M=1,3
      WRITE(6,*) Z(M)
      K=K+1
      X(K)=REAL(Z(M))
      Y(K)=AIMAG(Z(M))
   60 CONTINUE
  100 CONTINUE

      CALL PLOTS(0,0,10)
      CALL FACTOR(.5)
      CALL PLOT(.5,.5,-3)
      CALL SCALE(X,10.,3,1)
      CALL SCALE(Y,6.,3,1)
      X(4)=-35.E+03
      X(5)=35.E+03
      CALL AXIS(0.,3.,4HREAL,-4,10.,0.,X(4),X(5))
      Y(4)=-3.
      Y(5)=1.
      CALL AXIS(1.,0.,4HIMAG,-4,6.,90.,Y(4),Y(5))
      CALL LINE(X,Y,3,1,-1,1)
      CALL SYMBOL(0.,7.40,.15,'AC LOOP ZEROS'
     *,0.,13)
      CALL SYMBOL(0.,7.20,.15,'FAC=.02-.1',0.,10)
      CALL PLOT(0.,0.,999)
      STOP
      END
```

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SOME DESIGN CONSIDERATION OF SWITCHING REGULATOR USING CURRENT-INJECTED CONTROL

by

Tsu-Houng Lee

(ABSTRACT)

Open-loop stability analysis of multi-loop current-injected switching regulator is performed using a small signal model containing a power stage, an error processor and a duty cycle pulse modulator. Two design constraints and the effects of various critical control circuit parameters are pinpointed and the analysis-based design guidelines are established in order to optimize the switching regulator performances.

In addition, an external ramp slope is proposed to obtain the optimal performance and eliminate the 50% duty cycle instability when operated in constant frequency mode. The effects of the second stage output filter are also examined.