3D Commutation-Loop Design Methodology for a Silicon Carbide Based Matrix Converter run in Step-up mode with PCB Aluminum Nitride Cooling Inlay

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(ABSTRACT)

This work investigates three-dimensional power loop layout for application to a SiC based matrix converter, providing a symmetric, low-inductance solution. The thesis presents various layout types to achieve this design target, and details the implementation of a hybrid layout to the matrix converter phase-leg. This layout is more easily achievable with a surface-mount device package, which also offers benefits such as ease in manufacturing, and a compact package. In order to implement a surface-mount device, a PCB thermal management strategy should be utilized. An evaluation of these methods is also presented in the work. The final power loop solution that implements an aluminum nitride inlay is evaluated through simulated parasitic extraction and experimental double pulse tests. The layout achieves small, symmetric loop inductances. Finally, the full power, three-phase matrix converter demonstrates the successful implementation of this power loop layout.

3D Commutation-Loop Design Methodology for a Silicon Carbide Based Matrix Converter run in Step-up mode with PCB Aluminum Nitride Cooling Inlay

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(GENERAL AUDIENCE ABSTRACT)

In the United States, 40% primary energy consumption comes from electricity generation, which is the fastest growing form of end-use energy. Industries such as commercial airlines are increasing their use of electric energy, while phasing out the mechanical and pneumatic aircraft components, as they offer better performance and lower cost. Thus, implementation of high efficiency, electrical system can reduce energy consumption, fuel consumption and carbon emissions [1]. As more systems rely on this electric power, the conversion from one level of power (voltage and current) to another, is critical.

In the quest to develop high efficiency power converters, wide bandgap semiconductor devices are being turned to. These devices, specifically Silicon Carbide (SiC) devices, offer high temperature and high voltage operation that a traditional Silicon (Si) device cannot. Coupled with fast switching transients, these metal oxide semiconductors field effect transistors (MOSFETs), could provide higher levels of efficiency and power density.

This work investigates the benefits of a three-dimensional (3D) printed circuit board (PCB) layout. With this type of layout, a critical parasitic – inductance – can be minimized. As the SiC device can operate at high switching speeds, they incur higher di/dt, and dv/dt slew rates.

If trace inductance is not minimal, overshoots and ringing will occur. This can be addressed by stacking PCB traces on top of one another, the induced magnetic field can be reduced. In turn, the system inductance is lowered as well. The reduction of this parameter in the system, reduces the overshoot and ringing.

This particular work applies this technique to a 15kW matrix converter. This converter poses a particular design challenge as there are a large number of devices, which can lead to longer, higher inductance PCB traces. The goal of this work is to minimize the parasitic inductance in this converter for high efficiency, high power density operation.

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Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Aircraft AC-AC Conversion Needs

In the United States, 40% primary energy consumption comes from electricity generation, which is the fastest growing form of end-use energy. Commercial airlines are increasing their use of electric energy, while phasing out the mechanical and pneumatic aircraft components, as they offer better performance and lower cost. Aircraft like the Boeing 787 and Airbus 380 exemplify this increased demand in aviation for electric aircraft [1].

Included in this electric aircraft architecture in the need for AC-AC (Alternating Current) power generators and motors drives. 40% of total electricity demand in the United States arises from the industrial drives for these motors. Thus, implementation of high efficiency, variable frequency drives can reduce energy consumption by 10-30%. Other benefits incurred by the use of electrical systems include reduction in fuel consumption and carbon emissions [1].

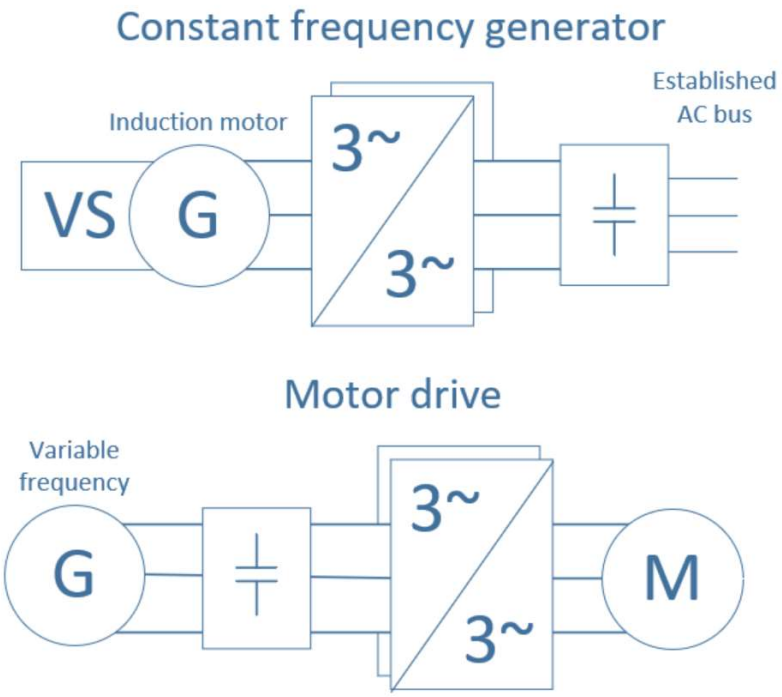


Figure 1.1 Block diagrams of applications for 3-Phase AC-AC Converters

1.2 AC-AC Converter Topologies

There are three categories that can be used to describe converter types under the umbrella of AC-AC conversion. The categories are converters with DC-link (Direct Current-link) storage, matrix converters, and hybrid matrix converters. Ref. [3] defines a matrix converter (MxC) as a forced commutated AC-AC converter that does not require an intermediary energy storage element in the power circuit as an essential function. This topology can be split into direct and indirect converters. On the other hand, DC-link converters, like voltage DC-link back-to-back converter (V-BBC) and the current DC-link back-to-back converter (C-BBC), implement a transitional capacitor or inductor, respectively. The hybrid matrix converter combines the basic matrix converter and the V-BBC topologies. Like the matrix converter, this topology can be categorized by direct and indirect converters.

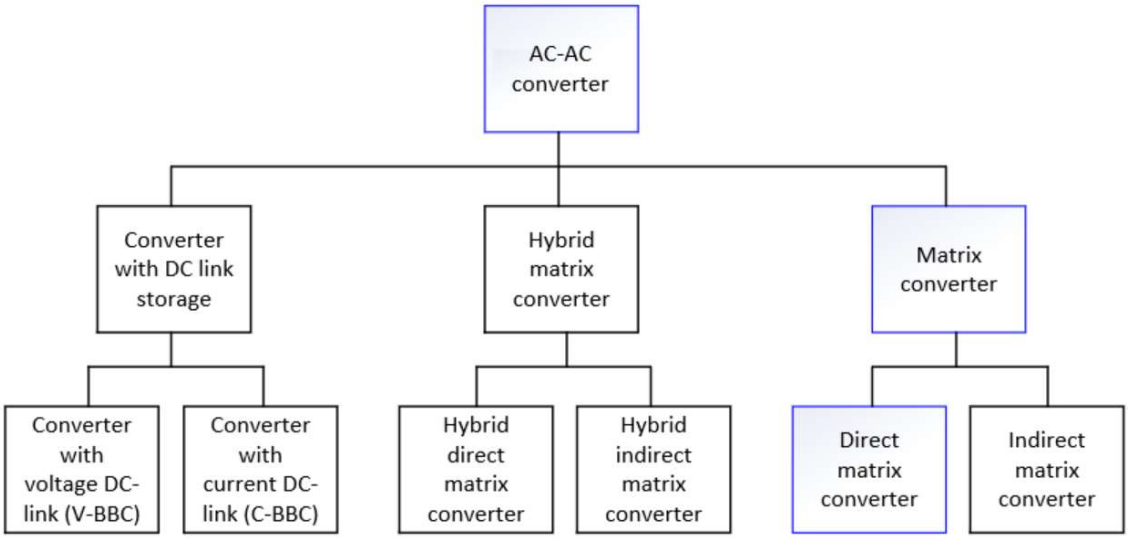


Figure 1.2 Categorization of AC-AC converter topologies

Refs. [2]-[4] compare the merits of the various DC-link direct matrix converter topologies based on metrics such as component number and area, efficiency across frequency, EMI (Electromagnetic Interference) filter size, and total weight of converter. Out of the circuits reviewed, the standard industry solution is the voltage back-to-back converter. It has precedence in the industry and is well established.

On the other hand, matrix converters, while heavily researched over the past 20 years, have not had significant market penetration due to this hurdle. Yaskawa offers an industrial Matrix drive, the U1000 series, which is rated up to 600kW [5]. The MxC does not allow for control of the input currents independent of the output currents, unlike the back-to-back converter. Another concern of the matrix converter is that, when operating in a step-down mode, the output voltage is limited to 86.6% of the input voltage. However, the matrix converter can offer lower semiconductor losses with an increase in switching frequency when compared to the V-BBC. The MxC also offers a smaller passive component volume, including EMI input filter, than the back-to-back converter. The matrix converter must offer benefits in terms of cost, size, and reliability to overtake the V-BBC converter in the market. The matrix has potential benefits

to be utilized as a high-power dense converter for aerospace applications with the implementation of SiC MOSFETs [12].

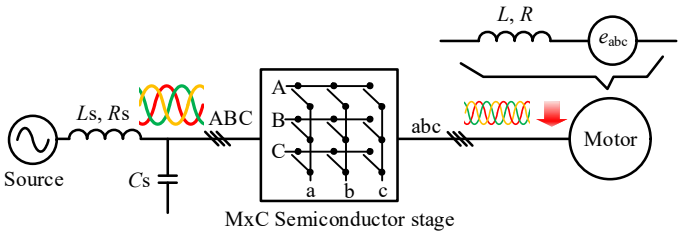
1.3 Introduction to the MxC

1.3.1 Matrix Converter Circuitry

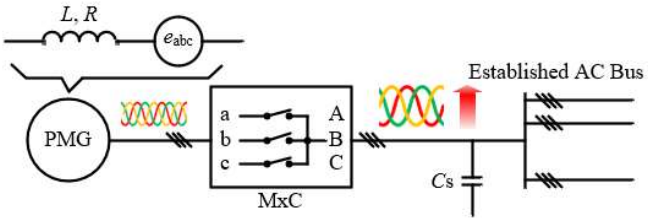
The matrix converter is an AC-AC converter that utilizes an array of controlled semiconductor switches to directly connect an m-phase voltage source to an n-phase load. Many of the desirable traits demanded of power frequency changers can be fulfilled by the matrix converter. It is simple and compact, it generates load voltage with arbitrary amplitude and frequency, has sinusoidal input and output currents, can operate at unity power factor for any load, and bidirectional power flow.

The converter can be implemented in a step-up or step-down configuration. As stated previously, the step-down configuration is limited to an 86% voltage gain. Most literature implements this arrangement, seen in Refs. [6]-[10]. This configuration is flipped from the conventional step-down configuration as shown in Fig. 1.3. The peak to peak output voltage

cannot be more than the minimum voltage difference between two input voltage phases in the configuration [9][11]. The voltage step-up mode avoids this limitation.



a.



b.

Figure 1.3 Block diagram of matrix converter in (a) step-down mode and (b) step-up mode configurations

The most practical configuration uses a 3x3 switch array with no DC link to perform AC-AC conversion, as seen in Fig. 1.4. While many AC-AC converters implement this DC link making the converter design bulky, complex, less efficient and with a shorter lifetime [13]. The direct conversion addresses these shortfalls and only requires small filters, with small volume energy storage components, to suppress ripple from switching action [14]. A key element to the MxC is the fully controlled bidirectional switches. There is interest in utilizing these capabilities, and increased research work has brought this converter closer to industry use in motor drives, renewable generation, grid interface and unified power flow controllers [13][14].

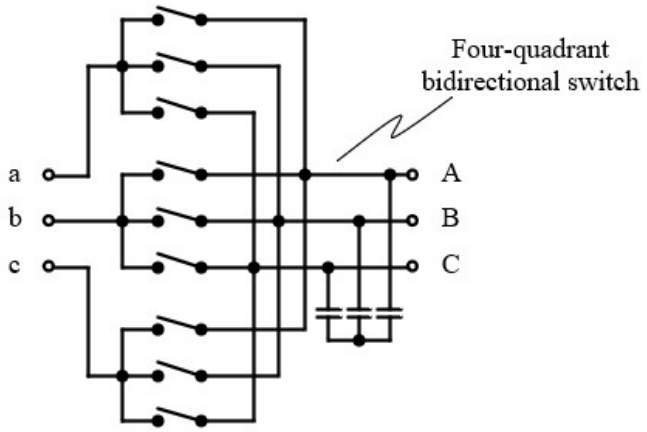


Figure 1.4 Diagram of three-phase to three-phase matrix converter topology

1.3.2 Switching Basics and Modulation

Nine switches make up the 3x3 matrix converter. Their switching action is dictated by two constraints: the voltage side (input) terminals cannot be shorted together and the current side (output) connections cannot be open. Using the following notation:

$$S_{Kj} = \begin{cases} 1, & Switch\, S_{Kj}\, closed \\ 0, & Switch\, S_{Kj}\, open \end{cases} \quad K = \{A, B, C\}, j = a, b, c \tag{1.1}$$

the constraints can be expressed by Equation 1.2.

$$S_{Aj} + S_{Bj} + S_{Cj} = 1, \quad j = \{a, b, c\} \tag{1.2}$$

Given the constraints, there are 27 valid switching combinations. Using the switch matrix, S, and the transpose of the switch matrix, S^T, the instantaneous relationships between the input and output voltages and currents are shown.

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ba} & S_{Ca} \\ S_{Ab} & S_{Bb} & S_{Cb} \\ S_{Ac} & S_{Bc} & S_{Cc} \end{bmatrix} \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} = \mathbf{S} \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} \tag{1.3}$$

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \mathbf{S}^{\boldsymbol{T}} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{1.4}$$

To accomplish this switching, bidirectional switches are needed [12][13].

1.3.3 Switching Cells

The main requirement of the matrix converter is the ability to block voltage and conduct current in both directions. As there are no devices that meet this need, discrete devices are used to make up switch cells, as seen in Fig. 1.5.

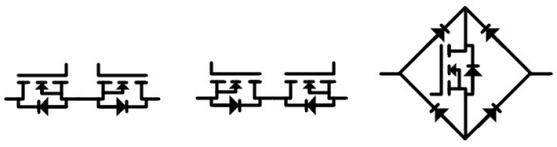


Figure 1.5 Bidirectional switch cell arrangements: (a) common-source configuration, (b) common-drain configuration, (c) diode bridge

With discrete semiconductors, there are three possible configurations to make this cell. The first methods are the common-source configuration, 1.5a, which connects the sources of the two devices, and the common-drain, 1.5b, that joins the drain connections. Both methods consist of two diodes and two IGBTs (insulated gate bipolar transistor) and their common connector provides benefits to the transients during switching. The last arrangement is the diode bridge bidirectional switch cell 1.5c. This method centers the IGBT within a single-phase diode bridge. The advantage of the diode bridge arrangement is that both current directions are carried by one switching device, and therefore only one gate driver is needed per cell. But, losses are high as three devices make up the conduction paths. Also, the direction of the current cannot be controlled, which is required of advanced communications methods. Both the common-source and the common-drain have smaller conduction losses; only two devices make up the conduction

paths. Unlike the diode bridge, the direction of the current can be controlled in these cases. The common-source configuration is generally the preferred switch cell make-up, due to constraints, namely the requirement to minimize stray inductances [12][13]. This configuration also is preferable for lower controller-side noise.

1.3.4 Phase-leg Commutation of Matrix Converter

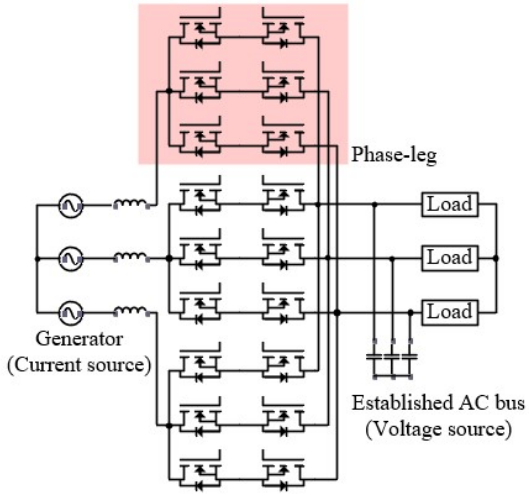


Figure 1.6 Circuit diagram of matrix converter topology with highlighted phase-leg

The switching cell creates one bidirectional switch, and each phase-leg contains three of these switches, as seen in Fig. 1.6. The three switches then make up three commutation loops and the current travels within each phase-leg via these loops; Fig. 1.7 illustrates this. In the matrix converter, these loops influence each other, and must be balanced for system operation.

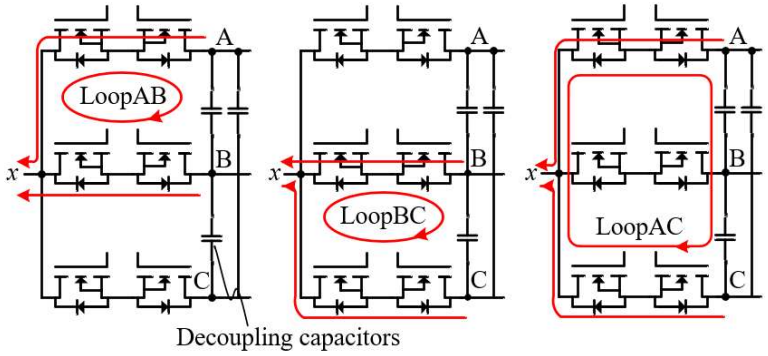


Figure 1.7 Circuit diagram of commutation loops within a three-phase matrix converter phase-leg

As stated above, the device configuration implemented is the common-source. This arrangement is illustrated by a typical bidirectional device-based circuit unit in Fig. 1.8(a). The left side of the setup is considered as the voltage source and the right side as the current source. In bidirectional switches multistep commutation must be used to avoid a short circuit of the voltage source or an open circuit of the current source. Fig. 1.8(a) depicts this multistep commutation, for both current (top) and voltage (bottom) commutation. As the current commutates from the top branch, blue, to the bottom branch, bottom, the gating signals are described in Fig. 1.8(b). Through the process the signals are changed from "1100" to "0011" for devices S_{Aa1}, S_{Aa2}, S_{Ba1}, and S_{Ba2} respectively. Given that v_{AB} and i_a have positive polarity, the transition from top to bottom branch occurs at different point in the commutation process. In current commutation this change occurs in the 3rd step out of four, whereas it occurs in the 2nd step in voltage commutation.

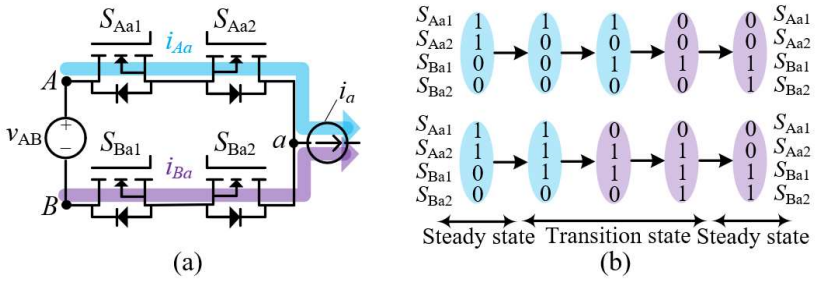


Figure 1.8 Commutation from one phase to another given that v_{AB} and i_a have positive polarity

In order to describe the switching transient circuit, the notations 'active', 'synchronous', and 'auxiliary' devices are defined. Again, assuming that $v_{AB} > 0$, and $i_a > 0$, S_{Aa1} is called the 'active' device as its change in gate signals dictates the current change, independent of the type of commutation used. The S_{Ba2} device is referred to as the 'synchronous' device in reference to conventional unidirectional circuits. The remaining devices, S_{Aa2} and S_{Ba1}, are named the 'auxiliary' devices, as they just provide the needed current paths without voltage change in the switching action. It should be noted that the bidirectional-device-based switching transient analysis is only relevant when the gating signal of the active device changes. The auxiliary and synchronous devices only move current between the channel and the body diode within the same device; there is no high voltage or current slew rate involved.

1.4 Silicon vs Silicon Carbide Devices

1.4.1 Benefits of Silicon Carbide

Silicon devices have material limits that prevent these devices from meeting demands like high frequency, high voltage, and high temperature operation [14][15]. Si devices tend to have high on-resistances at high voltages, causing massive increases in losses [14][15]. The possible switching frequency of silicon devices is also limited, due to the turn off current tail,

and high efficiency of Si devices beyond 900V is not feasible. Therefore, wide bandgap devices are being turned to in order to address these issues [14].

Wide-bandgap (WBG) materials, like silicon carbide and gallium nitride, have become more available in recent years. These materials have bandgaps greater than 1.7eV meaning they have higher energy gaps, breakdown electric fields, thermal conductivity, melting points, and electron velocities [16][18]. These qualities allow the devices made from WBG materials to operate at higher voltages, switching frequencies, and temperatures than Si [16][17][18]. Silicon carbide devices are suited for high voltage, high power operation, in the 600 V, kW or above range, but the lower range of this, 400 V to 1700 V, is more widely available commercially [18].

Silicon Carbide also provides low losses; the on-resistance of wide bandgap devices is lower due to the thin blocking layer and high doping concentration [17][18]. The resistance is also less variable over temperature in comparison to Silicon [14]. With this decrease in on-resistance, there is a significant decrease in conduction and switching losses, specifically turn off losses, when SiC devices are utilized [14][15][17]. The thermal conductivity of WBG materials is excellent and heat is easily extractable. This quality allows for SiC devices to operate at higher junction temperatures and therefore handle more power [18]. The use of WBG devices also offers higher power density, possible due to high switching frequencies and low conduction losses [14][17][18].

Wide Bandgap devices are being utilized to push matrix converters closer to acceptance in industry. Silicon Carbide devices are ideal for the high density needs of the MxC. The high switching speed and thermal capabilities allow the size of this converter to be minimized. This is a significant benefit to this converter, as the weight and volume are important factors. The

demand for light weight and low volume is high in hybrid electric vehicles and electric aircraft projects, where a large focus is on improving fuel efficiency [17].

1.4.2 Design considerations for Silicon Carbide Solutions

However, there are some considerations to be made when these devices are implemented. The benefit of high slew rates, dv/dts and di/dts, are limited as they can result in resonance and large over-voltages [18]. Care should be taken in gate drive and power loop layouts. Other potential issues include greater EMI emissions, insulation requirements for single devices blocking up to tens of kilovolts, high switching frequencies potentially in the megahertz range, and high junction temperatures over 200° C [18]. Balancing these with the positive qualities can be beneficial for power converters.

1.5 Existing Silicon Carbide Design and Build

The existing three-phase matrix converter design and tests were created and performed by Dr. Boran Fan and Dr. Qiong Wang [19][20].

1.5.1 Phase-leg Design

A preliminary SiC matrix converter is designed, built, and shown below in Fig. 1.9. The phase-legs are contained in each vertical PCB, along with a motherboard. The base of the fixture which connects the inputs and outputs via the phase-legs. It also contains the current and voltage sensors.

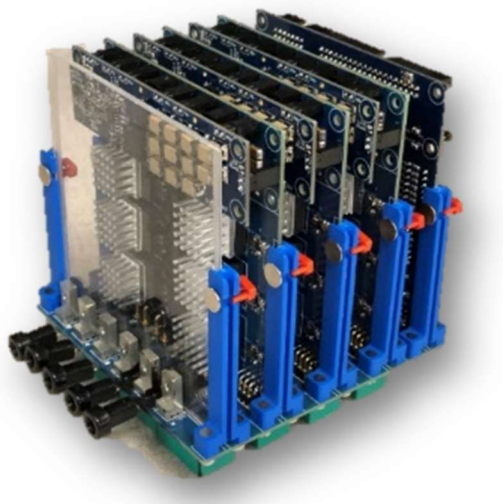


Figure 1.9 Preliminary SiC matrix converter build

Fig. 1.10 shows the individual phase-leg, with the dump circuit attached on top. On the top view of the phase-leg, the MOSFETs are contained, with individual heat sinks affixed. The bottom of the board holds the respective power supply and gate driver. This is detailed in Fig. 1.11. This converter implements the Cree C3M0030090K device in a TO-247-4 package. The device has four connections, the Drain, Source, Driver Source, and Gate. The driver source is a Kelvin connection, while the source connects to the power loop. This connection and back-to-back layout minimize path length and gate loop parasitics. It also reduces the interaction between the power and gate loops.

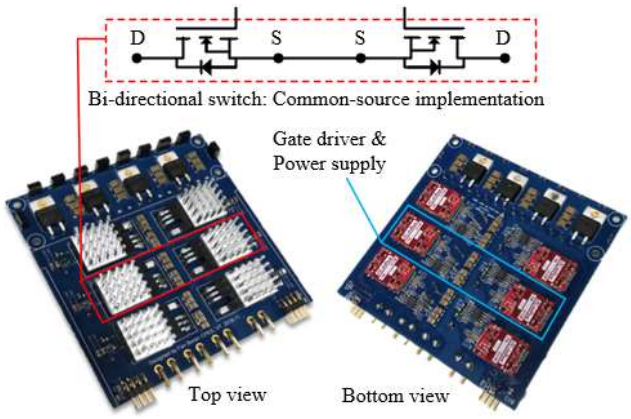


Figure 1.10 Phase-leg of preliminary hardware with highlighted bidirectional switch

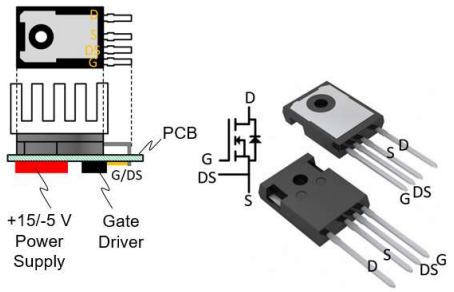


Figure 1.11 Arrangement of implemented SiC MOSFET, gate driver, and power supply

Fig. 1.12 displays the PCB layout of this phase-leg. Each commutation loop is outlined by the white arrows. The devices within one switch are intuitively placed across from the other, shortening the path length between the two. Still, this layout is unbalanced: one loop has a longer path length, and thereby incurs more parasitics than the other two.

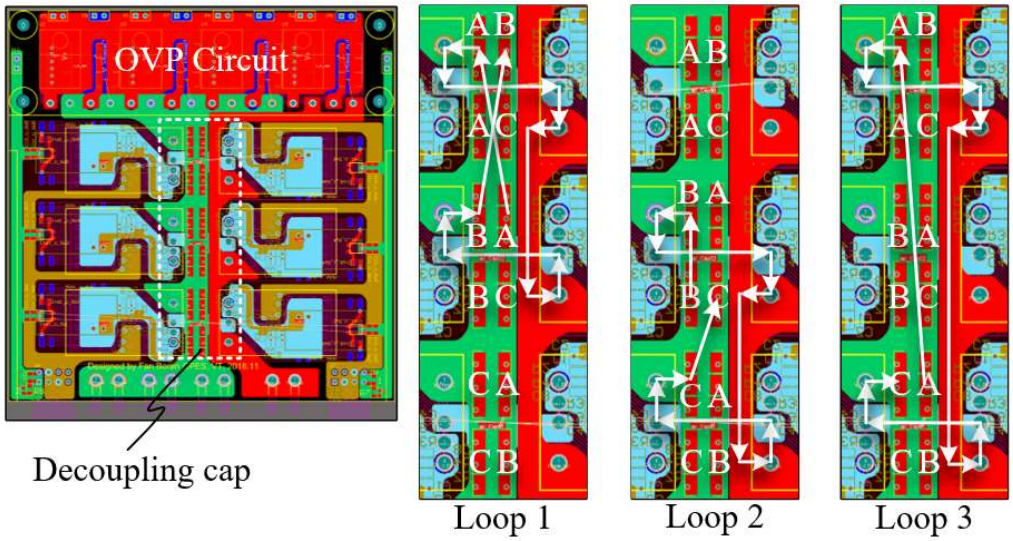


Figure 1.12 PCB Layout of preliminary phase-leg with outlined commutation loops

Table 1.1 Simulated AC inductance of phase-leg commutation loops

	AC Inductance (10MHz)
	L_{ac} [nH]
Power Loop 1	12.504
Power Loop 2	12.557
Power Loop 3	17.69

This can be illustrated through Finite Element Analysis (FEA) of the PCB traces. Table 1.1 displays the AC inductance at 10 MHz results of the simulation. This is simply the inductance of the PCB traces, the equivalent series resistance and inductance of the devices is not included. Again, the phase-leg loops are not symmetrical; loops 1 and 2 have about 5 nH less inductance than loop 3. Also, in general, due to the long length of the PCB traces, the loop inductances are high.

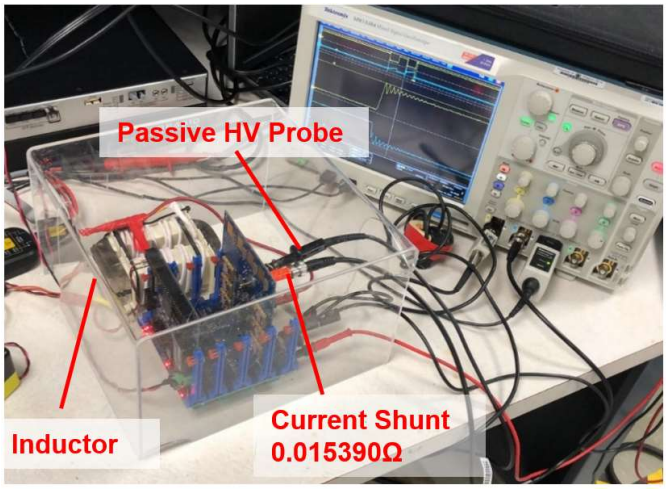


Figure 1.13 Double pulse test setup for matrix converter phase-leg

1.5.2 Phase-leg Validation

This design is then validated using a double pulse test (DPT), the setup of which is shown in Fig. 1.13. This test reveals the transient performance and the effect of the respective loop parasitics. Fig. 1.14 shows the circuit diagram and test board of an example single-phase-leg DPT. The setup shows a test of the AB loop, the Phase C devices, S_{Ca1} and S_{Ca2}, are kept off. S_{Aa1} is the active device and is switched on and off. Both S_{Aa2} and S_{Ba1} are kept on, while S_{Ba2} is kept off to provide the necessary current paths during switching. To test the AC loop the Phase A device states are unchanged, and the Phase B devices are kept off. The Phase C devices, S_{Ca1} and S_{Ca2}, are on and off respectively. This test setup does not allow for the measurement of the BC loop. Measurements of the switched voltage and switched current are taken with a passive high voltage probe and a current shunt respectively.

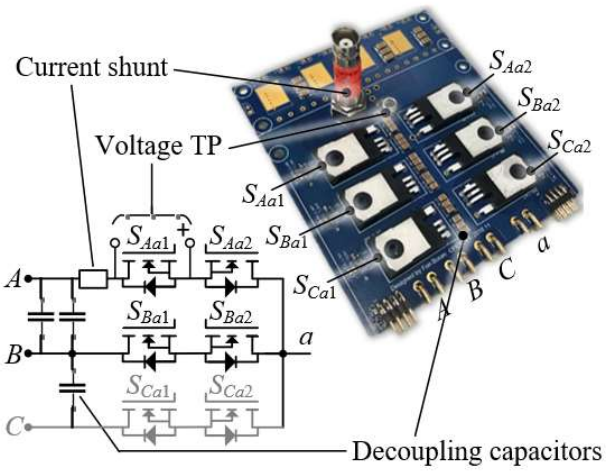


Figure 1.14 Single-phase-leg board for double pulse test

These DPTs are run at a DC voltage of 600V and output current of 42A and 25A. These results are shown in Fig. 1.15 the turn off of the system on the left and the turn on is on the right.

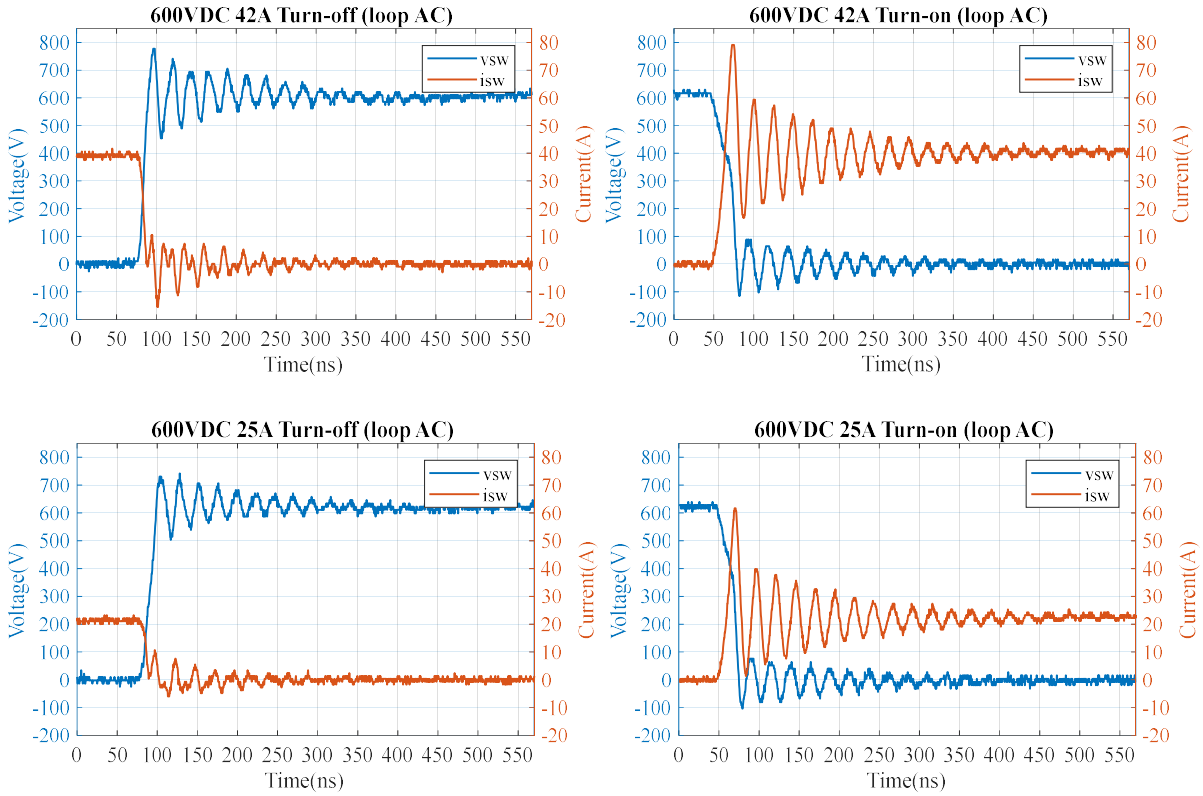


Figure 1.15 Double pulse test results (a) 600V 42A Turn off, (b) 600V 42A Turn on, (c) 600V 25A Turn off, (d) 600V 42A Turn on

The 42A turn off has a voltage overshoot of 192V, which is 32% of the final voltage, while the 25A turn off has a voltage overshoot of 100V, which is 17% of the final voltage.

The large amount of loop inductance is made evident by the amount of ringing in the DPT transients. The ringing arises from both the PCB traces and the leads of the through-hole device package. The traces and leads are long, with little inductance cancellation. High amounts of ringing incur higher switching losses, affecting the efficiency and performance of the system. The asymmetry of this phase-leg design is also observed in the comparison of results between the AB commutation loop and the AC commutation loop at a 35A condition, shown in Fig. 1.16.

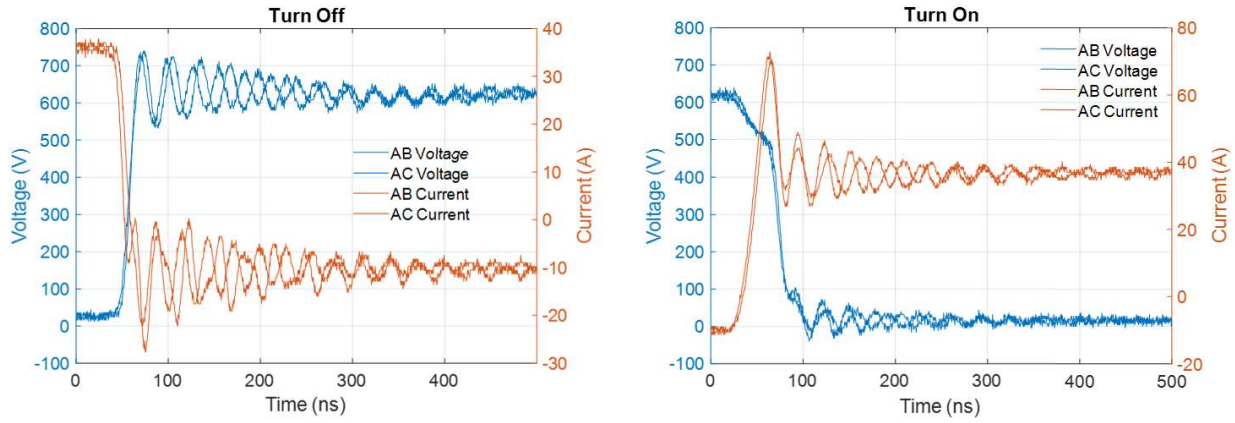


Figure 1.16 Double pulse test comparison between phase-legs

The ringing in the waveforms is mis-matched. Symmetry is crucial to the performance of the matrix converter. Asymmetric operation leads to uneven device stresses which can hurt the converter efficiency [21].

1.5.3 Motivation for Phase-leg Redesign

There are several issues with this preliminary matrix converter layout. First, there are high levels of parasitic inductances in the power loop leading to ringing and higher losses. This emerges from two factors; the long, lateral PCB traces lead to the high loop inductance. The

through-hole device also introduces parasitics of its own. The long leads of this type of device contributes to the systems inductance as well. Not only is there high inductance in the system, the inductance of the commutation loops is asymmetric.

The motivation of this work is to redesign the matrix converter phase-leg to address these issues to create a high-density, high-efficiency three-phase to three-phase solution. Surface mount devices are the first implemented change to address the high package parasitics of through-hole devices.

Chapter 2

Surface Mount Devices

2.1 Introduction

This chapter discusses the benefits and challenges of surface mount device (SMD) package implementation. A survey on SiC devices is conducted, and a device is chosen to address design needs outline in the previous chapter.

2.2 Benefits of Surface Mount Devices

Surface mount devices offer many benefits for a low inductance PCB layout. In general, these devices have smaller package inductances than their through-hole device counterparts [22][23]. In comparisons between the TO-247, a through hole device, and the TO-263, a surface mount device, in [23] the TO-263 package displayed a 32% lower drain-source inductance than the TO-247 package. The empirical results of [23] indicate a 29% reduction in total per-cycle switching losses with the TO-263. Common-source inductance, which is crucial to reduce as it is shared by both the power and gate loops, is also smaller in surface mount packages [22][23]. In [22], the through-hole device packages TO-247, TO-220, and I-PAK were compared to the surface mount packages D2-PAK, D-PAK, SOT-223, and SOT-23. The paper found that the surface mount packages studied had common-source inductances ranging from 1nH to 6nH, compared to 3nH to 8nH for the through-hole devices. The long through-hole device leads contribute to the high common-source inductance of the package [24]. Other benefits of surface mount devices include ease of 3D layout, and reduced manufacturing costs. Surface mount devices allow this 3D layout as the inner layers are not interrupted by the device leads. Stacked

layouts utilizing these inner layers provide inductance cancellation that can produce a low parasitic system design.

2.3 Considerations for Surface Mount Devices

However, there are some considerations that should be made for surface mount devices, primarily the thermal management of the package. It is difficult to mount heat sinks to surface mount devices, unlike through hole devices. Therefore, the heat must travel through the PCB, and a high thermal resistance will overheat the device [23][25]. In order to implement these devices, cooling strategies must be considered. Chapter 6 details this discussion. Also, at the time this survey was conducted, there were minimal numbers SiC devices offered in surface mount packages.

Table 2.1 SiC Device survey [26]-[30]

	Device	**Blocking Voltage**	**R_{dson}**	**Current Rating (@ 25°)**	**Package**
1	Cree C3M0030090K	900V	30mΩ	73A	TO-247-4
2	Cree C3M0016120K	1200V	16mΩ	115A	TO-247-4
3	United SiC UF3C120040K4S	1200V	35mΩ	65A	TO-247-4
4	Infineon IMZ120R030M1H	1200V	30mΩ	56A	TO-247-4
5	Microsemi MSC025SMA120S	1200V	25mΩ	89A	TO-268 (D3PAK)

2.4 Device Survey Comparison

Table 2.1 shows the discrete SiC MOSFETs that meet the desired criteria for the MxC phase-legs. Row one displays the characteristics of the Cree C3M0030090K device implemented in the preliminary hardware, detailed in Chapter 1. Devices 2 - 5 above fit these qualities and were available and considered at the time of the P2 design in November of 2019. The devices are

required to have a blocking voltage of 1.2 kV, and a low R_{dson}, ideally at or below 30 mΩ, like the P1 Cree device. The current rating should be at least 50A at 25°C.

Figure 2.1 SiC packages (a) TO-247-4, (b) TO-268

The surveyed SiC Devices are contained in both a through hole package, the TO-247-4, and a surface mount package, the TO-268, in Fig. 2.1ab respectively. As stated above, there was a minimal selection of SiC devices in surface mount packages, and only one that met the desired criteria. The footprint of this TO-268 package is also smaller; at most it is 16.3 mm by 25 mm, occupying an area of 407.5 mm^2. The TO-247-4 package is 17 mm by 30.4 mm, taking up an area of 516.8 mm^2. Relatively, the TO-263 package is 79% of the area that is occupied by the TO-247-4 package.

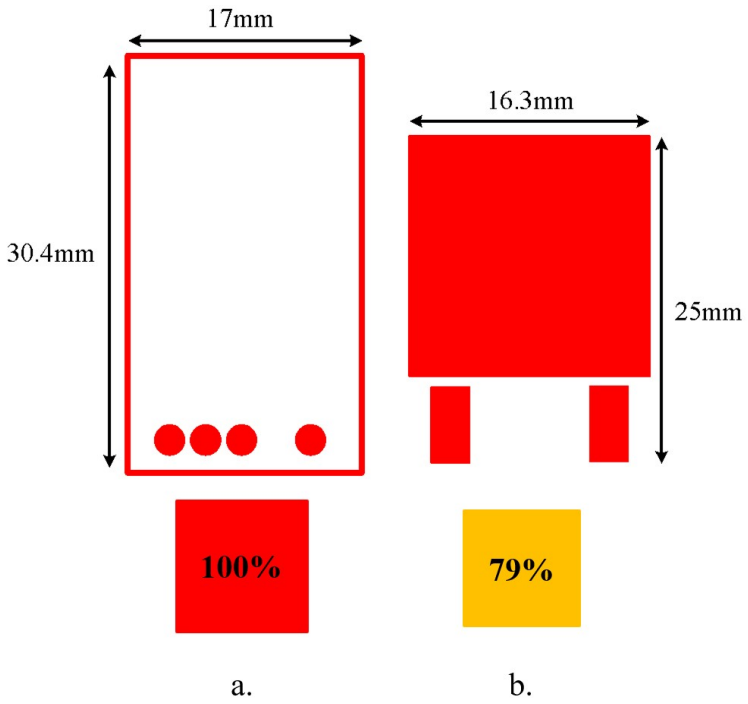


Figure 2.2 SiC package size and area comparison (a) TO-247-4, (b) TO-268

While the TO-247-4 device occupies a larger area, it does however, offer the benefit of a Kelvin source connection. This dramatically lowers the common-source inductance, providing faster switching capabilities. Especially in comparison with the TO-268, that does not have the Kelvin connection, this particular through hole device package has a much lower common-source inductance. Another benefit to the through hole package is its thermal performance. The thermal resistance of the junction to ambient is the same as the junction to case for these devices. However, for surface mount devices, the junction to ambient resistance also includes the PCB as stated above.

2.4.1 Device Selection

Overall, the benefits of the surface mount devices outweigh that of the through-hole devices. Specifically, the layout flexibility and low device parasitics are critical to the phase-leg improvement. This update targets the high loop inductances of the preliminary design, the

implementation of a surface mount device addresses this concern. The Microsemi MSC025SMA120S device is selected and the power loop design is created with this package. The device has a low on-resistance, and acceptable current rating.

2.4.2 Updated Device Survey

Since this original survey in November 2019, more SiC devices are being offered in surface mount packages. The devices in Table 2.2 are available as of April 2021 and meet the needed criteria of the converter. These surface mount packages also offer the benefit of kelvin connections.

Table 2.2 SiC devices secondary survey [31]-[32]

	Device	**Blocking Voltage**	**R_{dson}**	**Current Rating (@ 25°)**	**Package**
1	On Semiconductor NTBG020N120SC1	1200V	20mΩ	98A	D2PAK−7L
2	Infineon IMBG120R030M1H	1200V	30 mΩ	56A	TO263-7

Chapter 3

Matrix Converter Power Loop Redesign

3.1 Introduction

This chapter discusses trace arrangements and layouts to provide magnetic field cancellation and ultimately, low inductance power loops. The total loop inductance and capacitance of a set of PCB traces is calculated, and simulated. Two matrix converter phase-leg layouts are presented for a thermal via and ceramic inlay cooling solution. The ceramic inlay layout is selected, and the power loop design is verified with double pulse testing.

3.2 Layout for Inductance Cancellation

3.2.1 Trace Arrangement

As stated previously in Chapter 1, it is critical to reduce loop inductance in the converter layout to implement SiC devices. This reduces possibilities of high overvoltages and ringing in the system due to potential high current and voltage slew rates of the wide bandgap devices. With the choice of a surface mount package, there is reduction in device parasitics, and the layout inductance must be addressed as well. The target is low, symmetric inductance loops [33]. An effective method to achieve this target is to lay out traces such that magnetic flux cancellation reduces the overall loop inductance.

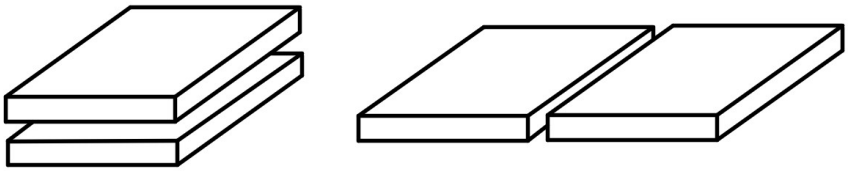


Figure 3.1 Arrangement of conductors (a) vertical, (b) coplanar

Parasitic inductance is caused by the magnetic field around a current carrying path; as current passes through PCB traces, a magnetic field is induced according to Ampere's law. This field gives rise to the trace inductance. If the magnetic field can be cancelled as much as possible, the inductance will be minimized. This is a similar idea to coax cables and twisted pair connectors. To provide this cancellation, there are two placement methods for conductors: the parallel plate layout, where the conductors are stacked vertically, and the coplanar layout, where the plates are placed in the same horizontal plane, side-by-side, illustrated in Fig. 3.1. Both cancel inductance, as they are close together so there is overlap of the magnetic fields. However, there is more overlap in the parallel plate configuration and therefore more magnetic field cancellation [34].

3.2.2 Layout Types

This parallel plate configuration can be leveraged in different PCB layouts, that are compared to a lateral layout, like the preliminary hardware, Fig. 3.2(a). A lateral layout does not overlap traces, they are all on the top of the board. The components of the commutation loop are contained on one side of the board, as well. The trace length dictates the inductance, and there is little magnetic field cancellation, similar to the coplanar arrangement above. One issue with this layout technique is the magnetic field impacts the surrounding components [35].

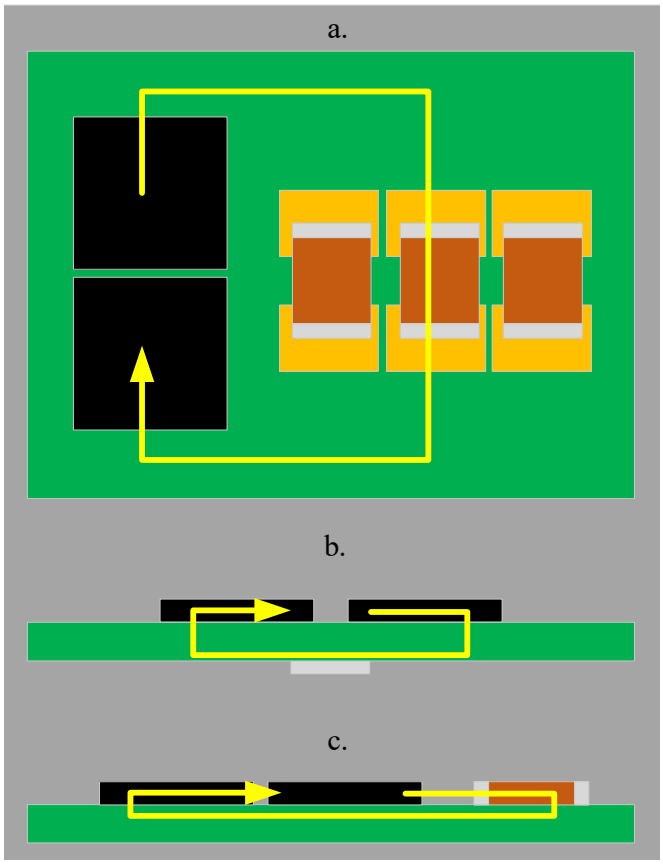


Figure 3.2 Types of PCB Layout, (a) Lateral, (b) Vertical, (c) Hybrid

A layout that utilizes the parallel plate arrangement above is the vertical layout, Fig. 3.2(b). In this arrangement, the device and capacitors are held on opposite sides of the board, one underneath the other. The traces exist on the top and bottom of the board, shortening the length of the loop. The induced magnetic field cancels, reducing the amount of inductance in the power loop. One drawback of this method is the amount of inductance cancellation is limited by the thickness of the PCB. As the number of layers of the PCB increases, the size of the loop, and the loop inductance will increase too [35].

The hybrid layout addresses this shortcoming, Fig. 3.2(c) shows this layout. Instead of placing the return path on the bottom trace, it is placed in the first inner layer. Doing this decouples the loop area from the board thickness. The components are then all placed on the top

of the board. This minimizes the area that contains the power loop, maximizing the magnetic field cancellation, and minimizing the loop inductance. However, the traces in the hybrid layout are longer than that of the vertical layout [35].

3.2.3 Examination of Parallel Plate Inductance and Capacitance [36]

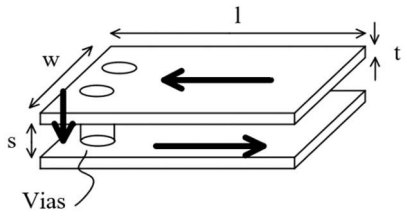


Figure 3.3 Simulated PCB trace layout

The approximate total loop inductance of the parallel plate configuration displayed in Fig. 3.3 can be calculated with Equation 3.1, where l is the length of the traces, w is the width of the traces, s is the distance between the traces, and μ_0 is the permeability of free space. This calculation is performed with the assumption that the depth of the trace, t, is significantly smaller that its length and width.

$$L = \mu_0 \frac{l \times s}{w} \tag{3.1}$$

Table 3.1 Trace dimensions for Simulation

Parameter	**l**	**w**	**t**
Value	25.654mm	10.414mm	0.0696mm

The inductance cancellation effectiveness can then be illustrated by the calculation of the trace setup, the dimensions of which are displayed in Table 3.1. The pitch, s, of the traces is varied to different distances that represent the layers in a 1.6 mm PCB that utilizes 2oz copper.

The parameters A, B, C in Fig. 3.4 are the distances between the bottom layer and the second signal layer, first signal layer, and the top layer respectively.

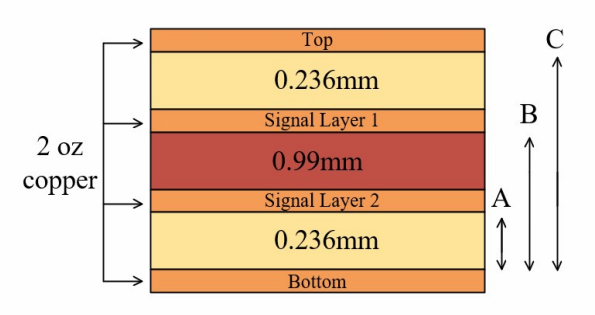


Figure 3.4 1.6mm 4-layer PCB with 2oz copper trace dimensions

Then, the system inductance was simulated with FEA using the same parameters. The results of these calculations and simulations are shown in Table 3.2.

Table 3.2 Parasitic inductance calculation and FEA simulation comparison

	Trace Location		
	Top/Signal 1	***Signal1/Signal2***	***Signal2/Bottom***
Pitch	A	B	C
Calculation	0.73 nH	3.79 nH	4.53 nH
FEA Simulation	0.7 nH	3.21 nH	3.81 nH

As stated previously, when the pitch between the traces is decrease, so is the area of the loop, and the total loop inductance decreases too. This decrease in inductance is somewhat limited by the capacitance between the traces. The closer the traces are, and the more they overlap, the higher the capacitance between them. The capacitance of the traces can be estimated by the following equation. An assumption made in this estimation is that the trace length and width are much larger than the distance between them, which is satisfied by this example setup.

$$C = \varepsilon \frac{A}{D} \tag{3.2}$$

Specifically, capacitance between jumping nodes and quiet nodes should be minimized. For example, in a half-bridge configuration, as seen in Fig 3.5, the output trace is a jumping node, and its overlap with the DC buses, the quiet nodes, should be minimized. This introduced capacitance can lead to additional switching losses. On the other hand, overlap, and therefore capacitance, is beneficial between two quiet nodes, like the positive and negative DC busses. This capacitance stabilizes the DC-link voltage.

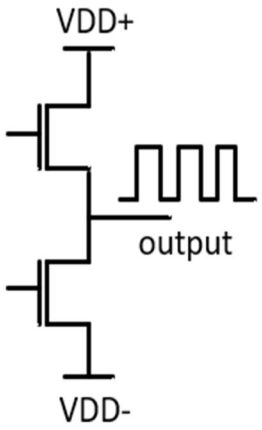


Figure 3.5 Quiet and jumping nodes of a half bridge

Using the equation 3.2, and FEA simulation, capacitance values are calculated and simulated for the trace pitches described in Fig. 3.3.

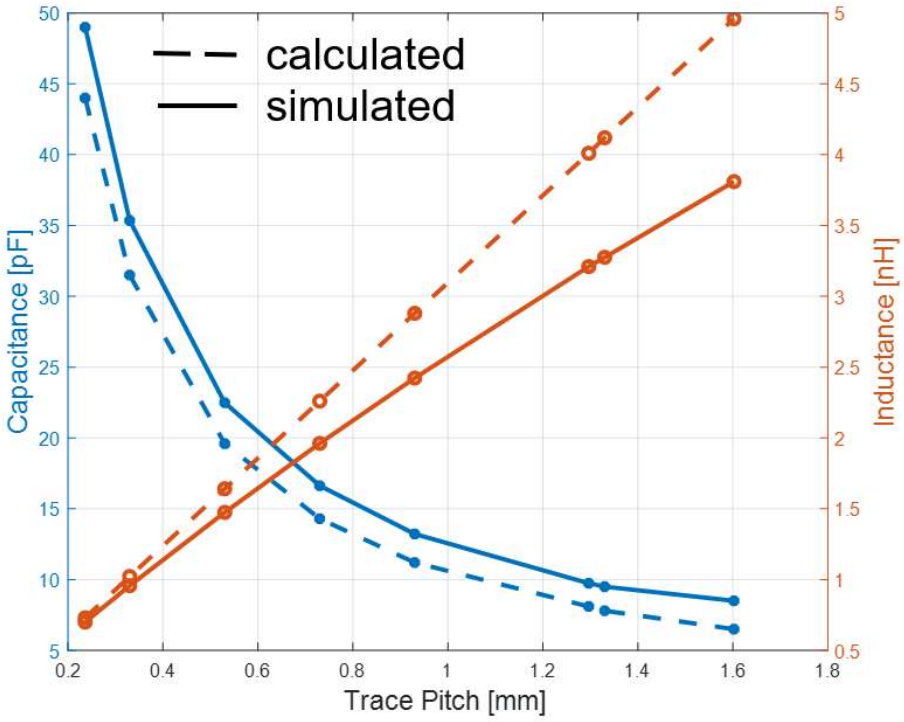


Figure 3.6 Calculated and simulated relationship between trace pitch and the capacitance and inductance

The relationship between separation of PCB traces and their inductance and capacitance are displayed in Fig. 3.6. The dashed lines represent the calculated values, while the full line represents the simulated values. The described inverse relationship of the inductance and capacitance must be balanced for an acceptable design. The amount of capacitance that is negligible must be leveraged to create a low-inductance layout. For this system, this level is determined by the output capacitance of the SiC MOSFET. In Fig. 3.7, the graph of the device output capacitance is shown against the drain-source voltage. At 600V, the standard V_{dc}, the output capacitance is 20 pF. Thus, the capacitance between jumping traces should be limited to 20pF.

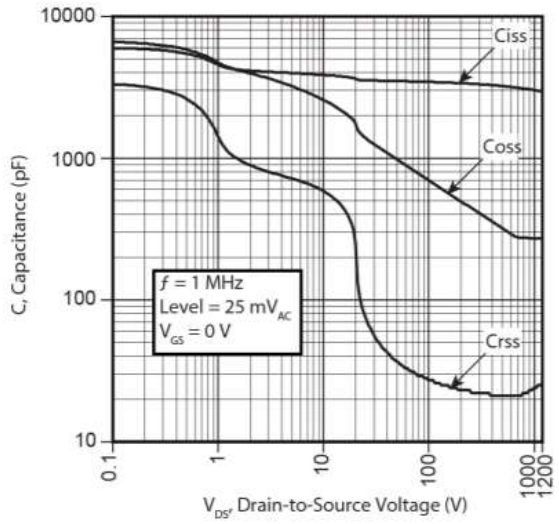


Figure 3.7 Relationship between device drain-to-source voltage and capacitance

3.3 Implementation of Inductance Cancellation in Matrix Converter Phase-leg Design

While utilizing inductance cancellation techniques while leveraging the amount of overlap and thereby induced capacitance, the following layouts are designed and evaluated. Two designs are made based on an aluminum nitride (AlN) ceramic inlay and thermal via heat dissipation strategies. A discussion on surface mount thermal management solution is contained in Chapter 6. Thermal vias and the ceramic inlay solutions provide the best thermal performance while allowing for inductance cancellation. The power loop layout is informed by the heat dissipation strategy. It is crucial to investigate this impact, as the power loop layout for the SiC Matrix Converter is critical to the converter performance.

3.3.1 Device Placement for Symmetric Power Loops

Both heat dissipation method layouts have the same device placement. To achieve the symmetric loop inductances the path length of each loop must be similar. For the lengths to be totally equal, the devices in a phase-leg would have to be in a three-pointed star configuration, as

seen in Fig. 3.8a, with each branch separated by 120°. However, this arrangement does not lend itself to a high-power dense design. To address this, one point of the star can be rotated up next to the second, whilst the third leg is shifted under the other two legs. This layout is displayed in Fig. 3.8b. Trace overlap and inductance cancellation are possible with this arrangement with the return paths of the loops contained in the bottom and middle layers.

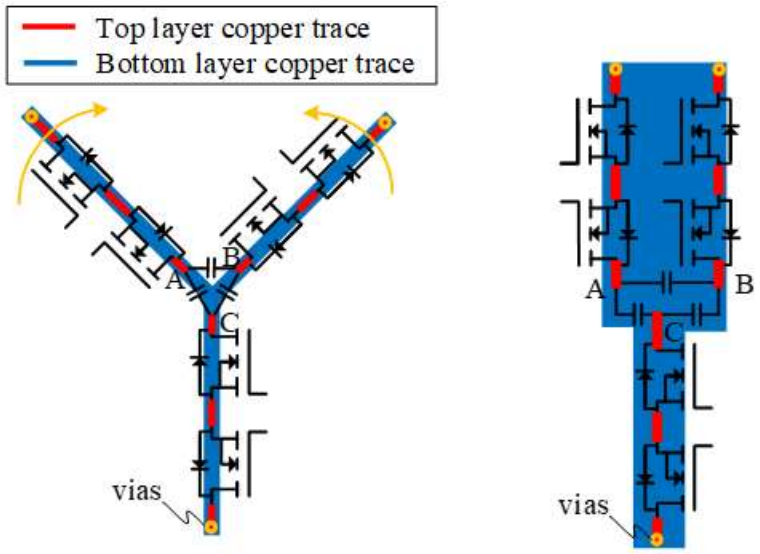


Figure 3.8 Device placement for symmetric path lengths and high power density

The established AC bus traces for each phase and the respective decoupling caps are located in the center of this arrangement. The branches of the arrangement hold the bidirectional switches which are connected with top layer copper traces. At the “points” of the arrangement vias connect these points through a bottom layer trace which is an input generator phase. The layout cross-sectional area should be minimized to achieve the most inductance cancellation. Three of these phase-legs make up the full converter.

3.3.2 Matrix Converter Phase-leg Layout for Thermal Via Heat Dissipation Method

Figure 3.9 displays a layer-by-layer PCB layout for the thermal via cooling method. The yellow arrows show the paths of the loops in the top and first middle layers, with the return path held in the second middle layer. A restriction imposed by the cooling method can be seen in the bottom layer, it must be shorted to the top layer. This contains the layout to the top, and inner layers. Also because of necessary shorted bottom layer, there is much more capacitance in the system. This severely limits the allowed area of the return path, increasing the resistance and inductance. The 3rd inner layer, in blue, illustrates this; The path must be small underneath the MOSFETs and the respective copper with different voltage potentials. This results in a simulated capacitance of 22 pF.

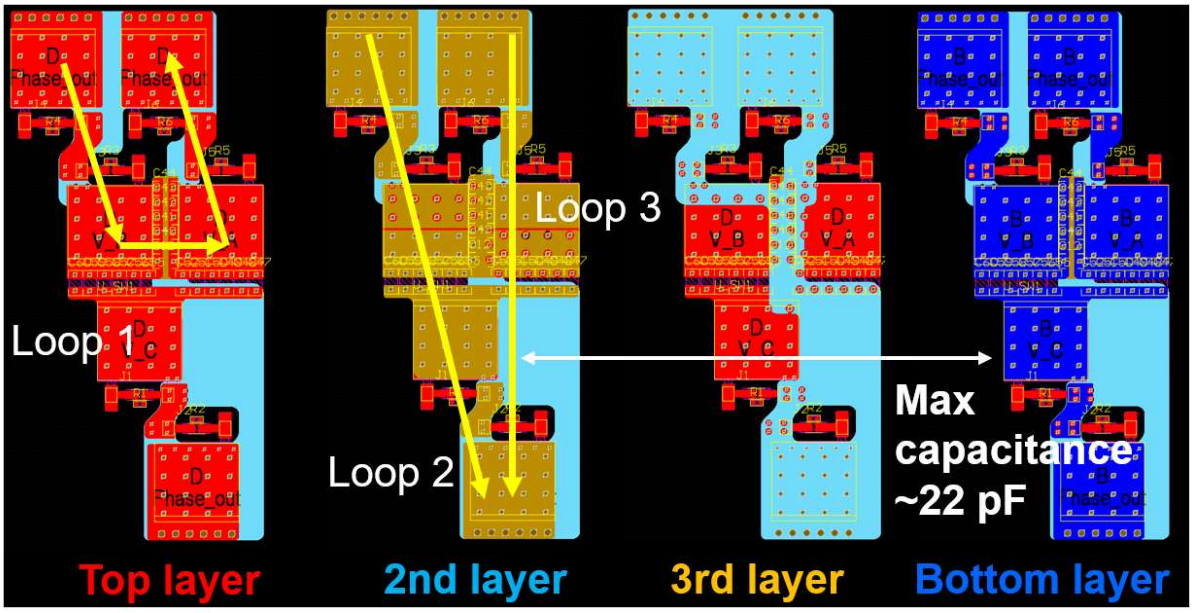


Figure 3.9 Layer-by-layer PCB layout of matrix converter phase-leg with thermal via heat management

Copper must also be removed around these vias on the inner layers, also restricting the area and further increasing the resistance and inductance of each loop. While more vias decrease the thermal resistance, there is less available area for the layout of the inner copper layers. This will increase the loop impedances. Fig. 3.10 shows a side view of the layout with a marked commutation loop. The yellow shading indicates the area of trace overlap, which should be

minimized. When the traces are placed closer together, there is a smaller bounded area and more magnetic field cancellation. This area is small as the light blue return path is held in an inner layer of the board. However, as stated above, the return path width is limited, as is the potential for inductance cancellation.

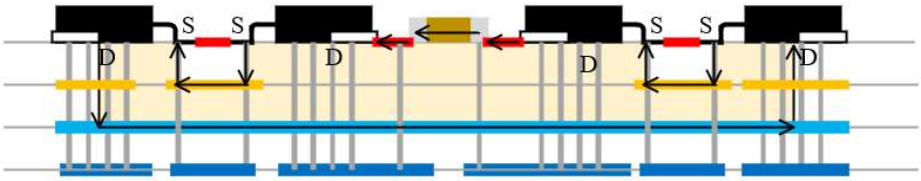


Figure 3.10 Side view of matrix converter phase-leg with thermal via heat management with outlined commutation loop

This layout was analyzed using an FEA simulation to determine the AC inductance at 10 MHz of each loop. The results of the PCB layout inductance simulation are displayed in Table 3.3. The inductance of two loops is similar, but still high at around 11 nH. The third, while much lower at 6 nH, is not symmetric with the first two loops. The long, skinny return path length of the second and third loops raises the inductance of those loops.

3.3.3 Matrix Converter Phase-leg Layout for Ceramic Inlay Heat Dissipation Method

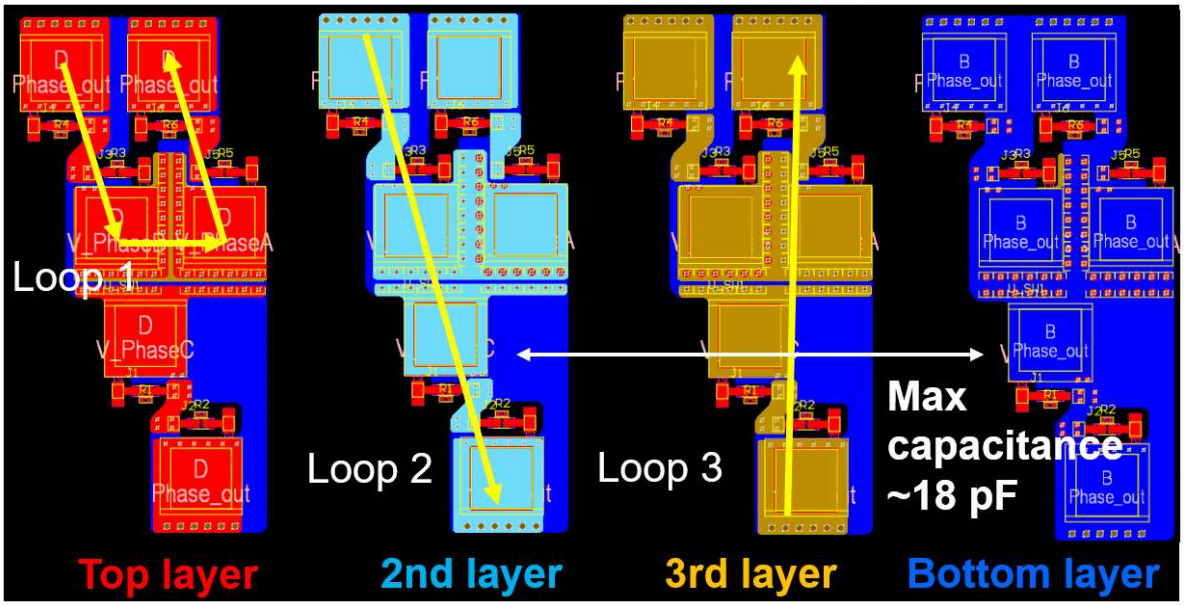


Figure 3.11 Layer-by-layer PCB layout of matrix converter phase-leg with ceramic inlay heat management

Fig. 3.11 shows the layer-by layer PCB layout for the AlN ceramic inlay heat dissipation method. Again, the yellow arrows show the commutation loops. Unlike the thermal vias, the layout has no layer restriction and can exist in all four layers on the board. However, space must be left under the devices for the ceramic block, no copper can be placed in these areas in the inner layers. This is noted by the red outlines in the figure. The traces are placed around the ceramic insert, which does reduce the amount of copper but also the amount of overlap, and thereby unwanted capacitance. The return path of the loops is thus not limited by this capacitance. The larger area of this return path increases the amount of inductance cancellation. Fig. 3.12 shows the cross-section of this layout, with a marked commutation loop. While the loop area is bounded by the top and bottom layers, the AlN inserts reduce this area. The traces around these inserts are close together and the parasitic inductance will be canceled.

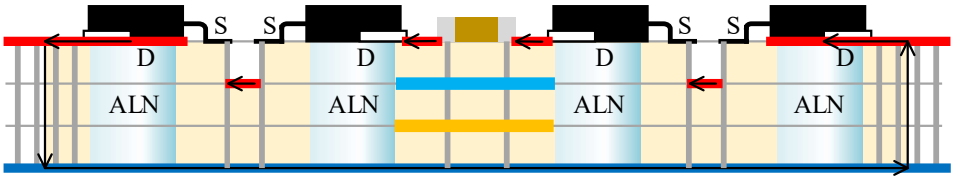


Figure 3.12 Side view of matrix converter phase-leg with ceramic inlay heat management with outlined commutation loop

This is seen in the FEA simulation, the results of which are shown in Table 3.3, displaying the AC inductance of the PCB traces at 10MHz. All of the loops are both symmetric and have a low inductance, around 5nH. The unwanted capacitance is simulated to be 18 pF, which is acceptable for this design.

Table 3.3 Comparison of AC loop inductance between thermal via and ceramic inlay heat management strategies

Thermal Solution	**AC Loop Inductance**		
	Loop AB	***Loop AC***	***Loop BC***
Thermal Via	6.4 nH	11.2 nH	11.9 nH
AlN Insert	4.7 nH	6.4 nH	5.9 nH

3.4 Ceramic Inlay Phase-leg Build [36]

The layout provided by the ceramic inlay cooling method is preferable to that of the thermal vias. This design has symmetric, low inductance commutation loops, minimal unwanted capacitance and will lend itself to a power dense solution. A single-phase-leg board, Fig. 3.13, is fabricated to verify the power loop layout through double pulse testing.

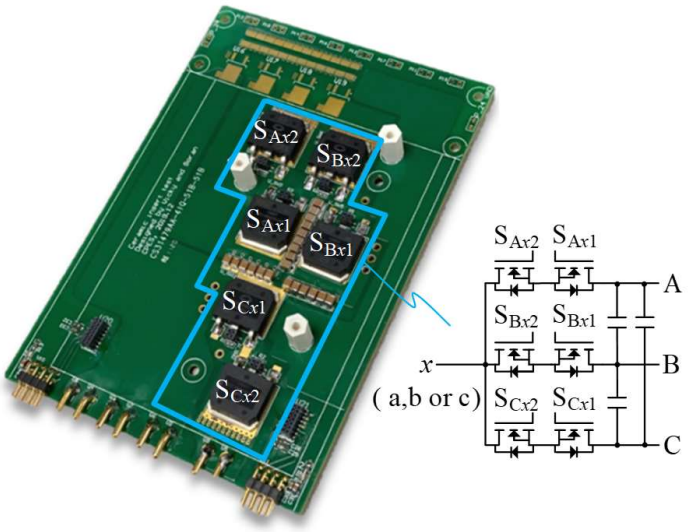
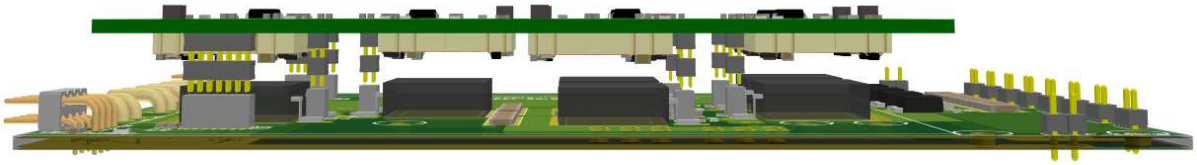


Figure 3.13 Matrix converter single phase-leg PCB with ceramic inlay cooling

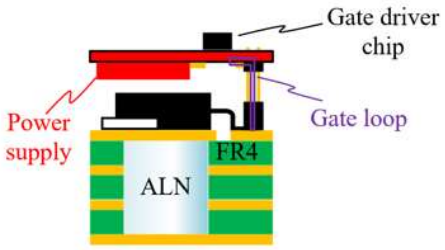
3.4.1 Gate Driver Board Design

A gate driver board sits on top of the power board as illustrated in Fig. 3.14a. The separation of the power and gate loops is crucial to accomplish. Overlap causes unwanted interaction, and higher common-source inductance which can be detrimental to system performance. The gate loop of each MOSFET is shown in Fig. 3.14(b).

The gate driver board contains the gate drivers for each MOSFET and the needed power supplies, the Si8271 from Silicon Labs and MGJ1D241505MPC from Murata respectively. The gate driver has high di/dt immunity and a low propagation delay. The driver has a high-side output terminal and low-side output terminal which are connected to the turn on and turn off gate resistors. These components sit close to the board-to-board connectors to minimize the gate loop. The gate resistors dictate the switching speed of the device, with maximum tested values of 4.7Ω.



a.



b.

Figure 3.14 Single-phase-leg test board (a) Side view (b) single MOSFET gate loop

3.4.2 Power Loop Design Verification through Double Pulse Test

The DPT setup is shown in Fig 3.15. It consists of the single-phase-leg power board and its gate driver board, an inductive load, and the controller interface. Measurements are taken in three places: the voltage across the switched device, the current on the complementary device, and the output current. The pulse tests can further verify the symmetry of the commutation loops. The tests below were run at a DC bus of 600V, an output current of 45A on the top and 25A on the bottom, with a turn on gate resistors of 4.7 ohms, and turn off gate resistor of 2.2 ohms. The AB loop shown in blue, the AC loop is shown in black, and the BC loop is shown in red. The three commutation loops match well, and thus they are symmetric. The turn off overshoot for the 45A case is 726V, which is 21% over the DC bus. For the 25A case, there a maximum voltage is 710V, which is a 18.3% overshoot.

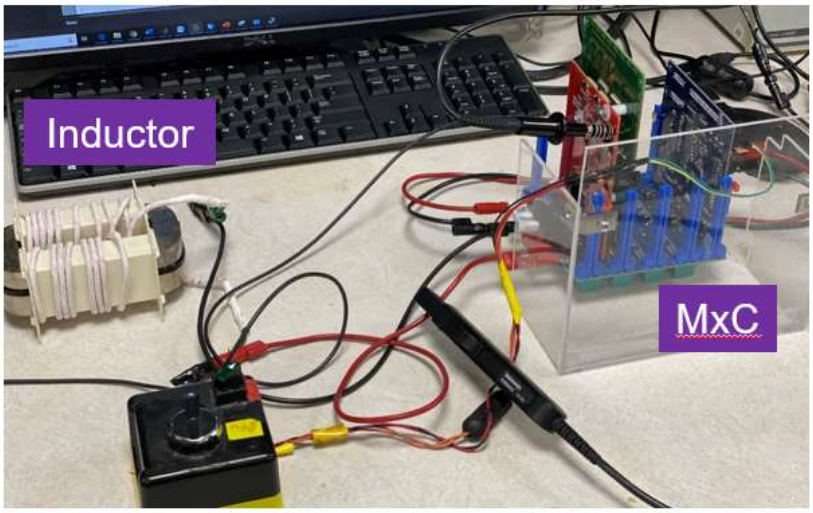


Figure 3.15 DPT Setup for matrix converter single-phase-leg

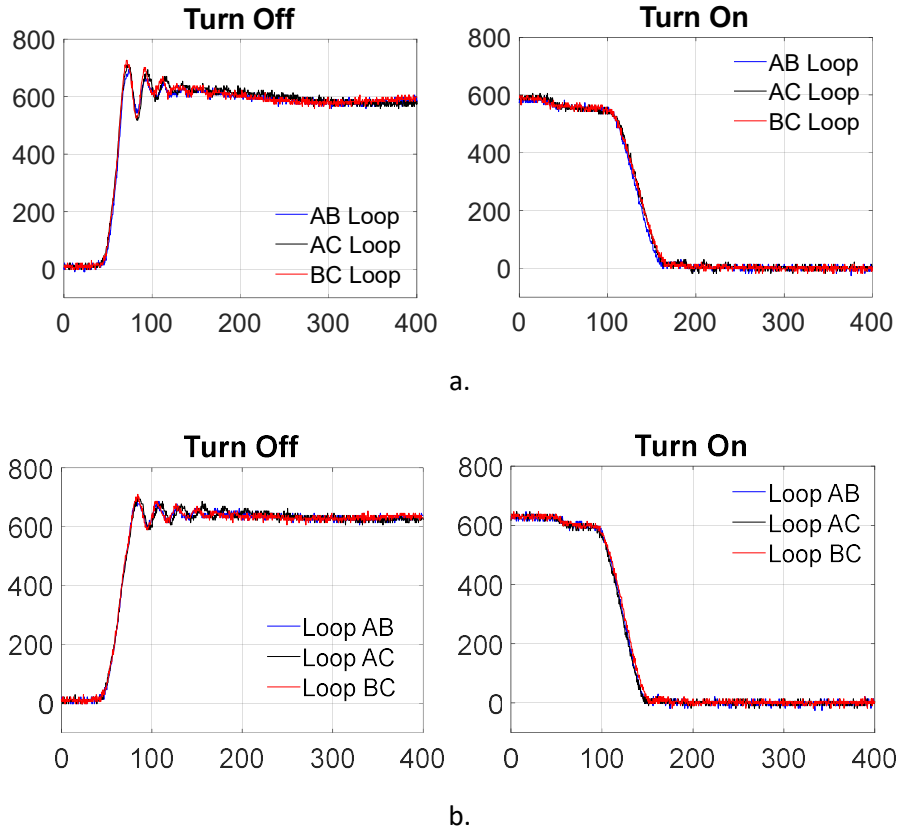
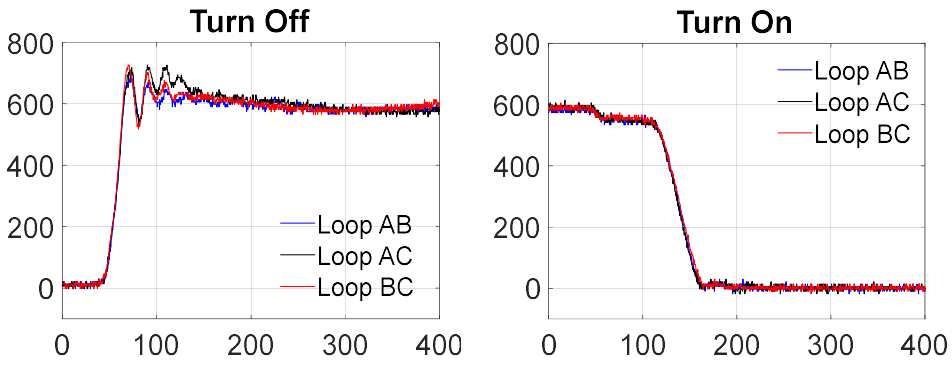
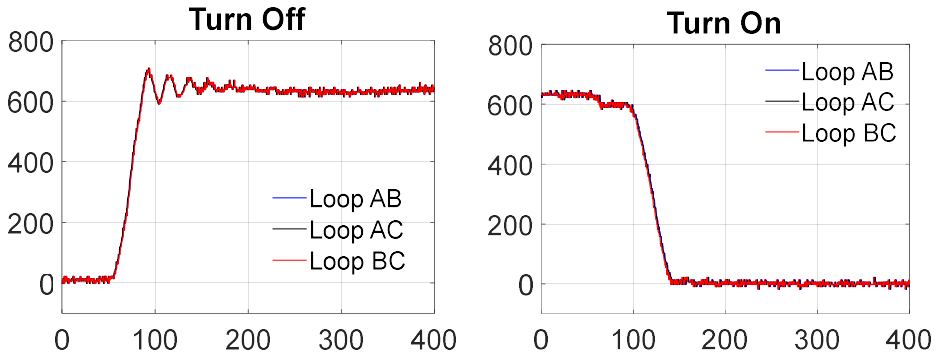


Figure 3.16 Double Pulse Test Results for Updated Power Loop Layout with a turn on resistor of 4.7 ohms and a turn off resistor of 4.7 ohms for (a) 45A, (b) 25A output current



a.



b.

Figure 3.17 Double Pulse Test Results for Updated Power Loop Layout with a turn on resistor of 2.2 ohms and a turn off resistor of 4.7 ohms for (a) 45A, (b) 25A output current

The turn on gate resistor is lowered to 2.2Ω. Fig. 3.17 shows the results of these tests, the 45A case on the top, and the 25A case on the bottom. Again, the symmetry of the commutation loops is observed. The waveforms have little ringing. There is an overshoot of 718V, a 19.7% overshoot, for the 45A case. In the 25A case there is a 18.3% overshoot of 710V. The gate resistors can continue to be lowered, however, at low gate resistor values and high current values a voltage overshoot phenomenon is observed. The overshoot is investigated in Chapter 5.

Chapter 4

Three-phase Integration of Matrix Converter Phase-leg

4.1 Introduction

This chapter details the integration of the single-phase power loop layout to the three-phase matrix converter design. The three-phase matrix converter design and tests were performed with Dr. Boran Fan. First, the design of both the power board and the controller board are discussed. The thermal management of the converter is then converter. Finally, experimental verification of the converter performance is presented for full power operation and thermal tests.

4.2 Three-Phase Integration

The three-phase matrix converter build is shown in Fig. 4.1; it has a rated power of 15 kVA, volume of 1 L, weight of 750 g and a power density of 15 kW/L and 20 kW/kg.

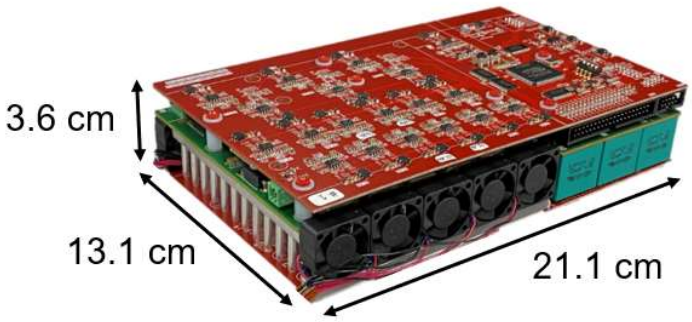


Figure 4.1 Revised Three-Phase to Three-Phase matrix converter build

4.2.1 Power Board

The configuration, like the single-phase-leg build, consists of two boards stacked one top of another. Fig. 4.2 shows the components contained in the power board, in green. This board

contains the phase-legs of the converter, one outlined in blue, on the top of the board. The voltage and current sensors also sit on top of the board, as well as part of the dump circuit. The other part of the dump circuit is contained on the bottom of the power board, along with the EMI filter choke and capacitor. Finally, the heat sink is attached under the power MOSFETs with thermal interface material (TIM).

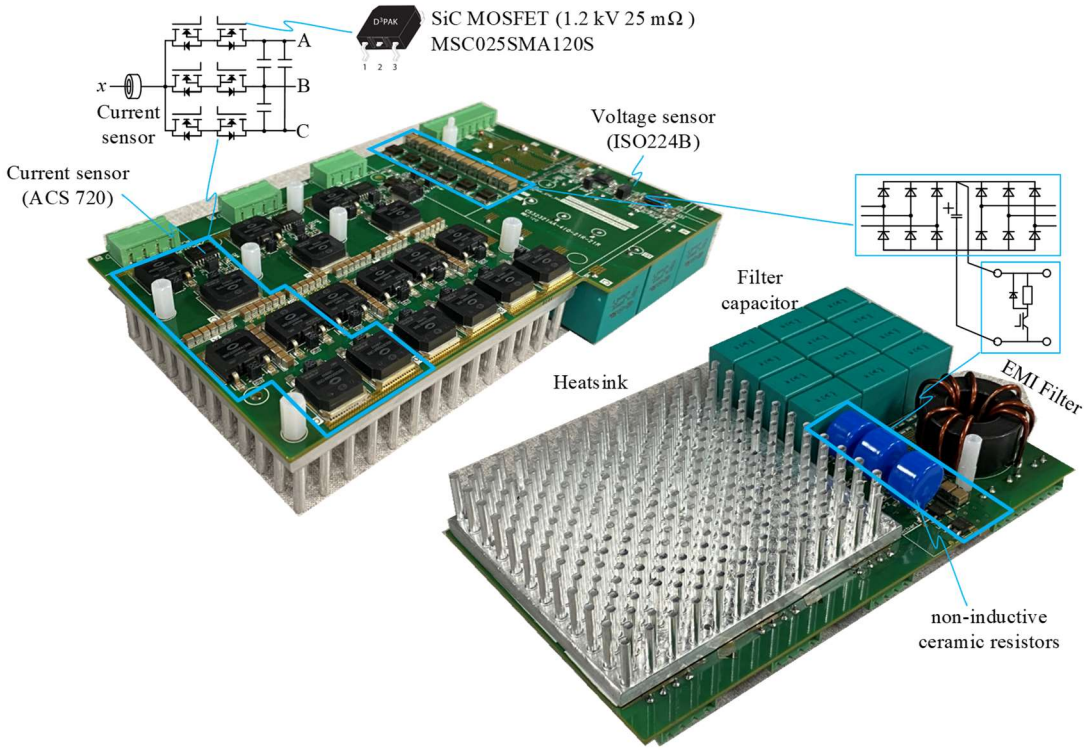


Figure 4.2 Three-phase to three-phase matrix converter power board component breakdown

Fig. 4.3 shows the layout of this power board. The purple blocks show the locations of the AlN inserts. The inputs and outputs are located along the bottom of the board. The power flows from the bottom left board connectors, through the phase-legs, filter, and out of the connector on the bottom left.

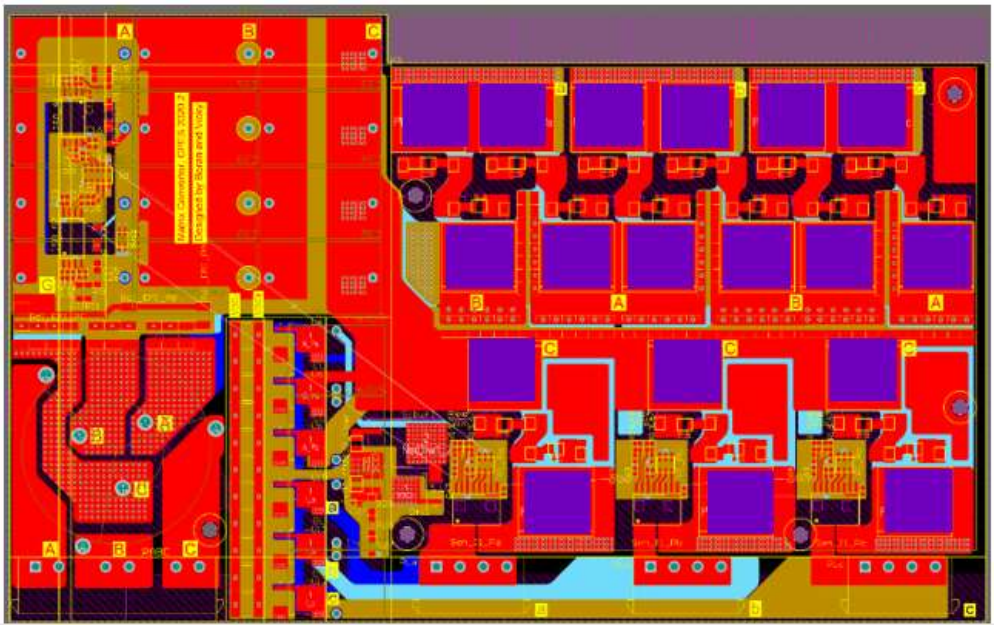


Figure 4.3 Power board layout with marked AlN inlays

4.2.2 Controller Board

The controller board, shown in Fig. 4.4, contains the microcontroller (MCU), control for the crowbar circuit, connectors to the rapid control prototyping (RCP) system, and the 18 gate drivers and respective power supplies for the corresponding MOSFETs on the power board. As with the single-phase configuration, the power supply and gate driver chip also sit above the MOSFET attached with board connectors forming the gate loop.

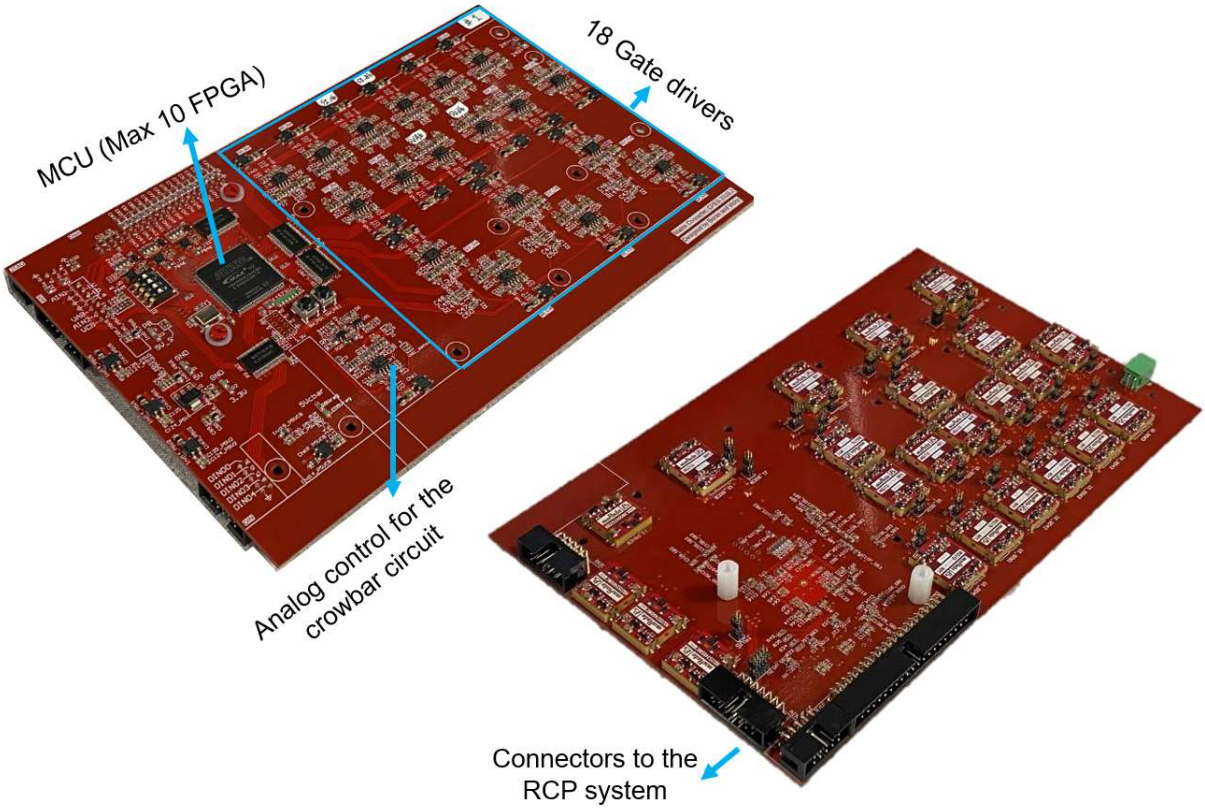


Figure 4.4 Three-phase controller board components

4.2.3 System Cooling

This design implements forced cooling from 12 fans mounted to the chassis. They cool the aluminum heat sink that sits under the phase-legs of the power board, and the choke of the EMI filter. The fans are 2.5 cm by 2.5 cm, with a power of 5W. The cooling system is shown in Fig. 4.5.

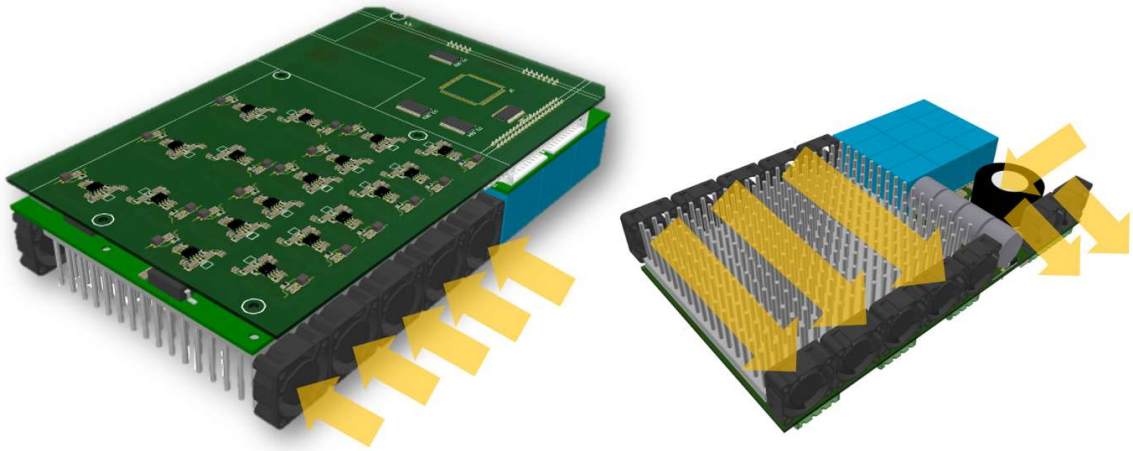


Figure 4.5 Three-phase heat management solution

4.3 Experimental Verification

4.3.1 Full Power Operation in Voltage Boost Mode

The operation of the matrix converter was verified in current conduction mode at the full power of 15kW. The input of 380V at 120Hz was boosted to a 460V, 60Hz output. The converter was operated at a 60kHz control frequency and a maximum switching frequency of 30kHz. Fig. 4.6 displays converter waveforms from this test. The voltage boost mode operation waveforms displayed, from top to bottom, are the established AC bus waveforms, the generator side currents, and the line-to-line voltages.

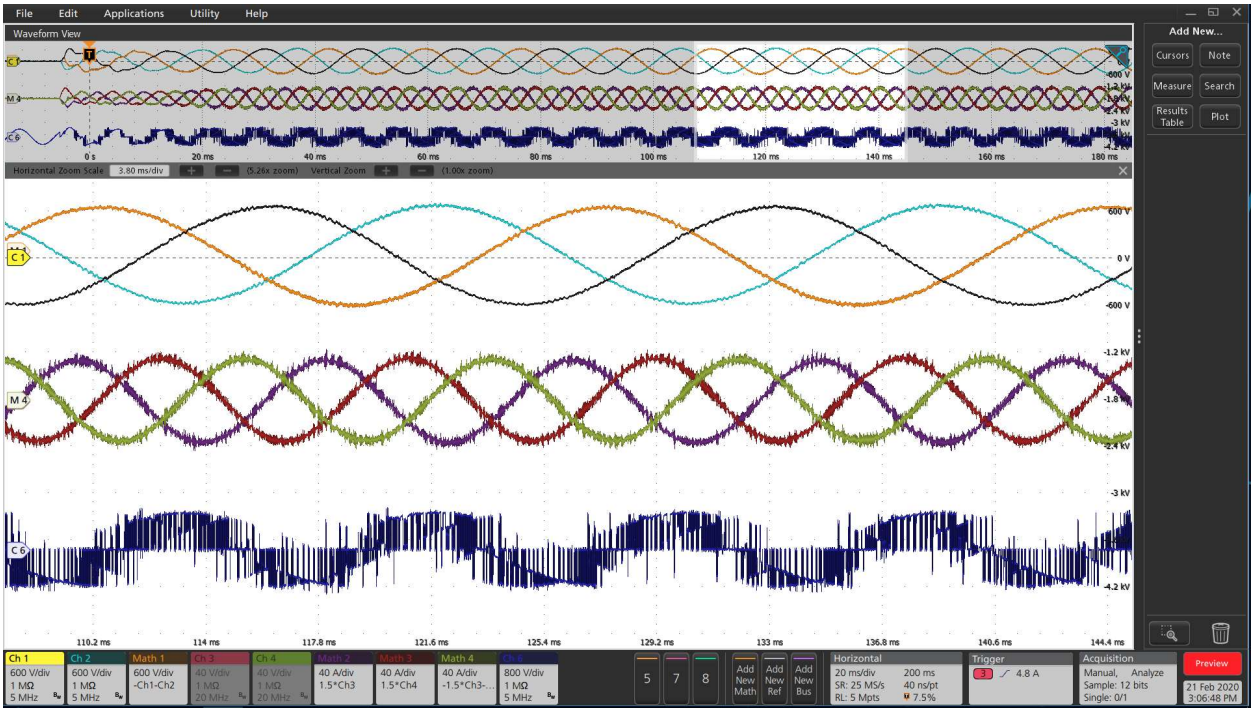


Figure 4.6 Matrix converter step-up mode operation

An FFT analysis of the AC bus waveforms and the generator side currents was performed. The THD for the AC bus waveforms was found to be 2.02%, and 4.01% for the generator side currents.

The three-phase design is further validated through a load transient test. In Fig. 4.7 the load is stepped from 0.6pu, 9kW, to 1pu, 15kW. Again, from top to bottom the waveforms displayed are the AC bus voltages, the generator side currents, and the line-to-line voltages.

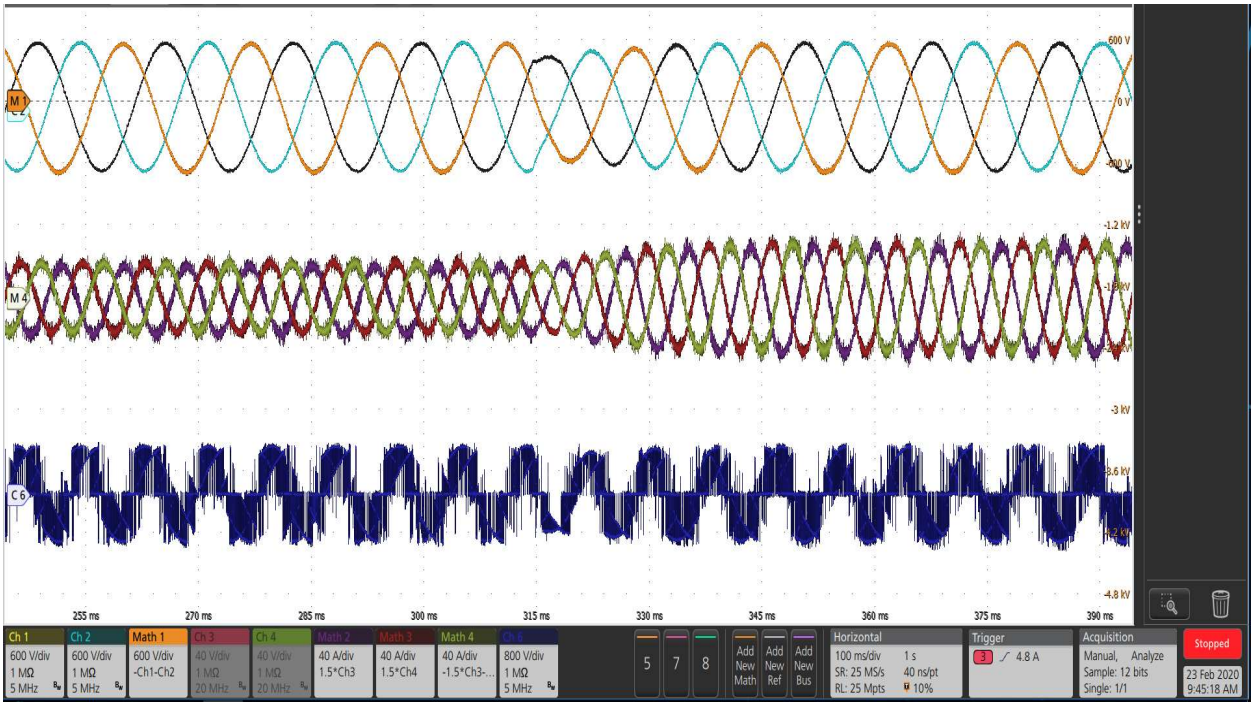


Figure 4.7 Transient load step from 0.6pu to 1pu

4.3.2 EMI Measurements

EMI measurements were taken according to the setup shown below in Fig. 4.8. The resulting attenuated common mode, differential mode, and total noise measured is shown in Fig. 4.9 with the corresponding DO-160 standard in green.

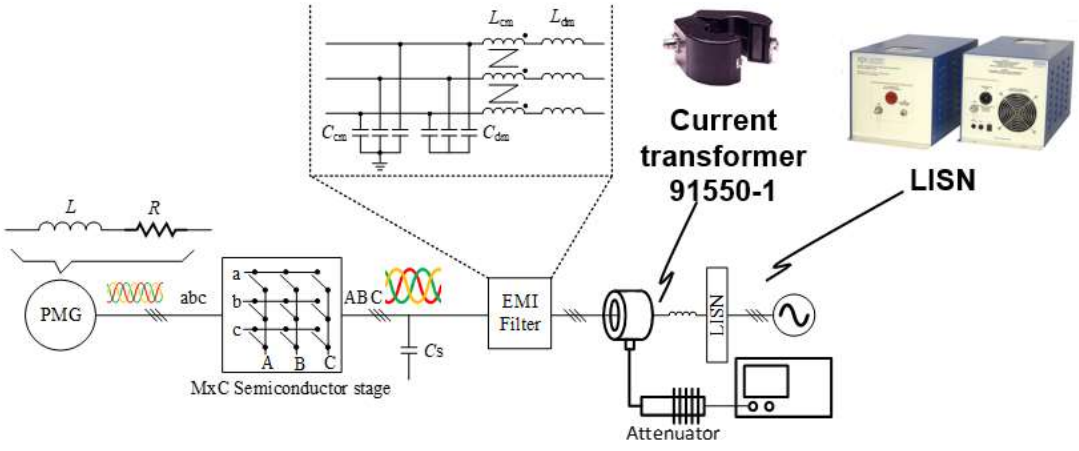


Figure 4.8 Block diagram of EMI test setup

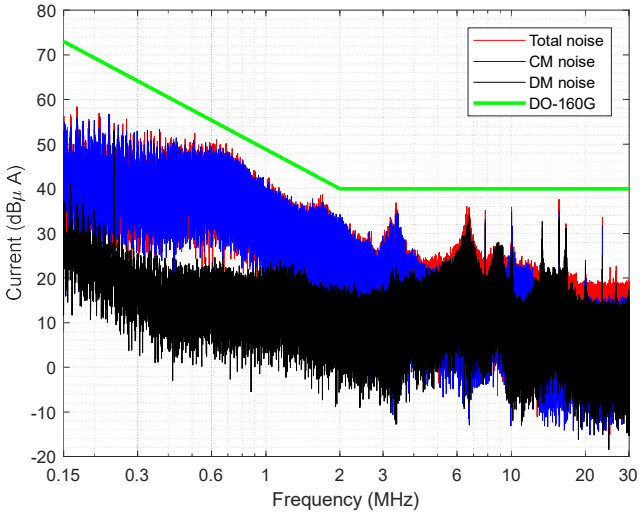


Figure 4.9 EMI test results with DO-160 standard passed

4.3.3 Efficiency Measurements

The converter noise levels are compliant with the DO-160 standard. The efficiency of the converter was also measured with the PA2203A power analyzer. The efficiency was determined with the following setup described in Fig. 4.10. Current and voltage waveforms were measured at both the inputs and outputs of the converter.

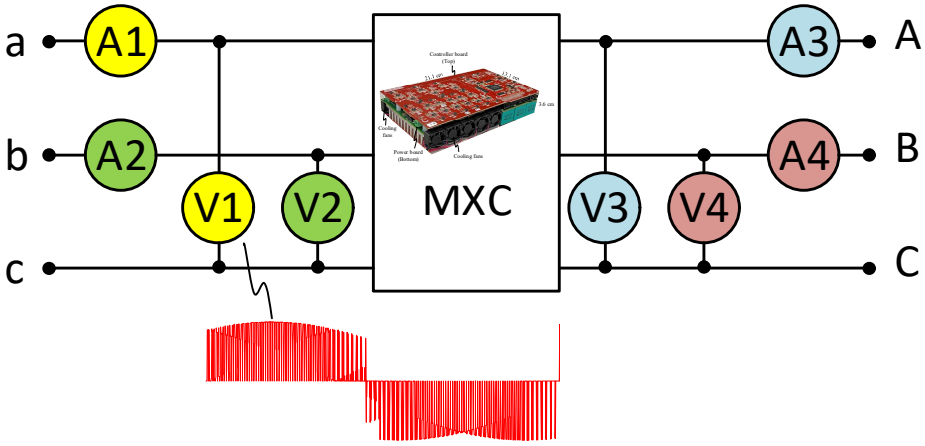


Figure 4.10 Efficiency measurement with power analyzer test setup

Measurements were made at increasing power levels, to full power of 15kVA. The results are shown in Fig. 4.11. The converter efficiency at full power is found to be 98.3%. It should be

noted that the power analyzer induces an error in measurement. The input voltage is a waveform with 20us pulses, while the sample rate of the power analyzer is 5Ms/s, resulting in a 1% error.

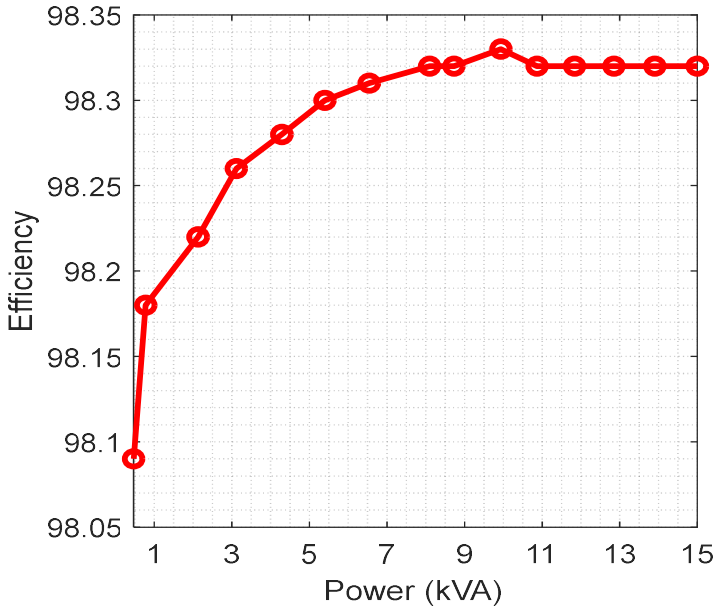


Figure 4.11 Efficiency measurement results, 98.3% efficiency at full power

4.3.4 Thermal Verification

Lastly, the thermal management of the system is validated. The converter is run at full power, 15kVA, in step up mode continuously for an hour. The temperature was monitored with thermal couplers attached to the device baseplate edge of two MOSFETS, as shown by the red dot in Fig. 4.12.

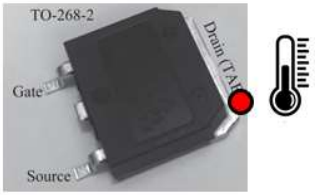


Figure 4.12 Thermal validation test measurement point

The resulting temperatures are graphed in Fig. 4.13. The maximum temperature measured was 80.2°C. Using the junction-to-case thermal resistance given by the data sheet of this MOSFET,

0.23°C/W, the junction temperature is estimated to be 84.3°C. This is a safe operating region for the device, which has an allowable maximum operating junction temperature of 175°C.

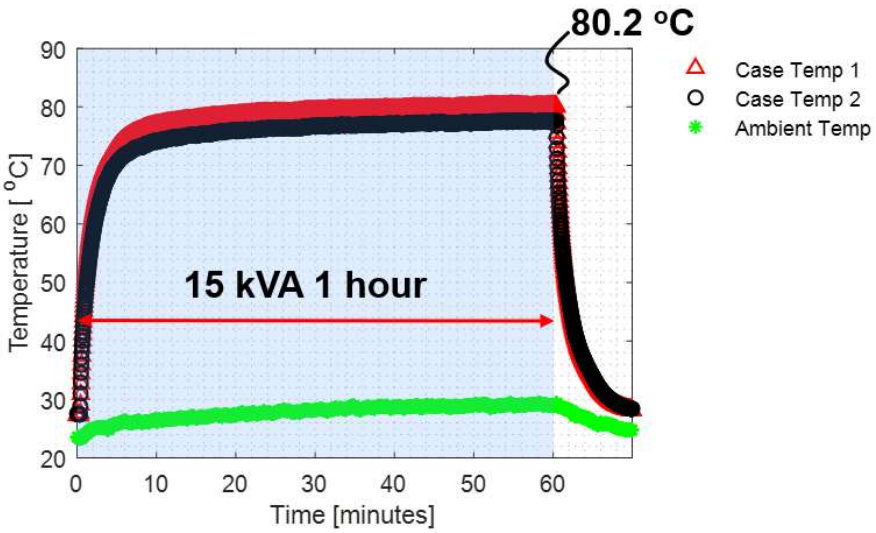


Figure 4.13 Thermal validation results of converter at full power for 1 hour

An overload test of the converter is performed at 25kVA, 167% of the rated power, for 1 minute of operation. Again, the temperature is monitored with thermal couplers as mentioned above. The resulting data is displayed in Fig. 4.14. A final temperature is measured to be 75.3°C, with a corresponding estimated junction temperature of 81.5°C.

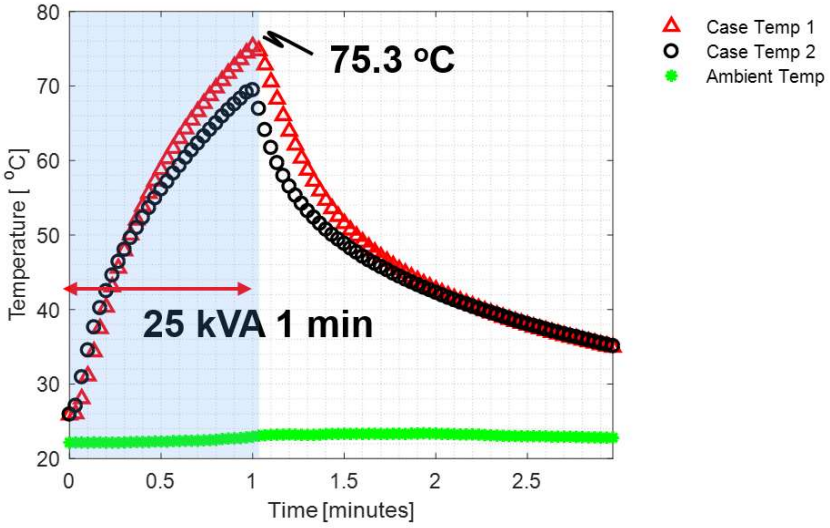


Figure 4.14 Converter overload test results for 1 minute

Additional testing was performed at 19kVA for an hour. These temperature results are graphed in Fig. 4.15. The final measured temperature was 99.2°C, and the junction temperature can then be estimated to be 104°C.

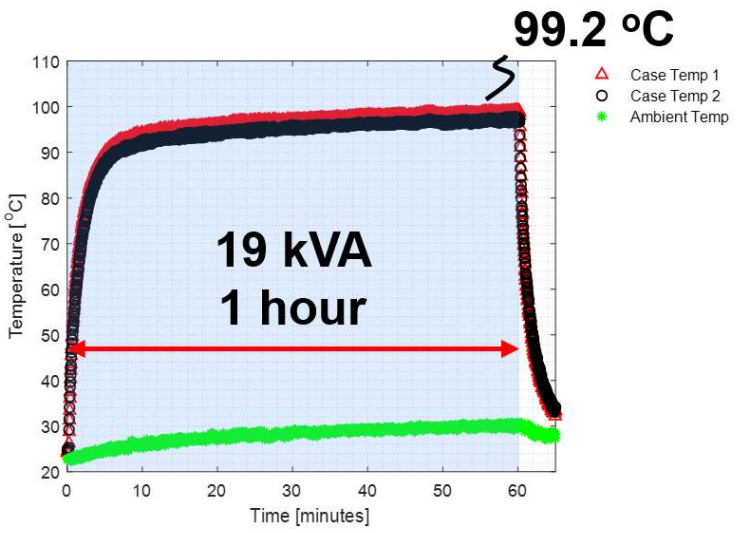


Figure 4.15 Further thermal testing conducted at 19kVA for an hour

The operation of the converter and its thermal management solution is verified.

Chapter 5

Common-source Inductance Induced Voltage Overshoot and Oscillation

5.1 Introduction

This chapter details the reason behind an observed voltage overshoot phenomenon, and begins to characterize it through simulation and experiment. This work was performed in collaboration with Dr. Boran Fan.

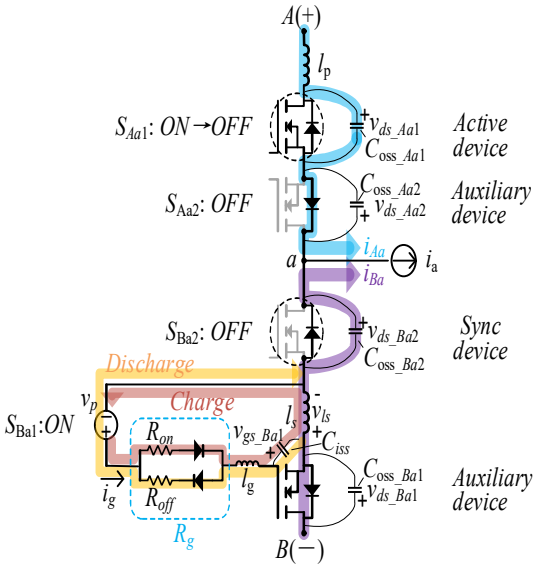


Figure 5.1 Switching transient circuit with parasitic and S_{Ba1} gate-loop illustrated. 'Active', 'synchronous' and 'auxiliary' devices are identified

5.2 Voltage Overshoot Mechanism

With the switching transient circuit identified, this section reveals the mechanism of the unusual turn-off voltage depicted in Fig. 5.1. In Fig. 5.1, critical inductive and capacitive parasitics and the S_{Ba1} device gate loop are illustrated. l_p is the equivalent power loop parasitic

inductor. l_g and l_s are the S_{Ba1} device gate-loop inductor and common-source inductor. C_{oss_Aa1}, C_{oss_Aa2}, C_{oss_Ba2} and C_{oss_Ba1} are the output capacitors for the four devices.

As shown in Fig. 5.1, when the active device S_{Aa1} turns off, the current commutes from the top to the bottom branch. It is critical that the channel of auxiliary device S_{Ba1} remains in 'ON' state to provide the necessary current path in the process. Yet during the switching transient, the presence of the current slew rate (di/dt) induces a voltage drop (v_{ls}) across the common-source inductor ls which results in discharge of the gate voltage v_{gs_Ba1}, as given by (5.1), where R_g, i_g and C_{iss} are the gate resistance, charging current and device input capacitance. v_p is the static on-state gate supply voltage.

$$v_{gs\_Ba1} = v_p - i_g R_g - l_g(di_g/dt) - v_{ls}, \quad i_g = C_{iss} \cdot (dv_{gs\_Ba1}/dt) \tag{5.1}$$

Insight on what impacts the voltage drop across the common-source inductor is needed. It is assumed the S_{Aa1} device turn-off miller plateau is lower than the gate threshold voltage, meaning the channel is immediately turned off after the gate charge dropped below the threshold. Therefore, the current sharing between the top and bottom bidirectional device is exclusively determined by the output junction capacitance of the active and synchronous devices. Meanwhile, (5.2) is assumed which can be verified to agree with the characteristics of most devices.

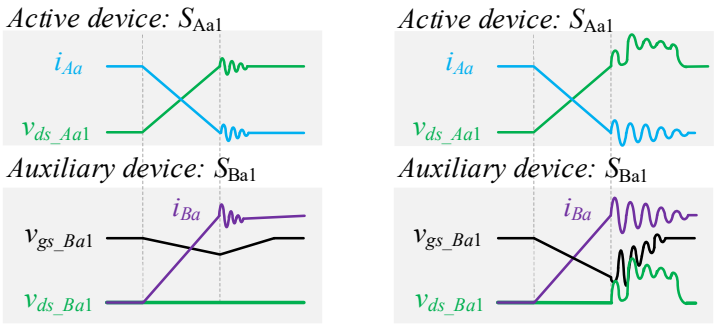
$$k = v_{ds\_Ba1} \cdot (dC_{oss\_Ba1}/dv_{ds\_Ba1}) \le C_{oss\_Ba1} \tag{5.2}$$

As a result, similar to the analysis in [37], a simple estimation for common-source inductor voltage is given by (5.3).

$$v_{ls} \approx -l_S \cdot (di_{Ba}/dt)$$

$$= -l_S {I_o}^2 \left(d\left(\frac{C_{oss\_Ba2}}{C_{oss\_Aa1}+C_{oss\_Ba2}}\right)/dv_{ds\_Aa1} \right) \frac{1}{C_{oss\_Aa1}+C_{oss\_Ba2}} \tag{5.3}$$

The common source inductance (CSI) induced voltage is proportional to the CSI, squared current and highly dependent on the nonlinearity of device output capacitance. Assuming a small CSI is presented, Fig. 5.2(a) demonstrates the typical turn-off switching transient waveform for the bidirectional devices where the voltage and current waveforms of the active S_{Aa1} and auxiliary device S_{Ba1} are illustrated. Note that the gate voltage v_{gs_Ba1} on device S_{Ba1} has a dip in Fig. 5.2(a), since the voltage drop is small, the channel of the auxiliary device is still in the 'on' state. The voltage across S_{Ba1} remains close to zero and no additional overshoot voltage is observed on S_{Aa1}. In comparison, if a moderate or a large CSI is presented, as depicted in Fig. 5.2(b), the voltage drop on v_{gs_Ba1} becomes deeper due to the increased v_{ls}. Meanwhile the current (i_{Ba}) flowing through the channel is increasing. In combination, device S_{Ba1} is dragged into saturation and thus the voltage across S_{Ba1} is increased and a significant voltage overshoot is observed on the S_{Aa1} as shown in Fig. 5.2(b)



(a) (b)

Figure 5.2 Bidirectional switching waveforms with (a) low CSI, and (b) high CSI

To further understand what occurs after device S_{Ba1} becomes saturated, a switching transient equivalent circuit is derived as shown in Fig. 5.3(a). Both the active and synchronous device are represented by their output capacitance, since, as aforementioned, the channel of S_{Aa1} is assumed to be completely off in the turn-off switching transient.

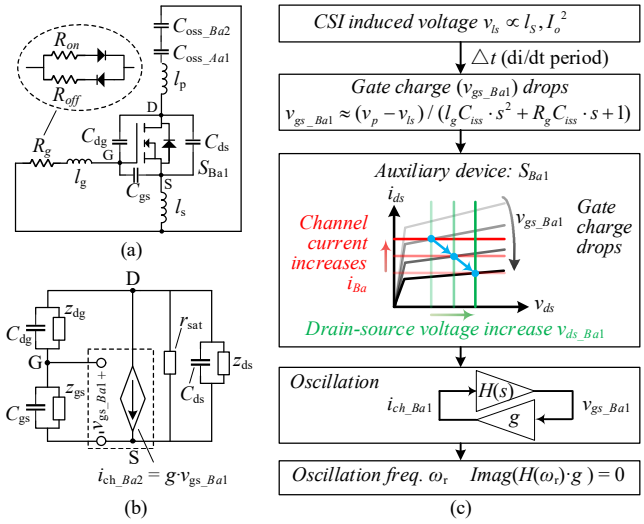


Figure 5.3 (a) Switching transient equivalent circuit (b) Switching transient analysis model. (c) Flow chart for the cause of the overvoltage and oscillation in the turn-off switching transient.

Knowing the auxiliary device S_{Ba1} is in saturation, it is replaced by a voltage controlled current source with a transconductance of g and a saturation resistance of r_{sat}. Fig. 5.3(b) shows the analysis model where a Y-delta transformation is conducted to simplify the impedance network around the device. Fig. 5.3(b) resembles the structure of a typical 3-point oscillator [38] where a positive feedback is formed between the gate voltage v_{gs_Ba1} and channel current i_{ch_Ba1}. This explains the oscillation in Fig. 5.3(b) during the overvoltage period. Assuming the transfer function from the channel current to gate voltage is H, then according to the Barkhausen criterion [38], the resonant frequency can be derived by assigning the imaginary part of the close-loop transfer function to be zero as in (5.4).

$$Imag(H(\omega r) \cdot g) = 0 \qquad (5.4)$$

The cause of the overvoltage and oscillation is summarized in Fig. 5.3(c): the CSI induced voltage discharges the auxiliary device gate voltage during the di/dt period, and eventually drags S_{Ba1} into saturation. With an increased current i_{Ba}, a voltage drop is formed across S_{Ba1} and thus a voltage overshoot across S_{Aa1}. The process is accompanied by strong oscillation tendency due to the positive feedback formed between i_{ch_Ba1} and v_{gs_Ba1}.

5.3 Turn-off Transient Characterization

Knowing the unusual turn-off voltage is associated with the CSI in the auxiliary device, the following section investigates how key circuit parameters affect the bidirectional device turn-off performance using simulation studies. Approaches are also discussed on how to eliminate or attenuate the detrimental effects.

5.3.1 CSI influences

As shown in (5.3) and Fig. 5.3(c), the voltage drop across the common-source inductor in auxiliary device S_{Ba1} is proportional to the CSI and squared current. Correspondingly, Fig. 5.4 illustrates the simulation study of the CSI influence on turn-off voltage with various current levels. The simulation is conducted in LTspice using 900V 30mΩ SiC MOSFET models. The circuit in Fig. 5.4 is used for simulation with v_{AB} equal to 600V. As shown in Fig. 5.4, larger CSI and current tend to result in higher turn-off voltage because it is more likely to saturate the auxiliary device. Two regions are identified in Fig. 5.4. Region 1 is where the CSI influence is limited, and a normal turn-off voltage is observed across the active device. In Region 2, the auxiliary device becomes saturated and significant turn-off overvoltage is monitored. With the current level increasing from 30A, 40A, 50A to 60A, the minimum CSI leading to auxiliary device saturation reduces from 17nH, 11nH, 9nH to 7nH respectively, which reveals that higher reduction on CSI is paramount if bidirectional devices are operated under high current levels.

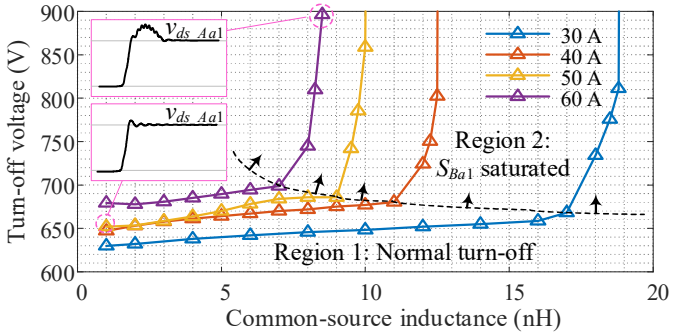


Figure 5.4 Simulation study of the CSI influence on turn-off voltage with different current levels

Fig. 5.5 shows the switching energy evaluation on the active and auxiliary device at 60A. The voltage and current on the two devices are also illustrated in Fig. 5.5. For normal turn-off with small CSI, the voltage (v_{ds_Ba1}) across device S_{Ba1} is close to zero, thus almost no switching loss is generated on the auxiliary device. However, if the CSI is higher than 7nH, significant v_{ds_Ba1} is observed. Meanwhile, since the current on S_{Ba1} is close to the output current, large switching loss is expected. Providing CSI is 8.5nH, 525μJ switching energy is created which is over 20 times higher than the 25μJ energy in the ideal condition of zero CSI. It is interesting to notice that even though the giant turn-off voltage overshoot is seen on the active device, unlike the auxiliary device, the switching energy of the active device remains relatively constant with different CSI, because the active device current i_{ds_Aa1} is close to zero in the overvoltage duration.

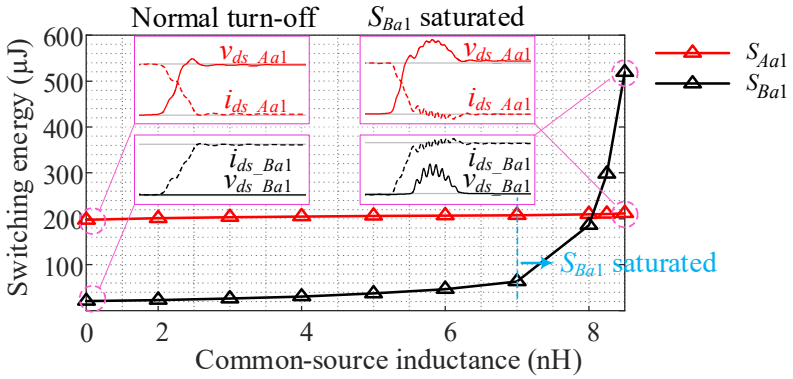


Figure 5.5 Simulation study of the switching energy characterization for the active device S_{Aa1} and the auxiliary device S_{Ba1} at 60A

5.3.2 Gate resistance influences

As shown in (5.1), the turn-off gate resistance plays a critical role on limiting the CSI induced voltage v_{ls} to discharge v_{gs_Ba1}, thus avoiding the device saturation. Correspondingly, Fig. 5.6 shows the simulation study of the turn-off gate resistance influence on voltage overshoot under various CSI providing the output current is 40A and the turn-on resistance is 4.7Ω. As expected, in Fig. 5.6, a larger turn-off resistance is helpful to attenuate or even eliminate the unusual overshoot voltage. In Fig. 5.6, if the CSI is below 4nH, even 0Ω resistance will not lead to S_{Ba1} saturation. However, with the CSI increasing from 6nH, 8nH to 10nH, the required minimum R_{off} to avoid S_{Ba1} saturation is increasing from 0.5Ω, 1.1Ω to 1.7Ω. Compared to turn-off gate resistance, the turn-on gate resistance is not as helpful on avoiding the auxiliary device saturation. Because, as shown in Fig. 5.1, in the gate-loop discharge path only turn-off resistance is presented.

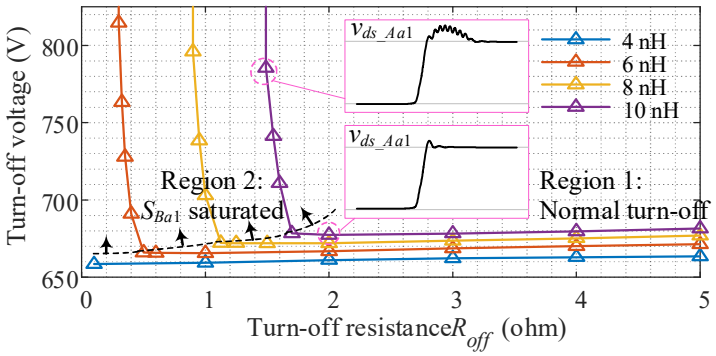


Figure 5.6 Simulation study of the turn-off resistance influence on turn-off voltage with different CSI levels (40A current, R_{on}=4.7 Ω)

5.3.3 Inductive gate loop influences

Besides the turn-off resistance, as shown in (5.1), the gate loop inductance l_g is the other critical parameter capable of blocking the gate discharge. Fig. 5.7 shows the simulation study of the gate-loop inductance level influence on voltage overshoot. The turn-on and turn-off resistance are set as 4.7Ω and 0.5Ω, and the CSI is 6nH. As expected, in Fig. 5.7, as the gate-loop inductance increases, the overshoot voltage is effectively attenuated.

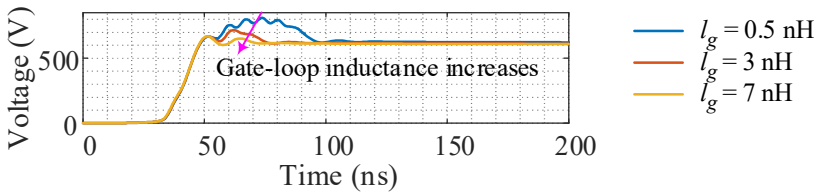


Figure 5.7 simulation study of the gate-loop inductive level influence

5.4 Solutions

The most straightforward way to avoid the CSI induced issue is to minimize the CSI. This can be achieved by using device packages with a Kelvin-source connection and optimizing the PCB layout to avoid traces shared by the power and gate loop. However, even with Kelvin-source, CSI cannot be fully eliminated, and it is possible the overshoot issue can still occur at higher current level. Providing a given CSI, according to the previous discussion, the overshoot issue can also be solved by the appropriate gate resistance design or making the gate loop more inductive. Larger turn-off gate resistance is preferred, yet one should be aware that an excessive turn-off resistance leads to higher switching energy and more serious crosstalk [39]. Similarly, larger gate-loop inductance is advantageous on eliminating the voltage overshoot and oscillation issue, yet comprehensive evaluations are still necessary because excessive inductance can cause detrimental gate loop ringing and switching delays [40].

5.5 Experimental Verification

In this section, a custom-build MxC phase-leg, as shown in Fig. 5.8, is used to experimentally demonstrate the voltage overshoot and oscillation issue. Three bidirectional devices are presented in a MxC phase-leg. Each one is constructed using two discrete 900V 30mΩ SiC MOSFETs in common-source configuration. To be consistent with Fig. 5.8, the

bottom bidirectional device is disabled. Voltage test points and a current shunt are included for voltage and current measurements. The PCB power loop layout inductance is 14nH as extracted using Ansys Q3D.

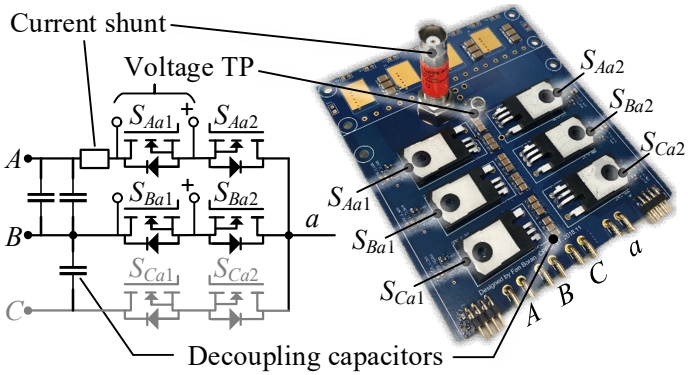


Figure 5.8 Switching transient test board for bidirectional devices

Fig. 5.9(a) shows the experiment verifications under current levels of 40A, 45A, 50A, 55A and 60A. Noting that although the device is packaged with Kelvin-source, the power-source is intentionally used in the gate loop to introduce around 5nH CSI. The device has 3Ω of internal gate resistance and the external turn-on and turn-off resistance are 4.7Ω and 0Ω respectively. In Fig. 5.9(a), from top to bottom, the waveforms are the active device voltage v_{ds_Aa1}, active device current i_{Aa} and auxiliary device gate voltage v_{gs_Ba1}. As expected, larger voltage dip is observed on v_{gs_Ba1} with higher current. When the current is above 50A, device S_{Ba1} becomes saturated and high voltage overshoot is monitored on S_{Aa1}. With 60A current, the device S_{Ba1} gate voltage drops from 15V to 2.82V and the turn-off voltage exhibits a detrimental 101.7 % overshoot. Serious oscillation is also monitored which can be explained by the analysis in Section 5.2.

As discussed in Section 5.3.3, inductive gate-loop helps blocking the CSI induced gate discharge for the auxiliary device. To experimentally verify the idea, a 5nH inductor is placed in the gate loop. The same experiments as in Fig. 5.9(a) are performed and the results are illustrated in Fig. 5.9(b). Due to the extra gate inductance, the v_{gs_Ba1} drops to 5.92V instead of 2.82V at

60A, effectively avoiding the S_{Ba1} saturation. Eventually the CSI induced overshoot voltage disappeared on the active device.

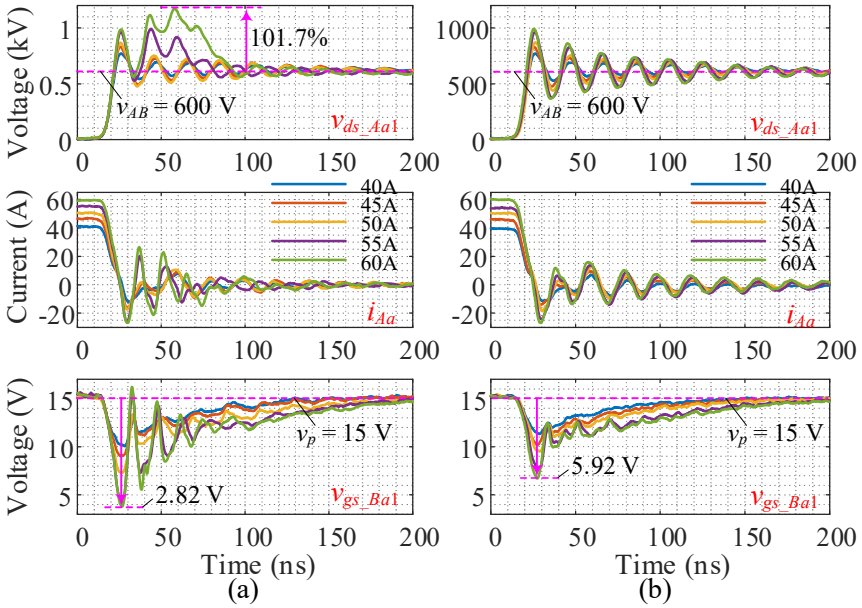


Figure 5.9 Experiment verification under various current levels. (a) Resistive gate loop (b) Inductive gate loop. From top to bottom: active device voltage v_{ds_Aa1}, active device current i_{Aa}, auxiliary device gate voltage v_{gs_Ba1}.

To experimentally verify the CSI influence, an additional 5nH CSI is introduced. Fig. 5.10 shows the experiment verifications at 40 A with various external turn-off resistance. Comparing the 40A, 0Ω R_{off} results in Fig. 5.9(a) and Fig. 5.10(a), the voltage overshoot is increased from 750V to 1370V because of the marginally increased 5nH CSI, revealing the serious impact of CSI in the turn-off transient. As discussed in Section 5.4, turn-off gate resistance is also beneficial for avoiding auxiliary device saturation. As shown in Fig. 5.10(a), With the increase of the turn-off resistance, the active device voltage overshoot is effectively attenuated. The auxiliary device voltage, current and switching energy are shown in Fig. 5.10(b). As the external turn-off resistance increases from 0Ω, 1Ω, 2.2Ω to 4.7Ω, the switching energy reduces 5 times from 1.22mJ, 0.96mJ, 0.55mJ to 0.22mJ.

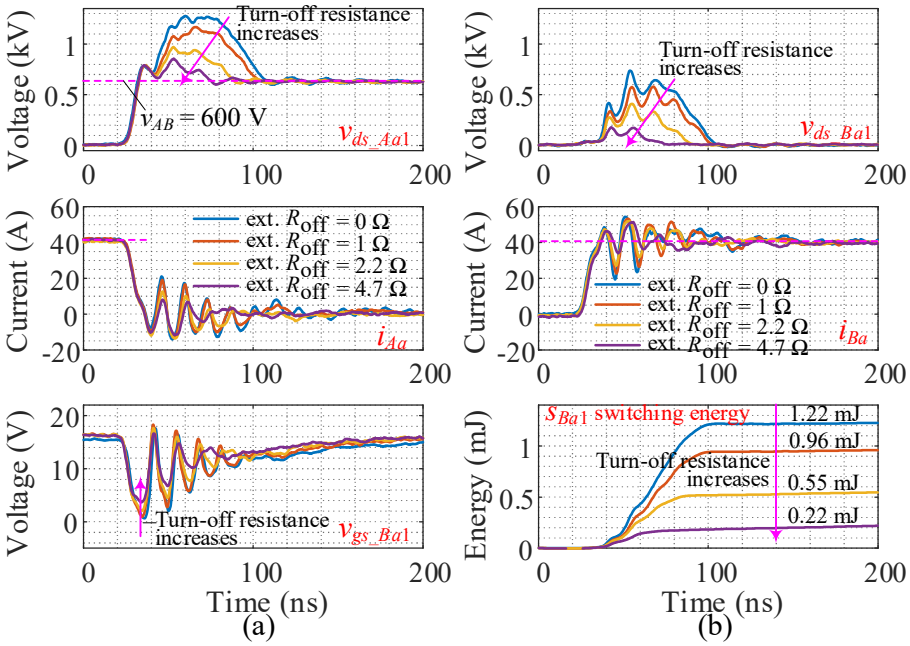


Figure 5.10 Experiment verification with different external turn-off resistance with additional 5 nH CSI. From top to bottom: (a) active device voltage v_{ds_Aa1}, active device current i_{Aa}, auxiliary device gate voltage v_{gs_Ba1}. (b) auxiliary device voltage v_{ds_Ba1},

Chapter 6

Evaluation of Thermal Management Strategies for Surface Mount Devices

6.1 Introduction

This chapter reviews several strategies for surface mount device thermal management, that include thermal via, aluminum nitride inlay, metal core PCB, and top-side heat sink. The strategies' thermal resistances are determined first mathematically then experimentally. The matrix converter application necessitates the heat management strategy to dissipate at least 10W. PCB layout limits imposed by the heat dissipation methods are discussed. These results are summarized and acceptable heat management strategies for the matrix converter application are revealed.

6.2 Motivation for heat management evaluation

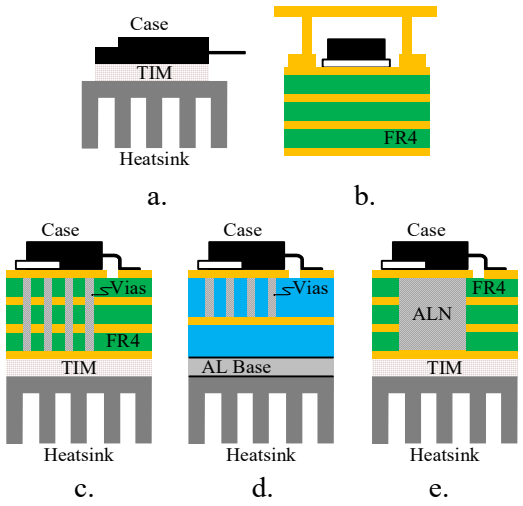


Figure 6.1 Heat management strategies for, (a) Through hole device, and surface mount device (b) Top side heat sink, (c) Thermal Via, (d) Metal core PCB, (c) AlN ceramic inlay

In order to utilize the benefits of surface mount devices, a heat dissipation strategy must be implemented in or on the PCB to lower its thermal resistance. Without an added thermal management strategy, the device and board will overheat and break. The solution will not be functional. Four surface mount cooling methods are evaluated using an analytical approach, and experiment, then compared to through-hole device performance, Fig. 6.1a. A top-side heat sink, metal core PCB (MC PCB), thermal via, and ceramic inlay heat dissipation methods [41], shown in Fig. 6.1b-e, are first evaluated analytically. The device package evaluated is the TO-268, or D-PAK3.

6.3 Analytical evaluation of surface mount device heat management strategies

6.3.1 Top-Side Heat Sink

The top-side heat sink channels heat through the top copper layer to a heat sink that sits over the device. The thermal resistance can be estimated using Equation 6.1 where d is the depth of path, A is the cross-sectional area that the heat passes through, and k is the thermal conductivity of the path material.

$$R_{th} = \frac{d}{kA} \tag{6.1}$$

Assuming the midpoint of the device base is the hottest point, the heat must travel half the width of the device, 8.75mm, through the cross-sectional area of the depth of the copper trace and length of the device, 12.7mm by 0.0696mm. Then the heat travels up to sides of the heat sink to its top. This thermal resistance can be represented by a parallel thermal circuit as there are two paths for the heat to travel, as illustrated by Fig. 6.2. Still, because the area of the path is so small, the calculated thermal resistance is very high at 13.3°C/W.

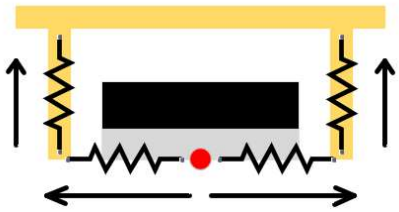


Figure 6.2 Top-side heat sink heat path

6.3.2 Metal Core PCB

The thermal resistance of the metal core material can be calculated again with Equation 1. In this case, the thermal conductivity is determined by the metal core material, which is higher than the traditional FR4 material, decreasing the thermal resistance. However, this parameter will vary, along with the produced resistance, depending on the material used. For this evaluation the Rodgers' Corporation RO 3010 material is used, with a thermal conductivity of 0.95 W/mK [42].

The heat travels the depth of the board, 1.6mm, through the area under the device, 12.7mm by 13.6mm. This area that is considered should also include the spreading angle, as the material is uniform, which can impact the thermal resistance. This affect can be calculated by dividing the depth of the board into smaller sections, Δd, recalculating the new area, A', and calculating a thermal resistance for that depth, Δd, and area, A', respectively. The total thermal resistance is calculated by summing these smaller thermal resistances, as shown in Equation 6.2.

$$R_{th} = \sum \frac{\Delta d}{kA} \qquad (6.2)$$

The total thermal resistance without spreading angle consideration is 9.85°C/W. Fig 6.3, shows the impact of this spreading angle on the total thermal resistance. The angle, theta, has a range of 0° to 70°, 0° representing no spreading angle, the maximum thermal resistance. The Fig. 6.3 shows the thermal resistance of the metal core PCB.

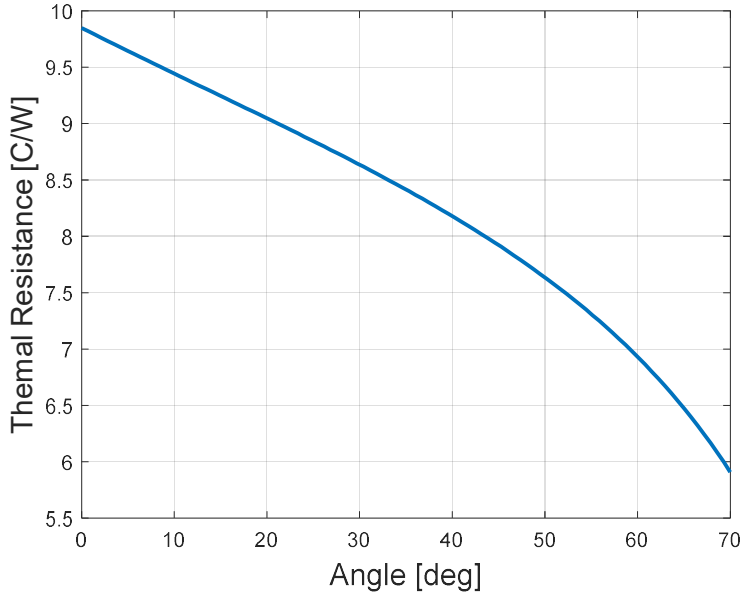


Figure 6.3 Relationship between spreading angle and metal core PCB thermal resistance

6.3.3 Aluminum Nitride Inlay

The thermal resistance of the AlN insert can be calculated with the Equation 6.1. Like the case of the thermal vias, the spreading angle is negligible. The thermal conductivity of the aluminum nitride is significantly higher than that of FR4, at 170W/mK. The AlN insert has an area of 12mm by 12mm, and a depth of 1.6mm. Its calculated thermal resistance is 0.065°C/W.

6.3.4 Thermal Via

The thermal via system can be considered as two resistances in parallel - the resistance of the FR4 and that of the vias. The significantly lower resistance of the vias will dominate the total resistance. Because of this the thermal resistance can be calculated with only the via information. The cross-sectional area of one via is calculated with the following equation.

$$A = \pi(r_2^2 - r_1^2) \qquad (6.3)$$

R_2 represents the outer edge of the via, while r_1 the inner, as displayed by Fig. 6.4. The distance between the two radii is assumed to be 35um, or 1oz of copper, for 2oz copper trace weight, given by the board manufacturer. Then, this area multiplied by the number of vias in the system, represents the total area of copper that directs heat through the FR4. Using the thermal conductivity of copper, 390W/mK, Equation 6.1 can be used to find the thermal resistance of the thermal vias.

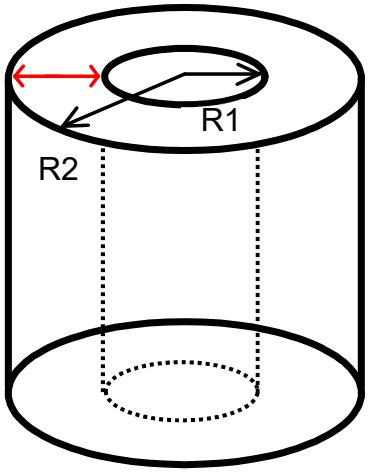


Figure 6.4 Diagram of Thermal Via radii for area calculation

The amount of copper removed for the vias must be leveraged against the benefits of thermal resistance. Higher numbers of vias will provide a lower thermal resistance for the heat management system. However, more vias will remove more copper from the device pad, and will produce higher impedances for other traces placed underneath the device. To begin, the number of vias is limited to take up only 15% of the device pad area. This number is determined through Equation 6.4.

$$n = \frac{device\ area\ \%}{\pi(diameter/2)^2} \tag{6.4}$$

The percentage of the area of the device pad is divided by the area of a single via with diameters of 8mils, 15mils, and 30mils. The results of this calculation are shown in Table 6.1.

The number of vias ranges from 56-798 in the 15% coverage. The respective thermal resistances are displayed in Table 6.2. They range from 0.81-0.195°C/W. The larger number of smaller vias produce a smaller thermal resistance.

Table 6.1 Number of vias for 8, 15, or 30 mil diameters with 15% or 25% percent pad coverage

Via Diameter	**Number of vias**	
	15% coverage	***25% coverage***
8 mil	798	1331
15 mil	227	378
30 mil	56	94

The thermal resistance of the thermal vias can decrease if the vias are filled. For this case, Sn43Pb43Bi14 solder-filled vias are considered. This solder has a thermal conductivity of 50W/mK. This resistance is again in parallel with the thermal vias. The cross-sectional area of the solder filled via is calculated with the area of a circle. The thermal resistances are then calculated, again with Equation 6.1, and are displayed in Table 6.2. With this consideration the thermal resistances range from 0.46-0.15°C/W. These results, however, are still more than double the resistance of the AlN ceramic inlay.

Table 6.2 Thermal resistance of via configurations of varying size and percent pad coverage

Via Diameter	**15% coverage**		**25% coverage**	
	Air filled	***Solder filled***	***Air filled***	***Solder filled***
8 mil	0.195	0.15	0.12	0.09
15 mil	0.39	0.27	0.24	0.16
30 mil	0.81	0.46	0.49	0.27

To determine the number of vias needed to yield a similar thermal resistance the device pad coverage is increase to 25%. Using the same calculation method as above, the number of vias is determined and displayed in Table 6.1. The range of vias increases to 94-1331. Resistances are once again calculated for both the air-filled and solder-filled cases and are

displayed in Table 6.2. The air-filled vias thermal resistances range from 0.49-0.12°C/W while the solder-filled vias resistances range from 0.27-0.09°C/W.

6.3.5 Comparison of analytical evaluation

A summary of the calculated thermal resistances is displayed in Table 6.3. Through calculation, the AlN heat management solution provides the smallest thermal resistance. Thermal vias can provide a similar magnitude resistance given a 25% device pad coverage of 8mil, filled vias. The top-side heat sink and metal core PCB, in comparison, have quite high thermal resistances. The resistance of the top-side heat sink, in fact, is too high to provide the needed 10W of power dissipation. To control the temperature of the device at 125°C, the maximum amount of power able to be dissipated is restricted to 9.4W. It will not be considered in further evaluation.

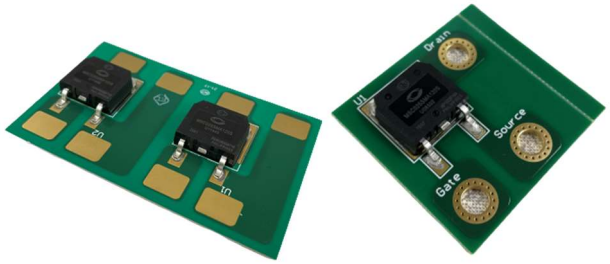
Table 6.3 Comparison of Calculated Resistances for SMD heat management strategies

	Calculated Resistances	
Top Side Heat Sink	13.3°C/W	
Metal Core	7.3°C/W	
AlN Inlay	0.06°C/W	
8mil Thermal Via	***Air Filled***	***Solder Filled***
15% coverage	0.195°C/W	0.15°C/W
25% coverage	0.12°C/W	0.09°C/W

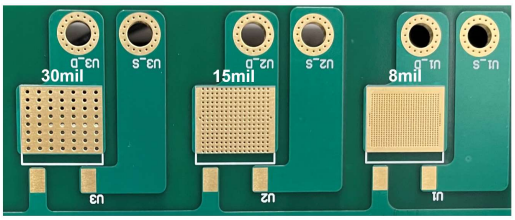
6.4 Experimental Validation

6.4.1 Test Setup

Test boards were developed to experimentally verify the calculated results. The boards are shown in Fig. 6.5. Fig. 6.5a. is the MC test board, 6.5b is the AlN inlay board, while the thermal via configurations are shown in 6.5c-d.



a. b.



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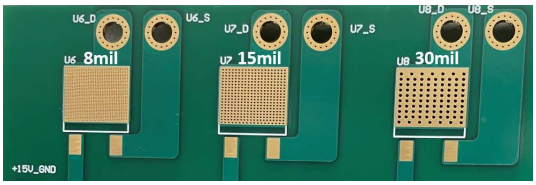

d.

Figure 6.5 Test boards for thermal analysis (a) MC PCB, (b) AlN Inlay, (c) 15% coverage thermal via, and (d) 25% coverage thermal via

The Phase 12B thermal analyzer from Analysis Tech was used to determine the thermal resistances of the heat management strategies. These tests are run according to the JEDEC JESD 51-14 standard, the setup of which is shown in Fig. 6.6.

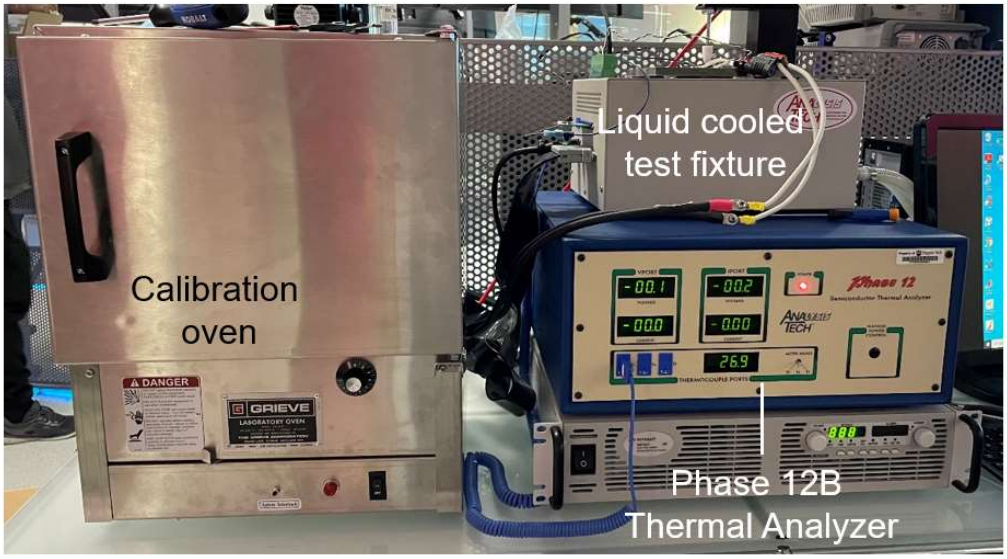

Figure 6.6 Phase 12B thermal analyzer test setup

First, junction calibration is completed to determine the relationship between the body diode forward voltage and the junction temperature, allowing the junction temperature to be measured non-invasively. Heating characterization can then be performed to determine the thermal resistance of each cooling method.

To complete the heating characterization tests the device is affixed to the liquid cooled test plate, and interfaces through a low thermally resistant stack. This stack is made up of either Dow Corning 340 thermal grease or silicone oil and a copper standoff and a sheet of indium. It is held in place with a pressure of approximately 55psi, that guarantees the indium has a low thermal resistance. This setup is illustrated in Fig. 6.7. The thermal analyzer then heats the device to a user specified temperature, 130°C in this case. The body-diode forward voltage is monitored as the device is heated and cooled. The thermal analyzer incurs a maximum error of ±2°C. This results in a maximum error of 1.5%.

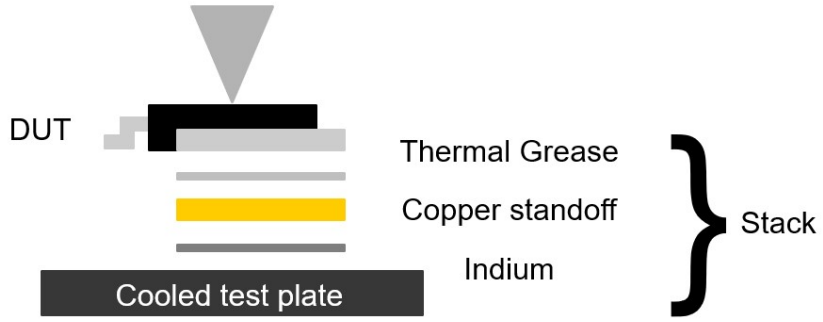

Figure 6.7 Thermal interface, "Stack", setup for thermal analysis

The results of these heating characterization tests can be presented in multiple ways, namely transient data, and a cumulative structure function. The cumulative structure function displays the cumulative thermal resistance on the x-axis and thermal capacitance of the system on the y-axis. More information about the cumulative structure function can be found in [43]-[47]. As the total thermal resistance is considered, the examination of the cumulative structure function is not paramount. The thermal analyzer provides a final thermal resistance for each test which will be utilized to compute the thermal resistances of each thermal management strategy.

6.4.2 Testing Results

The heating characterization is first completed on the device and stack in order to isolate the value of the thermal interfaces in later tests. The total resistance from the stack will be subtracted from the resulting total thermal resistance of each thermal management strategy. The results of the heating tests on the device and stack configuration are displayed in Fig. 6.8. The yellow and white curves correspond to the tests run with a thermal grease interface for just the device and the device and stack respectively. The total thermal resistance of the stack configuration is 0.9°C/W.

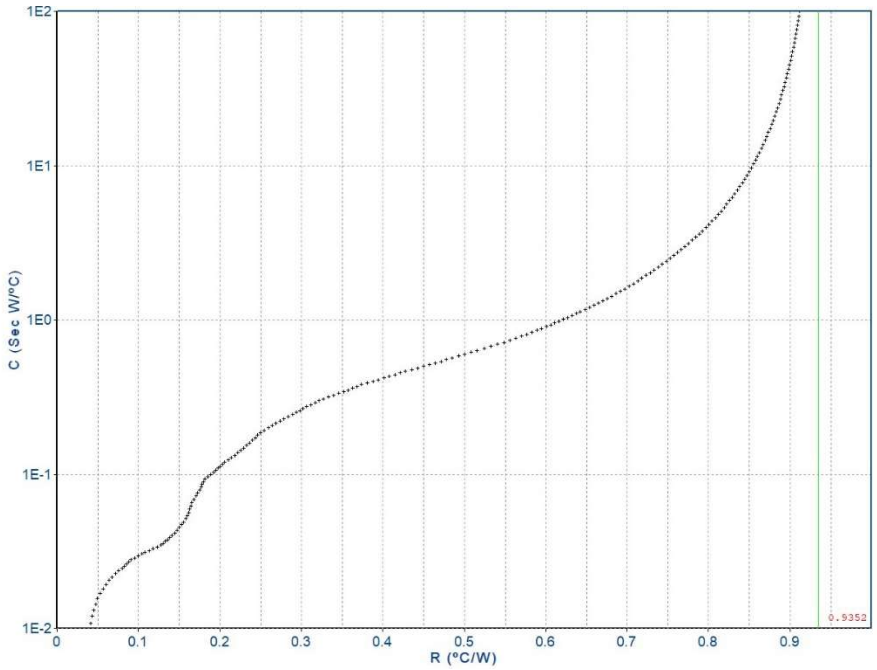

Figure 6.8 Cumulative structure function of DUT and stack

The metal core PCB is first tested. The total cumulative resistance is 5.95°C/W, and the resistance of the cooling approach isolated is 5.02°C/W. The associated spreading angle of this configuration can be estimated with the Equation 6.5 [48].

$$\alpha_a = arctan\left(\frac{k_a}{k_b}\right) \tag{6.5}$$

The spreading angle of the RO3010, material a, is calculated with the thermal conductivities of the material a, and the material b that is 'downstream' of the material a in the heat path. In this test configuration this is the thermal grease, with a thermal conductivity of 0.67W/mK. This results in a heat spreading angle of 54.8°. With this spreading angle, the measured resistance can be compared to the calculated value of 7.3°C/W.

The AlN result is much lower, with a measured resistance of 0.125°C/W. This thermal resistance could be higher due to a poor soldering connection. Because the thermal resistance of

the ceramic inlay is very small, the total thermal resistance is dominated by the solder connection.

Table 6.4 Measured thermal resistances of 8mil, 15mil and 30mil via configurations with 15% and 25% pad coverage

	Measured Resistance	
Via Diameter	***15% coverage***	***25% coverage***
30 mil	0.7°C/W	0.4°C/W
15 mil	0.4°C/W	0.16°C/W
8 mil	0.37°C/W	0.12°C/W

This ceramic inlay result is compared again to the thermal resistance provided by thermal vias. The results of these tests are displayed in Table 6.4. The calculated values describe a trend that can be seen in the measured results as well. At a constant drain pad coverage, as the via size decreases, and number increases, the thermal resistance decreases. The amount of via coverage is a strong determanent of the thermal resistance of the cooling method too. The increase in percent via converage from 15% to 25% decreases the thermal resistance by at least 33%. But still the smallest sized vias and the most coverage must be emplyed to provide the same thermal resistance as the ceramic inlay.

Table 6.5 displays a summary of both the calculated results and the measured thermal resistance values.

Table 6.5 Comparison of thermal impedance of surface mount heat management strategies

Heat Management strategy	**Thermal Resistance**		
	Calculated		***Measured***
Metal core	7.3°C/W		5.02°C/W
AlN Inlay	0.06°C/W		0.125°C/W
8 mil Thermal Via	*Air filled*	*Solder filled*	
15% coverage	0.195°C/W	0.15°C/W	0.37°C/W
25% coverage	0.12°C/W	0.09°C/W	0.12°C/W

6.5 Application to PCB layout for Matrix Converter

6.5.1 Layout Limits imposed by heat management strategies

The top cooling method, while not providing good thermal performance also incurrs spatial limits on a device layout. As seen in Fig. 6.9a, the top heat sink is large and requires more area than a solitary MOSFET. The traces then must be longer and wider to accommodate the heat sinks, but, any layout strategy may be implemented.

The Thermal Via cooling method requires the bottom and top copper traces to be shorted, shown by the dark orange vias in Fig. 6.9b. This limits the inductance cancellation possibilities of a hybrid loop, but a vertical loop could be implemented [36]. However, the shorted vias remove copper in all board layers, seen in Fig. 3b. The blue inner traces lose copper in favor of the vias shorting the top red layer to the bottom layer. This increases the trace DC resistance and in turn loss [49].

While multiple layer MC PCBs are possible, their thermal performance deteriorates quickly when the number of layers increase. In addition, this thermal strategy would disallow the use of through hole components which is inconvenient for an integrated design. It can further inconvenience an optimal layout. An optimized heat design for MC PCB, found in [50], spreads devices out, and would necessitate long, lateral traces that induce inductance in the system. While beneficial for thermal performance the system performance suffers. The lack of inner copper layers confines the layout greatly, and again, a lateral layout would need to be implemented.

The AlN ceramic insert is relatively new, and currently allows a four-layer PCB implementation. The insert removes the inner layer copper under the device, but the top and bottom side traces remain [41]. This heat dissipation method allows for both vertical and hybrid

layers, but extra copper must be placed around the AlN cutouts, exemplified by the top view in Fig. 6.9c.

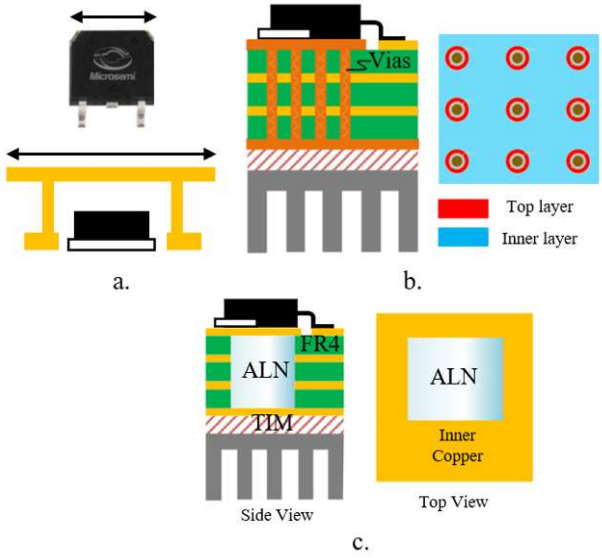

Figure 6.9 Layout limitations for (a) Top side heat sink, (b) Thermal via, (c) AlN inlay

6.5.2 Comparison to Thermal Performance of Through-Hole Devices

For the matrix converter application, the AlN ceramic inlay and thermal via are the most viable heat management solutions. The typical junction-to-case thermal resistance of the through-hole device used in the preliminary hardware, Cree C3M0030090K, described in Chapter 1, is 0.48°C/W. Implementing the Microsemi MSC025SMA120S, provides a solution with a typical junction-to-case thermal resistance of 0.27°C/W. When the AlN ceramic inlay and the 8 mil vias with 25% coverage are considered, both with thermal resistances of 0.12°C/W, the total thermal resistance is 0.39°C/W. This is comparable to the junction-to-case resistance of through-hole device. Phase-leg layouts are then created for each cooling approach and evaluated in Chapter 3.

Summary and Conclusions

7.1 Summary

A 3D power loop layout was successfully implemented in a matrix converter phase-leg to provide symmetric, low inductance power loops. This work limits the inductance of these three loops to approximately 5nH. In switching transients, the layout presented limits the overshoot to 21% of the final voltage at a DC bus of 600V and an output current of 45A. This thesis also demonstrates the effectiveness of an aluminum nitride cooling inlay to provide a PCB thermal resistance of 0.125ºC/W.

7.2 Conclusions

Due to the high dv/dt, and di/dt slew rates of silicon carbide devices, it is crucial to design PCB layouts with minimal inductance to avoid overshoots and ringing. This work demonstrates the effectiveness of 3D layouts to minimize power loop inductance and thereby decrease transient ringing and overshoot in a matrix converter phase-leg.

A hybrid layout, specifically, maximizes the amount of magnetic field cancellation among PCB traces to minimize the total loop inductance. It should be noted that this trace overlap increases the amount of capacitance in the system, which should be leveraged accordingly. In the case of the thermal via matrix converter phase-leg layout, discussed in Chapter 3, the amount of capacitance allowable in the system is a tradeoff with the symmetry and amount of inductance introduced. This issue was not present in the AlN ceramic layout, and the loop inductance was able to be minimized.

This thesis also demonstrates the benefits and drawbacks to implementing surface mount devices. The package was successfully implemented in the low inductance loop design, but has drawbacks thermally. It should also be noted the limited number of SiC die available in low R_{dson} surface mount packages. After the design was completed, more acceptable devices were released. One potential improvement to this work is the implementation of a surface mount device with a kelvin source connection. Chapter 2 details two possible devices that meet the needed criteria in such a package. Chapter 5 details the benefits of a low common-source inductance design, and the consequences of the opposite, particularly in a converter with bidirectional devices. The implementation of a surface mount device with a kelvin source can reap the benefits of a 3D layout and a low CSI design.

In conclusion, this thesis details the successful implementation of a 3D commutation loop for a 3-phase to 3-phase matrix converter. This layout reduces the loop inductance, which lowers ringing and overshoot in the switching transients.

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