Design of RF CMOS Power Amplifier for UWB Applications

Sajay Jose

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Dr. Dong S. Ha, Chair

Dr. Michael Buehrer

Dr. Sanjay Raman

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Design of RF CMOS Power Amplifier for UWB Applications

Sajay Jose

Dr. Dong S. Ha (Chairman)

Bradley Department of Electrical and Computer Engineering

Abstract

Ever since the FCC allocated 7.5 GHz (from 3.1 GHz to 10.6 GHz) for ultra wideband (UWB) technology, interest has been renewed in both academic and industrial circles to exploit this vast spectrum for short range, high data rate wireless applications. The great potential of UWB lies in the fact that it can co-exist with the already licensed spectrum users and can still pave the way for a wide range of applications.

However, this wide bandwidth complicates the circuit level implementation of key RF blocks like the power amplifier (PA), transmit/receive switch, low noise amplifier (LNA) and mixers in an UWB transceiver. Though expensive technologies like SiGe or GaAs have been used for transceiver realizations, the ultimate goal is to have a single-chip, low-cost solution which can only be achieved by using CMOS technology. Nevertheless, some of the inherent limitations of CMOS like lower f_T of transistors make the design of UWB circuits in CMOS an extremely challenging task.

Two proposals- Multi-Band OFDM and Direct-Sequence CDMA have been put before the IEEE 802.15.3a task group to decide on the industry standard for the commercial deployment of this technology. Though the debate on which standard is better has not been resolved, proponents of both the groups have already begun to develop prototypes of their respective proposals.

This thesis describes the design of a key RF block in the UWB transceiver – the Power Amplifier. For the first part of this work, a PA suitable for MB-OFDM specifications was designed and fabricated in TSMC 0.18μm CMOS technology. The class-AB PA is able to cover the lower UWB frequency band from 3.1 GHz to 4.75 GHz and delivers an output power of -2 dBm at 4 GHz. Simulated results show a gain of 19±2 dB achieved over the entire band and the PA consumes 36.54 mW from a 1.8V supply.

In the second part of this work, a PA that meets the DS-CDMA specifications was designed and fabricated. This PA operates in the class-AB regime, delivering an output power of -4.2 dBm with input-1dB compression point at -22 dBm. Complete design and implementation was done using TSMC 0.18μm CMOS technology and it consumes a very low power of 25 mW, while realizing a flat gain of 19±1 dB across the whole band of operation. All the above mentioned results are from simulations in SpectreRF and measurements are yet to be taken. Additional features like power ON/OFF scheme and output impedance control has also been incorporated in the design.

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This work is wholly dedicated to my parents and to my sister who have constantly showered their support and love during my accomplishments here. Nothing would have been possible without their relentless support. I also thank my past and present room mates for making me feel comfortable at home even though we are thousands of miles away from home.

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Chapter 1

Introduction

Ultra wideband (UWB) radio is the modern re-incarnation of a century old type of communication. The first cross-Atlantic wireless transmission by Guglielmo Marconi used spark-plug transmitters that can be thought of as impulse based UWB transmission [1]. Today, the same technology is being revisited for its immense potential in high data rate communications.

Ever since the FCC allocated 7.5 GHz (from 3.1 GHz to 10.6 GHz) for UWB technology, interest has been renewed in both academic and industrial circles to exploit this vast spectrum for short range, high data rate wireless applications [3]. The great potential of UWB lies in the fact that it can co-exist with the already licensed spectrum users and can still pave the way for a wide range of applications.

However, this wide bandwidth complicates the circuit implementation of key RF blocks such as the power amplifier (PA), transmit/receive switch, low noise amplifier (LNA) and mixers in an UWB radio. Though expensive technologies like SiGe (Silicon-Germanium) or GaAs (Gallium-Arsenide) have been used for transceiver realizations, CMOS technology is more desirable for a single-chip, low-cost solutions. However, some inherent limitations of CMOS (low breakdown voltage, poor passive components, lack of accurate models etc.) makes designing CMOS RFIC's (Radio Frequency Integrated Circuits) at such high frequencies and such a wide bandwidth a challenging task. Nevertheless, with current technology scaling and advances in CAD based models, CMOS is quickly catching up as the preferred choice for RFIC's.

Though UWB has been allotted a spectrum spanning 7.5 GHz, the entire bandwidth may not be used for initial transceiver deployments. The U-NII (IEEE 802.11a) system band falls in the center of the UWB band and hence a narrowband spectrum above 4.9 GHz is avoided for practical reasons. Another consideration is the received power when operating at very high frequencies above 5 GHz. The received power is a function of the transmitted power and the path loss, which are a function of the lower and upper frequencies of the operating bandwidth. Measurements revealed that for the same transmit power and a distance of 10m, the received power increases by only 2 dB when the frequency is extended up to 7 GHz (3 dB for 10.6 GHz) [11]. In terms of circuit realizations, this improvement comes at a disproportionately higher circuit complexity and higher power consumption. Hence current CMOS RF circuit design focus on the lower frequency band of the UWB spectrum: approximately 3.1-5 GHz. However, future advances in CMOS technology would enable designers to implement CMOS RF circuits covering the entire band allocated to UWB.

There is an ongoing debate for the IEEE physical layer (PHY) standard for UWB standardization. The IEEE 802.15.3a Wireless Personal Area Networks (WPAN) task group [10] is still contesting between MB-OFDM (Multiband-Orthogonal Frequency Division Multiplexing) and DS-CDMA (Direct Sequence-Code Division Multiple Access) proposals. MB-OFDM scheme has been proposed by a group of about 170 companies that include Intel, Texas Instruments etc [11]. In this scheme, data is transmitted using OFDM on different bands in a time-interleaved fashion. Each band has a minimum bandwidth of 500 MHz and frequency hopping is employed to cover a wide bandwidth. On the other hand, DS-CDMA scheme, proposed by Xtreme Spectrum and its alliances [13], uses traditional impulse UWB with M-ary Bi-Orthogonal Keying and a CDMA encoding scheme for multiplexing and channelization. Both the schemes have their merits and de-merits and the debate on a better standard is still unresolved.

This thesis investigates the design of a monolithic CMOS RF Power Amplifier for UWB radios. We have implemented, fabricated and tested two different PAs, which can be applied for the two proposals respectively. Our low-power PAs cover the frequency

band up to 5 GHz and can deliver an output power >-8 dBm to a 50 Ω load. The PAs were fabricated in TSMC 0.18 μm, 1.8 V CMOS process along with other RF front-end blocks of a transceiver. Though advanced 0.13 μm CMOS technology is widely used for very high frequency RF applications, the prohibitive costs involved can necessitate the need for 0.18 μm technology.

The material in this thesis is organized as follows. In chapter 2, some UWB preliminaries and a brief discussion about the two proposals are presented. Chapter 3 introduces concepts and the background related to the design of power amplifiers. Chapter 4 and Chapter 5 present the specification, design, and implementation of a power amplifier targeting for MB-OFDM and DS-CDMA proposals respectively. The testing results of our power amplifier for MB-OFDM are presented as well. Chapter 6 concludes this research effort with some future directions.

Chapter 2

Preliminaries

2.1 Introduction

This chapter provides background theory relevant to our research in UWB radios and describes the two proposals put forth to the IEEE 802.15.3a WPAN standards committee.

2.2 UWB Basics

By traditional definition, ultra wideband technology employs very narrow pulses, of the order of a few nano-seconds, in order to establish high data rate communications [3]. These narrow pulses translates to energy spread over a wide frequency band, and hence the name ultra-wideband (also called Impulse radio). Very high data rates can be achieved over a short distance in devices employing the UWB technology.

On Feb. 14 2002, the Federal Communications Commission (FCC) opened up the spectrum from 3.1 GHz to 10.6 GHz for unlicensed use of the UWB technology. Having such a huge and free spectrum at one's disposal is especially alluring for the industry and academia alike. However, one of the important conditions is that the power levels of the UWB signal in this spectrum must be low enough to avoid interference with the already existing technologies. The FCC specifies the power emission levels suitable for co-existing with other technologies in the UWB allocated band [2]. The spectrum mask for both indoor and outdoor emissions is shown in Fig. 2.1.

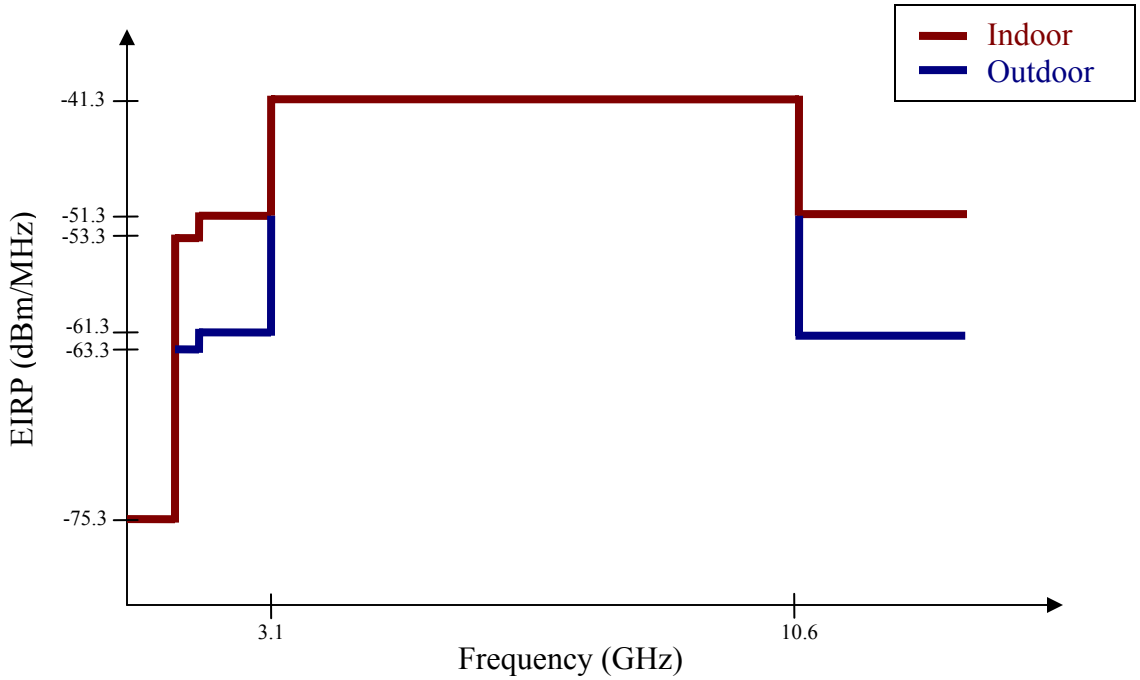


Figure 2.1: Acceptable power levels for indoor and outdoor emissions

The FCC defines a UWB transmitter as "an intentional radiator that, at any point in time, has a fractional bandwidth equal to or greater than 0.20 or has a UWB bandwidth equal to or greater than 500 MHz, regardless of the fractional bandwidth."

Fractional bandwidth is the bandwidth expressed as a fraction of the center frequency. If f_H is the highest frequency limit with signal 10dB below peak emission and f_L is the lowest frequency limit with signal 10dB below peak emission, the fractional bandwidth is defined as

$$\eta = \frac{2(f_H - f_L)}{f_H + f_L} \tag{2.2}$$

For UWB, the limits of η are given by $0.20 < \eta < 1.0$.

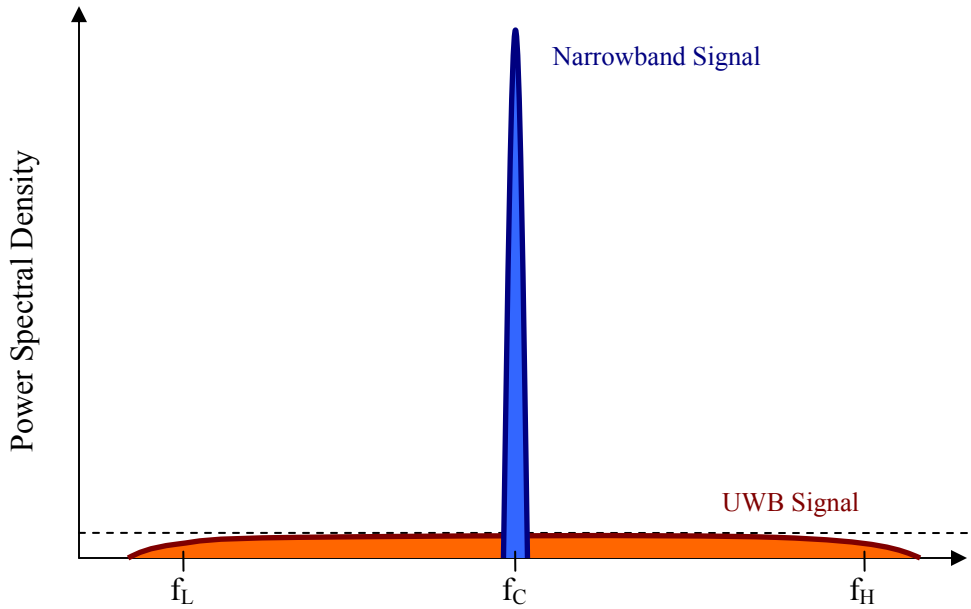


Figure 2.2: Power levels of UWB signal and a typical narrowband signal

2.3 UWB Applications

The wide spectrum allocated to UWB directly translates into a wireless channel with high spatial capacities. This is obtained from the famous Shannon's channel capacity theorem

$$C = B.\log_2(1 + SNR) \tag{2.1}$$

where C is the channel capacity in bits/second, B is the bandwidth in Hertz and SNR is the Signal-to-Noise Ratio.

Expression 2.1 shows a linear relation of the channel capacity with bandwidth and logarithmic relation with the SNR. Unlike narrowband systems whose data rate is limited by the bandwidth and SNR, UWB systems can achieve high data rates while operating below the noise floor. Nevertheless UWB is power limited which indirectly limits the overall channel capacity.

With attractive features like excellent multipath immunity and good immunity to external interference, UWB technology is projected to revolutionize a wide array of applications. The key for several applications is also the lower frequency content involved. Some of the potential applications of UWB include:

- Military communications
- Short range covert communication devices
- Collision avoidance sensors
- Ground-penetrating Radar
- Through-the-wall Radar
- Emergency motion and imaging
- Security devices
- Home networking without physical connections
- Radio Frequency Identification (RFID) devices

2.4 UWB Standards

The IEEE 802.15.3a task group, set up to investigate physical layer for next generation wireless PAN's, is considering UWB as the candidate for the physical layer. Though many proposals have been considered, two of them, DS-CDMA and MB-OFDM are the only promising candidates that are still vying for approval from the standards committee.

The DS-CDMA proposal, put forth by Freescale (formerly Xtreme Spectrum) and its associate companies, divides the entire allocated spectrum into two bands. Though initial proposals covered the entire 7.5 GHz bandwidth, later versions excluded the 802.11a WLAN band. The frequency ranges for this proposal are from 3.2 – 5.15 GHz and 5.825-10.6 GHz. The DS-CDMA scheme uses traditional impulse UWB with M-ary Bi-Orthogonal Keying and a CDMA encoding scheme for multiplexing and channelization. The concept is illustrated in Fig. 2.3.

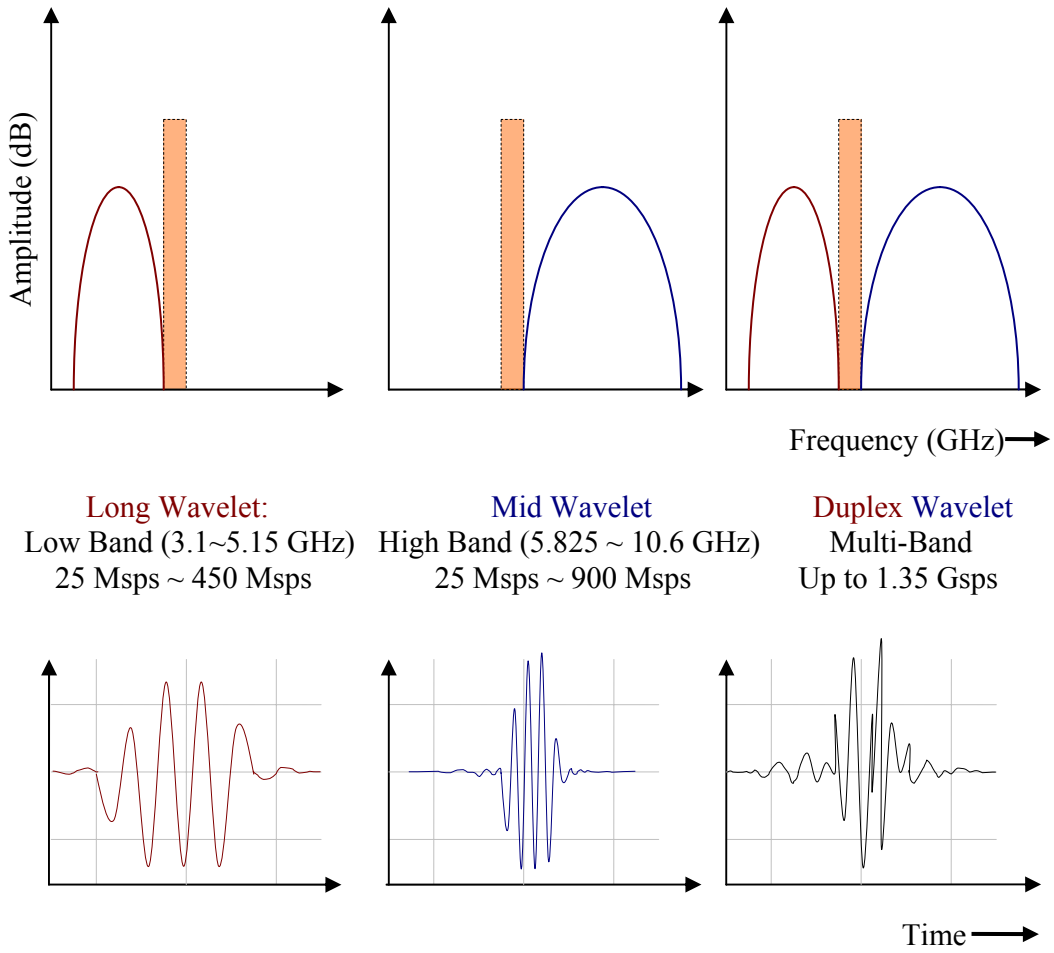


Figure 2.3: Time and frequency waveforms of DS-CDMA proposal (From [11])

The MB-OFDM (Multi-Band Orthogonal Frequency Division Multiplexing) proposal was put forth by a group of major companies like Intel, TI etc. In this approach, the spectrum is divided into 14 bands (each with bandwidth equal to 528 MHz), and devices are allowed to statically or dynamically select which bands to use for transmission. Further, OFDM is used in each of these bands. The data is then appropriately modulated using a concatenation of these bands.

The entire spectrum is divided into 4 distinct groups. Only Group-A spectrum is intended for first generation devices because of current technology limitations. Other groups have been reserved for future use.

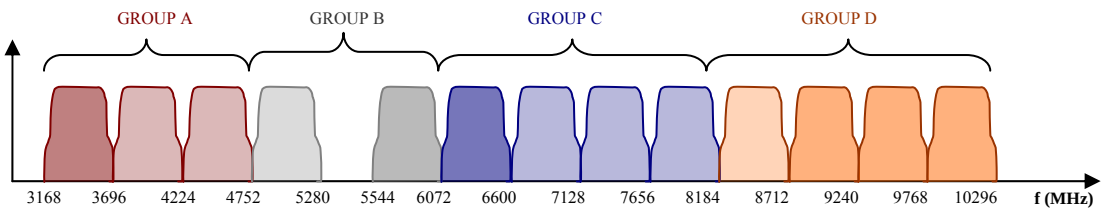


Figure 2.4: Band plan of MB-OFDM proposal (From [12])

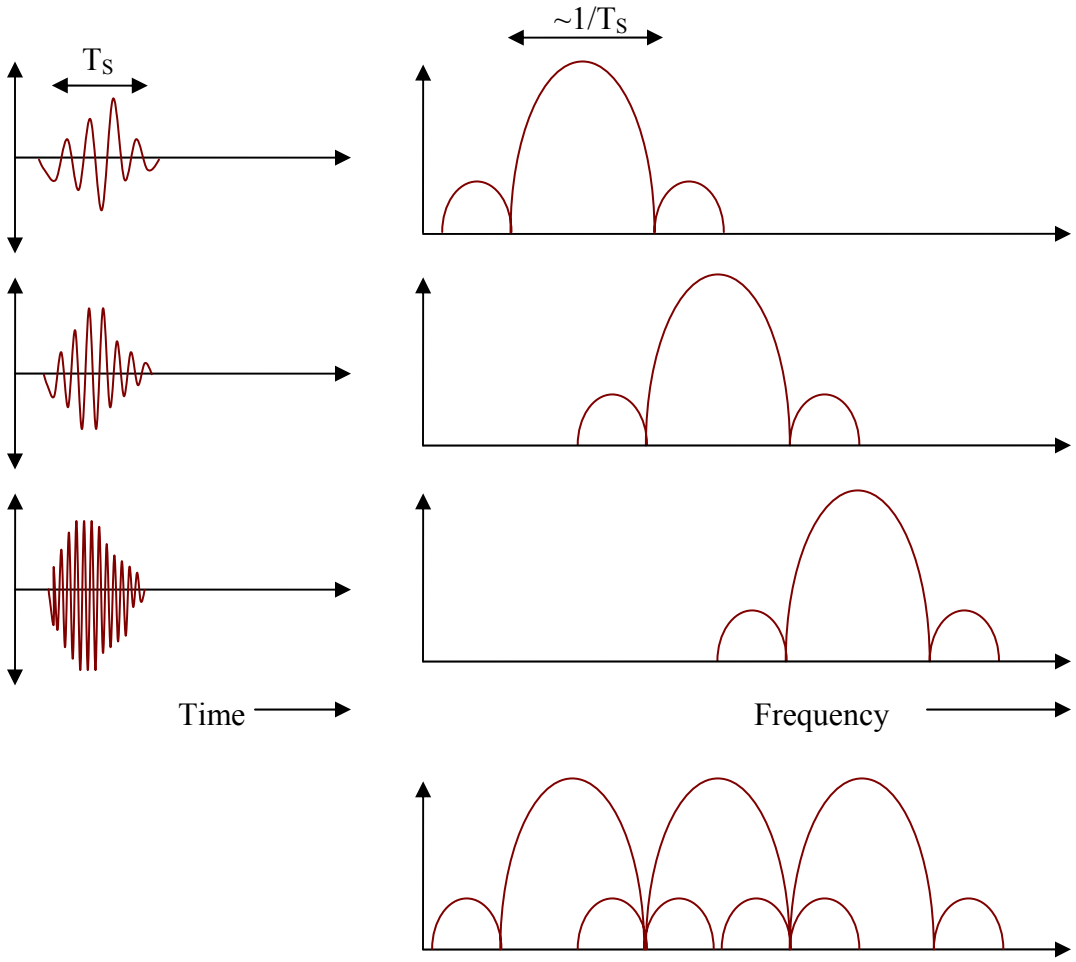


Figure 2.5: Time and frequency waveforms of DS-CDMA proposal

DS-CDMA claims to achieve high speed, low power consumption, low cost and small size. However, signal processing at high speeds of 100Mbps and above in the digital domain is a major concern for system designers. Timing synchronization, choice of technology (SiGe v/s CMOS), and sensitivity to ISI (inter-symbol interference) are also serious issues with this approach. On the other hand, MB-OFDM is thought of to be a more practical solution for global regulation, less sensitive to timing synchronization errors and easily realizable in CMOS. However, the opponents are questioning the circuit complexity, MAI (multiple access interference) and FCC compliance of this proposal. Before this deadlock can be resolved by the standardization committee, both the groups have decided to implement their respective proposals and verify its viability.

Chapter 3

UWB Power Amplifiers

3.1 Introduction

Power Amplifiers (PA) are a key part of the RF front-end in any transmitter. It is usually the last stage of the transmitter end and a very power-hungry block. PAs boost the signal power high enough such that it can propagate the required distance over the wireless medium. Typically, this power is delivered to an antenna which acts like a 50 Ω load. The output power level from a PA is determined by the application it is designed for. It can range from a few milli-watts for home networks to hundreds of watts at base stations

In UWB systems, the power level from the UWB transmitter should be small enough not to interfere with the already existing communication systems. This mandates the use of low output power levels; less than -41.25 dBm/MHz (as specified by the FCC). As a result, UWB systems need not require large transistors as part of the power amplifier circuit and this indirectly translates to lower power consumption. However, achieving a high gain and good impedance match over the entire frequency band makes the design a challenging task.

3.2 Specifications of the PA

In this section, some of the important terms and specifications related to a PA are discussed.

3.2.1 Frequency range of operation

In a narrowband application, the PA is designed for a particular frequency range and all the parameters are measured at that frequency. However, the frequency range to be covered for UWB radios is of the order of several GHz. The two proposals, MB-OFDM and DS-CDMA, have options covering the lower band of 3.1 to 5 GHz for initial deployment of UWB radios. So the PAs considered in this thesis target the 3.1 to 5 GHz range.

3.2.2 Output power

This parameter determines the amount of power that needs to be delivered to the load. As mentioned earlier, UWB transmitters are required to deliver very low output power of the order of a few hundreds of micro-watts. For a 2 GHz bandwidth and the average power level less than -41.25 dBm/MHz, the peak output power is approximately -8 dBm or 160 μW.

3.2.3 Efficiency

A measure of how efficiently the supply power is translated to output power is given by the efficiency.

$$\eta = \frac{Power\ delivered\ to\ load}{Power\ drawn\ \ from\ the\ source} \tag{3.1}$$

A 100% η implies that the entire supply power is delivered to the load. However, this is practically impossible to achieve.

The best way to improve the efficiency is the use of circuit techniques such that both voltage and current waveforms do not exist simultaneously. Switching amplifiers use this approach to achieve efficiencies up to 80%. However, as a trade-off, linearity needs to be compromised for better efficiency.

When comparing PAs with different input power levels, PAE (Power Added Efficiency) is a commonly used metric.

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{3.2}$$

Rewriting the above equation in terms of gain,

$$PAE = \frac{P_{in}(Gain - 1)}{P_{DC}} \tag{3.3}$$

However, for UWB applications, the input power levels are very low and hence as we will see later, the PAE can be misleadingly low. Instead, we emphasize high gain and low power as the appropriate metric for our PA's.

3.2.4 Power Gain/Voltage gain

PA's are required to boost the transmitted signal by providing a signal gain to the output of the preceding stage, usually a mixer. Power/Voltage gain is the ratio of output power/voltage (delivered to the load) to the input power/voltage (available from the source). The power gain will be equal to the voltage gain of the amplifier only if the input and output impedances are the same.

3.2.5 Gain Flatness

This is the measure of uniformity of the gain across the wide frequency range of interest. This parameter commonly used for wideband systems can impact pulse distortion in impulse-based UWB. It is desired that the gain be flat over the frequency band, typically with a tolerance of ±0.5 dB.

3.2.6 Linearity

Linearity is an important metric of any amplifier. It is desired that the amplifier operate with high linearity i.e., the output power be linear with input power. However, a device eventually saturates after a certain input power, and this introduces harmonics in the output power spectrum. Linearity in power amplifiers is of serious concern because they can be often made to operate in the non-linear region to deliver a large output power. 1-dB compression and third order intercept points are typically used to measure linearity.

1-dB compression:

As the name suggests, this is the input power at which the linear gain of the amplifier has compressed by 1 dB. The output referred 1-dB compression point (in dB) would then be given by the sum of the input referred 1-dB point (in dB) and the gain of the amplifier (in dB). This metric is a often used measure of the linear power handling capability of the PA.

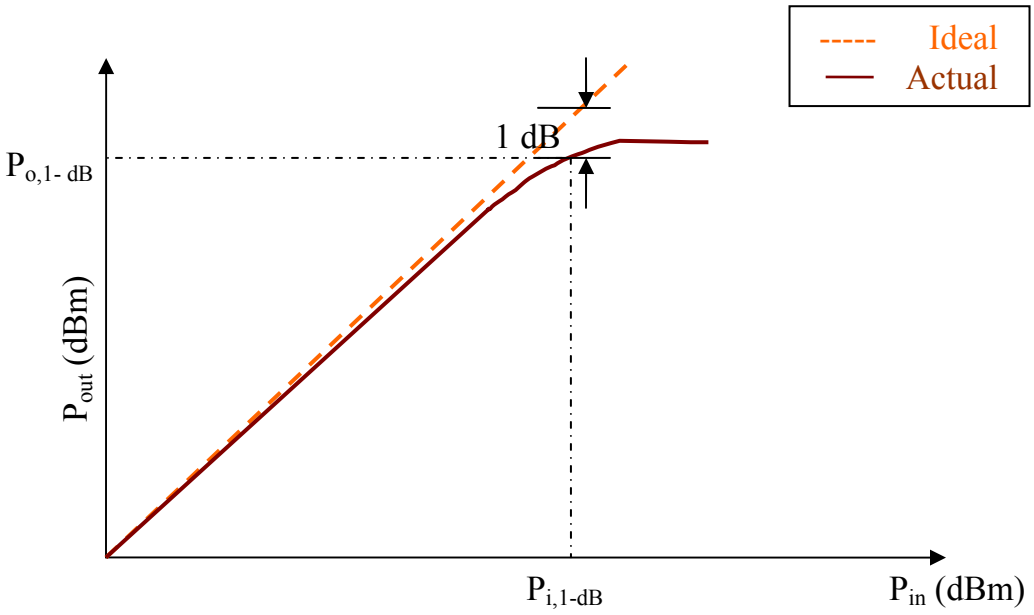


Figure 3.1: 1-dB Compression characteristics

Third-order intercept point:

This is a useful metric when comparing RF blocks with different specifications as it is independent of the input power levels. Assuming two interferers very close to the desired frequency, a non-linear output from the amplifier will generate inter-modulation products. The most important of the products is the third order product since it falls directly in the frequency band of interest. This situation is shown in Fig. 3.2 (a).

The amplitude of this IM3 product term increases in the order of cube of the fundamental amplitude and can be as significant as the fundamental tone after a certain input power. Fig. 3.2 (b) shows a plot of the IM3 product as a function of the input RF

level. The third-order intercept point is the extrapolated intersection of this curve and the fundamental power. The input/output referred IP3 can be estimated from this plot.

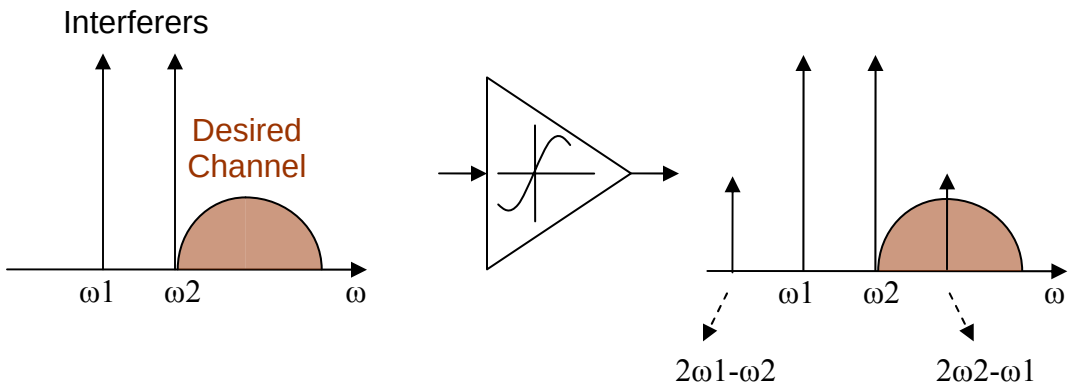


Figure 3.2 (a): Corruption of signal due to nearby interferers

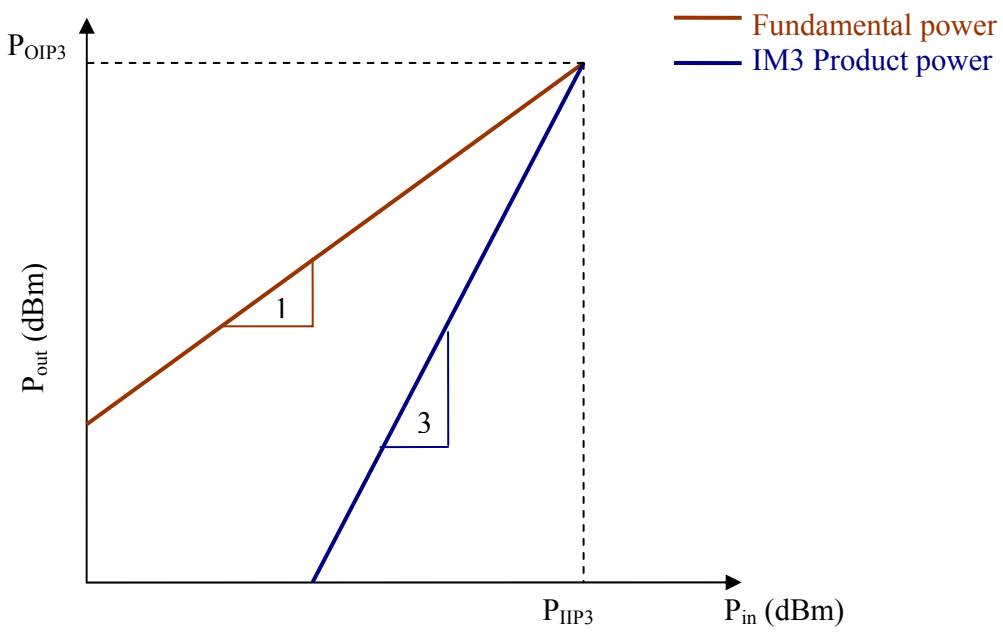


Figure 3.2 (b): Third-order Intercept calculation

Linearity can often be traded-off with efficiency depending on the class of operation. The choice of high linearity versus efficiency is based on the type of modulation used for transmission. For constant envelope modulation schemes like GMSK, FSK, the amplitude remains constant and the data is modulated using the phase

of the carrier signal. Whereas in non-constant envelope modulation schemes like CDMA, the amplitude of the signal also carries some data information and hence it is important to maintain the exact shape of the signal without introducing any distortion through the power amplifier. Extremely linear power amplifiers are required for non-constant envelope modulation techniques, while the linearity can be traded-off for better efficiency in constant envelope modulation schemes. Thus, the linearity requirements for MB-OFDM based UWB is more relaxed when compared to that of impulse based UWB.

Alternatively, techniques exist to improve the linearity while maintaining a good efficiency. Examples of such techniques are Doherty Amplifiers, Envelope elimination and restoration, Feed-forward technique etc.

3.2.7 Power consumption

In a typical transmitter, the PA consumes the most amount of power from the supply/battery. For portable devices, it is essential that this parameter be kept to a minimum. In UWB systems, the output power delivered is very low and hence the power consumption of the PA can be kept as low as possible. This can be achieved with smaller transistors and smaller bias currents.

3.2.8 Power control

One of the many power saving schemes, especially in cellular systems, is the use of power control circuitry. When the mobile system is near a base-station, a decision logic at the output of the PA senses that high output power levels are not required and the control circuitry controls the amount of bias/supply to reduce the power levels. The reverse operation is performed when the base-station is at a distance away from the mobile system. The battery life is thus improved, but at the expense of extra circuitry.

3.2.9 Power saving mode

Another power saving scheme is the use of power switching, wherein a switch transistor is used to turn off the power supply going into the core amplifier, thus reducing

the power consumption. This is particularly useful in UWB pulse based systems in which the transmitter might be idle for a long time after transmitting one pulse.

3.3 Classes of PA operation

Though there are different classifications for PAs, the most widely used is the distinction between linear and switching amplifiers. In linear amplifiers, the output amplitude of the signal is a linear function of the input amplitude. Class A, B, and AB amplifiers come under this type where the output transistor acts as a current source and the average output impedance during the operation is relatively high. The current and voltage waveforms through and across the output device are often full, or partial sinusoids. In switching amplifiers like Class-E, F and S, the power amplifier is driven with a large amplitude signal, turning the device ON or OFF as a switch. These amplifiers can achieve a very high efficiency at the expense of linearity.

Fig. 3.3 shows the basic topology of a PA. It usually consists of a power device (transistor), the input and output matching networks and some extra circuitry like the bias network, harmonic traps etc. The choice of PA class, the type of transistor and the choice of matching networks are dependent on its target application.

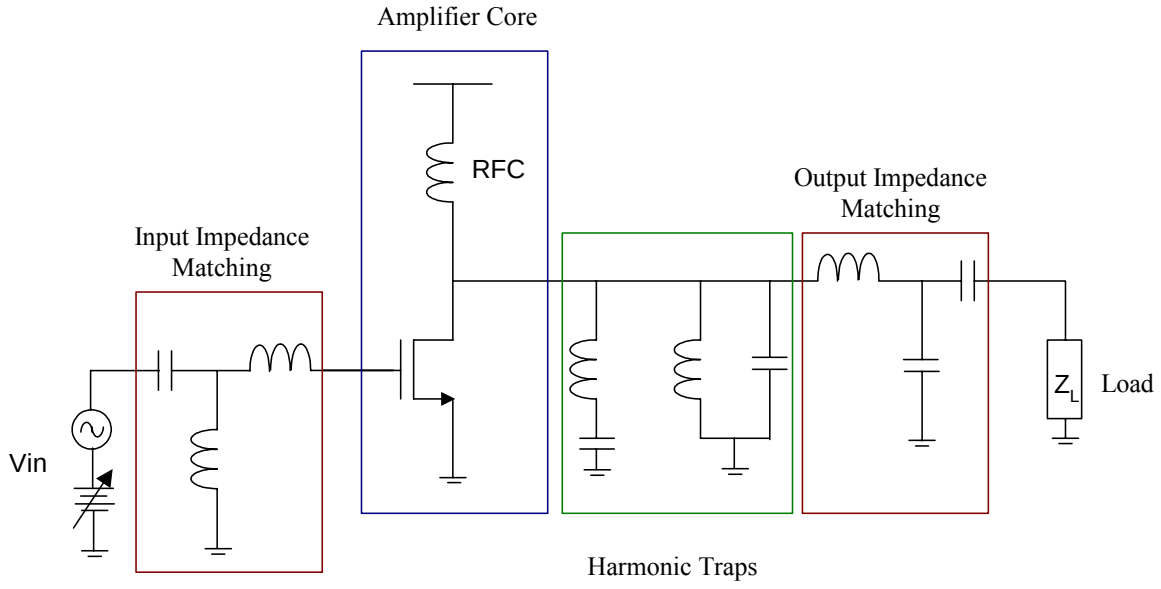


Figure 3.3: A basic PA topology

3.3.1 Linear Amplifiers

Linear amplifiers operate at constant gain and are based on the load-line theory, which states that the maximum power a transistor can deliver to a load is determined by the supply voltage and the maximum current of the transistor.

When the transistor load is a large inductor/RF choke, the maximum voltage swing possible at the drain of this transistor is 2*supply voltage. The load line (of the optimum load resistance) for maximum output power is plotted from

$$R_{l,opt} = \frac{2V_{\max}}{I_{\max}} \tag{3.4}$$

In other words, PAs can deliver maximum power to a load given by $R_{L,opt}$. This resistance is then transformed to 50 Ω using an impedance transformation network.

In CMOS PAs, $R_{L,opt}$ would be very small and hence the design of impedance transformation network becomes a major bottleneck. Even with technology advancements, passive networks in CMOS have poor properties causing power loss at the output. Fortunately for UWB, the transistor need not be driven for these maximum power conditions and this relaxes the overall PA design when considering the design of matching networks.

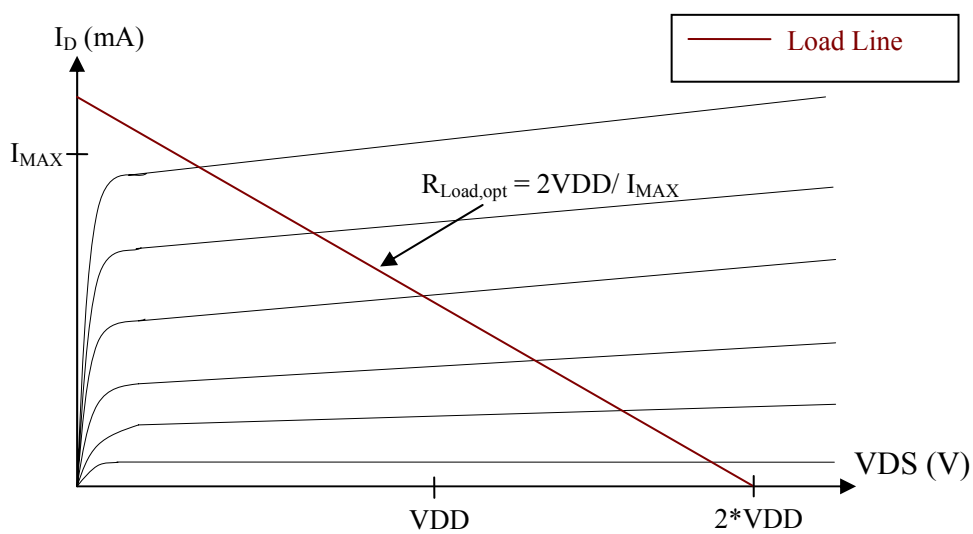


Figure 3.4: I-V characteristics of a typical transistor

The class of operation is determined by the operating point on the load-line i.e., from the I/V characteristics of the transistor. Fig. 3.5 shows the bias point for a transistor in Class-A operation. Here the transistor is biased at the center of the load line i.e., the transistor is in the active region at all times and the output voltage/current swings are maximum. The conduction angle α, which is the time for which the device is conducting, is equal to 2π in class-A amplifiers (Fig. 3.8).

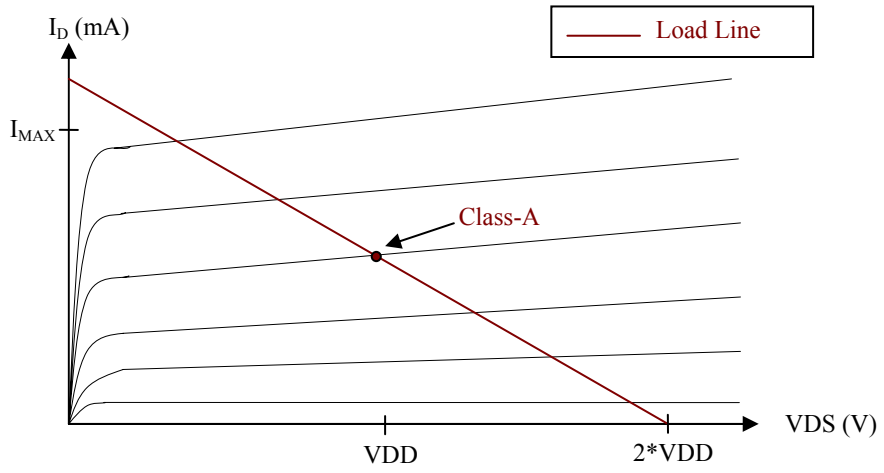


Figure 3.5: Class-A operation

The voltage, current and power waveforms of a class-A amplifier are shown in Fig. 3.6. As can be seen from the plots, the amplifier is always conducting, which results in a maximum efficiency of only 50%. However, the linearity is excellent as it preserves the input and output waveforms without any distortion.

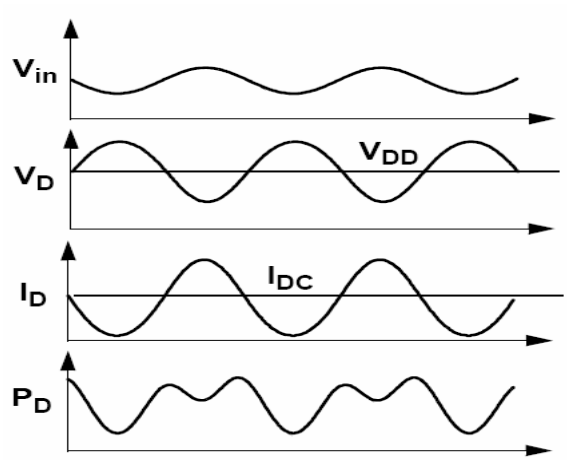


Figure 3.6: Class-A amplifier waveforms

Class-B amplifiers are biased at the threshold voltage of the transistor such that the conduction angle is now π (Fig. 3.8). The current waveform is positive only for one cycle of the input voltage. Hence the power consumption will be lower than class-A type. The optimal load resistance is now $R_{l,opt} = V_{max}/(I_{max}/2)$, which is the same as with Class-A type amplifiers. Theoretical efficiency is around 78%, but the linearity is worsened in these types of amplifiers. However, Class-B amplifiers also suffer from cross-over distortions at the switching points.

Class-A and B are two extremities of PA topologies in terms of efficiency and linearity. However, PA's operating in the region between these two operating points is widely used and they are aptly known as class-AB amplifiers. Good linearity and efficiency can be achieved with devices in this regime. The conduction angle now is $\pi < \alpha < 2\pi$.

Class-C amplifiers, which are non-linear, are biased below the cut-off region and their conduction angle is < π (fig. 3.8). With very low power consumption, the efficiency can reach up to 100%. However, the output power levels will also be quite low and unsuitable for most of the applications.

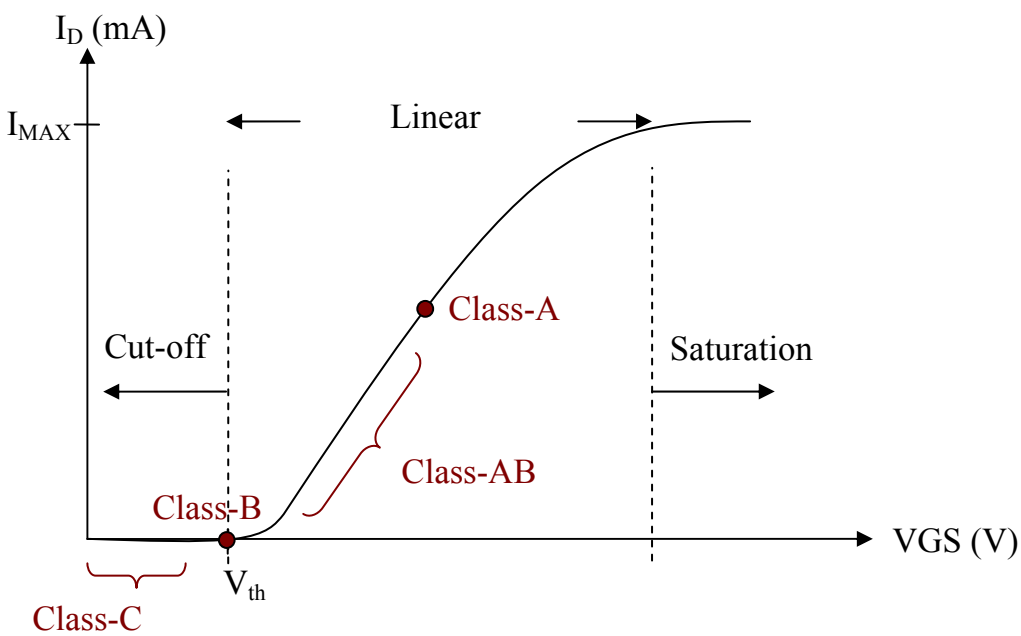


Figure 3.7: Q-point of Class-A, AB, B and C type amplifiers

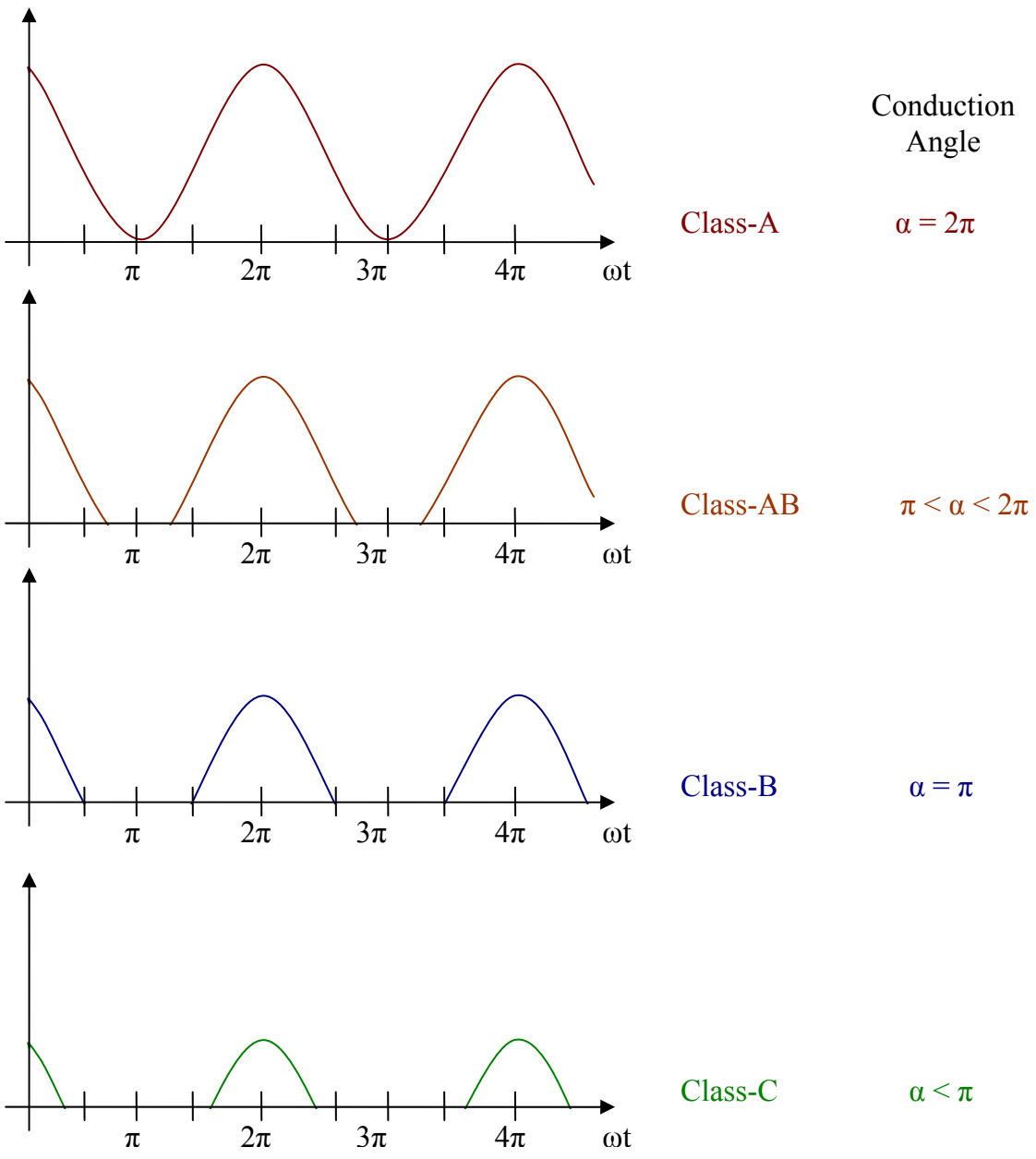


Figure 3.8: Conduction angle relations for linear amplifiers

3.3.2 Switching amplifiers

In switching amplifiers, the power amplifier is driven with a large amplitude signal, turning the device ON or OFF as a switch. They operate at constant input power (in saturated mode) and power control is obtained by varying the gain of the amplifier.

Class-E amplifiers are a relatively novel type of switching amplifier wherein the voltage and current waveforms are shaped using L's and C's in such a way to achieve an efficiency of 100%. Under ideal condition, the voltage of the switch transistor drops to zero and has zero slope just as the transistor turns on and conducts current. This ensures that neither voltage nor current exists simultaneously in the circuit, thus achieving 100% efficiency. Class-E amplifiers require only a single transistor and can operate at frequencies as high as tens of GHz. However, the shaping components in this amplifier are designed for a single frequency and hence cannot be used for UWB applications.

Class-F amplifiers employ harmonic resonators at the output to shape the drain waveforms. The harmonic traps are designed in such a way that the voltage waveform resembles a square wave (with the introduction of some harmonic components in the waveform) and the current wave resembles a half sine wave. Conversely, "inverse class-F" can also be designed. Again, both the voltage and current waveforms do not exist simultaneously, thus achieving good efficiency. With higher harmonics, the efficiency can be improved up to 100%, but linearity is severely worsened.

To summarize, the PA classification is given in Table 3.1.

Table 3.1: Summary of power amplifier classes

Class	***Modes***	***Conduction Angle (%)***	***Output Power***	***Maximum Efficiency (%)***	***Gain***	***Linearity***
A	Current Source	100	Moderate	50	Large	Good
B		50	Moderate	78.5	Moderate	Moderate
C		<50	Small	100	Small	Poor
D	Switch	50	Large	100	Small	Poor
E		50	Large	100	Small	Poor
F		50	Large	100	Small	Poor

3.4 Previous work on UWB power amplifiers

CMOS PAs for UWB transmitters were investigated in [19]. Christian Grewing et al. have implemented a 4-stage distributed amplifier in 0.13 μm CMOS process to cover the UWB band up to 8 GHz. Their PA achieves a small-signal gain of 17 dB with the 1-dB compression at +3.5 dBm.

Fig. 3.9 shows the schematic of the PA. The active transistor is divided into several stages connected by transmission lines to combine the transfer functions to the desired frequency behavior. The overall transfer function was shaped for higher bandwidth by the ratio and number of stages and the impedance and length of the transmission lines. The microstrip transmission lines is made up of metal layers where the top metal layer acts as signal conductor and the bottom layer as the ground plane.

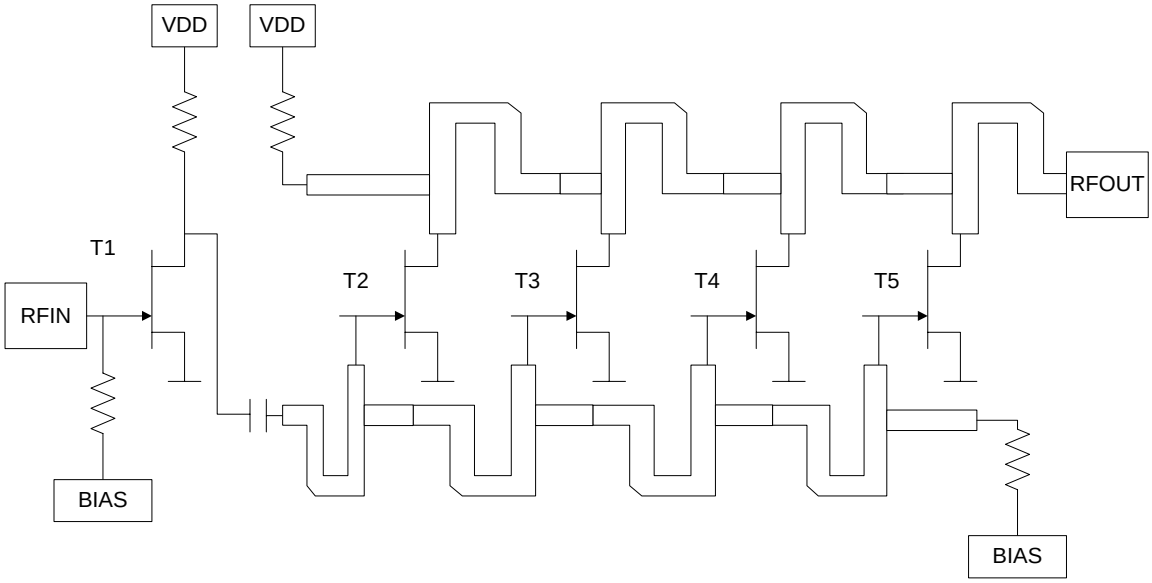


Figure 3.9: PA schematic [19]

Though this circuit achieves good linearity and frequency response, the power consumption is quite high (100 mW) for UWB applications.

Ansoft Corporations have recently proposed a UWB PA design that can be used for MB-OFDM specifications [20]. Though a chip level implementation has not be realized, simulations reveal that the PA covers a frequency band from 3.168 GHz to 4.752 GHz with an in-band gain >12 dB and a DC power consumption of 20 mW.

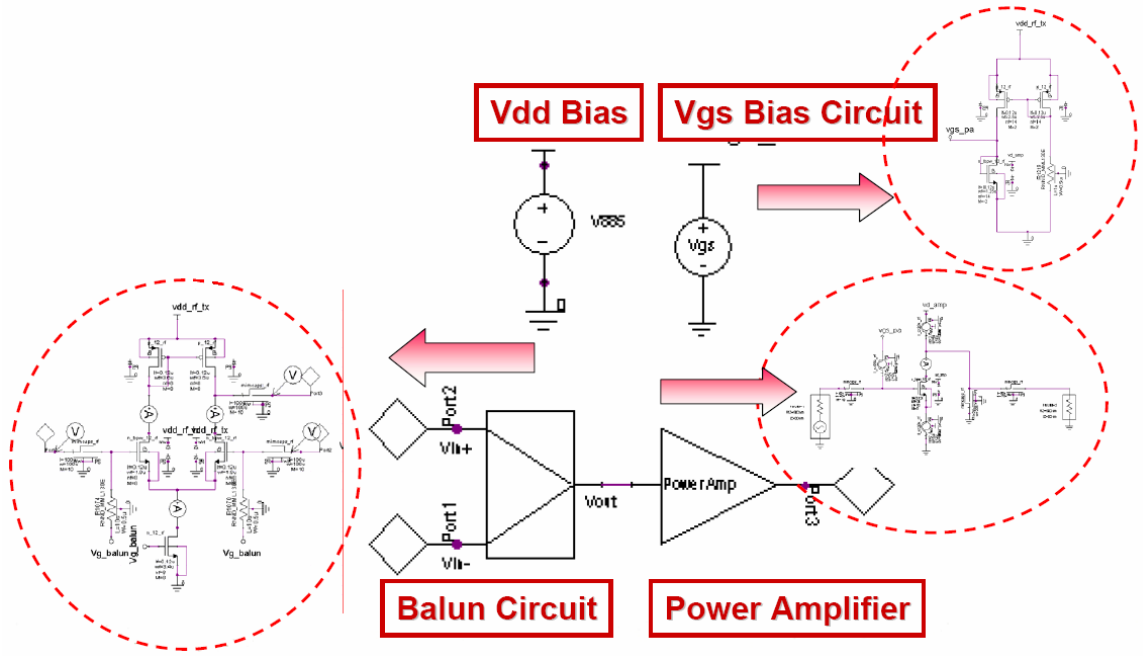
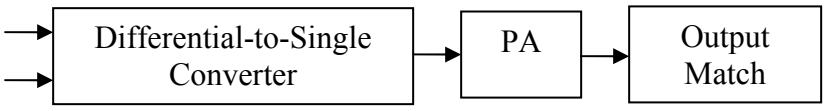


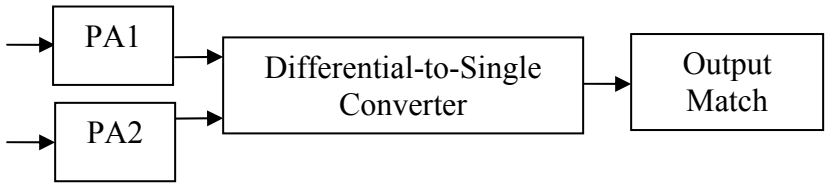
Figure 3.10: Top level PA schematic [20]

3.5 Design Topologies

Power amplifiers are usually preceded by an up-conversion mixer and followed by a T/R switch. A mixer output is typically differential to take the inherent advantages of differential topologies like good isolation and noise immunity. Therefore, the PA has to take differential inputs from the mixer and produce a single ended output to the T/R switch. Two different design approaches for a differential input-single ended output amplifier are shown in Fig. 3.11.



(a) Design-1



(b) Design-2

Figure 3.11: Realizations of differential input-single ended output PA

In design-1, the differential input is first converted to a single ended signal and then amplified. However, using separate power amplifiers for each single ended input relaxes the gain and linearity requirements on each of these PAs when compared to using a single PA. This technique is shown as design-2 in Fig. 3.11(b).

Either design can be used as the PA topology and in this thesis we have investigated both the designs. Design-1 was used for the MB-OFDM PA, while design-2 was used for the DS-CDMA PA. The implementation procedure and the performance comparisons are discussed in chapters 4 and 5.

Chapter 4

Power Amplifier design for MB-OFDM

Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM) technique was proposed by a group of companies that include Intel, Texas Instruments etc [11]. As described earlier in chapter 2, only group-A band of frequencies from 3.16 GHz to 4.75 GHz are being considered for the initial transceiver deployment. In this chapter we describe the design of a UWB PA covering this band of frequencies.

4.1 System Specifications

The specifications of our PA calculated based on the link budget of the entire transceiver, are given in Table 4.1. Some of the key specifications in the design of this PA are its frequency of operation, input impedance, power consumption, gain and the output power level. The mixer preceding the PA generates a differential output with an impedance of 200 Ω. Traditionally, all the impedances of any RF block are terminated to 50 Ω, especially to aid in the testing of these blocks. However, in our case, the output impedance of the mixer was designed for a larger value to improve its conversion gain. Since the impedances are different, the power gain and voltage gain would not be the same.

Table 4.1: Power Amplifier Specifications for MB-OFDM

Categories	*Specification*
Supply Voltage	1.8 V
Frequency range	3168 ~ 4752 MHz
Input P1dB	-22 dBm
Output P1dB	0 dBm
Maximum Output	> -8 dBm
Power gain	>15 dB
Voltage gain	>15 dB
Gain flatness	± 1 dB
S11-Input Return Loss	<-10 dB
S22-Output Return Loss	<-10 dB
S12-Isolation	<-30 dB
Efficiency	N/A
Power consumption	< 40 mW
Input Impedance	200 Ω(Differential)
Output Impedance	50 Ω(Single-ended)

When compared to a typical PA design, the difference in specifications is in the frequency of operation (2 GHz as opposed to a few MHz), and the low output power requirements (<0 dBm as opposed to >25 dBm).

The PA is required to deliver a peak output power >-8 dBm with a gain of 15 dB and a gain flatness of ± 1 dB across the band of interest. With such low output power, the DC power consumption can be kept below 40 mW.

4.2 Wideband matching techniques

The major challenge in the design of a UWB PA is its wide frequency range of operation. Typical narrowband applications use LC based networks to achieve matching at a particular frequency by exploiting the fact that the impedance of the network is resistive at the resonant frequency. In theory, this approach can be extended for wideband matching conditions [17]. However, when die area is limited, it is imperative that some performance metric be sacrificed for the area. This is especially true for broadband matching because multiple LC stages might be needed, and they can occupy a substantial die area.

The most primitive form of wideband input match is the use of resistive shunt-termination shown in Fig. 4.1 [18]. Though simple, this approach does not yield a good efficiency because a significant amount of power is wasted through the resistor.

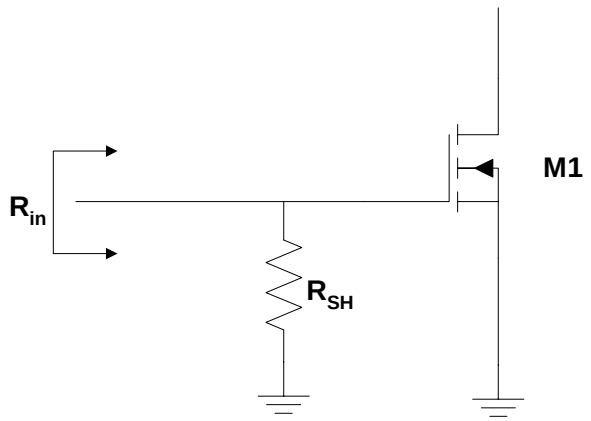


Figure 4.1: Resistive shunt termination for broadband matching

Another approach is to use a shunt feedback network (Fig. 4.2) usually comprising a resistor [18]. In this configuration the feedback network can be designed in such a way that it can provide the required match at both the input and output ends. This topology has the added advantage of providing stability to the amplifier and in achieving a flat gain response.

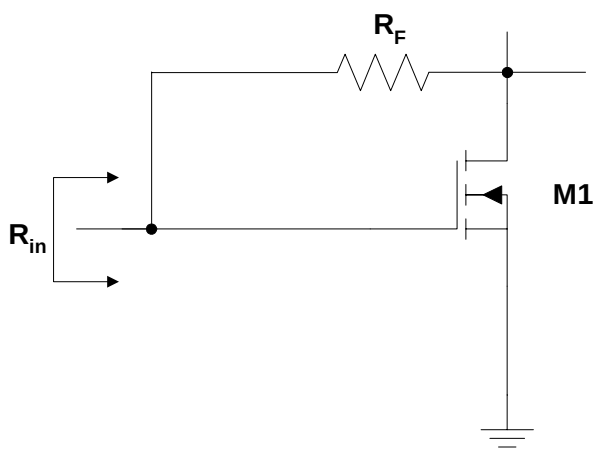


Figure 4.2: Resistive shunt feedback for broadband matching

For a transistor stage with gain A_v, the input resistance can be shown to be

$$R_{in} = \frac{R_F}{1 + A_v} \tag{4.1}$$

The value of the feedback resistance R_F has to be selected according to the matching and gain requirements of the amplifier. A small R_F (close to the desired impedance) can provide excellent matching, but the gain of the amplifier drops due to significant signal feedback through this path. On the other hand, a large R_F can provide good gain but reduces the effect of feedback. Through careful simulations, the optimum value of R_F can be achieved for the best matching and gain conditions.

4.2.1 Determination of feedback components

When the bandwidth requirements are really large, a straight-forward feedback resistor might not meet the requirements easily. Instead, some combination of passive/active elements might be needed in the feedback path.

Consider a practical common-source stage including the bond-wire inductance to ground that acts as source degeneration (Fig. 4.3).

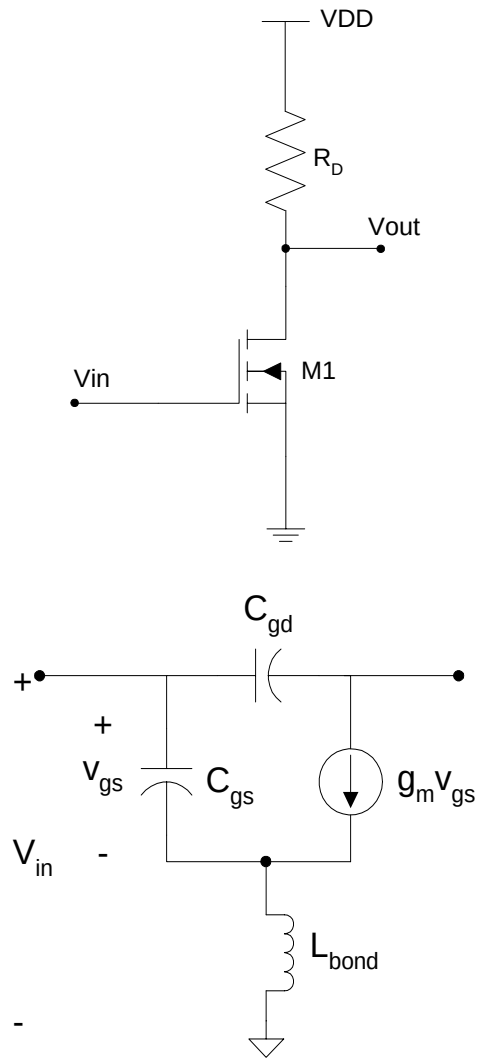


Figure 4.3: Common-Source amplifier and its small-signal model

If a feedback network Z_f is included to the amplifier in Fig. 4.3, the small signal equivalent can be redrawn as in Fig. 4.4, where

$$Z'_{in} = sL_{bond} + \frac{1}{sC_{gs}} + \frac{g_m L_{bond}}{C_{gs} + C_{gd}} \tag{4.2}$$

$$g_{m,eff} = \frac{g_m v_{gs}}{v_{in}} = \frac{g_m}{1 + sg_m L_{bond}} \tag{4.3}$$

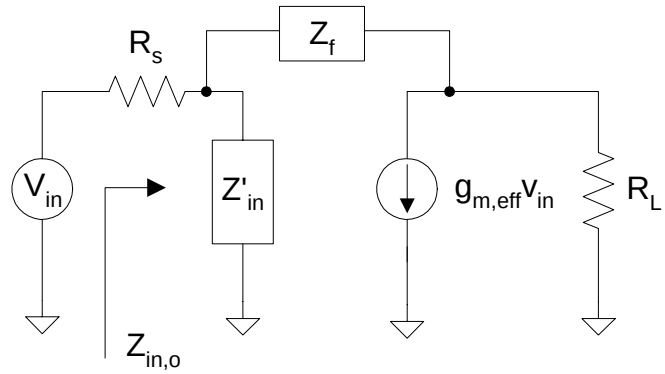


Figure 4.4: Small-signal model of CS-stage with the feedback configuration

For this configuration, the input and output impedances and the gain can be calculated to be

$$Z_{in,o} = \frac{Z'_{in} Z_f}{Z_f + (A_v - 1)Z'_{in}} \tag{4.4}$$

$$Z_{out,o} = \frac{Z_f + (R_s \parallel Z'_{in})}{1 + g_{m,eff}(R_s \parallel Z'_{in})} \tag{4.5}$$

$$A_v = \frac{R_L + g_{m,eff} Z_f R_L}{R_L - Z_f} \tag{4.6}$$

For a specified gain and impedance, plots of Z_f can be drawn at the desired frequency range of interest. Since the circuit parameters Z'_{in} and $g_{m,eff}$ are frequency dependant, the characteristics of Z_f will also vary accordingly over the frequency band. For example, consider the plot of Z_f shown in Fig. 4.5. This plot was constructed for a CS-amplifier with circuit parameters extracted from the design library of TSMC 0.18 μm CMOS technology kit. If this Z_f plot can be reproduced using some combination of R, L or C components, perfect matching and gain conditions can be achieved. The plot in Fig. 4.5 can be easily reconstructed using a series-RC combination as the feedback network. However, when designing for low noise or low power, the optimal solution for the feedback network can be realized only by tuning some of the circuit/transistor parameters and by iterating the above procedure. Various R,L,C combinations can reproduce the

same Z_f characteristics, but the trade-off between power, noise, gain and impedance match will eventually determine the best feedback network.

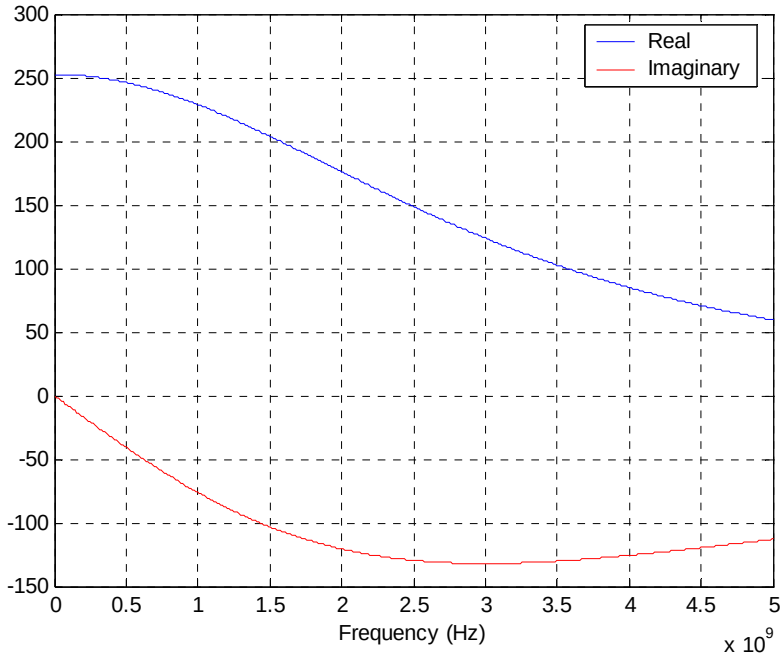


Figure 4.5: An example Z_f plot

The above described technique can be generalized to design any form of wideband matching using feedback networks. Our UWB PA for DS-CDMA application to be discussed in chapter 5 uses a series-RC feedback topology to realize wideband match at the input of the circuit.

4.3 PA Design

The MB-OFDM PA was designed and implemented using design-1 mentioned earlier in this thesis. This design includes a differential-to-single ended converter as the first stage and two common-source stages following it. The overall PA is a 3-stage design with the transistors biased in the Class-AB region.

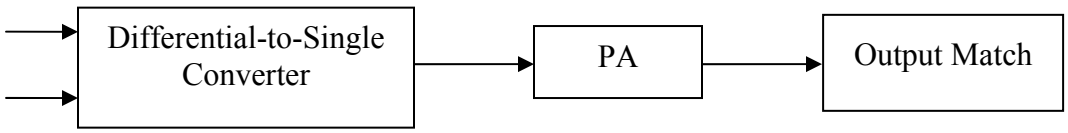


Figure 4.6: High level design strategy for the PA

Fig. 4.7 shows the operating regions of a 100 μm RF-NMOS transistor available from the Cadence Design Kit. The minimum length of the transistor for this process is 0.18 μm and the threshold voltage is approximately 0.52 V.

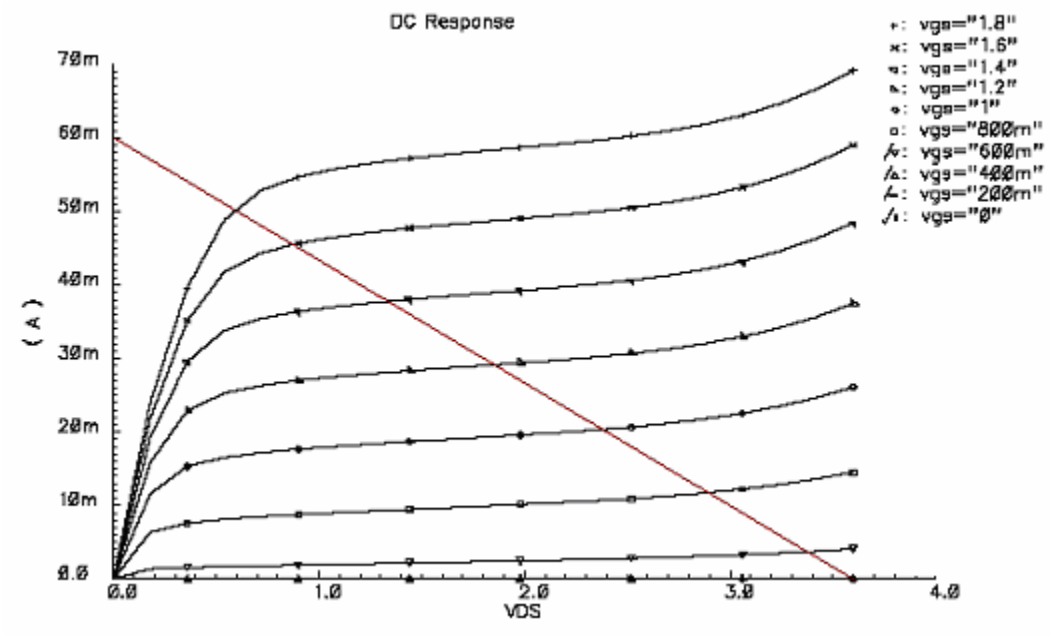


Figure 4.7 (a): IDS versus VDS characteristics for 0 V<VGS< 1.8 V

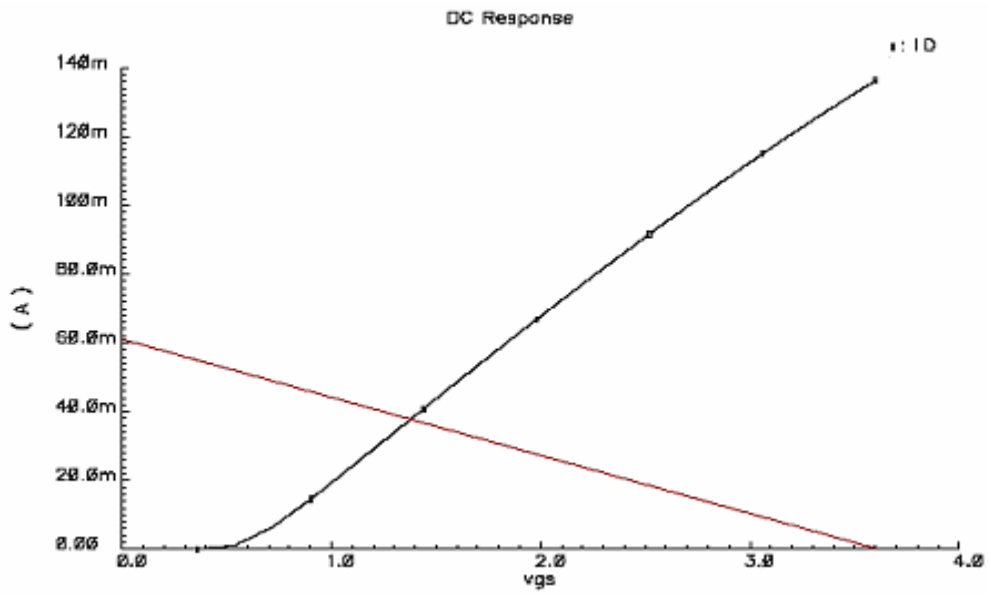


Figure 4.7 (b): IDS versus VGS characteristics with VDS=1.8 V

As can be seen from the plots, a VGS of 1.4 V would make the transistor to operate in Class-A region (from the discussion in 3.3.1 and Fig. 3.7), Class-AB for 0.52<VGS<1.4 V and Class-C for VGS<0.5 V.

4.3.1 Differential-to-single ended converter

The first part of the design was to realize a differential-to-single ended converter at the input side of the PA. One of the standard circuit topologies is to use a differential amplifier with current mirror load. This configuration is shown in Fig. 4.8. Two common-source connected transistors act as a differential pair and an active load formed by the current mirror generates the single-ended output. Though this stage can be designed to provide a very high gain, we have used it primarily as a simple converter with low power consumption. A tail current source is generally used to bias the transistors and this current source can also control the overall gain of the stage. However, in our design, we are biasing the transistor using a bias voltage applied at the gate of the transistor. This intends to include the bias resistor as a shunt termination for providing the wideband input impedance match.

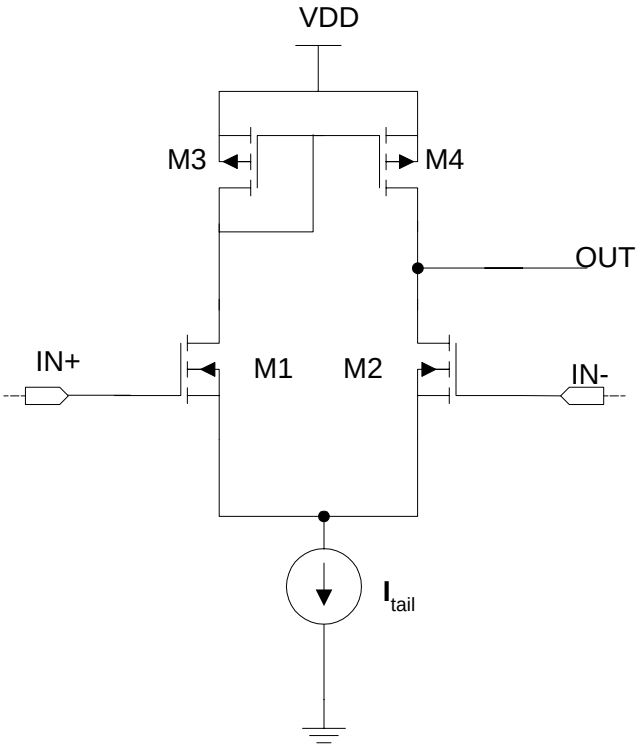


Figure 4.8: Differential-To-Single ended converter

4.3.2 PA stage design

The single-ended signal is then AC coupled to the first stage of the PA. This is done through a coupling capacitor, which must be large enough, so that there is no significant loss of signal across the coupling capacitor, due to the voltage division between the coupling capacitor and the gate capacitance of the PA stage [16]. Because of the space limitations, we designed this large coupling capacitor by combining 16 capacitors in parallel.

The output power from the amplifier is specified to be >-8dBm. This is equivalent to P_{out} = 0.16 mW. Assuming a P_{out} of 0.3 mW to a load of 50Ω, the output stage requires a peak-to-peak current of I_{PP}=7 mA ($P= I_{pp}^2R_L/8$). For a transistor to operate as a Class-A amplifier, the absolute minimum bias current is half of I_{PP}, but to achieve reasonable linearity, the bias current must be higher; leading to higher power dissipations.

The power consumption in the PA was specified not to exceed 40 mW. With a supply voltage of 1.8 V, that translates to a current of 22.2 mA. The transistor sizes were determined on the fact that they were to be operated in Class-AB operation and the current drawn should be around 10 mA per stage. The threshold voltage of the transistor provided in the library is around 0.52 V. Hence a bias of 0.8 V was decided to operate the transistor in Class-AB region. The transistor size was then fixed for this bias and it consumed 7 mA from the supply.

A single stage alone was not able to provide the required 15 dB gain. Hence, another stage was used as the final output stage of the PA. The signal from the first stage is again AC coupled using a 15.22 pF capacitor. To deliver adequate power, the transistor was sized at an appropriate value for the same bias of 0.8 V, drawing a current of 9 mA from the supply. The total power consumed by the whole PA circuit was later calculated to be 36.54 mW.

The PA stages also included small resistors of 80 Ω at the drain end of the transistor to improve the gain at lower frequencies.

4.3.3 Output stage design

The design of output stage is critical since a flat gain response can be realized with proper design techniques. Also, the output had to be matched to 50Ω. The RF choke (large inductance at the load of a PA: RFC), which is used to supply a constant current from the supply, can be used to aid in matching the output side if its size is not very large. The operating frequency can be pushed higher with a finite dc-feed inductor since the parasitic capacitance associated with the transistors is resonated out by the inductor. However, to achieve a wide match over 2 GHz, two stage matching was required.

The overall schematic of the PA is shown in Fig. 4.9.

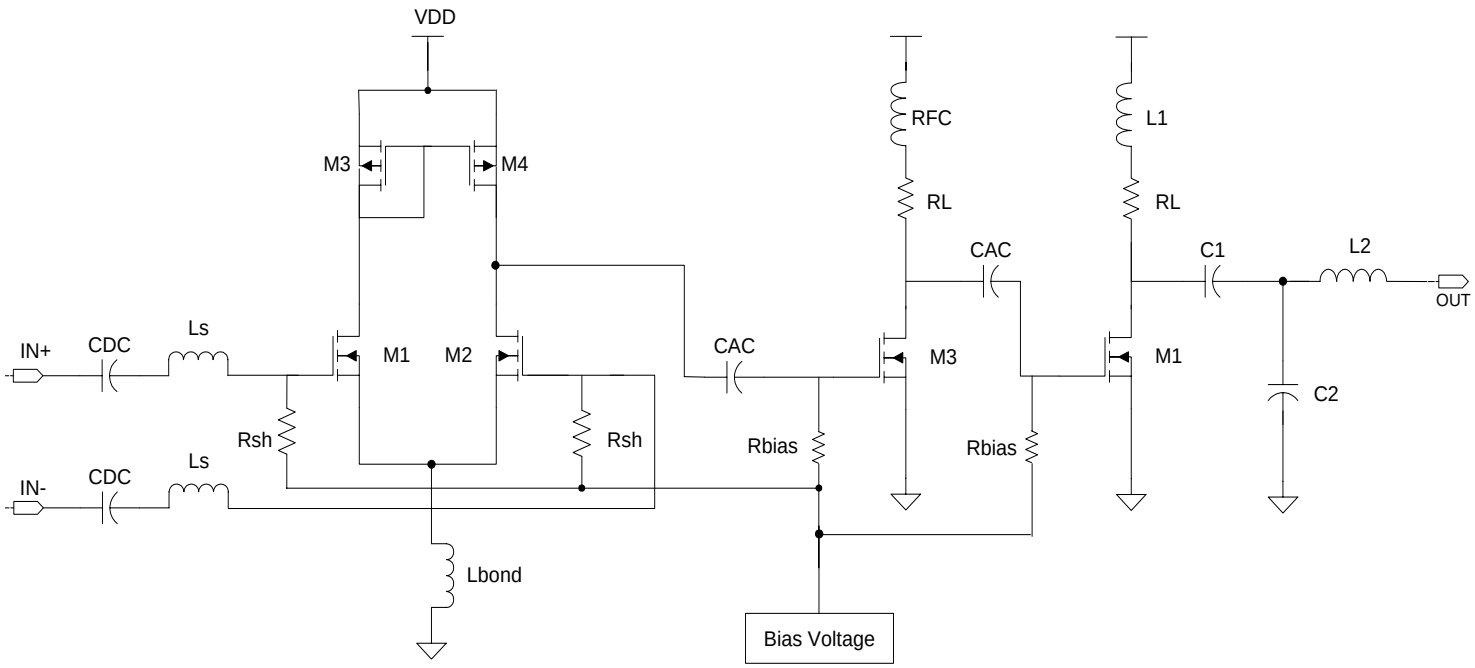


Figure 4.9: Complete PA schematic

4.3.4 Package model

For accurate simulation of any RF circuit, the equivalent model of the pad including the bond-wire also should be considered. In our case, we have used a wire-bond QFN (Quad Flat No-lead) package provided by Amkor Technologies (Fig. 4.10), and the typical equivalent model used is shown in Fig. 4.11.

QFN packages are known to provide exceptional benefits for high-speed circuits like improved heat dissipation, co-planarity and good electrical performance.

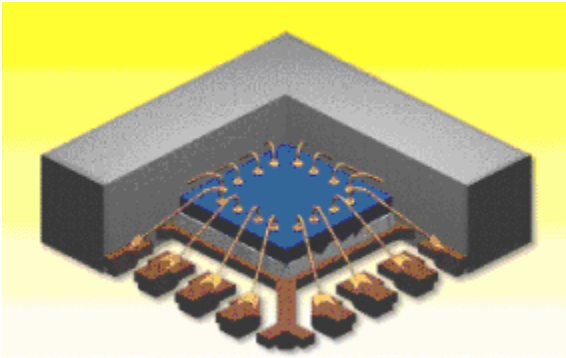


Figure 4.10: QFN package

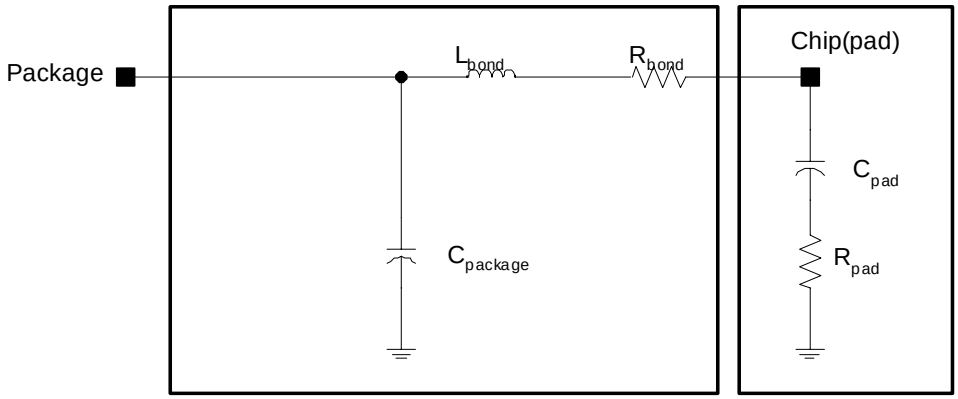


Figure 4.11: Wirebonding & Pad model

Ground Down-bonding:

In QFN packages, when the die area can accommodate more number of pads than the pins in the package, the free pads are down-bonded to a ground plane on the backside of the package. And the backside of the package is soldered to the PCB ground. Thus the circuit ground is formed from multiple ground wires that are connected from the chip's surface to the package. These multiple grounding also achieves low resistance and low impedance to ground. Fig. 4.12 shows the down-bonding equivalent of the pad and package with a lower bond-wire inductance and resistance.

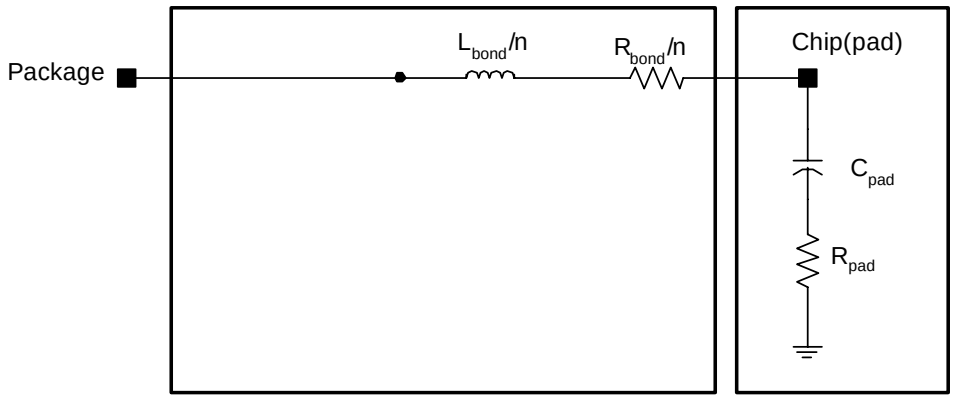


Figure 4.12: Down-bonding model

The values of bond-wire inductance, its associated resistance and the pad equivalent of the entire package were provided by the package manufacturer.

The final PA schematic including the package model is shown in Fig. 4.13. It should be mentioned that the component values, transistor sizes and other circuit-relevant parameters are not specified in this report due to IP related concerns.

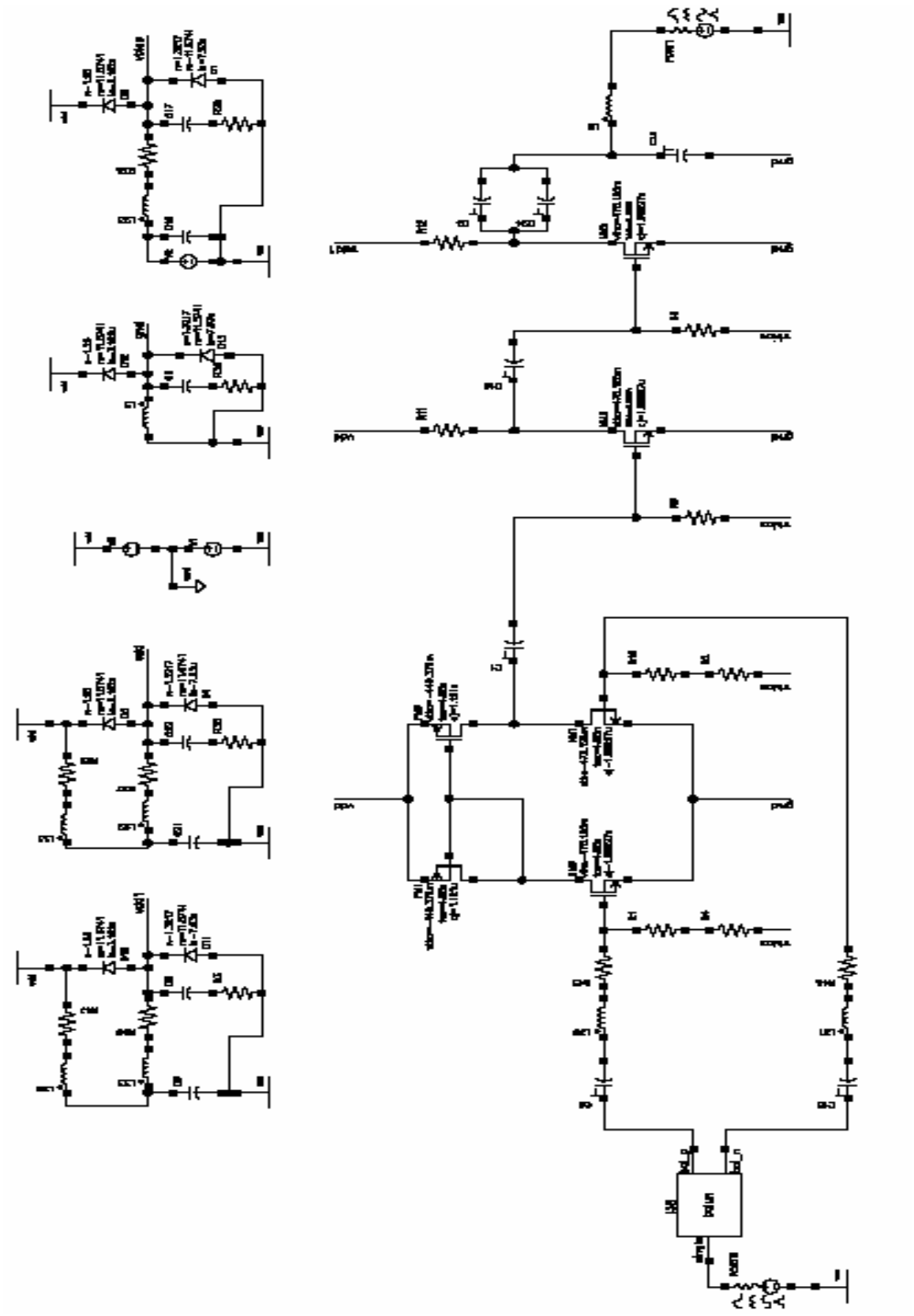


Figure 4.13: Final PA schematic

4.4 Simulation results

In this section the relevant simulation results of the PA design are presented.

Simulations at the schematic level were performed using SpectreRF tool available in Cadence. As already mentioned, the library used was provided by TSMC 0.18μm CMOS process kit. S-parameter simulations can generate plots for the return losses and small signal gain of the overall circuit. Power consumption can be calculated from DC simulations. For large signal analysis, i.e. to measure linearity and output power levels, the tool kit provides the option of Periodic Steady State (PSS) analysis on the circuit.

The S-parameter simulation results are shown in Fig. 4.14 and 4.15. The return losses at the input and output meet the specifications with a margin for post manufacturing errors. S11 and S22 are well below -13 dB over the entire 2 GHz bandwidth, thus showing good input and output match respectively.

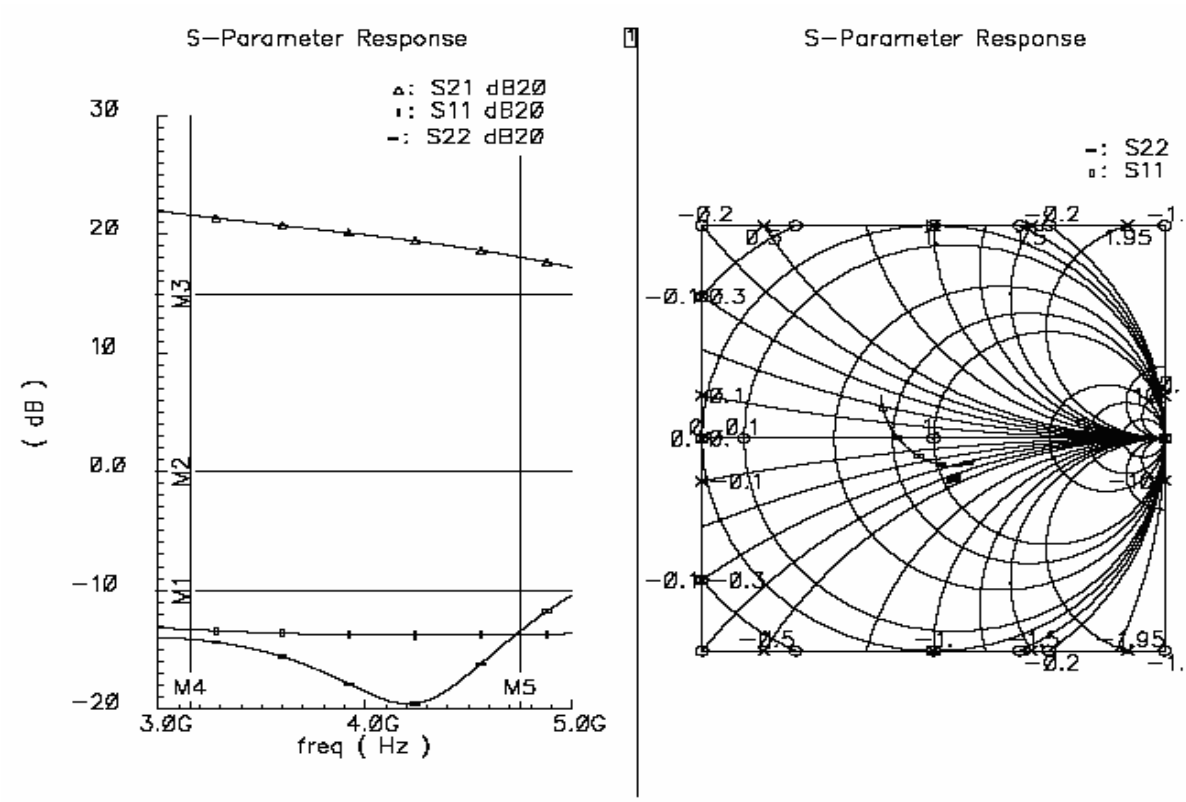


Figure 4.14: S-parameter simulations

The small signal gain S21 exceeds 18 dB. However, gain flatness has not been achieved in this design; the overall gain across the band of interest is 19 ± 2 dB. The resulting impact on the performance of OFDM system is that the peak amplitudes of the waveform in each band would be different.

The stability of the PA can be measured using the parameter K_f from S-parameter simulations. For $K_f > 1$, the circuit is unconditionally stable.

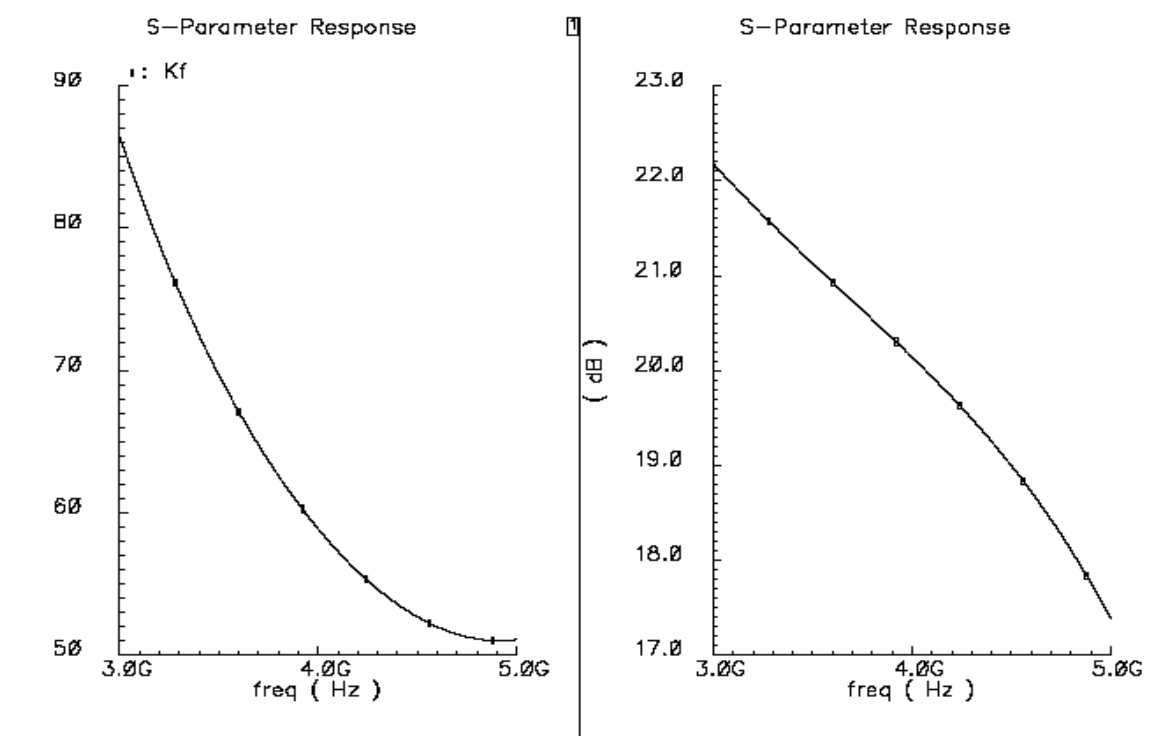


Figure 4.15: Stability and gain plots

PSS simulation results with a 4 GHz input signal is shown in Fig. 4.16. Linearity and output power levels can be estimated from these simulations. IP3 (3rd order inter-modulation) products can be estimated using a 2-tone test with PSS analysis. However, for large circuits, the simulation results may not converge and hence it is a common practice to obtain the third order intercept point from the 1-dB compression point using the relation

$$IIP3 \cong P_{1\text{-dB}} + 10\text{dB} \tag{4.7}$$

The input referred 1-dB compression point for our designed PA is estimated to be -16 dBm, and the output power level at this point is +2dBm. The required specifications are -22 dBm and 0 dBm respectively. Hence, input referred IP3 point as calculated from Eq. 4.7 would be -6 dBm.

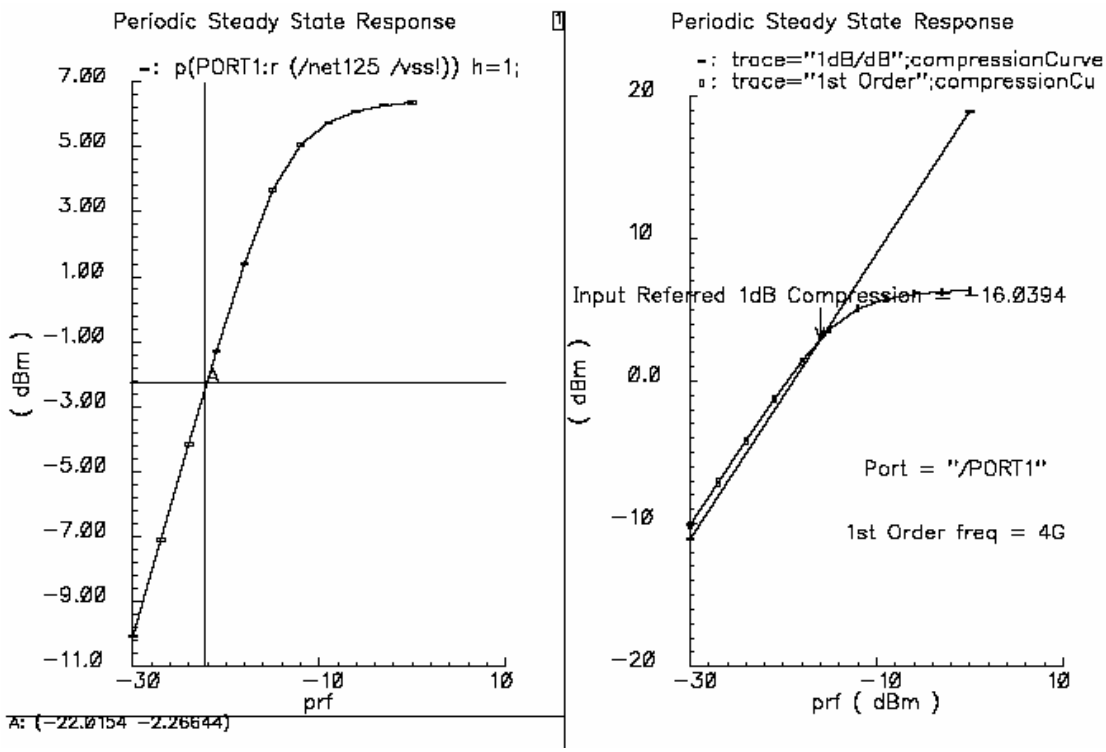


Figure 4.16: PSS Simulation results

To summarize, the required specifications and the simulated results are discussed in Table 4.2.

Table 4.2: Achieved PA Specifications for MB-OFDM

Categories	*Specification*	*Simulation*
Supply voltage	1.8 V	1.8 V
Frequency range	3168 ~ 4752 MHz	3168 ~ 4752 MHz
Output P1dB	0.0 dBm	2.0 dBm
Input P1dB	-22 dBm	-16 dBm
Maximum Output	> -8 dBm	-2.2 dBm
Power gain	>15 dB	>19 dB
Voltage gain	>15 dB	>17 dB
Gain flatness	± 1 dB	19 ± 2 dB
S11	<-10 dB	<-13 dB
S22	<-10 dB	<-14 dB
S12	<-30 dB	<-60 dB
Power consumption	<40 mW	36.5 mW

Comparing with the PA circuit in [19], this PA consumes a lower DC power. This can be attributed to the fact the PA in [19] occupies a wider bandwidth up to 8 GHz and uses a distributed amplifier topology. When compared to the PA in [20], our PA achieves a higher gain over the entire bandwidth and hence consumes almost twice the supply power. However, our design also delivers a higher peak output power which provides a margin for reduction in power levels after the design is fabricated.

4.5 RF Layout considerations

Unlike digital circuits that have automatic generation tools, RF/analog circuits still rely on manual design generation for efficient reproduction of the simulated results. Careful layout techniques need to be applied after the extraction of the mask diagram from the schematic.

In CMOS implementations, one of the biggest concerns is the isolation of devices with other devices and the substrate. Isolation is achieved by the use of guard rings around the devices. To reduce the parasitic gate resistance at the input of each transistor, fingered gate transistors are commonly used. The design kit is able to generate multi-fingered/folded transistors instead of a single huge transistor. The transistors also have dummy transistors along its sides to account for manufacturing defects. The layout is made symmetrical wherever possible to reduce offset errors due to mismatch and to suppress the effects of common-mode noise and even-order nonlinearities.

All the RF signals are routed in higher and adequately wide metal lines. Ground shielding for the sensitive RF signals is provided by using a ground plane around the signal path. Empty spaces within the layout are also filled with ground planes. Bias lines are drawn wide enough to accommodate the current flowing through it. When connecting wide metal lines to thinner lines, the wires are tapered gradually instead of a single-step tapering.

ESD protection in RF circuits is becoming a serious concern for designers. CMOS circuits use diodes at the input of the circuit to clamp the external discharge to ground or supply lines. We have implemented large diodes using a parallel combination of diodes and it can provide an ESD protection of about 1KV. This circuit affects the performance of the PA design because of the huge capacitance that it introduces and hence needs to be included in simulations for accurate modeling.

4.5.1 PA Layout description

The layout of the PA is shown in Fig. 4.17. The total size occupied by the PA is 1.170mm X 0.6mm; inductors and capacitors occupying the largest percentage of area. Large valued capacitors were implemented using a parallel combination of the largest available capacitor in the library. The capacitors were arranged in a common-centroid layout and combined in parallel by connecting all the top metal layers together and the bottom layers together. Due to height limitations in the layout, only one of the 2 inductors used for output match is implemented on-chip. The layout is DRC (Design Rule Check) and LVS (Layout versus Schematic) clean.

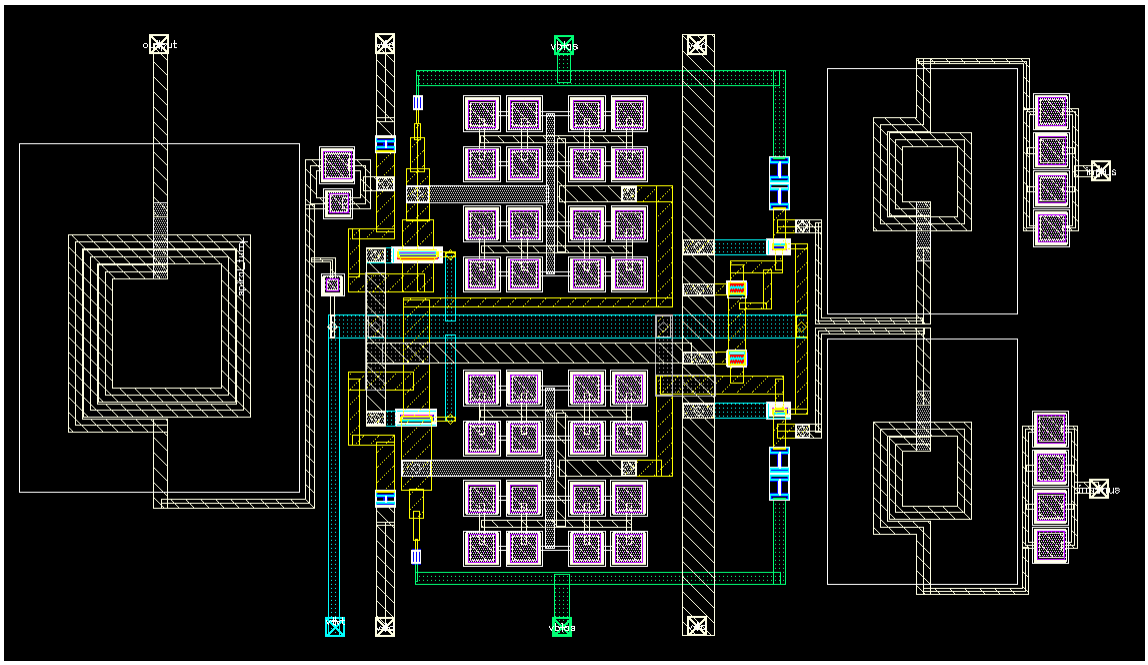


Figure 4.17: PA Layout

4.5.2 Floor Plan of the PA for the integrated version

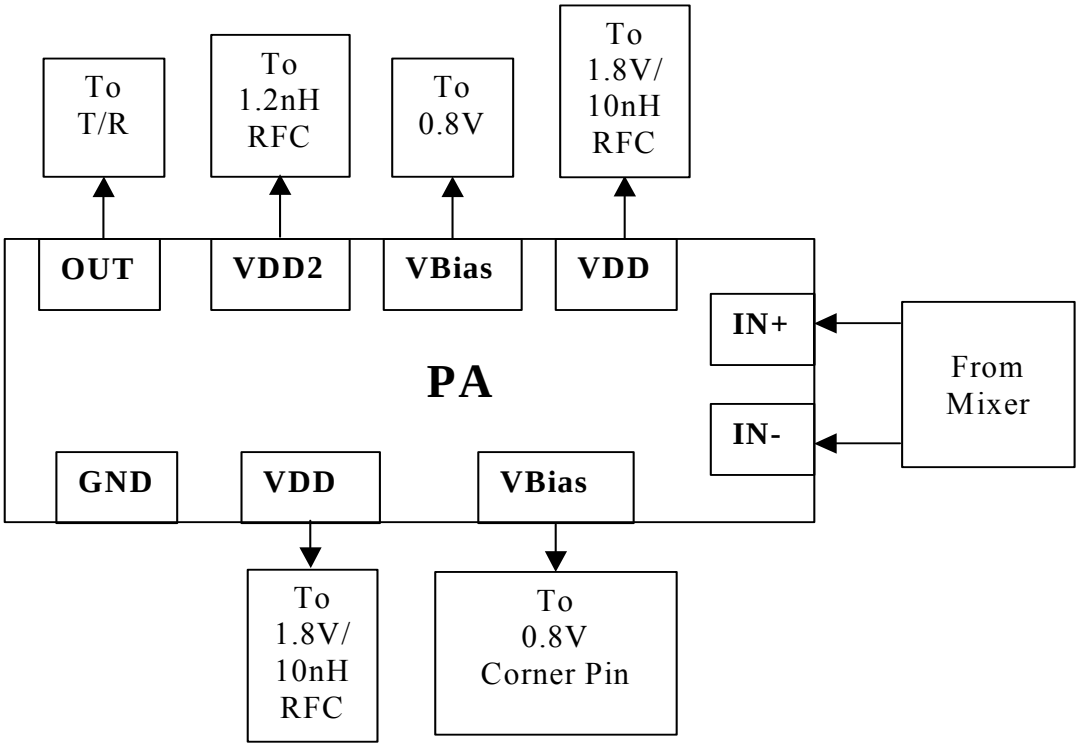


Figure 4.18: Floorplan of PA

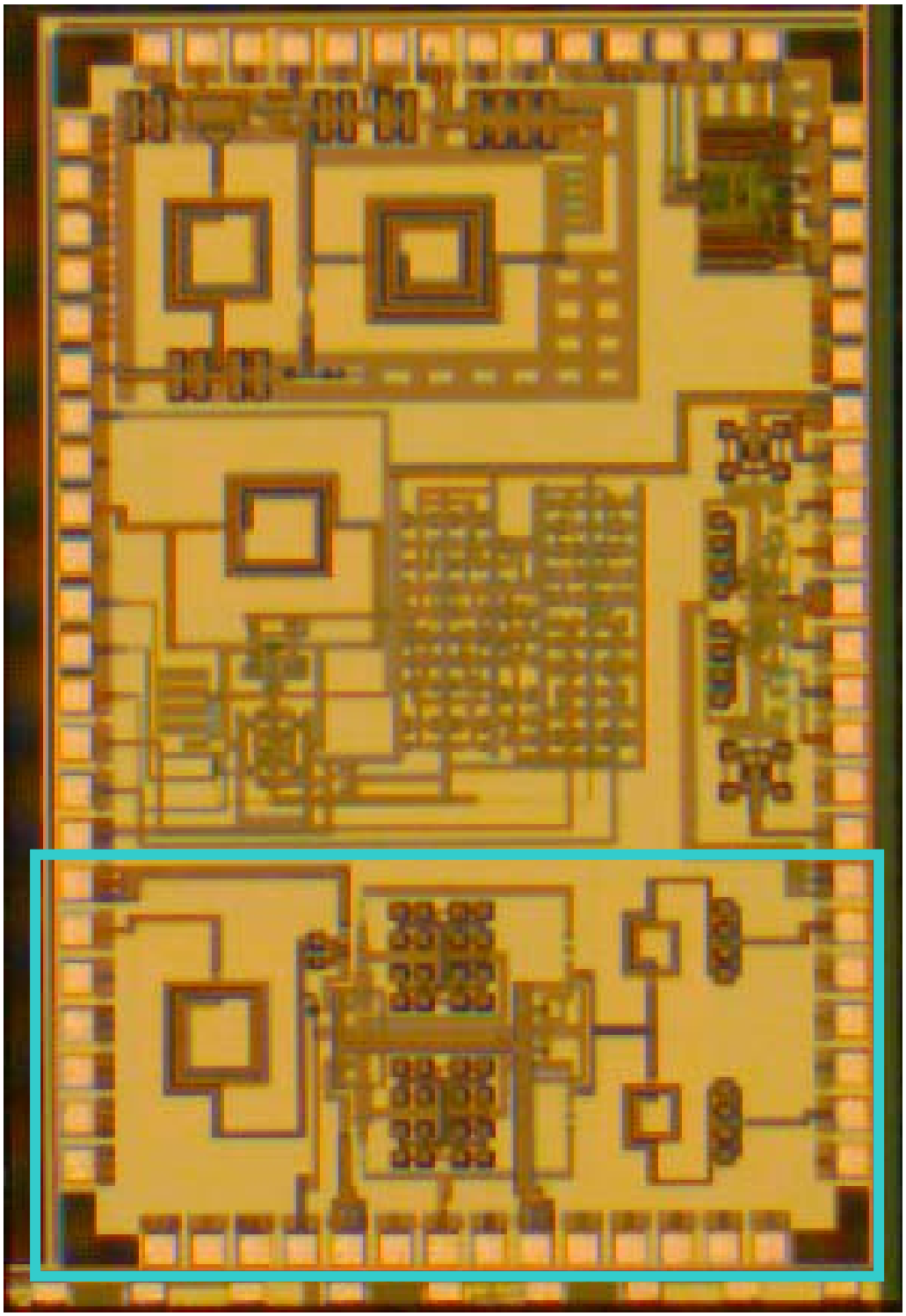


Figure 4.19: Microphotograph of the chip

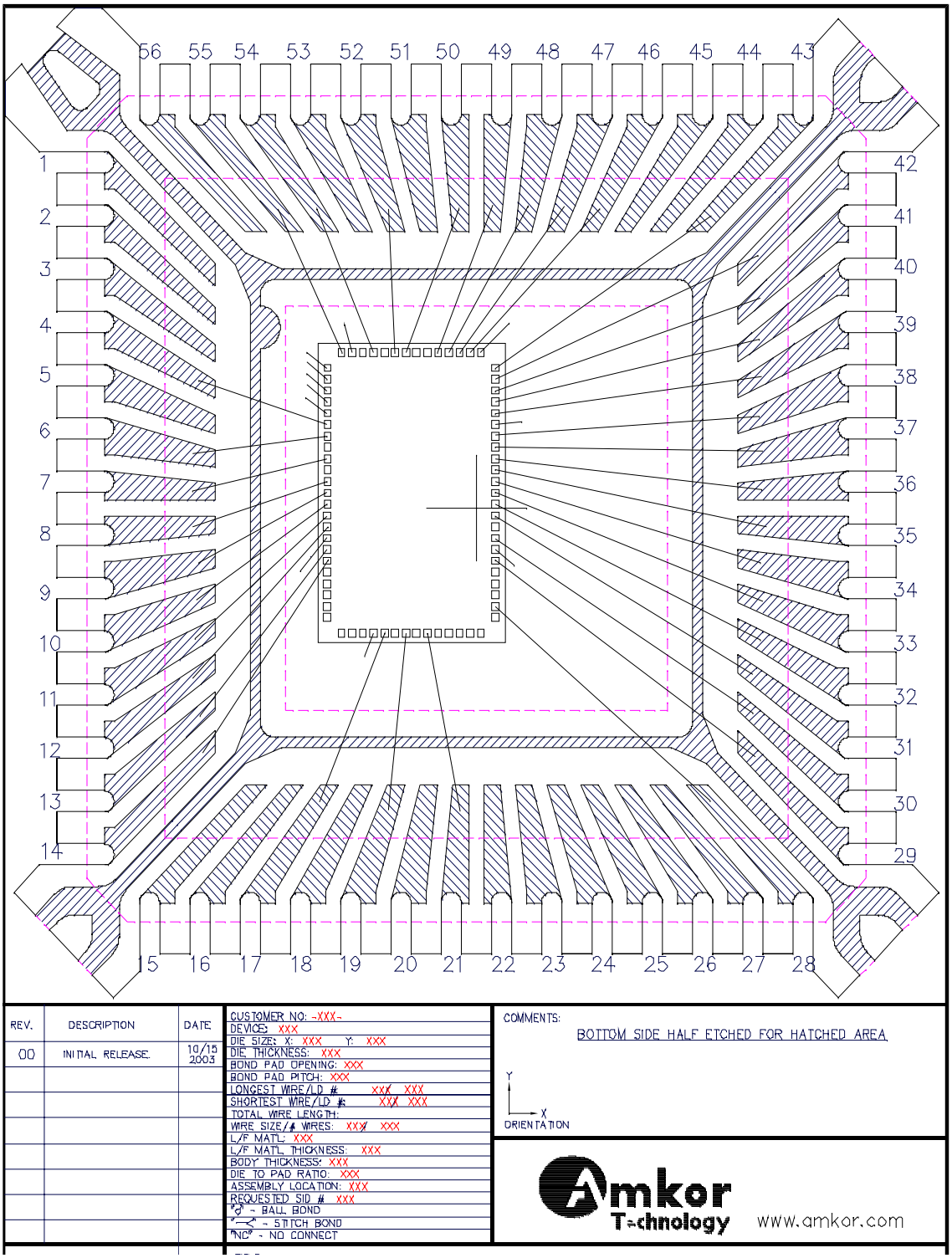


Figure 4.20: QFN package for the MB-OFDM chip

4.6 PCB Design

The PCB for testing of the chip was designed using Cadence Allegro and Agilent's ADS. Since the input side of the PA was matched to 200 Ω, impedance transformation to 50 Ω had to be performed. This is required because all the RF test instruments are terminated as 50 Ω ports.

4.6.1 The quadrature (90°) hybrid (Branch-line Hybrid)

Quadrature hybrids are 3-dB directional couplers with a 90° phase difference in the outputs of the through and coupled arms. This type of hybrid is often made in micro-strip or strip-line form as shown in Fig. 4.21, and is also known as a branch-line hybrid.

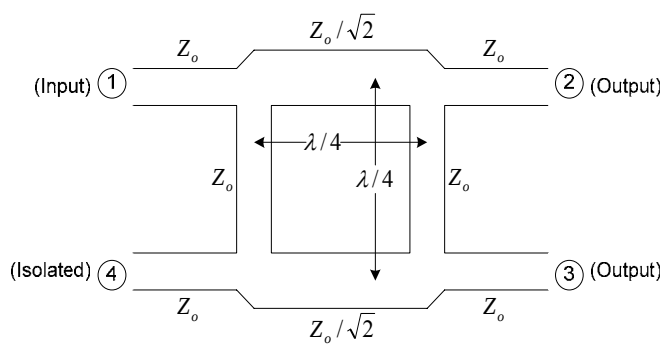


Figure 4.21: Geometry of a branch-line coupler

The basic operation of the branch-line coupler is as follows. With all ports matched, power entering port 1 is evenly divided between ports 2 and 3, with a 90° phase shift between these outputs. No power is coupled to port 4 (the isolated port).

In practice, due to the quarter-wave length requirement, the bandwidth of a branch-line hybrid is limited to 10% - 20%. But as with multi-section matching transformers and multi-hole directional couplers, the bandwidth of a branch-line hybrid can be increased to a decade or more by using multiple sections in cascade. In addition, the basic design can be modified for unequal power division and/or different characteristic impedances at the output ports.

Since we have to cover 3 to 5 GHz, a four-branch coupler was designed and its results are shown in Fig. 4.22. However, this design occupies a larger board area, resulting in significant signal losses.

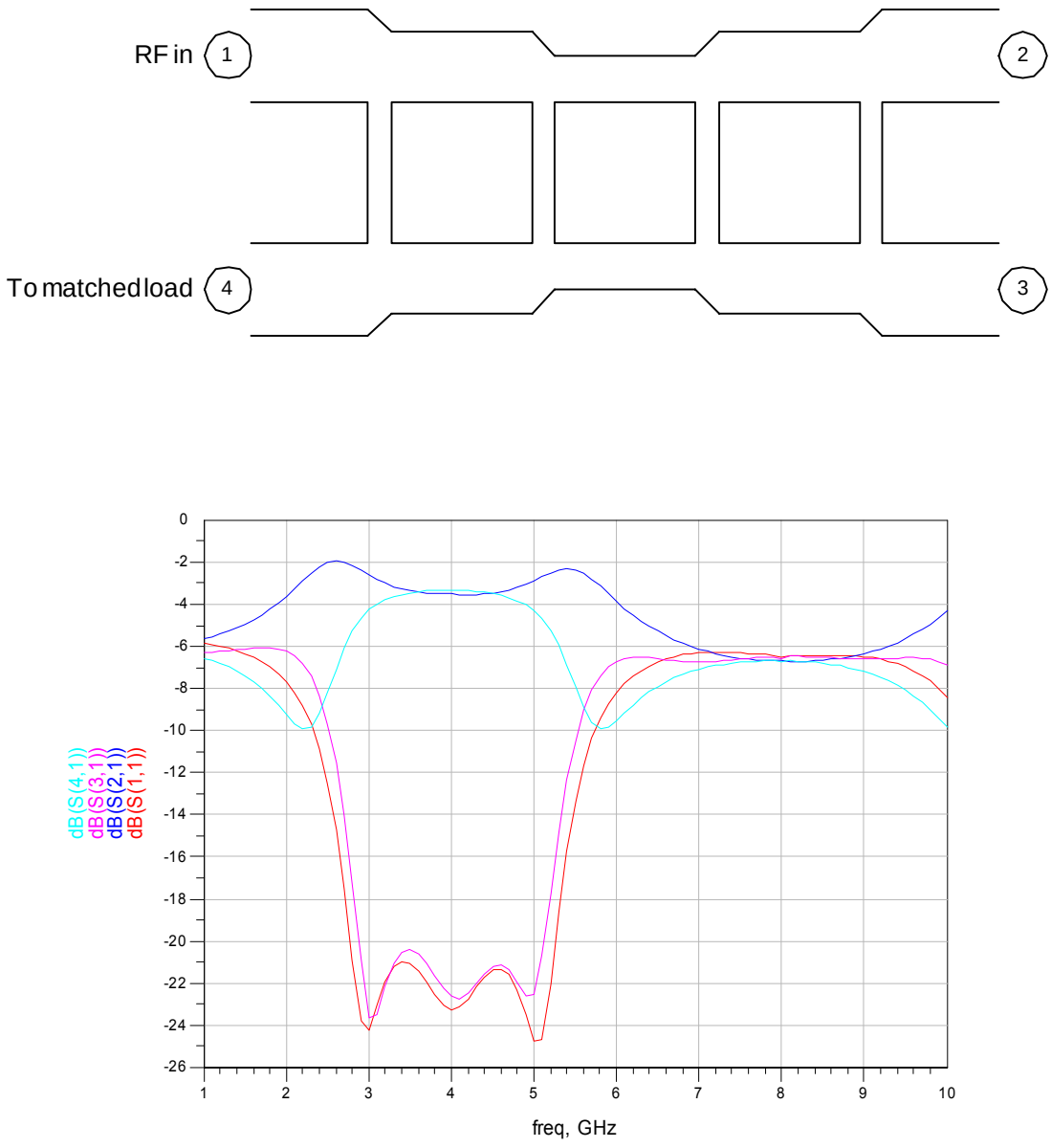


Figure 4.22: Four branch coupler and its characteristics

However, as seen from the coupler characteristics, some ripples exist in the pass band and hence we expect some degradation in the PA's measured performances.

Fig. 4.23 shows the PCB used for testing the PA including the chip and SMA connectors. As expected the wideband balun for impedance transformation occupies a major portion of the PCB.

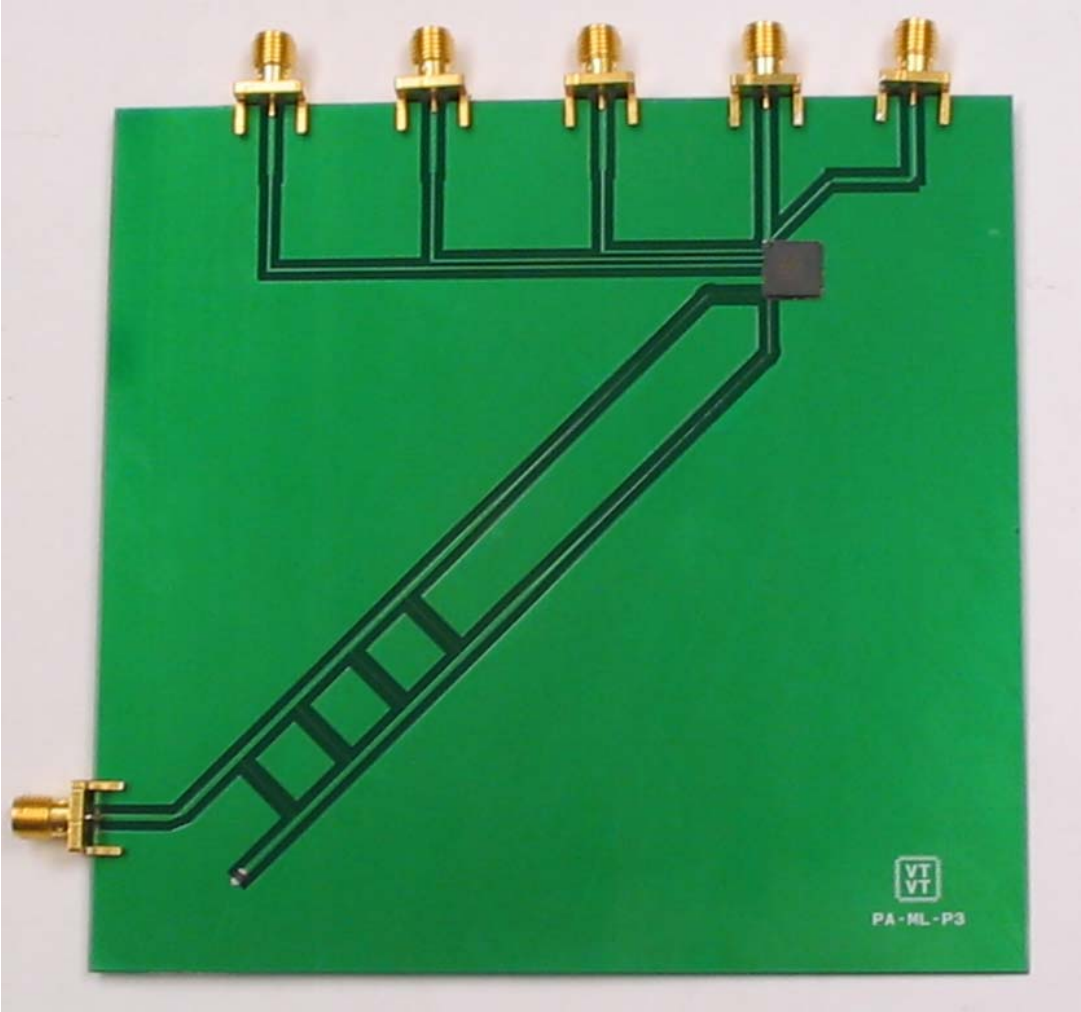


Figure 4.23: PCB of PA

4.7 Test setup and measurement results

The primary results that need to be measured of the PA are its gain, impedance matching, power consumption, output power levels and linearity.

S-parameter results were measured using a HP 8510C Vector Network Analyzer that has the capability to cover the frequency ranges 45 MHz-50 GHz. The first step involved is the calibration of the VNA to account for losses in the connecting wires, attenuators and the connectors. After the calibration has been performed using standard loads of open circuit, short circuit and 50 Ω, the small signal parameters can be measured using the setup shown in Fig. 4.24.

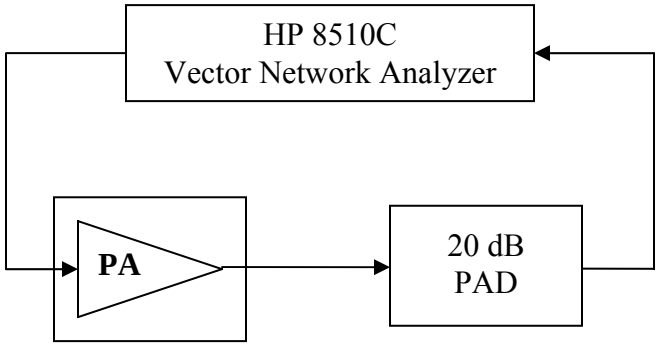


Figure 4.24: Test setup for S-parameter measurements

Linearity measurements require the use of a signal generator to feed in varying power levels to the PA and a spectrum analyzer to measure the output power. For our experiment, we have used the HP 83620B Series Swept Signal Generator and the HP 8563E Spectrum Analyzer.

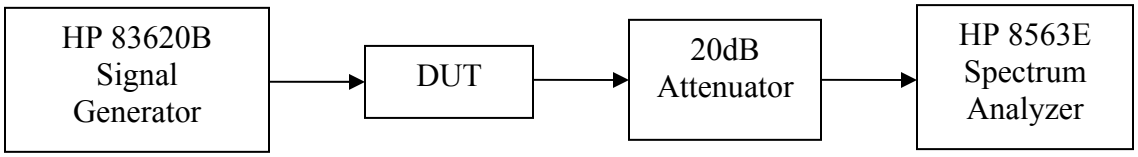


Figure 4.25: Bench setup for P1dB measurement

An RF signal of desired frequency is fed into the DUT from the signal generator. The input power levels are swept in steps of 1 dBm and the output spectrum is measured using the spectrum analyzer. The difference between the power levels at the output and input gives the gain of the LNA at that particular frequency.

A plot of the output power (excluding the 20 dB attenuation from the attenuator), against the input power can be used to determine the 1-dB compression point. IP3 measurements are done using a 2-tone test that requires two signal generators. The test setup is similar to the one used for 1-dB compression measurements except for the additional signal generator, which for our case is the HP 83592A Sweep Oscillator.

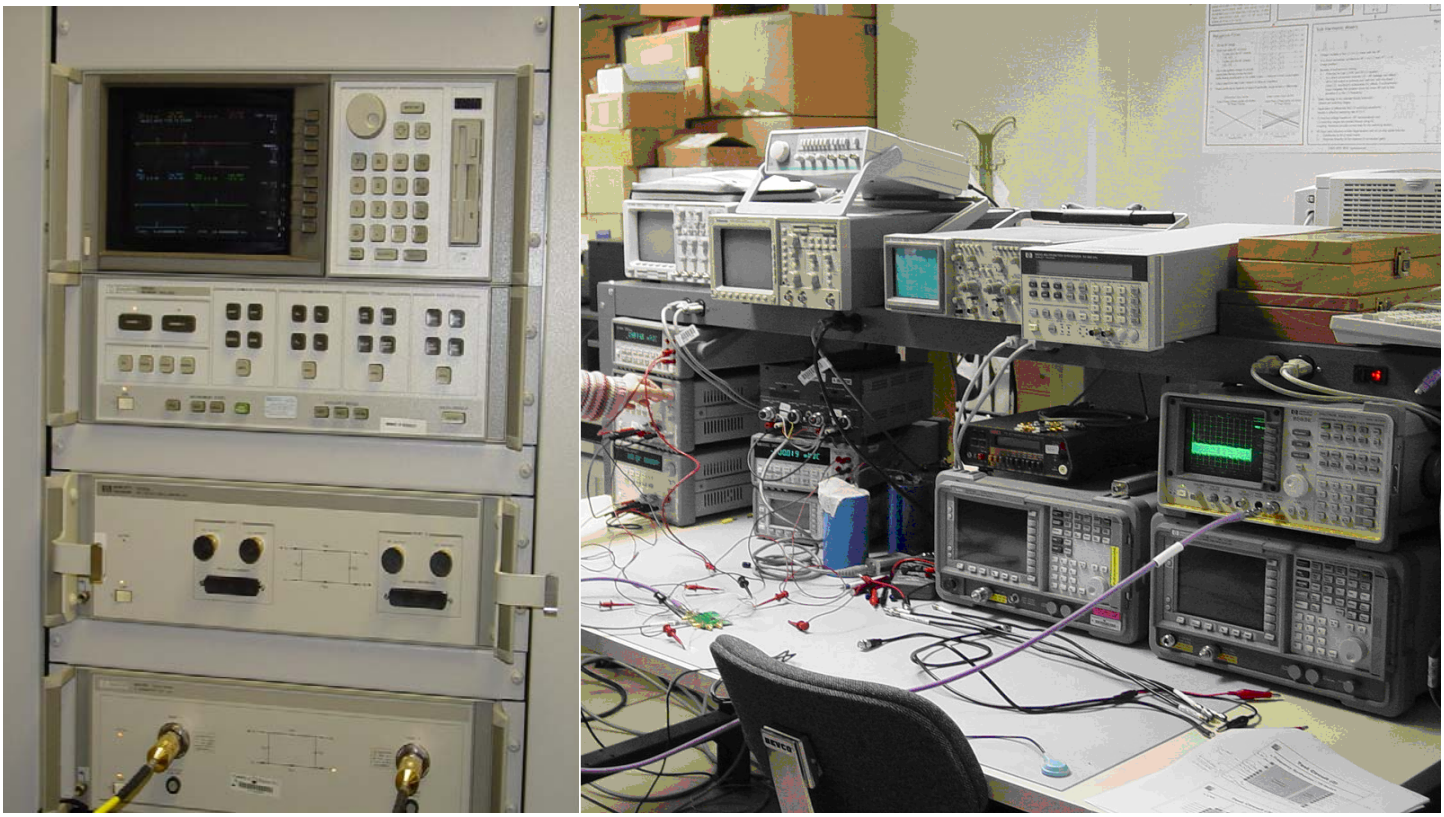


Figure 4.26: Test Equipments-setup

(Courtesy: Wireless Microsystems Laboratory, Virginia Tech)

The measured S-parameter results are shown in Fig. 4.27.

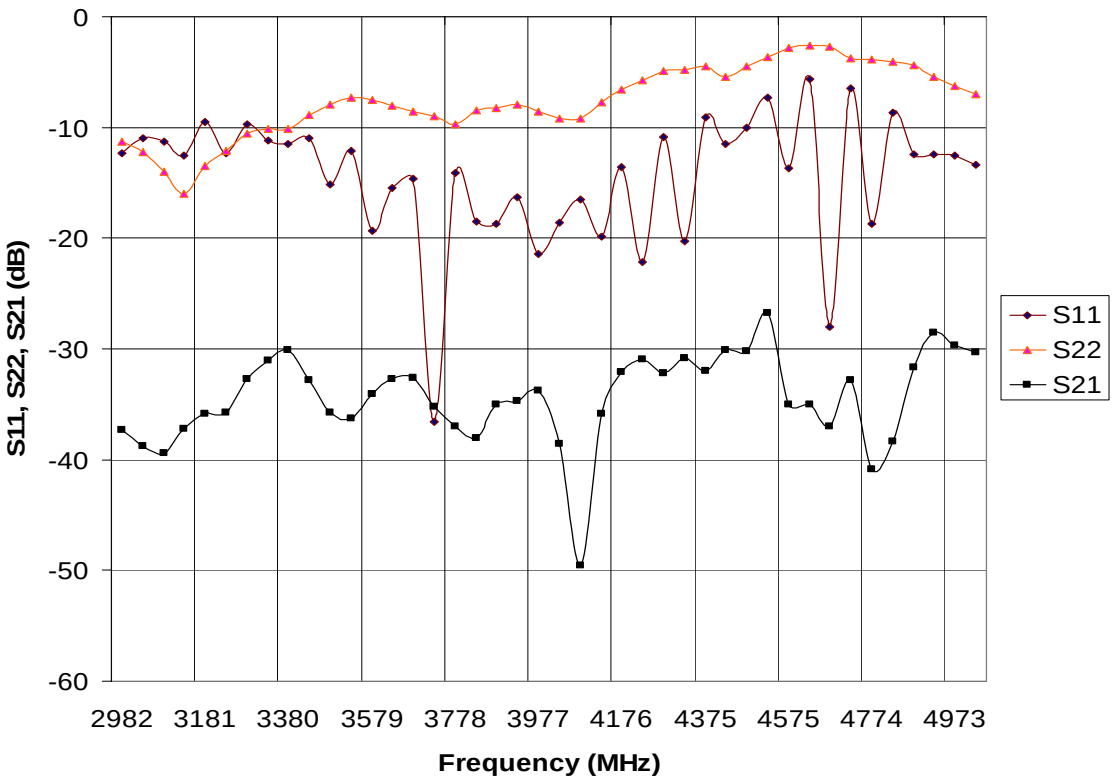


Figure 4.27: Measured S-parameter results

The small-signal gain S21 is -30 dB in the desired frequency band which shows that the PA failed to work. The reason was later identified to be due to an integration error. The PA had two bias pins that had to be taken out externally and only one of the pins was taken out. Since one of the three PA stages could not be biased/reached, there is no signal transmission/amplification from the input side to the output of the PA. Other measurements would not yield any meaningful results and hence were not taken.

4.8 Remarks

The complete design, implementation and measurement of a PA suitable for MB-OFDM proposal was presented in this chapter. The PA is a 3 stage design with the transistors operating in Class-AB region and delivering +2 dBm to a 50 Ω load. Simulation results met all the specifications of the MB-OFDM proposal. The design was

fabricated in TSMC 0.18 μm process and measurements were performed on the chip. Though the test chip set failed, we have been able to gain significant insight in the complete design cycle of RFIC's from conception to realization.

Chapter 5

Power Amplifier design for DS-CDMA

Introduction

Direct Sequence-Code Division Multiple Access (DS-CDMA) scheme was proposed by Freescale Semiconductor (formerly Xtreme Spectrum), and a group of other companies [13]. The main architecture difference between this proposal and the MB-OFDM proposal is that the entire 7.5 GHz bandwidth is divided into two bands unlike 13 bands in MB-OFDM. The lower band covers the frequency range from 3.2 to 5.15 GHz and the upper band covers the frequency range from 5.825 to 10.6 GHz. Our PA is designed to support the lower band of the DS-CDMA system

5.1 System specifications:

The major PA specifications are given in Table 5.1. These specifications are almost similar to MB-OFDM specifications (table 4.1), except for the frequency range and linearity requirements.

Table 5.1: Power Amplifier Specifications for DS-CDMA

Categories	*Specifications*
Supply voltage	1.8 V
Frequency range	3085.55 ~ 4934.8 MHz
Output P1dB	-2.0 dBm
Input P1dB	-17.0 dBm
Power gain	15 dB
Voltage gain	15 dB
S11	< -10 dB
S22	< -10 dB
Input impedance	Differential : 50 Ohm
Output impedance	Single-ended : 50 Ohm
Power Consumption	<40 mW
Power Saving	Supply ON/OFF scheme
Elimination of T/R switch	Switch transistor

The linearity requirements for the DS-CDMA system is higher than the MB-OFDM system because DS-CDMA scheme is impulse based and it is crucial that the pulses preserve their shapes with little distortion.

5.2 Design topology

The design topology shown in Fig. 5.1 is used for DS-CDMA PA. Each PA stage is designed to achieve a gain of around 12 dB and the overall design gives a gain >15 dB to meet our specifications.

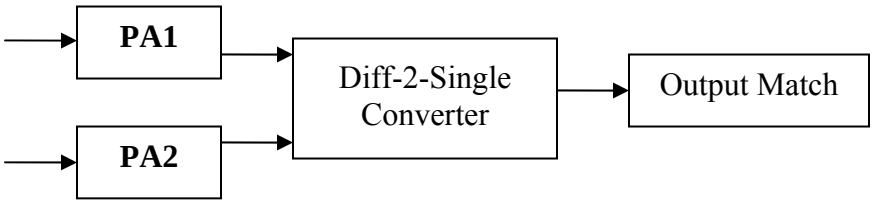


Figure 5.1: PA topology of DS-CDMA

5.2.1 PA ON/OFF Scheme

In typical applications, the transmitter may not be operational for all the time. To conserve power, it is a common practice to include some form of power control circuitry within the circuit. Adjusting the bias voltages to control the output power is one such technique. Another method is to use a power down switch at the supply end to "shut-down" the whole amplifier core [25], [26].

This can be achieved by using a large transistor acting as a switch at the power supply end. Using an external control voltage, this switch can be turned ON/OFF to regulate the supply voltage to the entire circuit. A simple NMOS transistor as the switch has a voltage loss across it when turned ON. Instead, a PMOS transistor can pass a good logic-1 and hence there is very little supply voltage drop to the amplifier core stage. Large sized transistors will have to be used to reduce the R_{ON} of the transistor.

5.2.2 Output Impedance control scheme

The function of a T/R switch is to show high impedance to the antenna when either the LNA or the PA is turned OFF [24]. For example, when the LNA is turned ON, the antenna should be able to see a very high impedance at the transmitter end so that all the received signal flows into the receiver path.

We use a switch transistor at the output of the PA to perform this operation. This switch transistor can be thought of as one of the branches of an ideal T/R switch. When ON, this switch transistor can be designed to show an output impedance of 50 Ω; and when OFF, impedance looking into this transistor would be large. At the receiver end, a similar switch topology will be applied to control the input impedance of the LNA when PA is ON.

The overall PA architecture used for DS-CDMA is shown in Fig. 5.2. As mentioned earlier, the common gate switch transistor used for output impedance control is also included in the architecture.

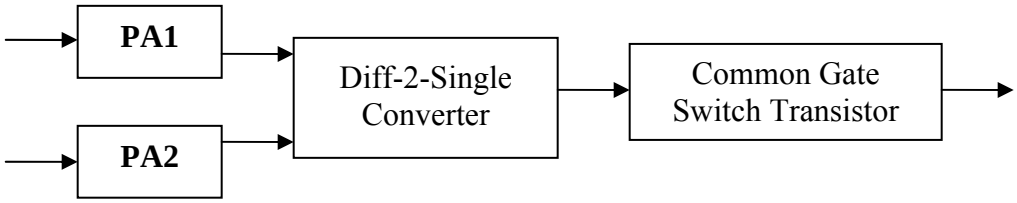


Figure 5.2: DS-CDMA PA with common gate transistor at output

Since our linearity requirement is not stringent, non-linear classes of PA like Class-AB, Class-B or Class-C can be used to achieve improvement in efficiency. In this design, Class-AB topology is used to achieve the same at the expense of linearity.

5.3 Design Methodology

One of the primary design specifications to meet is the matching of the circuit over such a wide band frequency range of interest. It is widely known that resistive terminations can be used for broadband matching. Unlike direct shunt termination, shunt-feedback approach will not incur a high power loss, thus improving the efficiency. A suitable value of the feedback components was selected using the approach described in chapter 4.2, while a trade-off between gain and impedance match is maintained. In order to isolate the input and output of this first stage we used a cascode transistor along with the feedback.

In the PA design for DS-CDMA, the overall linearity of the system is determined by the linearity of the last stage in the system. For our case, the common-gate switch transistor acts as the last stage. To improve the linearity, the switch transistor size has to be increased. But a large transistor will not provide good reverse isolation when the transistor is OFF., i.e. there is a signal feed-through even when the transistor is OFF. Hence an optimum width was determined through simulations to meet the required linearity specifications.

5.3.1 Wire bonding & Pad model

For accurate simulations, the wire bonding and pad model shown in Fig. 5.3 are also included in our design. The component values are given by the manufacturer for the specific package used. In multiple ground-bonding, this bonding wire inductance and resistance is significantly smaller.

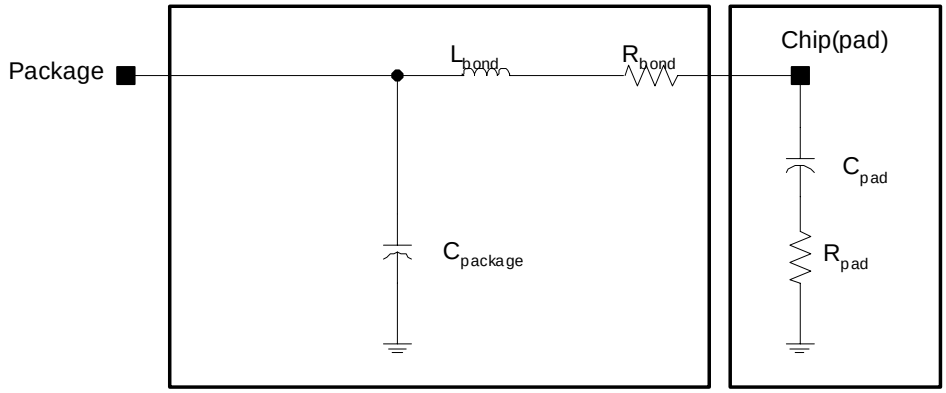


Figure 5.3: Package model

5.4 Simulation results and layout:

Fig. 5.4 shows the complete schematic of the PA intended for DS-CDMA proposal. The differential input is amplified separately using a Class-AB amplifier and then combined to generate a single ended output. The attractive feature of this design is that no off-chip components are required and hence is completely monolithic. Even RFCs, ac-bypass capacitors and bias resistors have been incorporated on-chip. Power control switches and the common-gate switch is included in the design and provides extra flexibility in terms of power saving.

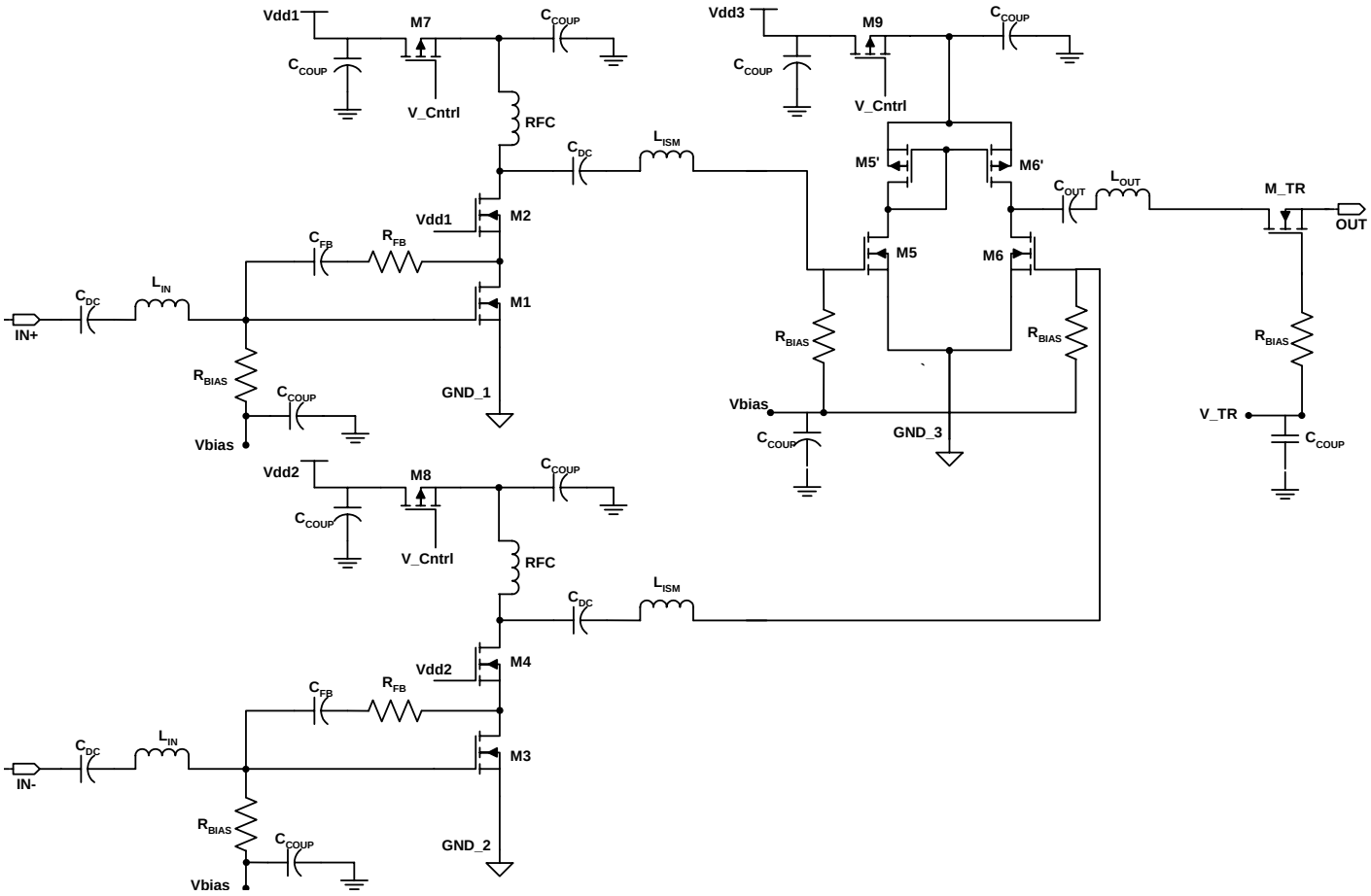


Figure 5.4: Complete PA schematic

S-parameter simulations to measure the return losses and small-signal gain are shown in Fig. 5.5. Though ideal matching (<-10 dB) is not achieved, a flat gain of 19±1 dB has been realized. The circuit is also unconditionally stable with a K_f >30. Large signal analysis (Fig. 5.6) reveals the P1-dB compression point to be -21.7 dBm and the output power at this point is -4 dBm. Unfortunately, these parameters do not meet the specifications of DS-CDMA proposal. The required values were -17 dBm and -2 dBm respectively. Since power consumption was a major criterion for this design, we had used a lower bias voltage for the transistors. This lowers the output power from the transistor and hence the linearity.

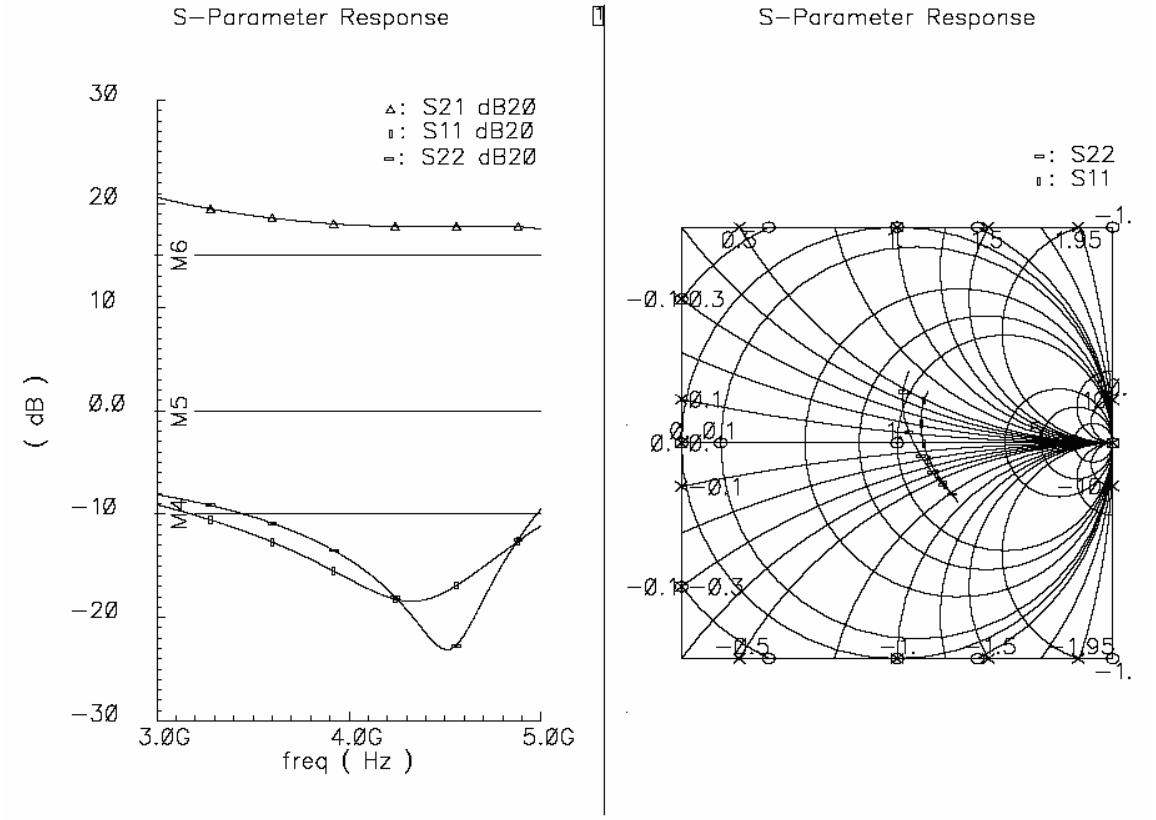


Figure 5.5: Gain and return loss characteristics

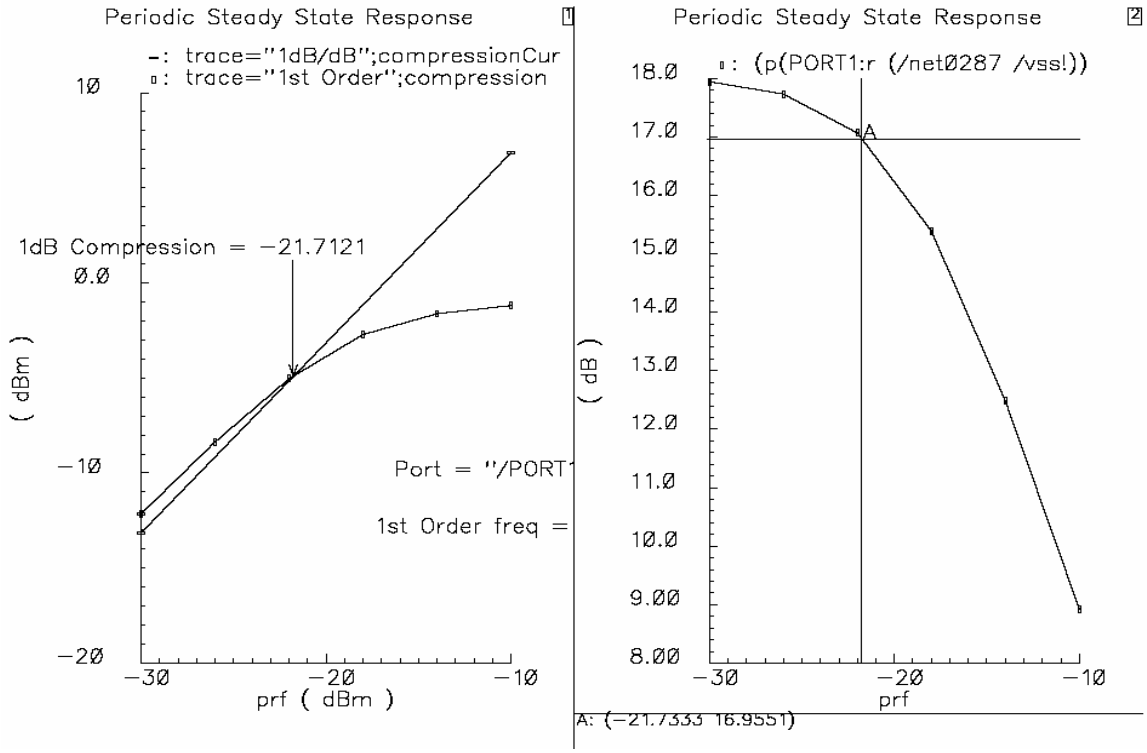


Figure 5.6: 1-dB compression and Power Gain characteristics

5.4.1 Output Impedance control scheme

The simulation results of our switch based impedance control scheme are shown in Fig. 5.7. The S-parameter plots shown indicate that there is no signal transmission when the control switch is OFF and the input matching is maintained. The plot of output impedance when the switch is turned ON/OFF is also depicted in the figure. When ON, the impedance seen by the PA is around 80 Ω; and when OFF, the PA sees an impedance of around 800 ~ 1.2 kΩ for the entire desired bandwidth. At this time the LNA would be turned ON so that most of the received signal flows into the receiver section without any degradation.

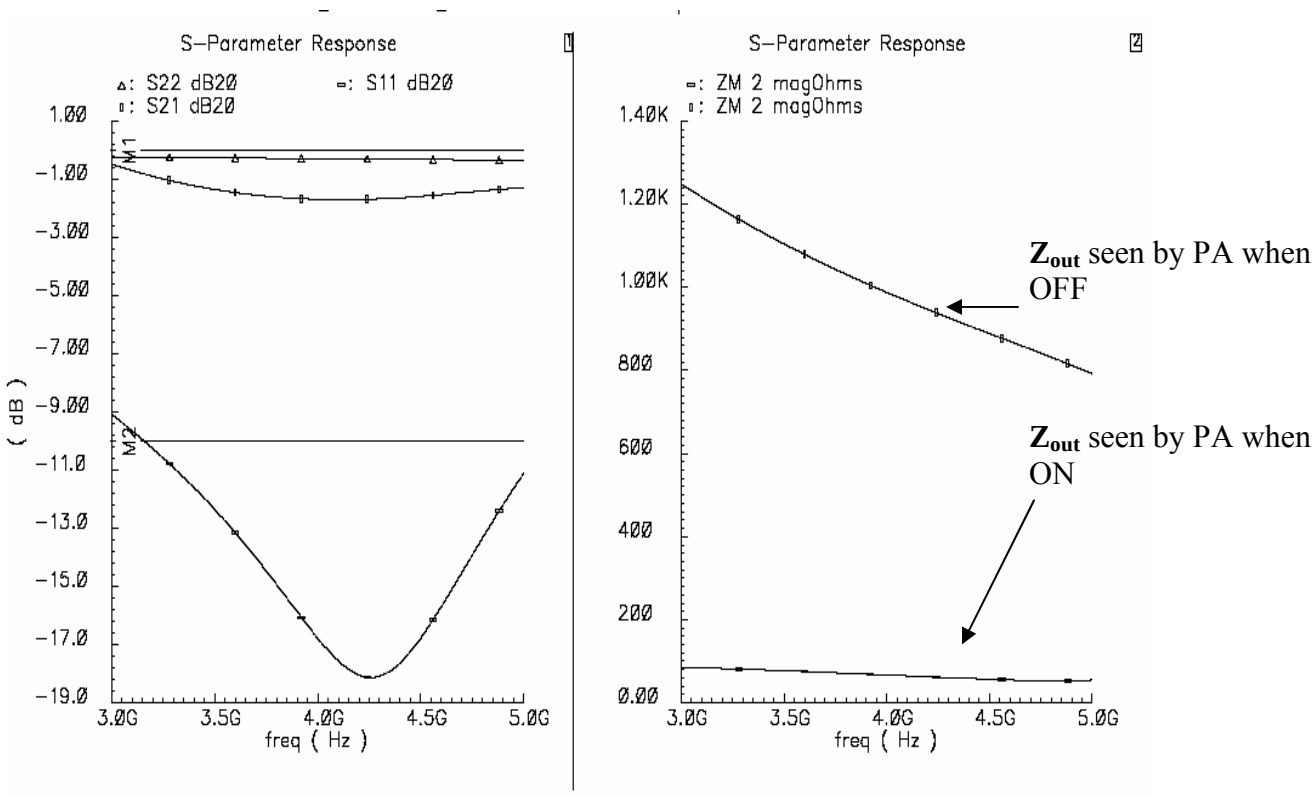


Figure 5.7: S-parameter response when control switch OFF

The final achieved specifications of the PA are shown in Table 5.2. Note that linearity and output power specifications have not been met for this design.

Table 5.2: Achieved PA Specifications for DS-CDMA

Categories	***Required Specifications***	***Achieved Specifications***
Supply voltage	1.8 V	1.8 V
Frequency range	3085.55~4934.8 MHz	3085.55 ~ 4934.8 MHz
Output P1dB	-2.0 dBm	-5.0 dBm
Input P1dB	-17.0 dBm	-22.0 dBm
Power gain	15 dB	>17 dB
Voltage gain	15 dB	19±1 dB
S11	< -10 dB	< -10 dB
S22	< -10 dB	< -8 dB
Input impedance	Differential : 50 Ω	Differential: 50 Ω
Output impedance	Single-ended : 50 Ω	Single-ended : 50 Ω
Power Consumption	<40 mW	25 mW
Power saving	Supply ON/OFF scheme	YES
Elimination of T/R switch	Switch transistor	YES

5.5 Layout of the PA

The PA layout shown in Fig. 5.8 was drawn using the guidelines discussed in chapter 3. Since the RFCs, ac-decoupling capacitors and bias resistors were included on-chip, the entire design occupies a huge area of 1 mm X 2 mm. DRC and LVS checks were performed on the layout and were successful. The design was fabricated using the TSMC 0.18 μm CMOS process and is currently in the packaging stage. Testing will be performed on these chips during the early part of next year.

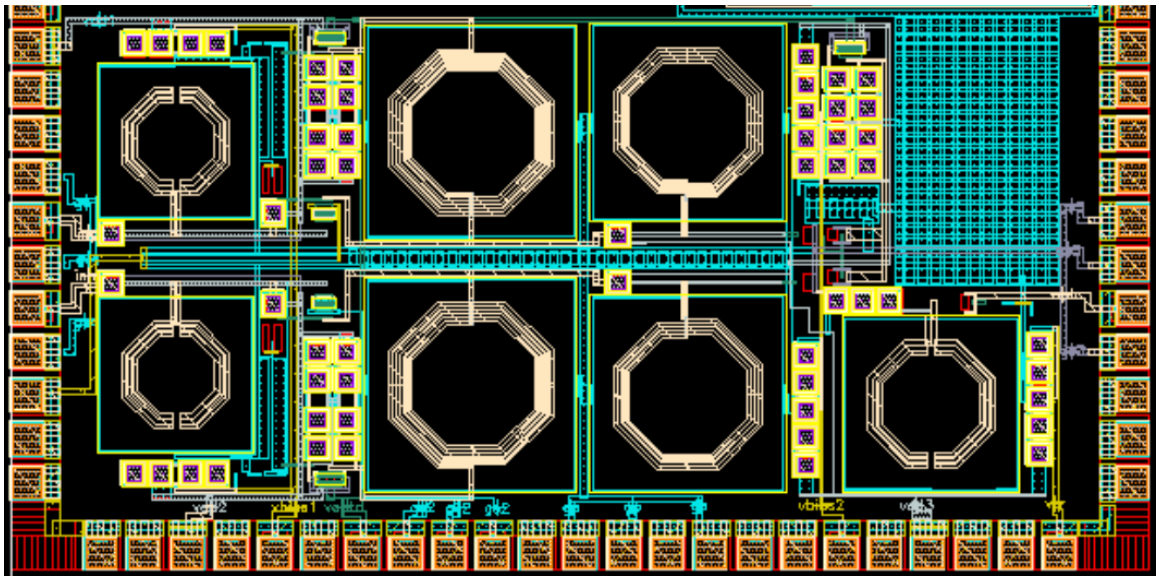


Figure 5.8: PA Layout

Fig. 5.9 shows the floor plan of the PA; requiring 14 pins. The chip will be enclosed in a 56-pin QFN package.

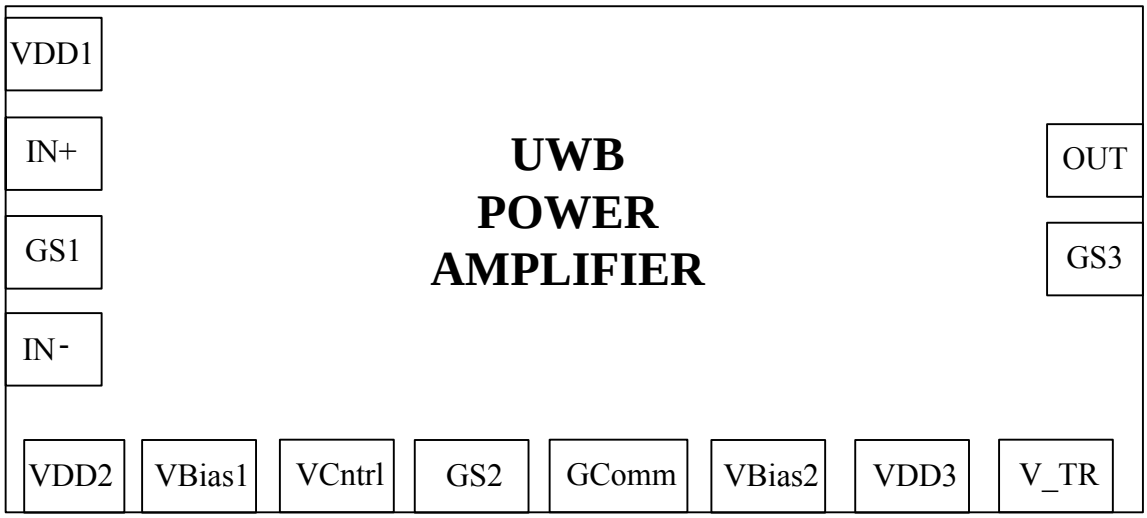


Figure 5.9: PA floor-plan

5.6 Remarks

This chapter described the design of a complete PA suitable for DS-CDMA proposal in UWB applications. The design topology used, simulation results and layout were also discussed. The design was fabricated using the TSMC 0.18 μm CMOS process and is currently in the packaging stage. Testing will be performed on these chips during the early part of next year.

Chapter 6

Conclusion

UWB technology is one of the hot topics today because of a tremendous promise it holds especially in the field of high data rate, short distance wireless communications. Once realized, UWB can hold its sway over a varied range of applications with the small hardware complexity.

In this thesis we have presented the design of a key RF block in the UWB transceiver – the power amplifier, in CMOS technology. Since the standard for UWB technology has not been finalized yet, we have designed and implemented two PAs that meet the specifications of the two proposals being considered viz., MB-OFDM and DS-CDMA. Both PAs cover the frequency band from 3 GHz to 5 GHz.

The PA for MB-OFDM is a 3-stage Class-AB design and uses resistive-shunt termination to achieve the wide band of operation. The design was laid out and fabricated in TSMC 0.18 μm CMOS technology along with other RF blocks of the transceiver. Simulation results exceeded the specifications required and hence provided a margin for any degradation in performance due to manufacturing limitations.

The PA for DS-CDMA is also a 3-stage design, albeit with a shunt-feedback topology to achieve the wide band of operation. In addition to regular features, this design also includes a power on/off switch to conserve power and an impedance control strategy at the output to explore possibilities of a T/R switch-less design. A completely monolithic realization with no off-chip components makes this PA ideal for a single system-on-a-chip solution. This design has been submitted for fabrication in TSMC 0.18 μm CMOS technology and is expected by the end of this year.

Comparing with the existing work discussed in [19] & [20], the PA's discussed in this thesis consume very low power yet providing a sufficiently high gain over a wide bandwidth. With better technology, the PA topology can be redesigned to cover even higher frequency ranges and bandwidths.

Initial UWB realizations in CMOS is targeted for lower band of frequencies covering the 2 GHz bandwidth from 3~5 GHz. However, to exploit the true potential of UWB, the higher frequencies will also have to be utilized. With the availability of 130 nm and 90 nm CMOS technologies, future implementations should be able to cover the entire spectrum from 3.1 GHz to 10.6 GHz.

- Existing wide band matching techniques are inefficient and may not be suitable for frequencies up to 10.6 GHz. Alternative techniques will have to be explored that can incorporate a single-stage design and strike a trade-off between power and area.
- Future research can also be directed towards the improvement of linearity in UWB PAs by including linearization schemes like Doherty topology, or linearization using non-linear components etc.

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Vita

Sajay Jose was born in Kerala, India on June 20, 1981. He graduated from Osmania University, Hyderabad, India in May 2002 with a Bachelor of Engineering degree in Electronics and Communications Engineering. He started on his Master of Science degree in Electrical Engineering from Virginia Tech, Blacksburg, Virginia from the fall semester of 2002.

He joined the Virginia Tech VLSI for Telecommunications (VTVT) Laboratory under Dr. Dong Ha in the summer of 2003 and since been working on the implementation of a single-chip CMOS UWB transceiver. Sajay completed the requirements for his Master's degree in December 2004.