TOPOLOGY AND ANALYSIS IN POWER CONVERSION AND INVERSION

by

Richard P.E. Tymerski

Dissertation submitted to the Faculty of the

Virginia Polytechnic Institute and State University

in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

in

Electrical Engineering

APPROVED:

Fred C. Lee, Co-Chairman

Vatché Vorpérian, Co-Chairman

William Baumann

Stanoje Bingulac

Terry Herdman

April 22, 1988

Blacksburg, Virginia

TOPOLOGY AND ANALYSIS IN POWER CONVERSION AND INVERSION

by

Richard P.E. Tymerski

Fred C. Lee, Co-Chairman

Vatché Vorpérian, Co-Chairman

Electrical Engineering

(ABSTRACT)

Basic PWM dc-to-dc converter structure is examined wherein a basic substructure of converters, known as a converter cell, is identified. Converter cells can be used in generation and classification of basic PWM dc-to-dc converters. A large number of new converters are generated.

Converter analysis, whereby the nonlinear response of the system to perturbations in the control or the input, is determined by two different methods.

A classical approach to nonlinear systems analysis is first used wherein the system is represented by a Volterra functional series. The alternative approach presented concentrates on deriving circuit models for the PWM switch. The PWM switch represents the static nonlinear substructure of the vast majority of converter cells. Analysis of converters then proceeds in an analogous fashion to ordinary transistor circuit analysis whereby the nonlinear device is replaced by its circuit model.

Topological considerations of single-phase dc-to-ac inverters are discussed. A number of zero-current switching quasi-resonant inverter topologies are derived. Schemes that permit these topologies to handle reactive loads are identified.

Acknowledgements

I would like to express my sincere gratitude to Dr. Fred C. Lee for accepting me into the power electronics group at Virginia Tech and for serving as a co-advisor. It has been a pleasure and a privilege to work under him in such well equipped laboratories which he has provided. His caring support is much appreciated.

I would equally like to express my sincere gratitude to co-advisor, Dr. Vatché Vorpérian whose academic guidance has been inspiring. His caring support is also much appreciated.

I am grateful to Dr. William Baumann for numerous enlightening discussions and to Dr. Stanoje Bingulac and Dr. Terry Herdman for serving on my advisory committee.

Thanks are also extended to fellow graduate students Chungjen Hsiao and Ray Ridley for their assistance in the use of the simulation program, COSMIR, used in this thesis.

I further wish to express my thanks to Kwang-Suz Jen for her assistance in the production of the figures in this thesis and for her valued friendship during my stay at Virginia Tech.

My gratitude is also extended to Dr. Kevan Daly of the University of New South Wales, Sydney, Australia, who, as my former advisor, played a crucial part in my developing an academic interest in power electronics and to whom I am much indebted for his support.

My stay at Virginia Tech has been supported by IBM, Lexington, Kentucky, and by the General Dynamics Corporation, Fort Worth, Texas and by the VPEC Industry-University Partnership Program for which I am grateful.

Table of Contents

Chapter 1: INTRODUCTION AND OVERVIEW

1.1 Power Conversion

1.1.1 Topologies

Power electronics is primarily concerned with the efficient conversion and conditioning of power. The four main areas of power conversion are:

1. Conversion (dc-to-dc)
2. Inversion (dc-to-ac)
3. Rectification (ac-to-dc)
4. Cycloconversion (ac-to-ac)

Power conversion can be from one voltage level to another, such as in dc-to-dc conversion or from one form to another, such as in dc-to-ac or ac-to-dc conversion or from one frequency to another, such as in ac-to-ac conversion.

In this thesis we are mainly concerned with the areas of dc-to-dc conversion and dc-to-ac inversion.

In each of the four types of power conversion listed above, three key areas can be identified [9]:

1. Topologies
2. Magnetics
3. Control

By *topologies* we mean those arrangements of inductors, capacitors and switches which form a working converter. In practical realizations of these converters, the semiconductor devices are almost invariably operated as switches, as this results in the most efficient processing of power. Inductive components, such as inductors or transformers, used in these topologies play an important part in the conversion process and thus the second key area of *magnetics* is identified. In order to guarantee converter performance in the face of uncertainty the aspect of *control* and, in particular, feedback control is identified as the third key area.

In this thesis it is the topological aspect of conversion which is addressed. Specifically, topologies that are useful for dc-to-dc conversion and dc-to-ac inversion are derived.

Within the area of topologies of different power conversion systems one can identity different conversion techniques, such as the three listed below.

1. Pulse-Width Modulated (PWM)

2. Resonant

3. Quasi-Resonant

Typical in PWM conversion systems are switching waveforms that are trapezoidal in shape. The non-zero switch voltage/current overlap during switching transitions causes large power dissipation for operation at high frequencies. In order to reduce the switching stress due to voltage/current overlap, the resonant and quasi-resonant topologies introduce resonant elements which reduce the rate of rise of switching waveforms. The recently introduced quasi-resonant [19,20,21] converters are derived from PWM converters by placing resonant components around the switching elements of a PWM converter. In fact, as the resonant components can be placed in a number of ways [45], a large number of quasi-resonant topologies can be derived from a single PWM topology.

PWM converter topologies play an important role since, as we've just seen, we can derive quasi-resonant converter counterparts through a rather straight-forward procedure. Moreover, dc-to-dc converter topologies form the basis for single-phase dc-to-ac inverter topologies.

The quasi-resonant waveform shaping techniques have, so far, been applied exclusively in the area of dc-to-dc conversion. Application of these techniques in the area of dc-to-ac inversion is presented for the first time in this thesis.

Therefore, in this thesis we are concerned with PWM dc-to-dc converter topologies and also quasi-resonant single-phase dc-to-ac inverter topologies.

1.1.2 Analysis

Along with addressing the issue of topologies comes the task of analysis of these topologies to determine steady-state, small-signal and large-signal performances. In this thesis, particular emphasis is given to the analysis of PWM converters and amplifiers/inverters and, in particular, in determining their large-signal models. A first-order approximation of this model gives the small-signal model. Two different analysis procedures are presented. In the first, the Volterra/Wiener approach to modelling nonlinear systems is used wherein the Volterra kernels are determined for PWM amplifiers/inverters. The second analysis procedure is, in fact, motivated by the PWM topology generation procedure given in this thesis. This analysis method determines circuit models of an important converter substructure (the one containing the nonlinear elements of the converter), known as the *PWM switch*. This substructure is present in almost all PWM converters and amplifiers/inverters and its derived models can then be used in analysis in an analogous fashion to ordinary transistor circuit analysis.

1.2 Objectives of the Research

The research into topologies and their analysis, presented in this thesis, resulted in the following areas of study in power conversion, inversion and analysis:

- The examination of basic PWM dc-to-dc converter structure with the aim of discovering fundamental properties and relationships between different converters

which would lead to a better understanding of converter functioning and performance. Basic converters, that is, converters that are devoid of transformers and tapped or coupled inductors, are of particular interest since from these converters a (usually) large number of converters can be derived.

- The determination of a classification scheme which more adequately classifies existing converters. Present classification schemes [7,8] do not account for the existence of a number of converters.

- The determination of whether there are still some undiscovered converters which have useful properties. To this end we would like to present a converter generation scheme with the hope that such a scheme is simple and will result in the generation of a large number of basic converters.

- The presentation of new analysis methods for the determination of the steady-state, small-signal and large-signal performances of converters and inverters. As previously mentioned, two different analysis approaches are presented in this thesis.

- The examination of basic single-phase inversion schemes and the assessment of their suitability for implementing quasi-resonant inverters. And then the derivation of a number of suitable quasi-resonant inverter topologies. Recall that the single-phase topologies we wish to derive can be done so from dc-to-dc converter topologies.

1.3 Thesis Outline

In the next chapter a generation and classification scheme for PWM dc-to-dc converter topologies is presented. In Chapter 3 the first of two analysis approaches is given, wherein nonlinear analysis is approached via the Volterra functional series. In Chapter 4 an alternative analysis approach is described which represents a considerable simplification to the Volterra series approach. The derivation of single-phase dc-to-ac inverter topologies using quasi-resonant techniques is presented in Chapter 5. Chapter 6 presents a summary which concludes the thesis.

Chapter 2: GENERATION AND CLASSIFICATION OF PWM DC-TO-DC CONVERTER TOPOLOGIES

2.1 Introduction

Over the past decade a number of different Pulse-Width Modulated (PWM) dc-to-dc converter topologies have appeared in the literature [1-6]. The methods used in deriving these converters do not, however, indicate any unifying connection between them. Whilst it would seem clear that there exists a basic set of converters from which others may be derived, a satisfactory enumeration of this basic set is yet to be determined. The present classification of basic converter topologies [7,8] does not account for the existence of several converters, for example, the well known Sepic converter [2,3]. In this chapter it will be seen that, in fact, the Sepic along with its dual/bilateral inversion counterpart and four other converters form the members of one particular family of

basic converters. Thus a unifying connection between seemingly unrelated converters is established.

Furthermore the "down" and "up" converters when first introduced by Landsman [10] were seen to be simply "topological transformations" of the buck and boost converters. We will see in a later section that these converters are the two other members of the family of converters of which the Cuk converter is a member.

Through the concept of a "canonical switching cell" Landsman was able to indicate the simple relationship between the buck, the boost and the buck-boost converters. Subsequently, a somewhat similar approach was taken by Rao [11] in the generation of converters. However, for the generation of *basic* converters Rao's approach suffers in that he considers a switching cell that includes a transformer and moreover he considers only one switching cell, as did Landsman.

An analytical approach to the generation of converters with specified properties or attributes is given by Erickson [5]. The two classes considered in [5] are (1) the class of single-inductor two-topology converters and (2) the class of converters featuring non-pulsating port currents. Converters in these two categories, not considered as distinct according to [5], are listed here because they have different electrical properties. Also, converter classes with conversion ratios which are not bilinear functions of the duty ratio, D and D' ($\equiv 1 - D$), are considered here as well.

For the generation of converter topologies the approach taken in this chapter is as follows; (1) given a converter we may identify a fundamental block hereafter referred to as the "converter cell", (2) with this cell one can generate other converters. This

approach is similar to that of Landsman [10] and Rao [11]. However, in contrast to previous work many different converter cells are considered from which different families of converters are derived. As a consequence of considering a large number of converter cells a more adequate classification of basic converter topologies than previously presented is proposed.

However, with the task of having to identify different converter cells comes the requirement of having to impose a certain structure on the converter cell. This is done also in an effort to present a more systematic basic converter topology generation scheme. Thus, to this end, only three-terminal converter cells devoid of transformers are considered. This contrasts Rao's work where the cell he considers is of a four terminal configuration which included a transformer. Whilst imposing a three-terminal structure on the converter cell seems restrictive at first, it is in fact quite efficacious, since for each three-terminal converter cell a family of three or six distinct members (depending on the symmetry of the cell) can be derived.

In the next section a formal definition of the term "converter cell" is given along with its relationship with basic converter structure. A number of different converter cells are subsequently used in the generation of converter-cell families. A classification of basic converter topologies is then proposed based on classification of converter cells. In Section 2.3 some selected converter properties and applications are examined. In particular some additions to the sets of two classes of converters previously considered by Erickson are made.

2.2 *Generation and Classification of Converter-Cell Families*

2.2.1 Basic Converter Structure

In this thesis only two-switch interval, alternatively, two-switched network or two topology, (for continuous inductor current conduction) and three-switch interval, alternatively, three-switched network or three topology, (for discontinuous conduction) basic PWM converters are considered. Moreover the general structure of dc-to-dc converters is assumed to be as shown in Fig. 2.1 where we see that a converter may be represented as consisting of three main parts:

1. the input voltage source
2. the converter cell
3. the output voltage sink, which consists of the parallel combination of the load resistance and output capacitor.

The converter cell is defined as the network remaining when the input source and output sink are removed. Alternatively, the converter cell may be defined as a topological combination of reactive elements (L's and C's) and switches arranged such that when an input voltage source and output voltage sink are connected the duty cycle has control of the output voltage. As we are interested in only basic converters, only converters devoid of transformers are considered. Thus the generic converter of Fig. 2.1

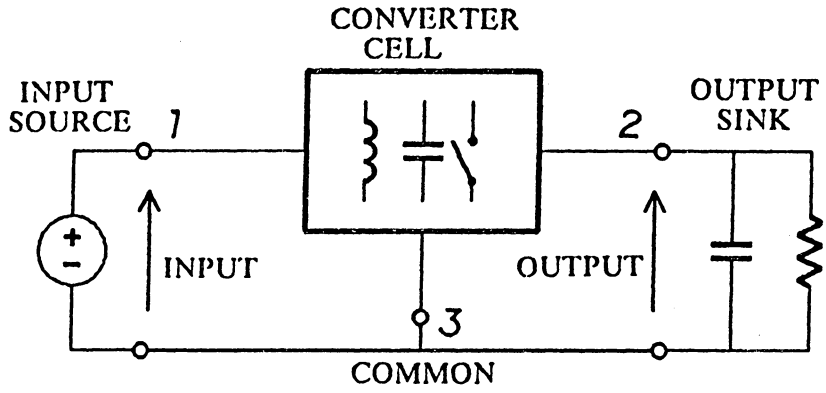


Fig. 2.1 *General structure of basic DC-to-DC converters.*

appears as an non-isolated converter with the further constraint of a common input/output line which prevents the load from floating.

A converter cell is now seen as a three-terminal device which can be connected in six different possible ways to the input source and output sink to generate different converters while preserving the general structure shown in Fig. 2.1. If we denote, arbitrarily, the three terminals of the cell as terminals 1 to 3 as shown in Fig. 2.2, the six ways of connection, designated as configurations 1 to 6, are listed in Table 2.1. Thus it is seen that the converter, as shown in Fig. 2.1, is connected in the configuration corresponding to configuration 5 in Table 2.1. Note that configurations 5 and 6 are bilateral inversions of each other, as are configurations 1 and 2 and also 3 and 4. Bilateral inversions are simply generated by the inversion of input source and output sink connections of a converter.

By using the terms input source and output sink we have tacitly assumed the property of unidirectional power flow in the converter from left to right. This is necessary, for the converter, in general, will feature different conversion properties when processing power in different directions, as will be seen later. Take for example the battery charger/discharger application. Power may flow in different directions at different times. Therefore a converter, for example, in configuration 5 which is processing power from left to right during some interval in time will need to be viewed as operating in configuration 6 when the direction of power flow reverses.

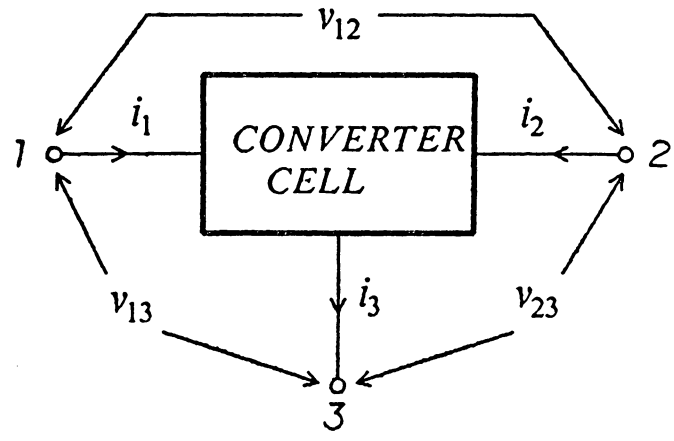


Fig. 2.2 *A three-terminal converter cell with designated terminal voltages and currents.*

Table 2.1 *The six ways of configuring a three-terminal converter cell to the input source and output sink. The table entries represent the terminal number of the converter cell.*

CONFIGURATION NUMBER	*1*	*2*	*3*	*4*	*5*	*6*
COMMON	*1*	*1*	*2*	*2*	*3*	*3*
INPUT	*2*	*3*	*1*	*3*	*1*	*2*
OUTPUT	*3*	*2*	*3*	*1*	*2*	*1*

2.2.2 Converter-Cell Generated Families - A Classification Scheme

It is evident from the six possible connections that, given a particular converter cell, a family of six converters may be derived. If however, for any of these configurations the converter cell is symmetric the number of distinct members of the family reduces to three. It is thus clear that a number of distinct converters may be generated from different converter cells. A classification scheme for these converters based on classification of converter cells is now proposed. These converter cells are classified according to their order, which indicates the number of storage elements used, and according to the number of single pole/single throw switches used. In this thesis only four classes of converter cells are considered and although higher order converter cells can be considered their usefulness becomes questionable. The four categories considered are:

1. 1st. order - 2 switch: converter cell A
   (1 family)
2. 1st. order - 4 switch: converter cell B
   (1 family)
3. 3rd. order - 2 switch: converter cells C to G
   (5 families)
4. 3rd. order - 4 switch: converter cells H to N
   (7 families)

These converter cells are shown in Table 2.2 along with their corresponding derived converters. No formal synthesis procedure is given for the derivation of these cells and

Table 2.2 *The converter-cell generated families of converters. See the text for an explanation of the active switch/conversion gain (M) entries in the table.*

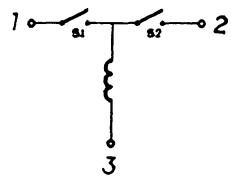
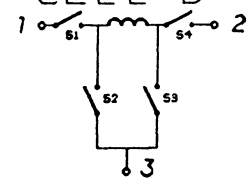
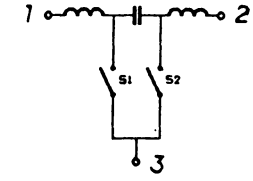
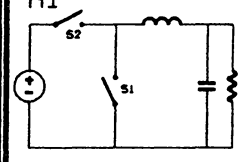
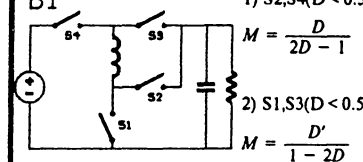
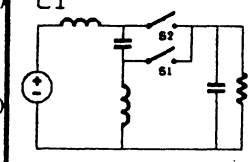
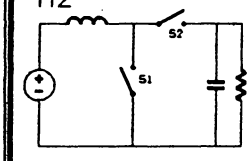
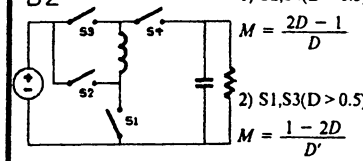
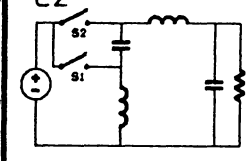
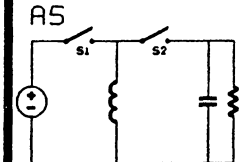
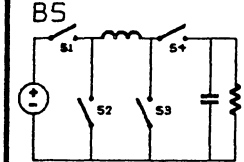
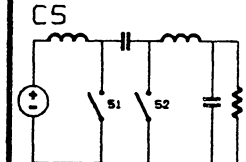
CONFIG.	CELL A	CELL B	CELL C
			
1	A1  S2 : $M = D$	B1  1) S2,S4(D < 0.5) $M = \frac{D}{2D-1}$ 2) S1,S3(D < 0.5) $M = \frac{D'}{1-2D}$	C1  S2 : $M = D$
2	A2  S1 : $M = \frac{1}{D'}$	B2  1) S2,S4(D > 0.5) $M = \frac{2D-1}{D}$ 2) S1,S3(D > 0.5) $M = \frac{1-2D}{D'}$	C2  S1 : $M = \frac{1}{D'}$
3	*THE SAME AS 1 ABOVE*	*THE SAME AS 1 ABOVE*	*THE SAME AS 1 ABOVE*
4	*THE SAME AS 2 ABOVE*	*THE SAME AS 2 ABOVE*	*THE SAME AS 2 ABOVE*
5	A5  S1 : $M = -\frac{D}{D'}$	B5  S1, S3 : $M = \frac{D}{D'}$	C5  S1 : $M = -\frac{D}{D'}$
6	*THE SAME AS 5 ABOVE*	*THE SAME AS 5 ABOVE*	*THE SAME AS 5 ABOVE*

Table 2.2 (cont'd).

* *The LC branch connected from source to ground or from sink to ground is redundant in these converters.*

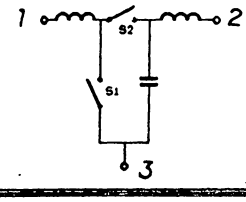
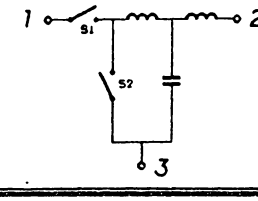
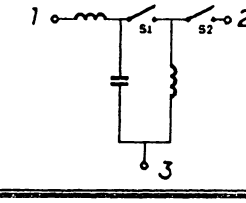
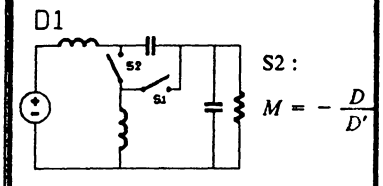
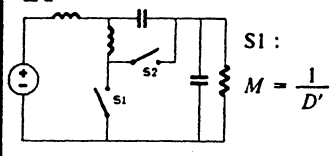
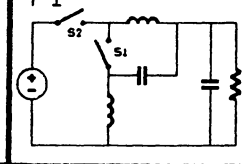
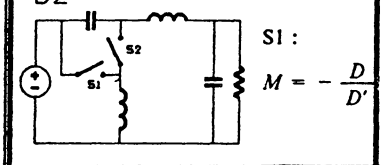
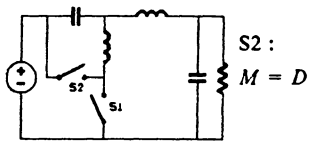
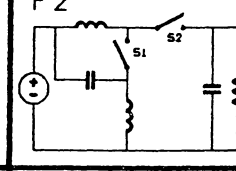
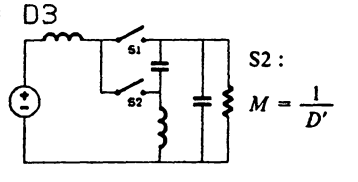
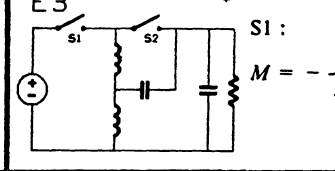
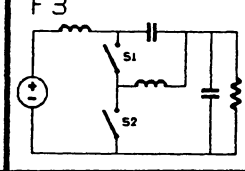
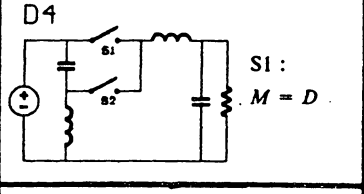
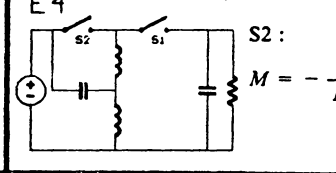
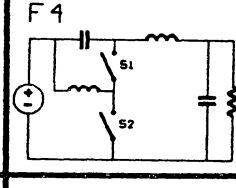
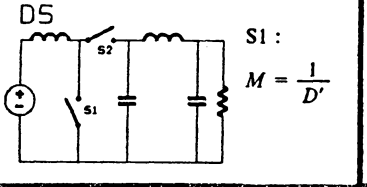
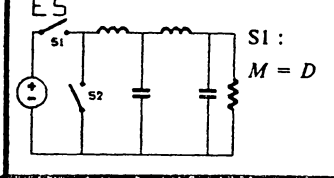
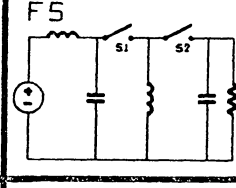
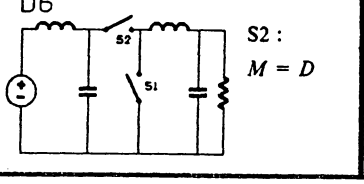
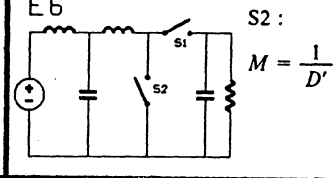
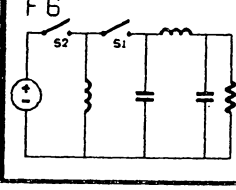
CONFIG.	CELL D	CELL E	CELL F
			
1	 S2 : $M = -\frac{D}{D'}$	 S1 : $M = \frac{1}{D'}$	 * S2 : $M = D$
2	 S1 : $M = -\frac{D}{D'}$	 S2 : $M = D$	 * S1 : $M = \frac{1}{D'}$
3	 S2 : $M = \frac{1}{D'}$	 * S1 : $M = -\frac{D}{D'}$	 S1 : $M = D$
4	 S1 : $M = D$	 * S2 : $M = -\frac{D}{D'}$	 S2 : $M = \frac{1}{D'}$
5	 S1 : $M = \frac{1}{D'}$	 S1 : $M = D$	 S1 : $M = -\frac{D}{D'}$
6	 S2 : $M = D$	 S2 : $M = \frac{1}{D'}$	 S2 : $M = -\frac{D}{D'}$

Table 2.2 (cont'd).

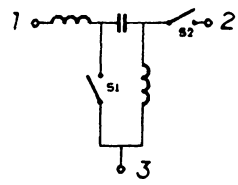
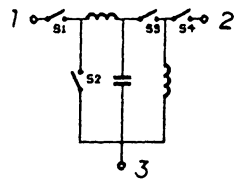
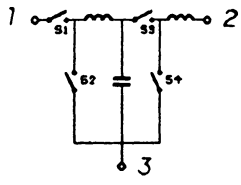
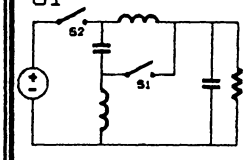
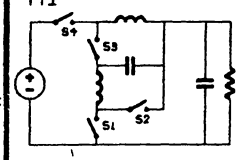
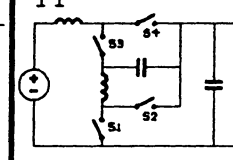
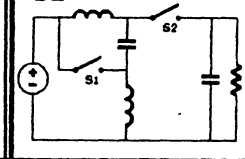
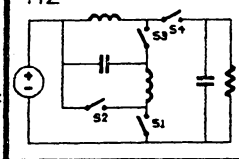
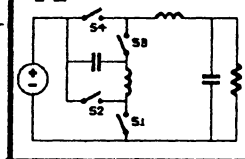
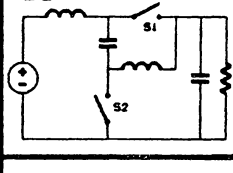
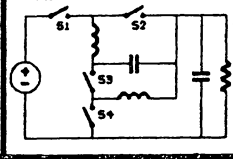
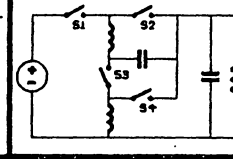
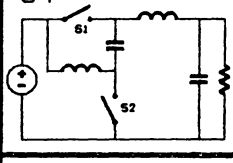
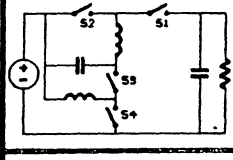
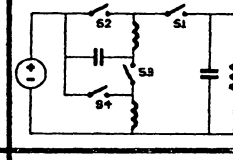
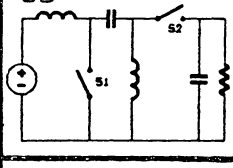
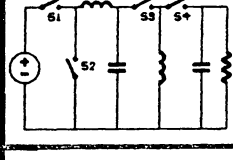
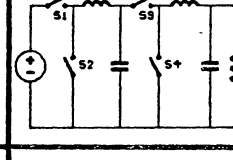
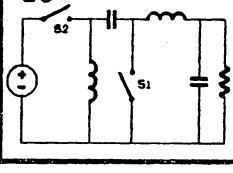
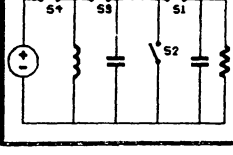
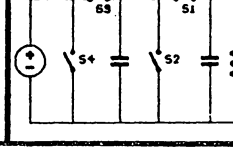
CONFIG.	CELL G	CELL H	CELL I
			
1	 1) S2 (D < 0.5): $M = \frac{D}{2D-1}$ 2) S1 (D < 0.5): $M = \frac{D'}{1-2D}$	 1) S2,S4 : $M = \frac{D}{D+D'^2}$ 2) S1,S4 : $M = \frac{1}{1+D'}$	 1) S1,S3 : $M = \frac{1}{1-D^2}$ 2) S1,S4 : $M = \frac{1}{1-DD'}$
2	 1) S1 (D > 0.5): $M = \frac{1-2D}{D'}$ 2) S2 (D > 0.5): $M = \frac{2D-1}{D}$	 1) S1,S3 : $M = \frac{D'+D^2}{D'}$ 2) S2,S3 : $M = 1+D$	 1) S2,S4 : $M = 1-D'^2$ 2) S1,S4 : $M = 1-DD'$
3	 1) S1 (D < 0.5): $M = \frac{D}{2D-1}$ 2) S2 (D < 0.5): $M = \frac{D'}{1-2D}$	 1) S1,S3 : $M = \frac{D^2}{D'+D^2}$ 2) S1,S4 : $M = \frac{D'}{1+D'}$	 1) S1,S3 : $M = \frac{D^2}{D^2-1}$ 2) S1,S4 : $M = \frac{DD'}{DD'-1}$
4	 1) S2 (D > 0.5): $M = \frac{1-2D}{D'}$ 2) S1 (D > 0.5): $M = \frac{2D-1}{D}$	 1) S2,S4 : $M = \frac{D+D'^2}{D'^2}$ 2) S1,S4 : $M = \frac{1+D'}{D'}$	 1) S2,S4 : $M = \frac{D'^2-1}{D'^2}$ 2) S1,S4 : $M = \frac{DD'-1}{DD'}$
5	 S1 : $M = \frac{D}{D'}$	 1) S1,S3 : $M = -\frac{D^2}{D'}$ 2) S1,S4 : $M = -D'$	 1) S1,S3 : $M = D^2$ 2) S1,S4 : $M = DD'$
6	 S2 : $M = \frac{D}{D'}$	 1) S2,S4 : $M = -\frac{D}{D'^2}$ 2) S1,S4 : $M = -\frac{1}{D'}$	 1) S2,S4 : $M = \frac{1}{D'^2}$ 2) S1,S4 : $M = \frac{1}{DD'}$

Table 2.2 (cont'd).

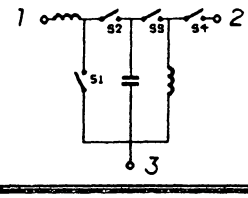
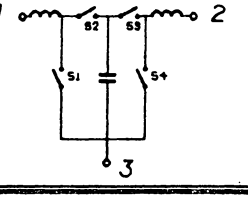
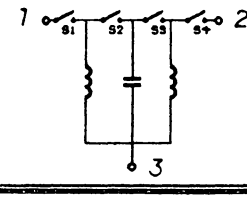
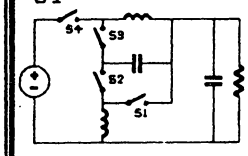
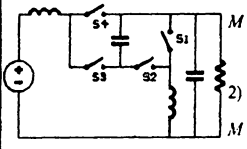
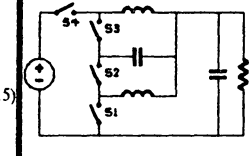
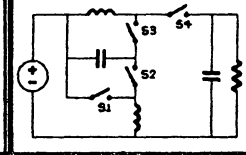
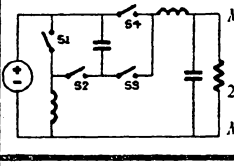
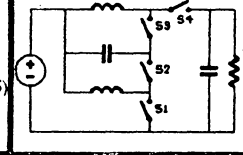
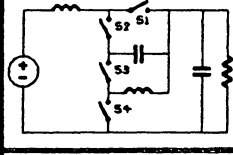
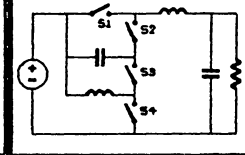
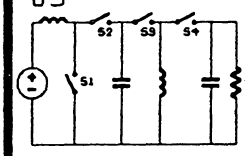
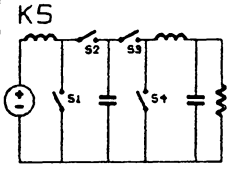
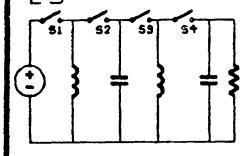
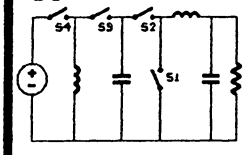
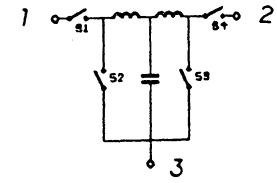
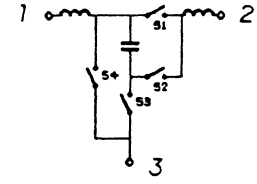
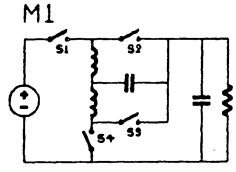
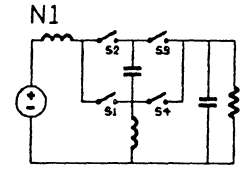
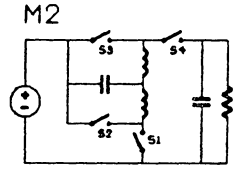
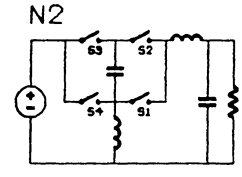
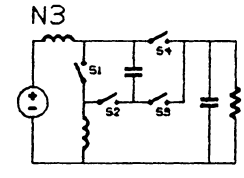
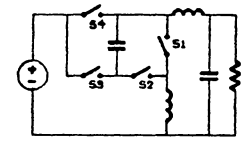
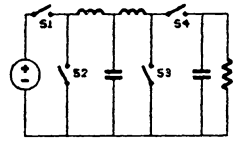
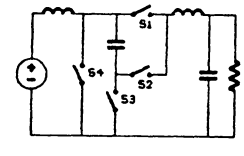
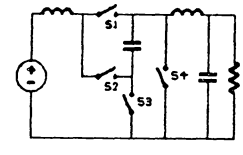
CONFIG.	CELL J	CELL K	CELL L
			
1	J1  S2,S4 : $M = \frac{D^2}{D' + D^2}$	K1  1) S1,S3(D < 0.5) $M = \frac{D'}{1 - 2D}$ 2) S2,S4(D < 0.5) $M = \frac{D}{2D - 1}$	L1  1) S2,S4(D < 0.5) $M = \frac{D^2}{2D - 1}$ 2) S1,S3(D < 0.5) $M = \frac{D'^2}{1 - 2D}$
2	J2  S1,S3 : $M = \frac{D + D'^2}{D'^2}$	K2  1) S1,S3(D > 0.5) $M = \frac{1 - 2D}{D'}$ 2) S2,S4(D > 0.5) $M = \frac{2D - 1}{D}$	L2  1) S1,S3(D > 0.5) $M = \frac{1 - 2D}{D'^2}$ 2) S2,S4(D > 0.5) $M = \frac{2D - 1}{D^2}$
3	J3  S1,S3 : $M = \frac{D}{D + D'^2}$	*THE SAME* *AS 1 ABOVE*	*THE SAME* *AS 1 ABOVE*
4	J4  S2,S4 : $M = \frac{D' + D^2}{D'}$	*THE SAME* *AS 2 ABOVE*	*THE SAME* *AS 2 ABOVE*
5	J5  S1,S3 : $M = -\frac{D}{D'^2}$	K5  S1,S3 : $M = \frac{D}{D'}$	L5  S1,S3 : $M = \left(\frac{D}{D'}\right)^2$
6	J6  S2,S4 : $M = -\frac{D^2}{D'}$	*THE SAME* *AS 5 ABOVE*	*THE SAME* *AS 5 ABOVE*

Table 2.2 (cont'd).

CONFIG.	CELL M	CELL N
		
1	M1  1) S1,S3(D < 0.5) $M = \frac{D}{2D-1}$ 2) S2,S4(D < 0.5) $M = \frac{D'}{1-2D}$	N1  S1,S3 (D < 0.5): $M = \frac{D}{D'}$
2	M2  1) S2,S4(D > 0.5) $M = \frac{2D-1}{D}$ 2) S1,S3(D > 0.5) $M = \frac{1-2D}{D'}$	N2  S2,S4 (D > 0.5): $M = \frac{D}{D'}$
3	*THE SAME AS 1 ABOVE*	N3  S2,S4 (D > 0.5): $M = \frac{2D-1}{D}$
4	*THE SAME AS 2 ABOVE*	N4  S1,S3 (D < 0.5): $M = \frac{D'}{1-2D}$
5	M5  S1,S3 : $M = \frac{D}{D'}$	N5  S2,S4 (D > 0.5): $M = \frac{1-2D}{D'}$
6	*THE SAME AS 5 ABOVE*	N6  S1,S3 (D < 0.5): $M = \frac{D}{2D-1}$

they are simply obtained from known converters. However, several new converter topologies are obtained by connecting these cells in the six different possible ways as explained earlier. These new converters include the following; D1 to D4, E1 to E4, F1 to F4, G1 to G4, H1 to H4, I1 to I4, J1 to J4, K1 and K2, L1 and L2, M1 and M2, and also N1 to N4. An alternative derivation of converters G1 to G4, to that given here, has subsequently appeared in [6]. In Chapter 5, converter G4, referred to there as the Sepic-variant converter, will be used in the synthesis of quasi-resonant inverters.

A few words about the format of Table 2.2 are now in order. In Table 2.2, for each cell considered, the family of converters which is generated from the different configurations, (as enumerated in Table 2.1), is given. An active switch assignment is also given along with the corresponding voltage conversion ratio (M). An active switch is defined as a switch in a converter which is controlled directly by the external control input. In a practical realization, this switch would be implemented by any of a variety of three-terminal semiconductor switches, such as a bipolar or a field effect transistor. Other switches, not considered active switches, can be indirectly controlled by the state of the active switch and other circuit conditions. These switches can be simply implemented as diodes. In terms of an active switch assignment it can be seen from Table 2.2 that for converter B1 of converter-cell B family, for example, two sets of active switch assignments can be made. First, switches S2 and S4 need to be the active switches for duty ratios (referred to these switches) of less than a half. The resulting voltage gain is $M = D/(2D - 1)$. A second active switch assignment is given with S1 and S3 as the active switches for operation with duty ratios (referred to these switches) of also less than a half. The resulting voltage gain is $M = D'/(1 - 2D)$, where $D' \equiv 1 - D$.

It can be seen from the family of converter-cell A that the buck, boost, and buck-boost belong to the same family. Also, the Cuk converter is seen to be one of the three members of converter-cell C family. Hence the classification of basic converter topologies given in [7,8] as Buck, Boost, Buck-boost and Cuk is not complete.

The classification and choice of converter cells given above is not arbitrary and is now explained. It is seen in this classification that three-switch cells are not considered because they correspond to three-switched intervals in continuous conduction mode as is the case of the converters considered in [12] and [13]. Three-switched interval mode of operation is not specifically considered in this thesis although the four-switch converter cell families can provide this mode of operation. For example, in converter B5 of converter-cell B family if S1 is turned off while S3 is on the inductor current will idle through S2 and S3. After this idling period S3 is opened giving rise to three-switched intervals in continuous conduction mode of operation. The motivation for eliminating cells with three switches has thus been explained. Next we consider the order of the cell. It is seen that the storage element in the first order cells is an inductor and not a capacitor. This is explained by requiring all ports of the converter cells considered to be *voltage ports* rather than *current ports.* This requirement is imposed since at the input a voltage source will be connected and at the output we wish to derive a voltage. Those ports which can be considered current ports will be redundant as current ports because the inductor of the source will combine with the inductor of the switch(es). For example, for cell A if port 3-1 is considered as a current port the inductor of the cell will be redundant. Therefore, since current ports are not considered here, a first-order cell with a capacitor as shown in Fig. 2.3 is not considered. It should be noted that no converters are lost or unaccounted for because of this restriction because converter-cell C

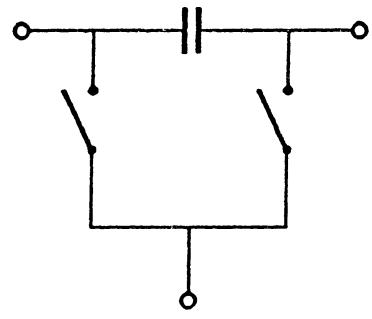


Fig. 2.3 *A first-order two-switch converter cell with current ports.*

automatically will include these cases. The choice of the first-order two-switch cell and also the first-order four-switch cell is now entirely explained.

It is seen that second-order two-switch cells are not considered either. This is easily explained by the choice of port characterization. To obtain a second-order cell from the first-order cell we would require a capacitor to be connected in parallel with any port which would be redundant since all ports are required to be voltage ports. This eliminates the choice of second-order two-switch cells. Since second-order three-switch cells are eliminated the next higher category considered is the third-order two-switch cell, of which all possible configurations with voltage port requirements give rise to converter cells C to G. Except for converter-cell N, the third-order four-switch cells are arrived at by cascading lower order cells. All possible cascade connections are given by converter cells H to M.

Note that the capacitor present in cells H to M are shown in Table 2.2 with a connection to terminal 3. In fact, this connection can be made to any of the three terminals of the cell without altering the conversion gain of any of the converters generated by the cells. Interestingly, if the cell capacitor connection of converter K5, for example, is moved from ground to the input we find that the topologies of the resultant converter are identical to that of converter G6. Alternatively, if this connection is made instead to the output, we find that the resulting converter topologies are identical to that of converter G5. Similar statements can be made showing the relationships between converters K1 and K2 and converters G1 to G4.

Switch reduction can be achieved in a number of the third-order four-switch cells. For cells J, K, and L the capacitor of the cell can be placed across the series connection

of switches S2 and S3. These switches can then be removed as they no longer serve any purpose and a reduction of switch number is effected. The resulting cells are identical to cells G, C, and the cell shown in Fig. 2.4c, respectively. All converters derived from cells J, K, L, G, and C are electrically distinct, however, and are thus included in Table 2.2. The cell of Fig. 2.4c along with other cells, such as those of Fig. 2.4a and 2.4b, have not been included in Table 2.2 nor in any of the four converter cell categories listed as they are not considered as *basic*. If we consider the cells of Fig. 2.4a and 2.4b, for example, it can be readily appreciated that the series LC branch in the cells do not alter the basic behavior of the cell without these extra elements. It is interesting to note in passing, however, that by implementing suitable coupling between the two inductors of the cell, zero current ripple in terminal 3 (which may represent the input or output ripple current of a converter) may be achieved, to a first order.

2.3 Selected Converter Properties and Applications

Having now generated a plethora of converters from fourteen different converter cells let us now look at some converter properties and applications.

2.3.1 The Class of Two-Topology Single-Inductor Converters

Members of converter-cell families A and B belong to the class of two-topology single-inductor converters. Tapped inductors can be used in family B to reduce the number of switches required. The converter of Fig. 2.5 may be derived from converter

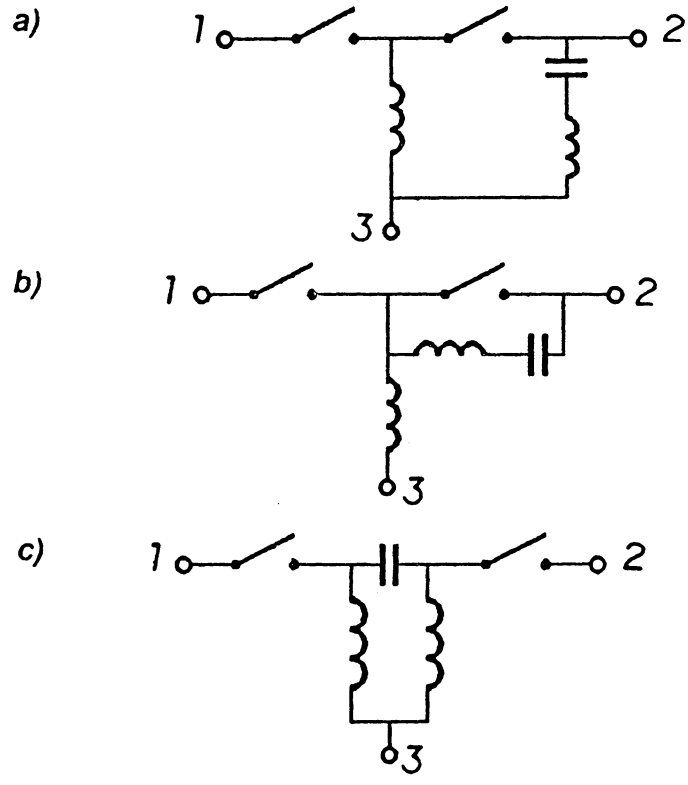


Fig. 2.4 *These converter cells are examples of cells which have not been considered as basic and, as such, are not included in the categorisation of basic converters.*

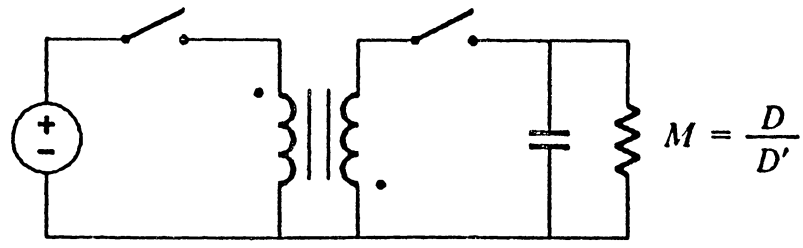


Fig. 2.5 *A member of the class of single-inductor, two-topology converters.*

B5 in this way. These converters have the same M but are electrically distinct. A simple permutation of the cell in Fig. 2.5 will generate the Watkins-Johnson converter and its inverse as considered in [5].

2.3.2 The Class of Converters Featuring Non-pulsating Port Currents

Erickson [5] has listed seven converters as being the distinct members of this class. Thirteen other converters which belong to this class, not considered as distinct in [5], are listed here because they have different electrical properties. For example, converters C1 and D6, considered identical by Erickson [16], have different average currents in one of the inductors.

Let us now examine a port current property of a converter cell. With reference to Fig. 2.2 we see that $\tilde{i}_1 + \tilde{i}_2 = \tilde{i}_3$, where $\tilde{i}_1$, $\tilde{i}_2$ and $\tilde{i}_3$, denote the instantaneous current levels flowing in terminals 1, 2 and 3, respectively. Therefore if the input and output currents $\tilde{i}_1$ and $\tilde{i}_2$, respectively, are non-pulsating, so $\tilde{i}_3$ will also be non-pulsating. Therefore, if one converter of a particular family features non-pulsating port currents then all converters of this family will feature the same property. It is seen then, that converters derived from converter cells C, D, K and N all feature non-pulsating port currents and it is from these converter cells that the thirteen extra members of this class may be derived.

2.3.3 Converter Applications

From the plethora of converters generated from the fourteen converter-cells considered we find some new and peculiar and useful dc conversion ratios emerge. For example, converters featuring dc conversion ratios that allow an output voltage of either polarity to be achieved may prove to be useful in dc-to-ac applications. Converters with the following conversion ratios allow either polarity of output voltage: $(2D-1)/D$, $(1-2D)/D'$, $(2D-1)/D^2$ and $(1-2D)/D'^2$ where $D' \equiv 1-D$. These conversion ratios are featured by converters in the following converter-cell families: B, G, K, L, M and N. As previously stated, converter G4 will be of special interest in Chapter 5 where a number of inverter topologies will be derived. Note also that the above listed conversion ratios achieve a large voltage step-down without requiring a very small duty ratio (and without a transformer). In fact, for duty ratios very close to $D = 0.5$ extremely large step-downs may be achieved and also at these values of duty ratios operation at very high frequencies is feasible. In conjunction, these properties are desirable for some applications [14].

Whilst all switches so far have been considered as ideal bidirectional switches, it is more cost effective and convenient in actual implementations (and if the application permits) to use unidirectional switches. This leads to the task of active switch assignment. From an appreciation of the function of an active switch one can make this assignment. For every pair of switches in a converter there is an associated inductor. An active switch provides a path for an increasing current in this inductor. This clearly must be the case as an active switch can turn off this increasing current, whereas, an inactive switch could not do so. A procedure for active switch assignment is given in the

following. Initially the active switch(es) can be arbitrarily assigned. A steady-state analysis is then performed on the converter from which positive inductor current directions and capacitor voltage polarities can be indicated. Given the direction of inductor current flow, an increasing current in an inductor implies a certain voltage polarity across the inductor. For the active switch assignment under consideration to be satisfactory, the voltage polarities across the inductor(s) (found from the steady-state analysis) during the interval when the active switch is on, must be consistent with the implied voltage direction of an increasing current in the inductor during this interval of the switching cycle. If there is a conflict an alternative switch assignment is made and the procedure is repeated until a satisfactory assignment is achieved.

2.4 Converter Analysis

In this chapter the concept of a converter cell has been utilized solely for the purposes of generation and classification of converter topologies. The concept, however, is even more versatile as converter cells can also be used most effectively in the analysis of the converters they generate. Each converter cell can be treated as a three-terminal device for which circuit models can be derived obviating the need to rederive these models for each of the converters of a particular family. The cell model can then be substituted point-by-point for the cell in any of the converters derived by the cell to give the converter model which can then be solved.

This approach to converter analysis is analogous to ordinary transistor circuit analysis. A converter cell and a transistor are both nonlinear three-terminal devices.

Operation of these devices for small excursions about a dc operating point allows one to derive small-signal models, for example, the hybrid-pi model of a transistor. Once these models have been derived the nonlinear device itself, be it the converter cell or a transistor, in a particular circuit may be replaced point-by-point by its linearized model. This allows ordinary linear circuit analysis techniques to be used to analyze the circuit within which the nonlinear device was imbedded, be it a converter or a transistor circuit.

With this analogy with ordinary transistor circuits we can see the analogy between the configurations of a converter cell in a family corresponding to the different configurations of a transistor in a circuit e.g. common base or common emitter configurations.

More detail on this approach to analysis is given in Chapter 4, where circuit models of the *PWM switch*, the nonlinear subcircuit of the converter-cell, are derived. These models can then be used in the dc, small-signal and large-signal analyses of PWM conversion systems. For the present, the relationship between the dc voltage gain ratios of different members of a converter-cell family, used in finding the conversion gains, M, given in Table 2.2, will be derived.

2.4.1 General dc Conversion Ratio Relationships Between Converter-Cell Family Members

As we have seen, a family of converters may be derived from one converter cell. Thus there exists a general relationship between the terminal voltages and currents between the different members of a family. In the following the general relationship between the

dc voltage conversion ratios of different family members will be derived (for the particular case of continuous inductor current conduction).

With reference to Fig. 2.2 let us denote the voltages between terminals 1 and 2, 2 and 3, and also 1 and 3 of the converter cell as v_{12}, v_{23} and v_{13}, respectively. Now, if we consider the converter cell in configuration 5 we have, as indicated in Table 2.1, terminal 3 as the common terminal, the input source being connected across terminals 1 and 2, and the output is taken across terminals 2 and 3. Let us now denote the voltage gain in continuous conduction mode from the input to the output as some function, f, of the duty cycle, D. Thus we have,

$$\left.\frac{\textit{output voltage}}{\textit{input voltage}}\right|_{\textit{config. 5}} = \frac{v_{23}}{v_{13}} = f(D) \tag{2.1}$$

So given (2.1) we may now derive the converter dc voltage gain relationship of any of the other configurations. For example, let us find the dc gain of a converter in configuration 4. Thus we would like to find

$$\left.\frac{\textit{output voltage}}{\textit{input voltage}}\right|_{\textit{config. 4}} = \frac{v_{12}}{v_{32}} = g(D) \tag{2.2}$$

where g is some function of D. Given (2.1) we can find how $g(D)$ is related to $f(D)$:

$$g(D) = \frac{f(D) - 1}{f(D)} \tag{2.3}$$

A summary of the dc voltage gains, M, for all the six different configurations is given in Table 2.3 in terms of the voltage gain of the converter in configuration 5, i.e. in terms

Table 2.3 *Relationship of the DC voltage conversion ratios (M) for the different members of a family.*

CONFIG. NUMBER	*1*	*2*	*3*	*4*	*5*	*6*
M	$\frac{1}{1-f(D)}$	$1-f(D)$	$\frac{f(D)}{f(D)-1}$	$\frac{f(D)-1}{f(D)}$	$f(D)$	$\frac{1}{f(D)}$

of $f(D)$. Note that the voltage gain entries given in Table 2.3 hold if the active switch position in the converter cell is invariant for the different configurations. In practice we find that the active switch position changes. This happens, in particular, for family members which are bilateral inversions of each other. If the active switch position changes the relevant entry in Table 2.3 for the conversion ratio also changes by the simple replacement of $1 - D$ for D.

2.5 Summary

From consideration of the structure of basic converter topologies one can identify three fundamental component blocks: (1) the input source, (2) the converter cell, and, (3) the output sink. Whilst the input source and output sink are invariant in structure, the converter cell, in contrast, may be either variant or invariant in structure. It is also variant in configuration to the input source and output sink. The converter-cell structure considered is of a three-terminal arrangement. The variations in configuration, of a particular converter cell, between input source and output sink, lead to the generation of a family of converters derived from this cell. Depending on the symmetry of the cell, three or six different converters may be generated. Different converter-cell structures will generate different converter families. Fourteen distinct basic converter cells have been considered in this chapter. A classification of basic converter topologies has been proposed based on classification of converter cells which are categorized according to their order and switch number. The fourteen cells considered have been categorized into four different classes. A number of new basic converter topologies have been generated. From these basic topologies, isolated versions may be derived. For an illustration of how

isolation may be introduced into basic topologies see, for example, [15]. By increasing the order and/or the switch number a greater number of converter cells may be considered. However, the usefulness of the resulting converters would be dubious.

Chapter 3: NONLINEAR ANALYSIS VIA THE VOLTERRA FUNCTIONAL SERIES

3.1 Introduction

Of particular importance in the design of converters is the derivation of converter models to assess small-signal and large-signal performances. Small-signal models provide a means of assessing local stability and are of great importance in the design of the feedback loop in regulated converters. On the other hand, large-signal models are obtained mainly in assessing the spectral purity of waveforms in systems where the integrity of the waveshape is important. Such systems include amplifiers, inverters and input-current-shaping ac-to-dc converters. This latter category, however, is not dealt with specifically in this thesis.

Small-signal analysis is synonymous to finding the response of the fundamental frequency component of the signal of interest (which is usually the output) to a

sinusoidal input excitation. Only in the case of dc-to-dc converters will the response actually be "small-signal," thus the standard terminology of "small-signal" can sometimes be somewhat of a misnomer. For dc-to-ac inverters or amplifiers and input-current-shaping ac-to-dc converters the fundamental frequency component of the signal of interest is large consequently the harmonic frequency output is usually no longer negligible. A large-signal analysis entails not only finding the response of the fundamental frequency component by using the small-signal model but also involves determining the harmonic frequency content. Thus the large-signal analysis provides an assessment of the *harmonic distortion* performance of the system.

In this chapter the control-to-output response of PWM dc-to-dc converters and dc-to-ac amplifiers/inverters is characterized via the Volterra functional series. As the use of this approach to nonlinear analysis has not, in the author's knowledge, appeared anywhere previously in the power electronics literature, a brief overview of this approach is given in this chapter.

Volterra first proposed this series in some of his work dated around 1910. Some of this work is presented in English in [23]. The original application of the Volterra series to the analysis of nonlinear circuits is due to Wiener [22] in 1942. Since then the Volterra series has been successfully applied in the analysis of a diverse variety of systems (for examples, see [24] and [25] and references therein).

The application of the Volterra series is restricted to systems which are "mildly" nonlinear as are the systems discussed in this thesis. Recent work [25] has been aimed at extending the classical Volterra series to handle highly nonlinear systems such as those featuring a saturation nonlinearity. Other recent work [26] has centered on applying rigor and consolidating some of the mathematical theory behind the series.

In this chapter, in applying the Volterra-Wiener theory, as it is known [27,30,31], to the nonlinear analysis of PWM conversion circuits, we first approximate what are essentially nonlinear time-varying sampled-data systems by a nonlinear time-invariant continuous-time model. This approach considerably simplifies the subsequent analysis. This model, which gives an internal representation of the system, is derived in Section 3.4. The Volterra series, characterizing an input/output representation of the PWM converter systems, is derived from this model in Section 3.5. But first, an overview of the Volterra series is presented in Section 3.2. In Section 3.3 the utility of the Volterra series approach in determining the nonlinear output response to a sinusoidal input is shown.

3.2 Nonlinear Systems Analysis

A system can be defined in a mathematical sense as a rule by which an input u is transformed into an output y. The rule can be expressed symbolically as

$$y(t) = \underline{T}[u(t)] \tag{3.1}$$

In this chapter, an operator is denoted by an under bar. In the following discussion, we will restrict ourselves to time-invariant systems. These are systems in which the operator $\underline{T}$ does not vary with time. Thus, if $y(t) = \underline{T}[u(t)]$, then for a time-invariant system, $y(t+\tau) = \underline{T}[u(t+\tau)]$ for any value of τ since the rule by which an input time function is transformed into an output time function does not change with time. If a system is linear and time invariant (LTI), then the output $y(t)$ can be expressed as the convolution of the input $u(t)$ with the system unit impulse response $h(t)$:

$$y(t) = \int_{-\infty}^{\infty} h(\tau)u(t-\tau)d\tau \tag{3.2}$$

The system unit impulse response $h(t)$ completely characterizes the LTI system since, once known, the response to any input can be determined from (3.2).

We also note from (3.2) that the contribution of the value of the input t' seconds in the past to the present value of the output is determined by $h(t')$. In this sense, the unit impulse response represents the memory of the LTI system. If the LTI system has no memory, then $h(t) = c\delta(t)$ in which $\delta(t)$ is the unit impulse and the system response is $y(t) = cu(t)$. The graph of $y(t)$ versus $u(t)$ for this case is a straight line.

If a no-memory system is nonlinear, then the graph of $y(t)$ versus $u(t)$ is a curve which, provided certain conditions are satisfied, can be expressed in a Taylor series

$$y(t) = \sum_{n=0}^{\infty} c_n u^n(t) \tag{3.3}$$

The extension of (3.3) to nonlinear time-invariant systems with memory is the Volterra series

$$y(t) = h_0 + \int_{-\infty}^{\infty} h_1(\tau)u(t-\tau)d\tau + \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} h_2(\tau_1, \tau_2)u(t-\tau_1)u(t-\tau_2)d\tau_1 d\tau_2$$

$$+ \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} h_3(\tau_1, \tau_2, \tau_3)u(t-\tau_1)u(t-\tau_2)u(t-\tau_3)d\tau_1 d\tau_2 d\tau_3 + \ldots \tag{3.4}$$

The function $h_n(\tau_1, \ldots, \tau_n)$ is called the *nth* order Volterra kernel or the *nth* order impulse response of the system. The multiple Laplace transform of the *nth* order impulse response

$$H_n(s_1, s_2, \ldots, s_n) = \begin{cases} h_0 \quad , \quad n = 0 \\ \\ \int_{-\infty}^{\infty} \cdots \int_{-\infty}^{\infty} h_n(\tau_1, \ldots, \tau_n) e^{(-s_1\tau_1 - \ldots - s_n\tau_n)} d\tau_1 \ldots d\tau_n \end{cases} \tag{3.5}$$

$$n = 1,2,3, \ldots$$

is called the *nth* order transfer function of the system. Observe that the *nth* order kernel, and hence also its transform, is not unique in the sense that several distinct *nth* order kernels may give the same *nth* order output for the same input. However, the *symmetrized kernel* and its associated *symmetrized transform* defined by (3.6) and (3.7), respectively, below are unique.

$$\bar{h}_n(\tau_1, \tau_2, \ldots, \tau_n) \equiv \frac{1}{n!} \sum_{\pi(.)} h_n(\tau_{\pi(1)}, \tau_{\pi(2)}, \ldots, \tau_{\pi(n)}) \tag{3.6}$$

$$\bar{H}_n(s_1, s_2, \ldots, s_n) \equiv \frac{1}{n!} \sum_{\pi(.)} H_n(s_{\pi(1)}, s_{\pi(2)}, \ldots, s_{\pi(n)}) \tag{3.7}$$

where $\pi(.)$ denotes any permutation of the integers 1,...,n, and where the summations are over all $n!$ permutations of these integers.

As a LTI system is completely characterized by its unit impulse response, so a nonlinear system which can be represented by a Volterra series is completely characterized by its Volterra kernels.

Another way of expressing (3.4) is

$$y(t) = h_0 + \underline{H}_1[u(t)] + \underline{H}_2[u(t)] + \ldots + \underline{H}_n[u(t)] + \ldots \tag{3.8}$$

in which

$$\underline{H}_n[u(t)] = \int_{-\infty}^{\infty} \ldots \int_{-\infty}^{\infty} h_n(\tau_1, \ldots, \tau_n) u(t-\tau_1) \ldots u(t-\tau_n) d\tau_1 \ldots d\tau_n \tag{3.9}$$

In this representation the symbol $\underline{H}_n$, which represents the multi-dimensional convolution, is called an *nth* order Volterra operator or functional. Figure 3.1 is a schematic representation of (3.8) as the sum of the outputs of the systems with the operators $\underline{H}_n$.

The Volterra series is a power series with memory. This can be seen by changing the input by a gain factor c so that the new input is $cu(t)$. By use of (3.8) and (3.9), the new output is then

$$y(t) = h_0 + \sum_{n=1}^{\infty} \underline{H}_n[cu(t)]$$

$$= h_0 + \sum_{n=1}^{\infty} c^n \underline{H}_n[u(t)] \tag{3.10}$$

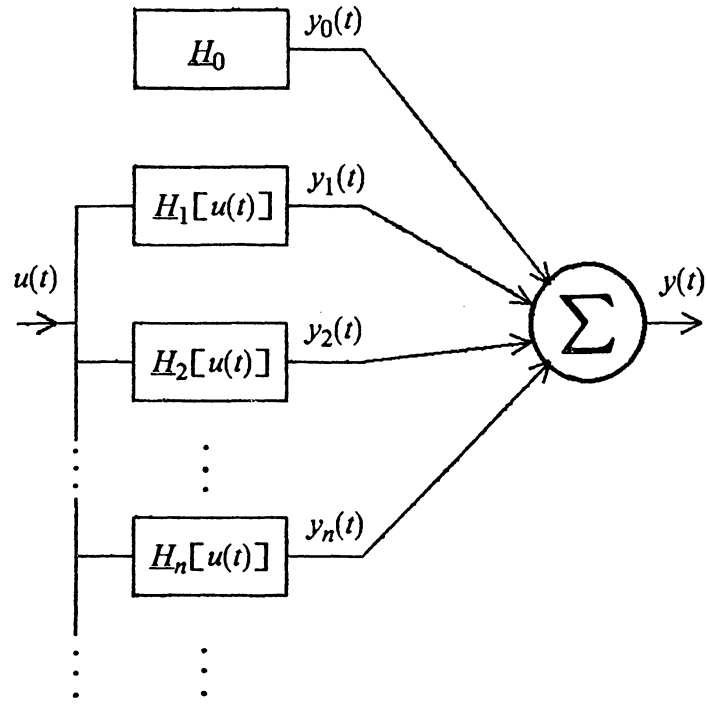


Fig. 3.1 *A nonlinear system partitioned into integer order Volterra systems.*

which is a power series in the amplitude factor c. It is a series with memory since the integrals for $H_n[u(t)]$ given in (3.9) are convolutions.

3.3 Nonlinear Response

Having characterized the nonlinear system by a Volterra series we can now determine the response of the system to any input. For harmonic distortion analysis the input is a sinusoid.

$$u(t) = U \cos \omega_0 t \tag{3.11a}$$

$$= \frac{U}{2} e^{j\omega_0 t} + \frac{U}{2} e^{-j\omega_0 t} \tag{3.11b}$$

By substituting (3.11b) into the first-order Volterra operator, and using (3.5), the response, $y_1(t)$, due to the linear part of the system to a sinusoidal input can be found.

$$\begin{aligned} y_1(t) &= \underline{H}_1[U \cos \omega_0 t] \\ &= U\,|H_1(j\omega_0)|\, \cos(\omega_0 t + \arg[H_1(j\omega_0)]) \end{aligned} \tag{3.12}$$

Similarly it can be found that the response, $y_2(t)$, of the second-order Volterra operator is given by

$$\begin{aligned} y_2(t) &= \underline{H}_2[U \cos \omega_0 t] \\ &= \frac{U^2}{2} |H_2(j\omega_0, j\omega_0)| \cos(2\omega_0 t + \arg[H_2(j\omega_0, j\omega_0)]) \\ &\quad + \frac{U^2}{2} |H_2(j\omega_0, -j\omega_0)| \cos(\arg[H_2(j\omega_0, -j\omega_0)]) \end{aligned} \tag{3.13}$$

Thus, we see that the second harmonic and dc frequency components appear at the output due to this operator.

The output, $y_3(t)$, of the third-order Volterra operator is given by

$$\begin{aligned} y_3(t) &= \underline{H}_3[U\cos\omega_0 t] \\ &= \frac{U^3}{4}\,|H_3(j\omega_0, j\omega_0, j\omega_0)|\cos(3\omega_0 t + \arg[H_3(j\omega_0, j\omega_0 j\omega_0)]) \\ &\quad + \frac{3U^3}{4}\,|H_3(j\omega_0, j\omega_0, -j\omega_0)|\cos(\omega_0 t + \arg[H_3(j\omega_0, j\omega_0, -j\omega_0)]) \end{aligned} \tag{3.14}$$

Thus the third harmonic and fundamental frequencies result. It should be noted that the higher order contributions to the output are usually of negligible amplitude when compared with the lowest order contribution at a particular frequency. Thus, for example, the contribution at the fundamental frequency from the third-order operator as given in (3.14) can generally be neglected as the response of the first-order operator given in (3.12) dominates.

Therefore, one can assess second harmonic distortion (HD_2) and third harmonic distortion (HD_3) relative to fundamental frequency output as follows.

$$HD_2 = \frac{U}{2}\,\frac{|H_2(j\omega_0, j\omega_0)|}{|H_1(j\omega_0)|} \tag{3.15}$$

$$HD_3 = \frac{U^2}{4}\,\frac{|H_3(j\omega_0, j\omega_0, j\omega_0)|}{|H_1(j\omega_0)|} \tag{3.16}$$

From the foregoing we see that to determine the distortion performance of a system we need knowledge of the Volterra kernels and in particular their form in the transform domain. That is, we require the *nth* order transfer functions, H_n, $n = 1,2,3,\ldots,$ of the

system. These transfer functions can be determined from an internal state-space description of the system. The derivation of such a description for PWM converters is given next. And subsequently the Volterra kernels are determined in a later section.

3.4 Converter Nonlinear State Model

In this section, the nonlinear state equations which describe PWM converters operating in the continuous conduction mode are derived. By using the "linear-ripple approximation" the nonlinear sampled-data system exemplified by the PWM converter is well aproximated by a nonlinear continuous-time model [32].

The first step in deriving this model is to write the linear state equations of the converter during the two switched intervals dT_s and $d'T_s$, where d is the duty ratio and $d' \equiv 1 - d$ and T_s is the switching period.

$$\dot{x}(t) = A_i x(t) + b_i V_g \quad , \; i = 1,2 \tag{3.17a}$$

$$y(t) = c^T x(t) \tag{3.17b}$$

where $i = 1$ during dT_s and $i = 2$ during $d'T_s$, and x is the state vector, V_g is the input, y is the output.

The "variation of parameters" solution of (3.17a) is

$$x(t) = e^{A_i(t-t_0)}x(t_0) + \int_{t_0}^{t} e^{A_i(t-\tau)}b_i V_g d\tau$$
$$= e^{A_i(t-t_0)}x(t_0) + A_i^{-1}\left[e^{A_i(t-t_0)} - I\right]b_i V_g \quad , \; i = 1,2 \tag{3.18}$$

provided A_i^{-1}, $i = 1,2$ exist.

The difference equation describing the propagation of the initial state vector from cycle to cycle can be formed by simply "connecting" the solutions (3.18) at the subinterval boundaries.

$$x[(n+1)T_s] = e^{A_2 d' T_s} e^{A_1 d T_s} x(nT_s)$$
$$+ e^{A_2 d' T_s} A_1^{-1}(e^{A_1 d T_s} - I)b_1 V_g + A_2^{-1}(e^{A_2 d' T_s} - I)b_2 V_g \tag{3.19}$$

Equation (3.19) describes the propagation of the initial state vector exactly, however, the subsequent analysis is greatly simplified by invoking the "linear-ripple approximation" which approximates the matrix exponentials appearing in (3.19) by the first two terms of their Taylor series expansions. This approximation is valid when the natural frequencies of the converter are all well below the switching frequency such that the solutions (3.18) are approximately linear. This is the case for a well designed PWM converter. Invoking this approximation in (3.19) and eliminating second order terms results in

$$x[(n+1)T_s] = [I + (dA_1 + d'A_2)T_s]x(nT_s) + (db_1 + d'b_2)T_s V_g \tag{3.20}$$

Equation (3.20) is the simplified difference equation which describes the response of the system. A continuous time model can be derived by using the Euler forward-differencing

approximation to estimate the continuous-time derivative of the state-vector, as shown below.

$$\frac{dx(t)}{dt} \approx \frac{x[(n+1)T_s] - x(nT_s)}{T_s} \tag{3.21}$$

This approximation is valid if all the natural frequencies of the converter are much lower than the switching frequency.

Applying (3.21) to (3.20) results in the continuous-time model.

$$\frac{dx(t)}{dt} = (dA_1 + d'A_2)x(t) + (db_1 + d'b_2)V_g \tag{3.22}$$

Perturbation of the duty ratio about a steady-state operating point will result in perturbation of the state vector and the output, so that

$$d = D + \hat{d} \tag{3.23a}$$

$$x = X + \hat{x} \tag{3.23b}$$

$$y = Y + \hat{y} \tag{3.23c}$$

where capitalized quantities represent steady-state values and perturbed quantities are indicated with a caret.

Substituting (3.23) into (3.22) and also (3.17b) and dropping steady-state terms we arrive at the final nonlinear continuous-time incremental model of the converter.

$$\frac{d\hat{x}}{dt} = A\hat{x} + N\hat{x}\hat{d} + b\hat{d} \tag{3.24a}$$

$$\hat{y} = c\hat{x} \tag{3.24b}$$

where

$$A = DA_1 + D'A_2 \tag{3.25a}$$

$$N = A_1 - A_2 \tag{3.25b}$$

$$b = (A_1 - A_2)X + (b_1 - b_2)V_g \tag{3.25c}$$

Equations (3.24) represents a set of nonlinear state equations due to the presence of the $N\hat{x}\hat{d}$ product term. Note, however, that this term vanishes when $A_1 = A_2$, which is the case for the buck converter. More will be said about the distortionless amplification property of the buck converter in the next chapter.

3.5 Volterra Kernels for PWM Converters

Having obtained a nonlinear differential equation description of the converter, we now have a number of different approaches at our disposal which can be used to determine the Volterra kernels. A popular and perhaps the simplest method to apply for the problem at hand is the "growing exponential approach" [30], also known as the "harmonic input probing method" [28,29]. This approach determines symmetric kernels in the transform domain and is suitable only for time-invariant systems. The method may be briefly stated as follows [30].

Given the nonlinear system described by the general time-invariant state equations

$$\frac{dx(t)}{dt} = a(x(t),u(t)) \quad , \quad x(0) = 0 \tag{3.26a}$$

$$y(t) = cx(t) \quad , \quad t \geq 0 \tag{3.26b}$$

where $a(0,0) = 0$ and $a(x,u)$ is analytic in x and u, the first K symmetric transfer functions corresponding to (3.26) are computed as follows. First replace $a(x,u)$ by a power series in x and u. Then assume an input of the form

$$u(t) = e^{\lambda_1 t} + \ldots + e^{\lambda_K t} \tag{3.27}$$

and assume a solution of the form

$$x(t) = \sum_m G_{m_1,\ldots,m_K}(\lambda_1, \ldots, \lambda_K) e^{(m_1\lambda_1 + \ldots + m_K\lambda_K)t} \tag{3.28}$$

where the vector coefficients are undetermined. Substituting into the differential equation, solve for

$$G_{1,0,\ldots,0}(\lambda_1), \quad G_{1,1,0,\ldots,0}(\lambda_1, \lambda_2), \quad \ldots, \quad G_{1,\ldots,1}(\lambda_1, \ldots, \lambda_K)$$

by equating coefficients of like exponentials. Then since the output is a linear functional of x,

$$H_1(s) = cG_{1,0,\ldots,0}(s)$$

$$\overline{H}_1(s_1, s_2) = \frac{1}{2!} cG_{1,1,0,\ldots,0}(s_1, s_2)$$

.

$$\overline{H}_1(s_1, \ldots, s_K) = \frac{1}{K!} cG_{1,\ldots,1}(s_1, \ldots, s_K) \tag{3.29}$$

Therefore, to determine the first three kernels for the system described by (3.24) we assume an input of the form

$$\hat{d}(t) = e^{\lambda_1 t} + e^{\lambda_2 t} + e^{\lambda_3 t} \tag{3.30}$$

and dropping arguments for simplicity, a solution of the form

$$\begin{aligned} \hat{x}(t) = {} & G_{100}e^{\lambda_1 t} + G_{010}e^{\lambda_2 t} + G_{001}e^{\lambda_3 t} \\ & + G_{110}e^{(\lambda_1 + \lambda_2)t} + G_{011}e^{(\lambda_2 + \lambda_3)t} + G_{101}e^{(\lambda_1 + \lambda_3)t} \\ & + G_{111}e^{(\lambda_1 + \lambda_2 + \lambda_3)t} + \ldots \end{aligned} \tag{3.31}$$

The terms hidden in the ellipsis in (3.31) do not contribute to the terms of interest and can be dropped.

Substituting (3.31) into (3.24a) and equating the coefficients of $e^{\lambda_1 t}$, $e^{(\lambda_1 + \lambda_2)t}$ and $e^{(\lambda_1 + \lambda_2 + \lambda_3)t}$ and using (3.29) the symmetric kernels can be determined. The asymmetric form of these kernels is given below.

$$H_1(s) = c(sI - A)^{-1}b \tag{3.32a}$$

$$H_2(s_1, s_2) = c[(s_1 + s_2)I - A]^{-1}N(s_1 I - A)^{-1}b \tag{3.32b}$$

$$H_3(s_1, s_2, s_3) = c[(s_1 + s_2 + s_3)I - A]^{-1}N[(s_1 + s_2)I - A]^{-1}N(s_1 I - A)^{-1}b \tag{3.32c}$$

From (3.32) the pattern for higher-order kernels is clear.

Using (3.32) the distortion performance of an amplifier can be assessed. We are primarily interested in this thesis in harmonic distortion evaluation, however, it should be pointed out that the kernels given in (3.32) can also be directly used in evaluating intermodulation and cross-modulation distortion products in PWM conversion systems.

3.6 Summary

In this chapter, the nonlinear control-to-output response of PWM conversion systems has been approached via the Volterra functional series. A brief overview of the series has been presented. It was seen that the Volterra series is a power series with memory. Each term in the series represents a convolution integral. The nonlinear response of the system, for any input, can thus be determined from a knowledge of the multidimensional Volterra kernels or impulse responses. The general system response was determined for the particular case of a single tone excitation, and it was seen that the magnitude and phase of the dominant component of the *nth* harmonic in the system output is given by taking the magnitude (with an appropriate scaling factor) and phase of the Laplace transform of the *nth* order Volterra kernel; which was also referred to as the *nth* order nonlinear transfer function.

PWM conversion systems are nonlinear time-varying sampled-data systems. To simplify the analysis, approximations were made which led to a nonlinear time-invariant continuous-time model. The Volterra kernels were determined using this model. The "harmonic input probing method" was used to determine the kernels in the transform domain. These kernels completely characterize the system, and, as such, not only can

they be used to determine harmonic distortion but also other forms of distortion, such as, intermodulation and cross-modulation distortions resulting from multi-tone inputs.

Chapter 4: NONLINEAR MODELLING OF THE PWM SWITCH

4.1 Introduction

In this chapter a new modelling approach is described which can be used in the analysis of dc-to-dc converters, dc-to-ac inverters or amplifiers and input-current-shaping ac-to-dc converters. Like the modelling approach of state-space averaging [34,35], the concept of averaging is used. In contrast, however, to obtain a converter model the new modelling approach simply replaces the *PWM switch* (the nonlinear substructure of a converter cell which is common to almost all converter cells and therefore also converters) by its (average) model valid at the particular frequency of interest. Replacement of the PWM switch with its fundamental frequency model for the given dc operating point results in a small-signal model of the converter. Higher frequency models for the PWM switch replace the switch to obtain higher frequency

models of the converter under analysis; thus permitting a large-signal analysis which provides an assessment of the harmonic distortion performance of the system.

It is the purpose of this chapter to derive the various harmonic frequency models of the PWM switch and to also demonstrate their use and application.

In this chapter, the converter is assumed to operate with continuous inductor current conduction. For converter operation with discontinuous inductor current the PWM switch along with its associated inductor need to be considered in the modelling process. Thus, in this case, the basic three-terminal structure for which circuits models are derived is that of converter-cell A shown in Table 2.2. In Appendix A the steady-state and small-signal models of this cell are derived and used in an illustrative example in the analysis of a boost converter operating with discontinuous inductor current.

It is readily seen that the proposed converter analysis approach is analogous to ordinary transistor circuit analysis whereby the nonlinear device is replaced by its circuit model. This approach has the advantage in that a converter model is much more easily obtained by replacement of the switch with its model than by performing an analysis on the converter as a whole which then yields a converter model.

In the next section the concept of the PWM switch is introduced and a general approach to nonlinear analysis is given as a precursor to the analysis of the PWM switch presented in Section 4.3. Use and application of the PWM switch models are demonstrated in a few examples in Section 4.4.

4.2 Nonlinear Analysis

4.2.1 The PWM Switch

PWM converters are nonlinear systems due to their inherent switching operation. Switching is accomplished by an active/passive switch pair which form a single-pole double-throw (SPDT) switch. It is this SPDT switch in PWM converters which is referred to in this thesis as the *PWM switch.* Figure 4.1 shows the buck, boost, buck-boost and Cuk converters with the PWM switch identified. The three terminals of the switch have been numbered 1, 2 and 3. Terminals 1 and 2 have been arbitrarily designated as the terminals connected to the active and passive switches, respectively. Terminal 3 is the common connection between the switches. Figure 4.2a shows the PWM switch where the *average* terminal currents i_1 , i_2 and i_3 and *average* terminal voltages v_{12} , v_{13} and v_{23} are indicated. The *instantaneous* currents $\tilde{i}_1$, $\tilde{i}_2$ and $\tilde{i}_3$, along with their respective average values i_1 , i_2 and i_3 are shown in Fig. 4.2b.

The PWM switch represents the total nonlinearity present in PWM converters. This nonlinearity has been separated from the remaining linear components of the converter and it has been conveniently lumped into a single three-terminal structure which now can be treated on its own as a *three-terminal device* for which equivalent circuit models can be found. It is the purpose of this chapter to derive the large-signal model of the three-terminal device represented by the PWM switch decomposed into the various harmonic frequency models. A first-order approximation of this model results in the small-signal model which is simply the fundamental frequency model for a given dc operating point.

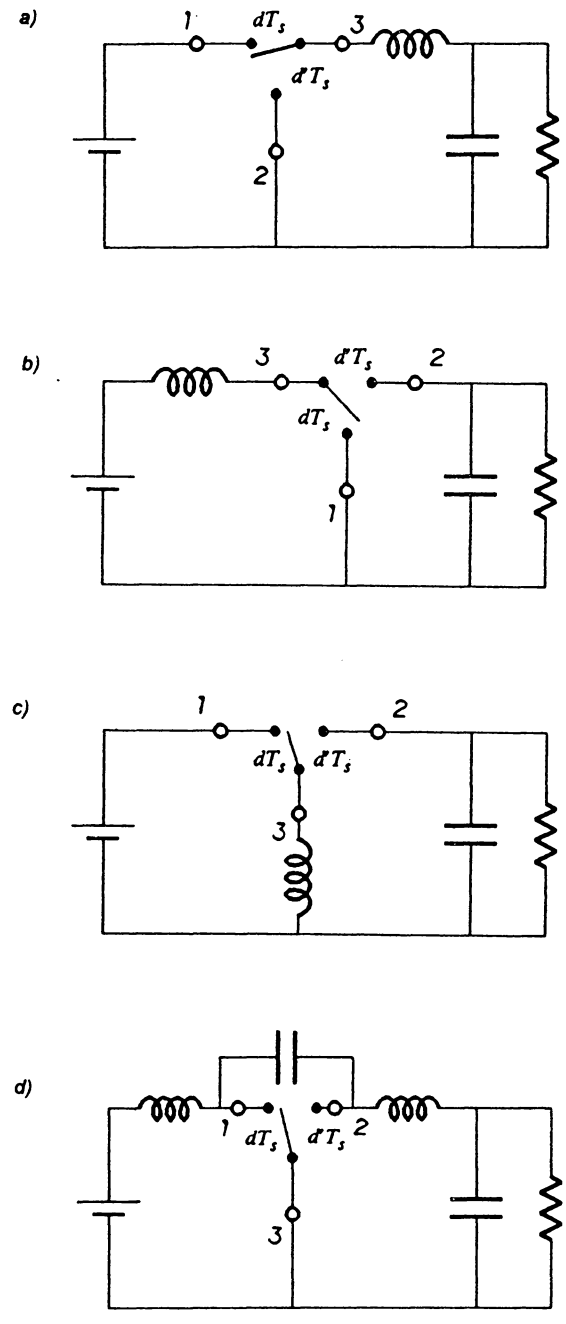


Fig. 4.1 *Typical PWM converters:*
(a) buck, (b) boost, (c) buck-boost, (d) Cuk.
The nonlinear three-terminal device, which contains all the switching elements, is termed the PWM switch.

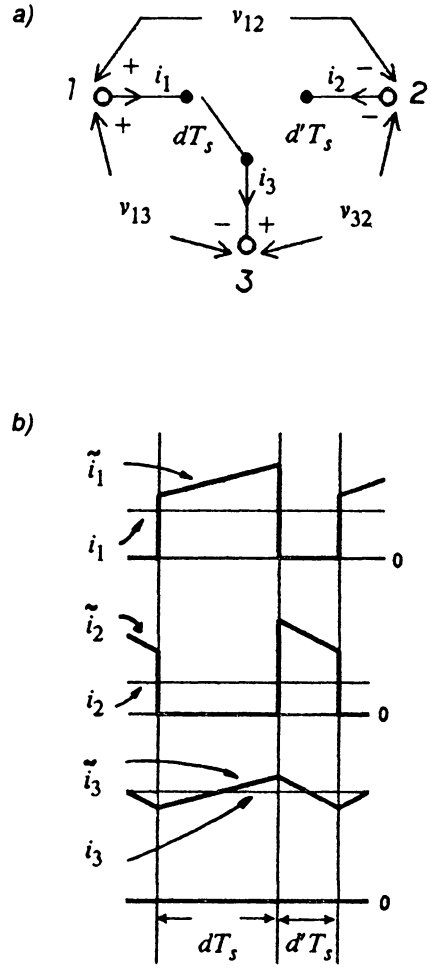


Fig. 4.2 *(a) The PWM switch showing designated terminal voltages and currents*
(b) Typical, instantaneous, terminal current waveforms, $\tilde{i}_1$, $\tilde{i}_2$ and $\tilde{i}_3$, and average terminal currents i_1, i_2 and i_3.

It should be pointed out that this separation of the nonlinear element from the linear part of the overall system is an approximation. The validity of this and other approximations performed in the ensuing analysis are established upon confirmation of the analytical predictions with simulation (or experimental) results.

4.2.2 General Theory

Before deriving the large-signal model of the PWM switch, it is useful to first look, in a general way, at the analysis of static nonlinearity as exemplified by the PWM switch, in contrast to the analysis of dynamic nonlinear systems treated in the previous chapter. This will aid in bringing out a few points which need to be made.

Consider the nonlinear system in Fig. 4.3a which is excited by a single input $x(t)$. The output $y(t)$ of this system is some nonlinear function of the input $y(t) = f[x(t)]$. For ease of discussion, the nonlinear response is assumed to be dependent on only a single variable which in this case is the input $x(t)$. Since a static nonlinear system does not possess memory, the value of the output at any instant of time is dependent on the value of the input only at that instant. A procedure to analyze such nonlinear systems involves decomposing the system into integer-order *subsystems*, the sum of whose outputs $y_n(t)$ gives the overall desired response of the system as shown in Fig. 4.3b. Thus,

$$y(t) = \sum_{n=0}^{\infty} y_n(t) \tag{4.1}$$

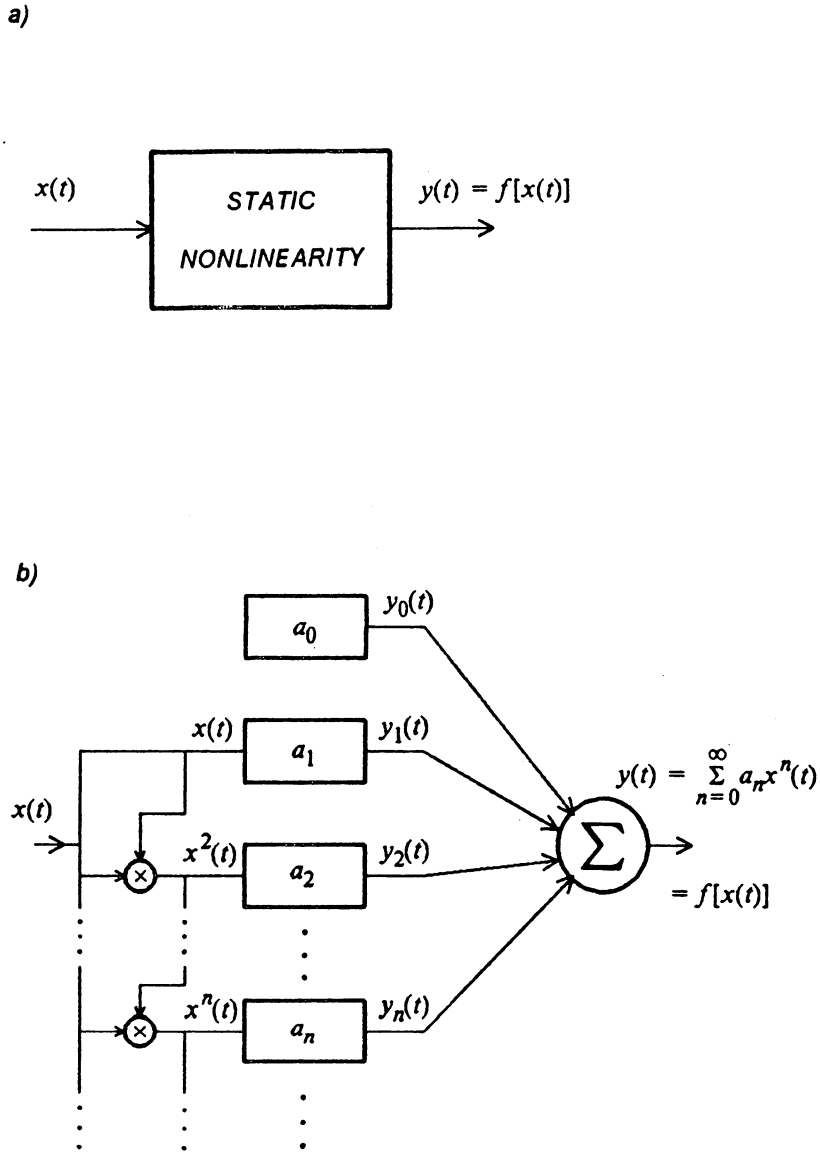


Fig. 4.3 *(a) General static nonlinear system, showing input/output relationship.*
(b) The nonlinear system partitioned into different integer-order subsystems.

These *subsystems* are of *nth* order in the sense that multiplication of the input by a constant A results in multiplication of the output by a constant A^n. Therefore, in this case,

$$y_n(t) \propto [x(t)]^n \quad ; \qquad n = 0,1,2,... \tag{4.2}$$

where we see that the output of the *nth* order subsystem is linearly related to the *nth* power of the input. Hence, the nonlinear system of Fig. 4.3a has been broken into an infinite number of coupled linear subsystems. The nonlinearity, of course, is now in the coupling between these linear subsystems. Clearly, if such an approach to the analysis of the nonlinear system is to be practical, the contribution of the higher order subsystems to the output must rapidly diminish, that is, the system must be "mildly" nonlinear.

Introducing the constant of proportionality in (4.2) we have

$$y_n(t) = a_n x^n(t) \quad ; \qquad n = 0,1,2,... \tag{4.3}$$

$$y(t) = \sum_{n=0}^{\infty} a_n x^n(t) \tag{4.4}$$

The nonlinear response of the system to an input $x(t)$ is given by

$$y(t) = f[x(t)] \tag{4.5}$$

A comparison of (4.4) and (4.5) suggests that (4.4) is the Taylor series expansion of the function $f(\cdot)$. For mildly nonlinear systems the number of terms required in (4.4), to accurately represent the system, is few.

Let us now briefly consider the case when the nonlinear system contains reactive elements so that its response is frequency dependent. In this case the outputs of the linear subsystems will not be simple scaled versions of their respective inputs as in (4.4), but will be convolution integrals, as pointed out in the previous chapter. Consequently, the resultant Taylor series will become the more general Volterra functional series in which treatment is considerably more difficult than the Taylor series. Hence, analyzing the PWM switch as opposed to the overall converter, as undertaken in the previous chapter, is a much less involved endeavor.

The following simple example will illustrate some of the points made so far. Let a static nonlinear system have a Taylor series expansion as in (4.4). If this system is excited with an input

$$x(t) = b \cos \omega t \quad ; \quad |b| < 1 \tag{4.6}$$

then the output will contain all the harmonics of the fundamental. The even harmonics will be generated from the even powers in (4.4) while the odd harmonics will be generated from the odd powers. By substituting (4.6) into (4.4) and using simple trigonometric relations it can be easily verified that the coefficients of the first three harmonics are given by

$$y(t) = B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t + B_3 \cos 3\omega t + \ldots \tag{4.7}$$

where

$$B_1 = a_1 b + \frac{3}{4} a_3 b^3 + \frac{5}{8} a_5 b^5 + \ldots \tag{4.8a}$$

$$B_2 = \frac{1}{2} a_2 b^2 + \frac{1}{2} a_4 b^4 + \ldots \tag{4.8b}$$

$$B_3 = \frac{1}{4} a_3 b^3 + \frac{5}{16} a_5 b^5 + \ldots \tag{4.8c}$$

From these equations the contributions of the different subsystems to the various harmonics via a_n are clear. In many practical situations the contributions of the higher order terms, which represent *beat products,* are negligible when $|b| < 1$. Hence, a solution of the form given by (4.4), (4.7) and (4.8) can be obtained whereby it is seen that the contribution of the higher order subsystems to the first few harmonics becomes rapidly negligible and that the higher harmonics themselves become rapidly smaller than the first few harmonics.

4.3 Analysis of the PWM Switch

The aim of the analysis presented in this section is to provide circuit models for the PWM switch which are valid at different harmonics of the excitation frequency. These models can be subsequently used in determining the small-signal as well as the large-signal response of converters to sinusoidal excitations in the duty ratio and in the input voltage. From Fig. 4.2a the average terminal voltages and currents are related by the following equations.

$$i_1 = d i_3 \tag{4.9}$$

$$v_{32} = d v_{12} \tag{4.10}$$

Note that (4.9) holds only if $\tilde{i}_3$ is continuous throughout the switching period as shown in Fig. 4.2b. A circuit model corresponding to (4.9) and (4.10) is shown in Fig. 4.4a.

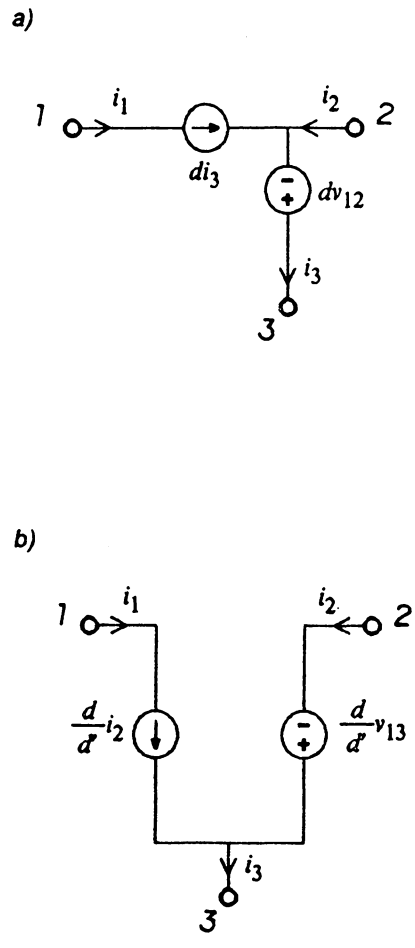


Fig. 4.4 *(a) A large-signal average model of the PWM switch.*
(b) An alternative large-signal average model of the PWM switch.

This model is simply an average circuit model of the PWM switch in which the average quantities are allowed to have slow time variations. This model is not unique since two other models can be obtained by considering two additional permutations of the orientation of the switch. Hence, if the current gain from terminal 1 to terminal 2 is considered, then

$$i_1 = \frac{d}{d'} i_2 \tag{4.11}$$

$$v_{32} = \frac{d}{d'} v_{13} \tag{4.12}$$

An average circuit model corresponding to (4.11) and (4.12) is given in Fig. 4.4b. Since the model of Fig. 4.4a is simpler to work with, we will continue the analysis using this model only. Perturbation of the duty ratio will result in perturbation of terminal currents and voltages so that

$$d = D + \hat{d} \tag{4.13a}$$

$$i_3 = I_3 + \hat{i}_3 \tag{4.13b}$$

$$v_{12} = V_{12} + \hat{v}_{12} \tag{4.13c}$$

where capitalized quantities represent steady-state values and perturbed quantities or contributions from these perturbed quantities are indicated with a caret. Expanding (4.9) and (4.10) in a two-dimensional Taylor series around their dc operating point, D, I_3, V_{12}, results in

$$i_1 = DI_3 + I_3\hat{d} + D\hat{i}_3 + \hat{i}_3\hat{d} \tag{4.14}$$

$$v_{32} = DV_{12} + V_{12}\hat{d} + D\hat{v}_{12} + \hat{v}_{12}\hat{d} \tag{4.15}$$

For sinusoidal modulation of the duty ratio we have

$$\hat{d}(t) = d^{(1)} \cos \omega t \quad ; \quad |d^{(1)}| < 1 \tag{4.16}$$

The terms $\hat{i}_3$ and $\hat{v}_{12}$ in (4.13) can each be represented in a Fourier cosine series as follows.

$$\hat{i}_3(t) = \sum_{n=0}^{\infty} i_3^{(n)} \cos(n\omega t + \varphi_n) \tag{4.17}$$

$$\hat{v}_{12}(t) = \sum_{n=0}^{\infty} v_{12}^{(n)} \cos(n\omega t + \theta_n) \tag{4.18}$$

Substitution of (4.16) and (4.17) into (4.14) gives

$$\begin{aligned} i_1(t) = DI_3 + I_3 d^{(1)} \cos \omega t + D \sum_{n=0}^{\infty} i_3^{(n)} \cos(n\omega t + \varphi_n) \\ + d^{(1)} \cos \omega t \sum_{n=0}^{\infty} i_3^{(n)} \cos(n\omega t + \varphi_n) \end{aligned} \tag{4.19}$$

Using the trigonometric identity

$$\cos a \cos b = 1/2[\cos(a - b) + \cos(a + b)]$$

the terms in (4.19) are grouped in order of increasing harmonics, $i_1^{(k)}$, k = 0,1,2,..., so that $i_1(t)$ now has the following form.

$$i_1 = i_1^{(0)} + i_1^{(1)} + i_1^{(2)} + ... + i_1^{(n)} + ... \tag{4.20}$$

where

$$i_1^{(0)} = DI_3 + Di_3^{(0)} + \frac{d^{(1)} i_3^{(1)}}{2} \cos \varphi_1 \tag{4.21a}$$

$$\begin{aligned} i_1^{(1)} &= I_3 d^{(1)} \cos \omega t + Di_3^{(1)} \cos(\omega t + \varphi_1) \\ &\quad + i_3^{(0)} d^{(1)} \cos \omega t + \frac{d^{(1)} i_3^{(2)}}{2} \cos(\omega t + \varphi_2) \end{aligned} \tag{4.21b}$$

$$\begin{aligned} i_1^{(n)} &= \frac{d^{(1)} i_3^{(n-1)}}{2} \cos(n\omega t + \varphi_{n-1}) \\ &\quad + Di_3^{(n)} \cos(n\omega t + \varphi_n) \\ &\quad + \frac{d^{(1)} i_3^{(n+1)}}{2} \cos(n\omega t + \varphi_{n+1}) \quad ; n = 2,3,... \end{aligned} \tag{4.21c}$$

Equations (4.21a-c) can be simplified by realizing that the last term in each of these equations represents contributions to that harmonic from higher frequencies beating down. These beat products are generally negligible, as are the terms containing $i_3^{(0)}$ in (21a-b), compared to the dominant terms in the expressions. Neglecting these terms, (4.21a-c) reduce to

$$i_1^{(0)} = DI_3 = I_1 \tag{4.22a}$$

$$i_1^{(1)} = I_3 d^{(1)} \cos \omega t + Di_3^{(1)} \cos(\omega t + \varphi_1) \tag{4.22b}$$

$$\begin{aligned} i_1^{(n)} &= Di_3^{(n)} \cos(n\omega t + \varphi_n) \\ &\quad + \frac{d^{(1)} i_3^{(n-1)}}{2} \cos(n\omega t + \varphi_{n-1}) \quad ; n = 2,3,... \end{aligned} \tag{4.22c}$$

A similar procedure for v_{32} in (4.15) using (4.16) and (4.18) gives

$$v_{32}^{(0)} = DV_{12} = V_{32} \tag{4.23a}$$

$$v_{32}^{(1)} = V_{12} d^{(1)} \cos \omega t + Dv_{12}^{(1)} \cos(\omega t + \theta_1) \tag{4.23b}$$

$$v_{32}^{(n)} = Dv_{12}^{(n)} \cos(n\omega t + \theta_n) + \frac{d^{(1)} v_{12}^{(n-1)}}{2} \cos(n\omega t + \theta_{n-1}) \quad ; n = 2,3,... \tag{4.23c}$$

Thus the model of Fig. 4.4a is decomposed into linear circuit models corresponding to each harmonic frequency as derived from (4.22) and (4.23). These harmonic-frequency circuit models are shown in Fig. 4.5 for the dc, fundamental and the *nth* harmonic, (n = 2,3...). The magnitude and phase of a particular harmonic in a dc-to-ac inverter or amplifier, for example, can be determined simply by substituting these circuit models point-by-point for the PWM switch and analyzing the resultant linear circuits. The process begins by substituting the dc model and then solving for the dc operating point. These dc quantities are then used as an input to the fundamental frequency model which is next substituted point-by-point for the PWM switch. This circuit is then solved yielding values which are used as input to the next higher harmonic frequency model. At each stage only *linear* circuits are solved resulting in generator values which are used in the subsequent stage.

4.4 Applications of the PWM Switch Models

To illustrate the use of the PWM switch model, three examples are given in this section. The first example illustrates that a first-order approximation of the nonlinear analysis of the PWM switch results in the small-signal analysis. Thus, in the first example use of only the dc and the fundamental frequency models are made to perform the small-signal analysis of a dc-to-dc boost converter whereby the control-to-output

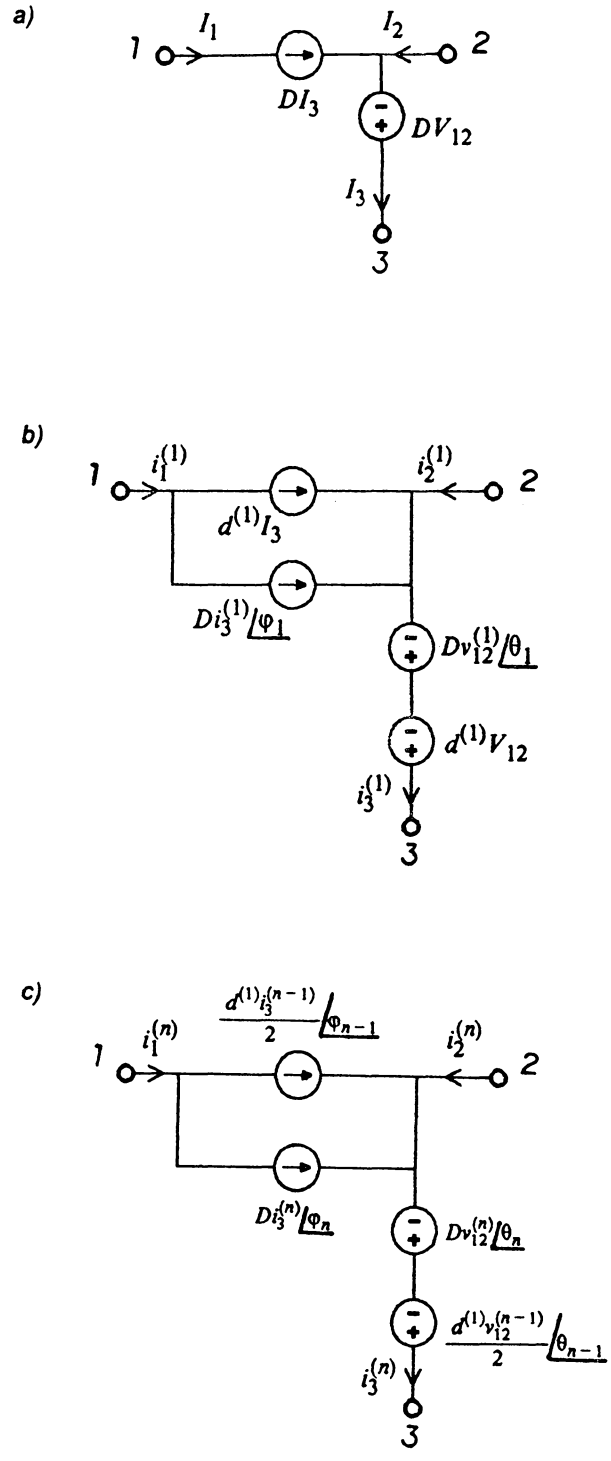


Fig. 4.5 *(a) DC model,*
(b) fundamental frequency model,
(c) nth harmonic ($n = 2, 3, \ldots$) frequency model of the PWM switch.

transfer function is determined. In the second example the boost converter is used as a dc-to-ac inverter or amplifier which requires large-signal duty-ratio modulation. In this case the large-signal PWM switch models are used to predict the magnitude and phase of the various frequency components in the output spectrum. In the third and final example we examine the distortionless amplification property of the buck converter.

4.4.1 Example 1: DC and Small-Signal Modelling of a dc-to-dc Boost Converter

In this example the dc and small-signal performance of the boost converter in Fig. 4.6 is determined by the use of the PWM switch models obtained in the previous section. After determination of the dc operating point the control-to-output transfer function is determined.

Substitution of the dc model of the PWM switch shown in Fig. 4.5a into the boost converter circuit of Fig. 4.6 results in the circuit of Fig. 4.7a where all the reactive elements have been shorted or opened as required at zero frequency. Inspection of this circuit shows that

$$V_{12} = -V \tag{4.24a}$$

$$I_3 = -I \tag{4.24b}$$

Solving the circuit we find the dc conversion ratio

$$V = \frac{D'R}{r_L + D'^2 R} V_g \tag{4.25a}$$

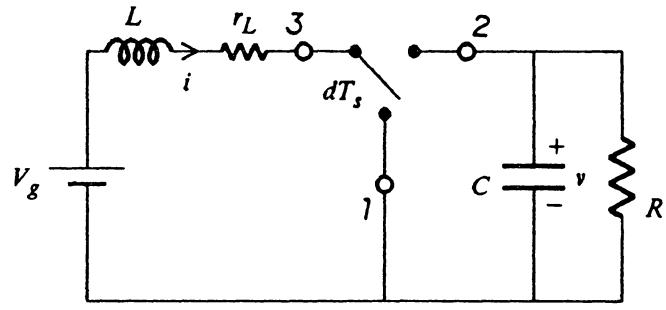


Fig. 4.6 *Boost converter showing the three-terminal PWM switch with inductor ESR included.*

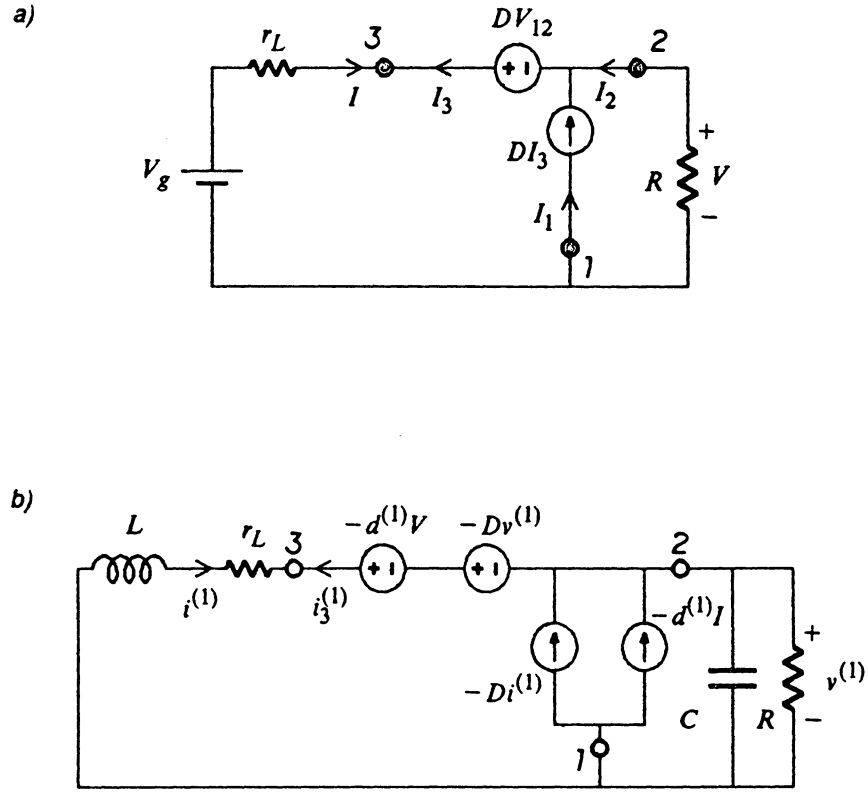


Fig. 4.7 *(a) DC model,*
(b) fundamental frequency model
of the boost converter of Fig. 4.6.

and

$$I = \frac{1}{r_L + D'^2 R} V_g \tag{4.25b}$$

The dc operating point found in (4.25) is used as input for the fundamental frequency model of Fig. 4.7b which has been arrived at by substitution of the fundamental frequency model of the PWM switch into the boost converter of Fig. 4.6. Since we are only considering perturbations in the duty ratio, the dc input voltage has no contribution to the control-to-output transfer function and, hence, is shorted as shown in Fig. 4.7b. Solution of the circuit of Fig. 4.7b may be approached by writing state equations.

$$\frac{d}{dt}\begin{bmatrix} i^{(1)} \\ v^{(1)} \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L} & -\frac{D'}{L} \\ \frac{D'}{C} & -\frac{1}{RC} \end{bmatrix}\begin{bmatrix} i^{(1)} \\ v^{(1)} \end{bmatrix} + \begin{bmatrix} \frac{V}{L} \\ -\frac{I}{C} \end{bmatrix} d^{(1)} \tag{4.26}$$

The control-to-output transfer function is now determined simply by taking the Laplace transform of (4.26) and inverting. The result, after making use of (4.25), is

$$\frac{v^{(1)}(s)}{d^{(1)}(s)} = G_{od} \frac{(1 + s/s_z)}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}} \tag{4.27}$$

where

$$G_{od} = \frac{(D'^2 R - r_L)R}{D'^2 R + r_L} V_g \tag{4.28a}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \sqrt{D'^2 + \frac{r_L}{R}} \tag{4.28b}$$

$$Q = \frac{D'^2R + r_L}{\omega_0(L + CRr_L)} \tag{4.28c}$$

$$s_z = -\frac{D'^2R - r_L}{L} \tag{4.28d}$$

These results agree with those of state-space averaging given in [35]. Further comparison with the results of state-space analysis are given in [33] where it is shown that if the esr of the capacitor, C, is included, *slight* discrepancies between the results of the two methods arise. These discrepancies are attributed to the approximation involved in separating the nonlinear part from the linear part of the circuit, which the method of state-space averaging does not perform.

4.4.2 Example 2: Large-Signal Modelling of a dc-to-ac Boost Amplifier

Let us now use the boost converter of Fig. 4.6 as an amplifier. This is done by translating input signal perturbations into duty-ratio modulations which can result in large-signal voltage excursions at the converter output. To assess the purity of the output waveform of this amplifier the harmonic content in the output is determined by using the derived PWM switch models.

The response of the amplifier at the fundamental frequency has already been obtained in the previous example. We need now obtain the response at the *nth* harmonic ($n = 2, 3,...$) frequencies. This is done by substituting the *nth* harmonic frequency model of the PWM switch given in Fig. 4.5c into the circuit of the boost converter as shown in Fig. 4.8. The state equations for this circuit are given by

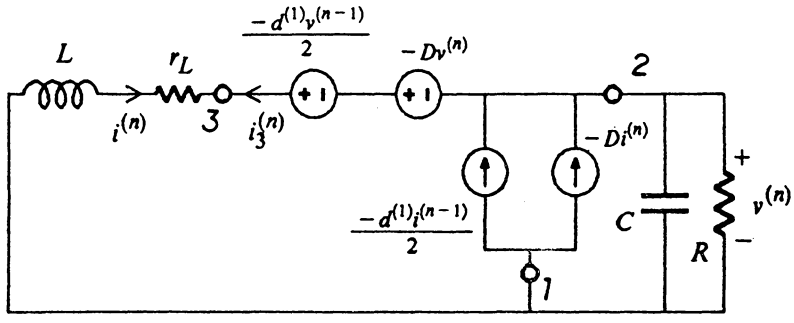


Fig. 4.8 *The nth harmonic ($n = 2, 3, \ldots$) frequency model of the boost converter of Fig. 4.6.*

$$\frac{d}{dt}\begin{bmatrix} i^{(n)} \\ v^{(n)} \end{bmatrix} = \begin{bmatrix} -\frac{r_L}{L} & -\frac{D'}{L} \\ \frac{D'}{C} & -\frac{1}{RC} \end{bmatrix}\begin{bmatrix} i^{(n)} \\ v^{(n)} \end{bmatrix} + \begin{bmatrix} \frac{v^{(n-1)}}{L} \\ \frac{-i^{(n-1)}}{C} \end{bmatrix}\frac{d^{(1)}}{2} \quad ; n = 2,3,... \tag{4.29}$$

Equation (4.29) may be solved as before. Note, however, that in order to compute the *nth* harmonic we must compute all lower harmonics since the input vector in (4.29) for the *nth* harmonic is dependent on the $(n-1)th$ harmonic.

Adopting the following component values (taken from [36]):

$$\begin{gathered} L = 530\mu H \ ; \ C = 10\mu F \ ; \ r_L = 2.4\Omega \ ; \\ R = 64\Omega \ ; \ V_g = 16V \end{gathered} \tag{4.30}$$

we compute

$$\omega_0 = 2\pi(1172)\text{rad/s} \quad ; \quad Q = 1.21 \tag{4.31}$$

The large-signal modulation in the duty ratio was chosen as

$$d(t) = 0.5 + 0.15\cos[2\pi(575)t] \tag{4.32}$$

For illustrative purposes the excitation frequency was chosen to be around 575Hz because the distortion of the converter was seen to be worst at this frequency. A simple explanation for this behavior of the distortion can be easily given by noting that the second harmonic gets amplified by the Q of the second-order circuit corresponding to the fundamental when the frequency of the second harmonic becomes coincident with $\omega_0 = 2\pi(1172)$rad/s of this circuit. Hence, for excitation frequencies around 550 to 600Hz the observed distortion is worst. The output waveform of the amplifier for an excitation

frequency of 575Hz is shown in Fig. 4.9. This waveform was produced using the COSMIR [37] computer simulation program. Shown in Table 4.1 are the magnitudes and phases of the fundamental and the first few harmonics obtained by the application of an FFT to the output waveform and also the corresponding results obtained by prediction using the analysis procedure given above. The FFT results match those of the prediction reasonably well. Beginning at about the fifth harmonic the level of the FFT output becomes immersed in the "noise" of the spectral leakage of the switching ripple produced by the FFT. Therefore, results at frequencies higher than the fifth harmonic are not included in Table 4.1.

Shown in Fig. 4.10 is the simulated output waveform for an excitation frequency of 300Hz. The predicted and FFT results at this frequency are given in Table 4.2 where we see again that the agreement is good.

4.4.3 Example 3: Distortionless Amplification - The Buck Amplifier

In this last example we see how the buck converter of Fig. 4.1a can be used as a distortionless amplifier even though it contains the PWM switch which is considered a nonlinear device.

Substitution of the dc, fundamental frequency and *nth* harmonic ($n = 2, 3, \ldots$) frequency models of the PWM switch into Fig. 4.1a results in the converter models of Fig. 4.11 where, as before, the reactive components are either shorted or opened in the dc model and the input source is shorted in the remaining models. Also, now a nondissipative impedance, Z_s, has been included in the converter models of Fig. 4.11. This impedance might represent the Thevenin impedance of an input filter, for example.

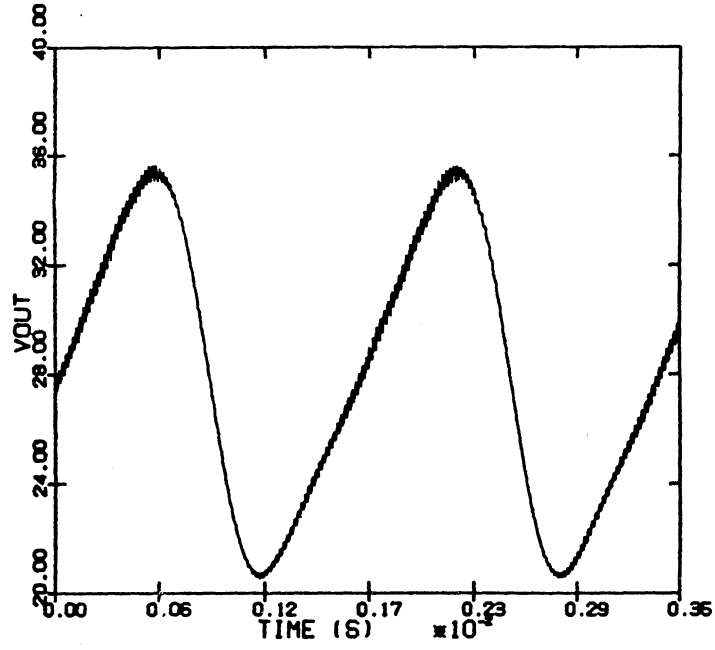


Fig. 4.9 *Simulated output waveform for an excitation frequency of 575Hz.*

Table 4.1 *Harmonic output of the boost amplifier of Fig. 4.6 for an excitation frequency of 575Hz. Maximum distortion occured at this frequency.*

FREQUENCY	PREDICTED			FFT		
	MAGNITUDE		PHASE (deg.)	MAGNITUDE		PHASE (deg.)
	V pk.	dB rel. to fund.	rel. to fund. at output	V pk.	dB rel. to fund.	rel. to fund. at output
FUNDAMENTAL	7.24	0	0	6.65	0	0
2ND HARMONIC	1.97	-11.3	-84	1.79	-11.4	-82
3RD HARMONIC	0.436	-24.4	-189	0.400	-24.4	-183
4TH HARMONIC	0.0526	-42.8	-310	0.0476	-42.9	-293
5TH HARMONIC	0.00469	-63.8	-439	0.00885	-57.5	-466

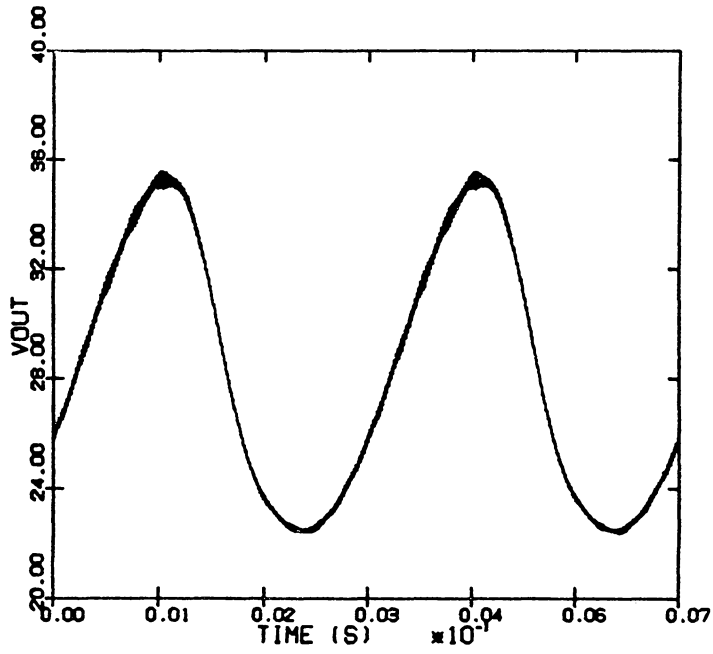


Fig. 4.10 *Simulated output waveform for an excitation frequency of 300Hz.*

Table 4.2 *Harmonic output of the boost amplifier of Fig. 4.6 for an excitation frequency of 300Hz.*

FREQUENCY	PREDICTED			FFT		
	MAGNITUDE		PHASE (deg.)	MAGNITUDE		PHASE (deg.)
	V pk.	dB rel. to fund.	rel. to fund. at output	V pk.	dB rel. to fund.	rel. to fund. at output
FUNDAMENTAL	6.46	0	0	6.35	0	0
2ND HARMONIC	0.995	-16.3	-44	0.934	-16.7	-49
3RD HARMONIC	0.351	-25.3	-110	0.317	-26.0	-113
4TH HARMONIC	0.121	-34.6	-195	0.101	-36.0	-192
5TH HARMONIC	0.0303	-46.6	-309	0.0283	-47.0	-294

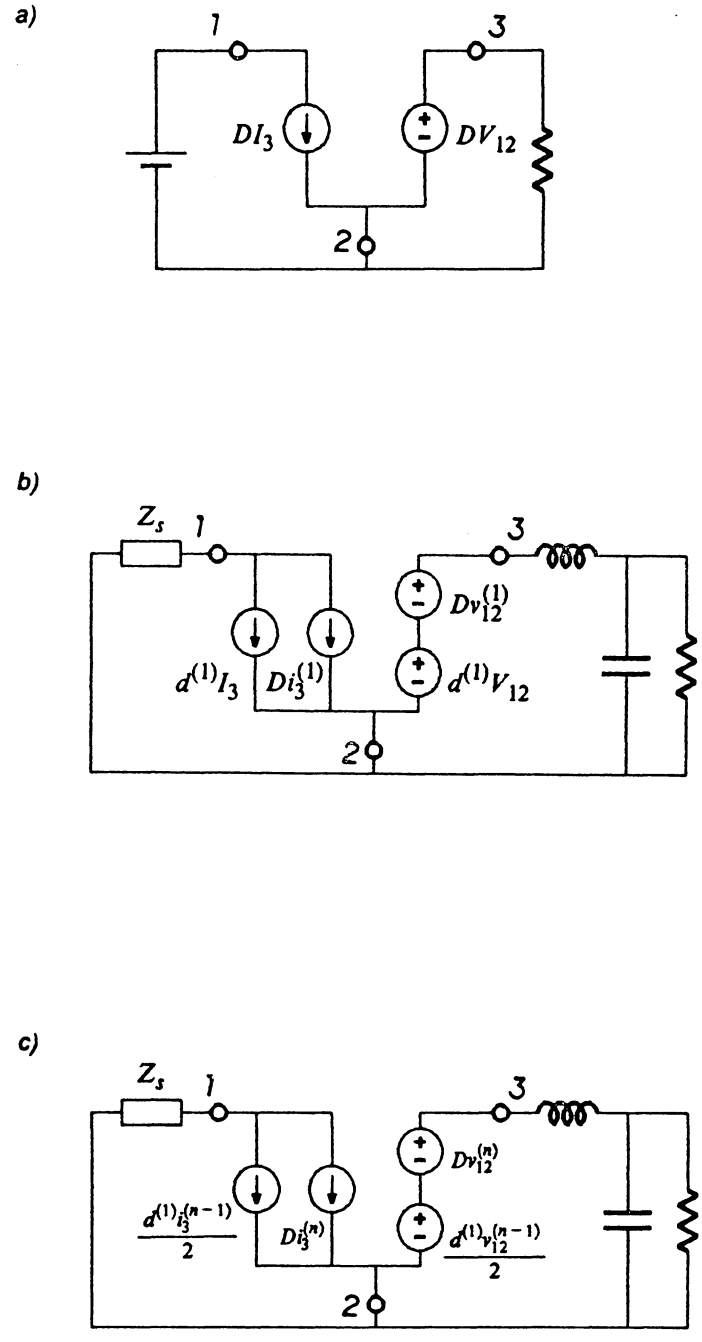


Fig. 4.11 *(a) DC model,*
(b) fundamental frequency model,
(c) nth harmonic ($n = 2, 3, \ldots$) frequency model of a buck converter with nondissipative source impedance, Z_s, included.

Solving the dc model results in values used in the fundamental frequency model. Inspection of the fundamental frequency model reveals that condition $Z_s = 0$ results in $v_2^{(1)} = 0$ and, consequently, only one of the two voltage sources in the output circuit contributes to the output signal. For the *nth* harmonic frequency model we see that if $Z_s = 0$ then we also have, $v_2^{(n)} = 0$, $(n = 2, 3, \ldots)$. Thus, there is no harmonic content in the output signal; consequently, the fundamental is amplified in a distortionless fashion. However, with the condition $Z_s \neq 0$ we can similarly surmise from the models of Fig. 4.11 that interaction between the input and output circuits will occur producing distortion. Therefore it is of great importance in the design of buck amplifiers to minimize Z_s in relation to other circuit impedances in order to minimize distortion. This problem has been tackled elegantly by Erickson [36].

4.5 Summary

The active/passive switch pair(s) in PWM converters represent the total nonlinearity in these converters. This switch pair can usually be combined into a three-terminal structure which excludes all linear elements of the converter. This structure has been termed the *PWM switch.*

An approach to modelling of PWM converters for both small and large signals has been given whereby the nonlinearity in these converters, the PWM switch, is treated directly, resulting in a simpler method of converter analysis. Equivalent circuit models of the PWM switch, now treated as a three-terminal device, are derived which are valid at different harmonics of the excitation frequency. These models are substituted for the

PWM switch in the converter being analyzed, be it a dc-to-dc converter, dc-to-ac inverter or amplifier or an input-current-shaping ac-to-dc converter. Solving the dc and fundamental frequency models results in a small-signal analysis. Continuing the analysis for the second and higher harmonics allows one to construct the nonlinear response of the converter. At each stage of the analysis only *linear* circuits are solved.

This approach to converter analysis is analogous to ordinary transistor circuit analysis. A number of examples have been given illustrating the approach.

Chapter 5 : DC-TO-AC INVERSION USING QUASI-RESONANT TECHNIQUES

5.1 Introduction

The zero-current and zero-voltage quasi-resonant switching techniques [19,20,21] were proposed as a solution to achieving a significant reduction in the size and weight of power conversion circuits. By employing the concept of the resonant switch a significant increase in switching frequency can be achieved without incurring a large switching loss. Increase in the magnitude of switching frequency also has the added benefit of producing a fast transient response.

The quasi-resonant techniques, until now, have been applied almost exclusively in the area of dc-to-dc conversion. Use of these techniques, at the present time, is limited to power levels of up to several hundred watts. In this range, a number of applications

exist for dc-to-ac amplifiers/inverters, where use of quasi-resonant techniques would bring the added benefits stated above.

In the range of 25VA to 100VA, inverters are used as telephone ringing-tone generators [38,39]. Use of inverters that feature high-frequency waveshaping techniques are also becoming popular in uninterruptible power supply (UPS) systems for computers [40,41], where use at power levels of 100VA to 3000VA have been reported [41]. Paralleling of several modules [42] to obtain greater output power or a level of redundancy for increased reliability is also becoming popular. For power levels above 1kVA, inverters are used in photovoltaic/utility interfaces [43,44]. However, perhaps the most demanding of applications, throughout the full range of power levels, might be in applications of audio, switching, power amplifiers which require a high level of purity in the output signal and the ability to reproduce an almost arbitrary waveshape at various signal levels.

These are just some of the many applications which could benefit with the use of quasi-resonant techniques, in particular, the zero-current switching technique. The large voltage stress of the zero-voltage quasi-resonant technique would limit its application in this area. Fortunately, the switch current stress in the zero-current technique presents less of a problem.

An important issue regarding inverters is how they handle reactive loads. The degree to which inverters need to supply reactive power varies from not at all or very little, as exemplified by utility-interactive interfaces [43] and low power computer peripheral UPSs [41], to the other extreme of supplying all power requirements of a load with a poor power factor, as exemplified by some stand-alone photovoltaic inverter/load combinations.

In Section 5.4 a number of different quasi-resonant amplifier/inverter topologies are presented. In the subsequent section various schemes are described which allow these inverters to handle reactive loads. But first, a review of basics and some of the problems encountered are given in Sections 5.2 and 5.3.

5.2 Amplifier/Inverter Basics

A schematic representation of an amplifier/inverter system is shown in Fig. 5.1. The purpose of such a system is to drive a load reproducing, at a higher power level, a frequency band-limited reference signal. Without loss of generality, the reference input is considered to be a sine wave, thus, ideally, a sine-wave output voltage is developed across the load. The load may be purely resistive, reactive, or even nonlinear. The ensuing discussion, however, will specifically focus on linear loads and, in particular, on resistive or series resistive-inductive (RL) loads.

The type of load imposes on the inverter different operating conditions dependent on the load power factor. This can be seen clearly in Fig. 5.2 which shows the voltage-current (v-i) waveforms for a resistive load (Fig. 5.2a) and also an RL load (Fig. 5.2b). One can divide the output v-i plane into four quadrants depending on the polarity of the output voltage and current, as shown in Fig. 5.3. Thus, from Fig. 5.2, we see that an inverter driving a resistive load need only operate in two quadrants, namely, quadrants I and III. However, for a reactive load, such as an RL load, four-quadrant operation is required. This complicates the design of the inverter. In particular, the number of switches required increases significantly. As seen in Fig. 5.2b, for part of the

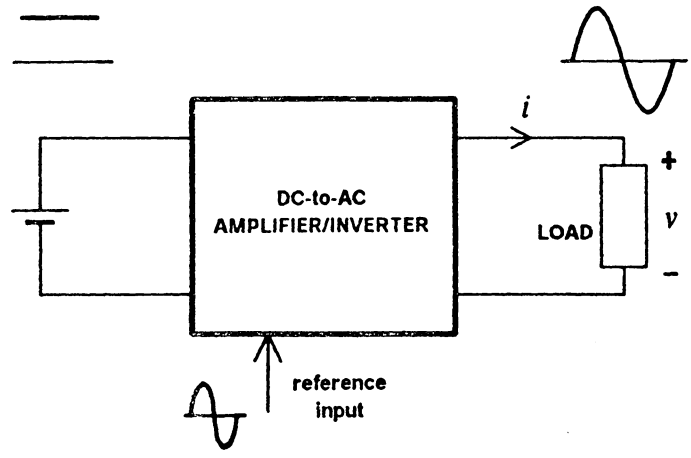


Fig. 5.1 *Schematic representation of a dc-to-ac amplifier/inverter system*

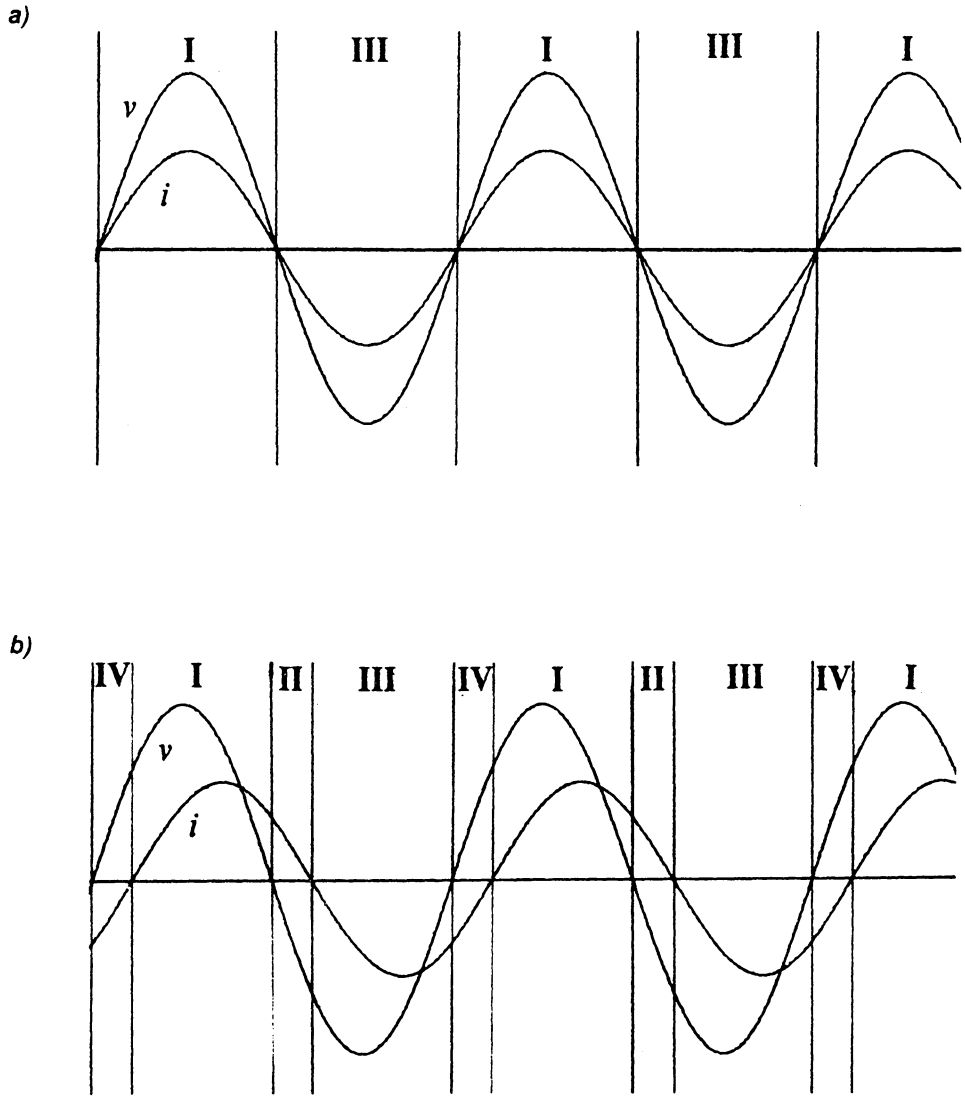


Fig. 5.2 *Load voltage (v) and current (i) waveforms indicating inverter quadrant operation*
(a) Resistive load
(b) Resistive-inductive load

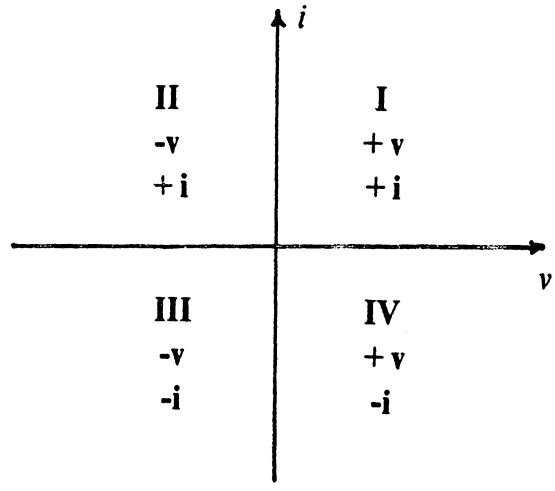


Fig. 5.3 *Inverter quadrant operation in the output v-i plane*

cycle (i.e. during operation in quadrants II and IV) power is returned to the inverter from a reactive load. Ideally, the inverter then returns this power to the source. Let us now review how bidirectional power flow may be achieved in PWM converters. Figure 5.4a shows a basic bidirectional buck converter which permits operation in quadrants I and IV. Figures 5.4b and 5.4c show which switches are used for the different directions of power flow. In the forward power direction (Fig. 5.4b), the converter looks like a one-quadrant buck converter. However, in the reverse power direction (Fig. 5.4c) the active switch position in the converter changes and it takes on the appearance of a boost converter. Note that the change of topology, due to change of current (power) flow, is done automatically using this bidirectional switch implementation.

An attempt to achieve bidirectional power flow for a buck zero-current-switched quasi-resonant converter (ZCS-QRC) [19,20] by augmentation of switches by a parallel transistor and diode, as shown in Fig. 5.5a, is not too successful. As we can see from the topologies during forward power flow (Fig. 5.5b) and reverse power flow (Fig. 5.5c), the basic mode of operation changes. During forward power flow, the topology looks like a full-wave, buck ZCS converter. However, during reverse power flow, instead of looking like a full-wave boost ZCS converter, it looks like a half-wave, boost zero-voltage switched (ZVS) converter [21]. This occurs as the positions of the resonant components have remained invariant in the topology. Thus, these components need to switch positions when the topology changes. Note also that topology changes are not automatic and they must occur by sensing power flow.

Figure 5.6a shows a bidirectional buck ZCS-QRC. Two complete resonant switches are used in this converter. During forward power flow (Fig. 5.6b), the resonant switch comprising {Q1, D1, D3, L1, C1} is used with the other switch inoperative. During

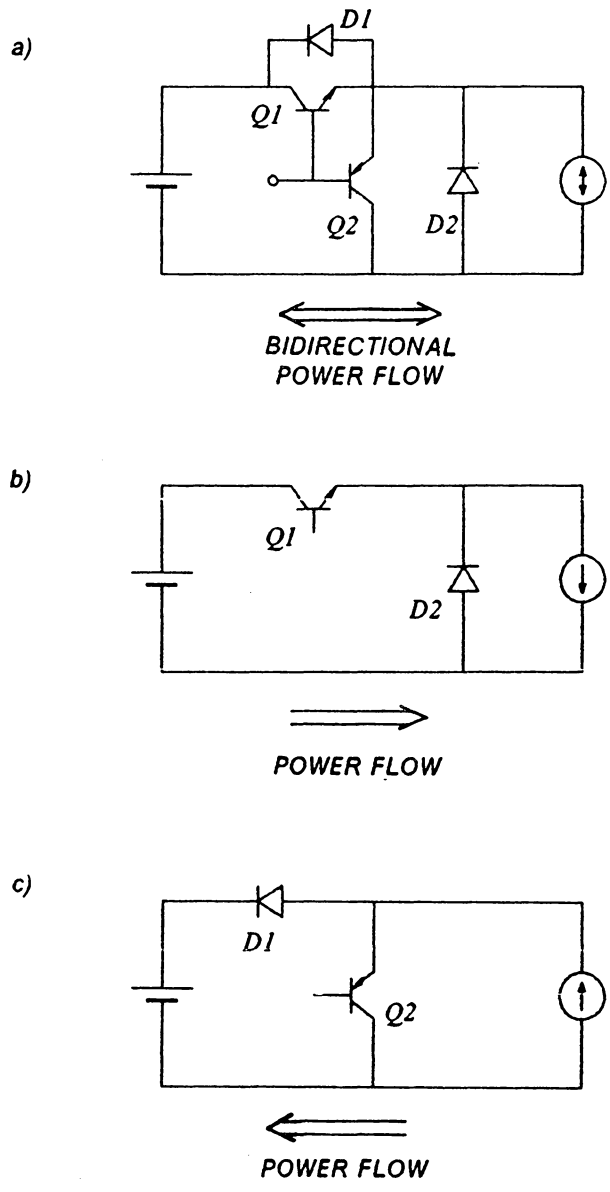


Fig. 5.4 *(a) Basic bidirectional PWM buck converter*
(b) Active topology during forward power flow: buck converter
(c) Active topology during reverse power flow: boost converter

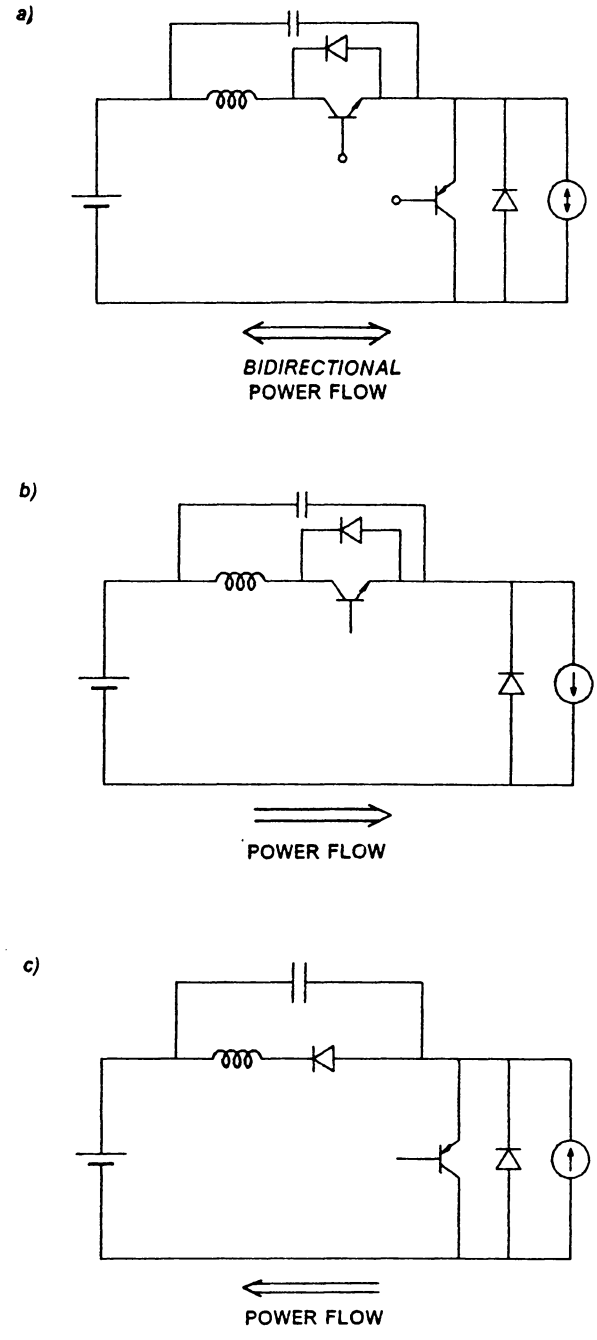


Fig. 5.5 *(a) An initial attempt to implement a bidirectional ZCS buck coverter*
(b) Active topology during forward power flow: buck ZCS (full-wave) converter
(c) Active topology during reverse power flow: boost ZVS (half-wave) converter

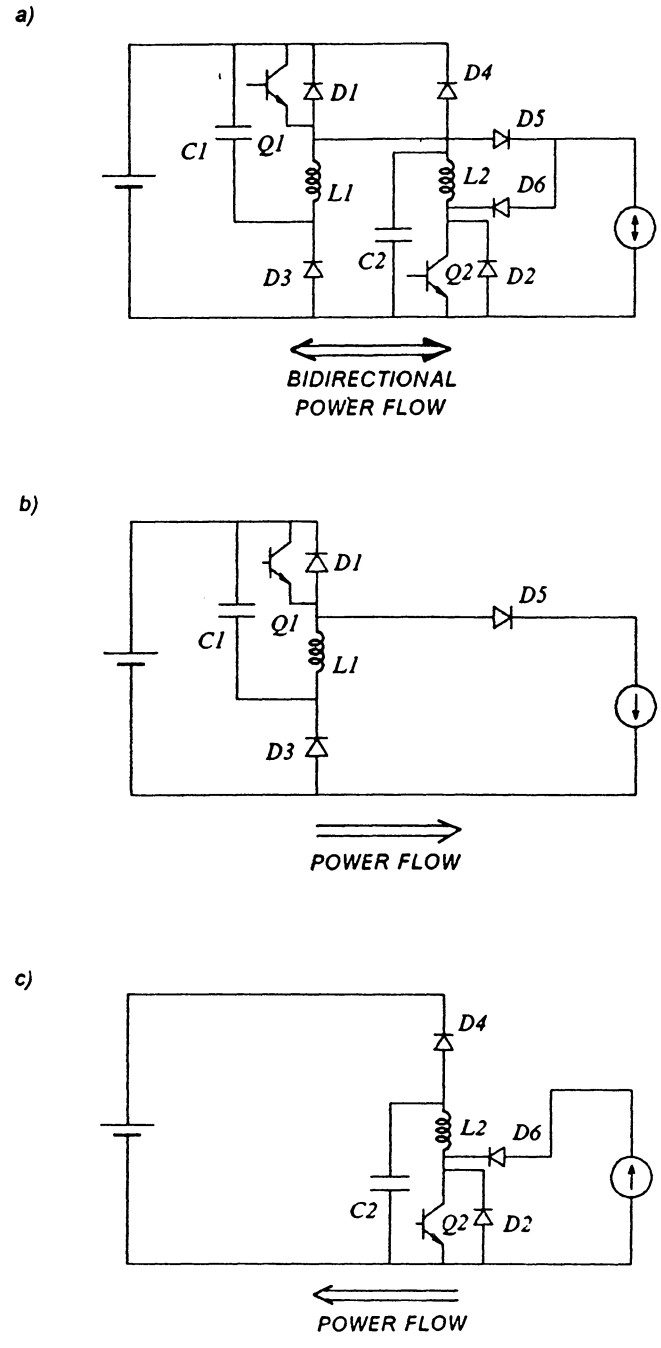


Fig. 5.6 *(a) A bidirectional buck ZCS converter*
(b) Active topology during forward power flow: buck ZCS (full-wave) converter
(c) Active topology during reverse power flow: boost ZCS (full-wave) converter

reverse power flow the reverse situation is true. The resonant frequencies of the switches should be made the same by making $L1 = L2$ and $C1 = C2$. The active resonant switch is selected by sensing the direction of power flow. Note also that the drive signals to the two resonant switches are not the same. If the switching frequency of drive during forward power flow is f_s, then the drive frequency of the other switch at the instant of changeover to reverse power flow should be $f_o - f_s$ (where f_o denotes the resonant frequency) so the output voltage does not change.

The converter of Fig. 5.6a uses two square-wave resonant switches [45]. Diodes D5 and D6 prevent interaction of the these switches. Sine-wave resonant switches [45] seem to be unsuited as interaction between the switches cannot be prevented.

5.3 Basic Approaches to Achieving dc-to-ac Inversion

5.3.1 Differential Load Excitation

Let us consider two basic approaches to achieving dc-to-ac inversion. Figure 5.7 shows one basic scheme which has been termed the Differential Load Excitation (DLE) scheme. In this figure the voltage sources represent control-variable modulated dc-to-dc converters. These converters produce a dc-biased sine wave output, such that each source only produces a unipolar voltage. The modulations of each source are 180° out of phase with the other, so as to maximize the voltage excursion across the load. The load is connected differentially across the sources. Thus, whereas a dc bias appears at

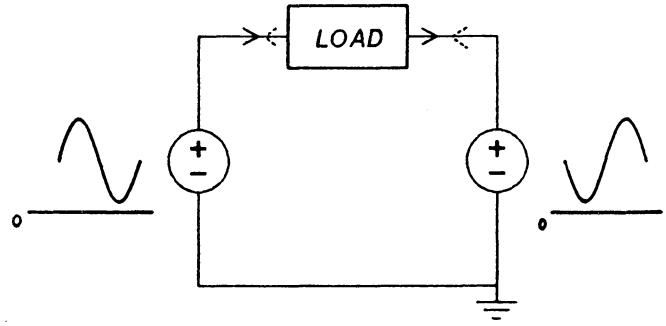


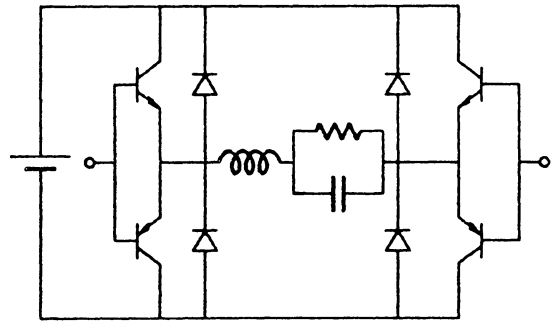
Fig. 5.7 *One basic approach to achieving dc-to-ac inversion: Differential Load Excitation (DLE) scheme*

each end of the load with respect to ground, the differential dc voltage across the load is zero (for equal dc-biased source voltages). As each of the converters, represented by the sources, does not need to produce a zero output voltage, voltage-crossover distortion problems do not exist. We can see from Fig. 5.7 that this push-pull arrangement of sources requires that one acts as a source, while the other as a sink. Thus, converter realizations need to be current bidirectional even when feeding only a purely resistive load. In this case, operation of each converter is restricted to quadrants I and IV. A circuit implementation of the DLE scheme is shown by the example of a buck-derived PWM inverter in Fig. 5.8a. A quasi-resonant counterpart, using the bidirectional switch implementation of Fig. 5.6, is shown in Fig. 5.8b. Considering the large number of components needed in Fig. 5.8b, one wonders whether a simpler solution exists. Fortunately, one does exist and is based on a different, basic inverter scheme which is explained next.

5.3.2 Switched Source Excitation

Figure 5.9 shows two ways of implementing an alternative basic scheme to achieving inversion. This scheme has been termed the Switched Source Excitation (SSE) scheme. In Fig. 5.9a two sources are used which, as before, may represent control-variable modulated dc-to-dc converters. Each source produces a unipolar voltage which varies from zero to some finite value. Switch S1 switches the appropriate source at the appropriate time to the load to produce a bipolar voltage output. If the load is purely resistive, each converter, represented by the sources, need only operate in one quadrant, thus reducing the number of switches required. This contrasts with the DLE scheme

a)



b)

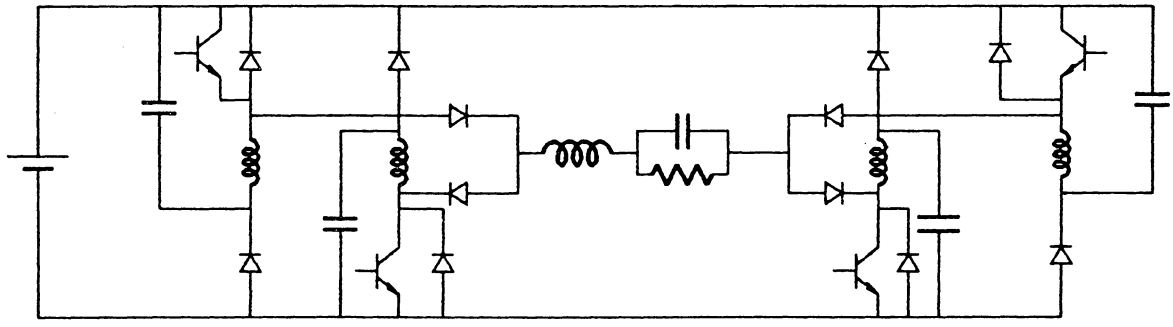


Fig. 5.8 *(a) PWM dc-to-ac inverter circuit implementation based on the DLE scheme of Fig. 5.7*
(b) Quasi-resonant four-quadrant dc-to-ac buck-derived inverter based on the DLE scheme

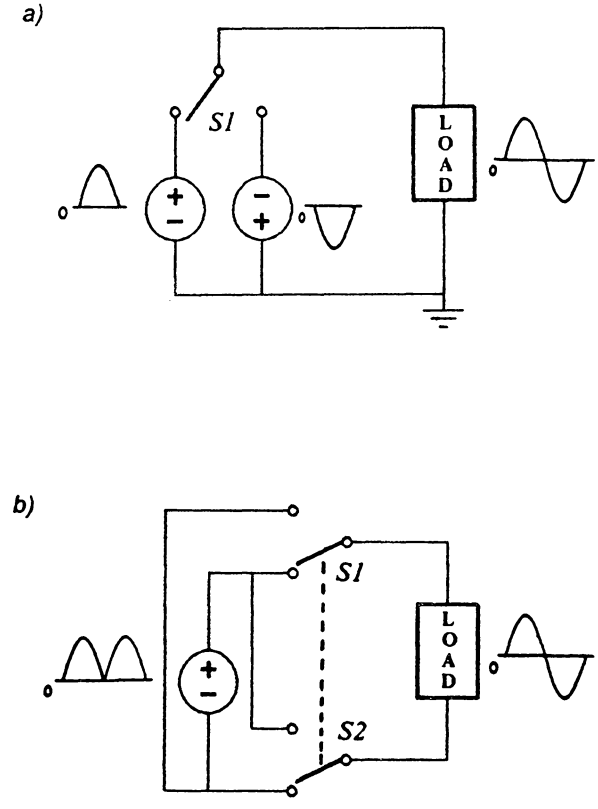


Fig. 5.9 *An alternative basic approach to achieving dc-to-ac inversion: Switched Source Excitation (SSE) scheme*

where two-quadrant operation is required even for resistive loads. Another advantage of the SSE scheme of Fig. 5.9a is that one side of the load is always grounded.

Figure 5.9b shows an extension of the basic scheme. Here, only one unipolar source (converter) is required producing a bipolar voltage across the load by suitably switching S1 and S2.

A disadvantage of the SSE approaches of Figs. 5.9a and 5.9b is that, in practice, when the output of a converter swings down to zero, we find performance aberrations occur which produce crossover distortion. Whilst this problem does exist, solutions also exist. As will be seen, even when required to drive a reactive load, inverters based on the SSE approach have the advantage of a reduced number of switches as compared to inverters based on the DLE approach. Therefore, let us take a closer look at the SSE scheme.

In the SSE scheme, we can identify two basic functions that need to be performed:

1. active waveshaping

2. polarity switching

Active waveshaping is performed by the converter(s) and, as indicated in Fig. 5.9, to synthesize a sine-wave output each converter must produce a half-sine waveform. For quasi-resonant converters, two different means of control can be used to effect control of the output voltage:

1. Switching-Frequency Modulation (FM)

2. Integral Pulse-Width-Modulation (IPWM)

Frequency modulation is the usual control method for quasi-resonant converters. The SSE scheme generally requires the switching frequency to be brought down to zero in order to bring the output voltage to zero. When this happens the output ripple performance deteriorates. However, in inverter applications where large output voltage excursions are required, the output of the converter spends little time near zero thus minimizing the ripple problem.

In a later section, two quasi-resonant converters, derived from converters generated in Chapter 1, will be presented that produce a zero output voltage when the switching frequency equals half the resonant frequency which can be quite a high value; thus, these converters do not exhibit the above problem.

The IPWM method of control is an alternative approach to controlling quasi-resonant converters. This control method basically entails operating the QRC at a fixed switching frequency and varying the output by pulsing the QRC on for varying duty cycles, which consist of an integral number of switching cycles. This scheme, at present has not been investigated and, therefore, attention will be directed toward FM control of QRCs. Note that the quasi-resonant topologies that will be presented below can operate with either control scheme.

The second function of the SSE scheme is polarity switching. This is done using S1 in Fig. 5.9a and S1 and S2 in Fig. 5.9b. Operating conditions for these switches are favorable as they switch at the much lower inversion-frequency rate. Moreover, for output-switched inverters (this terminology is explained below), switching occurs at

zero-voltage crossings and, for input-switched inverters (explained below), the switching devices switch at zero current. Thus, in both cases switching losses are eliminated.

These switches and others operating at the inversion frequency will be referred to collectively as inversion (IN) switches. Whereas switches operating to excite the resonant tank will be referred to as high-frequency (HF) switches.

In the following sections a number of different quasi-resonant inverter topologies will be presented based on the SSE approach. Extensions to this approach will also be given to show how reactive loads can be handled while using a one-quadrant converter.

5.4 Quasi-Resonant Inverter Topologies

In this section a number of different inverter topologies are presented based on full-wave, quasi-resonant dc-to-dc converters. Full-wave operation is desirable as the voltage-conversion ratio is virtually load independent. While the topologies proposed are really only suited to handling resistive loads, we will see how these basic topologies can be used to handle reactive loads, in a subsequent section.

Attention will be focused on two broad categories of inverters:

1. buck-derived

    a. output switched
    b. input switched

2. sepic-variant-derived (output switched)

The buck-derived inverters are of particular interest as their gain characteristics are a linear function of switching frequency thus minimizing harmonic distortion in the output. Sepic-variant-derived inverters are of interest because operation down to a zero output voltage with a high value of switching frequency is possible, thus minimizing output ripple and, also, because the output voltage can be swept over its full range with a minimal sweep of the switching frequency.

5.4.1 Buck-Derived Output-Switched Inverters

As previously mentioned, one function required by inverters using the SSE scheme is that of polarity switching. This may be done either at the output or input of the converter. Figure 5.10 shows an output-switched buck-derived inverter based on the SSE scheme of Fig. 5.9a. Transistors Q1 and Q2 are the high frequency switches, while Q3 and Q4 are the inversion switches. When Q3 is on, Q1 is modulated, producing positive voltage excursions across the load. During this time Q2 and Q4 are off. During negative voltage excursions the reverse situation is true with Q2 being modulated while Q4 is on and Q1 and Q3 are off. Figure 5.11 shows two oscillograms of the output voltage produced by this inverter. Evident from these oscillograms is the undistorted nature of the output signal except near zero crossings where ripple performance deteriorates, as previously discussed.

Figure 5.12 shows a buck-derived output-switched inverter based on the SSE scheme of Fig. 5.9b. Transistor Q1 is the high frequency switch while Q2-Q5 are the inversion switches. Whilst a unipolar voltage output is produced by the front end converter, the

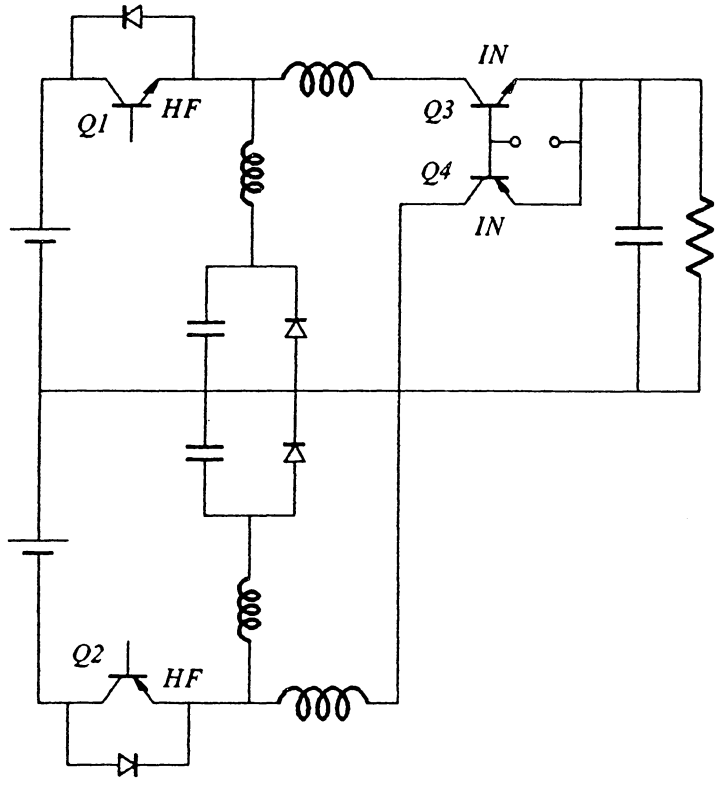
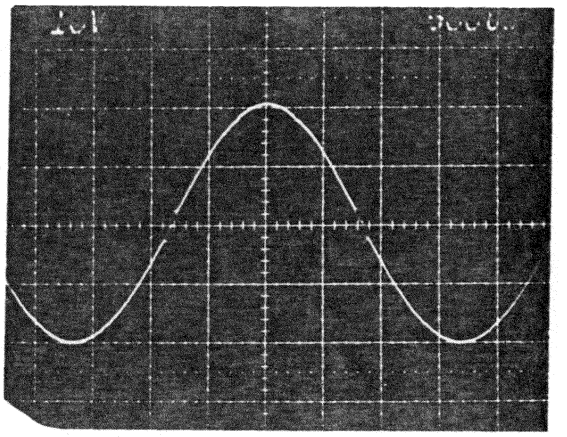


Fig. 5.10 *An output-switched buck-derived quasi-resonant inverter based on the SSE scheme of Fig. 5.9a*

a)



b)

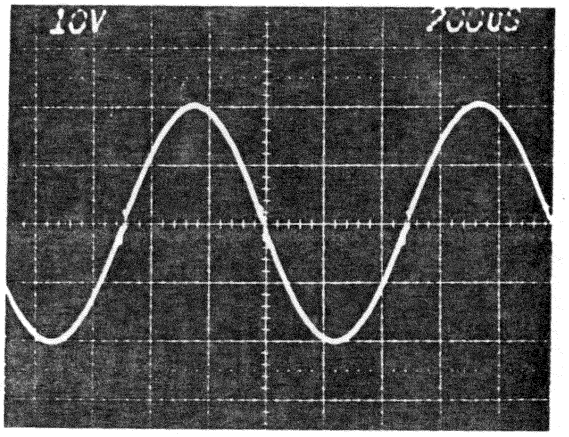


Fig. 5.11 *Output voltage waveforms of the inverter of Fig. 5.10*
(a) Inversion frequency = 300Hz, 10V/div., 500μS/div.
(b) Inversion frequency = 1000Hz, 10V/div., 200μS/div.

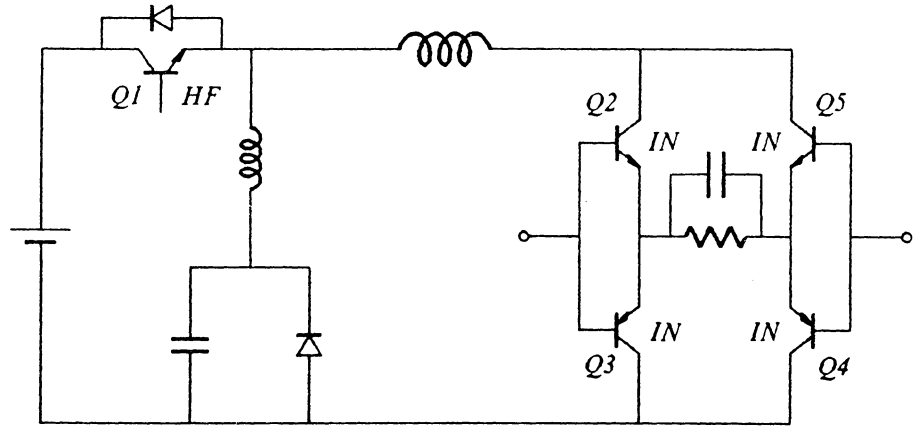


Fig. 5.12 *Buck-derived output-switched inverter based on the SSE scheme of Fig. 5.9b*

inversion switches invert the polarity across the load. When Q2 and Q4 are on (Q3 and Q5 are off), one polarity is impressed on the load; similarly, when Q3 and Q5 are on (Q2 and Q4 are off) the reverse polarity appears across the load.

As we can see, implementation of this inverter has resulted in a large, overall reduction in the number of components. The number of high-frequency switches has been reduced by one but at the expense of an increase of inversion switches. However, the requirements for these switches are much reduced due to slower switching-frequency operation.

5.4.2 Buck-Derived Input-Switched Inverters

To obtain a bipolar output voltage, one can switch the polarity of the output, as in Fig. 5.12, or alternatively, the polarity may be switched at the input, as in the inverter of Fig. 5.13. This buck-derived inverter might be considered a hybrid implementation of the two schemes shown in Fig. 5.9. For this inverter, a positive output voltage is derived by switching Q4 and Q5 on, with Q2, Q3 and Q6 off, and modulating Q1. A negative output voltage may be derived by modulating Q2, with Q3 and Q6 on, and Q1, Q4 and Q5 off. As shown, the inverter of Fig. 5.13 presents a square-wave voltage to the output inductor (this is also true of the inverters of Figs. 10 and 12) which minimizes the current ripple in the inductor [45]. If one wishes, the resonant inductor may be repositioned to present a sine-wave voltage [45] across the filter inductor. This, however, increases the inductor current ripple.

A large reduction of the number of switches used in the inverter of Fig. 5.13 may be achieved by altering the topology to that shown in Fig. 5.14. In this topology, there is

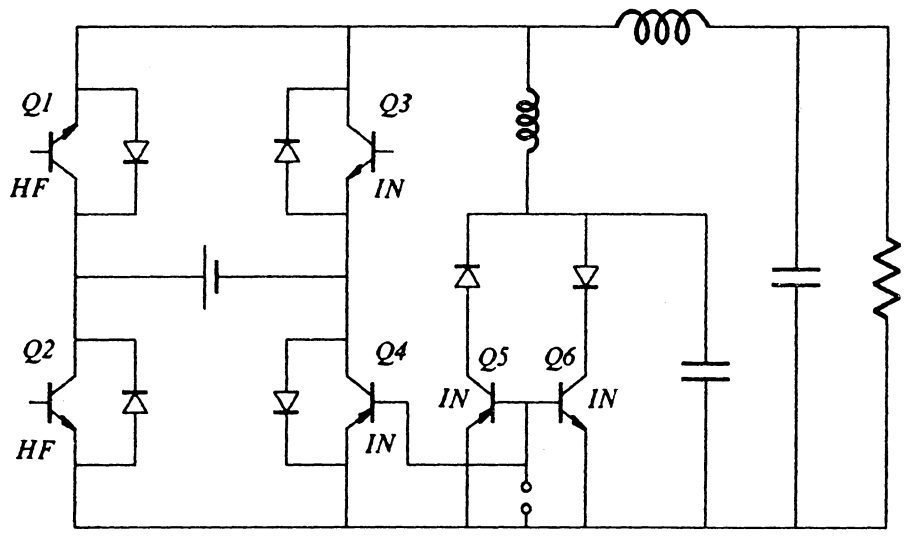


Fig. 5.13 *Buck-derived input-switched quasi-resonant inverter*

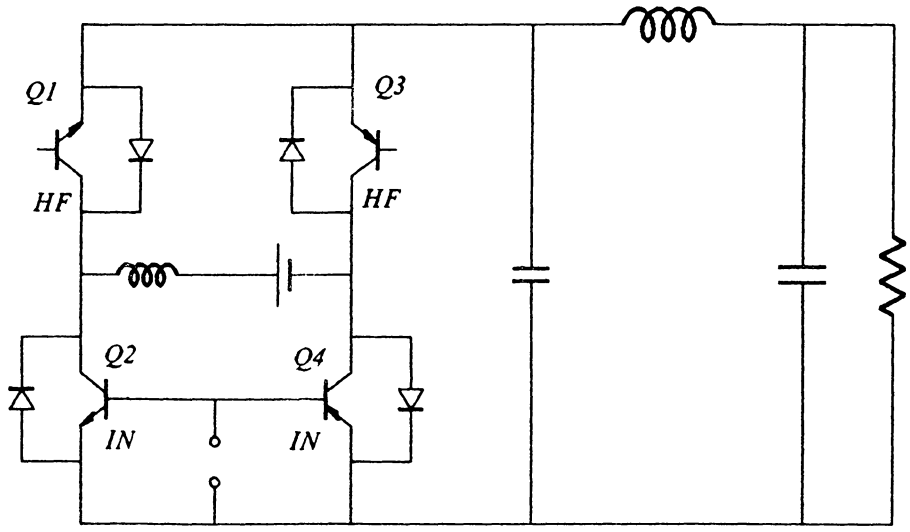


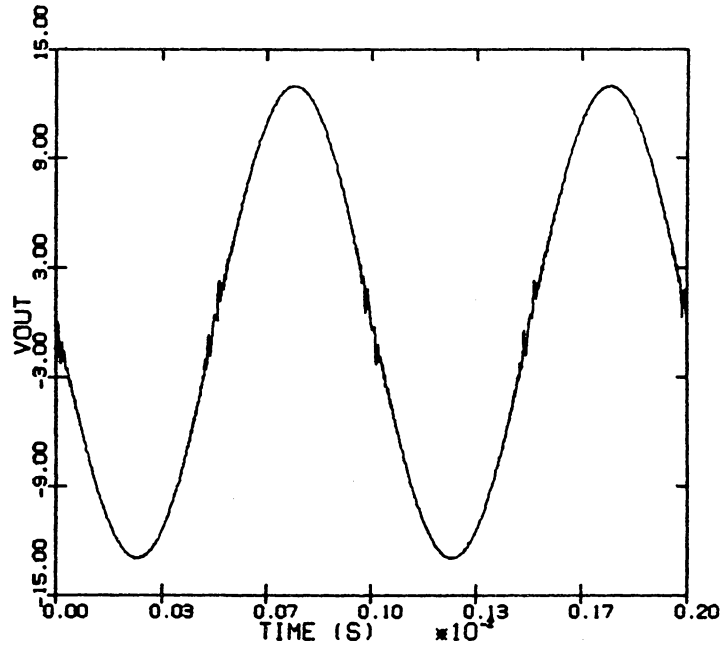
Fig. 5.14 *Buck-derived input-switched quasi-resonant inverter with a reduced number of switches*

still a bridge of transistors around the voltage source, but their function has changed. Transistors Q2 and Q4 are now the inversion switches with Q1 and Q3 functioning as the high-frequency switches. Note that this inverter impresses a sine-wave voltage [45] across the output inductor; a square-wave counterpart for this topology does not exist. During the positive half cycle of the output voltage, Q1 is modulated while Q4 is on, and Q2 and Q3 are off. Negative half cycles are derived by modulating Q3 with Q2 on and Q1 and Q4 off during that half cycle. Figure 5.15 shows simulated output waveforms at two different inversion frequencies. The rippling near zero crossings is quite evident at an inversion frequency of 1kHz (Fig. 5.15a), but the overall waveshape is quite good. At 20kHz (Fig. 5.15b), no rippling is seen as the regions near the zero crossings represent a much shorter time period. The overall waveshape is also seen to be quite good at this inversion frequency.

5.4.3 Sepic-Variant Inverters

As previously stated, a problem with the proposed inverter topologies is that ripple performance deteriorates near zero crossings. It is, therefore, of interest to search for topologies which achieve a zero output voltage while operating at a high switching frequency. Figure 5.16 shows two such dc-to-dc converter topologies. The resonant components in this figure have been denoted as Lo and Co. These converters, generated in Chapter 1 and denoted there as converter G4 in Table 2.2, have been named the Sepic-variant converters as they are derived from the Sepic converter (converter G5 in Table 2.2). The converters of Fig. 5.16 are essentially the same; the only difference is the position of the active switch. With the active switch in the bottom leg, as shown in Fig.

a)



b)

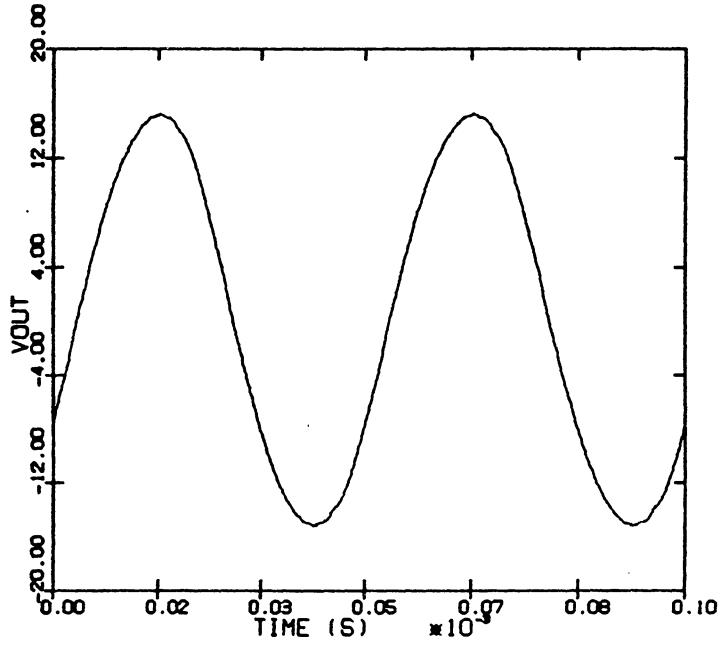


Fig. 5.15 *Simulated output voltage waveform of the inverter of Fig. 5.14*
(a) Inversion frequency = 1kHz
(b) Inversion frequency = 20kHz

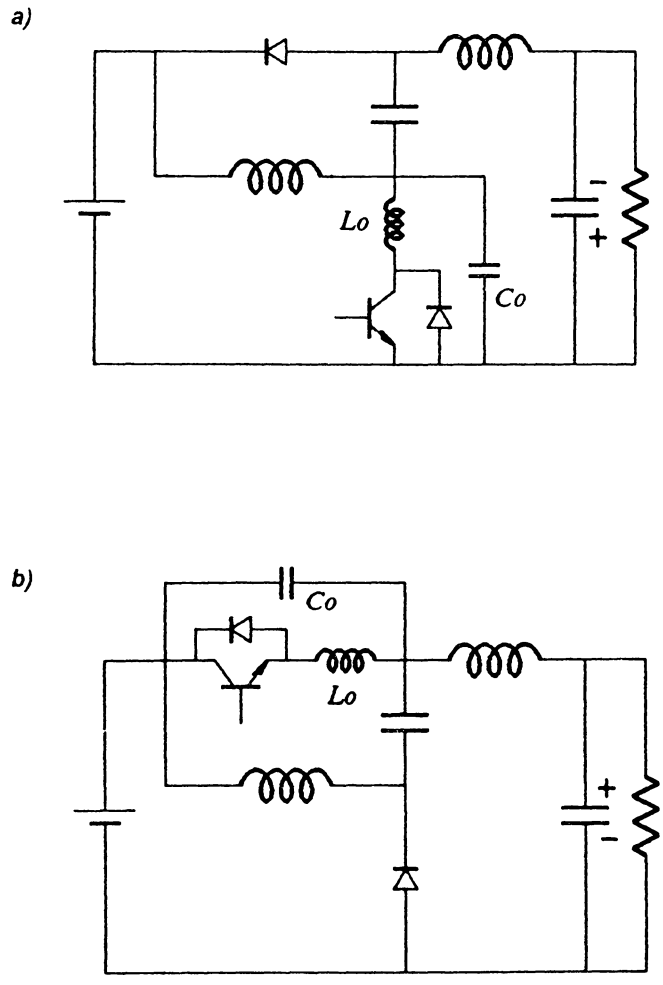


Fig. 5.16 *Sepic-variant dc-to-dc converter topologies*
(a) inverting
(b) non-inverting

5.16a, and for switching frequencies (f_s) greater than half the resonant frequency (f_o), the converter functions in an inverting mode. If, however, the active switch is placed in the top leg, as shown in Fig. 5.16b, then for $f_s > 1/2f_o$ the converter operates in a non-inverting mode. For both converters, ideally, at $f_s = 1/2f_o$ the output voltage is zero. The gain characteristics of these converters are shown in Fig. 5.17 for full-wave operation for different values of the normalized load parameter Q, (where normalization is with respect to the resonant tank characteristic impedance). It is interesting to note that the feature of zero output voltage for a nonzero switching frequency is lost when these converters operate in half-wave mode. Depending on the positions of the resonant components, a number of different variations of topologies may be achieved. In fact, each converter of Fig. 5.16 has 15 variations.

Figure 5.18 shows how output switching can be used with an inverting sepic-variant converter, similar to that shown in Fig. 5.16a (the resonant capacitor now appears in parallel with the freewheeling diode), in arriving at a sepic-variant inverter topology. The performance of this inverter is shown by the simulation in Fig. 5.19. Gone are the waveform deviations near zero crossings caused by ripple. Crossover distortion, however, still occurs and, as stated earlier, this is one of the shortcomings of the SSE scheme of Fig. 5.9 as implemented here. Despite the nonlinear gain characteristic shown in Fig. 5.16a, visibly absent from the simulation is distortion due to this characteristic. An FFT applied to the simulated waveform indicated a total harmonic distortion figure of only 2.85%.

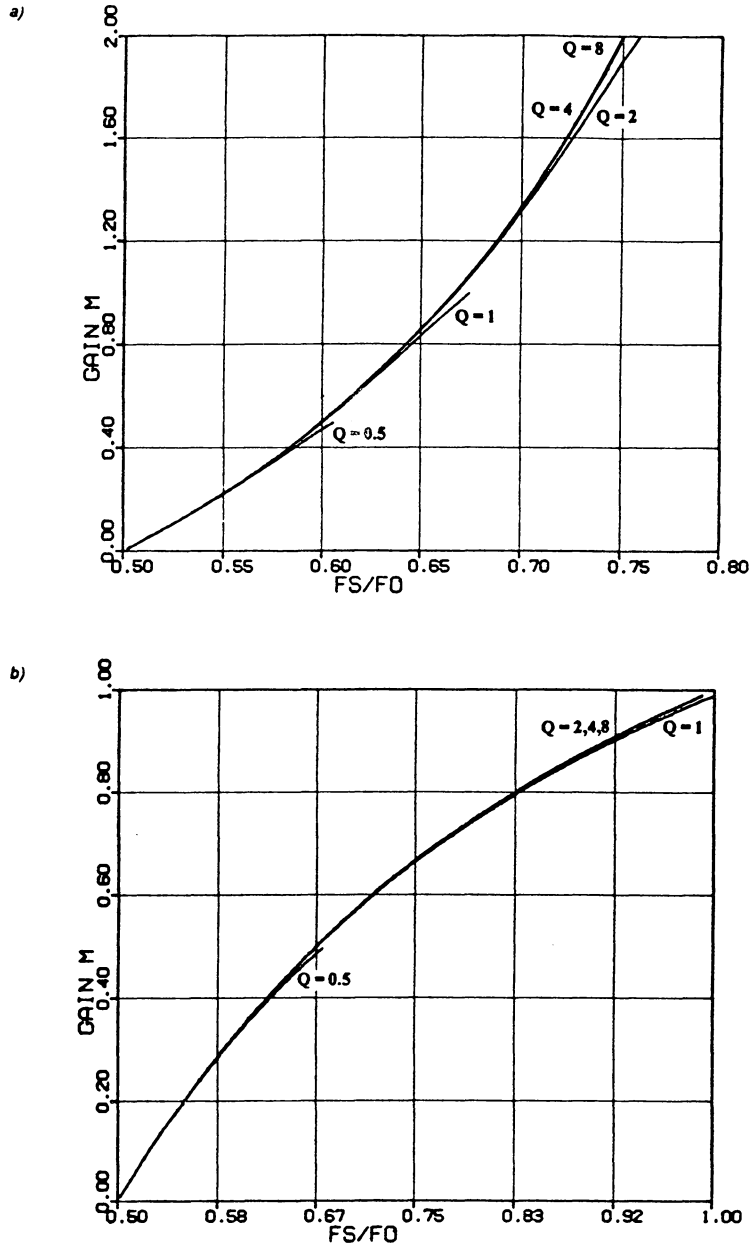


Fig. 5.17 *DC gain characteristics of the sepic-variant converters of*
(a) Fig. 5.16a
(b) Fig. 5.16b

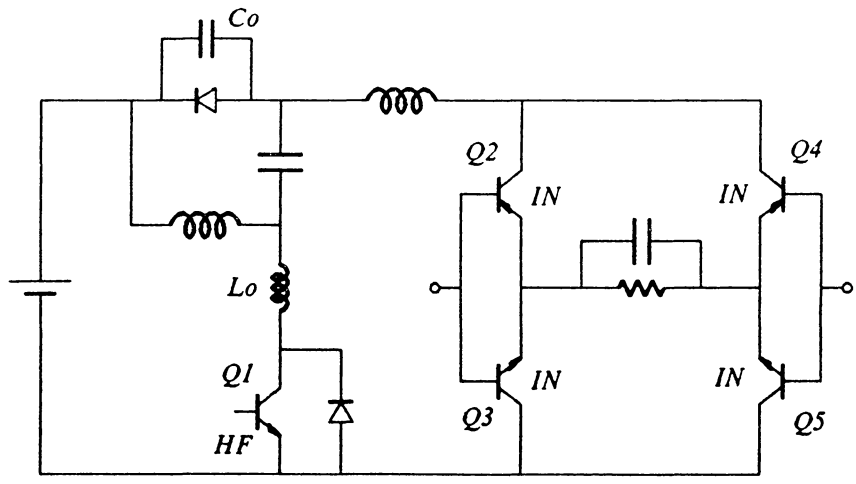


Fig. 5.18 *A sepic-variant quasi-resonant inverter*

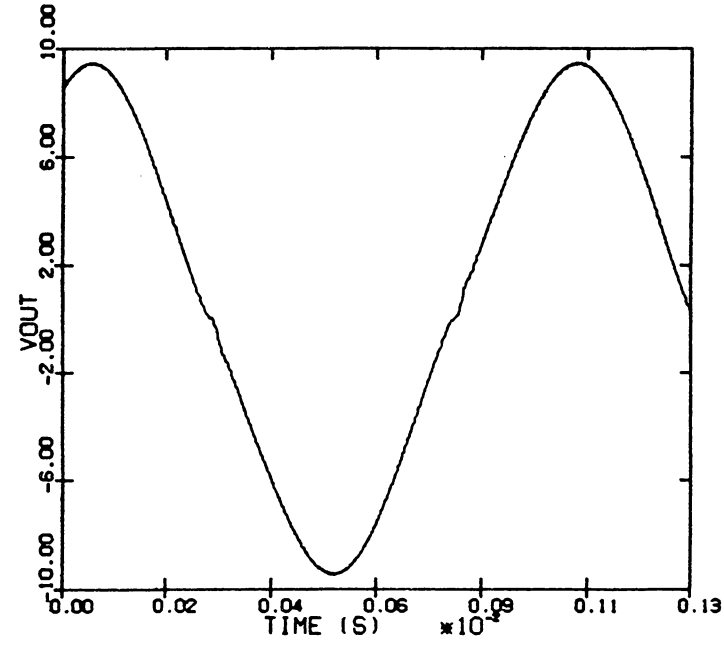


Fig. 5.19 *Simulated output voltage waveform of the inverter of Fig. 5.18 at an inversion frequency of 1000Hz*

5.5 Reactive Load Handling

The inverter topologies presented do not perform well when feeding a reactive load since a path is not provided for reverse load current, unless a capacitance is placed across the load. In the topologies presented a capacitor does appear across the load as part of the output filter. In these cases, reverse current from the load feeds into the capacitor thus charging it with a consequential deviation from that desired in the output waveform. The situation may be further aggravated by waveform rippling which occurs due to the resonance of the capacitor and an inductive load. This problem may be somewhat ameliorated by an increase in the value of the output capacitor thus lowering the resonant frequency; however, this limits the range of inversion frequencies that the inverter can handle.

In the following, three solutions to the problem of the handling of reactive loads are given. The first two schemes show how the reverse power from the load can be returned to the source thus maintaining high efficiency. In the third solution, the reverse power is dissipated; thus, inverter efficiency suffers. However, the degree to which efficiency is compromised is dependent on the load power factor and may be tolerable, especially, as this scheme has a number of major advantages.

Before presenting the three schemes for reactive load handling, it is of interest to consider the power level involved in reverse power flow from reactive loads. In the Appendix B we see that the ratio of the maximum, average, reverse power flow from a reactive load to the VA rating of the inverter is given by

$$\frac{P_r}{VA} = -\frac{1}{\pi}\,(\sin\phi - \phi\cos\phi)$$

where

$$\phi = \cos^{-1}(PF)$$

where PF is the load power factor.

For a power factor of 0.8, for example, the reverse power represents a mere 2.7% of the inverter VA rating. For a purely inductive load (PF = 0), the reverse power rises to 31.8% of the VA rating. In general, we can see that for loads that present a high-to-medium power factor, the amount of reverse power that needs to be handled is, in fact, quite small. This is an important factor, particularly, for the first scheme for handling reactive loads, which is presented next.

5.5.1 Regenerative Converter Scheme

This scheme [46,41,38] relies on providing a path for reactive current to flow back to the source via a regenerative converter, as shown in Fig. 5.20. During forward power transfer, that is, during operation in quadrants I and III as depicted in Fig. 5.2b, the main inverter is operating and waveshaping the output. During this time the regenerative converter is off. However, during operation in quadrants II and IV, as depicted in Fig. 5.2b, the main inverter is turned off and the regenerative converter is turned on directing power back to the source while, simultaneously, waveshaping the output. The power

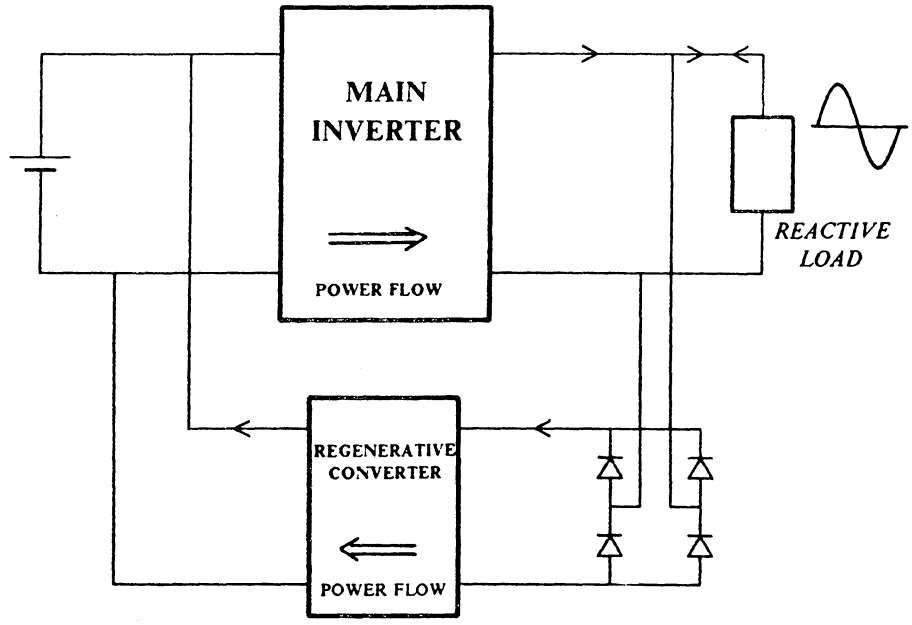


Fig. 5.20 *A basic scheme for reactive load handling by the use of a separate low-power regenerative converter*

rating of the regenerative converter need only be small as the reverse power delivered by the load is small.

This scheme for reactive load handling is a general scheme and can be applied to any of the inverters previously shown. The next two schemes are not as widely applicable; nevertheless, given this constraint, these schemes do have merit.

5.5.2 Modified Output Bridge Scheme

This second scheme [47] is mainly applicable to buck-derived inverters. The general scheme is shown in Fig. 5.21. The modified bridge that feeds the load performs two functions: 1) polarity switching and 2) reactive load handling. The operation of the inverter can best be understood by referring to the four load current paths the bridge provides, shown in Fig. 5.22, during operation in each of the four quadrants shown in Fig. 5.2b.

With quadrant I operation power from the QRC flows to the load via Q1, D1 and Q4 (Fig. 5.22a). All other switches in the modified bridge are off. The voltage across the load (v_l) is that appearing at the output of the QRC and ground (i.e., v_o, neglecting switch voltage drops). In quadrant II operation the load voltage is negative while positive current still flows through it (Fig. 5.2b). This constitutes reverse power flow which is directed back to the source via Q1, D1 and D4 (Fig. 5.22b). However, now the voltage across the load is $v_g - v_o$. It is thus apparent that the control of the QRC must change so the desired voltage across the load can be attained during operation in this quadrant. During operation in quadrants I and III when the voltage across the load (v_l) is that which appears between the output of the QRC and ground (v_o) the inverter

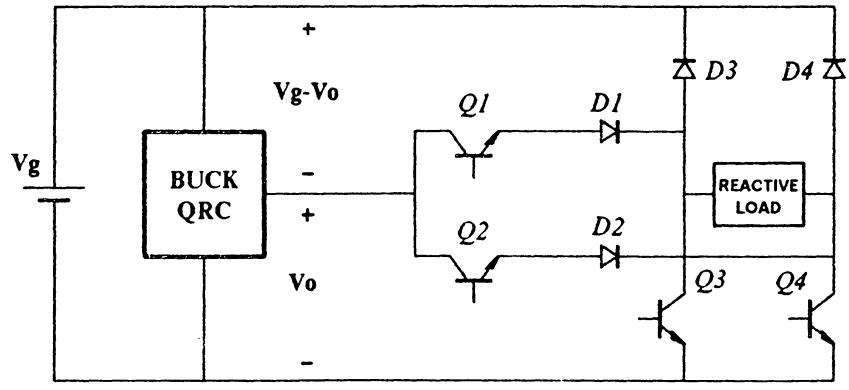


Fig. 5.21 *Reactive load handling by using a modified output bridge*

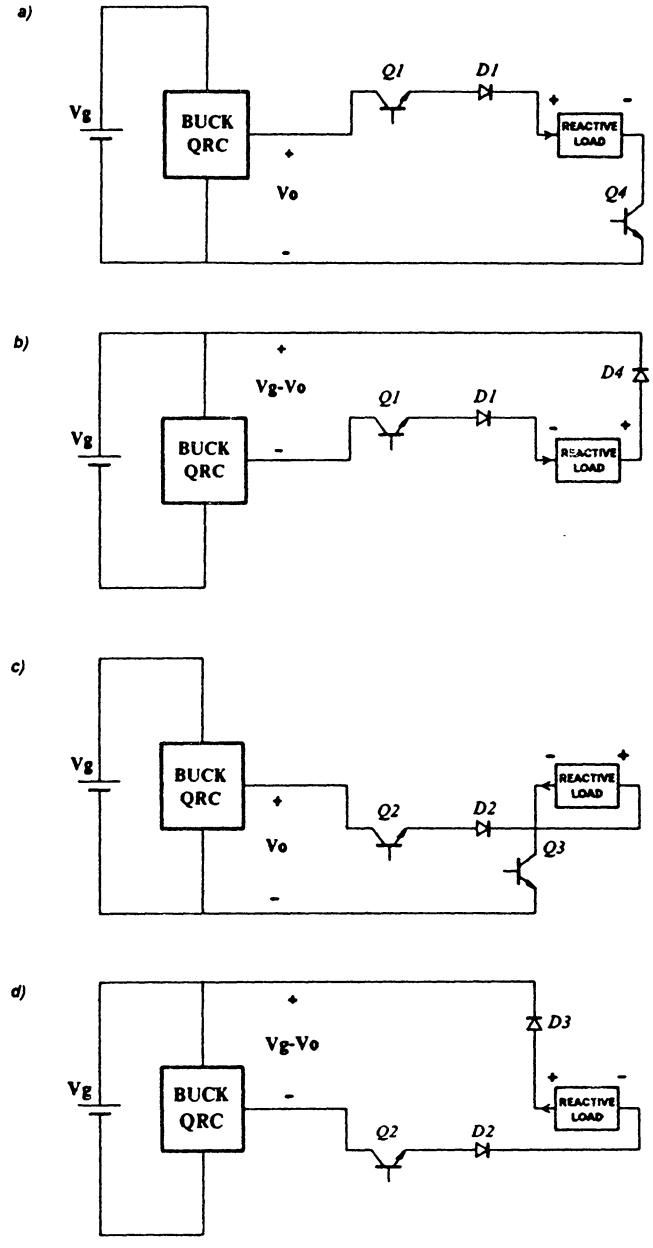


Fig. 5.22 *The four load current paths of the modified bridge for four quadrant operation*
(a) Quadrant I
(b) Quadrant II
(c) Quadrant III
(d) Quadrant IV

voltage gain, $q_f[\cdot]$, is a particular function of the normalized switching frequency (f_n) so

$$\frac{v_o}{v_g} = q_f[f_{n_f}(t)] = \frac{v_l}{v_g}$$

where the f subscript on the normalized switching-frequency function refers to the particular input present during operation in quadrants I and III. When operating in quadrants II and IV, the load voltage is taken from across the output of the QRC and input source ($v_l = v_g - v_o$) so the inverter gain $q_r[\cdot]$ is

$$q_r[f_{n_r}(t)] = \frac{v_l}{v_g} = \frac{v_g - v_o}{v_g} = 1 - q_f[f_{n_r}(t)]$$

where the r subscript on the normalized switching frequency function refers to the particular input present during operation in quadrants II and IV. Maintaining the output voltage at a desired level, while load current changes polarity, is easily done for buck-derived inverters since

$$\frac{v_o}{v_g} = q_f(f_n) \approx f_n$$

During operation in quadrants II and IV, the input $f_{n_r}(t)$ can be simply changed to

$$f_{n_r}(t) = 1 - f_{n_f}(t)$$

resulting in

$$\frac{v_l}{v_g} = f_{n_f}(t)$$

and the output follows the desired waveshape. For inverter applications

$$f_{n_f}(t) = |\sin \omega t|$$

would produce a sinusoidal output.

Operation of the modified bridge during quadrants III and IV (Figs. 22c and 22d) occurs in a way analogous to that in quadrants I and II and need not be discussed.

Figure 5.23 shows a buck inverter using the modified bridge. Comparison with the inverter of Fig. 5.8b, which is based on the DLE scheme, shows a much reduced parts count.

5.5.3 Composite Amplifier Scheme

The third, and final, scheme that may be used to handle reactive loads is the composite amplifier approach [48,53]. This scheme has been discussed in the literature [49,50,38] as a means of improving the quality of the output waveform in switching amplifiers. However, it also presents a way of handling reverse load current. References [48] and [53] give an excellent overview and generalizations of the composite amplifier approach, of which only one of four possible schemes will be discussed here. In its generalized form, the series-voltage composite amplifier approach is shown in Fig. 5.24. The voltage source v_m supplies most of the power needed in controlling the output voltage v_o, in fact, it produces a "rough" version of the output voltage. Source v_m may represent a switching amplifier. Voltage source v_c corrects the errors in the waveform presented by v_m thus producing a high-quality output waveform. Source v_c may represent a linear amplifier stage. The load current flows through both v_m and v_c, but as v_c only

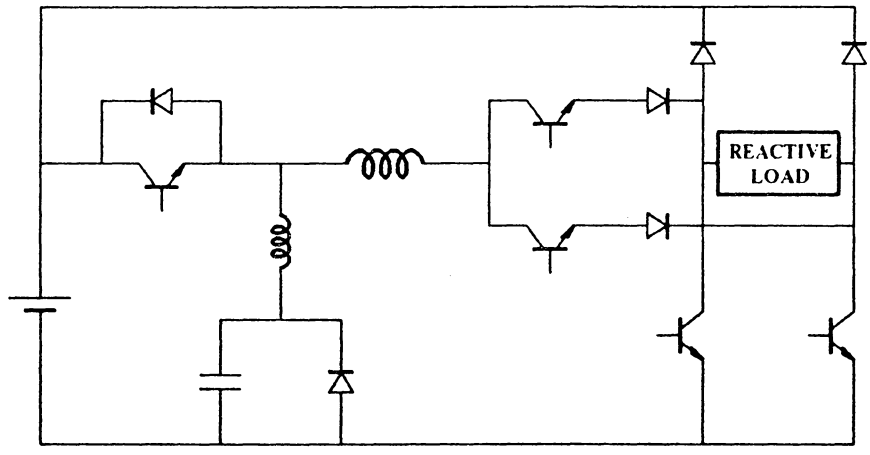


Fig. 5.23 *Buck inverter with modified output bridge*

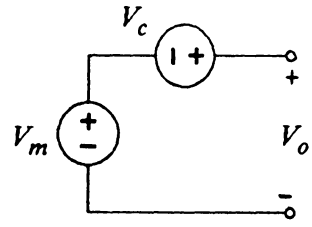


Fig. 5.24 *Series-voltage composite amplifier approach. Main power is supplied by v_m while v_c corrects for errors*

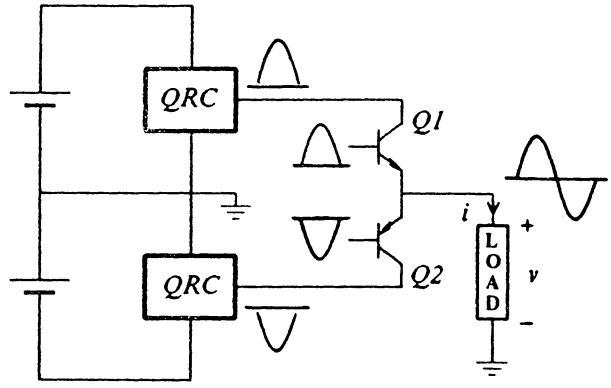


Fig. 5.25 *General schematic of a quasi-resonant amplifier/inverter using the series-voltage composite amplifier approach*

needs to be large enough to take up the difference between v_m and the desired v_o, the power dissipated in v_c is small.

Clearly, this scheme presents a way of achieving nearly the efficiency of a switching amplifier and at the same time producing an output waveform nearly the quality of a linear amplifier. Figure 5.25 shows, in a general way, how this approach can be applied to quasi-resonant amplifiers/inverters. The QRCs in this figure represent the v_m sources; whereas Q1 and Q2 represent v_c sources. Let us consider the positive half cycle of operation; Q1 collector and base terminals are modulated with positive half-sine excursions. The modulation at the collector has a slight dc offset of one or two volts greater than at its base terminal, therefore, Q1 is always operated in its linear region but the voltage differential is small enough not to cause much dissipation in the device. Similar operating characteristics apply for negative half cycles. If Q1 and Q2 together operate in a class AB mode, neither transistor turns off. Let us now consider the reactive load handling capability of this circuit. Due to symmetry, we need only consider one half cycle of operation. Assume that Q1 is being modulated so that a positive voltage appears across the load. At some part of this half cycle, for a reactive load, current flow will reverse direction. Now, as Q2 is always on, a path exists for this current to flow through Q2 to the negative power source. The reactive power is therefore dissipated in Q2. Thus, this approach shows a decrease in overall efficiency, dependent on the load power factor, but a marked improvement in the quality of the output waveform is achieved while furnishing the ability to handle a reactive load.

Crossover distortion is also minimized as crossover is now taken over by Q1 and Q2 where it is more easily handled than by the QRCs. Further distortion reduction can be achieved by applying feedback or the current dumping technique [51,52], (which is a

combination of feedforward and feedback control), to this circuit. However, this matter will not be discussed here.

Figure 5.10, in fact, shows one implementation of the principle shown in Fig. 5.25. If Q3 and Q4 are operated in their linear regions instead as switches as previously discussed, a high quality buck-derived quasi-resonant amplifier/inverter results. The ripple problem occuring at zero crossings previously associated with this inverter is now overcome using this approach. The offset voltage between the signals applied to the collector and base terminals of Q3 and also those associated with Q4 (needed to operate these transistors in their linear regions), now need to be large enough so that ripple voltage excursions do not saturate these transistors. Note, however, that the output of each buck QRC need not drop to zero for a zero output voltage as the dc offset must be maintained. Thus a lower, nonzero limit on the switching frequency excursions is set such that the maximum ripple voltages at the collectors of Q3 and Q4 are greatly minimized.

Figure 5.26 illustrates the operation of a breadboarded composite amplifier, the schematic of which is shown in Fig. 5.10 (with Q3 and Q4 operating in their active regions). The load voltage, v_l, and load current, i_l, are shown in Fig. 5.26a for an RL load. Clearly, the four quadrant operation of this inverter is evident, as is the high quality of the output voltage waveform. In Fig. 5.26b is shown the load voltage, v_l, and the voltages at the collectors, v^+ and v^-, of Q3 and Q4 (see Fig. 5.10).

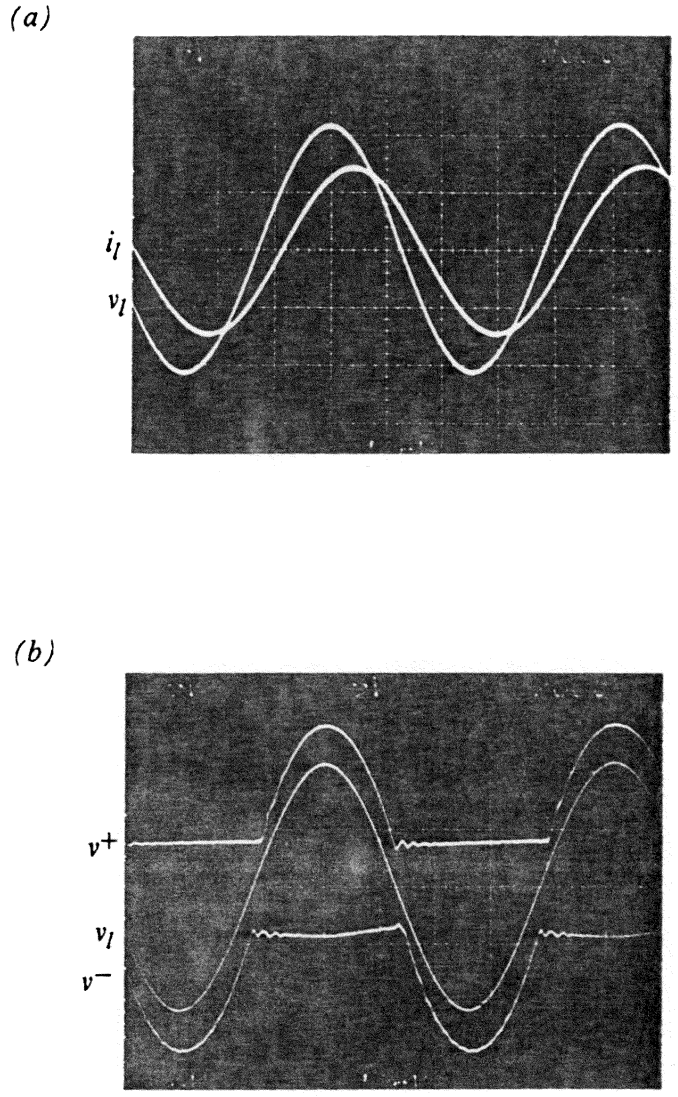


Fig. 5.26 *Composite-amplifier operation at 1000Hz using the circuit of Fig. 5.10*
(a) Load voltage, v_l, and load current, i_l
(b) Load voltage, v_l, and collector voltages, v^+ and v^-, of Q3 and Q4 (see Fig. 5.10)

5.6 Summary

Two basic approaches may be taken to achieve dc-to-ac inversion. The first, the Differential Load Excitation (DLE) scheme, relies on having two converters, driven out of phase, drive a load differentially. This scheme, unfortunately, requires a large number of components when implemented using quasi-resonant techniques. A more component effective approach uses the Switched Source Excitation (SSE) schemes. One SSE approach relies on having two converters where each handles one polarity of the signal. By appropriate switching, an amplified signal is reconstructed at the output. The second SSE approach entails only one converter but with a slightly more involved switching requirement. This second SSE approach allows for a significant overall reduction in the number of components needed and reduced performance requirements on most of the switches since most switch at the lower inversion-frequency rate.

A number of quasi-resonant inverter topologies, from two broad categories, were presented. The category of buck-derived inverters can be further subdivided into the two classes of output-switched and input-switched inverters. The buck-derived inverters are of particular interest as they display a linear control characteristic. The sepic-variant-derived inverters represent the second category discussed. These inverters permit operation down to zero output voltage with a high switching frequency and also provide a wide variation in output voltage with minimal control variation.

For applications which require inverters to supply reactive power, three schemes were discussed which can be applied to various inverters thus affording them reactive load handling capability.

The regenerative converter scheme provides a reverse path back to the source for reactive load power via a converter of a much smaller power capacity than that needed in the forward power path.

The modified output bridge scheme combines the functions of output voltage switching needed to reconstruct the output waveform and output current switching needed to handle reactive loads.

The composite amplifier scheme furnishes reactive load handling capability while simultaneously improving the output waveform quality and other performance measures. However, the efficiency of the overall inverter suffers at varying degrees depending on the load power factor.

Chapter 6: CONCLUSION

The area of topology forms a very important part of the field of power electronics. In this study into the topological aspects of power conversion and inversion, a number of different topologies have been presented.

In Chapter 2, PWM dc-to-dc converter topologies were examined. The structure of basic converters was identified. A basic converter was seen to consist of three basic substructures:

1. input source
2. converter cell
3. output sink

Particular attention was directed towards the converter cell which was seen to be a three-terminal structure which contains inductors, capacitors and switches connected in various arrangements. Given a particular converter-cell structure, it was found that either three or six different converters can be generated simply by permuting the connections of the converter cell to the input source and output sink. If the cell features

a symmetric structure, three different converters are generated, otherwise six different converters can be generated. A classification scheme of converters was proposed based on the order of the cell (i.e. the number of storage elements) and number of (single pole/single throw) switches present in the parent converter cell. Four categories of converter cells were considered:

1. 1st. order - 2 switch
2. 1st. order - 4 switch
3. 3rd. order - 2 switch
4. 3rd. order - 4 switch

A total of fourteen families of converters were identified in these categories. This led to the discovery of a large number of new converters. One, which was termed the Sepic-Variant converter, was found to be of particular use in inverter applications dealt with in Chapter 5.

Given the large number of generated converters the complete sets of two important classes of converters were enumerated. These converter classes were: 1) the class of two-topology single-inductor converters, and, 2) the class of converters featuring non-pulsating port currents.

The analysis of PWM converters was undertaken by two different approaches in Chapters 3 and 4. In Chapter 3, a classical approach to the analysis of nonlinear systems was adopted through use of Volterra/Wiener theory. The result of this analysis were mathematical models which describe the response of a particular harmonic of the excitation frequency which perturbs the control input. The analysis commenced by approximating PWM conversion systems, which are nonlinear time-varying

sampled-data systems, by a nonlinear time-invariant continuous-time model. This model represents an internal description of the system. Volterra kernels were then determined using this model, which then characterized an input/output description of the system which permits determination of the harmonic distortion performance.

The analogy between the different configurations of a converter cell in a converter-cell family and that of the different configurations of a transistor in a circuit, e.g. common base or common emitter configurations, is clear and, as such, motivates a new approach to converter analysis. Treating the converter cell, or alternatively, the PWM switch, as a nonlinear three-terminal device, circuit models were derived. These models can then be used in an analogous way in ordinary transistor circuit analysis whereby the nonlinear three terminal device is replaced by its model.

The PWM switch (i.e. the two single pole/single throw switches forming a single pole/double throw switch) represents the nonlinear substructure of a vast majority of converter cells. In Chapter 4, a nonlinear analysis of the PWM switch was performed. Equivalent circuit models were derived which are valid at different harmonics of the excitation frequency. A number of examples were given illustrating the use of these models.

The advantages of the PWM switch analysis approach of Chapter 4 over the Volterra series approach of Chapter 3 may be seen to be twofold:

1. A switch model is more versatile in that a converter model is much more easily obtained by replacement of the switch with its model than by performing an analysis on the converter as a whole which then yields a converter model. Moreover, as the PWM switch is present in

a vast number of PWM converters, once the switch model is obtained, it is trivial to obtain the converter model of a vast number of converters.

2. The PWM switch represents a static nonlinearity which is easily described by a Taylor series. In contrast, a PWM converter is a nonlinear system with dynamics which has a more involved mathematical description, such as that given by a Volterra series.

The area of topology was further pursued in Chapter 5 where a number of dc-to-ac inverter topologies, which use quasi-resonant techniques, were derived. After a discussion of amplifier/inverter basics, two basic approaches to inversion were identified. These approaches were termed the Differential Load Excitation (DLE) and the Switched Source Excitation (SSE) schemes. The means by which these approaches derive a zero dc-offset sinusoidal voltage across a load forms the essential difference between them. The SSE scheme was found to be more component effective and so use of this scheme was made in deriving a number of inverters. Buck and Sepic-Variant dc-to-dc converter topologies formed a basis for these inverters. The buck topologies feature a linear gain characteristic but suffer from an increased ripple content in the output voltage waveform near zero crossings. The Sepic-Variant topologies, on the other hand, do not suffer from ripple problems, however, their gain characteristics are somewhat nonlinear.

Three schemes which permit reactive load handling were identified. The regenerative converter scheme was seen to be the most generally applicable scheme. The composite amplifier scheme improves waveform quality at the expense of efficiency. The modified output bridge scheme was seen to be mainly applicable to buck derived inverters.

Both simulation and breadboarded prototypes have demonstrated the feasibility of the proposed approaches discussed above.

Appendix A. MODEL FOR CONVERTER-CELL A IN DISCONTINUOUS INDUCTOR CURRENT OPERATION

The dc and ac small-signal models of any converter cell can be derived and used in analyzing the converters comprising the members of the family generated by the cell. In the following the dc and ac small-signal models of converter-cell A will be derived for discontinuous inductor current operation. This converter cell, shown in Table 2.2, consists of the PWM switch (as defined in Chapter 4) and an associated inductor which forms a fundamental substructure of a large number of converter cells shown in Table 2.2. The derived model of converter-cell A can then be used to determine the dc operating conditions and the control-to-output transfer function as illustrated here for the specific case of the boost converter.

A.1 Derivation of Model for Converter-Cell A

Figure A.1a shows converter-cell A with the designated terminal voltages and currents and switch on-times for the cell operating in discontinuous conduction. Typical terminal current waveforms, for this mode, are shown in Fig. A.1b. Note there exists a subinterval, d_3T_s , when both switches are off. From the instantaneous waveforms we can find the average currents. Thus

$$i_1 = \frac{d^2 v_{13} T_s}{2L} \tag{A.1a}$$

$$i_2 = -\frac{d_2^2 v_{23} T_s}{2L} \tag{A.1b}$$

where d_2, defined in Fig. A.1b, will next be determined. From volt-second balance considerations on the inductor we find

$$d_2 = -\frac{dv_{13}}{v_{23}} \tag{A.2}$$

Thus (A.1b) becomes

$$i_2 = -\frac{d^2 v_{13}^2 T_s}{2Lv_{23}} \tag{A.3}$$

From (A.1a) and (A.3) the dc averaged model is given by

$$I_1 = \frac{D^2 V_{13} T_s}{2L} \tag{A.4a}$$

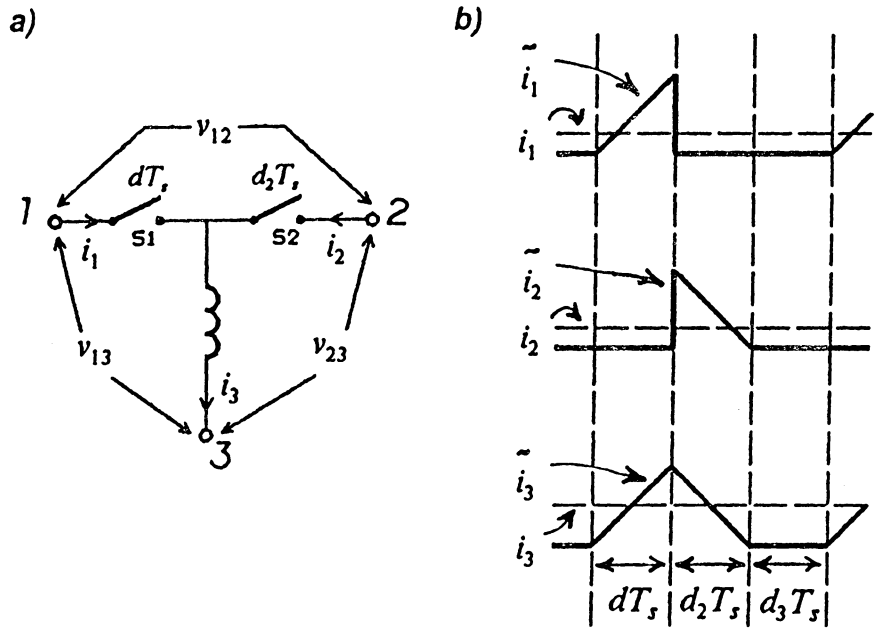


Fig. A.1 *a) Converter-cell A showing designated terminal voltages and currents and switch on-times for discontinuous conduction. During the d_3T_s sub-interval both switches are open.*
b) Typical instantaneous terminal currents, $\tilde{i}_1$, $\tilde{i}_2$ and $\tilde{i}_3$, and average terminal currents, i_1, i_2 and i_3, for converter-cell A in discontinuous inductor current operation.

and

$$I_2 = -\frac{I_1 V_{13}}{V_{23}} \qquad (A.4b)$$

To find the ac small-signal averaged model we perturb and linearize (A.1a) and (A.3) which gives

$$\hat{i}_1 = \frac{D^2 T_s}{2L}\,\hat{v}_{13} + \frac{2I_1}{D}\,\hat{d} \qquad (A.5a)$$

$$\hat{i}_2 = -\frac{2I_1}{V_{23}}\,\hat{v}_{13} - \frac{2I_1 V_{13}}{DV_{23}}\,\hat{d} + \frac{D^2 T_s V_{13}^2}{2LV_{23}^2}\,\hat{v}_{23} \qquad (A.5b)$$

From (A.4) and (A.5) a dc and ac small-signal averaged circuit model can be drawn. This model is given in Fig. A.2. One should note that in this model R_{13} is a dc and ac resistance whereas r_{23} is an ac-only resistance.

A.2 Example - Boost Converter in Discontinuous Conduction

In a similar fashion to that for continuous conduction, a dc and ac small-signal analysis for discontinuous conduction will now be performed on the boost converter shown as converter A2 in Table 2.2 and now also shown in Fig. A.3.

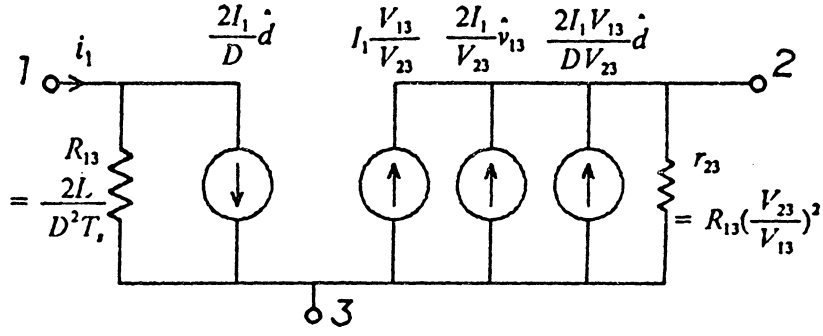


Fig. A.2 *dc and ac small-signal averaged model for converter-cell A operating in discontinuous conduction.*

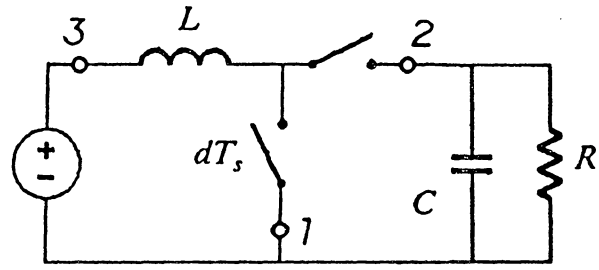


Fig. A.3 *The boost converter with converter-cell A terminals identified.*

dc Analysis

Replacing converter-cell A in Fig. A.3 point-by-point by its dc model in discontinuous conduction leads to the model of Fig. A.4. From this model we see that

$$V_o = \frac{I_1 V_{13}}{V_{23}} R \tag{A.6}$$

Also from Fig. A.4 we see,

$$\begin{aligned} V_{13} &= -V_g \\ V_{23} &= V_o - V_g \\ I_1 &= -\frac{V_g}{R_{13}} = -\frac{D^2 T_s}{2L} V_g \end{aligned} \tag{A.7}$$

Substituting (A.7) into (A.6) leads to

$$D = \sqrt{KM(M-1)} \tag{A.8}$$

where $M \equiv \frac{V_o}{V_g}$ and $K \equiv \frac{2L}{RT_s}$.

Solving the quadratic in M in (A.8) gives the dc voltage conversion ratio:

$$M = \frac{1 + \sqrt{1 + 4D^2/K}}{2} \tag{A.9}$$

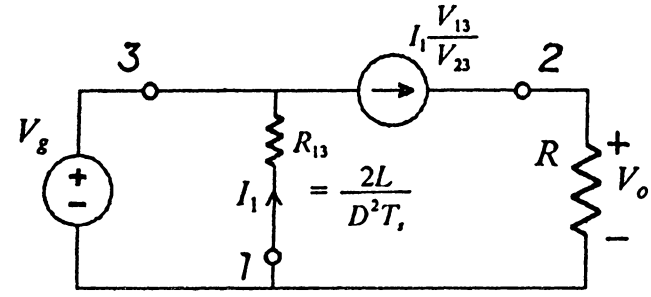


Fig. A.4 *dc model of the boost converter in discontinuous conduction.*

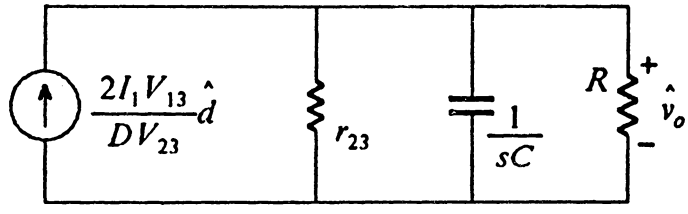


Fig. A.5 *ac small-signal model of the boost converter in discontinuous conduction used in deriving the control-to-output transfer function.*

ac Small-Signal Analysis

The ac model of the boost converter in discontinuous conduction used to derive the control-to-output transfer function is shown in Fig. A.5 and is given by substituting point-by-point the converter-cell model of Fig. A.2 into the boost converter of Fig. A.3.

ac resistance r_{23}, as specified in the model of Fig. A.2, is given by

$$r_{23} = \left(\frac{M-1}{M}\right)R \qquad (A.10)$$

where (A.7) and (A.8) have been used in deriving (A.10).

The circuit model of Fig. A.5 gives the required result:

$$\frac{\hat{v}_o}{\hat{d}} = \frac{2V_o}{2M-1}\sqrt{\frac{M-1}{KM}}\,\frac{1}{1+s\left(\frac{M-1}{2M-1}\right)RC} \qquad (A.11)$$

Appendix B. REACTIVE LOAD POWER

In this appendix the ratio of the maximum average reverse power, delivered by a reactive load, to the overall inverter VA rating, given a particular load power factor, is calculated. Without loss of generality, we will consider a resistive-inductive load for which voltage and current waveforms are given in Fig. 5.2b.

These waveforms may be expressed as follows:

$$v = V_m \sin \omega t$$

$$i = I_m \sin(\omega t - \phi)$$

where V_m and I_m are the maximum peak values of the voltage and current waveforms, respectively; ω represents the inversion angular frequency and ϕ represents the lag angle between voltage and current waveforms. The load power factor (PF) is simply

$$PF = \cos \phi$$

From Fig. 5.2b we see that, for one inversion cycle, reverse power flows during operation in quadrants II and IV. The maximum average reverse power is given by

$$P_r = \frac{2\pi}{\omega}\left[\int_0^{\phi/\omega}[V_m \sin \omega t][I_m \sin(\omega t - \phi)]dt + \int_{\pi/\omega}^{(\pi+\phi)/\omega}[V_m \sin \omega t][I_m \sin(\omega t - \phi)]dt\right]$$

Due to half-cycle odd symmetry the above expression can be reduced to

$$P_r = \frac{4\pi}{\omega} V_m I_m \int_0^{\phi/\omega} \sin \omega t \sin(\omega t - \phi)dt$$
$$= -V_m I_m\left[\frac{\sin \phi - \phi \cos \phi}{2\pi}\right]$$

The inverter's VA rating is simply

$$VA = \frac{1}{2} V_m I_m$$

Therefore,

$$\frac{P_r}{VA} = -\frac{1}{\pi}(\sin \phi - \phi \cos \phi)$$

REFERENCES

[1] S. Cuk and R.D. Middlebrook, "A New Optimum Topology Switching DC-to-DC Converter," IEEE Power Electronics Specialists Conference, 1977 Record, pp. 160-179 (IEEE Publication no. 77CH1213-8).

[2] R.P. Massey and E.C. Snyder, "High Voltage Single-Ended DC-DC Converter," IEEE Power Electronics Specialists Conference, 1977 Record, pp. 156-159 (IEEE Publication no. 77CH1213-8).

[3] P.W. Clarke, "A New Switched-Mode Power Conversion Topology Provides Inherently Stable Response," Proc. Powercon 10, The Tenth International Solid-State Power Electronics Conference, pp. E2.1-E2.7, March 1983.

[4] D.I. Sheppard and B.E. Taylor, "A New Converter Topology Imparts Non-Pulsating Currents to Input and Output Lines," Proc. PCI/MOTOR-CON, pp. 60-73, Sept., 1983.

[5] R.W. Erickson, "Synthesis of Switched-Mode Converters," IEEE Power Electronics Specialists Conference, 1983 Record, pp. 9-22. (IEEE Publication no. 83CH1877-0).

[6] A. Pietkiewiecz and D. Tollick, "Systematic Derivation of Two-State Switching DC-DC Converter Structures," IEEE International Telecommunications Energy Conference Record, Nov., 1984, pp. 473-477. (IEEE Publication no. 84CH2073-5).

[7] S. Cuk, "Survey of Switching Converter Topologies, Magnetics and Control," Proc. IEE International Conference on Power Electronics and Variable-Speed Drives, pp. 83-94, May, 1984.

[8] S. Cuk and Z. Zhang, "Power Electronics Circuits," Advances in Circuits and Systems, Proc. of China 1985 International Conference on Circuits and Systems, pp. 362-369, June, 1985.

[9] S. Cuk, "Basics of Switched-Mode Power Conversion: Topologies Magnetics and Control," Advances in Switched-Mode Power Conversion, Vol. II, TESLAco, Ca., 1981, pp.279-310.

[10] E.E. Landsman, "A Unifying Derivation of Switching Regulator Topologies," IEEE Power Electronics Specialists Conference Record, June, 1979, pp. 239-243. (IEEE Publication No. 79CH1461-3).

[11] N.R.M. Rao, "A Unifying Principle behind Switching Converters and Some New Basic Configurations," IEEE Transactions on Consumer Electronics, Vol. CE-26, Feb., 1980, pp. 142-148.

[12] N.R.M. Rao, "A Unified Analysis of the Linear-Domain Dynamic Behaviour of Three-State Switching Converters," IEEE Transactions on Consumer Electronics, Vol. CE-27, May, 1981, pp. 166-176.

[13] R. Mahadevan, S. El-Hamamsy, W.M. Polivka and S. Cuk, "A Converter with Three Switched-Networks Improves Regulation, Dynamics and Control," Proc. Powercon 10, The Tenth International Solid-State Power Electronics Conference, pp. E1.1-E1.15, March, 1983.

[14] R.D. Middlebrook, "Transformerless DC-to-DC Converters with Large Conversion Ratios," IEEE International Telecommunications Energy Conference Record, Nov., 1984, pp. 455-460. (IEEE Publication no. 84CH2073-5).

[15] R. Severns, "Switchmode Topologies - Make Them Work For You," Intersil, Inc. Applications Note AO-35.

[16] Private Correspondence R.W. Erickson to R.P.E. Tymerski, July, 1986.

[17] R.P.E. Tymerski and V. Vorperian, "Generation, Classification and Analysis of Switched-Mode DC-to-DC Converters by the Use of Converter Cells," IEEE International Telecommunications Energy Conference Record, Oct., 1986, pp. 181-195. (IEEE Publication no. 86CH2328-3).

[18] V. Vorperian, R.P.E. Tymerski, K. Liu and F.C. Lee, "Generalized Resonant Switches: Topologies and Analysis, Parts I and II," Conference Proceedings of the Virginia Power Electronics Center (VPEC), Virginia Polytechnic Institute and State University, Nov., 1986, pp. 116-131.

[19] K. Liu and F.C. Lee, "Resonant Switches - A Unified Approach to Improve Performance of Switching Converters," IEEE International Telecommunications Energy Conference Record, Nov., 1984, pp. 334-341. (IEEE Publication no. 84CH2073-5).

[20] K. Liu, R. Oruganti and F.C. Lee, "Resonant Switches - Topologies and Characteristics," IEEE Power Electronics Specialists Conference, 1985 Record, pp. 106-116. (IEEE Publication no. 85CH2117-0).

[21] K. Liu and F.C. Lee, "Zero-Voltage Switching Technique in DC/DC Converters," IEEE Power Electronics Specialists Conference, 1986 Record, pp. 58-70. (IEEE Publication no. 86CH2310-1).

[22] N. Wiener, "Response of a Nonlinear Device to Noise," MIT Radiation Lab., Rep. V-165, Apr. 6, 1942.

[23] V. Volterra, "Theory of Functionals and of Integral and Integro-Differential Equations," New York, Dover Publications Inc., 1959.

[24] Chin-Chun Su, "Volterra Functional Analysis of Nonlinear Systems with Deterministic and Stochastic Inputs," Ph.D. thesis, University of Pennsylvania, 1967.

[25] Josef Bartos, "Nonlinearities via Volterra Series with Applications," Ph.D thesis, Drexel University, August 1986.

[26] Stephen Boyd, "Volterra Series: Engineering Fundamentals," Ph.D thesis, University of California, Berkeley, March 1985.

[27] M. Schetzen, "Nonlinear System Modeling Based on the Wiener Theory," IEEE Proceedings, Vol. 69, No. 12, pp.1557-1573, December 1981.

[28] J.J. Bussgang, L. Ehrman and J.W. Graham, "Analysis of Nonlinear Systems with Multiple Inputs," Proceedings of the IEEE, Vol. 62, No. 8, pp.1088-1119, August 1974.

[29] E. Bedrosian and S.O. Rice, "The Output Properties of Volterra Systems (Nonlinear Systems with Memory) Driven by Harmonic and Gaussian Inputs," Proceedings of the IEEE, Vol. 59, No. 12, pp.1688-1706, December, 1971.

[30] W.J. Rugh, "Nonlinear System Theory," Baltimore, Md., The Johns Hopkins University Press, 1981.

[31] M. Schetzen, "The Volterra and Wiener Theories of Nonlinear Systems," New York, John Wiley and Sons, Inc., A Wiley-Interscience Publication, 1980.

[32] R.W. Erickson, S. Cuk and R.D. Middlebrook, "Large-Signal Modelling and Analysis of Switching Regulators," IEEE Power Electronics Specialists Conference, PESC 1982 Record, pp. 240-250. (IEEE Publication no. 82CH1762-4).

[33] R.P.E. Tymerski and V. Vorperian, "Generation, Classification and Analysis of Switched-Mode DC-to-DC Converters by the Use of Converter Cells," IEEE International Telecommunications Energy Conference Record, Oct., 1986, pp. 181-195. (IEEE Publication no. 86CH2328-3).

[34] R.D. Middlebrook and S. Cuk, "A General Unified Approach to Modelling Switching-Converter Power Stages," IEEE Power Electronics Specialists

Conference, 1976 Record, pp. 18-34. (IEEE Publication no. 76CH1084-3); also International Journal of Electronics, Vol. 42, No. 6, pp. 521-550, June 1977.

[35] S. Cuk, "Modelling, Analysis and Design of Switching Converters," Ph.D. thesis, California Institute of Technology, Nov., 1976.

[36] R.W. Erickson, "Large Signals in Switching Converters," Ph.D. thesis, California Institute of Technology, Nov., 1982.

[37] C.J. Hsiao, R.B. Ridley, H. Naitoh and F.C. Lee, "Circuit-Oriented Discrete-Time Modeling and Simulation for Switching Converters," IEEE Power Electronics Specialists Conference, 1987 Record, pp. 167-176. (IEEE Publication no. 87CH2459-6).

[38] E. Rhyne and L. Illingworth, "A New Concept for DC to AC Inverters and Ringing Generators," IEEE International Telecommunications Energy Conference, INTELEC 1986 Record, pp. 437-443, (IEEE Publication no. 86CH2328-3).

[39] P.U. Lind, "Four Quadrant Bilateral Power Converter," PCI March 1982 Proceedings, pp. 142-150.

[40] K. Harada, H. Sakamoto and M. Shoyama, "Small UPS Using Phase Control," IEEE International Telecommunications Energy Conference, INTELEC 1987 Record, pp. 516-520, (IEEE Publication no. 87CH2477-8).

[41] B. Brackus, "Switched Mode PWM DC/AC Inverter for Uninterruptible 50Hz AC Power Supply," IEEE International Telecommunications Energy Conference, INTELEC 1982 Record, pp. 49-54, (IEEE Publication no. 82CH1818-4).

[42] H. Kuyken, D. Baert and H. Simoens, "A Modular 0.5 - 5kW Inverter for UPS - Applications," IEEE International Telecommunications Energy Conference, INTELEC 1985 Record, pp. 249-255, (IEEE Publication no. 85CH2241-8).

[43] A. Cocconi, S. Cuk and R.D. Middlebrook, "High-Frequency Isolated 4kW Photovoltaic Inverter for Utility Interface," PCI September 1983 Proceedings; also, Advances in Switched-Mode Power Conversion, Vol. III, TESLAco, Ca., pp. 325-345.

[44] U. Boegli and R. Ulmi, "Realization of a New Inverter Circuit for Direct Photovoltaic Energy Feedback into the Public Grid," IEEE Transactions on Industry Applications, Vol. IA-22, No. 2, March/April 1986, pp. 255-258.

[45] T. Zeng, D.Y. Chen and F.C. Lee, "Variations of Quasi-Resonant DC/DC Converters," IEEE Power Electronics Specialists Conference, PESC 1986 Record, pp. 381-392, (IEEE Publication no. 86CH2310-1).

[46] G.P. Hicks and K.E. Banfield, "The Development of a Lightweight, Modular, Sinewave Inverter System Eliminating Common Control and Low Frequency Transformation," IEEE International Telecommunications Energy Conference, INTELEC 1981 Record, pp. 150-155, (IEEE Publication no. 81CH1653-5).

[47] M.F. Schlecht, "Bipolar Power Flow in a DC/AC Converter With Only One High-Frequency Switch Pair," IEEE Power Electronics Specialists Conference, PESC 1985 Record, pp. 181-187, (IEEE Publication no. 85CH2117-0).

[48] G.B. Yundt, "Series Parallel Connected Composite Amplifiers," IEEE Power Electronics Specialists Conference, PESC 1984 Record, pp. 121-128, (IEEE Publication no. 84CH2000-8).

[49] S. Kashiwagi, "A High-Efficiency Audio Power Amplifier Using a Self-Oscillating Switching Regulator," IEEE Transactions on Industry Applications, Vol. IA-21, No.4, July/August 1985, pp. 906-911.

[50] H. Nakagaki, N. Amada and S. Inoue, "A High-Efficiency Audio Power Amplifier," 70th Audio Engineering Society Convention, Oct./Nov. 1981, Reprint no. 1804.

[51] P.J. Walker and M.P. Albinson, "Current Dumping Audio Amplifier," Wireless World, Dec. 1975, p. 560.

[52] N.M. Allinson and J. Wellingham, "Distortion Reduction in Frequency-Dependent Feedback-Feedforward Amplifiers," International Journal of Electronics, 1985, Vol. 59, No. 6 , pp. 667-683.

[53] G.B. Yundt, "Series-Parallel Connected Composite Amplifiers," Master's thesis, Massachusetts Institute of Technology, March 1983.

The vita has been removed from the scanned document