CHAPTER II

PACKAGING OF METAL POST INTERCONNECTED PARALLEL PLATE STRUCTURE (MPIPPS) MODULES

Power Electronics Building Blocks (PEBBs) are envisioned as integrated power modules consisting of power semiconductor devices, power integrated circuits, sensors, and protection circuits for a wide range of power electronics applications, such as inverters for motor drives and converters for power processing equipment. Integration in power electronics is a rather complex process due to incompatibility of materials and processing methods used in fabrication, and due to the high energy levels these components must handle. Innovative 3-D integration technologies rather than planar integration approach must be developed in order to meet the system requirements. Packaging involves the solution of electrical, mechanical and thermal problems; it requires understanding at the molecular level not only of silicon but also of metals, ceramics, polymers and composites. As a result, packaging of PEBB requires a multidisciplinary effort, encompassing the areas of materials, power semiconductor devices, fabrication processes, circuits and control, magnetics, thermal design and analysis, packaging, computer aided design integration, manufacturing as well as application considerations.

This research is focused to design and fabricate a more reliable and high performance packaged PEBB module eliminating the usage of wire bond in the process. We have developed a low-cost approach, termed metal posts interconnected parallel plate structure (MPIPPS), for packaging high-performance modules of power electronics building blocks (PEBB). The new concept is based on the use of direct-bonding of copper posts, not wire-bonding of fine aluminum wires, to interconnect power devices as well as joining the different circuit planes together. This packaging approach requires less expensive equipment and has the potential to produce modules having superior electrical, thermal, and mechanical performance. We have demonstrated the feasibility of this approach by constructing PEBB modules (consisting of two IGBTs, two power diodes, and a few gate driver circuitry elements and passive components) which have been successfully tested at power levels over six kW.

2.1 INTRODUCTION

2.1.1 Converter Topology Selection

A review of high-power converter topologies shows two families of widely used phase leg structures[1]. One, as shown in Figure 2.1.1 (a), is the phase leg composed of two active switches and a diode anti-parallel with each of them. It can be used in AC/DC, DC/AC, and DC/DC converters, such as boost rectifier, voltage source inverter (VSI), and full/half-bridge converter. The other commonly used structure, shown in (b), is a phase leg that consists of two active switches with diodes in series with each of them. It can be configured as buck rectifier or current source inverter to perform AC/DC and DC/AC conversions. These two topologies can be called basic switching cells. These switching legs, together with driver circuits which can perform signal power amplification, level shift, isolation, protection and diagnostic functions, would make a switching cell that can perform as a generic computer-controlled power electronic building block. We chose a one-phase leg topology, shown as the shaded area in Figure 2.1.1(a), as the power stage of an elementary PEBB module. In order to reduce the stress imposed by the parasitic inductance outside the PEBB module, a clamping capacitor is used inside the package to absorb the possible *di/dt*. Meanwhile, integrated gate components, which can give better protection of the IGBTs, are also integrated into the package.

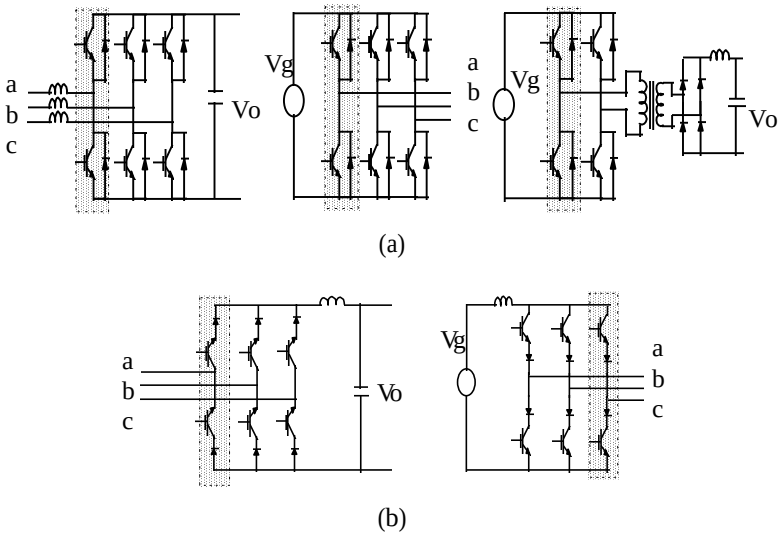


Figure 2.1.1. Converter topologies

2.1.2 Planar Wire-bonded Packaging vs. Three-Dimensional Multi-layer Packaging

From an electrical design point of view, traditional power modules are normally quite simple; however, these modules are often extremely difficult to fabricate due to high voltages and large currents, as well as thermal management considerations associated with the high power modules. Researchers at the Center for Power Electronics Systems have investigated the electrical parasitic effects associated with commercially available planar wire-bonded IGBT modules[1]. These results are used to compare conventional planar packaging with the new proposed technology of three-dimensional packaging. The basic concept of multi-layer package is to sandwich the semiconductor devices between a top and a bottom layers so that the interconnections between the devices go to a different plane, thus eliminating wire-bonds. Shown in Figure 2.1.2 are two planes of a proposed multilayer one-phase module with the IGBT rated 70A/1200V and the diode rated at 70A/1200V. The IGBTs and diodes are spread out in the bottom DBC substrate, completing the connections between the IGBT collector and diode cathode. The emitter and the anode connections are made through soldered metal interconnections. The passive components as well as a part of the driver circuitry are put on the patterned coppers in the top DBC layout. Finally, the top and bottom plates are attached to complete the module.

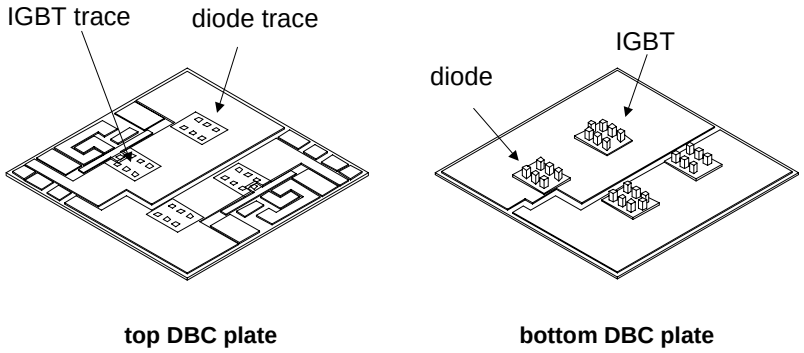


Figure 2.1.2. Top and bottom plates of a three-dimensional power module structure

Compared to the wire-bond packaging technique, a multi-layer packaging approach offers several advantages. Some of the key benefits of a multi-layer three-dimensional design over the conventional planar (wire-bond) design are summarized below[1,2,3,4].

- The substrate does not need to allocate the conductor traces for bonding wires; the whole real estate can be utilized efficiently at high power level.
- Both the bottom and top layers have a large copper layer serving as a ground plane, the mutual coupling effect will reduce the conductor trace inductance, thus reducing mutual inductance between the devices as well. Most importantly, the negative and positive terminal leads are located in different planes allowing the implementation of the laminated terminal design, which cannot be implemented in a wire-bond design. The laminated structure of a three-dimensional design would significantly reduce the termination inductance, which is a major concern in a wire-bond module.
- The wire-bond parasitic effects as well as mechanical stress and fatigue are removed.
- The closed packaging of gate passive components and capacitors will effectively protect the devices.
- Thermal management can be improved by using active cooling or double sided cooling.

Consequently, we can conclude that, in a packaging protocol for power electronics modules, a three dimensional structure would be significantly more efficient than the conventional planar wire-bond approach. However, in a three-dimensional packaging structure, device interconnects would also need to be realized in a vertical interconnection technique. Solder interconnects are specially suited for vertical interconnects, which has been widely used in IC packaging. In the following section, advantages of solder interconnection for three-dimensional packaging are described.

2.1.3 Advantages of Solder Interconnections over Wire-bonding

Currently, the commercially available, state-of-the-art wire bond module has reliability problems with a lifetime of only a few years[5]. A high power IGBT module (with 24 silicon devices) contains approximately 450 wires together with 900 wedge bonds[6]. For the longest time, reliability of chip and wire contact technology has been a concern. Wire detachment due to heel cracks, bond lift-offs, reconstruction of aluminum metallization on the chips and corrosion of wires are the major reliability limiting points of wirebond interconnection. Some of the more specific reliability problems associated with the wire-bond technology are listed below[1,5].

- The proximity effect (resulting from mutual coupling of bonding wires) affects the current distribution among the IGBT cells within one chip as well as among the paralleled chips. This imbalance will unevenly load the paralleled IGBTs with different fatigue mechanism, even though they are designed for identical operation.
- Magnetic field induced by the close-coupled bonding wires causes the problem of the device stress and bonding wire fatigue. The lateral mechanical force has a tendency to peel the aluminum coating off the silicon chip. In most cases, the IGBT chip surface tends to crack or the bonding wire opens after power cycling tests and thermal cyclings.
- Commercially available, state-of-the-art, wire-bond modules have large parasitic inductance associated mainly with the packaging of terminal leads. Since the bottom conductor pads have to accommodate both wire-bonds and terminal leads carrying a high current density, they occupy a large area of the module substrate (non-silicon area) contributing to parasitic inductance. As more IGBTs are paralleled, the inductance of the conductor pads becomes more dominant.

To mitigate these problems, power module manufacturers improved the composition of the wire, the shape of the bonding tool, the bonding parameters, the metallization on leads and the protective coatings rather than exploring alternative device interconnection schemes. Consequently, over the years, the research work on power electronics device interconnection have yielded limited success due to the inherent limitations of the wirebond technology.

On the other hand, in today's IC packaging industry, solder interconnections via solder bumping is a well-established technique. Compared to IC packaging, power electronics packaging is still at its infancy in terms of adopting novel interconnection schemes, which are considered state-of-the-art in the IC packaging industry. Power device manufacturers are making extremely slow progress in fabricating devices with

solderable contacts for commercial use. In the case of power electronics packaging, factors such as cost, manufacturability and reliability would primarily dictate a move toward implementation of solder interconnections, thus eliminating wire-bonded interconnects. However, in an ever-growing requirement on higher performance and denser packaging, the use of solder interconnections becomes inevitable. Motivations to use solder interconnects are multifaceted and well-researched and the technological, economic, and ergonomic features of direct solder interconnections are listed below[7]:

- Best performance in terms of speed, reduced inductance, improved power and ground distribution, enhanced signal propagation and noise isolation.
- Higher silicon integration with higher pad count per die through increased use of the die surface area.
- Increased wafer utilization. Integrated circuits specifically designed in area array for bump can result in smaller die size and consequently, more die per wafer.
- Retaining the same die footprint as the die shrinks.
- Wider pitches over the entire area of a die would offer cost and routing relief.
- Best ergonomics of size, weight, thickness, and consumer preferences.
- Creation of standardized footprints of the same die type from various suppliers.
- Enhanced machine utilization and throughput.

Advantages of solder interconnects over the other interconnection techniques are also evident from the following table where a few critical features of the most common interconnect technologies are compared[8].

Table 2.1.1. Comparison of common interconnection technologies[8]

Feature	Wirebond	TAB	Flip TAB	Flipchip Solder	Flipchip Adhesive
Maturity	Very Good	Good	Limited	Very Good	Improving
Die Availability	Very Good	Fair	Fair	Poor	Very Good
Edge Bond Pitch	4-7 mils	3-4 mils	3-4 mils	8-10 mils	8-10 mils
Max I/O	400-500	800-1000	800-1000	>1000	>1000
Footprint	20-100 mils	80-800 mils	80-100 mils	<20 mils	<30 mils
Assembly Rate	Slow	Good	Good	Good	Good
Repairability	Poor	Poor	Poor	Moderate	Moderate-Poor
Chip Bi/Test	Difficult	Good	Good	Improving	Improved
Cost	$0.001	$0.003-0.01	>$0.003	$0.002	$0.0001

Some of the unique advantages of solder interconnects over the wire-bond interconnections are summarized below[7,8].

- Solder interconnects allow a uniform and low inductance/resistance power feed across the face of the die, minimizes on-chip variation, which is a critical factor in wire-bonded device operation.
- Solder interconnects provide lower signal to power ratios than wire-bonds, resulting in lower inductance.
- Solder interconnects design allows placement of signal pads in very close proximity of the input/output pads rather than placing them on the peripherals, as in a wire-bond design.
- The cost of solder interconnection method is effectively the same with any change of patterns. However, in a wire-bond scheme, with reduced pitch size, the cost associated with assembly, yield and reliability would increase.
- Reliability of solder interconnects are well proven in industry. A conservative reliability estimate of solder bumps on a chip basis is less than 10 parts per billion per 1000 power on hours.
- Solder interconnects allow thermal management from both faces of a die, providing bi-directional heat dissipation paths.

Developed at IBM in the 1960's, C4 (controlled collapse chip connection) solder interconnects of devices have provided enhanced chip input/output density, uniform chip power distribution, improved cooling capability and high reliability. Solder interconnects have also resulted in increased packaging density, data bandwidths and operating frequencies while reducing system-level noise and other parasitics. Over the last few decades, C4 along with an extensive reliability database on solder fatigue and stress/strain relationship has allowed the packaging industry to develop new technologies such as Ball Grid Array (BGA) and Direct Chip Attach (DCA).

Raychem Corporation has introduced Chip Carrier Mounting Device (CCMD), which provides solder columns to surface mount the leadless ceramic chip carriers on to circuit boards[9]. The solder columns have a unique construction where solder is incorporated with a coil of flat copper wire. These columns can be of different heights for different applications; typically the height of the column varies from 0.05 to 0.1 inch with a typical diameter of 0.022 inch. The unique construction of the solder columns absorbs much of the stresses and strains generated in thermal cycling of the package. Numerous thermal and power cycling tests have been performed to prove the reliability of the CCMD structure.

Researchers at NTT Electrical Communications Laboratory have developed a flipchip interconnection using stacked solder bumps supported by polyimide films, which allowed improved reliability of large size chips[10]. As the solder bump equivalent height increases, shear strain decreases; furthermore, with an increased number of solder bump stacks, shear strain reduces even further. Thermal shock results indicate that the stacked solder have sixty times longer lifetime than the conventional un-stacked solder bumps. This interconnection technique can be applied to large size chips since the number of stacks can be easily increased. Moreover, various chips with different thermal expansion coefficients can be mounted on a single substrate, providing high terminal counts, self alignment during joining, high joint strength and excellent electrical properties at very high frequencies. In a stacked bump structure, as shown in Figure 2.1.3, the chip is joined with bumps supported by a polyimide film. Bump-limiting metal pads are used to separate solder bump at different levels. The ball limiting metallurgy consists of two copper layers sandwiching a titanium layer in between, which acts a diffusion barrier layer.

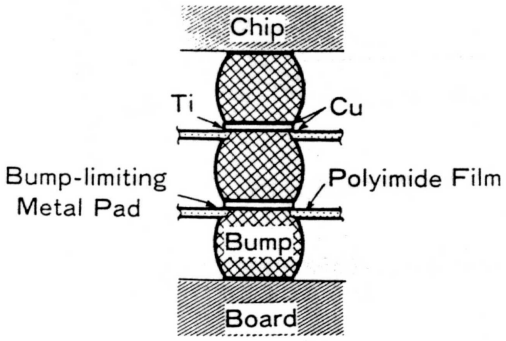


Figure 2.1.3. Stacked solder-bump interconnection[10]

A similar structure, known as Ceramic Column Grid Array (CCGA) was introduced by IBM several years ago[11]. The purpose of the Column Grid Array was to improve reliability of the device interconnections (as compared to Ball Grid Arrays) by adding height and compliance. These structures were typically attached to a ceramic substrate using no-clean flux and the columns could be reworked during module fabrication. Fatigue life modeling and thermal cycling tests were performed on these structures to prove their reliability.

Despite the well-established technology and multifaceted advantages of solder interconnections, power electronics industry is making extremely slow progress towards elimination of wirebonds and adaptation of solder interconnection schemes. In the following section, extents of the limited research to date on the alternative power electronics packaging by the power electronics industry are discussed.

2.1.4 Alternative Three-Dimensional Packaging Technologies of Power Modules

In the area of power electronics, several new technologies are under development by the module manufacturers[12,13,14]. New technologies that are under development to eliminate wire bonds typically employ spin-coating or tape-casting for laying down dielectric, dry or wet etching for opening up the contact pads and thin film deposition or plating for interconnecting devices. Other available techniques for device interconnections include gold stud-bumps and pressure contact assembly on the device pad[15,16,17]. General Electric researchers have developed the thin-film power overlay technology for packaging power devices; they use thin-film deposition followed by electroplating processes for device interconnections[13]. Recent power modules developed at Semikron contain spring-loaded metal strips that form electrical contacts on power devices by mechanical force[18]. Ferreira *et al.* proposed a packaging concept involving multiple layers of electromagnetic materials and switching function layers[19]. Linden *et al*. developed a power circuit substrate and packaging technology combining multichip module-laminated (MCM-L) technology with Insulated Metal Substrate (IMS) technology[20]. All of these technologies have yet to prove their manufacturability, reliability, and cost effectiveness.

2.1.4.1. GE's Power Overlay Technology

The Power Overlay (POL) Technology developed at General Electric Company is a high density interconnect (HDI) process for the interconnection of Multichip modules. This technology has an interconnect layer built on top of the semiconductor devices and baseplates. The schematic shown here illustrates the section view of the POL design concept.

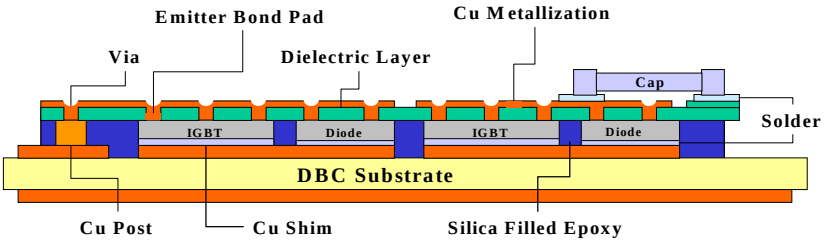


Figure 2.1.4. A cross-section schematic of a GE-POL structure[13]

Some of the anticipated advantages of the POL structure are described as follows:

- elimination of wire bonds with metallurgical interconnections improving reliability;
- better electrical performance through reduced interconnection parasitics;
- improved thermal performance via reduced numbers of thermal interfaces and two-sided heat removal;
- reduced profile and more flexible packaging options for stacking additional circuits;
- limited number of processing steps compared with other 3d packaging options; and
- low cost.

The POL process utilizes power semiconductor devices (IGBT, MOSFET, and diode) that are mounted to the backside of a Kapton™ tape using adhesive. The Kapton™ tape has pre-formed vias with specific pitch and size. These vias serve as electrical paths for circuit functioning. Metallization on the vias (making contact to the devices) and the polymer dielectric is achieved through a combination of sputtering and plating process[13,21,22]. First, a barrier and adhesion layer of Ti (typically 1000Å) is sputtered followed by a seed layer of copper (1000Å). On top of the seed copper layer, a five mil thick copper layer is deposited by electroplating. This thick copper layer provides a low-loss interconnection of the power devices. Finally, a thick photoresist is applied on the thick copper to pattern etch conductor pads on the electroplated metallization. DBC substrates are attached on the backside of devices through soldering. More layers can be built up repeatedly to realize a multilayered interconnect structure. Low profile passive components can also

be embedded into the overlay. The inherent multilayer nature of POL will facilitate the integration of gate drive and other circuits into a three-dimensional package.

However, GE-POL structure has not been successfully tested for high-power applications; furthermore, plated thick copper layers would most likely generate a significant amount of thermo-mechanical stress on the device interconnection joint, thus reducing reliability of the structure. Also rework on the module would be almost impossible since the entire structure is built on an additive process.

2.1.4.2. Pressure Contact Technology

Semikron's SKiiPPack module includes pressure contact design with a snap-on mounting configuration. Snap-on mounting contacts the PC board and mounts the heat spreader in a single manufacturing step[18]. As shown in Figure 2.1.5, a special spring with a C-shape in the middle provides the required pressure loading and also provides the electrical contact between the pc board and the internal contact to the DBC. The matrix of 40 to 60 spring-loaded contacts also provides distributed vertical pressure to press down the DBC evenly to the heat spreader. The spring contact material is a copper alloy with chromium, silicon and titanium, which provides good electrical conductivity, defined spring characteristics even after long-term temperature exposure and good manufacturability of the springs. Internal bus bar construction is supported by the plastic pressure spreader, which eliminates the need for additional mechanical support.

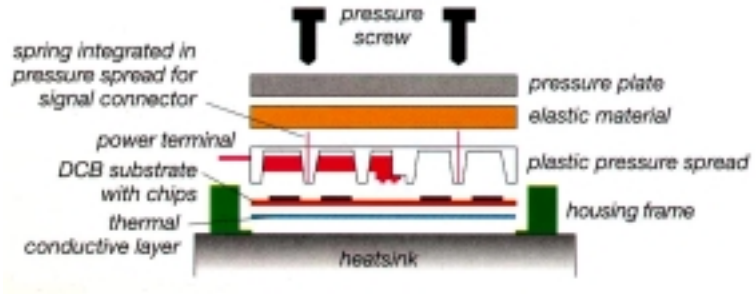


Figure 2.1.5. A cross-section view of Semikron's SkiiPPack with pressure contacts[18]

Despite the merits, the biggest disadvantage of pressure contact technology is its expensive manufacturing cost involved with precise machining and planarization, which may limit its usefulness. Also, limited research work has been published on the effects of thermo-mechanical stresses on these pressure contacts during actual operation of the devices and hence, the reliability of these modules is still under investigation.

2.1.4.3 Stud-Bump Technology

In a stud-bump bonding (SBB) approach as shown in Figure 2.1.6, gold bumps are formed on electrode pads by a wire-bonding machine. Bonded gold wire is cut-off by the capillary edge to form the tip on the upper surface of the bump. A flat surface is pressed against the Au bumps to level the bump height. The tips of the bumps are dipped in a layer of conductive adhesive. Next, the device with bumps and adhesive is flipped on to the circuit metallization and the epoxy is cured with a light pressure from the top. As a final step, an epoxy underfill material is inserted to fill the gap between the chip and the substrate. The underfill material is carefully selected to provide high structural stability and environmental protection. An SEM cross-section of the structure is shown in Figure 2.1.7. A slightly modified version of SBB technique uses solder as the attachment material replacing the conductive epoxy. This technique is very promising for low cost MCM-HDI applications because of its high stability and reparability[23,24]. Currently, at Matsushita, the SBB technique is widely used mount bare large-scale-integrated (LSI) chips directly on to glass ceramic and glass-epoxy organic substrates.

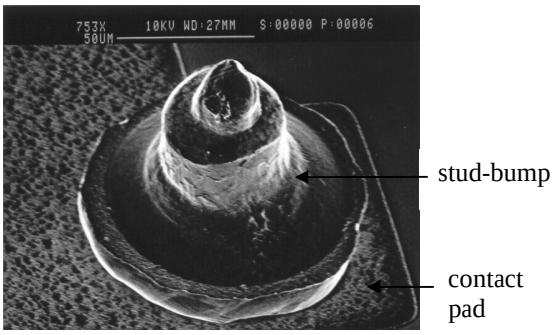


Figure 2.1.6. SEM image of a stud bump[15]

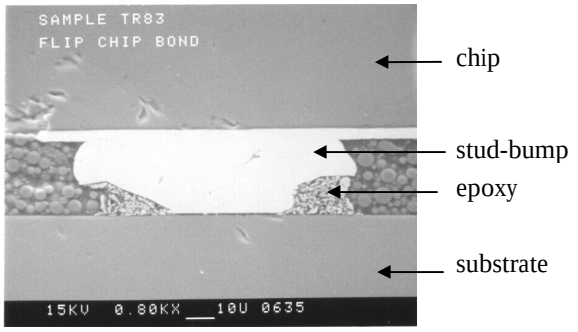


Figure 2.1.7. SEM image of a SBB cross-section[24]

To date, limited research has gone into implementing this technique on power devices. Conductive epoxies have shown extremely unreliable operation at high current and voltage levels[25]. Furthermore, as the bumps are produced on the contact pads, a significant amount of stress is exerted on the die, initiating microcracks, which may get more pronounced as the power devices get thinner.

2.1.4.4. Harris Thin Pack (HTP) Technology

Harris Semiconductor developed a novel packaging technique for power devices such as IGBTs and MCTs as a part of Navy's Power Electronic Building Block project[26]. The design includes a metallized (Ti-Ni on Al) device on top of which a machined ceramic (Al_2O_3 or AlN) with metallized grooves is attached. The top side of the ceramic piece is patterned with conductor metallization while the bottom side of the ceramic is metallized with a Ni followed by a flash gold coating. The grooves are filled with Pb-Sn solder paste, which is reflowed to connect the contact pads of the devices to the top metallization on the ceramic. A schematic of the HTP structure is shown in Figure 2.1.8, where the solder contacts for different terminals of the devices are achieved on the top and bottom sides of the device.

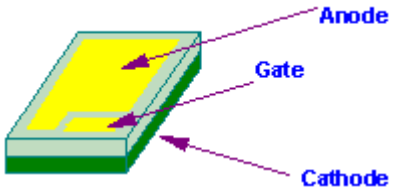


Figure 2.1.8. Schematic of a Harris Thin Pack with solderable contacts on both sides of the device[26]

Although the HTP technique was introduced a few years ago, to date, very little information is available about the reliability of the HTP lidded devices. Moreover, HTP devices have a low yield in the device fabrication as well as in the packaging protocol as reported by Harris.

All of the above-mentioned new technologies have yet to prove their manufacturability, reliability, and cost effectiveness. Some package designs are fundamentally limited in power due to poor thermal management, essentially containing one-dimensional heat flow path, while other designs may have reliability issues due to insufficient thermo-mechanical stress management. Most of these designs do not accommodate integration of passive components or driver circuitry within the module. Consequently, improved and low-cost three-dimensional integrated packaging technologies must be developed for power modules.

2.2 EXPERIMENTAL WORK

In designing a low-cost power electronic packaging structure, one must consider a few critical issues as listed below:

- requirement of solderable device
- reduced number of thermal/electrical interface
- low parasitic inductance
- good thermal performance
- high packaging density
- low inductance for capacitors
- low profile and small size
- hermetically sealed
- low cost
- manufacturability

All of the above mentioned features of a packaged module are extremely difficult to achieve under one packaging protocol. This situation is further aggravated by the fact that power electronics packaging has not kept pace with IC packaging. At the present time, in the area of power electronics module packaging, there are no preset standards. Chip and wire approach is still the state-of-the-art interconnection protocol. Power levels are now increasing, which in turn, is pushing the limit of existing planar packaging techniques.

2.2.1 MPIPPS Package Description

At the Center for Power Electronics Systems (CPES) at Virginia Tech, our goal is to design and implement a low-cost integrated power electronics module. MPIPPS is one of the primary candidate designs for a low cost packaging scheme. In this low-cost approach, metal posts are used for interconnecting devices as well as joining the different circuit planes together. We call this new concept -- Metal Post Interconnect Parallel Plate Structure (MPIPPS) as shown in Figure 2.2.1. This is a low cost approach for packaging high-performance modules of power electronics building blocks. The design concept is based on the use of direct bonding of copper posts, thus eliminating the use of wire bonds for power device interconnections.

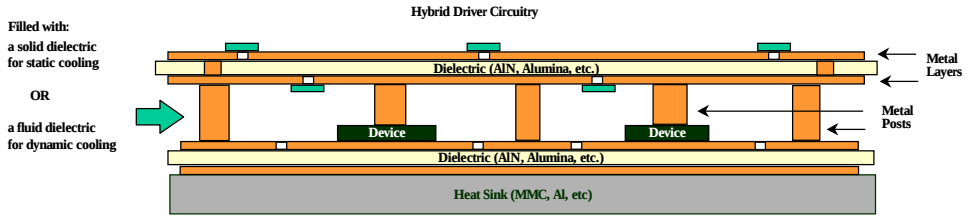


Figure 2.2.1. MPIPPS cross-section structure

This packaging approach offers several advantages:

- Ability to carry large currents with negligible parasitic inductance and capacitance because of short and thick metal posts that are used for the interconnections in the module;
- Better thermal management due to additional thermal paths offered by the posts and the option of dynamic cooling with the use of a dielectric fluid flowing directly through the devices in-between the plates;
- Ease of integration of passive components since multiple plates can be readily stacked on top of one another through metal posts; and
- Better reliability because of low thermal stresses with the use of identical plates for the circuit planes.

The power module has two layers of metallization with the devices sandwiched between the metallic layers. The bottom layer is an AlN-DBC with copper thickness of 10 mil. The copper layer is etched to a desired pattern where the IGBTs and diodes are attached by soldering. The copper posts, which have different sizes and heights for IGBT, diode, and top and bottom DBC plate connections, are soldered on top of devices and Cu metallization on AlN substrate. The top DBC plate is etched to a desired pattern and attached on to the copper posts of the bottom DBC plate to complete the electrical layout.

The feasibility of this packaging approach is demonstrated by constructing PEBB modules (in two different phases) consisting of two IGBTs, two power diodes a few gate driver circuit components. The first phase of the module fabrication is intended for evaluation of this packaging technique while the 2nd phase is focused towards fabrication of higher power modules with significant integration of gate driver circuitry. Figure 2.2.2 shows the schematic of the packaged circuitry in both phases of module fabrication.

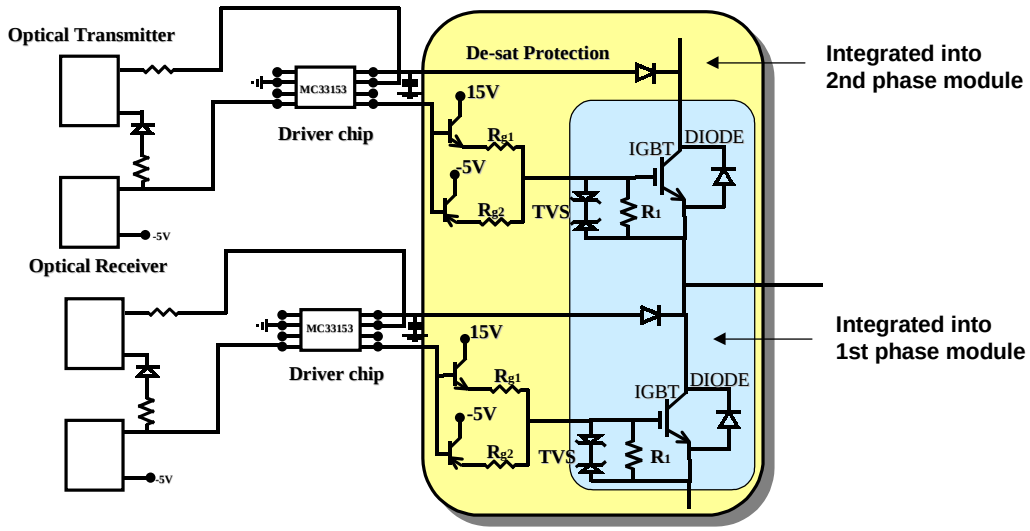


Figure 2.2.2. Proposed circuit diagrams for two phases of packaged module

The performance goals and the packaged power devices for the 1st phase MPIPPS modules are listed in Table 2.2.1. The 600V power devices (IXGD40N60A IGBT and C-DWEP55-06 diode), packaged in the first phase of module fabrication could be used for a 20kW power module with paralleling the devices, which would however, increase significant complexity in packaging. Consequently, in order to simplify the packaging process, we acquired higher power rated (1200V) devices (IGBT and diode) from IXYS.

Table 2.2.1. Performance goals and packaged components for 1st phase MPIPPS modules

Performance Goals and Components	**1st phase**	**2nd phase**
DC Bus	400 V	800 V
Single-phase power processing capability	3.3 kW	20 kW
Switching Frequency	20 kHz	20 kHz
IGBT (in die form) from IXYS	IXGD40N60A (600V/40A)	IXSD35N120A (1200V/70A)
Diode (in die form) from IXYS	C-DWEP55-06A (600V/50A)	C-DWEP69-12S (1200V/70A)

The fabrication procedures, theoretical modeling and experimental results on the fabricated MPIPPS modules are presented in the following sections.

2.2.2 Materials Research in MPIPPS Packaging

To eliminate wire bonds by using soldered post interconnects on the power devices (diodes and IGBTs) for enhanced electrical and thermal performances, we need to make the device contact pads solderable. Currently, the device manufacturers for IGBTs and diodes use aluminum contact pads, which are not solderable. As a result, we investigated thin film deposition of solderable films on the aluminum contact pads of the power devices. As represented in Figure 2.2.3, solder contacts provide a larger effective contact area between power semiconductor devices and overlying power metallization. The wide pitch of the device contact allows wider UBM (underbump metallalization) structures with taller solder interconnections. Taller bumps in the form of soldered posts would provide improved fatigue life. Solder joints would also provide tolerance for board flatness variation. Most importantly, large diameter bumps would enable handling of large currents and reduce electromigration[27]. The larger contact area greatly reduces current crowding and eliminates mechanical forces generated between wire bonds. This design also allows mechanical and thermo-mechanical forces to be distributed over a larger area, thus reducing equivalent mechanical stresses at the device connections.

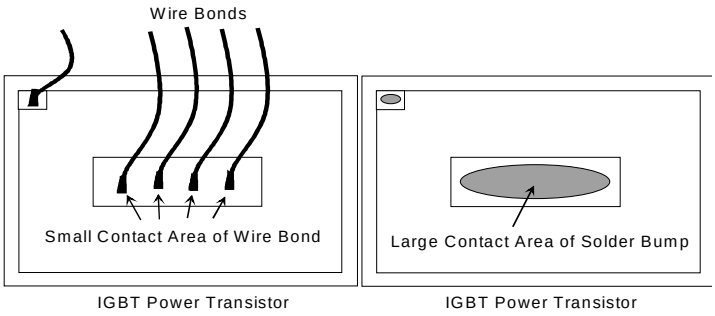


Figure 2.2.3. Comparison of contact geometries

Based on the availability and suitability of UBM processes, we have employed three different UBM schemes with two different types of deposition processes. First, we examined thin film deposition of Ti-Ni-Cu and Cr-Cu metal systems by a sputtering technique to make the contact pads of IGBTs and diodes solderable. Ti and Cr are used for the adhesion layer while Ni and a Cu thin film layers are deposited to make solderable contacts. The third UBM scheme includes an electroless deposition process of Zn-Ni-Au metallization on the device contact pads. Processing and characterization of the device interconnection scheme are discussed in detail in chapter 3.

One of the primary objectives of this research is to improve the thermal conductivity of power electronic packages. Our purpose in improving thermal performance is to reduce power device operating temperatures for a given power level. In this way, devices may be placed closer together (thus improving power density), thermal cycling fatigue should be reduced (by reducing the magnitude of temperature change), and thermal stresses should be reduced (by decreasing thermal expansion strain). In developing such a packaging and processing technology, various existing packaging technologies and substrate materials including metals, ceramics, tape ceramics, laminated to high-performance ceramics, copper-clad ceramics, metal matrix composites and other state of the art engineered materials have been thoroughly examined. Effects of interfaces and interlayers (based on the selected bonding techniques) on the properties of the assembled structure have also been studied for efficient packaging and are presented in chapter 4.

Hence, materials with excellent thermal conduction and CTE matched closely to the power devices are selected. The first selection for a high-performance ceramic substrate material is Aluminum Nitride (AlN). AlN exhibits a unique combination of thermal conductivity, electrical resistivity, thermal expansion and strength characteristics that match the needs for packaging, and cannot be achieved by either alumina (Al_2O_3) or beryllia (BeO). Compared to alumina, AlN has 10-15 times greater thermal conductivity, 50-75% greater bending strength and most importantly, a coefficient of thermal expansion close to silicon. Beryllia, on the other hand, possess more than half the thermal conductivity of copper and thus is used for applications demanding both thermal dissipation and electric isolation. However, BeO is brittle and is considered hazardous material to work with due to the toxic nature of BeO dust. AlN provides more than three times the bending strength of BeO, it can be sintered at a lower temperature and it is nontoxic. As a result, in the MPIPPS design, we have used commercially available Direct Bond Copper (DBC) on AlN substrates where 25 mil thick AlN is sandwiched between 10 mil thick Cu plates on both sides.

The other materials selection includes investigation of available metals, metallic alloys or metal matrix composites (MMCs) as heat sink, which will maximize heat removal, minimize thermal fatigue and improve reliability. We have paid special attention to composite materials with thermal conductivity and thermal coefficient of expansion matched to that of silicon. For example, copper or aluminum metal matrix composites, fabricated by reaction synthesis processes, have a great potential due to their high thermal conductivities (the processing techniques can produce clean, low thermal resistant matrix/dispersoid interfaces) and tailored thermal expansion coefficients. However, MMC heatspreaders are significantly more expensive than copper baseplate, and consequently, for a low-cost package design, we have selected thick copper baseplate as the heatspreader for MPIPPS modules.

2.2.3 Fabrication of MPIPPS Module

From the cross-sectional view of the MPIPPS module, shown in Figure 2.2.1, it is evident that the bonding techniques need to be optimized for joining different layers in the design. It is important for one to realize that joining of the components will inevitably generate interfaces and often interlayers between the different materials. Therefore, to assemble an efficient package, we have to consider the effects of interfaces and/or interlayers (depending on the technology used to bond the pieces) on the properties of the assembled structure.

Several soldering steps are required in the fabrication of the MPIPPS module. For the passive components and lead attachments on the DBC substrate, we used a 95%Pb-5%Sn solder. However, for the post attachment to the metallized contact pad on the device and module-substrate attachment to the copper heat spreader, we used Pb-Sn eutectic solder. It should be noted here that three different sizes of Cu posts are machined due to the differences in thickness of power devices and in the dimensions of the bonding pads of the devices. These different sized copper posts are used to attach the top and the bottom DBC AlN plates, diode and IGBT to the top plate. The processing steps and the issues, which we considered during each processing step in the fabrication protocol of an MPIPPS module are listed below in Table 2.2.2.

Table 2.2.2. Steps and issues of MPIPPS processing

Step Description	Issues
Step 1: Device sputtering for solderable metallization	availability of die from commercial manufacturers
	established UBM technology such as IBM-C4
	requires optimized deposition of UBM (adhesion, low stress, low resistance)
Step 2: Post attachment to sputtered devices	custom designed post adapter for easy device interconnection
	solder selection to reduce Cu-Sn intermetallics
	requires optimization of solder deposition and reflow parameters
Step 3: DBC substrate preparation	challenges of etching thin conductor widths and spacings on thick copper
	electrochemical etch can be used to prevent undercutting
Step 4: Die attach to DBC	selection of a solder with reduced fatigue characteristic at high temperature
	void-free solder attachment
	requires optimization of device spacings on the substrate
Step 5: Driver and passive components attachment	height of the components would dictate the module height
	spacings between low and high power components
Step 6: Top and bottom DBC attachment	alignment accuracy
Step 7: Heat spreader attachment to the module substrate	two attachment surfaces must be extremely clean and flat
	optimize the reflow process to minimize void content
	CTE mismatch between copper, DBC-AlN and silicon
Step 8: Silicone gel filling	bubble free encapsulation
Step 9: Case sealing	low curing temperature and high service temperature
	selection of epoxy with low curing temperature and high service temperature

Once the power module is completed, we integrate the gate driver circuit controller with the MPIPPS module. A double-sided printed-circuit board (consisting of the rest of the gate driver circuit and the connectors) is stacked on top of the MPIPPS module with through-hole connections between the top DBC plate and the PCB board. Figure 2.2.4 shows a few process steps of making a fully packaged MPIPPS module.

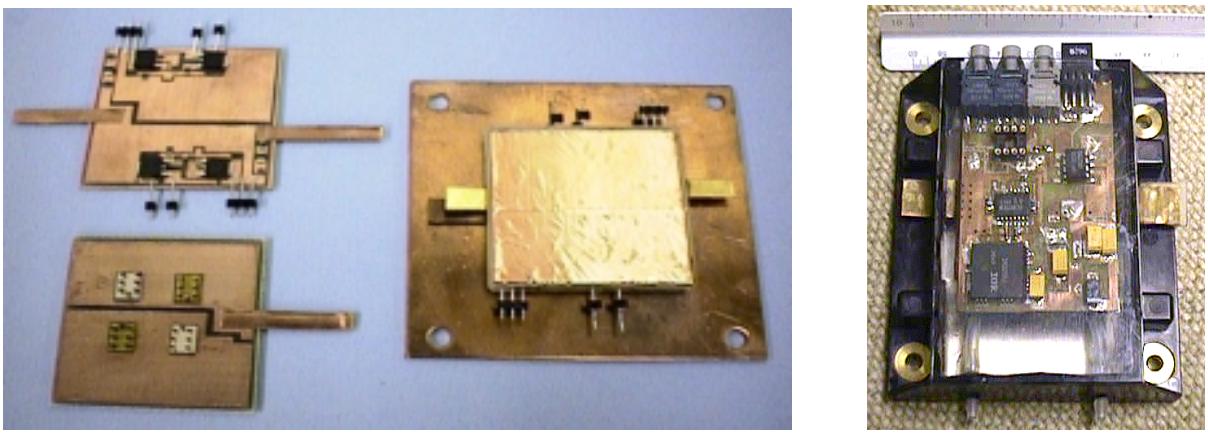


Figure 2.2.4. Processing steps of an MPIPPS module

2.3 TEST RESULTS ON THE PACKAGED MODULES

2.3.1 Parasitic Evaluation of an MPIPPS Module

Through parasitic inductance extraction and circuit simulation, package design is optimized. The bottom layer of the module and the device layout are shown in Figure 2.3.1. In this design, both the top layer and the bottom layer use the DBC material as the substrate, the "ground plane" effect is better utilized. The positive and negative terminals are introduced from the laminated layers. There is no space necessary for wire-bonds. Although the substrate area is not fully used in this design (for medium power application), there is no limiting factor in doing so for higher power applications with more power devices. The parasitic inductance in the power current path is greatly reduced, as shown in Figure 2.3.2.

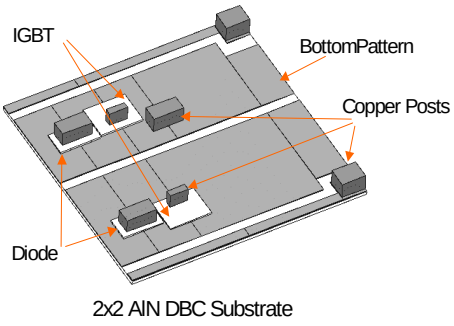


Figure 2.3.1. MPIPPS bottom layer with devices

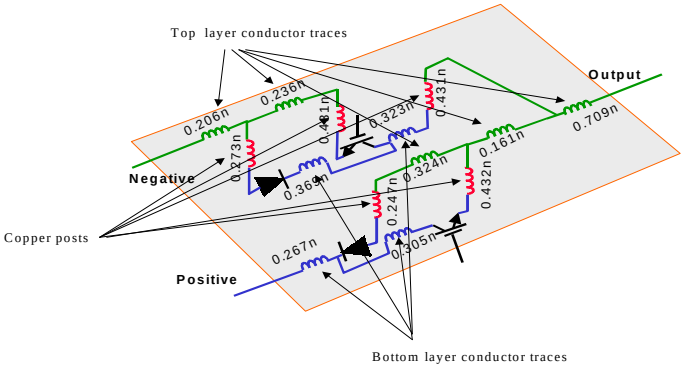


Figure 2.3.2. Parasitic inductance in an MPIPPS layout[1]

As mentioned before, a major goal of this research was to eliminate wire bond for power device (IGBT and diode) packaging. In the MPIPPS module, we have successfully eliminated the usage of wire bond and have implemented Cu post attachments to the bonding pads of the devices. From the circuit point of view, there are two major differences between the 3-dimensional MPIPPS design and the wire-bond design. The first difference is the termination inductance, which is ~30 nH for the wire-bond module compared to 8 nH for the multi-layer design. Since the terminals are placed in the same layer in a wire-bond design, it is difficult to make a lamination structure. The second difference is the mutual inductance between the devices. In a typical wire bond module, one bonding wire usually produces 6 to 16 nH inductance. Whereas, in the

MPIPPS module, one copper post (5 mm x 1.69 mm x 4 mm) generates only 1.27 nH inductance[28]. Although the bonding wires are parallel in the wire bond module, the equivalent inductance is still about twice the amount of inductance of the copper post. Moreover, the copper posts can be machined very precisely to maximize the usage of the solderable bonding area of the devices, thus resulting in further reduction of the overall inductance.

2.3.2 Thermal Test Results of the MPIPPS Module

In order to better understand the thermal spreading of the MPIPPS module in real operation, we have examined the following setup (Figure 2.3.3) with fine thermocouples inserted in different places of interest within the MPIPPS module and the heat sink. The thermocouples (TC) are attached with thermally conductive (electrically non-conductive) adhesive.

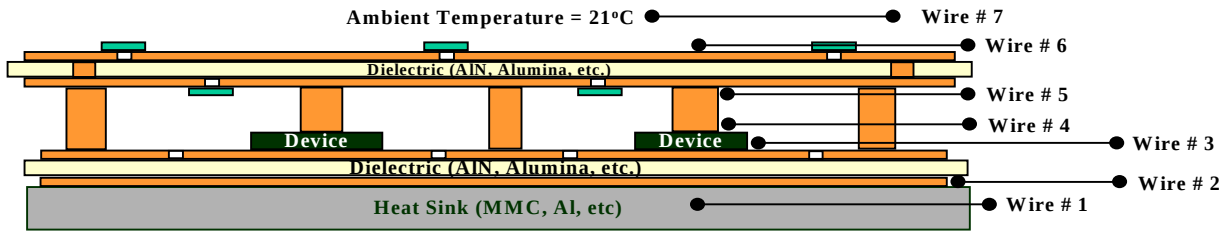


Figure 2.3.3. MPIPPS module with thermocouples attached for thermal testing

The objectives of the following preliminary thermal tests at different power levels with different cooling mechanisms are listed below[29].

- First, we powered up the MPIPPS module with a low power input to obtain a steady state junction temperature and to understand the transient and the steady-state thermal spreading through the parallel plate structure.
- Next, we increased the power level to a medium power input to obtain a correlation between the increased power and the increased junction temperature of the power device.
- Finally, we increased the power level of the module even further to a design specified operating range and checked to see if the device temperature was well within the safe operating temperature range specified by the manufacturer. Once the junction temperature reached steady state (within the safe operating limit of the device), we initiated a forced air cooling of the module while maintaining the same power level in order to simulate an actual operational condition of an MPIPPS module. In this case, the objective was to get a crude estimation of the junction temperature.

Accordingly, we started the experiment with an initial power input of 100 V and 5 A at 20 kHz to observe the temperature rise without any forced cooling mechanism. The time dependent temperature distribution of the module at this power rating is shown in Figure 2.3.4. Once the MPIPPS module is powered up, temperature readings are taken at every two minute interval until the peak temperature reaches steady state (~45 min). The power device i.e. the IGBT in operation exhibits the maximum temperature 55°C (wire 4). The temperature rise through the copper post (wire 5) is similar to that of the IGBT indicating an excellent spreading of heat from the source contact of the IGBT to the top DBC plate. Comparing the data from wires 1 (in the heat sink beneath the IGBT) and 6 (on top of the top DBC plate), we can see a uniform heat spreading in both upward and downward path from the IGBT. Lower temperature data are observed from wires 2 and 3 since these wires are laterally shifted from the heat spreading path of the IGBT. However, the ambient temperature (wire 7) stays constant at 21°C throughout the experiments and hence, it is not included in the plots.

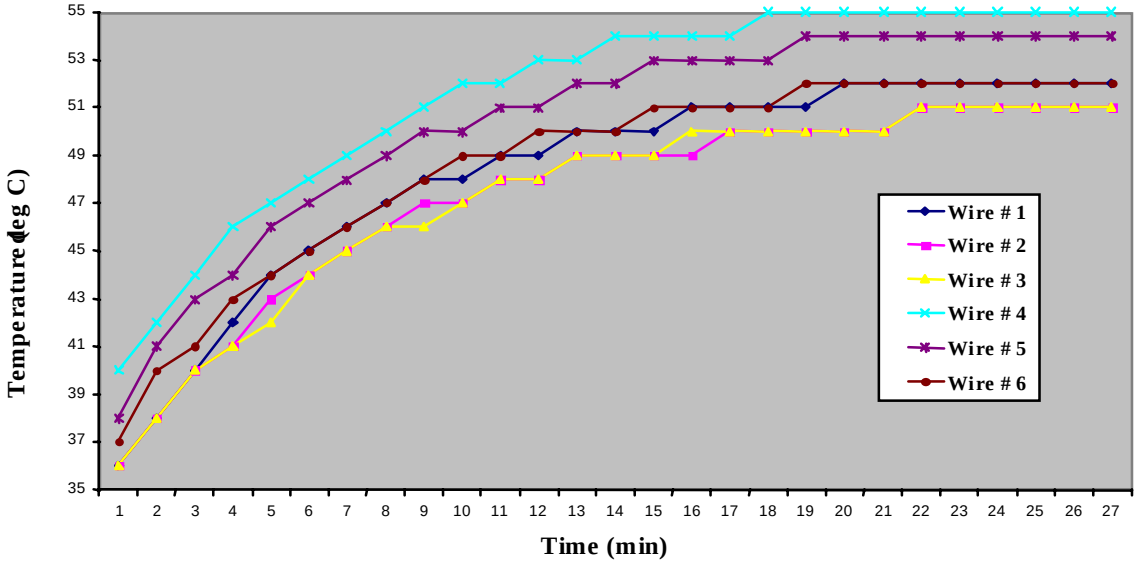


Figure 2.3.4. Time dependent temperature distribution of MPIPPS module
Power rating: 100V, 5A, 20kHz (natural convection air cooling)

Similar observations are made for the case when the power input of the MPIPPS module is increased to 150V and 9A at 20 kHz. The time dependent temperature distribution of the MPIPPS module at the elevated power level is plotted in Figure 2.3.5. The peak temperature of the IGBT (~74^{o}C) reaches steady state after ~55 minutes due to the increased input power level. Moreover, it is observed that a 50V increase in the input power level has resulted in a ~20^{o}C increase of the peak temperature of the IGBT from the previous case.

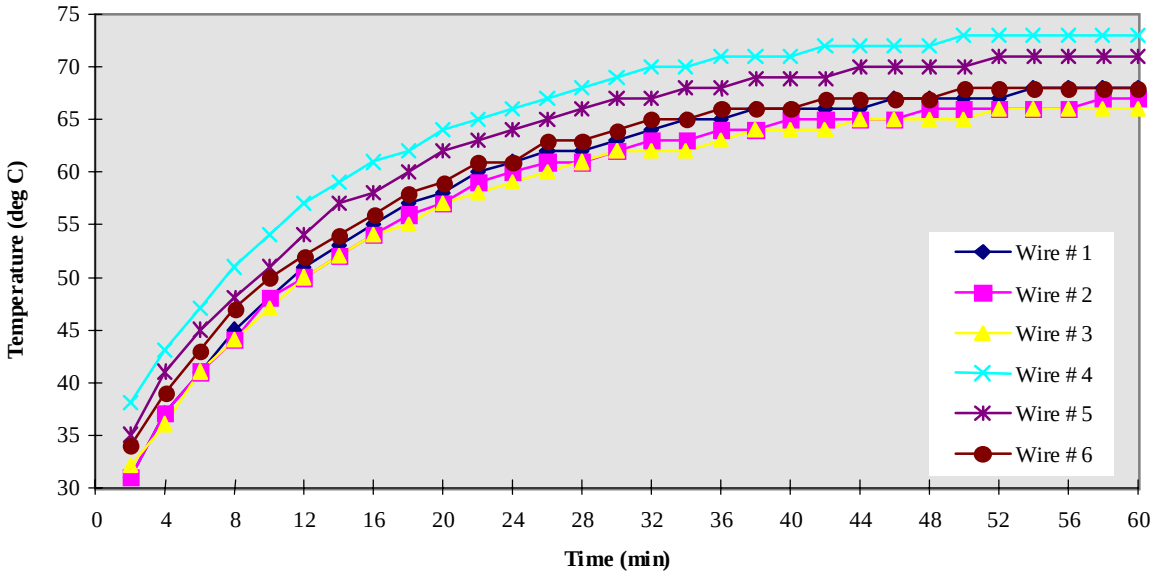


Figure 2.3.5. Time dependent temperature distribution of MPIPPS module
Power rating: 150V, 9A, 20kHz (natural convection air cooling)

As a final case, we increased the power rating of the module to 200V and 12A at 20 kHz, which increased the IGBT peak temperature to 100^{o}C and saturated after 55 minutes. After the 30th reading (60 minutes), we initiated an airflow with a fan through the experimental setup of the MPIPPS structure and continued with the temperature measurements at every two-minute interval. The temperature readings decreased very rapidly with the forced air cooling as shown in Figure 2.3.6.

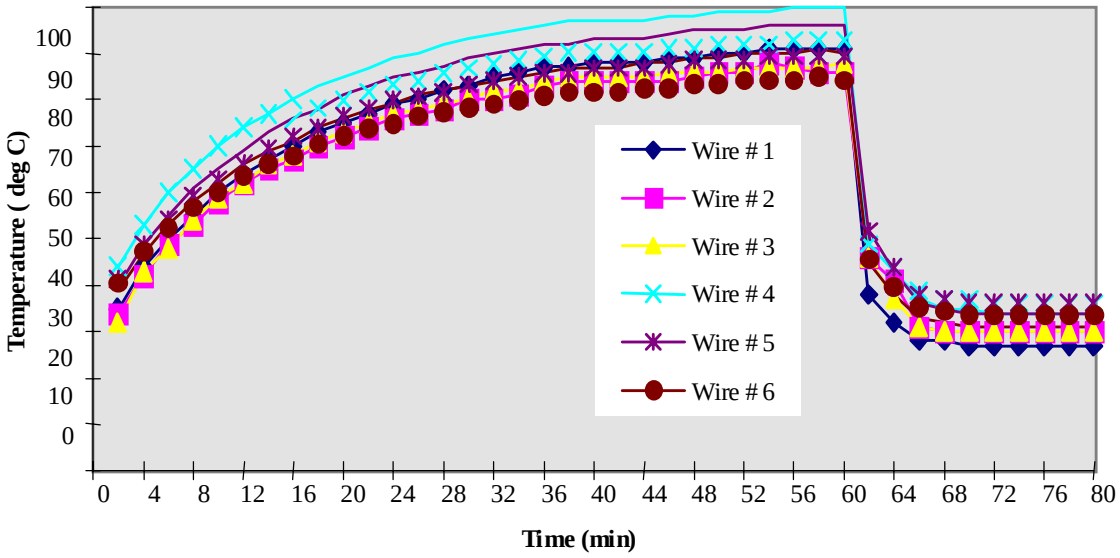


Figure 2.3.6. Time dependent temperature distribution of MPIPPS module
Power rating: 200V, 12A, 20kHz (convective air cooling)

The IGBT temperature reaches steady state at 34^{o}C within 10 minutes of the initiation of the air flow. During the natural convection air cooling period of this elevated power test, similar observations (as seen in the two previous power levels) are made for the thermal spreading throughout the MPIPPS module. Steady state temperatures during the forced air cooling period showed the same results as in the natural convection cooling period with one exception. In the case of forced air cooling, the thermocouple attached to the heat sink (wire 1) beneath the IGBT showed the lowest temperature since the forced air cooling through the fins of the aluminum heat sink keeps the heat sink colder than the surface of bottom DBC plate.

As it can be seen, the module temperature, especially the device temperature remained well within the safe operating temperature range of the targeted operating range. At the same time, an estimation of the amount of heat transfer through the post interconnections is achieved, which improved thermal management of the package structure. Presently, on-going research on thermal characterization of power modules is focused on high-power modules fabricated in the 2nd phase of the module fabrication scheme.

2.3.3 Power Stage Results

2.3.3.1 Test results of 1st Phase Modules

Fabricated PEBB modules are tested using both a curve-tracer and a real power stage units. A detailed description of the test procedure and the schematics of the test setup are presented below. Figure 2.3.7 (a) shows the test circuit setup for testing the low-side switch of the PEBB power module. The DC bus is supplied with an adjustable DC power supply. When the low-side switch, S1, is turned on and the high-side switch, S2, is turned off, the inductor, L (connected with the high-side switch) is charged by the DC power supply through the path of R, L, and S1, as shown in Figure 2.3.7 (b). After the low-side switch is turned off and the high-side switch is still off, the inductor is discharged through the path of R, L and D2, as shown in Figure 2.3.7 (c). The series resistor R limits the current flowing through the inductor. In this low-side switch test, the low-side IGBT, S1 carries the inductor charging current and the high-side anti-parallel diode, D2, carries the inductor discharging current.

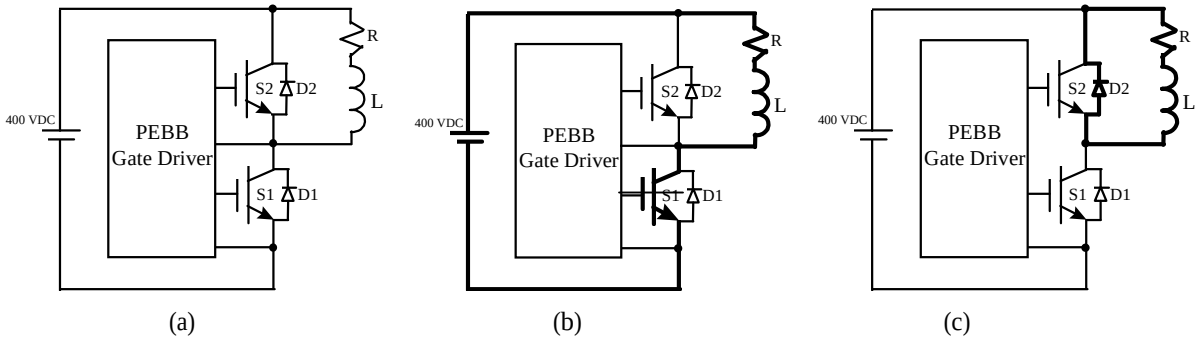


Figure 2.3.7 (a): Test Circuit for the Low-Side Switch Test; (b): Inductor Charging Path (thick line) of the Low-Side Switch Test; (c): Inductor Discharging Path (thick line) of the Low-Side Switch Test

Figure 2.3.8 shows the measured results of the low-side switch for an MPIPPS module driven by the PEBB gate driver with switching frequency, f_s=20 kHz. The upper waveform is the V_{ce} of the low-side IGBT and the lower waveform is the inductor current. The peak current of the inductor is 50 A. The average current through the inductor is 34.99 A. The average currents through the low-side IGBT and the high-side diode are 14.89 A and 20.1 A, respectively. The power handled by the low-side IGBT is 5.9 kW, which is significantly greater than our pre-set design goal of 3.3 kW (as described in Table 2.2.1 for the 1st phase of module fabrication).

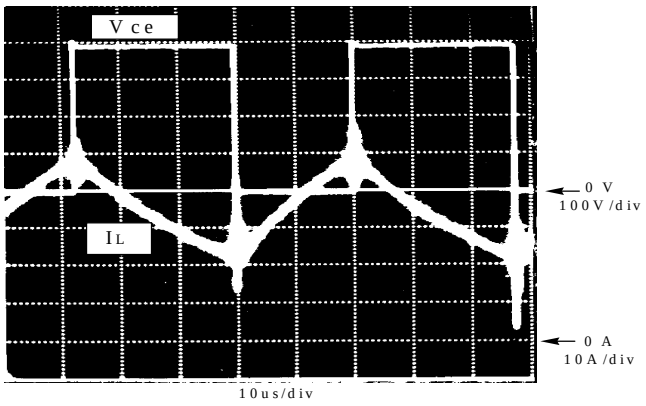


Figure 2.3.8. The measured results of the low-side IGBT in the MPIPPS module, f_s=20 kHz (Upper: V_{ce} Voltage Waveform of the Low-Side IGBT, Bottom: Inductor Current Waveform)

Figure 2.3.9 (a) shows the test circuit setup for testing the high-side switch of the PEBB power module. When the high-side switch, S2, is turned on and the low-side switch, S1, is turned off, the inductor, L, connected with the high-side switch, is charged by the DC power supply through the path of S2, R, and L, as shown in Figure 2.3.9 (b). After the low-side switch is turned off and the high-side switch is still off, the inductor is discharged through the path of D1, L, and R, as shown in Figure 2.3.9 (c). The series resistor, R, limits the current flowing through the inductor. In this high-side switch test, the high-side IGBT and S2, carries the inductor charging current and the low-side anti-parallel diode, D1, carries the inductor discharging current.

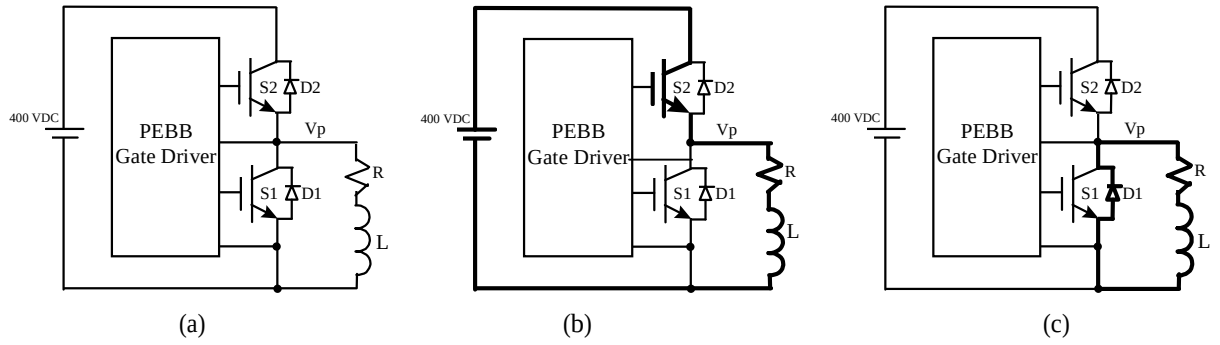


Figure 2.3.9 (a): Test Circuit for the High-Side Switch Test (b): Inductor Charging Path of the High-Side Switch Test (c): Inductor Discharging Path of the High-Side Switch Path

Figure 2.3.10 shows the measured results of the high-side switch for an MPIPPS module driven by the PEBB gate driver with switching frequency, f_s=20 kHz. The upper waveform is the V_p of the middle point at the IGBT half-bridge and the lower waveform is the inductor current waveform. The peak current of the inductor is 50 A. The average current through the inductor is 34.99 A. The average currents through the low-side IGBT and the high-side diode are 14.89 A and 20.1 A, respectively and the switching frequency is 20 kHz. The power handled by the high-side IGBT is 5.9 kW, which once again exceeds our design goal of 3.3 kW, as stated in Table 2.2.1.

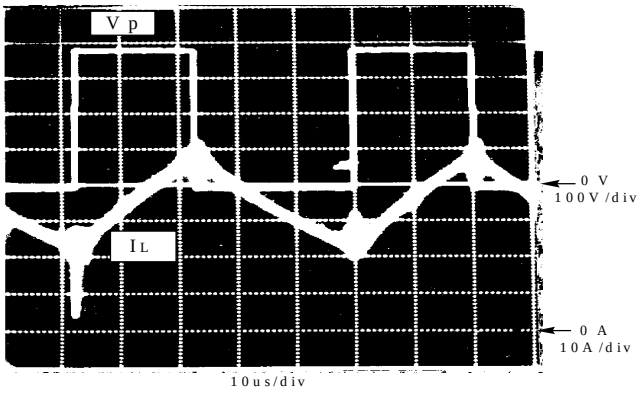
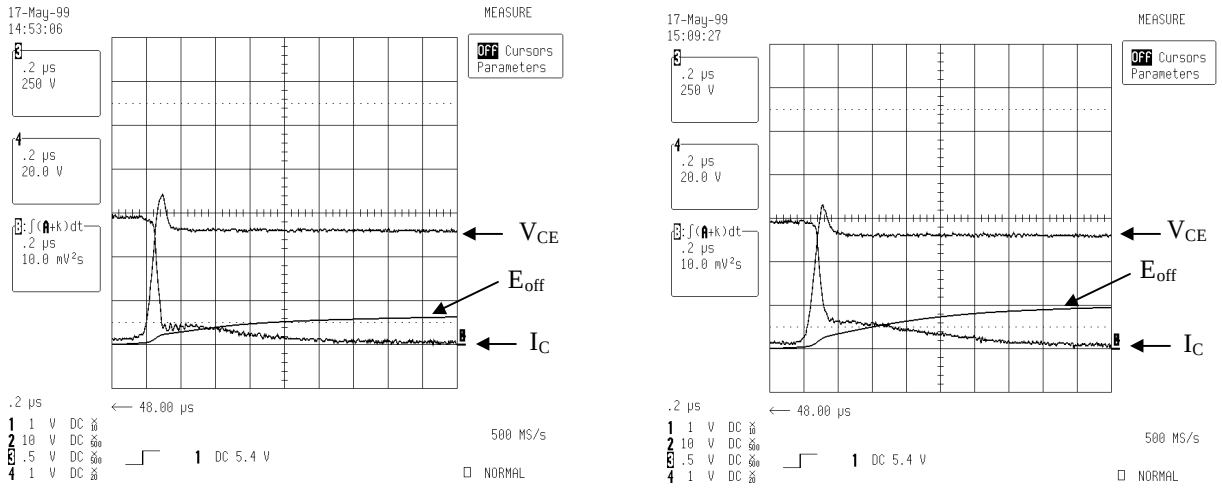


Figure 2.3.10. The measured results of the high-side IGBT in the MPIPPS module, f_s=20 kHz (Upper: V_p Voltage Waveform of the middle point at the IGBT half-bridge, Bottom: Inductor Current Waveform)

2.3.3.2 Test Results of 2nd Phase Modules

With the successful 1st phase prototype module fabrication and testing at ~6 kW, the research of module fabrication was continued for even higher power. However, with the new IGBTs (IXSD35N120A with polyimide passivation), unexpected difficulties with material processing were observed, which had incurred a very low yield in the packaging process. The development of solderable contacts on the 1200V IGBTs had been extremely slow and troublesome as compared to the similar work with IXGD40N60A devices.

In most cases, pulse test results on the metallized polymide passivated devices showed extremely inconsistent results, ranging from very low contact resistance to high contact resistance for the device interconnections. In some cases, sputtered IGBTs with an underbump metallurgy of Ti-Ni-Cu and Cr-Cu were packaged with solder interconnects and were tested (at room temperature and at 100°C) up to 780V and 55A in a pulse-switch tester. The turn-off characteristics of the packaged devices are shown in Figure 2.3.11.



(a) at 25°C (b) at 100°C

Figure 2.3.11. Pulse-test waveforms on packaged polyimide passivated 1200V devices

In most cases, the contact resistances were too high, therefore, the modules failed at high current and voltage levels. In other cases, the packaged devices failed even at low power levels at room temperature. Table 2.3.1 summarizes the sporadic results as observed during the pulse-switch test on the packaged devices with sputtered as well as electroless-deposited metallizations.

Table 2.3.1. Pulse-test results on packaged devices

Serial #	Metallization		Pulse-Test Results	
	Source	Gate	At 25°C	At 85°C
1	Ti-Ni-Cu	Ti-Ni-Cu	800V, 60A (pass)	800V, 60A (pass)
2	Ti-Ni-Cu	Ti-Ni-Cu	800V, 60A (pass)	800V, 60A (pass)
3	Ti-Ni-Cu	Ti-Ni-Cu	800V, 60A (pass)	800V, 60A (pass)
4	Ti-Ni-Cu	Al	200V (fail)	na
5	Zn-Ni-Au	Zn-Ni-Au	400V, 60A (pass)	300V
6	Zn-Ni-Au	Zn-Ni-Au	400V, 60A (pass)	400V
7	Ti-Ni-Cu	Ti-Ni-Cu	800V, 60A (pass)	800V, 60A (fail)
8	Ti-Ni-Cu	Ti-Ni-Cu	800V, 60A (fail)	na
9	Ti-Ni-Cu	Ti-Ni-Cu	550V (fail)	na
10	Zn-Ni-Au	Zn-Ni-Au	failed at processing	na
11	Ti-Ni-Cu	Al	300V (fail)	na
12	Ti-Ni-Cu	Al	failed at processing	na
13	Ti-Ni-Cu	Ti-Ni-Cu	500V (fail)	na
14	Ti-Ni-Cu	Ti-Ni-Cu	550V (fail)	na
15	Ti-Ni-Cu	Ti-Ni-Cu	550V (fail)	na
16	Ti-Ni-Cu	Al	400V (fail)	na
17	Ti-Ni-Cu	Ti-Ni-Cu	500V (fail)	na
18	Ti-Ni-Cu	Ti-Ni-Cu	800V, 60A (pass)	800V, 60A (fail)

A few packaged modules (which passed the pulse-switch stage) were tested at the high power stage along with commercial packages with same rated devices for comparison. The commercial modules were tested under four different input voltages -- 100V, 200V, 300V and 400V. The duty ratio was set at 0.6 for each testing, which lasted for 20 minutes, thus allowing the module under test to reach a thermal steady state. For the MPIPPS packaged module, the testing was successfully conducted up to an input voltage of 300 V

(applied voltage across the module during switching actions was 600 V). Beyond that range, the packaged module failed due to insufficient thermal management. Table 2.3.2 shows the high power testing results for commercial module MII 75-12 from IXYS (containing the same polyimide passivated 1200V devices) and the MPIPPS packaged module.

Table 2.3.2. Testing results for commercial and MPIPPS module

Parameters	**Commercial Module**				**MPIPPS Module**			
V_d (V)	100	200	300	400	100	200	300	400
I_{Lpeak} (A)	25.7	51.5	77.2	92.3	10.6	20.6	31	na
$I_{L\ rms}$ (A)	9.8	20.9	32	38.2	5.7	11.1	16.5	na
T_{room} (^oC)	24.1	24.1	24.1	24.1	25.2	25.2	25.2	na

At this point, it is realized that there must be some inherent differences between the devices (Si_3N_4 passivated and polyimide passivated) used in the 1st phase and 2nd phase of module fabrication, resulting in different device contact resistances under the same metallization schemes. A thorough characterization of the metallization process as well as the device interconnection interface is extremely crucial to understand the observed differences between these two types of devices. Consequently, in the next chapter, evaluations and characterizations of the metallization process and the device interconnection interface are described.

2.4 SUMMARY

This chapter documents the accomplishments on the development of an innovative technology for packaging power electronics building blocks (PEBBs). To define the structure and devices to be used in generic PEBB design, several power stage topologies were considered. A phase leg design was performed and appropriate gate driver configurations were investigated. These configurations were modeled to demonstrate their applicability for PEBB use. Consequently, an innovative packaging technique was developed and investigated as an alternative to the conventional designs. This new packaging technique, the metal post interconnected parallel plate structure (MPIPPS) uses copper posts to replace wire bonds and allows the incorporation of active cooling directly on the power devices. Some of the advantages of this three-dimensional packaging approach can be summarized as follows:

- The substrate does not need to allocate the conductor traces for bonding wires; the whole real estate can be utilized efficiently at high power level.
- The negative and positive terminal leads are located in different planes allowing the implementation of the laminated terminal design, which cannot be implemented in a wire-bond design. The laminated structure of a three-dimensional design would significantly reduce the termination inductance, which is a major concern in a wire-bond module.
- Thermal management can be improved by using active cooling or double sided cooling.

Eliminating wire bonds required the development of a solderable interface on the emitter contact and gate contact of the IGBTs and on the anode of the diodes used in the power stage circuit. Thermal and electrical test results of the prototype modules (implemented as an inverter phase leg in the first phase of the module fabrication scheme with Si_3N_4 passivated IGBTs) support the improved electrical performance of this new packaging technique. However, in the 2nd phase of the module fabrication, we encountered significant yield issues related to materials processing of the polyimide passivated polyimide passivated IGBTs, which is discussed in the next chapter.

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