5-6 GHz RFIC Front-End Components in Silicon Germanium HBT Technology

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(ABSTRACT)

In 1997 the Federal Communications Commission (FCC) released 300 MHz of spectrum between 5-6 GHz designated the Unlicensed National Information Infrastructure (U-NII) band. The intention of the FCC was to provide an unlicensed band of frequencies that would enable high-speed wireless local area networks (WLANs) and facilitate wireless access to the national information infrastructure with minimal interference to other devices. Currently, there is a lack of cost-effective technologies for developing U-NII band components. With the commercial market placing emphasis on low-cost, low-power, and highly-integrated implementations of RF circuitry, alternatives to the large and expensive distributed element components historically used at these frequencies are needed. Silicon Germanium (SiGe) BiCMOS technology represents one possible solution to this problem. The SiGe BiCMOS process has the potential for low cost since it leverages mature Si process technologies and can use existing Si fabrication infrastructure. In addition, SiGe BiCMOS processes offer excellent high frequency performance through the use of SiGe heterojunction bipolar transistors (HBTs), while coexisting Si CMOS offers compatibility with digital circuitry for high-level "system-on-a-chip" integration.

The work presented in this thesis focuses on the development of a SiGe RFIC front-end for operation in the U-NII bands. Specifically, three variants of a packaged low noise amplifier (LNA) and a packaged active x2 sub-harmonic mixer (SHM) have been designed, simulated and measured. The fabrication of the RFICs was through the IBM SiGe foundry; the packaging was performed by RF Microdevices. The mixer and LNA designs were fabricated on separate die, packaged individually, and on-chip matched to a 50 Ω system so they could be fully characterized. Measurements were facilitated in a coaxial system using standard FR4 printed circuit boards.

The LNA designs use a single-stage, cascoded topology. The input ports are impedance matched using inductive emitter degeneration through bondwires to ground. One

version of the LNA uses a shunt inductor/series capacitor output match while the other two variation use a series inductor output match. Gain, isolation, match, linearity and noise figure (NF) were used to characterize the performance of the LNAs in the 5 - 6 GHz frequency band. The best LNA design has a maximum gain of 9 dB, an input VSWR between 1.6:1 and 2:1, an output match between 1.7:1 and 3.6:1, a NF better than 3.9 dB and an input intercept point (IIP3) greater than 5.4 dBm. The LNA operates from a 3.3 V supply voltage and consumes 4 mA of current.

The SHM is an *active*, double-balanced mixer that achieves x2 sub-harmonic mixing through two quadrature (I/Q) driven, stacked Gilbert-cell switching stages. Single-ended-to-differential conversion, buffering and I/Q phase separation of the LO signal are integrated on-chip. Measurements were preformed to find the optimal operating range for the mixer, and the mixer was characterized under these conditions. It was found that the optimal performance of the mixer occurs at an IF of 250-450 MHz and an LO power of -5 dBm. Under these conditions, the mixer has a measured conversion gain of 9.3 dB, a P_{1-dB} of -15.7 dBm and an 2LO/RF isolation greater than 35 dB at 5.25 GHz. At 5.775 GHz, the conversion gain is 7.7 dB, the P_{1-dB} is -15.0 dBm, and the isolation is greater than 35 dB. The mixer core consumes 9.5 mA from a 5.0 V supply voltage.

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Chapter 1

Introduction

In the last few years, clear unlicensed frequency spectrum for RF applications has become a rare commodity. The explosion of wireless products including cordless phones, wireless local area networking (WLAN) products, Bluetooth and similar technologies has produced a large demand for unlicensed spectrum. Until recently, there were only a few bands available for unlicensed products. The most common bands were, and still, are the 900 MHz and 2.4 GHz Industrial, Scientific and Medical (ISM) bands. While these bands have great potential, and have been used extensively in various applications, they suffer from several drawbacks which have begun to limit their use for emerging applications. The ISM bands have recently become quite congested, increasing the potential for interference. In addition, their limited available bandwidth has restricted their use in wideband applications such as high speed data communications. Recognizing the problem, the FCC created the Unlicensed National Information Infrastructure bands (U-NII). The intention of the FCC was to provide a band of frequencies that would enable high-speed WLANs and facilitate wireless access to the national information infrastructure with a minimum interference to other devices [1].

Currently, there is a lack of cost-effective technologies for developing U-NII band components [2]. With the commercial market placing emphasis on low-cost, low-power, and highly-integrated implementations of RF circuitry, alternatives to the large and expensive distributed element components historically used at these frequencies are needed. Silicon Germanium (SiGe) BiCMOS technology represents one possible so-

lution to this problem. The SiGe BiCMOS process has the potential to be low-cost since it leverages mature Si process technologies and can use existing Si fabrication infrastructure. In addition, SiGe BiCMOS processes offer excellent high-frequency performance through the use of SiGe heterojunction bipolar transistors (HBTs), while coexisting Si CMOS offers compatibility with digital circuitry for high-level "system-on-a-chip" integration.

In the next few sections, overviews of the U-NII band and SiGe technology as well as a brief discussion on packaging will be presented. The objectives of this research project and an overview of the thesis will also be discussed.

1.1 The U-NII Band

In 1997 the Federal Communications Commission (FCC) released 300 MHz of spectrum designated the U-NII band for unlicensed use. The band is composed of three separate frequency sections at 5.15-5.25 GHz, 5.25-5.35 GHz, and 5.725-5.825 GHz. The 5.15 - 5.25 GHz portion of the U-NII band is restricted to indoor applications. A 200 mW Effective Isotropic Radiated Power (EIRP) limit is placed on all transmitting devices to prevent interference with other services operating within the same band, specifically mobile service feeder links. The second band at 5.25 - 5.35 GHz has a maximum transmit power limit of 1 W EIRP, allowing systems operating in this band to transmit at distances on the order of a mile, and possibly even more depending on data rate and location.. Finally, the 5.725 - 5.825 GHz band, with a maximum transmit power of 4 W EIRP and a directional antenna gain of up to 23 dBi, is ideal for point-to-point applications.

When the FCC placed the limitations on these bands, it did so based upon the envisioned uses. The lower band, with the restriction of indoor use only, is intended for indoor WLANs. With a maximum EIRP of 200 mW, it has a range of a only few hundred meters and works well for interconnecting computers within the same office. The middle band's maximum transmit power allows it to operate well as a means of connecting small campuses or neighborhoods. The FCC also realized the importance of making the middle band compatible with the European HIPERLAN system and thus ensured that the power limit and spectral bandwidths of the two bands were

Table 1.1: Overview of the U-NII band.

	Lower Band	Middle Band	Upper Band
Freq (GHz)	5.15-5.25	5.25-5.35	5.725-5.825
Max EIRP	200 mW	1 W	4 W
Antenna Gain	6 dBi	6 dBi	6 dBi/23 dBi
Typical Range	Interior building	Small neighborhood	6-mile radius

compatible. The upper band, with a maximum EIRP of 4 W and higher allowed antenna gain, is capable of transmitting over greater distances. The upper band was designed to be well suited for network backbones, T1+ replacements, and microwave point-to-point links.

Table 1.1 summarizes the spectrum set forth by the FCC. Further history and explanation of the U-NII band is found in Appendix A.

1.2 SiGe Technology

1.2.1 SiGe HBT

In the past, high-frequency, high-performance RFICs have been fabricated predominately in III-V technologies. However, with the commercial industry now designing products operating at higher frequencies previously dominated by military applications, the need for a high-performance technology which exhibits lower cost and higher levels of integration has arisen. These constraints would tend to support a Si BiCMOS based process – one solution which has gained momentum is SiGe BiCMOS. What make SiGe BiCMOS so attractive compared to a standard Si BiCMOS process is the ability to "band-gap" engineer Silicon. The addition of Ge to Si forms a $Si_{1-x}Ge_x$ alloy with a narrower band-gap than Si, allowing the formation of a SiGe heterojunction bipolar transistor (HBT). SiGe HBTs have better RF performance than standard Si bipolar junction transistors (BJTs), making them attractive for higher frequency design.

In a standard homojunction BJT, the collector, base and emitter are fabricated from the same material with identical band-gaps. Hole back-injection across the emitter-

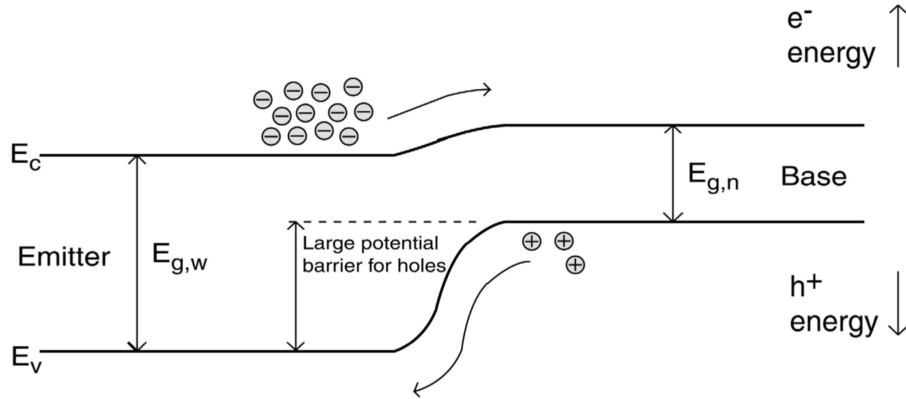


Figure 1.1: Energy band diagram illustrating the large potential barrier in the valence band created by a heterojunction. The barrier reduces the amount of hole back-injection from base to emitter.

base junction limits the beta (current gain) of the device and the base doping concentration. High beta is critical for high power gain; a heavily doped base is important for several reasons. Heavy doping lowers the resistance of the base and thus the noise of the transistor. It also increases the base punch-through breakdown voltage allowing the transistor to have a thinner base for a given breakdown voltage. Monolithic bipolar devices are vertical structures; therefore, reducing base layer thickness is critical for reducing the base transit time of the minority carriers, which directly relates to the high frequency performance (speed) of the transistor.

In a conventional HBT technology such as Gallium Arsenide/Aluminum Gallium Arsenide (GaAs/AlGaAs), the *emitter* of the transistor is band-gap engineered to have a wider band-gap than the base. This forms a heterojunction at the base-emitter junction and creates a discontinuity in the band structure. This discontinuity creates a potential barrier for the holes, limiting the hole back-injection across the emitter-base junction (Fig. 1.1). Thus the beta of the device is increased, and the base can be heavily doped and very thin.

SiGe HBTs are similar to conventional HBTs with several important advantages. A SiGe HBT uses a Si emitter and collector with a band-gap engineered SiGe base. The concentration of Ge can be varied throughout the base to create a band-gap gradient (Fig. 1.2). This creates a drift field and accelerates the minority carriers across the base reducing base transit time.

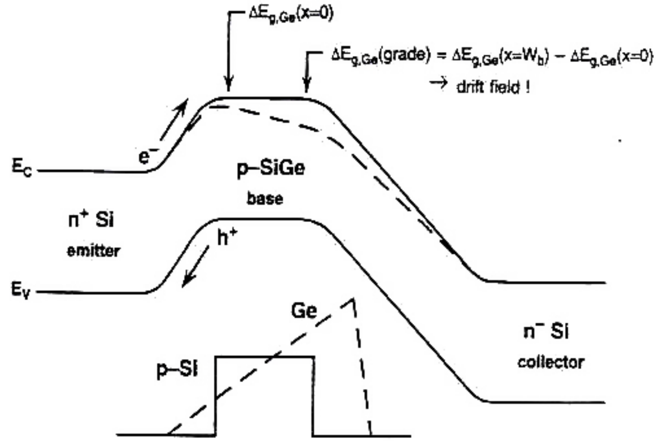


Figure 1.2: Energy band diagram of a graded-base SiGe HBT compared to a conventional Si BJT. The graded Ge concentration in the base of the SiGe induces a drift field from emitter to collector [3].

In addition, while the materials used in a conventional HBT are lattice matched, the Si/SiGe interface is not. Although this mismatch can cause problems in growing defect-free heterojuctions, the strain also favorably influences the band structure. When SiGe is grown on a Si substrate, the strain places the majority of the band-gap difference in the valence band offset. This increases the potential barrier for the hole back-injection, resulting in a more ideal HBT [4].

Lastly, the SiGe HBTs can be fabricated to be compatible with Si CMOS. This adds the advantage of high levels of integration with digital CMOS. However, the added integration does not come without its disadvantages. In a SiGe HBT only process, the collector, base and emitter can be grown epitaxially for high performance, defect-free layers. However, in a standard SiGe BiCMOS process, the long thermal cycling required for CMOS fabrication prevents the use of an epitaxial collector in the HBTs, leading to a structure similar to that in Figure 1.3. In this case, the collector of the HBT is ion implanted and the base and emitter are grown epitaxially. The long thermal cycling for the CMOS also increases the diffusion of the dopants in the base, emitter, and collector of the HBT making it appear more like a conventional ion-implanted base Si BJT [3]. Thus, in a SiGe BiCMOS process, the base thickness and doping can not be as well controlled as in an pure HBT process.

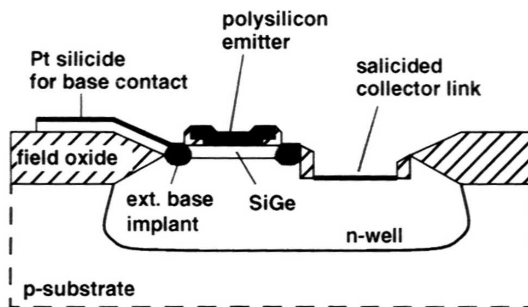


Figure 1.3: A standard SiGe HBT [5].

Another major drawback of SiGe BiCMOS is the low resistivity Si substrate which is several orders of magnitude lower than competing III-V materials such as GaAs. If the technology was based on HBTs only, a high-resistivity substrate could be used. However, a conductive Si substrate is desired to prevent latch-up in the coexisting CMOS devices. The low resistivity makes integrated passive devices more lossy and increases the parasitics to the substrate [6]. Inductors are especially affected by the substrate, with quality factors (Q) on the order of 5-15 for SiGe (in comparison to 15-20 for GaAs). Furthermore, the poor substrate lowers the maximum stable gain (MSG) of circuitry through increased feedback and increases parallel coupling paths between devices and RF sections [7]. Reducing the effect of lossy Si substrates has been an on going topic of research and many solutions have been proposed [8],[9],[10].

1.2.2 The IBM SiGe Process

The process used in this thesis is IBM's 5hp technology which is a three metal layer (Al) UHV/CVD Si/SiGe BiCMOS process on 200 mm wafers. The technology features a high-performance SiGe HBT with an f_t of 45 GHz and f_{max} as high as 65 GHz. A high-breakdown version of the HBT is also available with a BV_{CBO} of 14.4 V. In addition, the 5hp process offers 3.3 V CMOS ASIC-compatible devices.

The SiGe BiCMOS technology includes a wide range of passive and active device including standard and high-breakdown HBTs, high-Q metal-insulator-metal (MIM) and high-density poly-dielectric-metal capacitors (DCAP), diffusion and polysilicon

Table 1.2: Characteristics of devices in IBM's SiGe BiCMOS Technology.

Device	Characteristics
Standard NPN SiGe HBT	$f_t/f_{\max}$=47/65 GHz at BV_{CBO}=10.5 V
High-breakdown NPN SiGe HBT	$f_t/f_{\max}$= 25/55 GHz at BV_{CBO}=14.4 V
Si NFET	L_{eff} =0.39 μm, G_{msat}=195 μS/μm
Si PFET	L_{eff} =0.38 μm, G_{msat}=103 μS/μm
Schottky Diode	V_f=0.31 V
Varactor	C_J = 1.2 fF/μm^2
DCAP	C=1.5 fF/μm^2
MIM Capacitor	C=0.7 fF/μm^2
Inductor	L=1 nH, Q=17@5 GHz
PolySi Resistor	R_s = 220 $\Omega/\square$

resistors, varactors, Schottky diodes, and inductors. Table 1.2 shows the characteristics of the key active and passive devices within the IBM SiGe process [11].

Unlike modern submicron CMOS substrates processes which have substrate resistivities on the order of 0.01 $\Omega{\cdot}cm$, the IBM SiGe BiCMOS process uses a bipolar substrate with resistivity in the range of 10 - 20 $\Omega \cdot cm$, which helps reduce substrate effects. With stricter design rules, latch-up can still be avoided for the CMOS devices.

In addition to the higher resistivity substrate, deep trench isolation and n+ salicide are used to reduce substrate problems. Deep trenches etched into the substrate provide high resistance barriers in the lossy substrate, preventing strong coupling between elements. The n+ salicide works in an opposite fashion. The heavily-doped salicide is more conductive than the substrate, and is placed between a device (e.g. a bondpad) and the substrate. Instead of a device coupling through the substrate, the signal is diverted through the salicide, usually to ground. An illustration of deep trench and n+ salicide isolation is shown in Figure 1.4.

IBM supplies a design kit to licensees of their process. The design kit includes all the necessary elements for each step of the design process. Simulation models, layout artwork, and decks for design rule checks (DRC) and layout versus schematic (LVS) checks are included in the kit. In addition, the kit includes fully modeled and characterized active and passive devices including several variations of resistors, capacitors, inductors, and bondpads. For example, included in the kit are various

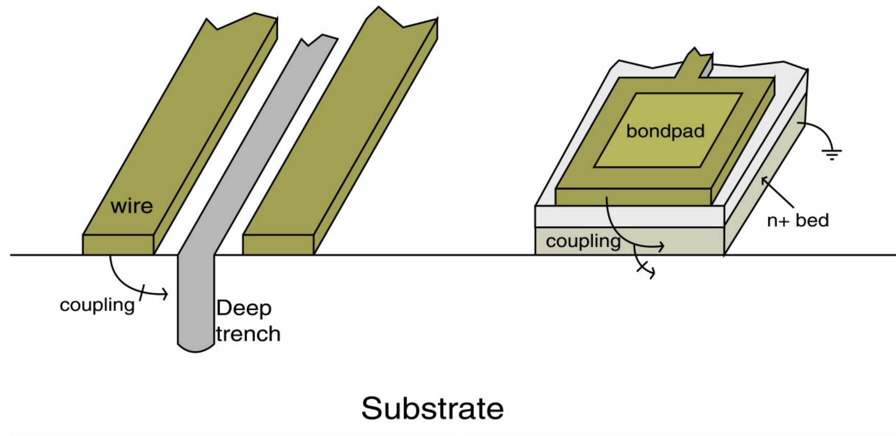


Figure 1.4: Conceptual drawing illustrating how deep trench isolololation and n+ salicide reduce substrate coupling problems (non-relevant process layers are not shown). Deep trenches provide a high resistance barrier between devices. The n+ salicide reduces coupling to substrate and other devices by diverting the signal to the salicide instead of the substrate.

inductors which have been fully modeled and include layout artwork. Bondpads and resistors are available with deep trench grids in the substrate, or a n+ salicide bed between substrate and the device. The models in the design kit include the effects of the deep trench and n+ salicide isolation.

The majority of the devices within the kit are scalable (including the HBTs) giving the designer more freedom in choosing device sizes, and allowing better control of layout and parasitics. Device sizes or parameters are automatically calculated depending on the user input, making device sizing very straightforward.

1.3 Packaging

Packaging plays a critical role in all production RFICs. Packages protect the die and wirebonds, provide heat dissipation, and acts as an interface between die and external circuitry such as printed circuit boards (PCB) traces. However, packaging also poses many difficulties for designers, particularly at RF frequencies. Packaging introduces unwanted parasitics into the circuitry. Packaged circuits also consume large board area and add to the cost of the product. The cost of packaging ICs often

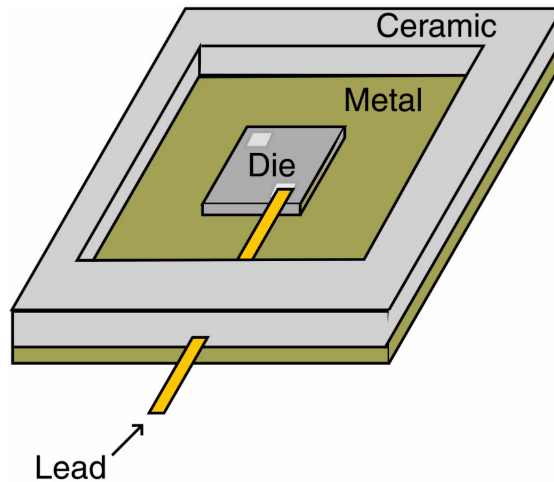


Figure 1.5: Illustration showing a cross-section of a metal-ceramic package. The metal provides a solid ground for the circuit and provides excellent heat dissipation. The ceramic provides heat dissipation and allows the leads to enter the package without shorting to the metal casing.

becomes more expensive than the IC itself.

There are a number of packages which can be employed at these frequencies. Each has its own associated benefits and drawbacks. The three types of packaging considered for this specific project were metal-ceramic, wafer scale, and plastic packaging.

Metal-ceramic packaging technology uses a combination of metal and ceramic to provide excellent thermal dissipation capability [12]. The packages are also very rugged and work well in environmentally harsh conditions. In addition, the metal casing provides an excellent ground contact and shield. In a typical metal-ceramic package, the die is encased in a metal package with a ceramic ring around the perimeter (Fig. 1.5). Contact leads, which typically have a 50 Ω characteristic impedance, run through the ceramic ring and contact the die where interconnects are needed. This style packaging is used substantially in high power and high frequency applications were its benefits can justify the high manufacturing cost and large package size.

Wafer-scale packaging can be used for applications where small area and low parasitics are critical. Wafer-scale packaging implies that the package size is no larger than the actual die. An emerging form of wafer-scale packaging technology known as flip-chip packaging has been successfully demonstrated at 5 GHz [13]. This technique involves

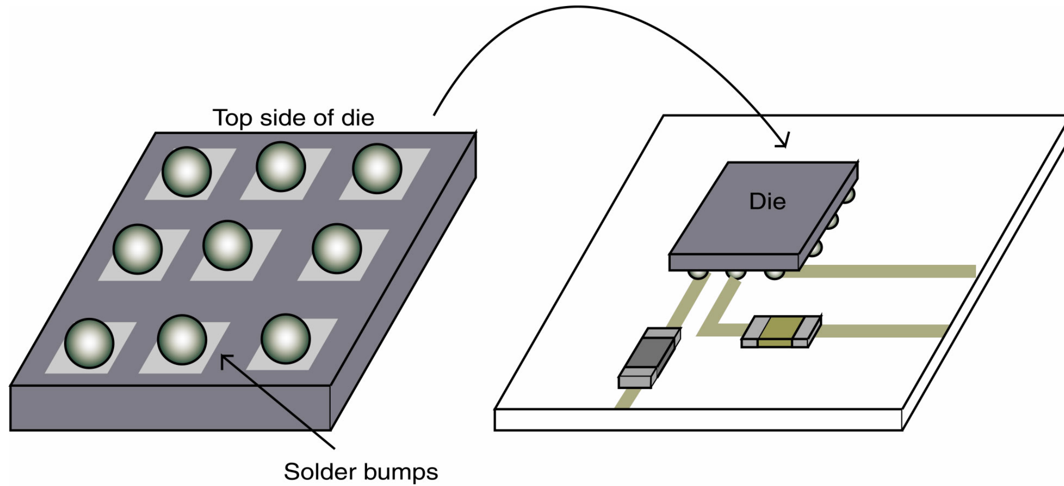


Figure 1.6: Illustration showing flip-chip packaging. Small solder bumps or posts are placed on the die and flipped onto a substrate or circuit board.

the deposition of small solder bumps or posts directly on the die were interconnects are needed. The die is then flipped onto a substrate or board which contains the circuitry external to the die; the solder is then reflowed to make the electrical connections (Fig. 1.6). This technique lowers parasitics by eliminating the need for bondwires. It also allows contacts to be made at any location on the die increasing IC layout flexibility. Currently, the main drawback of this packaging technology is that the complexity of the process adds significantly to the cost of the IC. In addition, modeling for flipchipped ICs/interconnects are an issue.

Plastic packaging is a less-expensive technology, well suited for high-volume manufacturing. Plastic packages come in many different styles – the most common packages used at RF are the leaded and leadless package. Ball-grid array (BGA) is another packaging technology which has recently emerged for RF applications. Figure 1.7(a) shows the top side of a BGA. A BGA package looks similar to the flip-chip implementation except the die is not mounted directly to the circuit board. Instead, the die is mounted in a package and wirebonded to vias which connect the top side of the package to the solder bumps underneath. The BGA has the advantage of a high pin density and is very useful for applications such as base-station RFICs. However, because of the way a BGA is constructed, it tends to be more expensive than the

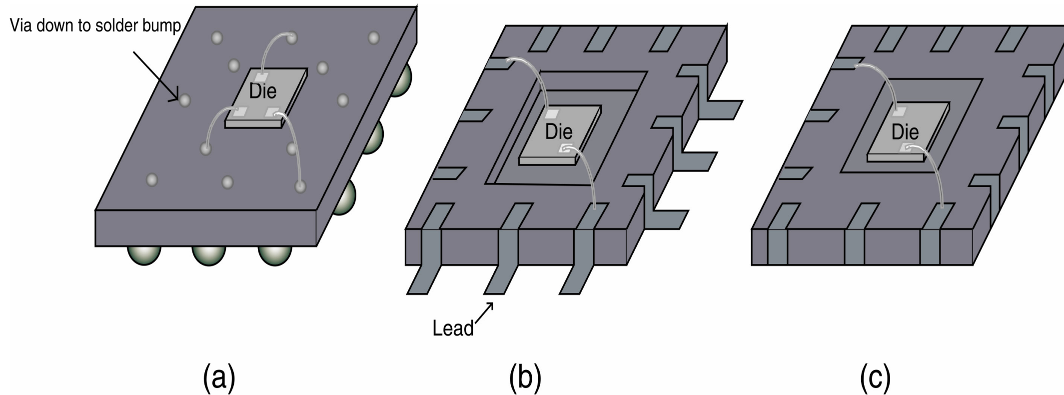


Figure 1.7: Plastic packages used in RFIC design (a) ball grid array (b) leaded package (c) leadless package.

other plastic packages.

In leaded package technology [1.7(b)], the die is mounted in the package and wire bonded to the pin contacts at the edge of the package or the "lead-frame". This implementation is low-cost and is the simplest of the three from the standpoint of manufacturing. For RF applications, a drawback of the leaded package is the pin parasitics. The lead-less package reduces this problem by eliminating the leads of the package [Fig. 1.7(c)]. The die is bonded to the top side and wirebonded to the pin contacts. The package pin contacts are exposed on the top and bottom sides of the package so the package can be soldered onto a board from underneath the BGA.

The circuits presented in this project use the low-cost plastic MLF series packages by Amkor. The MLF package is a leadless package with an exposed ground flag or paddle. Compared to available leaded packages, the MLF package is smaller and has lower parasitics. The exposed ground paddle allows the use of downbonds as opposed to bonding out to a pin for ground, further reducing the parasitics to ground.

1.4 Project Description and Objective

The objective of the project presented in thesis is the development of a SiGe RFIC front-end for operation in the U-NII band. Specifically, several packaged LNAs and a packaged active x2 sub-harmonic mixer (SHM) are designed, simulated and

measured. The IC fabrication is through the IBM SiGe foundry; the packaging and bonding are through RFMD. The mixer and LNAs are designed on separate die, packaged individually and matched to a 50 Ω system so that they each can be fully characterized. This thesis seeks to address the following issues:

- The performance of SiGe in the 5-6 GHz ISM band;
- The impact of low-cost plastic packaging and on-chip integration on the performance of high-frequency RFICs;
- The performance of an active harmonic mixing topology.

With the knowledge gained from this thesis, this project can ultimately be extended to the implementation of a 5-6 GHz SiGe direct conversion receiver.

The performance goals for the front-end are presented in table 1.3. The specifications were written considering the performance of the SiGe process, results of previously published designs, and application notes provided by RFMD.

1.5 Overview of Thesis

This thesis is composed of six chapters. In Chapter 2, an overview of LNA topology considerations is presented, and the design, simulation and layout of three LNA variants is discussed. Chapter 3 follows with the measurements of the fabricated LNAs. Test board layout, measurement set-ups and a comparison of the simulated and measured results are also included in the chapter. Chapter 4 gives a brief overview of SHMs and describes the design, layout, and simulation of an active x2 SHM. In addition, the on-chip LO buffering and phase separation for the mixer are detailed. Chapter 5 presents the measured results of the mixer. Chapter 6 concludes the thesis with a discussion on future work.

Table 1.3: Preliminary objectives for the 5-6 GHz RFIC front-end (T=298K).

Function	**Specification**			**Unit**
	Min	**Typ**	**Max**	
Overall				
Voltage	3.0	3.3	5.0	V
Power Consumption		40		mA
RF Frequency Range	5.0		6.0	GHz
IF Frequency Range	250		1250	MHz
LNA				
Noise Figure		3		dB
Gain		10		dB
Input IP3		0		dBm
Input VSWR		<2:1		
Reverse Isolation		20		dB
Output VSWR		<2:1		
Mixer				
Noise Figure		10		dB
Conversion Gain		4		dB
Input IP3		-5		dBm
Input VSWR		<2:1		
LO Level	-10		0	dBm
LO-RF Isolation		35		dB
LO Input VSWR		<2:1		

Chapter 2

LNA Design and Simulation

The LNA is a very important component in the front end of an RF receiver. In most applications, it is the first active block in the receive chain. Therefore, it has a large impact on the system noise figure (NF) and determines the overall input impedance. Because of these requirements, an LNA must exhibit low noise, high gain, and a well controlled impedance. In addition, the LNA must have a high degree of reverse isolation for stability and to prevent unwanted signals from leaking back through the LNA and reaching the antenna or transmitter section.

2.1 Topology Considerations

The most common transistor configurations for a bipolar-based LNA are the common emitter (CE) and common base (CB) topologies [14]. Emitter follower amplifiers do not provide the gain necessary for an LNA and thus are not used except in later stages of a multiple stage amplifier (for impedance transformation).

The CB configuration has several advantages over the CE amplifier. The input resistance of an ideal CB amplifier can be easily matched to 50 Ω by setting the transconductance (g_m) of the transistor to $\frac{1}{R_{in}}$. In addition, the CB amplifier provides better isolation between the input and output of the device. Figure 2.1 shows the small signal equivalent circuits of a CB and CE transistor configuration. In the CE configuration, the collector-base capacitance, C_μ, provides positive feedback between the

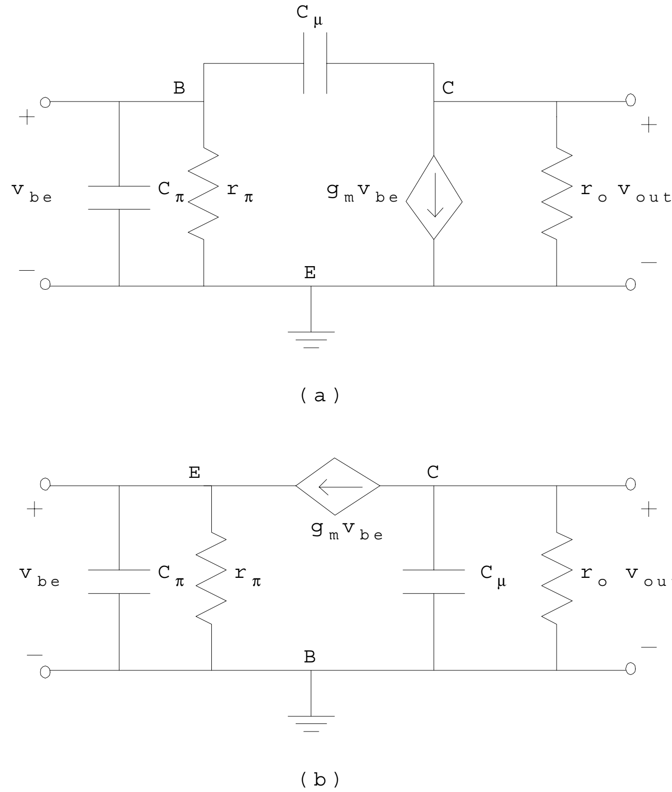


Figure 2.1: Small Signal Diagrams: (a) CE (b) CB.

output and the input of the transistor. Furthermore, feedback results in Miller multiplication causing the capacitance of C_μ to appear much larger at the input of the amplifier. In the CB configuration, C_μ is between the collector and ground. Since the capacitance is no longer in the signal path, little feedback occurs and the Miller multiplication is eliminated. Finally, CB amplifiers typically display higher linearity than CE amplifiers since the source resistance buffers the emitter impedance variation [15].

The primary limitations of the CB topology are its relatively high NF and less than unity current gain. The minimum NF of an ideal CB amplifier is 1.77 dB assuming only collector shot noise. In reality, the inherent minimum NF is much higher than this due to other noise sources within the transistor and circuit. Since these two figures of merit (FOM) are key specifications for an LNA, CB configurations are rarely seen as the first stage of an LNA.

Consequently, the CE topology is a more common choice for the first stage of an LNA. The CE configuration provides high voltage gain as well as moderate current gain. In addition, the CE topology does not inherently limit the NF of an LNA. This make the CE ideal for LNA applications where high power gain and a low NF are desired.

The CE configuration does not come without disadvantages. The CE configuration suffers from poor linearity and low reverse isolation. While these disadvantages seem to make the CE prohibitive in LNA applications, there are techniques for improving performance in these areas.

2.1.1 Noise Figure

Noise figure is one of the most important figures of merit for an RF LNA. NF measures the degradation in signal-to-noise ratio (SNR) from input to output of a circuit. The NF of a system of cascaded components is calculated by Equation 2.1 where NF_n represents the nth stage linear NF and G_{pn} represents the nth stage linear power gain [16].

$$NF = NF_1 + \frac{NF_2 - 1}{G_{p1}} + \frac{NF_3 - 1}{G_{p1}G_{p2}}... \tag{2.1}$$

The implication of 2.1 is that the first stage in a system, usually the LNA, has a large effect on the system noise performance. Therefore, it is important to have a good understanding of the different noise contributors in an LNA so they can be minimized in the design.

Figure 2.2 shows a bipolar transistor with the two dominant noise sources. The major contributors of noise are the collector shot noise, $\bar{\imath}_{n,c}$, and the base resistance thermal noise.

$\bar{\imath}_{n,c}$ is created by the charge flow across the collector-base p-n junction of the transistor. It can be estimated as $\sqrt{2qI_c}$, where q is the charge of an electron and I_c is the average collector current. Base shot noise also exists but is assumed small and is typically neglected. The base noise voltage arises from the thermal noise of r_b and is given by:

$$\bar{v}_{n,r_b} = \sqrt{4kTr_b} \tag{2.2}$$

where k is Boltzmann's constant, T is temperature in K, and r_b is the intrinsic base resistance.

Since NF is usually referenced to the input of the device, it is useful to refer all the noise sources to the input of the transistor. The base noise voltage remains unchanged and the collector shot noise becomes a noise voltage at the input equal to [17]:

$$\sqrt{4kT\frac{1}{2g_m}} \tag{2.3}$$

where g_m is the transconductance of the BJT biased at Ic. Given these noise sources, the equivalent noise resistance and NF are:

$$R_{eq} = r_b + \frac{1}{2g_m} \tag{2.4}$$

$$NF = 1 + \frac{R_{eq}}{R_s} = 1 + \frac{r_b}{Rs} + \frac{1}{2g_m Rs} \tag{2.5}$$

Intuitively, it would appear that a higher collector current would increase the noise contribution of channel shot noise and lead to a higher NF. However, equation 2.5 shows that an increase in collector current actually *decreases* the NF of the device. This is because the noise current (which is a square-root function of bias current) gets divided by the g$_m$ of the transistor (which has a linear relationship with bias current) when referenced to the input .

There are also other noise sources external to the transistor that will contribute to the overall NF. A general analysis to calculate NF of the entire circuit is first to identify all the noise sources. The next step is to move the noise sources to the output of the circuit by multiplying the noise source by the gain seen from the point of occurrence to the output. Then all the noise sources should be summed at the output (assuming all the sources are uncorrelated) and divided by the total voltage gain of the circuit to refer the noise back to the input. The NF is then represented by:

$$\frac{\bar{V}^2_{out,total}}{|A_v|^2\, 4kTRs}$$

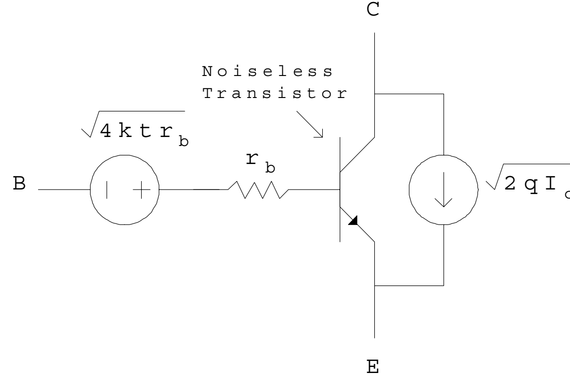


Figure 2.2: Noise model for a bipolar transistor.

The impact of this equation is that any noise sources present at the output of the circuit are attenuated by the gain of the LNA. However, any noise sources present at the input of the device directly add to the NF. For example, the NF for a single transistor LNA with a collector load resistor (neglecting base shot noise, parasitics and biasing) is given by:

$$NF = 1 + \frac{r_b}{R_s} + \frac{1}{2g_m R_s} + \frac{R_l}{R_s\left|A_v\right|^2} \tag{2.6}$$

Equation 2.6 shows that the collector load resistance also adds to the NF of the circuit, although it is attenuated by the gain of the circuit. This illustrates the need for high gain in an LNA.

2.1.2 Isolation and Stability

The majority of the isolation and stability problems in a CE amplifier are caused by C_μ. As mentioned previously in Section 2.1, C_μ provides a feedback path between collector and base reducing the maximum stable gain of the amplifier and increasing RF leakage from output to input. To improve stability and isolation, a means to reduce the impact of C_μ is required. This can be accomplished in several ways. Reducing the gain of the device will decrease the Miller effect and increase stability.

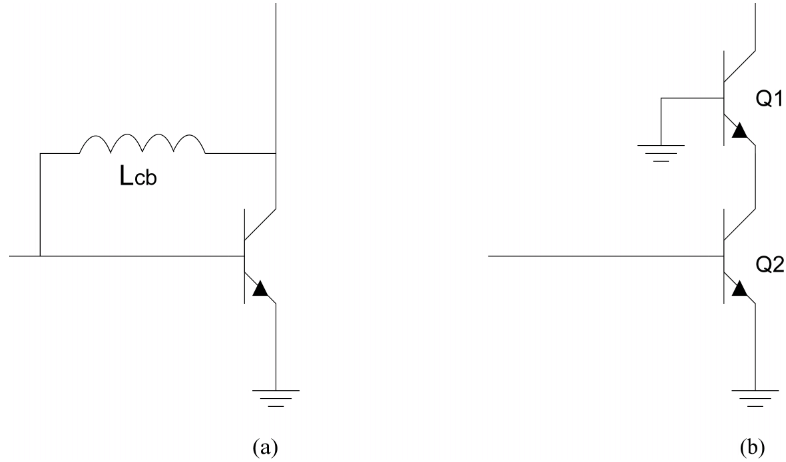


Figure 2.3: Isolation mechanisms: (a) neutralization (b) cascode.

However, this method is counterproductive to the basic goals of an LNA: high gain and low noise. More beneficial approaches involve changes in the amplifier topology. Figure 2.3 shows two possible implementations. The first circuit [Fig. 2.3(a)] is commonly referred to as *neutralization*. An inductance is placed in parallel with C_μ to effectively cancel the capacitance in the band of interest. This method has several major drawbacks which limit its practicality:

- For on-chip implementations, the required inductors usually occupy prohibitively large die area.
- The inductor must be very high quality factor (Q) and have very low capacitive parasitics. This usually is not possible for on-chip inductors, especially on silicon. The low resistivity of the substrate leads to losses and capacitive coupling to substrate, preventing sufficient neutralization.
- The inductive path must include a DC block to prevent any change in the DC operating point. The required blocking capacitor adds additional parasitics and consumes additional die area.
- The approach is inherently narrowband due to the resonance between C_μ and the neutralizing inductor.

A more attractive method to improve the isolation of an LNA is the use of a *cascode* configuration [Fig. 2.3(b)]. In the cascode configuration, Q2 is arranged as a CB transistor increasing the isolation between the input and output of the LNA. Furthermore, the low input impedance of the CB stage lowers the loaded voltage gain of the CE stage, reducing the Miller multiplication effect within Q1. The primary problem with using the cascode configuration is the introduction of additional noise in the signal path due to the CB device. However, the additional noise is somewhat attenuated by the voltage gain of the CE and is usually tolerable. Based on these advantages, the cascode topology has emerged as the topology of choice in many RFIC LNAs [18],[19],[20].

2.1.3 Impedance Matching

The filters which are commonly used before and after an LNA in a receiver chain are typically designed for a 50 Ω systems impedance. The characteristics of these filters may change if they are presented with different input or output impedances. It is therefore important to provide the filter a well matched termination over frequency. Furthermore, to achieve maximum power transfer, the LNA input and output ports should also be matched to the system impedance.

Many circuit topologies have been used in LNAs to achieve the desired input match [21]. Figure 2.4 shows the simplest and most common CE LNA matching topologies. The most straightforward approach is a simple 50 Ω shunt resistor at the input to the device [Fig. 2.4(a)] . The drawback of a resistive match is that the thermal noise generated by the resistor adds directly to the NF of the LNA without reduction. Using the analysis in Section 2.1.1, the placement of a 50 Ω resistor at the input of the LNA will result in a minimum NF greater than 3 dB. This is often higher than the total of all other noise contributors in the LNA.

Another method to achieve the input match is to use series/shunt feedback [Fig. 2.4(b)]. This method has been shown to have very high power dissipation due to the broadband nature of the topology [22]. It also increases the NF of the device due to the feedback resistors [23]. This method may be seen in the later stages of multiple stage LNAs, but is not commonly used for the first stage.

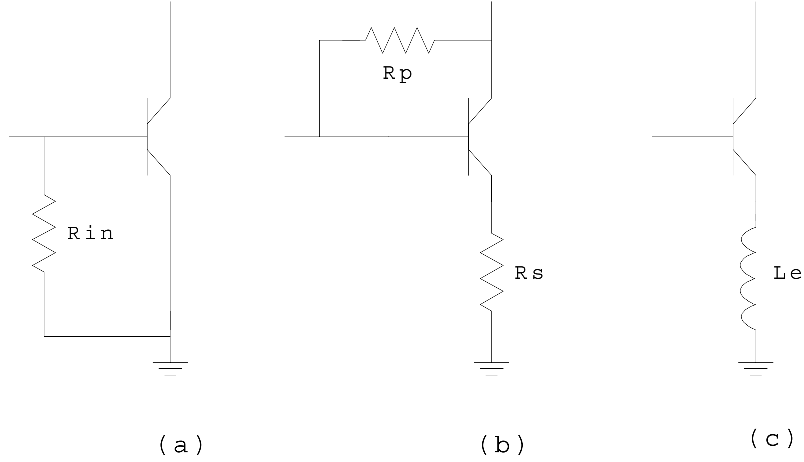


Figure 2.4: Impedance matching: (a) resistive termination (b) parallel/series feedback (c) emitter degeneration.

Perhaps the most common on-chip matching involves series feedback using emitter degeneration [Fig. 2.4(c)]. An inductive impedance is inserted at the emitter of the transistor to present a series feedback path. For the emitter degeneration case, the input impedance is given by:

$$Z_{in} = r_b + \frac{g_m}{2\pi(C_\pi + C_\mu)} L_e + j\omega L_e + \frac{1}{j\omega C_\pi} \tag{2.7}$$

In practice, the collector current, device size (C_π and C_μ), and L_e are chosen to achieve a 50 Ω real part, and the additional inductance presented by the RF input bondwire cancels any remaining capacitance.

Another common and often more convenient form of Eq. 2.7 is given by:

$$Z_{in} = r_b + 2\pi f_t L_e + j\omega L_e + \frac{1}{j\omega C_\pi} \tag{2.8a}$$

where f_t is the frequency at which the short-circuit CE current gain is unity and can be estimated as:

$$f_t \approx \frac{g_m}{(C_\pi + C_\mu)} \tag{2.9}$$

2.1.4 Linearity

A bipolar transistor is inherently non-linear due to its exponential I-V transfer characteristic. In the CE configuration, the collector current of a bipolar transistor is related to the input voltage by:

$$I_c = Is \cdot e^{(\frac{V_{BE}+v_{be}}{V_T})} \tag{2.10}$$

where Is is the reverse saturation current of the transistor, V_{BE} is the DC base-emitter voltage, v_{be} is the RF base-emitter voltage and V_T is the thermal voltage (25.9 mV at 298K).

The g_m of the transistor is therefore related to the input voltage by :

$$g_m = \frac{I_c}{V_T} = \frac{Is \cdot e^{(\frac{V_{BE}+v_{be}}{V_t})}}{V_T} \tag{2.11}$$

Expanding the transconductance equation using the first four power series terms of the exponential yields:

$$g_m = \frac{I_C}{V_T}\left[1 + \frac{v_{be}}{V_T} + \frac{1}{2}\left(\frac{v_{be}}{V_T}\right)^2 + \frac{1}{6}\left(\frac{v_{be}}{V_T}\right)^3 ...\right] \tag{2.12}$$

Therefor, the g_m of a bipolar transistor will exhibit a $\frac{1}{2}\left(\frac{v_{BE}}{V_T}\right)^2 + \frac{1}{6}\left(\frac{v_{BE}}{V_T}\right)^3$ nonlinearity due to the exponential nature of the transconductance.

Equation 2.11 shows that the g_m of a transistor can vary by 16.8 dB with a $\pm 50mV$ input signal. Therefore, it is clear that in order for the transistor to exhibit a high degree of linearity, some method of linearization is required.

An obvious means of increasing linearity is to increase the collector bias current (I_c). Equation 2.12 shows that a larger DC bias current will reduce the effects of the RF signal swing on the variation of g_m. However, the benefit of a high bias current comes at the cost of additional power consumption.

A more useful method to linearize the conductance waveform of a CE amplifier is to

add feedback to the circuit. Two of the more common configurations were discussed in Section 2.1.3 in the context of impedance matching. The shunt/series feedback, as mentioned before, suffers from additional noise and higher power consumption. A more common approach is the addition of a degenerating inductance at the emitter of the amplifier.

With the addition of emitter feedback, the equation for g_m then becomes:

$$I_c = I_s \cdot e^{\left(\frac{V_{BE}+(v_{be}-v_f)}{v_t}\right)} \tag{2.13}$$

where v_f is the voltage drop across the emitter inductor.

The voltage feedback lessens the variation in collector current by reducing the magnitude of the RF signal swing due to the $v_{be} - v_f$ term within the exponent. The main issues with using this technique is the reduction of gain associated with negative feedback and the need for a high quality inductor.

2.2 Design

The LNAs were designed and simulated using Agilent EESof Advanced Design System (ADS) v.1.3 software package [24] in combination with IBM's SiGe design kit v.2.1. Unlike common Spice simulators, the ADS package is a frequency based simulator. This makes frequency-domain simulations very easy and accurate. ADS also provides means to perform time-domain simulations through frequency-time translation. Since the IBM design kit was originally implemented for the Cadence design software and later ported to ADS, identical simulations were performed in ADS and Cadence to verify the relative accuracy of the ADS design kit.

2.2.1 LNA Design

The first step in the design process was to determine the packaging and bondwire parasitics. It was important to include the packaging parasitics and at least an estimate of bondwire parasitics at the beginning of the design since they have a large impact on performance at the frequencies of interest.

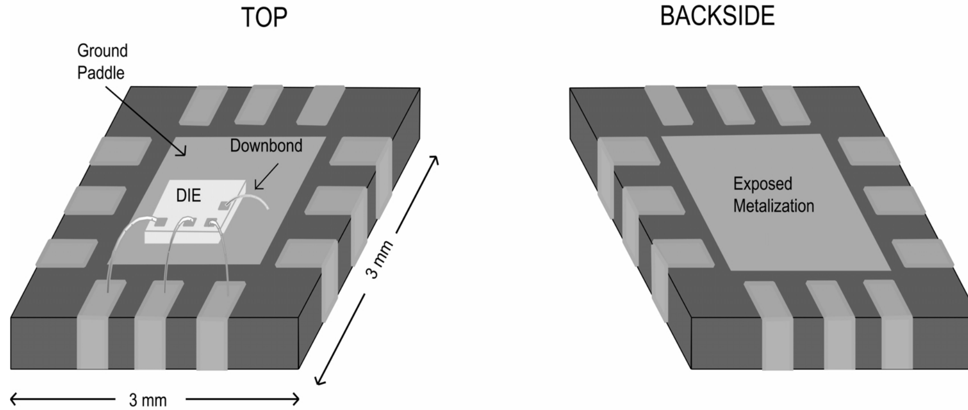


Figure 2.5: Conceptual diagram of the front and backside views of an MLF leadless package.

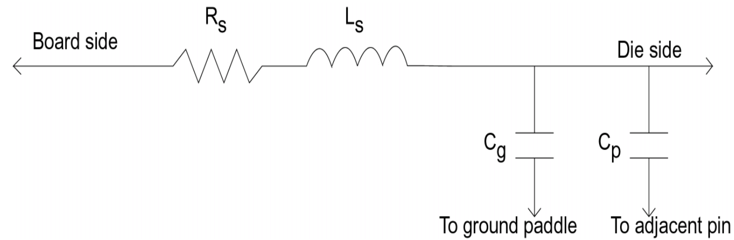


Figure 2.6: Circuit model of a package pin.

The original package chosen for the design was an Amkor MLF-12 leadless package (Fig. 2.5). The package had 12 pin contacts and measured 3 mm x 3 mm. As mentioned in the introduction, the package was chosen for its size, low parasitics, and exposed ground paddle.

The package pin circuit models used for the design were obtained from industry. Figure 2.6 shows the circuit models for the package pins. The model takes into account both the parasitics of the pin as well as the capacitive coupling between adjacent pins and between the pins and the ground paddle. The parasitics of the ground paddle were assumed to be small and were neglected.

The bondwire circuit model is shown in Figure 2.7. The bondwire is represented by a series resistance and inductance in parallel with an additional resistance. The distance between nearby bondwires were estimated so that the mutual inductance between adjacent bondwires could also be included.

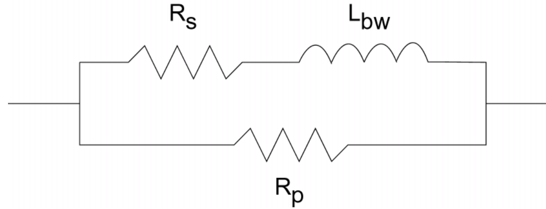


Figure 2.7: Circuit model of a bondwire.

With the packaging taken into account, design choices for the LNA were made. Initial simulations showed that a single transistor LNA provided sufficient gain but did not provide adequate input-output isolation or stability. This was due mainly to the coupling to other devices through the low resistivity substrate, and the pronounced effects of C_μ at higher frequencies [14]. To reduce the effects of C_μ, a cascode topology was chosen. Careful selection of device sizes and the careful layout of the circuitry was used to help reduce the coupling through the lossy substrate.

The input matching of the LNA was achieved through inductive emitter degeneration. Referring to Equation 2.7, emitter degeneration requires the proper choice of L_e, transistor size, and bias current. However, this was not sufficient to match the input of the LNA. The finite isolation of the circuit had an impact on the return loss at the input port. This meant that the output matching network and the CB transistors parasitics would have an impact on the input match. Therefore, the final input match was not achieved until the output match and cascode transistor size were known.

Downbonded wires on the emitter supplied the necessary inductance L_e for degeneration. Figure 2.8 shows the diagram used to calculate the bondwire length for a downbond and its value of inductance. The length of a typical downbond was approximately 700 μm, corresponding to an L_{bw} of 0.56 nH, an R_s of 0.2 Ω and an R_p of 1.6 kΩ [25].

Multiple parallel bondwires provided some tuning of the inductance. This provided a fixed range of tuning (0.56 nH, 0.23 nH, 0.19 nH...); therefore, the f_t (which is approximately determined by the choice of collector bias and device size) was calculated for the range of inductances allowed by the multiple downbonds. A general rule of thumb is to operate the transistor at one fifth or less of the f_t in order to have sufficient current gain from the device. With a single bondwire ($L_e = 0.56$ nH),

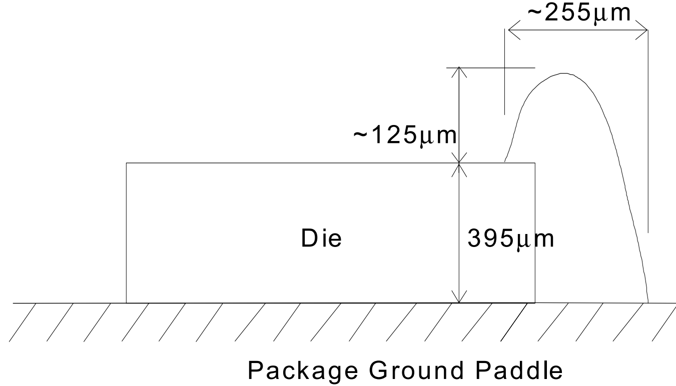


Figure 2.8: Diagram showing a typical downbond.

the required f_t as dictated by equation 2.7 was too low. Therefore, the design was restricted to two or more parallel bondwires.

The choice of device size and bias current to produce the required f_t was a challenge. Not only was the input match considered, but also effects on amplifier NF, linearity, gain, stability and power consumption. Equation 2.5 shows that r_b has a large impact on the NF of the device. In general, the CE transistor should be large in order to reduce r_b and therefore the NF. However, as the size of the transistor increases, so do the parasitics of the transistor. This is especially critical on the low resistivity silicon substrate in the SiGe process. If the transistor is made too large, a significant amount of signal is shunted to substrate by the large collector-substrate capacitance, resulting in a loss of gain. Also, as $C\mu$ becomes larger, positive feedback increases the possibility for instability and lowers the maximum stable gain (MSG).

Referring to Equation 2.9, the f_t of a transistor is proportional to the bias current and inversely proportional to parasitic capacitances. Since a larger transistor increases the parasitic capacitances, increasing the transistor size shifts the required f_t to a higher current (Fig. 2.9). Thus, increasing the size of the transistor increases the current requirements for the device as well.

In summary, the choice of the transistor size involved making a series of trade-offs. If the transistor was made larger, NF decreased and linearity increased (due to the required increase in collector current), while the stability and power efficiency decreased. If the transistor size was reduced, the power consumption decreased and

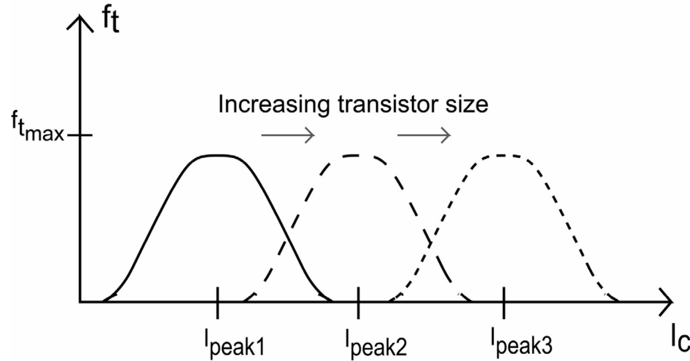


Figure 2.9: Conceptual diagram illustrating the shift of a transistors f_t with an increase in device size.

stability increased, while NF and linearity suffered. Therefore, a range of device sizes and number of parallel devices were simulated to find the best trade-off of these FOMs.

The CE transistor size (emitter length x emitter width x number of parallel devices) which provides the optimal balance between NF, current and parasitics was 20 μm x 0.5 μm x 2 (each unit transistor having two emitter fingers). The size of the cascoded transistor was initially chosen as 5 μm x 0.5 μm x 2 to minimize parasitics. Due to later difficulties with achieving acceptable stability and matching due to the parasitics and output capacitance of the cascoded device and on-chip inductors, the CB transistor was reduced to 5 μm x 0.5 μm x 1.

Using Equation 2.7, the necessary current for a 50 Ω match using a double emitter bondwire was 4 mA. Using more than two parallel bond wires provides too little feedback and decreased the linearity of the device. Furthermore, the addition of a third bondpad at the emitter of the CE transistor would add more parasitic capacitance to substrate making the input match more difficult. Therefore, only the double bondwire case was pursued for the LNAs.

Two approaches were taken to match the output of the LNA. The size of the CB transistor yielded a collector impedance with a real part very close to 50 Ω. As was done in [26], a series inductor between the collector of the CB transistor and the output pin of the package canceled the imaginary impedance to provide a 50 Ω

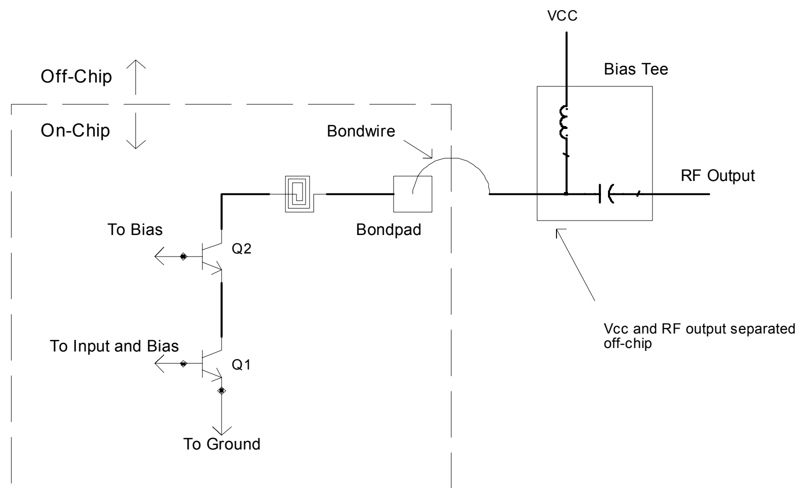
output impedance. To prevent the DC voltage supply (V_{CC}) from affecting the RF output match, the DC supply path was designed as an open-circuit termination at RF (Fig. 2.10).

Two versions of the LNA with the series inductor output match were designed, differing by how the RF termination at V_{CC} was achieved. The first version (series L v1) used an external bias tee to provide V_{CC} to the circuit [Fig. 2.10(a)]. For the second version (series L v2), V_{CC} was separated from the RF output on-chip and bonded out of the package separately [Fig. 2.10(b)]. The RF output was isolated from V_{CC} using a surface mount, wideband off-chip choke at V_{CC}. A small amount of resistance was added on-chip to the RF output for both versions to improve isolation and stability. The added resistance forms a low pass filter with the capacitance of the bondpads and package to improve the isolation between the LNA and the packaging parasitics. Simulations show that this resistance has little impact on the gain and NF of the device, but does affect the output match of the device. The inductor values for the output match were adjusted to account for the change in output match due to the added resistance.

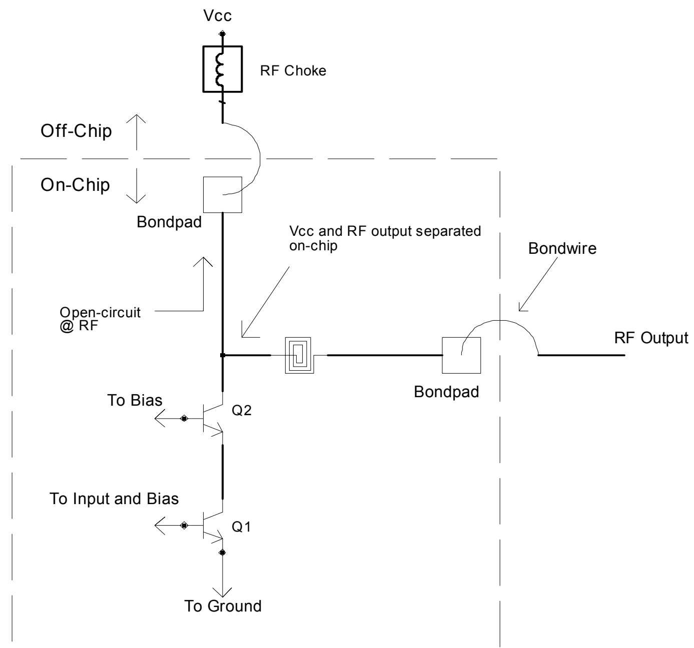
The available IBM design kit offered several inductor layouts with similar inductance values but different trace widths, trace spacings and number of turns. Only the inductors with sufficient Q over the band of interest and a series resonance frequency (SRF) above the band of interest were considered for the LNAs. Simulations were used to determine which of these inductors and their associated parasitics provided the best output match for each version of the LNA. The series L v1 LNA used a two-turn 3.4 nH inductor with a 20 μm trace width and 3 μm spacing (200 μm x 200 μm total die area). The circuit required more inductance than was possible given the available inductor values in the frequency range. Therefore, an additional 1.5 nH was provided by an off-chip surface mount (SMT) inductor.

In the series L v2 LNA, the additional bondpad and packaging parasitics for V_{CC} changed the requirements for the output match. The bondpad size at V_{CC} and the output matching inductor were chosen together to yield the best possible match. The final result used a 5-turn 2.5 nH inductor with a 15 μm trace width and 3 μm spacing (200 μm x 200 μm total die area), and a 75 μm x 75 μm bondpad at V_{CC}.

Voltage biasing for the CE transistor was implemented to minimize noise [27]. The



(a)



(b)

Figure 2.10: Diagram showing the output match of the LNAs with series L match: (a) version 1; (b) version 2.

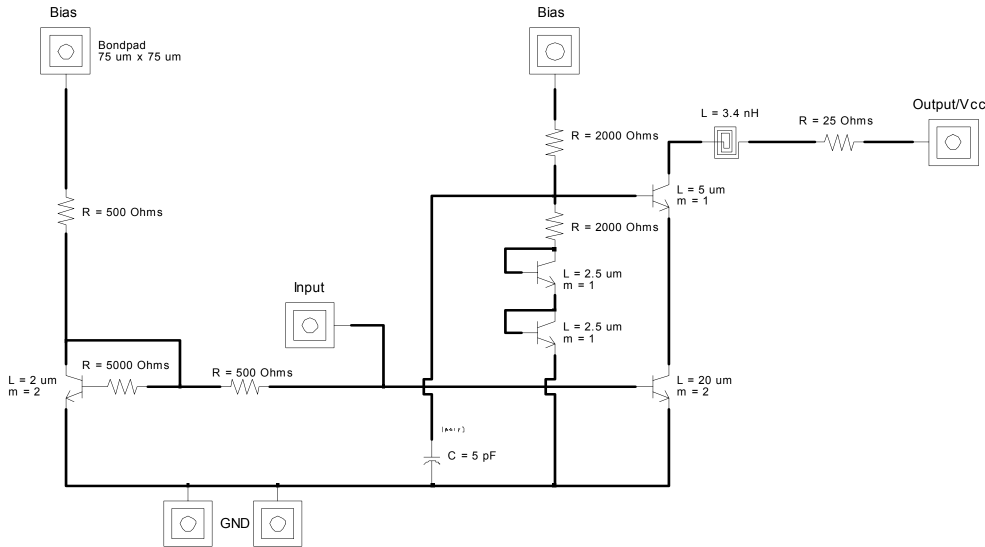


Figure 2.11: Schematic of the LNA with series L output match (v1).

biasing network can be viewed as a current mirror with some multiple of the reference current being mirrored to the CE transistor. This technique is considered voltage biasing since the base-emitter voltage of the reference transistor sets the base-emitter voltage of the CE transistor. A 500 Ω resistor was placed between the RF input and the bias circuitry to increase the impedance looking back into the mirror, reducing the amount of RF power which is lost to the bias network.

A 5 pF on-chip decoupling capacitor connected between the base of the CB transistor and the on-chip ground was used to provide the required RF ground at the CB transistor base. A voltage divider similar to that used in [27] set the voltage level at the base of the cascoded transistor. Diode connected transistors provided large voltage drops while requiring little space and current; two resistors set the voltage division.

The complete schematics for the two series inductor matched LNAs are shown in Figures 2.11 and 2.12. Both circuits were biased at a collector current of 4 mA. The reference transistor in the biasing circuitry drew 0.4 mA.

The alternative approach taken to output matching the output of the LNA was a shunt-L/series-C matching network (Fig. 2.13). An on-chip inductor placed between the collector of the CB transistor and V_{CC} provided the load for the LNA. V_{CC}

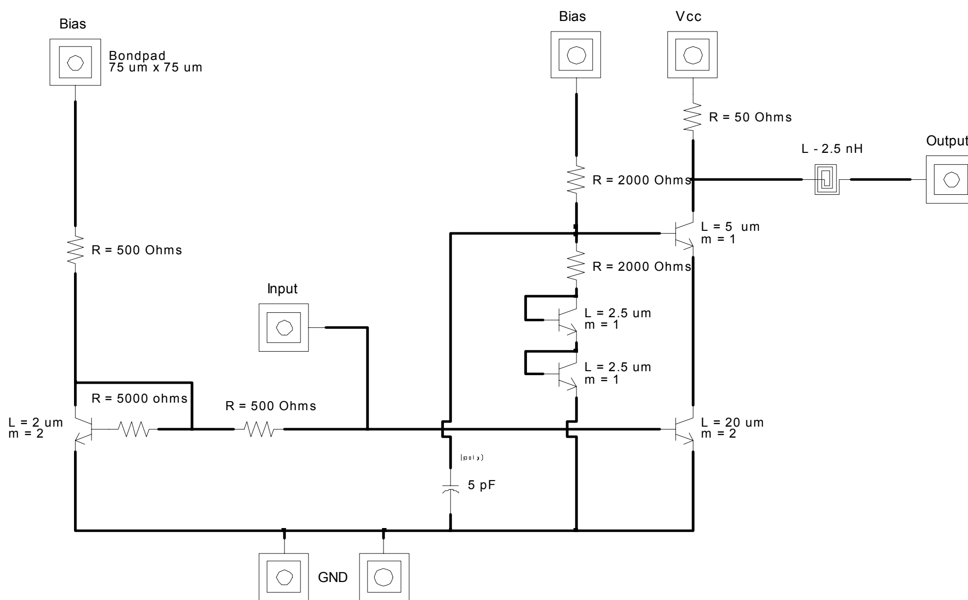


Figure 2.12: Schematic of the LNA with series L output match (v2).

was terminated with an RF ground off-chip to make the inductor appear as a shunt element at the RF output. A capacitor was placed between the CB collector and the output pin of the package to match the output of the LNA to 50 Ω (this also served at the output DC block). The topology used an 2-turn 1.1 nH inductor with a 20 μm trace width and 3 μm spacing (200 μm x 200 μm total die area) and a 0.34 pF on-chip series MIM capacitance.

The biasing of the CE transistor for this LNA design was identical to the approach used for the series inductor matched versions. However, the CB transistor was biased differently than the series inductor matched LNAs. Since V_{CC} was an RF short, the base of the CB transistor could be tied directly to VCC eliminating the need for the extra bias circuitry used in the series-L LNA designs. The RF short circuit termination at V_{CC} was supplied by an off-chip SMT capacitor.

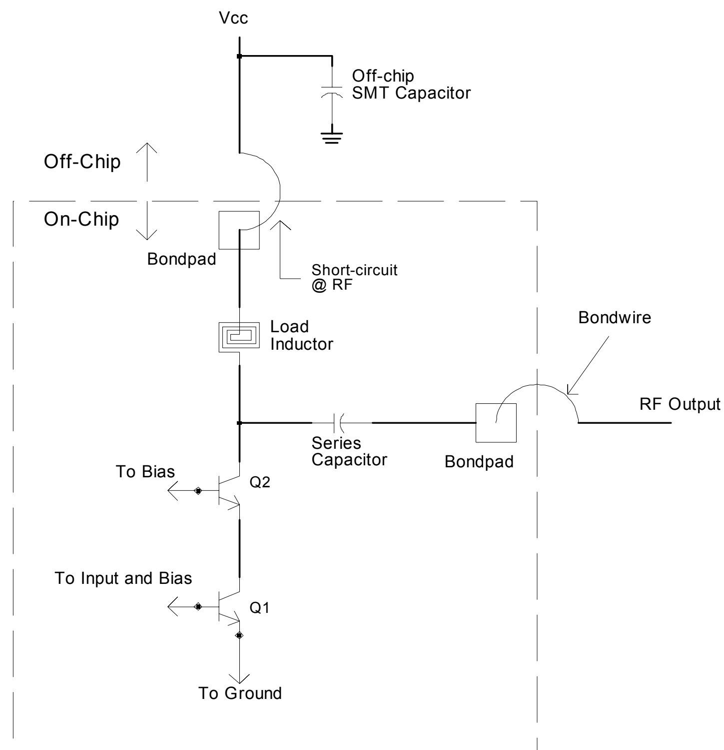


Figure 2.13: Diagram showing the output match of the LNA with LC match.

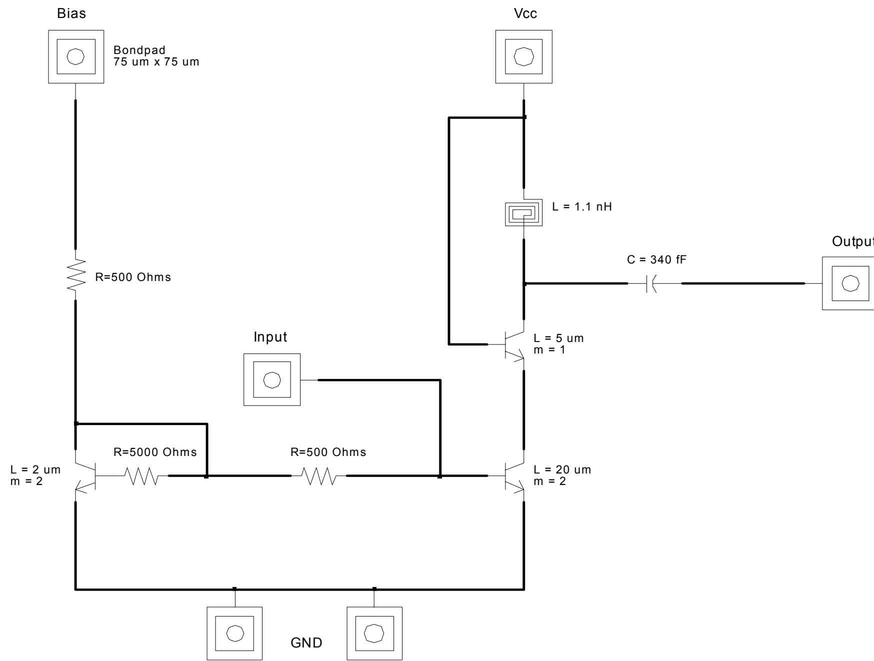


Figure 2.14: Schematic of the LNA with LC output match.

2.3 Simulated Results

As mentioned in the introduction, the IBM design kit includes all the necessary on-chip actives and passives for the design. The inductors, capacitors, resistors and bondpads used in the design come directly from the design kit. Both simulated and measured results at the design frequencies are included within the design kit documentation. This verified the validity of the design models in the band of interest.

S-parameter simulations in the frequency range of 4.8 GHz - 6.2 GHz were used to characterize the gain, match and isolation of the three designs. The NF option within the S-parameter stimulus was used to simulate the NF of the circuits. Rollett's stability factor (k) was used to test for stability. In addition, geometrically derived stability factors (μ and μ') were used to test for source and load stability. For linearity, a two-tone test using Harmonic Balance Analysis (HBA) was used. The two tones for the test were placed at 5.25 GHz and 5.252 GHz.

The actual ADS simulation set-ups for the LNAs are given in Appendix B.

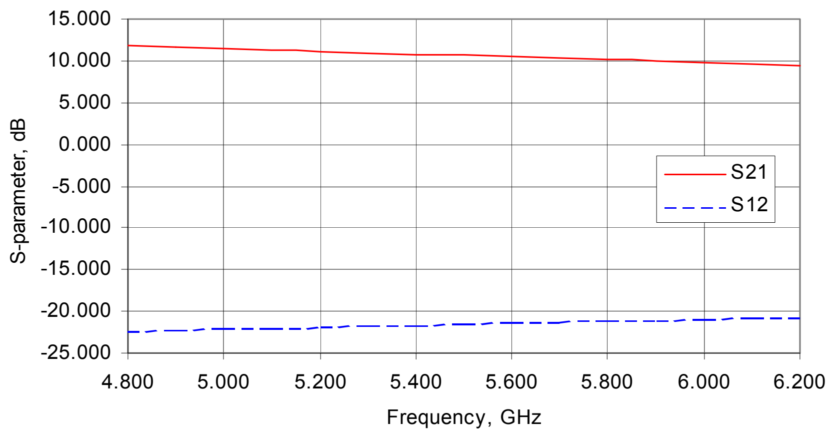


Figure 2.15: Simulated S_{21} and S_{12} of the LNA with LC output match.

2.3.1 LNA with LC Output Match

The simulated gain and isolation are shown in Figure 2.15. The gain is 12 dB at 5 GHz and 10 dB at 6 GHz. The isolation is greater than 20 dB over the entire band.

Figure 2.16 shows the reflection coefficients of the LNA. Over the band of interest, the input and output reflection coefficients are better than -10 dB and -14 dB, respectively. This results in a voltage standing wave ratio (VSWR) of less than 2:1 and 1.5:1 for the input and output ports, respectively (Fig. 2.17).

The simulated NF of the LC matched is shown in Figure 2.18. The NF is a minimum of 2.1 dB at 5 GHz and a maximum of 2.42 dB at 6 GHz.

Table 2.1 shows the stability of the LNA in the band of interest. The first two columns represent the geometric distance from the center of a smith chart to the nearest point of instability for the input and output, respectively. This can be viewed as the magnitude of the reflection coefficient a source or load impedance would need to present to the LNA to cause the circuit to become unstable. Any value greater than unity represents a stable circuit over all realizable passive terminations (all stable points lie inside the unit circle). This is an alternative to plotted stability circles. The third column shows the Rollet's stability factor k. This is a more common way of representing stability at a specific source and load impedance. A value greater than unity represents a stable circuit. The table shows that the circuit is unconditionally

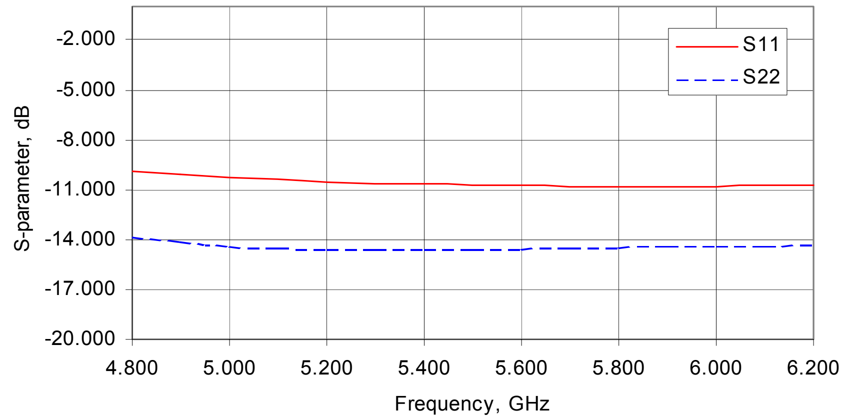


Figure 2.16: Simulated S_{11} and S_{22} of the LNA with LC output match.

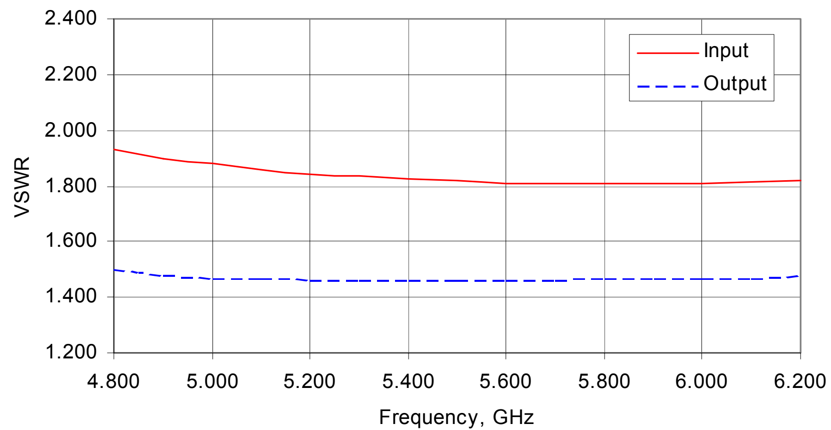


Figure 2.17: Simulated VSWR of the LNA with LC output match.

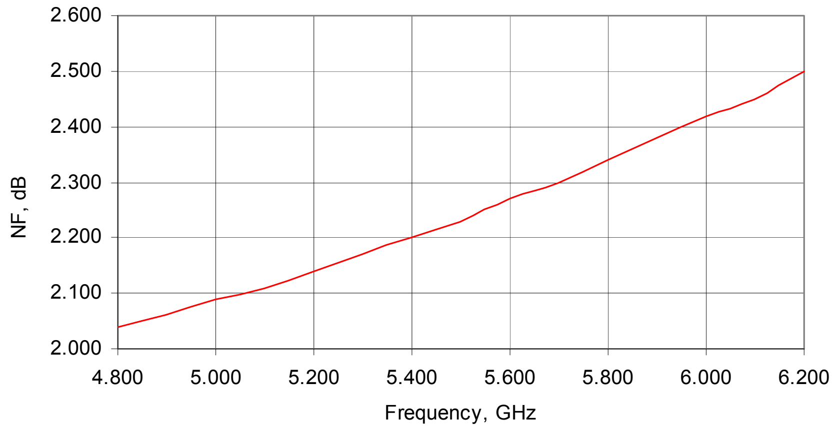


Figure 2.18: Simulated NF of the LNA with LC output match.

stable for all passive terminations in the band of interest.

The input third order intercept point (IIP3) is calculated by extrapolating the fundamental tone power and the larger of the two third-order intermodulation tone powers to the point at which they intersect (Fig. 2.19). The simulated IIP3 is 4 dBm.

2.3.2 LNA with Series L Match (v1)

The simulated gain and isolation are shown in Figure 2.21. The gain is 15.5 dB at 5 GHz and 14.7 dB at 6 GHz. The isolation is greater than 30 dB over the entire band.

Shown in Figure 2.20 are the reflection coefficients of the LNA. Over the band of interest, the input and output reflection coefficients are better than -10 dB. The input port has its best match at around 4.8 GHz while the output is best matched at 5.9 GHz. Both ports have a voltage standing wave ratio (VSWR) of less than 2:1 as illustrated in Figure 2.22.

The simulated NF of the series inductor match (v1) is shown in Figure 2.23. The NF is a minimum of 2.4 dB at 5 GHz and a maximum of 2.9 dB at 6 GHz.

Table 2.2 shows the stability of the LNA in the band of interest. The circuit is unconditionally stable for all passive terminations in the band of interest.

Table 2.1: Stability criteria of the LNA with LC match.

Freq (GHz)	Input Stability Coefficient (μ')	Output Stability Coefficient (μ)	k (50 Ω)
4.8	2.00	1.67	1.63
4.9	2.01	1.68	1.64
5.0	1.99	1.68	1.65
5.1	1.98	1.69	1.65
5.2	1.96	1.69	1.66
5.3	1.95	1.69	1.67
5.4	1.93	1.69	1.68
5.5	1.92	1.69	1.68
5.6	1.90	1.68	1.69
5.7	1.89	1.68	1.69
5.8	1.88	1.68	1.70
5.9	1.87	1.67	1.70
6.0	1.86	1.67	1.71
6.1	1.85	1.66	1.71
6.2	1.84	1.66	1.72

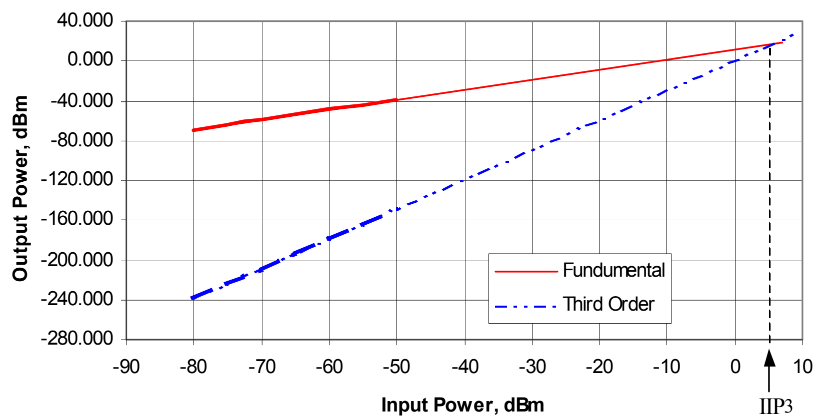


Figure 2.19: Simulated linearity of the LNA with LC output match.

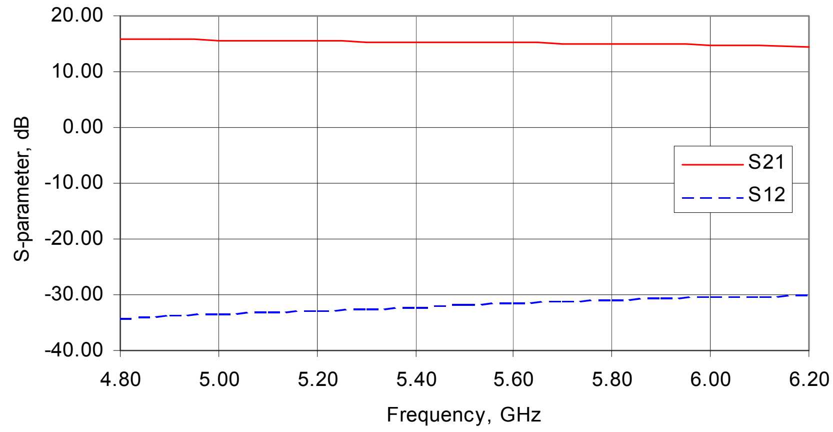


Figure 2.20: Simulated S_{21} and S_{12} of the LNA with series L output match (v1).

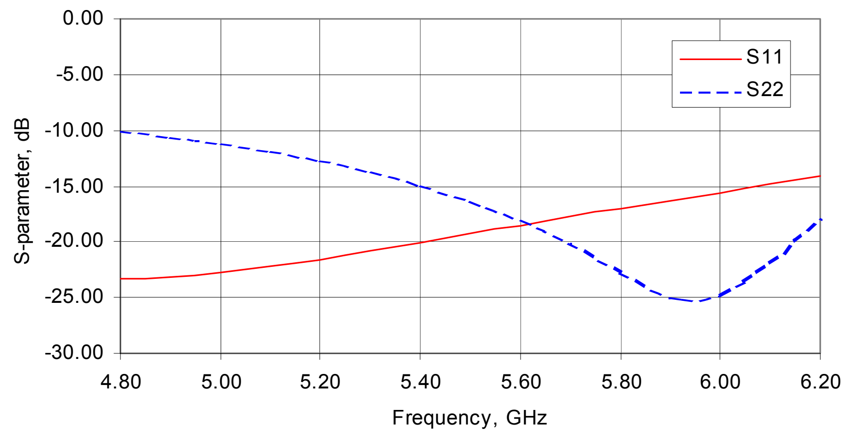


Figure 2.21: Simulated S_{11} and S_{22} of the LNA with series L output match (v1).

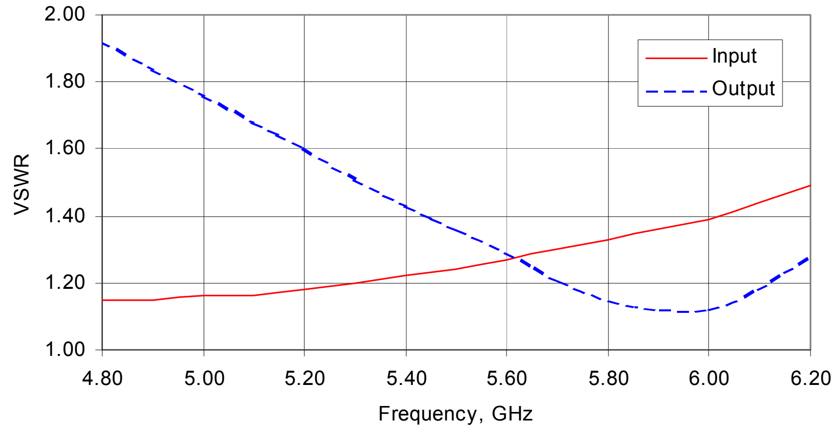


Figure 2.22: Simulated VSWR of the LNA with series L output match (v1).

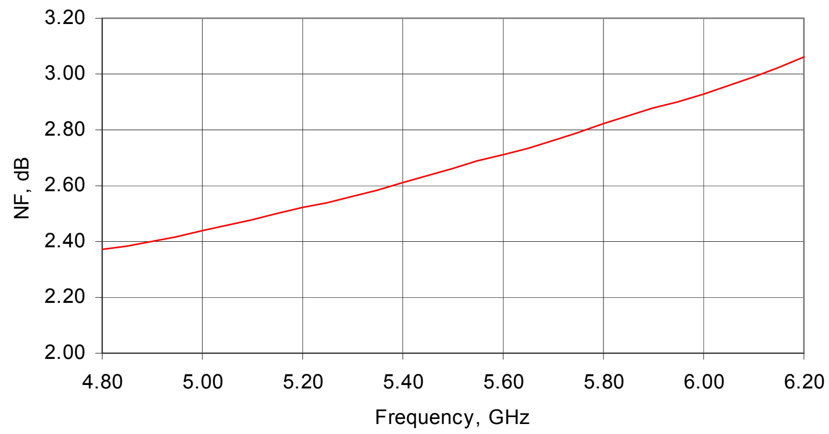


Figure 2.23: Simulated NF of the LNA with series L output match (v1).

Table 2.2: Simulated stability criteria of the LNA with series L match (v1).

Freq (GHz)	Input Stability Coefficient (μ')	Output Stability Coefficient (μ)	k (50 Ω)
4.8	2.27	4.41	3.72
4.9	2.34	4.31	3.66
5.0	2.43	4.21	3.61
5.1	2.54	4.08	3.54
5.2	2.66	3.96	3.48
5.3	2.80	3.84	3.42
5.4	2.97	3.71	3.36
5.5	3.17	3.59	3.30
5.6	3.40	3.48	3.24
5.7	3.70	3.36	3.17
5.8	4.04	3.26	3.12
5.9	4.40	3.16	3.07
6.0	4.66	3.07	3.02
6.1	4.35	2.98	2.96
6.2	3.75	2.89	2.91

The linearity is shown in Figure 2.24. The resulting IIP3 was 2.7 dBm.

2.3.3 LNA with Series L Match (v2)

The simulated gain and isolation are shown in Figure 2.25. The gain is 15.5 dB at 5 GHz and 14.7 dB at 6 GHz. The isolation is greater than 30 dB over the entire band.

Shown in Figure 2.26 are the reflection coefficients of the LNA. The input and output reflection coefficients over the band of interest are better than -10 dB. The input port is best matched at around 4.9 GHz while the output is best matched at 6.1 GHz. Both ports have a VSWR of less than 2:1 as illustrated in Figure 2.27.

The simulated NF of the series inductor match (v2) is shown in Figure 2.28. The NF is a minimum of 2.4 dB at 5 GHz and a maximum of 2.9 dB at 6 GHz.

Table 2.3 shows the stability of the LNA in the band of interest. The circuit is unconditionally stable for all passive terminations in the band of interest.

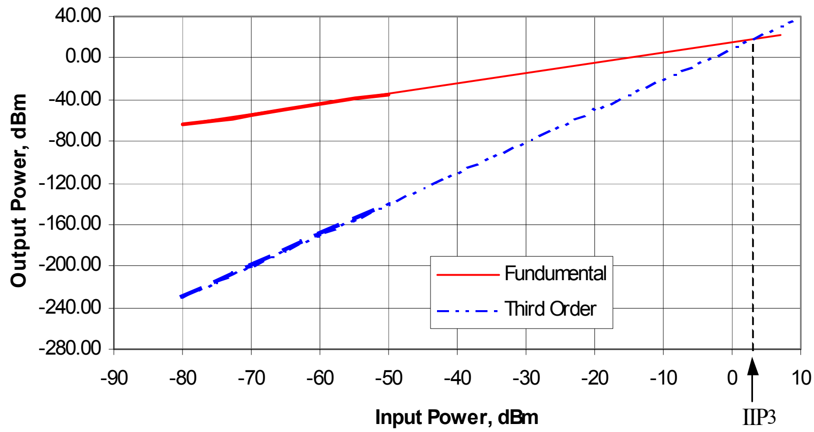


Figure 2.24: Simulated linearity of the LNA with series L output match (v1).

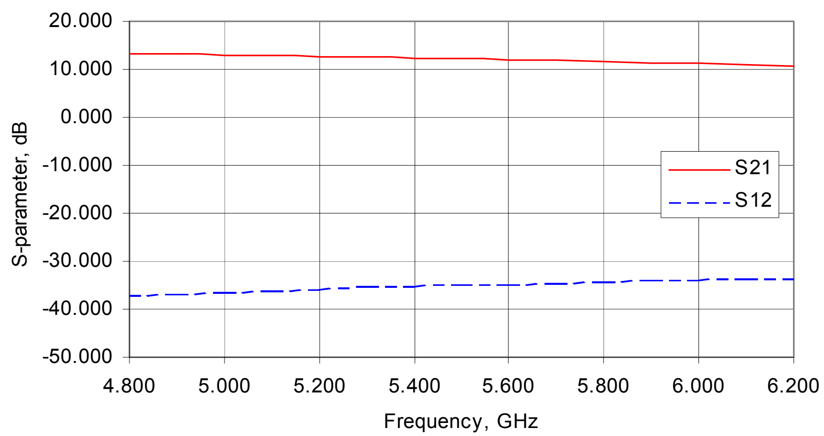


Figure 2.25: Simulated S_{21} and S_{12} of the LNA with series L match (v2).

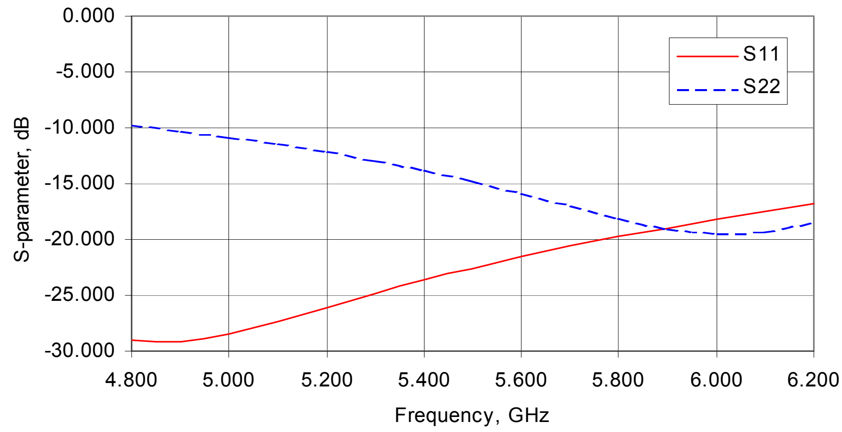


Figure 2.26: Simulated S_{11} and S_{22} of the LNA with series L match (v2).

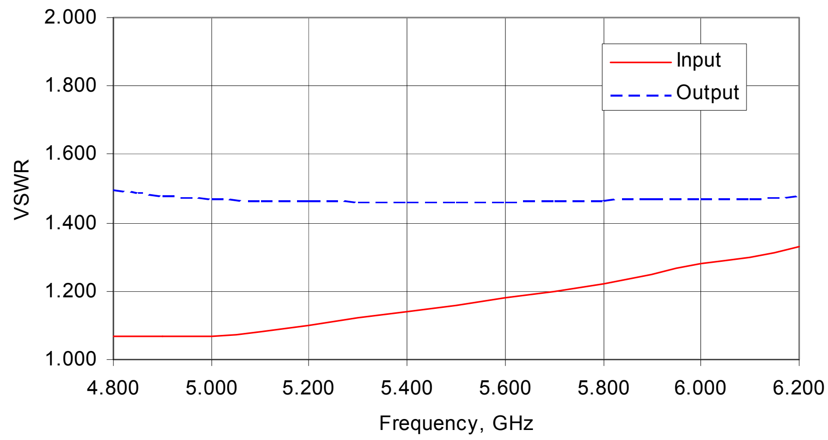


Figure 2.27: Simulated VSWR of the LNA with series L match (v2).

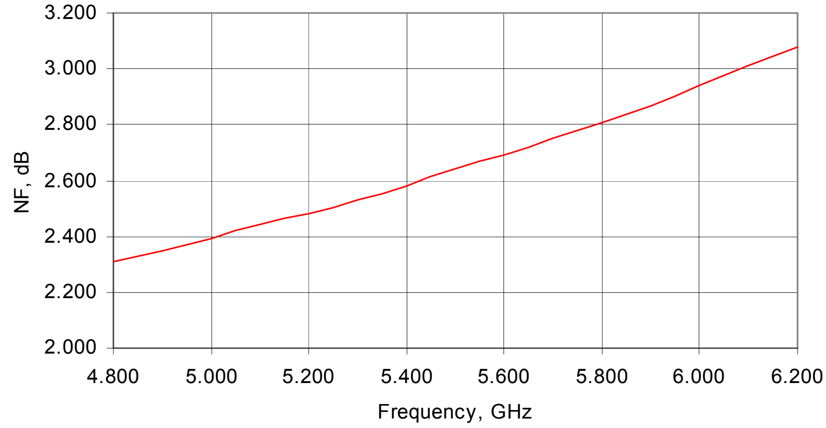


Figure 2.28: Simulated NF of the LNA with series L match (v2).

Table 2.3: Simulated stability criteria of the LNA with series L match (v2).

Freq (GHz)	Input Stability Coefficient (μ')	Output Stability Coefficient (μ)	k (50 Ω)
4.8	2.54	7.67	6.68
4.9	2.66	7.70	6.91
5.0	2.79	7.61	6.85
5.1	2.94	7.41	6.79
5.2	3.12	7.14	6.74
5.3	3.32	6.83	6.70
5.4	3.56	6.51	6.66
5.5	3.83	6.20	6.64
5.6	4.14	5.90	6.62
5.7	4.48	5.61	6.61
5.8	4.83	5.35	6.61
5.9	5.12	5.11	6.62
6.0	5.28	4.88	6.64
6.1	5.24	4.68	6.67
6.2	5.01	4.49	6.71

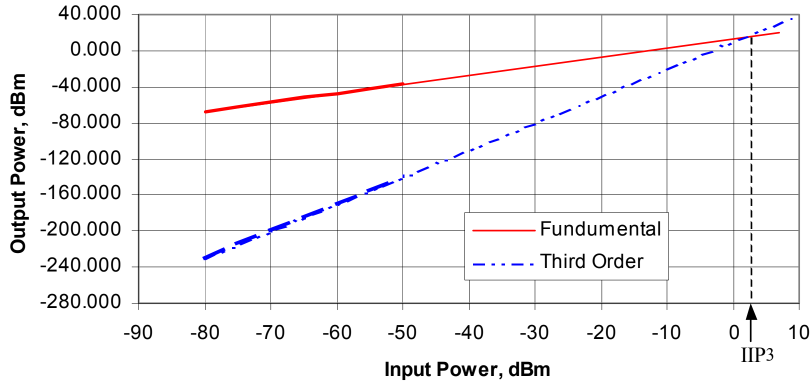


Figure 2.29: Simulated linearity of the LNA with series L output match (v2).

The linearity is shown in Figure 2.29. The resulting IIP3 was 1 dBm.

2.4 Layout and Bonding

Access to layout artwork for ADS is not available; therefore, the layout of the LNA was performed using Cadence Virtuoso [28] and IBM's design kit for Cadence v.2.1.

Bondpads with deep-trench isolation grids were used to reduce coupling between the pads and the circuitry. The dimensions of the pads were 75 μm x 75 μm, with a 100 μm pitch (center-to-center spacing) for the LC matched LNA, and a 100 μm vertical pitch and a 120 μm horizontal pitch for the series L matched LNAs. The size of the bondpads were chosen based on simulation. Smaller pads introduced less parasitics and provided a better match on the input and output of the LNA. However, further reduction in size to minimize parasitics were not possible since wire bonding difficulties would arise.

The signal bondpads were arranged to reduce coupling between the input and output bondwires. The inputs for the LNAs were placed so the bondwire would be at a 90 degree angle from the output bondwire. The power and ground bondpads were placed to provide the minimum routing distance to the attached devices.

Substrate contacts were placed throughout the layout to provide a low impedance

connection between substrate and ground. Also, Metal1 traces with substrate contacts were used to help isolate bondpads from other devices. Substrate contacts are important because of the low resistivity substrate. Placing substrate contacts to ground helps divert any signal to ground that might otherwise couple to neighboring devices via the substrate. A separate bondpad was used for substrate ground to prevent any noise from reentering the circuit through the signal ground. The ground pads were downbonded to the package ground paddle.

The devices were placed to minimize parasitics and coupling. The CE transistor was places close to the input bondpad to reduce the parasitic trace resistance. The on-chip inductors were placed away from signal paths and devices to reduce coupling. The devices associated with the biasing, such as resistors and bias transistors, were placed closer to the high frequency device to reduce the parasitics seen by the signal. The majority of the metal trace length was placed on the DC side of the bias networks.

All metal traces where sized according to current density rules. The top metal layer was thicker than the other two metal layers which allowed the metal layer to handle higher current densities for a given width. Therefore, top metal could be narrower and was used where ever possible to reduce parasitics. Multiple vias were placed where metal layer transitions were needed in an effort to minimize parasitic resistance and inductance.

To make optimal use of the available die area, both versions of the series inductor output matched LNAs were placed on a single die. Figure 2.30 shows the final layout of the series L matched LNAs The final layout of the LC matched LNA is shown in Figure 2.31. Both LNA die have an identical size of 0.74 mm x 0.54 mm.

Figure 2.32 shows the bonding diagram for the series L output matched LNA. Although both LNAs were to be wirebonded to the package, the intention was to have only one LNA active at a time to eliminate the potential for crosstalk between the two LNAs. The bonding diagram for the LC output match LNA was similar to the series L output matched LNAs, except with the single LNA bonded to the package.

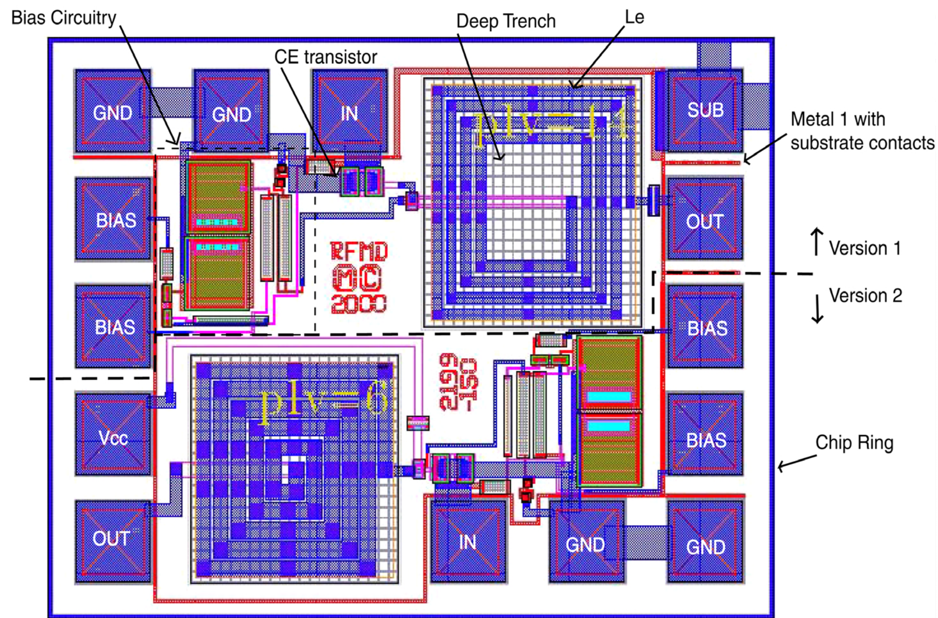


Figure 2.30: Layout of the LNAs with series L output match.

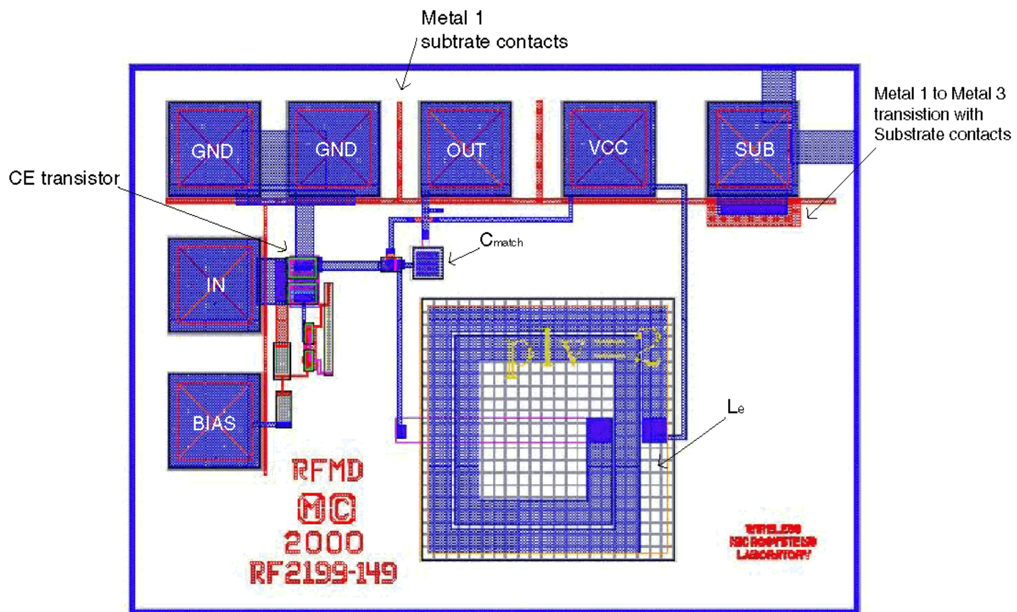


Figure 2.31: Layout of the LNA with LC output match.

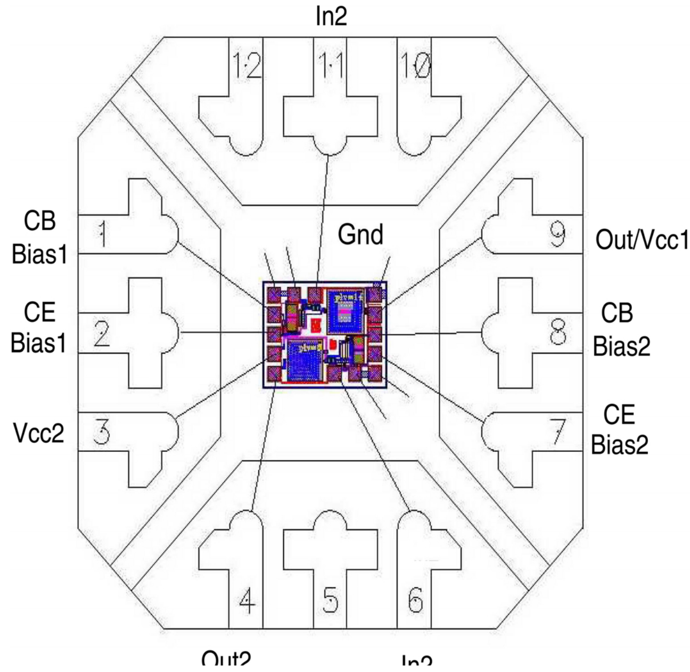


Figure 2.32: Bonding diagram of the LNAs with series L output match.

2.5 Summary

In summary, three LNAs were designed for the 5 GHz - 6 GHz band. All three LNAs use a single-stage cascode topology with emitter degeneration. Two of the LNAs use a series L match to achieve the output match, while the third uses an LC match. All critical components of the LNAs were integrated on-chip. The three LNAs all have a gain >10 dB, and are matched with a VSWR better than 2:1 at both ports, over the band of interest. The three simulated LNAs meet or exceed the goals set forth in Table 1.3. The total area used for each LNA die is 0.74 mm x 0.54 mm; the dies fit into 3 mm x 3 mm MLF-12 packages.

Overall, the simulated results are very competitive with previously presented results [29],[30],[31]. The simulated gains of the LNAs presented in this thesis are lower than other presented work due to the single-stage, fully matched topology used here, as opposed to multiple stage LNAs commonly seen in other works. The NF and linearity show improvement over many previously published papers. The improvement in noise figure (NF) and linearity may also be a product of the single-stage topology. The

additional stages of a multi-stage amplifier introduce added noise to the circuit. Also, a high gain in the first stage of multiple stage amplifiers leads to a reduction in the overall IIP3 by driving the subsequent stages into non-linear operation.

Chapter 3

LNA Implementation and Measurements

3.1 Fabrication

The low noise amplifiers (LNA) die were fabricated at IBM's Burlington SiGe Fab. The packaging and bonding of the die were done by RF Microdevices. Shown in Figures 3.1 and 3.2 are the photographs of the fabricated LNA circuits.

During the layout of the reticle, there was a issue with the die sizing. Compared to the die laid out for this project, the sizes of other unrelated die on the same reticle were much larger. Therefore, the dicing plan for the entire wafer required the die size for this project to be grown to 1.5 mm x 1.3 mm. Consequently, two of the original size LNA die were laid out on the larger die, and to accommodate the new die size, the package was changed to a 16 pin 4 mm x 4 mm MLF package This forced some bondwire lengths to be longer than originally designed for (Fig. 3.3).

3.2 Test Structures and Set-up

Coaxial system measurements of the LNAs were facilitated with 0.76 mm thick FR4 printed circuit boards (PCBs) with 1 oz. copper plating. The boards consist of front and backside metal layers, with microstrip signal traces on the top metal and a

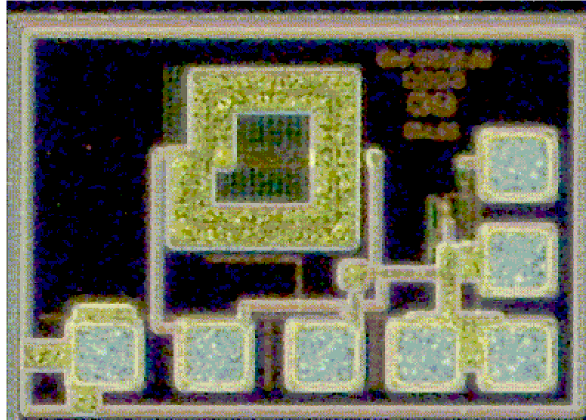


Figure 3.1: Photograph of the LC output matched LNA die.

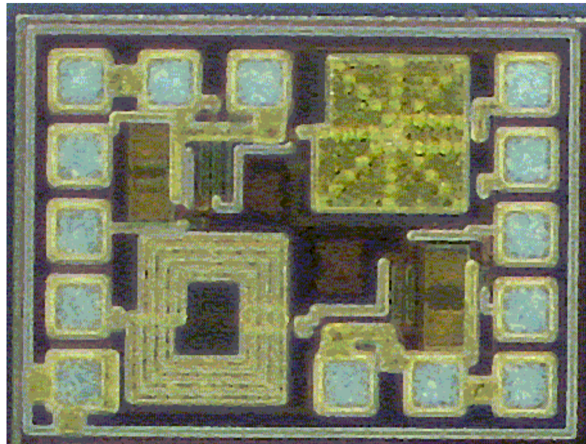


Figure 3.2: Photograph of the series L output matched LNA die (v2).

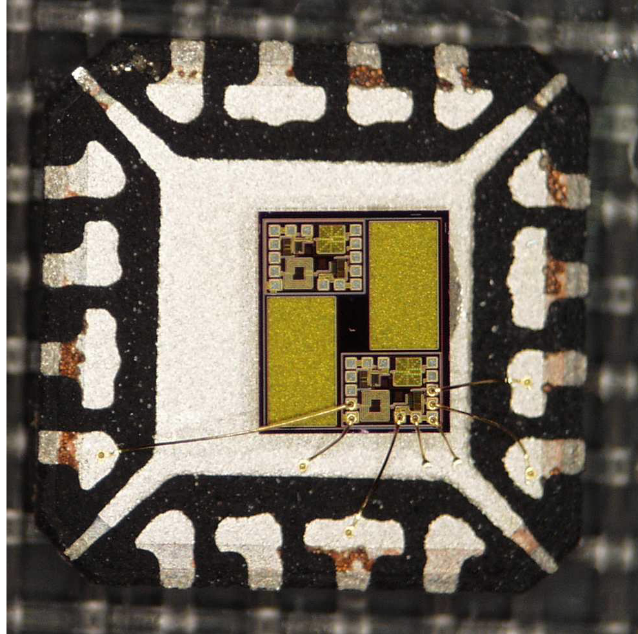


Figure 3.3: LNAs with series L output match in package.

ground plane on the backside metal. No ground plane was used on the top layer to reduce the chances of triggering coplanar waveguide modes. Subminiature assembly (SMA) connectors with direct launch center conductors were used to transition the signals from the coaxial cables to the test boards.

Figures 3.4 and 3.5 show the test boards used to characterize the LNAs. The widths of the input and output traces are approximately 1.27 mm, which gives a characteristic impedance of approximately 50 Ω. At the power pins, ground traces parallel to the power lines were placed to provide some tuning of the power supply filtering and decoupling using a surface mount (SMT) capacitor. By sliding the capacitor along the trace, the impedance at the power pin can be varied to provide an improved RF short or open circuit termination.

Calibration structures were used to calibrate out any parasitics and losses due to the test boards (Fig. 3.6). Through, open and quarter-wave delay line structures were used to perform a through-reflect-line (TRL) calibration. The lengths of the through and open standards were made identical to the trace lengths on the test boards to move the testing plane of reference to the RF input/output pins of the package. The NIST Multical software package [32] was used to measure and deembed

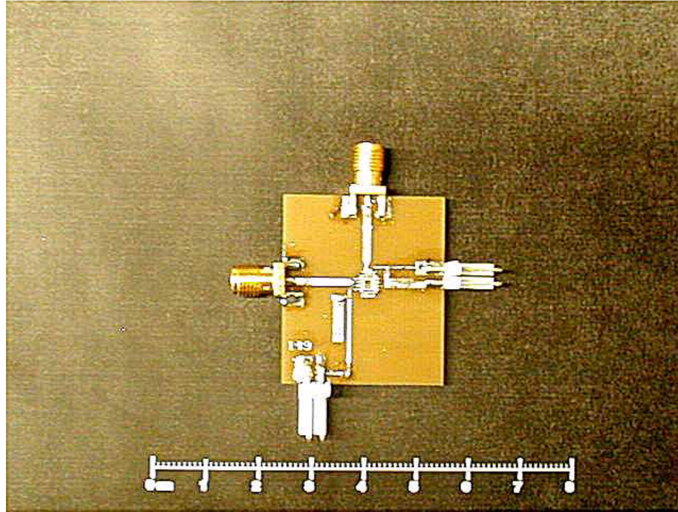


Figure 3.4: Photograph of the test board for the LNA with LC match. The board is standard FR4 with a 0.76 mm thickness. The input and output traces are 1.27 mm wide (50 Ω characteristic impedance). The package is grounded with vias to the backside of the board.

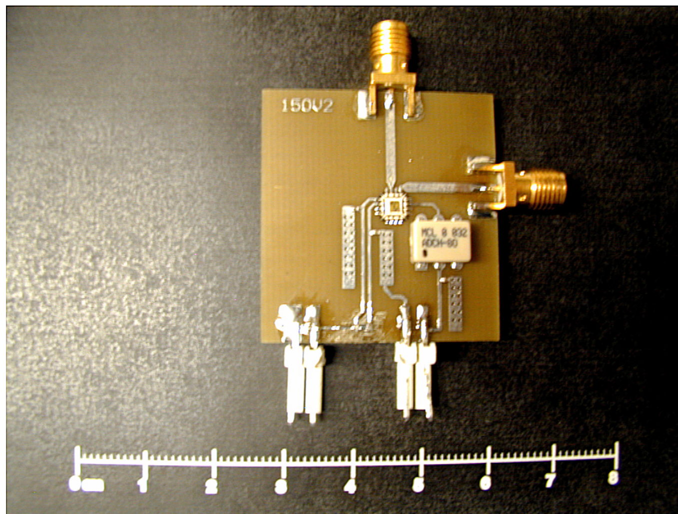


Figure 3.5: Photograph of the test board for the LNA with series L match (v2). The board is standard FR4 with a 0.76 mm thickness. The input and output traces are 1.27 mm wide (50 Ω characteristic impedance). The package is grounded with vias to the backside of the board.

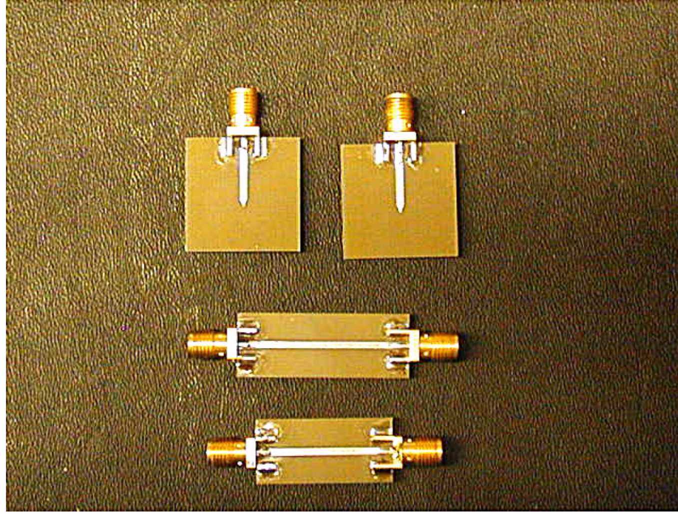


Figure 3.6: Standards used TRL calibration. The use of this calibration moves the test reference plane to the RF input/output pin of the package.

the information from the TRL calibration, and to load the calibration data into the network analyzer.

For S-parameter measurements, an HP 8510C rack system with the HP 8517B S-parameter test set (45 MHz - 50 GHz) was used (Fig. 3.7).

A single side band (SSB) noise figure (NF) was measured using an Agilent N8973A NF meter (10 MHz - 3 GHz) with a Agilent 346C noise source (10 MHz - 26.5 GHz) (Fig. 3.8). Since the NF meters upper operating frequency was limited to 3 GHz, a Mini-circuits ZMX-7GLHR (3.7 - 7 GHz) passive mixer was used to downconvert from the LNA operating frequency [33]. An HP83620B signal generator (10 MHz - 20 GHz) supplied the required LO signal for the mixer and was varied under the control of the NF meter from 6 GHz to 7 GHz to provide a constant IF frequency of 1 GHz. Terminated circulators at the input and output of the NF meter acted as isolators to reduce the reflections created by the poor VSWR of the Mini-Circuits mixer. The NF meter calibration was performed with the through PCB standard in place of the DUT; therefore, all the additional components (mixer, circulators, DC blocks etc...) as well as board losses were calibrated out of the measurement.

Linearity was measured using a standard two-tone test (Fig. 3.9). An HP 83620B signal generator produced the lower frequency tone and a S-parameter test set gen-

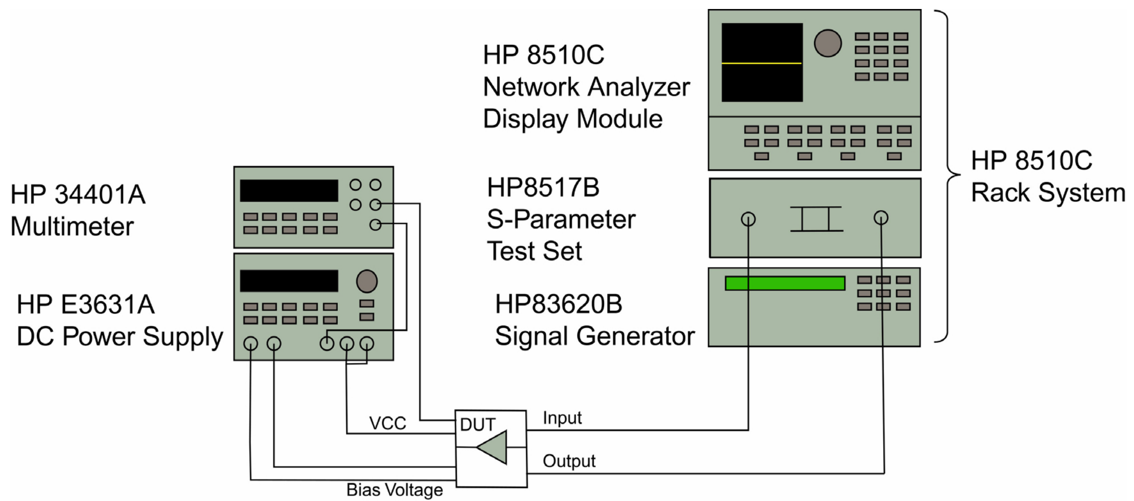


Figure 3.7: Test set-up used for LNA S-parameter measurements.

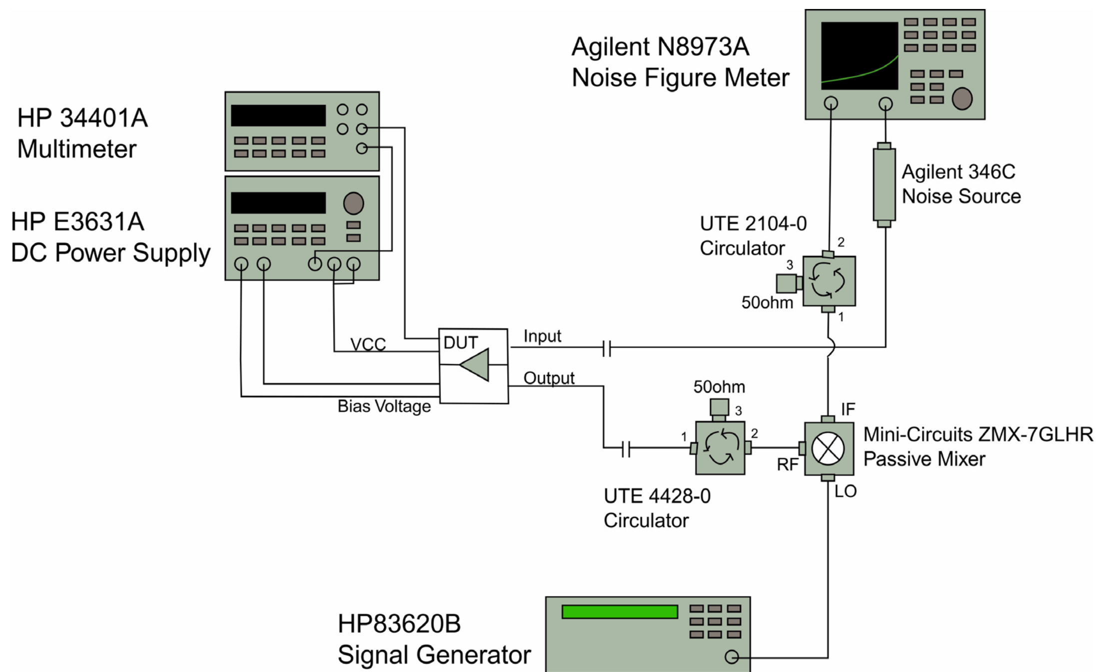


Figure 3.8: Test set-up used for LNA NF measurements.

erated the upper tone. Linearity in two bands were tested. A pair of tones at 5.25 GHz and 5.252 GHz tested linearity in the lower U-NII bands (5.15 GHz - 5.35 GHz), and a pair of tones at 5.775 GHz and 5.777 GHz tested linearity in the upper U-NII band (5.725 GHz - 5.825 GHz). A model 30057 Anaren hybrid (4 - 8 GHz) combined the two-tone signal prior to the input of the LNA. The output of the LNA was connected to a HP8563E spectrum analyzer (9 KHz - 26.5 GHz) to measure the output spectrum. The two signal sources were adjusted so the two tones had an equal -35 dBm power at the input of the LNA. In order to ensure accurate measurements, the tone power was chosen to be as low as possible to ensure the LNA and spectrum analyzer were both operating in their linear range, while being large enough to produce third-order intermodulation products (IMD3) above the noise floor of the spectrum analyzer. Once the measurements were taken, they were converted to a third-order intercept point (IIP3) using [17]:

$$IIP_3 = P_{in} + \frac{P_{out} - P_{IMD3_{out}}}{2} \tag{3.1}$$

.

3.3 LNA with Series L Output Match (v1)

The first version of the series L match LNA did not function properly. The reason is most likely associated with the external output inductor. At 5 GHz, the SMT inductor is near its series resonance frequency (SRF) of around 6 GHz. It is possible that the SRF was too low and led to instability in the LNA. Splitting the inductance into an on-chip component and off-chip component with the package parasitics in between may have created addition problems with the match not seen in simulations. Due to the poor performance of the LNA, full characterization was not performed.

3.4 LNA with Series L Output Match (v2)

The S-parameter results for the schematic shown in Figure 2.12 were measured at two common bias voltages, 3.3 V and 5.0 V, and at three different collector current

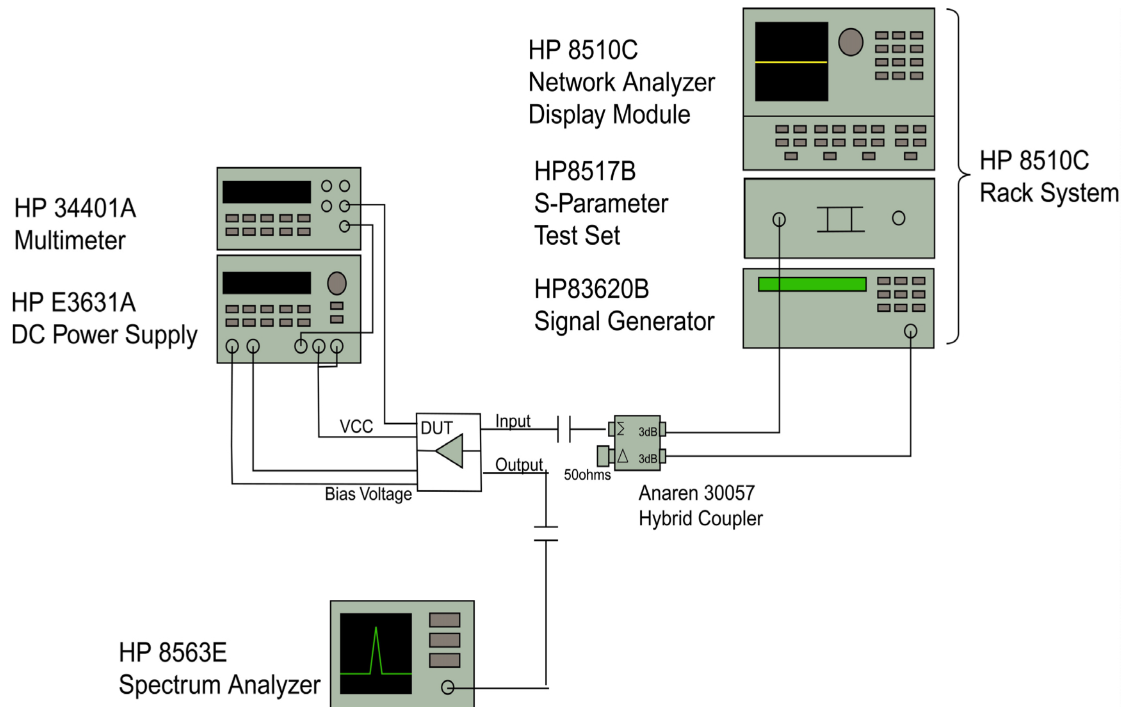


Figure 3.9: Test set-up used for LNA linearity measurements.

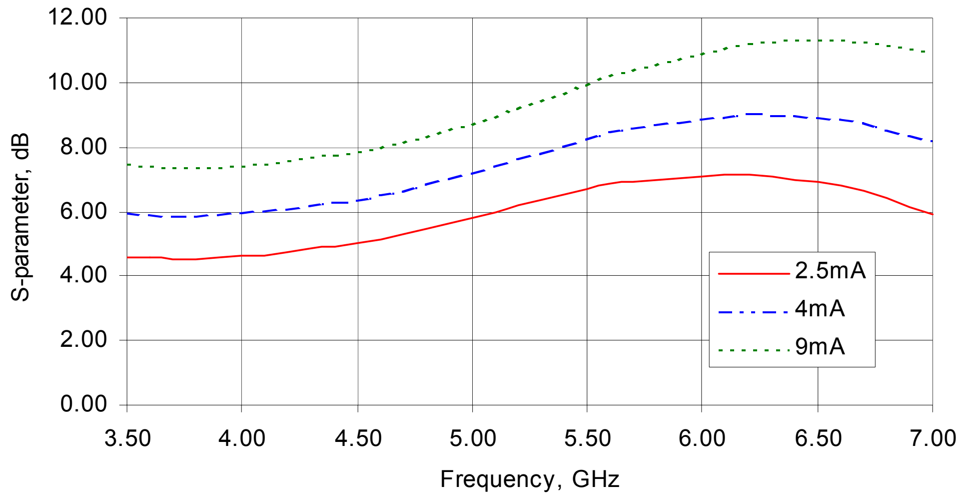
levels. Simulations were performed at 4 mA, therefore all measurements were taken at this bias current. In addition, currents of 2.5 mA and 9 mA were selected to show the variation in performance at different bias currents.

The gain for the LNA is shown in Figure 3.10. The gain at both voltage levels peaks at approximately 9 dB around 6.25 GHz with 4 mA bias. In the 5-6 GHz, band the gain is between 7.8 dB and 8.9 dB. Increasing and decreasing the biasing current changes the peak gain by about 2 dB. It also shifts the peak gain in frequency slightly.

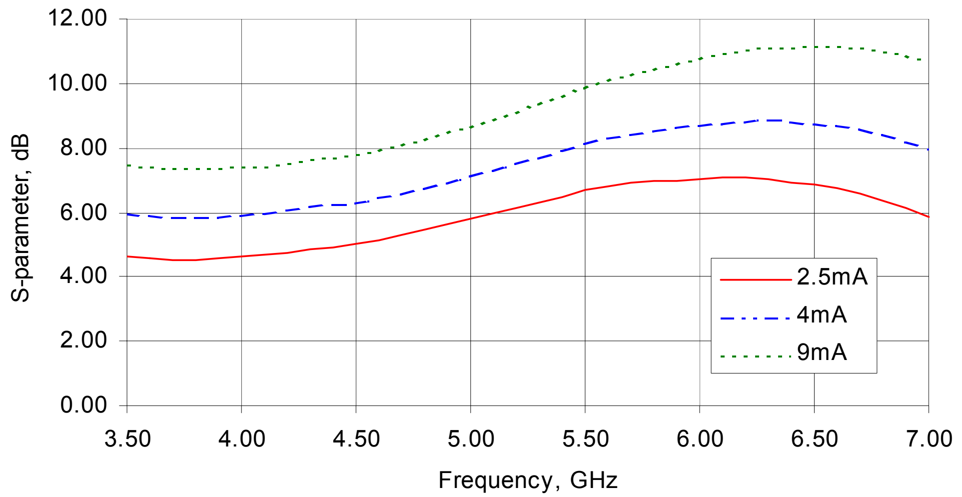
The input match of the LNA is shown in Figure 3.11. At 4 mA bias, the best match is obtained around 4.25 GHz. The best return loss is at a 2.5 mA bias. The match degrades with increased bias.

The input VSWR at 3.3 V, 4 mA is below 2:1 until 6 GHz; at 5.0 V, 4 mA the VSWR is below 2:1 until 6.2 GHz. Although the best overall match is obtained at 2.5 mA, the 2:1 VSWR bandwidth is the same as the 4 mA case.

The output match of the LNA is shown in Figure 3.12. At 3.3 V, 4 mA, the best

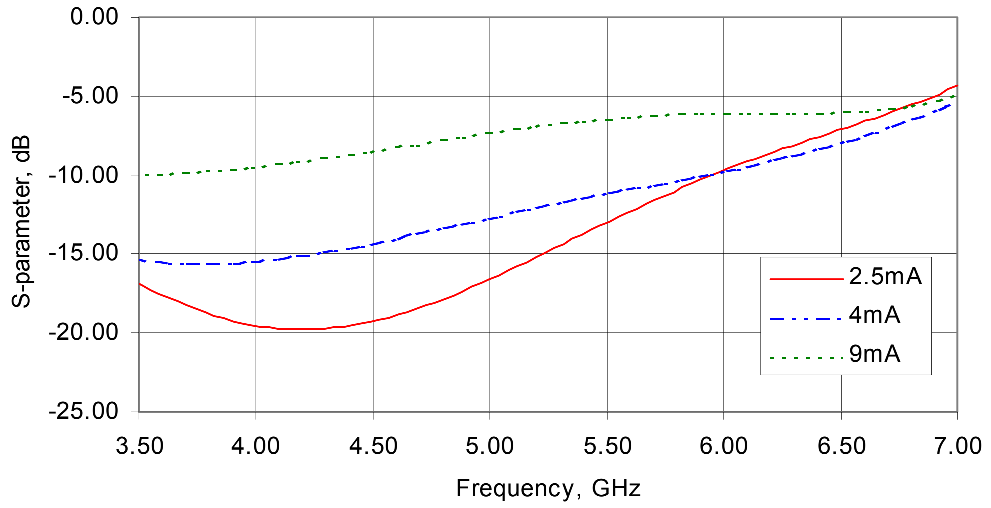


(a)

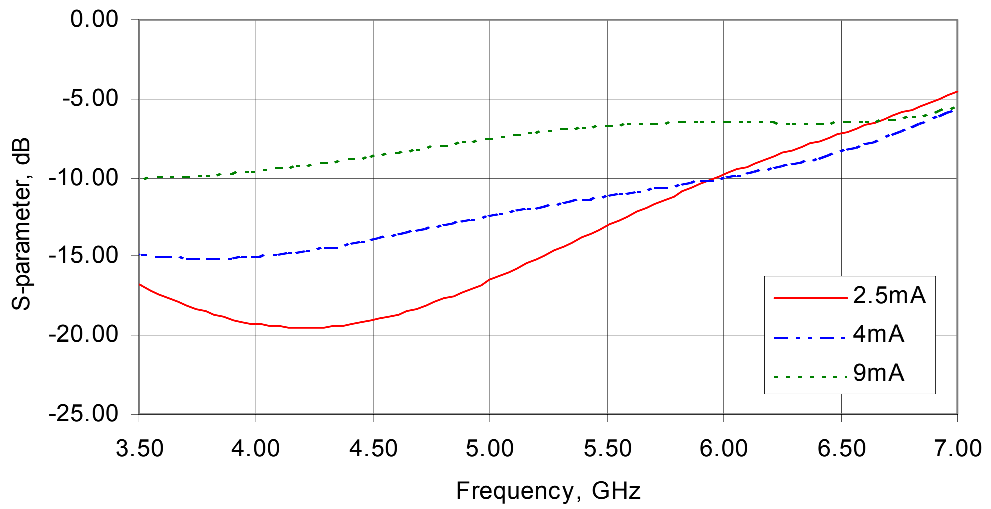


(b)

Figure 3.10: Measured S_{21} of the LNA with series L output match (v2) at (a) 3.3 V (b) 5.0 V.



(a)



(b)

Figure 3.11: Measured S_{11} of the LNA with series L output match (v2) at (a) 3.3 V (b) 5.0 V.

Table 3.1: Measured IIP3 of the LNA with series L match v2.

Voltage	**Current**	**IIP3 at 5.25 GHz**	**IIP3 at 5.775 GHz**
3.3 V	2.5 mA	0.19 dBm	-0.66 dBm
	4 mA	5.74 dBm	5.42 dBm
	9 mA	9.09 dBm	8.00 dBm
5.0 V	2.5 mA	1.19 dBm	0.00 dBm
	4 mA	6.42 dBm	5.83 dBm
	9 mA	10.24 dBm	9.34 dBm

match is obtained at 6.6 GHz, while at 5.0 V, 4 mA the best match is at 6.5 GHz. Overall, a bias level of 2.5 mA produces the best match at 3.3 V, while 4 mA produces the best match at 5.0 V.

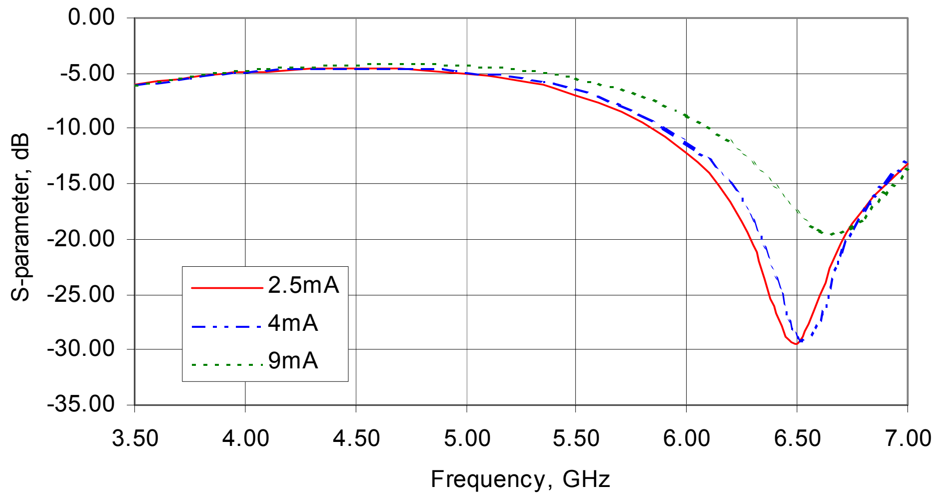
The output VSWR at 3.3 V, 4 mA is below 2:1 above 5.7 GHz; at 5.0 V, 4 mA the VSWR is below 2:1 above 5.9 GHz. With a 4 mA bias, the 2:1 VSWR bandwidth is greater than 1 GHz at 3.3 V and 5.0 V.

The reverse isolation of the LNA is shown in Figure 3.13. The isolation is around 25 dB at 3.5 GHz and decreases to 12 dB at 7 GHz. In the band of interest, the isolation is between 13.8 dB and 17.9 dB. The isolation is rather insensitive to supply voltage or bias current.

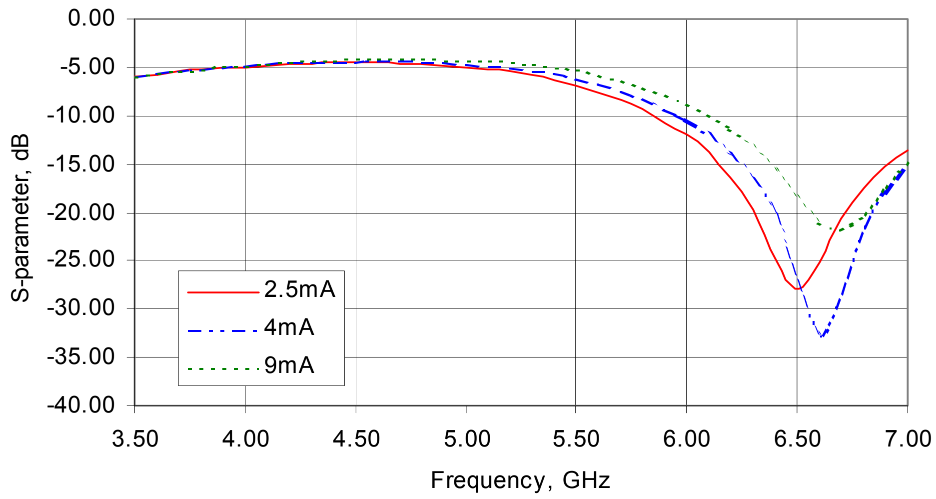
NF measurements at 3.3 V, 4 mA shows a maximum NF of 3.9 dB at 5.5 GHz (Fig. 3.14). The NF improves with an increase current bias and changes little with an increase in voltage level.

Figure 3.15 illustrates the two-tone measurement results. At 3.3 V, 4 mA the IIP3 is 5.74 dBm at 5.25 GHz and 5.42 dBm at 5.775 GHz. At 2.5 mA, the linearity decreases to 0.19 dBm and -0.66 dBm for 5.25 GHz and 5.775 GHz respectively. At 9 mA, the linearity increases to 9.09 dBm at 5.25 GHz and 8.00 dBm at 5.775 GHz. As expected, increasing the voltage supply or current bias increases the linearity of the circuit. Table 3.1 summarizes the linearity results.

While the *trends* of the measured results tend to match the simulated results, the values and frequency ranges do not. The output is best matched above the band of interest as simulations showed, but the measured match is shifted 500 MHz higher than predicted. This results in a poor output match over the 5-6 GHz band, but a

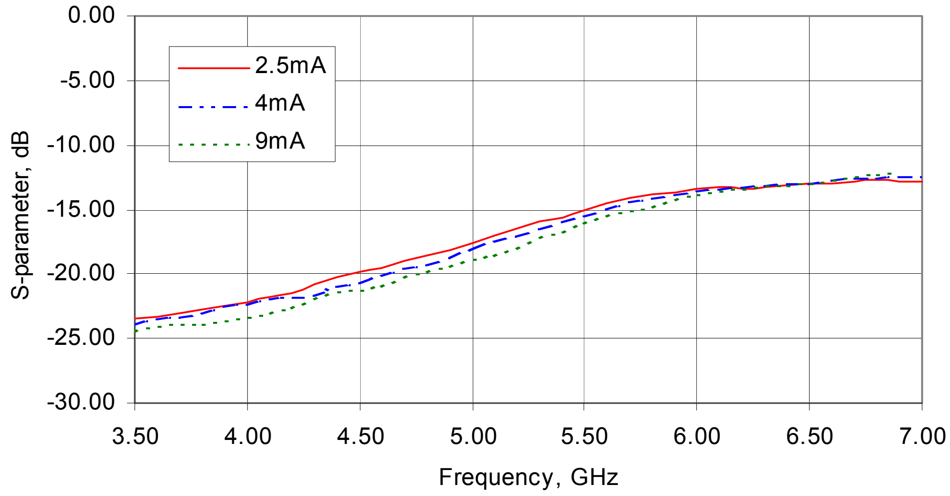


(a)

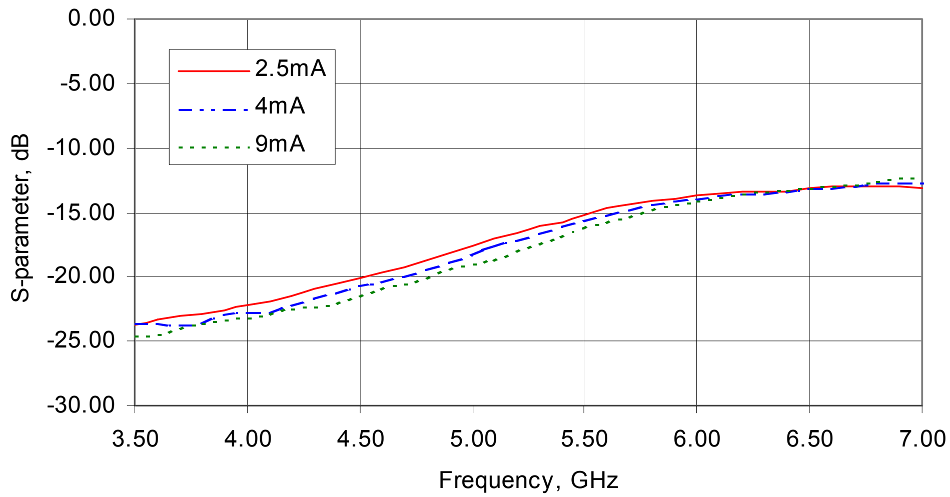


(b)

Figure 3.12: Measured S_{22} of the LNA with series L output match (v2) at (a) 3.3 V (b) 5.0 V.

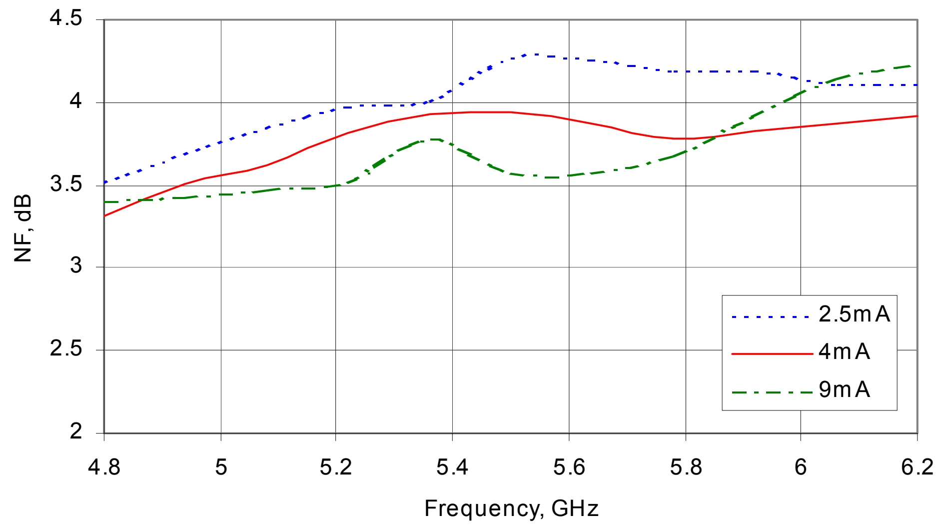


(a)

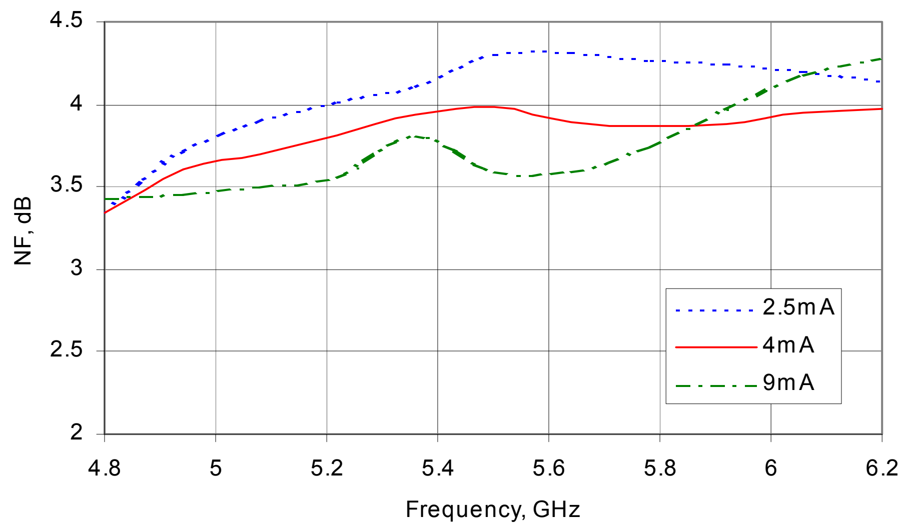


(b)

Figure 3.13: Measured S_{12} of the LNA with series L output match (v2) at (a) 3.3 V (b) 5.0 V.



(a)



(b)

Figure 3.14: Measured NF of the LNA with series L output match (v2) at (a) 3.3 V (b) 5.0 V.

(a)

(b)

Figure 3.15: Two-tone measurement of the LNA with series L output match (v2) at (a) 3.3 V, 4 mA (b) 5.0 V, 4 mA.

Table 3.2: Simulated and measured results of the LNA with series L match (v2).

Function	Simulated			Measured			Unit
	Min	Typ	Max	Min	Typ	Max	
Gain							dB
2.5 mA				5.9		7.0	
4 mA	11.2		13.0	7.3		8.9	
9 mA				8.8		11.0	
Reverse Isolation							dB
2.5 mA				13.3		17.3	
4 mA	-37.0		-33.5	13.5		17.7	
9 mA				13.6		18.6	
Input VSWR							
2.5 mA				1.3:1		2.0:1	
4 mA	1.1:1		1.3:1	1.6:1		2.0:1	
9 mA				2.5:1		3.0:1	
Output VSWR							
2.5 mA				1.6:1		3.5:1	
4 mA		1.5:1		1.7:1		3.6:1	
9 mA				2.0:1		4.0:1	
NF							dB
2.5 mA				3.8		4.1	
4 mA	2.4		2.9	3.6		3.9	
9 mA				3.5		4.1	
Input IP3							dBm
2.5 mA				-0.7		0.2	
4 mA		1.0		5.4		5.7	
9 mA				8.0		9.1	

good match from 6.5-7.5 GHz. For the input match, simulated results predicted a VSWR less than 1.5:1 over the 5-6 GHZ band with the best input match occurring at 4.9 GHz. Measured results show the best input match shifted lower in frequency to 4.2 GHz while maintaining less than 2:1 VSWR in-band. Table 3.2 compares the simulated and measured results.

Overall, the measured results are worse than what simulations predict. The input and output VSWRs are higher than simulated, which also explains why the measured gain is lower. The reverse isolation is also much worse, off by more than 20 dB at some frequencies. The linearity is the only figure of merit (FOM) that is better than

simulated. This may also be attributed to the poor match, and hence, lower gain of the circuit.

Because the equipment required to externally tune the input and output matches was not available during the testing, it was not possible to tune the output and input to help diagnose the problem. In addition, time constraints did not permit the fabrication and testing of a second design iteration. Some speculation on the sources of the discrepancies between simulations and measurements include:

- *Larger die than anticipated* - The last minute change in the die size increased the length of the output bondwire adding more inductance to the match which wasn't taken into account in simulations. The increased inductance may be partially responsible for the shift seen in the output match. In addition, the die did not fit the larger package well. This lead to more variation in the placement of the die on the package making bondwire lengths less predictable.

- *Poor placement of the inductors* - Substrate contacts placed in the vicinity of the inductors may have reduced the quality factor (Q) of the inductors leading to increased loss. This may have lead to the lower gain, poor matching and a higher NF.

- *Poor substrate modeling* - Some substrate effects were modeled by estimating the resistance between a given device and the closest substrate contact. Given the low resistivity of the Si substrate, poor estimates may have lead to inaccurate simulations. In addition, the simulations could not account for the substrate effects created by device layout.

- *Unknown inductor contact* - There was some confusion as to how an internal node in the inductor model should be connected in simulation. The node was not a physical node, but one for simulation purposes only. There was conflicting information on whether to connect the node to the RF ground in the schematic or to an ideal RF ground. It was decided to connect the inductor to the chip RF ground. This choice greatly affected other design choices in the circuit.

- *Inaccurate package models* - The package models have been used at frequencies as high as 2.4 GHz. However, they have never been verified in the range of 5 - 6

GHz. It was later discovered that the package may have had several resonances in the band of interest.

- *Inaccurate bondpad models* - There have been studies showing the drastic effects bondpad parasitics can have at these frequencies [34]. However, simulations did not show as large an impact on the design as these studies predict, calling into question the bondpad model validity from 5 -6 GHz.

- *Voltage biasing circuitry design* - The emitter of the reference transistor in the current mirror was connected to the emitter of the CE transistor; the emitter degeneration bondwires were attached to both transistors. This was originally done to provide more accurate voltage biasing. However, this may have reduced the effectiveness of the emitter degeneration since the emitter of the CE transistor sees the reference transistor's emitter impedance in addition to the bondwire impedance .

It should also be noted that when measuring the LNA, the bias circuitry in the LNA required more current than anticipated in order to produce the desired current level in the LNA. It is suspected that the beta of the transistors used in the mirror was lower than anticipated, resulting in an error in the mirror current ratio. Since the bias pin was separate from V_{CC}, the current error was easily compensated for by increasing the current on the bias side of the LNA.

3.5 LNA with LC Output Match

The S-parameter results for the schematic shown in Figure 2.14 were measured at three different collector current levels. Once again, the current bias levels were chosen as 2.5 mA, 4 mA, and 9 mA. It was not possible to test the LNA at V_{CC}=5.0 V since this would lead to collector-emitter breakdown in the CE transistor.

Shown in Figure 3.16 is the gain of the LNA. The gain peaks at approximately 10.1 dB at 3.75 GHz with 4 mA bias. The gain with a 4 mA bias is 7.2 dB at 5 GHz, falling to 4.3 dB at 6 GHz. Increasing and decreasing the biasing current increases and decreases the peak gain by about 1 dB, respectively.

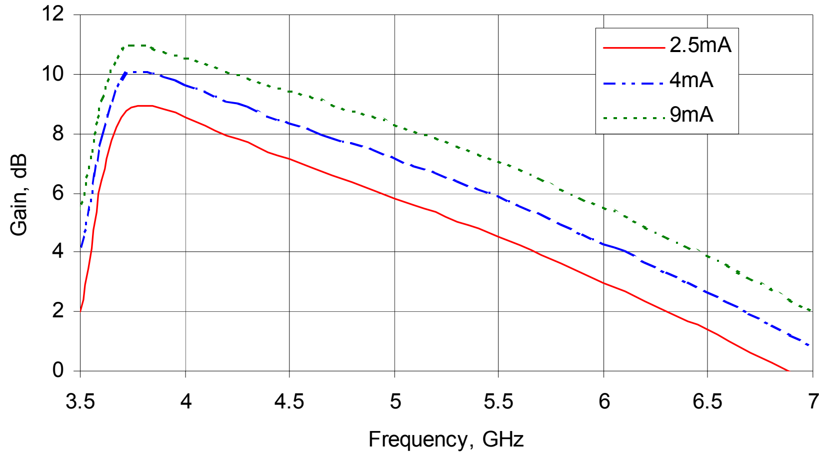


Figure 3.16: Measured S_{21} of the LNA with LC output match at 3.3 V.

At 4 mA, the input return loss for the LNA varies between 6.8 dB and 6.4 dB in the 5-6 GHz band (Fig. 3.17). The VSWR for the input does not fall below 2:1 over the measured frequency range but is below 3:1 from 3.8 GHz to 6.1 GHz. There is little change in input match when the current bias is changed.

The measured results for the output match are shown in Figure 3.18. The return loss at a 4 ma bias is between 7.2 dB and 6.4 dB from 5 - 6 GHz. As with the input match, the output match is rather insensitive to current bias levels. Also, the output match does not fall below a 2:1 VSWR. The best VSWR in the band is 2.5:1 at 5.3 GHz.

The isolation follows a similar trend to the series L matched LNA. Figure 3.19 shows that at 4 mA, the highest isolation is 26.9 dB at 3.5 GHz. The isolation is greater than 16.5 dB over the band of interest for all current levels.

The measured results for linearity are shown in Table 3.3. The linearity at a 4 mA bias is 7.60 dBm and 7.49 dBm for 5.35 GHz and 5.775 GHz, respectively. Once again, increasing the bias current increases the linearity of the LNA.

The measured results of the LNA with the LC matched follow the same basic trends as simulations predict, while the values do not. The measurements show worse gain and match than what simulations predict. The NF is also higher than predicated. As with the LNA with series L match, the linearity is the only FOM that is better

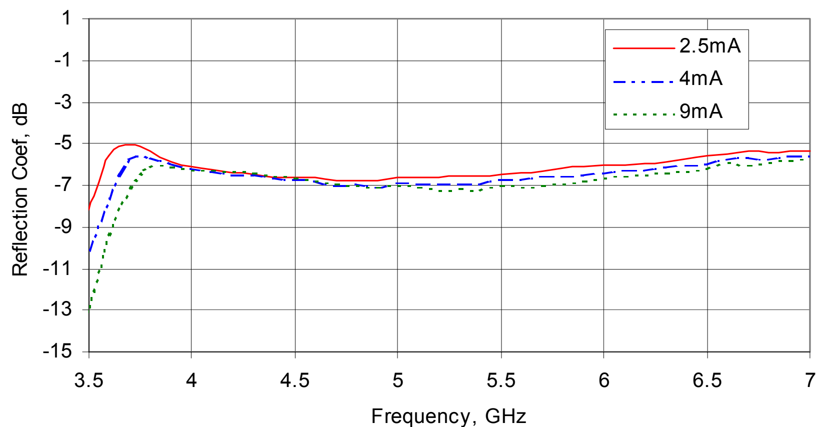


Figure 3.17: Measured S_{11} of the LNA with LC output match at 3.3 V.

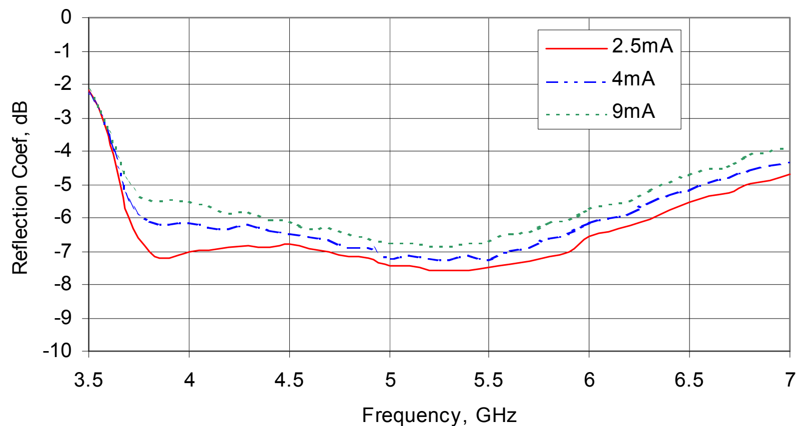


Figure 3.18: Measured S_{22} of the LNA with LC output match at 3.3 V.

Table 3.3: Measured IIP3 of the LC matched LNA.

Voltage	**Current**	**IIP3 at 5.25 GHz**	**IIP3 at 5.775 GHz**
3.3 V	2.5 mA	2.82 dBm	3.52 dBm
	4 mA	7.60 dBm	7.49 dBm
	9 mA	11.42 dBm	17.00 dBm

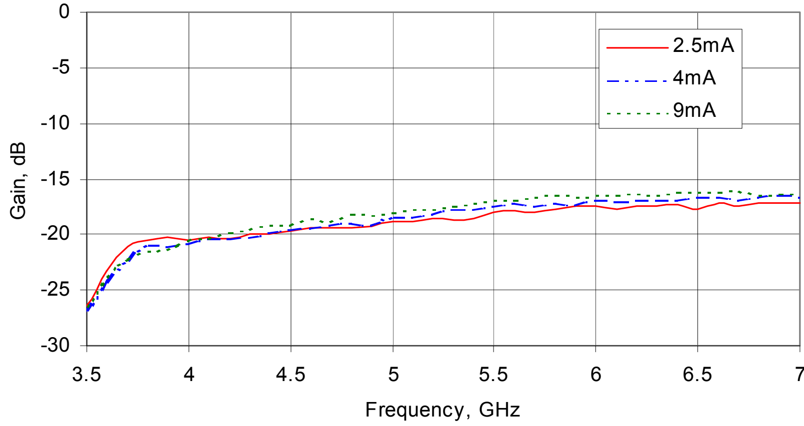


Figure 3.19: Measured S_{12} of the LNA with LC output match at 3.3 V.

than simulated. This is most likely for the same reason given for the previous LNA – the lower-than-simulated gain increases the linearity.

A summary of the simulated and measured results from 5-6 GHz is shown in Table 3.4.

The LNA with series L match and LC match have in common much of the same basic topology. They both use the same transistor sizes, bondwire degeneration, packaging, and current bias circuitry. The major difference between the two LNAs is the output match. It is therefore likely that many of the discrepancies seen between simulations and measurements will be similar in both LNAs. This is what is observed for most of the FOMs with the exception of the impedance matching. The port matching is much worse on the LC matched LNA than the series L matched LNA. This can be explained by the observed sensitivity of the LC matched LNA's to the RF termination at V_{CC}. Compared to the series L matched LNA, the output and input match of the LC matched LNA was very sensitive to this termination. Measurements of the LC matched LNA were taken with several different external terminations in an attempt to provide the RF with the most ideal short circuit termination, but no optimal solution could me obtained. Therefore, the poor input and output matchs were further degraded by the poor RF termination at V_{CC}.

Table 3.4: Simulated and measured results of the LNA with LC match.

Function	**Simulated**			**Measured**			**Unit**
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	
Gain							dB
2.5 mA				3.0		5.8	
4 mA	9.8		11.6	4.3		7.2	
9 mA				5.5		8.3	
Reverse Isolation							dB
2.5 mA				17.5		18.8	
4 mA	21.0		22.2	17.0		18.4	
9 mA				16.4		18.0	
Input VSWR							
2.5 mA				2.7:1		3:1	
4 mA		1.8:1		2.6:1		2.8:1	
9 mA				2.5:1		2.7:1	
Output VSWR							
2.5 mA				2.4:1		2.8:1	
4 mA		1.4:1		2.5:1		2.9:1	
9 mA				2.7:1		3.1:1	
NF							dB
2.5 mA				2.7		3.1	
4 mA	2.1		2.4	2.6		3.0	
9 mA				2.9		3.2	
Input IP3							dBm
2.5 mA				2.8		3.5	
4 mA		4.0		7.5		7.6	
9 mA				11.4		17.0	

Chapter 4

Mixer Design and Simulation

4.1 Background on Sub-harmonic Mixing

In sub-harmonic mixing (the following discussions will focus on receive mixers; however, the same general concepts are applicable to upconversion as well), the input signal is mixed with an integer multiple of the LO frequency to produce the desired output frequency ($f_{IF} = |f_{RF} - nf_{LO}|$). Sub-harmonic mixers (SHM) have several advantages over fundamental mixers which make them useful for many applications. Since the frequency mixing with the RF is at some multiple of the LO frequency, LO leakage is easily filtered at the RF port; therefore, SHMs can have a high degree of LO/RF isolation. This is particularly important in reducing LO radiation from the antenna of receivers. In addition, SHMs reduce the demand on the voltage controlled oscillators (VCOs) and frequency synthesizers by reducing the required LO frequency. This can lead to lower cost and higher performance LO sources. In the U-NII band, SHMs are very convenient in this respect because frequency synthesizers and VCOs designed for the 2.4 GHz ISM band can be used with little or no modification.

Sub-harmonic mixing has been used in a wide variety of applications, the majority being at microwave/millimeter-wave frequencies. In the past, SHMs have been typically implemented as passive mixers. Antiparallel diode topologies, ring diode mixers and resistive HFET mixers are just of few of the topologies that have been successfully demonstrated [35],[36],[37],[38]. Recently, there has also been research into using *active* SHMs at lower RF/microwave frequencies (<6 GHz). Although active mixers

have higher power consumption and lower linearity than passive mixers, they have the advantage of positive (dB) conversion gain and lower LO power requirement.

The recent interest in SHMs at the lower frequencies is mostly due to the increasing popularity in direct conversion architectures [39]. The most critical issue in direct conversion is the DC-offset at the IF port of the downconversion mixer created by self-mixing of the LO. This DC offset can corrupt signals which lie close to DC, and may saturate subsequent stages.

LO self-mixing occurs when the LO signal arrives at the RF port and mixes with itself to create a DC offset. The LO signal can reach the RF port by several means, the most significant being radiation from the LO source, substrate coupling and low mixer LO/RF isolation. The use of sub-harmonic mixing has shown promise in addressing these issues. In a SHM, the LO is at an integer fraction of the frequency which mixes with the RF signal; therefore LO radiation and leakage will not self-mix.

4.2 Sub-Harmonic Mixer Design

4.2.1 Topology

Several SHM topologies were considered for the mixer in this thesis. In [40], an active SHM topology using pulse-width modulation was proposed for a direct-conversion receiver. As mentioned in the introduction, it was decided to first implement the LNA and mixer independently before designing a direct conversion receiver. Therefore, the mixer in this project was designed as though intended for operation in a heterodyne system. The pulse-width modulated mixer cannot operate in a heterodyne receiver due to the nature of its operation. The topology relies on the phase difference between the LO signal and the RF input signal to produce the IF. In a heterodyne system, phase error would accumulate due to the significant frequency difference of the LO and RF signals. Therefore, it was not pursued in this thesis.

Alternatively, active topologies based on the familiar Gilbert-cell mixer (Fig. 4.1)have been reported in [41] and [42]. A Gilbert-cell has several key advantages which make it ideal for a mixer. In a heterodyne architecture, a doubly-balance Gilbert-cell displays a high degree of isolation for all ports due to the differential topology. The

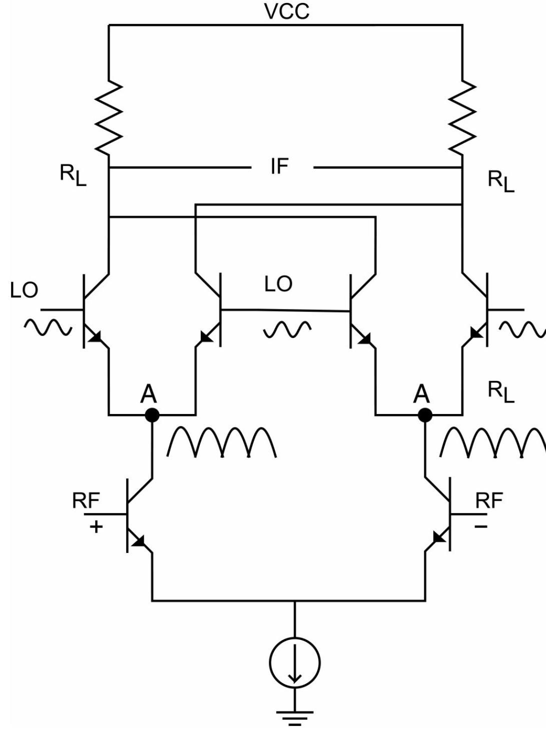


Figure 4.1: LO signal at the RF port of a double balanced Gilbert cell mixer.

LO signal at each branch of the differential RF port appear in phase at point A in Figure 4.1, and cancel to provide excellent LO/RF isolation. This makes the Gilbert-cell mixer well suited for a direct-conversion system. In addition, the balanced nature of the topology generates less even-order harmonics, lowering the beat components which can potentially corrupt the IF signal (or in the case of a direct conversion receiver, the baseband signal).

The mixer proposed in [41] is similar to a doubly-balanced Gilbert-cell mixer with two switching stages in series (Fig. 4.2). In [42], the Gilbert-cell mixer is modified by adding an additional transistor in parallel to each transistor in the RF transconductor. Both basic mixer topologies can operate as a heterodyne mixer with no modifications; however, the work in [42] was not published when the mixer design in this thesis was performed. Therefore, the stacked switching stage method of sub-harmonic mixing was chosen as the basis for the mixer design.

For the topology in Figure 4.2, when the switching core of the SHM is driven with I/Q LO inputs at one half the desired mixing frequency, the overall switching core appears

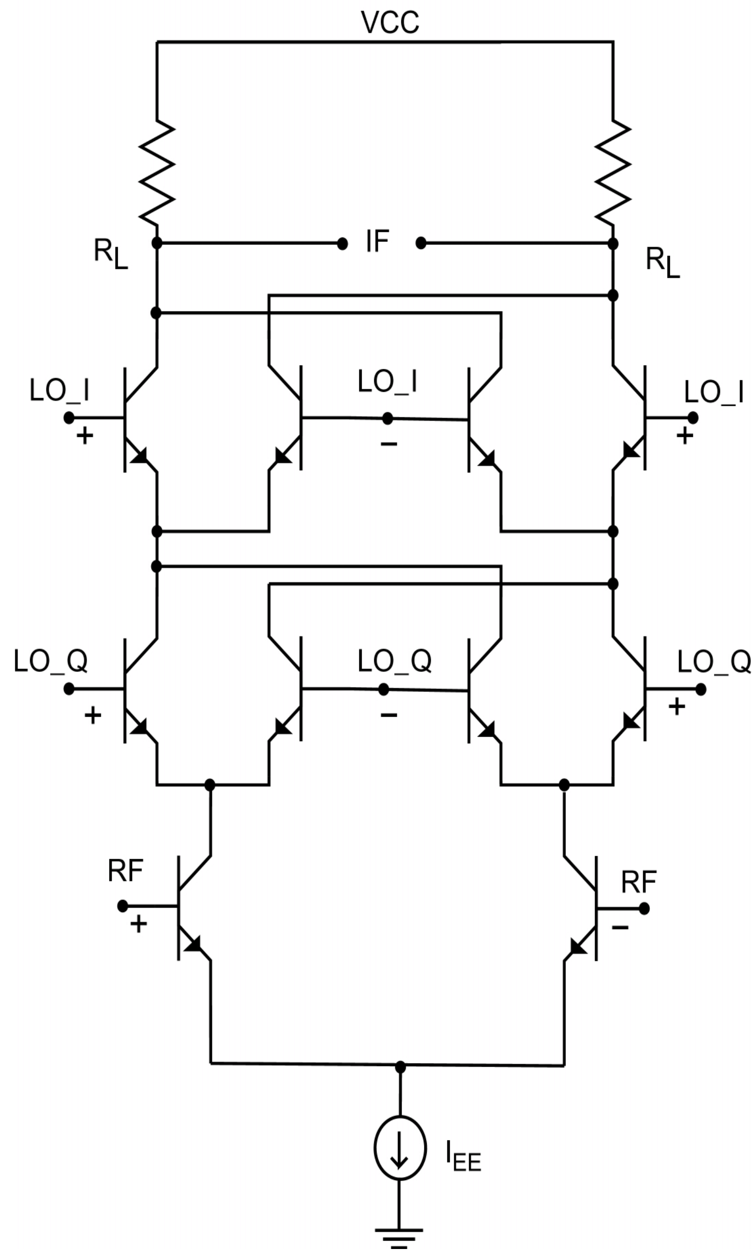


Figure 4.2: Basic topology of the sub-harmonic mixer.

to be switching at LO_Q*LO_I=2*LO (Fig. 4.3). The RF current sees the twice LO frequency (2LO) switching waveform resulting in mixing to the IF. This form of sub-harmonic mixing differs from the conventional passive mixer which uses the non-linearity of a device to mix the RF with a higher harmonic of the LO. Therefore, the expected 3 dB degradation in conversion gain for every doubling of the harmonic number of the LO does not apply to this topology.

If the LO signals are ideal I/Q differential signals, the 2LO signal will cancel at the RF port and the 2LO/RF isolation will be excellent. In fact, it has been shown that the 2LO rejection is relatively insensitive to I/Q mismatch, being more of a function of the *duty cycle* of $V_{LO,Q}$ and $V_{LO,I}$ [41].

Although this SHM topology shares many of the benefits associated with a standard Gilbert-cell mixer, the additional switching stage reduces the voltage headroom of the mixer. Assuming a 3.3 V supply and a turn-on voltage of 0.85 V for each transistor:

$$I_E R_{EE} + v_{be_{RF}} + v_{be_I} + v_{be_Q} + I_C R_L = 3.3V \quad (4.1)$$

$$I_E R_{EE} + I_C R_L \approx 0.75V \quad (4.2)$$

The addition of an extra switching stage leaves a minimum of 0.75 V to be split between the load and biasing circuitry. If a large voltage gain is needed, gain compression can become a problem.

4.2.2 Design

To improve the headroom of the mixer, several solutions were explored. An obvious solution was the use of inductors in place of resistors to eliminate the DC voltage drop across the load of the mixer. While this would be an excellent solution if off-chip inductors were used, the size and low quality factor (Q) of on-chip inductors made this solution less attractive. The use of bondwires to eliminate the voltage drop in the current biasing circuitry was also considered, but the bondwires provided insufficience inductance. Instead, the RF section of the mixer was biased in parallel to the switching core as shown in Figure 4.4.

Capacitive AC coupling was used between the two sections, allowing the RF section and switching section to each operate with the full 3.3 V supply [43]. A simple way of

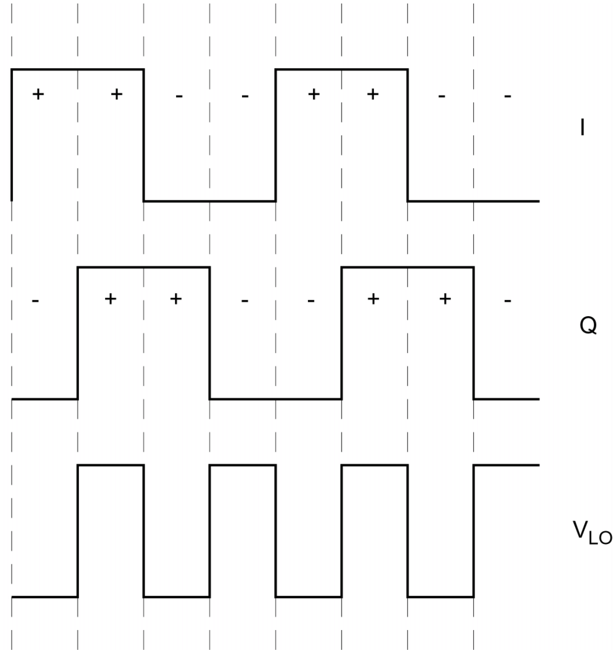


Figure 4.3: Generation of the 2LO signal from the I/Q inputs.

viewing the circuit is as a differential pre-amplifier driving a mixer with a resistive RF stage. It has been shown in [44], that a resistive RF stage lowers the conversion gain and isolation of a mixer; however, the addition of a pre-amplifier helps compensate for these losses. The drawback to this approach is the mixer can no longer current share between the switching stage and the RF section; thus, this scheme consumes more power.

The additional headroom afforded by the parallel biasing allowed the use of higher load resistor values and a slightly increased bias current. This increased the possible voltage and power gain of the mixer. The transistors in the switching section were sized according to the collector current they were required to handle. No attempt to match the LO port was made at this point since on-chip LO buffering was planned.

The design of the RF section consisted of trade-offs between linearity, power consumption, noise and input matching. Two common topologies for the RF section were explored in the design. As was used in [41], the multi-tanh approach was considered, but the difficulty in providing a 50 Ω differential match made it a less attractive choice. Instead, inductive emitter degeneration was used. A single 0.6 nH inductor

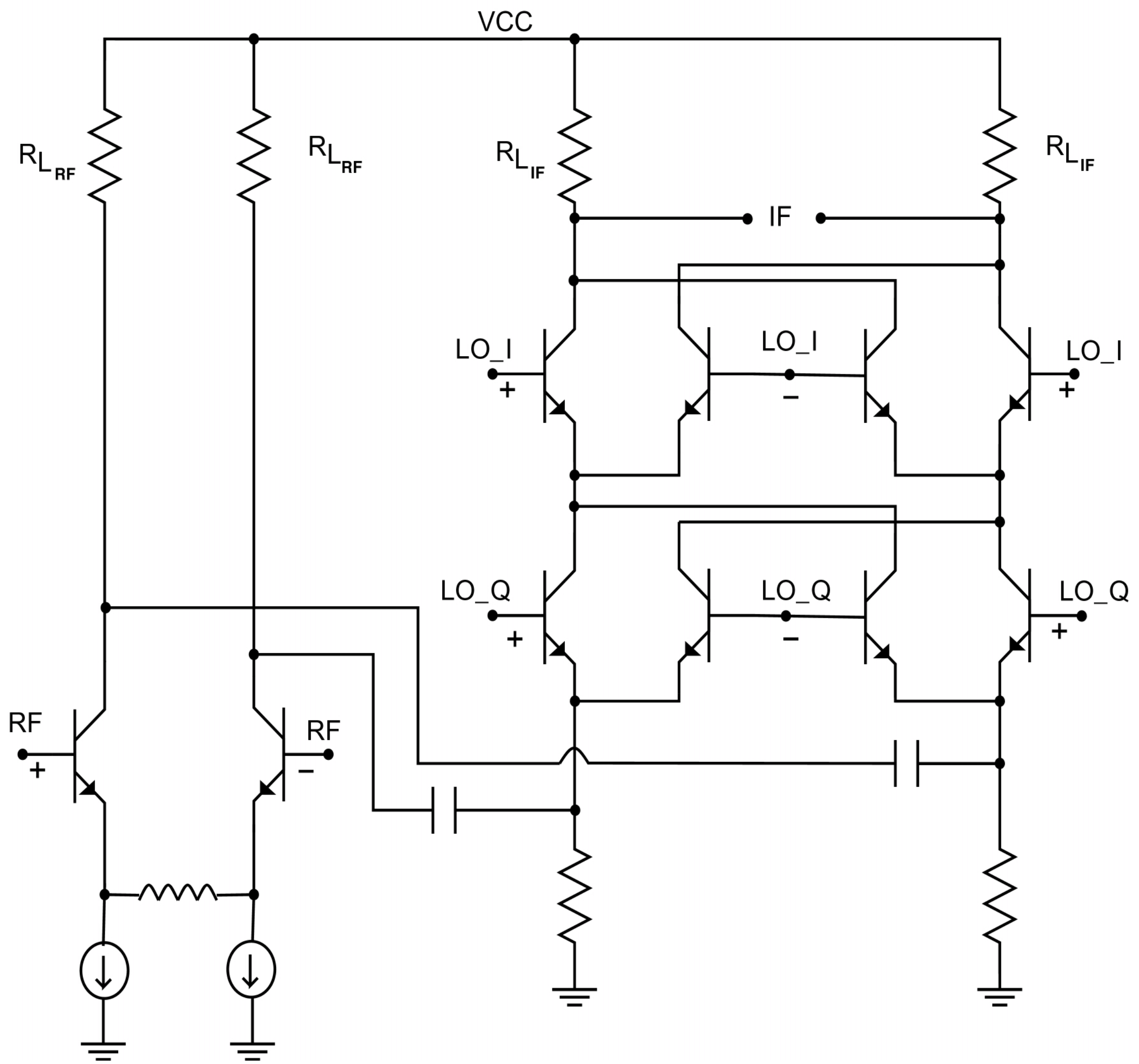


Figure 4.4: Mixer with resistive RF section and decoupled RF transconductor.

was used between the two emitters of the RF transistor pair. The two RF transistors were each sized to 25 um x 0.5 um x 2.

While the inductance value did provide a 50 Ω match over the band, it was not large enough to sufficiently linearize the RF section; therefore, linearity was traded for a better match. It should be noted that in a follow-on direct conversion receiver, 50 Ω RF input matching is not required. Therefore, better optimization of the linearity will be possible.

Like the LNA, the mixer design used an MLF leadless package. The same approach to bondwire and package modeling was taken for the mixer.

4.2.3 Biasing

The switching section and the RF section were biased at a total current of 2.8 mA each. To bias the RF section of the mixer, current mirrors with resistive degeneration were used. The degeneration helped minimize the imbalance in the differential signal. It can be shown that the output resistance of a bipolar current mirror with resistive degeneration is represented by [45]:

$$R_o \simeq r_o(1 + \frac{IcR_E}{V_T}) \tag{4.3}$$

where r_o is the small signal resistance output resistance, V_T is the thermal voltage (25.9mV at 298 K), and R_E is the resistor value used for the degeneration.

The resistors used to degenerate the mirror were chosen to see approximately a 200 mV drop. The result is an increase in output resistance equal to about $8r_o$. The importance of this is seen by examining the differential-mode (G_{dm}) and common-mode (G_{cm}) gains of a differential amplifier. $G_{dm}$and G_{cm} of a differential amplifier are given by:

$$G_{dm} = -g_m R_c \tag{4.4a}$$

$$G_{cm} = \frac{-g_m R_c}{1 + 2g_m R_o(1 + \frac{1}{\beta_0})} \tag{4.4b}$$

If R_o is large, the differential amplifier will reject the common-mode component of the

signal while amplifying the differential component. Since imbalance in a differential signal can be represented by a common-mode component, a higher R_o improves the balance of the signal.

To set the voltage levels within the various sections of the mixer, a series of current mirrors were used. The voltage levels were set by the voltage drops across the load resistors between the voltage rail and each mirror transistor. To isolate the signal from the DC biasing, large resistors (1 kΩ) were inserted between the current mirrors and the RF circuitry. Also, high-value decoupling capacitors were used in the DC bias circuitry to eliminate any feedthrough problems by shunting any possible RF signal directly to ground. The decoupling capacitors were given a separate ground from the RF ground to further isolate the bias circuitry from the RF signal. The final circuit design, including the bias circuitry, is shown in Figure 4.5.

4.3 Supporting Circuitry

In an effort to maximize the level of circuit integration, it was decided to design all LO conditioning functions on chip. These functions include two amplifier stages and a phase splitter (Fig. 4.6). The buffer amplifier is used to isolate the phase splitter from the packaging parasitics, and to overcome the losses in the phase splitter. In addition, the buffer amplifier serves as a single-ended-to-differential converter to allow a single-ended LO input to the chip (thereby eliminating the need for an off-chip balun). The phase splitter converts the differential signal to an differential I/Q signal. To reduce the external LO power required to ensure complete switching of the LO core of the mixer, an additional amplifier stage was added after the phase splitter in both I/Q arms.

Each functional block of the LO conditioning chain was first designed and simulated individually before being integrated together. This was done to explore the individual performance characteristics of each block under different source and load conditions. The gain or loss of each block and the effects on signal error were examined. AC simulations using Agilent ADS v.1.3 were performed on each individual block, and on the LO chain after each block was cascaded in the chain.

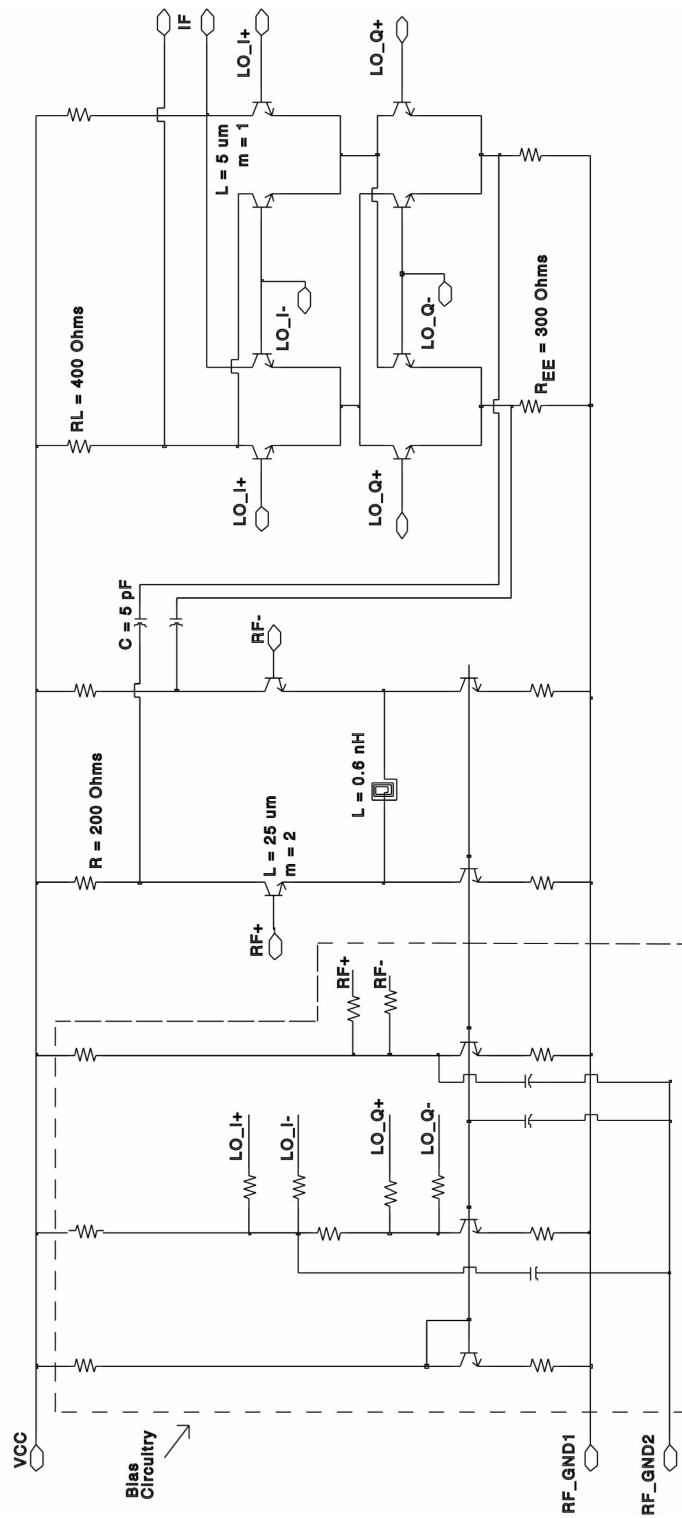


Figure 4.5: Schematic of the mixer.

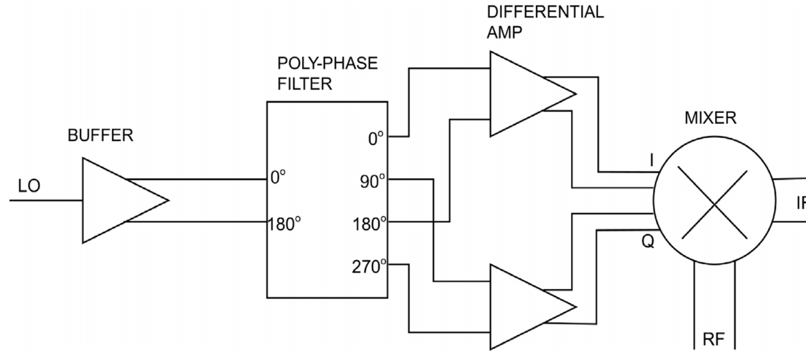


Figure 4.6: Block diagram of the mixer.

4.3.1 Buffer Amplifier

The buffer amplifier serves to buffer the poly-phase filter and perform the single-ended-to-differential conversion. Several approaches to accomplish this conversion were considered. A simple LC network could be used, but the low Q and large die area of on-chip inductors make it a less desirable choice. Integrated baluns have also been used to perform signal conversion [46]; however, insufficient modeling has limited their use on-chip [47]. In addition, monolithic transformers on Si substrates have high loss and poor coupling factors [48]. The best choice for this application is an active implementation using a differential amplifier as shown in Figure 4.7(a). This implementation requires a relatively small die area and provides additional gain to the circuitry.

The disadvantage of this implementation lies in the inaccuracy of the output signal balance. The output of the differential amplifier displays a relatively high amplitude and phase error when one input is directly grounded. Figure 4.7(b) shows a modified version of the same differential amplifier [49]. This amplifier has less phase and amplitude error at the output. The improved accuracy can be explained by examining the RF equivalent circuits of two circuits (Fig. 4.8). When an ideal differential amplifier is driven with a purely differential signal, node “A” is a virtual ground. However, when the differential amplifier is no longer symmetric, as is the case when one input is grounded, the amplifier is no longer balanced about node “A”, creating phase and amplitude error in the output signal. This problem can be mitigated with the addition of a resistance R_1 as shown in Figure 4.8(b). By setting R_1 equal to

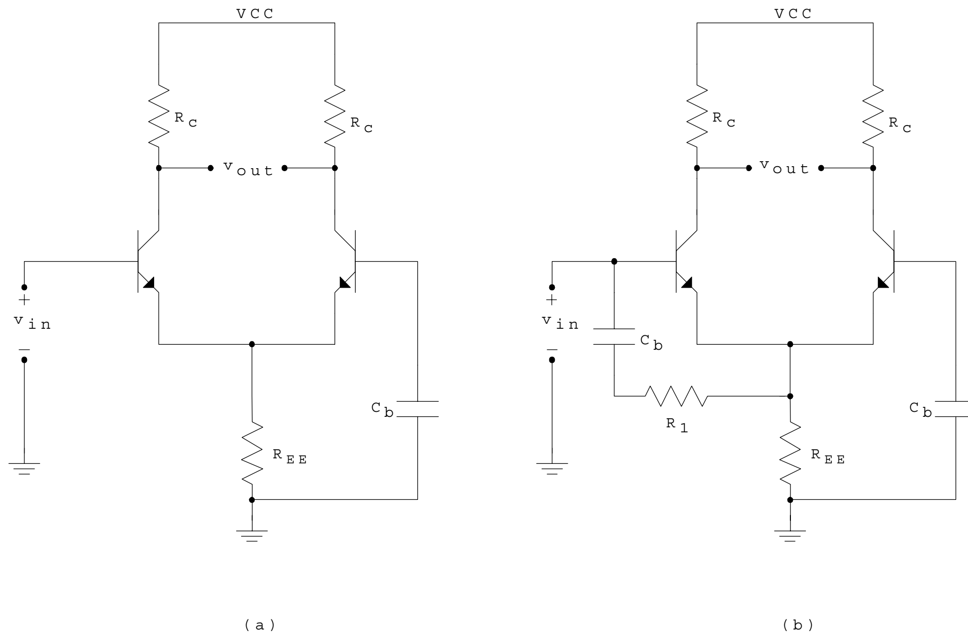


Figure 4.7: Single-ended-to-differential conversion amplifiers.

R$_{EE}$, the RF equivalent circuit is symmetric about node "A". The result is greatly improved output balance.

An external shunt 50 Ω resistor was used to provide a simple match at the LO input. Simulations show that the added resistance has little impact on the NF of the mixer since the NF is referenced to the RF port, not the LO port. The load and degeneration resistances of the buffer amplifier were chosen to give a gain that equalled the 11 dB loss simulated for the phase splitter (refer to Section 4.3.2). An additional emitter-follower stage was added to the output of the buffer to provide the phase splitter with a low-impedance input termination.

The complete buffer amplifier is shown in Figure 4.9. The differential amplifier section was biased at a total of 2.8 mA and the emitter follower section of the buffer was biased at a total of 2.2 mA. These values, in conjunction with the choice of load resistances ensured that the slew rate of the buffer was sufficient to produce a low distortion signal.

The simulated output of the buffer amplifier is shown in Figures 4.10 and 4.11. The maximum amplitude and phase error at the output of the buffer are approximately

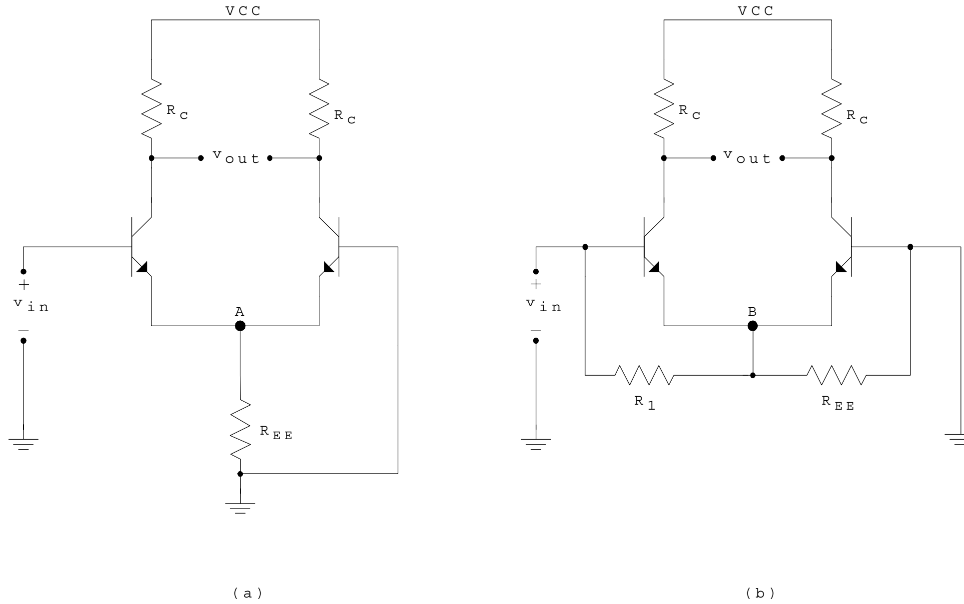


Figure 4.8: RF equivelent of the single-ended-to-differential converters.

0.32 dB and 1.5 degrees, respectively.

4.3.2 Phase Splitter

The poly-phase filter design shown in Figure 4.12 produces the I/Q LO signals from the differential output of the buffer. The architecture is a simple two-pole passive RC filter similar to that used in [50]. The in-phase inputs are supplied by the buffer amplifier while the quadrature phase inputs of the filter are terminated with a ground. The filter is designed for a center frequency of 2.45 GHz with the first pole at 2.4 GHz and the second at 2.5 GHz. This center frequency set the optimal IF frequency range from 100 MHz (at an RF of 5 GHz) to 1.1 GHz (at an RF of 6 GHz). The two pole design allows for some tuning of the LO (and hence the IF) while maintaining adequate amplitude and phase balance. The nature of the poly-phase filter is such that the amplitude balance worsens outside the bandwidth of the filter, while the filter maintains a near 90° phase relationship between outputs for frequencies much wider than the bandwidth. Therefore, the filter will still have adequate performance outside its bandwidth as long as the amplitude imbalance is compensated for.

Figure 4.9: Schematic of the buffer amplifier.

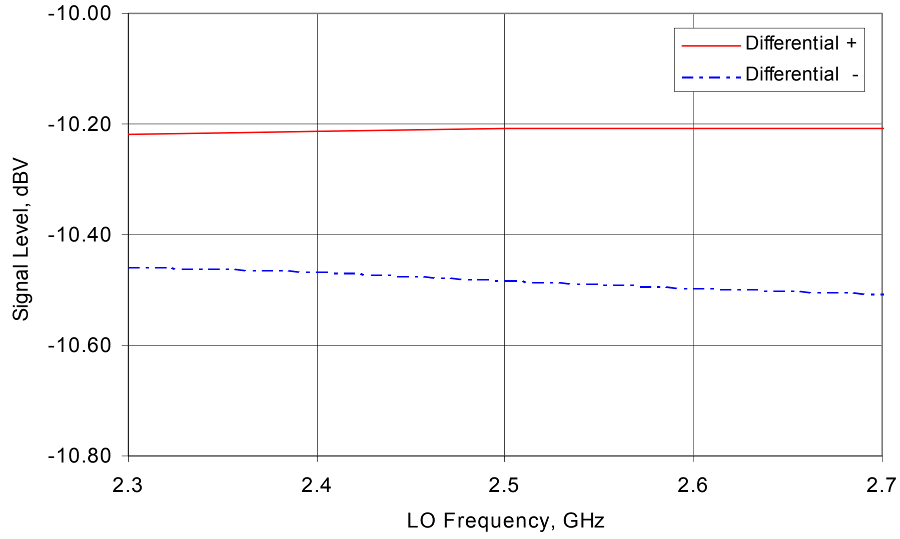


Figure 4.10: Simulated output amplitude of the input buffer.

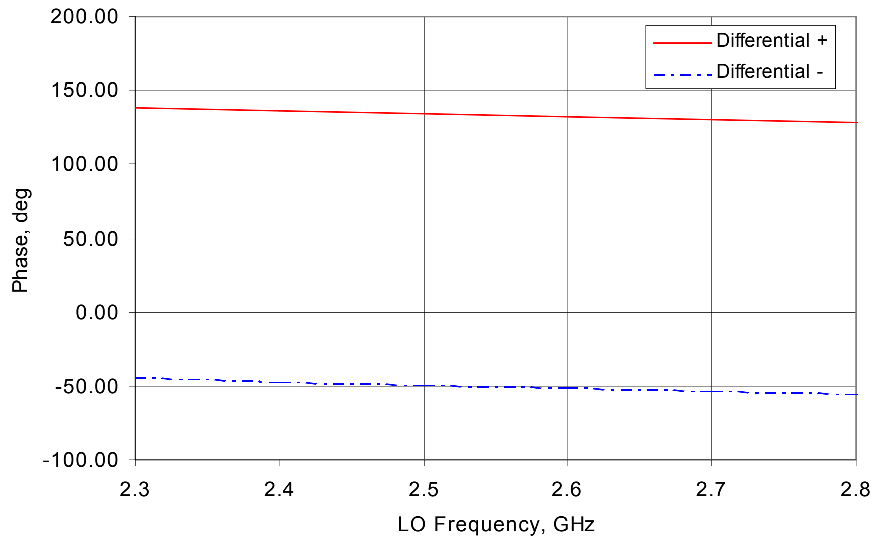


Figure 4.11: Simulated output phase of the input buffer.

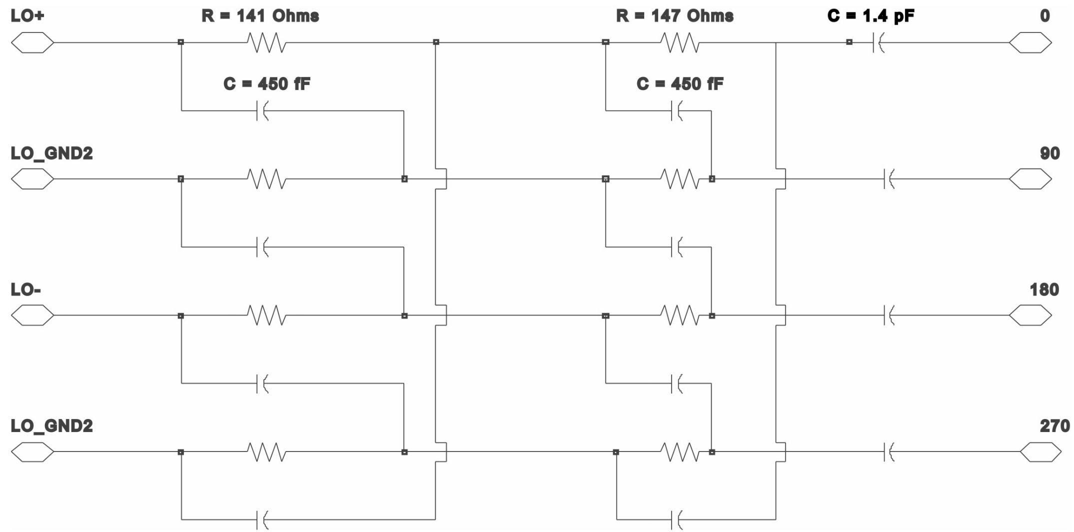


Figure 4.12: Schematic of the poly-phase splitter.

In future designs, the center frequency and poles of the filter can be moved for operation in a direct conversion receiver. For example, if the center frequency is set to 2.75 GHz, with the two poles set at 2.6 GHz and 2.9 GHz, each U-NII band can be directly converted to DC.

The simulated poly-phase filter performs very well when ideal sources and loads are used. At an LO frequency of 2.45 GHz, the worst-case simulated phase error was 0.9 degrees and the maximum simulated amplitude error was 0.2 dB. However, once non-ideal sources, loads and grounds were presented to the filter, phase and amplitude error worsened. Simulations showed that as the imbalance of the differential input increased, the filter became much less accurate. In addition, when the ideally grounded quadrature inputs were changed to the non-ideal on-chip ground, the accuracy worsened further. As mentioned previously, the buffer amp was optimized to help eliminate the input imbalance to the filter. To improve the quality of the ground, the quadrature inputs of the phase splitter were given their owns ground connections on the die.

Despite the additional ground connection and the optimization of the buffer amplifier, the simulated phase and amplitude errors remained high. Figures 4.13 and 4.14 show the output of the poly-phase filter driven by the input buffer amplifier. At 2.45 GHz, the phase error increases to 2.4 degrees and the amplitude error increases to 1.1 dB.

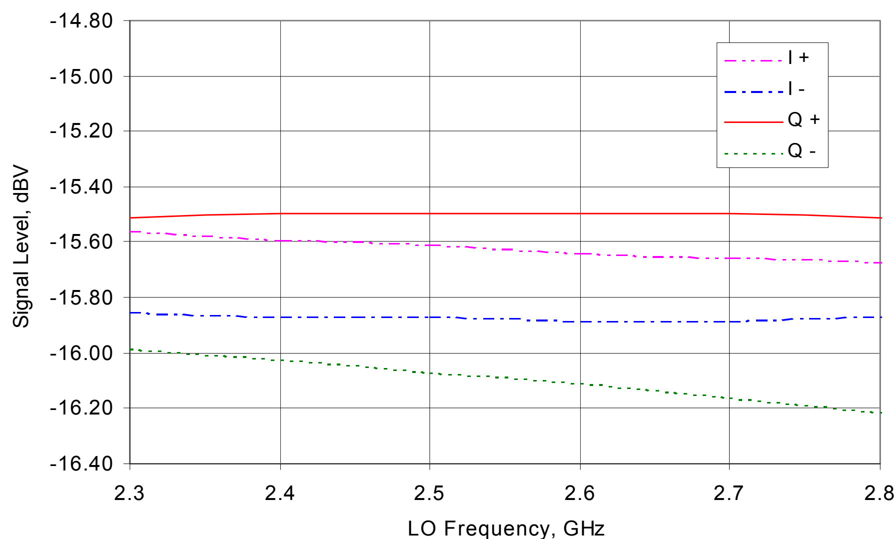


Figure 4.13: Simulated output amplitude of the poly-phase splitter.

The amplitude error worsens as the frequency increases, while the phase error remains constant.

As mentioned previously, imbalance in the duty cycles of the individual $V_{LO,I}$ and $V_{LO,Q}$ signals pumping the mixer can lead to LO feedthrough at the mixer RF and IF ports. Therefore, further improvement in the filter balance was sought.

4.3.3 Two-stage Amplifier

A differential amplifier is used to provide gain following the phase splitter. As mentioned in Section 4.2, a differential amplifier rejects the common-mode component of a signal, thereby improving the balance of the signal. This provides a very convenient way of improving the balance of the filter output. Two stages of differential amplification are used to provide improved phase and amplitude balance for the $V_{LO,I}$ and $V_{LO,Q}$ signals.

The two stages were DC-coupled to eliminate the need for die-consuming DC blocking capacitors and additional voltage biasing circuitry. A 50 Ω resistor was placed between V_{CC} and the first stage amplifier to create a voltage drop which would lower

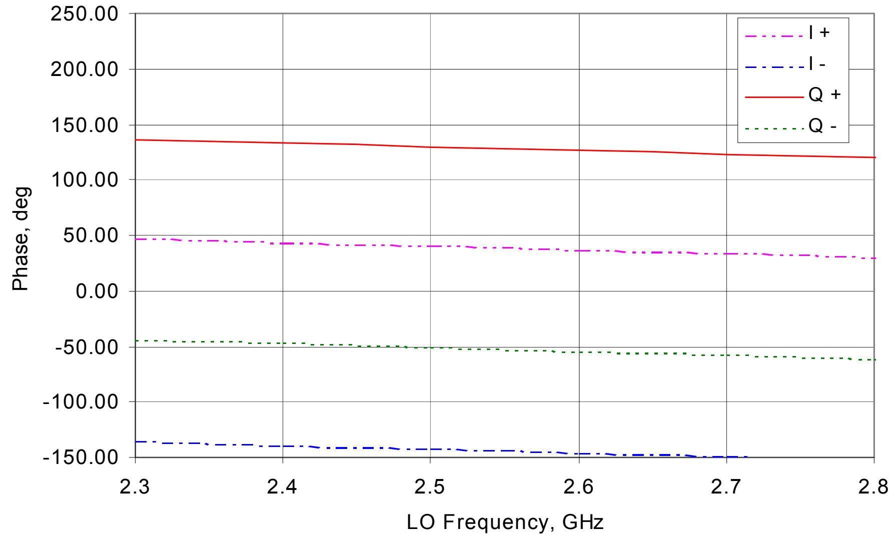


Figure 4.14: Simulated output phase of the poly-phase splitter.

the DC level of the first stage's DC output to the level required to directly bias the second stage's transistor pair.

Simulations of the mixer with *ideal* LO sources showed that a voltage level of -8 to -4 dBV per transistor would be required to sufficiently switch the mixer core. This provided a starting point for setting the gain of the amplifier. The actual gain of the amplifier resulted in -3.8 dBV delivered to each of the mixer switching transistors. Load resistors of 250 Ω, and a bias current of 2 mA for the first stage and 3.8 mA for the second stage, were chosen to provide this signal level given about -5 dBm of external LO input. Although current saturating the differential amplifier was not a problem for the LO (a square wave is the ideal waveform for mixer switching), a 50 Ω emitter resistor was added to the second stage of the amplifier to reduce the amount of saturation in the second stage. Driving any amplifier section of the LO chain into heavy saturation greatly increased the simulation time for the mixer. Therefore, emitter degeneration was done as a practical matter to reduce the simulation time.

The current and voltage bias levels for the transistors were set using an identical method to the mixer core. The emitter degenerated current sources are especially important in this circuit to maximize the balance of the amplifiers.

The final design of the differential amplifier is shown in Figure 4.15. The simulated output of the differential amplifier is shown in Figures 4.16 and 4.17. The amplitude and phase errors at 2.45 GHz are reduced to 0.14 dB and 0.4 degrees, respectively. Furthermore, outside the poly-phase bandwidth, the amplitude and phase imbalances remain small and rather constant. This can be explained by the common-mode rejection of the differential amplifier, and the previously mentioned phase characteristics of the poly-phase filter.

4.4 Simulated Mixer Results

The Harmonic Balance Analysis (HBA) simulator within Agilent ADS v.1.3 was used to simulate the mixer conversion gain, noise figure (NF), linearity, and isolation; S-parameter simulations (S_{11}) were used to analyze the impedance match at the RF input. Because of the very long of the HBA simulation times, mixer simulations were limited to two frequency points. These frequency points were chosen at 5.25 GHz and 5.775 GHz to correspond to the center frequencies of the lower and upper U-NII bands. The simulation set-up used for this analysis is included in Appendix C.

The mixer design was simulated using an ideal balun to perform the single-ended-to-differential conversion at the RF port. Figure 4.18 shows the simulated single-ended input match (S_{11}) of the RF port. The VSWR at the RF input is less than 2:1 over the entire RF band.

The conversion gain and single-sideband (SSB) NF were simulated over a range of LO powers (Fig. 4.19 and 4.20). The conversion gain at both frequencies peaks at an LO power of 0 dBm, after which the conversion gain degrades again. The maximum simulated conversion gain is 7.6 dB at 5.25 GHz and 7.65 dB at 5.775 GHz. The NF decreases with increasing LO power until $P_{LO} = 0$ dBm , at which point no further benefit of increasing LO power are seen. At 5.25 GHz and 5.775 GHz, the minimum simulated NF is 9.0 dB and 8.0 dB respectively.

The optimum range of LO power is between -5 and 0 dBm. The benefits of a higher LO power beyond -5 dBm does not outweigh the increase in required LO power, therefore -5 dBm power is used for further simulations.

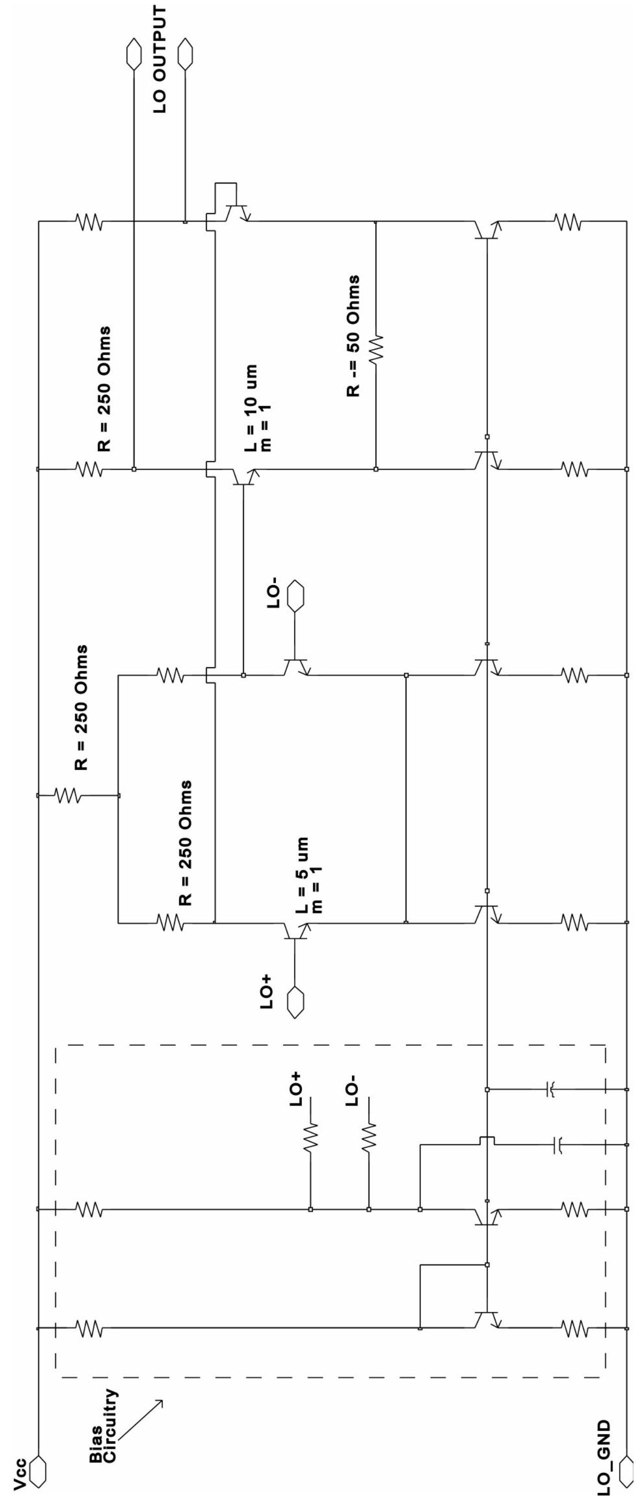


Figure 4.15: Schematic of the two-stage differential amplifier.

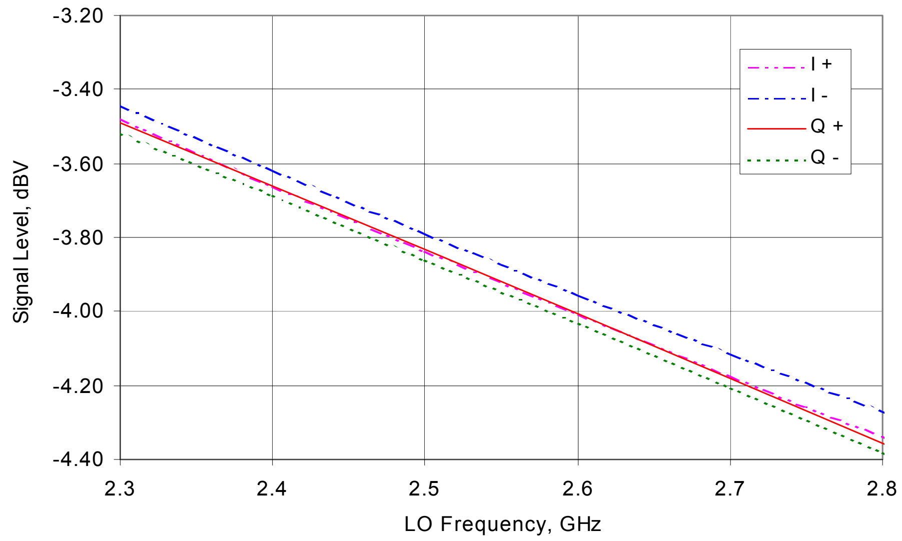


Figure 4.16: Simulated output amplitude of the differential amplifier.

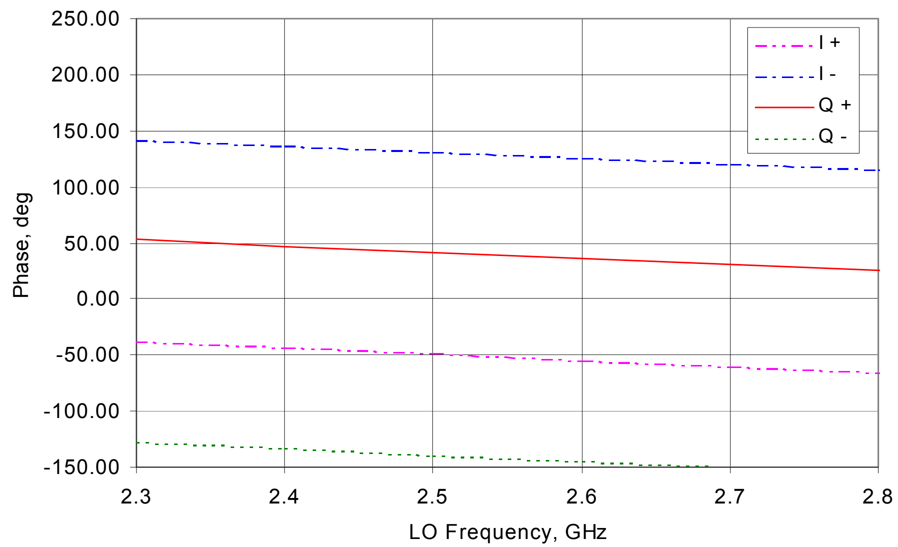


Figure 4.17: Simulated output phase of the differential amplifier.

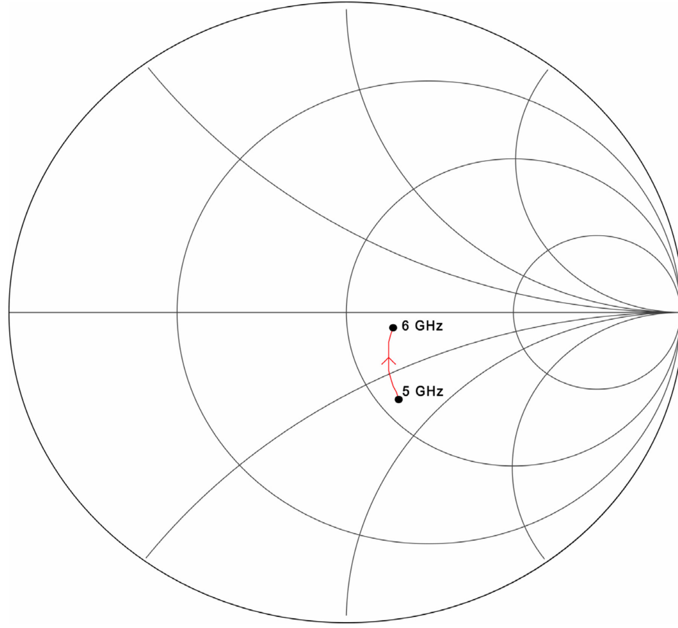


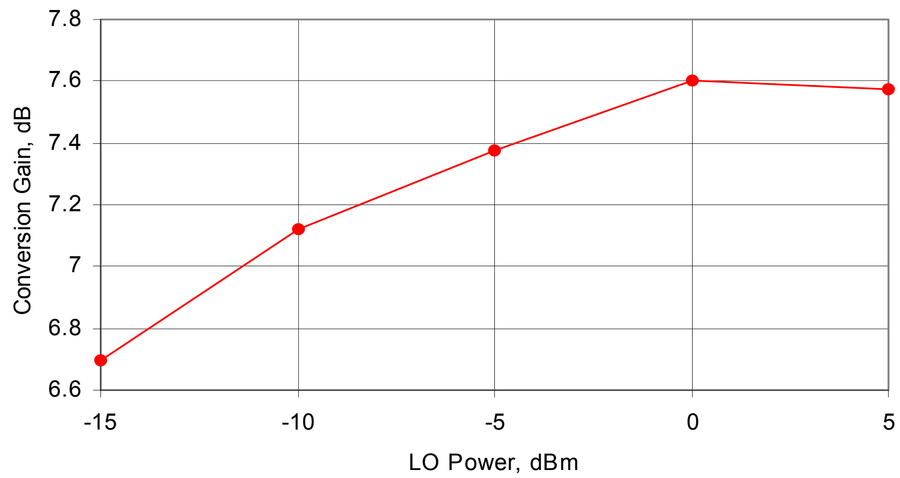
Figure 4.18: Simulated input match (S_{11}) at the RF port of the mixer.

Table 4.1: Simulated RF and LO port isolation of the mixer.

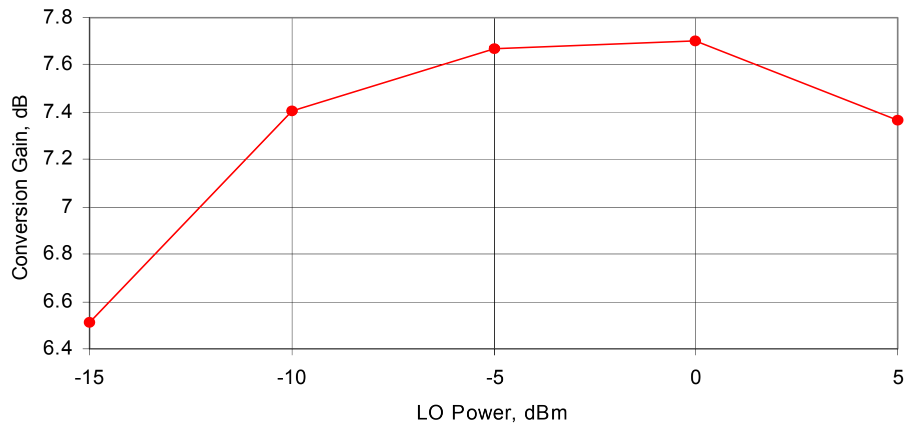
	Isolation	
Frequency	**LO/RF**	**2LO/RF**
5.25 GHz	82.2 dB	86.2 dB
5.775 GHz	86.9 dB	86.0 dB

The linearity of the mixer is simulated based on the 1-dB compression point of the IF signal (Fig. 4.21). At 5.25 GHz, the simulated 1-dB compression point occurs with an RF signal level of -20 dBm. At 5.775 GHz, the simulated compression point occurs at a slightly higher -19 dBm RF input level. The IIP3 of the mixer is estimated by adding 9.6 dB to these values [17]. The resulting IIP3 values are approximately -10.4 dBm and -9.4 dBm respectively.

The LO rejection at the RF port is shown in Table 4.1. The isolation at the RF port for both the LO and 2LO signal was greater than 80 dB.

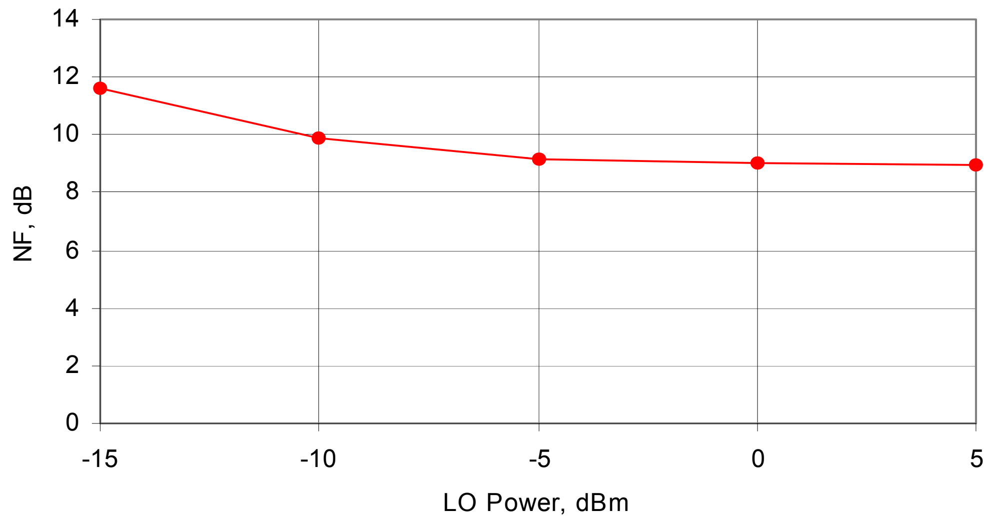


(a)

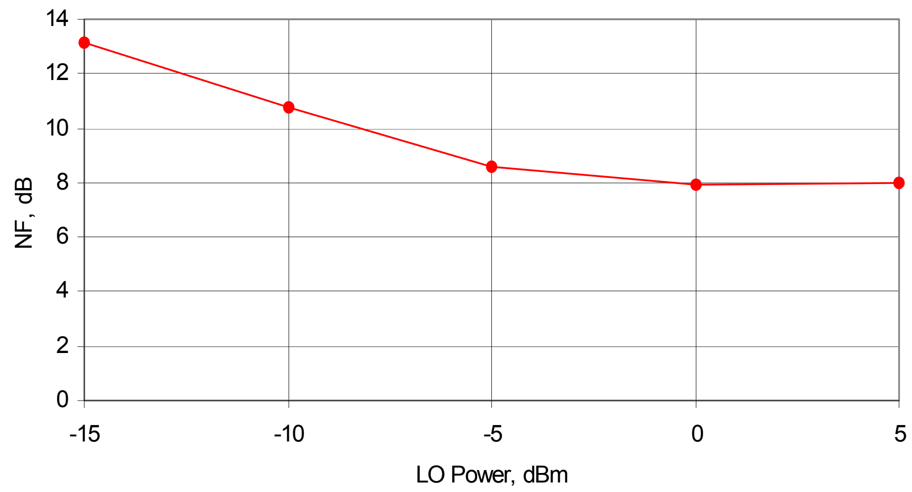


(b)

Figure 4.19: Simulated Conversion Gain vs. LO power of the mixer at an RF frequency of (a) 5.25 GHz (b) 5.775 GHz.

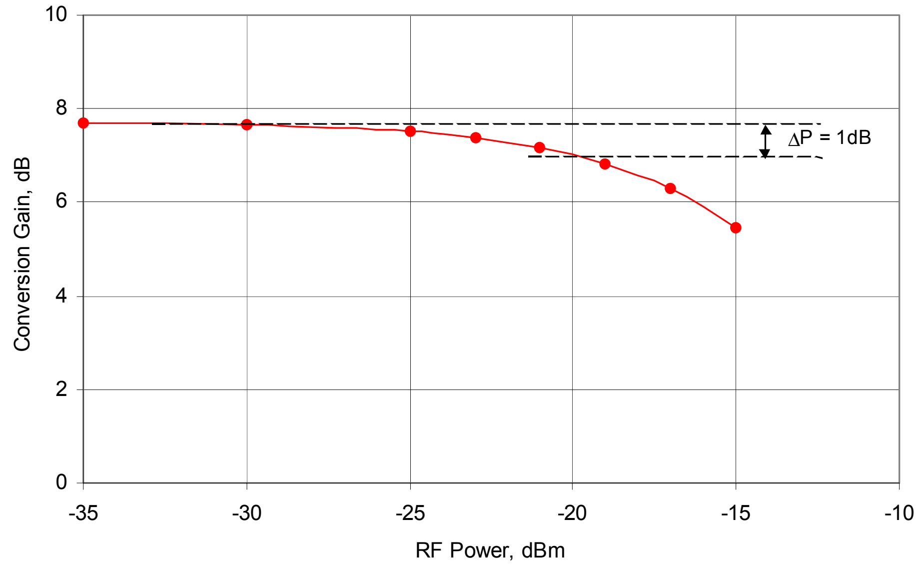


(a)

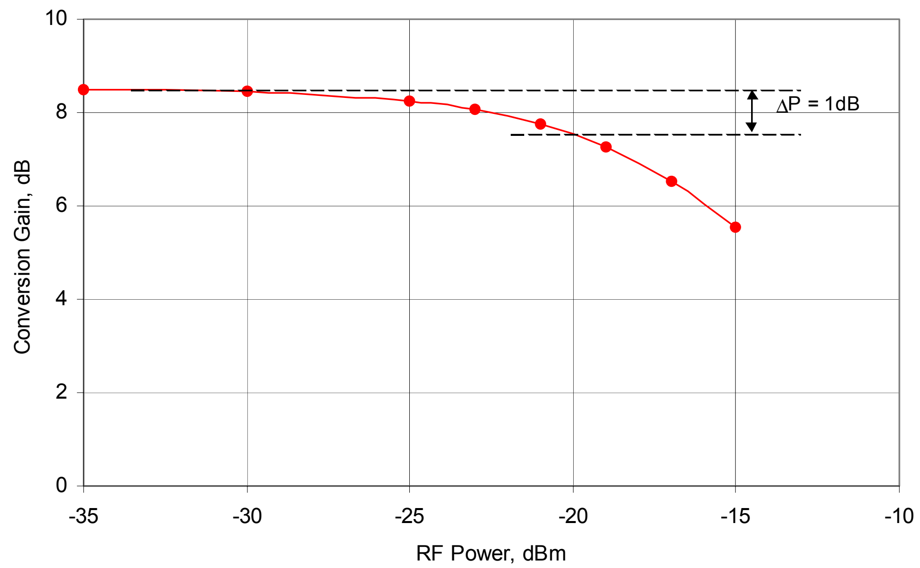


(b)

Figure 4.20: Simulated NF vs. LO power of the mixer at an RF frequency of (a) 5.25 GHz (b) 5.775 GHz.



(a)



(b)

Figure 4.21: Simulated 1-dB compression point of the mixer at an LO power of -5 dBm and an RF frequency of (a) 5.25 GHz (b) 5.775 GHz.

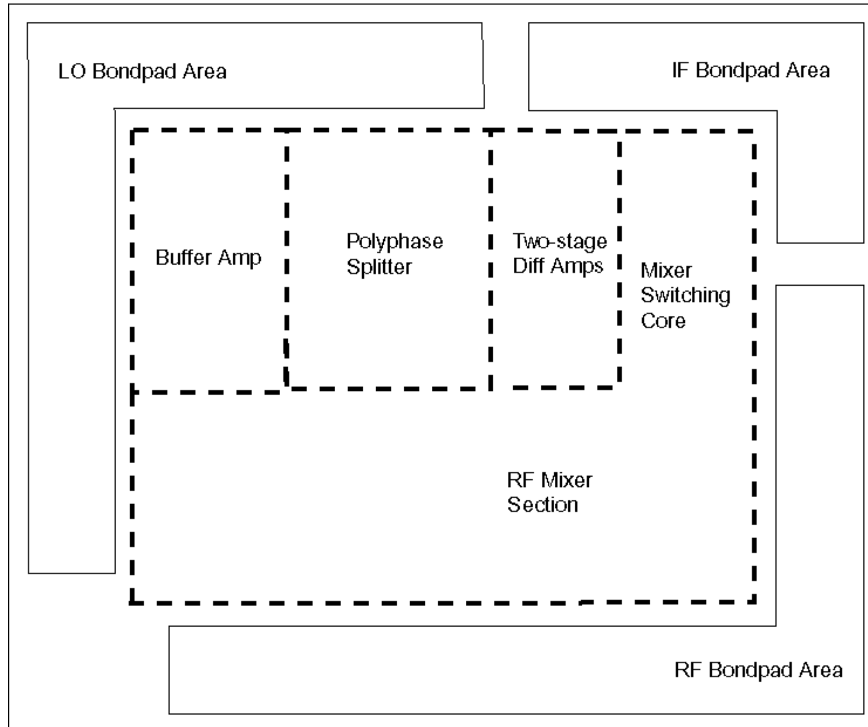


Figure 4.22: Floor plan for the layout of the mixer.

4.5 Layout and Bonding

The layout of the mixer was performed using Cadence Virtuoso [28] and IBM's design kit for Cadence v.2.1. Due to the size of the circuitry, the mixer was floor planned using hiearchical blocks (Fig. 4.22). The layouts of the buffer, polyphase filter, differential amplifiers and the mixer core were each completed separately before being combined and routed together at the top level. This approach greatly simplified the layout versus schematic (LVS) and design rule checking (DRC) of the design. In addition, this approach will allow future modifications and additions to more easily be added to the mixer layout.

The mixer core is divided into two sections in the layout. As shown in Figure 4.22, the RF section was placed below the two-stage differential amplifier, while the switching core was placed next to the two-stage differential amplifier. This was done to conserve space on the die and had little effect on the function of the mixer since the AC coupling capacitors between the RF and switching sections were sized to fill

in the space between.

The LO, RF and IF bondpads were placed away from one another to reduce the potential of coupling through circuitry or bondwires. The simulated performance of the mixer was found to be relatively insensitive to bondpad sizing; therefore, the size of the bondpads were increased to 90 μm x 90 μm (in comparison to the 75 μm x 75 μm pads used for the LNA designs) to make wire bonding easier. Since there were relatively few bondpads compared to the space available on the edges of the chip, there was no set spacing between bondpads; rather bondpads were placed closest to their corresponding circuitry.

The layout of the mixer used many of the same techniques utilized in the LNA layout, including:

- Metal1 traces with substrate contacts were connected to a dedicated bondpad used to separately ground the substrate;
- Bondpads with deep-trench grids underneath were used to reduce the parasitic coupling to substrate and surrounding circuitry;
- Thicker Metal3 was used where ever possible to reduce the losses in traces;
- The inductor was placed away from other circuitry to reduce potential coupling; and,
- All metal traces where sized to meet or exceed current density rules.

In addition, the following techniques were used to ensure good balance and rejection of common-mode noise in the differential circuitry:

- Differential signal traces were run in parallel to reduce common-mode coupling;
- Line widths, metal transitions and via placement were made as similar as possible within each trace of a differential path to provide near identical losses and parasitics;
- Identical devices in each differential branch of a circuit were placed adjacent to one another to provide close matching of values; and,

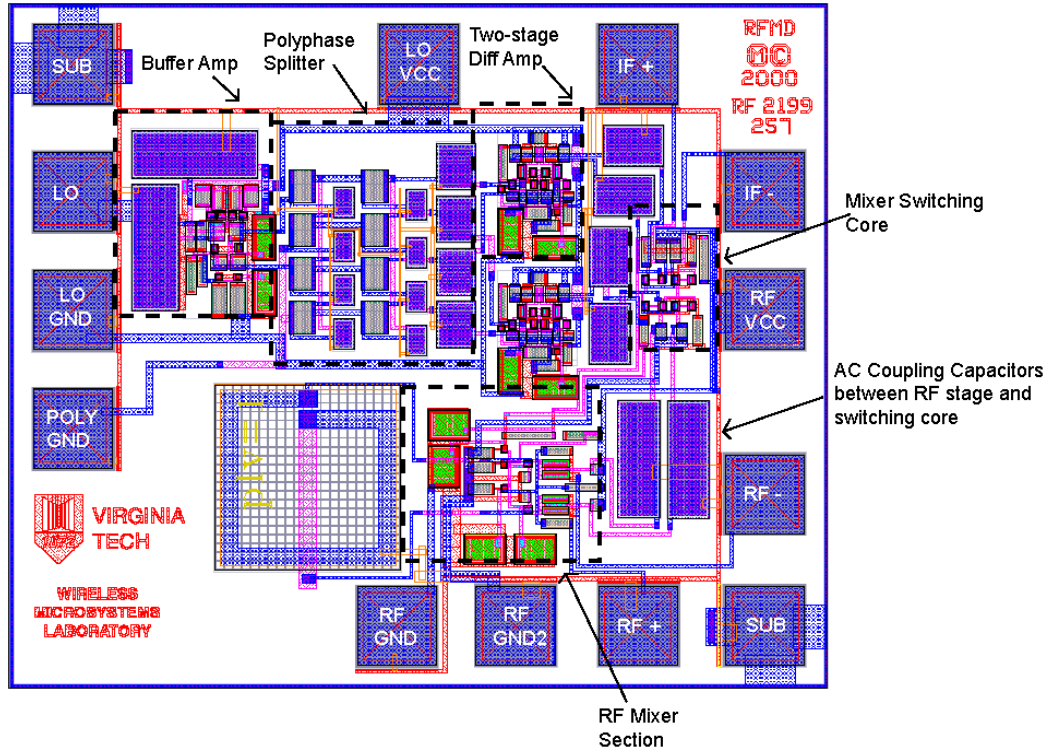


Figure 4.23: Layout of the mixer die.

- Differential circuitry was laid out symmetrically with identical trace lengths when ever possible.

The dimensions of the final layout were 0.935 mm x 0.735 mm. The package to be used for the mixer was an Amkor MLF-12 3 mm x 3 mm plastic package. The mixer layout is shown in Figure 4.23; the packaging and bonding diagram is shown in Figure 4.24.

4.6 Summary

A x2 sub-harmonic mixer was designed and simulated for applications in the U-NII bands. At an LO power of -5 dBm and an LO frequency of 2.45 GHz, the mixer showed a simulated conversion gain of 7.6 dB, an IIP3 of -10.4 dBm and a NF of 9.0 dB at 5.25 GHz, and a simulated conversion gain of 7.7 dB, an IIP3 of -9.4 dBm and a

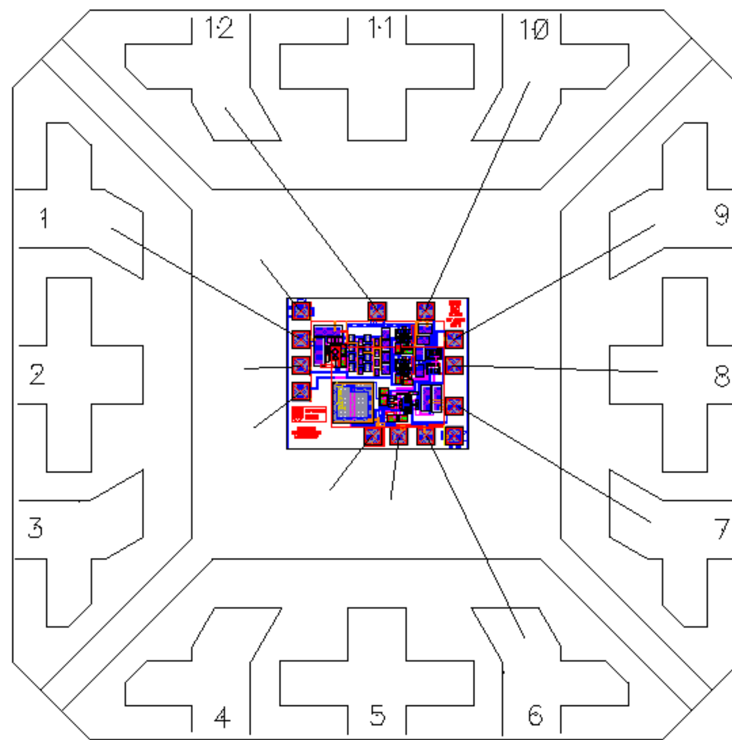


Figure 4.24: Package and bonding diagram of the mixer die.

NF of 8.0 dB at 5.775 GHz. The simulated conversion gain and NF exceed the goals outlined in Table 1.3. However, the simulated linearity did not meet the objectives as result of the mixer input matching technique used. The total dimensions of the mixer die was 0.935 mm x 0.735 mm; the circuit was designed for an MLF-12 3 mm x 3 mm package.

To date, there are no published *active* SHMs in this frequency range with which to compare these simulated results. However, the simulated mixer does compare well to the aforementioned active SHMs [40],[41],[42], although the simulated 2LO/RF isolation for this design was extremely high (>80 dB). It is believed that the simulations are inaccurate due to insufficient substrate modeling. The actual isolation is expected be closer to the values reported for other similar SHMs (30-40 dB) [41],[42].

Chapter 5

Mixer Implementation and Measurements

5.1 Fabrication

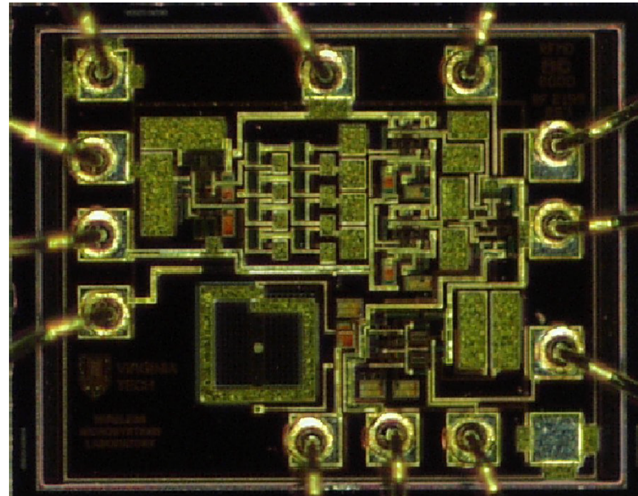
The layout and bonding diagrams for the mixer design were sent to IBM for mask generation and fabrication. The fabricated dies were mounted and bonded into MLF-12 packages by RF Microdevices. Photographs of a the wire bonded and packaged die are shown in Figure 5.1.

5.2 Test and Measurement Set-up

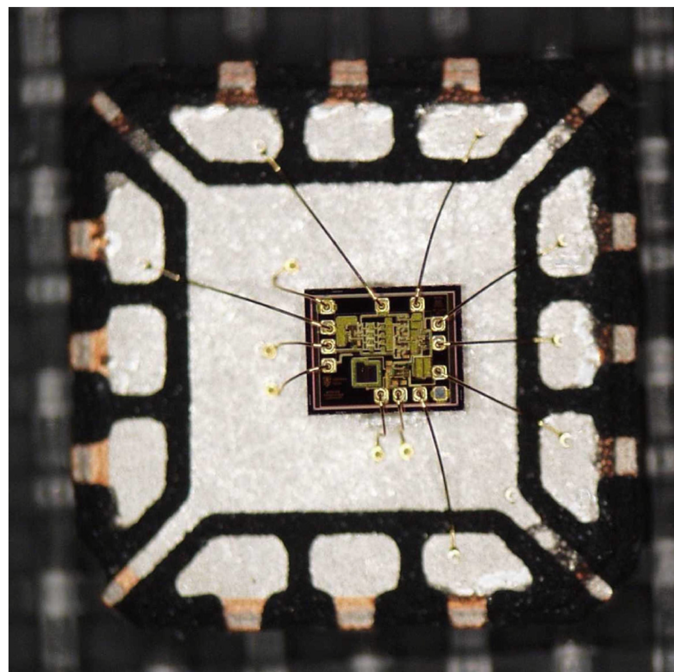
5.2.1 Test boards

Measurements of the mixer performance were conducted in a similar manner as with the LNAs. Coaxial (50 Ω) system measurements were facilitated on 0.76 mm thick FR4 test boards with 1 oz. copper plating. The metal layer stack-up was identical to the LNA test boards. SMA connectors with direct launch center conductors were used to transition the signals from the coaxial cables to the test board traces.

The traces for the RF and LO signals were 1.27 mm wide (50 Ω characteristic



(a)



(b)

Figure 5.1: Photograph of (a) bonded mixer die (b) packaged mixer die.

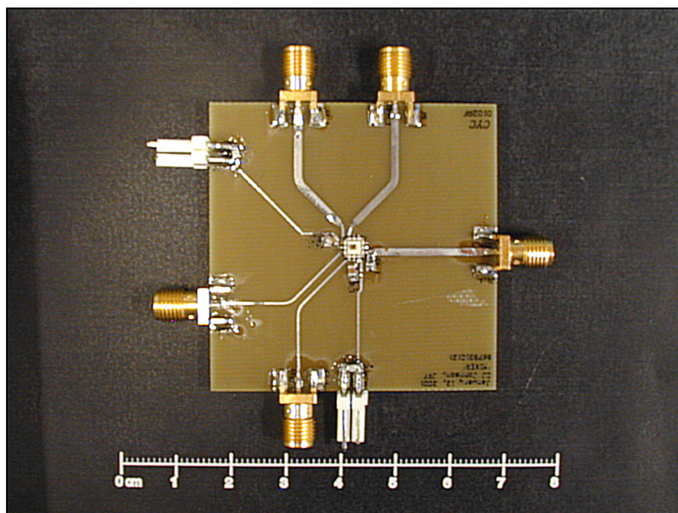


Figure 5.2: Photograph of the mixer test board. The board is 0.76 mm FR4 . The RF port and LO port are 1.27 mm wide (50 Ω characteristic impedance). The package is grounded with vias to the backside of the board.

impedance), while the IF signal traces were 0.30 mm. The differential signal traces for the RF and IF were laid out symmetrically with identical lengths to maintain good signal balance. A photograph of a mixer test board with package die mounted is shown in Figure 5.2.

5.2.2 Calibration

The calibration of the test set-up did not require board-level calibration standards as were used for the LNA measurements. Instead, a standard Maury Microwave 8050G 3.5 mm calibration kit was used for a coaxial short, open, load, through (SOLT) two-port calibration. Using a HP83620B signal generator (10 MHZ - 20 GHz) and a HP8563E spectrum analyzer (9 KHz - 26.5 GHz), losses in the test set-up were measured, including the hybrids, baluns, cables and test boards. These losses were then calibrated out of the mixer measurements.

The measurement set-up for conversion gain and linearity is shown in Figure 5.3. The 8517B S-parameter test set (45 MHz - 50 GHz) generated the RF signal for the mixer. An Anaren 30057 180° hybrid coupler (4-6 GHz) was used to perform the single-ended-to-differential conversion at the RF port. An HP 83620B signal

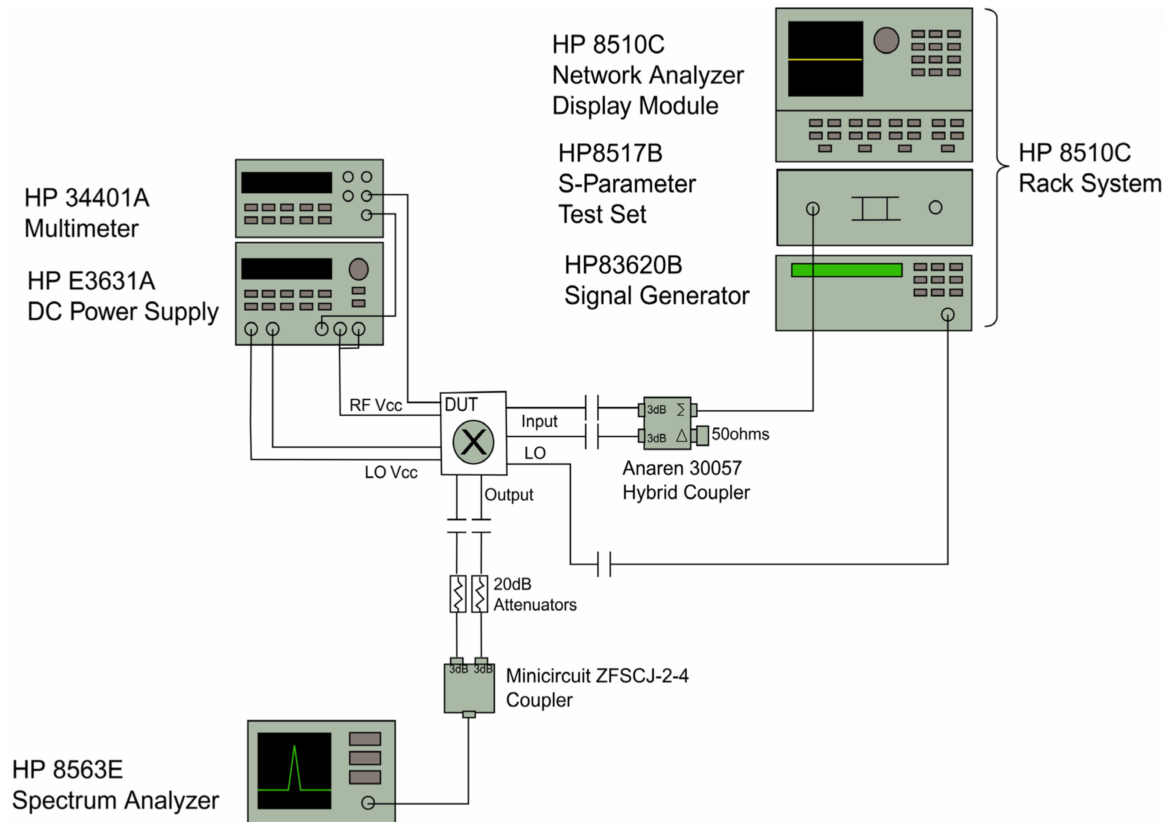


Figure 5.3: Test set-up used for mixer conversion gain and linearity measurements.

generator was used to generate the LO signal.

At the output of the mixer, a wideband Mini-Circuits ZFSCJ-2-4 balun (50 MHz - 1000 MHz) converted the differential IF to a single ended output. An HP8563E spectrum analyzer measured the output power at the IF.

The measurement set-up for 2LO/RF isolation is shown in Figure 5.4. The mixer was pumped with the LO, and the 2LO signal was measured at the RF port using the spectrum analyzer. A 50 Ω termination was used after the balun to terminate the IF port.

It was realized after the fabrication of the mixer that the RF input to the mixer had been incorrectly simulated. An ideal balun was used in simulations to convert the single-ended RF input to a differential signal. Therefore, the mixer was designed to have a 50 Ω differential output (25 Ω in each branch). However, in the actual

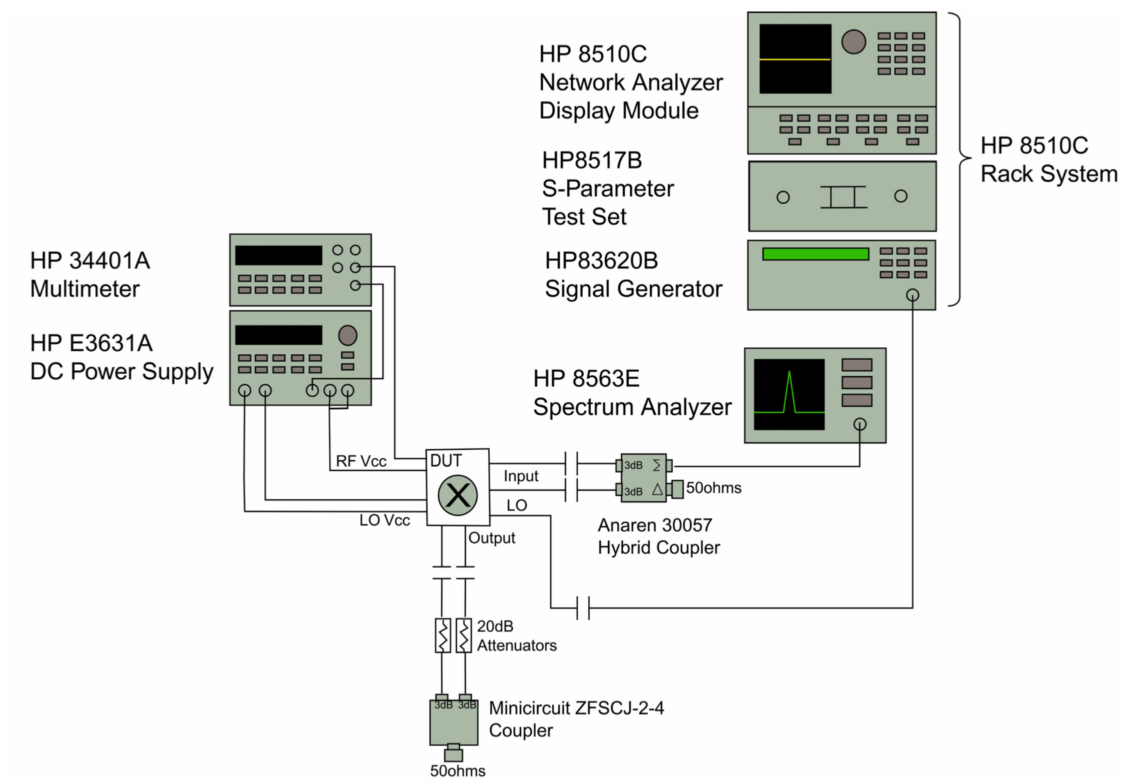


Figure 5.4: Test set-up used for mixer 2LO/RF isolation measurements.

measurements a 50 Ω hybrid was used, creating an impedance mismatch at the RF port of the mixer during testing. The method described in Appendix D was used to calibrate out this mismatch.

In addition, a 50 Ω balun was used at the IF output (400 Ω in each branch) to perform the single-ended-to differential conversion creating a significant loss in the measurement system. Because this loss was an artifact of the test set-up and would not be present in a normal system, the loss was estimated in simulation and calibrated out of the measurements.

In measuring the output spectrum of the IF, it was discovered that the impedance mismatch between the relatively high impedance IF port and the 50 Ω balun created a severe standing wave. To help alleviate this problem, 20 dB coax attenuators were inserted into each branch of the IF between the test board and the balun to significantly reduce the reflections. This attenuation factor was also calibrated out of the measurements.

5.3 Test Plan

Measurements for the mixer were taken over the three U-NII bands: 5.15-5.25 GHz; 5.25-5.35 GHz; and 5.725 -5.825 GHz. Conversion gain, linearity and 2LO/RF isolation were measured in the aforementioned bands. Unfortunately, due to the bandwidth limitations of the Anaren 30057 hybrid, LO/RF isolation could not be measured accurately. Furthermore, due to mismatch and calibration difficulties with the Agilent N8973A noise figure meter, noise figure measurements were not performed.

Agilent VEE [51] was used to automate the measurements of the mixer. This saved significant time, enabling multiple measurements over a range of mixer variables. VEE code was written to take the following measurements:

- Return loss of RF port vs. frequency
- Port isolation vs. RF frequency
- Conversion gain vs. LO power
- Conversion gain vs. LO frequency

- Conversion gain vs. RF Power
- Conversion gain vs. RF frequency
- Conversion gain vs. IF frequency

In addition, the VEE code allowed measurements to be nested inside other measurements. For example, conversion gain vs. LO power could be swept over multiple LO frequencies to see if the LO power for peak conversion gain varied with LO frequency. Conversion gain vs. RF frequency could be swept over LO frequency to see how conversion gain in a band varied for different IF frequencies.

The measurement plan was designed to first find the optimal LO power for each band, then to find the best IF band, and finally to characterize the mixer at these points. Since the two lower U-NII bands are contiguous, it was decided to determine one set of operational points to cover the 5.15 GHz - 5.35 GHz band of frequencies. Furthermore, it was decided to use different LO frequencies for the combined lower bands and the upper band in order to downconvert them both to a common IF band [Fig. 5.5(a)]. This lessened the bandwidth requirements of the external IF circuitry and allowed the use of the same IF circuitry (filters, amplifiers, demodulators, etc) after the mixer output regardless of the band of operation. This is an alternative to having a single LO frequency downconvert the entire U-NII band to a large IF band as was originally intended [Fig. 5.5(b)].

In Section 4.3.3, Figures 4.16 and 4.17 show that the LO signal at the switching stages of the mixer is well balanced over a wide range LO input frequencies. Therefore, the mixer could be tested over a wide range of LO frequencies (and IF bands) with little performance degradation.

5.4 Measurements

Initial mixer measurements revealed that at the designed for 3.3 V supply voltage, the measured conversion gain was significantly lower than simulated. The biasing of the mixer relies on the accurate mirroring of the reference current to set the bias voltages and currents in the mixer. It is believed that there is a problem with the

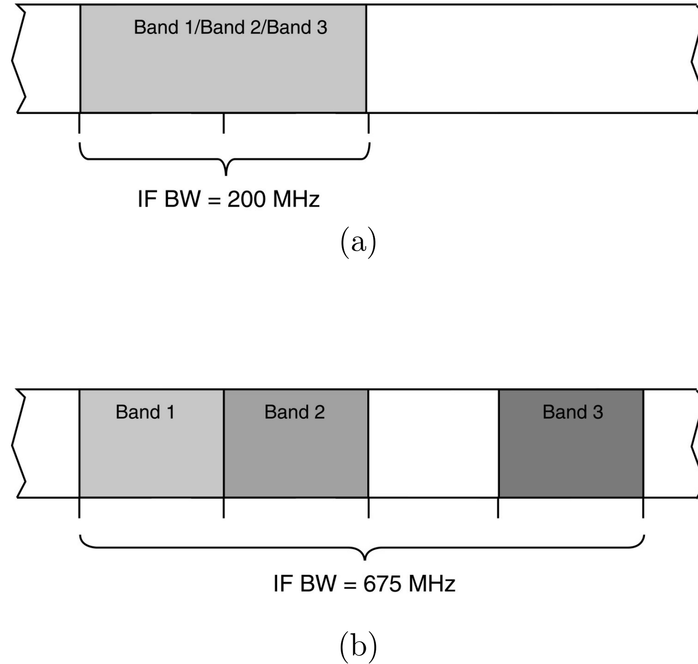
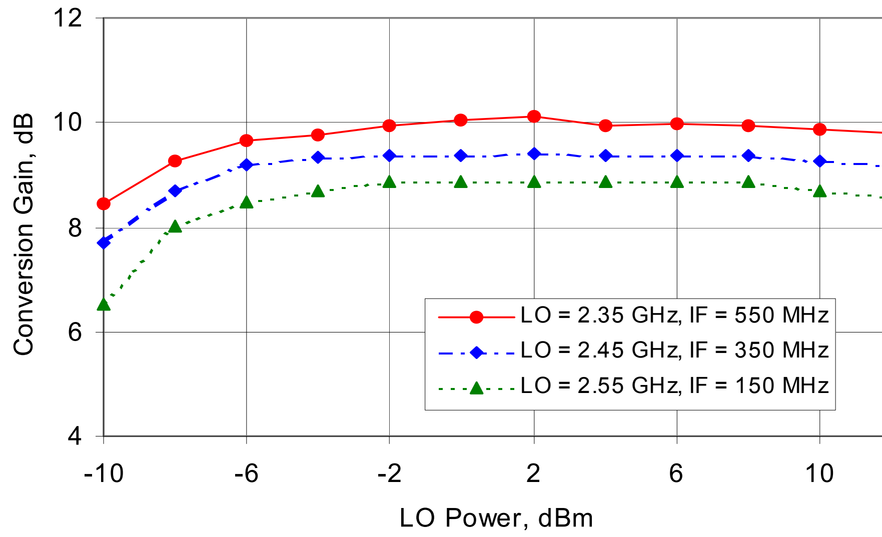


Figure 5.5: Illustration showing (a) a common IF for all U-NII bands (b) a different IF for each U-NII band.

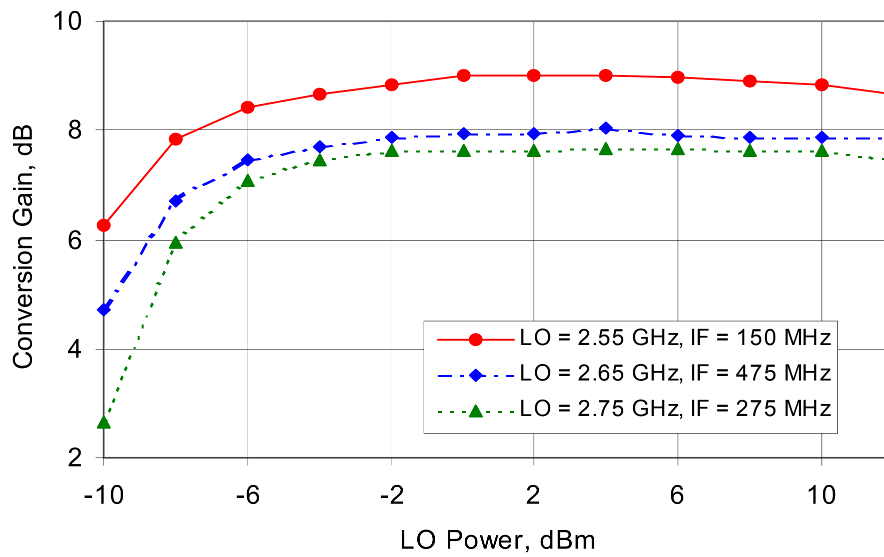
biasing networks (as seen in the LNA designs), such that the current mirror ratios did not provide an adequate amount of current to the mixer or voltage bias circuitry. Unlike the LNA designs, where bias current could be adjusted externally without modification to the supply voltage level of the LNA itself, for the mixer the bias circuitry and the mixer core shared a common voltage rail. Therefore, the only means available to compensate for a current or voltage bias error was to raise the supply voltage to the next standard voltage level of 5.0 V.

Conversion gain measurements swept over LO power were used to determine the minimum external LO power required for adequate conversion gain (Fig. 5.6). Three LO frequencies in each band were chosen to verify that the optimal LO power was consistent over a range of IF bands, allowing selection of the optimal IF band for subsequent measurements.

The conversion gain essentially follows the same trend for each of the different LO frequencies, peaking at 0 dBm of LO power and starting to degrade again at 8 dBm. The optimal operating range is between -6 dBm and 0 dBm of LO power for all LO frequencies.



(a)



(b)

Figure 5.6: Measured conversion gain of the mixer vs. LO power at (a) 5.25 GHz (b) 5.775 GHz.

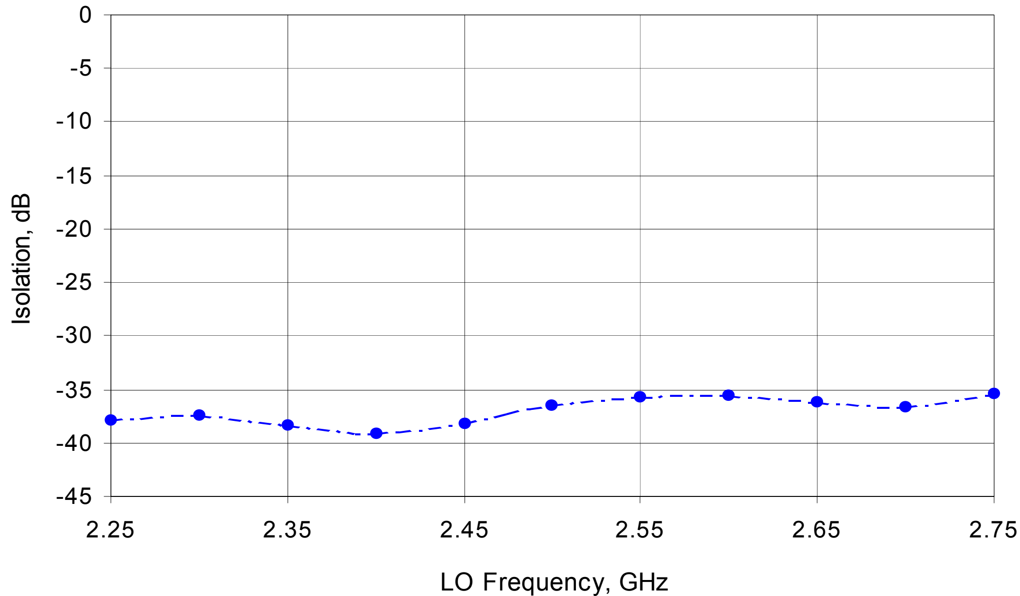
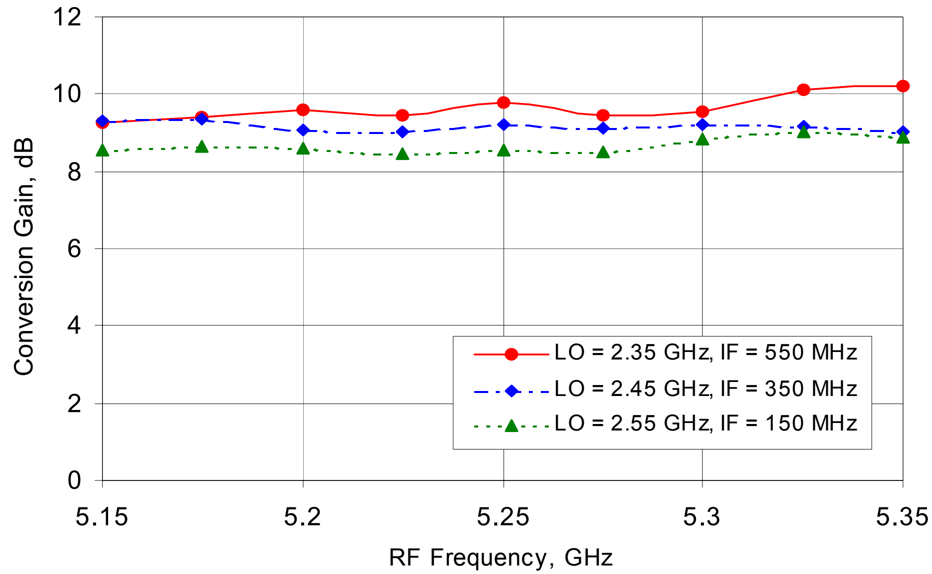


Figure 5.7: Measured 2LO/RF isolation of the mixer vs. LO frequency.

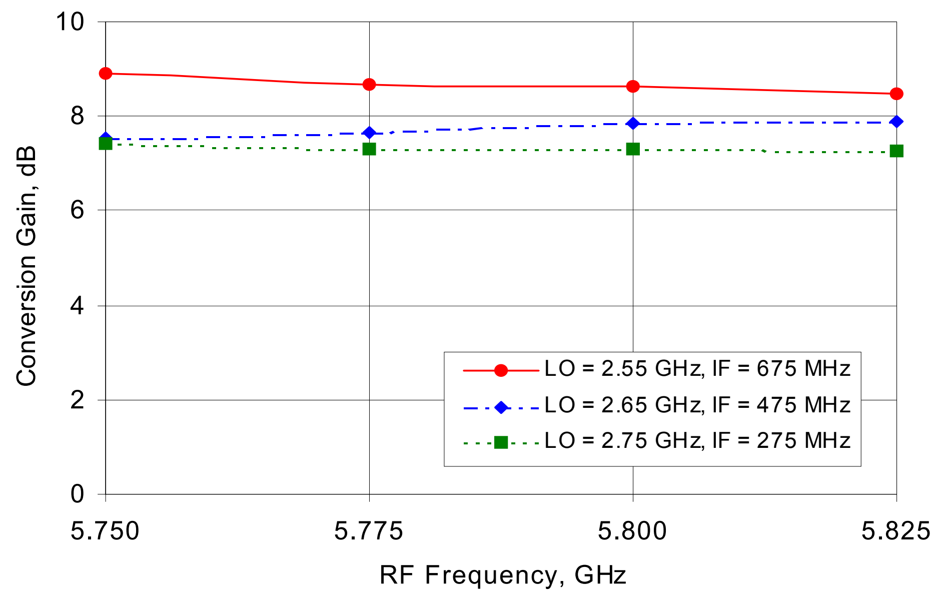
The 2LO/RF isolation measured over a range of LO frequencies is shown in Figure 5.7. The isolation is better than 35 dB throughout the range of LO frequencies. The isolation displays very little degradation over LO frequency, making the choice of LO frequency relatively independent of isolation.

The conversion gain versus RF frequency at different LO frequencies was used to study the trends in conversion gain over different IF frequency bands. Figure 5.8 shows that higher frequency IF bands (lower LO frequencies) produced a higher conversion gain. However, it is desirable to keep the IF frequency low in order to minimize the requirements of the IF circuitry. Therefore, a slightly higher LO frequency of 2.45 GHz (IF = 250 - 450 MHz) was chosen for the lower U-NII bands as a trade-off between higher conversion gain and a low IF frequency. The LO frequency for the upper U-NII band was chosen as 2.7375 GHz (IF = 250 - 350 MHz) to place the IF within the same band of frequencies as the lower U-NII bands.

Figures 5.9 and 5.10 show the optimal conversion gain and linearity measurements. The lower frequency bands [Fig. 5.9(a) and 5.10(a)] were measured at an LO power of -5 dBm and an LO frequency of 2.45 GHz. The conversion gain in this band is between 9.0 and 9.3 dB and the 1-dB compression point of the IF signal occurs with



(a)



(b)

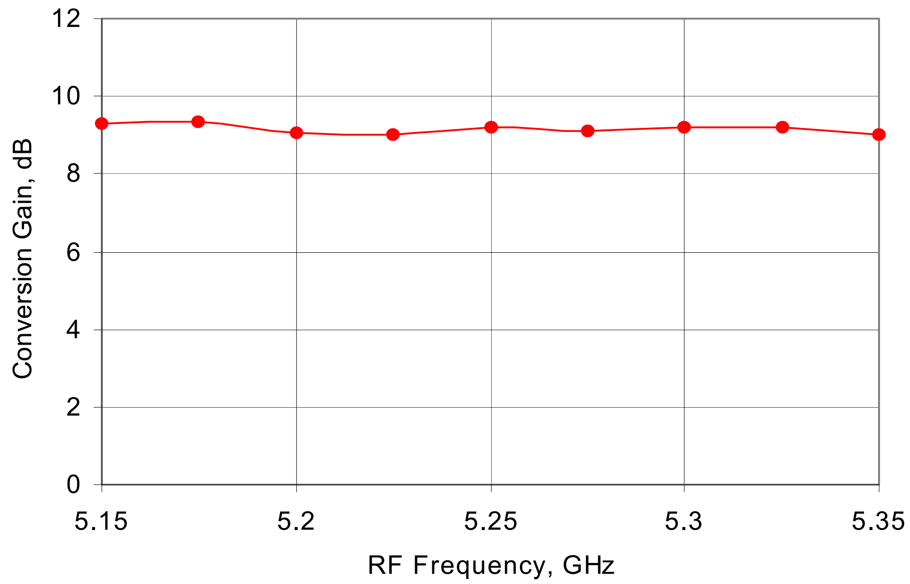
Figure 5.8: Measured conversion gain of the mixer vs. RF frequency over the (a) 5.25 GHz band (b) 5.725 GHz band, with -5dBm LO power.

-15.7 dBm of RF input power. The upper frequency band [Fig. 5.9(b) and 5.10(b)] is measured at an LO power of -5 dBm and an LO frequency of 2.7375 GHz. The conversion gain is a minimum of 7.5 dB at 350 MHz and a maximum of 7.9 dB at 275 MHz. The 1-dB compression of the IF signal occurs with -15.0 dBm input power.

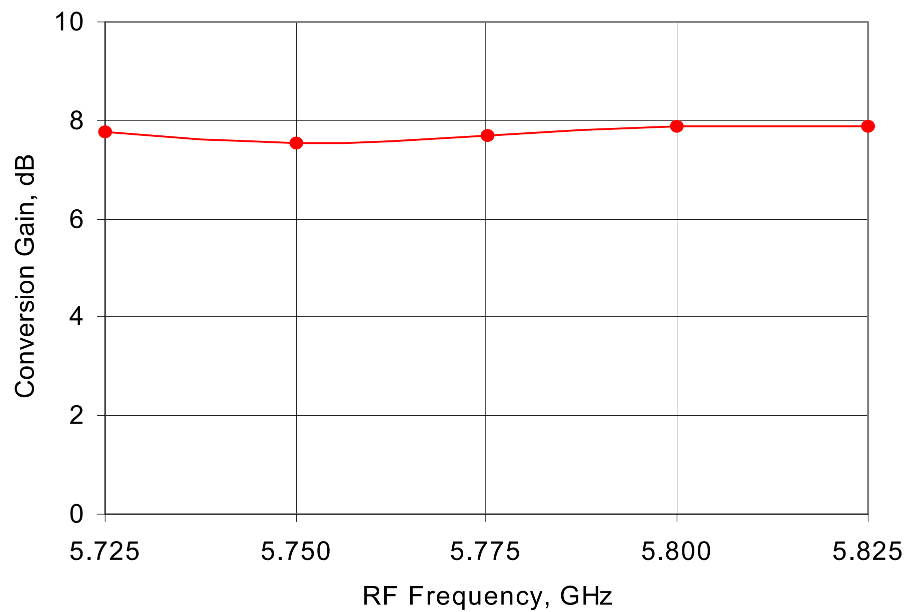
5.5 Conclusions

A x2 sub-harmonic mixer in SiGe HBT technology has been realized for use in the U-NII band. Measurements were performed to find the optimal operating range for the mixer, and the mixer was characterized under these sets of conditions. It is found that the optimal performance of the mixer occurs at an IF of 250-450 MHz with LO power ranging from -6 dBm to 0 dBm. Under these set of conditions, the mixer displays a conversion gain of 9.3 dB, P_{1-dB} of -15.7 dBm and an 2LO/RF isolation greater than 35 dB at 5.25 GHz. At 5.775 GHz, the conversion gain is 7.7 dB, the P_{1-dB} is -15.0 dBm, and the isolation is greater than 35 dB.

A comparison of the simulated and measured results are presented in Table 5.1. In most areas of the design, the measured mixer performed very well compared to the simulated results. The measured conversion gain and linearity were better than simulated. This can be attributed to the higher bias currents created by the higher voltage supply that was necessitated due to the suspected error in the bias circuitry. The only measured specification which was worse than simulated was isolation. It is likely that this discrepancy is due to the simulations not accounting for substrate coupling effects between devices.

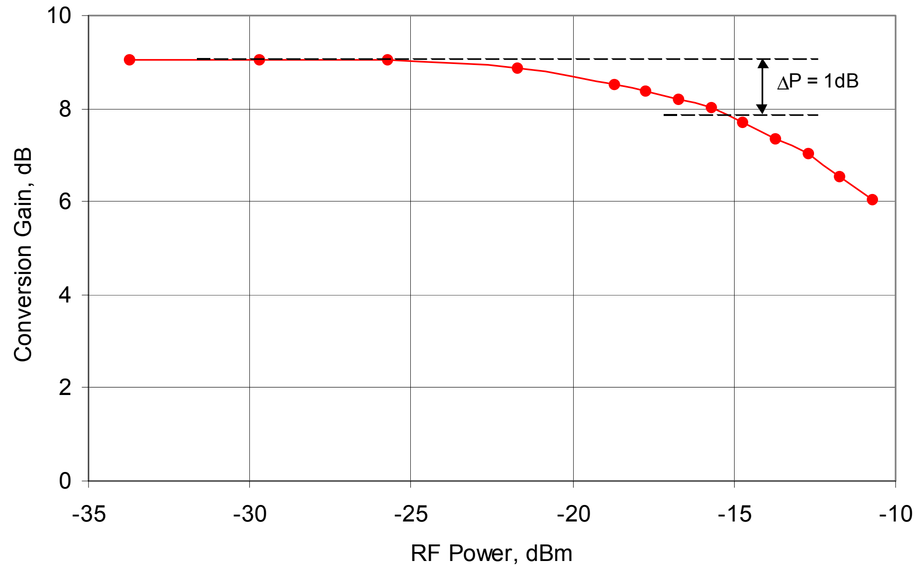


(a)

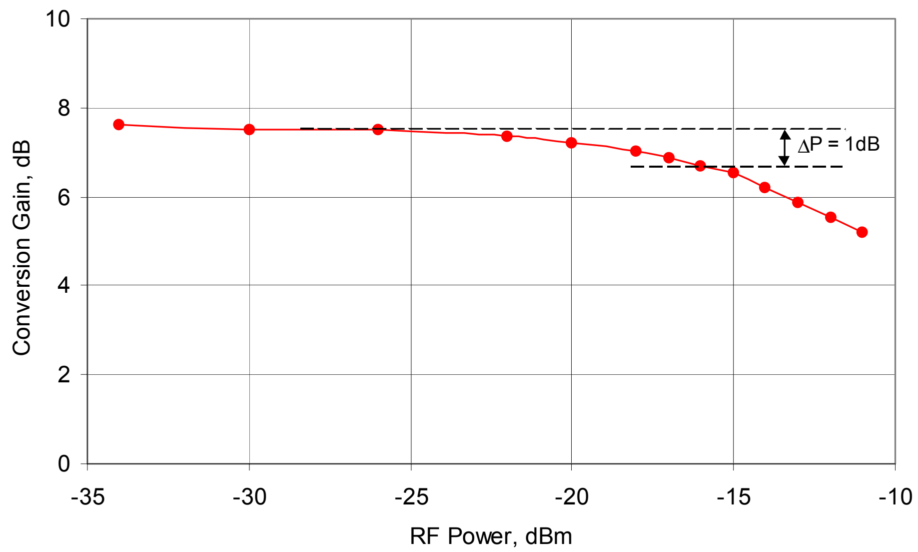


(b)

Figure 5.9: Measured conversion gain of the mixer vs. RF frequency with -5 dBm of LO power at (a) RF = 5.15-5.35 GHz, LO = 2.45 GHz (b) RF = 5.725-5.825 GHz, LO = 2.7375 GHz.



(a)



(b)

Figure 5.10: Measured 1-dB compression point of the mixer with -5 dBm LO power at (a) RF = 5.25 GHz, LO = 2.45 GHz (b) RF = 5.775 GHz, LO = 2.7375 GHz.

Table 5.1: Simulated and measured results of the mixer.

Function	**Simulated**			**Measured**			**Unit**
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	
Voltage		3.3			5.0		V
Current Consumption (mixer)		5.6			9.5		mA
Current Consumption (LO)*		17.2			25.1		mA
RF Frequency Range	5.0		6.0	5.15		5.875	GHz
IF Frequency Range	250		1250	250		450	MHz
Noise Figure @ LO = -5 dBm**	8.3		8.4		TBD		
Conversion Gain**	7.6		7.7	8.5		9.3	dB
Input IP3**	-10.4		-9.4	-6.1		-5.4	dBm
Input VSWR		<2:1			N/A		
LO Level	-5		0	-6	-5	0	dBm
2LO-RF Isolation		>80			>35		dB

*results do not include bias circuitry; measured results estimate the contribution of the bias circuitry

**specified at 5.25 GHz and 5.775 GHz

Chapter 6

Future Work

The objective of this thesis was the development of a packaged RFIC front-end in SiGe technology for operation in the U-NII bands. Specifically, several versions of a cascode LNA with emitter degeneration, and an active SHM based on the Gilbert cell were designed and tested. Through this research, the basic groundwork has been laid for the future research and development of a SiGe direct-conversion receiver.

6.1 LNA and Mixer Design Improvements

Sections 3.4, 3.5 and 5.5 give some insight into sources of error between the simulated and measured results in the LNA and mixer designs. To address these issues, further investigation is warranted in the following areas:

- *Package models* - It is believed that the models used in this work may not be accurate at 5 GHz. Models derived from measurements of the package at 5 - 6 GHz would greatly improve the accuracy of the simulations.
- *Bias networks* - Providing the bias reference transistor and the CE transistor in the LNA designs with separate grounds may improve the input impedance match of the LNAs. In addition, it is believed that the beta of the transistors may have been lower than originally expected; therefore, beta compensation should be added to all current mirrors to improve bias accuracy.

- *RF terminations at V_{CC}* - The use of off-chip microstrip or coplanar stub tuning, instead of the SMT chokes and capacitors used in this work, may improve the quality of the RF terminations at V_{CC}.

- *Isolation rings* - The use of deep trench rings with substrate contacts could be used to help isolate different functional blocks within the mixer and increase 2LO/RF isolation. They may also help increase the reverse isolation of the LNA.

- *Non-standard inductors* - Due to time constraints, the designs in this project were limited to the use of the existing IBM design kit inductors. The IBM kit inductors were relatively large. In addition, there were concerns on how to simulate the inductors (see Section 3.4). Smaller inductors could be designed which would have a higher degree of confidence in simulation.

- I*nput impedance match of the mixer* - For a heterodyne system, the input match of the mixer should be matched to 100 Ω differential by changing the amount of degeneration, bias current, and/or transistor sizes.

- *Layout* - It may be beneficial to look at different layout structures to examine the impact of layout on performance at 5 - 6 GHz. This could include EM simulations of inductors with close and far proximity to substrate contacts, or on-wafer measurements of isolation techniques such as different combinations of deep trench and substrate contacts.

6.2 Direct Conversion Receiver Implementation

The work performed in this thesis provided the foundation for the design of a direct conversion receiver. Experience designing in the SiGe process was gained and the basic functional blocks for direct conversion receiver– LNA, phase splitting, and SHM–were examined. As mentioned previously, SHMs are ideally suited for direct conversion receivers.

A direct conversion receiver implementation using this particular SHM design is shown in Figure 6.1. To fully implement the receiver, additional circuitry would be needed. To produce I/Q IF outputs, two mixers driven 45° out-of-phase from each other are

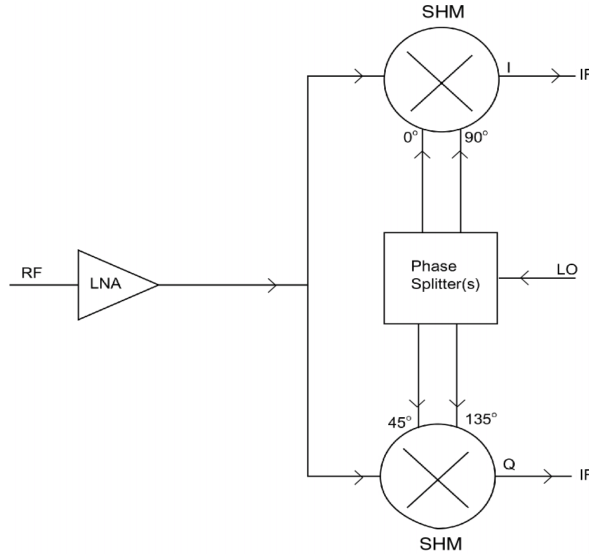


Figure 6.1: A direct conversion receiver implementation using the SHM design from this work.

required This would require either an alternative phase splitter topology which can supply all necessary phases, or the addition of a second phase splitter which is offset 45° from the first. In addition, the bandwidth of the phase splitter should be increase to allow down conversion of all U-NII bands to baseband.

Since the mixer design is fully differential, it is logical to implement the LNA as a differential LNA. Furthermore, because the LNA no longer needs to be output-matched to 50 Ω, the load of the LNA could be changed to provide better gain and better isolation. A simple way to accomplish this would be to use an LC tank as the load.

A different configuration for the RF input to the mixer should be explored to better linearize the mixer. A multi-tanh approach or resistive degeneration could be used to save die space and increase linearity. Changing the linearization technique would also allow the size of the RF transistors to be decreased. This should help with amplifier reverse isolation and also allow the transistors to operate at peak f_t with less bias current.

Appendix A

The U-NII Band

A.0.1 History

In the early part of 1997, the FCC adopted "Report and Order in ET Docket No. 96-102 [1] which made available 300 MHz of spectrum for use in a new category of unlicensed equipment called U-NII. This spectrum consists of three 100 MHz bands between 5-6 GHz. The three bands were opened primarily due to the petitioning of Apple Computer and a group of major PC vendors known as the Winforum.

In 1991 Apple submitted a petition to the FCC for a new unlicensed band of spectrum. Apple wanted an open band of frequency were users of personal digital assistant (PDA) devices could gather and form wireless community networks without the necessity of a service provider. They complained that the current ISM bands were too crowded. They needed a new band where people could form these networks without the interference of other devices.

In response to the petition, the FCC created a 20 MHz unlicensed band between 1.91 GHz and 1.93 GHz. The fatal problem with this band was it was already in use for fixed point microwave links. The FCC had proposed that the microwave users be relocated to a different spectrum at the expense of the new users. For every device sold, an addition $20 was added to cover the cost of the microwave relocation. This made the PDA devices too expensive for normal consumers rendering the band uneconomical for its envisioned use.

In 1995 Apple and the WinForum decided to try again. The second petition took a different approach. This time they asked for bands in the 5-6 GHz range and for 350 MHz of bandwidth. Their vision was to create a band of frequencies that could provide low cost computer network connections that would support multimedia applications such as the Internet. In additional it would allow a low cost means to provide wireless access to the National Information Infrastructure (NII) for libraries, schools, businesses and hospitals. In response to this latest petition, Part 15 of the FCC regulations was amended to include the U-NII bands. The new band would consist of three separate bands of frequencies, a lower band from 5.15-5.25 GHz, a middle band from 5.25-5.35 GHz and an upper band from 5.725-5.825 GHz.

A.0.2 FCC Rules

The U-NII bands fall under Part 15 of the FCC regulations. Part 15 rules provide guidelines for unlicensed bands in order to limit their interference with licensed bands. Some of the general points of the Part 15 rules (which also govern all ISM bands) are:

- If an unlicensed piece of equipment interferes with a licensed piece of equipment, the unlicensed equipment must yield to the licensed
- If a licensed piece of equipment interferes with an unlicensed piece of equipment, the unlicensed equipment must tolerate the interference
- If an unlicensed piece of equipment interferes with another unlicensed piece of equipment, the unlicensed equipment must tolerate the interference.

Since each region of spectrum has the potential to interfere with different licensed devices, Part 15 also includes specific requirements for each band. The most important specification is the definition of the frequency range and its maximum transmit power. Other specifications may include modulation efficiency, modulation schemes, and/or channel modeling.

When U-NII was introduced, Part 15 was amended to include the new spectrum allocation. They rules set forth for this spectrum are summarized as followed:

For the lower band 5.15-5.25 GHz, the peak transmit power over the frequency of operation should be no greater than 50 mW total or 4 dBm +10logB over a section of bandwidth, where B is the 26 dB emission bandwidth in MHz. In addition to these power requirements, several other rules for the lower band were set forth. The lower band of frequencies must be restricted to indoor use. Also, any system operation in this band must use an antenna that is an integral part of the device.

For the middle band 5.25-5.35 GHz, the peak transmit power over the frequency of operation should be no greater than 250 mW total or 11 dBm + 10logB over a section of bandwidth, where B is the 26-dB emission bandwidth in MHz. If a directional antenna with gain greater that 6 dBi is used, the system must reduce the peak PSD and transmit power by 1 dB for every 1 dB of antenna gain over 6 dBi.

For the upper band 5.725-5.825 GHz, the peak transmit power over the frequency of operation should be no greater than 1 W total or 17 dBm + 10logB over a section of bandwidth, where B is the 26-dB emission bandwidth in MHz. If a directional antenna with gain greater that 6 dBi is used, the system must reduce the peak PSD and transmit power by 1 dB for every 1 dB of antenna gain over 6 dBi. However, if the purpose of the system is to provide a fixed point-to-point link, antenna gains as high as 23 dBi may be used before any reduction of power is required. Once the 23 dBi limit is reached the system must reduce the peak PSD and transmit power by 1 dB for every 1 dB of antenna gain over 23 dBi. It is important to note that point-to-point does not include point-to-multipoint, omni directional applications or multiple collocated transmitters transmitting the same spectrum.

When the FCC placed the limitations on these bands it did so based upon the bands envisioned uses. The lower band, with the restriction of indoor use only, was intended for indoor wireless networking. With an EIRP of 200 mW, it has a range of a only few hundred meters and works well for interconnecting computers within the same office. The middle band has an EIRP of 1 W allowing it to transmit at distances on the order of a mile and possibly even more depending on data rate and location. This allows the middle band to operate well as a means of connecting small campuses or neighborhoods. The FCC also realized the importance of making the middle band compatible with the European HIPERLAN system and thus ensured that the power limit and spectral bandwidths of the two bands were compatible. The upper band, with an EIRP of 4 W and higher antenna gain, is capable of transmitting over greater

distances. The upper band was designed to be well suited for network backbones, T1+ replacements, and microwave point-to-point links.

Appendix B

LNA Analysis with ADS

This appendix contains the Agilent ADS v.1.3 testing stimuli for the LNA designs described in chapter 2.

Each LNA is represented by a top level view and a circuit level view. The top level contains the package level schematic with package and bondwire models and the testing stimuli. All the models used at this level are ideal lumped elements with the exception of the Coilcraft off-chip inductor model which uses an imported .S2P (S-parameters) file. The circuit level view contains the chip level circuitry. Every model at this level is directly from IBM's design kit v.2.1. including bondpads and inductors. The top level views are given in Figures B.1, B.2, B.3 for reference on how the LNAs were simulated.

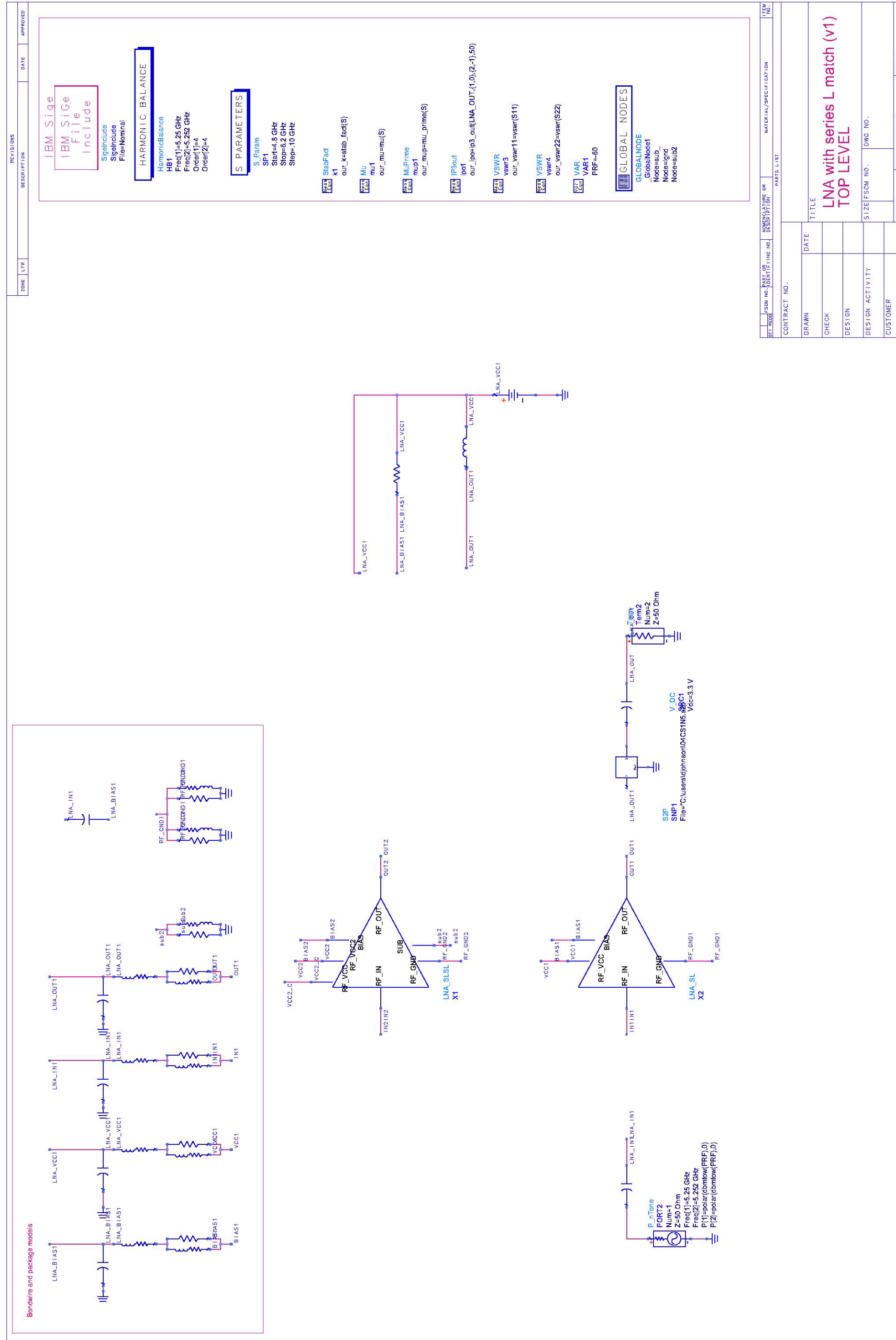


Figure B.1: Top level schematic view used in simulation of the LNA with series L output match (v1).

Figure B.2: Top level schematic view used in simulation of the LNA with series L output match (v2).

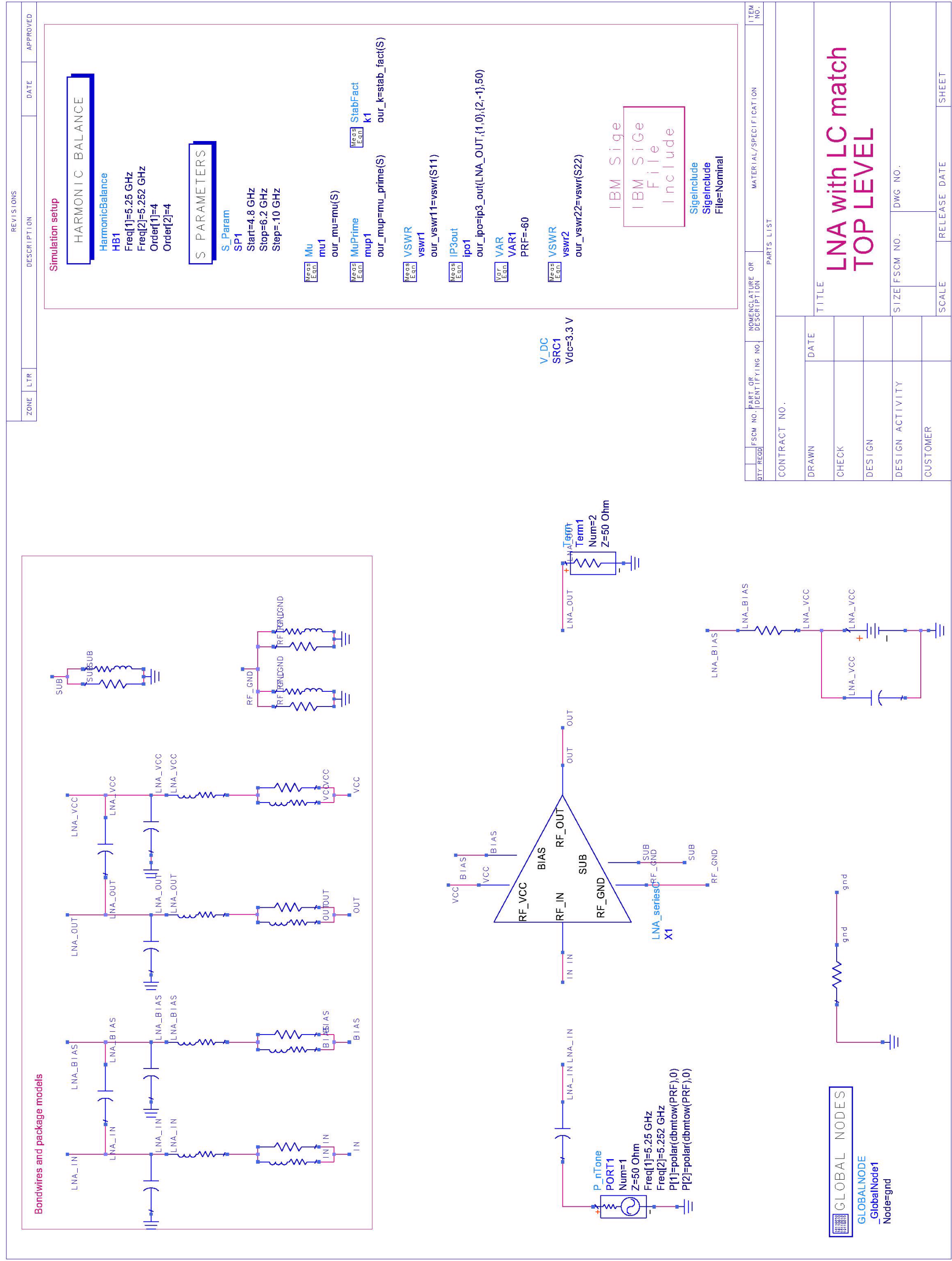


Figure B.3: Top level schematic view used in simulation of the LNA with LC output match.

Appendix C

Mixer Analysis with ADS

This appendix contains the Agilent ADS v.1.3 testing stimulus and basic set-up for the SHM. The total mixer schematic is represented by a package level schematic, a functional level schematic, and the circuit level schematics.

The package-level schematic contains all the off-chip modeling as well as all the testing stimuli. All the models at this level are ideal lumped elements. The functional-level schematic contains the block diagram for the on-chip circuitry. Since much of the on-chip circuitry had common bondpads, the bondpads were added at this level. The circuit-level schematics represent the chip-level circuitry. All models used at this level were directly from the IBM design kit v.2.1

The package-level and functional-level views, as well as the equations used in the testing of the mixer, are shown in Figures C.1, C.2, and C.3, respectively. They are provided as a reference on the testing of the mixer.

It is important to note the simulation technique used for noise figure simulations of the differential output. At the IF port, a SDD equation block is used to convert the differential IF to an single-ended output. The block converts the input signals to a single-ended output using the equation:

$$V_{out} = \frac{V_{in,+} - V_{in,-}}{2} \tag{C.5}$$

Since the ports on the equation block are not physically connected to the mixer, the block does not load down the circuit. This is necessary to accurately simulate the

noise figure of a differential circuit in ADS [52].

Figure C.1: Package level schematic used in the simulation of the mixer.

Figure C.2: Functional schematic used in the simulation of the mixer.

```
NF=nf(3)
PLO=dBm(mix(HB.LO_lx,{1,0}),50)
PRF=dBm(mix(HB.RFIN,{0,1}),50)

VIF=dB(mix(HB.IF_p,{-2,1})-mix(HB.IF_n,{-2,1}))
PIF=dBm(mix(HB.IF_p,{-2,1})-mix(HB.IF_n,{-2,1}),800)
VIFspec=dB(HB.IF_p-HB.IF_n)
PIFspec=dBm(HB.IF_p-HB.IF_n,800)
ConvGain=PIF-PRF
LO2_RF=dBm(mix(HB.RFIN,{2,0})-mix(HB.RFIN,{0,1}),50)
```

Figure C.3: Dataset equations used in the simulation of the mixer.

Appendix D

Mixer Differential RF Port Impedance Measurements

Measurements were performed to find the impedance mismatch at the RF port of the mixer. The difficulty in making impedance measurements was created by the differential nature of the RF port. Simple S_{11} measurements could not be used to extract the return loss or port impedance, since S_{11} is a single port measurement. Instead the set-up shown in Figure D.1 was used.

The Anaren 30057 180° hybrid is replaced with an Anaren 1H0567-3 90° hybrid. The IN port of the hybrid is connected to port 1 of the S-parameter test set and the ISO port is attached to port 2. Under an S_{21} measurement, the 90° hybrid converts the voltage waveform from port 1 of the S-parameter test-set to two signals 90° out of phase from one another and delivers them to the RF port of the mixer [Fig. D.2(a)]. The reflection due to impedance mismatch at the RF port passes back through the hybrid and is phase-shifted such that at the ISO port, the two reflected waveforms add in-phase and at the IN port the two signals cancel out of phase [Fig D.2(b)]. Therefore, the voltage measured at the ISO port is the total reflected voltage of the RF port and the S_{21} measured by the S-parameter test set is the reflection coefficient of the differential RF port. The power loss due to the impedance mismatch can be calculated from the magnitude of S_{21} (Fig. D.3). In addition, if S_{21} is shifted back by 270°, the port impedance can be extracted (Fig. D.4).

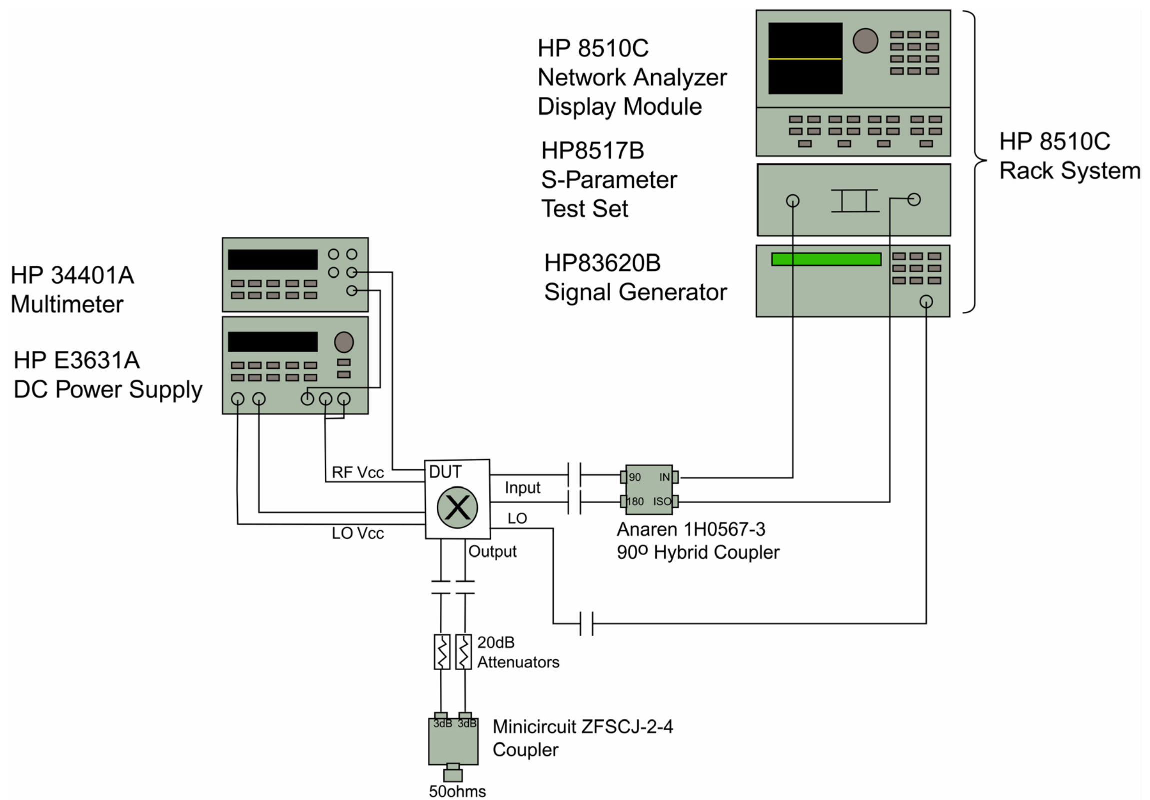


Figure D.1: Test set-up for the RF port impedance measurement.

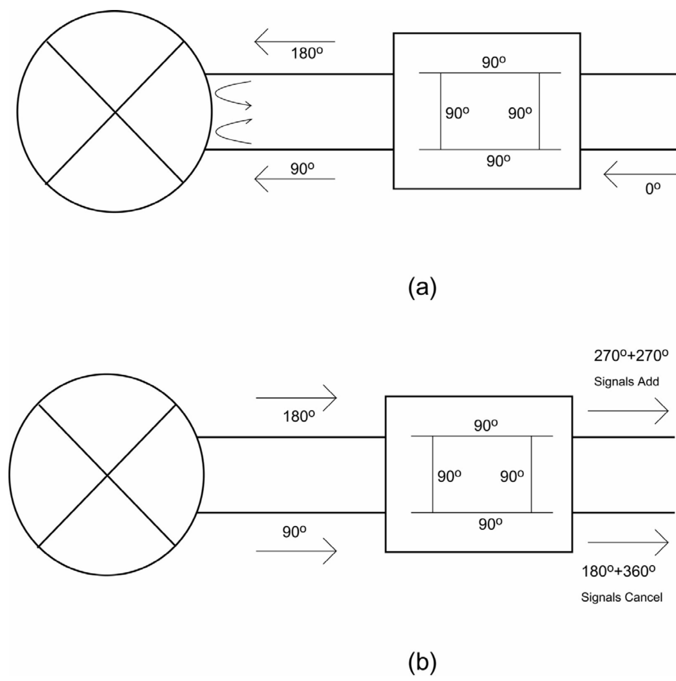


Figure D.2: Illustration depicting the phase relationships of the voltage signal (a) during the forward transmission of the signal (b) after the signal has reflected from the mixer port.

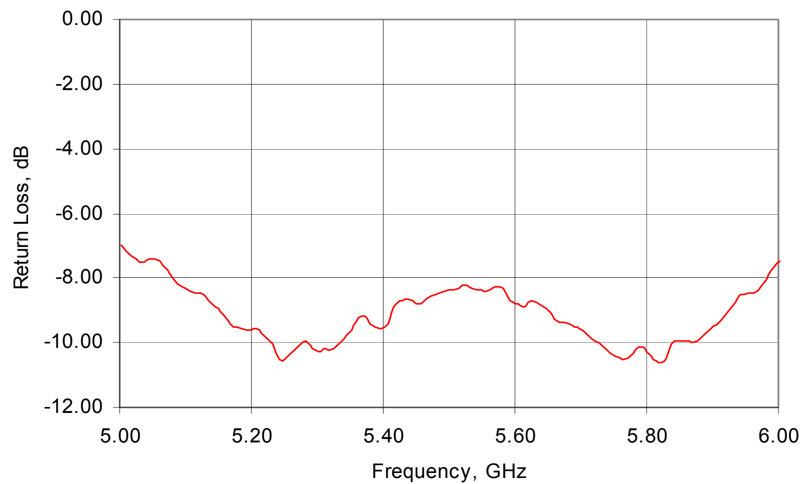


Figure D.3: Measured return loss of the RF port for the mixer in this thesis.

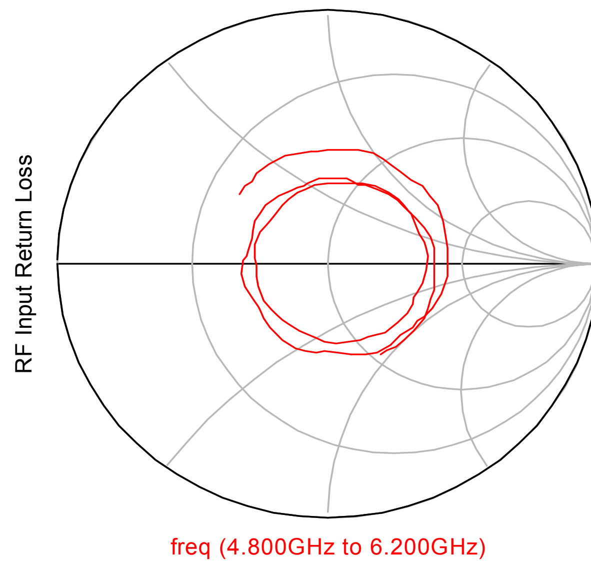


Figure D.4: Measured RF port impedence for the mixer in this thesis.

Bibliography

[1] Federal Communications Commission, *Unlicensed NII Devices in the 5 GHz Frequency Range [ET Docket No. 96-102; FCC 97-5]*, Jan. 1997.

[2] M. Soyuer, H. A. Ainspan, J. N. Burghartz, J.O. Plouchart, B. P. Gaucherand T. J. Beukema, F. J. Canora, E. Pilmanis, and M. M. Oprysko, "A cost-effective approach to a short-range, high-speed radio design in the U-NII 5.x GHz band," in *Proceedings of the IEEE 1998 Radio and Wireless Conference*, 1998, pp. 133–136.

[3] J. D. Cressler, "SiGe HBT technology: A new contender for Si-based RF and microwave circuit applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 5, pp. 572–589, May 1998.

[4] P. Narozny, M. Hamacher, H. Dambkes, H. Kibbel, and E. Kasper, "Si/SiGe heterojunction bipolar transistor with graded gap SiGe base made by molecular beam epitaxy," in *Proceedings of the IEEE 1988 Electron Devices Meeting*, 1988, pp. 562–565.

[5] W. Winkler, and B. Heinemann J. Borngraber, and H. Erzgraber, D. Knoll, H. J. Osten, M. Pierschel, K. Pressel, and P. Schley, "Wireless communication integrated circuits with CMOS-compatible SiGe HBT technology modules," in *Proceedings of the IEEE 1998 Custom Integrated Circuits Conference*, 1998, pp. 15.3.1–15.3.7.

[6] M. Ono, N. Suematsu, S. Kubo, Y. Iyama, T. Takagi, and O. Ishida, "1.9GHz/5.8GHz-band on-chip matching Si-MMIC low noise amplifiers fabricated on high resistive substate," in *IEEE 1999 Radio Frequency Integrated Circuits Symposium Digest*, 1999, pp. 189–192.

[7] K. Joardar, "A simple approach to modeling cross-talk in integrated circuits," *IEEE Journal of Solid State Circuits*, vol. 29, pp. 1212–1219, Oct. 1994.

[8] Y. Chih and M. Chen, "Design model and guidelines for N-well guard ring in epitaxial CMOS," *IEEE Transactions on Electron Devices*, vol. 41, pp. 1806–1810, Oct. 1994.

[9] K. Joardar, "Comparison of SOI and junction isolation for substrate cross-talk suppression in mixed-mode integrated circuits," *IEEE Electron Device Letters*, vol. 31, no. 15, pp. 1230–1231, July 1995.

[10] J.-S Rieh, L. Lu, L. P. B. Katehi, P. Bhattacharya, E. T. Croke, G. E. Ponchak, and S. Alterovitz, "X- and Ku-band amplifiers based on Si/SiGe HBT's and micromachined lumped components," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 5, pp. 685–694, May 1998.

[11] D. C. Ahlgren, N. King, G. Freeman, R. Groves, and S. Subbanna, "SiGe BiCMOS technology for RF device and design applications," *Proceedings of the IEEE 1999 Radio and Wireless Conference*, pp. 281–284, 1999.

[12] L. Tao, J.A Pla, P. H. Aaen, and M. Mahalingam, "Equivalent-circuit modeling and verification of metal-ceramic packages for RF and microwave power transistors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 6, pp. 709–714, June 1999.

[13] S. Donnay, P. Pieters, K. Vaesen, W. Diels, P. Wambacq, W. D. Raedt, E. Beyne, M. Engels, and I. Bolsens, "Chip-package codesign of a low-power 5-GHz RF front end," in *Proceedings of the IEEE*, Oct. 2000, vol. 88, pp. 1583–1597.

[14] R. Charpurey and T. R. Viswanathan, "Design of front-end RF circuits," in *IEEE 1999 Southwest Symposium on Mixed-Signal Design Digest*, 1999, pp. 134 –139.

[15] B. Gilbert, *The Design of Bipolar Si/SiGe LNAs from the Ground Up*, Analog Devices, Mar. 1998.

[16] H. L. Krauss, C. W. Bostian, and F. H. Raab, *Solid State Radio Engineering*, John Wiley and Son, Inc., New York, New York, 1st edition, 1980.

[17] B. Razavi, *RF Microelectronics*, Prentice Hall PTR, Upper Saddle River, New Jersey, 1st edition, 1998.

[18] J. Plouchart, H. Ainspan, and M. Soyuer, "A 5.2 GHz 3.3 V I/Q SiGe RF transceiver," *Proceedings of the IEEE 1999 Custom Integrated Circuits Conference*, pp. 217–220, 1999.

[19] B. Foleyand P. Murphy and A. Murphy, "A monolithic SiGe 5 GHz low noise amplifier and tuneable image-reject filter for wireless LAN applications," *High Frequency Postgraduate Student Colloquium*, pp. 26–31, 2000.

[20] S. Yoo, D. Heo, J. Laskar, and S.S. Taylor, "A C-band low power high dynamic range GaAs MESFET low noise amplifier," in *Proceedings of the IEEE 1999 Radio and Wireless Conference*, 1999, pp. 191–194.

[21] B. K. Ko and K. Lee, "A comparative study on the various monolithic low noise amplifier circuit topologies for RF and microwave applications," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 8, pp. 1220–1225, Aug. 1996.

[22] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 5, pp. 745–759, May 1997.

[23] R. Myer and W. Mack, "A 1-GHz BiCMOS RF front-end IC," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 3, pp. 350–355, Mar. 1994.

[24] Agilent Technologies, *EESof Advanced Design System V1.3*, Agilent Technologies, Palo Alto, CA, 1999.

[25] M. Forrester, "Conversation on bondwire modeling," Personal communication, RF Microdevices, 2000.

[26] O. Shana'a, I. Linscott, and L. Tyler, "Frequency-scalable SiGe bipolar RFIC fron-end design," in *Proceedings of the IEEE 2000 Custom Integrated Circuits Conference*, 2000, pp. 183–186.

[27] S. Gerlach R. Gotzfried and, F. Beisswanger and, "Design of RF integrated circuits using SiGe bipolar technology," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 9, pp. 1417–1422, Sept. 1998.

[28] Cadence Design Systems Inc., Sunnyvale, CA, *Cadence Virtuoso V4.4.3*, 1998.

[29] U. Lott, "Low DC power monolithic low noise amplifier for wireless applications at 5 GHz," in *IEEE 1996 Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest*, 1996, pp. 81 –84.

[30] H. Ainspan, M. Soyuer, J.-O. Plouchart, and J. Burghartz, "A 6.25-GHz low DC power low-noise amplifier in SiGe," in *Proceedings of the IEEE 1997 Custom Integrated Circuits Conference*, 1997, pp. 177–180.

[31] U. Erben, H. Schumacher, A. Schuppen, H. Dietrich, and J. Arndt, "Application of a production ready SiGe HBT process to 1.9, 5.7 and 10 GHz low noise MMICs," in *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 1998, pp. 100 –104.

[32] R. B. Marks and D. F. Williams, *Multical V1.00*, NIST, Boulder, CO, 1995.

[33] "Noise figure measurements: Principles and applications," Application note, Hewlett Packard, Jan. 1989.

[34] T. J. Colvin, S. S. Bhatia, and K. K. O, "A bond-pad structure for reducing effects of substrate resistance on LNA performance in a silicon bipolar technology," in *Proceedings of the IEEE 1998 Bipolar/BiCMOS Circuits and Technology Meeting*, 1998, pp. 109 –112.

[35] S. Raman, F. Rucky, and G. M. Rebeiz, "A high-performance W-band uniplanar subharmonic mixer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 6, pp. 955 –962, 1997.

[36] Kok Yon-Lin, M. Ahmad, Wang Huei, B.R. Allen, and T. Lin, "A Ka-band monolithic single-chip transceiver using sub-harmonic mixer," *IEEE 1998 MTT-S International Microwave Symposium Digest*, vol. 1, pp. 309 –311, 1998.

[37] K. Z. Cai and P. Mambo, "Subharmonic mixers simplify high frequency designs for personal communications system," in *Proceedings of the 4th International Conference on Millimeter Wave and Far Infrared Science and Technology*, 1996, pp. 169 –172.

[38] H. Zirath, I. Angelov, and N. Rorsman, "A millimeterwave subharmonically pumped resistive mixer based on a heterostructure field effect transistor technology," in *IEEE 1992 MTT-S International Microwave Symposium Digest*, 1992, vol. 2, pp. 599–602.

[39] B. Matinpour and S. Chakraborty J. Laskar, "A compact monolithic C-band direct conversion receiver," *IEEE Microwave and Guided Wave Letters*, vol. 10, no. 2, pp. 67 –69, Feb. 2000.

[40] T. Yamaji, H. Tanimoto, and H. Kokatsu, "An I/Q active balanced harmonic mixer with IM2 cancelers and a 45deg phase shifter," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 2240 –2246, Dec. 1998.

[41] L. Sheng, J. Jensen, and L. Larson, "A Si/SiGe HBT sub-harmonic mixer/downconverter," *Proceedings of the IEEE 1999 Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 71–74, 1999.

[42] K. Nimmagadda and G. M. Rebeiz, "A 1.9 GHz double-balanced subharmonic mixer of direct conversion receivers," in *To appear in the IEEE 2001 RFIC Symposium Digest*, 2001.

[43] B. Razavi, "A 1.5 V 900MHz downconverion mixer," in *Proceedings of the IEEE 1996 International Solid-State Circuit Conference*, 1996, pp. 48–49.

[44] A. Vauhkonen and K. J. Grahn, "Low power down-conversion RF mixer based on the gilbert cell approach," *Analog Integrated Circuits and Signal Processing*, vol. 18, pp. 33–42, 1999.

[45] P. R. Grey and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiley and Sons, Inc., New York, New York, third edition, 1993.

[46] S. V. Kishore, C. Glenn, and C. Hull, "A SOI-BiCMOS RF-transmitter for personal digital cellular communication (PDC)," in *IEEE 2000 Symposium on VLSI Circuits Digest*, 2000, pp. 62 –65.

[47] Y. Koutsoyannopoulos, Y. Papananos, S. Bantas, and C. Alemanni, "Novel Si integrated inductor and transformer structures for RF IC design," *Proceedings of the IEEE 1999 International Symposium on Circuits and Systems*, vol. 2, pp. 573 –576, 1999.

[48] D. C. Laney, L. E. Larson, J. Malinowski P. Chan, D. Harame, S. Subbanna, R. Volant, and M. Case, "Lateral microwave transformers and inductors implemented in a Si/SiGe HBT process," in *IEEE 1999 MTT-S International Microwave Symposium Digest*, 1999, pp. 855–858.

[49] D. Curran, "Conversation on differential amplifiers," Personal communication, RF Microdevices, 2000.

[50] B. De Muer M. Borremans and and M. Steyaert, "The optimization of GHz integrated CMOS quadrature VCO's based on a poly-phase filter loaded differential oscillator," in *The IEEE 2000 International Symposium on Circuits and Systems Digest*, 2000, vol. 2, pp. 729 –732.

[51] Agilent Technologies, *VEE*, Palo Alto, CA, 1998.

[52] Agilent Technologies, "MixerDiffMode," Example project included within ADS v.1.3.

Vita

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After college graduation, Daniel worked for Alcatel Telecom as a hardware engineer. There, he participated in the design of ADSL (Asymmetric Digital Subscriber Line) modems and performed standards work. He also worked at an independent contractor where he designed an ADSL reference analog front-end for Virata Communications. In August, 1999 Daniel returned to Virginia Tech to pursue graduate studies in Electrical Engineering.

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