Chapter 1. Introduction

In this chapter, ferroelectric materials are briefly introduced with emphasis on their non-volatile memory properties and their potential impact on the current state of digital memories. In the first section, ferroelectric materials are described in terms of their characteristic non-volatile memory properties. In the second section, the current state-of-the art in ferroelectric memories is illustrated, and the applications of ferroelectric materials to commercial memory devices are discussed. In the third section, current processing and integration issues for developing high density ferroelectric random access (FRAM) devices are addressed. Finally, the specific objectives of this research are outlined in the last section.

1.1 FERROELECTRIC MATERIALS

Ferroelectric materials are generally defined by reversible spontaneous polarization in the absence of electric field [1]. The spontaneous polarization is generated from noncentrosymmetric arrangement of ions in unit cell, which produces an electric dipole moment related to the unit cell. Adjacent unit cells are inclined to polarize in the same direction and form a region called a ferroelectric domain. Unit cell of typical ferroelectric material, ABO_3, is illustrated in Figure 1.1 where A atom, B atom, and oxygen occupy the corner site, body-centered site, and face-centered site, respectively. The ferroelectric materials exhibit a characteristic hysteresis loop as shown in Figure 1.2. When an electrical field is applied to the ferroelectric material, the B atom, which has two thermodynamically stable positions inside oxygen octahedra, is displaced relative to the oxygens upward or downward, depending on the polarity of the electric field. This displacement generates a dipole moment inside the oxygen octahedra, which is called as saturated polarization

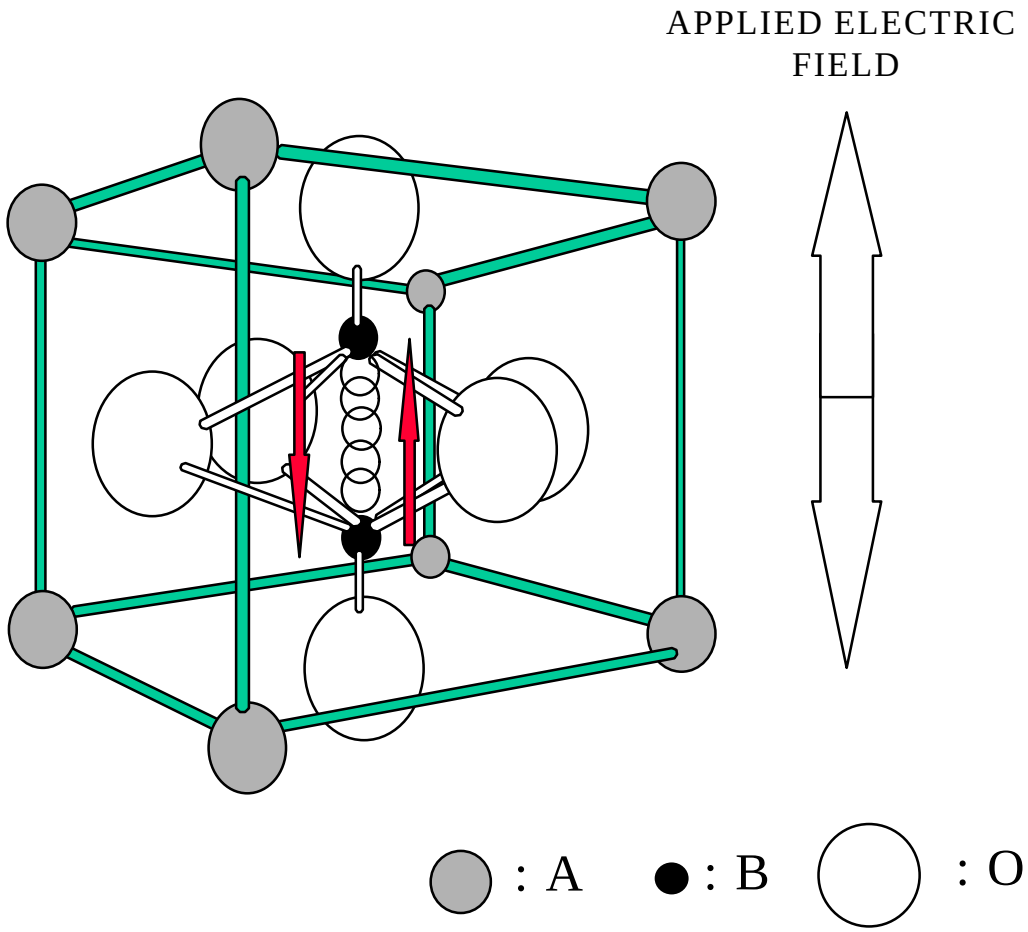

Figure 1.1 ABO_3 perovskite unit cell

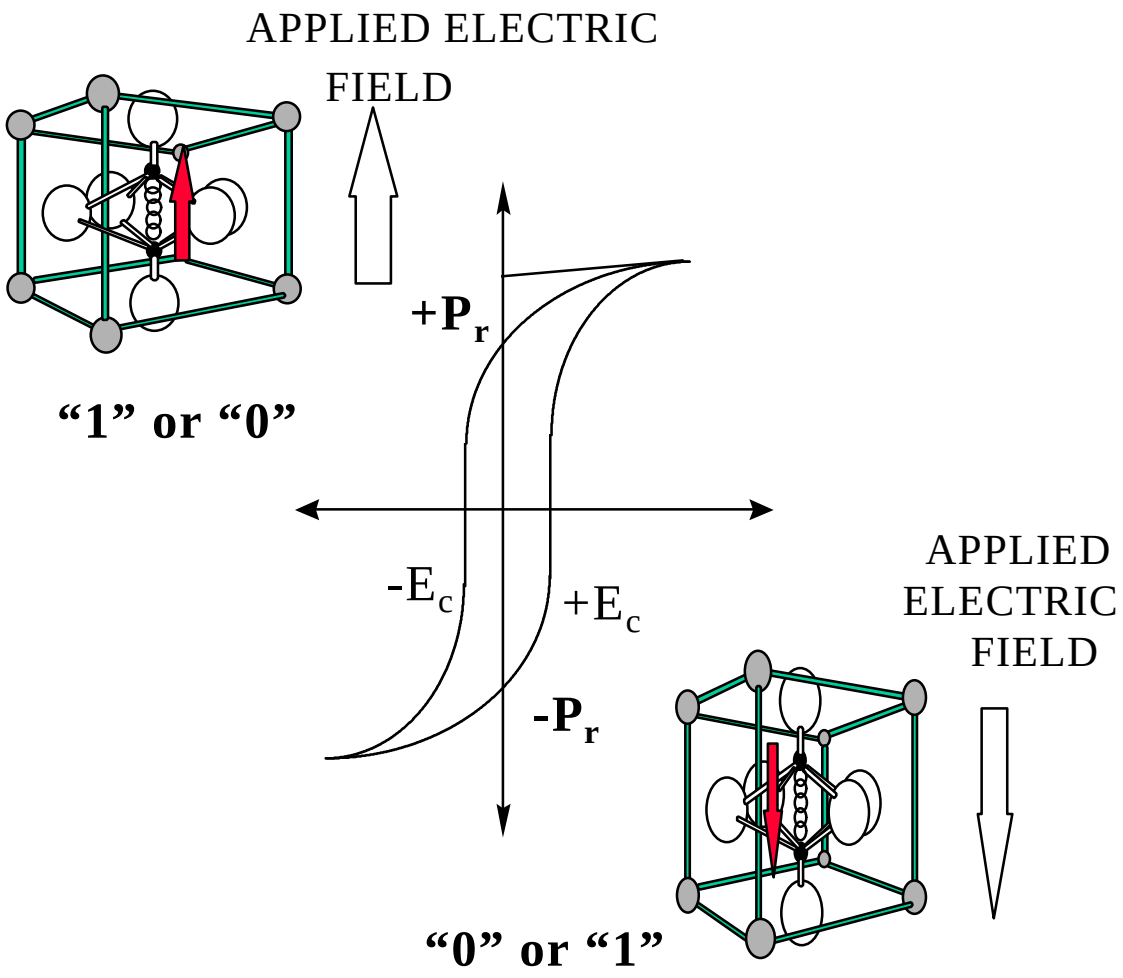

Figure 1.2 Hysteresis loop of a ferroelectric material

($\pm P_s$). When the applied electric field is removed, the B atom remains in the displaced position and generates a residual polarization in the absence of applied electric field, or remanent polarization ($\pm P_r$). In order to reverse the direction of polarization, we need to apply a coercive electric field ($\pm E_c$), which is defined as a minimum electric field for switching the polarization. Therefore, the basic characteristics of a ferroelectric material that make it suitable for non-volatile memory applications are its ability to retain two stable remanent polarization values at zero field, thus providing nonvolatility. The state of polarization can be controlled and sensed by reversing the polarization from up (+1) to down (0) or vice versa as a function of applied voltage.

1.2 FERROELECTRIC MEMORIES

In general, there are two major memory applications for ferroelectrics. First, ferroelectric materials are incorporated into dynamic random access memory (DRAM) [2]. Second, they are used in non-volatile ferroelectric RAM (FRAM) [3]. Since ferroelectric materials typically show large dielectric constant, the ferroelectric thin films have been considered as a strong candidate for high density DRAM application. As the density of DRAM increases over 1 Gbit, the unit cell size is tremendously reduced so that current dielectric layer, SiO_2, is regarded as impractical for the high density DRAM due to low dielectric constant. There have been attempts to overcome the low dielectric constant problem by developing a trench or stack structure, which provides greater capacitative area, and thus increases the capacitance charge [4]. However, these designs will make the processing undoubtedly complicated and thus not be suitable for the 1 Gbit or 4 Gbit DRAM. Practically, the charge storage capability can be improved by increasing the capacitative area or dielectric constant in the given thickness of dielectric layer. Therefore, the other reasonable choice is to look for dielectric materials which have significantly high dielectric constants. Since most of the commonly used ferroelectrics have dielectric constant at least two

orders of magnitude higher than that of SiO_2, the ferroelectric thin films can be used as nonswitching capacitor materials in 1 Gbit DRAM.

In addition to the high dielectric constants, the ferroelectric materials also exhibit characteristic polarization response to an electric field, which makes them potential candidate materials for use as nonvolatile memory devices. The information in current DRAM is stored in the form of charge in a linear capacitor. In order to maintain the stored information securely, a constant voltage is always required on the capacitor which is recharged by a refresh circuitry hundreds of times every second. If the power is interrupted, the DRAM forgets the information stored in it (volatile). In contrast, the information in ferroelectric memories is stored in the polarization states ($\pm P_r$) of the ferroelectric material itself. The ferroelectric capacitor has a highly nonlinear dielectric with permanent charge retention capabilities after application of a voltage by an external circuit. Therefore, the stored information cannot evaporate even when the power is turned off (non-volatile). Table 1.1 summarizes the state of the art in nonvolatile memory technologies [5]. The main advantages of FRAM over other non-volatile memories are fast write and erase access times on the order of nanoseconds, low operating voltages around 5 V, long write/erase lifetime (10^6 times higher than the EEPROM and flash memories), wide operating temperature range (-180 °C to 350 °C), and high radiation hardness required for military and space applications. In principle, the FRAM could replace the SRAM in cache memory, DRAM in main computer memory, and EEPROM in the lookup tables. Furthermore, if high density FRAM can be developed, and its cost can be reduced to the level of magnetic core, it could also replace the hard disk as the mass storage device, because the FRAM has faster access speed and no mechanical wear problems. Therefore, these researches mainly aim to develop the high density FRAM as future memories. Table 1.2 shows the prospect of several integrated ferroelectric devices [5].

Table 1.1 State of the Art in Nonvolatile memory Technologies

	Floating Gate EEPROM	Flash EEPROM	Silicon/ Nitride/ Oxide/ Silicon	Metal/ Nitride/ Oxide/ Semiconductor	Ferroelectric Destructive Read-Out	Ferroelectric Nondestructive Read-Out	Magnetic RAMs
Size	1 Mbit	1 Mbit	8 Kbit x 8	1 Mbit	1 Mbit	1 Kbit x 8	16 Kbit x 1
Speed (Access)	150 ns	120 ns	35 ns	150 ns	60 ns	200 ns	200 ms - 2 μs
Write Time	10 ms/byte	high	35 ns, 11 ms rewrite time	10 ms/byte	60 ns	100 ns	100 ns
Endurance	10^5 writes	10^4 writes	10^5 read-write	10^5 writes	10^{12} read-write	10^{12} writes	no limits
Source	Xicor Atmel Seeq	Intel Atmel AMD	Simtek	Hitachi	NEC	Westinghouse	possibly: Honeywell NVE

Table 1.2 Prospects for Integrated Ferroelectrics

Device	Ferroelectric Random Access Memory (FRAM) Destructive Read-Out	Ferroelectric RAM Nondestructive Read-Out	High-Dielectric Dynamic Random Access Memory	High Dielectric Bypass Capacitors on GaAs	Room-Temperature Pyroelectric Detectors
Material	$SrBi_2Ta_2O_9$ $Pb(Zr_{1-x}Ti_x)O_3$	BaMgF4 Bismuth Titanate $SrBi_2Ta_2O_9$	$(Ba,Sr)TiO_3$ (BST)	BST	Scandium Tantalate?
Market Date	256 Kbit in 1994	1997?	64 Mbit in 1996	1993	1994-5
Supplier	Matsushita Micron Symetrix Ramtron Seiko	Westinghouse Symetrix	Matsushita Olympus NEC Samsung	Panasonic -National	GEC-Marconi Mitsubishi
Problems	scaling to high density	Si interface	leakage current	none	processing temperature

1.3 BASIC OPERATION

The FRAM devices are divided into two categories, based on the readout technique: destructive read-out (DRO) FRAM and non-destructive read-out (NDRO) FRAM [6-7]. In the DRO FRAM devices, the ferroelectric thin films are used as a capacitor material, which is incorporated into complementary metal-oxide-semiconductor (CMOS) transistor. The basic unit of DRO FRAM devices is 1 transistor and 1 capacitor. The CMOS transistor provides electrical isolation to each memory cell, allowing the circuit to select which capacitor is to be switched and creating individually addressable bits. The stored information is read by sensing the electrical charge created by switching the polarization of ferroelectric materials in the capacitor. After the reading operation, the polarization state is changed from $+P_r$ to $-P_r$ or vice versa. Thus, the information must be rewritten for restoring the polarization state after every read operation. On the other hand, in the NDRO FRAM, the ferroelectric thin films are employed as the gate material in the transistor, and thus, no additional capacitor layer is needed. The basic unit of NDRO FRAM device is 1 transistor. The information is read by sensing the modulation of surface conductivity of the silicon. The surface conductivity is controlled by the remanent polarization of the ferroelectric films rather than the polarization switching, which is seen in the DRO FRAM devices. Therefore, the information can be read over and over again until the next write operation.

1.3.1 Destructive Read-Out FRAM

In DRO device, reading operation is carried out destructively i.e. reversing the original polarization state, and reading the switching current. Figure 1.3 illustrates the reading procedure of DRO FRAM. In order to read the stored information, a reading pulse higher than coercive

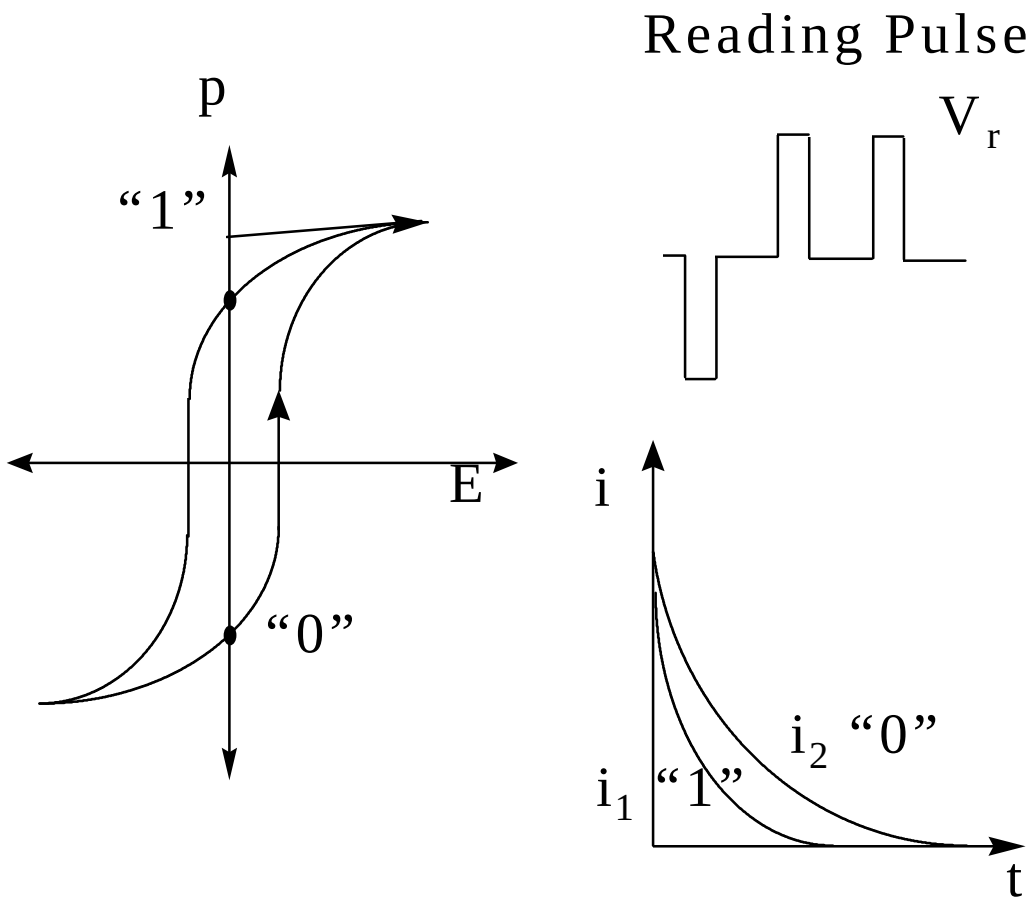

Figure 1.3 Reading procedure of DRO FRAM devices.

electric field is applied, and two distinguishable currents are generated from the displacement of polarization. For example, if a positive reading pulse is applied, $+P_r$ and $- P_r$ are displaced to $+P_s$, giving rise to current I_1 and I_2, respectively. I_1 is a non-switching current which is generated only from dielectric component of the ferroelectric films, while I_2 is a full switching current, which is generated from both ferroelectric domains and dielectric component. Therefore, the difference between these two currents corresponds to the net amount of switched charge for each polarization reversal. The memory devices can read the stored information by sensing the two different currents. After reading operation, $-P_r$ is reversed to $+ P_r$, which results in destroying the original stored information. Thus, reset procedure is required to restore the switched polarization state to the original position and secure the stored information. Even though this DRO FRAM needs a reset pulse, it has advantage of very fast access speed over NDRO FRAM.

1.3.2 Nondestructive Read-Out FRAM

The major difference between DRO and NDRO memories is the polarization switching, which is necessary for reading operation in the DRO device. On the other hand, the NDRO device reads the stored data by sensing the modulation of the surface conductivity of the silicon rather than switching the polarization state. Figure 1.4 shows how the NDRO devices store and read information. Since the surface conductivity of the silicon depends on the direction of remanent polarization, “on” or “off” channel is generated on the surface of the silicon. If ferroelectric films are prepared on p-type Si, and a positive voltage is applied to the films, the direction of polarization goes down and induces the negative charges on the surface of the silicon, giving rise to conductive channel (“on”) on the substrates. Even though the applied voltage is removed, the “on” channel is maintained due to the remanent polarization of the ferroelectric films. In case of applying a negative voltage, the opposite positive charges are induced on the surface of the silicon, generating non-conductive (“off”) channel. These “on” and

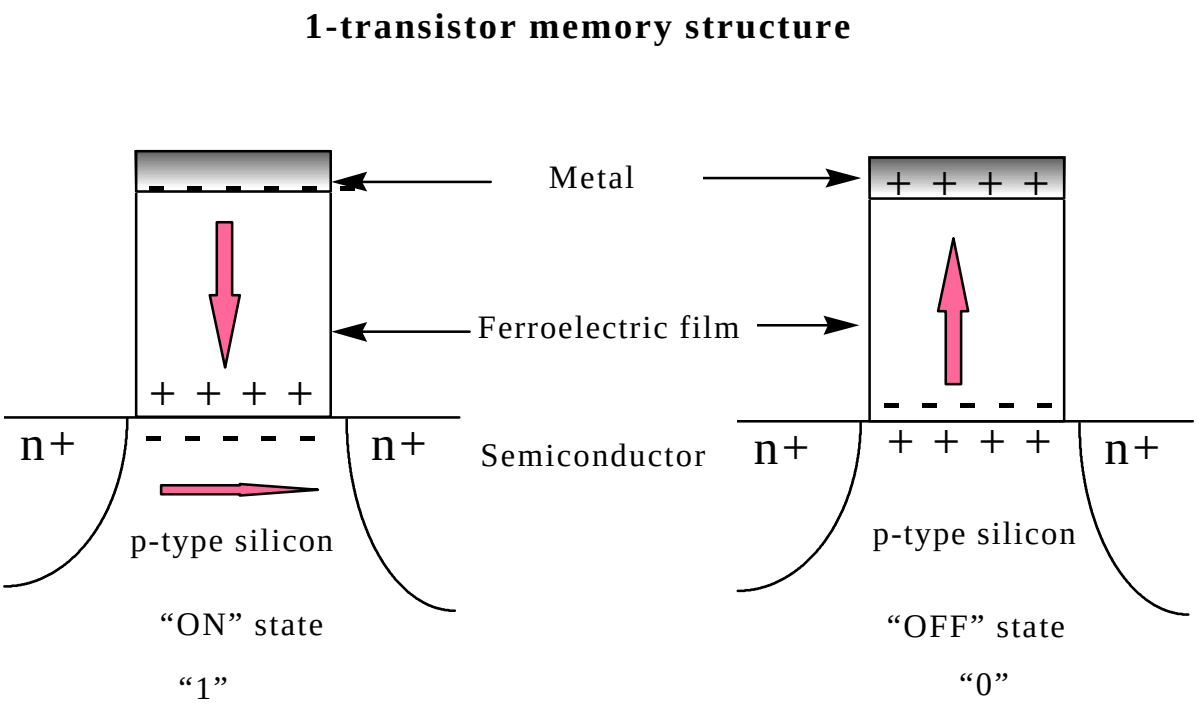

Figure 1.4 Schematic view of NDRO FRAM structure

“off” channels work as binary (“0” and ‘1”) in the memory logic. The reading operation is thus carried out by identifying whether the current flows from source to drain or not. This reading method provides a privilege of non-destructive readout and eliminates the reset procedure.

1.4 PURPOSE OF RESEARCH

1.4.1 Destructive Readout (DRO) FRAM

There has been significant progress in ferroelectric memory technology, but the commercial high density DRO FRAMs are still restricted by several challenging problems such as reliability and integration issues. In particular, the integration issue is very critical for achieving the high density DRO FRAMs. The basic unit of the current DRO FRAM is 1 transistor and 1 capacitor, shown in Figure 1.5, where ferroelectric thin films are used as capacitor materials. The cross-sectional view illustrates the structure of low density and high density DRO FRAM device. As the memory density increases, the cell areas are so tremendously reduced that the capacitor is stacked on the top of the transistor rather than being placed next to the transistor, which is seen in low density memory devices. This stacked structure demands the use of the plug (polysilicon) in high density DRO FRAM to establish communication between the ferroelectric capacitor and the transistor. Typically, ferroelectric films are prepared at relatively high annealing temperature in strong oxygen environment, which causes the polysilicon to be easily oxidized and form an insulating layer such as SiO_2. Since the insulating layer severely destroys the device performance, barrier layers are required to prevent the undesired layer. Ideal diffusion barrier layers should exhibit good adhesion to the plug, excellent electrical conductivity, and maintain their conductivity at ferroelectric processing temperatures [8-10]. However, the currently used diffusion barrier layers are stable only up to

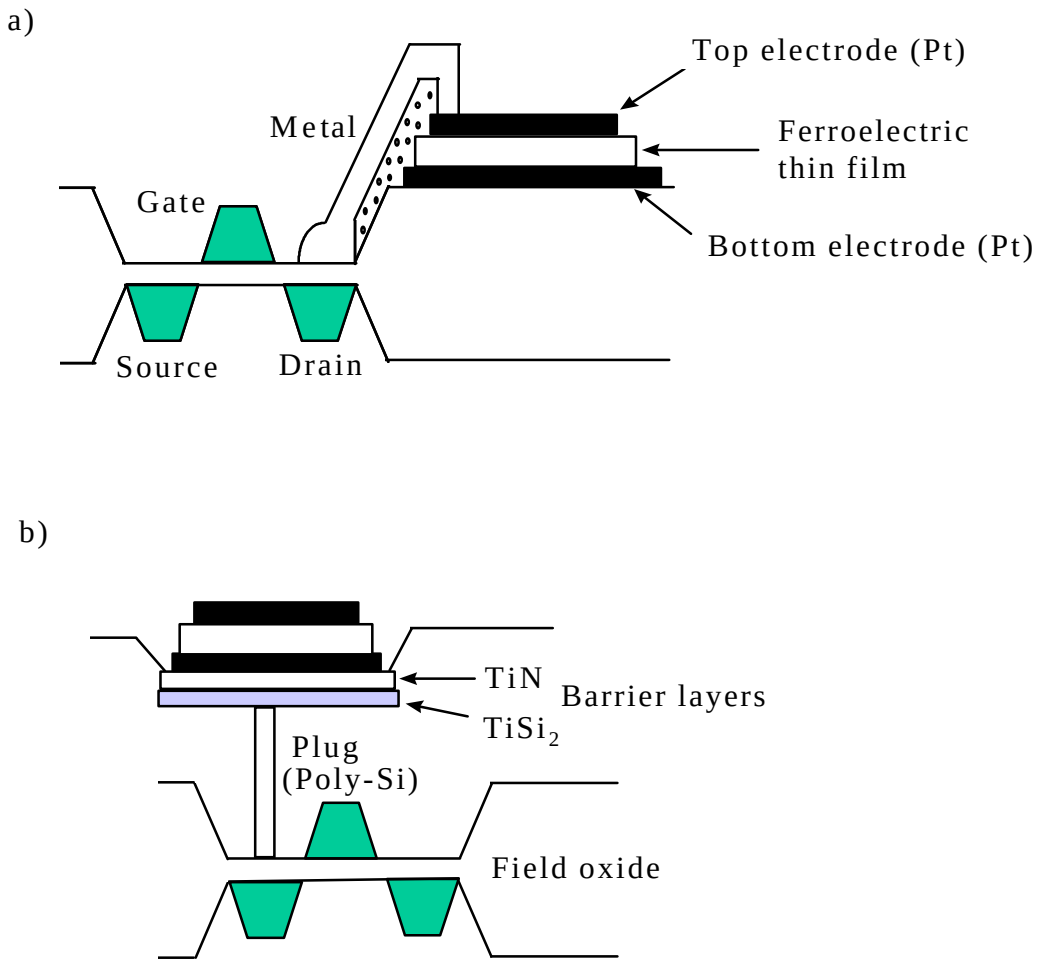

Figure 1.5 Cross sections of DRO FRAM cell structure in a) low density device and b) high density device.

550 °C, which is lower than the typical ferroelectric processing temperatures (>650 °C). After integrating the ferroelectric films into the polysilicon, the barrier layers lose their conductivity and become insulating. Therefore, in order to integrate the ferroelectric films into the existing diffusion barrier layers, low temperature processing (<550 °C) is strongly demanded.

The processing issues involved in the high density integration process are highly dependent on the ferroelectric and electrode-barrier materials. Hence, the selection of materials is a critical factor in determining the performance of the device. There have been numerous researches on developing ideal ferroelectric thin films for the high density DRO FRAM. The ideal ferroelectric material should possess a high remanent polarization (P_r), low coercive electric field (Ec), low dielectric loss, low leakage current, low processing temperature, good thermal stability and high but suitable Curie temperature for curing process. Some of the suggested major requirements for ferroelectric capacitors for DRO FRAM applications are listed as follows [2-4]:

(1) The lower limit of charge capacity should be from 5 - 10 $\mu C/cm^2$.

(2) The coercive electric field should not be greater than 50 - 60 kV/cm.

(3) The desirable dielectric constant is around 500.

(4) Leakage current density should be smaller than 10^{-8} A/cm^2 at an operating voltage of 5 V.

(5) Fatigue lifetime up to 10^{12} cycles, the ideal lifetime being 10^{15} cycles.

(6) Wide operating temperature range: -55 °C to 120 °C.

(7) Compatible with VLSI process.

(8) Etch rates at least 20 nm/min.

It is now widely recognized that $Pb(Zr_{1-x}Ti_x)O_3$ (PZT) and $SrBi_2Ta_2O_9$ (SBT) are most promising materials for the DRO FRAM application [11-12]. PZT and SBT films have their own pros and cons. The PZT thin films show excellent ferroelectric properties such as large P_r and

small E_c, and relatively low processing temperature, but are severely degraded during switching cycles. On the other hand, the SBT thin films exhibit very low coercive electric field and no degradation over repetitive switching cycles, but shows very high processing temperature (750 °C), which is a crucial restriction for achieving high density DRO FRAM. Therefore, in this research, the PZT films are selected over the SBT films, because low processing temperature and higher P_r are most important requirement to be satisfied for high density memory devices. Chapter 2 and 3 are devoted to lowering the processing temperature and investigating the electrical properties of PZT films.

Electrode and barrier materials are also critical in determining the performance of DRO FRAM device. Thus, the electrode-barrier materials have been intensively investigated associated with the integration issue. Ideal electrode material should have excellent compatibility with VLSI processing, high electrical conductivity, no interaction with ferroelectric and substrate materials at the ferroelectric processing temperature, and amenability to dry etching. One of currently used electrode materials is platinum (Pt), which has several advantages of high electrical conductivity and outstanding chemical and thermal stability. The high density integration requires barrier layers between electrode and polysilicon plug for preventing oxygen diffusion into the plug. Ideal diffusion barrier layers should exhibit good adhesion to the plug, excellent electrical conductivity, and maintain their conductivity at ferroelectric processing temperatures. The most used barrier layers in low density FRAM are titanium silicide and titanium nitride, which have poor thermal stability at the ferroelectric processing temperature (<600 °C) [13-16]. Therefore, it is desired to develop high temperature electrode-barrier layers for the high temperature processing. In Chapter 4, hybrid multi-electrode barrier layers are introduced and discussed as the high temperature electrode-barrier layers.

1.4.2 Non-Destructive Readout (NDRO) FRAM

The processing of ferroelectric materials on silicon substrate is a major concern for NDRO FRAM applications. The basic unit of the ferroelectric non-destructive readout (NDRO) device is 1 transistor (1T), which serves both as the storage element and the sensing device. Since the ferroelectric materials are directly processed on Si substrates at high temperature, there is always undesired reaction between the ferroelectric materials and the Si substrate. Therefore, two device structures are utilized in the NDRO FRAMs: a metal-ferroelectric-semiconductor (MFS) or metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure [17-18]. In the MFMIS structure, an insulating barrier layer such as SiO_2 and metal layer are inserted between the ferroelectric films and the silicon, and no undesired reaction occurs between ferroelectric films and silicon. However, the actual voltage applied to the ferroelectric films is too small to switch the domain, because the applied voltage is divided into SiO_2 and ferroelectric films. The amount of divided voltage is inversely proportional to the dielectric constant. In general, the dielectric constant of the ferroelectric films is around 300 - 800, which is two order higher than that of SiO_2. Most of applied voltage is loaded on SiO_2, and eventually causes an electrical breakdown as the voltage is increased for domain switching in the ferroelectric films. Therefore, ideal ferroelectric materials for the NDRO device should possess low dielectric constant and low coercive electric field. Chapter 5 presents novel ferroelectric materials for satisfying these requirements. Some of the suggested requirements of ferroelectric thin films for NDRO FRAM applications are summarized below [5,7].

(1) No interaction with Si substrate.

(2) Desirable dielectric constant less than 100.

(3) Small coercive electric field.

(4) Low remanent polarization.

(5) Leakage current smaller than 10^{-8} A/cm^2.

1.5 OBJECTIVES OF RESEARCH

The objectives of this research are outlined as follows:

1. To develop a low temperature processing of PZT thin films based on the understanding of the PZT transformation kinetics.
2. To demonstrate the integration of PZT films into existing barrier layers.
3. To optimize the fabrication of novel barrier layers for high temperature processing.
4. To devise chemical processing procedures of $Sr_2(Ta_{1-x}Nb_x)_2O_7$ thin films.
5. To investigate the effect of compositional ratio on the structural and electrical properties of $Sr_2(Ta_{1-x}Nb_x)_2O_7$ thin films.

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