Digital-Based Zero-Current Switching (ZCS) Control Schemes for Three-Level Boost Power-Factor Correction (PFC) Converter

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ABSTRACT

With the increasing demands on electronic loads (e.g. desktop, laptop, monitor, LED lighting and server) in modern technology-driven lives, performance of switched-mode power supply (SMPS) for electronics have been growing to prominence. As front-end converters in typical SMPS structure, ac-dc power-factor correction (PFC) circuits play a key role in regulations of input power factor, harmonics and dc output voltage, which has a decisive effect on entire power-supply performances. Universal ac-line and low-power system (90–264 V_{rms}, up to 300–400 W) is one of the most common power-supply specifications and boost-derived PFC topologies have been widely used for the purpose. In order to concurrently achieve high efficiency and low-cost system in the PFC stage, zero-current switching (ZCS) control schemes are highly employed in control principles. Representative schemes are discontinuous conduction mode (DCM) and critical conduction mode (CRM). Both modes can realize ZCS turn-on without diode reverse recovery so that low switching losses and low-cost diode utilizations are obtainable.

Among various boost-family PFC topologies, three-level boost (TLB) converter has generated considerable research interest in high-voltage high-power applications. It is mainly due to the fact that the topology can have halved component voltage stresses, improved waveform qualities and electromagnetic interference (EMI) from phase interleaved continuous conduction mode (CCM) operations, compared to other two-level boost PFC

converters. On the other hand, in the field of universal-line low-power applications, TLB PFC has been thoroughly out of focus since doubled component counts and increased control complexity than two-level topologies are practical burden for the low-cost systems. However, recent researches on TLB PFC with ZCS control schemes have found that cost-competitiveness of the topology is actually comparable to two-level boost PFC converters because the halved component voltage stresses enable usage of low voltage-rating components of which unit prices are cheaper than higher-rating ones. Based on the justification, researches on ZCS control schemes for TLB PFC have been conducted to get enhanced waveform qualities and performance factors.

Following the research stream, a three-level current modulation scheme that can be adopted in both DCM and CRM is proposed in Chapter 2 of this dissertation. Main concept of the proposed current modulation is additional degree-of-freedom in current-slope shaping by differentiating on-times of two active switches, which cannot be found from any other single-phase boost-derived PFC topologies. Using the multilevel feature, proposed operations in one switching period consist of three steps: common-switch on-time, single-switch on-time and common-switch off-time. The single-switch on-time step is key design factor of the proposed modulation that can be utilized either in fixed or adjustable form depending on control purpose. Based on the basic modulation concept, three-level CRM control scheme, adjustable three-level DCM control scheme, and spread-spectrum frequency modulation (SSFM) with adjustable three-level DCM scheme are proposed in Chapter 3–5, respectively.

In each chapter, implemented control scheme aims to improve different performance factors. In Chapter 3, the proposed three-level CRM scheme uses increased single-switch on-time period to reduce peak inductor current and magnitude of variable switching frequency. It

is generally accepted fact that CRM operations suffer from high switching losses and poor efficiency at light load due to considerable increment of switching frequency. Thus, efficiency improvement effect by the proposed CRM scheme becomes remarkable as load condition goes lighter. In experimental verifications, maximum improvement is measured by 1.2% at light load (20%) and overall efficiency is increased by at least 0.4% all over the load range. In Chapter 4, three-level DCM control scheme adopts adjustable single-switch on-time period in fixed switching-frequency framework. The purpose of adjustable control scheme is to widen the length of non-zero inductor current period as much as possible so that discontinued current period and high peak current of DCM operations can be minimized. Experiment results show that, compared to conventional two-level DCM control, full-load peak inductor currents are reduced by 20.2% and 17.1% at 110 and 220 V_{rms} input voltage conditions, respectively. Moreover, due to turn-off switching energy decrements by the turn-off current reductions, efficiency is also improved by at least 0.4% regardless of input voltage and load conditions. In Chapter 5, a downward SSFM technique is developed first for DCM operations of boosting PFC converters including two-level topologies. This chapter aims to achieve significant reduction of high differential-mode (DM) EMI amplitudes from DCM operations, which is major drawback of DCM control. By using the simple linearized frequency modulation, peak DM EMI noise at full load condition is reduced by 12.7 dBμV than conventional fixed-frequency DCM control. On top of the proposed SSFM, the adjustable three-level DCM control scheme in Chapter 4 is adopted to get further reductions of EMI noises. Experimental results prove that the collaborations of SSFM and adjustable DCM scheme reduce the EMI amplitudes further by 2.5 dBμV than the result of SSFM itself. The

reduced EMI amplitudes are helpful to design input EMI filter with higher cut-off frequency and smaller size.

Different from two-level boosting PFC converters, TLB PFC topology has two output capacitors in series and inherently suffers from voltage unbalancing issue, which can be noted as topological trade-off. In Chapter 6, two simple but effective voltage balancing schemes are introduced. The balancing schemes can be easily built into the proposed ZCS control schemes in Chapter 3–5 and experimental results validate the effectiveness of the proposed balancing principles.

For all the proposed control schemes in this dissertation, detailed operation principles, derivation process of key equations, comparative analyses, implementation method with digital controller and experimental verifications with TLB PFC prototype are provided.

Digital-Based Zero-Current Switching (ZCS) Control Schemes for Three-Level Boost Power-Factor Correction (PFC) Converter

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GENERAL AUDIENCE ABSTRACT

Electronic-based devices and loads have been essential parts of modern society founded on rapid advancements of information technologies. Along with the progress, power supplying and charging of electronic products become routinized in daily lives, but still remain critical requisites for reliable operations. In many power-electronics-based supplying systems, ac-dc power-factor correction (PFC) circuits are generally located at front-end to feed back-end loads from universal ac-line sources. Since PFC stages have a key role in regulating ac-side current quality and dc-side voltage control, the importance of PFC performances cannot be emphasized enough from entire system point of view. Thus, advanced control schemes for PFC converters have been developed in quantity to achieve efficient operations and competent power qualities such as high power factor, low harmonic distortions and low electromagnetic interferences (EMI) noises.

In this dissertation, a sort of PFC topologies named three-level boost (TLB) converter is chosen for target topology. Based on inherent three-level waveform capability of the topology, multiple zero-current switching (ZCS) control schemes are proposed. Compared to many conventional two-level PFC topologies, TLB PFC can provide additional degree-of-freedom to current modulation. The increased control flexibility can realize improvements of various waveform qualities including peak current stress, switching frequency range, harmonics and EMI amplitude. From the experimental results in this dissertation, improvements of waveform

qualities in TLB PFC with the proposed schemes are verified with comparison to two-level current control schemes; in terms of efficiency, the results show that TLB PFC with the proposed schemes can have similar converter efficiency with conventional two-level boost converter in spite of increased component counts in the topology. Further, the proposed three-level control schemes can be utilized in adjustable forms to accomplish different control objectives depending on system characteristics and applications.

In each chapter of this dissertation, a novel control scheme is proposed and explained with details of operation principle, key equations and digital implementation method. All the effectiveness of proposals and analyses are validated by a proper set of experimental results with a TLB PFC prototype.

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Table of Contents

List of Figures

List of Tables

Chapter 1.
Introduction

In this chapter, background, overview of current conduction modes and topologies in boosting power-factor correction systems, research motivations and objectives are presented. Outline of the dissertation is also included with brief summaries of the following chapters.

1.1 Background

In the recent decade, there has been an explosive increase of end-use commercial electronics. Devices such as computers, displays, smart phones and LED lightings, now, get settled in modern life as basic essentials. As shown in Fig. 1-1, in order to properly utilize those electronic devices, supplying and charging with universal ac-voltage (i.e. 90–264 V_{rms}) also become daily routines. Representative global standards of universal ac-input voltages are 110 V_{rms} and 220 V_{rms}. Power supplies for electronic devices convert ac input voltage and current to certain dc specifications required by end-use electronics.

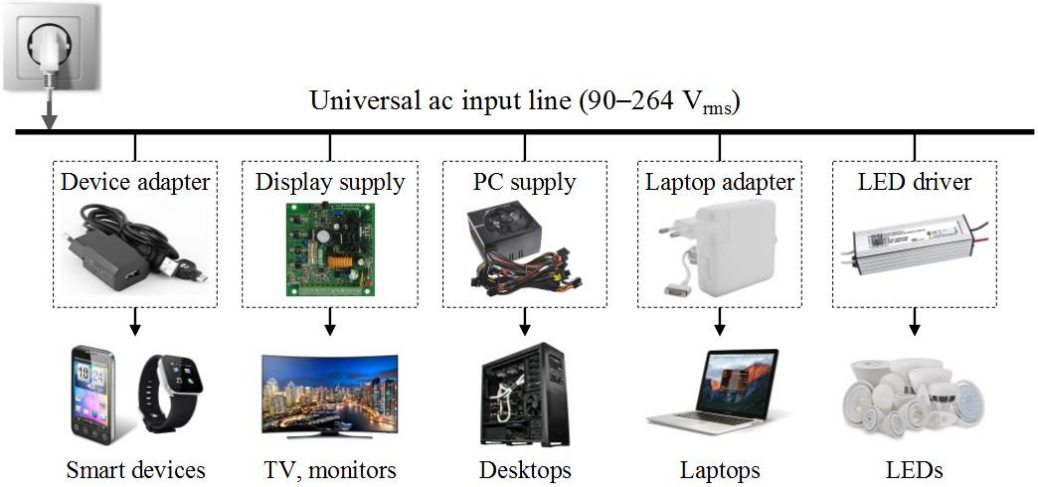


Fig. 1-1. Examples of end-use electronics with universal ac input.

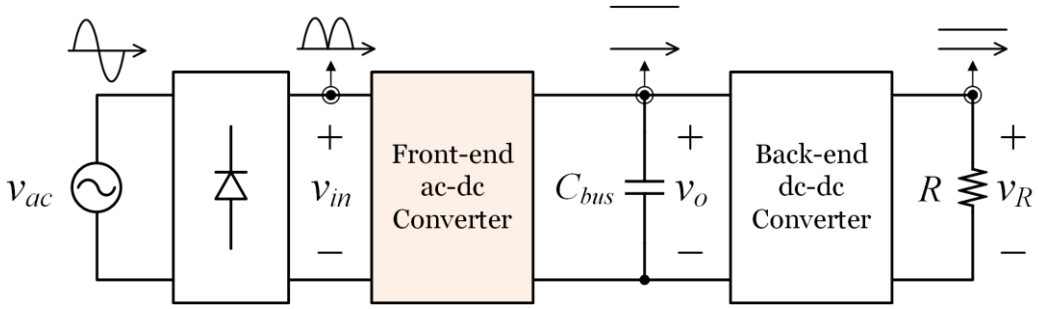


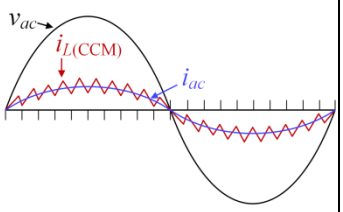
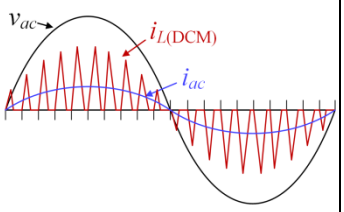
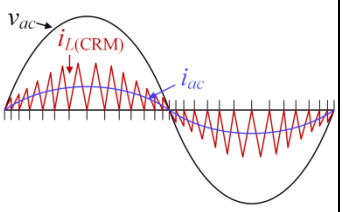
Fig. 1-2. Configuration of two-stage ac-dc power conversion.

Since ratings of dc voltage and power level are all different by application, general configurations of electronic power supplies follow the two-stage structure in Fig. 1-2. The front-end ac-dc converters with universal voltage rating should be able to handle wide-range of input rms voltage, producing boosted dc-bus voltage at desired level. Then, back-end dc-dc converters step down the bus voltage to certain values for point-of-load voltages. The two stages in Fig. 1-2 are actively operated for regulation purposes; it is generally accepted that using active front-end ac-dc converters can bring benefits of high input power factor (PF), low total harmonic distortion (THD) of input current and controlled dc-bus voltage, compared to passive diode-bridge rectifier [1]. Thus, it can be noted that overall system performances are highly influenced by the capability of front-end ac-dc converter.

1.2 Current Modes of Power-Factor Correction (PFC) Converters

Active front-end ac-dc converters in Fig. 1-2 are commonly called as power-factor correction (PFC) converters because input current can be controlled and effectively in phase with input ac voltage by the stage, achieving high PF near unity [2]–[3]. Accordingly, input current control is main part of PFC control and can be classified into three by inductor current waveforms, which are continuous conduction mode (CCM), discontinuous conduction mode

Table 1-1. Summary of current conduction modes.

Mode	CCM	DCM	CRM
Waveform			
Operating frequency	Fixed frequency	Fixed frequency	Variable frequency
Reverse recovery	Yes	No	No
Cost	High	Low	Low
Current ripple	Low	Highest	High
Application	High power (up to kW)	Low power (< 300 W)	Low power (< 300 W)
Voltage switching	Hard switching	Partial soft switching (ZVS on if $\|v_{ac}\|<v_o/2$)	Partial soft switching (ZVS on if $\|v_{ac}\|<v_o/2$)
Current switching	Hard switching	Soft switching (ZCS on)	Soft switching (ZCS on)

(DCM) and critical conduction mode (CRM) [4]–[5]. Characteristics of the three current modes are summarized in Table 1-1 with typical input waveforms. As can be seen, CCM control has continuous inductor current waveforms cycle by cycle, while DCM and CRM control methods show zero-current beginning of each switching cycle. Due to the fundamentals, DCM and CRM controls have a lot in common to each other than CCM. Since each switching cycle in both DCM and CRM begins with zero-current switching (ZCS) turn on, there is no reverse recovery issue and low-cost diode can be used for cost-competitiveness [6]–[9]. However, both modes have high inductor current ripples and corresponding

differential-mode (DM) electromagnetic interference (EMI), which practically limits their usages to low power applications up to 300 W. Since majority of modern electronic devices mentioned in the previous section mostly belong to low-power applications and low-cost power supplies are preferred for them, front-end PFC converters equipped with ZCS methods (DCM and CRM) have been exploited in those systems.

1.3 Boosting PFC Converter Topologies

Universal-line front-end PFC converters should be able to handle wide-range input rms voltage and it is good for back-end dc-dc converters if output voltages of PFC converters can be standardized even under wide universal inputs. Thus, many boost-family topologies which can step up universal input to higher level are widely employed in PFC stage. Since boosted PFC output voltage should be higher than peak of maximum universal input voltage (i.e. 373 V: peak of 264 V_{rms}), a voltage in 380–400 V range is usually chosen for PFC outputs.

With the general specifications, three well-known boost-derived PFC topologies have been researched in great quantity and implemented in many real-life applications [10]–[40]. The titles of topologies are conventional boost PFC converter (Fig. 1-3), bridgeless dual-boost PFC converter (Fig. 1-4) and bridgeless totem-pole boost PFC converter (Fig. 1-5). The detailed circuit diagrams can be found and compared from the following figures.

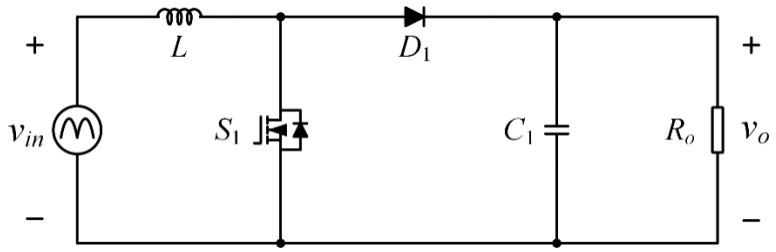


Fig. 1-3. Circuit diagram of boost PFC converter.

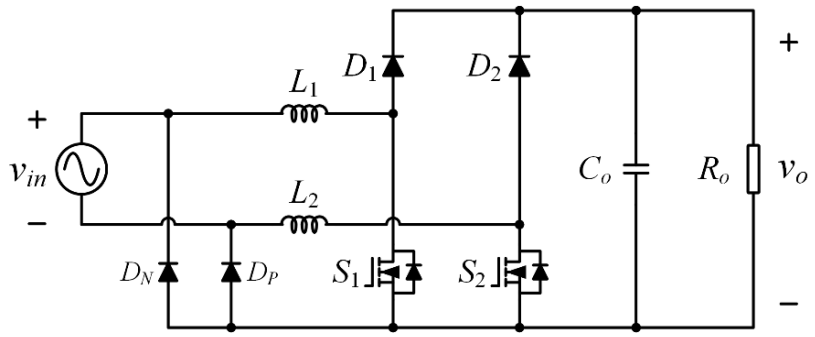


Fig. 1-4. Circuit diagram of dual-boost PFC converter.

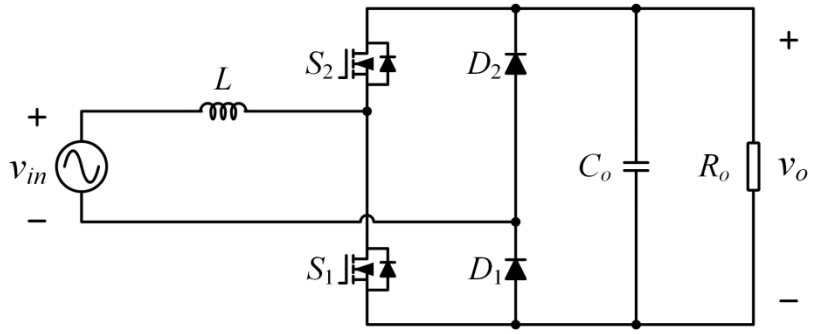
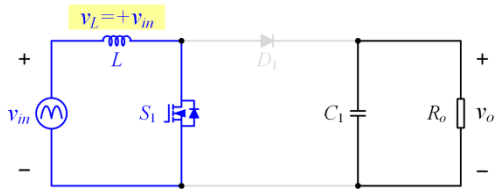
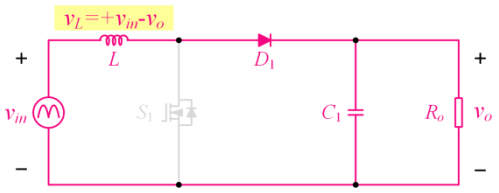
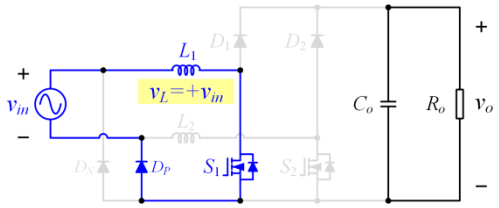
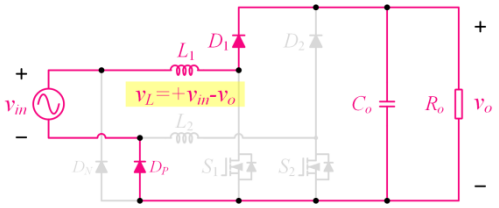
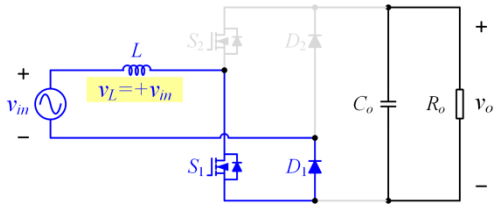
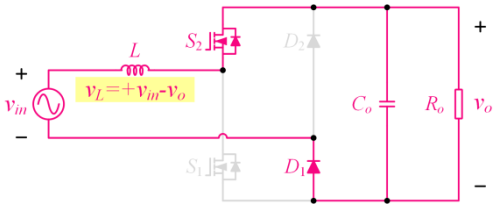
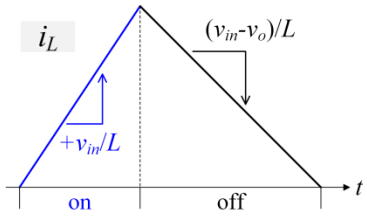
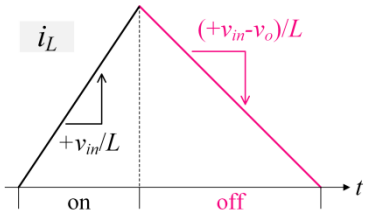


Fig. 1-5. Circuit diagram of totem-pole boost PFC converter.

Although configurations of the three PFC topologies are all different, their operation principles are mostly identical. Conventional boost converter in Fig. 1-3 faces rectified ac input voltage and synthesizes inductor voltage and current by manipulating main switch S_1. When turning on S_1, input voltage v_{in} is applied across the inductor L and inductor current i_L increases with a slope of v_{in}/L. If S_1 turns off and D_1 gets conducted, the inductor voltage becomes $(v_{in}-v_o)$ which is negative so that inductor current decreases with a slope of $(v_{in}-v_o)/L$. By using the principles, DCM and CRM can be easily achieved in boost PFC converter. The other two bridgeless PFC converters can control inductor current in the same way except the fact that additional diodes provide input current path instead of diode-bridge in boost PFC. Detailed circuit operations by each topology's switching status are shown in Table 1-2.

Table 1-2. Circuit operations by main switch status.

	Main switch: on	Main switch: off
Boost PFC		
Dual-boost PFC		
Totem-pole boost PFC		
Inductor current waveform		

Synthesization principles of inductor current in the three boosting PFC topologies are equal, which can be noted from identical inductor-current slopes and shapes in Table 1-2 under same inductance and voltage conditions. Thus, the topologies can achieve both DCM and CRM operations in Table 1-1 by adjusting the on-time duration of main switch *S*, considering the inductance, input/out voltages and power conditions. There still exist differences of conducted device counts in current path and corresponding conduction losses by topology, but input current quality such as peak, PF and THD will remain equal under same conditions.

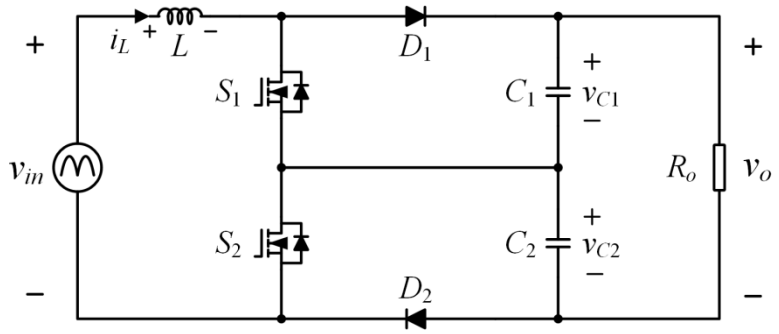


Fig. 1-6. Circuit diagram of three-level boost PFC converter.

As one sort of boost-derived family, three-level boost (TLB) PFC converter in Fig. 1-6 was also developed and implemented in wide-range applications [41]–[58]. The topology consists of two boost cells and each cell includes switch *S*, diode *D* and output capacitor *C*. Although the component counts in TLB PFC is twice more than those in conventional boost PFC, main advantage of using TLB topology is that voltage stress of all components becomes $v_o/2$ which is half of component voltage stresses in the other boost-family topologies. Due to the halved voltage rating, TLB PFC has been more implemented in high voltage applications (e.g. high-power renewable generation, medium-voltage solid-state transformer, dc fast charging station [50]–[58]) than the other boosting PFC topologies. Since those kinds of applications need high power supplies at least several kW level, previous literatures regarding TLB PFC mostly focused CCM control rather than the ZCS methods.

On the other hand, for universal-line low-power applications, the potentials of TLB topology have rarely been explored. It is mainly due to underlying judgments that there's no reason to use the topology because increments of component counts, cost and losses make it unpractical than the other topologies [59]. However, in pragmatic aspects, TLB PFC can be also a good option for low-cost universal-line applications. In the market, lower-voltage-rated

components with similar parameters involve lower expenses than higher-voltage-rated ones. Table 1-3 refers cost evaluations of boost PFC and TLB PFC with similar circuit parameters.

Table 1-3. Cost comparison of major components (http://www.digikey.com, as of June 3rd, 2020).

	Boost PFC	Three-level Boost PFC
Switch	FCB15N50 (On semiconductor) 500 V, 15 A, 380 mΩ, TO-263AB {∗Unit price: $2.69}	FQD16N25 (On semiconductor) 250 V, 16 A, 270 mΩ, TO-263AB {∗Unit price: $0.93}
Diode	FES16HT-E3/45 (Vishay) 500 V, 16 A, 1.5 V (V_F), TO-220AC {∗Unit price: $1.30}	VS-15ETH03-M3 (Vishay) 300 V, 15 A, 1.25 V (V_F), TO-220AC {∗Unit price: $1.00}
Capacitor	450MXG470MEFCSN35X40 (Rubycon) Alum. E-cap, 450 V, 470 μF (20%) {∗Unit price: $8.01}	250MXG470MEFCSN25X30 (Rubycon) Alum. E-cap, 250 V, 470 μF (20%) {∗Unit price: $3.55}
Total price	$ 12.00 (1 switch, 1 diode, 1 capacitor)	$ 10.96 (2 switches, 2 diodes, 2 capacitors)
Note	Miscellaneous circuit parts (e.g. gate-drivers) are not included in this comparison.	

The components are selected based on typical universal-line specifications with 90–264 V_{rms} input, 400-V output and 300-W full-load conditions. Major components in conventional boost, then, experience maximum 400-V voltage stresses while those in TLB PFC face 200-V voltage stresses. The selections in Table 1-3 are based on the stress levels and voltage margins. Although low-cost diodes with 300-V and 500-V ratings don't have much cost differences, switches and bus capacitors show considerable differences depending on voltage ratings. As a result, the net price of major components in TLB topology could be less than that of boost PFC. Since miscellaneous circuit parts such as gate-drivers are not fully considered in the

evaluation, it cannot be simply concluded by TLB PFC's superiority. However, it can be noted from the Table 1-3 that TLB PFC has similar cost-competitiveness with the other boosting PFC topologies for universal-line lower-power applications.

1.4 Motivations and Objectives

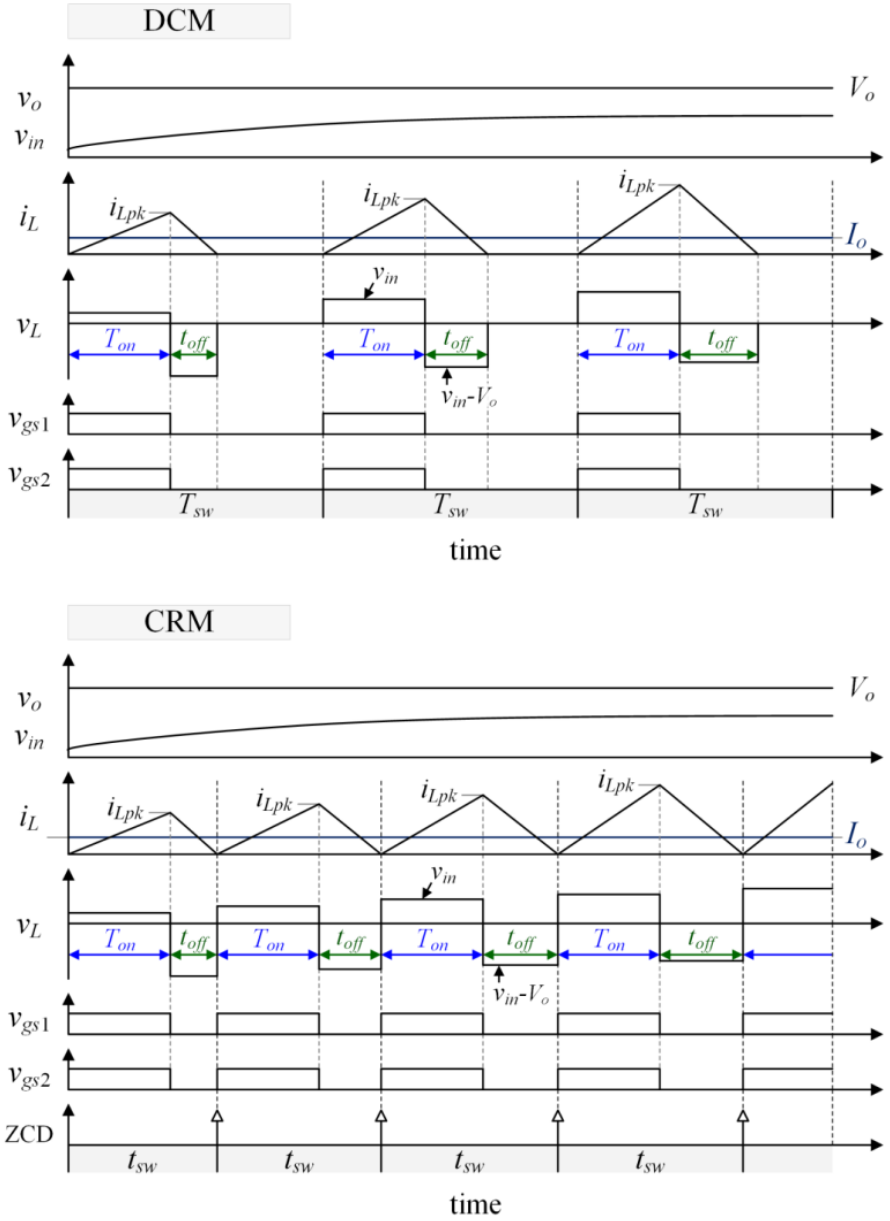


Fig. 1-7. Key waveforms of TLB PFC with conventional two-level ZCS methods.

In spite of acceptable prices, TLB PFC converter with conventional ZCS (i.e. DCM and CRM) control methods is not worthy of implementation. In order to operate TLB PFC with the two-level triangular current shown in Table 1-2, the two switches S_1 and S_2 in TLB PFC must turn on and off together and the diodes are conducted at the same time, as Fig. 1-7 [60]. With the schemes, TLB PFC will show equal input current qualities as the two-level boosting PFC topologies, but the additional devices S_2 and D_2 will cause more conduction losses and efficiency drop. These meritless features in terms of efficiency and waveform quality have made TLB topology lose its place in universal-line low-power applications. Moreover, inherent topological issue of unbalanced voltages between v_{C1} and v_{C2} is another barrier that doesn't need to be worried at all in the other boost PFC converters [60].

Due to the reasons, there have few research attempts that utilize multi-level waveform capability of TLB PFC for DCM and CRM operations. It means that there exists potential of three-level capacity to improve both efficiency and waveform quality for universal low-power systems. In general, multilevel topologies and modulation schemes can bring enhanced waveform qualities (e.g. PF, THD, EMI) at ac-side, which was proven by many researches on ac-dc PFC rectifiers and dc-ac inverters [61]–[65].

Based on these backgrounds, this dissertation aims to achieve the following objectives. First, a methodology to fully utilize the three-level capability is to be devised based on operation principles of TLB PFC converter. Second, several DCM/CRM control methods are to be proposed on top of the methodology to improve performance factors such as losses, component stresses and DM EMI. Lastly, output voltage balancing schemes that can be easily applied to the proposed methods are to be introduced for resolving the inherent unbalancing issue of TLB topology.

1.5 Outline of Dissertation

The remainder of this dissertation consists of six chapters and the contents of each chapter are briefly summarized below.

In Chapter 2, operation principles and characteristics of TLB topology are discussed and a basic methodology of three-level current modulation is devised based on the fundamentals.

Chapters 3–5 are dedicated to propose multiple control schemes for DCM and CRM operations using the basic three-level modulation. In Chapter 3, a novel three-level CRM control scheme is proposed. With the scheme, TLB PFC gets quadrangular inductor current waveforms throughout ac line cycles. Expected effects are reduction of variable switching frequency, peak inductor current, switching losses, component stresses and THD value. Resultantly, efficiency of TLB CRM PFC can be comparable to that of boost PFC and even higher at light load conditions. Details of the effects are to be verified by analysis and experimental results. In Chapter 4, a three-level DCM control scheme is proposed for TLB PFC. The purpose of control is to reduce high peak current of DCM operation close to CRM level by adjustable three-level switching duration. Under time-varying input voltage and power conditions, the proposed method can provide proper switching mechanism to synthesize quadrangular inductor currents which fit to the fixed switching period similar to CRM operation. With the scheme, TLB PFC can be rewarded by hybrid benefits of fixed frequency (DCM) and lower peak current (CRM) at the same time, achieving efficiency improvements. In Chapter 5, a spread-spectrum frequency modulation (SSFM) scheme is proposed for DCM TLB PFC. Due to the fixed frequency of DCM control, the magnitudes of DM EMI are generally much higher than CRM control so that high-volume input filter is required. In order to mitigate dense EMI energy, intentional frequency distribution is

implemented and it can significantly reduce the peak amplitude of DM EMI. Then, the adjustable three-level modulation scheme in Chapter 4 can be applied on top of the proposed SSFM to get further reduction of DM EMI noises. The spread-spectrum frequency range can be also selected in downward direction to increase converter efficiency. The effects of SSFM and three-level modulation are proved by experimental results with EMI measurements.

In Chapter 6, two approaches of output-voltage balancing schemes are introduced. One approach is to set one switch as master balancing device and the other approach is to toggle two switches by turns for balancing output voltages under asymmetric operations. Both approaches work well with the proposed DCM and CRM operations in Chapter 3–5. Key equations and implementation method for balancing schemes are derived in this chapter and the effectiveness is validated by experimental results.

In Chapter 7, conclusion of this dissertation and direction for future work are organized.

1.6 List of Publications

Parts of this dissertation have been published already or being in the publication process with peer-refereed journals. The list of publications is summarized in the next page.

Table 1-4. List of publications (as of Aug. 12th, 2020).

Chapter	Publication
Ch. 3	**M. Lee**, J.-W. Kim, and J.-S. Lai, "Digital-Based Critical Conduction Mode Control for Three-Level Boost PFC Converter," *IEEE Trans. on Power Electronics*, vol. 35, no. 7, July 2020. (Published)
Ch. 4	**M. Lee**, and J.-S. Lai, "Fixed-Frequency Hybrid Conduction Mode Control for Three-Level Boost PFC Converter," *IEEE Trans. on Power Electronics*. (Under Revision)
Ch. 5	**M. Lee**, and J.-S. Lai, "Spread-Spectrum Frequency Modulation With Adaptive Three-Level Current Scheme To Improve EMI and Efficiency of Three-Level Boost DCM PFC," *IEEE Trans. on Power Electronics*. (In Press, doi: 10.1109/TPEL.2020.3016238)
Ch. 6	**M. Lee**, and J.-S. Lai, "Unified Voltage Balancing Feedforward for Three-Level Boost PFC Converter in Discontinuous and Critical Conduction Modes," *IEEE Trans. on Circuits and Systems–II: Express Briefs*. (In Press, doi: 10.1109/TCSII.2020.3003113)

Chapter 2.
Analysis of Three-Level Boost PFC Converter

In this chapter, characteristics of TLB PFC converter are analyzed with operation principles. A distinctive degree-of-freedom in current-slope shaping is the key concept of TLB PFC which cannot be found from the other boosting PFC topologies. Based on the distinctive feature, a basic three-level modulation with quadrangular current waveform is introduced in this chapter, which consolidates the theoretical ground for multiple ZCS control schemes proposed in the following chapters. Expected effects of the proposed modulation are also described with operational benefits and issues.

2.1 Operation Principles

As illustrated in Fig. 1-6, TLB PFC topology consists of two basic boost cells; each cell contains active switch *S*, complimentary diode *D*, and output capacitor *C*. Boost inductor *L* is located at the input current path. Inductor voltage v_L can be synthesized at different levels and inductor current i_L can flow into both cells depending on the on/off status of S_1 and S_2 which are summarized in Table 2-1. The diodes D_1 and D_2 are conducted in complimentary manner

Table 2-1. Switching States of TLB PFC by S_1 and S_2.

State	S_1	S_2	v_L
1	On	On	v_{in}
2	On	Off	v_{in}-v_o/2
3	Off	Off	v_{in}-v_o/2
4	Off	Off	v_{in}-v_o

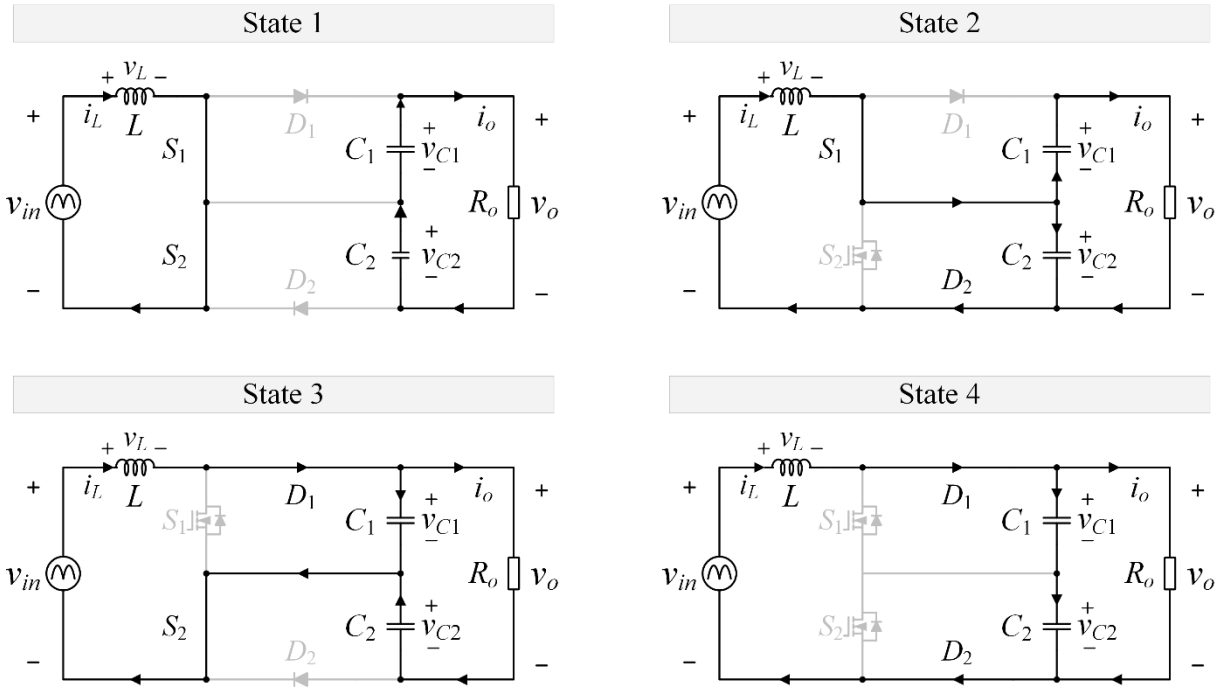


Fig. 2-1. Circuit operation by switching state.

in turn-off cases of S_1 and S_2, respectively. Thus, it can be noted that operations of TLB PFC are totally determined by switching status of the two switches.

Along with the Table 2-1, circuit operations by the matched switching states are demonstrated in Fig. 2-1. In State 1, both switches are conducted so that positive input voltage v_{in} is applied across the inductor and build up energy in it. During the state, output load R_o is supplied by the two output capacitors. In State 2 and State 3, only one of the two switches turns on and a diode in the other boost cell goes conducted; the voltage across inductor becomes (v_{in}-v_o/2). As can be seen from current-flow arrows, the inductor current charges one output capacitor with (i_L-i_o) current and the other capacitor is to be discharged by load current i_o. Lastly, in State 4, all the switches are off and the complimentary diodes are conducted. The inductor voltage, here, is negative-polarity (v_{in}-v_o) so that built-up inductor energy is released to load side and inductor current decreases. Regardless of input, output and

power conditions, TLB PFC operations throughout line cycles can be categorized by the aforementioned four switching states.

2.2 Degree-of-Freedom in Current-Slope Shaping

As a PFC regulator, TLB converter should be able to operate with time-varying ac input voltage in universal specifications. In Fig. 2-2, input voltage variation in half of line-cycle T_1 is drawn as an example. As shown in the figure, the operation of TLB PFC can be divided into two modes by input voltage level.

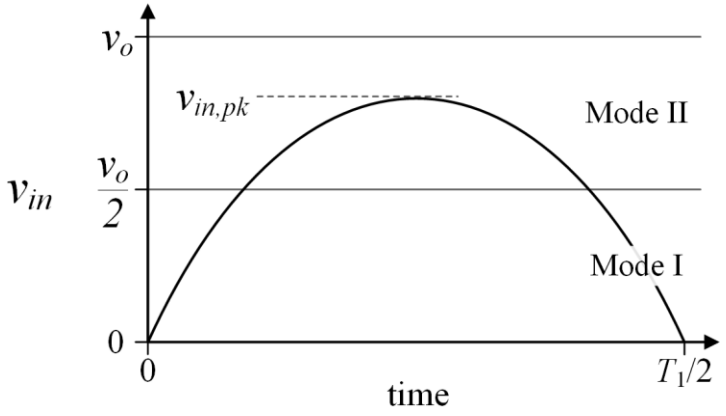


Fig. 2-2. Operation modes by input voltage level.

The boundary condition of voltage modes is $v_{in}=v_o/2$. Mode I happens when the magnitude of input voltage v_{in} is between 0 and $v_o/2$ while Mode II is defined when v_{in} is between $v_o/2$ and v_o. Different from the two-level boost-derived PFCs, TLB topology in Fig. 1-6 has the two output capacitors of which voltages are controlled to $v_o/2$. Thus, depending on the switching status in Table 2-1, the switch-side electrical node of inductor can be connected to three potential levels which are 0, $v_o/2$ and v_o. Since input voltage is always between 0 and v_o, the two voltage modes I and II come from comparison with $v_o/2$.

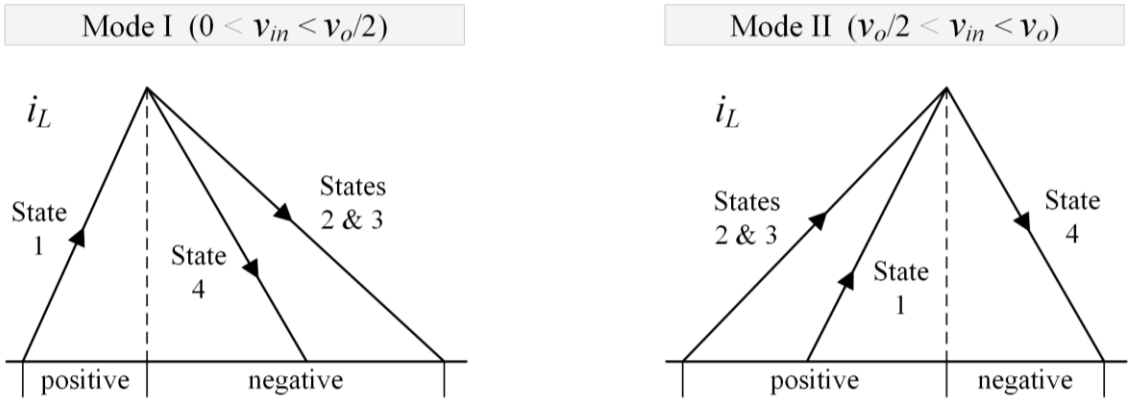


Fig. 2-3. Degree-of-freedom in current-slope shaping by input voltage mode.

From Table 2-1, it can be noted that there are three equivalent switching states in TLB PFC (State 1, State 2 & 3, and State 4). The three switching states form different circuit operations as Fig. 2-1 and their effects on inductor voltage and current vary depending on the input voltage level.

First, when both the two switches are on in Mode I (State 1), input voltage is fully loaded across the inductor and inductor current increases with a positive slope v_{in}/L. If only a single switch turns on between S_1 and S_2 (State 2 & 3), the right-side electrical node of inductor is connected to the in-between point of two output capacitors so that inductor voltage will be $(v_{in}-v_o/2)$ which is negative in Mode I; the inductor current decreases with a negative slope $(v_{in}-v_o/2)/L$ in those switching states. Lastly, when both the switches are off together (State 4), voltage across the inductor becomes negative $(v_{in}-v_o)$, causing a descending inductor current with a negative slope $(v_{in}-v_o)/L$. The negative slope in State 4 is steeper than that in State 2 & 3. In brief, there exist three current-slope shaping options in Mode I including one positive-slope option and two negative-slope options, as shown in Fig. 2-3.

For Mode II, TLB PFC has identical three switching states to Mode I. The operation principles of State 1 and State 4 are exactly same with those in Mode I. However, for State 2

& 3, the polarity of voltage across the inductor (v_{in}-v_o/2) becomes positive in Mode II. It means that the inductor current in State 2 & 3 of Mode II will have a positive current-slope (v_{in}-v_o/2)/L. As shown in Fig. 2-3, the composition of inductor current-slopes in Mode II is differentiated from that of Mode I. Now, there are three current-slope options including two positive slopes and one negative slope.

Compared to the two-level boost-derived PFC topologies (conventional boost, dual-boost, and totem-pole boost) introduced in Chapter 1, TLB PFC topology has additional degree-of-freedom in inductor current-slope shaping, which can give options to synthesize inductor current in multilevel waveforms for both Modes I and Mode II. By utilizing the inherent three-level characteristics in modulation schemes, there arise chances to improve performance factors of the two ZCS current control methods.

2.3 Basic Three-Level Current Modulation

Based on the additional degree-of-freedom in current-slope forming, a basic three-level current modulation scheme is proposed in this section [59]. The modulation scheme facilitates asymmetric gate signals for two switches S_1 and S_2 in TLB PFC, fully applying the inherent three-level capability to the DCM and CRM operations. In the following chapters, this basic current modulation will be implemented to those ZCS operations with extended techniques.

Key waveforms of the proposed three-level modulation scheme working with DCM and CRM operations are described in Fig. 2-4 and Fig. 2-5, respectively. A new feature in the proposed method is that one switching period of DCM or CRM operations consists of three switching states which are common on-time duration T_{on}, single-switch on-time duration T_{α}, and common off-time duration T_{off}; forming three-level inductor currents.

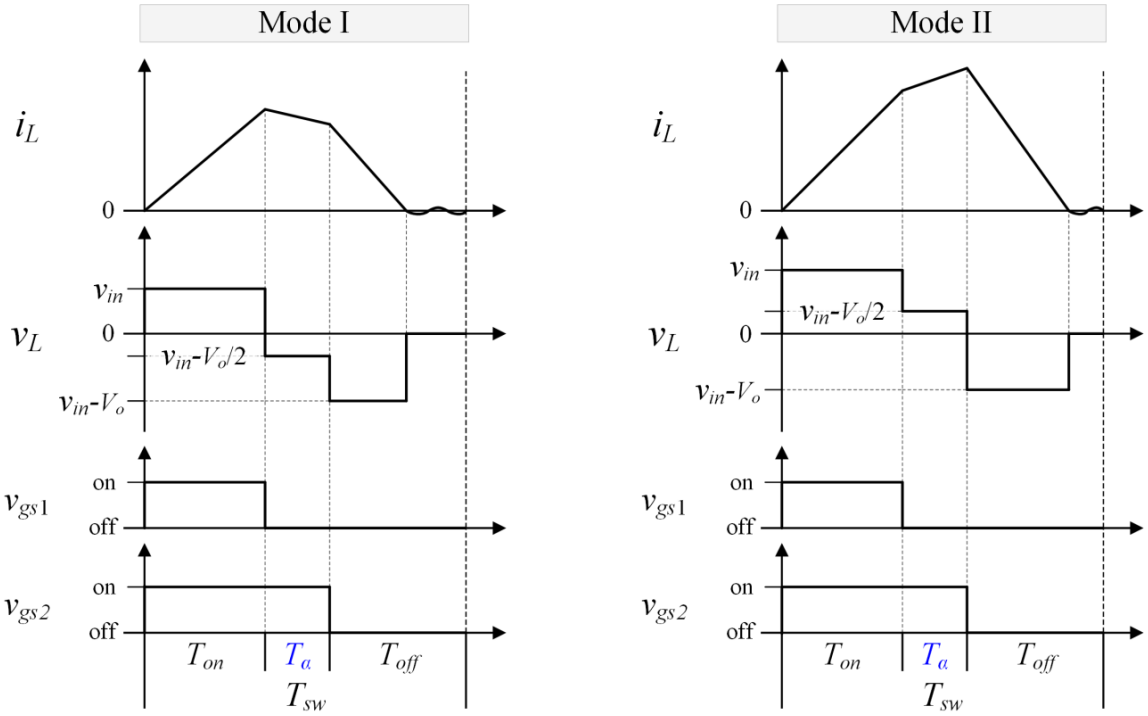


Fig. 2-4. Key waveforms of proposed three-level modulation scheme in DCM operation.

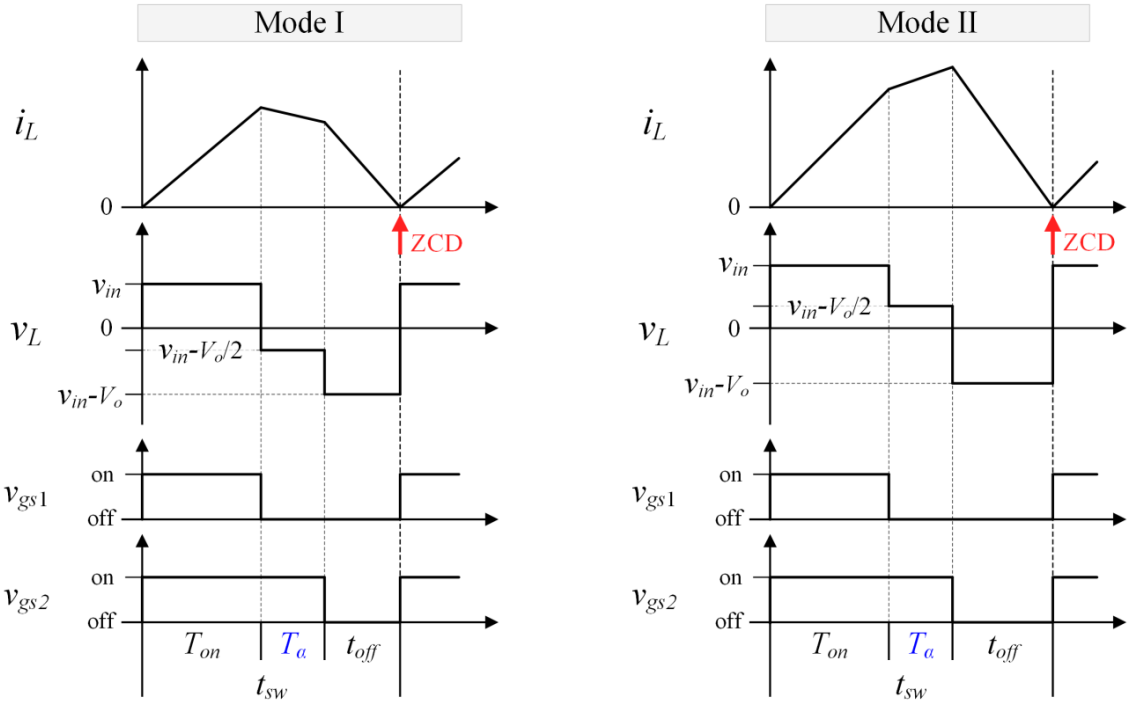


Fig. 2-5. Key waveforms of proposed three-level modulation scheme in CRM operation.

For better explanations of control schemes, several assumptions are made first as follows.

1) Any fixed, constant and controlled parameters will be written in upper-case letters and time-varying variables will be expressed in lower-case letters for the rest of this dissertation.

2) Total output voltage is assumed to be controlled to V_o by a properly designed voltage control-loop. In general, the voltage compensator has slow control dynamics with 1–5 Hz control bandwidth. The common on-time T_{on} is resulted from the slow-dynamic compensator and it remains almost constant during ac line cycles [61].

For DCM operation with the proposed modulation scheme, switching frequency F_{sw} and switching period T_{sw} are fixed as shown in Fig. 2-4. Both switches S_1 and S_2 turn on concurrently at the beginning of each switching cycle. Within the switching period, the single-switch on-time T_α brings an additional current-slope $(v_{in}\text{-}V_o/2)/L$ in the middle and quadrangular current waveforms. Depending on input voltage modes, the polarity of T_α periods can be either positive or negative.

On the other hand, CRM operation with the three-level modulation scheme is based on inherently variable switching frequency f_{sw}. It is mainly due to the fact that each switching period t_{sw} begins at the zero-crossing detection (ZCD) moment of inductor current [62]–[63]. Regardless of the variable switching operations, the three-level current modulation scheme can harmonized with the ZCD techniques and the single-switch on-time T_α will also bring operational benefits by quadrangular inductor current waveforms.

2.4 Expected Effects of Three-Level Current Modulation

As mentioned, TLB PFC with DCM and CRM operations haven't been actively employed in universal-line low-power applications. The reason is that it suffers from more conduction

losses while input current quality remains equal, compared to the other two-level boosting PFC converters. However, if the devised three-level modulation scheme works with TLB PFC, there arises chance to improve performance factors by using multilevel characteristics.

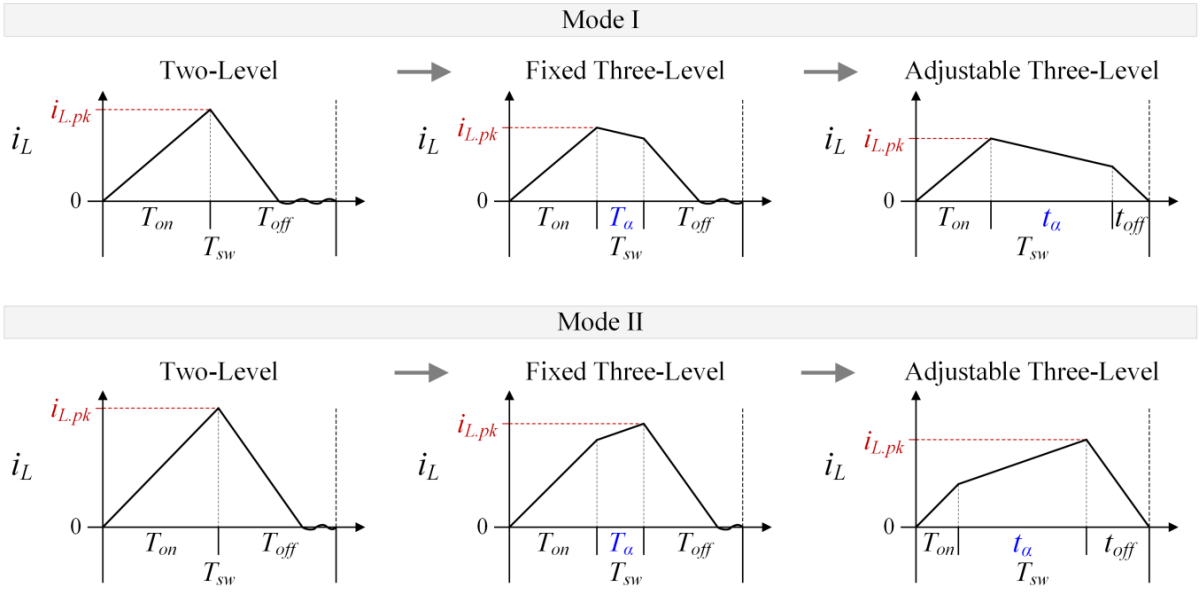


Fig. 2-6. DCM current waveforms by modulation scheme.

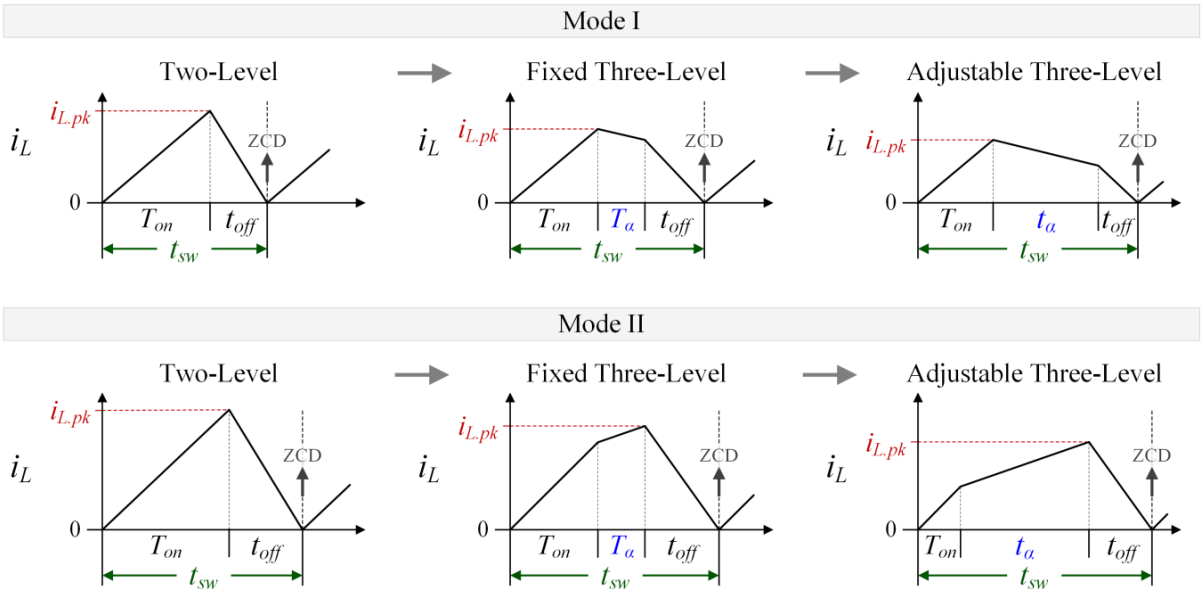


Fig. 2-7. CRM current waveforms by modulation scheme.

In Fig 2-6 and Fig. 2-7, possible techniques using the modulation scheme and expected effects on current waveforms are demonstrated. For all conduction modes and input voltage modes, the basic three-level current modulation can be implemented in two ways.

First, fixed ratio between T_{on} and T_{α} can be used. Since T_{on} remains constant during line cycles (50–60 Hz) from slow-dynamic voltage compensator, T_{α} can stay unchanged by maintaining the ratio fixed. Under the same input/output and power conditions, average inductor current in a switching cycle should be equal irrespective of current waveform. Thus, as shown in Fig. 2-6 and Fig. 2-7, the non-zero current duration by the fixed three-level modulation become longer than that of conventional two-level modulation; consequently the peak inductor current in a switching cycle can be reduced under same input current condition. The peak reduction effects will be more remarkable especially in DCM since the peak current of DCM control is the highest among PFC controls as mentioned in Table 1-1. The chain effects of reduced peak current are reductions of device current stresses, turn-off current and switching losses. The fixed-ratio control can be also applied to CRM control. As can be seen from Fig. 2-7, the variable switching period t_{sw} of CRM control becomes longer and the peak inductor current gets lowered. Accordingly, switching losses can be decreased by reduced turn-off current and switching frequency. At light load condition, CRM control generally suffers from very high switching frequency up to several hundred kHz range. Thus, the three-level modulation is expected to be helpful to improve the light-load efficiency.

Second, the single-switch on-time duration can be extended in adjustable form t_{α} for each switching cycle. For DCM in Fig. 2-6, the adjustable approach can make inductor waveform close to CRM operation, achieving the lowest peak current under given conditions. For CRM in Fig. 2-7, the extended three-level technique can be utilized to achieve desired switching

frequencies and further reduced peak current. For both modes, the adjustable t_α can bring benefits by changing parameters such as peak current, switching period and EMI noises.

However, as can be seen from Fig. 2-6 and 2-7, the proposed three-level current modulation scheme is based on asymmetrical operations of main switches in the two boost cells. This principle can cause severe unbalancing between the two output-capacitor voltages without any voltage balancing schemes. Further, the unbalancing issue in universal-line TLB PFC is critical because low-cost electrolytic capacitors in the market are widely used for the output capacitors in the low-power applications. Typical parameter tolerances are ±20% as highlighted in Fig. 2-8. Experimental waveforms of TLB PFC by two-level DCM operations

Image	Digi-Key Part Number	Manufacturer Part Number	Manufacturer	Description	Quantity Available	Unit Price USD	Minimum Quantity	Packaging	Series	Part Status	Capacitance	Tolerance
	493-7246-ND	LLG2W471MELB40	Nichicon	CAP ALUM 470UF 20% 450V SNAP	4,053 - Immediate	$10.06000	1	Bulk	LLG	Active	470µF	±20%
	493-7247-ND	LLG2W471MELC35	Nichicon	CAP ALUM 470UF 20% 450V SNAP	4,902 - Immediate	$10.13000	1	Bulk	LLG	Active	470µF	±20%
	493-2869-ND	LGU2W471MELC	Nichicon	CAP ALUM 470UF 20% 450V SNAP	2,158 - Immediate	$10.50000	1	Bulk	LGU	Active	470µF	±20%
	565-3475-ND	EKMS451VSN471MA40S	United Chemi-Con	CAP ALUM 470UF 20% 450V SNAP	1,687 - Immediate	$10.52000	1	Bulk	KMS	Active	470µF	±20%
	493-7069-ND	LGG2E471MELA30	Nichicon	CAP ALUM 470UF 20% 250V SNAP	17,326 - Immediate	$3.78000	1	Bulk	LGG	Active	470µF	±20%
	565-2797-ND	ESMQ451VSN471MR45S	United Chemi-Con	CAP ALUM 470UF 20% 450V SNAP	7,494 - Immediate	$5.78000	1	Bulk	SMQ	Active	470µF	±20%
	565-3031-ND	EKMQ451VSN471MA45S	United Chemi-Con	CAP ALUM 470UF 20% 450V SNAP	5,103 - Immediate	$6.55000	1	Bulk	KMQ	Active	470µF	±20%
	493-2619-ND	LLS2W471MELC	Nichicon	CAP ALUM 470UF 20% 450V SNAP	4,957 - Immediate	$6.72000	1	Bulk	LLS	Active	470µF	±20%
	338-2733-ND	381LX471M450A052	Cornell Dubilier Electronics (CDE)	CAP ALUM 470UF 20% 450V SNAP	347 - Immediate	$8.19000	1	Tray	381LX	Active	470µF	±20%
	1189-1975-ND	450HXG470MEFCSN35X45	Rubycon	CAP ALUM 470UF 20% 450V SNAP	1,391 - Immediate	$8.55000	1	Bulk	HXG	Active	470µF	±20%

Fig. 2-8. Electrolytic capacitors for dc-bus purpose (http://www.digikey.com, as of June 5th, 2020).

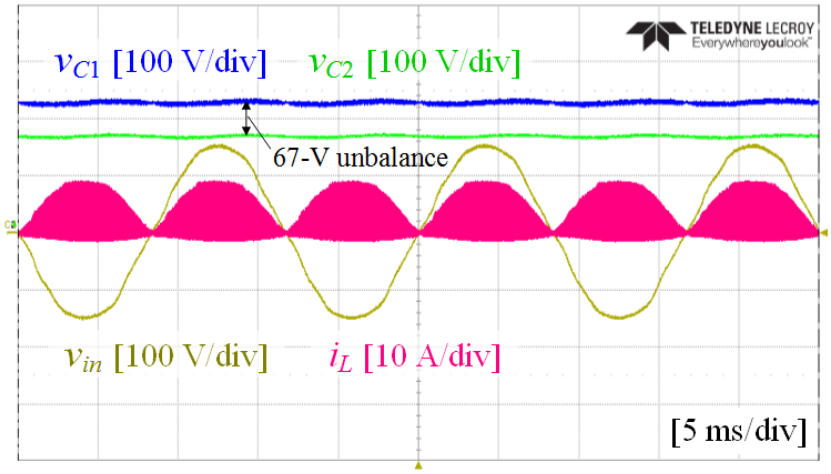


Fig. 2-9. Experimental waveforms of conventional two-level DCM.

are shown in Fig. 2-9. Even with the symmetric operations of S_1 and S_2, the output capacitor voltages become unbalanced by 67 V mainly due to parameter differences (ECET2WP471, 470 μF, ±20%, Panasonic), and corresponding disparities of consumptions and thermal unbalances in the two boost cells. That means the unbalanced voltages will become worse if modulations of two boost cells go asymmetric on top of the parameter tolerances.

In conclusion, it is expected that TLB PFC can be rewarded with reductions of peak current, harmonics and switching losses, and improved efficiency by implementing the proposed three-level current modulation scheme. However, asymmetry in the modulation scheme can cause severe voltage unbalance at the output capacitors and there should be additional voltage balancing schemes to compensate the disparity. Detailed implementation and extension of the three-level modulation scheme in DCM and CRM controls, mathematical analysis of operation effects and key equations, voltage balancing methods and experimental verifications are provided in the following chapters.

Chapter 3.
Digital-Based Three-Level CRM Control Scheme

In this chapter, a novel three-level CRM control scheme for TLB PFC is proposed based on the degree-of-freedom of current-slope shaping introduced in Chapter 2 [59]. Main advantage of adopting the three-level scheme to CRM operations is reduction of variable CRM switching frequency and switching losses, especially prominent for light load condition. Thus, TLB PFC can achieve improved efficiency throughout wide-load range at the small cost of input PFC decrement. Moreover, decreased peak inductor current brings waveform quality improvement such as THD and EMI peak. Detailed analysis of effects, derivation of key equations, PFC control design, and digital implementation are explained step by step. The verification of proposed control scheme is also conducted by a series of experimental results.

3.1 Proposed Three-Level CRM Control Scheme

The degree-of-freedom in TLB modulation schemes gives various options to shape inductor current slopes in both input voltage modes, Modes I and Mode II. Based on the three-level modulation scheme in Chapter 2, digital-based three-level CRM control scheme is proposed in this section [59]. First, the key waveforms of proposed CRM control schemes are presented by different input voltage range in Fig. 3-1. In the key waveforms, two switching cycles of TLB PFC operations are illustrated under the assumption that input voltage v_{in} and output voltage V_o remain constant; the output capacitor voltages v_{C1} and v_{C2} are also assumed to be balanced and controlled to half of output voltage $V_o/2$. The common on-time T_{on} is also assumed to be constant value during line periods by voltage compensator design.

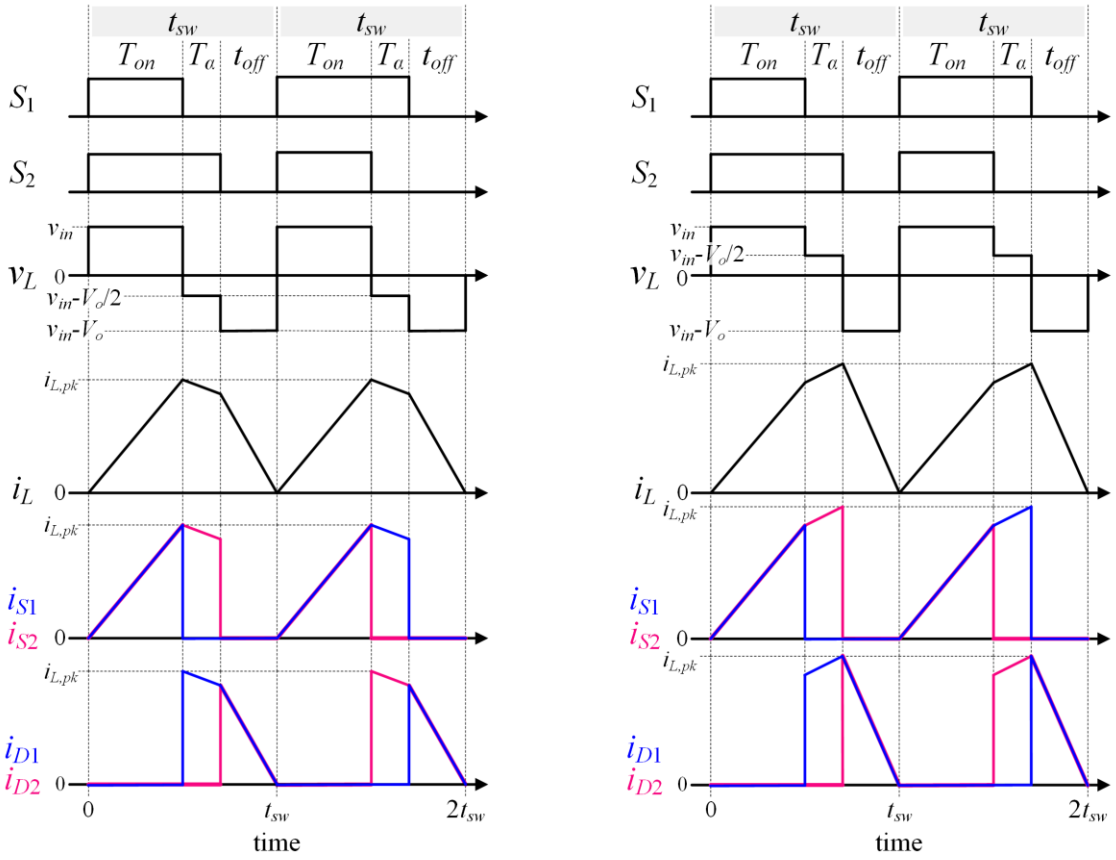


Fig. 3-1. Key waveforms of proposed three-level CRM control scheme by input voltage level.

The basic modulation schemes of proposed three-level CRM control in each switching cycle can be organized as following orders.

1) **Common on-time (T_{on}):** Two main switches S_1 and S_2 turn on together when inductor current reaches at zero and ZCD detection is triggered. The switches remain conducted and complimentary diodes are open for the duration of T_{on}. In this time, positive v_{in} is applied across the inductor and inductor current linearly increases with a v_{in}/L slope.

2) **Single-switch on-time (T_α):** After the duration of T_{on}, one of the switches becomes off and the other still remains conducted for additional on-time T_α. In the proposed CRM scheme, the ratio between T_α and T_{on} is fixed and defined with α as (1).

$$T_{\alpha} = \alpha \cdot T_{on} \tag{1}$$

where α is the designed ratio. In this period, the inductor voltage becomes (v_{in}-V_o/2) and the slope of inductor current (v_{in}-V_o/2)/L can be either positive or negative depending on the input voltage range as shown in Fig. 3-1.

3) **Common off-time (t_{off}):** As the last step in each switching cycle, both the two switches go off to release the inductor energy and to supply load side. In this duration, (v_{in}-V_o) is applied across the inductor so that the inductor current linearly decreases with (v_{in}-V_o)/L slope.

4) **ZCD interruption:** In general, CRM operations rely on the moment of ZCD to begin a new switching cycle. By implementing an external ZCD circuit with comparator, it is easy for digital signal processor (DSP) to detect the moment and to set a switching period by turning on both the switches at the same time.

Throughout ac line cycles, the repetition of four steps ***1)–4)*** will make TLB PFC be able to obtain the three-level quadrangular-current CRM operations. Compared to the conventional two-level CRM operations, all the hardware of power stage and digital controller can be used as they are; the only additional scheme is a three-level switching state for T_{α} which is realized by several sentences in DSP code. Thus, it can be noted that the implementation of proposed three-level CRM control scheme is easy. However, the beneficial effects are relatively considerable as analyzed in the following sections.

In order to balance the two output-capacitor voltages, the proposed control schemes toggle a conducted switch between S_1 and S_2 for single-switch on-time T_{α} in every switching cycle. It is also recommended in circuit design stage to select output capacitors C_1 and C_2 with even capacitance and effective-series-resistance (ESR) parameters [59].

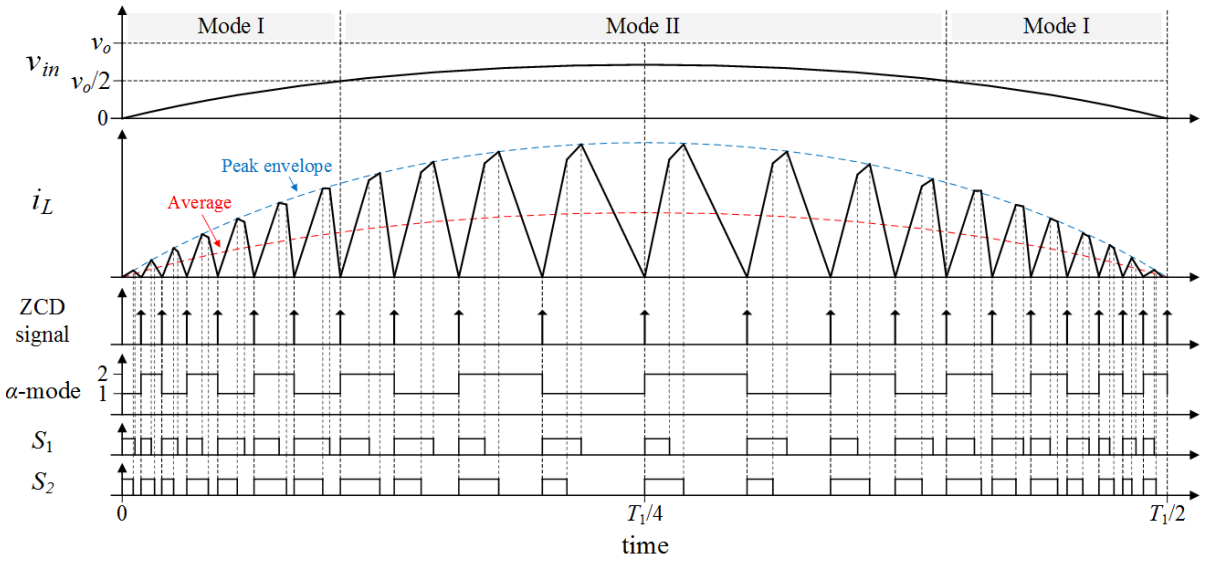


Fig. 3-2. Half line-cycle waveforms of TLB PFC by proposed CRM control scheme.

As the final outcome, the operation principles of proposed three-level CRM control scheme can be summarized with Fig. 3-2 which shows a half period of ac line cycle.

3.2 Key Equations and Effects Analysis

From the operation waveforms described in Fig. 3-1, key equations and effects of the three-level control scheme can be analyzed. Major operating parameters such as switching frequency, average common on-time T_{on}, average/peak of inductor current, and rms current of each components are essential for PFC regulation, component selection, and passive part design. Equations of the mentioned parameters are derived as follows.

First, a volt-sec balancing relationship in inductor voltage waveform is used for formulating common off-time t_{off}.

$$t_{off} = \frac{(1+\alpha)v_{in} - (\alpha/2)V_o}{V_o - v_{in}} \cdot T_{on} \tag{2}$$

Then, using (1) and (2), switching frequency in the switching period can be calculated by (3).

$$f_{sw} = \frac{1}{T_{sw}} = \frac{1}{T_{on} + T_{\alpha} + t_{off}} = \frac{1}{(1+\alpha/2)T_{on}} \cdot \frac{V_o - v_{in}}{V_o} \tag{3}$$

As can be inferred from (3), the design ratio α is located in the denominator so that higher α value will result lower switching frequency in the switching cycle.

Peak inductor current of CRM operation is equal to the turn-off switch current. Accordingly, the parameter is related to turn-off switching losses and current stresses. From the inductor current waveforms in Fig. 3-1, the equations of peak inductor current in Mode I and Mode II can be derived and expressed by (4).

$$i_{L.pk} = \begin{cases} \dfrac{v_{in}}{L} \cdot T_{on} & \text{, Mode I} \\ \dfrac{(1+\alpha)v_{in} - (\alpha/2)V_o}{L} \cdot T_{on} & \text{, Mode II} \end{cases} \tag{4}$$

Average input current of TLB PFC can be also calculated from Fig. 3-1 because it is equal to average inductor current. By integrating and averaging inductor current waveforms in two switching cycles, average input current can be formulated in (5).

$$\overline{i_{in}} = \overline{i_L} = \frac{T_{on}}{2L(1+\alpha/2)} \left\{ \left(\frac{\alpha^2}{2} + \alpha + 1 \right) v_{in} - \frac{\alpha^2}{4} V_o \right\} \tag{5}$$

Average input current is important variable since high input PF of TLB PFC can be obtainable only when average input current is in phase with ac input voltage v_{in}.

Rms currents of major components (switch, diode and inductor) can be derived from two switching-cycle waveforms in Fig. 3-1. In (6)–(8), the rms current equations of major components in two switching periods are expressed.

$$i_{S.rms} \cong \sqrt{\left(\frac{1/3+\alpha/2}{1+\alpha/2}\right)\frac{V_o - v_{in}}{V_o}} \cdot \frac{T_{on}}{L} \cdot v_{in} \tag{6}$$

$$i_{D.rms} \cong \sqrt{\left(\frac{1/3+\alpha/2}{1+\alpha/2}\right)\frac{v_{in}}{V_o}} \cdot \frac{T_{on}}{L} \cdot v_{in} \tag{7}$$

$$i_{L.rms} \cong \sqrt{\left(\frac{1/3+\alpha/2}{1+\alpha/2}\right)} \cdot \frac{T_{on}}{L} \cdot v_{in} \tag{8}$$

Those rms equations can be used for component selection, design and loss estimation.

From the beginning of control explanation, the value of common on-time T_{on} is assumed as constant value resulted from slow-dynamic voltage compensator. Here, average equation of T_{on} in line cycles can be derived under assumption that output dc-power P_o is equal to input ac power without losses. Ac-side input power can be calculated by multiplication of input rms voltage and current. Then, average value of T_{on} can be derived as (9).

$$T_{on} = \frac{2LP_o}{v_{in.rms}^{\ 2}} \cdot \left(\frac{1+\alpha/2}{1+\alpha}\right) \tag{9}$$

This average T_{on} will be resulted from voltage compensator for the given specifications and remain almost constant throughout ac line cycles. Then, by using the average T_{on}, instantaneous equations of many variables can be computed. For example, real-time switching frequency and peak inductor current during a line cycle can be calculated by (10)–(11), which are induced from replacing T_{on} in (3)–(4) with (9).

$$f_{sw} = \frac{1}{2LP_o} \cdot \frac{1+\alpha}{(1+\alpha/2)^2} \cdot \frac{v_{in.rms}^{\ 2}(V_o - v_{in})}{V_o} \tag{10}$$

$$i_{L.pk} = \begin{cases} 2P_o \cdot \dfrac{v_{in}}{v_{in.rms}^{\ 2}} \cdot \left(\dfrac{1+\alpha/2}{1+\alpha}\right) & \text{, Mode I} \\ 2P_o \cdot \dfrac{(1+\alpha)v_{in} - (\alpha/2)V_o}{v_{in.rms}^{\ 2}} \cdot \left(\dfrac{1+\alpha/2}{1+\alpha}\right) & \text{, Mode II} \end{cases} \tag{11}$$

By using (10), instantaneous variable switching frequency of CRM operations can be plotted. In Fig. 3-3, an example of switching frequency variation is shown with specifications of v_{in}=110 V_{rms}, V_o=400 V, L=230 μH, P_o=300 W and α from 0 to 1 (at an interval of 0.1).

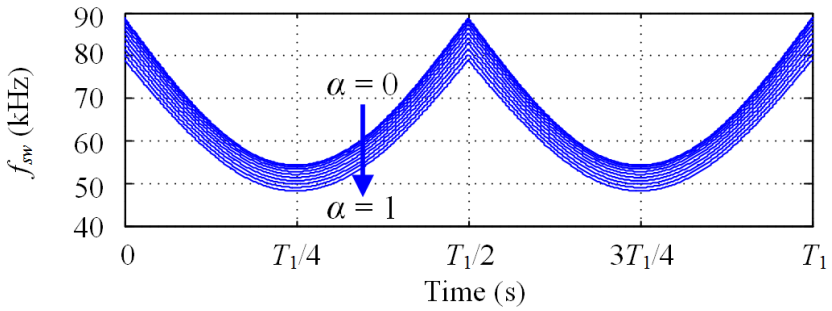


Fig. 3-3. Switching frequency variation by α-ratio.

As the ratio α in the denominator of (10) increases, the magnitudes of instantaneous switching frequency in CRM operations decrease. The effect of reduced CRM switching frequency will lead to reduction of switching losses and improvement of converter efficiency. In general, the switching frequency range of CRM control goes higher as input rms voltage increases and load level decreases. Especially for light-load condition with high input rms voltage, switching frequency can easily move to several hundred kHz and near MHz region. In those regions, TLB CRM PFC suffers from high switching losses and efficiency drops. Thus, switching frequency reduction by proper α-ratio can bring significant efficiency improvement.

From the equations in (11), expected maximum of peak inductor currents can be calculated. In Fig. 3-4, two input-rms-voltage conditions (110 V_{rms} and 220 V_{rms}) are used to check the peak currents in Mode I and Mode II; other conditions are V_o=400 V, L=230 μH, P_o=300 W and α from 0 to 1.

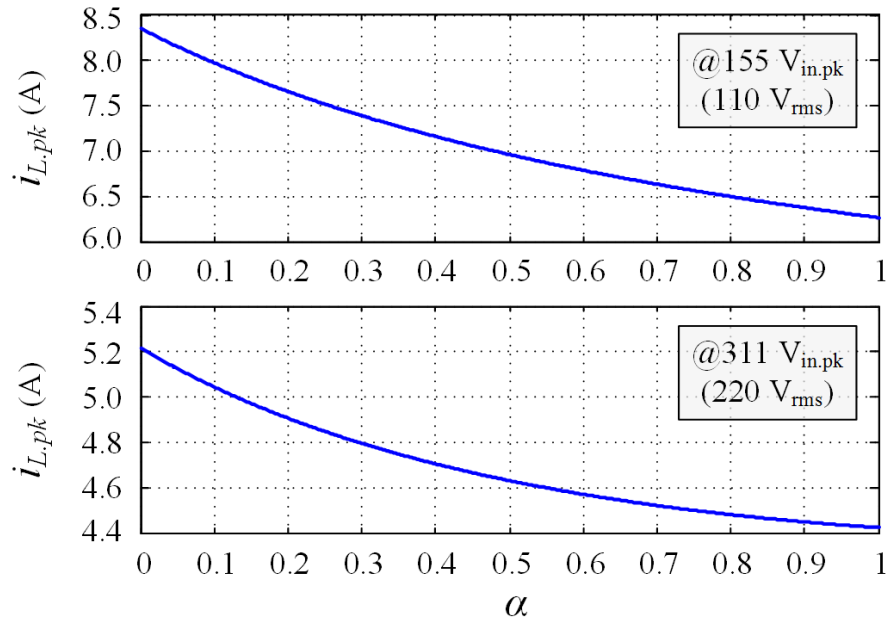


Fig. 3-4. Peak inductor current by α-ratio.

As shown in the plots, the maximum peak inductor current can be reduced by higher α ratio. With the value of α=1, the maximum peak current can be reduced by 2.2 A (26.2%) in 110 V_{rms} case and 0.75 A (14.4%) in 220 V_{rms} case, respectively. Since the peak inductor current in each switching cycle is equal to turn-off current of devices, it has influence on turn-off switching losses and converter efficiency.

With the average equation of T_{on} in (9), component rms currents in two switching cycles (6)–(8) can be extended to line-cycle (T_1) calculation. By substituting (9) for (6)–(8), the rms currents of major parts can be calculated by (12)–(14).

$$i_{S.rms(T_1)} \cong \frac{2P_o}{v_{in.rms}} \sqrt{\frac{(1/3+\alpha/2)(1+\alpha/2)}{(1+\alpha)^2}} \sqrt{\frac{V_o - v_{in.rms}}{V_o}} = k_\alpha \frac{2P_o}{v_{in.rms}} \sqrt{\frac{V_o - v_{in.rms}}{V_o}} \tag{12}$$

$$i_{D.rms(T_1)} \cong \frac{2P_o}{v_{in.rms}} \sqrt{\frac{(1/3+\alpha/2)(1+\alpha/2)}{(1+\alpha)^2}} \sqrt{\frac{v_{in.rms}}{V_o}} = k_\alpha \frac{2P_o}{v_{in.rms}} \sqrt{\frac{v_{in.rms}}{V_o}} \tag{13}$$

$$i_{L.rms(T_1)} \cong \frac{2P_o}{v_{in.rms}} \sqrt{\frac{v_{in.rms}}{V_o}} = k_\alpha \frac{2P_o}{v_{in.rms}} \tag{14}$$

where $k_\alpha = \sqrt{(1/3+\alpha/2)(1+\alpha/2)/(1+\alpha)^2}$. The rms currents in a line-cycle can be used for component conduction-loss calculations. For switches S_1–S_2 and inductor L, conduction losses are proportional to square of rms currents; for diodes D_1–D_2, their forward-conduction losses are directly proportional rms currents. Thus, from (12)–(14), it can be noted that conduction losses of diodes are proportional to k_α while conduction losses of switches and inductor are proportional to k_α^2. In Fig. 3-5, the tendency curves of k_α and k_α^2 are plotted with α from 0 to 1.

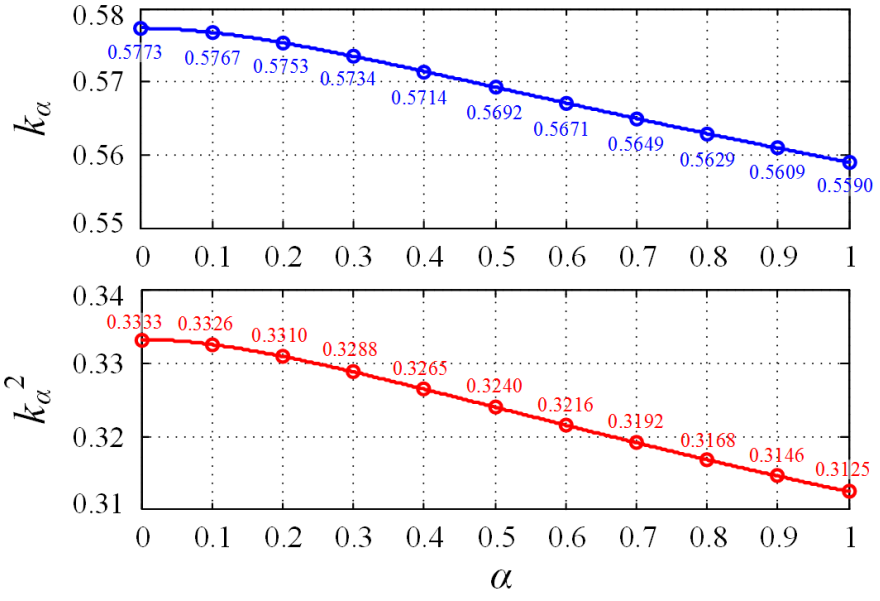


Fig. 3-5. Conduction loss coefficients by α-ratio.

As shown in the plots, conduction-loss reductions can be achieved by higher α-ratio; with the case of α =1, diode conduction losses can be reduced by 3.29% and conduction losses from switches and inductor can be decreased by 6.24%.

In Summary, by using higher α ratio in the proposed three-level CRM control scheme, TLB PFC can have operational benefits including switching losses reduction, conduction losses reduction and efficiency improvement. The mitigated switching losses are enabled by reduction effects of switching frequency and peak turn-off currents while the reduced conduction losses are realized by lowered rms currents.

3.3 Basic PFC Regulations

As a sort of PFC converter, TLB PFC must have two basic regulation capabilities on input PF and dc-output voltage. First, for achieving high input PF close to unity factor, average input current is needed to be aligned in phase with ac input voltage. The in-phase condition can be guaranteed when average input current and ac input voltage have a proportional relationship ($\overline{i_{in}} = k \cdot v_{in}$). In the proposed three-level CRM control scheme, the two input variables in (5) can become proportional to each other when α^2 is small enough to be neglected. If the condition is satisfied, then (5) is approximated to (15).

$$\overline{i_{in}} = \left\{ \frac{T_{on}}{2L} \frac{(1+\alpha)}{(1+\alpha/2)} \right\} \cdot v_{in} \tag{15}$$

However, as analyzed in the previous section, the proposed control scheme can bring more benefits when higher α value is implemented. It means that a technical trade-off exists at the selection of α ratio. Thus, if a higher α is selected in the proposed three-level control

scheme, significant reductions of switching and conduction losses are expected at the cost of input PF decrement. In Fig. 3-6, the simulated input PF results are plotted based on two nominal input voltages and conditions of V_o=400 V, L=230 μH, P_o=300 W and α from 0 to 1.

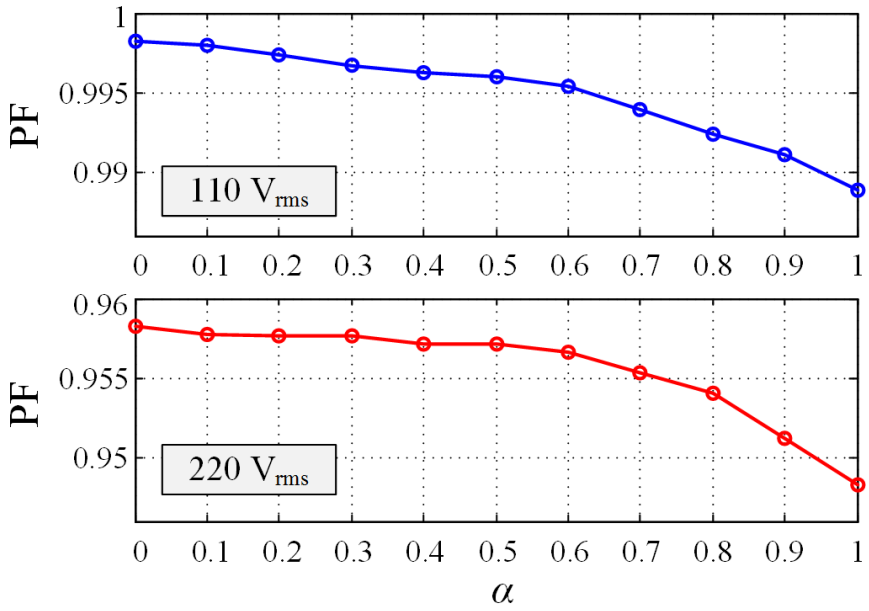


Fig. 3-6. Input PF curves by α-ratio.

As can be seen, input PF of TLB PFC goes lower as α value increases and the decreasing rate becomes steeper around α=0.5. This trade-off should be considered at the control design stage and proper boundary of α is necessary for the proposed control scheme.

Secondly, dc-output voltage control must be guaranteed under wide-range load condition. The output voltage control is generally based on feedback control structure and typical feedback compensators such as proportional-integral (PI) can be used for the regulation. For designing the compensator, derivation of control-to-output voltage transfer function is needed and common on-time T_{on} is generally used as control variable in CRM control schemes. The transfer function $G_{vt}(s)$ between T_{on} and v_o can be derived to (16) from small-signal modeling.

$$G_{vt}(s)=\frac{\hat{v}_o(s)}{\hat{T}_{on}(s)}=\frac{R_o}{4L}\frac{{v_{in}}^2}{V_o}\frac{(1+\alpha)}{(1+\alpha/2)}\cdot\frac{1}{1+sCR_o/4} \tag{16}$$

where R_o is the equivalent load resistance and C is the output capacitance of C_1 and C_2.

For the proposed three-level CRM control scheme, a PI-type voltage compensator in the form of (17) is used and total closed control-loop gain $T_v(s)$ can be formulated by (18).

$$H_v(s)=\frac{k_v}{s}\left(1+\frac{s}{\omega_z}\right) \tag{17}$$

$$T_v(s)=H_v(s)\cdot G_{vt}(s)\cdot FM \tag{18}$$

where FM is the modulation ratio in pulse-width-modulation (PWM) in DSP control unit. It is general practice to set the cut-off frequency of closed-loop gain at relatively low range near 1–5 Hz, which is less than line frequency by an order. By designing in that way, the result of voltage compensator, T_{on}, can remain unchanged during 50/60-Hz line cycles.

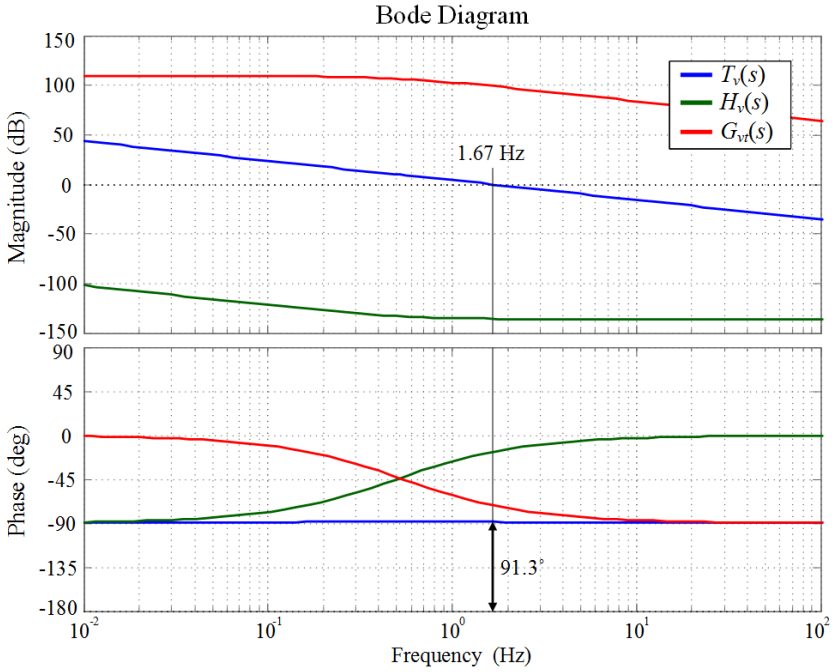


Fig. 3-7. Bode plot of transfer functions.

For the proposed CRM control scheme, PI gains in (17) are selected to $k_v = 5\times10^{-6}$ and $\omega_z = 2\pi\times5$. Fig. 3-7 shows the bode plots of transfer functions in (16)–(18) based on the designed compensator and the design can obtain sufficient phase margin near 90 degree at the cut-off frequency 1.67 Hz.

3.4 Soft-Switching Turn-on

As one of ZCS control technique, the proposed three-level CRM control scheme begins every switching period with zero-current turn-on. Although inductor current waveforms in Fig. 3-1 and Fig. 3-2 are drawn with linear shapes before and after ZCD moments, pre-turn-on process with resonance physically exists and its duration should be considered before new switching period begins. Since two switches S_1 and S_2 are always off before new switching cycle, the switch-junction capacitors C_{oss} are fully charged and the charged voltages should be discharged enough for upcoming conduction. In Fig. 3-8, the discharging path is illustrated and it shows that the discharging current faces the two C_{oss} and boost inductor L in series.

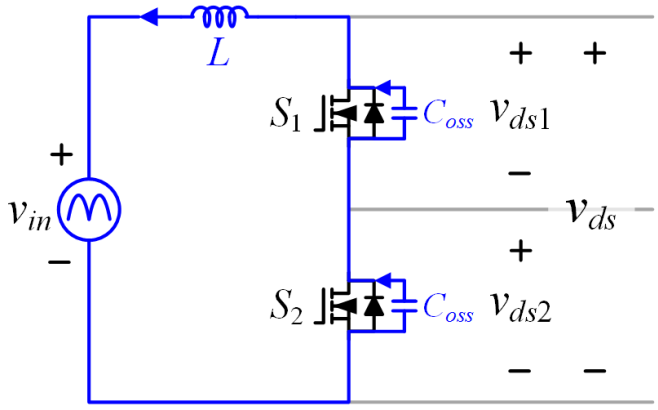


Fig. 3-8. Pre-turn-on process in the proposed scheme.

Due to the resonance condition in Fig. 3-8, the discharging current through inductor and the voltages across two switches will have resonance frequency in (19).

$$f_{res} = \frac{1}{2\pi\sqrt{L_{res} \cdot C_{res}}} = \frac{1}{2\pi\sqrt{L \cdot C_{oss}/2}} \tag{19}$$

During the pre-turn-on resonant period, key waveforms of the proposed CRM control scheme by input voltage range can be described with Fig. 3-9.

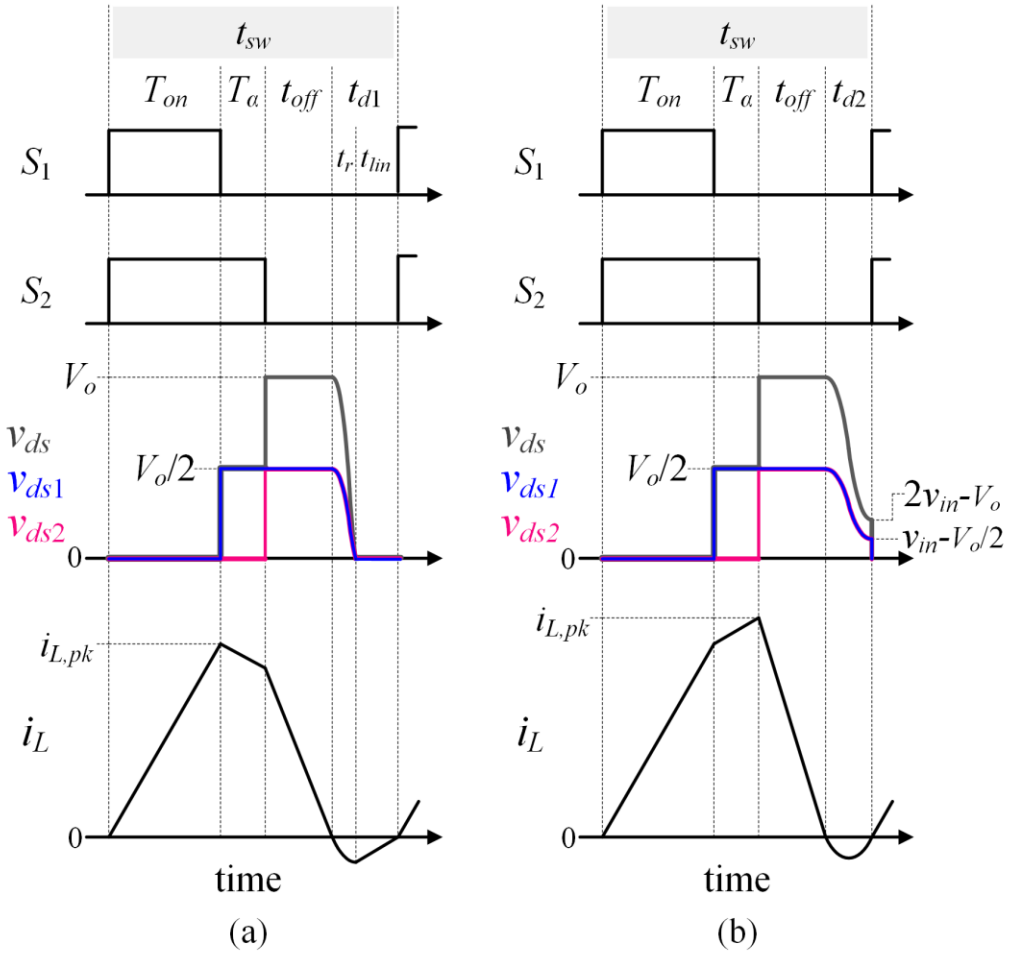


Fig. 3-9. Key waveforms of pre-turn-on process by input voltage range.

As can be seen, drain-to-source voltage v_{ds} of each switch starts decreasing when the inductor current reaches at zero and turns to negative to release charged C_{oss}. The voltages v_{ds1} and v_{ds2} go down in the sinusoidal form with resonant frequency in (19) and amplitude of (V_o-v_{in})/2.

In Mode I (v_{in}<V_o/2) of Fig. 3-9, the drain-to-source voltages are pulled down to zero by the resonant discharging after the zero-current moment. After reaching at zero, the drain-to-source voltages are clamped to zero and inductor voltage becomes equal to input voltage, synthesizing linear current increment with v_{in}/L slope. As a result, at the beginning moment of new switching cycle, both switches turn on conducted with ZCS and zero-voltage switching (ZVS) characteristics. Considering these principles, the pre-turn-on process in Mode I can be divided into two as resonant delay zone (t_r) and linear increment zone (t_{lin}); the total duration of pre-turn-on process t_{d1} can be calculated as follows.

$$t_{d1} = t_r + t_{lin} = \left\{ \frac{1}{2\pi f_{res}} \cdot \cos^{-1}\left(-\frac{v_{in}}{V_o - v_{in}} \right) \right\} + \left\{ \frac{1}{2\pi f_{res}} \sqrt{\frac{V_o}{v_{in}}\left(\frac{V_o}{v_{in}} - 2 \right)} \right\} \tag{20}$$

In Mode II ($V_o/2$<v_{in}<V_o), the discharging level of drain-to-source voltages is different from that of Mode I due to the input voltage range. With the resonance amplitude (V_o-v_{in})/2, the drain-to-source voltages in Mode II cannot reach at zero. As shown in Fig. 3-9, the resonant v_{ds1} and v_{ds2} reach at the lowest voltage (v_{in}-V_o/2) after a half period of resonant frequency. In order to minimize turn-on switching losses as much as possible, it is necessary to turn on both switches at the moment of lowest drain-to-source voltages. Then, required delay duration (t_{d2}) in Mode II can be calculated by (21).

$$t_{d2} = \frac{1}{2 f_{res}} = \pi \sqrt{L \cdot \frac{C_{oss}}{2}} \tag{21}$$

This type of switching operation is widely used in Mode II of CRM controls and called as valley switching (VS) method.

3.5 Passive Component Guideline

In the TLB PFC topology, there are two passive components, inductor and output capacitors. In general, component design and selection guidelines are necessary for those passive components; there are several things to be considered in the design and selection procedures [64]–[66].

First, for inductance L value, two physical factors should be taken into account: minimum and maximum frequencies of variable switching frequency CRM operation. Minimum frequency is generally designed beyond 20 kHz (e.g. 30–40 kHz) in order to avoid audible noise. Maximum switching frequency is designed less than gate driver's maximum operating frequency. After getting the boundary of switching frequency, acceptable range of inductance L can be acquired by (22).

$$L = \frac{v_{in.rms}{}^2}{2P_o f_{sw(\min/\max)}} \cdot \frac{(1+\alpha)}{(1+\alpha/2)^2} \cdot \frac{V_o - v_{in}}{V_o} \tag{22}$$

Secondly, for the output capacitances C ($=C_1=C_2$) selection, voltage ripples on output-capacitor voltages are important factors. From the total output-voltage point of view, the effective output capacitance is $C/2$ and dominant frequency is fundamental line frequency. And, the voltage ripples are maximized when output is at full-load $P_{o.\max}$ condition. Thus, considering all the factors, the relationship between output capacitance and desired voltage ripple limit ΔV_o can be formulated by inequality in (23).

$$\frac{C}{2} \geq \frac{P_{o.\max}}{2\pi f_1 V_o} \cdot \frac{1}{\Delta V_o} \tag{23}$$

3.6 Performance Assessment

In this section, TLB PFC with the proposed CRM control scheme is evaluated with several performance factors including losses, PF, THD and EMI. Tendencies of the factors are discussed with α-variation and compared with conventional two-level CRM control scheme which is identical to α=0 case.

1) **Loss analysis:** In the TLB PFC topology, seven major components exist: two switches S_1–S_2, two diodes D_1–D_2, inductor L, and two output capacitors C_1–C_2. Each component has two kinds of operating losses which are switching-related losses and conduction-related losses. Among them, losses from the two output capacitors are small enough to be neglected. Losses from the other five components are listed in Table 3-1 with variation of α-ratio.

Table 3-1. Loss Breakdown with α-variation.

Components	Losses	α-ratio		
		0 (triangular)	⟷	higher
Switches (S_1–S_2)	$P_{S,sw.}$	Highest	⟷	Lower
	$P_{S,cd.}$	Highest	⟷	Lower
Diodes (D_1–D_2)	$P_{D,rr.}$	Negligible		
	$P_{D,cd.}$	Highest	⟷	Lower
Inductor (L)	$P_{L,core}$	Highest	⟷	Lower
	$P_{L,cd.}$	Highest	⟷	Lower

For clear understanding, all the switching-related losses and conduction-related losses are formulated in (24) and (25), respectively.

$$\begin{aligned} P_{S.sw.} &\cong \int_0^{T_1} E_{off}\, f_{sw}\, dt \\ P_{D.rr.} &\cong 0 \\ P_{L.core} &= V_{core} \int_0^{T_1} A_{B-H}\, f_{sw}\, dt \end{aligned} \tag{24}$$

$$\begin{aligned} P_{S.cd.} &= I_{S.rms(T_1)}{}^2 R_{ds.on} \\ P_{D.cd.} &\cong I_{D.rms(T_1)} v_F \\ P_{L.cd.} &= I_{L.rms(T_1)}{}^2 R_L \end{aligned} \tag{25}$$

where E_{off} is the turn-off switching energy of switches, V_{core} is the volume of inductor core, A_{B-H} is the swing area on core B-H curve, $R_{ds.on}$ is the switch on-resistance, v_F is the forward-drop voltage of diode, and R_L is the equivalent resistance of inductor.

As analyzed in section 3.2, switching frequency f_{sw} goes lower as the value of α is set to be higher value; E_{off} and A_{B-H} can be also smaller because the turn-off current and peak inductor current are reduced by higher α-ratio. Thus, all the switching-related losses except $P_{D.rr}$ can be reduced by increasing α. The reverse-recovery loss $P_{D.rr}$ of two diodes is originally negligible because the ZCS turn-of switches eliminate the reverse-recovery issue.

For conduction-related losses in (25), all the rms-current terms are already proven to be reduced by higher α value, from Fig. 3-5 and equations (12)–(14). Thus, regardless of series resistances and forward drop, the conduction-related losses can be also improved by setting non-zero α-ratio in the proposed CRM control scheme.

2) **Input PF:** As mentioned in section 3.3, the technical trade-off of proposed three-level control scheme is decrement of input PF. Expected drops of input PF at full-load condition

are about 1% for both 110 V_{rms} and 220 V_{rms} nominal voltages. In general, input PF becomes worse as PFC converter operates at lighter load condition, which means that the input PF under the proposed control could be further decreased over than 1% at light-load condition. However, as plotted in Fig. 3-6, by properly limiting the range of α, severe PF decrement can be avoided. In the following experimental verification section, the range of α in the proposed control method is limited from 0 to 0.3.

3) **THD:** In ad-dc PFC rectification system, low THD can be practically interpreted with reduced peaks of harmonic components. Accordingly, it is acceptable to evaluate input THD with the calculation of (26) [67].

$$\mathrm{THD} = \frac{\sqrt{\sum_{j=2}^{\infty}\left(i_{in,pk(j)}\right)^2}}{i_{in,pk(1)}} \tag{26}$$

where $i_{in.pk(j)}$ is the peak current of j-th order harmonic. In CRM operations, the major harmonic components come from variable switching-frequency range. Since the peak inductor currents can be reduced by higher α, theoretical value of THD is expected to be reduced by the proposed three-level CRM control scheme.

4) **EMI:** In the CRM operations of TLB PFC, main EMI components are differential-mode (DM) EMI which are resulted from high current ripples and peaks. Since the design of higher α-ratio can bring the reduction of peak inductor current, it is natural to expect the maximum magnitude of DM EMI can be reduced by the proposed three-level CRM control scheme. In Fig. 3-10, EMI simulation plots are presented for both DM and common-mode (CM) cases.

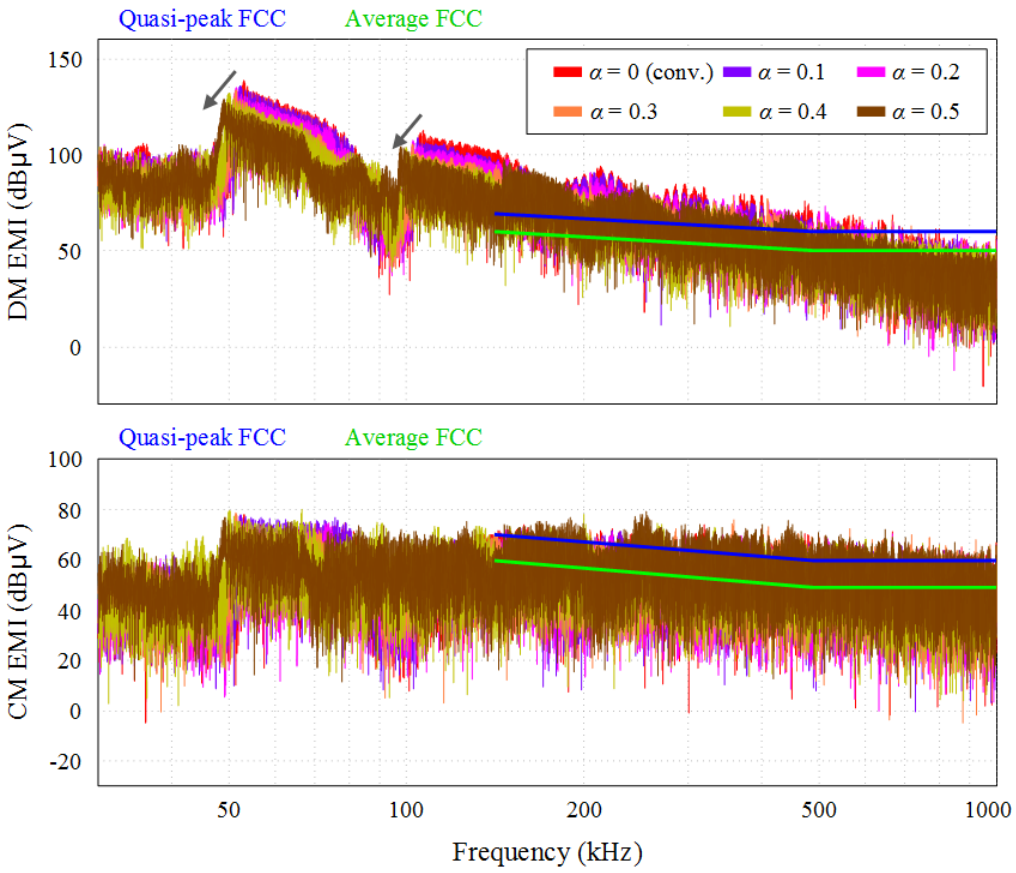


Fig. 3-10. EMI responses by α-variation.

As highlighted with arrows in the plots, the effects of α increments from 0 to 0.5 can be found by peak reduction of DM EMI and decreased range of switching frequencies. Thus, it can be said that the proposed three-level CRM control scheme can suppress DM EMI magnitudes by just using non-zero α value in the modulation scheme.

3.7 Digital Implementation

The proposed CRM scheme can be easily realized by digital implementation in DSP. In order to accomplish the implementation, external ZCD circuit and modulation algorithm should be equipped with DSP control unit.

First, external ZCD circuit is depicted in Fig. 3-11. It consists of four components including secondary winding of inductor, resistor, capacitor and zener diode.

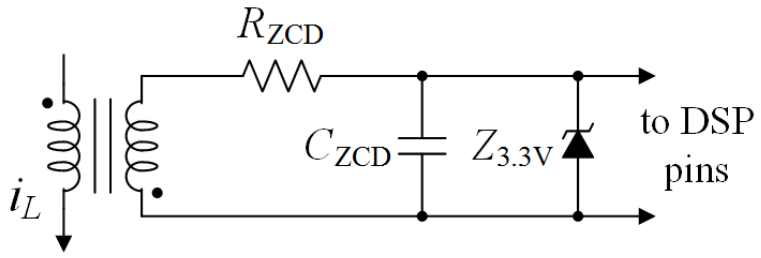


Fig. 3-11. External ZCD circuit.

The secondary wire converts the inductor voltage to lower voltage level. Then, the reflected voltage is applied to the *R/C/Z* impedance network. The role of R_{ZCD} is to limit the current flow to DSP side under certain level. The value of R_{ZCD} is generally selected to several kΩ to limit the current in mA range. For selecting C_{ZCD}, time constant τ formed by R_{ZCD} and C_{ZCD} should be considered. From the previous literatures regarding ZCD scheme, the time constant is designated to be quarter of the pre-turn-on resonant period in (19) to detect the accurate ZCD moment. Then, C_{ZCD} can be determined by (27) [63].

$$\tau = R_{ZCD}C_{ZCD} = \frac{T_{res}}{4} = \frac{\pi\sqrt{L \cdot C_{oss}/2}}{2} \tag{27}$$

The voltage across the parallel capacitor and zener diode is directly connected to differential comparator inside DSP control unit. Therefore, zener diode with breakdown voltage 3–3.3 V is necessary in the external ZCD circuit for DSP protection purpose.

Secondly, hardware-wise connection inside DSP controller and algorithm generation are required. In Fig. 3-12, control block diagram of proposed CRM control scheme is illustrated.

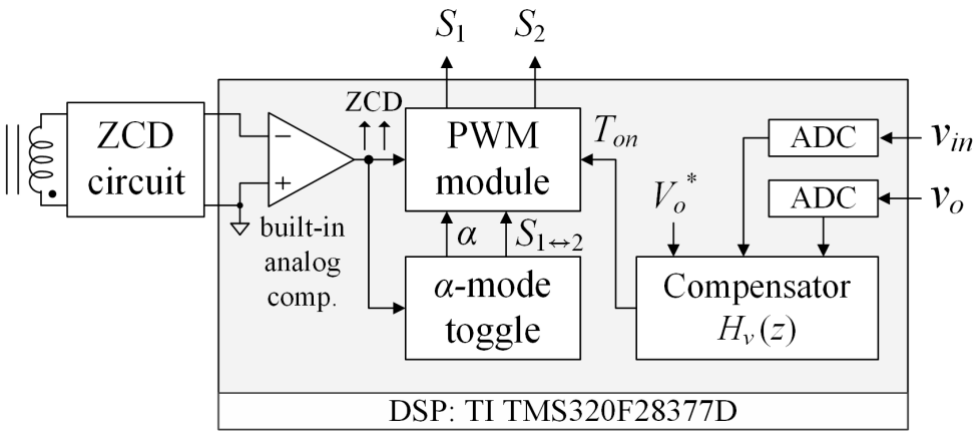


Fig. 3-12. Control block diagram.

The output of external ZCD circuit links to direct input of internal analog comparator which can trigger ZCD signals. At the ZCD moment, DSP controller resets PWM modules, turns on both switches S_1 and S_2, and toggles the conducted switch in T_α duration. Detached from the ZCD signals, regular interrupt routines are produced every sampling frequency and execute compensation of output voltage with designed voltage compensator H_v. As a result, common on-time T_{on} is resulted and provided to PWM modules.

In order to explain practical implementation with real DSP, an example of digital sequences is shared with a widely-used model (TMS320F28377D, Texas Instruments). In Fig. 3-13, key waveforms of several DSP control registers are shown [68]. Matched digital sequences are explained in detail as follows.

1) **Basic control setup**: ePWM register [PHSDIR] is assigned to toggle between 0 and 1 whenever the analog comparator in Fig. 3-12 sets the ZCD signals. The role of [PHSDIR] is to determine the ePWM counter direction [CTRDIR] at the next trigger event. By the value of [CTRDIR], the ePWM counter [TBCTR] goes up and down. And, ePWM phase register [TBPHS] is the numerical location where the counter will move to, whenever the ZCD signal

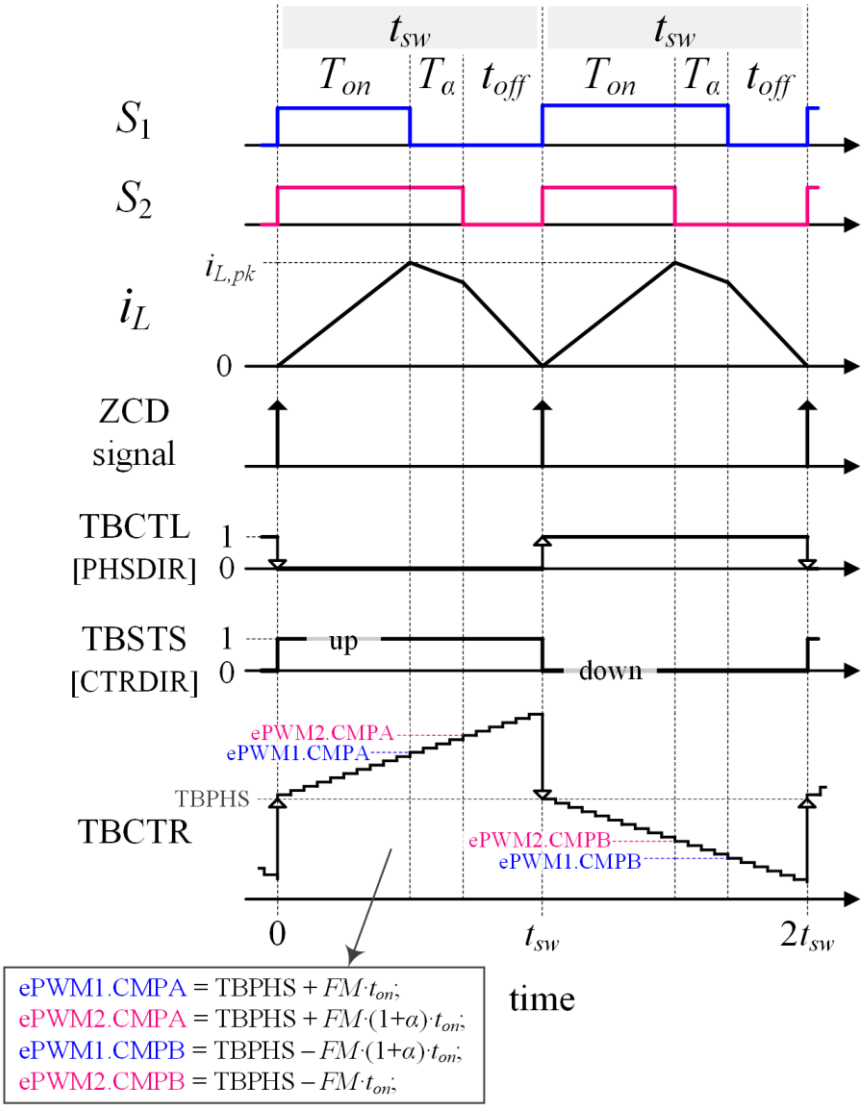


Fig. 3-13. Key waveforms of digital implementation with TI 28377D.

goes up. By these basic settings written in initialization code, the ePWM counter [TBCTR] can move as shown in Fig. 3-13.

2) **ZCD interruption:** At the moment of ZCD, the built-in analog comparator produces ZCD signals. Then, an immediate interruption in DSP will be executed to toggle [PHSDIR]; ePWM counter [TBCTR] register is replaced by the pre-determined [TBPHS] value.

3) **Regular interrupt routine**: In sampling frequency cycle, a regular interrupt routine is activated and output voltage compensation is conducted by PI controller. Then, the common on-time T_{on} is generated and converted to an ePWM-scale value. Now, the scaled-value is provided to ePWM modules and compared with ePWM counter [TBCTR]. By setting the comparison registers (CMPx) as in the box of Fig. 3-13, the toggled driving of S_1 and S_2 for T_α duration can be realized.

By combination of steps ***2)–3)*** on the basis of setting ***1)***, the proposed three-level CRM control scheme can be enabled by DSP control unit.

3.8 Experimental Results

In order to validate the effectiveness of proposed CRM control scheme, a prototype of TLB PFC in Fig. 3-14 has been built and tested by a set of experiments. The specifications of experiments are summarized in Table 3-2.

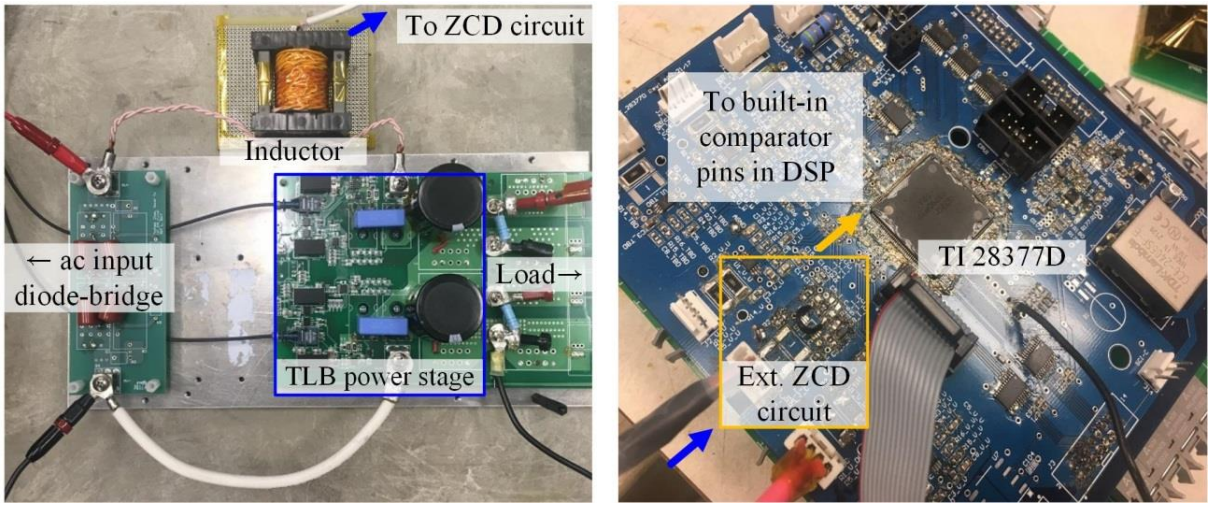


Fig. 3-14. Prototype of TLB PFC with DSP control unit.

Table 3-2. Experimental specifications.

Input voltage	110/220 V_{rms}
Output voltage	400 V
Full load condition	300 W
Switches (S_1, S_2)	IPW60R041P6 (C_{oss}=310 pF, $R_{ds.on}$=41 mΩ)
Diodes (D_1, D_2)	C4D10120D (v_F=1.4 V)
Inductance (L)	230 μH (turn-ratio 21:1 for ZCD circuit)
Output capacitance (C)	470 μF
ZCD circuit	R_{ZCD}=9 kΩ, C_{ZCD}=33 pF, $Z_{3.3V}$: MMSZ5221BT1
DSP control unit	Texas instruments TMS320F28377D
Sampling frequency	50 kHz

110 V_{rms} and 220 V_{rms} are used input voltages since the two voltages are nominal universal-line specifications all over the globe. The prototype is tested from 60 W (20%) to 300 W (100%) load conditions. Passive *LC* components and parts in the external ZCD circuit are selected based on the guidelines. For DSP control unit, an in-house digital control board using TI 28377D chip has been used to realize the proposed CRM control scheme. The range of tested α is from 0 to 0.3.

In Fig. 3-15 and Fig. 3-16, inductor current waveforms by α-variation are shown for different input ranges Mode I and Mode II, respectively. The two figures are captured when the input voltage crosses 100 V (Mode I: $v_{in}<V_o/2$) and 300 V (Mode II: $V_o/2<v_{in}<V_o$) during a 220 V_{rms}/300 W test. As can be seen, one switching cycle of the proposed CRM control scheme consists of four operation steps including common on-time, single-switch on-time, common off-time and pre-turn-on resonant process; the green-color highlighted boxes present the duration of single-switch on-time T_α.

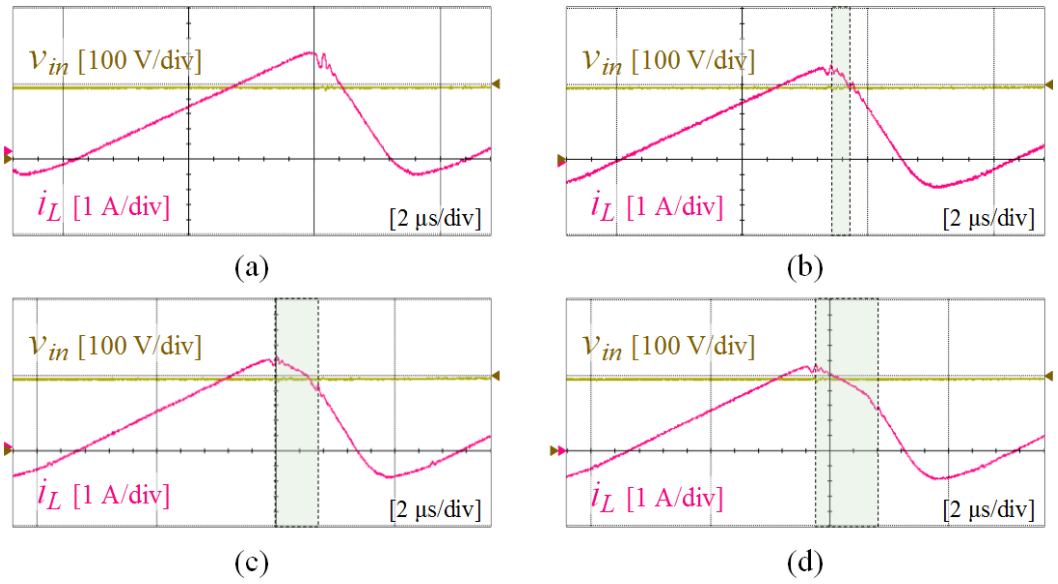


Fig. 3-15. Example of inductor current waveform in Mode I.

(a) α=0 (b) α=0.1 (c) α=0.2 (d) α=0.3.

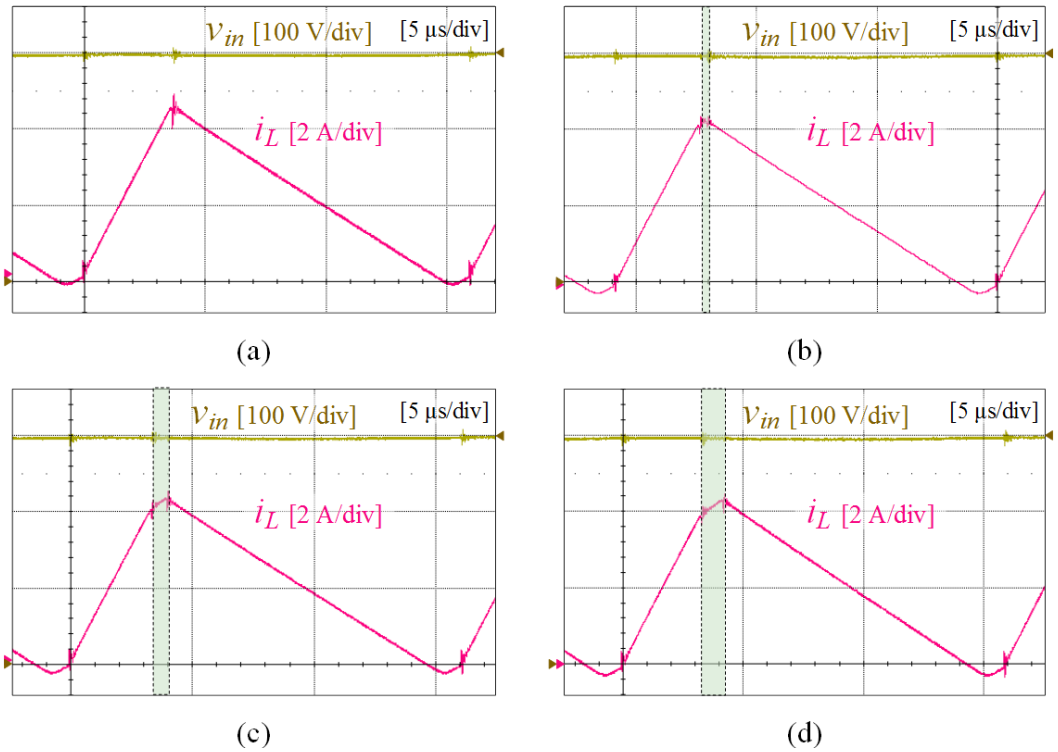


Fig. 3-16. Example of inductor current waveform in Mode II.

(a) α=0 (b) α=0.1 (c) α=0.2 (d) α=0.3.

It can be noted that the TLB PFC prototype can perform the three-level current modulation as expected based on digital implementation with DSP control unit. The peak inductor current and frequency of one switching cycle become reduced in both voltage modes as the value of α is set to higher value, which shows good agreements with analysis.

In Fig. 3-17–Fig. 3-20, steady-state CRM waveforms of TLB PFC with α-variation are arranged by different input voltage and load conditions.

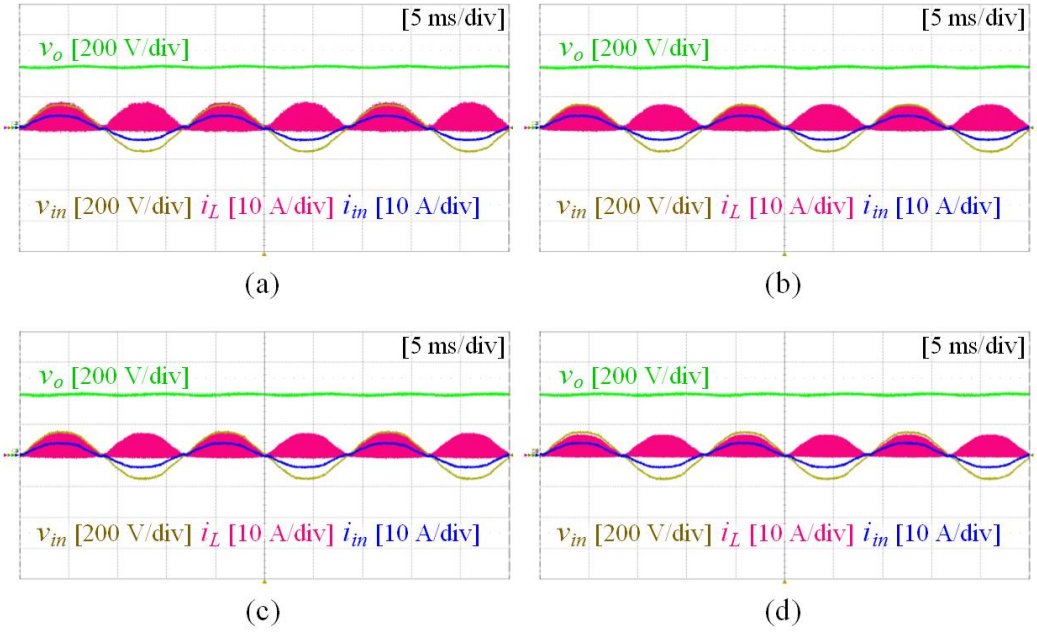


Fig. 3-17. Experimental waveforms by α at 110-V_{rms} and 300-W (100%) conditions.

(a) α=0 (b) α=0.1 (c) α=0.2 (d) α=0.3.

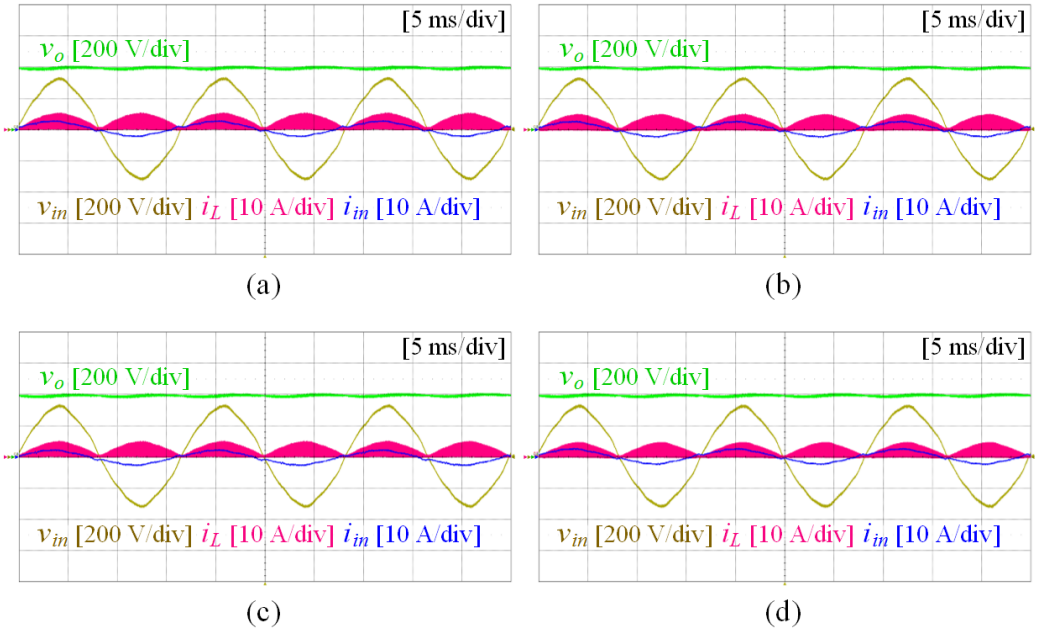


Fig. 3-18. Experimental waveforms by α at 220-V_{rms} and 300-W (100%) conditions.

(a) α=0 (b) α=0.1 (c) α=0.2 (d) α=0.3.

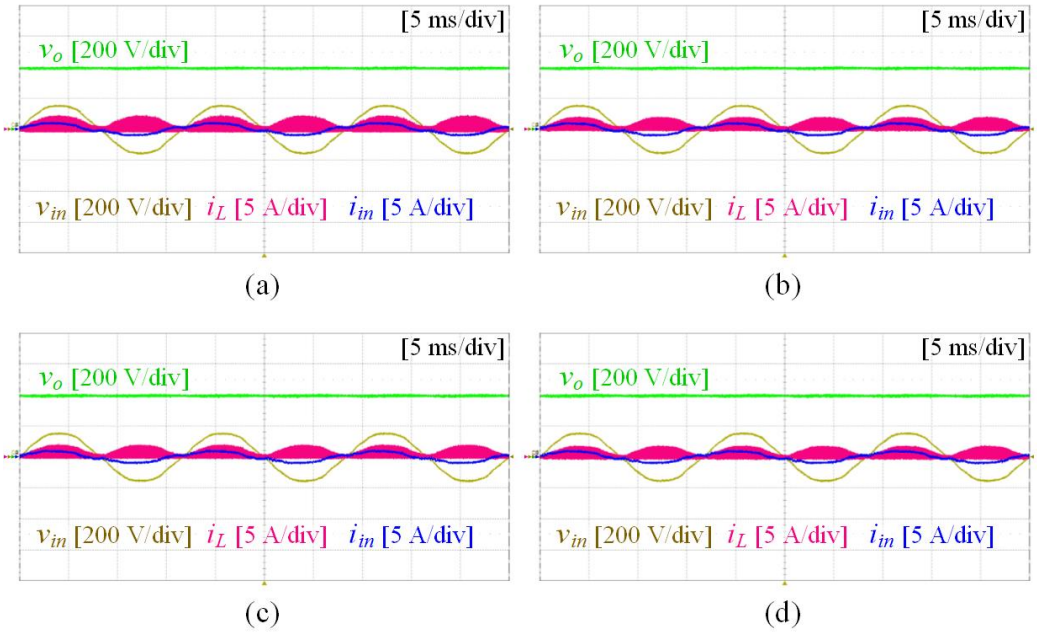


Fig. 3-19. Experimental waveforms by α at 110-V_{rms} and 60-W (20%) conditions.

(a) α=0 (b) α=0.1 (c) α=0.2 (d) α=0.3.

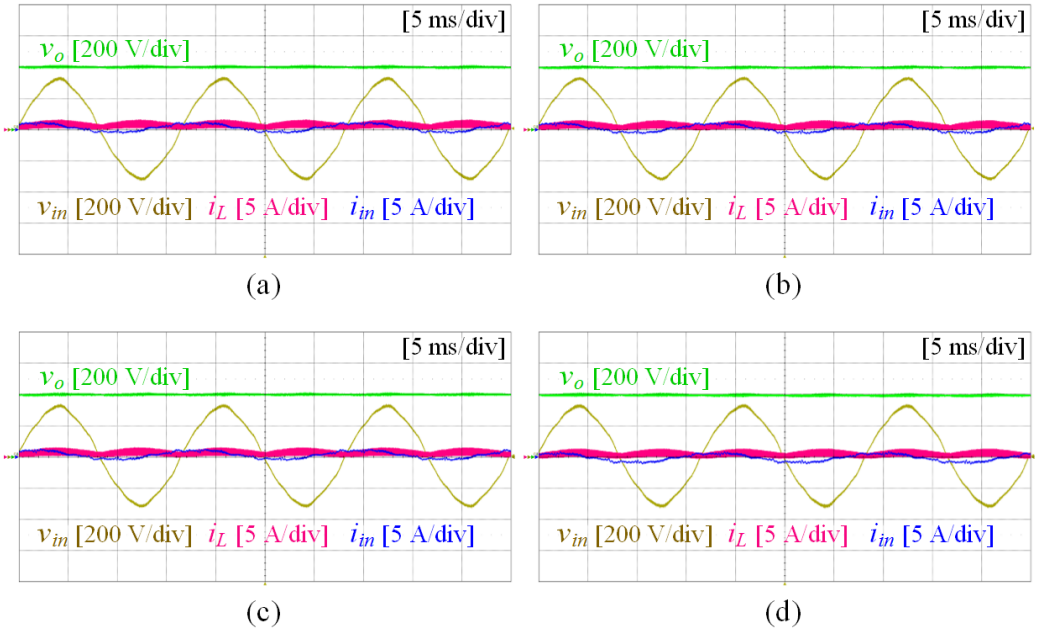


Fig. 3-20. Experimental waveforms by α at 220-V_{rms} and 60-W (20%) conditions.

(a) α=0 (b) α=0.1 (c) α=0.2 (d) α=0.3.

From the experimental waveforms, two aspects of the proposed control scheme can be found. First, basic PFC regulation capabilities including input PF and dc-output voltage are verified with the results. Although the in-phase alignment between the average input current (i_{in}) and the input voltage (v_{in}) becomes dislocated in cases of higher input voltage and lighter load, the input PF remains in reasonable range throughout the wide-operating range by properly limiting the range of α up to 0.3. For the dc-output voltage regulation, all the waveforms show that the output voltage (v_o) is well controlled to 400 V as desired, which proves that the design and implementation of voltage compensator work well. Second, the peak inductor currents of all cases are effectively reduced with higher α setup. In Table 3-3, measurement results of peak inductor currents are summarized.

Table 3-3. Measured peak inductor currents.

v_{in} = 110 V_{rms}				
	$\alpha = 0$	$\alpha = 0.1$	$\alpha = 0.2$	$\alpha = 0.3$
300 W (100%)	8.62 A_{pk}	8.19 A_{pk}	7.72 A_{pk}	7.58 A_{pk}
60 W (20%)	2.08 A_{pk}	2.03 A_{pk}	1.97 A_{pk}	1.83 A_{pk}
v_{in} = 220 V_{rms}				
	$\alpha = 0$	$\alpha = 0.1$	$\alpha = 0.2$	$\alpha = 0.3$
300 W (100%)	5.41 A_{pk}	5.18 A_{pk}	4.96 A_{pk}	4.73 A_{pk}
60 W (20%)	1.42 A_{pk}	1.38 A_{pk}	1.35 A_{pk}	1.29 A_{pk}

From Fig. 3-21 to Fig. 3-23, measurement curves of converter efficiency, input PF and input-current THD are plotted.

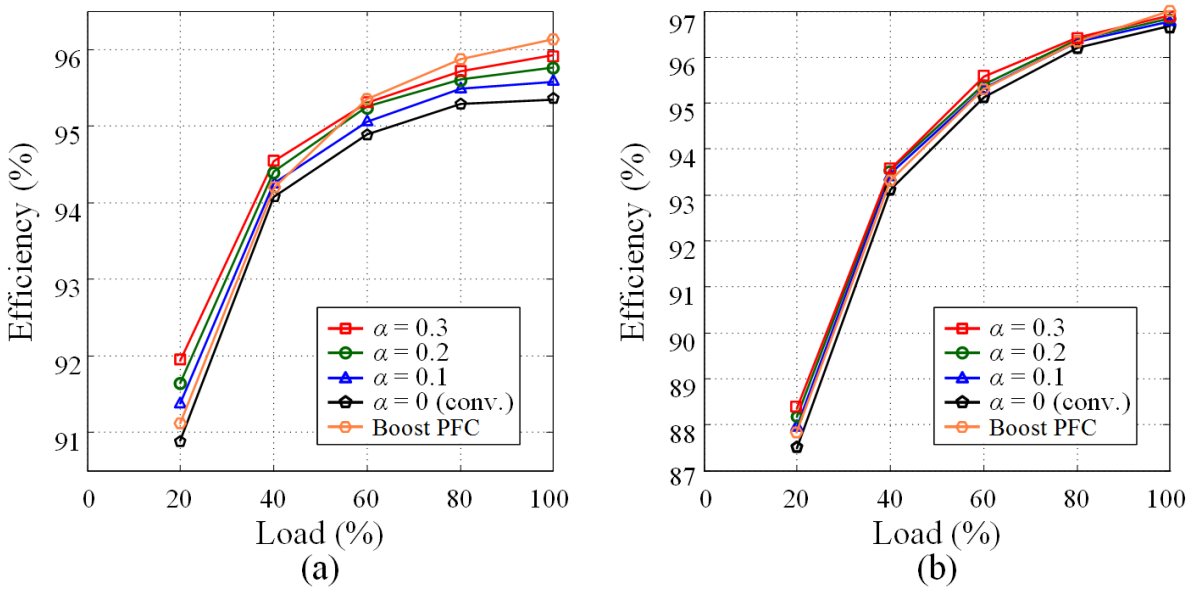


Fig. 3-21. Efficiency measurement by load. (a) 110 V_{rms} (b) 220 V_{rms}.

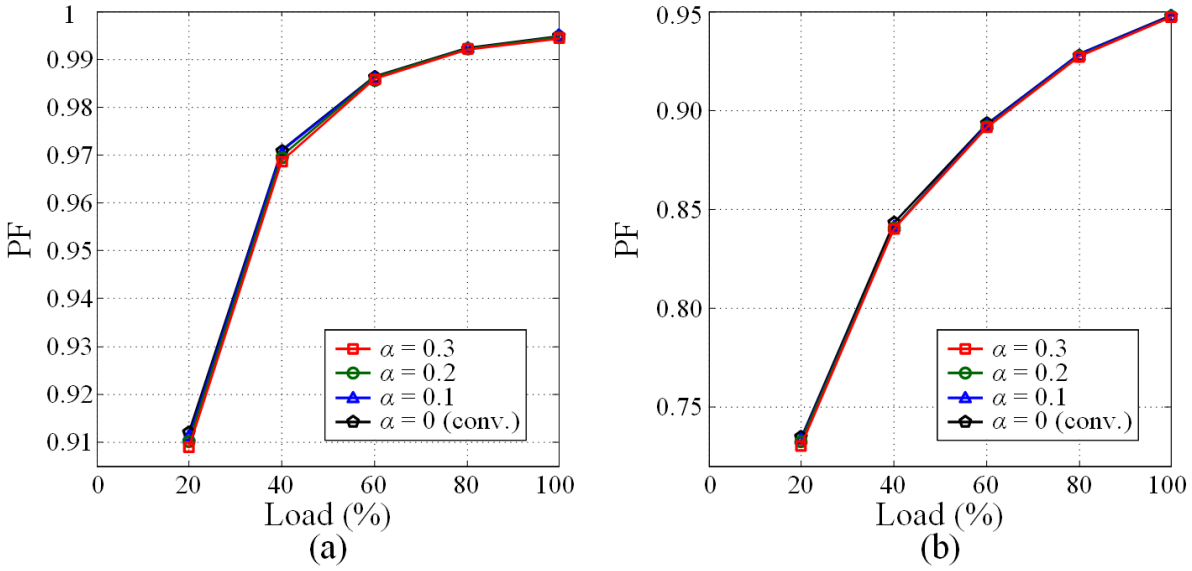


Fig. 3-22. Input PF measurement by load. (a) 110 V_{rms} (b) 220 V_{rms}.

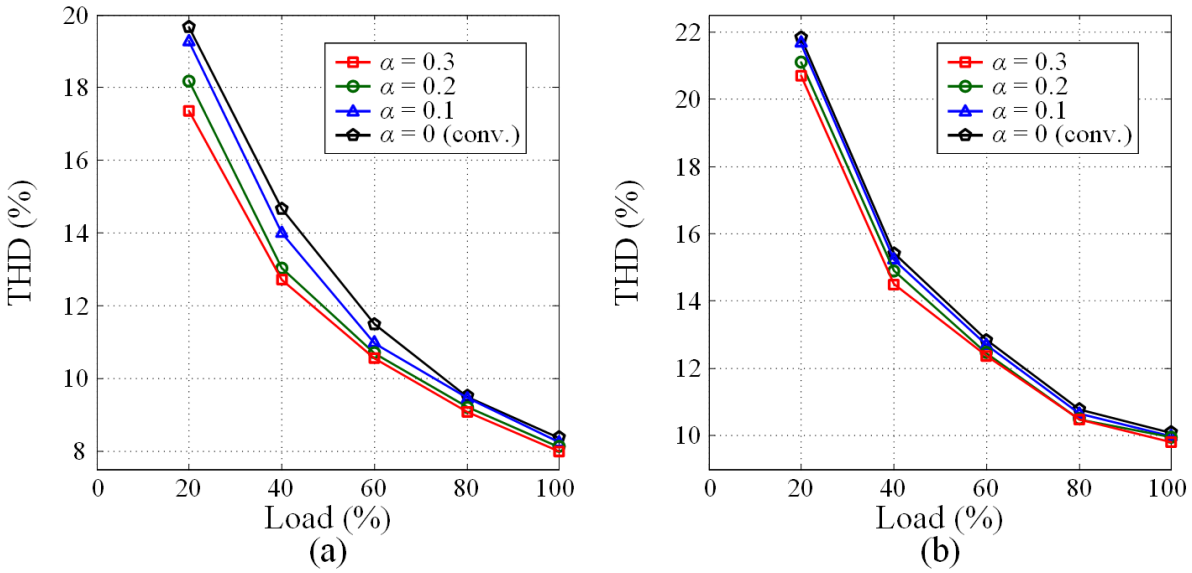


Fig. 3-23. THD measurement by load. (a) 110 V_{rms} (b) 220 V_{rms}.

As shown in Fig. 3-21, measured efficiency of TLB PFC with conventional two-level modulation case (α=0) becomes worse as load condition goes lighter. It is mainly due to the fact that variable switching frequency of CRM operation goes very high, especially going up

to 850 kHz range at 20% load. Accordingly, switching losses from switches and inductor are dominant among major losses. However, by using non-zero α in the proposed three-level control scheme, the switching frequency and turn-off peak current decrease so that converter efficiency can be improved. Overall, at 110 V_{rms} input condition, more than 0.5% improvement is measured and 1.2% improvement is observed for light load in α=0.3 case. At 220 V_{rms}, efficiency is increased by more than 0.3% in entire load range and by 1% at light load condition. Comparison with boost PFC converter is also conducted using one boost cell of the TLB prototype. In summary, TLB PFC with α>0.1 shows better efficiency at light load than boost PFC for both input voltage conditions; at 220V_{rms}, full-load efficiency with α=0.3 is almost comparable to that of boost PFC. Entirely, the measured efficiency at 110 V_{rms} shows better results than 220 V_{rms}; it is mainly because 110 V_{rms} is always working in Mode I so that ZVS+ZCS turn-on can be achieved. However, full-load efficiency at 110 V_{rms} is less than that of 220 V_{rms} due to significant diode conduction losses by high current conditions.

Input PF curves in Fig. 3-22 confirm that trade-off of the proposed three-level CRM control scheme is decrement of input PF. However, as recommended in the analysis, properly limited α range can avoid severe input PF drop. By using α-ratio up to 0.3 for the prototype experiments, the decrements of input PF in both input voltages are less than 0.4% compared to the two-level triangular modulation case (α=0).

THD of input current plotted in Fig. 3-23 shows good agreement with the analysis that expected improvement of THD due to the reductions of peak inductor current and corresponding peak harmonic contents. The effectiveness becomes noticeable at lighter load condition. Maximum differences of THD between α=0 and α=0.3 are 2.5% at 110-V_{rms}/60-W

condition and by 1.3% at 220-V_{rms}/60-W condition, respectively. Overall, improvements of THD results are observed in wide operation range by higher α setup in the proposed scheme.

3.9 Chapter Summary

In this chapter, a three-level CRM control scheme is proposed for TLB PFC. Different from conventional two-level triangular modulation, the proposed scheme fully utilizes three-level current-slope shaping capability in each switching cycle. By using the scheme, TLB PFC can be rewarded with reductions of switching frequency, peak current and switching losses as well as efficiency improvement. However, the degradations of input PF is shown as a trade-off, which limits the range of proposed scheme in terms of α. Thus, compensation method for input PF drop is needed to be considered as a future work. In addition, there is no special balancing method for two output-capacitor voltages except the T_α-mode toggling between S_1 and S_2. The unbalancing issue could surface with severe voltage difference as the load goes heavier and the operations in the two boost cells become more asymmetrical by higher α setting; also, at the lighter load, CRM switching frequency will be much higher than sampling frequency in DSP control unit. Thus, comprehensive works on balancing method with DSP utilization should be further studied.

Chapter 4.
Three-Level DCM Control Scheme with Adjustable On-Time

In this chapter, a three-level DCM control scheme is proposed for TLB PFC converter. The basic three-level current modulation in Chapter 2 is applied to fixed-frequency-based DCM control format with a feature of adjustable single-switch on-time t_α. By properly adjusting the duration of t_α in each fixed switching period, inductor currents can be synthesized in quadrangular waveforms and can work in the shape of CRM operations. Main advantages of the proposed scheme are that high peak inductor current in DCM can be sufficiently reduced to CRM level, while fixed-frequency DCM frame doesn't need to suffer from high switching losses of CRM operation even under light load condition. In brief, the proposed three-level DCM control scheme can have benefits of both DCM and CRM methods. Research background, operation principles, key equations, balancing scheme, and comparative analysis are included in this chapter. A set of prototype experiments is also delivered to support the proposal and analyses.

4.1 Background

As mentioned in the introductory chapter, the two ZCS control methods, DCM and CRM, have been widely employed in universal-line low-power applications due to no reverse-recovery issue and low-cost system design. Although both ZCD control schemes have been positioning in the similar application fields with overlapped roles, their characteristics are distinctly far from each other as summarized in Table 4-1.

Table 4-1. Characteristics of DCM and CRM.

	DCM	CRM
Switching frequency	Fixed	Variable
Peak current	Higher	Lower
High switching-losses operating region	Heavier load Lower input voltage	Lighter load Higher input voltage
Frequency spectrum	Concentrated	Distributed
DM-EMI amplitude	Higher	Lower
Filter design criteria	Simple	Complicated
Current sensing	Not required	External ZCD circuit

Major factors that bring those differences are switching frequency and peak current level. First, in terms of switching frequency, DCM works with fixed frequency while CRM experience inherently changing frequency. Variable frequency range of CRM goes higher when average input current becomes smaller. Thus, CRM operations suffer from high switching-related losses at lighter load and higher rms input conditions. Distributed EMI noises on frequency spectrum due to variable CRM frequency make input-filter design complicated. On the contrary, DCM operation can bring relative benefits from fixed frequency operation. It includes lower switching losses and higher efficiency for wide-range load conditions, and definite input-filter design criteria due to fixed frequency spectrum.

Second, for peak current level, DCM operation experiences higher peak inductor current in a switching cycle than CRM, under same operating condition. Accordingly, current stresses of DCM PFC are higher and larger turn-off losses are expected by high turn-off current at heavier loads. Higher peak current also causes large DM-EMI amplitudes; furthermore, dense

frequency spectrum of DCM PFC at one frequency makes EMI noises much larger than CRM PFC which has inherent spread spectrum. On the other hand, CRM PFC shows relative strength in lower current stress and DM-EMI amplitudes.

For many years, there have been performance improvements on efficiency, input PF and THD of DCM and CRM PFCs, separately. Then, recently, research attempts have been made to get the operational merits of both ZCS methods at the same time [69]–[72]. In [69], variable on-time t_{on} feedforward was devised for conventional boost CRM PFC to obtain fixed switching frequency. The control method [69] achieved fixed-frequency-based CRM PFC operation for the first time and rewarded with efficiency improvement and reductions of peak current, switching losses and output voltage ripples. However, inductance L is required to change depending on input rms voltage conditions and input PF drops significantly as a trade-off. To solve the issues, two different approaches were tried in [70]–[71]. In [70], variable inductance circuit and control method were proposed for boost CRM PFC; the method can provide real-time changing inductance in response to wide input voltage variation, which was physical issue of [69]. In [71], switching-frequency optimization control based on harmonic content analysis was introduced to compensate input-PF drop in [69] which became severer at higher input voltages. By the method, fixed-frequency CRM operation becomes quasi-constant frequencies in limited range and PF was improved. In [72], to reduce high peak inductor current and increase input PF in boost DCM PFC, boundary inductance control with optimized third/fifth-order harmonics was facilitated; DCM operations in [72] achieved not only improvements of input PF and efficiency, but also reduction of peak inductor current, device current stresses and turn-off losses.

The state-of-the-art researches in [69]–[72] were able to attain merits of both DCM and CRM by realizing fixed frequency operation and reduced peak current with minimum PF drops. However, highly distorted input current at higher input-voltage condition by third harmonics was found in common; the common tendency is plotted in Fig. 4-1.

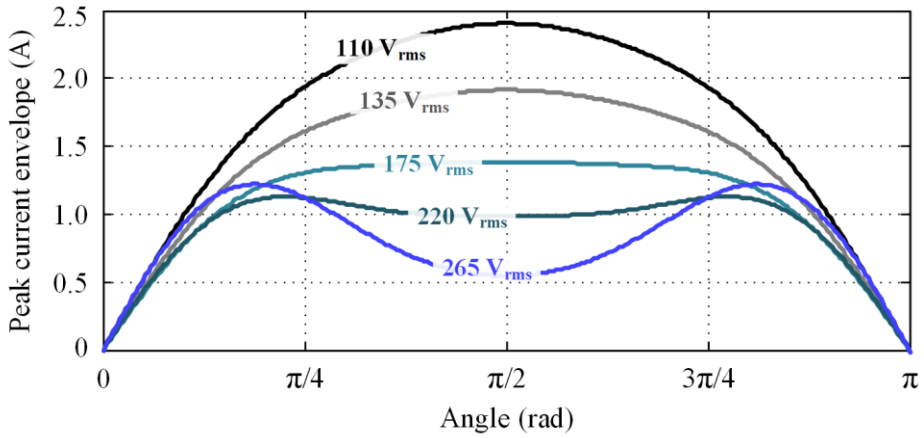


Fig. 4-1. Input current distortion by input rms voltage [69]–[72].

Due to the distortions by harmonic contents, test ratings of boost DCM/CRM PFC experiments in [69]–[72] were limited to 120 W, not to violate the third-harmonic limit of IEC-61000-3-2 Class-D (<600 W) standard [73]–[74]. The main reason is originated from lack of degree-of-freedom in those conventional two-level boost PFC controls. As demonstrated in Fig. 4-2 of the next page, boost PFC in DCM and CRM is controlled by the on-time T_{on} of main switch and there is no other control option unless the passive diode in topology is replaced by active switch. Thus, with the limited control variable T_{on}, the researchers in [69]–[72] had to optimize T_{on} by calculation and feedforward it.

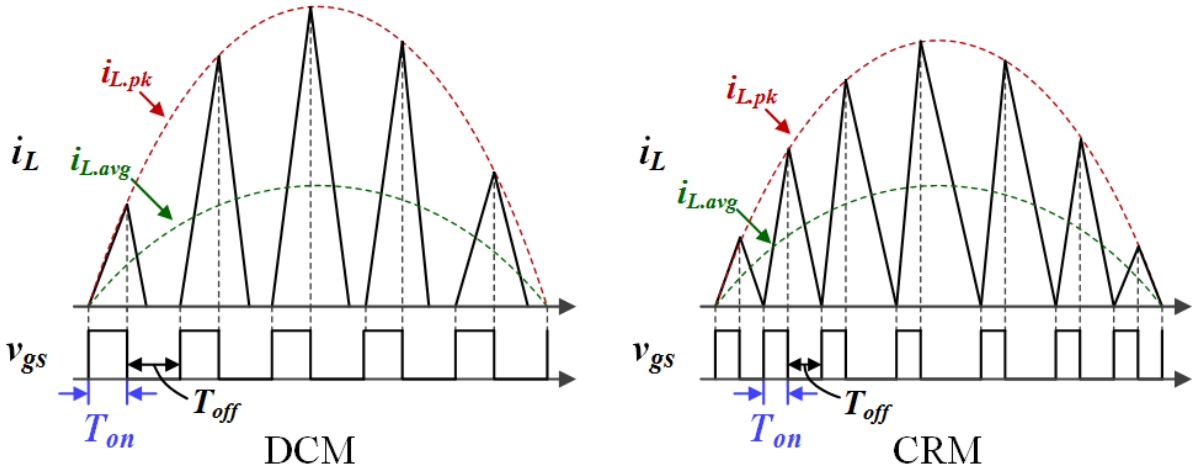


Fig. 4-2. DCM and CRM modulations of two-level boost PFC.

In order to maintain fixed-frequency period, however, T_{on} should be longer enough at lower input region and shorter at higher input region for both DCM and CRM operations. By the mechanism, third-harmonic-oriented distortion in Fig. 4-1 is inevitable while keeping PF at certain level.

In this chapter, following the research trends in [69]–[72], a fixed-frequency three-level current control for TLB PFC is proposed. The proposed method also aims to get the merits of fixed switching frequency and reduced peak current, based on the three-level current modulation scheme introduced in Chapter 2. For a given fixed switching period, the new method calculates required duration of single-switch on-time t_α in each switching cycle, not the common on-time T_{on}. And, it adjusts the duration to make inductor current in quadrangular CRM waveform of which non-zero durations are fitted to given switching period. At low input region like zero-crossing, however, it is natural for fixed-frequency TLB PFC to enter DCM. Thanks to the concurrent benefits of DCM and CRM, the proposed control can reduce switching losses and current stresses in wide-range input voltage and load conditions. In addition, it can satisfy harmonic limits of IEC-61000-3-2 up to 300W,

overcoming the power limitation of [69]–[72] due to third-harmonic distortion in two-level boost PFC. A simple voltage balancing approach is also included in the proposed three-level DCM control scheme. Operation principles, key equations, comparative analyses, digital implementation and experimental verifications are delivered step by step.

4.2 Proposed Three-Level DCM Control Scheme

In order to realize constant switching frequency, two-level DCM control scheme becomes a technical foundation of the proposed method. The fixed switching period is expressed by T_{sw}. The capital and lower-case letters present constant values and time-varying values, respectively. To explain the operation principles, two basic assumptions are introduced as below.

1) A switching period T_{sw} is much shorter than ac line period T_1. Thus, in each switching cycle, it can be assumed that input voltage v_{in} remains constant.

2) Output voltage V_o is regulated by slow-dynamic voltage compensator. The compensator results in common on-time T_{on} which remains almost constant for ac line cycles.

Based on the underlying assumptions, key waveforms of the proposed three-level DCM control scheme are shown in Fig. 4-3; in the figure, four switching cycles are shown before and after $v_{in}=V_o/2$. The key concept of proposed operation is simple. In each sampling period, DSP control unit receives sensed input and output voltages, and generates the common on-time T_{on} by running feedback voltage compensator; then, required duration of single-switch on-time t_α for each switching period can be calculated based on the given information.

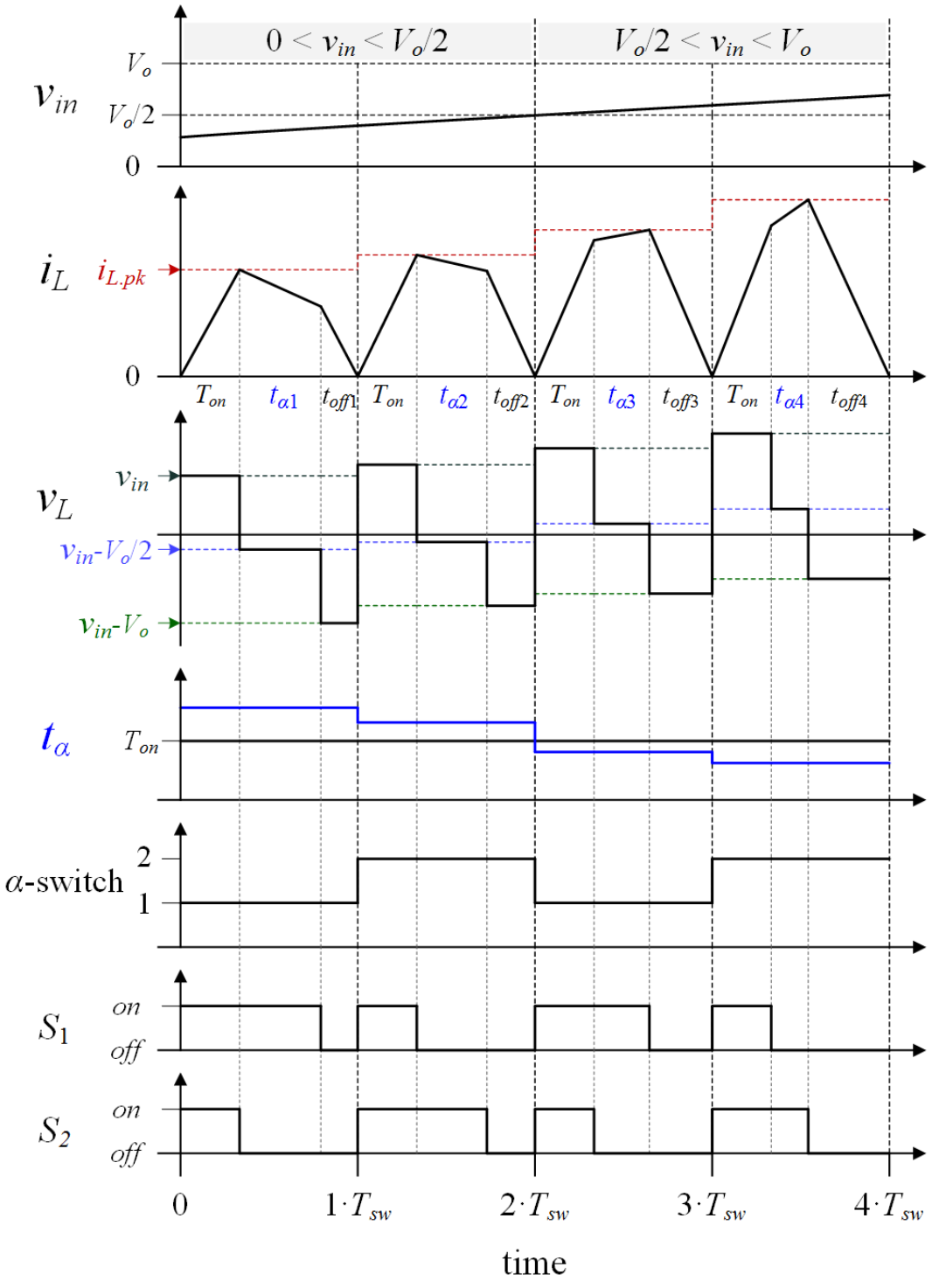


Fig. 4-3. Key waveforms of proposed adjustable three-level DCM control scheme.

By doing so, zero-crossing moment of descending inductor current can be matched to the end of fixed switching period T_{sw}. It can be noted from Fig. 4-3 that the concept of adaptive t_α can obtain quadrangular CRM-shaped waveforms under the varying input conditions. The three-level DCM control scheme consists of three inductor-current slopes in one switching cycle: v_{in}/L for T_{on}, $(v_{in}-V_o/2)/L$ for t_α and $(v_{in}-V_o)/L$ for t_{off}, respectively. The current slope in each step changes as input voltage varies. Especially for the slope in t_α duration, the polarity of $(v_{in}-V_o/2)$ can be either positive or negative depending on the input voltage range.

Fig. 4-3 shows that conducted switch in single-switch on-time t_α durations is toggled between S_1 and S_2 by turns, as the same approach with balancing attempt for CRM control in Chapter 3. The main purpose is to mitigate unbalancing phenomenon between output capacitor voltages v_{C1} and v_{C2}. However, only with the toggling approach, it is practically hard to achieve voltage balancing for the proposed DCM control scheme. It is because the duration of t_α goes much longer than that of three-level CRM case (e.g. α=0–0.3) in order to match the zero-crossing point of i_L to the end of T_{sw}, causing more asymmetry between the two boost-cell operations. Thus, for the proposed DCM control scheme, additional simple balancing method will be added later in this chapter.

The concept of adjustable t_α control can bring fixed-frequency CRM-shaped current to TLB DCM PFC. However, at low input voltage such as near zero-crossing point, it is hard to avoid discontinued current as Fig. 4-4. It is mainly because peak inductor current which is high enough for synthesizing quadrangular current cannot be built up by the low input voltage v_{in}. For that low input region, even the descending current slope of $(v_{in}-V_o/2)/L$ in t_α duration is too steep and inductor current reaches at zero quickly after one switch turns off. Zero inductor current continues clamped until the next switching cycle begins.

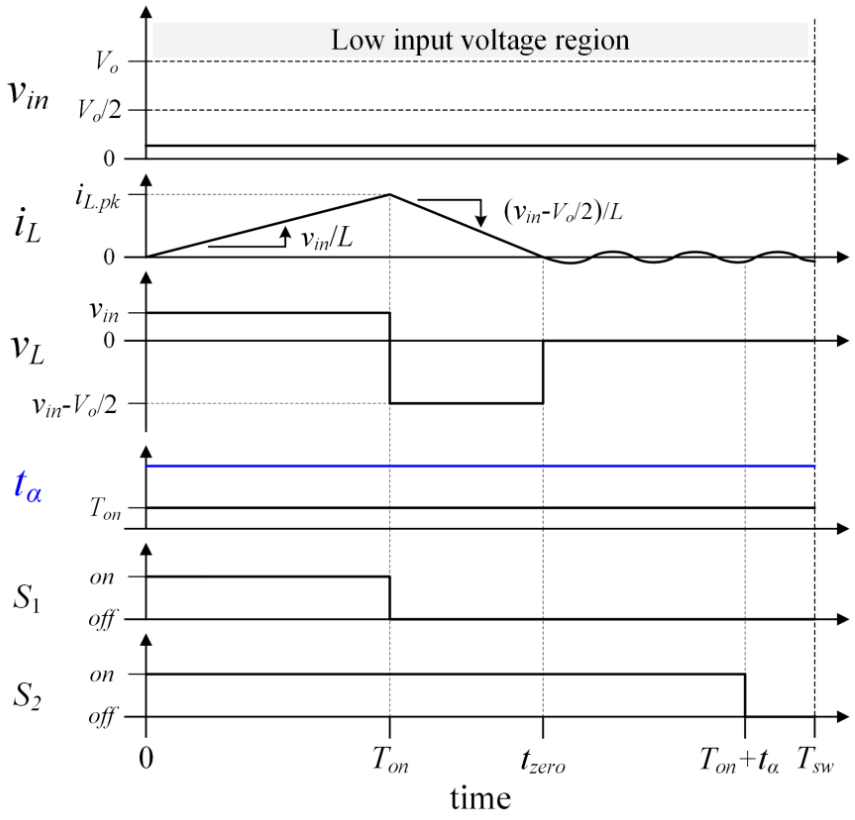


Fig. 4-4. DCM operation at low input-voltage condition.

In summary, TLB PFC with the proposed three-level DCM control scheme will experience both DCM and CRM depending on input voltage variation. The key equations including DCM/CRM boundary condition are derived in the following section.

4.3 Key Equations

In Fig. 4-5, waveforms in a switching period are shown by input voltage range to derive key equations. In the plots, it is assumed that required single-switch on-time is calculated and provided to control unit as reference t_α^*; common on-time T_{on} is resulted from slow-dynamic voltage compensator and remains almost constant during line cycles.

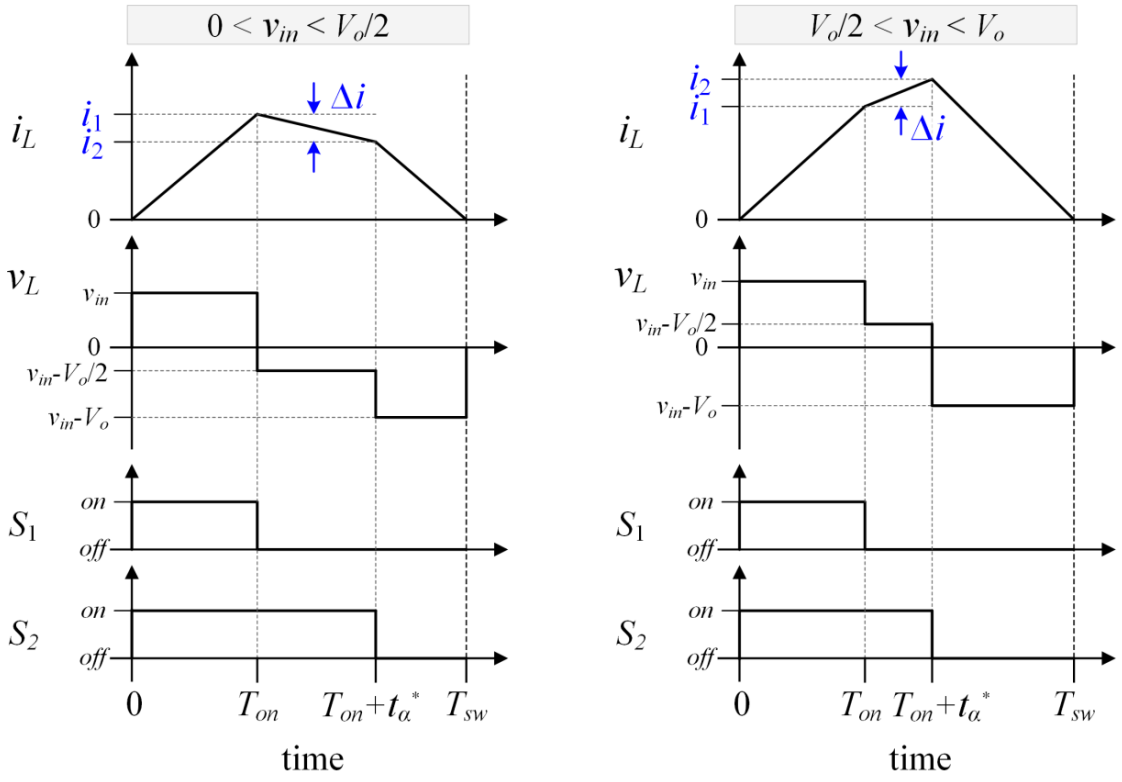


Fig. 4-5. Waveforms for derivation by input voltage range.

Based on the assumption, TLB PFC can achieve three-level CRM-shaped current in the quadrangular form which is fitted to given switching period T_{sw}. by the modulation. In order to derive a correct equation for calculating the reference t_α^*, three inductor-current variables (i_1, i_2 and Δi) are defined in Fig. 4-5; where i_1 is the inductor current after T_{on}, i_2 is the inductor current after $T_{on}+ t_\alpha^*$, and Δi is the absolute difference between i_1 and i_2, respectively.

First, for both Mode I and Mode II, the variables i_1 and Δi can be expressed by (28)–(29).

$$i_1 = \frac{v_{in}}{L} \cdot T_{on} \tag{28}$$

$$\Delta i = |i_1 - i_2| = \frac{|(v_{in} - V_o/2)|}{L} \cdot t_\alpha^* \tag{29}$$

Second, the magnitude of i_2 can be computed by descending amount to zero in the common off-time period as follows.

$$i_2 = \frac{V_o - v_{in}}{L} \cdot \left(T_{sw} - T_{on} - t_\alpha{}^* \right) \tag{30}$$

From the inductor current waveforms in Fig. 4-5, the value of i_2 can be also calculated by (31) depending on the input voltage range.

$$i_2 = \begin{cases} i_1 - \Delta i & \text{, Mode I} \\ i_1 + \Delta i & \text{, Mode II} \end{cases} \tag{31}$$

By replacing (31) with (28) and (29), the key equation of reference $t_\alpha{}^*$ for quadrangular CRM-shaped current can be derived in common as (32).

$$t_\alpha{}^* = \frac{\left(V_o - v_{in} \right) \cdot T_{sw} - V_o \cdot T_{on}}{V_o / 2} \tag{32}$$

As can be noted from the equation, all the variable information can be provided to DSP control unit in each sampling cycle by measurement and compensator routine. For example, v_{in} and V_o can be measured by voltage sensors, T_{on} comes from feedback voltage compensator, and T_{sw} is a pre-determined system specification.

Therefore, the proposed three-level DCM control scheme can easily calculate proper duration of $t_\alpha{}^*$ by (32) and add it up on top of the constant common on-time T_{on} in each switching period. Accordingly, TLB PFC is able to synthesize quadrangular CRM-shaped currents with fixed switching frequency at the sufficient input voltage level.

As described in Fig. 4-4, however, TLB PFC inevitably enters DCM at the vicinity of low input voltage because peak current level is too low to maintain non-zero current until the end of switching period. Thus, boundary condition between DCM and CRM-shaped currents is needed to be analyzed under given specifications. Since the proposed control scheme is based on the DCM control framework, calculation of average T_{on} in two-level DCM control should be preceded and then extended to three-level control. The average equation of T_{on} for two-level DCM control scheme can be expressed by (33), which was already proven in [75].

$$T_{on.2L} = \frac{T_{sw}}{V_{in.pk}} \sqrt{\frac{2\pi f_{sw} L P_o}{\int_0^{\pi} \frac{\sin^2\theta}{\left(1-\frac{V_{in.pk}}{V_o}|\sin\theta|\right)} d\theta}} \tag{33}$$

where $V_{in.pk}$ is the peak of ac input voltage and θ is the angle of ac input voltage, respectively. In order to supply same amounts of input current and input power, the area of inductor current in each control scheme should be mathematically equal. Thus, by assuming the equal area of current waveforms in two-level DCM and three-level DCM, the average value of T_{on} in the three-level control can be derived to (34) using $T_{on.2L}$.

$$T_{on.3L} = \left(\frac{V_o}{V_o - V_{in.rms}} \cdot \frac{T_{on.2L}}{T_{sw}} \right) \cdot T_{on.2L} \tag{34}$$

where $V_{in.rms}$ is the input rms voltage. All the operating conditions such as input and output voltages, switching frequency, inductance and power level are all reflected in (34). With the derived $T_{on.3L}$, boundary condition of the proposed three-level DCM control scheme can be analyzed. As drawn by black line in Fig. 4-6, the boundary condition is a moment when descending current with $(v_{in}\text{-}V_o/2)/L$ slope can meet zero at the end of switching period T_{sw}.

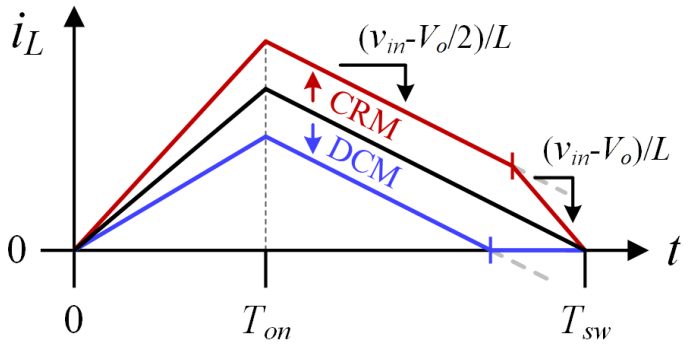


Fig. 4-6. Boundary condition of DCM and CRM operations.

If input voltage can build up higher peak current than that of black line within $T_{on.3L}$, the calculated reference t_α^* by (32) can synthesize three-level CRM current as red line in Fig. 4-6; if the peak current is lower than that of boundary black line, inductor current will enter DCM in the switching period. Under given specifications, the boundary condition in each switching cycle can be derived as (35).

$$\begin{aligned} \frac{v_{in}}{V_o} &< \frac{\left(T_{sw}-T_{on.3L}\right)}{2T_{sw}}, \quad \text{DCM} \\ \frac{v_{in}}{V_o} &> \frac{\left(T_{sw}-T_{on.3L}\right)}{2T_{sw}}, \quad \text{CRM} \end{aligned} \tag{35}$$

When TLB PFC with the proposed three-level control scheme works in low voltage and DCM operation, it can have lower peak current and longer conducting duration than conventional two-level DCM under same specifications, as displayed in Fig. 4-7. As can be seen, the reduction of peak current in three-level DCM is enabled by its slower descending current-slope than that of conventional two-level DCM control.

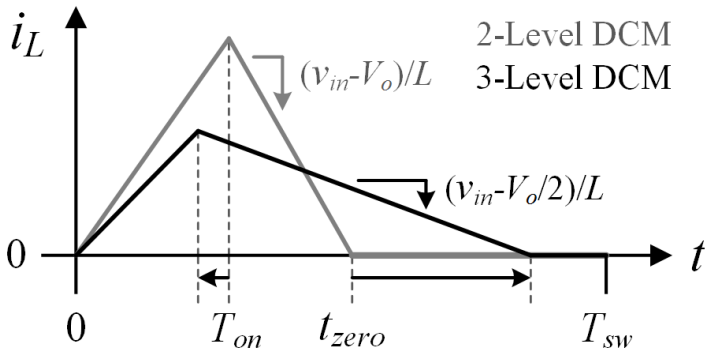


Fig. 4-7. Comparison of two-level and proposed three-level DCM methods.

With those mathematical derivations, two example cases of the proposed three-level control scheme are shown by different input rms voltages in Fig. 4-8.

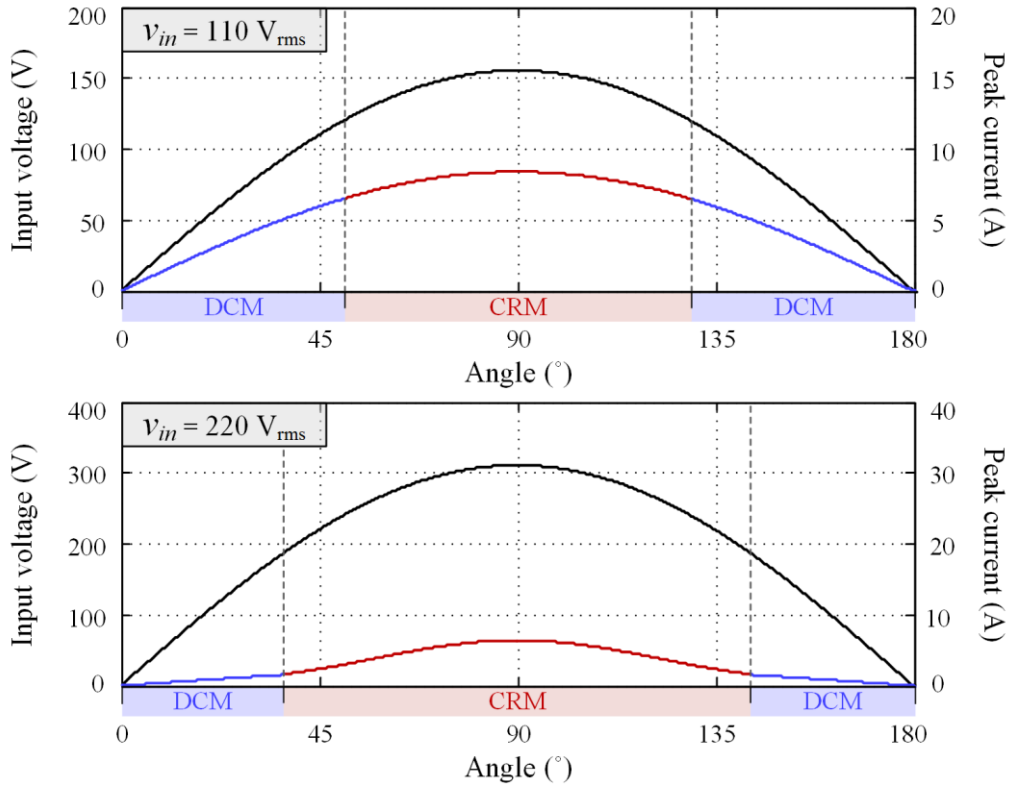


Fig. 4-8. Boundary plots in a half-line cycle at 300-W load condition.

110/220 V_{rms} are used as input voltages for analysis and verifications because the two voltages are the most widely-used universal voltages. In Fig. 4-8, peak inductor-current envelopes are shown in colors for both input voltages with 230-μH inductance, 400-V output voltage and 300-W load conditions. As can be seen from the plots, DCM/CRM boundary conditions of the proposed three-level control scheme can be affected by following factors.

1) **Power level:** The duration of CRM zone in red color will be shortened if average/peak input currents are reduced by lower power level. It is because low current level cannot maintain non-zero inductor current until the end of switching period.

2) **Input voltage:** With higher input voltage condition (e.g. Mode II), the duration of CRM in red color can be extended and longer than that of lower input case (e.g. Mode I). It is due to fact that t_α^* duration can increase peak inductor current further by $(v_{in}-V_o/2)/L$ slope if input voltage is high enough to satisfy $v_{in}>V_o/2$ (Mode II).

After all, for both 110 V_{rms} and 220 V_{rms} at full-load condition in Fig. 4-8, the maximum peak inductor current can remain in CRM operations so that the beneficial effects of fixed-frequency and reduced peak current (e.g. low current stresses, switching losses and DM-EMI) are valid in TLB PFC.

4.4 Comparative Analysis

In order to grasp the advantages of proposed three-level DCM control scheme, comparative assessments with two-level DCM control and three-level CRM control in Chapter 3 are made in terms of peak current, switching frequency and loss analysis. For comparison, specifications are given as v_{in}=110/220 V_{rms}, L=230 μH, and P_o=60–300 W.

First, peak inductor current $i_{L.pk}$, which has influences on device current stresses, turn-off losses and DM-EMI, is compared. In Fig. 4-9, peak inductor current envelopes at full load by the three control schemes are shown in a half line-cycle angle.

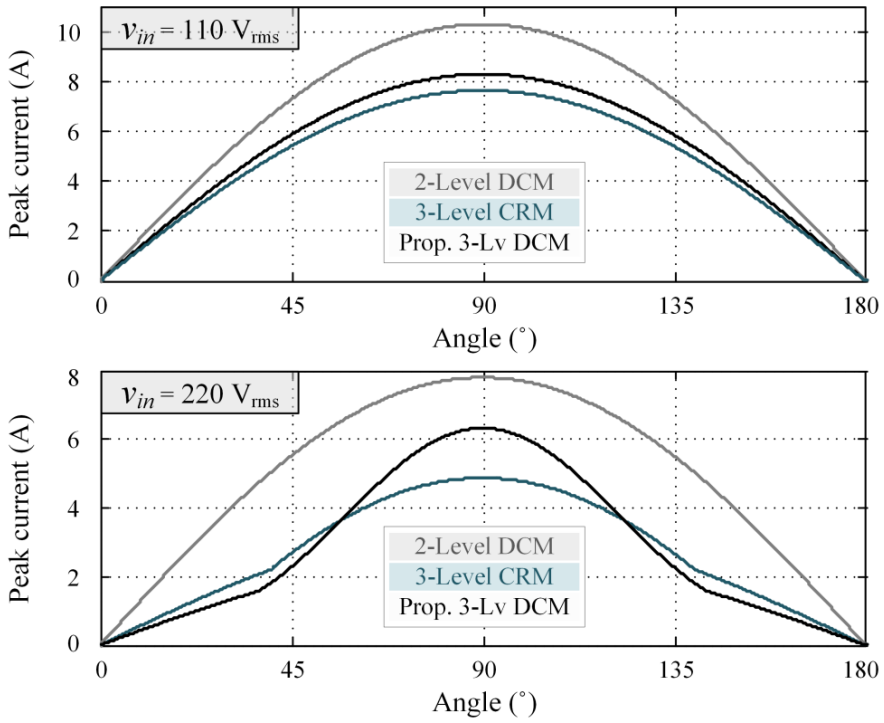


Fig. 4-9. Peak-envelope plot of inductor current by control method.

As shown in the plots, the peak envelope by the proposed three-level DCM control is definitely lower than that of two-level DCM control regardless of input rms voltages. The lowest peak envelope is recorded by the three-level CRM control scheme with fixed α=0.3. The proposed DCM control shows in-between peak value among three and highly reduced envelope close to the three-level CRM in 110 V_{rms} input condition.

As the second criteria, switching frequency range of each control method is displayed in Fig. 4-10. The variable frequency of three-level CRM in Chapter 3 shows the minimum frequency 36.5 kHz at the maximum current under 110 V_{rms} input condition.

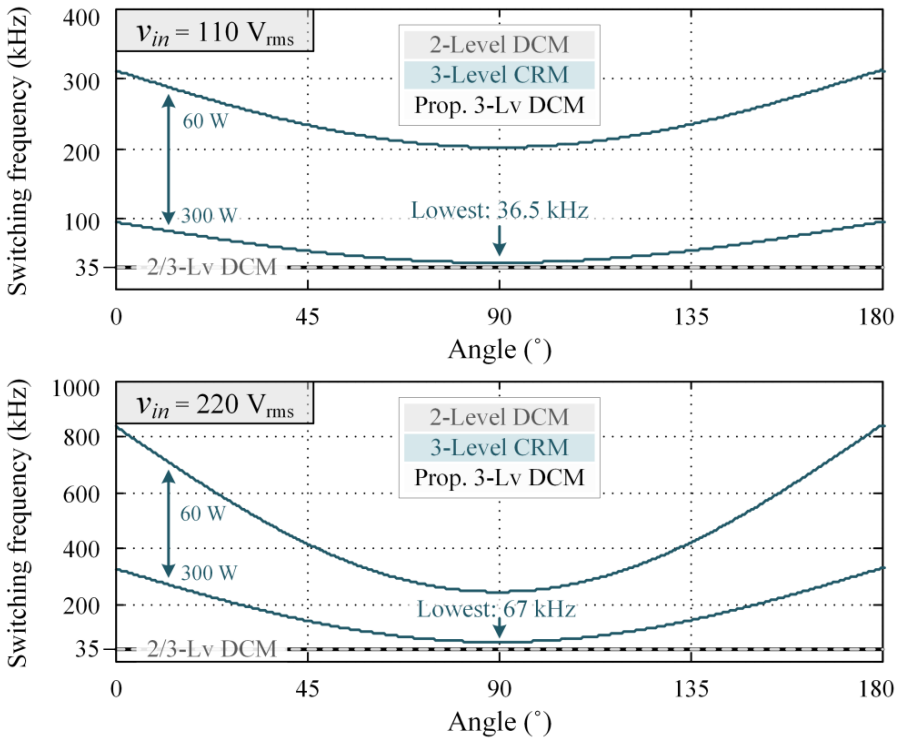


Fig. 4-10. Switching frequency plot by control method.

Based on the minimum frequency of CRM scheme, the switching frequency of two-level and three-level DCM control schemes must be set less than 36.5 kHz with the same inductance condition. Thus, 35 kHz frequency is used for the two DCM cases in the analysis and experiments. Irrespective of operating conditions, both the DCM control schemes can always operate TLB PFC with lower switching frequency than the three-level CRM control. The variable frequency of CRM control gets higher as input current goes lower. As shown in Fig. 4-10, the three-level CRM method has higher frequencies at lighter load (60 W) and higher input voltage (220 V_{rms}) conditions.

The mentioned two factors have significant impacts on component stress, losses and efficiency. Thus, loss analysis is also conducted for the three control methods. TLB PFC has four major lossy components: inductor L, switches S_1–S_2, diodes D_1–D_2 and diode-bridge-

rectifier (DBR). Each component x has switching-related loss $P_{x.sw}$ and conduction-related loss $P_{x.cd}$. Then, major losses can be summarized by the following equations.

$$P_{L.sw} = V_{core} \int_0^{T_1} A_{B-H} \, f_{sw} \, dt \tag{36}$$

$$P_{L.cd} = {I_{L.rms}}^2 R_L \tag{37}$$

$$P_{S.sw} \cong \int_0^{T_1} E_{off} \, f_{sw} \, dt \tag{38}$$

$$P_{S.cd} = {I_{S.rms}}^2 R_{ds.on} \tag{39}$$

$$P_{D.cd} = I_{D.rms} \cdot v_{F(D)} \tag{40}$$

$$P_{DBR} = I_{in.rms} \cdot v_{F(DBR)} \tag{41}$$

Switching losses of diodes and diode-bridge rectifier can be neglected because of no reverse recovery and ac line-frequency switching, respectively.

Based on the key loss equations in (36)–(41), loss analyses for the three control methods are conducted and the results are plotted in Fig. 4-11 by different input voltage and load conditions. It can be noted from the graphs that the conduction losses of diodes and DBR generally take 30-40% of the total losses, regardless of control schemes and operating conditions. In other words, main factors causing efficiency differences among the control schemes are the switching-related losses, especially from inductor ($P_{L.sw}$) and switches ($P_{S.sw}$). Those losses are function of switching frequency and peak turn-off current. Since the three-level CRM control scheme inherently faces very high switching frequency near 900 kHz at low input current as analyzed in Fig. 4-10, its switching-related losses become highly dominant at lighter load and higher input-voltage conditions. Thus, the total loss of three-level CRM control records the worst at 60-W load conditions of both 110 V_{rms} and 220 V_{rms}.

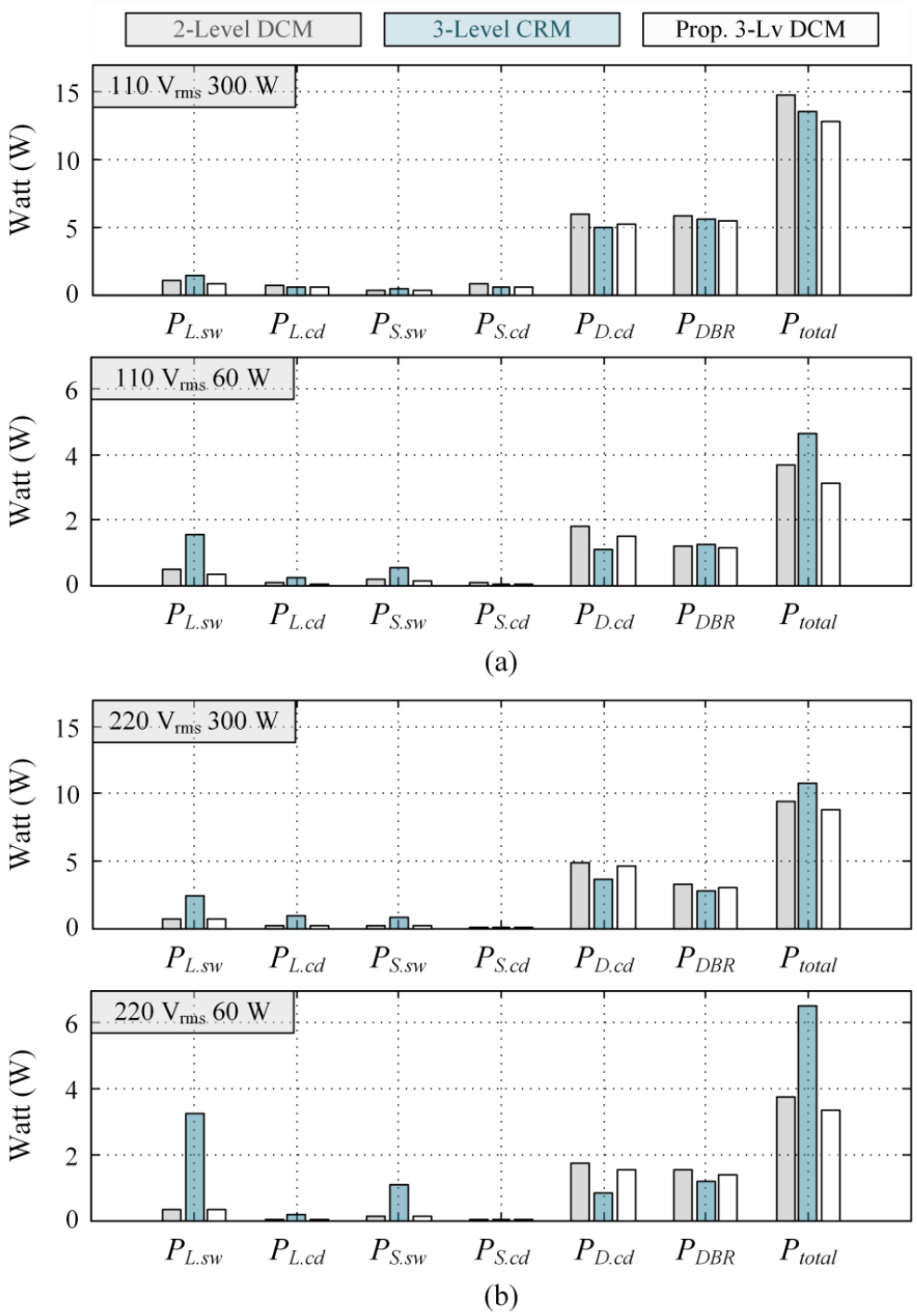


Fig. 4-11. Loss analysis by control method.

On the other hand, the two-level DCM control scheme has the highest peak and rms currents so that switching and conduction losses become considerable at heavy load conditions of both input voltage conditions.

Unlike the aforementioned two control methods, the proposed three-level DCM control can have the lowest losses for wide-range load and input voltage conditions. It is mainly possible because fixed-frequency operation and reduction of peak current of the proposed control allow TLB PFC to have the lowest switching losses than the other two methods.

4.5 Digital Implementation with Voltage Balancing Scheme

TLB PFC topology has two output capacitors and unbalanced output-capacitor voltages are practical issue which must be handled by control schemes. The root cause of unbalancing is tolerances of capacitance and equivalent series-resistance, generally 20% [76]. Due to the inescapable tolerance, TLB PFC even with symmetric two-level gate signals for S_1–S_2 shows voltage differences, as shown in Fig. 2-9; even the toggling of conducted switch in single-switch on-time duration cannot guarantee the balancing because charging and discharging amounts of the output capacitors cannot be exactly same for a full line cycle.

Therefore, in this section, a simple voltage balancing method that can be easily equipped to the proposed three-level DCM control scheme is introduced. The proposed control scheme can use a fixed-frequency sampling and control routine to check up unbalanced voltages and give asymmetric switching commands for balancing purpose. Using the fixed-frequency control framework, a devised balancing scheme is depicted in Fig. 4-12.

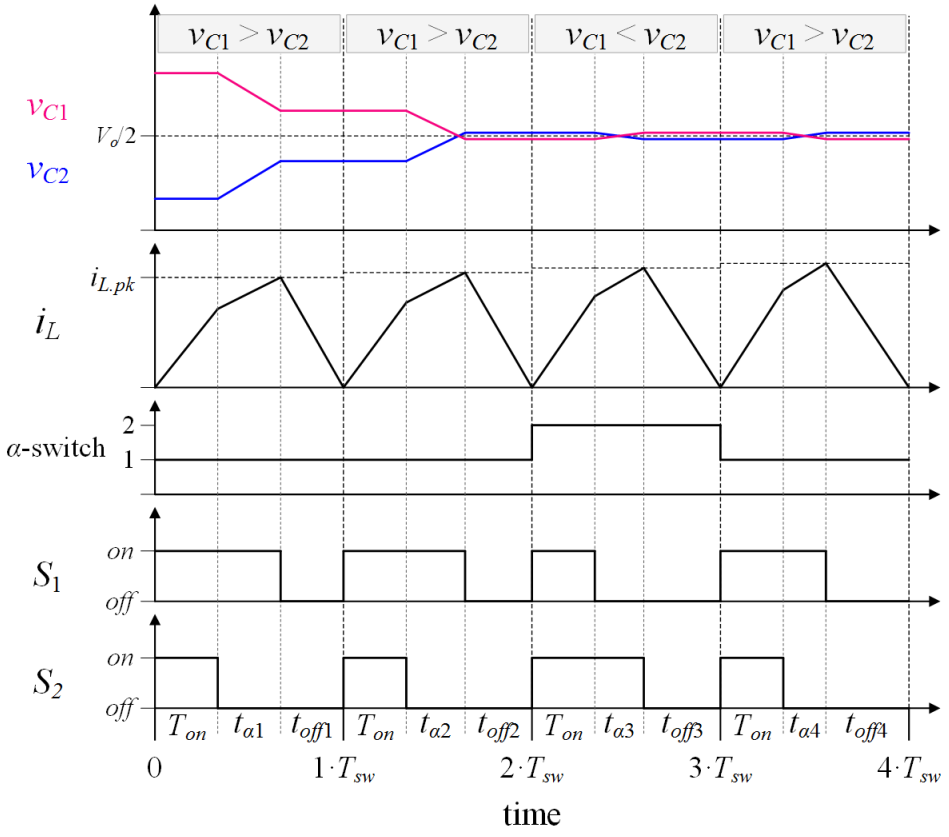


Fig. 4-12. Key waveforms of proposed voltage balancing scheme.

The balancing concept is to allow longer discharging period of t_α^* in an output capacitor of which voltage is higher than the other capacitor. A switch conducted further for t_α^* period will draw more discharging current through the output capacitor in the same boost cell. The mechanism can be found from single-switch turn-on states in Fig. 2-1. The principle of voltage balancing can be easily applied to the proposed control as following sequences ***1)***–***4)***.

1) The two capacitor voltages are measured in each sampling cycle and compared.

2) Higher capacitor voltage is defined to V_h as (42).

3) Required duration of t_α^* is calculated for quadrangular CRM-shaped current by (43) with the sensed V_h value.

4) The calculated t_α^* is applied to the switch in the higher-voltage boost cell by PWM action qualifier in DSP control unit.

$$V_h = \max\left(v_{C1},\, v_{C2}\right) \tag{42}$$

$$t_\alpha^* = \frac{\left(V_o - v_{in}\right)\cdot T_{sw} - V_o \cdot T_{on}}{V_h} \tag{43}$$

Compared to the key reference equation in (32), the denominator $V_o/2$ under balanced assumption is replaced by V_h. With the voltage balancing sequences, a control routine flowchart of proposed three-level DCM control scheme can be illustrated as Fig. 4-13.

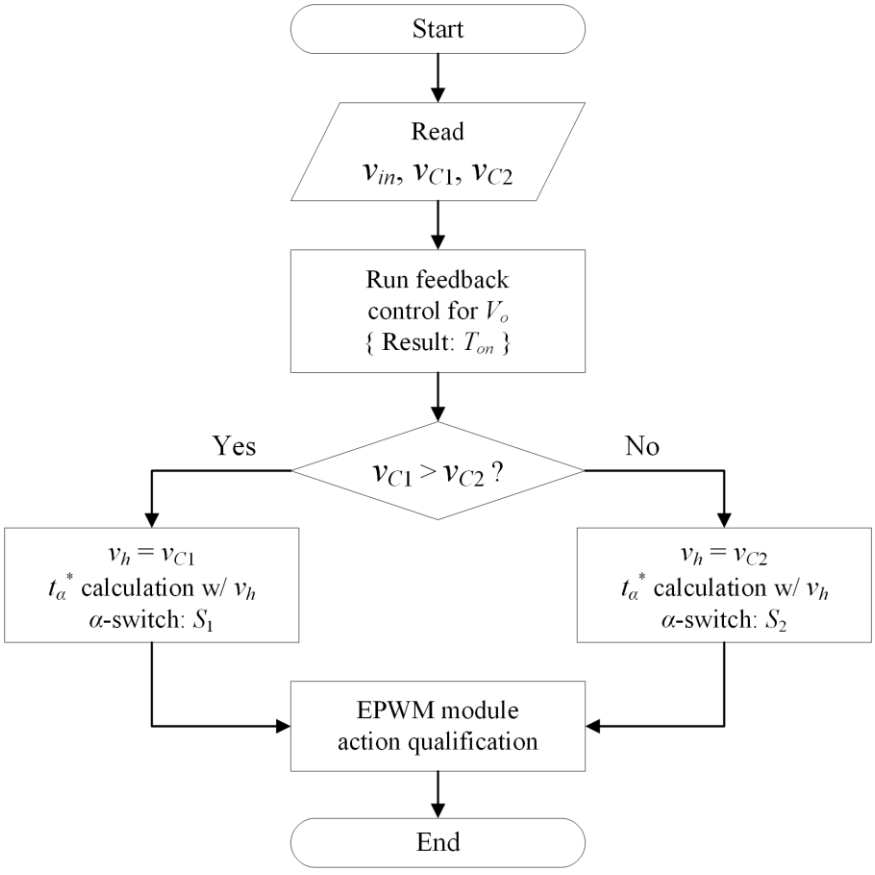


Fig. 4-13. Flowchart of proposed control with balancing scheme.

In this chapter, the common on-time T_{on} has been assumed constant by feedback compensator for V_o. Compensator design for the proposed DCM control scheme is very similar to that of three-level CRM control in Chapter 3 in terms of slow control-bandwidth at 1–5 Hz range. The transfer function required for three-level DCM control can be found from [6] which dealt with control design for conventional two-level DCM control scheme. For the experimental verification, the output voltage compensator was designed by the procedure of [6] in the PI form with the gains of K_p=3.18e-9 and K_i=1e-7. The closed-loop cross-over frequency and phase margin were 2.46 Hz and 75 degree, respectively. Accordingly, almost constant value of T_{on} for 60 Hz periods is easily obtainable and the total output voltage V_o is regulated to desired value.

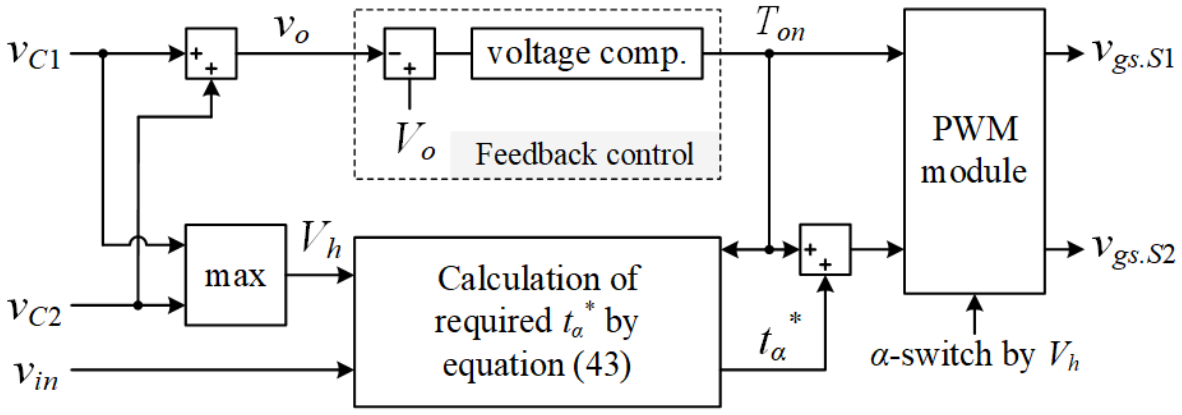


Fig. 4-14. Control block diagram of proposed there-level DCM control.

In summary, digital implementation of the proposed three-level DCM control scheme can be organized as a control block diagram in Fig. 4-14. Voltage measurement, output voltage compensation, and key t_α^* calculation with voltage balancing scheme for quadrangular current synthesization can be found part by part in Fig. 4-14.

4.6 Experimental Results

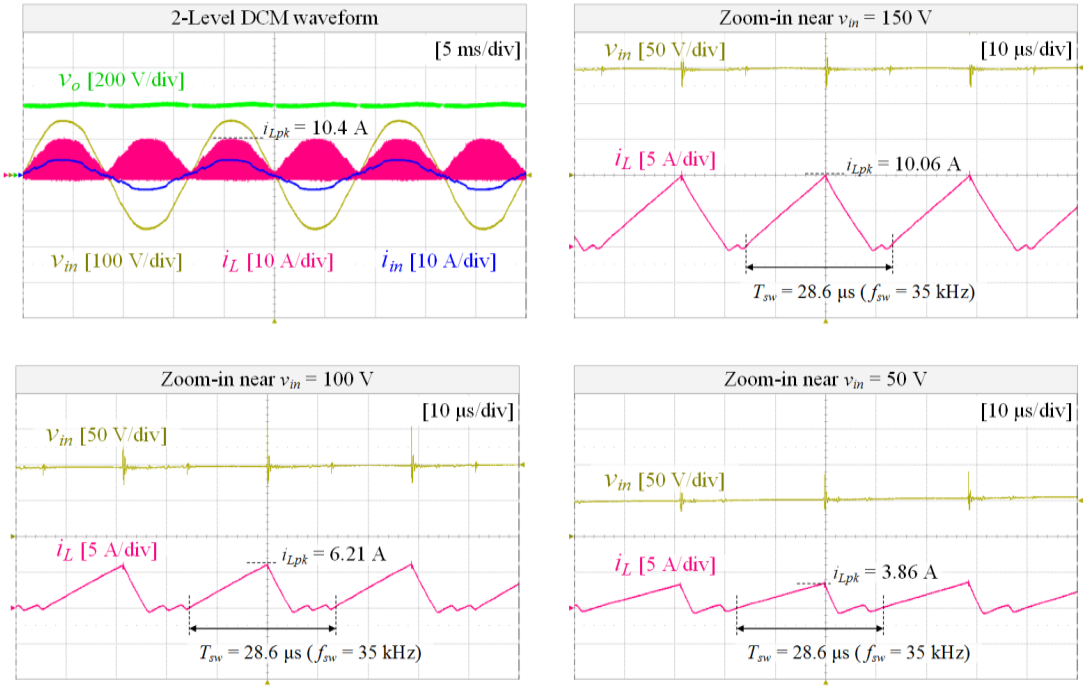
In order to prove the effectiveness of proposed three-level DCM control scheme and operational advantages, a 300-W prototype of TLB PFC is equipped with the control method and tested by a set of experiments. The prototype is the same one which was used for the experiments in Chapter 3. The experimental specifications are organized in Table 4-2.

Table 4-2. Experimental Specifications.

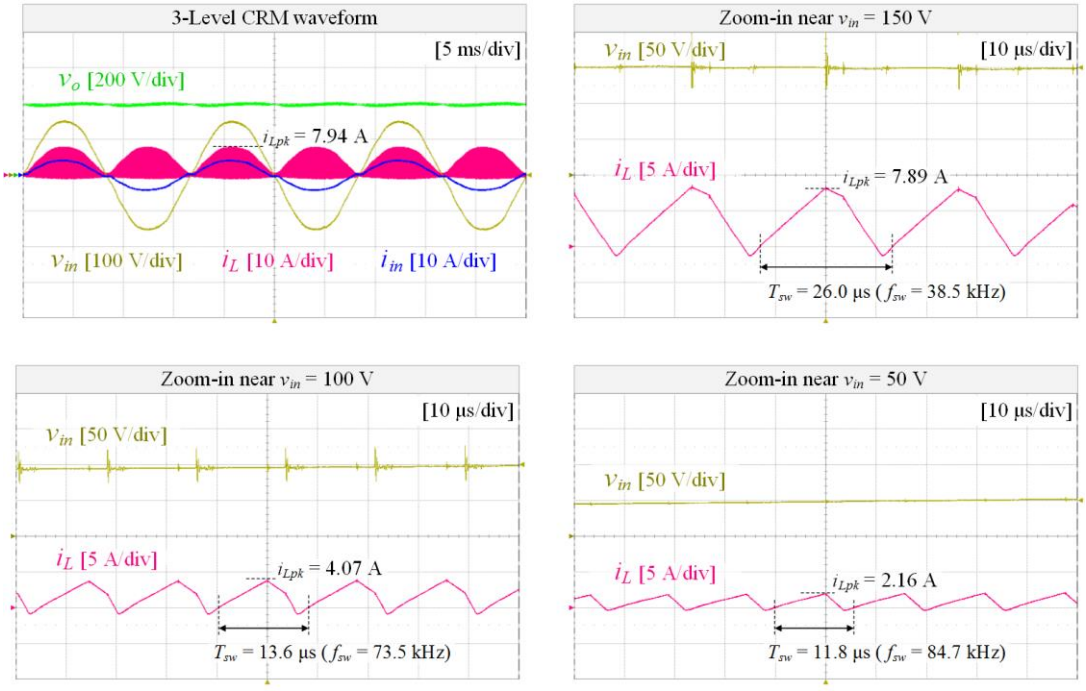
Input voltage	110/220 V_{rms}
Output voltage	400 V
Load	60–300 W (20–100%)
Switches (S_1, S_2)	IPW60R041P6 (C_{oss}=310 pF, $R_{ds,on}$=41 mΩ)
Diodes (D_1, D_2)	C4D10120D (v_F=1.4 V)
Inductance (L)	230 μH
Capacitance (C_1, C_2)	470 μF (measured: 403μF, 519μF)
DSP control unit	Texas instruments TMS320F28377D
Switching frequency	35 kHz (2/3-Lv. DCM), variable (3-Lv. CRM)
Sampling frequency	35 kHz

Two representative ac voltages 110/220 V_{rms} are used and power range from 60 W (20%) to 300 W (100%) is tested. A 230-μH inductance which was used for analysis and comparative assessment is adopted; a PI voltage compensator in the last section was implemented for output voltage control. To verify the operation merits of fixed-frequency operation and reduced peak current analyzed in section 4.4, the experimental results of proposed three-level DCM are compared to those of two-level DCM and three-level CRM with α=0.3 [59].

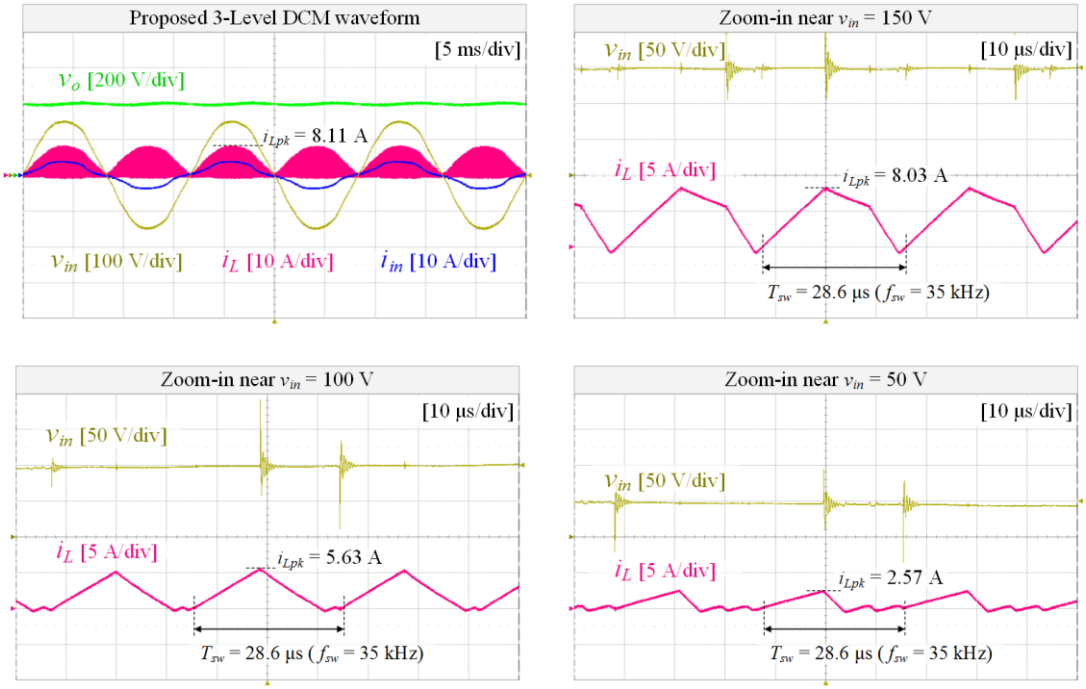
In Fig. 4-15, experimental waveforms of two-level DCM control, three-level CRM control and proposed three-level DCM control methods are shown for 110-V_{rms} (155-V_{pk}) input and 300-W load conditions. Overall view of input and output is shown in the first plot of each figure; zoom-in waveforms of inductor current near v_{in}=150 V, 100 V, and 50 V are also shown in order. As shown in the three overall-view waveforms in Fig. 4-15(a)–(c), TLB PFC prototype is able to achieve regulation on 400-V output voltage and certain level of input PF with all the three control methods. From the zoom-in waveforms, the two major factors can be compared.



(a)



(b)



(c)

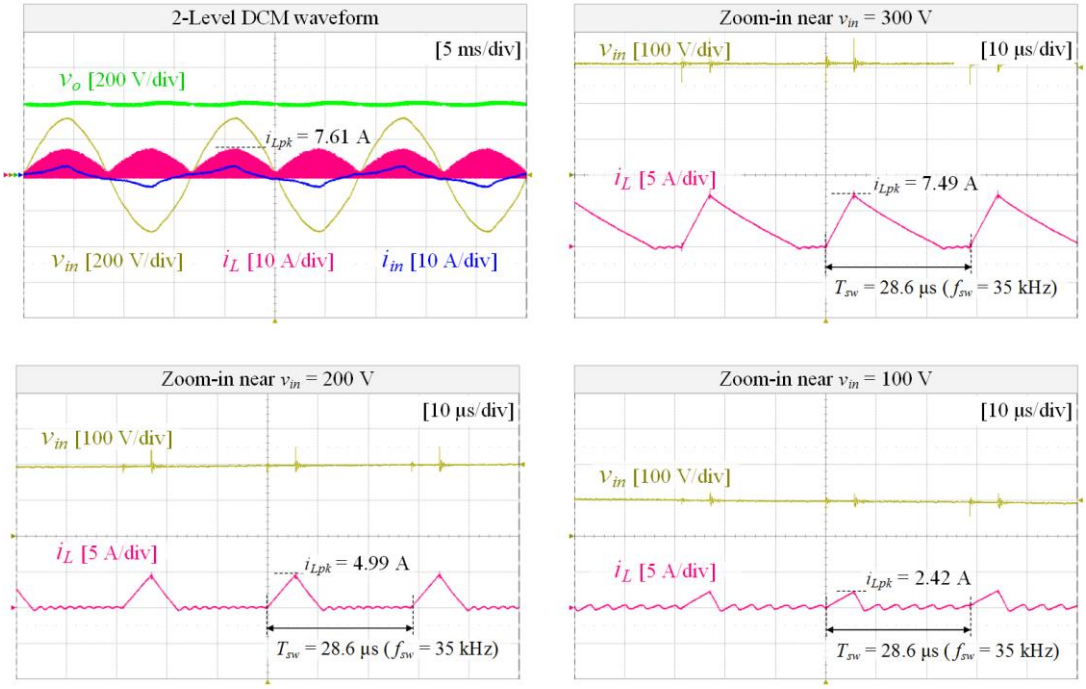
Fig. 4-15. Experimental waveforms at 110 Vrms with full load by control method.

(a) two-level DCM. (b) three-level CRM. (c) proposed three-level DCM.

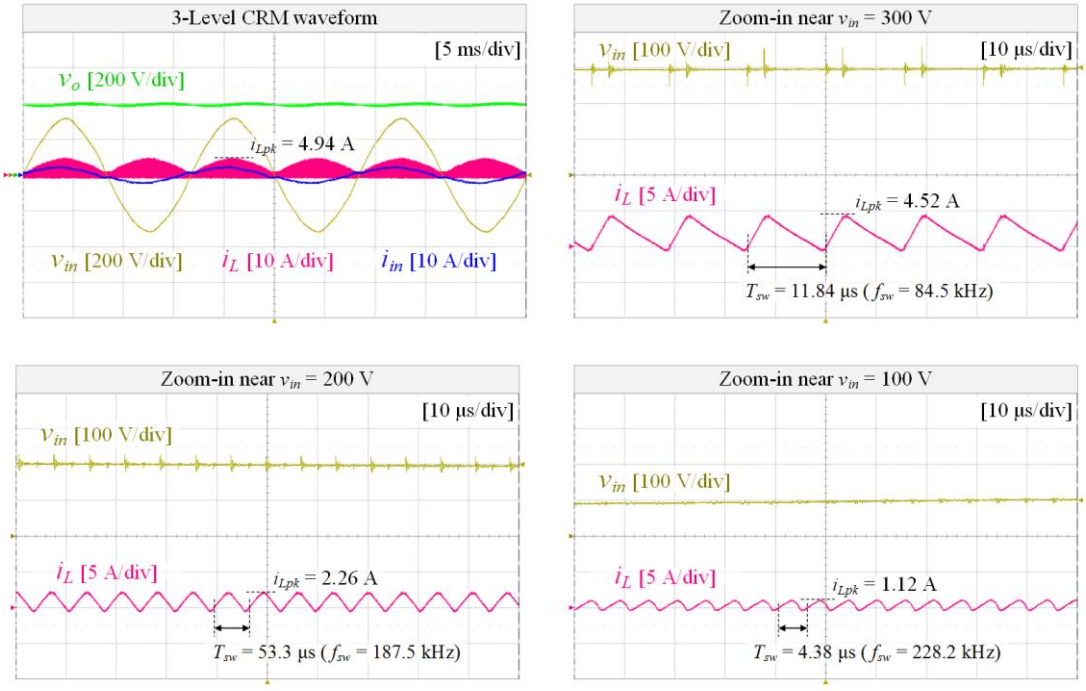
First, in terms of peak inductor current, two-level DCM control shows the highest 10.4-A current stress which is higher than that of three-level CRM by 31.2%. Although the proposed three-level DCM scheme is based on DCM-based control framework, it gains significant peak reduction by quadrangular waveforms and its peak inductor current is higher than that of three-level CRM control only by 2.1%.

Second, conventional two-level DCM and proposed three-level DCM methods operate at fixed-frequency 35 kHz, while the measured frequency of three-level CRM control varies from 36.4 kHz to 94.7 kHz by input voltage variation.

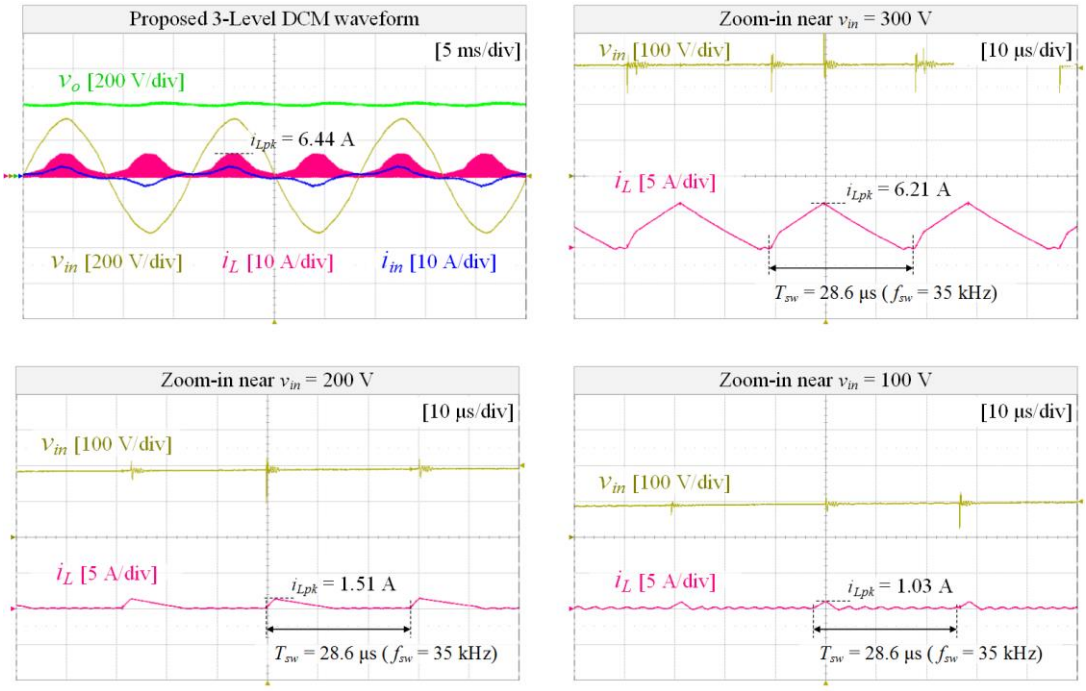
From the switching losses and overall efficiency points of view, the proposed control is the most favorable among all. It is because switching losses can bring major difference to total loss amount, as analyzed in the section 4.4; only the proposed control can get low turn-off currents near CRM case and low fixed switching frequency of DCM case at the same time.



(a)



(b)



(c)

Fig. 4-16. Experimental waveforms at 220 V_{rms} with full load by control method.

(a) two-level DCM. (b) three-level CRM. (c) proposed three-level DCM.

Similar tendencies of waveform factors can be found from the experiment results at 220 V_{rms} (311-V_{pk}) input and 300-W load conditions in Fig. 4-16. The proposed three-level control scheme shows 15.4% reduction of peak inductor current than that of conventional two-level DCM control; compared to the three-level CRM control, it is higher by 29%. In terms of operating switching frequency, both two-level and three-level DCM control methods run TLB PFC at 35 kHz while the three-level CRM control experiences variable frequency from 67 kHz to 340 kHz. At lighter load condition, TLB PFC with the CRM control is expected to suffer from higher switching-frequency losses. For example, frequency variation from 235 kHz to 847 kHz was measured at 220-V_{rms} input and 60-W (20%) load conditions.

With the 220 V_{rms} input voltage in Fig. 4-16, the common on-time T_{on} in the two-level and three-level DCM methods becomes much shorter than 110 V_{rms} input in Fig. 4-15. It can be inferred from the $V_{in.pk}$ term in the denominators of (33)–(34). Due to shorter T_{on}, the disparity between peak inductor current and average input current in Fig. 4-16 gets larger than that of Fig. 4-15. It makes input currents of the two DCM control methods more distorted than that of three-level CRM control, causing further input PF drops. Since the proposed control scheme always has shorter $T_{on.3L}$ than the $T_{on.2L}$ by (34), the input PF of proposed control is even lower than that of two-level DCM control; therefore, it can be noted that the proposed control scheme can have fixed-frequency, reduced peak current and secondary benefits at the cost of input PF degradation.

The output-voltage balancing scheme built in the proposed DCM control method has been also verified with the prototype tests. As can be seen in Fig. 4-17, TLB PFC is initially operated by the two-level DCM control scheme before activating the proposed three-level DCM control.

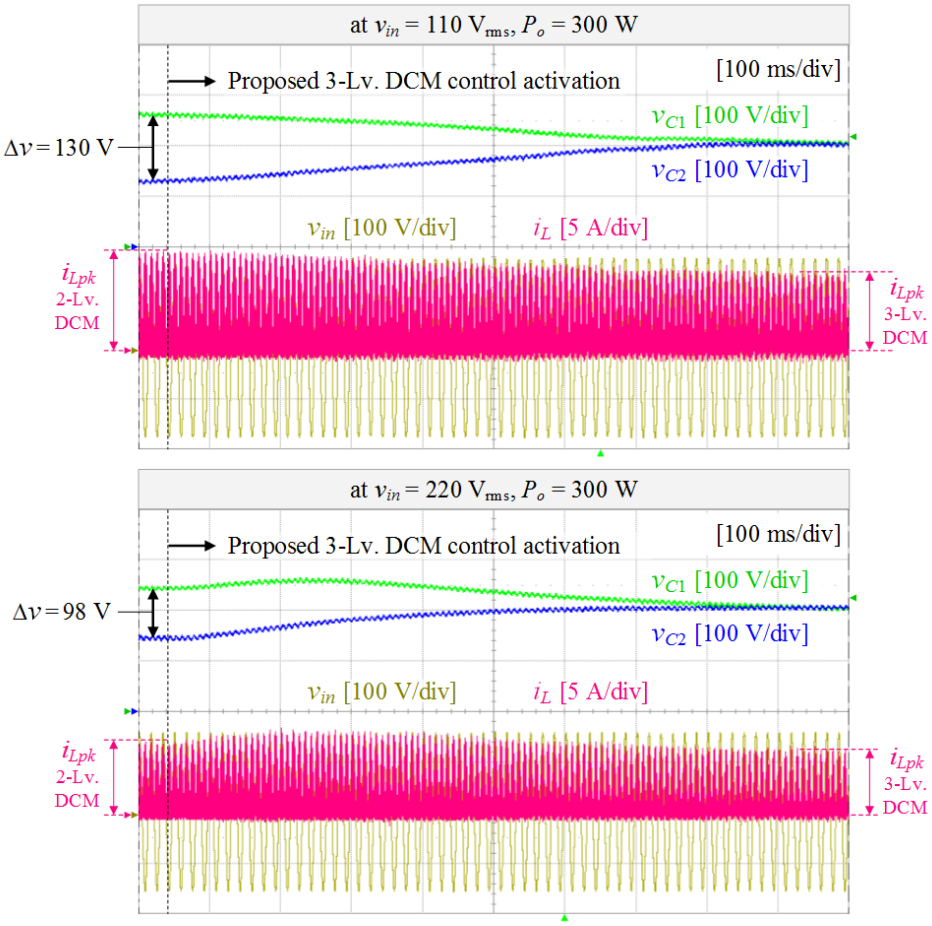


Fig. 4-17. Voltage balancing results of proposed three-level DCM control.

Even with equal charging/discharging capacitor currents by symmetric gate signals for S_1 and S_2, the two output-capacitor voltages v_{C1} and v_{C2} show substantial differences up to 130 V due to parameter tolerances and corresponding thermal unbalance between two boost cells. However, as can be seen from Fig. 4-17, the unbalancing phenomenon is effectively resolved by activating the proposed control with the voltage balancing scheme. It can be noted from the results that the balancing principle which makes higher-voltage cell's switch be conducted longer for t_α^* period is effective, overcoming the inherent topological issue of TLB PFC.

From Fig. 4-18 to Fig. 4-20, the measured results of quantitative factors including efficiency, input PF and harmonics are plotted.

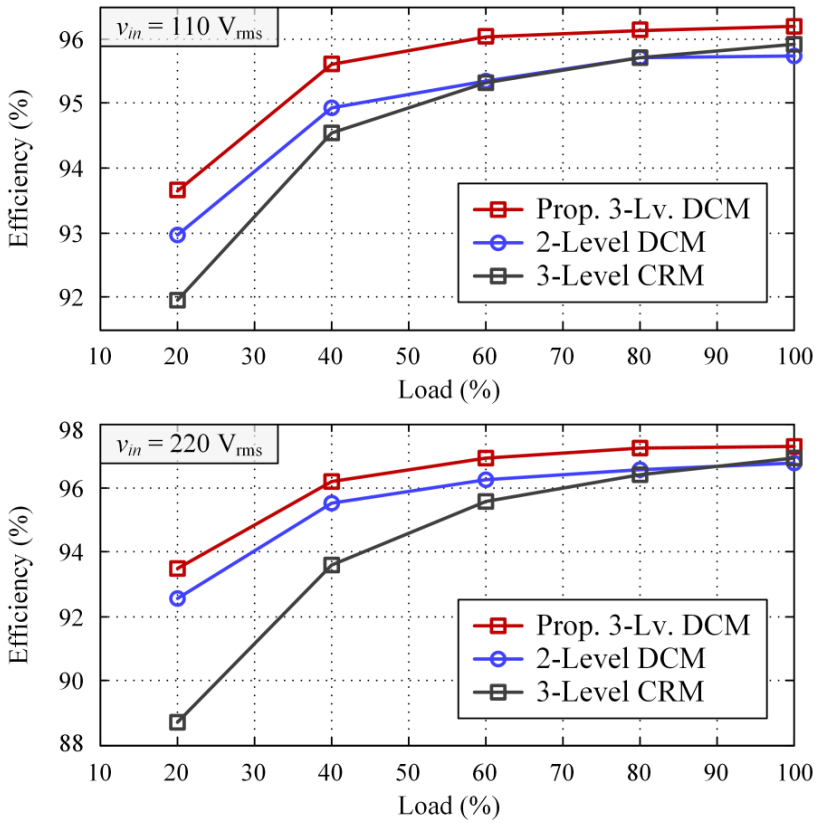


Fig. 4-18. Efficiency curve by control method.

First, efficiency curves by three control methods are compared in Fig. 4-18. Regardless of input rms voltages, the three-level CRM control in Chapter 3 shows the lowest light-load efficiency due to high switching frequency and corresponding switching losses; especially for 220 V_{rms} input condition, its light-load efficiency becomes much lower than the other two by 4–5% since the frequency goes up to 850 kHz, while the others run at fixed 35 kHz. In terms of turn-off current, the two-level DCM has the highest value and it leads to high switching losses at heavier load conditions. Due to the effects, the efficiency of two-level DCM control

becomes similar and even lower than that of three-level CRM at the full load (300 W) of both input rms voltages. On the other hand, the proposed three-level DCM control scheme, which has fixed-frequency operation and reduced peak current similar to three-level CRM, can record the highest efficiency all over the input voltage and load conditions.

As explained with Fig. 4-16, TLB PFC achieves higher efficiency and secondary benefits at the cost of input PF drops. Fig. 4-19 shows the measured results of input PF for the three control methods.

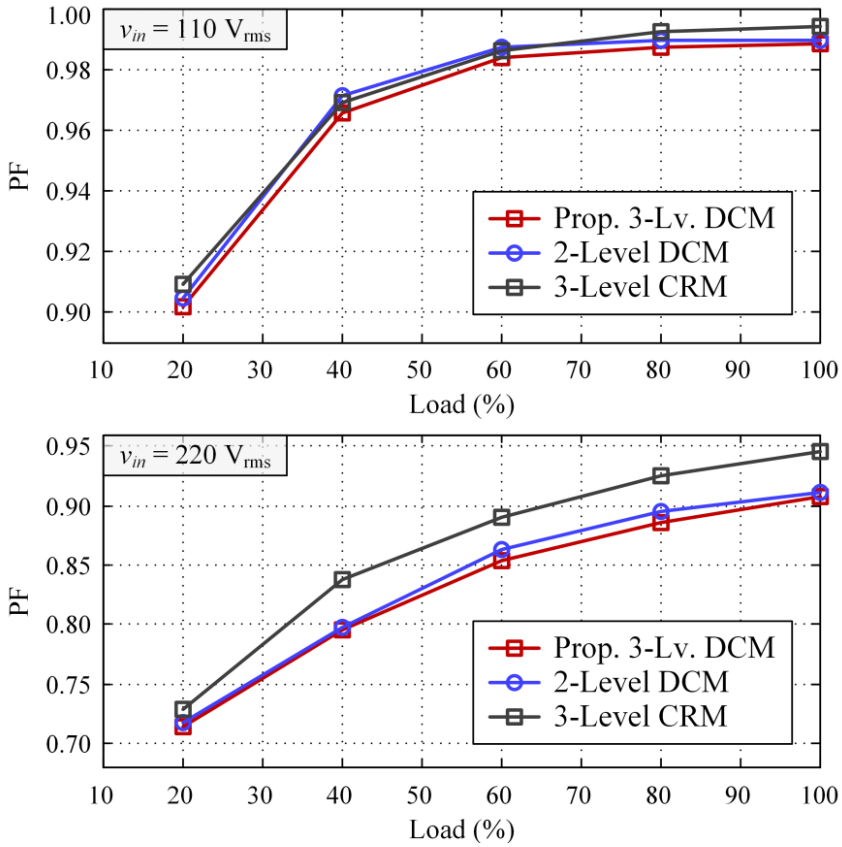


Fig. 4-19. Input PF curve by control method.

Since the disparity of peak inductor current and average input current becomes larger in the two-level and three-level DCM controls, their PFs are lower than that of three-level CRM and

the differences become noticeable at higher input 220 V_{rms}. The input PF of proposed three-level DCM shows slightly lower PF results than two-level DCM control by 0.4%–1% because $T_{on.3L}$ is shorter than $T_{on.2L}$ by (34) so that the average current is distorted more.

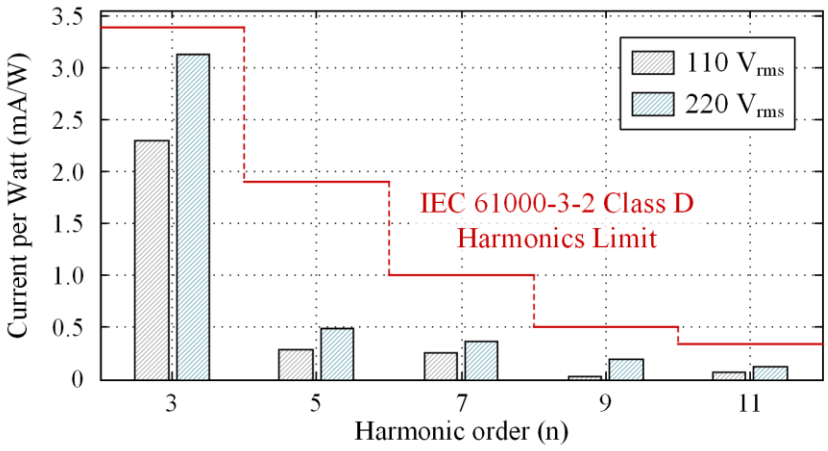


Fig. 4-20. Harmonic measurement results by input voltage range.

Lastly, in Fig. 4-20, low-order harmonic contents have been measured by TLB PFC with the proposed three-level DCM control scheme. As mentioned in the section 4.1, various two-level DCM/CRM control methods [69]–[72] developed to get fixed-frequency and reduced peak current at the same time had common issue of input current distortion by the third-order harmonic due to the lack of control degree-of-freedom. With the large amount of the third-order contents, experimental power ratings in the previous researches were limited to 120 W not to violate the IEC-61000-3-2 harmonic standards. However, as can be seen from Fig. 4-20, TLB PFC with the proposed control can achieve full-load (300W) supply for both input 110/220 V_{rms}, satisfying the standard limits with margins.

In summary, the experimental results of TLB PFC prototype verify that the proposed three-level DCM control scheme can bring benefits of DCM and CRM in Table 4-1 at the

same time, obtaining high converter efficiency. The inherent voltage unbalancing issue can be also effectively suppressed by the balancing principle built in the proposed control. Moreover, the proposed scheme overcomes the power limitations of state-of-the-art ZCS PFC converters due to third-order harmonics. TLB PFC is able to achieve these operational improvements with a technical trade-off of input PF drop.

4.7 Chapter Summary

In this paper, a three-level DCM control scheme is proposed for TLB PFC based on quadrangular inductor current availability introduced in Chapter 2. The key control concept is the time-varying adjustment of single-switch on-time t_{α}^{*} in each switching period to synthesize quadrangular CRM-shaped current waveform. The adjustable three-level current modulation can bring not only fixed-frequency operation of DCM but also reduction of peak current close to CRM, with a trade-off of input PF drop. Thus, it would be better if compensation technique for the input PF decrements can be discussed as a future work. Operational benefits from the proposed control are reductions of current stresses, switching losses, DM-EMI and improvement of efficiency, compared to conventional two-level DCM and three-level CRM methods. In low input-voltage region, however, TLB PFC with the proposed control gets into DCM operations due to low input current level. On top of the current control principle, the proposed DCM control can be equipped with output-voltage balancing scheme which can easily solve the inherent topological unbalance issue. In order to validate the feasibility and operational benefits, experimental verifications with a 300-W TLB PFC prototype are conducted.

Chapter 5.
Spread-Spectrum Frequency Modulation with Adjustable Three-Level DCM Control Scheme

In this chapter, a spread-spectrum frequency modulation (SSFM) technique is proposed which can be applied to many boost-derived PFC converters with DCM control method [95]. The frequency modulation can reduce severe DM EMI amplitudes caused by high inductor current ripples at single switching frequency, which is major drawback of DCM operations. Moreover, a down-spectrum technique adopted in the proposed SSFM can reduce switching losses. On top of the proposed SSFM, the basic three-level current modulation of TLB PFC is used with the adjustable single-switch on-time introduced in Chapter 4. By the SSFM harmonized with the three-level DCM control scheme, current ripples and EMI noises from DCM operations can be further reduced than the reduction amount by SSFM itself [95]. Analyses and experimental results in this chapter validate that the proposed SSFM and adjustable three-level DCM scheme bring improvements of both DM EMI and efficiency at the cost of increased output-voltage ripples.

5.1 Background

Boost-derived PFC converters with DCM control method run with constant switching frequency, while CRM control method brings inherently time-varying switching frequencies to boosting PFC converters. Due to the operational difference, DCM control schemes can exclude external ZCD circuitry from hardware and accurate switching-cycle control from software respectively, achieving simpler converter structures [77]. However, higher inductor

current peak/ripple and device current stresses are relative drawbacks compared to CRM method, as organized in Table 4-1. Furthermore, DM EMI amplitudes from DCM operations are much higher than those of CRM operations since all the EMI-related switching energies in DCM are concentrated on a single switching frequency, causing requirement of increased size of input EMI filter [78]–[80].

In recent years, solid EMI-reduction techniques called spread-spectrum frequency modulation (SSFM) have been widely studied and implemented to power converter systems in various applications [81]–[88]. Majority of SSFM clients has been dc-to-dc power converters, especially for resonant-type converters of which characteristics are deeply related to operating frequencies [81]–[86]. With SSFM techniques, switching frequency can be intentionally distributed to wide range on spectrum so that critical peak of EMI amplitudes can be significantly reduced at the reasonable cost of output-voltage ripple increments [87]–[88]. According to the effects of SSFM proven in previous literatures, high DM EMI amplitudes of DCM operations in boosting PFC converters can be apposite target to solve. However, to the best of author's knowledge, there has never been a single research attempt to implement SSFM technique directly to PFC converters. Only a sort of hysteresis control with fixed switching frequency, called sigma-delta modulated pulse-space control, was proposed for PFC converters to reduce EMI amplitudes by naturally spreading spectrum from hysteresis boundary [89]–[91].

In this chapter, along with the research trend, a simple SSFM technique suitable for DCM control in many boosting PFC converters is proposed for the first time. The proposed SSFM can be applied not only to TLB PFC but also to many two-level boosting PFC topologies mentioned in section 1.3. The goal of proposed frequency modulation is to suppress DM EMI

amplitudes by distributing DCM switching energies on frequency spectrum. Moreover, the distinctive multilevel current-slope capability of TLB PFC is used on top of the proposed SSFM to further reduce the peak inductor current and corresponding DM EMI amplitudes. Detailed operation principles, key equations, and implementation with voltage balancing scheme are presented in this chapter. And, a set of experimental results including EMI measurement is also provided to verify the effectiveness of proposals.

5.2 Proposed SSFM with Three-Level DCM Control Scheme

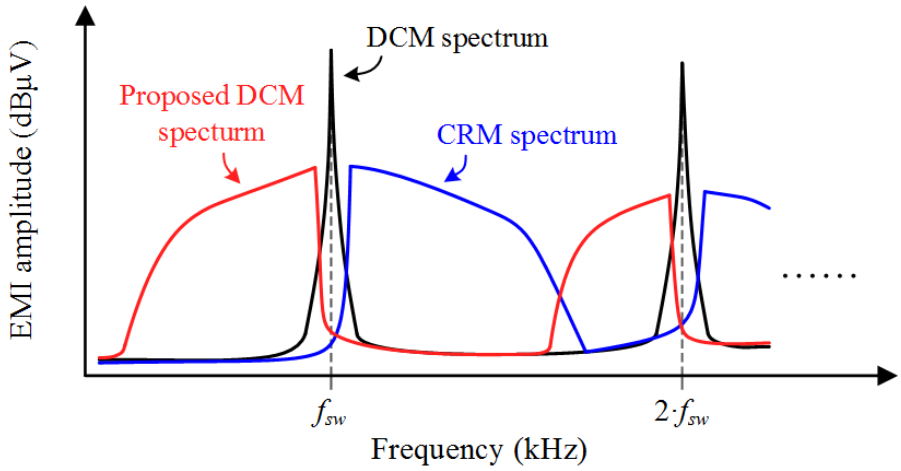


Fig. 5-1. Frequency spectrum by PFC control method.

In Fig. 5-1, a desired spectrum of the proposed SSFM on DCM is shown with conventional ZCS control spectrums. Under equal conditions of input-output voltages, inductance and power level, conventional DCM spectrum in black color has much higher peak amplitudes at switching frequency f_{sw} than inherently distributed CRM spectrum in blue color [92]–[94]. Amplitudes at integer multiples of switching frequency keep showing similar tendencies. Since current conduction mode of boosting PFC under DCM control can easily

violate CCM losing ZCS turn-on if switching frequency is increased near boundary conditions, the proposed DCM spectrum aims to be located at lower switching frequency region as red color in Fig. 5-1, which is called by down-spread spectrum technique [81]; the maximum amplitudes of DM EMI is designated to show up at the highest frequency point to let the cut-off frequency of input filter increased as much as possible and make the filter size smaller [95]. The frequency distribution lower than f_{sw} (conventional DCM) facilitates reduced switching losses so that improved efficiency can be additional benefit of the SSFM.

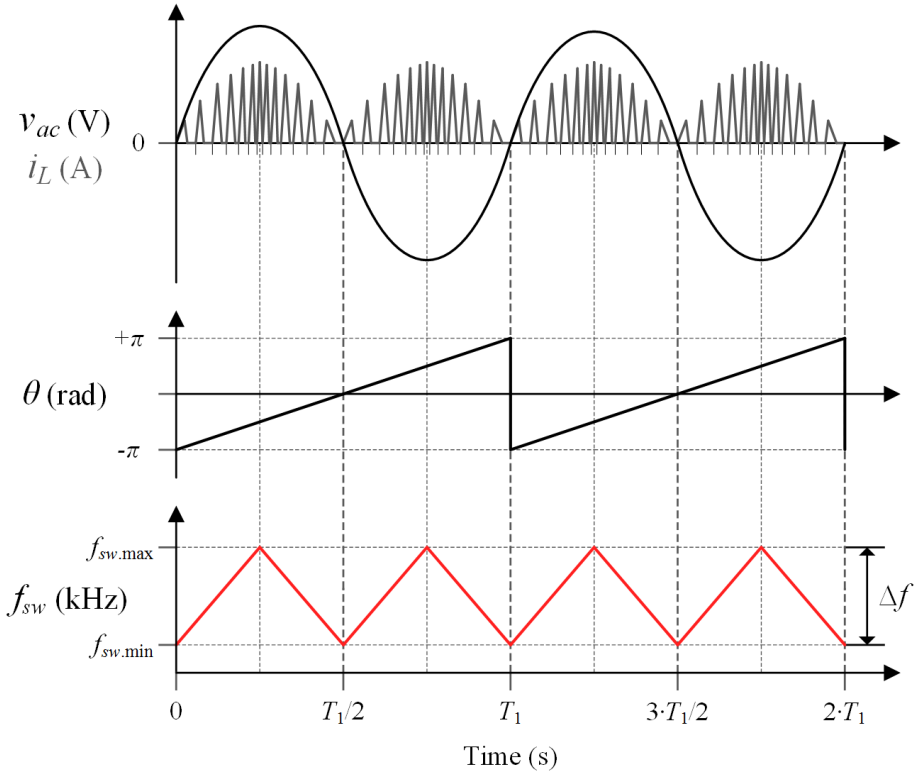


Fig. 5-2. Key waveforms of proposed SSFM.

Fig. 5-2 shows key waveforms of the proposed SSFM for DCM PFC control. The method is founded on typical phase-locked-loop (PLL) control of ac input voltage [55]. From the PLL control, angle information θ of sinusoidal ac input voltage can be extracted and utilized to

generate linearized switching-frequency distribution in Fig. 5-2 during ac line period T_1. Minimum and maximum switching frequencies are designed to locate at zero-crossing and peak input voltages, respectively. By the design, the desired down-spread spectrum in Fig. 5-1 can be realized. The proposed triangular-shaped frequency modulation in Fig. 5-2 can be formulated by (44) in terms of θ.

$$f_{sw} = \left(\left| |\theta| - \frac{\pi}{2} \right| - \frac{\pi}{2} \right| \cdot \frac{2}{\pi} \right) \cdot \Delta f + f_{sw.\min} \tag{44}$$

where Δf is the frequency range of SSFM and $f_{sw.\min}$ is the minimum frequency respectively.

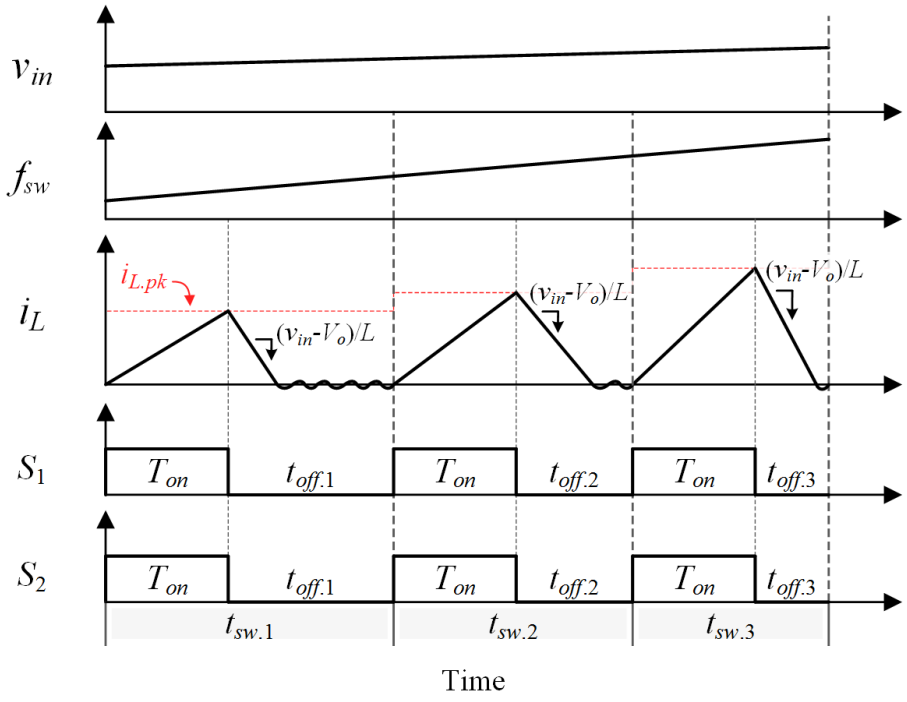


Fig. 5-3. Conventional two-level DCM scheme with proposed SSFM.

With the proposed SSFM technique, conventional two-level DCM current modulation can be used as Fig. 5-3 under varying frequency condition. In the similar way of previous chapters,

common on-time T_{on} is resulted from a slow-dynamic (1–5Hz) compensator for output voltage v_o and can remain almost constant during 50/60 Hz ac line cycles [75]. With a properly designed compensator, the two-level DCM operations in Fig. 5-3 can be obtainable not only by TLB PFC, but also by two-level boosting PFC topologies (e.g. conventional boost PFC, dual boost PFC and totem-pole boost PFC) introduced in Chapter 1. Their main switch S can be driven as the gate signals of S_1 and S_2 in Fig. 5-3 and equivalent inductor current slopes and shapes can be obtained. As a result, boosting PFC topologies with SSFM and two-level DCM scheme can achieve distributed EMI noises on frequency plot; accordingly, the maximum amplitude will be reduced, resulting in smaller input filter requirement.

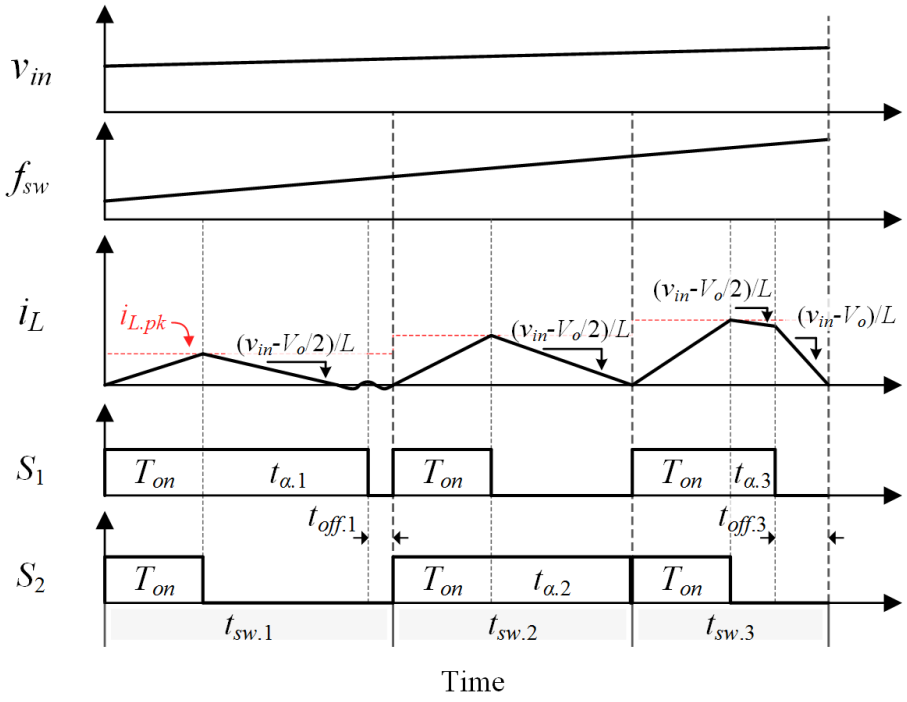


Fig. 5-4. Adjustable three-level DCM scheme with proposed SSFM.

With the proposed SSFM, DM EMI amplitudes of DCM operation can be significantly suppressed. However, with TLB topology, there still remain chances to reduce EMI noises

further. In general, multilevel feature is exploited to improve waveform qualities at ac side (e.g. THD, EMI) in ad-dc PFC rectifiers and dc-ac inverters [96]–[97]. From this technical standpoint, three-level current-slope capability of TLB can bring additional improvement with the proposed SSFM. In Fig. 5-4, key waveforms of the adjustable three-level DCM scheme are shown with time-varying switching frequency. The key concept is adding and changing an adjustable single-switch on-time t_α in each switching cycle to make non-zero inductor current waveform fit into the variable switching period t_{sw}. However, if input voltage level is too low, inductor current will be operated in DCM form as shown in Fig. 5-4. Toggling of switch conduction for t_α is executed between S_1 and S_2 by turns to mitigate output-voltage unbalance.

As can be compared from Fig. 5-3 and Fig. 5-4, the main advantage of adjustable three-level DCM control scheme is reduction of peak inductor currents which directly affects the amplitudes of DM EMI. Under assumption of equal input-output voltages, power and inductance, the average input currents of two-level DCM and adjustable three-level schemes can be equal only when the areas of inductor currents in each switching cycle are matched to each other. Since the non-zero inductor current time in Fig. 5-4 is longer than that of Fig. 5-3, it is acceptable to expect lower peak current from the proposed three-level scheme under SSFM. Mathematically, the fact has already been proved by (33)–(34) in Chapter 4 that common on-time T_{on} with three-level DCM scheme is shorter than that of two-level DCM scheme. Since peak inductor current is proportional to T_{on}, it is obvious that the proposed SSFM with adjustable three-level DCM scheme will have further EMI reductions than SSFM with conventional DCM scheme. It can be noted that this additional improvement is distinctively achievable by none other than TLB PFC topology because other two-level boosting PFCs don't have the additional degree-of-freedom in current modulation.

5.3 Digital Implementation with Voltage Balancing Scheme

Although the toggling function of conducted switch for t_α is applied to the adjustable three-level scheme in Fig. 5-4, voltage balancing between v_{C1} and v_{C2} cannot be guaranteed. It is mainly because input voltage and switching frequency conditions keep changing for entire line cycle T_1 so that asymmetric charging/discharging amounts of C_1 and C_2 from t_α durations are inevitable. Thus, a simple voltage balancing algorithm that can be easily equipped with the proposed scheme is also devised. Detailed implementation with the voltage balancing method is explained in this section.

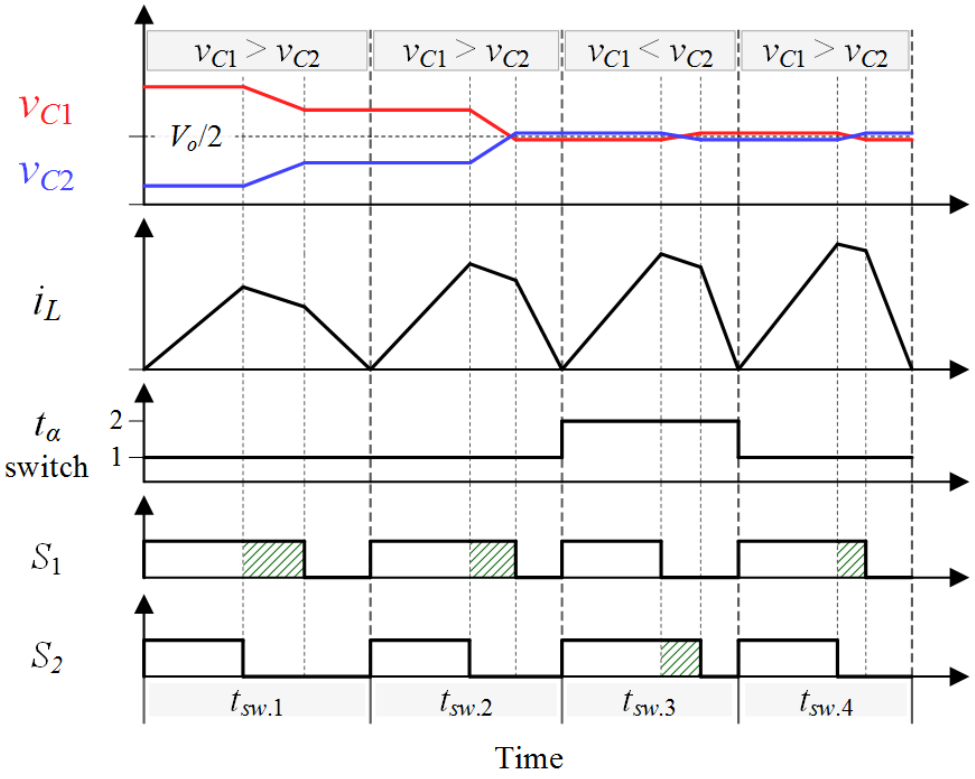


Fig. 5-5. Output voltage-balancing method in the adjustable three-level scheme.

In Fig. 5-5, key waveforms of balancing scheme are shown. The principle is mostly similar to the voltage balancing method in Fig. 4-12. One different thing is, now, the switching period t_{sw} in each cycle keeps changing. In order to work with the variable frequency, following steps are needed.

Setup) Sampling frequency of DSP control unit should be set higher than $f_{sw.max}$.

1) Output voltages v_{C1} and v_{C2} are measured and higher voltage is defined as V_h in every sampling/control routine.

2) Higher-voltage boost cell's switch is chosen to turn on in t_α period for more discharging.

3) Required t_α in a cycle which can be calculated by (45) is applied to the selected switch through pulse-width-modulation (PWM) module.

$$t_\alpha = \frac{(V_o - v_{in}) \cdot t_{sw} - V_o \cdot T_{on}}{V_h} \tag{45}$$

The above equation for t_α is in the same form of (43) except that the switching period is now variable t_{sw}, not constant T_{sw}. By the setting and ***1)–3)*** steps in each sampling cycle, TLB PFC with the proposed SSFM and adjustable three-level DCM scheme can get balanced outputs. The explained procedures and principles are summarized with flowchart of one sampling routine (Fig. 5-6) and control block diagram (Fig. 5-7) in the following page.

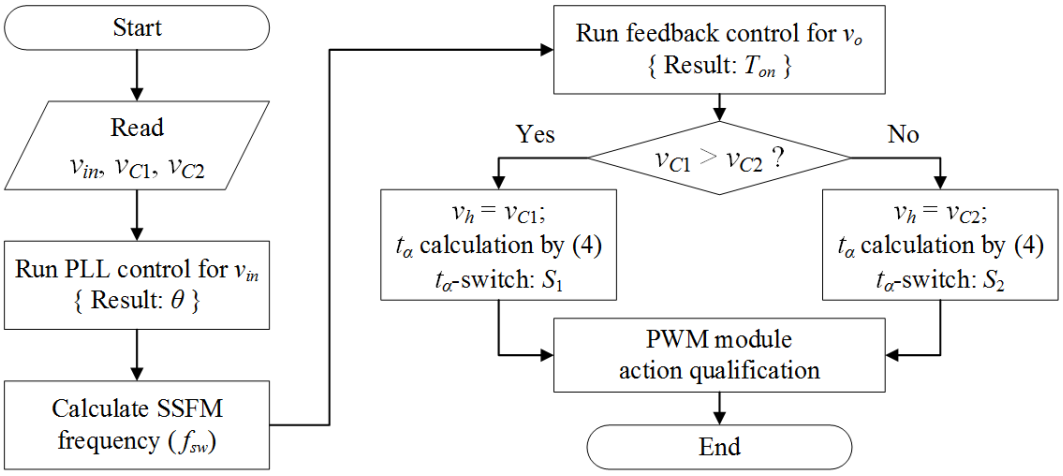


Fig. 5-6. Flowchart of proposed SSFM with three-level DCM control and voltage balancing schemes.

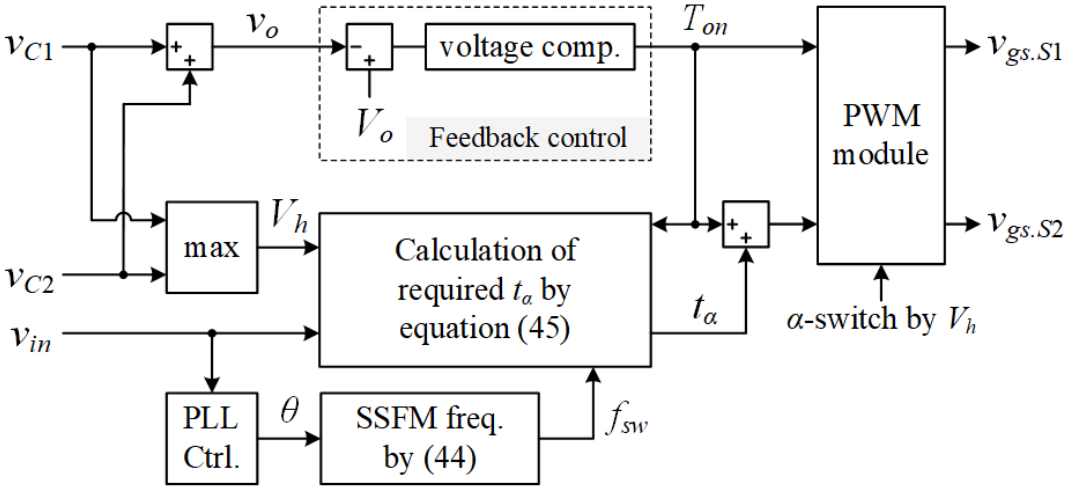


Fig. 5-7. Control block diagram of proposed control schemes.

5.4 Experimental Results

In order to confirm EMI reduction and efficiency improvement by the proposed SSFM technique and three-level DCM scheme, a TLB PFC prototype has been built and tested with experimental specifications in Table 5-1. For DM EMI measurement, equipment under test (EUT) is installed as Fig. 5-8 and actual laboratory EMI-test setup is shown in Fig. 5-9.

Table 5-1. Experimental Specifications.

Input voltage	110 V_{rms}
Output voltage	400 V
Load	60–300 W (20–100%)
Switches (S_1, S_2)	IPW60R041P6 (C_{oss}=310 pF, $R_{ds,on}$=41 mΩ)
Diodes (D_1, D_2)	C4D10120D (v_F=1.4 V)
Inductance (L)	230 μH
Capacitance (C_1, C_2)	470 μF
DSP control unit	Texas instruments TMS320F28377D
SSFM frequency	$f_{sw.min}$=25 kHz, $f_{sw.max}$=35 kHz
Sampling frequency	40 kHz
EMI spectrum analyzer	Agilent N9320B

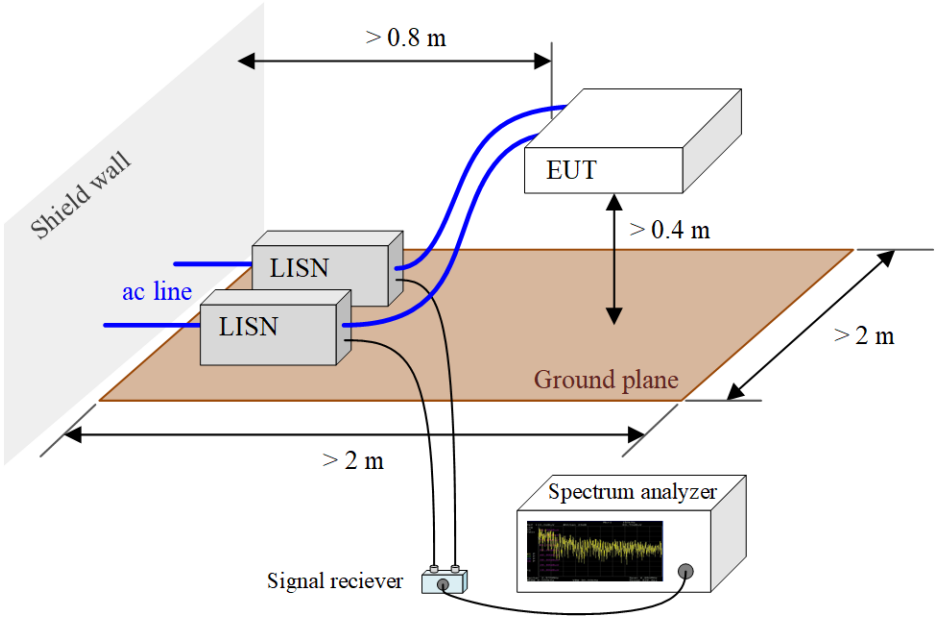


Fig. 5-8. Configuration of EMI measurement setup.

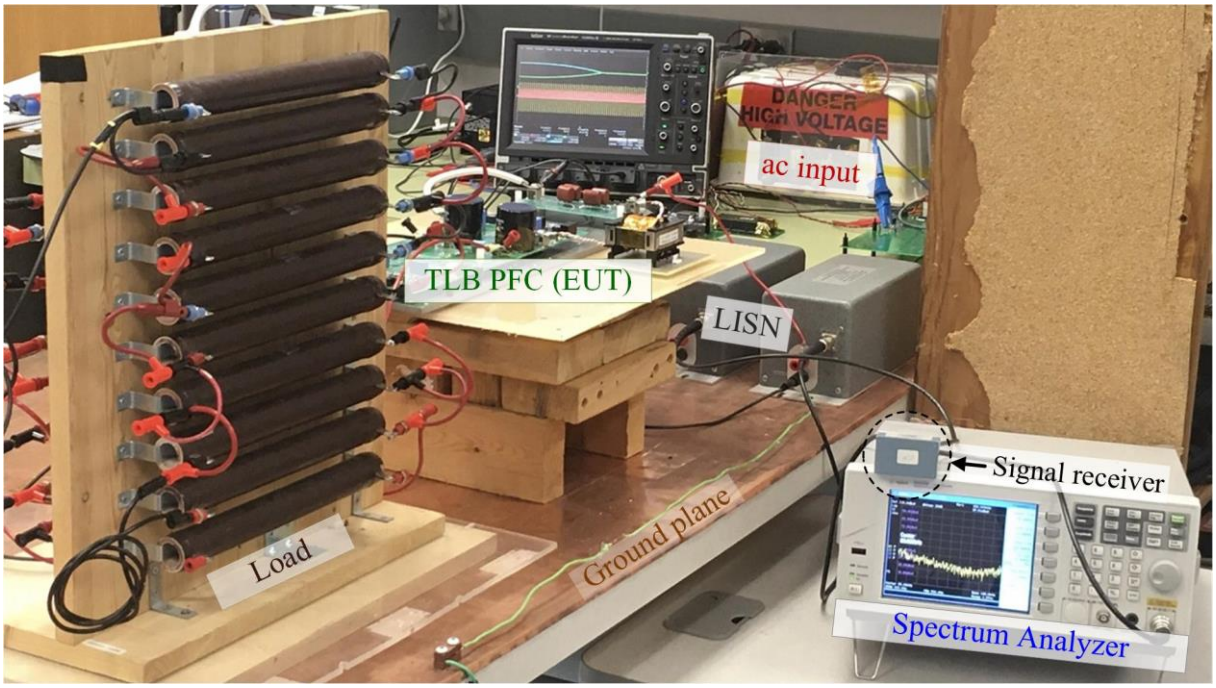


Fig. 5-9. Actual laboratory setup for EMI measurement test.

For EMI measurement, 110-V_{rms} input voltage and 300-W power conditions are used. The main reason is that a combination of the lowest input voltage and full-load power results in the highest input current level; accordingly, the highest amplitudes of DM EMI noises can be measured and critical points can be used for input filter design. Thus, between the nominal voltages 110 V_{rms} and 200 V_{rms}, the lower one is chosen for input condition.

Based on the specifications, the proposed SSFM technique and adjustable three-level DCM control scheme is tested. The experimental waveforms of the proposed operations in steady state are firstly shown in Fig. 5-10(a). The switching frequency linearly varies between 25 kHz–35 kHz along with input voltage variation, as designed Fig. 5-2. As can be seen, the PFC regulations including in-phase alignment of input voltage/current and dc-bus voltage control are achieved without instability issue.

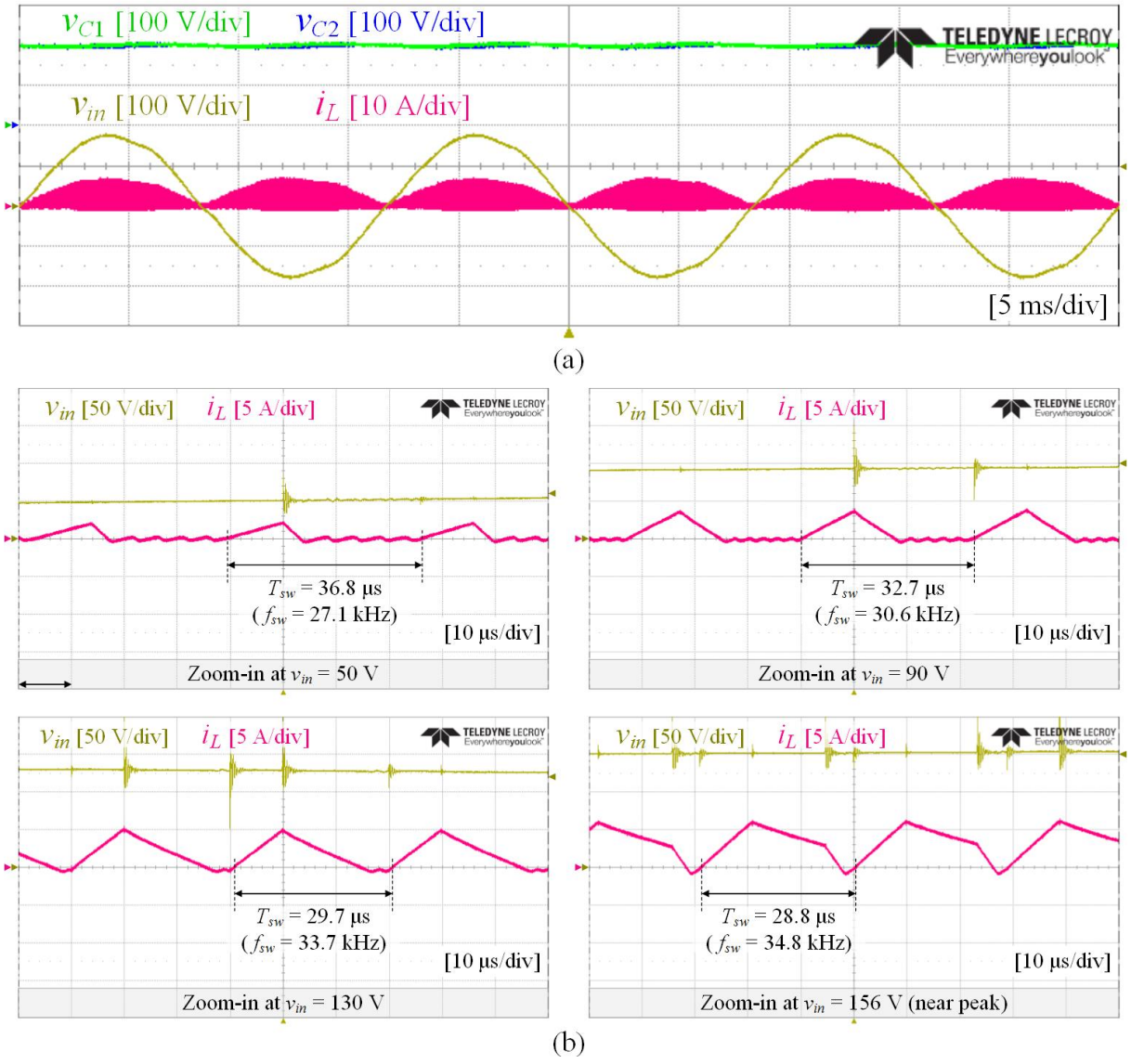


Fig. 5-10. Experimental waveforms of proposed SSFM with three-level DCM control scheme.

(a) steady state waveform. (b) zoom-in waveforms by input voltage.

In Fig. 5-10(b), zoom-in inductor current waveforms are captured. As expected, inductor current waveforms by the proposed methods become DCM and CRM depending on input voltage variation, showing good agreement with the key waveforms in Fig. 5-4. Especially at high input voltage near peak value, the proposed control schemes provides exactly matched t_α to synthesize quadrangular inductor current with reduced peak stress. Even for the lower input

conditions, TLB PFC operates with reduced peak current than the conventional two-level DCM control scheme. And, the linearly varying switching frequency f_{sw} for line cycle T_1 can be found from the zoom-in waveforms. The frequency distribution effects can be found from the EMI measurement plots in the following pages.

In Fig.5-11, the effectiveness of voltage balancing scheme equipped in the proposed SSFM is tested by activating the voltage balancing method.

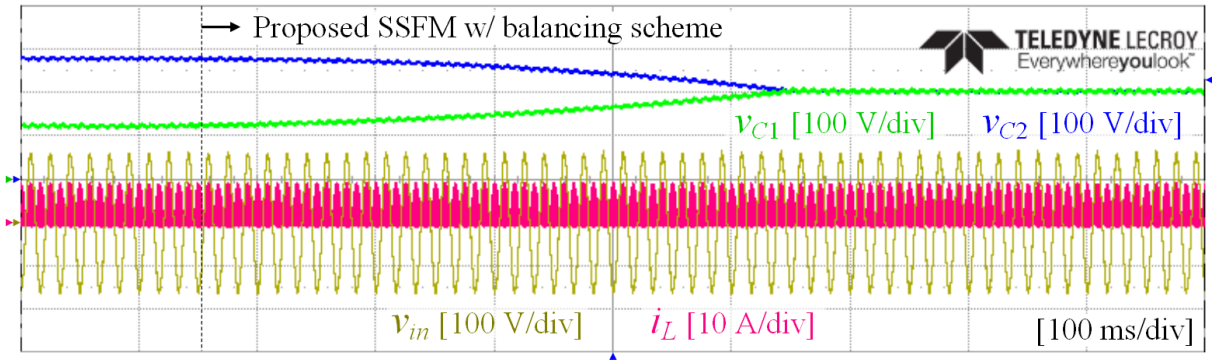
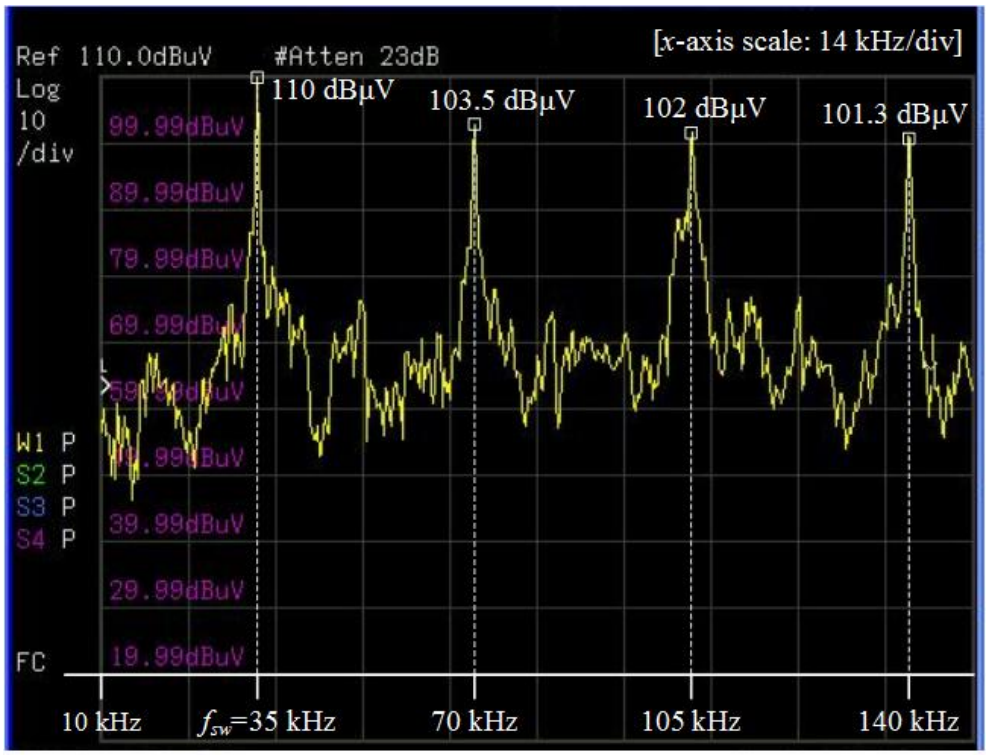
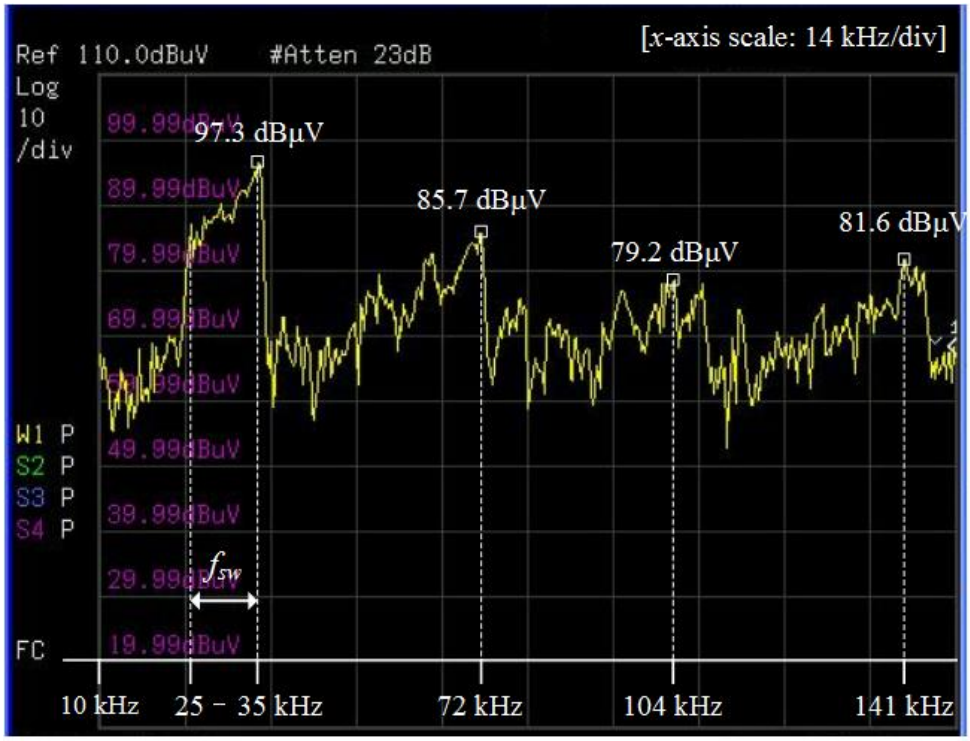


Fig. 5-11. Experimental waveforms with and without voltage balancing scheme.

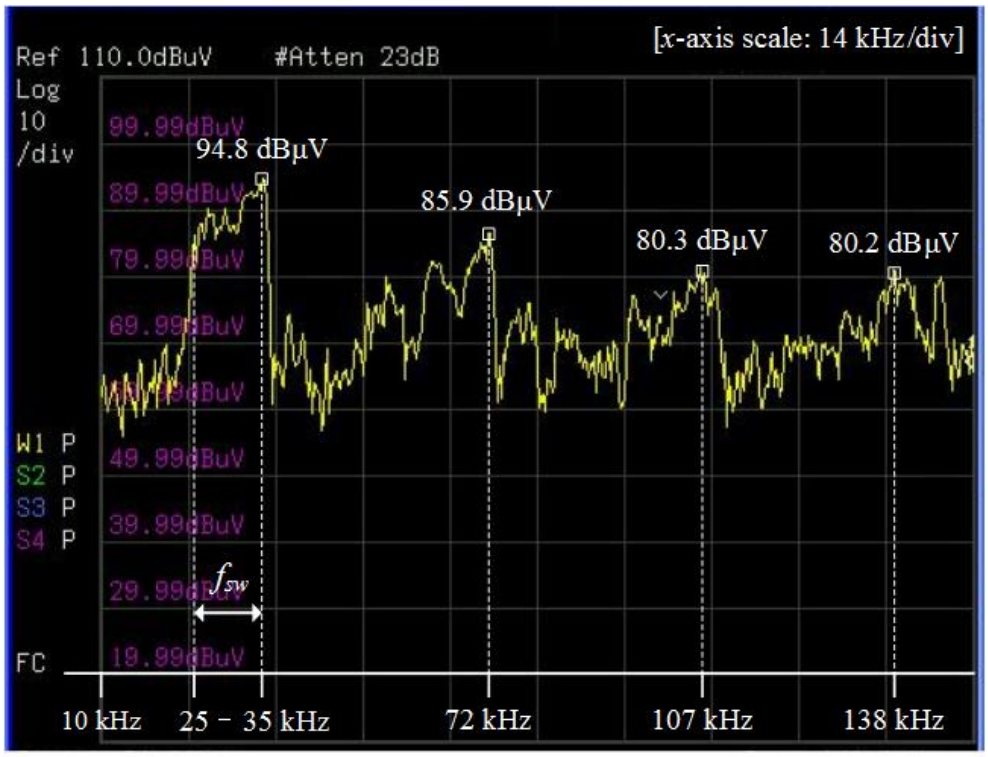
Before activating the voltage balancing scheme, TLB PFC prototype was controlled by the proposed SSMF plus adjustable three-level DCM scheme in Fig. 5-3 with the toggling of conducted switch in t_α. Even with the efforts to mitigate asymmetry, there exists 176-V voltage disparity between v_{C1} and v_{C2}. The main reasons of the unbalance are parameter differences in the two capacitors and asymmetric charging/discharging amounts due to time-varying converter conditions (i.e. input voltage and switching frequency). However, after the activation of voltage-balancing scheme in Fig. 5-11, the unbalance is effectively resolved and the average values of v_{C1} and v_{C2} waveforms meet at 200 V which is half of the total output voltage. From the balanced operations, disparities of voltage/current stresses and thermal behaviors in the two boost cells can be sufficiently mitigated.


Ref 110.0dBuV
#Atten 23dB
[x-axis scale: 14 kHz/div]
Log
10
/div
110 dBµV
103.5 dBµV
102 dBµV
101.3 dBµV
99.99dBuV
89.99dBuV
79.99dBuV
69.99dBuV
39.99dBuV
29.99dBuV
19.99dBuV
W1 P
S2 P
S3 P
S4 P
FC
10 kHz
f_{sw}=35 kHz
70 kHz
105 kHz
140 kHz

(a)


Ref 110.0dBuV
#Atten 23dB
[x-axis scale: 14 kHz/div]
Log
10
/div
97.3 dBµV
85.7 dBµV
79.2 dBµV
81.6 dBµV
89.99dBuV
49.99dBuV
39.99dBuV
W1 P
S2 P
S3 P
S4 P
f_{sw}
FC
10 kHz
25 – 35 kHz
72 kHz
104 kHz
141 kHz

(b)



(c)

Fig. 5-12. DM EMI measurement by control method. (a) fixed-frequency two-level DCM. (b) proposed SSFM with two-level DCM. (c) proposed SSFM with adjustable three-level DCM.

In Fig. 5-12, the measured DM EMI spectrums by control method are demonstrated. At the original switching frequency 35 kHz of fixed-frequency modulation in Fig. 5-12(a), the conventional DCM scheme recorded 110-dBμV peak amplitude and its integer multiple frequencies also showed highly concentrated energies above 101 dBμV.

In Fig. 5-12(b), DM EMI spectrum from the proposed SSFM operation is displayed. The effects of down-spectrum technique designated for linear distribution in lower frequency range can be found in the plot. Since the maximum inductor current happens at the peak of input voltage with maximum switching frequency, the plot in Fig. 5-12(b) shows good matches with the desired spectrum in Fig. 5-1. As can be seen, the peak amplitude near

original switching frequency is decreased by 12.7 dBμV than fixed-frequency DCM scheme in Fig. 5-12(a). The DM EMI amplitudes at the integer multiple ranges are also reduced by more than 17.8 dBμV.

On top of the SSFM, the proposed adjustable three-level DCM scheme is implemented to TLB PFC and DM EMI spectrum of the case is also measured in Fig. 5-12(c). Since the SSFM technique is applied, the amplitude level is sufficiently lowered already. However, in addition to that reduction, the adjustable three-level scheme brought further EMI reduction by 2.5 dBμV at the original switching frequency. The amplitudes around integer multiple frequencies are also similar or lower than Fig. 5-12(b).

Although it was not able to measure EMI responses in higher frequency region because high-frequency signal receiver (150 kHz–5MHz) was out of function, it is reasonable to expect that the reduction effects by the proposed SSFM and three-level scheme will be continued in higher frequency region. Since general EMI regulation standards such as FCC and CISPR have detailed limits on noises above 150 kHz, the critical design point of input filter is usually the first highest peak at or after 150 kHz. Considering the peak amplitudes near 150 kHz in Fig. 5-12, the cut-off frequencies of input filter design for the proposed methods can be higher than fixed-frequency DCM scheme, leading to smaller input filter size.

As mentioned in the introductory chapter, in practical point of view, main disadvantages of DCM control scheme compared to CRM control scheme are highly induced current ripple, corresponding high DM EMI and large input filter size; due to that, CRM control is preferred among the ZCS methods. However, the proposed SSFM technique and adjustable three-level DCM scheme can collaborate to resolve the inherent demerit and even can have relative advantage by lower switching losses with the down-spectrum SSFM method.

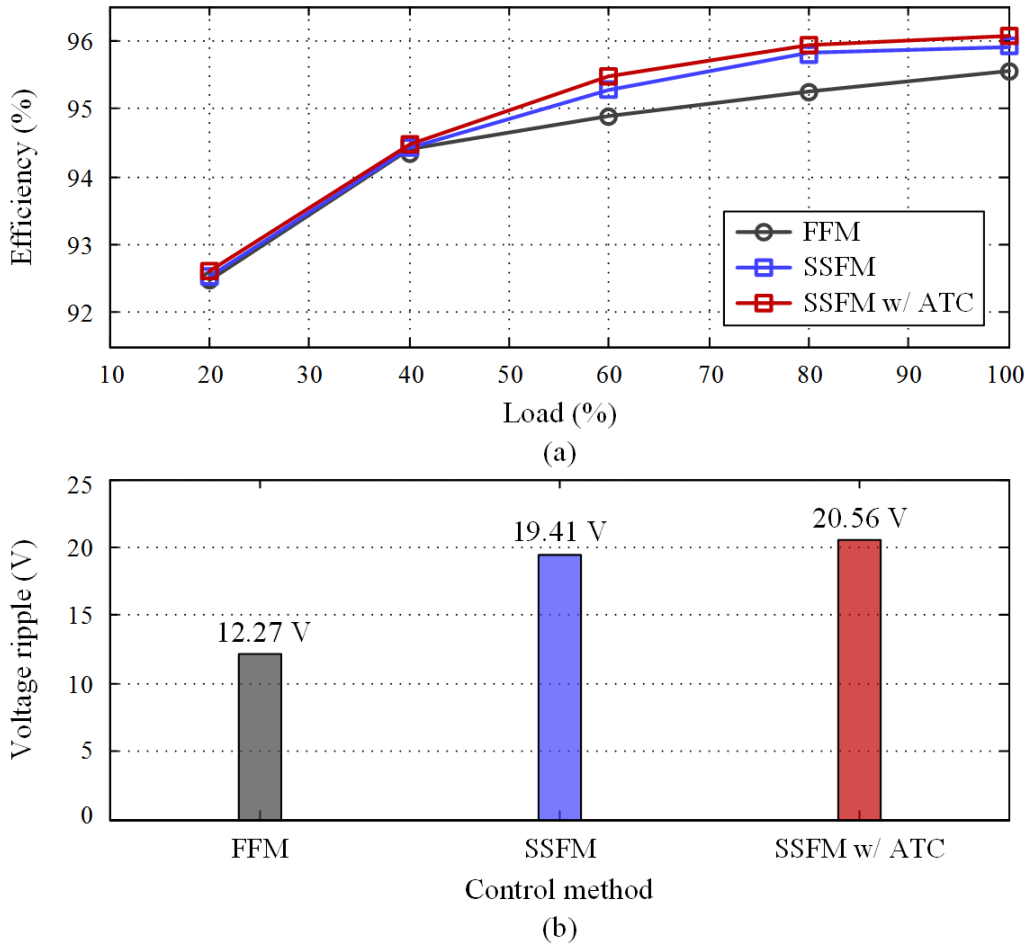


Fig. 5-13. Measurement results by control method.

(a) efficiency. (b) output voltage ripple.

In Fig. 5-13, measured efficiency curves and output voltage-ripple values are plotted. The proposed SSFM based on down-spectrum is rewarded with improved efficiency by 0.43% in average than fixed-frequency modulation (FFM). Moreover, the collaboration of SSFM and three-level DCM scheme brings additional 0.12% efficiency increment in average.

As mentioned in the section 5.1, increased output voltage ripple is well-known trade-off of SSFM techniques. The results in Fig. 5-13(b) show that 7.14-V and 8.28-V increments were measured from the SSFM and SSFM with three-level DCM scheme, respectively.

Though the increment rates are significant, the magnitudes of output voltage ripples are still in acceptable range since the values are less than ±5% boundary of 400-V output voltage.

5.5 Chapter Summary

In this chapter, a SSFM technique for DCM boosting PFC converters including TLB topology is proposed. The technique aims to reduce DM EMI amplitudes originated from high inductor current ripple and peak from DCM operations. To maintain DCM operations under the proposed SSFM, down-spectrum-based frequency distribution is adopted to the SSFM. Thus, reduction of switching losses is given as secondary benefit. On top of the proposed SSFM, this chapter utilizes the adjustable three-level DCM scheme in the last chapter for further reductions of peak current and DM EMI amplitude. The concept of adaptive single-switch on-time was able to bring additional decrements of current ripple and EMI by synthesizing inductor current in quadrangular CRM form, especially at the peak of input voltage. From the effects, it is expected to use smaller-size input filter for TLB PFC under the proposed DCM operations, overcoming main disadvantages of conventional DCM control schemes. Experimental results verify that the proposed methods can improve both EMI and efficiency at the cost of output voltage ripple increment.

Chapter 6.
Output Voltage Balancing Schemes

As introduced in the previous chapters, voltage unbalancing between v_{C1} and v_{C2} in TLB converter can happen even by equal charging and discharging currents through C_1 and C_2. In both DCM and CRM schemes, the voltage differences without any balancing attempt easily go over than 100 V. And, the phenomenon will cause severe differences of component voltage stresses and thermal behaviors. Therefore, in this chapter, two possible output voltage-balancing approaches are introduced in order to resolve the inherent unbalancing issue in TLB PFC topology. The operation principles, implementation methods and experimental verifications are included.

6.1 Background

Different from two-level boos-derived PFC topologies, TLB PFC in Fig. 1-6 consists of two boost cells and each one consists of one switch, one complimentary diode and one output capacitor. Thus, voltage unbalance between the two output capacitors has been always at practical issue. Even under well-controlled output voltage V_o, there can be huge voltage difference between v_{C1} and v_{C2} by characteristics of passive components, which will sacrifice a set of switch, diode and capacitor in the higher-voltage boost cell. The root causes of unbalance are mostly hardware-wise circuit asymmetry and tolerance of components. Although the circuit asymmetry can be mitigated by careful layout of printed circuit board (PCB) circuits, the tolerance issue of passive components is unavoidable. Fig. 6-1 shows the output capacitor leg in TLB topology with simplified capacitor structures [98].

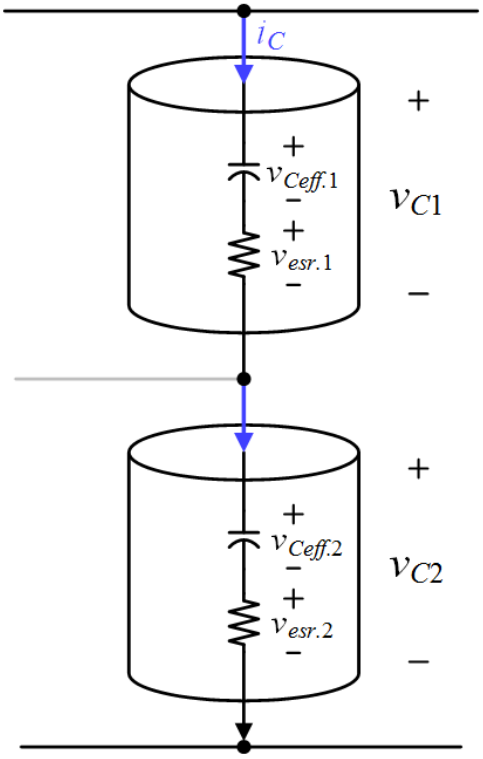


Fig. 6-1. Simplified equivalent capacitor structures.

As depicted, the equivalent capacitor structure can be expressed with a series connection of effective capacitor and parasitic ESR. In the figure, the two switches S_1 and S_2 are assumed to operate with symmetric gate signals. Then, even with the assumption of same current flow i_C, the capacitor voltages can be different by the equations in (46).

$$\begin{aligned} v_{C1} &= \int \frac{i_C}{C_1} dt + i_C \cdot R_{esr.1} \\ v_{C2} &= \int \frac{i_C}{C_2} dt + i_C \cdot R_{esr.2} \end{aligned} \tag{46}$$

Since the tolerances of electrolytic capacitors widely used in DCM and CRM PFC converters are ±20% range, dc-bias offset by the ESR-term and double-line frequency voltage ripple by the capacitive term can vary in wide range. These factors are the first root-cause of the

voltage unbalance. During the operations, the voltage difference will cause unbalanced power consumptions in each boost cell's components due to the different voltage stresses and turn on/off energies, inducing further unbalanced thermal behaviors in two boost cells. Thus, there must be proper balancing schemes to overcome this inherent issue.

In order to do that, researchers have developed balancing control methods for TLB PFC topology, as organized in Table 6-1.

Table 6-1. List of literatures on TLB PFC balancing schemes.

Ref.	Mode	Controller type	Balancing	Complexity
[46]–[47]	CCM	Dual-loop (v_o & i_L) + FF (T_{on})	Yes	Mid
[50], [54]		Predictive control	Yes	Highest
[99]	DCM	Two-loop (v_{C1} & v_{C2}) + Phase	Yes	Mid
[59]	CRM	Single-loop (v_o)	No	Lowest

For TLB CCM PFC, dual-loop controls for voltages and input current became popular [46]–[47]; model-based predictive controls have been also employed in [50], [54]. For TLB DCM PFC, researchers in [99] proposed the usage of two separate voltage control-loops for v_{C1} and v_{C2} with additional phase control. However, the phase angle control in [99] can be only applied selectively at low input voltage condition, making entire control-complexity high in practical point of view; in addition, the method wasn't confirmed by simulation or experiment with mismatched capacitances. For TLB CRM PFC, the research [59] suggested toggling of conducted switch for t_α and using parameter-matched capacitors usages without detailed balancing technique. Considering the literatures in Table 6-1, it can be said that a practical balancing scheme is quite necessary for TLB PFC with DCM and CRM operations. Based on

this motivation, two types of voltage balancing methods are introduced in this chapter. One approach is the toggling principle that was used for the proposed CRM/DCM control schemes in the previous chapters. The other type is to select one switch as a master agent to deal with unbalanced voltage by adjusting its own on-time duration.

6.2 Toggling of Conducted Switch in Single-Switch On-Time Period

The toggling of conducted switch between S_1 and S_2 for single-switch on-time t_α is implemented to the proposed control schemes in Chapter 3–5. The common balancing principle can be found in Fig. 3-2, Fig. 4-3 and Fig. 5-4. The principle can mitigate the asymmetry of charging and discharging amounts in C_1 and C_2 to some degree, but it doesn't guarantee that the average voltages of v_{C1} and v_{C2} exactly stay at half of total output voltage. It is mainly due to the time-varying converter conditions such as ac input voltage, instantaneous input power and frequency change by SSFM. Thus, in Fig.4-12 and Fig. 5-5, the toggling function considering the real-time unbalance condition is proposed for DCM schemes in Chapter 4–5. The key concept is that measuring the real-time values of v_{C1} and v_{C2} in each sampling cycle and letting a switch of the higher-voltage cell conducted for additional on-time t_α in order to discharge the cell's capacitor more. By doing so, the proposed three-level DCM schemes are able to achieve stable and balanced output operations. One important feature in terms of implementation is that sampling frequency of DSP control unit should be equal or higher than maximum converter switching frequency. Due to the reason, the proposed balancing scheme worked well in the DCM schemes of which switching frequencies are fixed or linearly varied in limited range; but, it was not able to work with three-level CRM scheme in Chapter 3 of which variable switching frequency can go up near 1 MHz region at

lighter load condition. If sampling frequency of the CRM scheme is set beyond the highest operating frequency, the balancing scheme can be also realized with the CRM control method. In that case, however, the control designer should confirm that the calculation time in one sampling cycle is less than the period of sampling frequency with some margin.

6.3 Adjusting a Master-Module Switch's On-time Period

In this section, another approach of voltage balancing in TLB PFC is presented which can be used for both DCM and CRM control methods [60]. Operation principles of the method are explained as follows.

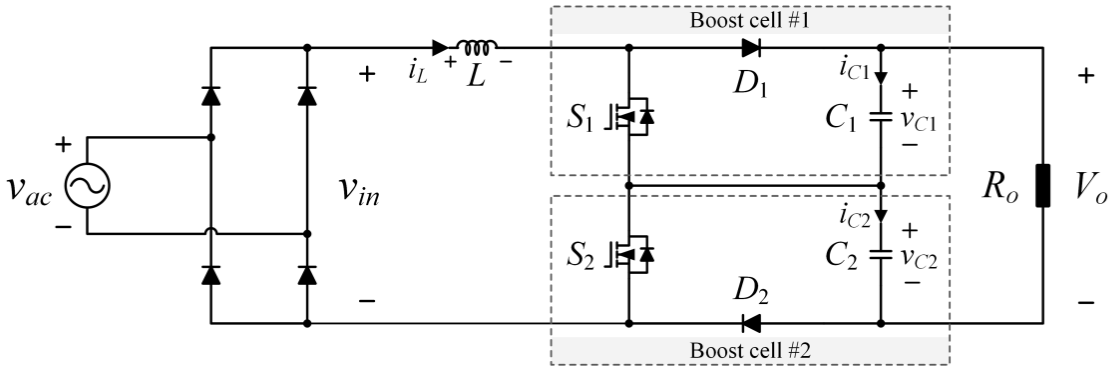


Fig. 6-2. Two boost cells in TLB PFC topology.

In Fig. 6-2, detailed two boost cells are drawn. Underlying assumption is that the total output voltage, which is equal to $v_{C1}+v_{C2}$, is controlled to V_o by properly designed feedback voltage compensator. By the feedback control, the result of compensator T_{on} remains constant for ac line cycles. The key concept of balancing scheme is that a switch of one boost cell is selected as a master switch to deal with unbalanced voltages. In this section, the switch S_1 in the upper boost cell of Fig. 6-2 is chosen for the role. And, v_{C1} is assumed to be higher than v_{C2} for explanation. Based on the assumptions, key waveforms of the proposed master-switch-

balancing scheme are shown in Fig. 6-3. Matched circuit operations are also described in Fig. 6-4 by switching status ①-④.

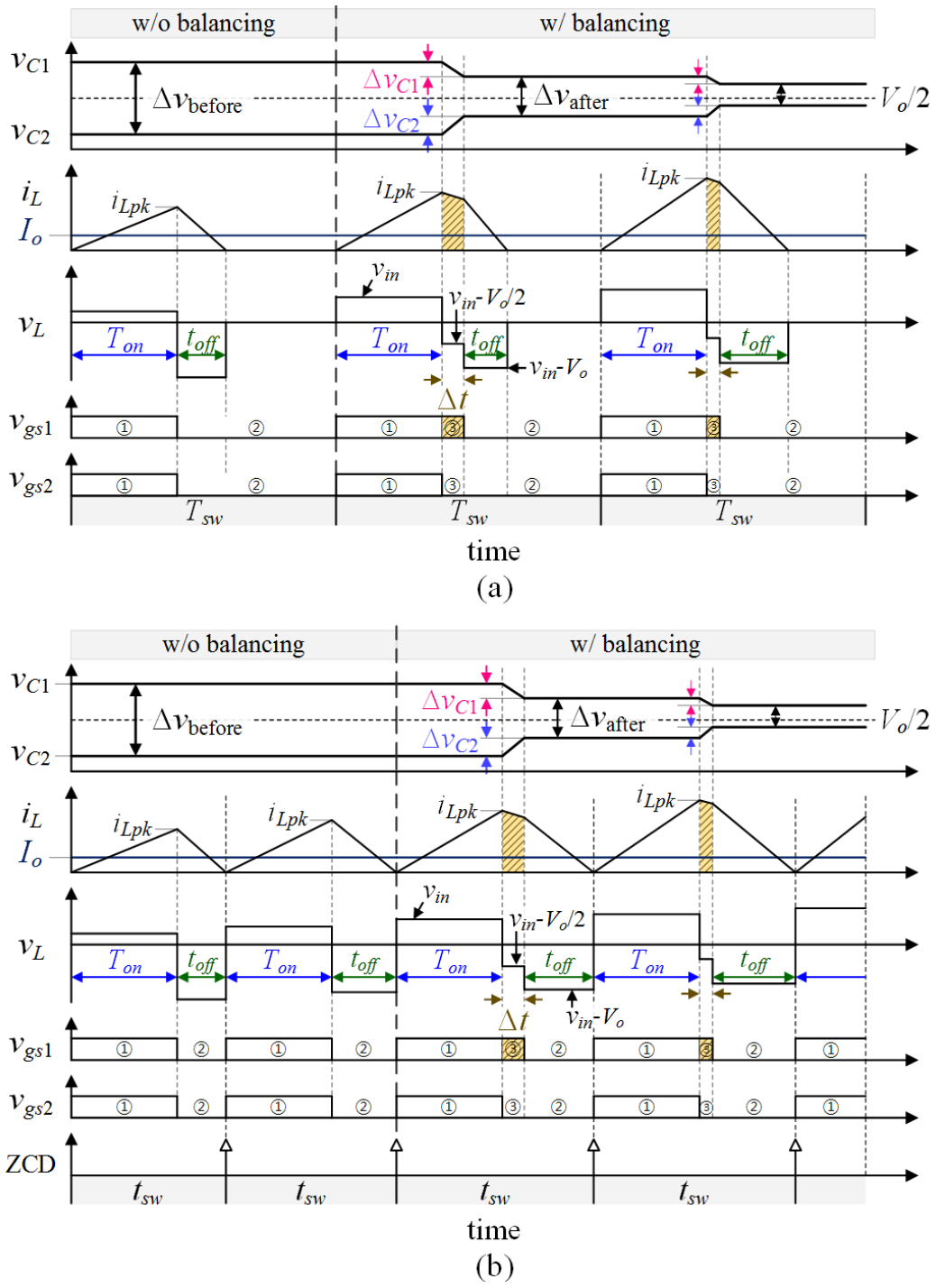


Fig. 6-3. Key waveforms of proposed balancing scheme by control method. (a) DCM. (b) CRM.

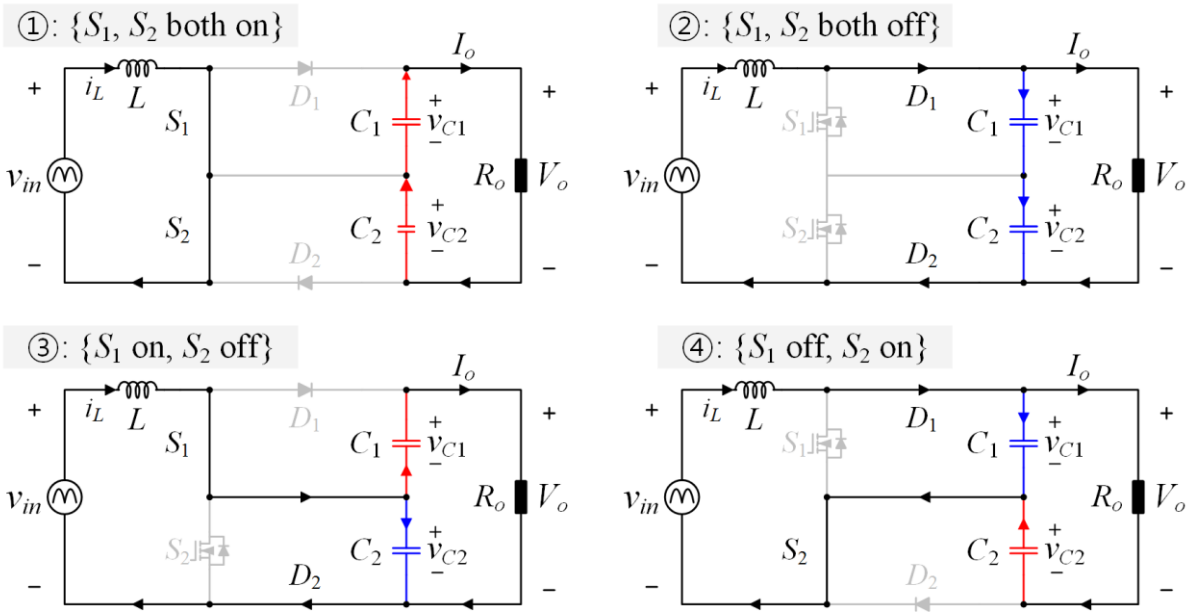


Fig. 6-4. Charging and discharging operation by switching state.

The basic function is to adjust on-time of the selected switch S_1 to longer or shorter than the other switch's on-time in each sampling cycle, depending on instantaneous unbalance condition. The on-time difference and capacitor voltage difference shown in Fig. 6-3 can be formulated first by (47).

$$\begin{aligned} \Delta t &= T_{on.1} - T_{on.2} \\ \Delta v &= v_{C1} - v_{C2} \end{aligned} \tag{47}$$

For the assumed unbalance condition $v_{C1}>v_{C2}$, the proposed method in Fig. 6-3 extends the on-time of S_1 longer than that of S_2 to realize the third switching state which is {S_1 on, S_2 off} of Fig. 6-4; then, the two capacitor's current flows for Δt period become opposite so that C_1 is discharged and C_2 is charged, respectively. Thus, the voltage difference Δv can be reduced during the duration by the three-level modulation.

From the operation principles in Fig. 6-3 and Fig. 6-4, the reduction amount of voltage difference can be calculated as follows. First, the effect of adding Δt interval on each output capacitor can be computed by (48) under the assumption that Δt is much shorter than T_{on}.

$$\begin{aligned} \Delta v_{C1} &= \frac{i_{C1}}{C_1} \cdot \Delta t = -\frac{I_o}{C_1} \cdot \Delta t \\ \Delta v_{C2} &= \frac{i_{C2}}{C_2} \cdot \Delta t = \frac{\left(i_{Lpk} - I_o\right)}{C_2} \cdot \Delta t \end{aligned} \tag{48}$$

where I_o is the output current. Since it is hard to know exact capacitances and use the values for control, both capacitances C_1 and C_2 in (48) are assumed to be manufacturing nominal parameter C. Though the assumption can cause some numerical error, the parameters are still in equal orders so that derived equations will be in technically acceptable range. Then, the voltage unbalance amount after Δt interval in Fig. 6-3 becomes (49).

$$\Delta v_{\text{after}} = \Delta v_{\text{before}} - \left(\left|\Delta v_{C1}\right| + \left|\Delta v_{C2}\right|\right) = \Delta v_{\text{before}} - \left(\frac{i_{L.pk}}{C} \cdot \Delta t\right) \tag{49}$$

From the equation, a relationship between the added interval Δt and expected voltage reduction can be organized by (50).

$$\Delta v_{\text{reduced}} = \left|\Delta v_{\text{after}} - \Delta v_{\text{before}}\right| = \frac{i_{Lpk}}{C} \cdot \Delta t = \frac{v_{in} T_{on}}{LC} \cdot \Delta t \tag{50}$$

It can be interpreted in a way that if the master-switch S_1 is conducted alone for Δt interval, the unbalance voltage will be reduced by $\Delta v_{\text{reduced}}$ in the switching cycle. Further, if the instantaneous voltage difference Δv is known by measuring v_{C1} and v_{C2}, and substitute for $\Delta v_{\text{reduced}}$ in (50), required length of interval Δt^* can be expressed by (51).

$$\Delta t^* = \frac{LC}{v_{in} T_{on}} \cdot \Delta v \tag{51}$$

By calculating and providing Δt^* to the master-switch S_1 in real-time, the output capacitor voltages can be balanced in average.

However, after achieving balanced voltages in steady-state operations, there still remains non-zero Δv in ac line cycles due to the double-line-frequency ripple difference shown in Fig. 6-5. Since the different voltage ripples of v_{C1} and v_{C2} are originated from tolerance of capacitances and capacitive terms in (46), the non-zero Δv is unavoidable even under balance.

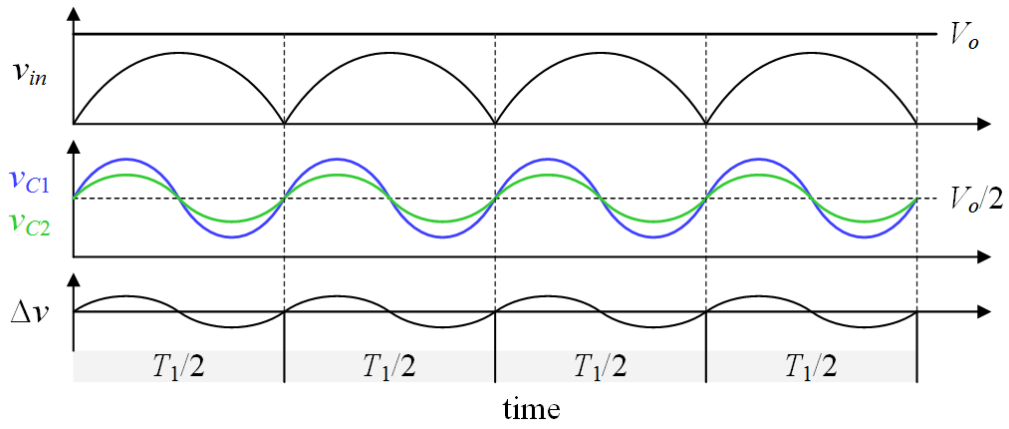


Fig. 6-5. Double-line frequency ripples at balanced voltage condition.

Digitally implemented balancing scheme in DCM and CRM control structures are shown in Fig. 6-6. As can be seen, the control block diagrams in Fig. 6-6 are almost same to those of DCM and CRM control diagrams in Chapter 3–5. The only added parts are calculation blocks using (51) and feedforwarding path of Δt^* to gate signal of the master-switch S_1. Due to the simplicity, relative merits of the proposed scheme are easy implementation and low control complexity, compared to other balancing controls introduced in Table 6.1.

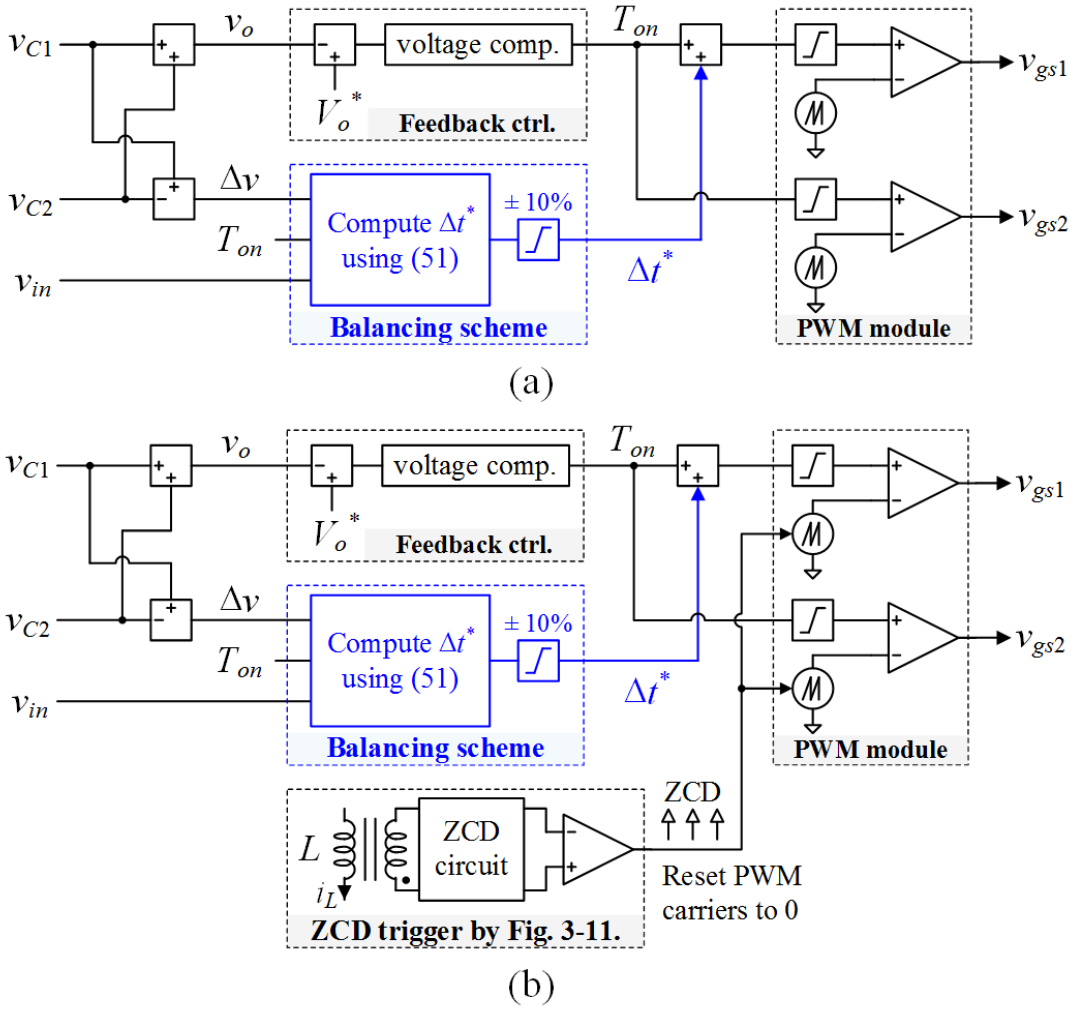


Fig. 6-6. Control block diagram of proposed balancing scheme by control method.

(a) DCM. (b) CRM.

At the output of calculation block for Δt^*, limiters exist. It is essential because input voltage v_{in}, which varies from zero to peak value, is part of denominator in (51). Therefore, the value of Δt^* frequently goes infinite so that limiter is necessary for safe operation; the limits can be set by ±10% of T_{on} to validate the assumption of (48) and to get stable transition without instability. It can be noted that all the information in the key solution (51) can be provided by measurement and feedback compensation in each sampling cycle. For example, v_{in} and Δv can

be measured by voltage sensors; T_{on} is resulted by output compensator. Thus, the proposed balancing scheme can be executed in each sampling period based on the information.

Until now, the case of $v_{C1}>v_{C2}$ is only considered in this section. For case of $v_{C1}<v_{C2}$, the proposed method is still valid since negative Δv in (51) will make the on-time of master-switch $T_{on.1}$ shorter than $T_{on.2}$, adding an interval of {S_1 off, S_2 on} in Fig. 6-4.

As a summary, a flowchart of proposed balancing scheme in one sampling cycle is shown in Fig. 6-7. The procedures are as follows: ***1)*** Input-output voltages are sensed. ***2)*** Common on-time T_{on} is generated from feedback compensator. ***3)*** Desired reference Δt^* is calculated by (51) and goes through the limiter. ***4)*** The length of Δt^* is added on T_{on} and feed-forwarded to PWM action qualifier. ***5)*** The master-switch will turn on for $T_{on}+\Delta t^*$ while the other switch will remain on for T_{on} duration.

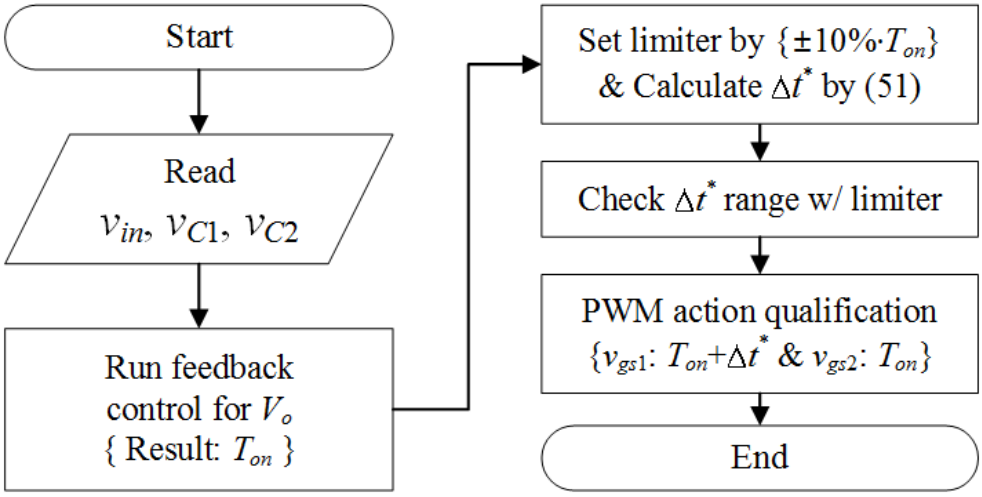


Fig. 6-7. Flowchart of proposed balancing algorithm.

6.4 Experimental Results

The voltage balancing scheme based on toggling of switches (section 6.2) is already verified by multiple sets of experiments in Chapter 3–5. In this section, the other approach based on adjusting the master-module switch in section 6.3 is verified by experimental results. The detailed experimental specifications by control method are summarized in Table 6-2.

Table 6-2. Experimental Specifications.

	DCM	CRM
v_{in}	110 V_{rms} (0–155 V_{pk})	
V_o	400 V	
P_o	300 W	
f_1	60 Hz	
C_1	403 μF (-14.2%)	
C_2	519 μF (+10.4%)	
S_1–S_2	IPW60R041P6 (Infineon)	
D_1–D_2	C4D10120D (Cree)	
DCU	TMS320F28377D (TI)	
L	65 μH	230 μH
f_{sw}	100 kHz	variable switching

For the two output capacitors, 470-μF electrolytic capacitors (Panasonic, ECE-T2WP471 [100]) with ±20% tolerance are used. Before the balancing test, the actual capacitances were measured by LCR impedance meter at frequency range of 120 Hz. The measured values of C_1 and C_2 were 403 μF and 519 μF respectively so that the disagreement was 116 μF to each other.

The test conditions of input voltage and power level were 110 V_{rms} and 300 W. The main reason for the selection is that 110 V_{rms} is lower nominal voltage among universal-line standards and 300-W load is about full-load range for ZCS controlled PFC converters. The combination of low input voltage and full load conditions can bring the highest input current condition and the condition is the worst case in terms of output voltage unbalancing. Under the condition, the proposed balancing scheme has been tested.

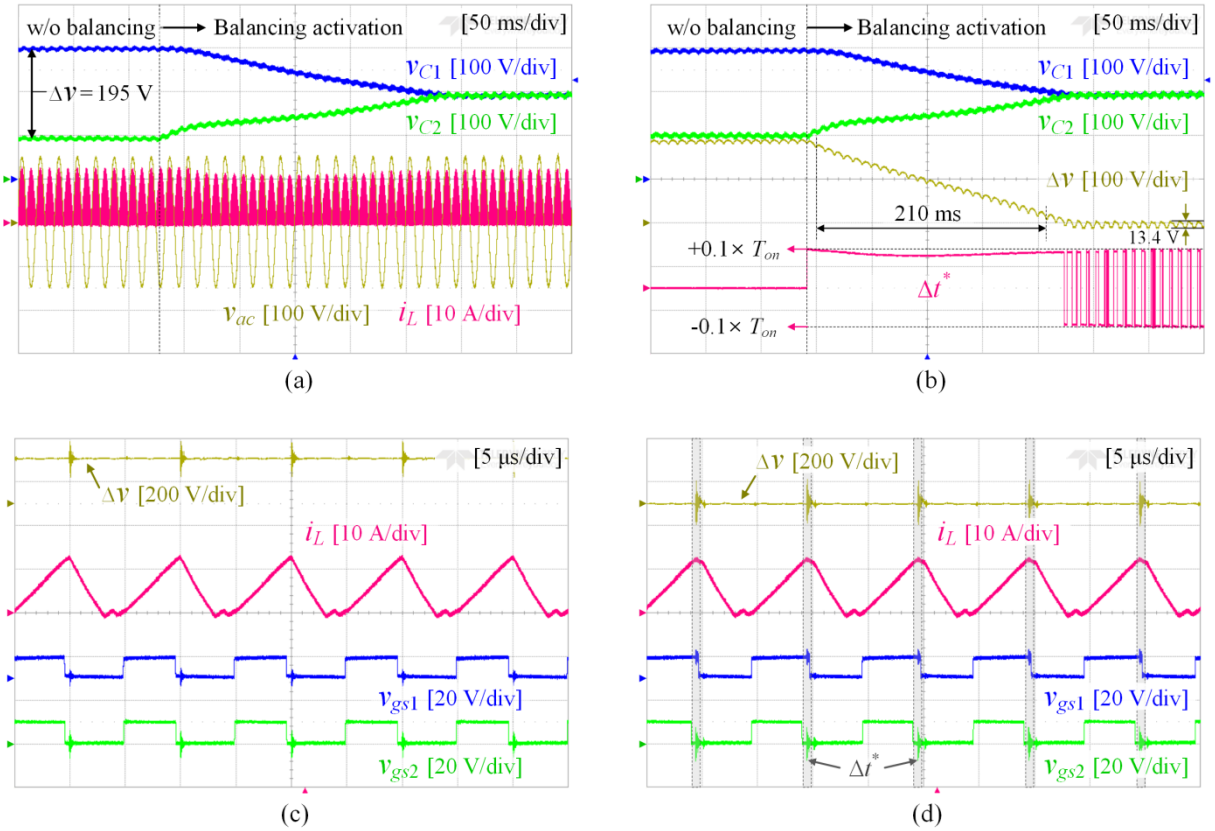


Fig. 6-8. Experimental waveforms of DCM operation with proposed balancing scheme.

(a) transition with input waveforms. (b) transition with control variables.

(c) steady-state without balancing scheme. (d) steady-state with balancing scheme.

In Fig. 6-8, waveforms of TLB DCM PFC with the proposed balancing scheme are shown. As shown in (a)–(b), the voltage difference was about 195 V without balancing scheme. It can be noted that components in the lower-voltage boost cell operate with 102.5-V voltage stresses while components in the other cell experience 297.5-V voltage stresses, even under symmetric operations. However, after activating the balancing scheme, voltage unbalance is resolved. In Fig. 6-8(b), instantaneous voltage difference Δv is plotted by digital-to-analog (DAC) converting function in DSP board; the graph shows that the unbalance level Δv goes down to zero with limited slopes due to the practical limits of ±10% of T_{on}. During the transient period, the feedforward term Δt^* was saturated at the upper limit first due to the huge positive voltage difference by (47). After balanced, Δt^* varies within the limiter boundary; the reference periodically meets the upper and lower limits when PFC input voltage in (51) reach at zero. In Fig. 8(c)–(d), steady-state waveforms with and without the balancing scheme are captured at v_{in}=155 V_{pk} and compared to each other. It can be concluded that adding the gray-boxed three-level interval Δt^* by the proposed scheme can be a simple but effective way to achieve voltage balance of TLB PFC in DCM operations.

In Fig. 6-9, waveforms of TLB CRM PFC are displayed and the unbalanced Δv without balancing scheme was 115 V. The proposed balancing scheme in CRM works the same way as DCM in Fig. 6-8 and the voltage unbalance is also eliminated after multiple line cycles.

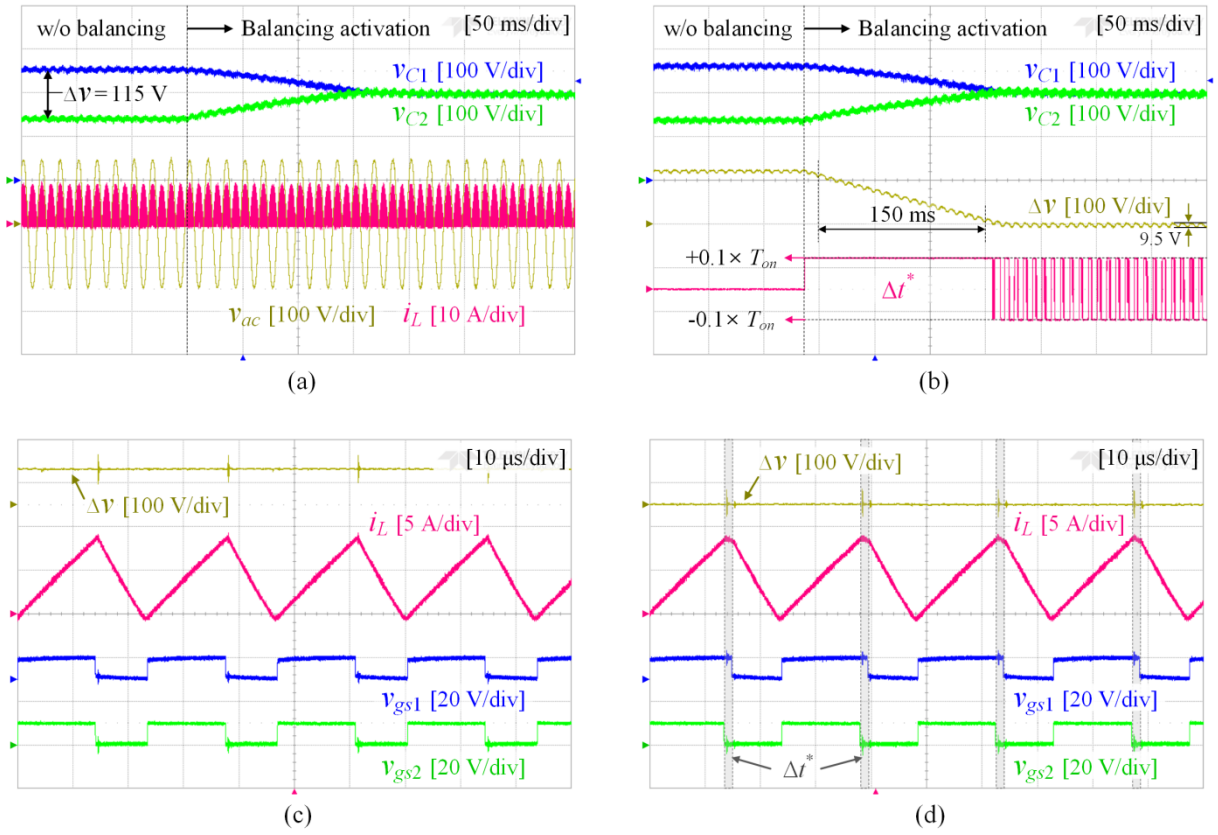


Fig. 6-9. Experimental waveforms of CRM operation with proposed balancing scheme.

(a) transition with input waveforms. (b) transition with control variables.

(c) steady-state without balancing scheme. (d) steady-state with balancing scheme.

In Fig. 6-10 of the next page, efficiency measurement results with and without the proposed balancing scheme are plotted. TLB PFC with the scheme shows improved efficiency in both DCM and CRM cases by 0.09% and 0.14% in average, respectively. From the results, it can be noted that balanced thermal behaviors in two boost cells and small reductions of device turn-off currents lead to efficiency improvement.

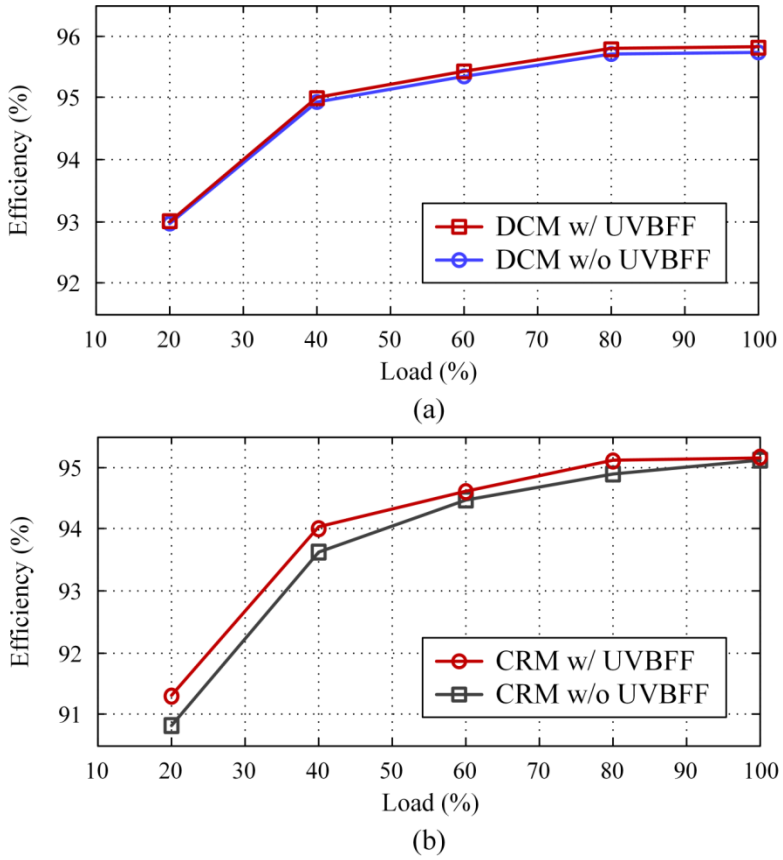


Fig. 6-10. Efficiency curves by control method. (a) DCM. (b) CRM.

6.5 Chapter Summary

In this chapter, the root cause of output voltage unbalance in TLB PFC is firstly discussed and two different directions of balancing principles are introduced. First method is toggling of conducted switch in single-switch on-time period to manage discharging amounts of higher-voltage boost cell's output capacitor. Second approach is selecting one boost cell's main switch as master agent and providing longer or shorter on-time to the switch depending on real-time unbalanced voltage magnitude and polarity. Details of the first method are already analyzed and verified in Chapter 3–5. Operation principle, key equation and experimental results of the second balancing scheme are delivered in this chapter.

Chapter 7.
Conclusion

Demands on universal-line low-power ac-dc power converters have kept growing due to the increasing usages of electronic devices and switch-mode power supplies in modern lives and technologies. Boost-derived PFC topologies have taken major positions in front-end rectifying stages of those applications, pursuing high efficiency, high power density and low system cost at the same time. In order to achieve the goals, representative ZCS control schemes DCM and CRM have been researched in quantities and adopted to real-life systems. Among many boost-derived topologies, TLB PFC converter has been more engaged in high voltage and high power applications rather than universal-line low-power applications. The main reasons and barriers were that TLB topology consists of more component counts than many of two-level boosting PFCs and the increased parts may cause more conduction losses and system cost, while there is no relative merit in terms of waveform quality. However, in previous literatures regarding the topology, there have rarely been papers coming up with effective ZCS control schemes that fully utilize TLB PFC's multilevel characteristics. Since multilevel features beyond two level have been proven to have capability of improving ac waveform qualities in dc-ac inverter applications, this dissertation aims to utilize the inherent three-level characteristics of TLB PFC to improve input ac current waveform qualities (e.g. EMI, harmonics, current stress) than conventional two-level boost-derived PFC converters. From the motivations, a novel three-level current modulation scheme is proposed in this dissertation and applied to both CRM and DCM schemes in various forms. By the proposed modulation, typical drawbacks of CRM and DCM control schemes have been improved. For

example, in this dissertation, high switching frequency losses and poor light-load efficiency of CRM operations are improved by the proposed scheme; high inductor current ripples and corresponding DM EMI amplitudes in DCM operations are mitigated by the modulation. Both ZCS control methods equipped with the proposed scheme are rewarded in common by reduced turn-off currents, mitigated device current stresses, and overall efficiency improvement. Detailed chapter summaries of this dissertation are organized in the next section, followed by potential future works on TLB topology and control schemes.

7.1 Summary by Chapter

In Chapter 1, this dissertation begins with introduction and comparison of boost-derived PFC converter topologies. It is obvious that TLB topology has more converter parts and no relative operational merits by conventional two-level ZCS schemes, compared to many other two-level boosting PFC converters. In addition, there is output-voltage unbalancing problem which only occurs in TLB topology. However, halved voltage-rating requirements on TLB components actually lead to lower unit price of each component. As a result, the cost competitiveness of TLB PFC has been proven with cost comparison from the market values. The limit of operational merits by conventional control schemes becomes research motivations. The objectives of this dissertation are claimed in Chapter 1 with the following three: developing a current control scheme using inherent three-level capability, applying it to DCM and CRM operations, devising simple but effective output-voltage balancing methods.

In Chapter 2, operation principles of TLB PFC converter are analyzed first and additional degree-of-freedom in three-level current-slope shaping is discussed. Then, a novel basic three-level current modulation scheme is proposed based on the TLB characteristics.

Regardless of input voltage range and conduction modes, the basic scheme can be applied to both DCM and CRM operations with the three-level states in a switching period: common on-time, single-switch on-time and common off-time. Various implementation ways and expected effects of the basic three-level scheme are discussed step by step. The root-cause of voltage unbalancing problem, the tolerance of output electrolytic capacitors, is also covered with a survey of practical capacitors on the market.

In Chapter 3, a three-level CRM operation of TLB PFC is proposed based on the basic current control scheme. The key design factor, single-switch on-time, is utilized in a fixed-ratio form throughout ac line cycles. By increasing the portion of single-switch on-time in a switching period, TLB CRM PFC was able to achieve several operation merits including reductions of switching frequency range, switching-related losses, peak inductor current and harmonics. By the changes, the efficiency of TLB PFC with the proposed CRM scheme is also improved. Poor light-load efficiency, which is the typical drawback of CRM-based boosting PFCs, has been improved by more than 1%, achieving higher efficiency than that of conventional two-level boost PFC. Also, overall efficiency curves are boosted so that the efficiency of TLB PFC becomes somewhat comparable to the conventional boost PFC, even with the increased component counts. The improvements of waveform qualities and efficiency at the cost of input PF drop are verified by the experimental results.

In Chapter 4, a three-level DCM operation of TLB PFC is developed based on the basic current modulation in Chapter 2. Different from the CRM operations in Chapter 3, the three-level DCM operations work with fixed-frequency switching framework. It allows more freedom to accurately execute specific functions on physical waveforms. With the feature, the proposed three-level DCM scheme utilizes adjustable single-switch on-time in each switching

cycle. By doing so, inductor current waveform can be extended as close as quadrangular CRM waveforms so that maximized reduction of peak inductor current and efficiency improvement are obtained. In addition, cycle-by-cycle measurement and detection of unbalanced voltages with fixed-frequency switching allow the proposed DCM scheme to change the longer-time conducted switch in each switching cycle so that voltage balancing can be easily achieved. A set of experimental verifications confirmed that maximum 23.6% of peak current reduction and 0.9% of efficiency improvement are measured, compared to conventional two-level DCM control scheme.

In Chapter 5, a novel SSFM technique for boost-derived PFC converters with DCM operation is proposed based on general PLL control-loop. High amplitude of DM EMI noises at concentrated switching frequency is the well-known drawback of DCM boosting PFC converters. In general, the dense EMI noises result in low cut-off frequency of input EMI filter design, causing large size of input filter. By using the SSFM technique, not only TLB PFC but also two-level boost-derived PFCs can have significantly reduced peak amplitudes of DM EMI noises under DCM operations. From the experimental results, the peak amplitude of SSFM with two-level DCM scheme was 97.3 dBμV while the conventional fixed-frequency DCM case showed 110 dBμV peak amplitude at switching frequency. On top of the SSFM, the adjustable three-level DCM control scheme in Chapter 4 is also implemented to TLB PFC prototype and tested. The test results showed that the collaboration of SSFM and adjustable DCM scheme can get further 2.5 dBμV reductions of peak amplitude in the switching frequency band. Thus, the inherent limit of DCM operations and burden of large input filter size have been relieved by the proposed methods. In addition, the SSFM technique in this chapter utilizes a down-ward frequency distribution so that reduction of switching losses is

given as secondary benefit. Experimental results showed that the SSMF technique brought 0.43% average efficiency improvement in overall load range.

In Chapter 6, two directions of output-voltage balancing scheme for TLB PFC is summarized. One direction is to swap the longer-time conducted switch depending on which boost cell has higher output voltage. This toggling approach is implemented to the CRM/DCM control schemes in Chapter 3–5. The other balancing principle is to select one switch as a master agent to manage unbalanced situation. This approach can provide longer or shorter on-time length Δt to the master switch in a feedforward form, based on the real-time measurement of voltage difference Δv. By multiple sets of experiments in Chapter 3–6, the effectiveness of both output-voltage balancing schemes are verified.

7.2 Future Works

In the development process of this dissertation, several challenges and possibilities have been found as follows and left as potential future works.

1) For the three-level CRM control scheme in Chapter 3, the output-voltage balancing performance based on the cycle-by-cycle toggling function is not enough to fully guarantee balanced voltages under increased single-switch on-time T_{α} condition over 30% of T_{on} and corresponding asymmetric boost-cell operations. Also, inherent variable switching frequency of CRM operations can go up to very high region near MHz range depending on input voltage and load conditions. In that case, the sampling frequency of DSP control unit is too low to compensate unbalancing by controlling gate signals at the physical switching frequency. Thus, development of more effective balancing scheme for proposed CRM operation is needed.

2) For both DCM and CRM control schemes proposed in this dissertation, their common trade-off was input PF. The decrement of input PF can get worse if the proposed single-switch on-time or input rms voltage increase. Since detailed mathematical derivation of the index was not covered, the key factor that worsens input PF during the proposed operations is needed to be studied further. Thus, a compensation method to resolve the trade-off can be future work.

3) In this dissertation, core principle of the proposed schemes is asymmetric on-time operations of the switches S_1 and S_2. From the gate signaling, the single-switch on-time period occurs and three-level current modulation capability is brought. However, in the TLB PFC topology, there still remain a chance to extend degree-of-freedom in modulation and control. For examples: (a) Phase angles of the gate signals can be out-of-phase to each other in order to add up interleaving characteristics on the three-level inductor current. (b) Replacing the complimentary passive diodes D_1 and D_2 with active devices can be another degree-of-freedom increment in terms of modulation. By using the totally-active-switching TLB PFC, inductor current can be synthesized even in negative polarity; extended control schemes such as triangular conduction mode (TCM) can be tried to improve waveform qualities or converter efficiency by widening ZVS range.

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