Model Development, Synthesis and Validation Using the Modeler's Assistant

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(ABSTRACT)

This thesis discusses 'Modeler's Assistant', an interactive graphics tool which aids in the rapid development of VHDL models. The tool provides modeling, test bench generation, simulation, synthesis and validation features. The 'Process Model graph' which has representations for the concurrent processes is used as the basis on which the Modeler's Assistant is built. Test generation environment is integrated into the tool. A range of test bench options are provided to the user. The tool interfaces to 'Synopsys' VHDL analyzer, graphics debugger and synthesis tools. Validation of the behavioral model versus the synthesized structural model is also discussed. A detailed programming manual with many examples is provided for the benefit of the user.

To Amma, Anna and Soujanya

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