Bayesian Optimization of PCB-Embedded Electric-Field Grading Geometries for a 10 kV SiC MOSFET Power Module

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ABSTRACT

A finite element analysis (FEA) driven, automated numerical optimization technique is used to design electric field grading structures in a PCB-integrated bus bar for a 10 kV bondwireless silicon-carbide (SiC) MOSFET power module. Due to the ultra-high-density of the power module, careful design of field-grading structures inside the bus bar is required to mitigate the high electric field strength in the air. Using Bayesian optimization and a new weighted point-of-interest (POI) cost function, the highly non-uniform electric field is efficiently optimized without the use of field integration, or finite-difference derivatives. The proposed optimization technique is used to efficiently characterize the performance of the embedded field grading structure, providing insights into the fundamental limitations of the system. The characterization results are used to streamline the design and optimization of the bus bar and high-density module interface. The high-density interface experimentally demonstrated a partial discharge inception voltage (PDIV) of 11.6 kV rms. When compared to a state-of-the-art descent-based optimization technique, the proposed algorithm converges 3x faster and with 7x smaller error, making both the field grading structure and the design technique widely applicable to other high-density high-voltage design problems.

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GENERAL AUDIENCE ABSTRACT

Innovation trends in electrical engineering such as the electrification of consumer and commercial vehicles, renewable energy, and widespread adoption of personal electronics have spurred the development of new semiconductor materials to replace conventional silicon technology. To fully take advantage of the better efficiency and faster speeds of these new materials, innovation is required at the system-level, to reduce the size of power conversion systems, and develop converters with higher levels of integration. As the size of these systems decreases, and operating voltages rise, the design of the insulation systems that protect them becomes more critical. Historically, the design of high-density insulation system requires time-consuming design iteration, where the designer simulates a case, assesses its performance, modifies the design, and repeats, until adequate performance is achieved. The process is computationally expensive, time-consuming, and the results are not easily applied to other insulation design problems. This work proposes an automated design process that allows for the streamlined optimization of high-density insulation systems. The process is applied to a 10 kV power module and experimentally demonstrates a 38% performance improvement over manual design techniques, while providing an 8 times reduction in design cycle time.

Dedication

Dedication goes here.

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List of Abbreviations

$\boldsymbol{E}(\cdot)$ Electric Field Vector

$\boldsymbol{K}(\cdot,\cdot)$ Covariance Matrix

ϵ Dielectric Constant (Permittivity)

η Field Intensity Factor

λ Field Grading Coefficient

$\mathbb{E}(\cdot)$ Expectation

$\mathcal{N}(\cdot,\cdot)$ Normal Distribution

$\mathcal{P}(\cdot)$ Probability

$\Phi(\cdot)$ Cumulative Normal Density Function

$\sigma^2(\cdot)$ Variance Function

ε Singularity Buffer

$\vec{x}$ Optimization Variables

$a(\cdot)$ Acquisition Function

$E(\cdot)$ Electric Field Magnitude

$f(\cdot)$ Cost Function

h_{min} Minimum Mesh Element Size

$m(\cdot)$ Mean Function

p Penalty Term

$V(\cdot)$ Scalar Electric Potential Field

$W(\cdot)$ Electric Field Energy

BD Break Down (Dielectric Breakdown Strength)

BEM Boundary Element Method

EI Expectation of Improvement

FEA Finite Element Analysis

FEM Finite Element Method

FOS Factor of Safety

GP Gaussian Process

GPR Gaussian Process Regression

LCB Lower Confidence Bound

PD Partial Discharge

PDIV Partial Discharge Inception Voltage

PI Probability of Improvement

POI Point of Interest

UCB Upper Confidence Bound

WBG Wide Bandgap

Chapter 1

Introduction

1.1 Project Overview

The ever-evolving field of power electronics requires new innovations in device packaging to further improve density, efficiency, and reliability of future power conversion systems. Emerging topics such as renewable energy, electrification of transportation, and hybrid electric aircraft, require new levels of package integration, and improved wide bandgap materials to deliver higher performance at lower costs.

The high degree of integration and compact form factors of future power electronics packages present new design challenges. Package subsystems that could once be designed by independent teams now require comprehensive co-design in the same room and, in some cases, the same equation. The increasing density poses significant insulation design problems, especially as device blocking voltages climb to 10 kV and greater on a single device.

This work will focus on the solution to one such insulation problem, specifically the intense electric field that forms around the power terminals of a high-voltage power electronics package. The proximity and sharp geometries of the power terminals present a significant reliability concern due to intense electric field crowding, which allows partial discharge to slowly degrade the insulation performance over the lifetime of the package. Successful mitigation of this risk is key to further improving density and reliability of high-voltage insulation

systems.

The design of high-density insulation systems is non-trivial, due impart to difficulties in modeling, the intricate geometric structures, and the complexity of experimental verification. The proposed work adds to this by introducing a PCB integrated field grading structure which, while alleviating field crowding, further increases modeling and design complexity.

Historically, high-density insulation systems are designed using an iterative, manual design technique which requires extensive input from the designer. For a typical design case, the designer would select an appropriate insulation structure based on past experiences, simulate the design case, assess the performance graphically, and then iterate. The design is re-simulated, then re-assessed, then tweaked again, repeating until an acceptable design is achieved. The process is laborious and time-consuming, while commonly resulting in sub-optimal performance, long cycle times, and single-point designs that are not easily transferred to other systems.

The first version of the proposed PCB-integrated field grading geometry was designed in this manner and, upon realizing its shortcomings, a numerical optimization process was derived to streamline design, and ensure optimal performance given a set of design constraints. Numerical optimization has been used in the design of insulation systems before; however, the applications of these techniques to highly nonuniform electric fields (such as those observed around the package power terminals) has several challenges. Most notably, non-uniform electric fields typically result in poor optimization domains, that are difficult for conventional techniques to navigate.

In the state-of-the-art, it is common to use sophisticated heuristic techniques such as neural networks and swarming algorithms to navigate the non-convex and discontinuity-ridden optimization domain. The claim of this work is that the poor quality of the domain is simply a

symptom of the more fundamental problem, that is computational error in the FEA solution. This work will seek to improve on the state-of-the-art by introducing mechanisms to deal with the error directly, and inherently improve the efficiency of the workflow by addressing problems rather than symptoms.

A similar symptom/problem relationship can be seen in state-of-the-art cost functions, such as field integration techniques, which sacrifice computational efficiency and cloud physical interpretation, in the name of reducing the impact of FEA noise. To expand on this, field integration techniques rely on minimizing the energy contained in the electric field, which lacks a clear physical interpretation when compared to engineering design requirements, such as minimum partial discharge inception voltage. The cost function is inherently inefficient as it relies on the electric field intensity of the entire domain, rather than at the locations that ultimately limit system performance.

On a fundamental level, the contribution of this work is an automated optimization workflow for high-density insulation systems that addresses the problems, rather than the symptoms of the problems, in a way that is both intuitive and easily implemented with off-the-shelf software packages.

1.2 Research Objectives

The objective of this work is to develop an automated design and optimization workflow that directly addresses the challenges associated with the optimization of high-density insulation systems with highly nonuniform electric fields. The workflow should be implemented with commercially available software with an emphasis on simplicity, to allow for widespread adoption. Complexity will be added strictly on an as-needed basis. Additionally, priority will be given to those techniques which allow for clear physical interpretation, and afford

insights into the fundamental trade-offs and limitations of the system.

The proposed workflow should utilize:

1. An FEA solver due to wide spread availability of both open-source and commercial offerings and the general familiarity with the technique in the field.

2. A cost function that directly relates to pertinent design and material properties, while being computationally efficient and highly scalable to large 2D and 3D arbitrary geometry.

3. An optimization technique that prioritizes simplicity and ease of integration while directly addressing the associated challenges of highly nonuniform electric fields, most notably the lack of accurate derivative information, the computational error from the FEA, and the potentially non-linear and non-convex nature of the domain.

The workflow will be demonstrated on PCB embedded field grading structures in a high-density module interface for a 10 kV SiC multi-chip power module. Verification of the design will take place in the form of experimental partial discharge testing. The benchmark for the study will be a previous version of the bus bar (also designed as part of this work) designed exclusively with manual, iterative techniques. The goal is to achieve a partial discharge inception voltage (PDIV) of the system greater than the 10 kV voltage rating of the multi-chip power module.

The following chapter will provide a detailed review of the motivation for this work, as well as a survey of state-of-the-art numerical design techniques and their shortcomings when applied to highly nonuniform electric field problems. This will be followed by a chapter on the formulation of a novel cost function and Bayesian optimization as a means of addressing these shortcomings.

The design workflow will be applied to the optimization of PCB-integrated field grading geometry for a high-density, 10 kV, 80 A SiC MOSFET power module. The interface will be verified experimentally in a partial discharge test setup and compared to the manually designed version of the interface. The work will conclude with a discussion of impact, and how the work can be extended to other applications in power electronics packaging.

Chapter 2

Background

The advantages of high-voltage power electronics are increasing steadily, and with them, the urgency for adoption is growing [4]. The electrification of consumer and commercial vehicles has increased the demand for high-frequency power conversion at 400 V, 800 V, and 1.2 kV voltage levels on a global scale [4][5]. Renewable energy and green grids demand more cost-effective and efficient, mega-watt-class power conversion systems with ultra-high reliability[6][5]. All-electric war ships and carrier ships are exploring the use of micro-grids powered by renewable and fossil sources which will require high-voltage dc transmission systems enabled by lightweight, high-frequency dc-dc converters [7][8][9]. More electric aircraft (MEA) and hybrid power trains require ultra-high efficiency variable frequency drives (VFD) paired with high current battery charging solutions [10][11][12].

For decades, silicon (Si) has been the standard in power electronics, with a range of medium-voltage, and high-voltage active devices available such as field-effect transistors (FET), bipolar junction transistors (BJT), insulated gate bipolar transistors (IGBT), integrated gate-commutated thyristors (IGCT), gate turn-off thyristors (GTO), and emitter turn-off thyristors (ETO) that are widely used and exhaustively researched [13]. These devices benefit from their long history and proven track record, allowing for ease of availability and support, streamlined manufacturing, and well-understood performance characteristics [10].

However, new and emerging applications have required engineers and scientists to push the boundaries of these technologies, bringing several key limitations to light, most notably

switching speed, blocking voltage, and high-temperature performance [14]. The switching speed of bipolar Si devices, and even more so with unipolar Si devices, is ultimately limited by the low saturation drift velocity of the material [15]. The low drift velocity limits the on-state resistance and switching speed, increasing conduction and switching losses. The low switching speed and higher on-state loss of the devices manifest in higher device counts for a given current rating, increased complexity and size of the cooling system, and larger passive components to filter the low-frequency switching noise [16].

The temperature rating of commercial Si devices is largely determined by their high intrinsic carrier concentration. As the temperature of the device rises, the increased carrier concentration provided by the dopants degrades until only the intrinsic carrier concentration remains [17]. Other factors affecting thermal performance include the thermal conductivity of the material which is one of the limiting factors of expelling heat to the ambient. The low thermal conductivity of Si requires cooling systems to maintain lower ambient temperatures and places a lower bound on active area density, which in turn increases device manufacturing cost [18].

Historically, the blocking voltage of high power Si devices such as IGBTs, IGCTs, and GTOs has been limited to 6.5 kV in the commercial market [19]. The presents a significant concern as high-voltage dc distribution systems in microgrids, MEAs, and electric ships push to voltages exceeding 20 kV [12]. With existing Si technologies, multiple active devices must be used in series to achieve the desired blocking voltage. This results in complicated multi-level converter topologies requiring advanced isolation and control techniques[19]. To ensure acceptable reliability, multi-level topologies require the voltage to be carefully shared across all devices and thus must use additional high-voltage passives and significantly de-rate the devices, further penalizing power density [20].

In light of these concerns, wide bandgap (WBG) materials such as silicon carbide (SiC),

gallium nitride (GaN) and gallium oxide (Ga_2O_3) have entered the market as a potential solution [21][22][23]. As the name implies, WBG materials have a larger band gap, typically greater than 3 eV, compared to the 1.12 eV of Si. This directly affects the materials ability to block higher voltages over a smaller drift layer, increasing device blocking capability while lowering on-state resistance [17].

2.1 Silicon Carbide in Power Electronics

Of the available WBG materials, SiC has emerged as the preferred technology in high-voltage active devices [24][25][26]. Unlike its GaN counterpart, SiC does not suffer from dynamic R_{ds-on} characteristics that can easily lead to thermal runaway if not properly managed [17]. In addition, SiC can be readily doped as both n-type and p-type, which is not necessarily true for all WBG materials, allowing for the fabrication of both unipolar and bi-polar devices [27]. Thus far, bipolar SiC devices have demonstrated up to 15 kV although it is commonly accepted that the reasonable limit of SiC bipolar technology is between 10 kV and 15 kV as above 15 kV the R_{ds-on} of the device becomes prohibitively large [28]. Unipolar SiC, however, is anticipated to reach a voltage level of 20 kV and greater with a single device [29].

Figure 2.1 shows how SiC compares to Si and other WBG materials in terms of five key material properties: bandgap, saturation drift velocity, electron carrier mobility, electric field breakdown strength, and thermal conductivity. In addition to the high drift saturation velocity, as discussed earlier, the high thermal conductivity is another significant driver behind the adoption of SiC technology [30]. Of all the WBG materials shown in Figure 2.1, SiC has the highest thermal conductivity. This is critical as high-voltage devices require thick passivation layers, making their fabrication very expensive. Improved thermal conductivity allows higher active area densities, reducing total die area and, in turn, reducing

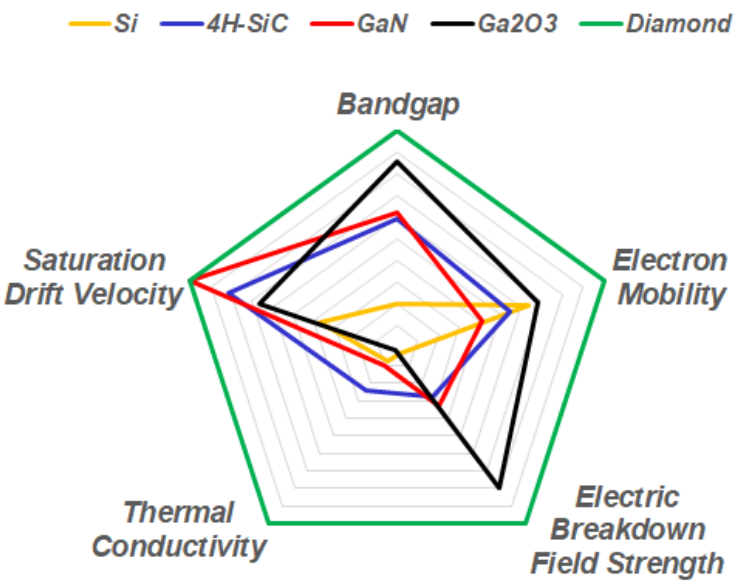


Figure 2.1: Radar plot showing the five key material properties of WBG semiconductors compared to diamond.

manufacturing costs [18].

In the literature, SiC MOSFETs up to 15 kV [31][32], as well as 20 kV IGBTs[33] have been demonstrated, although SiC MOSFET development has been the primary focus of the research community given their potential to dramatically reduce converter footprint[22][34]. CREE has been at the forefront of this effort, having debuted its first-generation 10 kV 123 mΩ devices in 2004 [35] that demonstrated switching characteristics at 1.4 A with a leakage current of 197 μ at 10 kV. This was followed by a 10 kV, 5 A device [36], 10 A devices in 2010 [37] and, more recently, third-generation 10 kV, 20 A and 15 kV, 10 A devices which have experimentally demonstrated an R_{ds-on} below 300 mΩ with a leakage current less than 100 nA at 10 kV V_{ds} [38]. These devices have been tested externally, in integrated packages in both academia and industry.

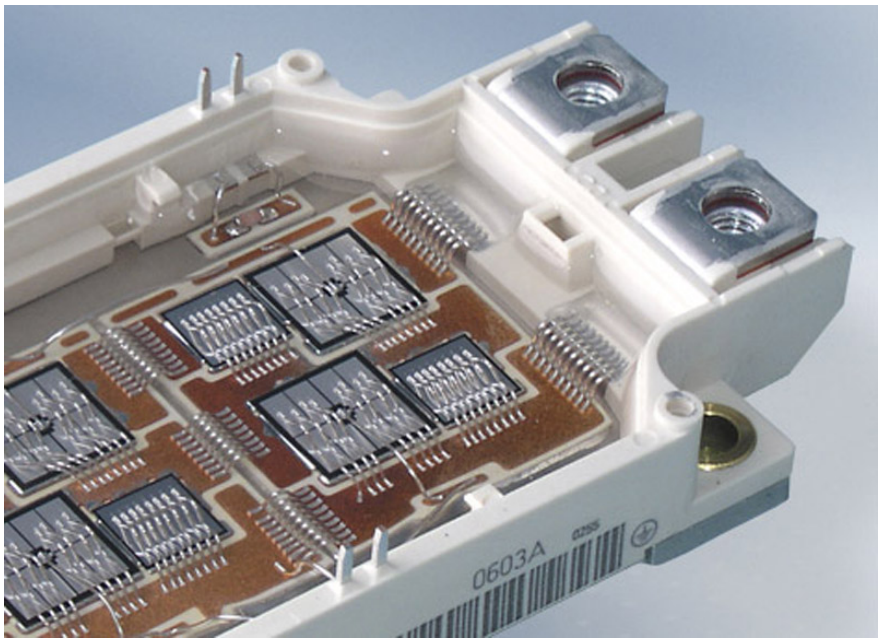


Figure 2.2: Vincotech FZ06NPA070FP SiC IGBT/diode buck module showcasing conventional packaging technology as applied to SiC devices [1].

2.2 High-Density Integrated Packaging

Translating the desirable performance characteristics of high-voltage SiC MOSFETs to the package and system levels requires new, innovative packages that improve on the shortcomings of traditional packaging technologies. To take advantage of the increased switching speed, higher blocking voltages, and improved thermal conductivity, it is critical to ensure that the package is not the limiting factor [39]. It is widely accepted that packaging technology represents the largest barrier to widespread adoption of high-voltage SiC devices [40].

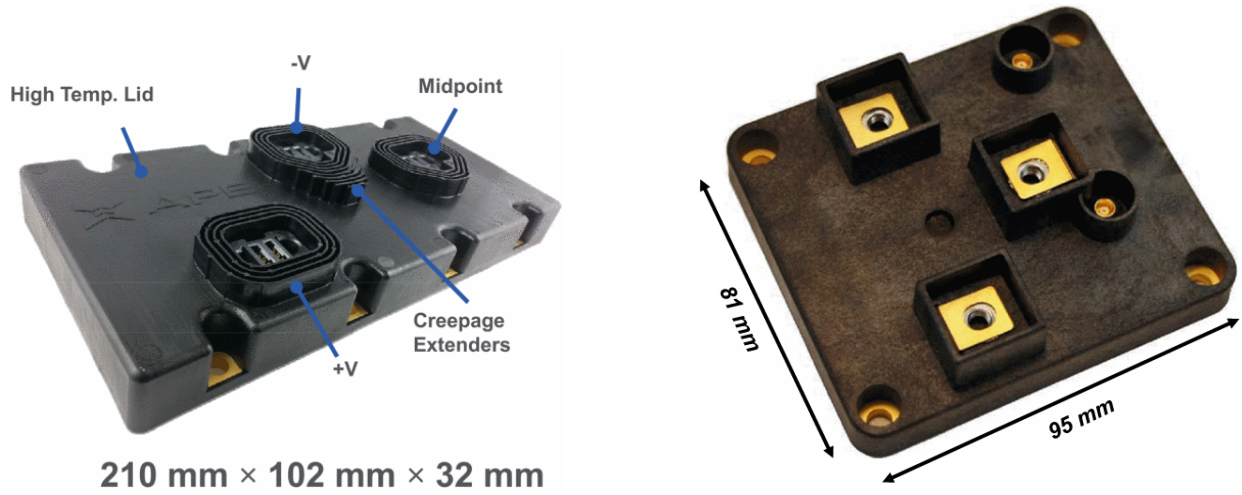
Conventional packaging technology, such as the one shown in Figure 2.2 falls short of the needs of WBG devices for several key reasons: junction-to-case thermal resistance θ_{jc}, commutation loop inductance L_p, gate loop inductance L_g, creepage distance, and noise immunity. The θ_{jc}, as well as the case-to-ambient thermal resistance θ_{ca}, if not minimized, will

quickly dominate the impedance of the heat flow path, voiding the positive effects of SiC's high thermal conductivity [3]. Typical packages rely on Al_2O_3 and Si_3N_4 direct bonded copper (DBC) substrates as the device mounting surface due to their high fracture toughness and reasonable thermal conductivity [41]. The die are mounted to the substrate using solder, and then the substrate is mounted to a heat spreader of some variety, usually copper, for interfacing to the cooling solution. This stack-up topology not only presents thermal concerns, due to the sub-optimal thermal conductivity of the ceramic and the die-attach, but also presents reliability concerns due to the CTE mismatch of ceramic and bonded metallization [42].

Both L_p and L_g are affected by the trace and interconnect layout, as well as by the use of bondwires. Typical Si-based power modules have a higher tolerance for stray inductance due to the lower switching speed. However, as the transition time increases, the added stray inductance not only throttles speed, but also increases current/voltage overshoot and ringing, resulting in de-rated performance and higher conducted noise emissions from the package [43].

Maintaining adequate creepage distances between the power terminals is also a concern. Because Si devices rarely exceed a 6.5 kV voltage rating, conventional package footprints and the employed insulation materials cannot withstand the increased electric field intensity that comes with devices rated above 10 kV [19]. To reduce the electric field intensity and maintain adequate creepage distances, the package size must be increased, with terminals and traces spaced further apart, penalizing both power density and stray inductance [44].

To addresses these concerns, several innovative packages have been proposed in the literature. Unfortunately, many details for proposed packages are not yet available as many are still early in the development phase, with a few exceptions. In 2015, APEI demonstrated a 15 kV SiC power module (Figure 2.3) capable of 120 A continuous operation with eight parallel



(a) (b)

Figure 2.3: a) APEI multichip power module based on eight parallel 15 kV SiC devices and rated for 120 A continuous operation; b) ARL 20 kV, 30 A SiC IGBT power module measuring 81 x 95 x 25 mm^3 [2].

devices [2]. The module used integrated temperature sensors and was rated for an operating temperature of 200°C. The module employed a high-temperature solder for die-attach and a stacked substrate topology with bondwire interconnects. It was developed as a benchmark for a similar SiC package developed by ARL. The ARL package (Figure 2.3b) was based on 20 kV SiC IGBTs from CREE.

CREE has also developed packages for their third-generation 10 kV SiC MOSFETs in both 240 A (Figure 2.4) and 90 A variants [45]. The 240 A variant employs 24 parallel devices in a chopper configuration and utilizes bondwires with a high-temperature solder die-attach. This package from CREE was one of the first to be designed with a high-voltage laminate bus bar in mind. The terminals were designed to allow for the use of a laminate bus bar as opposed to a conventional copper bus bar as a means of reducing commutation loop inductance outside of the package. This package/bus bar configuration was successfully demonstrated in [46]. While the laminate bus bar helps, the need to honor the creepage and clearance distances at 10 kV ultimately determines the size of the package, resulting in poor

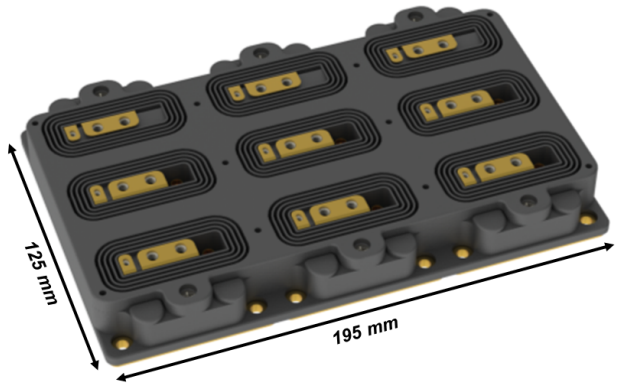


Figure 2.4: CREE 10 kV, 240 A package based on third-generation 300 mΩ SiC MOSFETs measuring 195 x 125 x 23.5 mm^3.

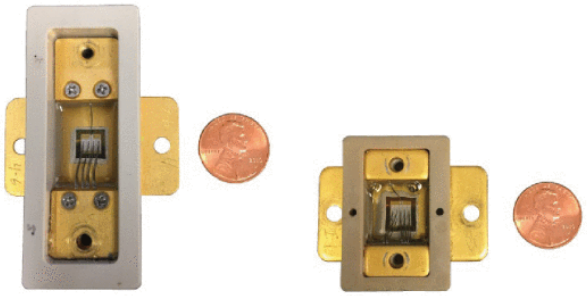


Figure 2.5: Texas Tech University (left) 15 kV SiC MOSFET discrete package and (right) 20 kV SiC IGBT discrete package.

power density.

Texas Tech University has developed discrete packages based on 15 kV SiC MOSFETs and 20 kV IGBTs (Figure 2.5) from CREE [33]. These packages were built and tested specifically for pulsed power applications and make use of a PCB integrated bus bar as well. However, unlike the CREE module, adequate creepage and clearance distances cannot be maintained between the terminals and thus the entirety of the interconnect must be encapsulated during operation. This yields an improvement in the power density of the CREE module, but sacrifices system modularity as a result.

As a solution to the creepage/density trade-off, an 80 A, 10 kV SiC MOSFET phase leg

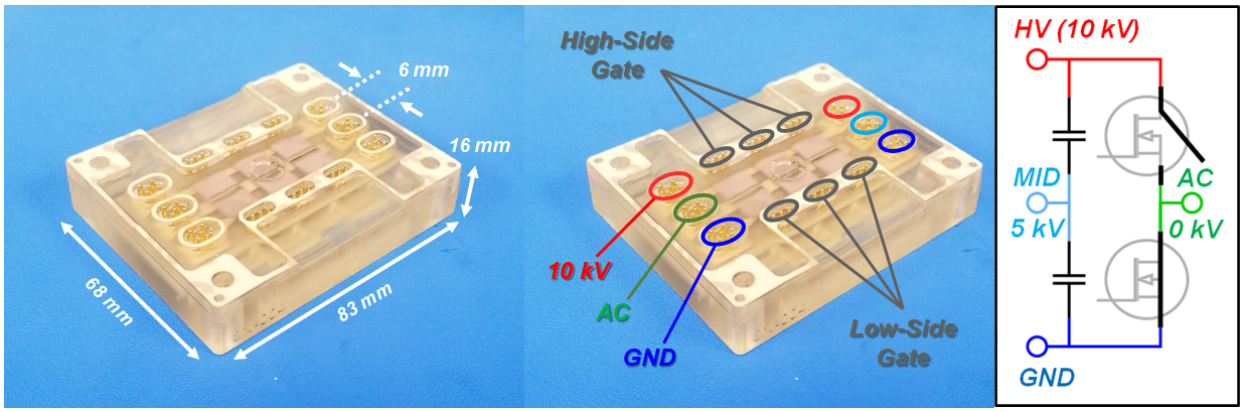


Figure 2.6: 10 kV, 80 A bondwire-less SiC MOSFET power module phase leg from CPES.

(Figure 2.6) was proposed by CPES in 2019 which employed an innovated terminal design to void the creepage and clearance requirement while maintaining both high power density and system-level modularity [43]. The power module voids the clearance requirement by fully enclosing the spring pins and thus eliminating any in-air path between the terminals. Since there is no in-air path between the terminals, standard creepage distances are not required.

Figure 2.7 shows a cross-section of the module that illustrates this concept. The figure shows the spring-pin interconnects attached to the substrates of the module and interfacing with the PCB bus bar. Each cluster of spring-pins is fully enclosed by the housing, encapsulant, and bus bar, removing any in-air path between the terminals.

The result is a dramatic decrease in terminal spacing. The UL-840 standard for insulation coordination of medium voltage equipment requires a minimum creepage distance of 40 mm for a 10 kV system [47]. The CPES power module reduces this by 85% to only 6 mm, resulting in a record power density [44].

This approach of creepage mitigation does have some limitations. Creepage extenders, as shown on the CREE power module in Figure 2.4, can be specified for any range of voltage, altitude, and environmental pollution degree [47]. Existing experimental verification and design of the fully-enclosed interface in Figure 2.7 has only taken place in a laboratory

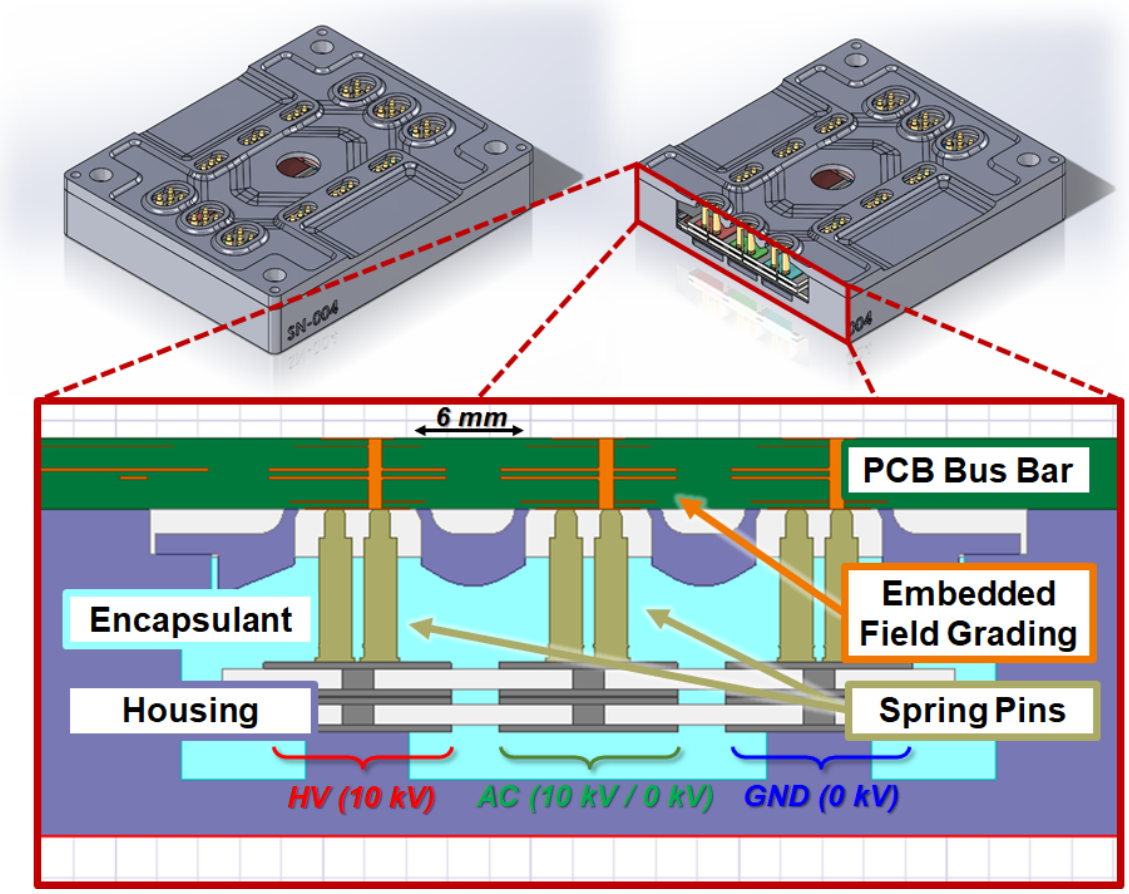


Figure 2.7: Cross-section of the CPES bondwire-less 10 kV, 80 A SiC power module (Figure 2.6 on pg. 14) with PCB integrated bus bar and embedded field grading geometry (Figure 2.9 on pg. 19). Housing is used in conjunction with PCB bus bar to fully enclose each terminal, removing the in-air path and voiding the creepage and clearance requirement.

environment with a pollution degree of 1 [3].

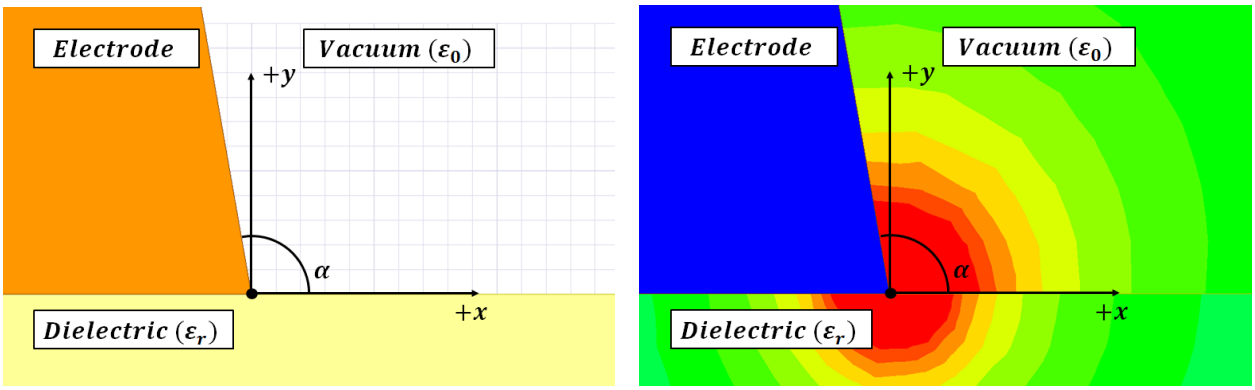
The proximity of the spring-pins results in high-intensity electric field around the interface. Any surface contaminants or environmental pollutants could result in premature failure of the system. Additional work is required to verify the insulation performance of the interface in high-pollution environments. This work will not focus on the pollution degree problem but rather the high-intensity electric field problem.

Even in a low pollution degree environment, the electric field intensity is high enough to exceed the breakdown strength of air, resulting in partial discharge and potential breakdown around the interface. Mitigating this issues requires the use of embedded field grading structures inside the PCB bus bar. This work will focus on the design, optimization, and test of these embedded structures in a low pollution degree environment.

2.3 Electric Field Grading

Electric field grading structures are most commonly found on a macroscopic scale in high-voltage insulation systems such as transmission cable terminations [48][49][50] and on a microscopic scale as edge terminations on high-voltage semiconductor devices [51][52][53]. Field grading is achieved by one or more of three key mechanisms: 1) resistive field grading, where the field is graded by varying conductivity of the material; 2) permittivity grading, where the permittivity of the material is varied, and 3) capacitive grading, where geometry is varied to manipulate where the electric field lines terminate [54].

The purpose of field grading is to alleviate the electric field crowding that occurs as a result of sharp geometry, or a junction of two or more dissimilar materials [55]. Figure 2.8 shows an example of a composite junction of a conductor placed on a flat dielectric and



(a) (b)

Figure 2.8: a) Composite junction of an electrode placed on a flat dielectric and exposed to air, known as a triple-point; b) an electrostatic field simulation showing the electric field intensity increase around the triple-point. ($\alpha = 110°$, $\varepsilon_r = 4.4$, and $V = 1$ kV)

exposed to ambient, commonly referred to as a triple-point due to the interaction of three dissimilar materials. The field intensification caused by triple points and composite junctions poses a significant partial discharge risk and can lead to premature insulation degradation or destructive breakdown if the electric field intensity exceeds the dielectric breakdown strength of any of the materials [56].

While triple-points have been studied extensively over the past 30 years, there is a significant knowledge gap in their electric field behavior, especially under high-frequency excitation such as the high-voltage PWM signals generated in SiC converters [57]. This is due predominantly to the fact that field crowding is a microscopic phenomenon that is a strong function of geometry and thus is largely dependent on variations in manufacturing and materials, surface roughness, defects, and environmental conditions [58]. Deriving analytical expressions for these arbitrary geometries is time-intensive and sometimes prohibitively so, and thus experimental results are typically the driving factor of design on a case-by-case basis [59].

The power module shown in Figure 2.6 employs a PCB-integrated bus bar where the internal

traces are used as a capacitive field grading structure. Triple points are located on the surface of the PCB where the copper trace is in contact with both the air and the FR-4 dielectric as shown in Figure 2.9 [3]. The structure works by manipulating the electric fields in the air, redirecting them to terminate inside the FR-4 dielectric. The FR-4 has a significantly higher breakdown electric field strength of 20 kV/mm (compared to the 3 kV/mm average strength of air) and thus can support the intense electric field without significant PD [60].

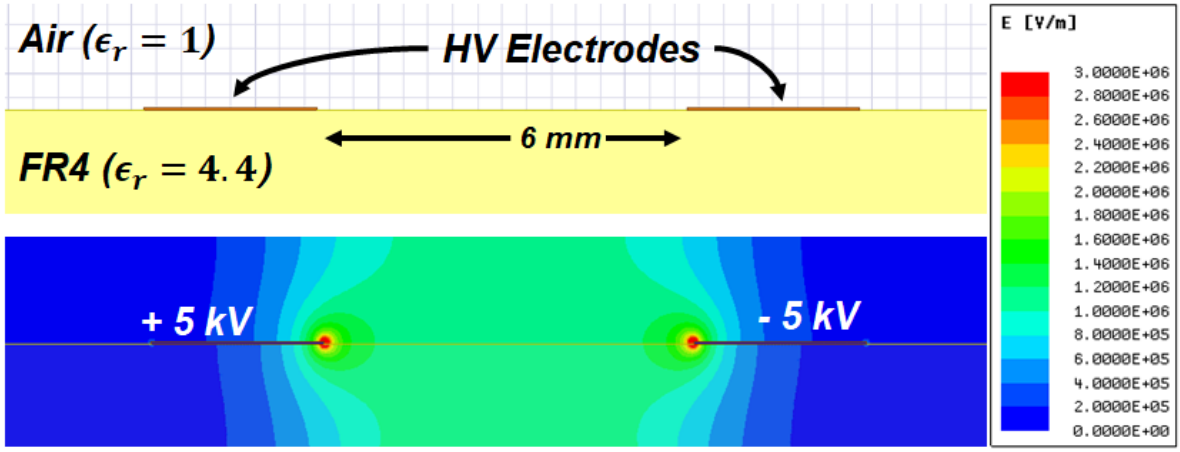
Similar embedded field grading structures have been employed in other PCB and laminate bus bars but only to reduce electric field crowding around the edges of the bus bar, never to grade the field around the terminal [61][62].

A cross-section of the bus bar with field grading mated to the bondwire-less package is shown in Figure 2.7. The proposed design eliminates the need to adhere to standard creepage and clearance distances by using the module housing in conjunction with the bus bar to eliminate any in-air path between the terminals. The resulting field crowding is then alleviated using the embedded field grading and the module housing geometry [58].

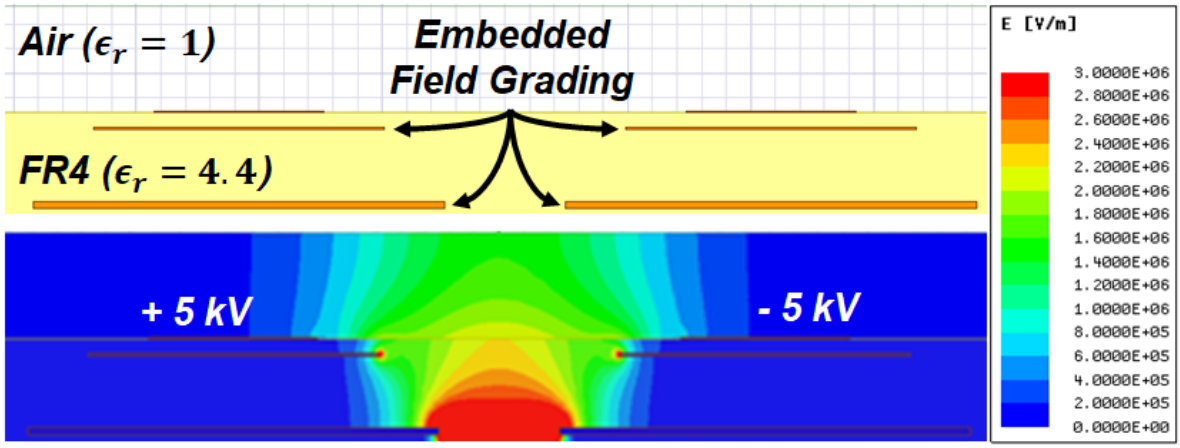
The design, characterization, fabrication, and test of this field grading structure will be the focus of this work. The following section will provide a review of design techniques and methodologies used in the optimization of field grading and insulation systems, focusing primarily on automated numerical optimization techniques.

2.4 Numerical Optimization

Typically, field grading structures, and non-uniform fields in general, are designed using a manual optimization technique, where design variables are swept independently and their impact is assessed graphically [63][64][65][66][67]. When the geometric complexity of the



(a)



(b)

Figure 2.9: The capacitive field grading structure proposed in [3] to mitigate the high electric field intensity around the terminals of the CPES 10 kV SiC MOSFET power module (shown in Figure 2.6 on pg. 14)

system is high and the design variables cannot be visualized in a few dimensions, numerical optimization techniques have been employed. Historically, when the problem is non-convex, neural networks have been used [68][69][70][71] and more recently, genetic [72] and particle swarm algorithms [73][74][75]; however, the usefulness is often limited by long simulation times, large training sets, and marginal insulation performance improvements.

Descent-based algorithms have been used sparingly and are intended to improve the computational efficiency but have been met with varied success [76][77][78][79]. When used in conjunction with an FEM solver, descent-based techniques can exhibit poor convergence due to non-physical shallow minimums and finite-difference derivative errors stemming from singularities in the domain [80][55].

To improve the convergence of descent-based techniques, and smooth the domain of more sophisticated algorithms, field integration cost functions have been used [81]. This class of cost function works by calculating the energy W contained in the electric field using Gauss's law

$$W = \frac{\epsilon}{2}\left(\int_{\mathcal{V}} E^2 d\tau + \oint_{\mathcal{S}} V\boldsymbol{E}\cdot d\boldsymbol{a}\right) \tag{2.1}$$

where ϵ is permittivity, $\boldsymbol{E}$ and V are the electric field and scalar potential field respectively, $\int_{\mathcal{V}}$ is the volume integral over the domain, and $\oint_{\mathcal{S}}$ is the surface integral around the domain [82]. The optimal design is that which minimizes the energy contained within the electric field. The integration of the field requires a finely resolved mesh over the entire domain which significantly increases the computational load of the FEM as well as the integration.

Another approach to improve convergence is to use a solver more conducive to singularities, such as a boundary element solver (BEM) [83][84]. A BEM technique can accurately resolve singularities by only discretizing and solving the boundaries; however, they typically require material properties that are not readily available from PCB manufacturers [59]. Besides,

BEM solvers are not readily available in commercial software packages such as ANSYS Electronics Desktop® and MATLAB®.

2.5 Summary

This chapter provided the necessary background and survey of the state-of-the-art which will lay the foundation for the following chapters. A discussion of the shortcomings of conventional Si active devices was presented along with the key advantages of WBG materials and how they address these shortcomings. The higher thermal conductivity, drift saturation velocity, bandgap, and breakdown voltages of SiC make it particularly attractive as a replacement for Si devices in high-density, high-voltage power converters. High-voltage SiC MOSFETs have been gaining popularity in the research community with commercial offerings from CREE demonstrating blocking voltages of 15 kV with conduction resistance on the order of 300 mΩ and reverse leakage on the order of 100 nA.

Packaging technology was discussed, specifically the limitations of existing packaging technologies and the resulting barrier to electrical performance. A survey of state-of-the-art SiC MOSFET packages was discussed including designs from CREE, ARL, APEI, and CPES. The bondwire-less 10 kV package from CPES was discussed along with some of the innovative techniques and design elements used, most notably the PCB-integrated bus bar which enables a power terminal spacing of 6 mm. The tight terminal spacing and high power density of the CPES module is made possible by the embedded field grading structures inside the PCB which work in conjunction with the module housing to alleviate electric field crowding around the terminals.

The need for electric field grading was discussed along with a demonstration of the field crowding that occurs as a result of triple-points and composite dielectric junctions. An

overview of field grading techniques and their applications was presented, both in general and as applied to PCB bus bars for high-density converters. The chapter concluded with a survey of field grading design techniques. Manual design techniques were discussed along with a survey of numerical optimization techniques such as neural networks, genetic algorithms, and descent techniques and their shortcomings.

The following chapter will present in detail the numerical optimization procedure developed specifically for the efficient optimization of embedded field grading structures; however, it can be generalized to many non-uniform electric field design problems. A detailed overview of the optimization challenges will be discussed along with a derivation of the cost function and overview of Bayesian optimization.

Chapter 3

Optimization Theory

The miniaturization trends of modern power electronics systems require more advanced, more efficient design strategies to ensure safe, reliable operation at higher power densities and higher operating voltages. The increased power density comes with new risks for partial discharge, insulation degradation, and destructive breakdown if the high-density insulation systems are not carefully designed. Simplicity in both the design and the design process is pivotal to the widespread adoption of high-density, high-voltage power conversion systems.

The previous chapter discussed the key aspects of high-voltage power modules that currently limit density, as well as the associated design challenges that come with mitigating these limitations. Regions such as triple points and composite junctions both inside and outside the power module cause highly nonuniform electric fields which increase the risk of partial discharge and premature failure. Typical manual design techniques are time-consuming and yield single-point designs that are not easily transferred to other systems.

This chapter presents an overview of the underlying theory and techniques which enable the numerical optimization of highly nonuniform electric fields in high-density power electronics applications. A detailed overview of the challenges of non-uniform electric field optimization is presented, followed by a discussion of the proposed mitigation strategies. Then, a derivation of the cost function and a detailed description of Bayesian optimization and its advantages is discussed.

3.1 Optimization Challenges

The following sections detail three of the primary challenges of applying automated numerical design techniques to the design of high-density insulation systems for non-uniform electric fields as well as a discussion on how each of these will be mitigated with the proposed optimization scheme.

3.1.1 Geometric Complexity

Geometric complexity is the first of three main challenges of applying numerical optimization. In high-density power electronics modules and systems, a high degree of geometric complexity is a given and can pose a significant design challenge for several reasons. Most notably, parametric modeling in 3D is time-consuming and can yield complex constraint matrices which are non-trivial to derive and time-consuming to debug. These complicated constraint matrices can slow convergence rates, increase iteration times, and most importantly, cloud the insights into system performance that numerical optimization affords [85].

A critical advantage to the proposed numerical optimization technique is that it affords the designer insights into the fundamental trade-offs that exist in a system that is otherwise void of any governing equations. Numerical optimization provides the designer a means to quickly optimize a design for a broad range of operating points or requirements and build intuition as to the fundamental limitations, and behavior of the system. Increased geometric complexity and complicated constraint matrices can cloud these insights and thus will be avoided in this work.

To that end, the proposed technique will focus mainly on the optimization of simplified 2D cross-sections as opposed to full feature 3D models. While the proposed cost function

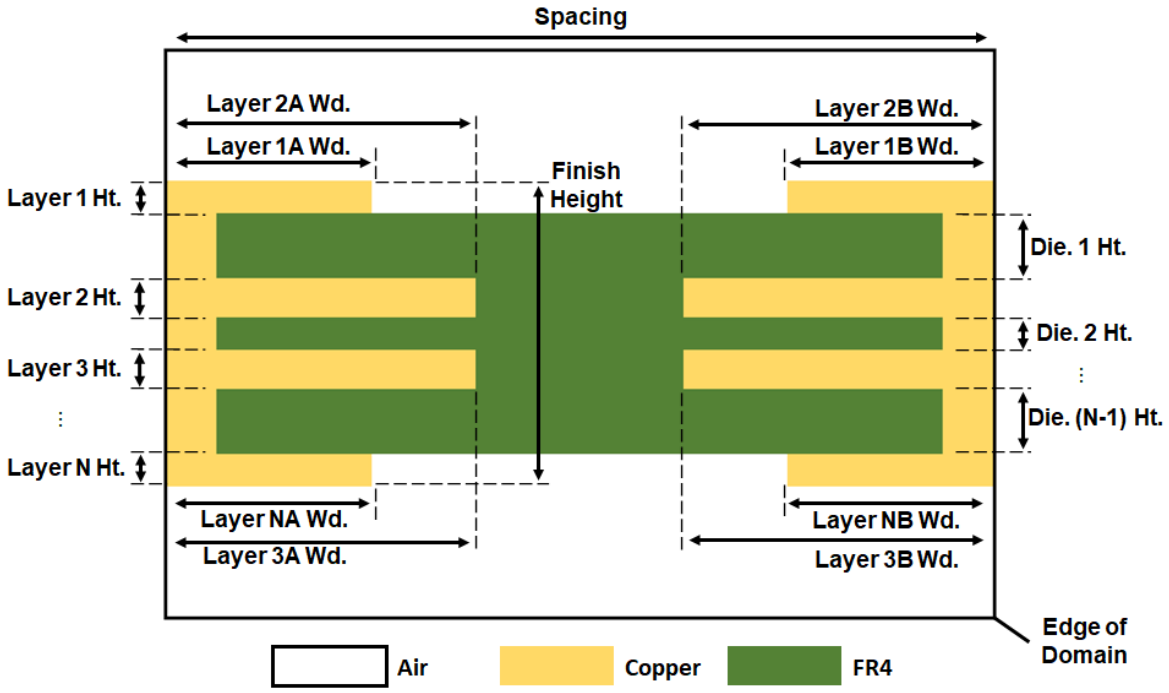


Figure 3.1: Decomposed 2-D model of the 4-layer embedded field grading structures from Figure 2.9 (pg. 19) with key design parameters.

(Section 3.2) is scaleable to more complex 3D geometry, this will not be the focus of this work. Geometries of interest, such as the embedded field grading structure of Section 2.3 will be decomposed into 2D cross-sections. These cross-sections will be further simplified by the use of symmetry.

Figure 3.1 shows an example of a 2D decomposition and parameterization of a 4-layer embedded field grading geometry. Even in a 2D representation, this simple structure still contains 17 design variables. Using symmetry and thoughtful constraints, this can be reduced to only two optimization variables and two fixed variables as shown in Figure 3.2. The total height of the PCB stack-up is fixed, and the spacing between the terminals is fixed. The height and the spacing are taken to be non-optimizable design parameters. The height of the copper layers is fixed at 1.4 mils (1 oz.) thick for all layers and symmetry is assumed along both the X-axis and Y-axis.

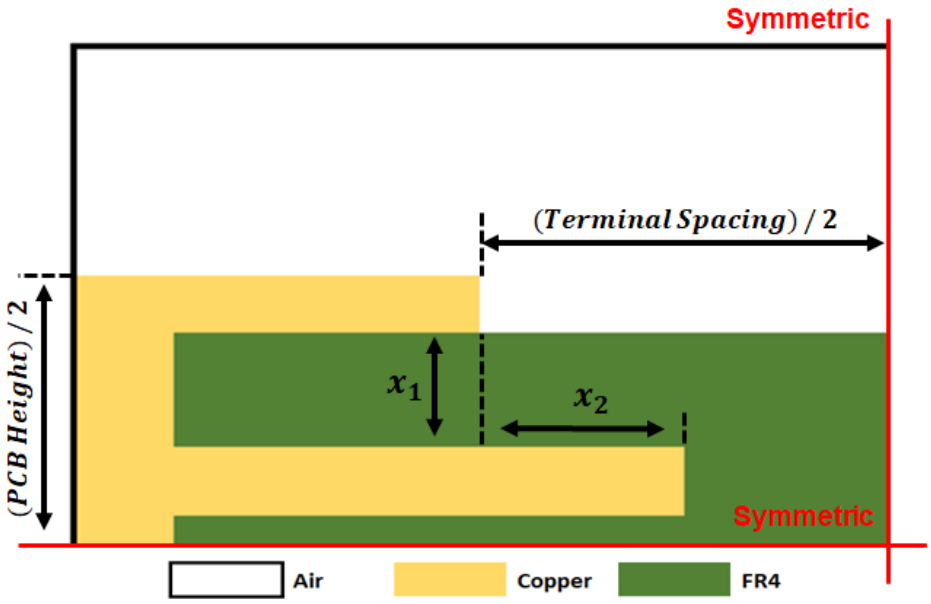


Figure 3.2: Simplification of 4-layer embedded field grading geometry to only two optimization variables: dielectric height x_1 and plate width x_2; and two fixed design variables: terminal spacing and PCB height.

Simplifying the geometric structures in this manner not only helps to protect the valuable insights into system performance but accelerates the design cycle time with faster FEM simulation times, faster iteration times, and simpler parametric modeling and constraint matrices.

3.1.2 Singularities

The second major challenge that must be addressed is the presence of singularities in the computational domain. Singularities in the context of this work are regions or points in the 2-D computational domain where the derivative is undefined [85]. This is critical as electric field FEM solvers typically solve for the potential field ϕ according to Poisson's equation (Eq. 3.1) for electrostatics. The electric field is then calculated as the gradient of the scalar potential field. [82] If the derivative is undefined at a location, then the quantity of interest,

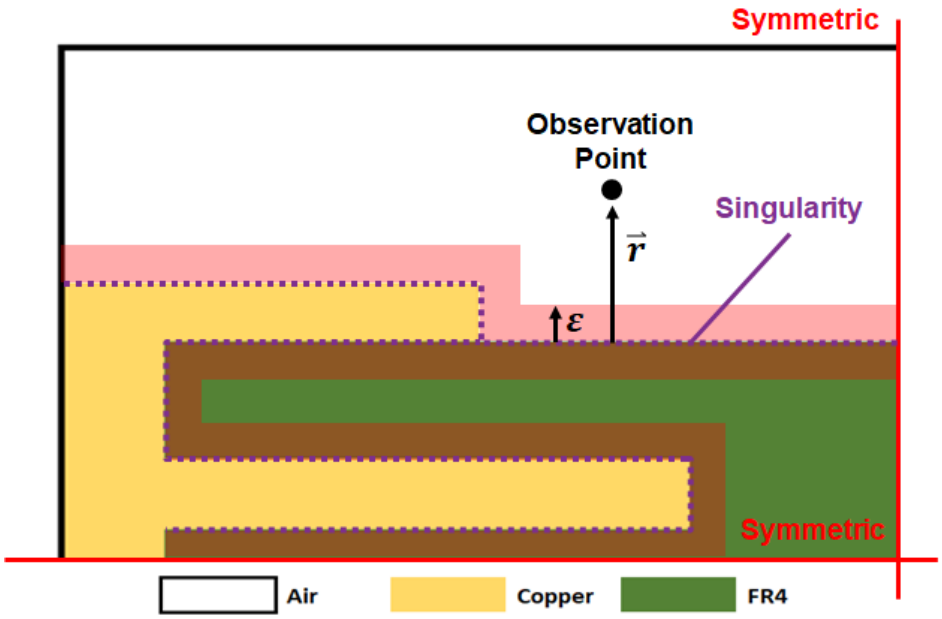


Figure 3.3: Buffer term applied to the 4-layer field geometry. Data observed at the observation point is only valid if $|\vec{r}| > \epsilon$ where $\vec{r}$ is the distance to the observation point normal to the boundary.

electric field, is also undefined.

$$\nabla^2\phi = 0 \quad \rightarrow \quad \boldsymbol{E} = -\nabla\phi \tag{3.1}$$

As addressed in Section 2.4, there are several ways around this problem such as using an analytical solution [55] or a BEM solver [59][83][84]. While both BEM and analytical approaches allow for accurate prediction of electric field strength around singularities, the point of this work is to build qualitative models that capture the behavior of relative design variations as opposed to predicting the exact partial discharge performance of a given design variant. In this way, the proposed design strategy utilizes relative performance as opposed to absolute performance.

To that end, a simpler technique is used which allows for the capture of relative changes

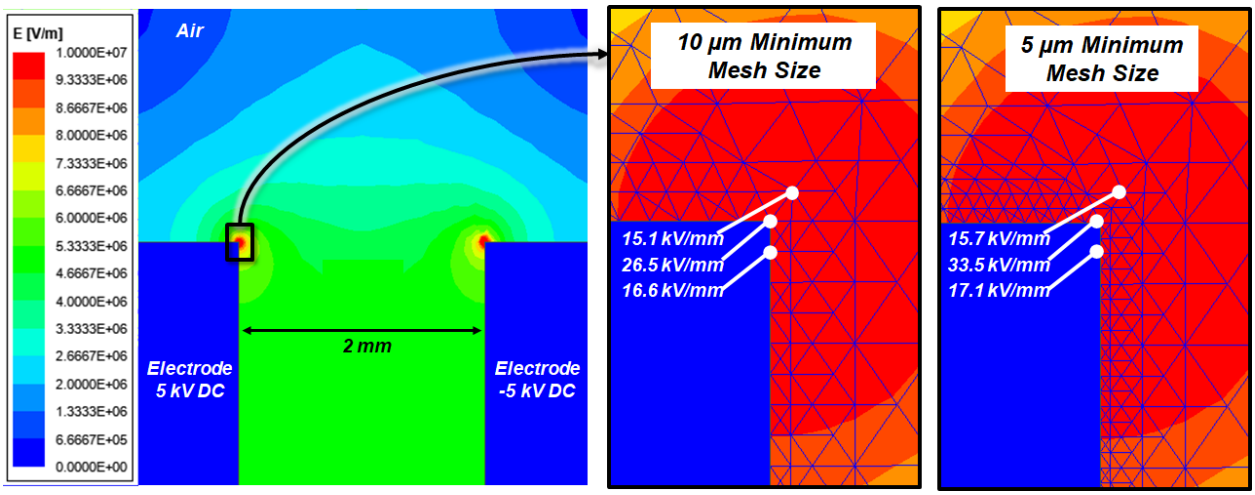


Figure 3.4: Variations in meshing result in significant variation in electric field strength across a range of observation points. ($\varepsilon_{air} = 1$)

in behavior and can be easily implemented in commercial FEM software. This technique employs a buffer term ϵ which sets the buffer around the singularity, within which, no data should be collected [86]. Figure 3.3 shows the implementation of the buffer term. which is selected to be small enough to accurately represent the field intensification but large enough to ensure the result is stable.

Figure 3.4 illustrates the instability of the electric field magnitude near singularities when computed using an FEM technique. In this example, the minimum mesh element size around the singularity is taken to be 10 μm and 5 μm in order to stimulate a small variation in mesh node placement. The peak electric field is measured at three mesh points and the electric field strength varies significantly from 26.5 kV/mm to 33.5 kV/mm at one of the sense locations. Further impacts of mesh dependency on singularities and the other regions of the domain will be discussed at length in Section 3.1.3. The effect of ϵ on the peak electric field strength has been studied extensively in the literature and it is decided that an appropriate value of ϵ for geometry of this scale is 15 μm [86]. From this point on, ϵ will be taken as 15 μm unless otherwise stated.

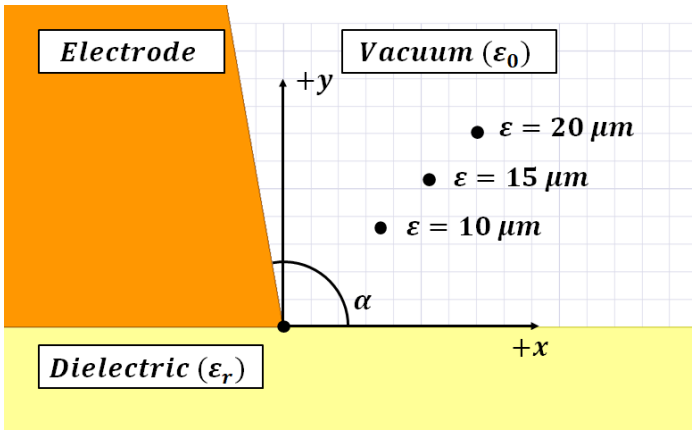


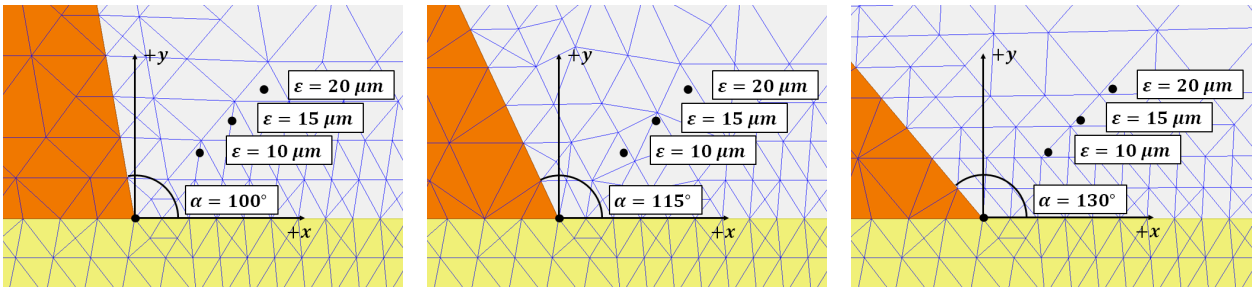
Figure 3.5: Schematic of a typical composite junction of an electrode on a flat dielectric where α is the contact angle and three observations points are defined at ϵ = 10, 15, 20 μm respectively. (Simulated with electrical properties listed in Figure 2.8 pg. 17)

3.1.3 Mesh Dependency

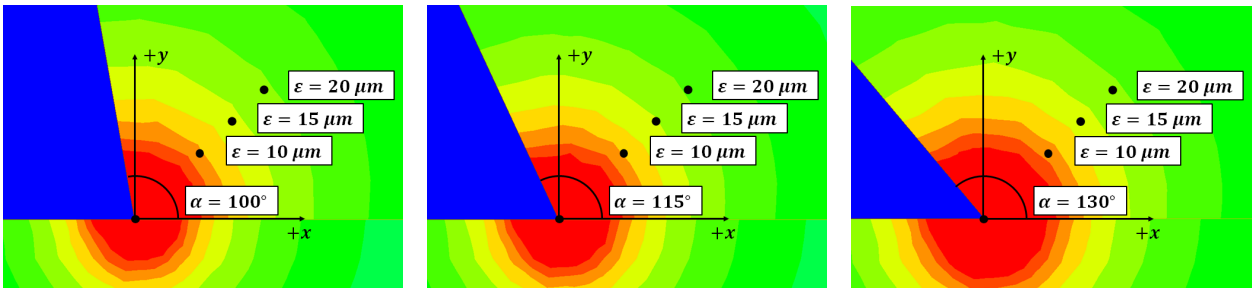
The third and final major challenge that must be addressed is the dependency of the solution on the mesh. This builds on the previous section in that these issues stem from the presence of singularities in the computational domain but adds a discussion of data corruption and noise that permeates the cost function as a result of the mesh-dependent singularities.

Figure 3.4 showed how the peak electric field strength varies with minimum element size. While this is a concern, it can be mitigated by setting a small minimum mesh size ($h_{min} < \epsilon$) around the singularity and maintaining this constraint throughout the optimization process.

This section will discuss how the calculated electric field strength at singularities can vary with minor shifts in mesh position. The shifts in mesh position as design revisions are re-meshed throughout the optimization process. For example, Figure 3.5 shows a typical composite junction (triple point) formed by an electrode placed on a flat dielectric in a vacuum ambient environment with a given contact angle α. This structure has been studied extensively for electron beam formation in vacuums and electrical discharge prevention in laminate insulation structures [62][87].



(a) Mesh Plot ($\alpha = 100°$) (b) Mesh Plot ($\alpha = 115°$) (c) Mesh Plot ($\alpha = 130°$)

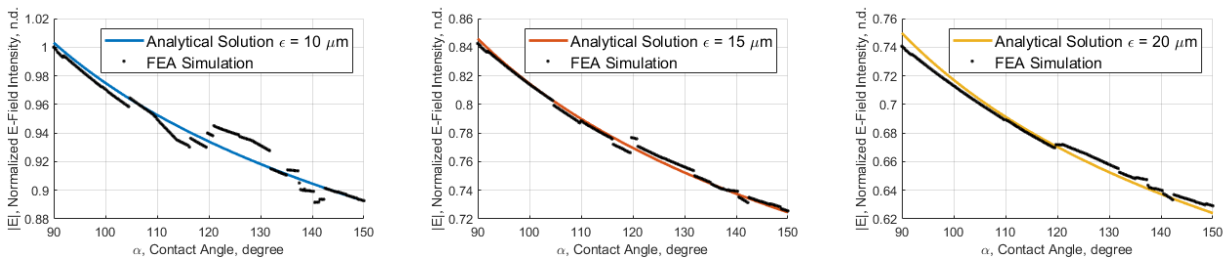


(d) E-Field Plot ($\alpha = 100°$) (e) E-Field Plot ($\alpha = 115°$) (f) E-Field Plot ($\alpha = 130°$)

Figure 3.6: a), b), c) Mesh plot of a flat dielectric composite junction for a contact angle α of 100°, 115°, and 130°respectively with a 5 μm h_{min} around the singularity. c), d), e) The corresponding electric field FEM simulation of each design variant. (Simulated with electrical properties listed in Figure 2.8 pg. 17)

An analytical solution to the electric field crowding around the junction is presented in [88] where the electric field strength is found to be proportional to r^{n-1} where r is the distance from the junction to the observation point and n is an exponent determined by the boundary conditions. Three different design variations are shown in Figure 3.6 for a contact angle α of 100°, 115°, and 130°along with their respective mesh and FEM field solution.

As the contact angle is varied, three observation points are selected at $\epsilon = 10, 15, 20$ μm. These observation points may not necessarily fall on mesh nodes and thus the electric field locations at the observation points will be calculated using interpolation between the closes mesh nodes. Note that ϵ has been selected such that it is significantly larger than the minimum mesh element length h_{min} around the singularity, as discussed in the previous section.



(a) $\epsilon = 10\mu m$ (b) $\epsilon = 15\mu m$ (c) $\epsilon = 20\mu m$

Figure 3.7: Variation between the analytical solution and the FEA solution for the flat dielectric composite junction shown in Figure 3.6 for $\epsilon = 10$, 15, 20 μm respectively.

Figure 3.7 shows the simulated electric field magnitude at each of the three observation points plotted against the corresponding analytical solution presented in [88]. The result shows how the behavior of the triple point is "smooth" with variations in geometric parameters but the added variation of mesh in the FEM simulation causes a significant error. This effect can be reduced by further increasing the buffer term ϵ, but is always present when interpolation is required to evaluate the field at observation points.

The presence of the error due to mesh variation can be detrimental to descent-based numerical optimization techniques. For example, Eq. 3.2 shows a one-dimensional least-squares optimization problem with a cost function based on the electric field strength at two observation points P_1 and P_2 a distance of 15 μm from a singularity. In this case, the system has two flat dielectric junctions with complementary contact angles $\alpha_1 = \alpha$ and $\alpha_2 = 180° - \alpha$.

$$\begin{aligned} \min_{\alpha} \quad & ||E(P_1) + E(P_2)||^2_{L^2} \\ \text{s.t.} \quad & 90° \leq \alpha \leq 150° \end{aligned} \tag{3.2}$$

Using the analytical and FEM solution to the electric field strength for $\epsilon = 15$ μm from Figure 3.7b, the cost function for the entire solution domain of $90° \leq \alpha \leq 150°$ for both the analytical solution and the FEM solution can be calculated as shown in Figure 3.8.

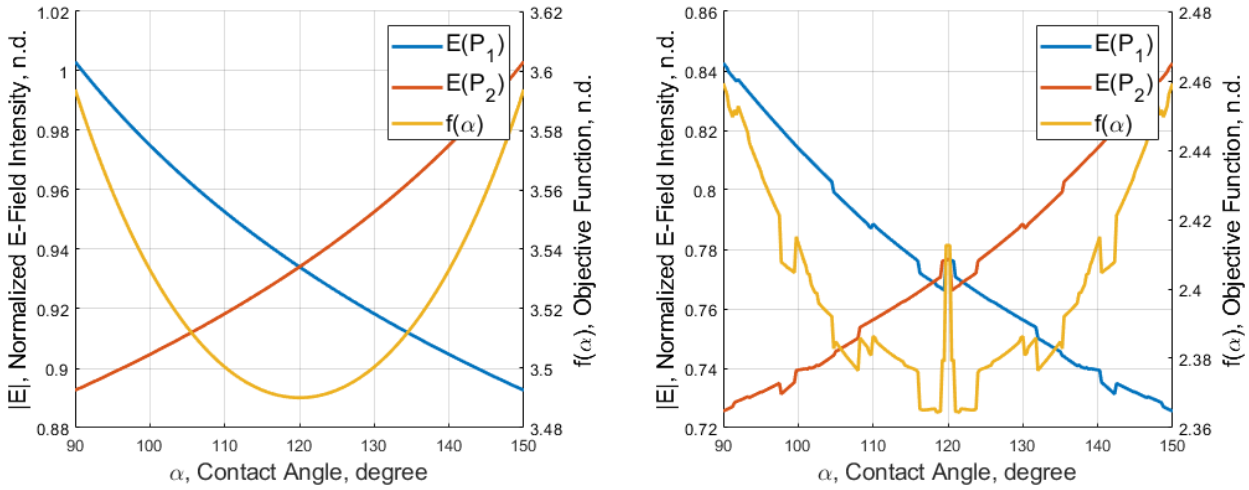


Figure 3.8: a) The electric field magnitude at observation points P_1 and P_2 according to the analytical solution and the corresponding least-squares cost function $f(\alpha)$ in Eq. 3.2. b) The electric field magnitude and corresponding cost function calculated using the FEM data from Figure 3.7.

The resulting cost function from the analytical solution is smooth and perfectly convex, ideal for gradient-based optimization techniques. However, when FEM data is substituted in place of the analytical result, the mesh-dependent error quickly corrupts the cost function with artificial minimums and sharp discontinuities, rendering any classical descent-based optimization techniques useless. Section 3.2 will build on this discussion and show how different cost function formulations and optimization techniques can be used to combat the data corruption caused by mesh variations.

3.1.4 Summary

This section reviewed the key challenges when applying numerical optimization techniques to non-uniform electric field problems. A difficulty occurs early on simply due to the geometric complexity and dense constraint matrices that arise from the intricate structures. Even

when decomposed into 2-D cross-sections, simple structures like the 4 layer field grading geometry shown in Figure 3.1 can contain several tens of variables. Further reduction and simplification are required using symmetry and thoughtful constraints.

The presence of singularities in the computational domain poses challenges from a modeling and stability standpoint. Singularities cannot be effectively modeled using an FEM technique and instead required a sophisticated analytical solution or BEM technique. Analytical solutions are time-consuming to derive and validate, and cannot be mapped to arbitrary geometry. BEM techniques are non-standard in many commercial simulation tools and require extensive knowledge of material properties that are not always readily available from material manufacturers. As a result, a buffer term is used to help stabilize the result over large changes in mesh geometry but does not compensate for the loss of fidelity in the model.

Small changes in mesh geometry for different design variations pose one of the greatest challenges as they corrupt the FEM data, injecting false minimums and sharp discontinuities into the data and, in turn, the cost function. These discontinuities quickly render many classical descent-based optimization algorithms useless and make finite-difference derivatives and Hessian approximations difficult.

3.2 Cost Function

Typically, insulation systems are optimized using field integration (or field quadrature for numerical optimization) cost functions that minimize the energy contained in the electric field [81]. Immunity to the mesh-dependent noise is gained as a result of the integration, which causes the error at each mesh node to be averaged over the entire domain. The result is a relatively smooth cost function suitable for descent-based optimization algorithms.

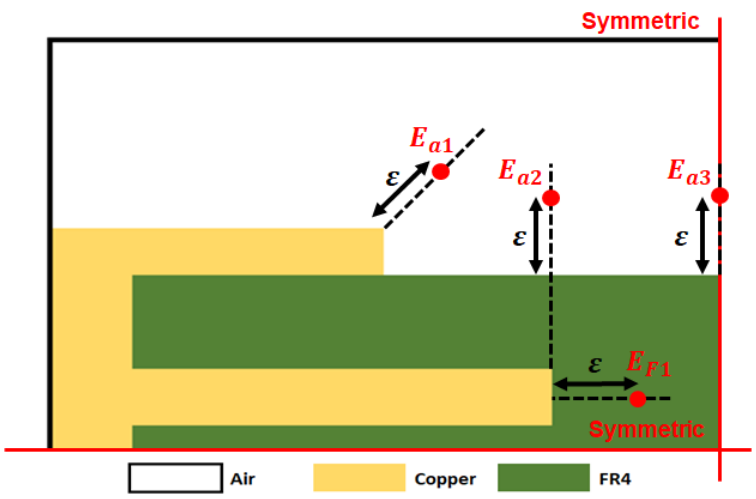


Figure 3.9: Points of interest are placed at a distance of ε away from known field crowding locations. POIs located in the air are labeled E_{a1} - E_{a1} and the POI located in the FR-4 dielectric is labeled E_{F1}.

While this technique is viable for some field grading geometries, the laminate PCB structures discussed in this work are not suitable. In these structures, the design case with the lowest energy is typically the design case with no field grading and the highest intensity crowding, with very low electric field magnitude in the rest of the domain.

In addition to convergence issues, this class of objective functions also suffers from scaling issues as it requires a dense mesh of the entire geometry to calculate accurate field energy. The dense mesh increases the computational cost of both the FEM solver and the field integration of the cost function, making it expensive to scale to larger and more intricate systems with high numbers of field crowding locations.

As a result, a new cost function is proposed called the weighted point of interest (POI) technique. The technique works by building a least-squares cost function on the electric field strength at field crowding locations (or points of interest). The points of interest are located near the electric field crowding, a distance ε from the singularity, as shown in Figure 3.9.

These POIs are the only locations where the electric field solution is required. As a result, a

dense mesh is only needed around the POIs, while the mesh everywhere else in the domain is only dense enough to ensure the stability of the solution. In this way, the weighted POI cost function gives an immediate gain in terms of computational time in that no 2D or 3D field integration is required, and meshes can be significantly lighter.

Given the POIs, the weighted cost function is constructed in terms of a unit-less field intensity factor η

$$\eta = \frac{E_{pk}}{E_{BD}} \tag{3.3}$$

where E_{pk} is the electric field magnitude at a given POI and E_{BD} is the dielectric breakdown strength of the material where the POI is located. When the field grading design is invalid, that is, the electric field strength exceeds the breakdown strength of the material, the intensity factor η will be greater than 1. Conversely, when the system is valid, η will be less than 1. The intensity factor is calculated for each POI and then summed in a least-squares-style cost function.

$$f_p(\vec{x}) = \sum_{i=1}^{N} (FOS_i \cdot \eta_i)^p = \sum_{i=1}^{N} \left(FOS_i \cdot \frac{E_{pk-i}(\vec{x})}{E_{BD-i}} \right)^p \tag{3.4}$$

The cost function uses a penalty term $p > 1$ which is used to penalize POIs that are greater than 1, i.e. POIs where the electric field strength is greater than the breakdown strength of the containing medium. Once a POI becomes compliant, the penalty term reduces its impact on the cost function, ensuring that the focus is kept on those POIs that are not compliant. The penalty term can be tuned by the designer but will be taken to be 2 for the balance of this work.

In the system shown in Figure 3.9, the two mediums are air, with an average breakdown

strength of 3 MV/m, and FR-4 dielectric, with an average breakdown strength of 20 MV/m. Since there is usually some ambiguity around the breakdown strength of a material, the cost function also incorporates a factor of safety (FOS) term that can be applied to different materials. For example, while FR-4 is rated for a breakdown strength of 20 MV/m, its performance can degrade significantly with thermal cycling. A factor of safety of at least 2 is recommended [60]. For the balance of this work, an FOS of 2 will be applied to all field intensity factors.

The cost function for the structure in Figure 3.9 can then be written as shown below with each of the peak electric fields written as a function of the design variables $\vec{x}$.

$$f(\vec{x}) = \left(2 \cdot \frac{E_{pk-a1}(\vec{x})}{3 \text{ MV/m}}\right)^2 + \left(2 \cdot \frac{E_{pk-a2}(\vec{x})}{3 \text{ MV/m}}\right)^2 + \left(2 \cdot \frac{E_{pk-a3}(\vec{x})}{3 \text{ MV/m}}\right)^2 + \left(2 \cdot \frac{E_{pk-F1}(\vec{x})}{20 \text{ MV/m}}\right)^2 \quad (3.5)$$

3.3 Bayesian Optimization

Bayesian optimization is the final piece of the optimization workflow that allows for efficient optimization of highly nonuniform electric fields using simple, scalable POI objective functions. Bayesian optimization algorithms are a class of optimization algorithms that do not require any derivative information about the cost function, be it numerical or analytical. At a high level, the algorithm works by building a Gaussian process model of the cost function and optimizing the model as opposed to optimizing the cost function itself.

Bayesian techniques are optimal for problems with:

1. No available analytical derivative information
2. Computationally expensive or time-intensive cost function evaluation
3. Objective functions which can only be observed with some amount of Gaussian noise or corruption, e.g. $f_{obs}(\vec{x}) = f(\vec{x}) + e_0$

From these criteria, non-uniform electric field optimization problems as described in Sections 3.1 and 3.2 are prime candidates for Bayesian optimization. The following sections will describe in detail the two dominant components of the algorithm: 1) Gaussian process regression, which fits a Gaussian process model to the objective function; and 2) acquisition functions, which efficiently (meaning more efficient than cost function evaluations) optimize the process model. The discussion will conclude in Section 3.3.3 with the implementation of the Bayesian algorithm in MATLAB.

3.3.1 Gaussian Process Regression

A Gaussian process is a predictive modeling tool derived from a multivariate Gaussian distribution with infinite dimensionality. A Gaussian process is defined by a mean function $m(x)$ and a covariance function $K(x, x')$ where $x \in \boldsymbol{X}$.

$$f(x) \sim GP(m(x), K(x, x')) \tag{3.6}$$

The model can be trained using a set of training data $\vec{x} = \{x_1, x_2, ...x_N\} \in \boldsymbol{X}$ by using the training data to calculate the covariance function $\boldsymbol{K}(x, x')$ as shown in Eq. 3.7

$$K_{ij} = \sigma^2 e^{-\frac{1}{2L^2}(x_i - x_j)^2} \tag{3.7}$$

where L is a hyper-parameter (one which must be observed from data) which describes at what vector length N the data is no longer correlated, and σ^2 represents the variance in the training values $\vec{x}$, that is, the distribution of unwanted error in the observation points. Given a training set, the Gaussian model can be used to predict output $f(x^*)$ for a given data point x^* with given confidence range σ_y. These techniques are used extensively in machine learning and non-linear regression problems where a set of observation data with some amount of Gaussian noise serves as the training set and the predictive nature of the model acts as a nonlinear curve fit for the data, which can, in turn, be used to interpolate data at intermediate observation points.

In general, Gaussian processes can be used as a predictive model in any problem of the form

$$\begin{aligned} y(x) &= f(x) + e\sigma_y \\ p(e) &= \mathcal{N}(0, 1) \end{aligned} \tag{3.8}$$

where the function of interest $f(x)$ can only be observed with some amount of Gaussian distributed error e with variance σ_y^2.

To use Gaussian processes to make predictions, they must be represented in a finite form as they are inherently infinite objects. This is done using the marginalization property of Gaussian objects which allows the properties of the process to be projected on a finite basis - a basis which would include the training set as well as the query set or the points to be predicted.

$$
\begin{aligned}
p(\boldsymbol{y_1}) &= \int p(\boldsymbol{y}_1, \boldsymbol{y}_2) d\boldsymbol{y}_2 \\
p(\boldsymbol{y}_1, \boldsymbol{y}_2) &= \mathcal{N}(\begin{bmatrix} \boldsymbol{a} \\ \boldsymbol{b} \end{bmatrix}, \begin{bmatrix} \boldsymbol{A} & \boldsymbol{B} \\ \boldsymbol{B}^T & \boldsymbol{C} \end{bmatrix}) \rightarrow p(\boldsymbol{y}_1) = \mathcal{N}(\boldsymbol{a}, \boldsymbol{A})
\end{aligned}
\tag{3.9}
$$

In this way, the desirable properties of the model are projected onto the discrete mean vector $\boldsymbol{a}$ and the discrete covariance matrix $\boldsymbol{A}$.

Given the discrete representation of the Gaussian process, predictions can be made using Bayes Theorem (Eq. 3.10) which yields the probability distribution $p(\boldsymbol{y}_1)$ of a predicted data point $\boldsymbol{y}_1$ given the probability distribution $p(\boldsymbol{y}_2)$ of the training data $\boldsymbol{y}_2$.

$$
p(\boldsymbol{y}_1|\boldsymbol{y}_2) = \frac{p(\boldsymbol{y}_1, \boldsymbol{y}_2)}{p(\boldsymbol{y}_2)} = \mathcal{N}(\boldsymbol{a} + \boldsymbol{B}\boldsymbol{C}^{-1}(\boldsymbol{y}_2 - \boldsymbol{b}), \boldsymbol{A} - \boldsymbol{B}\boldsymbol{C}^{-1}\boldsymbol{B}^T) \tag{3.10}
$$

This yields a means predicting the value of a function $f(x^*)$ evaluated a query point x^* from a given sample set $f(\vec{x})$ for $\vec{x} \in \boldsymbol{X}$, where the only significant limiting factor computationally is the inversion of the matrix $\boldsymbol{C}$, which is the covariance matrix of the sample data $f(\vec{x})$. The only remaining step is to formulate the problem as a regression problem so the Gaussian process model can be fit to the sample data.

To formulate the process regression, the probabilistic model is formed as shown in Eq. 3.11 where e is the Gaussian distributed error and the coefficients β are estimated from the training data $y_i = f(\vec{x}_i)$ for $y \in \mathcal{R}$, $\vec{x}_i \in \mathcal{R}^N$, and $i = \{1, ...M\}$.

$$
y = \vec{x}^T \beta + e \tag{3.11}
$$

From this point, the following model is proposed where $h(\vec{x})$ represents a transformation of

the data $\vec{x}$ from $\mathcal{R}^N \rightarrow \mathcal{R}^P$ where $P << N$ and β is now of size $P \times 1$.

$$y_i = h(\vec{x}_i)^T \beta + f(\vec{x}_i) \tag{3.12}$$

Assuming $\vec{y} = f(\boldsymbol{x}) \sim GP(m(\boldsymbol{x}), K(\boldsymbol{x}, \boldsymbol{x}'))$, where $\boldsymbol{x}'$ is the query data, then applying Bayes rule (Eq. 3.10) yields the following expression for a predicted functional value $y^* = f(\vec{x}^*)$

$$P(y^*|f(\boldsymbol{x}), \vec{x}^*) \sim N(\vec{y}|\boldsymbol{H}\beta + f, \sigma^2 \boldsymbol{I}) \tag{3.13}$$

where $\boldsymbol{H} = \{h(\vec{x}_1^T), h(\vec{x}_2^T), ...h(\vec{x}_M^T)\}$ and $f = \{f(\vec{x}_1), f(\vec{x}_2), ...f(\vec{x}_M)\}$, $\boldsymbol{I}$ is the identity matrix and σ^2 is the variance of the Gaussian distributed error term e from Eq. 3.11.

An example of a GPR applied to an arbitrary data set is shown in Figure 3.10. In this example the system dynamics to be modeled are shown as the function $f(x)$ in black. The

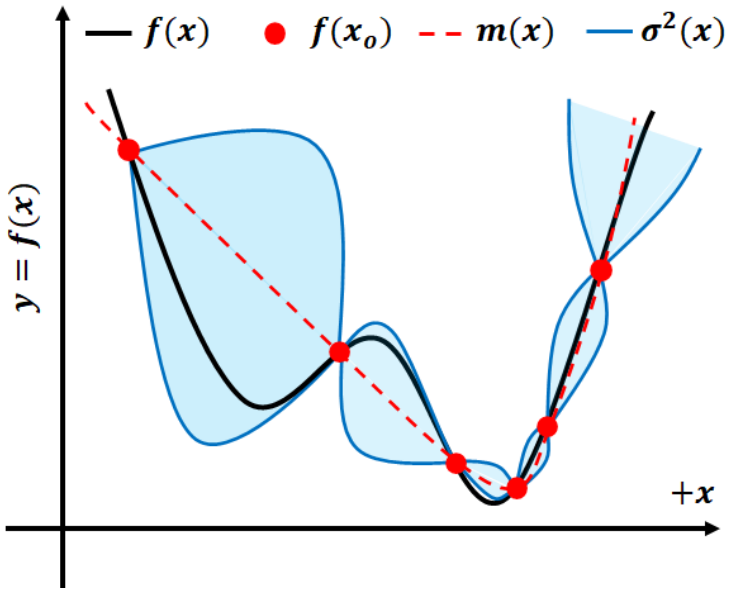


Figure 3.10: An example of Gaussian process regression used to model a function $f(x)$ given the random sampling $f(x_0)$.

red points $f(x_0)$ represent a sampling of the function at 6 random points x_0. Given the sample set, Eqs. 3.9 and 3.10 are applied to fit the mean function $m(x)$ and the variance function $\sigma^2(x)$ as indicated by the red and blue curves respectively.

In conclusion, this section has discussed the first of the two key underlying principles in Bayesian optimization. Gaussian process regression was presented along with how it can predict a real-valued function given a set of training data. In Bayesian optimization, a Gaussian process regression is used to approximate the cost function based on a random set of cost function evaluations, called seed points. Once the model is trained, the minimum of the model is calculated using an acquisition function which will be discussed in the following section. The resulting approximate minimum can then be compared by evaluating the true cost function. In this way, optimization problems where the cost function is corrupted with some amount of Gaussian distributed noise, can be optimized efficiently, without the need for derivatives.

3.3.2 Acquisition Functions

Acquisition functions serve as an efficient means to optimize the Gaussian process model discussed in Section 3.3.1 without analytical or numerical derivatives. Acquisition functions take into account not only where a minimum is likely to exist but also where the solution space has not been significantly investigated. This helps prevent the optimization algorithm from tunneling into the first optimum it finds without thoroughly investigating the domain.

There are many possible acquisition functions for Bayesian optimization algorithms, many of which are already implemented in off-the-shelf toolboxes and libraries for commercial software applications like MATLAB and Python. In general, there are three main types of acquisition functions, of which many variants exist. Each type seeks to balance exploring

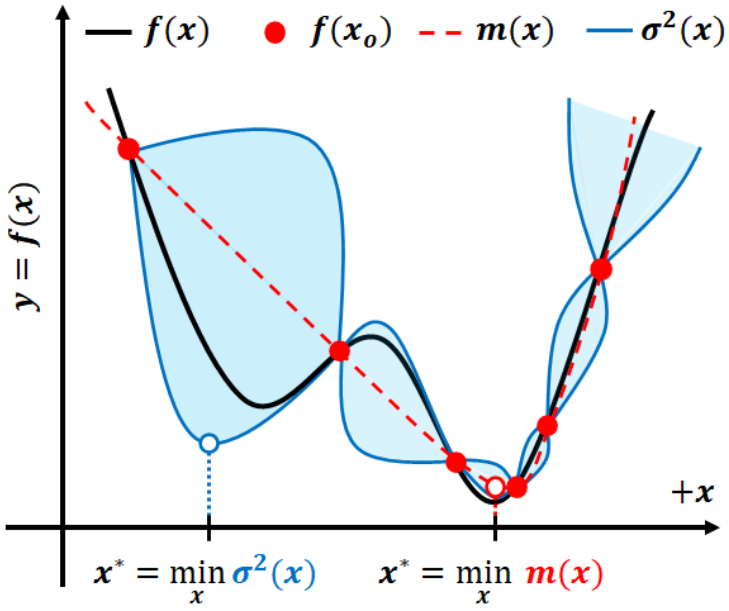


Figure 3.11: An example of the effects of minimizing the variance function $\sigma^2(x)$ as opposed to minimizing the mean function $m(x)$.

new regions of the solution domain (i.e. prioritizing regions with higher variance σ^2) or exploiting regions of known minimums (i.e. prioritizing regions with lower mean $m(\vec{x})$.

The effect of exploration vs. exploitation can be seen from Figure 3.11. By minimizing the mean function, algorithm will exploit regions that are heavily sampled, and well-understood (i.e. low variance). My minimizing the variance function, the algorithm prioritizes areas that are lightly sampled, exploring unknown regions where a minimum may exist. In general, acquisition functions are formulated as some form of a weighted sum of the variance and mean functions, as will be shown in the following sections.

Probability of Improvement (PI)

Probability of improvement is simple in that it is only concerned with locating the point with the highest probability of improving upon the currently observed best value f_{max}. The problem can then be formed as

$$\vec{x}_{i+1} = \max_{\vec{x}} PI(\vec{x}) = \max_{\vec{x}} \mathcal{P}[f(\vec{x}) > f_{max}] \tag{3.14}$$

The equation is typically written in terms of a cumulative normal density function $\Phi(\cdot)$ where $m(\vec{x})$ and $\sigma(\vec{x})$ are the mean and variance of the function f. [89]

$$\vec{x}_{i+1} = \max_{\vec{x}} \Phi\left(\frac{m(\vec{x}) - f_{max}}{\sigma(\vec{x})}\right) \tag{3.15}$$

This acquisition function is the simplest of the three discussed, but can suffer from exploration issues due to the variance term in the denominator. If the variance term becomes small, the cumulative density function can become very large, and the mean term will dominate, causing the algorithm to tunnel into early minimums. PI techniques are effective in problems where a.) the concern of many local minimums is low, or b.) the problem is convex, with only a single global minimum but some degree of Gaussian corruption.

Expected Improvement (EI)

The class of expected improvement acquisition functions builds on PI functions by first calculating an improvement matrix $\boldsymbol{I}(\vec{x})$ (Eq. 3.16) the expectation of which can be maximized to locate $\vec{x}_{i+1}$ as shown in Eq. 3.18. [90]

$$\boldsymbol{I}(\vec{x}) = \begin{cases} f(\vec{x}) - f_{max} & f(\vec{x}) > f_{max}, \sigma(\vec{x}) > 0 \\ 0 & \text{otherwise} \end{cases} \tag{3.16}$$

$$\mathbb{E}(\boldsymbol{I}(\vec{x})) = \frac{\sigma(\vec{x})}{\sqrt{2\pi}} \exp\left(-\frac{(m(\vec{x}) - f_{max})^2}{2\sigma^2(\vec{x})}\right) + (m(\vec{x}) - f_{max})\Phi\left(\frac{m(\vec{x}) - f_{max}}{\sigma(\vec{x})}\right) \tag{3.17}$$

$$\vec{x}_{i+1} = \max_{\vec{x}} \mathbb{E}(\boldsymbol{I}(\vec{x})) \tag{3.18}$$

The right most term of the improvement expectation in Eq. 3.17 is identical to the probability of improvement function except for the mean function $m(\vec{x})$ which is used to weight the term. Conversely, the leftmost term is weighted according to the variance function $\sigma^2(\vec{x})$. Is the way, the acquisition function is designed to balance exploration and exploitation.

Upper/Lower Confidence Bound (UCB/LCB)

Upper and lower confidence bound functions take on the form of a weighted sum of the mean function $m(\vec{x})$ and the variance function $\sigma^2(\vec{x})$.

$$\begin{aligned} UCB(\vec{x}) &= m(\vec{x}) + \alpha\sigma(\vec{x}) \\ LCB(\vec{x}) &= m(\vec{x}) - \alpha\sigma(\vec{x}) \end{aligned} \tag{3.19}$$

This class of functions is a simpler approach to balancing exploration and exploitation by means of a user-defined coefficient $\alpha > 0$ which determines how much one is prioritized over the other. [91]

3.3.3 Bayesian Algorithm Implementation

Given a technique for fitting Gaussian process models (Section 3.3.1) and a means of optimizing these models by way of an acquisition function (Section 3.3.2), the Bayesian optimization algorithm can be assembled as shown in Algorithm 1. In this work, the algorithm has been implemented in MATLAB due to the availability of built-in functions and routines.

The FEM solver used for the cost function has also been implemented in MATLAB for ease of integration between the optimization solver and the FEM solver. In practice, any

FEM solver may be used. The required code for both the optimization and the FEM solver can be implemented using the "Partial Differential Equation" and "Optimization" toolboxes available from MATLAB as shown in Figure 3.12.

Algorithm 1: Bayesian Optimization Algorithm

Generate random seed points $\boldsymbol{X}_0$ and objective function evaluations $\boldsymbol{f}_0 = f(\boldsymbol{X}_0)$
while $\Delta f = f_{i-1} - f_i > \Delta f_{tol}$ **do**
  Build Gaussian process model from training sets $\boldsymbol{X}_i$ and $\boldsymbol{f}_i$ (Eq. 3.13)
  Maximize the acquisition function $\vec{x}_{i+1} = \max a(\vec{x})$ (Eq. 3.15, 3.18, or 3.19)
  Evaluate the objective function $f_{i+1} = f(\vec{x}_{i+1})$ (Algorithm 2)
  Update observations $\boldsymbol{X}_{i+1} \rightarrow \boldsymbol{X}_i \cup \vec{x}_{i+1}$, $\boldsymbol{f}_{i+1} \rightarrow \boldsymbol{f}_i \cup f_{i+1}$
  Index $i \rightarrow i + 1$
end

Algorithm 2: Objective Function Evaluation $f(\vec{x})$

Given h_{min}, ε, and $\vec{x}$
Draw geometry given design variables $\vec{x}$
Apply h_{min} along all singularities
Locate sense points a distance of ε away from POIs
Mesh and solve FEM problem
Record $\vec{E}_p k = \{E_{pk1}, E_{pk2}, ...E_{pkN}\}$ at sense points
Compute weighted POI objective function $f = f_p(\vec{E}_{pk})$ (Eq. 3.4)
return f

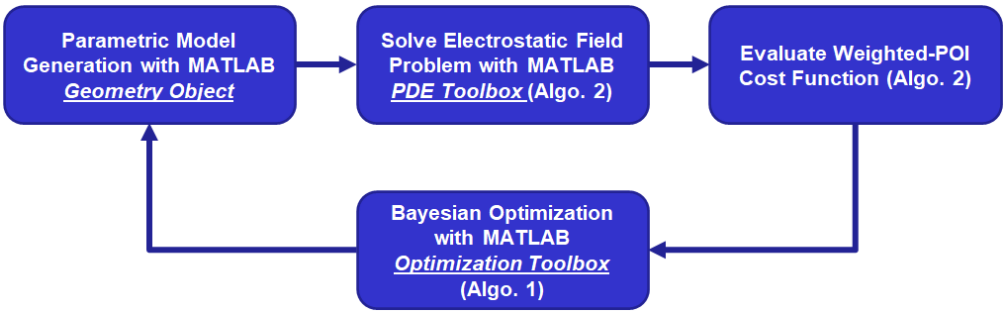


Figure 3.12: Flowchart showcasing the key aspects of the Bayesian optimization workflow as implemented in MATLAB®.

3.3.4 Limitations

Typically, in the discussion of Bayesian optimization techniques, the limiting factor is the scalability of the Gaussian process regression. Improving scalability of Gaussian process regression is currently an area of active research; however, it is important to note that this does not contradict the claims of scalability made earlier. In a GPR, fitting the covariance matrix requires the inversion of a matrix of size $N \times N$ where N is the number of samples. The matrix is not only large, but very dense, making the inversion computationally expensive. In non-linear curve fitting and machine learning applications with millions of sample points, the inversion of this matrix can quickly become prohibitively expensive; especially when considering that the inversion takes place at each iteration.

The proposed class of field grading optimization problems generally requires less than 50 iterations, and thus less than 50 sample points, as will be demonstrated in Chapter 4. Thus, the inversion is of size 50×50 or less and is computationally trivial when compared to the expense of the FEA solution. It is important to note that as the system complexity increases, and more samples are required to resolve the domain, the expense of the inversion will increase.

A more pressing limitation of the proposed work is the distribution of the noise from the FEA solution. Bayesian optimization requires that the noise distribution of the cost function is Gaussian. Failing to fulfill this requirement can lead to convergence issues due to poor reconstruction of the domain. Several simple, qualitative studies have been carried out on the following design cases to ensure the noise distribution was not bimodal or significantly skewed and it was found that the FEA noise distribution is largely uniform.

While the analytical proof of this behavior is outside the scope of this work, key conclusions can be made from the result. Since the noise distribution is not necessarily Gaussian, it is

important that the noise is small with respect to the system dynamics. In general, this class of problems has shown smooth underlying system dynamics which are easily distinguished from the FEA noise. If however, the domain contained some discontinuity that was on the order of the FEA noise, the algorithm could potentially fail to distinguish between the discontinuity and the noise. Such a discontinuity could be introduced if using a categorical variable for the optimization (which Bayesian optimization allows).

If including some sort of categorical variable, it would be important to first ensure that the discontinuity in the domain is significantly larger than the noise floor. If the noise floor is too high, Bayesian techniques may be ill-suited to the problem and a more complicated heuristic technique might be required.

The final point is the lack of consideration of non-ideal conditions, such as variations in material properties, manufacturing tolerances, surface contaminants, environmental pollution, etc. While in theory, a more sophisticated FEA simulation could be used which takes these effects into consideration, such is not the case in this work. The purpose of this work is to optimize relative performance of various field grading structures and understand their behavioral characteristics and limitations at a high level using an innovative optimization approach. The discussion of the non-ideal effects is outside the scope of this work.

3.4 Summary

Chapter 3 has outlined the underlying theory and techniques that allow for the optimization of highly non-uniform electric fields. Section 3.1 highlighted the key challenges associated with optimizing these structures, most notably the geometric complexity, the presence of singularities in the computational domain, and the data corruption that stems from the dependency of the solution on the mesh. A design example consisting of two triple points

was given in Section 3.1.3 which showed how the analytical behavior of such structures is generally smooth but the mesh-dependent noise makes the system nearly impossibly to optimize with traditional techniques.

Sections 3.2 and 3.3 followed with discussions of cost functions and the Bayesian optimization procedure which seek to address these challenges. The weighted POI cost function proposed in this work offers an improvement over existing field integration techniques due to the fact that it only requires a dense mesh around the field crowding regions, while the rest of the domain can be coarsely meshed. This directly translates to faster meshing and computation times, as well as improved scalability over field integration techniques.

A Bayesian optimization algorithm is used in conjunction with the weighted POI cost function to optimize the field grading structures without the use of derivatives. A Gaussian process model is fitted to the objective function and acquisition functions are used to optimize the model as opposed to directly optimizing the cost function. In this way, the mesh-dependent noise cannot corrupt the minimum and the algorithm can repeatably converge to true global minimums. The resulting workflow is scalable and computationally efficient with the only significant limitations being the need to ensure that FEA noise threshold is significantly small with respect to the system dynamics and that the optimization domain can be effectively modeled with relatively few ($< 10^4$) samples.

Chapter 4

Simulation Results

The advantage of a numerical optimization technique in design is twofold. First, automated optimization algorithms simplify and accelerate design processes by reducing the required number of iterative design evaluations. Second, they can provide insights into high-dimensional systems that are otherwise void of governing equations. Typical manual design techniques used in the design of field grading systems or high-density insulation systems rely to some degree on a trial and error approach. The designer will select a design based on previous design work or intuition, simulate the design, evaluate the performance, propose a design revision, and repeat until the desired performance is achieved. Numerical optimization not only accelerates the process, but also allows for the design to be optimized over a wide range of operating points or design specifications. In this way, insight can be gained into the fundamental trade-offs and limitations of a design.

This chapter will illustrate the ability of numerical optimization to provide such insights. Section 4.1 will begin with a discussion of the optimization workflow, followed by Section 4.2 which will show the improved convergence performance of the Bayesian optimization algorithm with weighted POI cost function when compared to a state-of-the-art descent-based interior-point algorithm. Sections 4.3 and 4.4 will discuss the characterization of 4-layer and 6-layer the PCB-embedded field grading structures using numerical optimization. The behavior of the system, as well as its limitations in practical application, will be derived from the numerical optimization process.

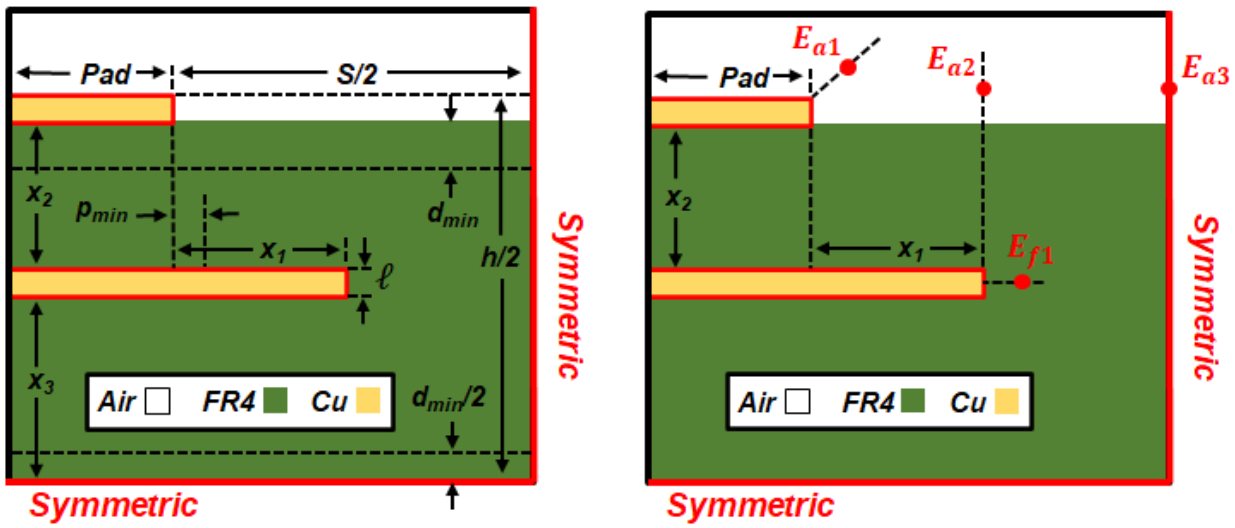
4.1 Optimization Workflow

To demonstrate the Bayesian optimization algorithm, the symmetric 4-layer field grading system from Figure 3.2. The system is parameterized as shown in Figure 4.1a and the POIs are placed according to Figure 4.1b.

To ensure convergence to a reasonable minimum, the optimization variables x_1 and x_2 must be constrained. The grading plate length x_1 can be constrained by a minimum plate length p_{min} since the plate must extend beyond the pad to affect the field formation in the air.

$$x_1 \geq p_{min} \tag{4.1}$$

Since the system is symmetric, the place cannot extend past the vertical line of symmetry, located a distance $S/2$ from the pad edge



(a) (b)

Figure 4.1: a) Parameterized symmetric 4-layer field grading structure from Figure 2.9 (pg. 19) with constraints and fixed design variables b) POI as defined in Figure 3.9 (pg. 34) used for cost function formulation placed a distance ε from the singularity location.

$$x_1 < \frac{S}{2} \tag{4.2}$$

and thus the first optimization variable is constrained. Similarly, the dielectric heights x_2 and x_3 can be constrained by fixing the height of the PCB h as a design parameter

$$h = 4\ell + 2x_1 + x_3; \tag{4.3}$$

where ℓ is the copper trace thickness (1.4 mils for 1-oz. copper foil). Assuming a minimum practical dielectric thickness of d_min, the third optimization variable x_3 can be removed from the optimization as shown in Eq. 4.4.

$$d_{min} \leq x_2 \leq \frac{h}{2} - 2\ell - \frac{x_3}{2} \leq \frac{h}{2} - 2\ell - \frac{d_{min}}{2}; \tag{4.4}$$

Given the constraints in Eq. 4.1-4.4 and the POIs as defined in Figure 4.1b, the optimization problem can be formulated as in Eq. 4.5.

$$\begin{aligned} &\min_{\vec{x}} \sum_{i=1}^{4} (FOS_i \times \eta_i)^p \\ &p_{min} \leq x_1 \leq S/2 \\ &d_{min} \leq x_2 \leq h/2 - 2\ell - d_{min}/2 \end{aligned} \tag{4.5}$$

Table 4.1 shows the optimization and simulation parameters. Figure 4.2 shows the mesh, POI locations, FEM simulated electrostatic performance, and the cost function value of the optimized design. Figure 4.3 shows the Gaussian process regression at various stages in the optimization process. Figure 4.3a shows the initial process regression built from four

Table 4.1: Optimization and Simulation Parameters

Parameter	Value	Parameter	Value
PCB Thickness h	80 mils	Relative Permittivity of Air	1.0
Terminal Spacing S	200 mils	Dielectric Strength of Air	3 MV/m
Voltage V_{dc}	10 kV	Relative Permittivity of FR-4	4.4
Trace Thickness ℓ	1.4 mils (1 oz.)	Dielectric Strength of FR-4	20 MV/m
Penalty Term p	2	Factor of Safety in Air	2
Buffer Term ε	15 μm	Factor of Safety in FR-4	2
Minimum Mesh Size h_{min}	5 μm	Acquisition Function	EI

randomly selected seed points. Once the initial regression is built, the acquisition function is used to select the next evaluation point. Figures 4.3b and 4.3c show the regression after 5 and 10 iterations respectively, followed by Figure 4.3d which shows the regression after the algorithm completes 20 iterations, at which time the predictions of the process model match the cost function and the algorithm terminates.

The next section will discuss the convergence rate of the proposed technique, how well it converges to the known minimum, and how it compares quantitatively to manual optimization and a state-of-the-art descent-based technique.

4.2 Convergence Performance

The convergence performance of the proposed Bayesian optimization algorithm with weighted POI cost function was benchmarked against an interior-point algorithm with weighted POI. The benchmarks were evaluated on a symmetric 4-layer field grading structure as described in Figure 4.1 with two optimization variables x_1 and x_2. The design is limited to two optimization variables so that the cost function can be easily visualized in a 3D plot.

A critical difference between Bayesian optimization and descent-based techniques, such as the interior-point algorithm, is that Bayesian techniques do not start from an initial point.

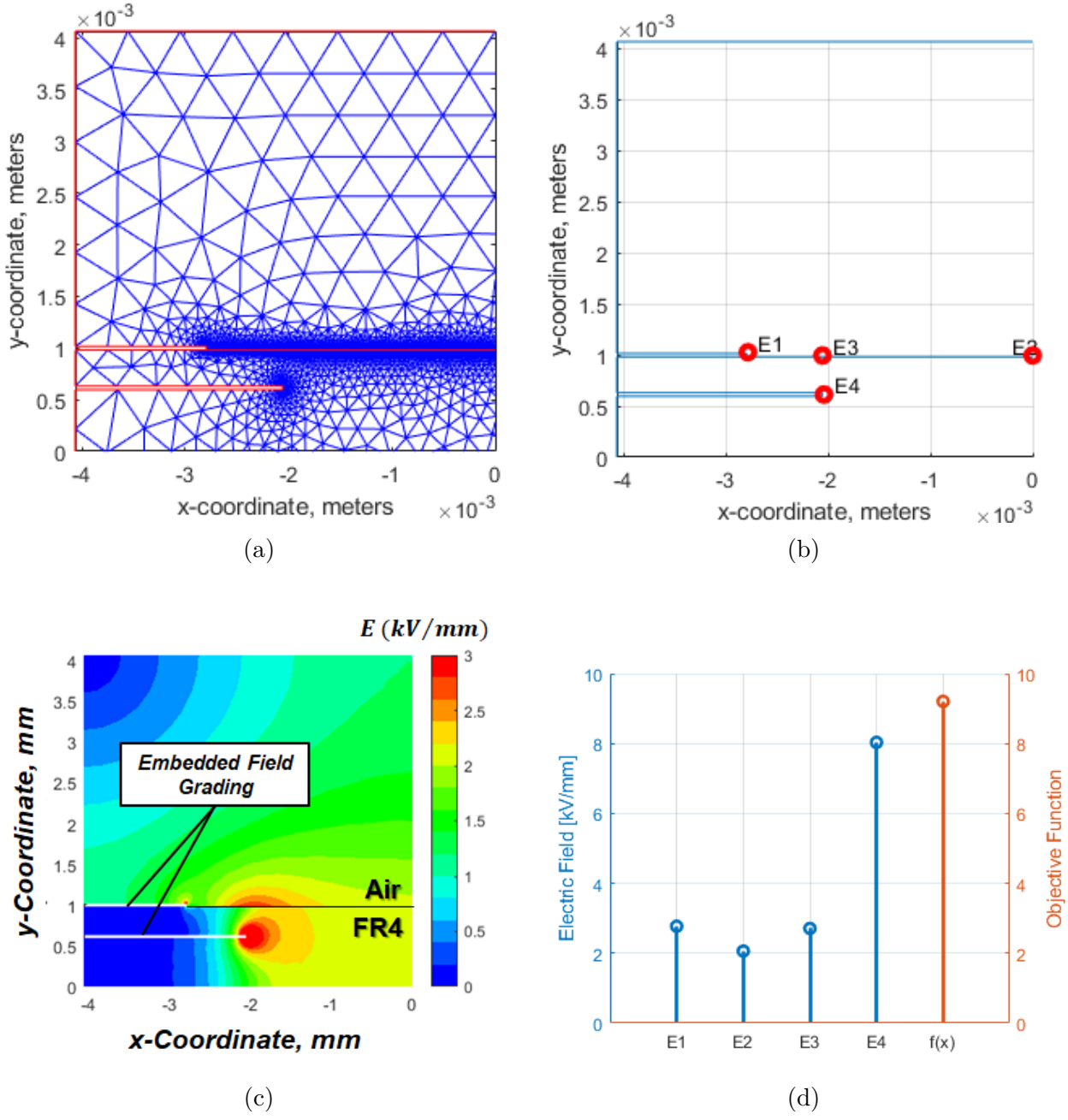
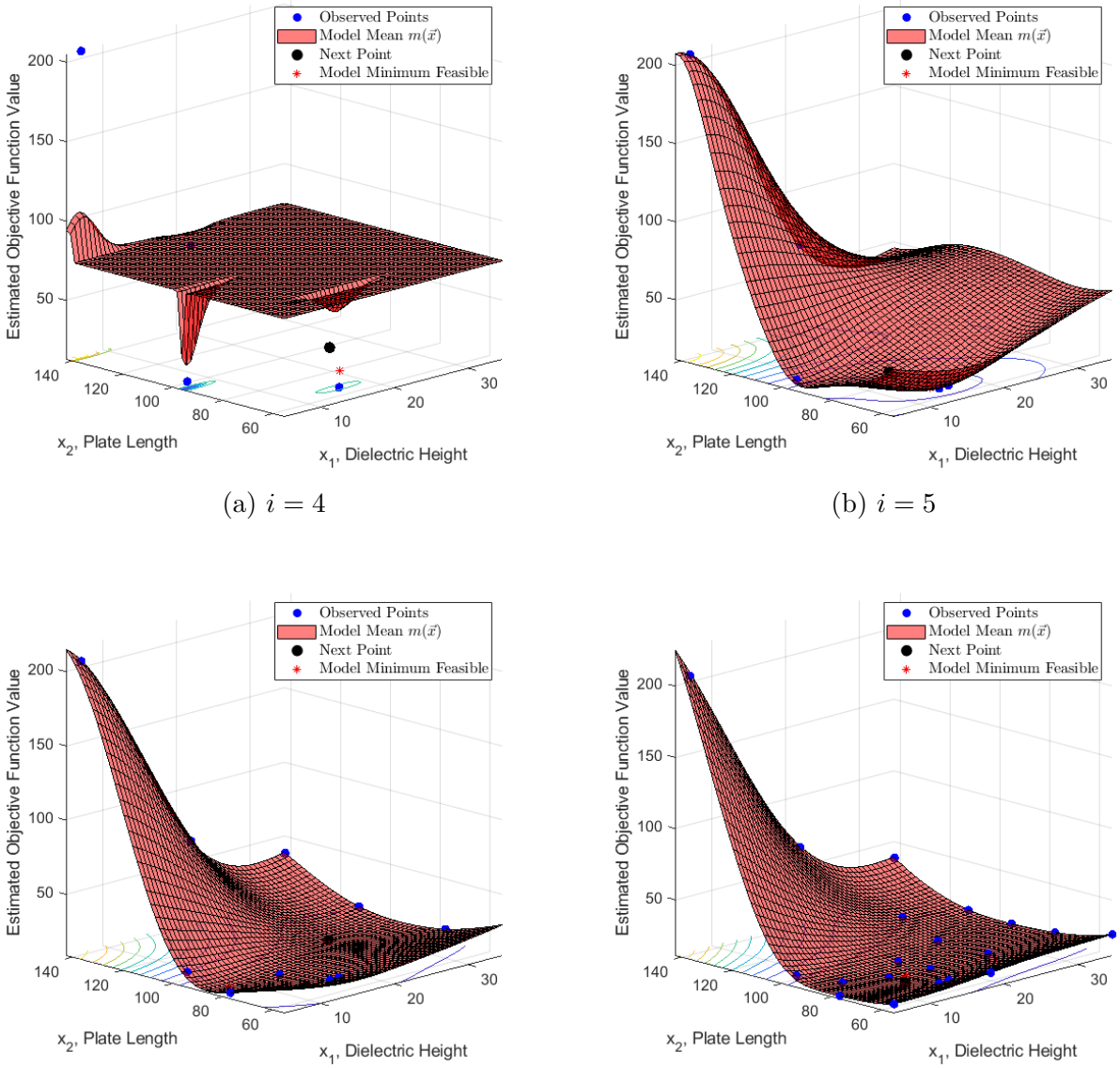


Figure 4.2: a) Mesh plot of optimized geometry showing a 5 μm h_{min} around the singularity; b) four POIs placed in the known field crowding locations a distance of ε from the singularity; c) simulated electric field shows field crowding around the edges of the traces; d) the electric field intensity at each POI and the minimum cost function value. (See Table 4.1 on pg. 52 for material and simulation parameters.)



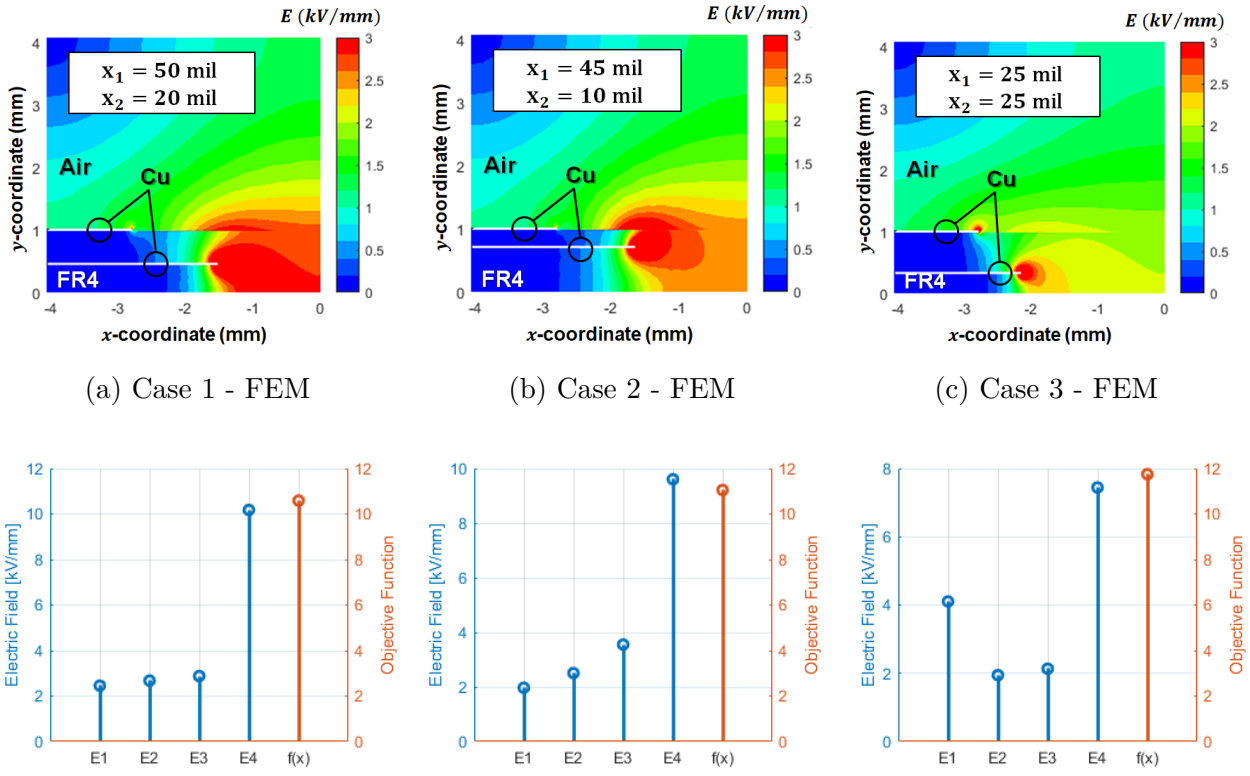
(a) $i = 4$ (b) $i = 5$

(c) $i = 10$ (d) $i = 20$

Figure 4.3: The Gaussian process model for a symmetric 4-layer field grading structure being refined throughout the optimization process. a) The GP model after collecting 4 randomly selected seed points; b) acquisition function is employed to locate the 5 evaluation points; c.) GP is significantly refined by iteration 10; d) GP now accurately predicts the cost function minimum and algorithm terminates.

Instead, the algorithm starts with a random sampling of the domain and begins from the anticipated minimum of the process model constructed from the sampled points (Algorithm 1). The interior-point algorithm, in contrast, requires the designer to assign an initial design point at which the gradient will be evaluated to determine the first step. Since convergence depends on the initial design point, each algorithm will be run three times. The interior-point algorithm will start from three reasonable design structures shown in Figure 4.4, while the Bayesian algorithm will gather seed points from a random sampling.

The convergence performance of the interior-point algorithm with weighted POI as compared



(a) Case 1 - FEM (b) Case 2 - FEM (c) Case 3 - FEM

(d) Case 1 - Objective (e) Case 2 - Objective (f) Case 3 - Objective

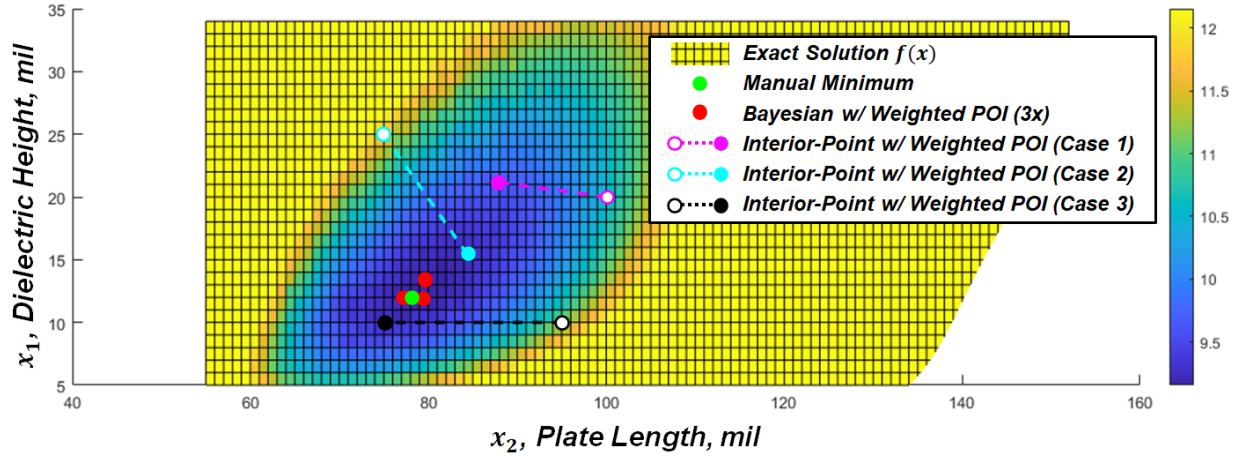
Figure 4.4: a), b), c) FEM simulated electric field strength for the case 1, 2, and 3, initial designs for the symmetric field grading structure defined in Figure 4.1 (pg. 50); d), e), f) the peak electric field strength at the POIs and the objective function evaluation for each initial design case. (See Table 4.1 on pg. 52 for material and simulation parameters.)

to the Bayesian technique is shown in Figure 4.5. Here the value of the cost function is calculated for all combinations of design variables to show the shape of the domain and location of the true minimum. As discussed in Section 3.1.3, the domain is shown to be largely convex with only small non-convexities due to the mesh-dependent error.

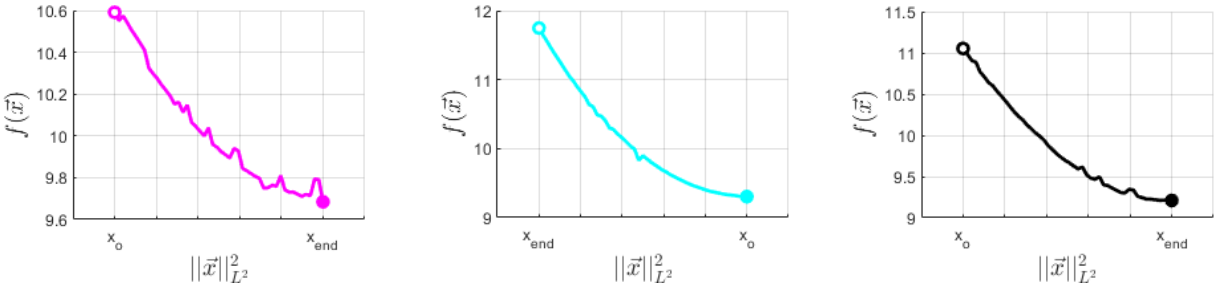
Figures 4.5b - 4.5d show the descent path between the initial and final design points of each of the interior-point routines and the slight non-convexities that cause the algorithm to hang before it reaches the global minimum. The Bayesian technique is immune to these noise issues and reliably converges to the known minimum. Table 4.2 shows the relative error of each case as it relates to the known minimum. The average error of the Bayesian technique is 1.1 mils, approximately 7 times lower than the interior point algorithm.

In addition to verification of convergence, Figure 4.5 serves as a demonstration of the effectiveness to which the Gaussian Process Model (GPM) defined in Chapter 3 is able to model the solution domain. The purpose of the GPM is not to model the domain in Figure 4.5 exactly, but rather, to model the domain to the extent that the location of the minimum can be successfully predicted. The proximity of the predicted minmum (red dots in Figure 4.5) to the known minimum (green dot) and the repeatability of the proximity, are strong indicators that the GPM can accurately model the domain to the required extent. The average convergence error of 1.11 mils, as reported in Table 4.2, is on the order of the manufacturing tolerance of a typical PCB and thus, further improvements in convergence error, i.e. further improvements in GPM accuracy, are not required for this application.

In addition, the Bayesian technique terminates in 30 iterations. In this implementation, there is no termination condition in the Bayesian optimization as there is in the interior point algorithm. In this work, no significant improvement was ever observed beyond 30 iterations. Since the objective function evaluation is responsible for most of the computational time, the number of objective function evaluations can be taken to be proportional to the



(a)



(b) Case 1 (c) Case 2 (d) Case 3

Figure 4.5: a), The converged minimums of three independent Bayesian routines and three interior-point routines both with weighted POI plotted against the known minimum; b), c), d.) the descent path of each of the three interior-point design cases showing the minor non-convexities stemming from the mesh error as described in Figure 3.7 on pg. 31.

Table 4.2: Relative Error of Interior-Point vs. Bayesian Algorithm

	Interior-Point (Weighted POI)	**Bayesian (Weighted POI)**
Case 1	13.49 mils	0.29 mils
Case 2	3.33 mils	2.18 mils
Case 3	7.24 mils	0.86 mils
Average	**8.02 mils**	**1.11 mils**

Table 4.3: Objective Function Evaluations

		Cost Function Evaluations	**Average Speed Increase of Bayesian**
Interior-Point (Weighted POI)	**Case 1**	149	3x
	Case 2	78	
	Case 3	79	
Bayesian (Weighted POI)		30	1x
Manual Optimization (Weighted POI)		2940	100x

computation time. Table 4.3 shows the number of objective function evaluations for the Bayesian technique, interior-point, and the manual optimization process. The low iteration count of the Bayesian technique makes it 3x faster than the interior point and 100x faster than the manual optimization process.

This section has demonstrated the ability of the proposed Bayesian optimization technique with weighted POI cost function to deliver 7x smaller error and 3x faster computation time with more repeatable convergence than a state of the art non-linear, descent-based optimization routine. Compared to more conventional manual optimization, the proposed technique is 100 times faster on the presented 2D optimization problem and converges to within 1 mils of the known minimum. The following two sections will discuss how this technique can be applied to a 4-layer and 6-layer field grading geometry to develop design equations and insights in the system performance and limitations.

Table 4.4: 4-Layer Design Parameter Sweep

Parameter	Minimum	Increment	Maximum	Variants
Terminal Voltage	5 kV	1 kV	15 kV	11
Terminal Spacing	150 mils	10 mils	400 mils	26
PCB Thickness	60 mils	30 mils	180 mils	5
			Total Design Variants:	1430

4.3 Characterization of 4-Layer Grading Structure

The purpose of this study is to characterize the fundamental trade-offs and performance limitations of a 4-layer symmetric field grading structure using Bayesian optimization with weighted POI. The result of this study enables the designer to assess the fitness of a 4-layer structure for a given application with limited FEM and numerical optimization. The rules and design guidelines are directly enabled by the ability of Bayesian optimization to quickly and efficiently optimize the design over a range of operating conditions.

The symmetric 4-layer field grading structure is optimized over its three primary design constraints: 1) terminal voltage, 2) terminal spacing, and 3) PCB thickness. The range of each design variable is summarized in Table 4.4. Relative design performance will be compared with a field grading coefficient λ which is defined to be

$$\lambda = \frac{E_{pk-Grading}}{E_{pk-No-Grading}} \quad \rightarrow \quad E_{pk-Grading} = \lambda E_{pk-No-Grading} \tag{4.6}$$

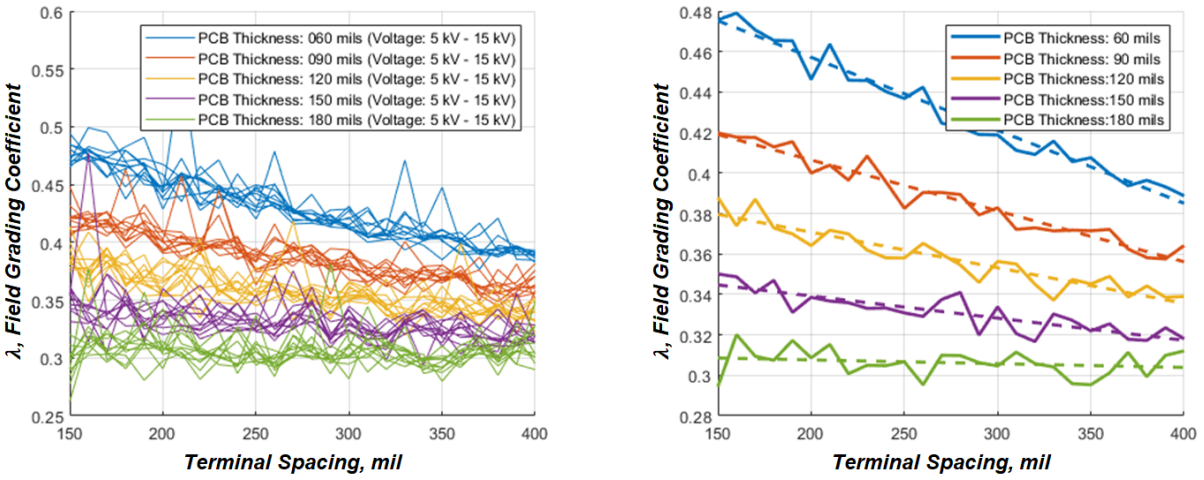
where $E_{pk-Grading}$ is the peak electric field strength with field grading, and $E_{pk-No-Grading}$ is the peak field strength without field grading.

By computing λ for a range of design cases, the designer need only run a single FEM simulation to establish the peak electric field strength without any field grading, and then determine an appropriate lambda to maintain the field at an acceptable level. In addition,

this approach will normalize out of the effect of terminal voltage meaning only two critical design parameters must be swept: terminal spacing and PCB height.

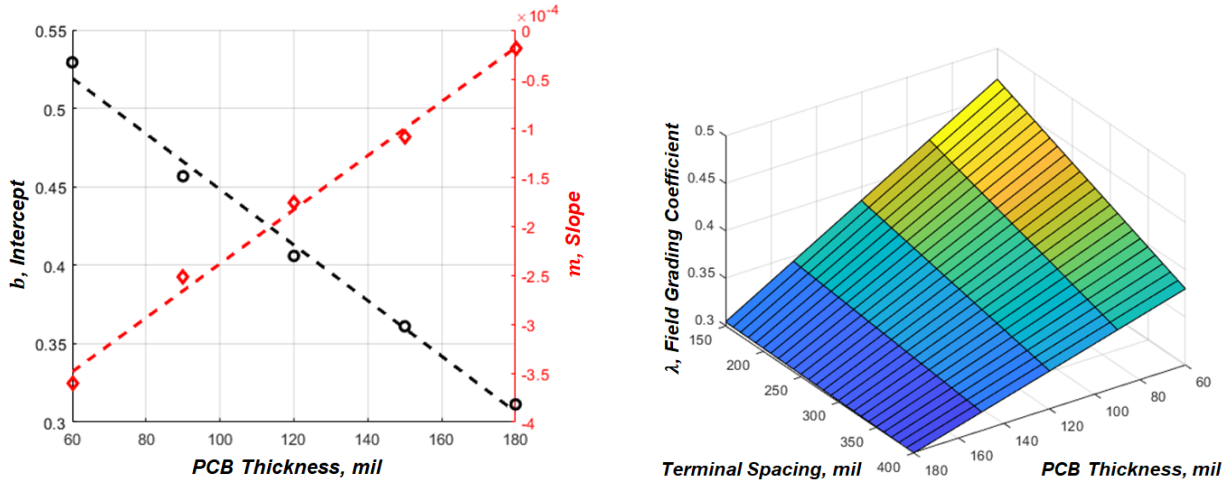
Figure 4.6 shows the results of the optimization. Figure 4.6a shows the field grading coefficient λ plotted for over the entire design range and shows how Eq. 4.6 normalizes out the dependence on voltage. Each grouping of curves is a sweep from 5 kV to 15 kV with no discernible difference in performance. Any dependence that does exist is less than the convergence tolerance and thus can be considered negligible.

Given the voltage independence, the curve groupings are averaged as shown in Figure 4.6b and a linear regression is fit. The slope and intercept of each linear regression are plotted vs. PCB thickness in Figure 4.7a. Similarly, the slope and intercept can be fitted with a linear regression which is combined with the regression data from Figure 4.6b to arrive at the surface approximation of λ as shown in Figure 4.7b. The field grading coefficient can now be expressed as a linear function of terminal spacing S, where the slope m and intercept



(a) (b)

Figure 4.6: a) The field grading coefficient λ (Eq.4.6) plotted vs. all design variants from Table 4.4 (pg. 59) shows that lambda is largely independent of voltage; b) The averaged data from all voltage curves plotted along with a linear regression (dashed line).



(a) (b)

Figure 4.7: a) The slope and intercept information from Figure 4.6b are plotted vs. PCB thickness and fit to a linear regression; b) The surface approximation of λ (Eq. 4.6) as a function of terminal spacing and PCB thickness.

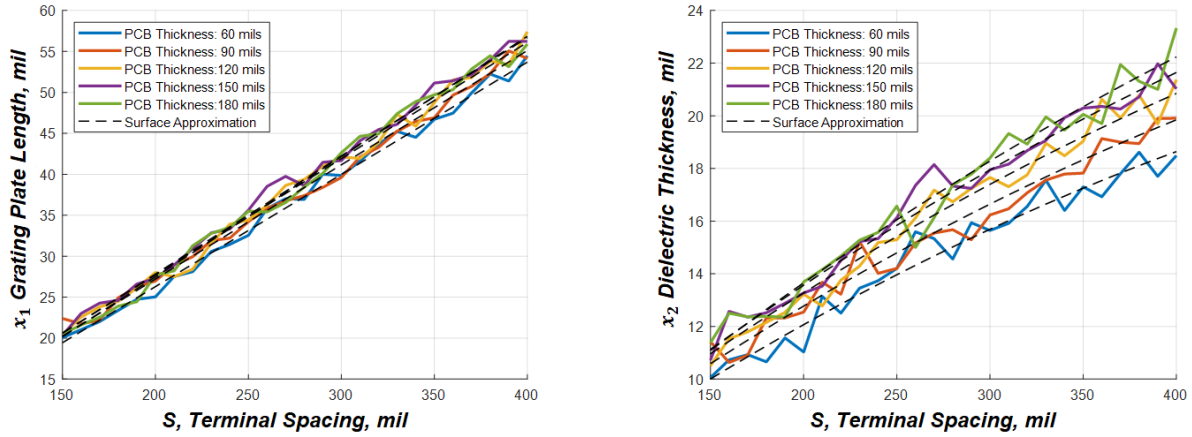
b are linear functions of PCB thickness h, as shown in Eq. 4.7.

$$\lambda(S,h) = m(h)S + b(h) \quad \text{where} \quad \begin{cases} m(h) = m_1 h + b_1 \\ b(h) = m_2 h + b_2 \end{cases} \tag{4.7}$$

Rearranging the above equation and substituting in the regression coefficients m_1, m_1, b_1, and b_2 yields the following surface approximation. The standard deviation of the regression error is 0.0054 which translates to approximately $\pm 5\%$ error.

$$\lambda(S,h) = c_1 + c_2 h + c_3 S + c_4 hS \qquad \begin{cases} c_1 = 0.626 & c_2 = -1.77e\text{-}3 \\ c_3 = -0.51e\text{-}3 & c_4 = 2.75e\text{-}6 \end{cases} \tag{4.8}$$

Given an efficient means of calculating the field grading coefficient for a given design case, the optimal design variables x_1 and x_2 must now be considered. Figure 4.8 shows the optimal



(a) x_1 (b) x_2

Figure 4.8: a) The optimal grading plate length x_1 as a function of the PCB height h and the edge-to-edge terminal spacing S; b) identical plot for the optimal dielectric thickness x_2.

dielectric height x_1 and the optimal plate length x_2 for the same design cases considered above. The curves shown are the average value of all the voltage curves, identical to the procedure used in Figure 4.6b. In a similar manner to Eq. 4.8, a surface is fit to both x_1 and x_2 as shown in Eq. 4.9 and 4.10 respectively. In these surface fits, additional quadratic terms are introduced to better model the behavior of the optimal design parameters. The resulting curve fits are overlaid in Figure 4.8 and the coefficients are shown in Eq. 4.9 and 4.10.

$$x_1(S,h) = c_1 + c_2 h + c_3 S + c_4 hS + c_5 h^2 \qquad \begin{cases} c_1 = -3.24 & c_2 = 49e\text{-}3 \\ c_3 = 132e\text{-}3 & c_4 = 81e\text{-}6 \\ c_5 = -231e\text{-}6 \end{cases} \tag{4.9}$$

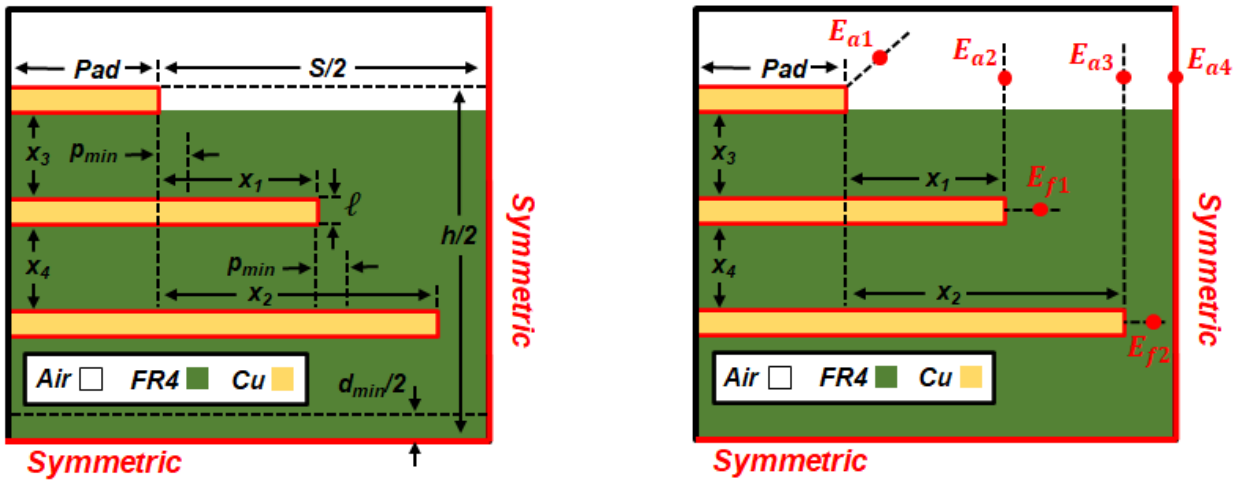
$$x_2(S,h) = c_1 + c_2 h + c_3 S + c_4 hS + c_5 h^2 + c_6 S.^2 \qquad \begin{cases} c_1 = 1.78 & c_2 = 24e\text{-}3 \\ c_3 = 48e\text{-}3 & c_4 = 83e\text{-}6 \\ c_5 = -114e\text{-}6 & c_6 = -33e\text{-}6 \end{cases} \tag{4.10}$$

Given Eq. 4.8, 4.9, and 4.10, both the field grading performance, and the optimal design parameters can be computed to within 5% by running only a single FEA simulation with no field grading plates to compute $E_{pk-no-grading}$. With the $E_{pk-no-grading}$ and the surface fit from Eq. 4.8, relative performance can be compared between all design variants without any additional FEA. From this comparison, a suitable PCB thickness h and terminal spacing S are selected, and the optimal design parameters can then be calculated using 4.9 and 4.10.

In this way, Bayesian optimization with weighted POI can be used to quickly and effectively characterize a field grading system with highly non-uniform electric fields quickly and efficiently. From the characterization, the fitness of the system for a given application can be quickly evaluated and systems can be designed and modified for a range of operating conditions, with limited simulation effort.

4.4 Characterization of 6-Layer Grading Structure

Building on the previous section, the complexity of the system can be scaled to a symmetric 6-layer field grading structure and characterized similarly. The parameterized geometry, as well as the necessary POIs are shown in Figure 4.9. The system requires four optimization variables x_1 - x_4 and six POIs, with four located in air E_{a1} - E_{a4} and two located in the FR-4 dielectric E_{f1} and E_{f2}



(a) (b)

Figure 4.9: a) Parameterized symmetric 6-layer field grading structure as described in Figure 4.1 (pg. 50) with constraints and fixed design variables b) POIs placed a distance ε from the singularity location. (See Table 4.1 on pg. 52 for material properties.)

The constraints are built out similarly to the previous section using a minimum useful plate length p_{min} and a minimum feasible dielectric thickness d_{min}. The plate length constraint is modified, ensuring that each plate is at least p_{min} longer than the previous plate or pad and does not extend past the line of symmetry.

$$\begin{aligned} p_{min} \leq x_1 \leq \frac{S}{2} \\ x_1 + p_{min} \leq x_2 \leq \frac{S}{2} \end{aligned} \tag{4.11}$$

The constraints for the dielectric heights x_3 and x_4 are constrained by fixing the PCB height h and solving for dielectric thickness just as in the previous section.

$$\begin{aligned} d_{min} \leq x_3 \leq h/2 - 3\ell - d_{min}/2 - x_4 \\ d_{min} \leq x_4 \leq h/2 - 3\ell - d_{min}/2 - x_3 \end{aligned} \tag{4.12}$$

Combining constraint equations 4.11 and 4.12, the 6-layer symmetric field grading optimiza-

tion problem can be formulated as shown in Eq. 4.13.

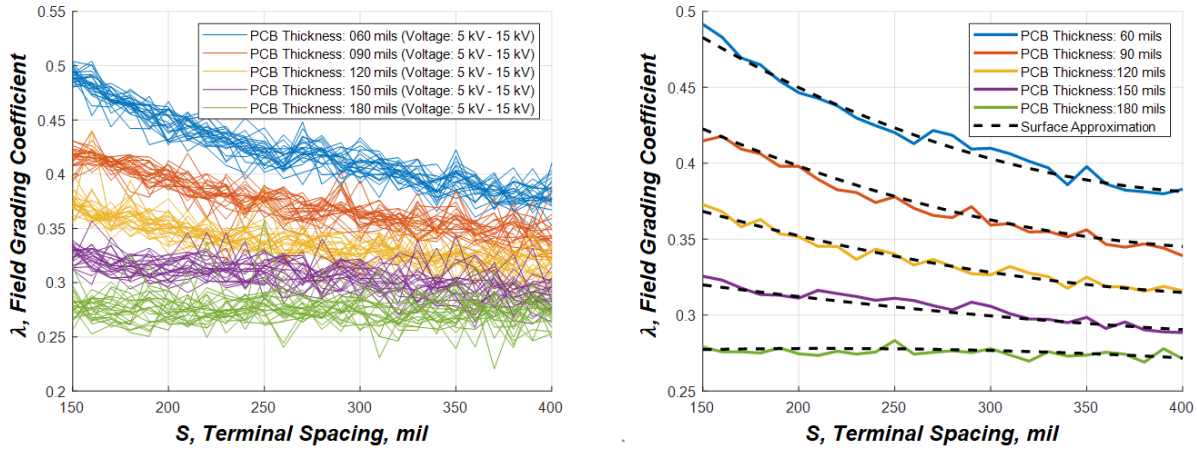
$$\begin{aligned} \min_{\vec{x}} \sum_{i=1}^{6} (FOS_i \times \eta_i)^p \\ p_{min} \leq x_1 \leq S/2 \\ x_1 + p_{min} \leq x_2 \leq S/2 \\ d_{min} \leq x_3 \leq h/2 - 3\ell - d_{min}/2 - x_4 \\ d_{min} \leq x_4 \leq h/2 - 3\ell - d_{min}/2 - x_3 \end{aligned} \tag{4.13}$$

The system is optimized for the same range of voltage V_{dc}, edge-to-edge terminal spacing S, and PCB thickness h as listed in Table 4.4 from the previous section. The performance in terms of a field grading coefficient λ is shown in Figure 4.10. Figure 4.10a once again shows how the field grading coefficient can normalize out the effect of terminal voltage and show the relative field reduction of the design. Figure 4.10b shows the averaged performance with a surface approximation shown by the dashed line. The equation of the surface regression is shown in Eq. 4.14.

$$\lambda_6(S,h) = c_1 + c_2 h + c_3 S + c_4 hS + c_5 h^2 + c_6 S^2 + c_7 hS^2$$

$$\text{where} \begin{cases} c_1 = 0.829 & c_2 = -3.69 \times 10^{-3} \\ c_3 = -1.69 \times 10^{-3} & c_4 = 9.79 \times 10^{-6} \\ c_5 = 3.24 \times 10^{-6} & c_6 = 1.98 \times 10^{-6} \\ c_7 = -12.0 \times 10^{-9} \end{cases} \tag{4.14}$$

The optimal design variables x_1 - x_4 along with their corresponding surface fit approximations are shown in Figure 4.11. Four separate quadratic surface regressions are required to fit all of the optimization variables. The coefficients of the equations will be summarized in table



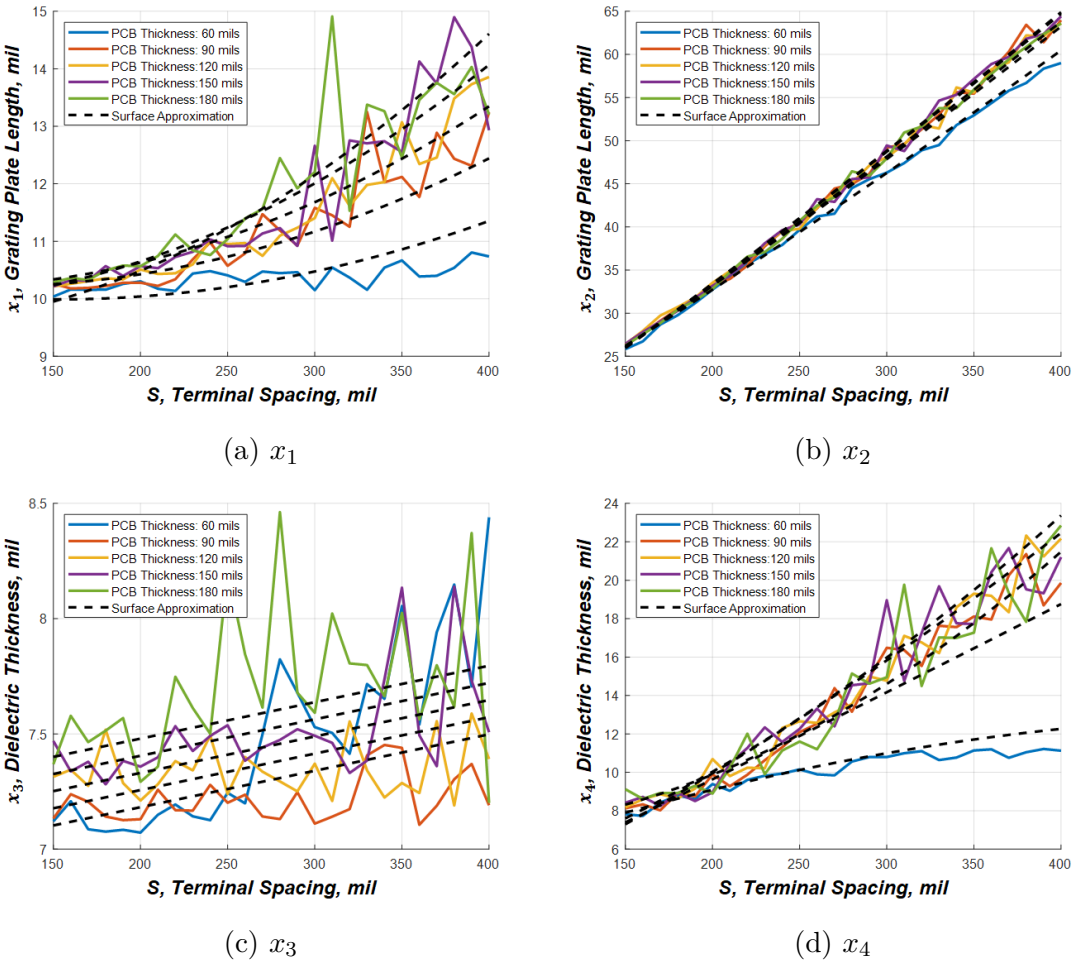
(a) (b)

Figure 4.10: a) The field grading coefficient λ (Eq. 4.6) plotted vs. all design variants from Table 4.4 (pg. 59) shows that lambda is largely independent of voltage; b) The averaged data from all voltage curves plotted along with a surface regression (dashed line).

format in the following section.

Several key observations can be made from the optimized variables and their corresponding surface approximations in Figure 4.11. First, note how the case for $h = 60$ mils is an outlier in almost every case. It is suspected that the sudden change in optimal value could be caused by the algorithm converging to a higher minimum on account of the preferred minimum lying outside the constrained region. The constraint for x_4 (Eq. 4.12) is a function of h. As a result, a minimum that exists at $x_4 = 25$ mils is only valid for $h > 60$ mils, assuming a d_{min} of 5 mils. It is possible that as h decreases, the preferred minimum becomes either invalid or too close to the axis of symmetry, dramatically changing the system dynamics. A more detailed system characterization could use finer increments of h to resolve and clarify this behavior.

The second observation is the noise present in the results, most notably in x_1 and x_3 and the general poor quality of the surface fits. The prominent error of x_3 stems from the convergence tolerance of the algorithm. Section 4.2 found the convergence error of the algorithm to be



(a) x_1 (b) x_2

(c) x_3 (d) x_4

Figure 4.11: The optimal plate lengths x_1 (a) and x_2 (b), and dielectric heights x_3 (c) and x_4 (d) for a symmetric 6-layer field grading structure vs. PCB thickness h and edge-to-edge terminal spacing S, with quadratic surface approximations shown by the dashed line.

on the order of 1 mil which becomes increasingly prominent as the value of the optimization variable decreases, as in the case of x_3 which is on the order of 8 mils. This amount of noise makes a high-quality surface fit difficult, however, the application does not require a surface fit more accurate than the one provided. While the fit appears sub-optimal, it can deliver a 3σ error bar of ± 0.8 mils, which is below the convergence error of the algorithm and on the order of PCB manufacturing tolerance.

4.5 Summary

This chapter demonstrated how the Bayesian optimization algorithm with weighed POI excels at the optimization of highly non-uniform electric fields in systems with intense field crowding and complicated geometry. The convergence performance of the technique was qualitatively compared to a state-of-the-art nonlinear descent-based interior-point algorithm and a manual optimization technique.

A 2D benchmark problem was selected so the domain, as well as the initial and final design points, could be easily visualized. The domain was demonstrated to be largely convex, but corrupted with shallow minimums and discontinuities as stated in Chapter 3. The convergence performance and simulation time of each technique was compared and it was found that on average, the proposed algorithm is 3x faster and converges with 7x less error than interior-point algorithm, and is 100x faster than manually optimizing the system.

Next, Bayesian optimization was used to characterize the performance limitations and trade-offs of a 4-layer and 6-layer symmetric field grading structure. With the proposed technique, each system is quickly characterized using a field grading coefficient, allowing the performance of each design to be evaluated over a set of design variables. After characterization, the optimal design variables and grading coefficient of each system are approximated using a low-order polynomial surface regression, yielding a framework for systems to be quickly design and evaluated with limited FEA simulation. A summary of the polynomial surface fits is provided in Tables 4.5 and 4.6.

The following chapter will show how these characterization results can be used for the rapid design and optimization of a high-density, PCB-integrated bus bar and module interface for a 10 kV, 80A SiC MOSFET power module.

Table 4.5: 4-Layer Polynomial Surface Approximations

	units	$\lambda_4(h,S)$	$x_1(h,S)$	$x_2(h,S)$
1	mils	0.829	-3.24	1.78
h	mils	-3.69e-3	49.4e-3	24.0e-3
S	mils	-1.69e-3	132e-3	48.0e-3
hS	mils^2	9.79e-6	81.2e-6	83.5e-6
h^2	mils^2	3.24e-6	-232e-6	-114e-6
S^2	mils^2	1.98e-6	-	-33.6e-6
h^2S	mils^3	-12e-9	-	-
hS^2	mils^3	-	-	-
$3\sigma\ Tol.$	mils		$\pm$ 2.5	$\pm$ 1.6

Table 4.6: 6-Layer Polynomial Surface Approximations

	units	$\lambda_6(h,S)$	$x_1(h,S)$	$x_2(h,S)$	$x_3(h,S)$	$x_4(h,S)$
1	mils	0.829	9.89	13.9	6.72	15.6
h	mils	-3.69e-3	16.4e-3	-132e-3	2.47e-3	-281e-3
S	mils	-1.69e-3	-8.54e-3	79.5e-3	1.58e-3	-21.0e-3
hS	mils^2	9.79e-6	29.9e-6	828e-6	-	1.36e-3
h^2	mils^2	3.24e-6	-101e-6	467e-6	-	1.29e-3
S^2	mils^2	1.98e-6	13.5e-6	33.5e-6	-	-101e-6
h^2S	mils^3	-12e-9	-	-	-	-7.11e-6
hS^2	mils^3	-	145e-9	-2.96e-9	-	1.16e-6
$3\sigma\ Tol.$	mils		$\pm$ 1.5	$\pm$ 2.1	$\pm$ 0.8	$\pm$ 3.5

Chapter 5

Design Case Study

With the performance of 4-layer and 6-layer field grading systems fully characterized, a design case study is presented for a high-density PCB-integrated bus bar for a 10 kV SiC MOSFET power module. The design will build on the system presented in [3], (Figure 2.7) with improved internal field grading and a redesigned module housing to assist further alleviate field crowding. Both the internal structures and module housing will be designed with the Bayesian optimization procedure, with some initial design evaluation carried out with manual optimization.

Section 5.1 will give an overview of the module footprint and system layout and how it is decomposed into critical design regions which can be modeled in the optimization framework. Sections 5.2 and 5.3 will discuss the optimization and design of both the bus bar and module housing respectively, including how both portions of the design can be rapidly accelerated using the characterization data from the previous chapter. It is important to note that a full system characterization is not required for the design of the presented field grading system. As shown in the following section, this particular system contains many critical design regions with different terminal spacings, all requiring slightly different variants of the field grading geometry and thus it is beneficial, though not required, to have a comprehensive characterization of the geometry.

This will be followed by an overview of the experimental results. The designed bus bar will be tested in a PDIV test setup along with a previous version of the bus bar that was

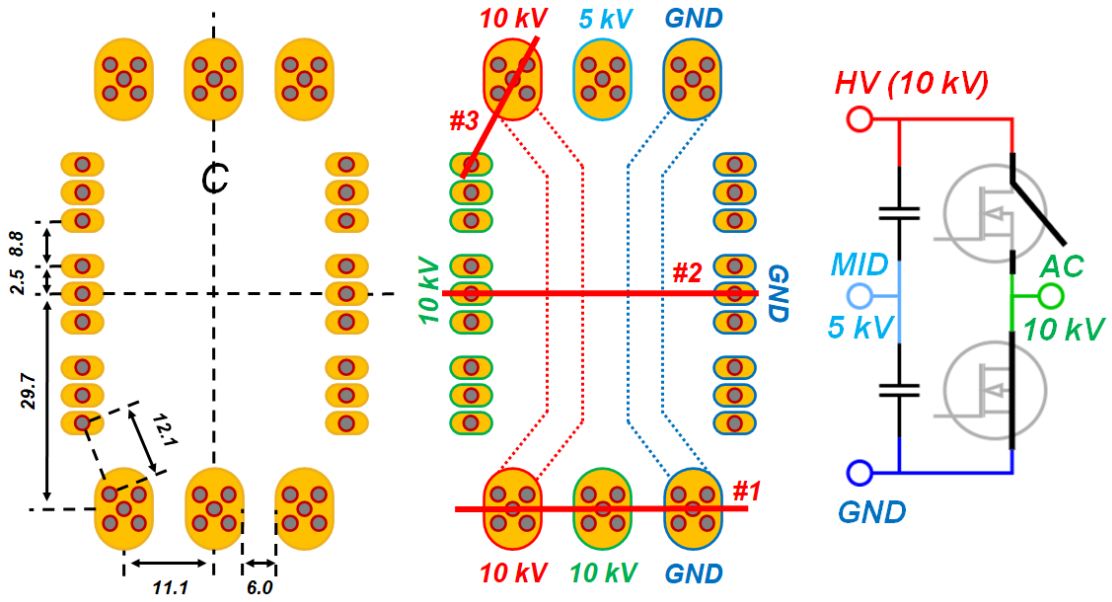
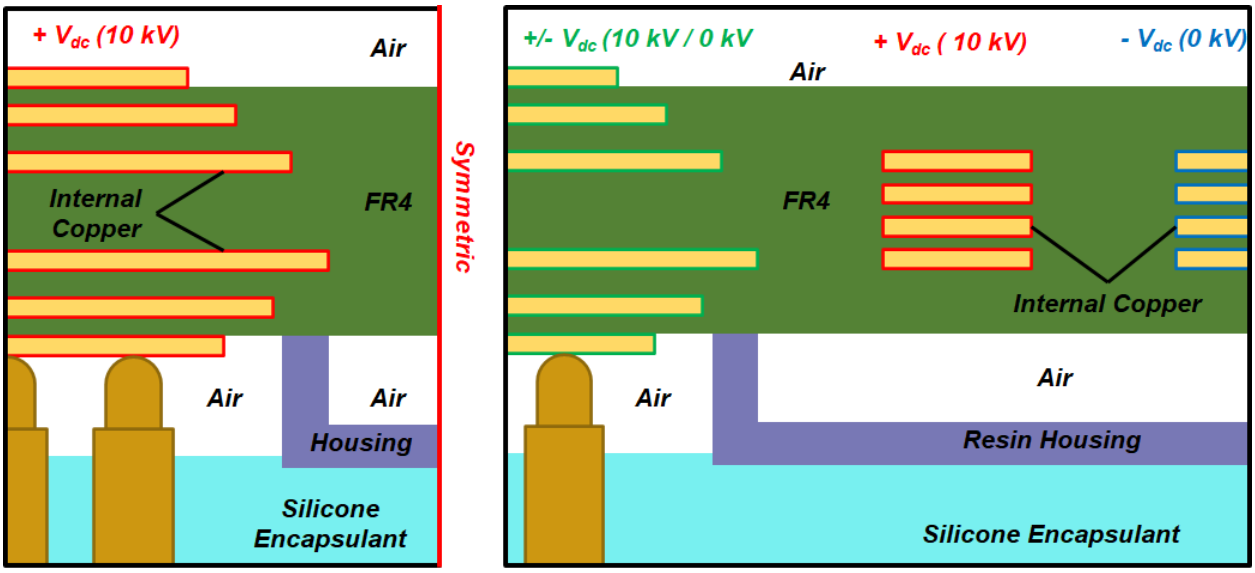


Figure 5.1: Footprint of 10 kV, 80 A, SiC MOSFET power module with key dimensions (shown in mm) and potentials. Critical design regions are indicated with a bold red line and labeled #1 - #3.

design exclusively using manual optimization techniques. The previous version will serve as a benchmark from which to compare the performance and design cycle time of the current version.

5.1 Module Layout

The module layout is shown in Figure 5.1 along with pertinent dimensions and the potential of each pad during operation. Figure 5.1 also shows three critical regions indicated by the bold red lines and numbered #1 - #3. Critical regions are identified as locations with the highest voltage potential across the smallest spacings. While the spacing between the pads in region #2 is large relative to the other spacings, the internal high-voltage traces in the PCB (indicated by dashed lines) exacerbate field crowding around the terminals.



(a) (b)

Figure 5.2: a) Critical regions #1 and #3 (as defined in Figure 5.1 on pg. 71) shown as one half of the symmetric domain; b) critical region #2 which cannot be simplified by symmetry.

With critical regions identified, the footprint and housing can be represented in 2D as shown in Figure 5.2. Figure 5.2a shows the 2D representation of regions #1 and #3 as both regions are identical except for the terminal spacing and both can be further reduced by symmetry. Fig. 5.2b shows regions #2 which cannot be reduced by symmetry.

Each section can now be parameterized in terms of the critical design variables. The design process of critical region #1 will be discussed in detail in the following sections. The other regions were designed identically.

5.2 Bus Bar Design Optimization

Critical region #1 is designed in two sections, the top side and the bottom side, as shown in Figure 5.3. Splitting the domain between top and bottom, in addition to the symmetric condition along the y-axis, reduces the number of optimizable variables in each problem,

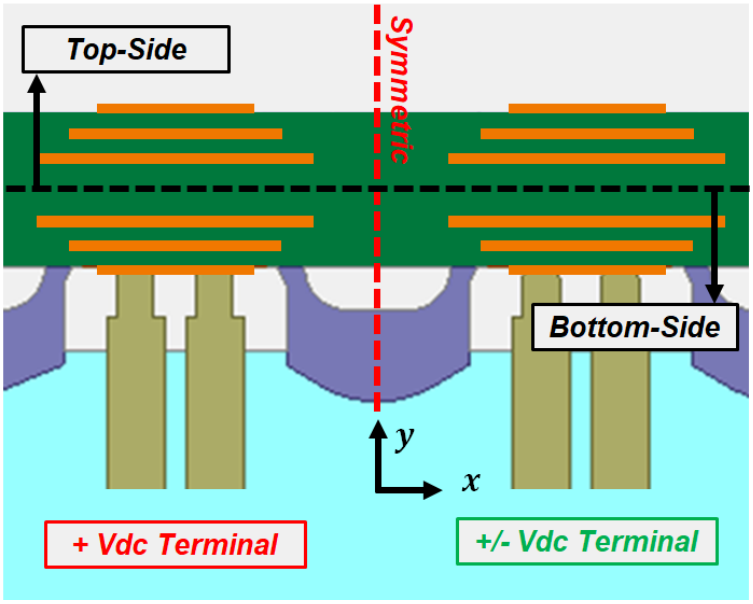


Figure 5.3: Full schematic of critical region #1 (as defined in Figure 5.1 on pg. 71) showing how the domain is split between the top and bottom as well as the symmetry condition along the y-axis.

simplifying the optimization.

From the footprint in Figure 5.1, the terminal spacing of critical region #1 is 6.1 mm or 240 mils. Using the field grading coefficient surface fits from Eq. 4.8 and Eq. 4.14, the achievable field reduction of a 4-layer and 6-layer structure with a terminal spacing of 240 mils vs. height is plotted in Figure 5.4. From the polynomial regression, it is seen that a 6-layer structure provides significantly more field reduction than a 4-layer structure with the same terminal spacing of 240 mils. In addition to providing improved field reduction, a 6-layer structure will allow for additional design flexibility when the housing is designed and mated to the bus bar. A PCB finish height of 150 mils is selected, which yields an estimated electric field reduction of $1 - \lambda$ or approximately 70%. The completed bus bar will have a total of 10 layers, six for field grading and four reserved for the high-current internal traces (visible in Figure 5.2b).

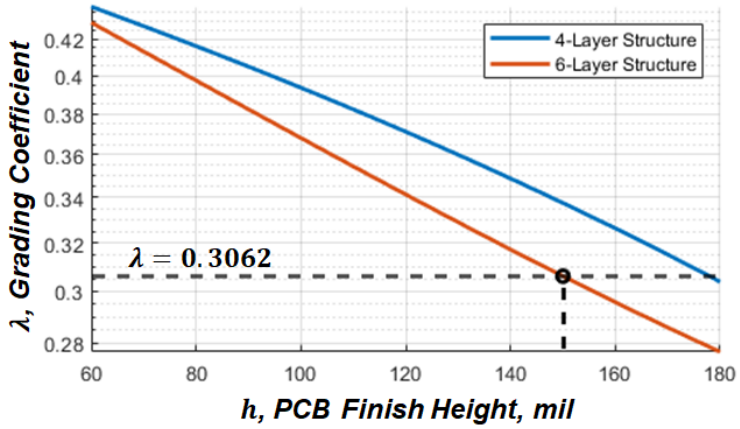


Figure 5.4: The polynomial surface approximations from Eq. 4.8 and 4.14 used to determine the structure (layer count) and PCB height of critical region # 1 (as defined in Figure 5.1 on pg. 71).

With the layer count and h selected, the quadratic surface approximations from Table 4.6 are used to calculate the optimal design parameters x_1, x_2, x_3, and x_4. The optimized bus bar design for critical region #1 is summarized in Table 5.1 and the resulting FEA field simulation is shown in Figure 5.5. These parameters are used as the final design for the top section, and as an initial design point for the bottom section to evaluate potential housing designs.

5.3 Housing Design Optimization

The optimized bus bar design in Table 5.1 can now be used as an initial design point to evaluate potential housing designs. Figure 5.6 shows three prospective design variants as well as a baseline design, each with the corresponding simulated electrostatic performance.

Design 3 (Figure 5.6d) is selected from the proposed design variants as it achieves the greatest electric field reduction when compared to the baseline and also falls within the manufacturing

Table 5.1: Parameters for Optimized Field Grading Geometry

	Parameter	Value
Design Parameters	Spacing S	240 mils
	PCB Height h	150 mils
	Terminal Voltage V_{dc}	10 kV
Optimization Parameters	x_1	269 μm
	x_2	989 μm
	x_3	184 μm
	x_4	291 μm
Performance Metrics	E_{pk} at Pad Edge	2 kV/mm
	Grading Coefficient λ	0.3062
	Field Reduction $(1-\lambda)$	70%

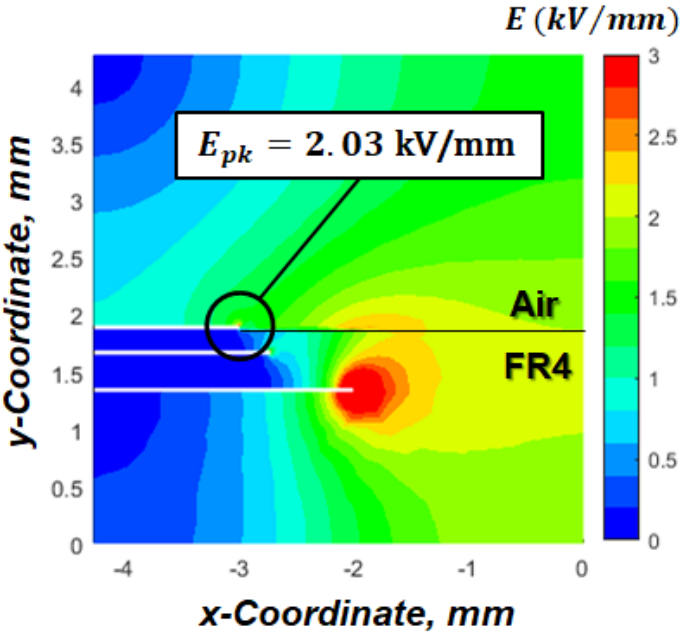
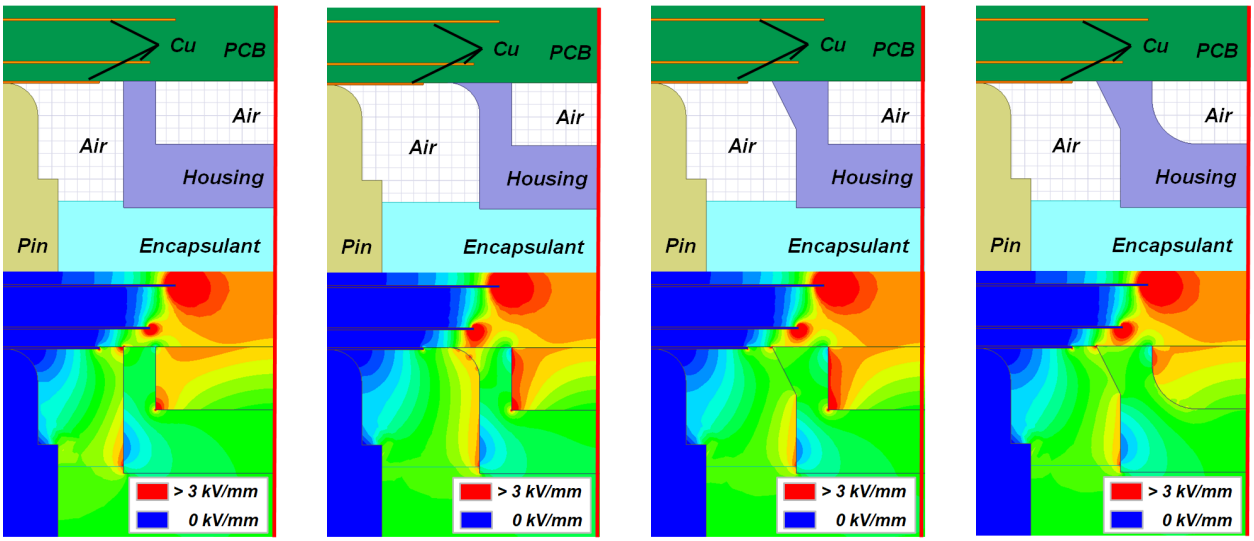


Figure 5.5: FEA electrostatic field simulation of optimized symmetric 6-layer field grading structure for critical region #1 (as defined in Figure 5.1 on pg. 71). See Table 4.1 on pg. 52 for material properties and Table 5.1 on pg. 75 for dimensions.



(a) Baseline (b) Design 1 (c) Design 2 (d) Design 3

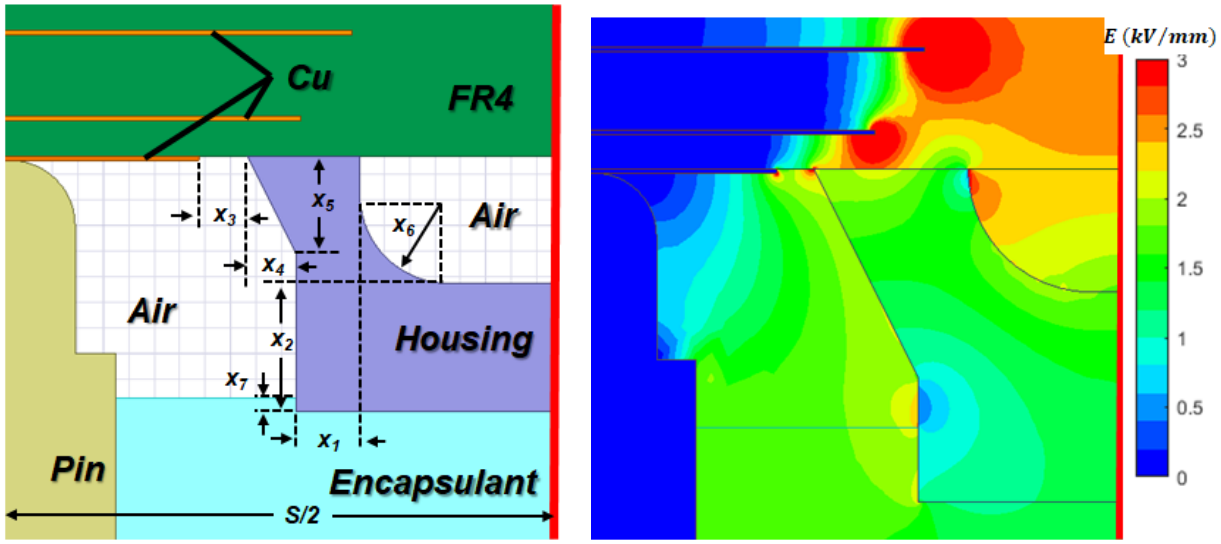
Figure 5.6: Four potential design variants for the housing (as shown in Figure 5.3 on pg. 73) evaluated for the shape of the housing interface. Each variant is simulated to qualitatively assess its effect on the field grading performance before detailed design optimization. See Table 4.1 on pg. 52 for material and simulation parameters.

capability of standard processes such as injection molding and printing. Design 1 (Figure 5.6b), in contrast, uses a thin, tapered geometry to mate with the bus bar and is not readily manufacturable using conventional techniques.

With the design selected, the system is parameterized as shown in Figure 5.7a, and a constraint system is built out similarly as for the 4-layer and 6-layer field grading geometries from the previous section. The design is optimized and the resulting electrostatic field performance of the optimized design is shown in Figure 5.7b. The optimized design parameters are shown in Table 5.2.

Table 5.2: Optimal Design Parameters for Housing Interface

Parameter	**Value**	**Parameter**	**Value**
x_1	400 μm	x_4	850 μm
x_2	1.7 mm	x_5	1.7 mm
x_3	300 μm	x_6	1.0 mm

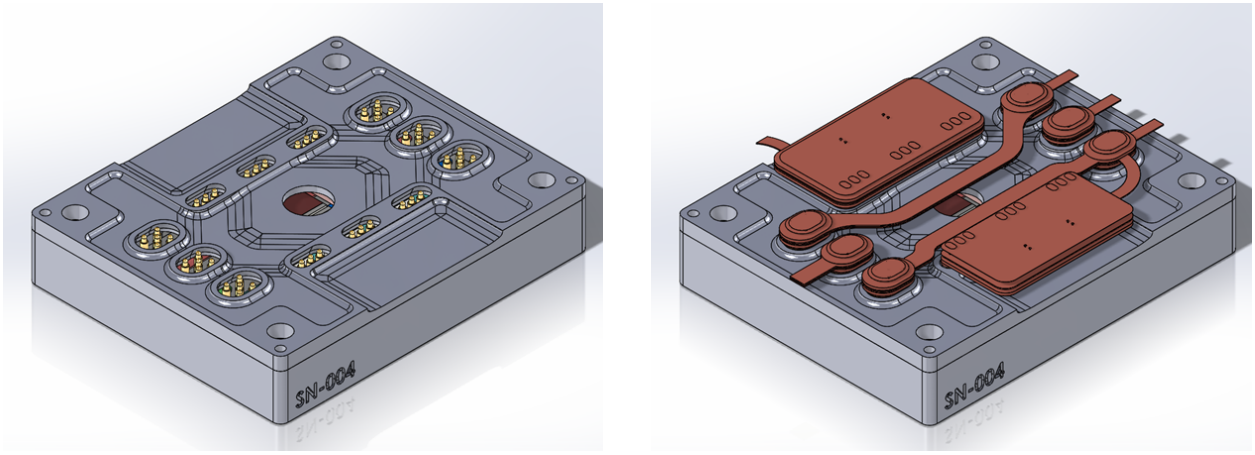


(a) (b)

Figure 5.7: a) The parameterized lid design used for optimization in addition to the field grading optimization parameters from Figure 4.9 on pg. 64; b) the simulated electrostatic performance of the optimized lid and bus bar design. See Table 4.1 on pg. 52 for material and simulation parameters and Table 5.2 for dimensions.

With the housing and bus bar optimized for the first critical region. The same process is applied to each of the two remaining regions. Using the characterization data from Chapter 4, the complete system was designed and optimized in a matter of days. The Bayesian optimization and resulting characterization data enable a significant reduction in design cycle time when compared to conventional manual optimization techniques. The cycle time of the previous bus bar design was on the order of eight weeks and no significant performance insights were gained.

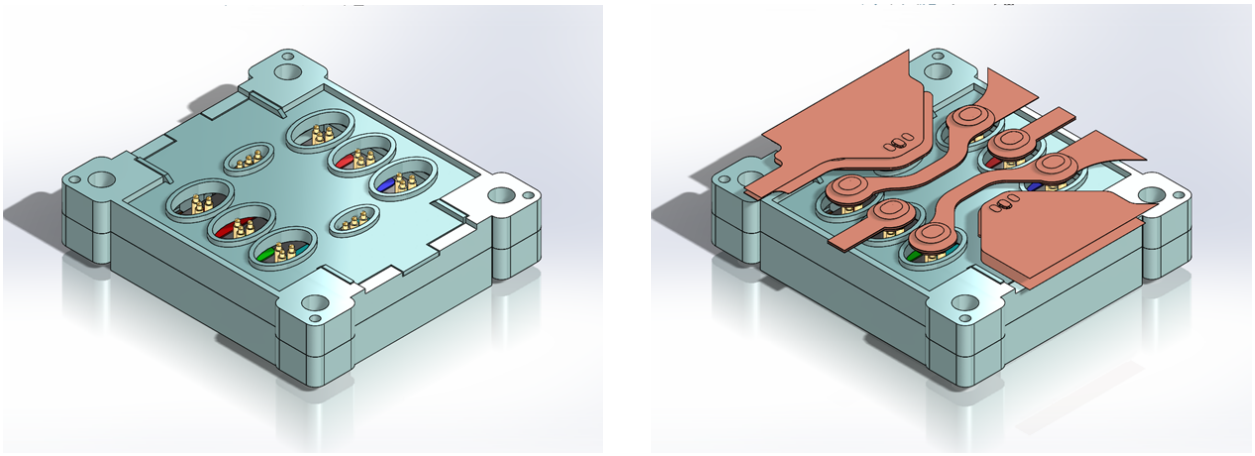
The final designs of both the bus bar and module housing are shown in Figure 5.8. The manually-optimized previous version is shown in Figure 5.9. The footprint of the old region is slightly different as it was designed for a 25 A version of the SiC MOSFET power module and thus has only a single gate connection on the high- and low-side for a single device. However, the critical design regions are the same for both footprints. The critical regions of



(a) (b)

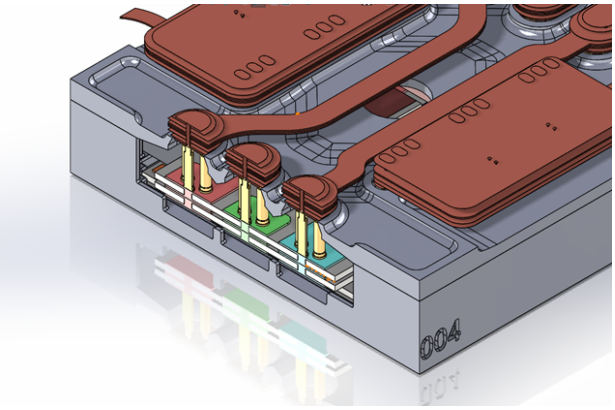
Figure 5.8: a) The high-density 10 kV module housing designed with Bayesian optimization; b) the housing shown with the internal geometry of the PCB-integrated bus bar.

each design are shown in Figure 5.10.

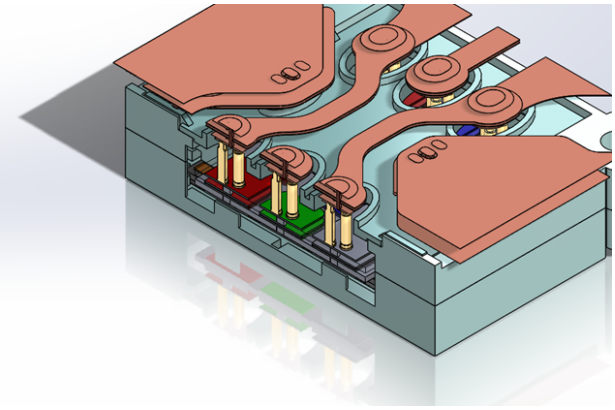


(a) (b)

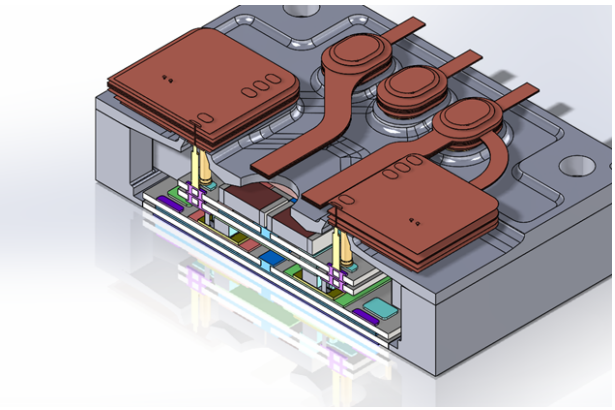
Figure 5.9: a) The previous version of the 10 kV module housing designed exclusively via manual optimization; b) the housing shown with the internal geometry of the old PCB-integrated bus bar.



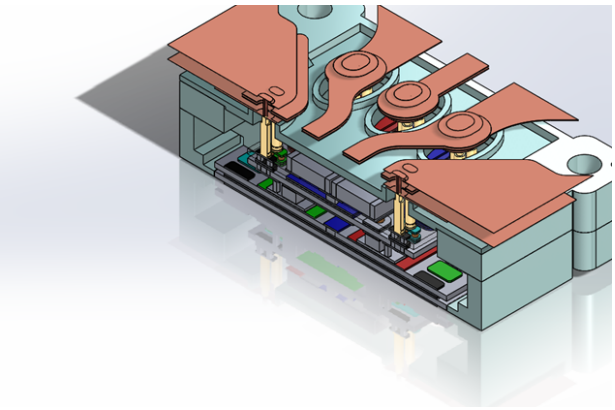
(a) Bayesian: Region #1



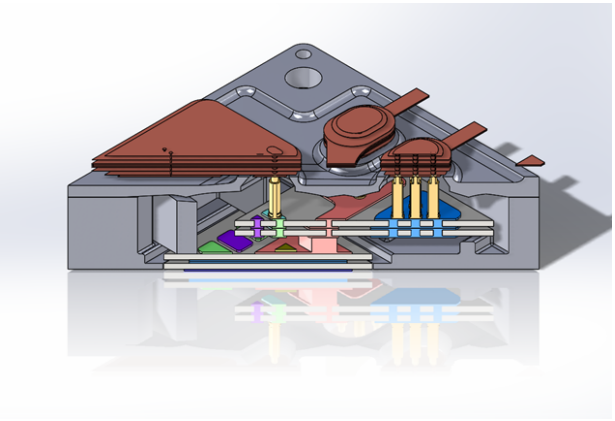
(b) Manual: Region #1



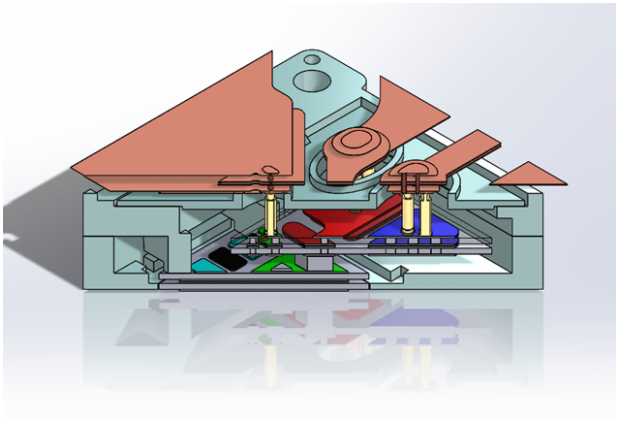
(c) Bayesian: Region #2



(d) Manual: Region #2



(e) Bayesian: Region #3



(f) Manual: Region #3

Figure 5.10: All optimized critical design regions as defined in Figure 5.1 (pg. 71) for both the manually optimized (Figure 5.9) and the Bayesian optimized (Figure 5.8) versions of the bus bar and housing.

5.4 Experimental Verification

Experimental verification of the module housing and PCB-integrated bus bar are carried out by partial discharge testing. The numerically optimized geometry is benchmarked against the manually optimized geometry shown in Figure 5.10. The manually optimized variant was tested early in the project before more advanced PD test capability was available and thus no phase-resolved partial discharge (PRPD) plots are available. The manual variant was tested using a high-frequency current transformer (HFCT) in an EMI chamber which while accurate, does not allow for PRPD plots. The numerically optimized variant was tested using more sophisticated equipment (Section 5.4.1), allowing for a more in-depth analysis of the results.

5.4.1 Partial Discharge Test Setup

The partial discharge test setup is shown in Figure 5.11 and uses a variable output, 100 kV 60 Hz ac supply with a 1 nF, 100 kV coupling capacitor, and an Omicron® MPD 600 PD measurement and analysis system. The system is calibrated per the IEC 60270 standard with a 10 pC charge injection.

PD tests were carried following IEC 60664 standard for insulation coordination for equipment within low voltage systems, except for a few minor deviations due to capability limitations. Required voltage ramp rates and timing as outlined in IEC 60664 could not be achieved due to the use of a manually controlled voltage source. In addition, since the high-voltage source is simply a transformer fed from 120 Hz ac from a standard wall outlet, some distortion is present in the excitation. The distortion can vary based on the capacitance of the test coupon as shown in the following section.

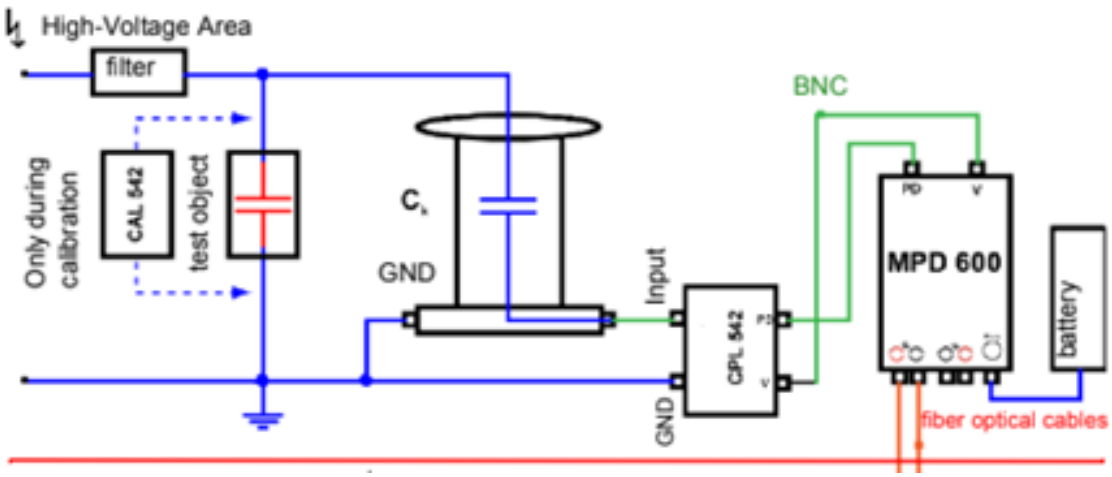
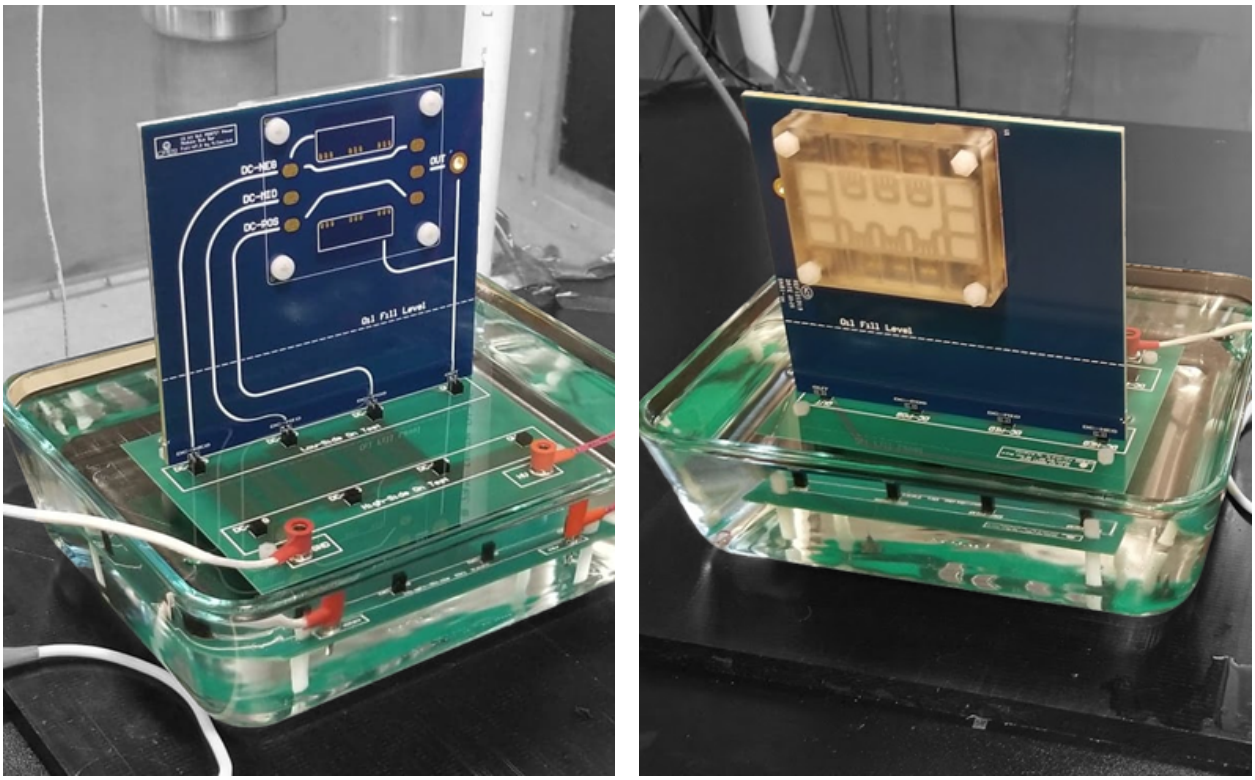


Figure 5.11: Schematic of the partial discharge test setup showing the test coupon and coupling capacitor interfaced to the MPD 600. (Image courtesy of Omicron® MPD 600 Operator Manual.)

The PCB integrated bus bar is tested both as a bare PCB, to verify the field grading design, and mated to the module, to verify the module interface. The interface is tested using a PD test module as opposed to a functional package. The module is constructed to be electrostatically equivalent to a functional package but contains no functional devices, and the internal geometry is de-featured.

Fig. 5.12 shows the PCB-integrated bus bar both with and without the PD dummy module attached. For testing, the bus bar is inserted into a baseboard which energizes the terminals of the bus bar differently depending on the test slot that is used. This allows for testing of both high-side-on and low-side-on test conditions. During partial discharge testing, the baseboard, as well as the high-voltage connections from the power supply, are submerged in Shell Diala® S4 dielectric oil to ensure PD only occurs in the desired test region.

The high-side-on and low-side-on test conditions are required as the bus bar will be energized differently depending on whether the high-side or low-side switch of phase leg is active. A schematic representation and associated potentials are shown in Figure 5.13. A capacitor bank made of high-voltage MLCCs is integrated onto the baseboard and used as a voltage



(a) (b)

Figure 5.12: Partial discharge test setup showing the PCB-integrated bus bar mounted to the baseboard with the high-voltage interconnects submerged in oil, a) the bare PCB and b) the PCB mated to the partial discharge test module.

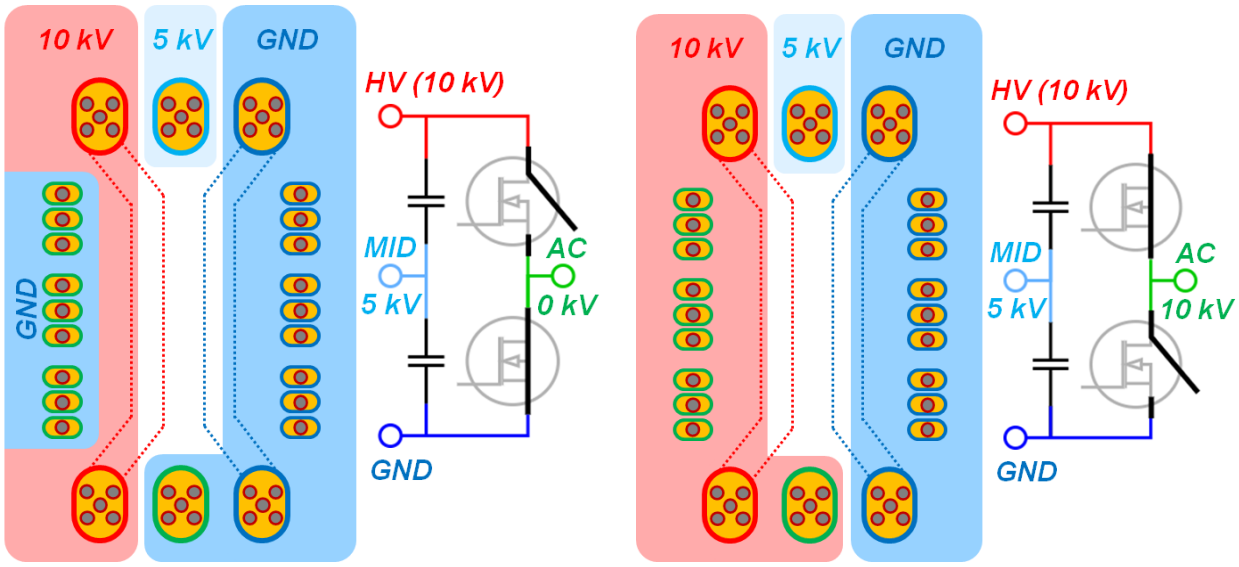


Figure 5.13: a) Low-side-on PD test condition connects the high-side gate, low-side gate, and AC node to ground, leaving only the high-side drain connected to high-voltage; b) High-side-on test condition connects only the low-side gate and source to ground.

divider to generate the mid-point voltage for the footprint.

Lower distortion of the excitation voltage is present when testing with the PD test module as the test module contains additional embedded high-voltage MLCCs. Capacitors are included in the PD test module as they are present in the functional module and are placed close to the spring terminals, and thus affect the electric field near the spring pins.

5.4.2 Test Results

Ten PCBs in total were tested starting with the bare PCB (no PD test module). Of the ten PCBs, four failed during the test due to destructive breakdown across the test region before any PD was observed. The damage on the PCB pads after a breakdown is shown in Figure 5.14. This behavior of breakdown before observed PD indicates a highly uniform electric field in the test region and thus serves as a preliminary verification of the system.

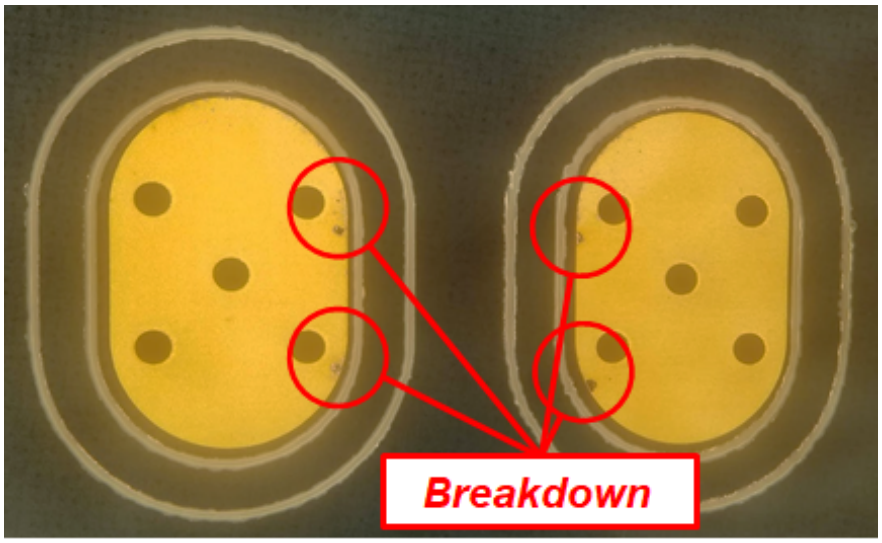


Figure 5.14: Destructive breakdown occurring on the surface of the PCB when PD tested without the PD test module attached. The breakdown occurred between the $+V_{dc}$ and $\pm V_{dc}$ pads of the bus bar along critical cross-section 1 (as defined in Figure 5.1 on pg. 71)

The damage on the pads shows symmetric discharge occurring evenly over the width of the pad, further suggesting and highly uniform electric field.

Of the size remaining PCBs, the median partial discharge inception voltage (PDIV) was 12.3 kV rms. The PRPD plot and corresponding Q_{IEC} (as defined in IEC 60664) vs. time plot is shown in Figure 5.15. The plot shows no PD $>$ 10 pC in magnitude up to 12.1 kV rms. The $\sim$2 pC Q_{IEC} visible for the duration of the test is the noise threshold of the test setup and is not representative of PD occurring in the system. To avoid potential breakdown, the test was stopped before significant PD occurred.

Given the test results for the bare PCB, the PD test module was mated to the bus bar and the same tests were run again. The median PDIV of the tests was 11.6 kV rms. The PRPD plot and corresponding Q_{IEC} plot are shown in Figure 5.16. Note the harmonic distortion of the excitation wave is significantly lower due to the added capacitance of the PD test module. In this test, significant sustained PD occurred at ll.7 kV rms.

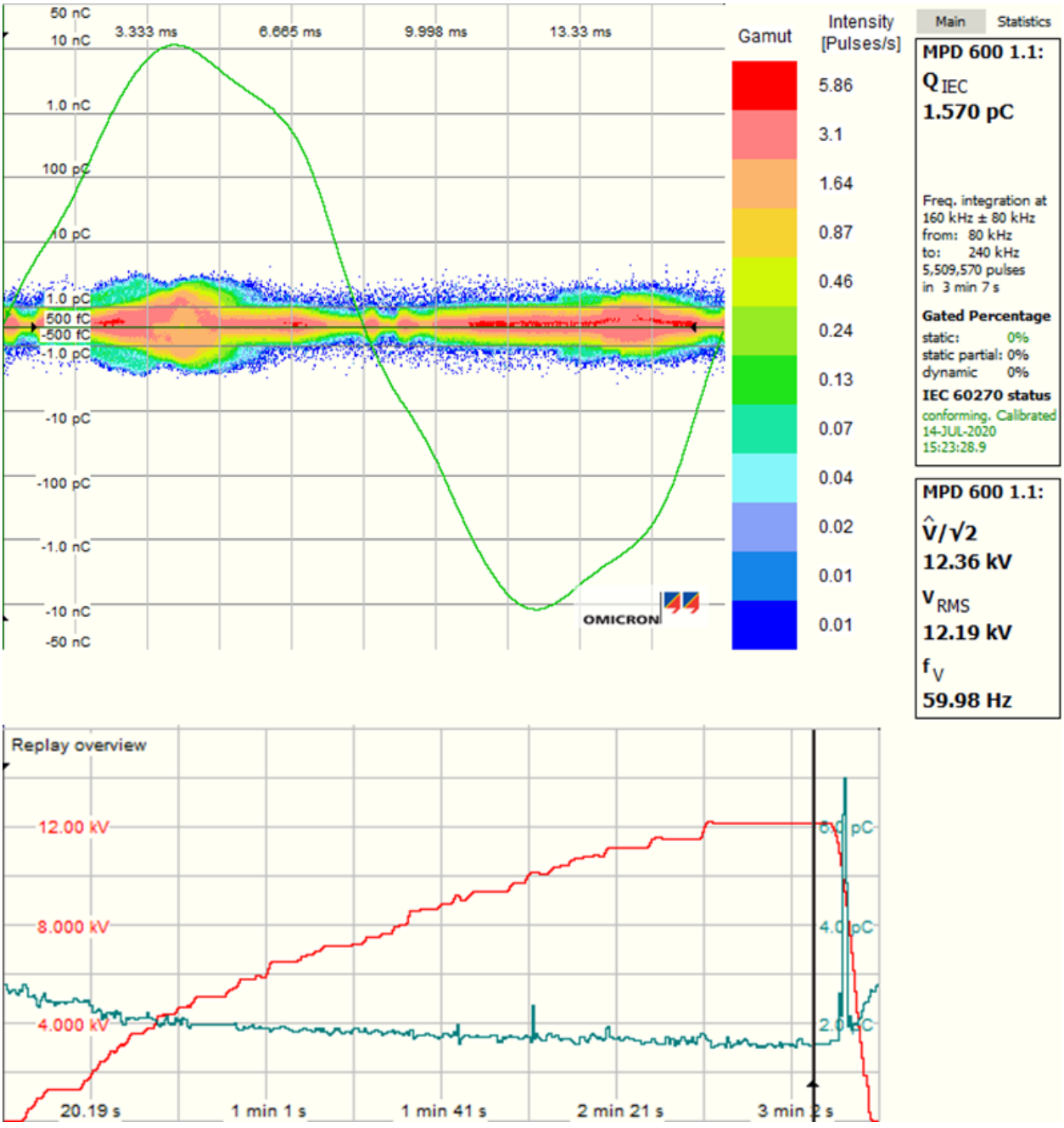


Figure 5.15: PRPD plot of low-side-on test with bare PCB bus bar as shown in Figure 5.12a on pg. 82.

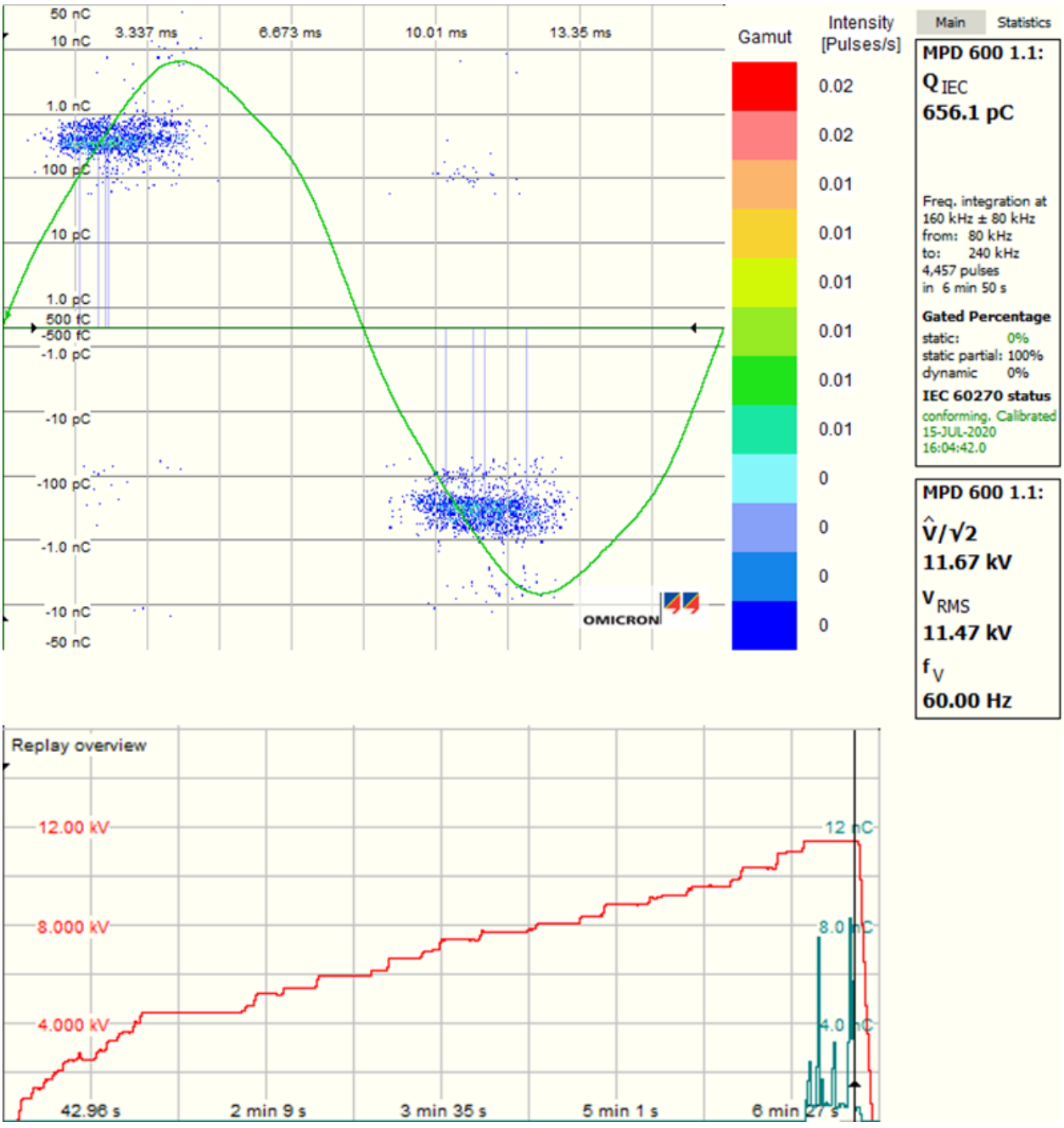


Figure 5.16: PRPD plot of low-side-on test with PCB bus bar mated to PD dummy module as shown in Figure 5.12b on pg. 82.

From the PD distribution from the PRPD plot is indicative of PD occurring within a void as opposed to corona discharge in the air[92]. While the void could be present in the FR-4 of the PCB, the previous tests of the bare PCB did not indicate this behavior and thus it can be concluded the void is present in the PD test module, contained either in the silicone encapsulant or perhaps within the contained AlN substrate. This test result indicates that the PCB bus bar and the housing/bus bar interface are not the limiting factors of the design and instead, the insulation performance of the system is limited by the fabrication techniques of the 10 kV power module.

This contrasts with the performance of the manually optimized variant, where the performance is limited by the interface. The manual variant was tested similarly, with the individual test performed for the low-side-on and high-side-on configurations, both with and without a PD test module. The only significant test variation was the use of an HFCT to detect PD as opposed to the MPD-600.

Comparing the performance of the two systems using two different test setups is allowable because, when tested with the PD test module, the manual variant exhibited a destructive breakdown before observable PD as shown in Figure 5.17 Since the means of measuring the voltage is consistent between both tests, direct comparison of the breakdown voltages is allowable. The breakdown of the manual variant occurred at 8.4 kV rms, 38% lower than the 11.6 kV rms PDIV of the numerically optimized version. A summary of the test results is shown in Table 5.3.

5.5 Summary

This chapter presented the design, optimization, and experimental verification of a high-density, PCB-integrated bus bar with embedded field grading geometry that successfully

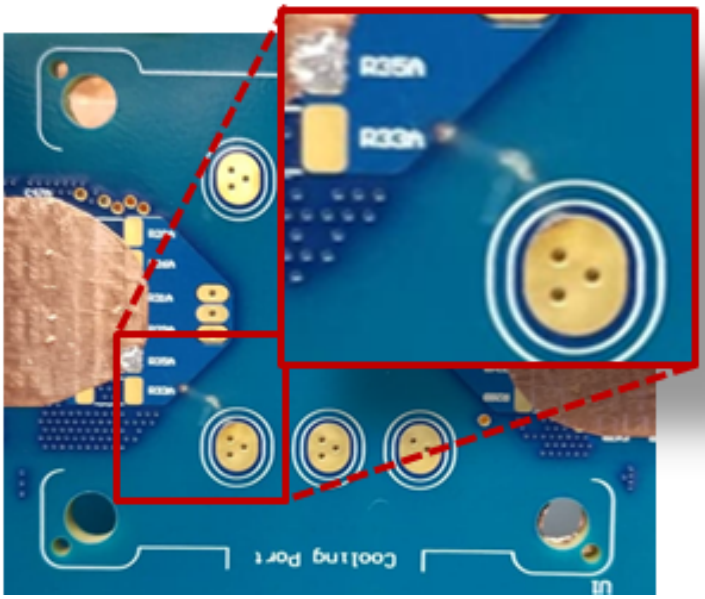


Figure 5.17: Destructive breakdown occurring on the surface of the PCB when PD tested with the PD test module attached. The breakdown occurred between the $+V_{dc}$ and high-side gate pads of the bus bar along critical cross-section 3 (as defined in Figure 5.1 on pg. 71).

Table 5.3: Summary of Partial Discharge Test Results

	w/o PD Test Module					
	Low-Side-On			High-Side-On		
	Method	Result	Voltage (rms)	Method	Result	Voltage (rms)
Numerical	MPD-600	MAX	12.1 kV	MPD-600	MAX	12.3 kV rms
Manual	HFCT	PDIV	9.6 kV	HFCT	PDIV	10.1 kV rms
Improvement	+26 %			+22 %		
	w/ PD Test Module					
Numerical	MPD-600	PDIV	11.6 kV	MPD-600	PDIV	11.6 kV
Manual	HFCT	BD	8.4 kV	HFCT	PDIV	8.6 kV
Improvement	+38 %			+35 %		

**MAX = Maximum voltage tested with no observed PD.
**PDIV = Voltage at which sustained PD greater than 10 pC in magnitude occurred.
**BD = Destructive breakdown observed before PD.

supported a voltage of 11.6 kV rms (16.4 kV peak) over a terminal spacing of 6 mm in air. The Bayesian optimization with weighted POI from Chapter 3 and the characterization data from Chapter 4 were used to streamline the design process and efficiently optimize the geometry. The system was decomposed into critical cross-sections and parameterized accordingly. Field grading characterization data was used to select appropriate field grading structures. Bayesian optimization was used to introduce the housing as an additional field grading measure and optimize its performance in parallel with the embedded field grading.

The system was built and tested experimentally via PD tests. A previous version of the PCB bus bar and module housing were used as a benchmark. PD testing was carried out following IEC 60664 using an Omicron MPD 600 partial discharge measurement and analysis system and a 60 Hz ac source. During the test, the numerically optimized variant demonstrated a 38% performance increase with a PDIV of 11.6 kV rms, as opposed to the manually optimized variant which experienced a destructive breakdown at 8.4 kV rms.

The test results serve as validation that the embedded field grading geometry successfully mitigated the PD risk in the air by improving field uniformity. The limiting factor of the system from an insulation standpoint is now the manufacturing process of the module, as indicated by the PRPD plot, as opposed to the 6 mm terminal spacing of the module and bus bar. In addition to the 38% improvement in PD performance, the applied numerical optimization technique reduced the design cycle to a matter of days, down from several weeks required to manually design the original version.

Given successful demonstration of PCB bus bar and module housing, gate drivers for both the high-side and low-side switch positions, as well as DC link capacitors, were added to the PCB, enabling full control and operation of the module up to its rated voltage using only a single PCB with a footprint of 200 x 167 mm^2 as shown in Figure 5.18. Figure 5.19 shows the bus bar configured for a double-pulse switching test.

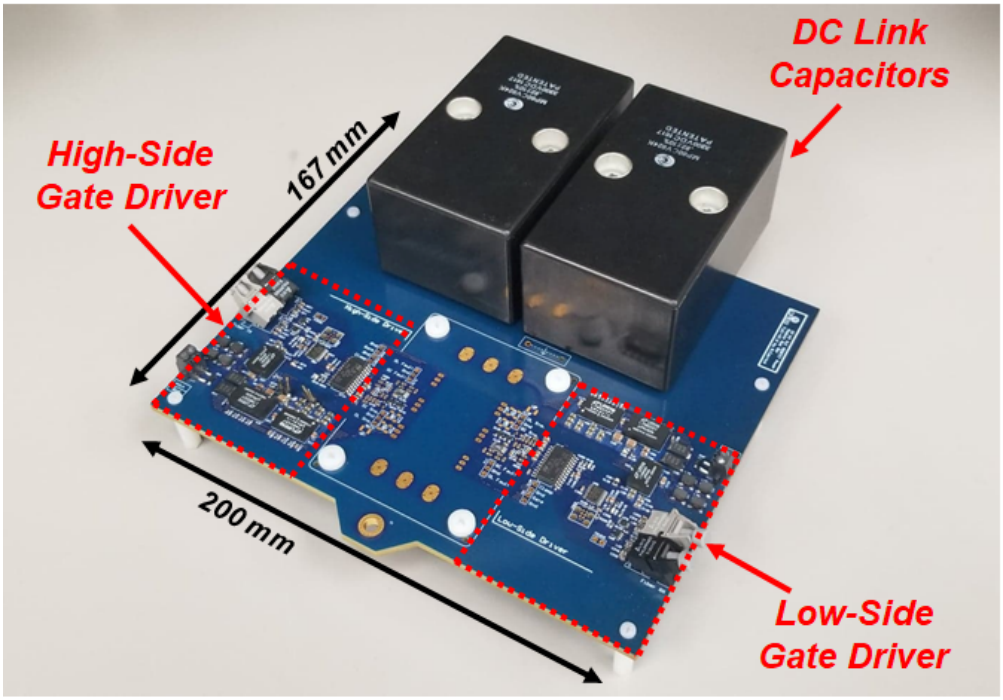


Figure 5.18: High-density PCB bus bar with integrated gate drivers for both the high-side and low-side devices.

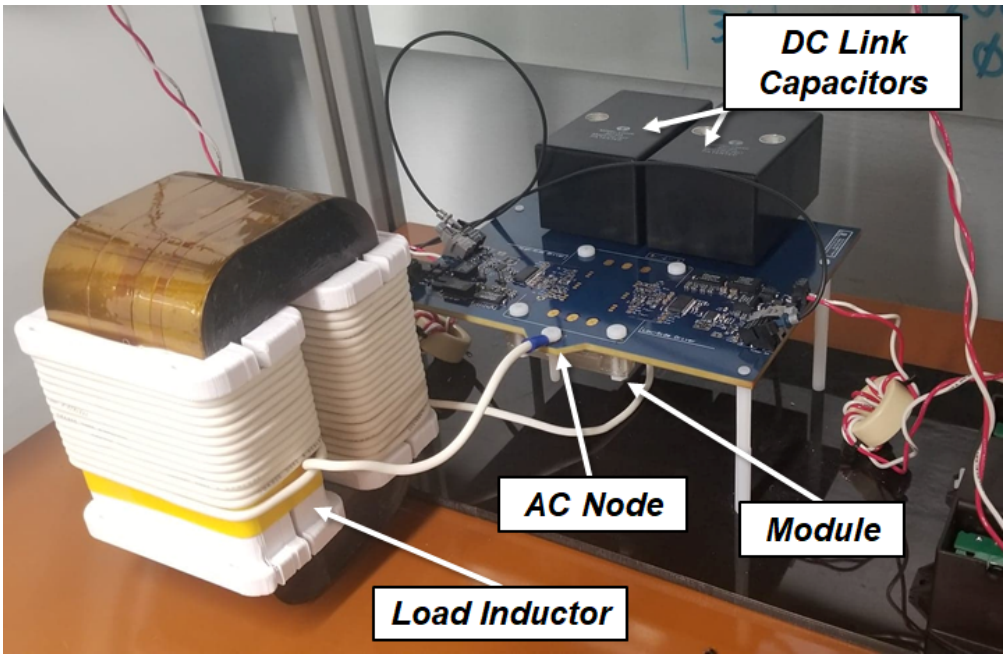


Figure 5.19: PCB Bus bar with bondwire-less module and gate drivers configured for double-pulse switching test.

Chapter 6

Conclusion

6.1 Summary

High-voltage SiC MOSFETs in conjunction with innovative packaging technologies have the potential to revolutionize a broad range of industries. A combination of the higher saturation drift velocity, larger bandgap, improved thermal conductivity, and higher breakdown field strength allows SiC MOSFETs to operate at higher temperatures, with lower conduction losses, faster-switching speeds, and larger blocking voltages making them an attractive alternative to conventional Si active devices. These benefits directly affect power density, allows SiC-based power conversion systems to be smaller, lighter, and more reliable than existing systems. Industry trends such as the electrification of transportation, renewable energy, as well as electric and hybrid-electric ships and planes are all in a position to reap the benefits of improved power density and higher operating voltages.

Currently, high-voltage SiC technology is largely limited by the materials, processes, and paradigms of traditional packaging technologies. Accepted practices such as bondwires, single-sided cooling, copper bus bars, and lateral layout limit both the thermal and electrical performance of SiC technology, voiding its benefits. Many innovative packages have been proposed in the literature to combat these shortcomings, most notably the high-density bondwire-less power module from CPES in 2018.

The module focuses on addressing the fundamental trade-off between high-density and high-voltage, proposing an innovative spring pin termination style and PCB integrated bus bar to enable 10 kV operation while maintaining a power terminal spacing of 6 mm. The system voids the creepage and clearance requirement by fully enclosing the spring pin terminals using the module housing the PCB bus bar. The proximity of the terminals presents a significant partial discharge risk as intense field crowding occurs around the terminals.

To prevent partial discharge, an embedded field grading structure is proposed which utilizes the internal traces of the bus bar as a capacitive grading mechanism to redirect the electric field lines into the FR-4 dielectric and out of the air, where the higher breakdown strength of the material can support the fields without partial discharge. This approach allows for a modular module interface, with no additional sealants or encapsulants, while ensuring safe, reliable operation.

The design of the embedded field grading structures is time-consuming and inefficient. Traditional design techniques for field grading structure rely on an iterative process where the designer manually tunes the performance of the system based on simulation data. The result is a time-consuming design process, with leads to both single-point and sub-optimal designs.

This work proposes a Bayesian optimization procedure and weighted point-of-interest cost function as a means of efficiently characterizing and optimizing complicated field grading structures. The technique relies on lightweight, FEA simulations with coarse meshes to identify and record the field strength at the crowding location. The result is passed to a Bayesian optimization algorithm which constructs a Gaussian process model of the system and then efficiently optimizes the model. The result is a workflow that is easily implemented with commercially available software, scalable to large systems, and immune to the computation error of FEA around singularities.

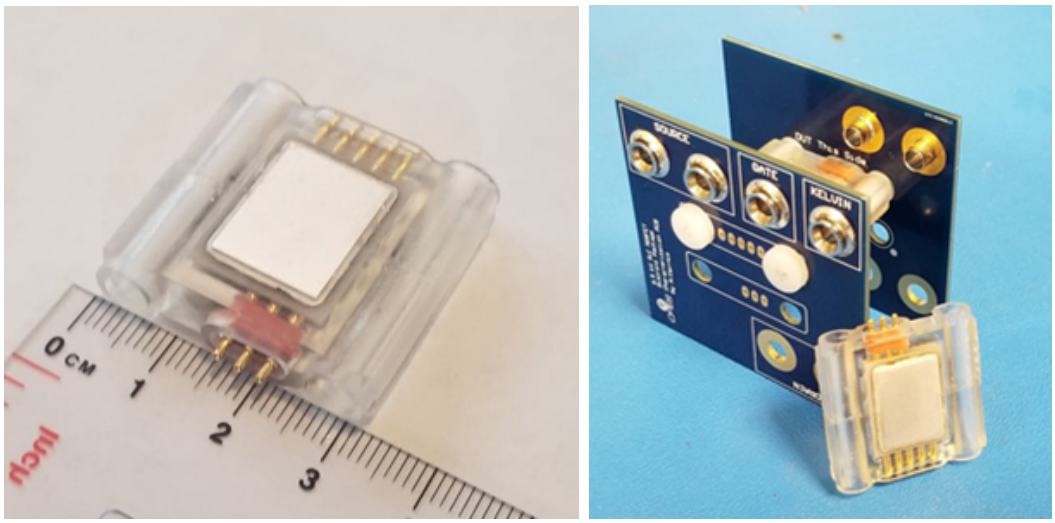
Bayesian optimization is used to characterized the field grading structures to assess the limitations and trade-offs of the structures. Performance metrics are derived and low order polynomial models are generated to further streamline the design process. Both the characterization data and the optimization workflow are used to design and updated PCB integrated bus bar and module housing for the 10 kV bondwire-less SiC module.

The bus bar and housing are assembled and experimentally verified by utilizing partial discharge testing on an IEC 60664 compliant testbed. During testing, the numerically optimized system is benchmarked against the previous version of the bus bar, which was designed exclusively using manual, iterative design. The improved version outperformed the baseline by 38%, demonstrating a partial discharge inception voltage of 11.6 kV rms compared to the 8.4 kV rms capability of the manually optimized version. Upon completion of the experimental verification, gate drivers and DC link capacitors are integrated into the bus bar allowing full control and operation of the module up to 10 kV using a single PCB with a footprint of 200 x 167 mm^2.

In addition to the 38% performance increase, the Bayesian optimization technique enabled a significant reduction in design cycle time, cutting design time from a matter of weeks for the manual version, to a matter of days for the improved version.

6.2 Future Work

An immediate extension of this work is to apply Bayesian optimization and the weighted POI cost function to arbitrary 3D geometry. Figure 6.1 shows an innovative 6.5 kV discrete SiC MOSFET package that was designed in parallel with this work. The package utilizes dual cooling surfaces on either side of the die to reduce the overall junction-to-case thermal resistance as well as an innovative lateral spring-pin termination.



(a) (b)

Figure 6.1: a) Bondwire-less 6.5 kV discrete SiC MOSFET package with double-sided cooling and a lateral spring-pin termination; b) the package mounted between the opposing bus bar PCBs.

Figure 6.2 shows a 2D representation of the lateral spring-pin termination. The spring-pin is soldered to a terminal block made of copper or molybdenum that is silver sintered to the upper and lower substrate. The spring pin passes through the housing and interfaces to a PCB bus bar such as the one designed in this work. A silicone gasket is used to seal between the spring-pin and the module housing, allowing the package to be encapsulated with silicone gel without the encapsulant leaking out of the package.

Challenging geometries arise specifically near the edges of the package where the electric fields are affected by the spring-pin body, the upper and lower substrates, as well as the trace geometry at the corner of the substrates and the copper heat spreader. Figure 6.3 shows a CAD representation of the spring-pin near the edge of the substrate and the critical geometries.

Systems such as that shown in Figure 6.3 are not easily decomposed into 2D cross-sections and parameterized. The tight radii of the spring-pin body and the rounded corners cause

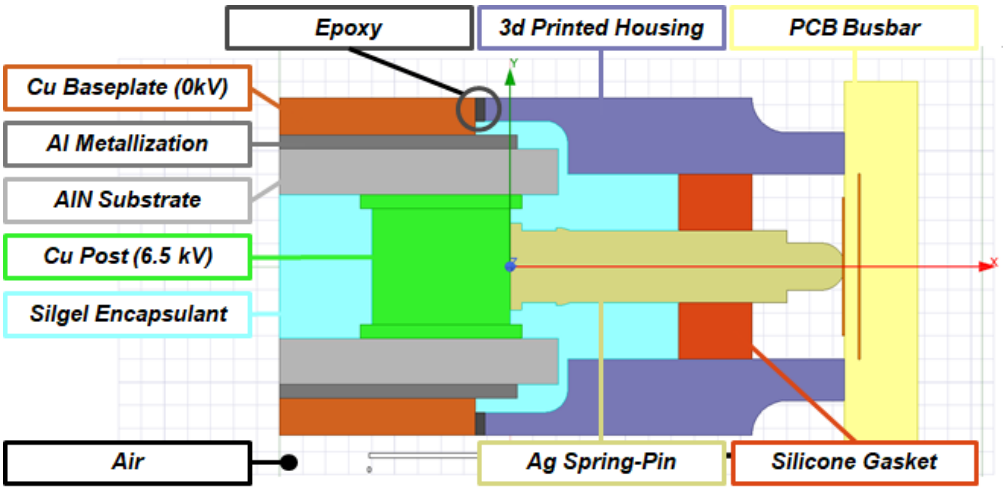


Figure 6.2: Lateral spring-pin termination design showing the spring-pin soldered to the terminal block and interfaced to the PCB bus bar through the housing and silicone gasket.

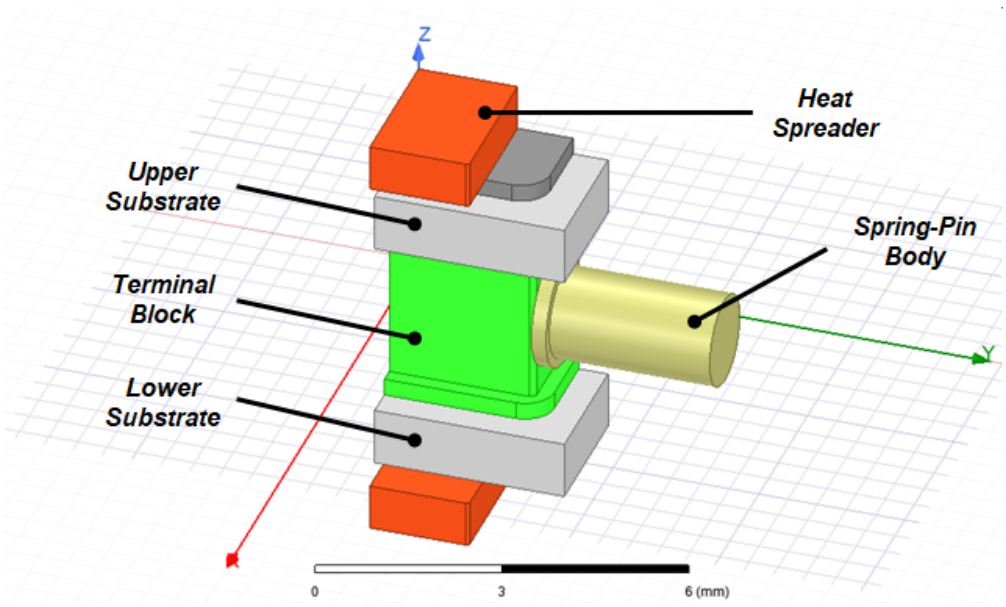


Figure 6.3: 3D design geometry of the lateral spring-pin termination near the edge of the substrate where complicated geometry makes decomposition into 2D structures infeasible.

additional field crowding that can only be captured in 3D.

The largest barrier to achieving automated optimization of arbitrary 3D geometries is the transfer of data between the parametric modeling application and the FEM solver application. A wide range of open-source and commercial software packages are available with comprehensive parametric modeling capabilities, that also allow for scripted automated model generation. Similarly, the options for FEM solvers are plentiful, with many offerings able to simulate a broad range of physics. The challenge lies in linking the applications and enabling a data transfer without discrepancies due to floating point errors.

Many existing design workflows rely on an export/import structure to interface the CAD tool to the FEM tool. This approach comes with significant challenges when utilized with automated design procedures due to small discrepancies in the node and vertex positions stemming from floating point errors. These discrepancies make the automated boundary and mesh assignments challenging due to the ambiguity of the position data. Successful demonstration of electrostatic optimization on arbitrary 3D geometry requires a pipeline that allows for seamless data transfer between the modeling and FEM software, as well as automation from the optimization software.

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