CHAPTER 4: ON-GOING AND FUTURE DEVELOPMENT

Discussion and results presented up to this point were intended to document the past PEBB thermal management effort, while providing a foundation from which future development can be built upon. Several significant design directions are expected to require additional thermal consideration:

4.1 Top Path Thermal Bus

The general layout of multi-chip modules for the PEBB design, as given in Figure 2, restricts access to top path heat removal. If a significant convective environment could be brought to the upper surface, essentially doubling the effective heat transfer area, chip temperatures and failure rates could be lowered further. Several key elements must be addressed before such a system can be successfully implemented, including routing for control and I/O connections, structural connections for possible top and bottom heat transfer paths, and implementation with other electrical devices. (From a modeling perspective, this effort would simply change the top level heat transfer coefficient, h1, within TAMS™ and can be readily implemented.)

Heat removal from the upper surfaces of chips in MCMs has been utilized for quite some time. In particular, IBM has used the thermal conduction module (TCM) over the last 20 years to cool individual chips on mainframe processors with very good results. This system uses an array of spring-loaded pistons to make contact with the upper chip surface. The thermal path leads to chilled cooling water, which fills each piston and is circulated to a separate heat exchanger (Simons, 1995).

More flexible cooling schemes have been devised that permit top path conduction with minimal development. This concept utilizes so-called conformable cold plates to make intimate contact with different size and shape chips through a thin metal sheet. The sheet conforms to the chips with fluid pressure or plungers, and is designed as part of a closed, liquid coolant loop. Results have indicated that heat removal of 100 W per chip can be achieved at operating temperatures 60 °C above ambient (Mansingh and Horine, 1995).

Current development within the NSF Center for Power Electronics Systems (CPES) at Virginia Tech is directed towards the implementation of advanced packaging techniques that will improve the thermal, mechanical, and electrical performance of the PEBB module. This concept, termed MPIPPS (metal posts interconnected parallel plate structure) incorporates direct-bonded copper posts as interconnects between power devices (Haque, et al., 1998). These posts create interior space between adjacent parallel plates (see Figure 34) that can be used as a flow channel for forced air or liquid cooling. Alternately, this space can be filled with a high conductivity solid or dielectric liquid for additional thermal bussing. Preliminary estimates indicate that a dual conductive path PEBB, assuming similar heat transfer on either side, reduces the temperature rise of the device by about 22 %.

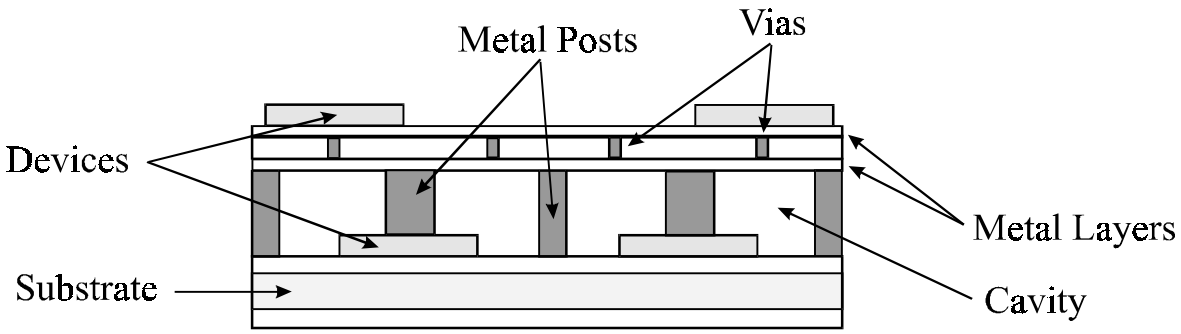

Figure 34: MPIPPS thermal design details

4.2 Metal Matrix Composites (MMC)

Metal matrix composites (MMCs) are finding widespread use in the automotive and aerospace industry where strength, weight, thermal conductivity and thermal expansion are important. They are a composite of an element or alloy metal bound into a 'matrix' structure, formed by a reaction synthesis process. The most common material combinations are aluminum (Al) and silicon carbide (SiC). Because of their composite nature, the properties of MMCs can be tailored to suit the particular application based on the contribution of individual materials. Current applications find them in automotive and aircraft brake rotors, where toughness and dimensional stability at temperature extremes are important.

Applied to electronics cooling applications, the primary advantage of MMCs is the ability to tailor the CTE to match bonded and mating materials, such as copper, braze material, ceramic substrates, and silicon. This reduces interfacial shear stresses that result from relative expansion or contraction, and improves fatigue and failure rate characteristics. For the PEBB design, application of MMCs was explored as a two-step evolution. First, the copper heat spreader from the previous model (Figure 10) would be replaced by a MMC spreader that is CTE matched to that of the braze, eliminating one possible thermal fatigue interface. This model produces slightly higher surface temperatures (about 2 °C) due to the lower k of MMC (210 W/mK) compared to copper. The next step essentially replaces the substrate with MMC, further reducing the mismatches of material CTE (see Figure 35). Application of alumina is accomplished by a thin film technique, and the thick film copper layer is bonded in a manner similar to DBC substrates. Fundamental in this model is the elimination of any thermal grease layer, which significantly reduces the external thermal resistance, h2. Results are indicated in Figure 36, and show a reduction in maximum surface temperature (4.4 °C) compared to the final iteration results for forced convection from Figure 21. This reduction is similar to the improvement from cold plate cooling.

Development of MMCs for use in the PEBB thermal design is quite promising considering the superior thermal and fatigue characteristics. Adaptation of MMCs is seen simply as an evolution

of the current work, requiring little additional thermal development effort. It is expected that future PEBB packaging design will focus heavily on utilizing MMC materials.

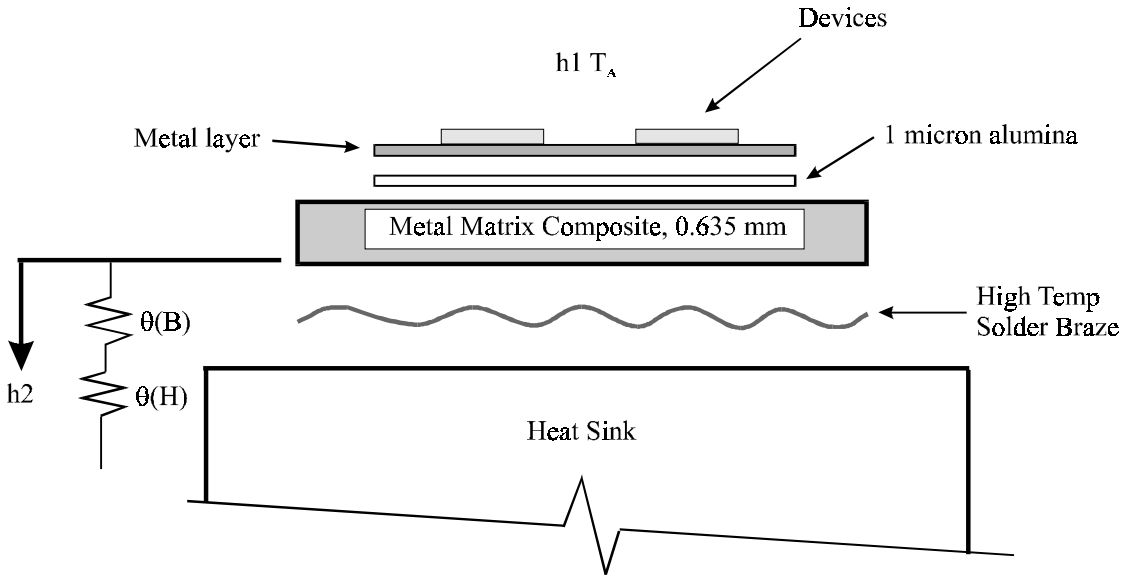

Figure 35: Metal matrix composite thermal model

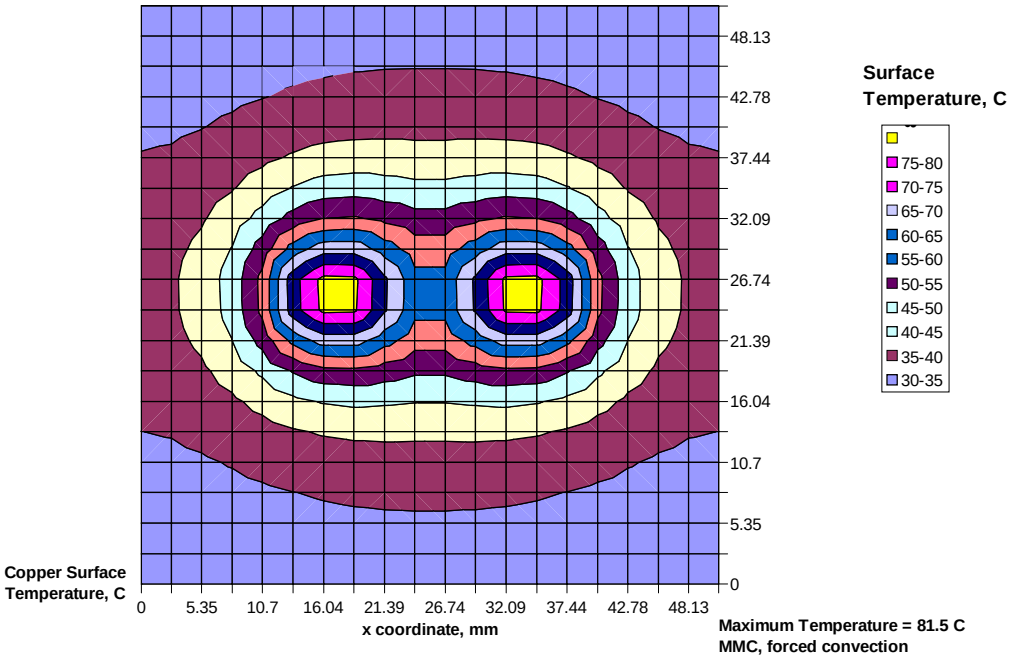

Figure 16: Metal matrix composite thermal map, forced air heat sink

4.3 Multi-Module Integration

Integration of several PEBB modules is, obviously, quite important if they are to be used in a modular fashion. Certainly, a thermal management solution for a single PEBB module will not necessarily suffice for a multi-module application. Close attention must be paid to thermal interactions of adjacent modules while issues such as electrical interactions, noise, and mechanical design must be simultaneously considered. Figure 37 illustrates one very practical, inexpensive solution to a multi-module PEBB. Using a convoluted fin, or other high fin density heat sink, it is possible to integrate three PEBBs onto a single thermal bus and achieve low effective thermal resistances (Cowan, 1995). The results of such an application indicate maximum sink temperatures of approximately 35 °C above ambient while maintaining a very small size. This application of advanced, convoluted fin heat sinks indicates that the capability exists for scaling forced air sinks for multi-module applications.

In higher power applications or severe environments, where ambient temperatures are too high for effective heat transfer with forced air sinks, cold plate cooling is a practical alternative. This allows use of ambient air for heat transfer through a separate heat exchanger that may be remotely located. The high heat capacity of fluids and the use of remote air for heat exchange also results in a locally-compact thermal management solution. Effective heat removal capacities can be readily increased through additional plumbing, cold plates, and coolant pumps.

For military and certain industrial applications, a thermal bus that implements top and / or bottom conductive paths for PEBBs and other heat generating electronics is another possible thermal solution. This system would serve as a common structural rail and have integrated high capacity heat removal media such as embedded single phase coolant loops using standard plumbing or micro-channels, refrigeration lines, heat pipes, pool boiling systems, or even high velocity forced air with internal passages.

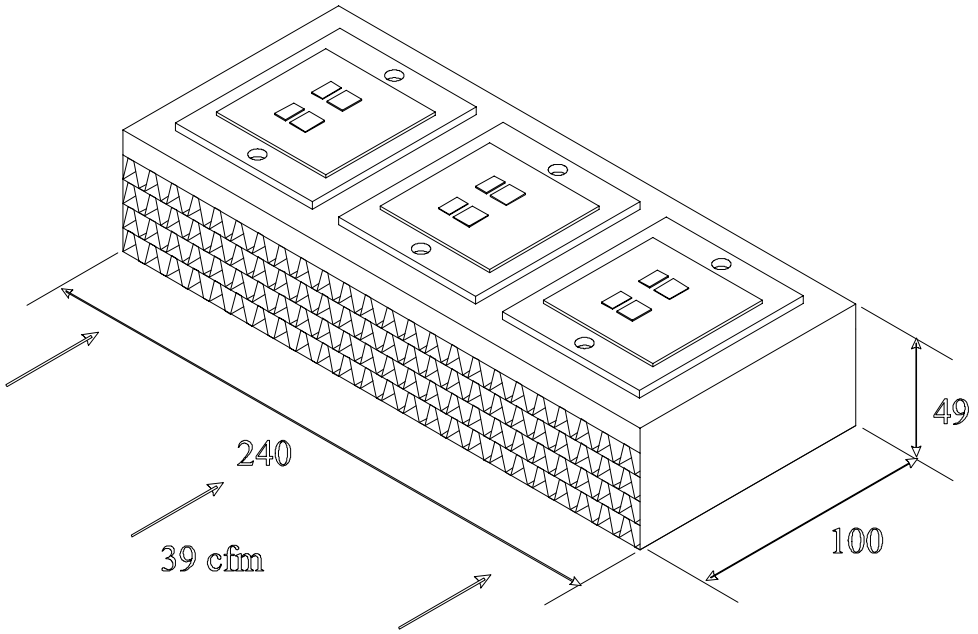

Figure 37: Multi-module solution using forced air, convoluted fin heat sink

CHAPTER 5: CONCLUSIONS AND RECOMMENDATIONS

The on-going effort of development of Power Electronic Building Blocks (PEBB) is a promising "enabling technology" which will promote future electrical power systems. These PEBB devices will have the distinct advantages of low-cost, high reliability, modularity, and scalability that set them apart from current power electronic devices. Key in this development is the thermal characterization and design of the PEBB packaging scheme to manage the high heat dissipation levels. As operating temperatures are closely associated with operating efficiency and device failure rates, thermal management is necessary to ensure proper and reliable device performance.

Current work undertaken by the Mechanical Engineering Department at Virginia Tech, in cooperation with the NSF Center for Power Electronic Systems (CPES) and the Office of Naval Research (ONR), has proposed a preliminary thermal design for the PEBB module. This design effort was inherently similar to other design problems, where numerous variables were optimized within particular constraints. The design direction was not so complicated as to require an application of design of experiments (DOE), but instead lent itself to a concurrent engineering approach for consideration of electrical, thermal and materials issues. This technique enabled separate components of the larger system to be considered simultaneously, but was flexible such that a systematic study could be accomplished and reported.

Many critical *system considerations* were factored into an electronic packaging effort that required close attention across the mechanical, electrical and materials fields. For the PEBB, these elements consisted of such areas as integration requirements, parasitic capacitance, and matched coefficients of thermal expansion. Careful consideration ensured that these elements were properly addressed while meeting the general requirements for the PEBB thermal design. Summarizing these requirements, from section 2.4, with the relevant design variables presented in Chapter 3:

a. Packaging should be kept as small as possible: Substrate and heat sink sizes are optimized for the heat dissipation levels and allowable operating temperatures. Low thermal resistance liquid cooling is offered as an additional compact option.

b. Design should provide for maximum life: Operating temperatures are minimized within the constraints of the design variables. Coefficients of thermal expansion for substrate are used as a design guideline.

c. Costs should be minimized: Lower-cost aluminum nitride substrates and forced air heat sink solutions are proposed as cost effective design solutions. The final design requires little development effort for integration of the thermal management solution.

d. Flexible integration into a number of different environments: Both forced air and cold plate heat sink options offer flexible implementation depending on environment.

e. Scalable with PEBB evolution: Modularity of forced air and cold plate cooling options is discussed.

f. Intrinsically robust: Thicker substrate and copper layers are suggested for durability; heat sink issues are also addressed. Device separation distances affecting parasitic capacitance and device temperatures are recognized as contributing to module performance.

There were several key issues that came out of the design that were considered important to the PEBB thermal management knowledge base. These are:

- Interaction between the substrate spreading resistance, θ_{sp}, and other sources such as external thermal resistance, θ_{h2}, was identified (3.3.1). This is meaningful when considering the balance of the thermal performance of the system. For maximum heat removal in the PEBB design, both substrate and external (including sink) thermal resistance should be minimized.
- An important balance between electrical and thermal concerns came from the lateral spacing of the device pairs on the substrate (3.4.2). For minimum parasitic capacitance, electrical devices should be placed close together. However, this will result in elevated device operating temperatures. After design iterations on substrate geometry, model results indicated that the original device spacing produced peak temperatures that were about 2.5 ° C from optimum. The conclusion was that this difference was small compared to the possible impact on parasitics.
- The effect of substrate thickness on surface temperature was found to be a strong function of substrate thermal conductivity (3.5.1). For low k substrates such as alumina, a less thick substrate is desirable. For materials such as aluminum nitride (AlN), from typical ranges of electronic substrates, an increase in thickness will result in lower surface temperatures for the design conditions (substrate size, power level, etc.). This compares well with the requirements of a thick substrate for mechanical robustness.

Limitations were identified regarding the design effort that should also be addressed. Both are offered as recommendations for possible improvement. First, while the software used (TAMS™) was quite satisfactory for performing preliminary thermal simulations, more involved computer models such as finite element or finite difference are desirable to better characterize the PEBB. These models have fewer restrictions on modeling assumptions and are capable of potentially greater accuracy with node refinement. Other 'engineered' software such as FloTherm™ or certain CFD packages could be equally as accurate. Next, due to the timing of this work, and availability of a suitable prototype, no effort was made to correlate these model results with experimental measurements. Though good experimental comparisons have been made in the past with TAMS™ (Hussein, et al., 1991), the correlation accuracy of the current work cannot be stated with a high level of confidence.

Efforts for future PEBB thermal design are important from a two-tiered perspective. At the most basic level, modeling should support the fundamental direction of the PEBB design such that immediate thermal needs are realized. This would take place on a near-term basis, utilizing proven materials and technologies for design solutions. Such an approach was illustrated in Chapter 3 of this thesis. Longer-term thermal solutions, however, will require more effective

and advanced technologies, as the PEBB power density is scaled to larger, more integrated applications. At this level investigative modeling and research into advanced design and materials will be required to meet these future challenges. An example of this approach is demonstrated in Chapter 4.

APPENDIX A: HEAT SPREADING

Application of the thermal resistance boundary condition can take into account the resistance components that exist from two- and three-dimensional conduction effects. This spreading *resistance* was defined for the PEBB thermal model in section 3.3.1 and is related to the heat spreading.

In general, heat spreading depends on the thermal resistance in the z direction, θ_z, compared to that in the x, θ_x, and y, θ_y, direction from junction to ambient (see Figure 38). Within the heat sink shown, the thermal resistance is proportional to the conduction path distance, and inversely proportional to the cross sectional area through which heat flows. This is seen in Equation 5 from section 3.2.1. For real applications where the thickness, t, and resistive path are not infinitesimally small, this path will spread out into the sink similar to the simplified two-dimensional diagram in Figure 39(a). The conductive path is defined to be the path of least resistance (t') where heat flux spreads out radially to increase the active conduction areas (A'). As more heat diverges from the one-dimensional conductive path, a larger spreading resistance component will result. The effect of device interaction and device to substrate size will influence the spreading by introducing insulated boundary conditions and lines of symmetry.

A convenient means of qualifying the two- and three-dimensional conduction for a model similar to the PEBB relies on comparing the internal resistance of the heat sink to that of the external environment. When the resistance below the sink due to convection is greater than the resistance through the thickness, heat will tend to spread radially where the transfer area is much larger, towards a lower resistance. This is illustrated in Figure 39(b). When the resistance below the sink is smaller than that through the thickness, the spreading is less (Eades and Nelson, 1991). This is seen in Figure 39(c). The ratio of thermal resistance due to conduction through the heat sink to the resistance of convection from the sink to ambient is called the Biot number. Specifically,

$$Bi = \frac{R_{\text{int}}}{R_{ext}} = \frac{R_{cond}}{R_{conv}} = \frac{ht}{k} \qquad (11)$$

A large Biot number represents a heat sink whose convective (or external) boundary has much lower resistance than the conductive (or internal) path. As explained, the heat flux would flow downward to the bottom of the sink with little spreading. For small Biot numbers the external boundary has a much higher thermal resistance than the internal path and the heat flux will flow in a more radial direction. In the PEBB design, the heat spreading was included in the calculations for the substrate and metallization layers within the TAMS models. The associated resistance was calculated assuming that the one- and two- / three-dimensional resistance components add up much like series resistors (Kraus and Bar-Cohen, 1983). For the external heat sink, spreading was assumed to be included in the total external thermal resistance, θ, discussed in section 2.3.

APPENDIX A: HEAT SPREADING

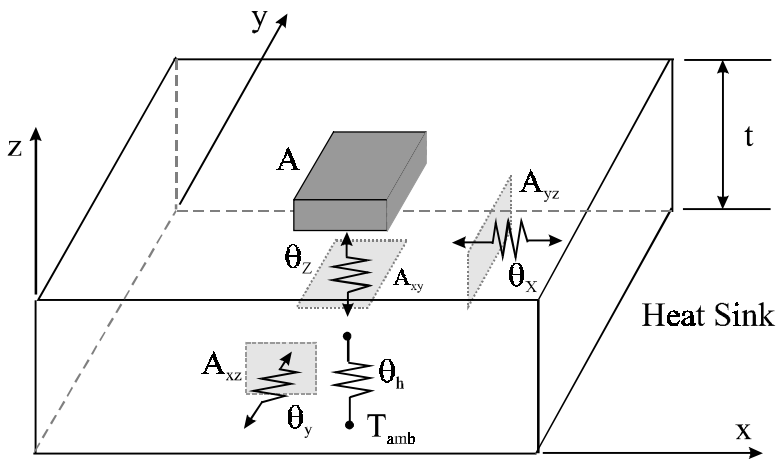

Figure 38: General spreading resistance model

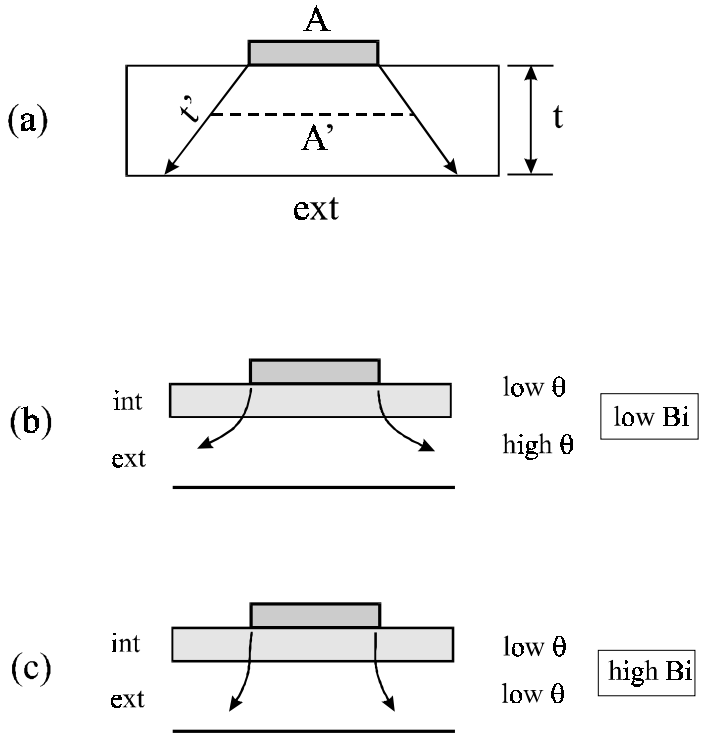

Figure 39: Simplified heat spreading (Biot number)

APPENDIX B: GEOMETRY ITERATION SUMMARY

Iteration	**Matl**	**Conv**	**A** mm	**B** mm	**Area** m^2	**R (trans)** K/W	**h2** W/m^2K	**Tmax*** C
Orig	Alumina	NAT	31.75	31.75	1.0081E-03	0.3058	1386	164.5
		FOR					2445	126.4
		LIQ					2788	119.9
	AlN	NAT					1386	143.9
		FOR					2445	107.1
		LIQ					2788	100.9
It 1	AlN	NAT	36.90	31.75	1.1716E-03	0.2631	1268	128.0
		FOR					2351	92.8
		LIQ					2726	87.0
It 2	AlN	NAT	46.90	31.75	1.4891E-03	0.2070	1088	124.8
		FOR					2187	89.1
		LIQ					2613	83.1
It 3	AlN	NAT	46.90	41.75	1.9581E-03	0.1574	900	123.7
		FOR					1984	87.5
		LIQ					2462	81.2
It 4	AlN	NAT	50.80	44.45	2.2581E-03	0.1365	810	123.2
		FOR					1873	86.7
		LIQ					2375	80.3
It 5	AlN	NAT	50.80	50.80	2.5806E-03	0.1195	732	124.4
		FOR					1766	87.0
		LIQ					2287	80.1
It 6	Alumina	NAT	50.80	50.80	2.5806E-03	0.1195	732	142.0
		FOR					1766	103.1
		LIQ	Centered				2287	95.7
	AlN	NAT	IGBTs				732	122.8
		FOR					1766	85.9
		LIQ					2287	79.1

* matrix surface temperature (may not represent device centers)

APPENDIX C: PRELIMINARY ITERATION DETAILS

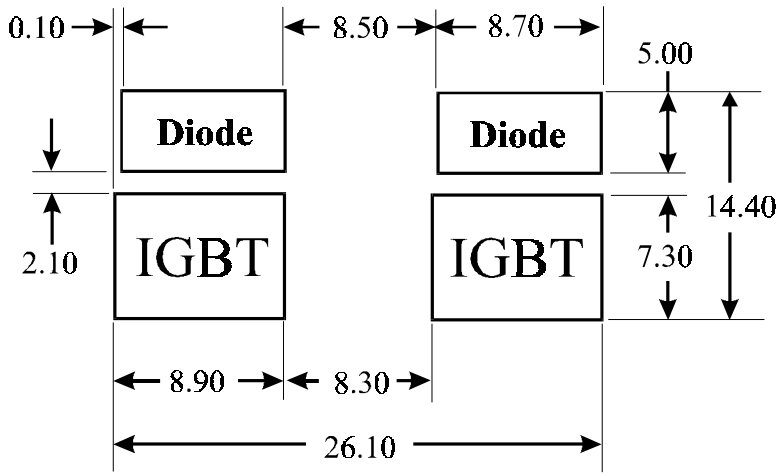

Figure 40: Original design, device spacing detail

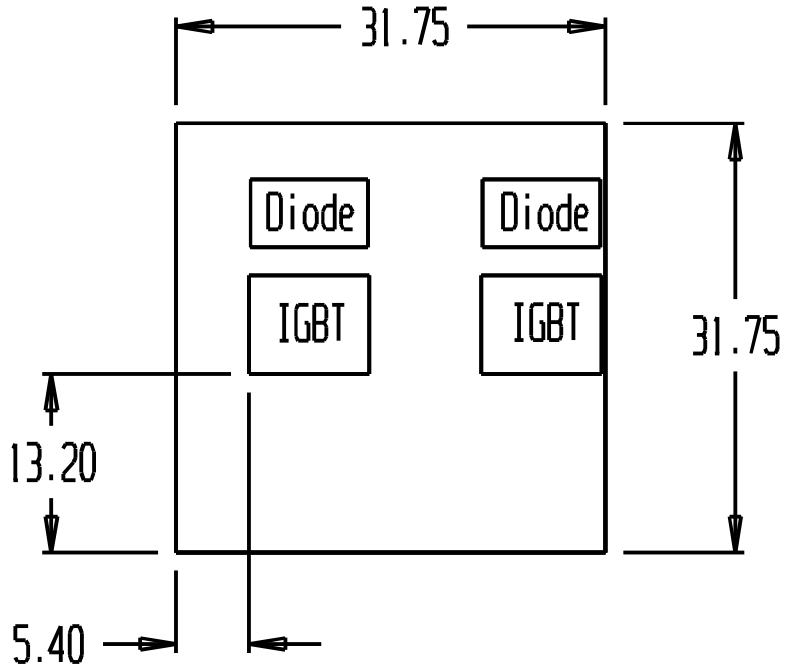

Figure 41: Original design, overall geometry

APPENDIX C: PRELIMINARY ITERATION DETAILS

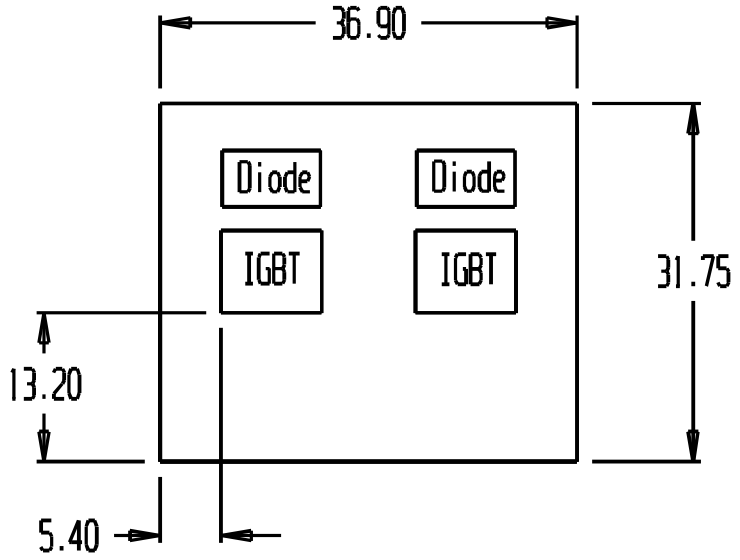

Figure 42: Iteration 1 overall geometry

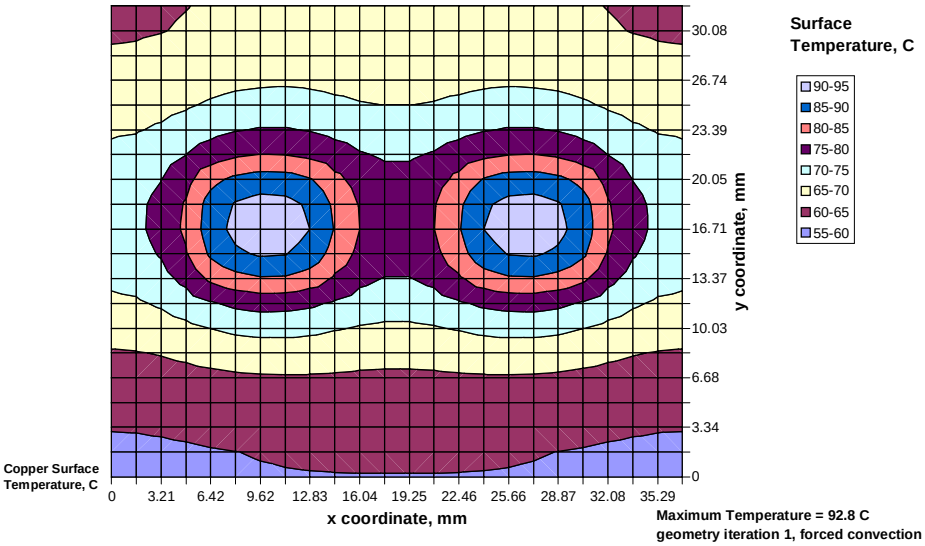

Figure 43: Iteration 1 thermal map, AlN substrate, forced air heat sink

APPENDIX C: PRELIMINARY ITERATION DETAILS

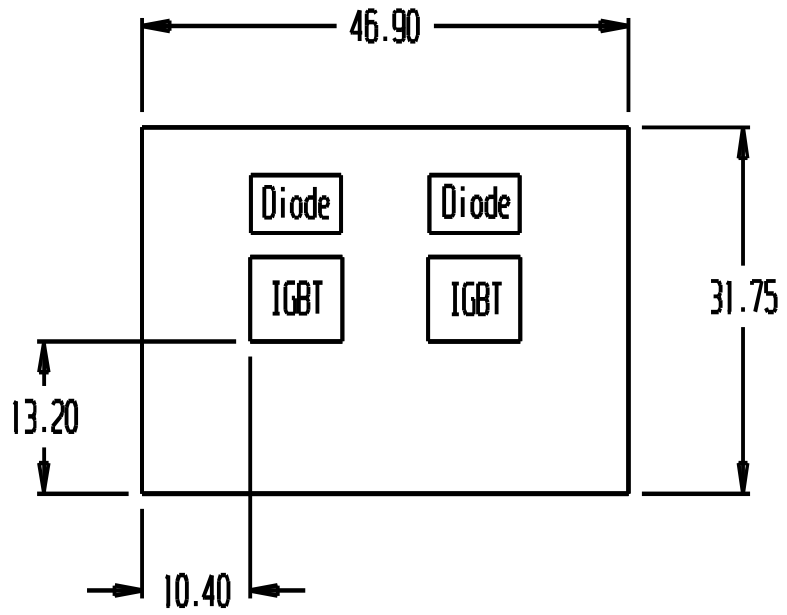

Figure 44: Iteration 2 overall geometry

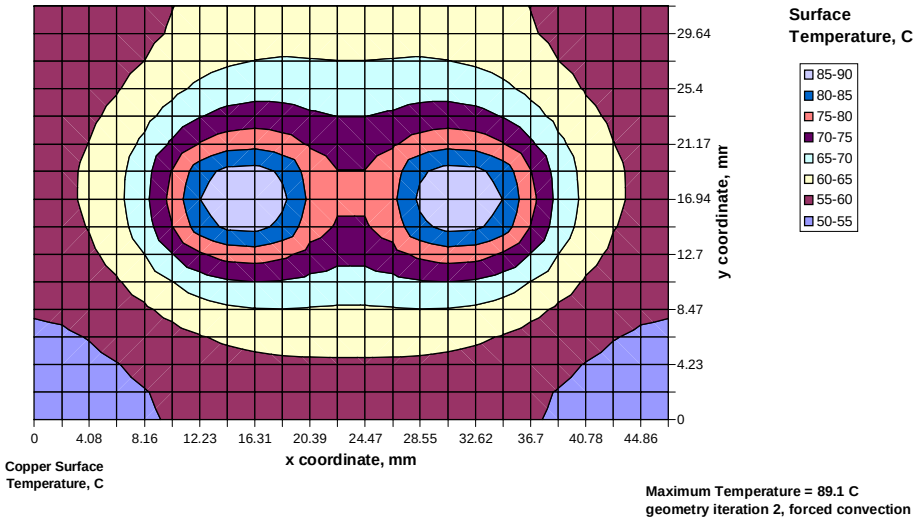

Figure 45: Iteration 2 thermal map, AlN substrate, forced air heat sink

APPENDIX C: PRELIMINARY ITERATION DETAILS

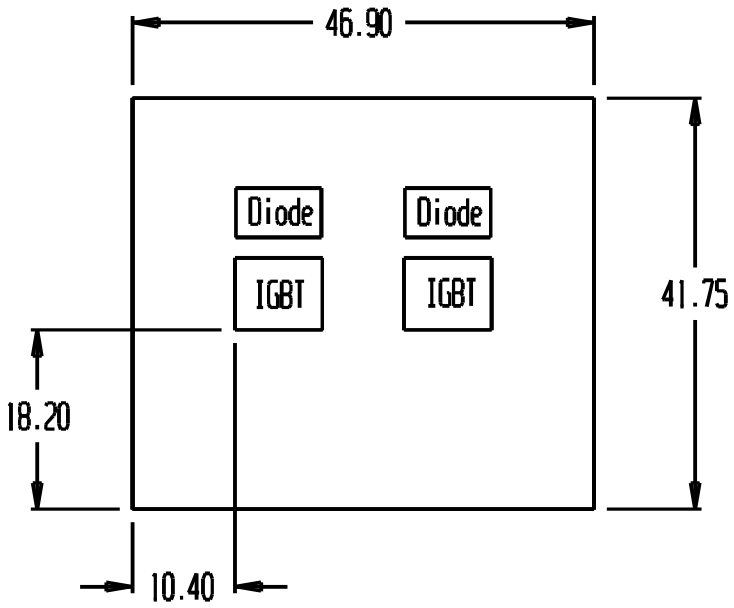

Figure 46: Iteration 3 overall geometry

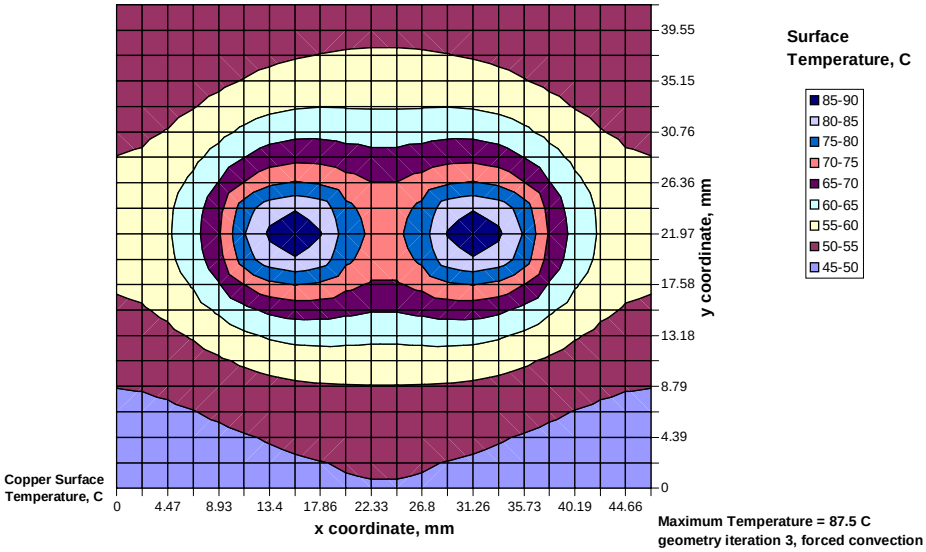

Figure 47: Iteration 3 thermal map, AlN substrate, forced air heat sink

APPENDIX C: PRELIMINARY ITERATION DETAILS

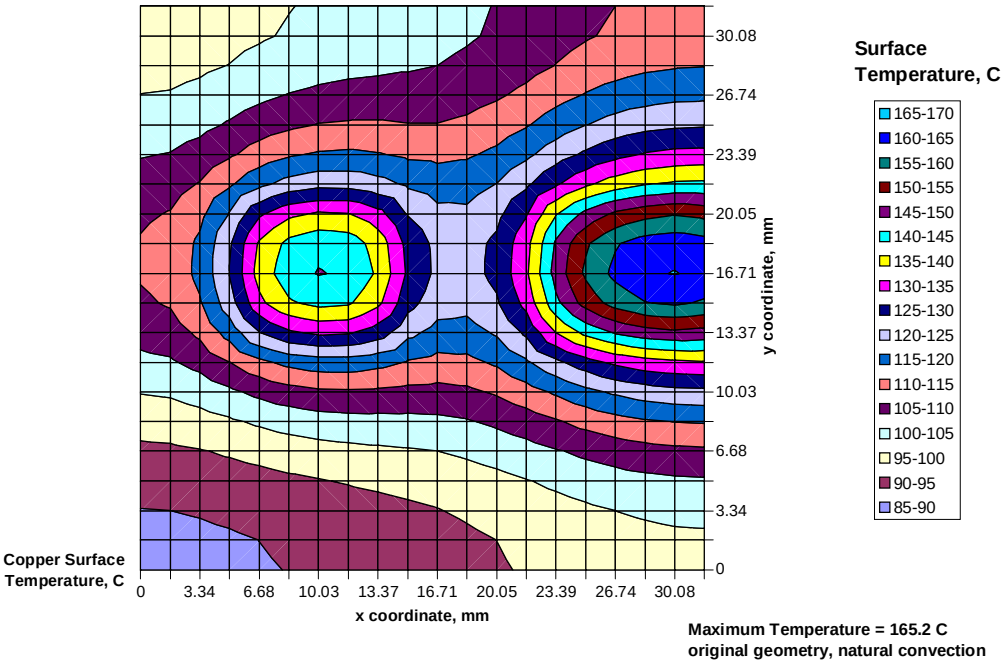

Figure 48: Original geometry thermal map, alumina substrate, natural convection, h1 = 0

APPENDIX D: BASIC CODE

```
'   TAMS-3D.BAS, DATA POST-PROCESSOR FOR TAMS
'   (EXCEL 3-D SURFACE PLOT FORMAT)
'
'   BILL STINNETT
'   LAST EDIT 1-26-99
'
'   This program uses as input the D4OUT file from TAMS, which
'   is typically located in the D:\ETAP subdirectory.  This file
'   should be renamed and placed into a separate directory if
'   multiple simulations are run.  The exact directory location
'   of these files needs to be edited below.
'
      CLS
      CLOSE
      CLEAR
'     max number of total grid points (from TAMS)
      MAXGRID = 491
'     max number of x or y grid points = 50 (change DIM TEMP)
      DIM TEMP(50, 50), XP(MAXGRID), YP(MAXGRID), TP(MAXGRID),
XGRID(MAXGRID), YGRID(MAXGRID)
      PRINT

'
'     *  MODIFY DEFAULT PATH DIRECTORY HERE AND
'     *  LEAVE SPACES INTACT (SHOULD HAVE 30)
'
      DIR$ = "D:\ETAP\                          "

      COLOR 3
      PRINT "PATH FOR DATA FILES SET TO DEFAULT "
      PRINT "---> ("; RTRIM$(DIR$); ")"
      INPUT "TO CHANGE, MODIFY PROGRAM - <CR> TO CONTINUE"; QQQ$
      DIRLEN = LEN(DIR$)
      PRINT
      COLOR 7
      PRINT "Input file name (in dir "; RTRIM$(DIR$);
      INPUT "): "; IN$
      OUT$ = IN$
      INLEN = LEN(IN$)
      MID$(OUT$, INLEN - 2) = "EXC"
      PRINT
      PRINT "Output file name (in dir "; RTRIM$(DIR$); ")"
      PRINT "<CR> for default ("; OUT$; ")"
```

APPENDIX D: BASIC CODE

```
      INPUT OUTPUT$
      IF OUTPUT$ = "" THEN OUTPUT$ = OUT$
      OUTLEN = LEN(OUTPUT$)
      INPATH$ = DIR$
      OUTPATH$ = DIR$
      MID$(INPATH$, DIRLEN - 29) = IN$
      INPATH$ = RTRIM$(INPATH$)
      MID$(OUTPATH$, DIRLEN - 29) = OUTPUT$
      OUTPATH$ = RTRIM$(OUTPATH$)
      PRINT
      OPEN INPATH$ FOR INPUT AS #1
      PRINT "Input:   "; INPATH$; "  opened successfully"
      PRINT
      INPUT "<CR> to continue"; QQQ$

      YNUM = 1
      XP(0) = 0
      TOTAL = 0
'
'     READ IN ALL DATA POINTS INTO 1-D ARRAY
'
      TP(0) = 0
      LASTMAX = 0
      TTEMP = 0
      FOR K = 1 TO MAXGRID
        INPUT #1, XP(K), YP(K), TP(K)
        TTEMP = TTEMP + TP(K)
        ON ERROR GOTO 70

'     FIND MAX TEMP IN ARRAY (which may not represent max
'     surface temp because array points may not coincide with
'     center of sources)
'
        IF TP(K) > TP(K - 1) AND TP(K) > LASTMAX THEN MAXTEMP = TP(K)
        LASTMAX = MAXTEMP

        IF XP(K) < XP(K - 1) THEN YNUM = YNUM + 1
        TOTAL = TOTAL + 1
      NEXT K

70    XNUM = TOTAL / YNUM
      AVGTEMP = TTEMP / K
      XDELTA = XP(2) - XP(1)
```

APPENDIX D: BASIC CODE

```
      YDELTA = YP(2 * XNUM) - YP(XNUM)
      PRINT

      PRINT "MAX TEMP:  "; LASTMAX
      PRINT "AVG TEMP:   "; USING "###.#"; AVGTEMP
      PRINT "XGRID:  "; XNUM
      PRINT "YGRID:  "; YNUM
      PRINT "# of data points:  "; TOTAL
'
'     FIND X AND Y VALUES
'
      FOR M = 1 TO XNUM
        XGRID(M) = XDELTA * (M - 1)
      NEXT M
      FOR N = 1 TO YNUM
        YGRID(N) = YDELTA * (N - 1)
      NEXT N
'
'     BREAK TEMP DATA INTO 2-D ARRAY
'
      NUM = 0
      FOR N = 1 TO YNUM
      FOR M = 1 TO XNUM
        NUM = NUM + 1
        TEMP(M, N) = TP(NUM)
      NEXT M
      NEXT N
'
'     WRITE X, Y, TEMP DATA TO OUTPUT FILE
'     (X POSITIVE TO RIGHT, Y POSITIVE DOWN)
'
      PRINT
      OPEN OUTPATH$ FOR OUTPUT AS #2
      PRINT "Opening output file...."
'
'     PRINTS X VALUES ACROSS TOP ROW
'
        PRINT #2, ",";
      FOR M = 1 TO (XNUM - 1)
        PRINT #2, USING "###.##,"; XGRID(M) * 1000;
      NEXT M
        PRINT #2, USING "###.##,"; XGRID(XNUM) * 1000
'
```

APPENDIX D: BASIC CODE

```
'       PRINTS Y VALUE AND TEMPS ON EACH LINE BELOW
'
        FOR N = 1 TO YNUM
          PRINT #2, USING "###.##,"; YGRID(N) * 1000;
        FOR M = 1 TO (XNUM - 1)
          PRINT #2, USING "###.###,"; TEMP(M, N);
        NEXT M
          PRINT #2, USING "###.###,"; TEMP(XNUM, N)
        NEXT N
        PRINT
        PRINT "Output:  "; OUTPATH$; "  written successfully"
        ERASE TEMP, XP, YP, TP, XGRID, YGRID
        END
```

APPENDIX E: MATERIAL PROPERTIES (Weast, 1987; Incropera and DeWitt, 1990)

Property	units	Alumina Al_2O_3 99.5%	Aluminum Nitride AlN	Beryllia BeO 99.5%	Diamond	Quartz	Sapphire	Silicon	Silicon Carbide SiC	Zirconia	Copper, pure
Density	g/cm^3	3.8-3.9	3.19-3.25	2.86	3.52	2.2	3.97	2.33	3.08-3.2	5.79-6.05	8.91
Young's Modulus	MPa	310-379	428	340-400	1220	80	760-1035	200	462	900-980	117
Hardness	GPa	13.8-17.6	10.4-11.7	-	98	11.5-13.5	18.5-21.5	11.3	23.5-24.5	11.0-12.7	24.5
Linear Thermal Expansion	$x10^{-6}/°C$	8.0-9.4	4.6-5.7	8.4-9.0	1.1	0.55	7.9-8.8	2.3-2.6	4.0-4.5	9.2-10.3	17
Thermal Conductivity	W/mK	25.1-35.6	100-260	200-260	1000-2000	1.4	40	125	75-155	2.2-3.8	400
Thermal Shock Resistance	ΔT (°C)	200	400	-	>1,000	100	200	-	350-500	280-360	-
Max. Use Temperature	°C	1600-1750	1600	-	2500+	1200	2000	1350	1400	2400	1000
Dielectric Constant		9.6-10.2	8.0-9.0	6.9	5.7	3.75	9.3-11.5	11.7	4.0	5.3-9.2	-

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VITA

William (Bill) Stinnett was born on April 30, 1969 in South Charleston, WV to Harold and Gretchen Stinnett. After a short time in WV, his family moved to a Chesterton, Indiana where they settled into a comfortable small-town environment. Upon graduation from high school in 1987, he gained early admission to Purdue University, and entered as a burgeoning mechanical engineer. Two years later, in late 1989, he left Indiana, and his schoolwork behind, to follow his family to Roanoke, VA. After a year or so working for Grove Worldwide in Salem, VA he went back to school full time in 1991 and completed his Associate in Science degree at Virginia Western Community College, in Roanoke, VA – graduating magna cum laude. In the fall of 1992, he transferred to Virginia Tech and finished the mechanical engineering degree he started, graduating magna cum laude as well in August of 1994. He continued on to graduate school, and entered the Master's program in mechanical engineering during the fall of 1994. Here he was able to further develop a student involvement project he helped start, as a graduate assistant for the Hybrid Electric Vehicle Team. The next year was spent designing and building a car with a group of enthusiastic team members and a supportive faculty advisor. In June of 1995, the team attended the HEV Challenge at the Chrysler Corporate Research Center in Auburn Hills, MI.

During the summer and fall of 1995, Bill worked on the PEBB design project in collaboration with the Virginia Power Electronics Center within the Bradley Department of Electrical Engineering. The details of that project are discussed within this thesis.

In early 1996 Bill accepted a position in Akron, OH with The Goodyear Tire and Rubber Company as a development engineer in the tire-vehicle engineering technology department. After two-and-a-half enjoyable years there he took a leave of absence and returned to Virginia Tech to work as a research associate and finish his thesis. He will return to Goodyear in February 1999, where he will work on analytical and experimental vehicle dynamics.