Packaging of Enhancement-Mode Gallium Nitride High-Electron-Mobility Transistors for High Power Density Applications

Shengchang Lu

Dissertation submitted to the faculty of
the Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
In
Electrical Engineering

Guo-Quan Lu
Khai D.T. Ngo
Louis Guido
Qiang Li
Yuhao Zhang

May 04, 2022
Blacksburg, Virginia

Keywords: Power electronics packaging, gallium nitride high-electron-mobility transistors, parasitic inductance, junction-to-case thermal resistance, high-temperature encapsulation materials, reliability.

© 2022, Shengchang Lu

Packaging of Enhancement-Mode Gallium Nitride High-Electron-Mobility Transistors for High Power Density Applications

Shengchang Lu

ABSTRACT

Gallium nitride (GaN) high-electron-mobility transistors (HEMTs) are favored for their smaller specific on-resistance, lower switching losses, and higher theoretical temperature limits as compared to traditional silicon (Si) power switches. They have the potential to dramatically increase the power density and efficiency of power electronics systems by replacing traditional Si-based switches.

However, GaN HEMTs have a faster switching speed compared to their Si-based counterparts. Minimizing the parasitic loop inductances of the GaN HEMT package is crucial for reducing electromagnetic interference (EMI) noise and voltage spikes. Another concern with GaN HEMTs comes from their lower thermal conductivity and smaller die size. The HEMTs generally have a higher heat flux density, and accordingly, demand better heat dissipation. Thus, innovations are needed for making GaN HEMT packages with low parasitic inductances and higher thermal performances to further their applications in high-frequency, high-power-density converters.

To reduce loop inductance, other researchers have embedded GaN HEMTs in a printed circuit board (PCB) and used plated vias for interconnections and heat dissipation. However, this approach requires more complex manufacturing steps and has lower thermal performance.

This dissertation introduces different embedded packaging techniques for 650V, 150A GaN HEMTs; this method involves interconnecting the bare chips between direct-bonded copper (DBC) and a PCB or between two DBCs, as discussed in Chapter 2. Vertical interconnections by gold pins and silver rods are introduced and implemented in embedded packages to limit the parasitic loop inductance within 1.5 nH and parasitic resistances within 1.5 mΩ.

The thermal performance of the embedded GaN HEMT packages is experimentally verified in Chapter 2; then, the junction-to-case thermal resistance (R_{thJC}) measurement is discussed in Chapter 3. The common temperature-sensitive electrical parameters (TSEPs) of a GaN HEMT for junction temperature measurement lack sufficient sensitivity or stability due to the electron-trapping effect. The non-uniform distribution of the case temperature and a large temperature gradient between the case and heatsink also make it difficult to accurately measure the case temperature. In Chapter 3, gate-to-gate resistance (R_{g2g}) is selected as the TSEP for junction temperature measurement. The stacked thermal interface material (TIM) technique was used to reduce errors in case temperature measurement. This technique was implemented in a custom GaN HEMT package and in embedded GaN HEMT packages for measuring junction-to-case thermal resistance. The discrepancy between measurement and simulation is less than 20%, and the junction-to-case thermal resistance for embedded packages is within 0.1 ^{o}C/W.

Chapter 4 evaluates the reliability of the GaN HEMT embedded packages developed in Chapter 2 by utilizing a power cycling test. Monitoring the junction temperature of the embedded packages online is challenging during the power cycling test. Other approaches have used the on-resistance as the TSEP in order to monitor junction temperature for GaN

HEMTs but this is not accurate due to electron trapping. As discussed in Chapter 3, R_{g2g} is chosen as the TSEP to monitor the junction temperature without worrying about the influence of electron trapping, and this approach cycles the embedded packages at 75 A from 25°C to 125°C. The packages can endure 23,000 power cycles before failure.

This work is the first to develop, fabricate, and characterize embedded packages for 650V, 150A GaN HEMT bare chips. These embedded packages with high-power-rated GaN HEMT bare dice provide an opportunity to reduce the number of paralleled power switches, reduce the system's cooling size, and increase the system’s power density. In addition, this work is the first to develop the junction-to-case thermal resistance measurement technique by gate-to-gate electrical resistance and stacked-TIM for GaN HEMT packages. The technique helps enable solid thermal design for power electronics systems.

Packaging of Enhancement-Mode Gallium Nitride High-Electron-Mobility Transistors for High Power Density Applications

Shengchang Lu

GENERAL AUDIENCE ABSTRACT

Power switches are everywhere in our daily life. They are the fundamental elements in power converters for converting power to electric vehicles. As global power demand for these applications continues to increase, high levels of both efficiency and power density are crucial for power switches. However, traditional silicon-based switches are already very mature, and their properties are very close to their theoretical limits. For further improvement, researchers have tried to replace traditional Si switches with wide-bandgap switches, which have much higher theoretical limits. Gallium nitride high-electron-mobility transistors (GaN HEMTs) are one of the candidates.

However, packaging these switches (GaN HEMTs) is challenging due to their initial properties. They naturally switch very quickly and have smaller sizes compared to traditional Si-based switches. The fast switching speed brings high *dv*/*dt* and *di*/*dt* during the switching period. It causes voltage spikes and electromagnetic interference (EMI) issues. And the smaller size contributes to higher heat flux density, thus requiring more efficient heat dissipation. To solve the challenge of packaging GaN HEMTs, this dissertation has developed embedded packaging techniques to achieve quiet switching and good heat dissipation. These packaging techniques enable GaN HEMTs' advantages and increase the power density and efficiency of power electronics systems.

To experimentally verify the thermal performance of the embedded packages developed a junction-to-case thermal resistance measurement technique was introduced. The thermal resistance of a custom GaN HEMT package was measured, as were those of the embedded packages CPES also developed. The simulation results and the experimental results are close to each other.

Finally, to further evaluate whether or not the newly developed embedded packages are reliable, power cycling tests were carried out at I = 75 A. The packages survived over 23,000 cycles before failure.

Acknowledgments

This work is supported by the Center for Power Electronics Systems (CPES) High-Density Integration (HDI) consortium at Virginia Tech. I also thank the Bradley Department of Electrical and Computer Engineering (ECE), Materials Science and Engineering (MSE) at Virginia Tech and the Vehicle Technology Office of the Department of Energy (DOE) for funding my research during the Ph.D. study.

I am very grateful to my advisor, Dr. Guo-Quan Lu, who has guided not only my research topic but also my attitude towards my life. He has been so patient in facilitating my research and encouraging me when I encountered difficulties. He helps me improve my oral presentation and writing skills. I hope I can always learn something from his clear mind and positive attitude towards obstacles.

I also thank my committee members, Dr. Khai D. T. Ngo, Dr. Louis Guido, Dr. Qiang Li, and Dr. Yuhao Zhang for their valuable suggestions and comments on my research. I also appreciate the help given by Dr. Rolando Burgos, Dr. Christina DiMarino, and Dr. Cyril Buttay during my research.

It has been a great pleasure to work with many fantastic colleagues in CPES, the ECE department, and the MSE department. I thank Dr. Yi Yan, Dr. Shan Gao, Ms. Weizhen Sun, Dr. Lanbing Liu, Dr. Chao Ding, Mr. Zichen Zhang, Dr. Ting Ge, Dr. Han Cui, Dr. Lujie Zhang, Dr. Junjie Feng, Dr. Yue Xu, Mr. Boyan Wang, Mr. Ruizhe Zhang, Mrs. Yingying Gui, Dr. Jiewen Hu, Mr. Cong Tu, Mr. Bo Li, Ms. Tianyu Zhao, and Dr. Joseph Kazak for their help and friendship. There are more names not listed here but many thanks to you all.

My thanks go to the CPES staff: Mr. David Gilham, Ms. Teresa Rose, Ms. Teresa Shaw, Ms. Marianne Hawthorne, Ms. Linda Long, Ms. Lauren Shutt, Ms. Na Ren, Ms. Yan Sun, Mr. Dennis Grove, Mr. Matthew Scanland, Ms. Audri Cunninghan and Ms. Brandy Grim for their support and help over the past six years.

Finally, I would like to give my sincere gratitude to my parents Guoqing Lu and Meilan Yan, and to my girlfriend Yaxuan Zhang for emotional support during my Ph.D. study.

Table of Contents

Chapter 1 Introduction **16**

1.1 Power Module Requirements in Electric Vehicles 16

1.2 Introduction of GaN HEMTs 19

1.3 Challenges for Packaging and Characterizing GaN HEMTs 23

1.4 The State-of-the-Art Packaging Techniques for GaN HEMTs 27

1.5 Significance and Objectives 30

1.6 Summary of Dissertation Organization 31

Chapter 2 Embedded Packaging of eGaN HEMTs: Design, Simulation, Fabrication, and Electrical Characterization **33**

2.1 Introduction of Embedded Packaging Techniques for eGaN HEMTs 33

2.2 GaN HEMT Bare Chip for Packaging 35

2.3 Embedded Packaging for a Single GaN HEMT Chip: PCB-Interposer-on-DBC Packaging 37

2.4 Embedded Packaging of GaN HEMT Half-Bridge Module 45

2.4.1 Single-Sided Cooling GaN HEMT Module 45

2.4.2 Double-Sided Cooling GaN HEMT Module 60

2.5 Chapter Summary 70

Chapter 3 Junction-to-Case Thermal Resistance Measurement of the Embedded Packages **71**

3.1 Introduction of the R_{thJC} Measurement for GaN HEMTs 71

3.2 R_{thJC} Measurement Methodologies 72

3.2.1 Junction Temperature Determination 72

3.3 R_{thJC} Measurement of GaN HEMT Packages 78

3.3.1 A Custom Wire-Bonding GaN HEMT Package 78

3.3.2 R_{thJC} Measurement of the Single-Sided Cooling GaN HEMT Package 82

3.3.3 R_{thJC} Measurement of the Double-Sided Cooling GaN HEMT Package 86

3.4 Summary 89

Chapter 4 Reliability Evaluation of the Embedded Packages **90**

4.1 Introduction of Reliability Evaluation of GaN HEMT Packages 90

4.2 Design of GaN HEMT Power Cycling Test 91

4.2.1 Test Circuit Diagram and LabVIEW Control Program Design 91

4.2.2 Power Cycling Sample Preparation, PCB Test Board Design, and Assembly 96

4.3 Power Cycling Test 98

4.4 Summary 102
Chapter 5 Conclusion and Future Work 103
5.1 Conclusion 103
5.1.1 Embedded Package Development for GaN HEMTs 103
5.1.2 Junction-to-Case Thermal Resistance Measurement and Reliability Assessment 104
5.2 Future Work 105
Appendix A: Packaging and Characterization of GaN HEMTs for High-Temperature Applications 106
A.1 Introduction of High-Temperature Packaging and Characterization of GaN HEMTs 106
A.2 High-Temperature GaN HEMT Package Design and Fabrication 106
A.2.1 Wire-Bonding GaN HEMT Package With a Nitrogen Atmosphere 106
A.2.2 Surface-Mounted GaN HEMT Package With Silver Rod Interposers 109
A.3 High-Temperature Characterization of GaN HEMT Packages 112
A.3.1 High-Temperature Static Characterization 112
A.3.2 High-Temperature Dynamic Characterization 116
A.4 Summary 119
References 121

List of Figures

Fig.1-1. 2019 U.S. greenhouse gas emissions distribution [5]. 16
Fig.1-2. Components of the generic electric traction drive system [7]. 17
Fig.1-3. The specific on-resistance versus breakdown voltage for different semiconductor materials. [8]. 20
Fig.1-4. Summary of Si, SiC, and GaN relevant material properties [9]. 20
Fig.1-5. Traditional GaN HEMT device structure. 21
Fig.1-6. GaN HEMT cascode device structure [10]. 22
Fig.1-7. The typical structure of an E-mode GaN HEMT [21]. 22
Fig.1-8. A typical buck converter circuit diagram with parasitic inductances. 24
Fig.1-9. The typical cooling structure of a GaN HEMT package (without interconnections). 25
Fig.1-10. Safe operation area plot for Si, SiC, and GaN devices. 25
Fig.1-11. (a) The dual small outline (DSO) package from Infineon [28], and (b) the Quad flat no-lead (QFN) package from Texas Instruments [29]. 27
Fig.1-12. A structure of PCB-embedded packaging of GaN HEMT [32]. 29
Fig.1-13. (a) Stud bump interconnection of power switch packaging [33], and (b) metal foam interconnection of power switch packaging [34]. 29
Fig.1-14. The structure of an insulated metal substrate (IMS) based GaN HEMT power module [36]. 29
Fig.1-15. (a) A PCB/DBC hybrid GaN HEMT packaging structure [37], and (b) a DBC/DBC sandwich GaN HEMT packaging structure [39]. 30
Fig.1-16. Comparison of the state-of-the-art GaN HEMT packages [21, 28, 29, 32, 37, 38]. 30

Fig. 2-1. An example of a wire-bonding package with lateral interconnection. 33
Fig. 2-2. An example of an embedded package with vertical interconnection. 34
Fig. 2-3. The overview of the 650 V, 150 A GaN HEMT bare die. 36
Fig. 2-4. The surface finish of the bare die in Fig. 2-3. 36
Fig. 2-5. The cross-sectional view of the embedded package for the single GaN HEMT in Fig. 2-3. 37
Fig. 2-6. The fabricated embedded package discussed in Fig. 2-5. 38
Fig. 2-7. Circuit diagram of the single chip GaN HEMT package in Fig. 2-5 with parasitic inductances labeled. 38
Fig. 2-8. Schematic of the structure model of a package based on: (a) the GaN Systems's GaNPX technology; (b) a typical PCB-embedded package; and (c) the PCB-interposer-on-DBC package in this work. In Fig. 2-8(c), Both TIM 1 and TIM 2 can be high-thermal-conductivity solder or sintered silver. However, in Fig. 2-8(a) and (b), the TIM must provide insulation. Hence, they have a low thermal conductivity. 40
Fig. 2-9. Results of the simulated steady-state temperature profile over die surface of: (a) Fig. 2-8. (a); (b) Fig. 2-8. (b); and (c) Fig. 2-8. (c). The heating power was set to be 20 W. Air cooling with 3 m/s was applied to all the three structures. 41

Fig. 2-10. The fabrication process of the PCB-interposer-on-DBC package in Fig. 2-6. The alignment blocks and the die were fixed by a PCB fixture and sintered on an etched DBC. The functional PCB was guided by the alignment blocks and aligns the pins to the die's bonding pads. 42
Fig. 2-11. PCB-interposer-on-DBC package after trimming off the alignment region and testing pads of the package in Fig. 2-6. 42
Fig. 2-12. (a) Measured R_{on} of the bare die in Fig. 2-3 and the package in Fig. 2-6; and (b) measured leakage current of the bare die in Fig. 2-3 and the package in Fig. 2-6. For R_{on} measurement, V_{GS} is set to be +6 V to fully turn on the switch. For leakage current measurement, V_{GS} is set to be -4 V to make sure the switch is off. The measurement error is within 1 μΩ. 43
Fig. 2-13. (a) Measured I_D vs. V_{DS} of the package in Fig. 2-6; and (b) measured I_D vs. V_{GS} of the package in Fig. 2-6. 44
Fig. 2-14. (a) Three-dimensional view of the single-sided cooling half-bridge module; and (b) exploded view of the module. 46
Fig. 2-15. A cross-sectional diagram of the single-sided cooling half-bridge module in Fig. 2-14. 46
Fig. 2-16. Circuit diagram of the half-bridge module from Fig. 2-14 including parasitic inductances. 47
Fig. 2-17. Parasitic inductances depicted in Fig. 2-16 of the module in Fig. 2-14. Gate pin inductance is not shown here. 48
Fig. 2-18. (a) Simulated structure for the half-bridge module package in Fig.1; (b) simulated structure for a half-bridge module made with GaN System's GaN_{PX} package; and (c) simulated structure for a PCB-embedded GaN half-bridge module. In Fig. 2-18(a), both solder and sintered silver have high thermal conductivity. However, in Fig. 2-18(b) and (c), the TIM must provide insulation. Hence, they have a low thermal conductivity. 50
Fig. 2-19. Plots of junction temperature versus thermal transfer coefficient for the three different structures in Fig. 2-18. 51
Fig. 2- 20. (a) Temperature distribution of the structure in Fig. 2-19(a); (b) temperature distribution of the structure in Fig. 2-19(b); and (c) temperature distribution of the structure in Fig. 2-19(c). 52
Fig. 2-21. The fabrication process of the single-sided cooling half-bridge module in Fig. 2-14. 53
Fig. 2-22. A fixture made for testing the bare die in Fig. 2-3 on a curve tracer. 54
Fig. 2-23. (a) Double-pulse test board for characterizing the dynamics of the single-sided cooling half-bridge module in Fig. 2-21; and (b) power loop design for DPT board in Fig. 2-23(a). 55
Fig. 2-24. Schematic of the DPT setup in Fig. 2-23. 55
Fig. 2-25. The DPT test circuit diagram with simplified parasitic inductances. L_{power} is the sum of package inductances in Fig. 2-17. Since the decoupling capacitor is removed, the total power loop inductances, $L_{powerloop}$ is the sum of package inductances, L_{power} and PCB trace inductance, L_{PCB} in the DPT testing board in Fig. 2-23. 56

Fig. 2-26. (a) DPT waveform of the single-sided cooling half-bridge module in Fig. 2-21;(b) detailed turn-on waveform of the module in Fig. 2-21; and (c) detailed turn-off waveform of the module in Fig. 2-21. 58
Fig. 2-27. The typical package layout for a double-sided cooling package. 60
Fig. 2-28. Traditional double-sided cooling layout for the half-bridge module using MOSFETs. 60
Fig. 2-29. Traditional double-sided cooling layout for the half-bridge module using GaN HEMTs (gate pads are not drawn in the figure). 61
Fig. 2-30. (a) Three-dimensional view of the double-sided cooling half-bridge module; and (b) exploded view of the module. 62
Fig. 2-31. Cross-sectional view of the double-sided cooling half-bridge module in Fig. 2-30. 63
Fig. 2-32. Circuit diagram of the double-sided cooling half-bridge module in Fig. 2-30 including parasitic inductances. 64
Fig. 2-33. Parasitic inductances depicted in Fig. 2-32 of the module Fig. 2-30. Gate bond wire inductance is not shown here. 64
Fig. 2-34. Simulated structure for the DSC half-bridge module package in Fig. 2-30. 65
Fig. 2-35. Plots of junction temperature versus thermal transfer coefficient for the single-sided cooling module in Fig. 2-14 and the double-sided cooling module in Fig. 2-30. 66
Fig. 2-36. Temperature distribution of the structure in Fig. 2-34. 67
Fig. 2-37. The fabrication process of the double-sided cooling half-bridge module in Fig. 2-30. 68
Fig. 2-38. Summary of the embedded packages in Fig. 2-5, Fig. 2-14, and Fig. 2-30. 69

Fig. 3-1. (a) Schematic of the measurement setup with the stacked-TIM technique; and (b) depiction of R_{thJTIM} versus t plot with the nonlinear fitting curve for extracting R_{thJC}. 74
Fig. 3-2. A simple thermal model for deriving an analytical expression for the nonlinear fitting curve: (a) Cross-sectional view of heat spreading in the TIM stack; and (b) top view showing the dimensions of the die and the package case. 76
Fig. 3-3. A procedure for improved measurement of R_{thJC} of a GaN HEMT package using R_{g2g} as the TSEP and stacked-TIM technique to avoid inaccurate measurement of the case temperature. 77
Fig. 3-4. (a) Schematic of the package cross-section; and (b) top view of a custom wire-bonding GaN package. 78
Fig. 3-5. (a) Overview of calibration setup for TSEP determination of the package in Fig. 3-4; and (b) R_{g2g} versus temperature calibration result of the package in Fig. 3-4. 79
Fig. 3-6. Plots of the measured (red and blue circles) and simulated (red and blue crosses) junction-to-TIM thermal resistances with each TIM type. The dashed lines are the fitted curves of the experimental data by using Eq. (3-4). The intercepts of the fitting curves on the y-axis are the experimentally determined R_{thJC}. 81

Fig. 3-7. Simplified single-sided cooling package: (a) cross-section view; (b) 3D view; and (c) top view of a completed package. 83
Fig. 3-8. R_{g2g} versus temperature calibration result for the simplified single-sided cooling package in Fig. 3-7. 84
Fig. 3-9. The plot of the measured junction-to-TIM thermal resistances for the simplified single-sided cooling package in Fig. 3-7. The dashed line is the fitted curve of the experimental data by using Eq. (3-4). The intercepts of the fitting curves on the y-axis are the experimentally determined R_{thJC}. 84
Fig. 3-10. Simplified thermal resistances in the double-sided cooling GaN HEMT package in Fig. 2-30. 85
Fig. 3-11. (a) R_{g2g} versus temperature calibration result for the top-side GaN chip in the double-sided cooling package in Fig. 2-30; and (b) R_{g2g} versus temperature calibration result for the bottom-side GaN chip in Fig. 2-30. 86
Fig. 3-12. (a) The plot of the measured junction-to-top-TIM thermal resistance ($R_{thJTTIM}$) of the package in Fig. 2-30; and (b) the plot of the measured junction-to-bottom-TIM thermal resistance, ($R_{thBTTIM}$) in Fig. 2-30. The dashed lines are the fitted curves of the experimental data by using Eq. (3-4). The intercepts of the fitting curves on the y-axis are the experimentally determined R_{thJTC} and R_{thJBC}. 87

Fig. 4-1. Circuit diagram of power cycling test. 91
Fig. 4-2. In the power cycling test: (a) the signal applied to the control switches; (b) power generated by the DUT; and (c) the temperature profile of the DUT. 92
Fig. 4-3. Data acquisition (DAQ) device, NI USB-6211from National Instruments. 94
Fig. 4-4. LabVIEW program control logic diagram for the power cycling test in Fig. 4-1. 94
Fig. 4-5. Fabricated wire-bonding GaN HEMT package. 95
Fig. 4-6. Fabricated two GaN HEMT embedded packages and wire-bonding packages. 96
Fig. 4-7. The fabricated power cycling test board of the circuit diagram in Fig. 4-1. 97
Fig. 4-8. LabVIEW front panel for K factor calibration. 98
Fig. 4-9. Power cycling setup with a clamp and a water-cooling plate. 98
Fig. 4-10. LabVIEW front panel for power cycling test. 99
Fig. 4-11. (a) R_{on} versus numbers of cycles for the single-sided cooling embedded package sample 1 in Fig. 4-6; and (b) R_{on} versus numbers of cycles for the single-sided embedded package sample #2 in Fig. 4-6. 100
Fig. 4-12. Failed wire-bonding package after conducting 75 A for 0.1 s. 101

Fig. A-1. Cross-sectional schematic of the wire-bonding GaN HEMT package with nitrogen atmosphere. 106
Fig. A-2. Fabrication steps of the wire-bonding GaN HEMT package with nitrogen atmosphere Fig. A-1. 107
Fig. A-3. 3D model of the design for surface mount GaN HEMT package with silver rod interposers. 109

Fig. A-4. Cross-sectional view of the surface mount GaN HEMT package with silver rod interposers in Fig. A-3. 109
Fig. A-5. Schematic of the parasitic inductance of the surface-mounted GaN HEMT package with silver rod interposers in Fig. A-3. 109
Fig. A-6. The fabrication process of the surface-mount GaN HEMT package with silver rod interposers. 110
Fig. A-7. Setup for measuring the static characteristics of the GaN HEMT package in Fig. A-2 up to 250 ^{o}C. 112
Fig. A-8. Left: Dummy package substrate showing a thermocouple affixed on top of a nonfunctional chip; right: after sealing the interconnected substrate inside a PEI housing in Fig. A-2. 112
Fig. A-9. I_D - V_{GS} transfer characteristics at different temperatures (V_{DS} = 20 V) for the package in Fig. A-2. 113
Fig. A-10. Threshold voltage vs. temperature of the GaN HEMT packaged in Fig. A-2. 113
Fig. A-11. I_D - V_{DS} curves at different temperatures of the package in Fig. A-2. 114
Fig. A-12. Packaged GaN HEMT on-resistance ($R_{on_package}$) vs. junction temperatures of the GaN HEMT package in Fig. A-2. 115
Fig. A-13. The plot of the leakage current, I_D at V_{DS} = 400 V vs. temperature of the GaN HEMT package in Fig. A-2. 115
Fig. A-14. The schematic of DPT for the high-temperature test. 116
Fig. A-15. The overview of high-temperature DPT setup for the packaged GaN HEMT in Fig. A-6. 117
Fig. A-16. The DPT waveform @ 400 V, 40 A, and 250 ^{o}C for the GaN HEMT package in Fig. A-6. 117
Fig. A-17. Switching loss versus temperature at different temperatures of the GaN HEMT package in Fig. A-6. 118

List of Tables

Table 1-1. Technical target for high voltage power electronics [7]. 17
Table 1-2. Wide bandgap advanced integrated power module 2025 technical guidelines [7]. 17
Table 1-3. Comparison of commercial 650-V, 30-A Si MOSFET, SiC MOSFET, and GaN HEMT. 22
Table 1-4. Thermal conductivity of different semiconductor materials. 24

Table 2-1. Values of the simulated parasitic inductances in Fig. 2-7. 38
Table 2-2. Values of the simulated parasitic inductances in Fig. 2-16. 48
Table 2-3. Simulated thermal resistances of the three cooling structures. 52
Table 2-4. Average on-resistance and leakage current from two devices measured in the chip form or in the package in Fig. 2-21. 54
Table 2-5. Component values of the DPT Setup in Fig. 2-23. 56
Table 2-6. ANSYS Q3D extracted values of the parasitic inductances and capacitances of the DPT setup in Fig. 2-23. 56
Table 2-7. Values of the simulated parasitic inductances from Fig. 2-32. 65
Table 2-8. Simulated thermal resistances of the two proposed structures in Fig. 2-14 and Fig. 2-30. 66
Table 2-9. Average on-resistance and leakage current from two switches measured in the chip form or in the DSC half-bridge module. 68

Table 3-1. Comparison of different temperature-sensitive electrical parameters. ... 71

Table 4-1. Typical power cycling evaluation test conditions. 92

Table A-2. Calibration of the temperature difference between junction and case. 111

Chapter 1 Introduction

1.1 Power Module Requirements in Electric Vehicles

As power consumption has increased, global warming has become a severe issue. Until 2021, the global temperature was 0.85°C higher than NASA's baseline. Moreover, the rate by which the sea level is increasing, 4.4 mm/year, had reached its maximum value in 1993 [1]. The combustion of fossil fuels and the generation of greenhouse gases, mainly carbon dioxide (CO2), are the major causes of global warming. The United Nations has arranged the Paris Agreement to limit emissions [2]. In November 2020, Joe Biden, the president of the United States, announced the plan and signed an executive order to rejoin the Paris Agreement [3, 4].

Shown in Fig.1-1, traditional gasoline transportation contributes a significant portion to greenhouse gas emissions, almost 30% in the United States in 2019. Given that gasoline engines are the climate killers, electric vehicles (EVs) have come to the forefront as an essential component of limiting emissions [5]. Compared to traditional gasoline vehicles, EVs have better fuel economy, lower fuel cost, and no tailpipe emissions [6].

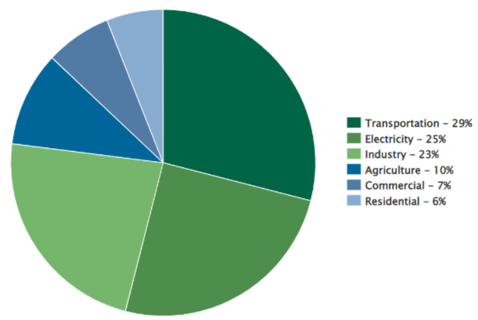


Fig.1-1. 2019 U.S. greenhouse gas emissions distribution [5].

As EVs emerge as being favored by both the government and individuals in the United States, EV industries face significant challenges, including limited range, slow charging speed, and limited power density and efficiency using traditional silicon-based power switches. Recently, the Electrical and Electronics Technical Team (EETT) under the Vehicle Technologies Office (VTO) of the Department of Energy (DOE) started a mission to accelerate the development of electric traction drive systems for EVs. The mission's baseline is to reduce the cost of electric traction systems by $6/kW for a 100-kW peak system and boost the power density to 33 kW/L [7].

Fig.1-2 shows the typical components inside a generic electric traction drive system. The box with a dashed line frame indicates the high-voltage power electronics sub-systems, which are the main focus of the EETT. And Table 1-1 gives the technical targets for high-voltage power electronics.

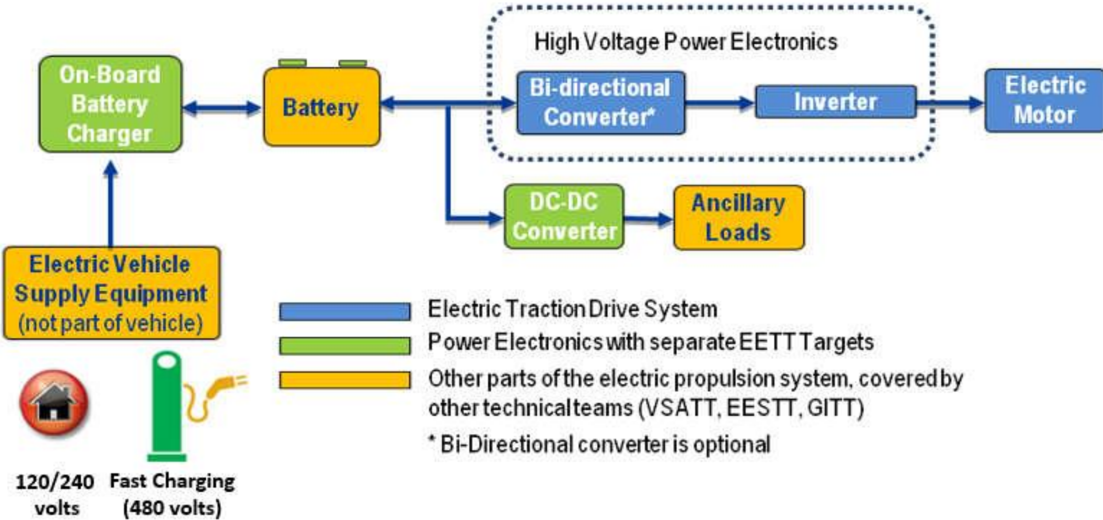


Fig.1-2. Components of the generic electric traction drive system [7].

Table 1-1. Technical target for high voltage power electronics [7].

Power Electronics Targets			
Year	2020	2025	Change
Cost ($/kW)	3.3	2.7	18% cost reduction
Power Density (kW/L)	13.4	100	87% volume reduction

Since traditional silicon devices are very mature and already reaching their theoretical limit, to achieve the goal of dramatically boosting the power density, implementation of commercialized wide-bandgap semiconductor power devices, like silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) and gallium-nitride (GaN) high-electron-mobility transistors (HEMTs) show promise as the way to go. Furthermore, wide-bandgap semiconductor power devices also have the potential to increase the maximum operating temperature. Therefore, the power electronics systems can be smaller, and the size of the cooling systems can also be reduced. Table 1-2 shows part of the 2025 technical guideline requirements for wide-bandgap advanced integrated power modules proposed by the EETT.

Table 1-2. Wide bandgap advanced integrated power module 2025 technical guidelines [7].

Requirement	Current State-of-Art (WBG)	AIPM (Nominal)	Scalability
Peak power (kW)	**30**	**100**	**200**
Continuous power (kW)	15	55	110
Voltage rating (V)	900 – 1,200	900	1,200
Maximum device current (A)	100	200	200
Device metallization			
Top	NO	NO	YES
Bottom	YES	YES	YES
Maximum junction temperature (°C)	180	250	250

1.2 Introduction of GaN HEMTs

Wide-bandgap (WBG) semiconductor power devices have become increasingly popular in recent years. Compared with traditional Si materials, which have a bandgap of 1-1.5 electronvolts (eV), wide-bandgap semiconductor materials such as SiC and GaN have bandgaps above 2 eV.

From a materials perspective, WBG semiconductor materials like GaN and SiC are favored in power electronics applications for their superior performance over Si. Table 3 compares Si, 4H-SiC, and GaN semiconductor materials; as shown, GaN has the widest bandgap (3.4 eV), and the highest electron mobility (2000 $m^2/V/s$), and the highest saturation velocity (2.5×10^7 cm/s). All these promising features contribute to the potential to achieve the lowest specific on-resistance and a faster switching capability for GaN power devices. Fig.1-3 shows the specific on-resistance versus breakdown voltage for different semiconductor materials and their theoretical limits [8]. From this plot, GaN devices have a greater limit than SiC and Si devices to achieve higher power density and lower conduction loss. Fig.1-4 also highlights some key material properties of WBG semiconductors [9]. GaN has the best features over SiC and Si materials (e.g., high electron velocity, high electric field, high bandgap). However, bulk GaN crystal quality limitations make it hard to develop vertical GaN devices like Si or SiC MOSFETs. Instead, GaN HEMTs came out by growing heteroepitaxy and creating an AlGaN/GaN layer on a-Si, SiC, or sapphire substrate. This AlGaN/GaN piezoelectric layer enables a two-dimensional electron gas (2DEG) channel and achieves lower on-resistance and fast switching features. Power electronics engineers favor these features to develop high-frequency, high-efficiency power converters. With the increasing demands, GaN-on-Si HEMTs are available on the commercial market.

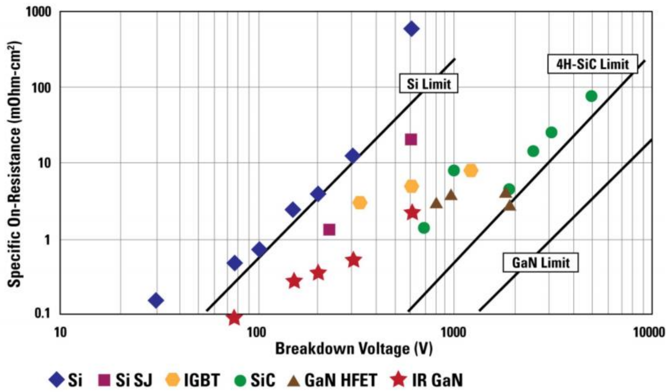


Fig.1-3. The specific on-resistance versus breakdown voltage for different semiconductor materials. [8].

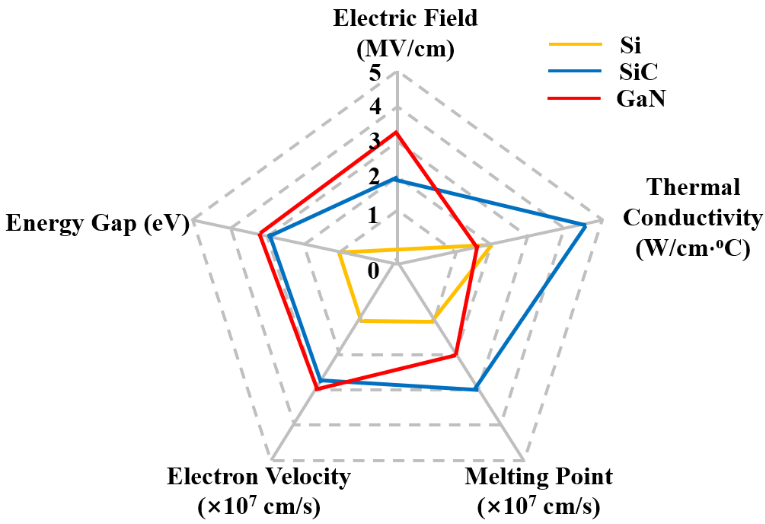


Fig.1-4. Summary of Si, SiC, and GaN relevant material properties [9].

However, as shown in Fig.1-5, traditional GaN HEMT is a normally-on (depletion-mode, D-mode) switch. This feature makes traditional GaN HEMTs require a negative gate-source voltage to fully turn off their 2DEG channel. Power electronics engineers do not favor it because it is not easy for them to design a proper gate driver to control the GaN devices. People have different approaches to making normally-off (enhancement-mode, E-mode) GaN HEMTs. One typical practice is to use a separate low-voltage Si MOSFET and connect it between the gate and source

of a GaN HEMT, as shown in Fig.1-6 [10]. In this structure, when the Si MOSFET turns off, the voltage between the GaN HEMT's gate and the source is negative, and this keeps the GaN HEMT turned off. When the Si MOSFET turns on, the GaN HEMT's gate and source are of the same potential, and the GaN HEMT is on. This method to achieve an E-mode GaN HEMT is straightforward and friendly for electrical engineers. However, the extra Si MOSFET adds another device to the system, which incurs more losses, extra packaging workload, extra cost, and even reliability issues [11-13].

Another way to achieve an E-mode GaN HEMT is on the wafer level. Several methods have been reported. Some tried to make a metal-insulator-semiconductor (MIS) gate structure and remove the AlGaN layer below the gate [14, 15]. Some use negatively charged ions' implants into the AlGaN layer below the gate [16, 17]. However, the most common method in the industry is to add a p-type GaN layer between the gate and the AlGaN layer to deplete the channel [18-20].

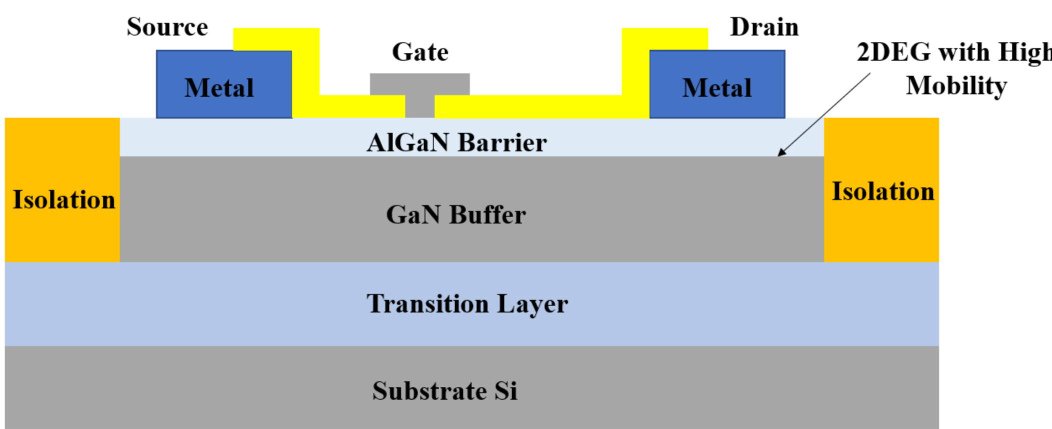


Fig.1-5. Traditional GaN HEMT device structure.

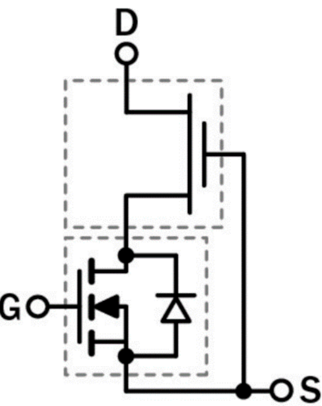


Fig.1-6. GaN HEMT cascode device structure [10].

The typical structure of an enhancement-mode GaN HEMT using a p-type GaN layer is shown in Fig.1-7 [21, 22]. The threshold voltage is around 1 V, and the gate turn-on voltage is usually set to 6 V. In this way, the E-mode GaN HEMT behaves like a traditional Si MOSFET with a slightly low turn-on voltage. Also, thanks to the 2DEG layer, GaN HEMTs have much smaller on-resistance and junction capacitances than their Si and SiC counterparts, as shown in Table 1-3. These features allow GaN HEMTs to achieve significantly less conduction and switching loss in power-conversion systems.

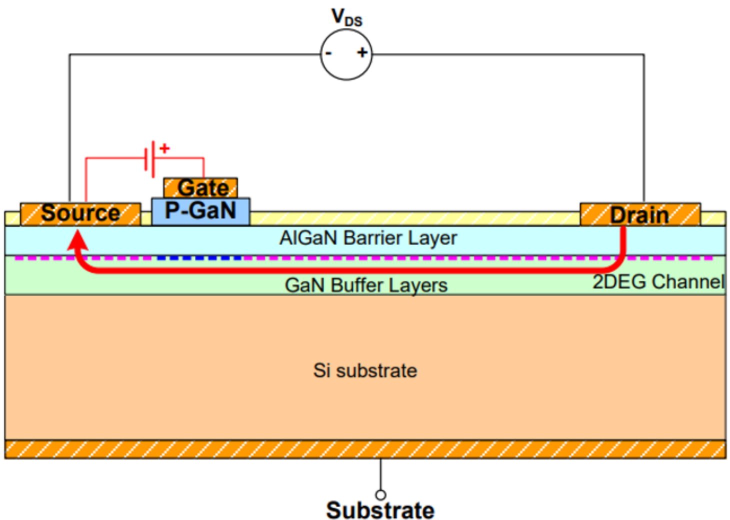


Fig.1-7. The typical structure of an E-mode GaN HEMT [21].

Table 1-3. Comparison of commercial 650-V, 30-A Si MOSFET, SiC MOSFET, and GaN HEMT.

650V, 30 A	Si Super Junction	SiC MOSFET	GaN HEMT
C_{iss} (pF)	5030	1020	242
C_{oss} (pF)	215	80	65
dv/dt (V/ns)	<10	18	90

The HEMT structure is on a Si substrate. The Si substrate helps protect the channel and provides insulation. Also, since Si substrates are much cheaper than SiC, GaN, and sapphire substrates, this solution can cut down the device cost and is also commercialization friendly.

1.3 Challenges for Packaging and Characterizing GaN HEMTs

Although GaN HEMTs have benefits in terms of low specific on-resistance, low switching loss, and high-temperature capability, it is significantly challenging to fully realize these good features and characterize their packaging performance.

The first challenge for GaN HEMT packaging is to compensate for its high dv/dt and di/dt during switching. In the previous section, Table 4 shows that GaN HEMTs have much smaller junction capacitance than their Si and SiC counterparts. From the switching loss perspective, this is beneficial. However, it also brings high dv/dt and di/dt during switching events. And, in a converter system, there are some inevitable parasitic inductances and capacitances. If GaN HEMT packages introduce significant parasitic inductances or capacitances (e.g., bond wires, terminations), the high dv/dt and di/dt will induce large current and voltage overshoots on the parasitic capacitances and inductances. Also, ringing will occur in the system. These overshoots and ringing can increase the system's electromagnetic interference (EMI) noise, significantly stress

the device and its gate driver, and increase loss due to the ringing. Finally, the whole system's reliability will be impacted.

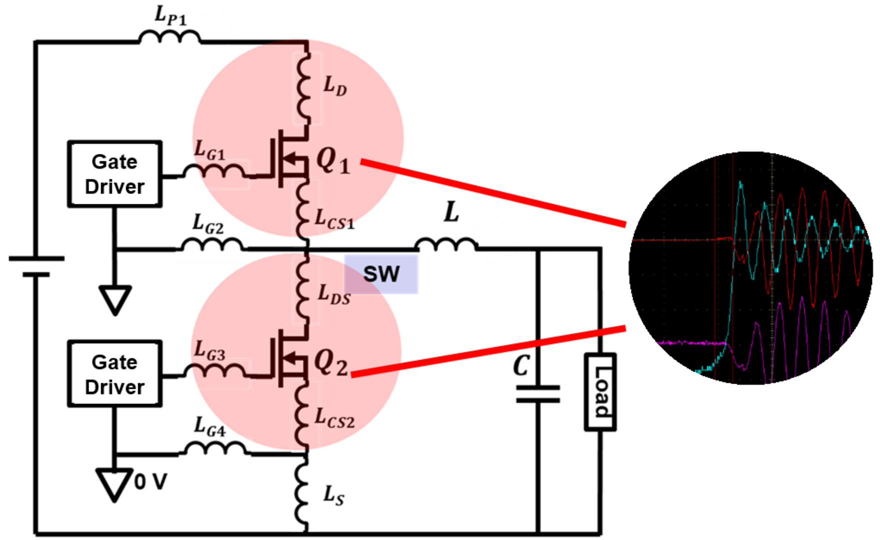


Fig.1-8. A typical buck converter circuit diagram with parasitic inductances.

Thermal management is the other challenge for GaN HEMT packaging. Compared to Si and SiC devices, GaN devices can achieve the same on-resistance with smaller die sizes. This means GaN devices have higher heat flux than their Si and SiC counterparts during operation. However, the thermal conductivity of the GaN or its silicon substrate is around four times smaller than that of the SiC, as shown in Table 1-4. Therefore, considering single-sided cooling from the GaN HEMT Si substrate, the generated heat has to go through the 2DEG channel, Si substrate, die-attachment layer, and device case, as shown in Fig.1-9. The safe operation area plots for the Si MOSFET, SiC MOSFET, and GaN HEMT are shown in Fig.1-10. Since the GaN HEMT has a larger junction-to-die-substrate thermal resistance (R_{thJS}) and higher heat flux than the Si and SiC switches, carefully optimizing the die-substrate-to-case thermal resistance (R_{thSC}) is crucial.

Table 1-4. Thermal conductivity of different semiconductor materials.

	Si	SiC	GaN
Thermal Conductivity (W/cm^2K)	1.5	5	1.3

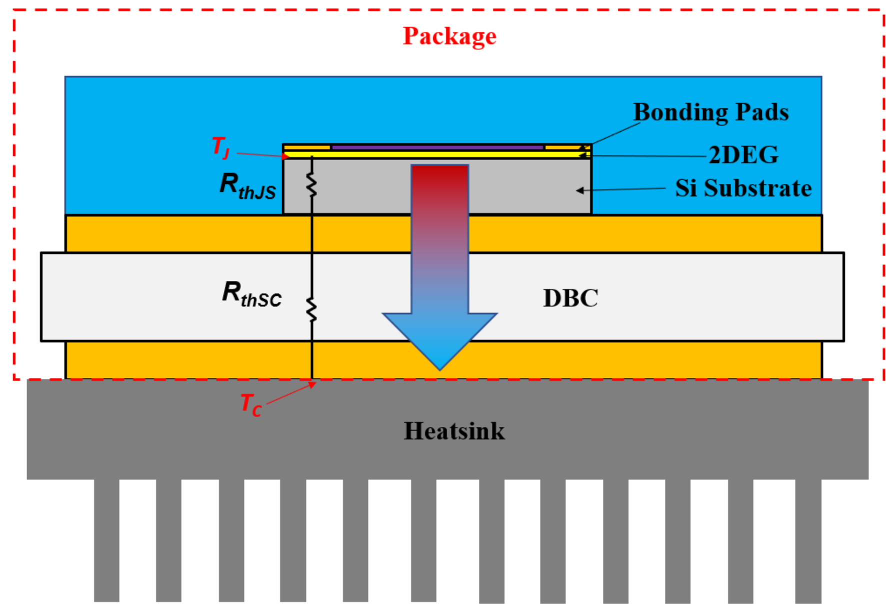


Fig.1-9. The typical cooling structure of a GaN HEMT package (without interconnections).

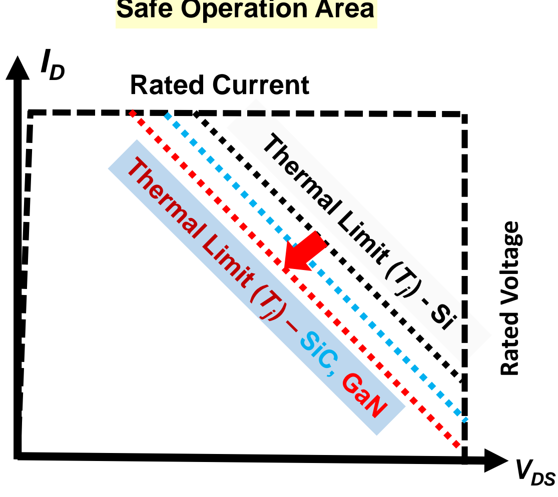


Fig.1-10. Safe operation area plot for Si, SiC, and GaN devices.

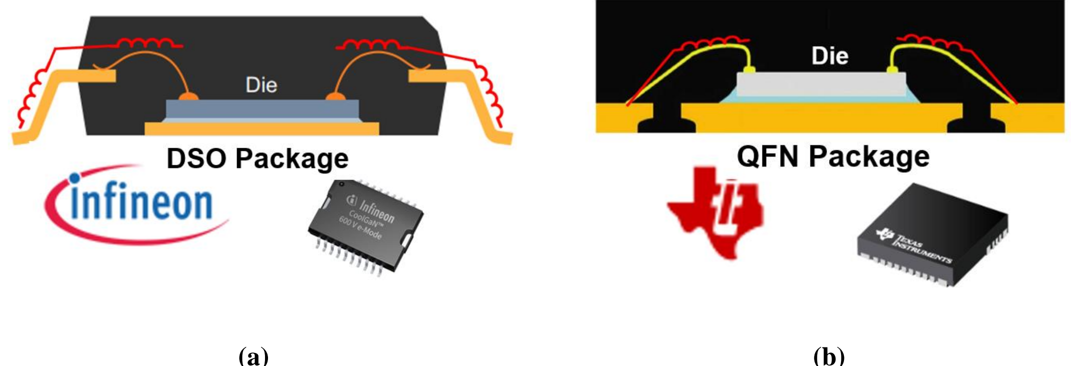
Also, experimental verification of the electrical and thermal performance of GaN HEMT packages is the key to ensuring package development success. Electrical static characterization of GaN HEMT packages, including I-V and breakdown voltage tests, is straightforward. It is the minimum requirement for a GaN HEMT package. On the other hand, dynamic characterization is crucial to test the switching performance of GaN HEMT packages. Engineers favor a double pulse test (DPT) to evaluate the dynamic performance and obtain voltage, current spikes, ringing, and switching loss of GaN HEMTs. Based on the ringing period in the DPT waveform, one can also measure and evaluate the parasitic inductances and capacitances. There are established standards for both static and dynamic tests.

However, for thermal characterization (e.g., junction-to-case thermal resistance, R_{thJC} measurement), there is no test standard for GaN HEMT packages. Therefore, the main challenge of measuring the R_{thJC} of a GaN package is the lack of accurate techniques to determine the device's junction temperature, T_J. Although common temperature-sensitive electrical parameters (TSEPs) to determine T_J work well with Si and SiC devices, they lack sufficient sensitivity or stability due to the GaN HEMT's buffer layer charge-trapping effect [23, 24]. Also, accurately measuring case temperature is another challenge.

After electrical and thermal characterizations, reliability evaluation is the last step to envision how well the GaN HEMT packages would perform in the long term. The power cycling test is an efficient reliability test, and it not only provides temperature stress but also simulates the power switch's actual operation [25-27]. However, an accurate way to monitor T_J is important for conducting a power cycling test for a GaN HEMT package.

1.4 The State-of-the-Art Packaging Techniques for GaN HEMTs

To solve the packaging challenges for GaN HEMTs, researchers have put great effort into developing and improving packaging technologies for GaN HEMTs. As shown in Fig.1-11(a) and (b), there are some commercial packaging practices for GaN HEMTs to avoid the traditional transistor outline (TO) packages with long leads [28, 29]. These surface-mounted packages can significantly reduce the footprint and parasitic inductance related to terminations. However, traditional bond wires are used for interconnections. These bond wires still limit the device's footprint and add additional inductance to the GaN HEMTs' package. The bonded area may also encounter fatigue failure because of the thermal expansion coefficient (CTE) mismatch between the GaN HEMT bare die and the bond wires [30].



(a) (b)

Fig.1-11. (a) The dual small outline (DSO) package from Infineon [28], and (b) the Quad flat no-lead (QFN) package from Texas Instruments [29].

To avoid bond wires and further increase packaging density, one can integrate GaN HEMTs onto a printed circuit board (PCB). The typical PCB-embedded structure is shown in Fig.1-12. The PCB-embedded technology in [31] can be applied for GaN HEMT packaging, and plated copper vias were used for the interconnections. In [32], the GaN HEMTs bare dice were buried between

a second and third layer of a four-layer PCB, and the device's thermal pads were connected to the bottom copper layer. However, that approach required a 5-10 mm copper finish on the dice, not a standard process in die fabrication. Also, an extra buffer layer is required when using ultraviolet (UV) laser drilling in the PCB to avoid damaging the die surface. However, there are other versions of PCB-embedded technology using mechanical drilling and requiring stud bumps or a metal foam interposer for PCB-to-die interconnection [33-35]. They are shown in Fig.1-13 (a) and (b). However, the composite material, FR-4 in the PCB, has low thermal conductivity, and thermal vias are insufficient to extract heat.

Furthermore, there is no insulation between the die's substrate to the heatsink for PCB-embedded packages. Usually, a thick non-conductive thermal interface material (TIM) is required for electrical isolation, and this addition reduces heat-dissipation efficiency. GaN Systems developed an insulated metal substrate (IMS) based GaN HEMT power module in [36] to improve the package's thermal performances and to solve the insulation issue in Fig.1-14. However, since the insulation for IMS is a thin polymer dielectric layer, the thermal conductivity (3-7 W/mK) and thermal-mechanical reliability are much lower than with an aluminum nitride (AlN) direct-bonded copper (DBC) substrate (up to 170 W/mK). A single-sided cooling module and a double-sided cooling module with two DBC substrates were proposed in [37, 38]. Their structures are shown in Fig.1-15(a) and (b). They can achieve less than 3 nH parasitic inductance, reliable ceramic insulation, and better thermal performance than PCB-embedded solutions. However, they directly sandwiched the GaN HEMTs bare dice between two rigid substrates using solder without any interposers or buffer layers, which can cause significant thermal-mechanical stresses by the coefficient of thermal expansion (CTE) mismatch and lower the reliability of the GaN HEMT packages. The state-of-the-art (SOA) packages for GaN HEMTs are concluded in Fig.1-16.

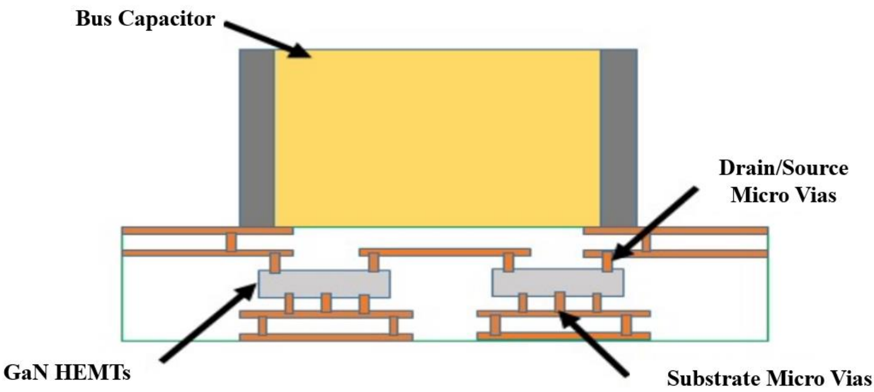
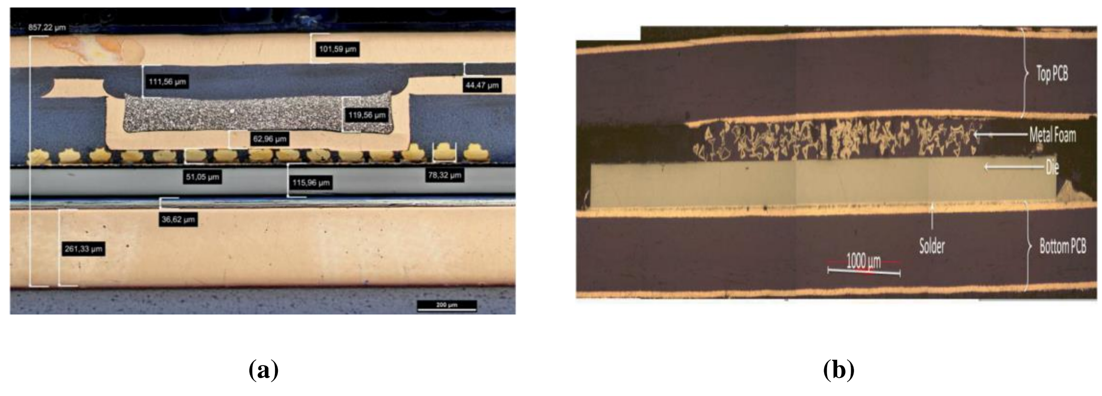


Fig.1-12. A structure of PCB-embedded packaging of GaN HEMT [32].



(a) **(b)**

Fig.1-13. (a) Stud bump interconnection of power switch packaging [33], and (b) metal foam interconnection of power switch packaging [34].

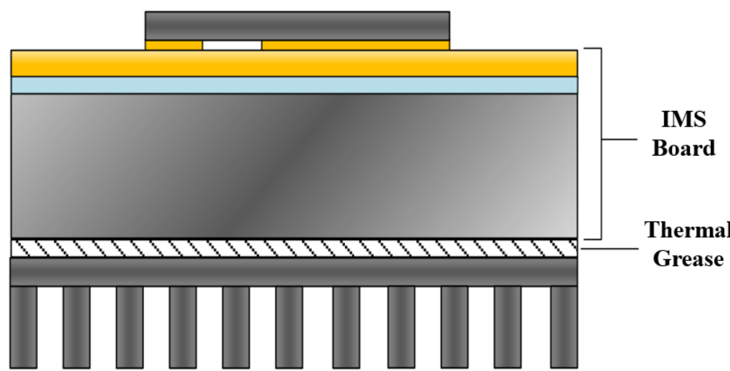


Fig.1-14. The structure of an insulated metal substrate (IMS) based GaN HEMT power module [36].

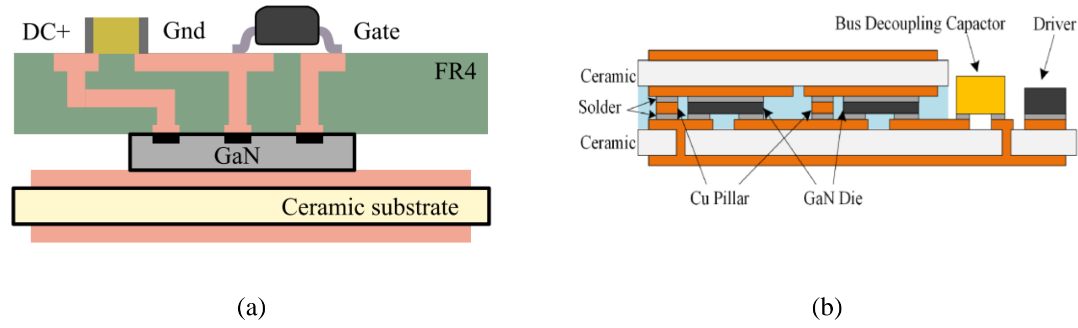


Fig.1-15. (a) A PCB/DBC hybrid GaN HEMT packaging structure [37], and (b) a DBC/DBC sandwich GaN HEMT packaging structure [39].

	Package	Key Features	Voltage Ratings	Current Ratings	Parasitic Inductance	Footprint Density $A_{die}/A_{package}$	Thermal Resistance
1. Wire-Bond Interconnect	Infineon	DSO Package (Wire-Bonded)	600 V	14 A	3~5 nH	<0.1	1 °C/W
		QFN Package (Wire-Bonded)	600 V	12 A	1~3 nH	~0.1	0.5 °C/W
2. Planar Interconnect	GaN Systems	GaN_{PX} Package (Copper Pillars)	650 V	60 A	<0.5 nH	0.6	0.3 °C/W
		PCB-Embedded Package (Vias)	650 V	60 A	<0.5 nH	~1	NA
		PCB-DBC Hybrid Package (Vias)	650 V	60 A	<3 nH	NA	NA
		DBC-DBC Package (Solder)	650 V	30 A	< 1 nH	0.4	0.3 °C/W

Fig.1-16. Comparison of the state-of-the-art GaN HEMT packages [21, 28, 29, 32, 37, 38].

1.5 Significance and Objectives

This dissertation aims to develop packaging techniques for gallium-nitride high-electron mobility-transistors (GaN HEMTs) to achieve high power density, low parasitics, and low thermal resistance for power electronics applications and develop high-temperature GaN HEMTs packages

to characterize them up to 250 °C. Embedded packaging techniques with vertical interconnections were developed to solve the challenges. The electrical performance of the GaN HEMT embedded packages was characterized. An improved junction-to-case thermal resistance measurement method was introduced to measure the junction-to-case thermal resistance experimentally. To provide reliable high-temperature characterization data of commercially available GaN-on-Si HEMTs, high-temperature packages have been designed and fabricated, and then are characterized at temperatures up to 250 °C.

The specific objectives of this dissertation are summarized as follows.

1. Design, fabricate, and electrically characterize embedded packages for 650-V, 150-A GaN HEMTs to achieve high density, low parasitic loop inductance, and good thermal performance.
2. Experimentally characterize and verify the thermal performance of the fabricated embedded GaN HEMT packages.
3. Evaluate the reliability of the fabricated embedded GaN HEMT package by conducting a power cycling test.

1.6 Summary of Dissertation Organization

Following the introduction chapter, in Chapter 2, embedded packaging techniques will be discussed in detail. First is the chapter introduction. Then, in Section 1, a 650-V, 150-A, 10-mΩ GaN HEMT bare chip is introduced for potential high-power application in an electric drive system. To first demonstrate embedded packaging technology for a single GaN HEMT device and to achieve low parasitic inductances, small footprint, and good thermal performance, a PCB-interposer-on-DBC package with vertical interconnections is introduced. The layout design and the fabrication process of the single device package are later introduced. The single device

package's static and dynamic characterization results are also shown. Then, an embedded GaN HEMT half-bridge module is proposed based on the concept of a PCB-interposer-on-DBC single device package. The embedded packaging technique of the GaN HEMT half-bridge module with double-sided cooling and stacked-dice structure was finally designed and verified.

To characterize the thermal performance of the embedded GaN HEMT packages proposed in Chapter 2, an accurate junction-to-case thermal resistance, the R_{thJC} measurement technique is introduced in Chapter 3. First, the junction temperature, T_J, was obtained using a gate-to-gate electrical resistance as the TSEP. Then, the stack thermal interface materials (TIMs) technique was introduced to reduce errors in case temperature measurement. Next, a wire-bonded package was fabricated and characterized to verify the measurement technique. The measurement results were also compared with the finite element analysis (FEA) simulation. Finally, the thermal resistances of the embedded packages were tested.

Chapter 4 studies the reliability of the embedded GaN HEMT packages for potential application in electric traction drives by carrying out power cycling tests. The embedded package testing samples were fabricated together with traditional wire-bonded samples. Using the T_J measurement technique in Chapter 3, the power cycling junction temperature range was controlled from 25°C to 125°C. The testing current was 75 A, half of the rated current. Finally, the power cycling results were concluded.

Chapter 5 summarizes the dissertation topic of GaN HEMT packaging and characterization. Potential future work is also proposed in Chapter 5.

Chapter 2 Embedded Packaging of eGaN HEMTs: Design, Simulation, Fabrication, and Electrical Characterization

2.1 Introduction of Embedded Packaging Techniques for eGaN HEMTs

As discussed in the first chapter, GaN HEMTs benefit from low specific on-resistance and fast switching speed as compared with their Si and SiC counterparts. However, these benefits also bring packaging challenges over ultra-low packaged inductance and effective junction-to-case thermal resistance. A traditional wire-bonding GaN HEMT package with lateral interconnection is shown in Fig. 2-1. The GaN HEMT bare chip is attached to a substrate or leadframe by adhesive materials like solder. On the top side, bond wires are used for interconnections. One side of the bond wires connects to the gate, drain, and source bonding pads. The other side connects to the termination or leadframe. So, this traditional way can be considered a lateral interconnection. It is a cost-effective solution since wire bonding is a standard process established for Si and SiC devices. However, it also increases the footprint, hence, lowing package density. Compared to Si and SiC devices, GaN HEMTs are more sensitive to parasitic inductance. The wire-bonding interconnection also has a relatively large parasitic inductance (3-10 nH), which can cause overshoots and ringing.

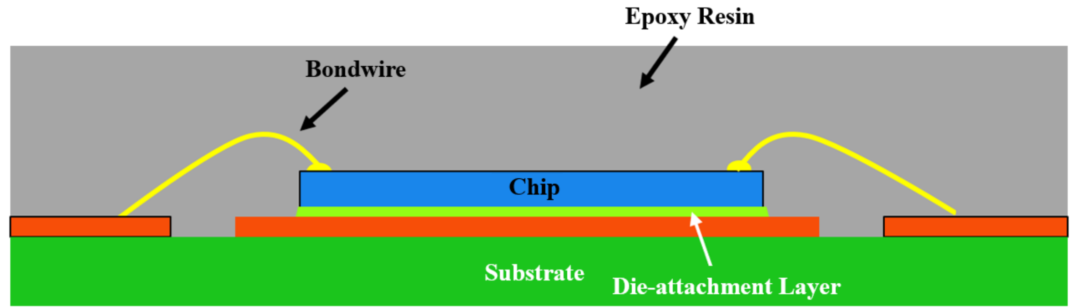


Fig. 2-1. An example of a wire-bonding package with lateral interconnection.

Embedded packaging was first introduced in integrated circuit (IC) packaging. It is specifically called embedded die packaging [40, 41]. Nowadays, embedded packaging is popular and favored by the IC industry. However, most studies have focused on wafer-level integration for low-voltage-rating IC chips. Inspired by the embedded packaging technology from the IC industry, an embedded packaging concept for GaN HEMT power devices was developed. The structure is shown in Fig. 2-2. The main difference between wire bonding and embedded packaging is the interconnection type. Embedded packaging uses either plated vias or metal interposers directly connecting the bonding pads to the top layer. The GaN HEMT bare chip is buried between the substrate and top layer. In this way, the embedded package can achieve a 50% smaller footprint, a 50% lower profile, and only one-third of the parasitic inductance as compared with the wire-bonding package. Therefore, compared to wire-bonding packages, embedded packages can help tackle various challenges faced in implementing GaN HEMTs.

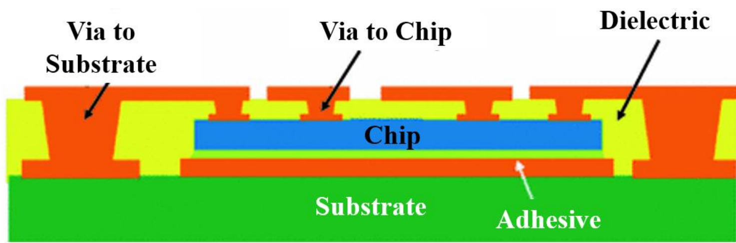


Fig. 2-2. An example of an embedded package with vertical interconnection.

However, the SOA embedded packaging mainly uses the PCB process, as discussed in Chapter 1 [10, 31-35, 37]. The major challenge is the significant junction-to-case thermal resistance that occurs due to the poor thermal conductivity (1 W/m-K) of the FR-4 lamination materials in the PCB. To solve the packaging challenges and demonstrate novel embedded packaging techniques for the latest GaN HEMT (650 V, 150 A, 10 mΩ), this dissertation introduces single-sided and double-sided cooling embedded GaN HEMT packages.

In Chapter 2, Section 2, the detailed structure of the latest version of GaN HEMT (650 V ,150 A, 10 mΩ) is introduced. The challenges for packaging this latest GaN HEMT bare die are also highlighted. Section 3 demonstrates a rapid embedded package demo (PCB-interposer-on-DBC package) for a single GaN HEMT using gold-plated pins for all the interconnections. The technique in Section 3 is further improved and extended to half-bridge module packages with more robust interposers and integrated decoupling capacitors in Section 4. Finally, Section 5 summarizes the embedded package techniques.

2.2 GaN HEMT Bare Chip for Packaging

Recently, GaN Systems developed 650-V, 120-A, and 150-A eGaN HEMTs (GS-065-120-1-D and GS-065-150-1-D) only in bare die form. Since these devices are for high-power applications

and the die size and current rating are very large, no commercial package is available yet. The overview layout of the bare chips is the same, as shown in Fig. 2-3. The total size of the chip is 12650.0 μm × 5600.0 μm. The gate, drain, and source bonding pads are on the top copper redistribution layer (RDL). The gate bonding pads are tiny, only 420 μm × 330.5 μm and the gap between the gate and the source pad is only 50 μm. There are two gate pads on one bare die, located on the left and right corners. This design of the bare die is to ease the PCB design in real application. The drain and source bonding pads are two high-aspect-ratio rectangles (12030.4 μm × 499.5 μm). Apart from the gate, drain, and source bonding pads on the top RDL, there is a fourth terminal called the body -- the chip's substrate. To avoid the backgate effect and maintain the driving voltage for GaN HEMTs, it is better to connect the body of the GaN HEMT to the source and keep them at the same potential.

The bare die finish is shown in Fig. 2-4. The die is made of 8.0-μm thick copper on the top layer and 0.1-μm thick titanium (Ti), 0.3-μm thick nickel (Ni), and 1.0-μm thick silver (Ag) on the bottom.

When the 2DEG is conducting, most of the heat is generated at the 2DEG and spreads to both the copper redistribution layer (RDL with gate, drain, and source bonding pads) and the Si substrate. Although the 2DEG is close to the RDL, the junction-to-RDL thermal resistance (0.18 ^{o}C/W) is much greater than that of the junction to the substrate (0.07 ^{o}C/W) due to the air gap or dielectric insolation between the electrodes.

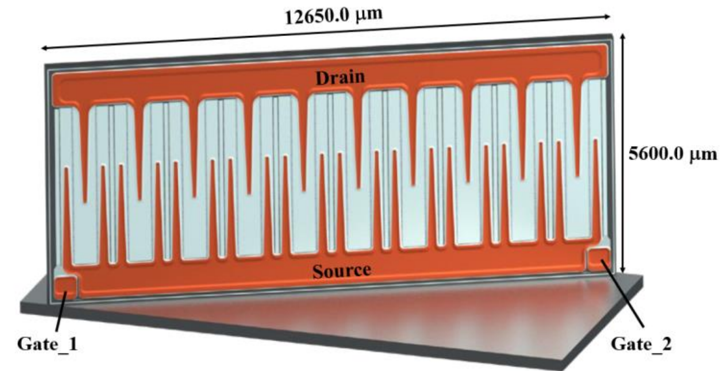


Fig. 2-3. The overview of the 650 V, 150 A GaN HEMT bare die.

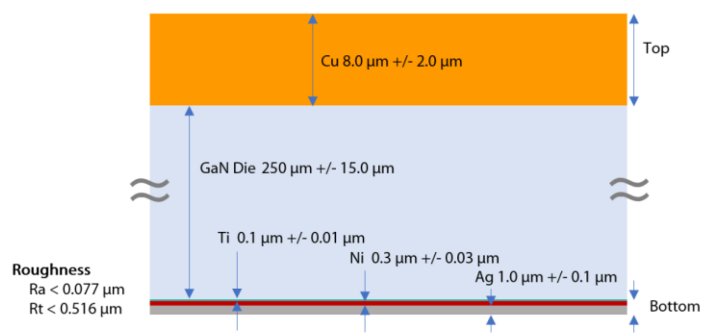


Fig. 2-4. The surface finish of the bare die in Fig. 2-3.

2.3 Embedded Packaging for a Single GaN HEMT Chip: PCB-Interposer-on-DBC Packaging

A cross-sectional view of the embedded package for a single GaN HEMT chip is shown in Fig. 2-5. Dimensional details of the package were worked out for a 650 V, 120 A GaN E-HEMT bare die (GS-065-120-1-D) from GaN Systems. Following the chip manufacturer's recommendation, the die's thermal pad was bonded to a DBC substrate by silver sintering. For heat extraction, a heat sink would be attached to the DBC. To interconnect the chip terminals on the top, gold-plated pins of about 254 μm in diameter were used. They were dropped through the 300-μm diameter vias in the PCB interposer board. The gold pins and the chip terminals were also bonded by silver sintering. The heads of the pins were soldered to the PCB using a tin-lead alloy so that the chip terminals

were connected to the circuit on the PCB. To adjust the clearance space between the PCB and the top surface of the chip, shims were used on the DBC. Since the gate pads are small, the functional PCB board with vias was carefully aligned to the bare die to get a good connection and to avoid shorting. The alignment blocks were used to align the PCB with the bare die. Fig. 2-6 shows the fabricated embedded GaN package. The circuit diagram of the package is shown in Fig. 2-7. The ANSYS Q3D Extractor was used to simulate parasitic inductances, as shown in Fig. 2-7. The simulated values are shown in Table 2-1. The whole package is embedded between a PCB and a DBC. The PCB interposer on the top aligns gate connections and interconnections. The package is also called a 'PCB-interposer-on-DBC package.' The large pads on the PCB board in Fig. 2-6 are for testing. It can be further cut to a smaller size for high density. In the future, it can also enlarge to a bigger size and integrate gate drivers and power supplies.

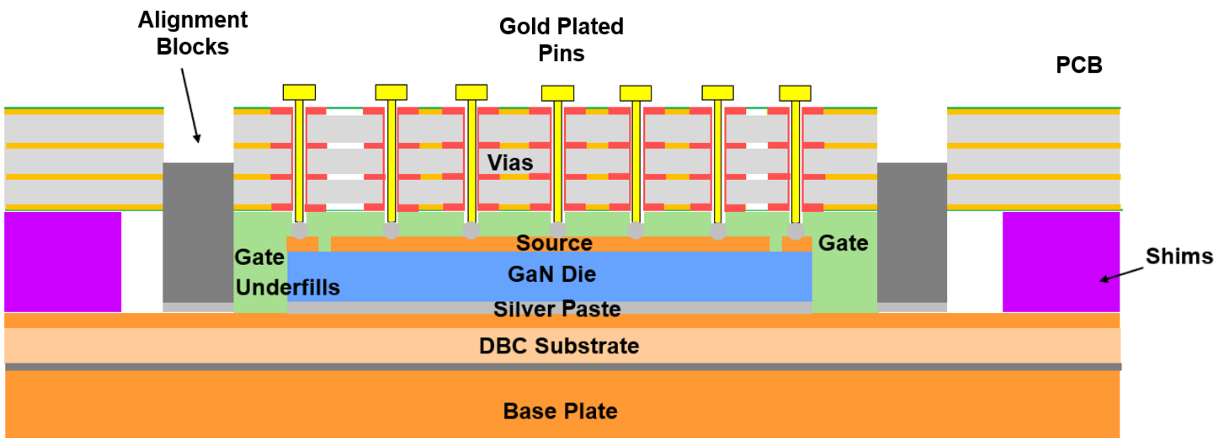


Fig. 2-5. The cross-sectional view of the embedded package for the single GaN HEMT in Fig. 2-3.

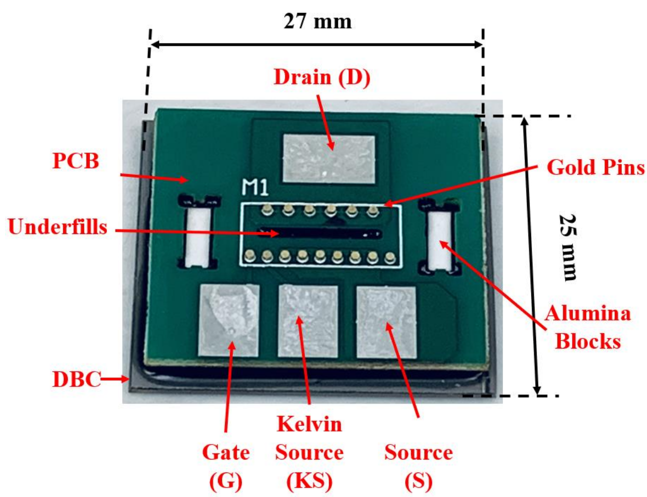


Fig. 2-6. The fabricated embedded package discussed in Fig. 2-5.

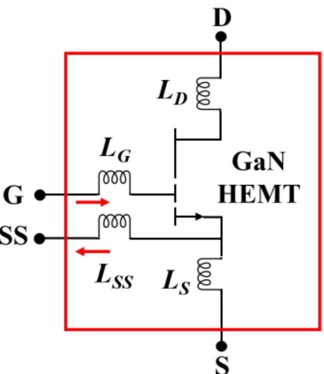


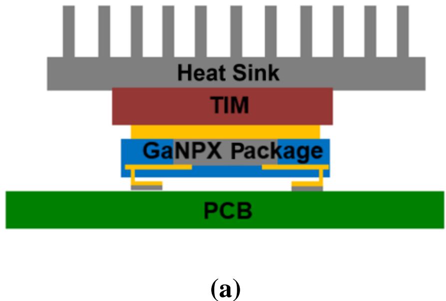
Fig. 2-7. Circuit diagram of the single chip GaN HEMT package in Fig. 2-5 with parasitic inductances labeled.

Table 2-1. Values of the simulated parasitic inductances in Fig. 2-7.

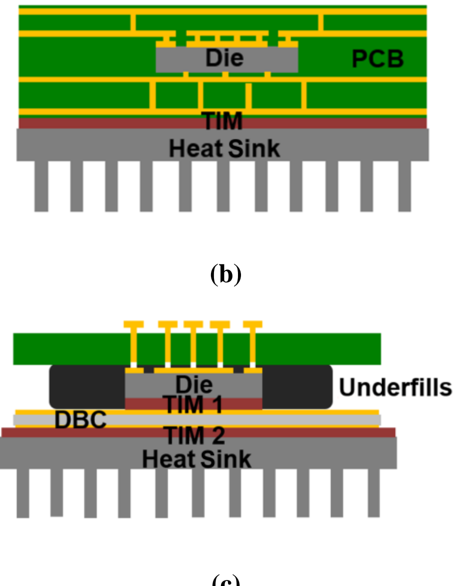
	L_D	L_S	L_G	L_{SS}
Simulated Inductance Values (nH)	0.55	0.65	1.83	1.83

First, all the interconnections are vertical and integrated into the top of the PCB. Therefore, the parasitic inductances can be controlled to be very small. On the bottom side, the DBC substrate used in this package offers electrical insulation and a low-resistance path for heat flow from the

die. The use of sintered silver for die bonding and interconnection provides reliable joints. In addition, it eases the assembly process and improves heat extraction because the sintered silver has a thermal conductivity of over 100 W/mK. To know the relative thermal performance of this package, FEA thermal simulations have been run using an ANSYS Icepak on this package, a GaN Systems's GaN_{PX}-type package, and on a typical PCB-embedded package reported in other research [32]. A schematic of the structure model created for the GaN_{PX} package is shown in Fig. 2-8(a). The GaN HEMT die is sandwiched between an interconnect PCB and a metal substrate. Since the metal substrate is not electrically isolated in the GaN_{PX} package, a relatively thick dielectric thermal interface material is needed between the pad and heat sink for cooling through the thermal pad. This work followed the company recommendation for the simulation by selecting Gapfiller-GS3500S35-07 as the interface material with a layer thickness of 17 µm. Fig. 2-8(b) is a schematic of the structure model of a PCB-embedded package consisting of a die inserted between the second and third layers of copper in a four-layer PCB. Heat extraction from the die is achieved through thermal vias in the PCB. Fig. 2-8(c) is a schematic of the structure model of this PCB-interposer-on-DBC package. A lead-free solder of 50-µm thick was utilized to bond the DBC substrate to the heat sink.



(a)

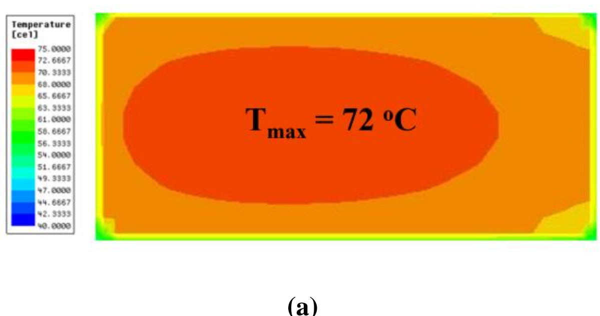


(b)

(c)

Fig. 2-8. Schematic of the structure model of a package based on: (a) the GaN Systems's GaN$_{PX}$ technology; (b) a typical PCB-embedded package; and (c) the PCB-interposer-on-DBC package in this work. In Fig. 2-8(c), Both TIM 1 and TIM 2 can be high-thermal-conductivity solder or sintered silver. However, in Fig. 2-8(a) and (b), the TIM must provide insulation. Hence, they have a low thermal conductivity.

All three packages simulated were assumed to have the exact same dimensions. They were all self-heated with a power of 20 W. The heating power was determined based on the chip loss for an application in [42]. The heat sink was the same for all, and the airflow rate was assumed to be at 3 m/s. Shown in Fig. 2-9(a), (b), and (c) are the simulated steady-state temperature profiles of the three packages, respectively.



(a)

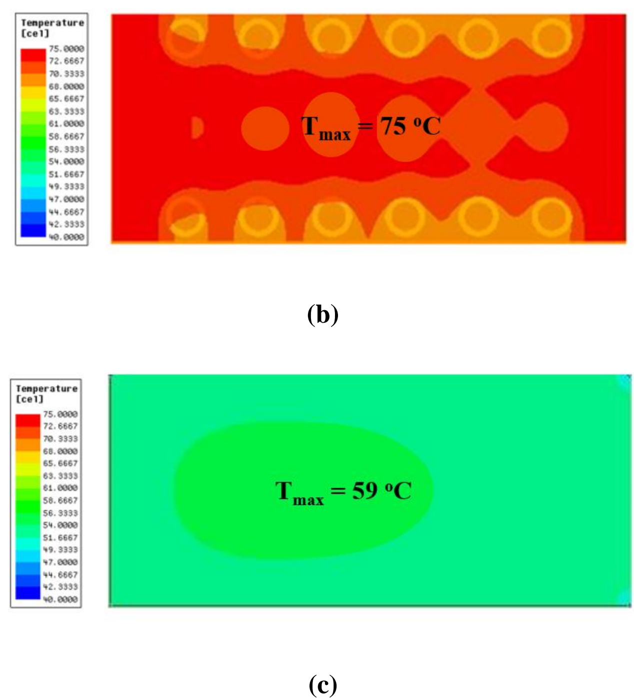


Fig. 2-9. Results of the simulated steady-state temperature profile over die surface of: (a) Fig. 2-8. (a); (b) Fig. 2-8. (b); and (c) Fig. 2-8. (c). The heating power was set to be 20 W. Air cooling with 3 m/s was applied to all the three structures.

The maximum temperature in this dissertation's package was 13 degrees lower than that in the GaN_{PX}-type package and 16 degrees lower than that in the PCB-embedded package. The primary reason for the better thermal performance of this package is due to the thinner thermal interface material and its higher thermal conductivity. Additionally, this package's junction-to-case thermal resistance (R_{thJC}) was measured and found it to be 0.14 ^{o}C/W.

To fabricate the PCB-interposer package for 650-V, 120-A eGaN HEMT bare die, an AlN DBC (from Rogers Corporation) was selected as the substrate due to its good thermal conductivity. In order to align the PCB with the bare die, 1-mm thick ceramic alignment blocks were used to fix the location of the die. Before sintering, the location of the die and the alignment blocks were fixed and attached to the DBC by using nanosilver paste (from NBE Tech, LLC.). Sterling silver shims were also sintered to the DBC substrate. After sintering, the functional PCB with slots was aligned with

the die. Gold-plated pins were inserted into the vias in the PCB and attached to the die's gold pads by a silver-sintering paste. After sintering the pins, the die, PCB, and DBC were bonded together and encapsulated using an underfill polymeric material. After injecting the underfills, the heads of the pins were soldered to the functional PCB. The processing procedure is shown in Fig. 2-10. Fig. 2-11 shows the final package after trimming off the alignment region and testing pads.

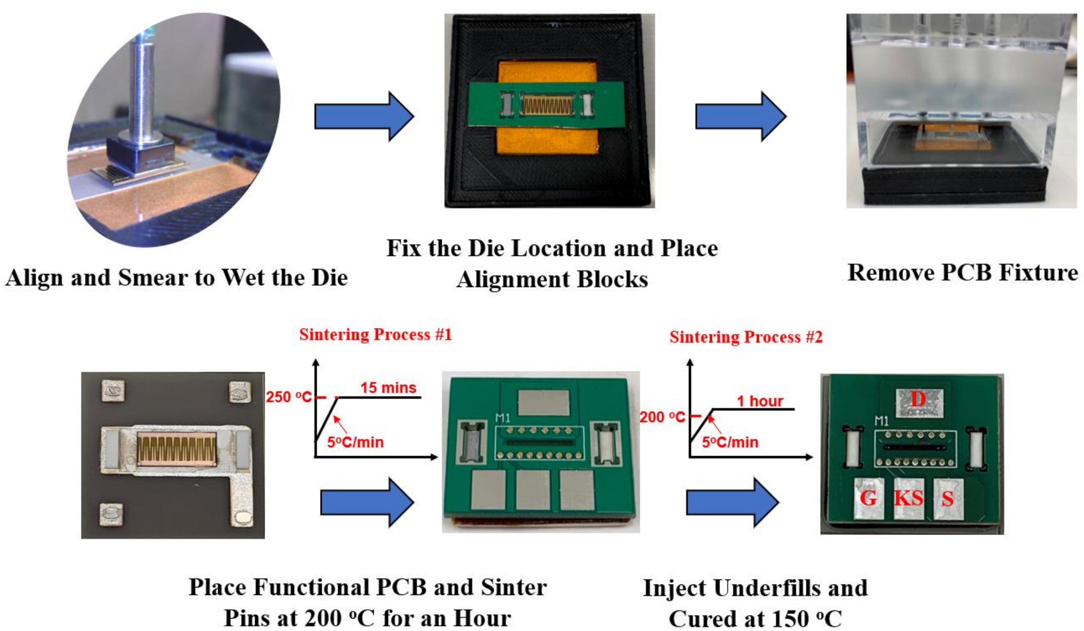


Fig. 2-10. The fabrication process of the PCB-interposer-on-DBC package in Fig. 2-6. The alignment blocks and the die were fixed by a PCB fixture and sintered on an etched DBC. The functional PCB was guided by the alignment blocks and aligns the pins to the die's bonding pads.

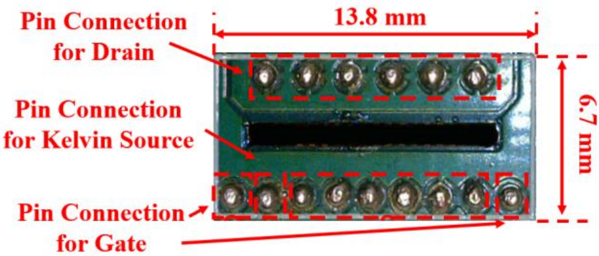
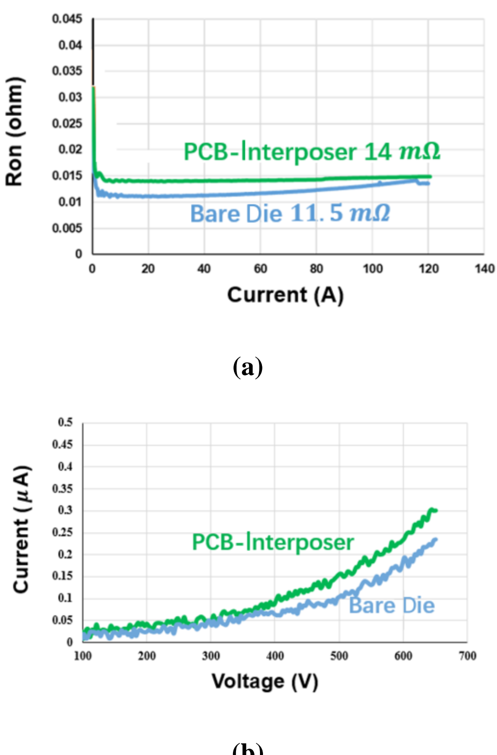


Fig. 2-11. PCB-interposer-on-DBC package after trimming off the alignment region and testing pads of the package in Fig. 2-6.

The fabricated packages were tested for static characteristics using a curve tracer. Fig. 2-13(a) and (b) show the on-resistance, R_{on}, and leakage current measurement results. The I_D vs. V_{DS} and I_D vs. V_{GS} characteristics are shown in Fig. 2-14(a) and (b). The PCB-interposer package added a small resistance from the interconnect pins and sintered joints, while the leakage current was almost the same compared to that from the bare die. The overall static I-V characteristics of the package were similar to those on the bare die.



(a)

(b)

Fig. 2-12. (a) Measured R_{on} of the bare die in Fig. 2-3 and the package in Fig. 2-6; and (b) measured leakage current of the bare die in Fig. 2-3 and the package in Fig. 2-6. For R_{on} measurement, V_{GS} is set to be +6 V to fully turn on the switch. For leakage current measurement, V_{GS} is set to be -4 V to make sure the switch is off. The measurement error is within 1 μΩ.

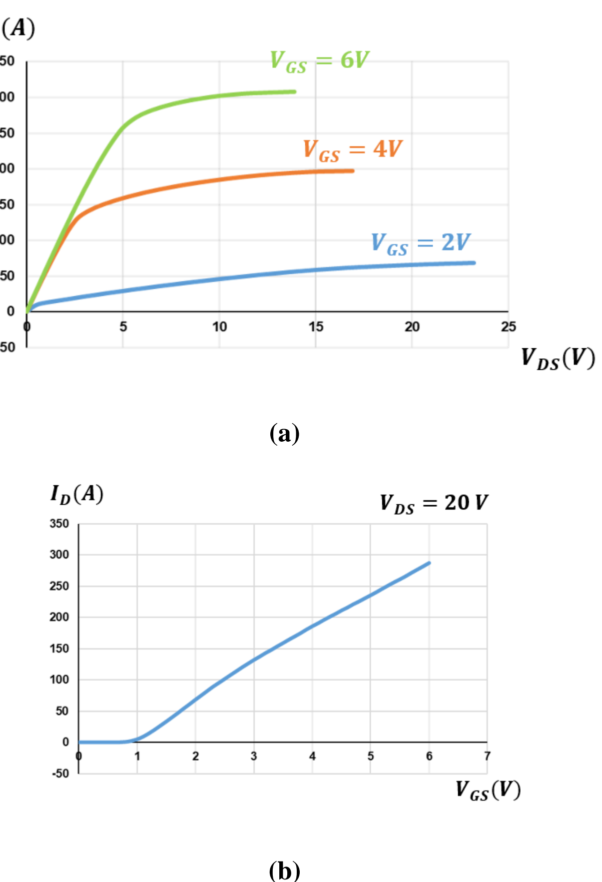


Fig. 2-13. (a) Measured I_D vs.V_{DS} of the package in Fig. 2-6; and (b) measured I_D vs.V_{GS} of the package in Fig. 2-6.

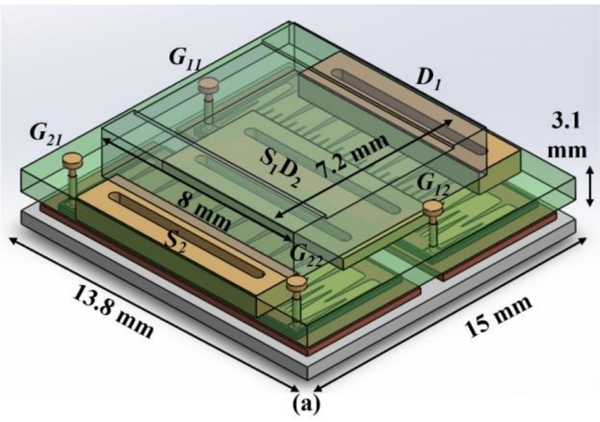
2.4 Embedded Packaging of GaN HEMT Half-Bridge Module

2.4.1 Single-Sided Cooling GaN HEMT Module

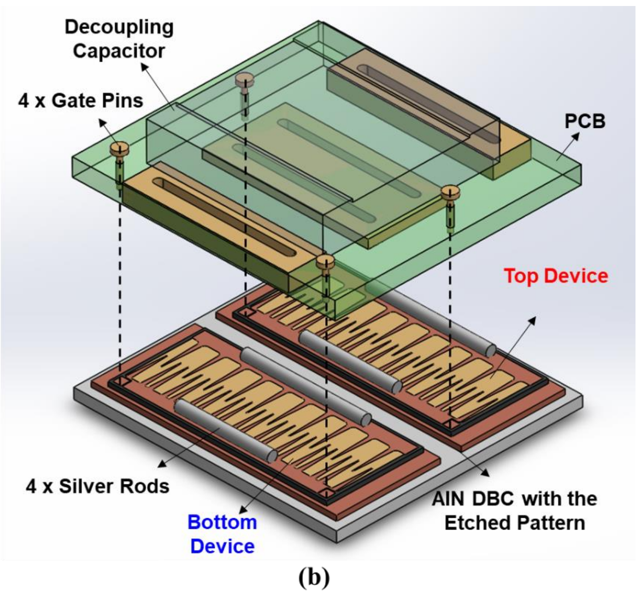
2.4.1.1 Package Layout Design

This section extends the GaN HEMT packaging technique in the previous section to half-bridge modules. In order to further reduce parasitic resistances and inductances, a single-sided cooling GaN HEMT half-bridge module is demonstrated in this section. Fig. 2-14(a) is a three-dimensional (3D) model of the half-bridge module, and (b) is its exploded view. Fig. 2-15 is a cross-sectional schematic of the half-bridge module layout. The module consists of two eGaN chips connected

between an AlN DBC substrate and a PCB. The sandwich structure is similar to that of the single-die package discussed in the previous section. However, unlike the previous package, short segments of silver rods are utilized for joining the drain and source pads on the chips to plated-through slots and metal patterns in the PCB. Replacing the pins with rods reduces mutual parasitic inductance and increases current-handing capability and thermal performance. Since the silver rods have very small inductance, the Kelvin source pins are removed to improve yield. Gate pins still connect the gate pads through pre-drilled holes in the PCB. The PCB not only serves for interconnecting the terminals but also for mounting decouple capacitors across the source of the top chip and the drain of the bottom chip, resulting in a shorter power loop. The PCB is aligned to the chips by matching the PCB openings to alumina studs on the DBC. Metal shims on the DBC control the gap spacing between the PCB and the chips. The chip manufacturer recommends shorting the chip's silicon substrate to its source pad to avoid the back-gate effect and to reduce its dynamic on-resistance [43, 44]. This is achieved through a metal trace in the PCB that connects the source to the metal shim. Die-attachment and connections to the bare chips are achieved by silver-sintering instead of soldering to improve bonding reliability and facilitate module assembly that requires multiple heating/cooling steps.



(a)



(b)

Fig. 2-14. (a) Three-dimensional view of the single-sided cooling half-bridge module; and (b) exploded view of the module.

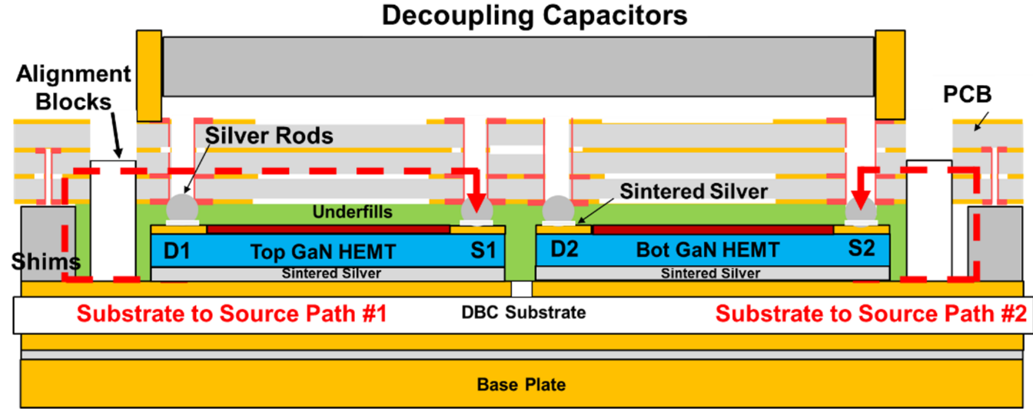


Fig. 2-15. A cross-sectional diagram of the single-sided cooling half-bridge module in Fig. 2-14.

2.4.1.2 Parasitic Extraction

Fig. 2-16 is the circuit diagram of the half-bridge module showing the various parasitic inductances. Fig. 2-17 shows where these parasitic inductances are located in the package from Fig. 2-14. All the parasitic inductances in Fig. 2-16 were simulated using an ANSYS Q3D

Extractor and are listed in Table 2-2. The parasitic inductances, L_{D1}, L_{CS1}, and L_{CS2} are the inductances of the silver rods, which are all 0.07 nH. L_{G1} and L_{G2} are gate-pin inductances, which are 1.83 nH. The power-loop inductance, L_{power} is the sum of package inductances, decoupling capacitor inductance, and bare chip inductance. The loop is from one side of the decoupling capacitor to the other side. At 100 MHz, the power-loop inductance is 1.122 nH -- sufficiently small for use in MHz converters.

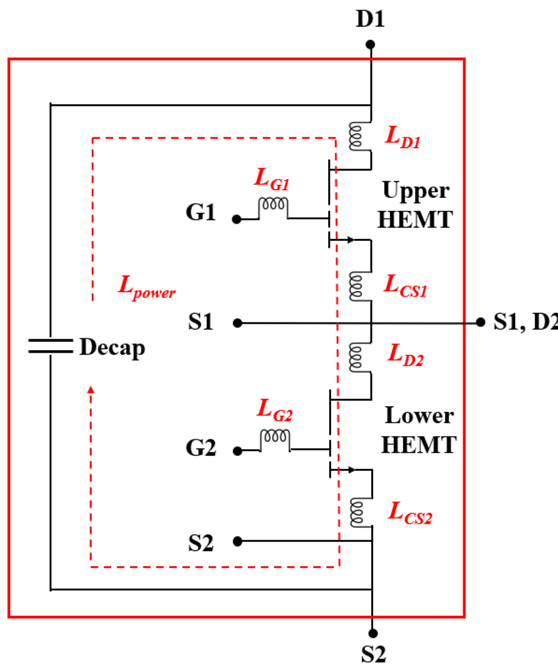


Fig. 2-16. Circuit diagram of the half-bridge module from Fig. 2-14 including parasitic inductances.

Fig. 2-17. Parasitic inductances depicted in Fig. 2-16 of the module in Fig. 2-14. Gate pin inductance is not shown here.

Table 2-2. Values of the simulated parasitic inductances in Fig. 2-16.

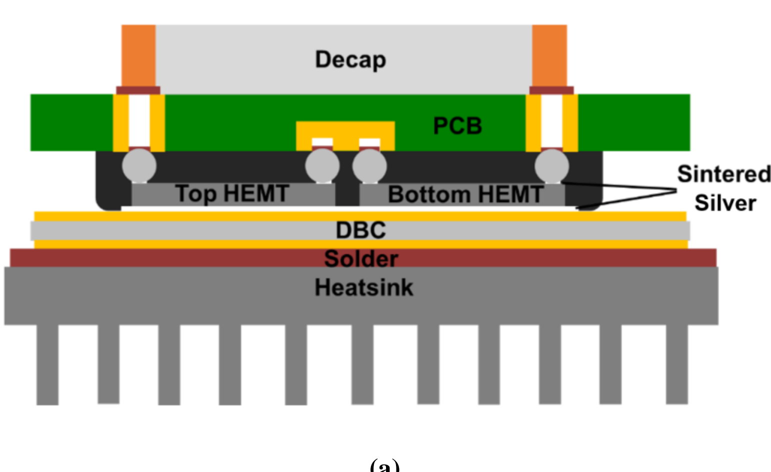
	L_{D1}	L_{CS1} or L_{CS2}	L_{D2}	L_{G1} or L_{G2}	L_{power}
Simulated Inductance Values (nH)	0.07	0.07	0.29	1.83	1.122

2.4.1.3 Thermal Simulation

Heat extraction of the package in Fig. 2-15 is by one-sided cooling through the bottom copper plane of the DBC substrate. Because the middle ceramic layer of the substrate provides electrical isolation of the chips, the module can be directly mounted on a heat sink using a TIM with high thermal conductivity, such as a lead-free solder (k = 52 W/mK). Fig. 2-18(a) is a design for cooling the module by soldering its substrate directly on a pin-fin heatsink. The design of Fig. 2-18(a) was simulated in COMSOL Multiphysics to evaluate the thermal performance of the module. For comparison, using the same pin-fin structure for cooling, the thermal performance of the half-

bridge modules was also simulated using GaN Systems's HEMT package or the GaN_{PX} package and modules based on a PCB-embedded structure modeled after [40].

The simulated structure for the GaN_{PX} package is depicted in Fig. 2-18(b) [45]. It is a flip-chip configuration with all three chip terminals connected by soldering to a PCB. The thermal pads of both chips are attached to the pin-fin heatsink through a dielectric TIM for electrical isolation. The chip manufacturer's recommendation was to select a TIM, Gapfiller-GS3500S35-07, 178-µm thick from Henkel. Moreover, the junction-to-case thermal resistance, R_{thJC}, of the chip package needed for the thermal simulation was taken from its datasheet. As for the simulated structure of the PCB-embedded package shown in Fig. 2-18(c), the PCB is a 2s2p board (13.6 mm × 13.6 mm) with 1 oz copper. The bare dice are buried between the second and the third copper layers. The multiple micro-vias in the PCB are machined and electroplated with copper for access to the chips, the terminals on one side for electrical connection, and the thermal pads on the other side for heat dissipation. Again, as required for electrical isolation, the same TIM used for the GaN_{PX} package was also used for the PCB-embedded package.



(a)

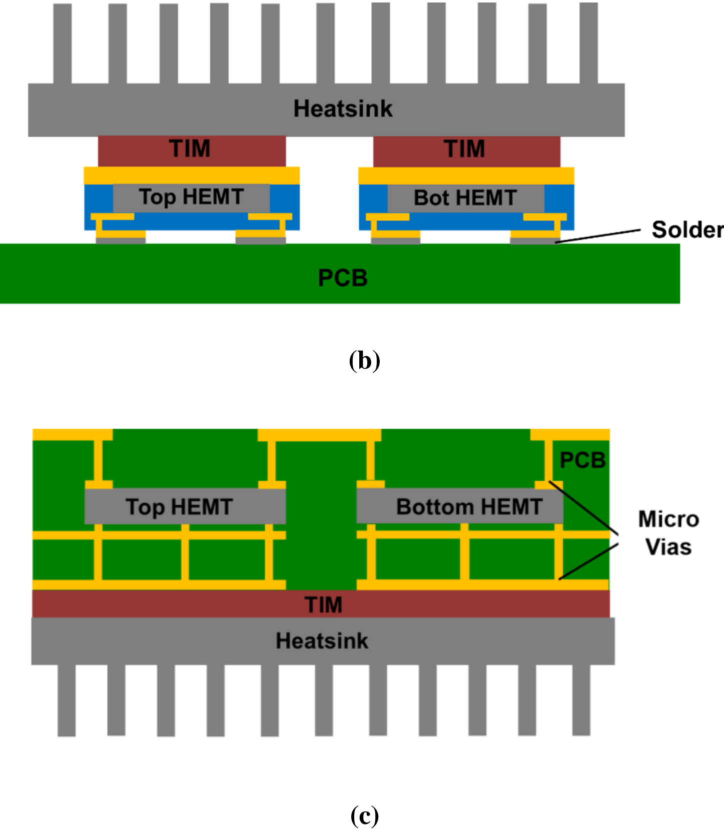


Fig. 2-18. (a) Simulated structure for the half-bridge module package in Fig.1; (b) simulated structure for a half-bridge module made with GaN System's GaN_{PX} package; and (c) simulated structure for a PCB-embedded GaN half-bridge module. In Fig. 2-18(a), both solder and sintered silver have high thermal conductivity. However, in Fig. 2-18(b) and (c), the TIM must provide insulation. Hence, they have a low thermal conductivity.

To ensure a fair comparison, the three structures were assumed to have the same dimensions. Each of the chips was assumed to generate a heat power of 20 W under an operation at 400 V and 60 A [42]. Results of the simulated junction-to-case thermal resistance (R_{thJC}) and junction-to-ambient thermal resistance (R_{thJA}) for each cooling structure are summarized in Table 2-1. Plotted in Fig. 2-20 are the chip junction temperature versus heat transfer coefficient for the three cooling structures. The steady-state temperature distributions in the three cooling structures of Fig. 2-19(a), (b), and (c) -- all at a heat transfer coefficient of 3000 W/m^{2}K -- are plotted in Fig. 2- 21(a), (b), and (c), respectively. The module package of this work has a maximum temperature that is 22.2

°C lower than that in the GaN_{PX}-type package, or 25.2 °C lower than that in the PCB-embedded package.

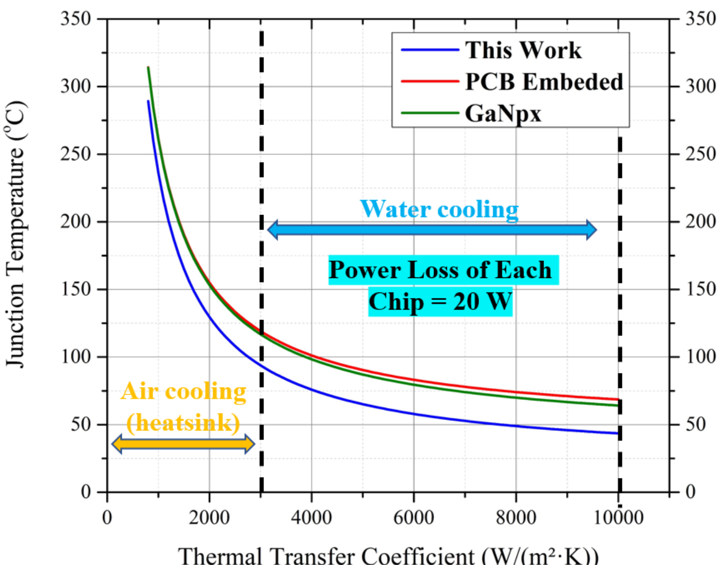
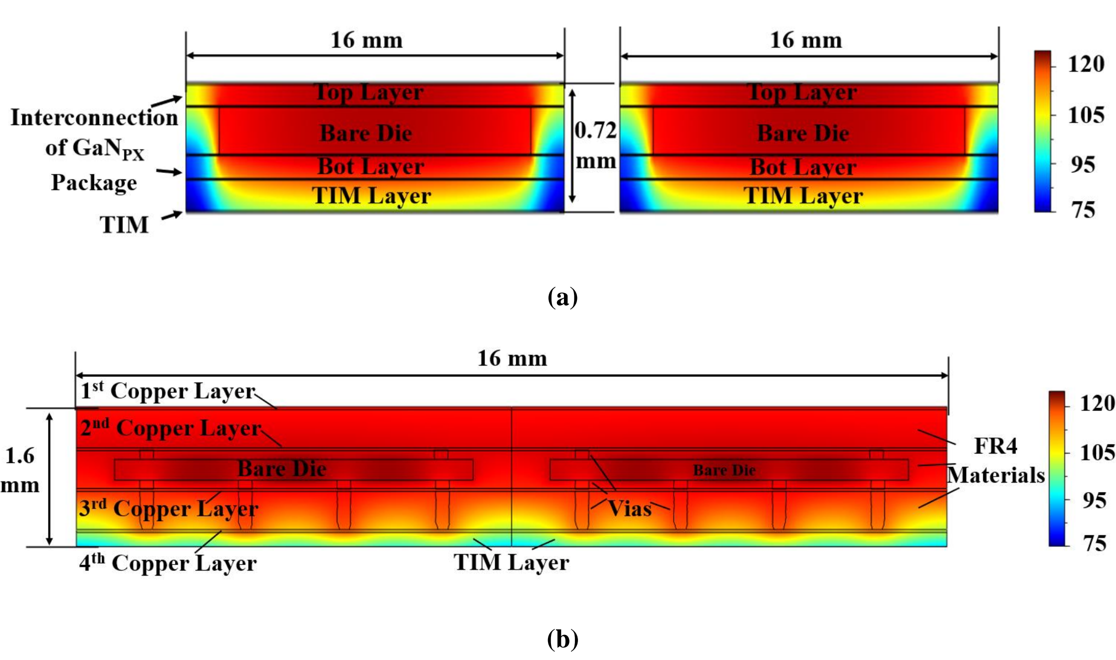
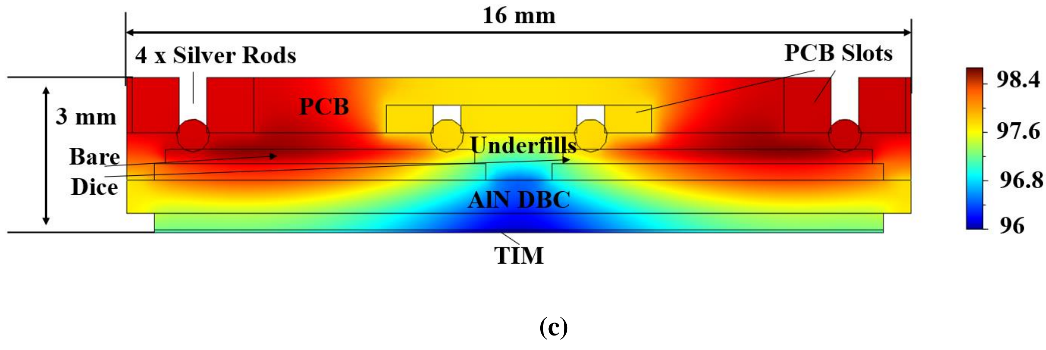


Fig. 2-19. Plots of junction temperature versus thermal transfer coefficient for the three different structures in Fig. 2-18.





(c)

Fig. 2- 20. (a) Temperature distribution of the structure in Fig. 2-19(a); (b) temperature distribution of the structure in Fig. 2-19(b); and (c) temperature distribution of the structure in Fig. 2-19(c).

Table 2-3. Simulated thermal resistances of the three cooling structures.

Simulated Structure (Module+Heatsink)	Junction-to-Case Thermal Resistance, $R_{\theta JC}$ (°C/W)	Junction-to-Ambient Thermal Resistance, $R_{\theta JA}$ (°C/W)
Our Half-Bridge Module	0.099	1.902
GaN_{PX} Module	0.144	2.421
PCB-Embedded Module	0.458	2.550

2.4.1.4 Module Fabrication

Bare dice of GaN Systems's 650-V, 10-mΩ (150-A) eGaN HEMTs (GS-065-150-1-D) were purchased from the company. The backside or thermal-pad side has a silver surface finish, which is suitable for die-attach by silver-sintering. The bonding pads on the three terminals of the chip have a copper surface finish, which is also compatible with silver-sintering of a pressure-less sintering paste (NanoTach®: X Series) from NBE Technologies. The fabrication process for the half-bridge module is shown in Fig. 2-22. Because of their excellent thermal conductivity (up to 230 W/mK), AlN DBC substrates with a silver surface finish from Rogers Corporation were used for building the module. Patterning of the DBC substrates was done by chemical etching. Placement of the dice, and alignment of the alumina studs and silver shims on the substrate, were

guided by a PCB fixture. After removing the fixture, the dice, studs, and shims were bonded on the substrate by pressureless sintering at 250 ºC for 15 minutes. Then, short silver rods (0.85 mm in diameter) were soldered onto 0.5 mm open slots in a multilayer interconnect PCB, followed by flipping the PCB and mounting the rods on the source and drain pads of the chips. The gate pads were connected to the PCB by gold-plated pins dropped through the via holes in the board. The alignment of the rods and pins to the chip bonding pads was aided by the alignment blocks on the substate and corresponding openings in the PCB. And they were bonded by silver-sintering at 200 ºC for an hour. The shims on the substrate were soldered on the PCB for shorting each of the thermal pads to its corresponding source pad. The shims also served to level the board. The empty space between the DBC substrate and the PCB was filled with an underfill (ME-531 from LORD Corporation), which provided electrical insulation and improved both the structural integrity and the thermo-mechanical reliability [46-48].

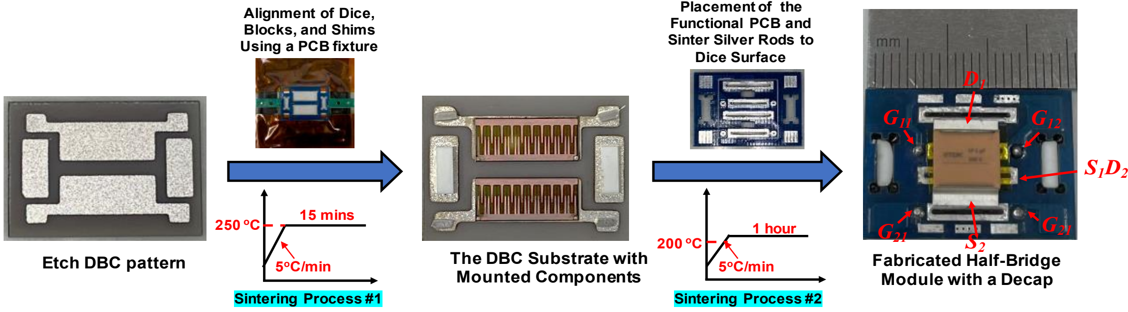


Fig. 2-21. The fabrication process of the single-sided cooling half-bridge module in Fig. 2-14.

2.4.1.5 Electrical Static Characterization

Static characteristics of the fabricated half-bridge modules and those of the bare dice were tested on a curve tracer. For testing the modules, electrical leads were soldered onto the various terminals

of the module and were then connected to the curve tracer. For testing the bare dice, a fixture consisting of a 3D-printed case and a PCB with pushpins and soldered leads was utilized, as shown in Fig. 2-23. Table 2-2 lists the average on-resistance and the leakage current of the two switches measured in the chip form and in the module. The on-resistances were measured at V_{GS} = 6 V, I_D = 40 A, and the leakage currents were measured at V_{GS} = - 4 V and V_{DS} = 650 V. On average, the interconnect and leads of the package added about 1 mΩ to the on-resistance of each switch. The leakage current of the packaged switch was about the same as that of the bare chip.

Table 2-4. Average on-resistance and leakage current from two devices measured in the chip form or in the package in Fig. 2-21.

	Average On-Resistance, R_{on}@ V_{GS} = 6V, R_{on} = 40 A	Average Leakage Current, I_D @ V_{GS} = - 4 V, V_{DS} = 650 V
Bare Die	10.5 mΩ	2.4 μA
Half-Bridge Module	11.5 mΩ	2.5 μA

Fig. 2-22. A fixture made for testing the bare die in Fig. 2-3 on a curve tracer.

2.4.1.5 Electrical Dynamic Characterization

Fig. 2-23(a) shows a double-pulse test (DPT) board for measuring the dynamic characteristics of the half-bridge modules, and (b) is the power-loop design of the board. In the test, the top GaN HEMT switch was used for freewheeling. As shown in Fig. 2-24, the decoupling capacitor was

detached to connect the module to the DPT testing board, and the half-bridge module was soldered to the DPT board as a surface-mounted device (SMD). The specifications of the components in the test are shown in Table 2-5. Before the test, the parasitic parameters of the DPT setup were simulated in an ANSYS Q3D Extractor. The test-circuit schematic with parasitic capacitors and inductors is shown in Fig. 2-26, and Table 2-3 lists the values of the extracted parameters.

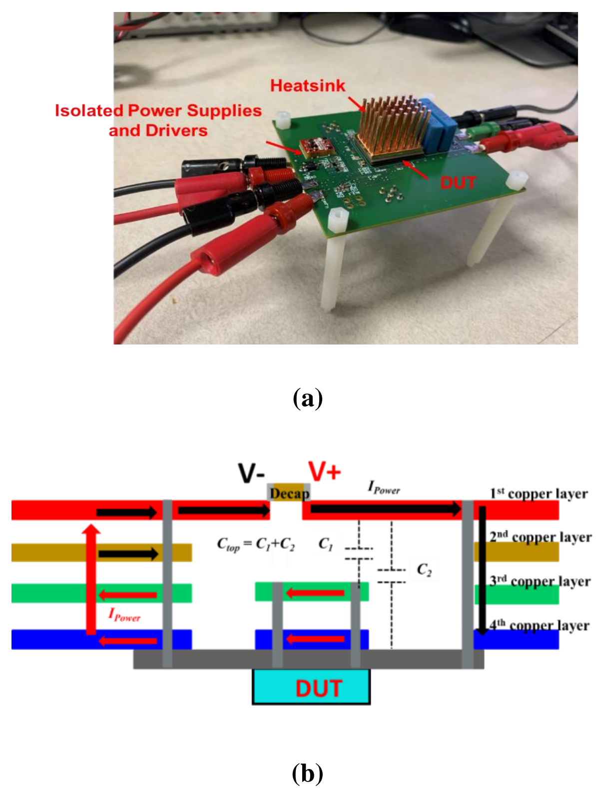


Fig. 2-23. (a) Double-pulse test board for characterizing the dynamics of the single-sided cooling half-bridge module in Fig. 2-21; and (b) power loop design for DPT board in Fig. 2-23(a).

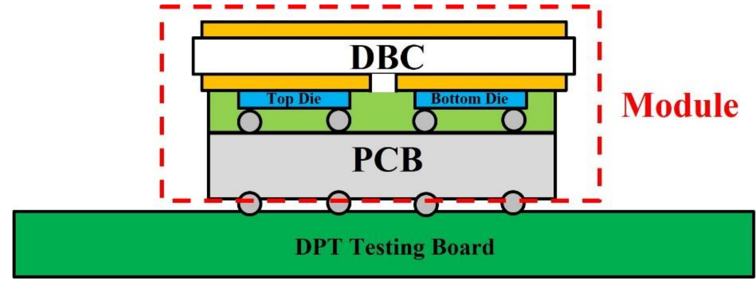


Fig. 2-24. Schematic of the DPT setup in Fig. 2-23.

Table 2-5. Component values of the DPT Setup in Fig. 2-23.

Names	Descriptions	Values
DC-Link Capacitor, C_{DClink}	Electrolytic Capacitor	10 µF
Decoupling Capacitor, C_{de}	Ceramic Capacitor	1.8 µF
DPT Inductor, L_{DPT}	UI Core Inductor	50 µH
Turn-on Gate Resistor, R_{gon}	Surface-Mount Resistor	10 Ω
Turn-off Gate Resistor, R_{goff}	Surface-Mount Resistor	2 Ω
Gate Driver	Si8271	NA

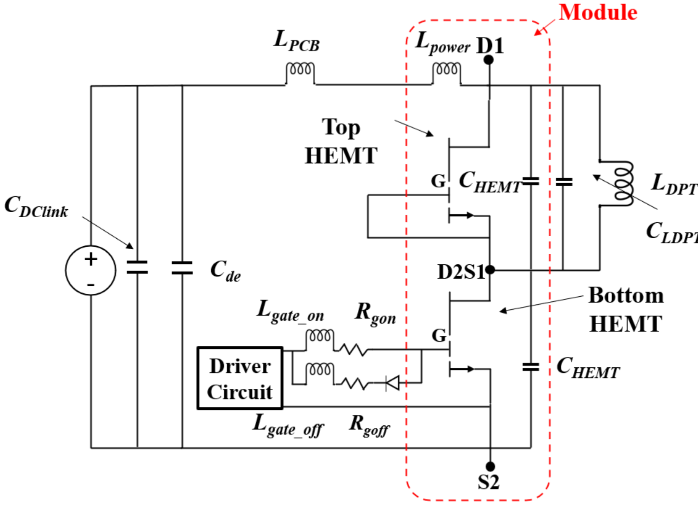


Fig. 2-25. The DPT test circuit diagram with simplified parasitic inductances. L_{power} is the sum of package inductances in Fig. 2-17. Since the decoupling capacitor is removed, the total power loop inductances, $L_{powerloop}$ is the sum of package inductances, L_{power} and PCB trace inductance, L_{PCB} in the DPT testing board in Fig. 2-23.

Table 2-6. ANSYS Q3D extracted values of the parasitic inductances and capacitances of the DPT setup in Fig. 2-23.

Circuit Element	Value
PCB Trace Inductance in Power Loop, L_{PCB}	1.85 nH
Module Inductance in Power Loop, L_{power}	1.12 nH
Power-Loop Inductance in the DPT Setup, $L_{power} + L_{PCB}$	2.97 nH
Gate-Turn-on Inductance + PCB Traces, $L_{turn\text{-}on}$	3.51 nH
Gate-Turn-off Inductance + PCB Traces, $L_{turn\text{-}off}$	3.00 nH
HEMT Capacitance, C_{HEMT}	373 pF
PCB Capacitance in Parallel With Top HEMT, C_{top}	3.35 pF

Fig. 2-27(a) illustrates the experimental DPT waveforms of V_{GS}, V_{DS}, and inductor current (I_L) obtained at 25 ºC ambient, and Fig. 2-27(b) and (c) are the detailed waveforms for turn-on and turn-off, respectively. In the turn-off period, the power-loop inductance of the DPT setup, $L_{powerloop,}$ resonated with the bottom HEMT's output capacitance, $C_{HEMT,}$ and the PCB parasitic capacitance, C_{top}. So, the total power loop inductance can be calculated as:

$$L_{powerloop} = \frac{T^2}{4\pi(C_{HEMT} + C_{top})} , \quad (2\text{-}1)$$

where T is the ringing period, C_{HEMT} is the output capacitance of the top GaN HEMT, and C_{top} is the parasitic capacitance of the DPT test board in parallel with C_{HEMT} in Fig. 2-23(b). It is calculated to be 3.45 nH, a sum of the module inductance and the DPT board inductance. This value is close to the simulated result of 2.97 nH. The difference may be attributed to the parasitic inductance of the decoupling capacitors and slight inaccuracy in measuring the ringing period. The half-bridge module was able to switch at 400 V, 90 A with only 17 V voltage overshoot and at a dv/dt up to 42.67 V/ns.

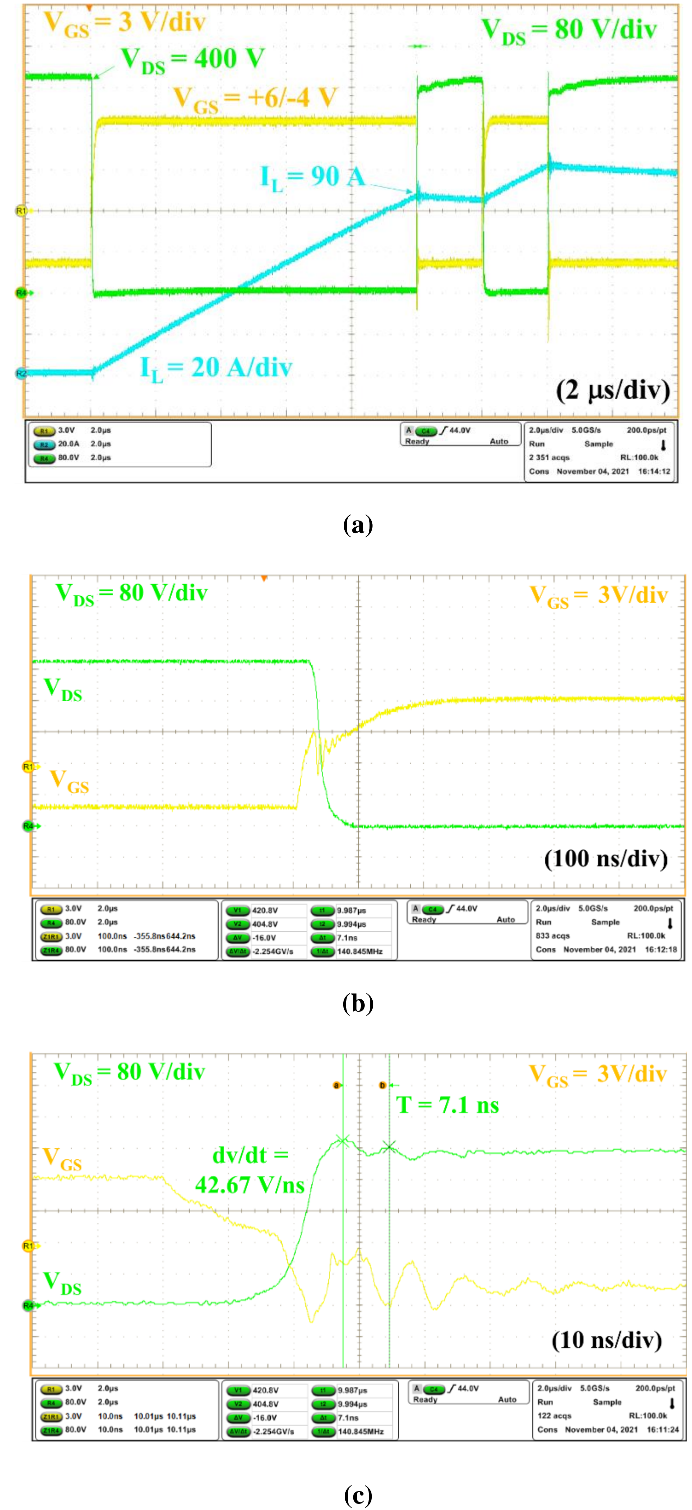


Fig. 2-26. (a) DPT waveform of the single-sided cooling half-bridge module in Fig. 2-21;(b) detailed turn-on waveform of the module in Fig. 2-21; and (c) detailed turn-off waveform of the module in Fig. 2-21.

2.4.2 Double-Sided Cooling GaN HEMT Module

2.4.1.1 Motivation and Challenges

The single-sided cooling GaN HEMT module has low loop inductance and thermal resistance. However, thermal management is still a challenge when pushing to higher-current applications. The system requires a more efficient cooling system to maintain a cool working temperature at a higher loss. This issue could increase the cooling system size, total cost, and design effort. A double-sided cooling packaging technique is introduced to increase the cooling efficiency for power modules while maintaining a similar power density.

The double-sided cooling concept introduces a second heat flow path for a power module, so that heat generated inside the module can be extracted in two heat flow paths, as shown in Fig. 2-27 [39, 49-51]. In this way, the total junction-to-case thermal resistance is two separate thermal resistances in parallel. In Fig. 2-28, the traditional double-sided cooling structure for the half-bridge module has dice substrates attached to the same DBC. The top side is connected via metal posts (interposers) to the other DBC. As a result, the cooling efficiency can be increased by 30% to 70% percent based on the contact area between the die's top surface and the interposer. However, unlike Si or SiC switches, GaN HEMTs are lateral switches with gate, drain, and source pads on the top RDL layers. Therefore, insulation must be applied to the top layer to isolate the bonding pads. As a result, the total metal area on the top side of a GaN HEMT bare die is limited to 20% to 30% of the total die surface area. Typically, the junction-to-top-RDL thermal resistance of a GaN HEMT bare chip is two times larger than the junction-to-bottom-Si-substrate thermal resistance. This makes the cooling from the top RDL side less efficient.

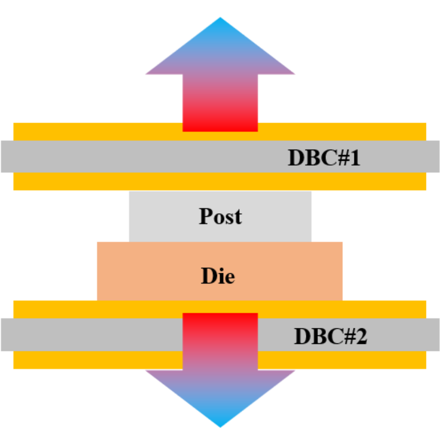


Fig. 2-27. The typical package layout for a double-sided cooling package.

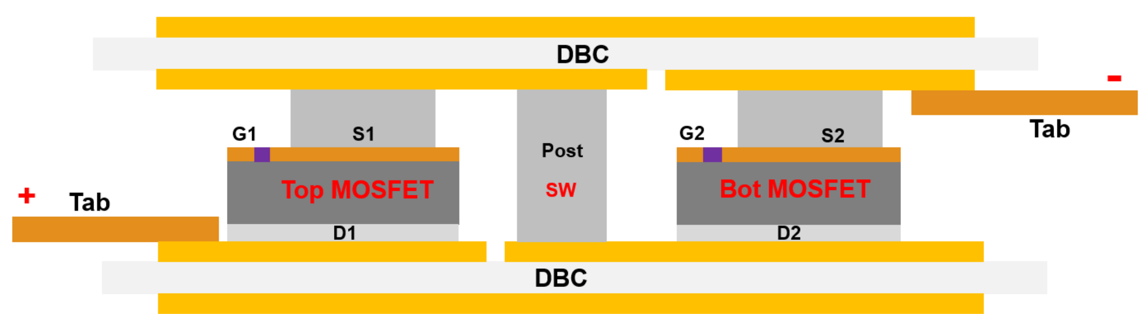


Fig. 2-28. Traditional double-sided cooling layout for t*he* half-bridge module using MOSFETs.

The traditional double-sided cooling structure for a GaN HEMT is shown in Fig. 2-31. To avoid the backgate effect, the substrate of each die is connected to the source by a metal interposer. Because of the small bonding pads, it is hard to find proper interposers for interconnection and heat dissipation. In [38], GaN HEMTs were directly soldered between the top and bottom ceramic substrates without any interposers. However, there are some limitations. First, the structure is rigid without interposers. There is no buffer for stress relief. Second, the solder's reliability is a concern when it is to be used for die-attachment and interconnection from bare die bonding pads. Third,

the total footprint area of the module is limited by the summation of two dice areas and two interposers' areas.

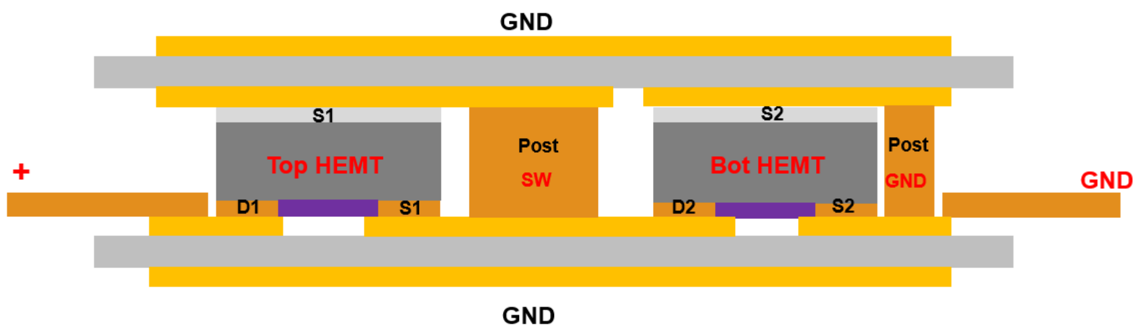


Fig. 2-29. Traditional double-sided cooling layout for the half-bridge module using GaN HEMTs (gate pads are not drawn in the figure).

2.4.1.2 Package Layout Design

Fig. 2-30(a) and (b) introduce a layout with a die-stacking structure to tackle the design challenges. Its cross-sectional view is shown in Fig. 2-33. The top HEMT is stacked on the bottom HEMT with silver rods as interposers in the vertical direction to reduce the footprint area. In this structure, a third DBC is introduced to insulate the top HEMT's drain pad and bottom HEMT's source pad. Meanwhile, to connect from the top HEMT's source pad to the bottom HEMT's drain pad, a silver block interposer is embedded in the third DBC. Decoupling capacitors are integrated to shorten the power loop inductance in the half-bridge module, and the power loop is inside the module. Also, each HEMT is on different DBC substrates to improve cooling efficiency, and the lowest thermal impedance path is utilized.

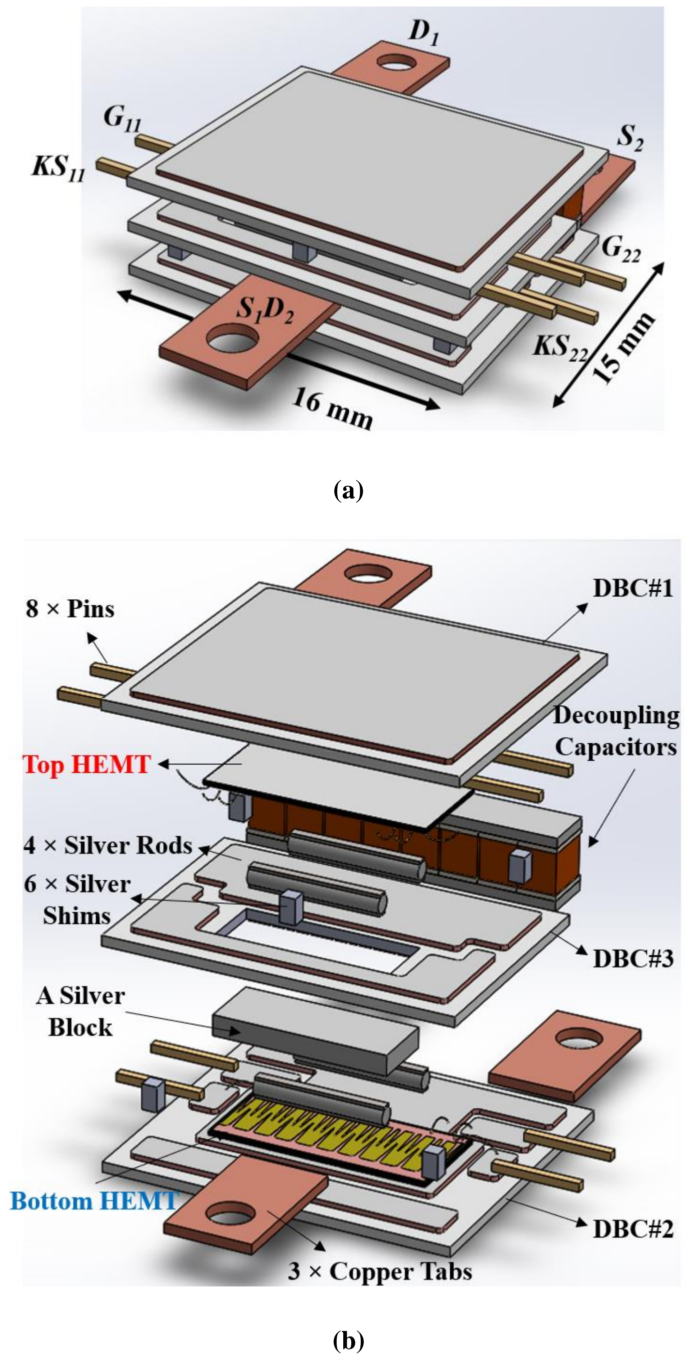


Fig. 2-30. (a) Three-dimensional view of the double-sided cooling half-bridge module; and (b) exploded view of the module.

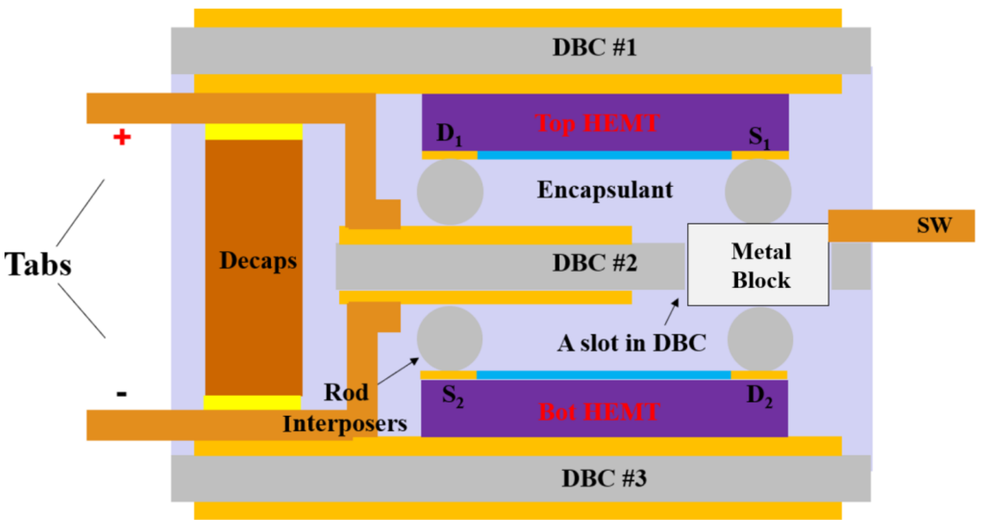


Fig. 2-31. Cross-sectional view of the double-sided cooling half-bridge module in Fig. 2-30.

2.4.1.3 Parasitic Extraction

The circuit diagram of the double-sided cooling half-bridge module is shown in Fig. 2-32. Gate and Kelvin source connections are through 2-mil gold bond wires connected to DBC copper patterns. Fig. 2-33 shows where these parasitic inductances are located in the package shown in Fig. 2-30. All the parasitic inductances were simulated using an ANSYS Q3D Extractor, and these values are listed in Table 2-7. The parasitic inductances, L_{D1} and $L_{S2,}$ are the inductances of silver rods, which are all 0.07 nH. L_{D2} is the summation of two silver-rod inductances and a silver-block inductance, 0.09 nH. L_{G1} and L_{G2} are gate-bond-wire inductances, which are 1.83 nH. The power-loop inductance, $L_{power,}$ is the summation of package inductances, DBC trace inductance, L_{DBC_trace}, decoupling capacitor inductance, and bare chip inductance. The loop is from one side of the decoupling capacitor to the other side. At 100 MHz, the power-loop inductance is 1.347 nH, which is sufficiently small for use in MHz converters.

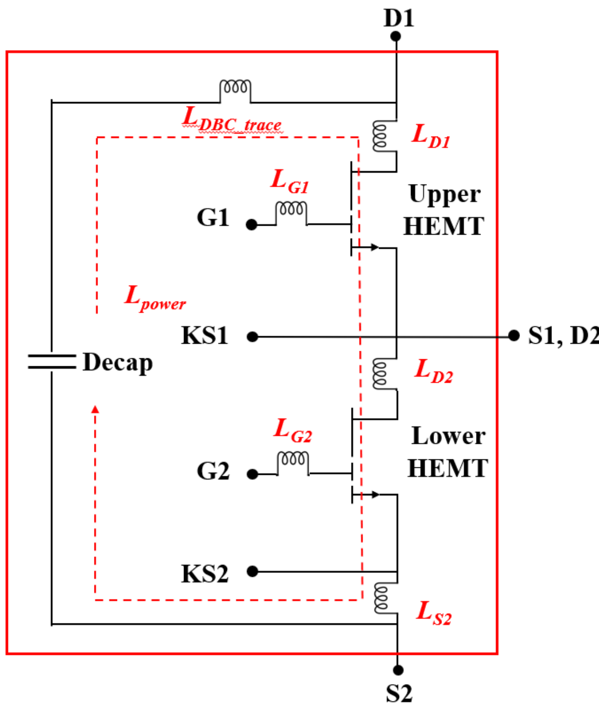


Fig. 2-32. Circuit diagram of the double-sided cooling half-bridge module in Fig. 2-30 including parasitic inductances.

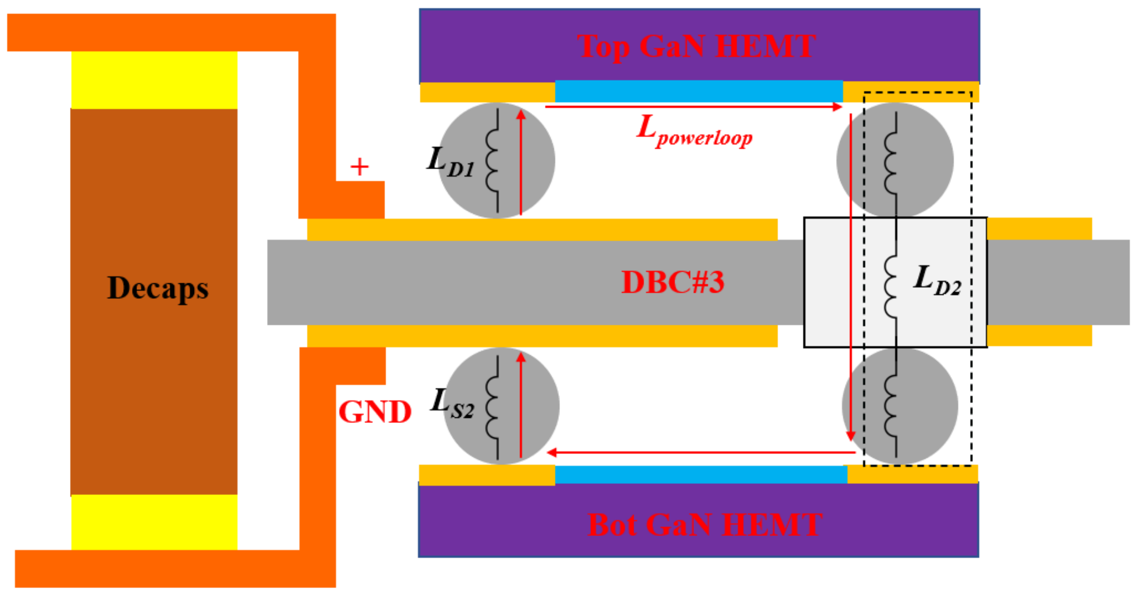


Fig. 2-33. Parasitic inductances depicted in Fig. 2-32 of the module Fig. 2-30. Gate bond wire inductance is not shown here.

Table 2-7. Values of the simulated parasitic inductances from Fig. 2-32.

	L_{D1} or L_{S2}	L_{D2}	L_{G1} or L_{G2}	L_{power}
Simulated Parasitic Inductances (nH)	**0.09**	**0.57**	**3.92**	**1.347**

2.4.2.4 Thermal Simulation

Heat extraction of the package in Fig. 2-30 is by double-sided cooling through the top and bottom copper plane of the DBC substrate. The module can be directly mounted on two heat sinks using a TIM with high thermal conductivity, such as a lead-free solder. Fig. 2-34 is a design for cooling the module by soldering its substrate directly on a pin-fin heatsink. To evaluate the thermal performance of the proposed module structure, the design of Fig. 2-34 was simulated in COMSOL Multiphysics.

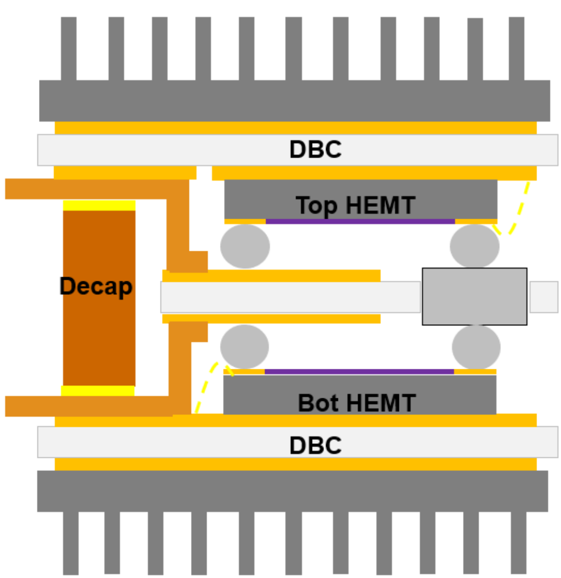


Fig. 2-34. Simulated structure for the DSC half-bridge module package in Fig. 2-30.

The simulated junction-to-case thermal resistance (R_{thJC}) and junction-to-ambient thermal resistance (R_{thJA}) results for each cooling structure are summarized in Table 2-8. Fig. 2-35 illustrates the module junction temperature versus heat transfer coefficient for the double-sided cooling module and single-sided cooling half-bridge module in the previous subsection. The steady-state temperature distribution in the double-sided cooling module of Fig. 2-34 -- at a heat transfer coefficient of 3000 W/m^{2}K -- is plotted in Fig. 2-36. The double-sided cooling (DSC) module has a 46 ^{o}C lower junction temperature than that in the single-sided cooling (SSC) half-bridge module.

Table 2-8. Simulated thermal resistances of the two proposed structures in Fig. 2-14 and Fig. 2-30.

Simulated Structure (Module + Heatsink)	Junction-to-Case Thermal Resistance, R_{thJC} (^{o}C/W)	Junction-to-Ambient Thermal Resistance, R_{thJA} (^{o}C/W)
SSC Half-Bridge Module	0.099	1.902
DSC Half-Bridge Module	0.060	0.675

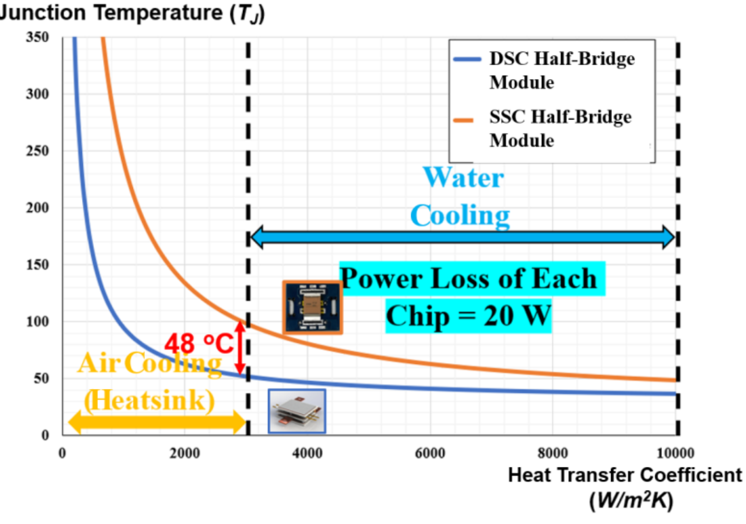


Fig. 2-35. Plots of junction temperature versus thermal transfer coefficient for the single-sided cooling module in Fig. 2-14 and the double-sided cooling module in Fig. 2-30.

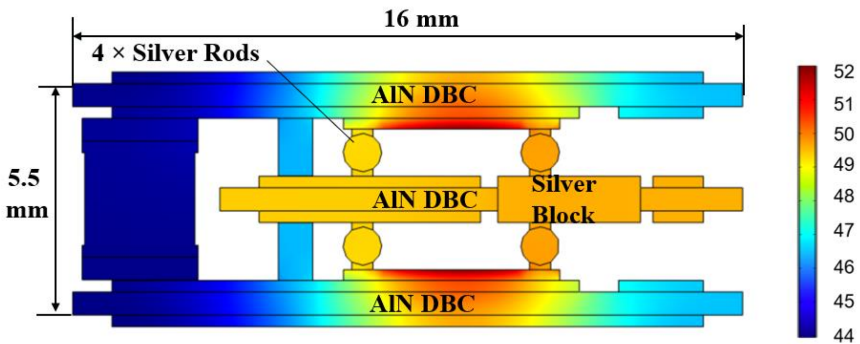


Fig. 2-36. Temperature distribution of the structure in Fig. 2-34.

2.4.2.5 Module Fabrication

The fabrication process for the half-bridge module is shown in Fig. 2-37. First, the top and bottom AlN DBC substrates were designed and etched. Then, the bare dice were sintered on different DBC substrates at 250 ^{o}C for 15 minutes. Since the die's surface finish is copper, it got oxidized during the sintering process. First, a low concentration of chlorhydric acid was used to clean the copper oxide. Next, distilled water was used for flushing away the residue. Later, silver rod interposers, gate-pins, Kelvin-source-pins, decoupling capacitors, terminal tabs, and silver shims were soldered on the top and bottom DBC in nitrogen at 320 ^{o}C by high-lead solder (Sn10/Pb88/Ag2). After soldering, 2-mil gold wires were used to connect the dies' gates and Kelvin source bonding pads to DBC copper patterns.

Meanwhile, the middle DBC was prepared. First, a slot was cut inside the middle DBC by laser. Next, a silver block was buried in the slot, and a power tab was also soldered to the middle DBC. Next, the three DBCs were assembled with lead-free solder (Sn96.3/Ag3.7). Finally, the space between the three DBC substrates was filled with an underfill (ME-531 from LORD Corporation) for encapsulation.

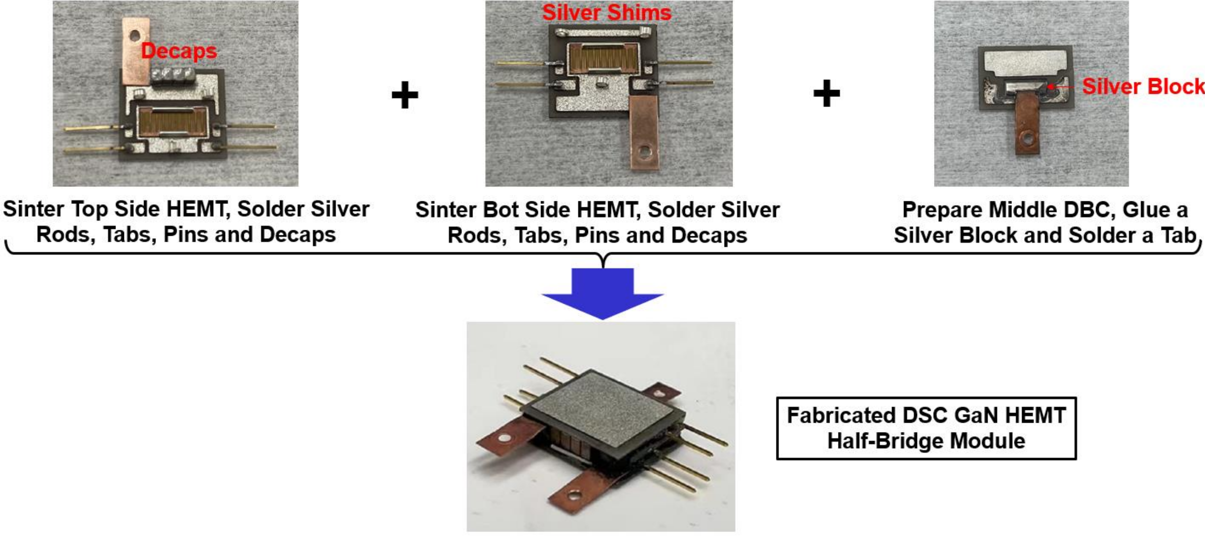


Fig. 2-37. The fabrication process of the double-sided cooling half-bridge module in Fig. 2-30.

2.4.2.6 Electrical Static Characterization

Static characteristics of the double-sided cooling half-bridge modules and those of the bare dice were tested on a curve tracer. The testing condition is the same as that in the previous subsection. Table 2-9 lists the average on-resistance and the leakage current of the two switches measured in the chip form and the module.

Table 2-9. Average on-resistance and leakage current from two switches measured in the chip form or in the DSC half-bridge module.

	Average On-Resistance, R_{on}@ V_{GS} = 6V, R_{on} = 40 A	Average Leakage Current I_D @ V_{GS} = - 4 V, V_{DS} = 650 V
Bare Die	10.5 mΩ	2.4 μA
DSC Half-Bridge Module Top Device	10.8 mΩ	2.8 μA
DSC Half-Bridge Module Bot Device	11.6 mΩ	3.1 μA

2.5 Chapter Summary

Embedded packaging techniques were applied for commercial (650-V, 10-mΩ, 150-A) eGaN HEMTs. First, a PCB-interposer-on-DBC package is developed for a single GaN HEMT switch. Gold-plated pins were used for all the interconnections from the die's bonding pads. Then, to increase the integration level and shorten loop inductance, single-sided cooling and double-sided cooling half-bridge modules were introduced. Silver rods replaced gold-plated pins for drain and source interconnections to reduce parasitic inductances and resistances. As for the single-sided cooling half-bridge module, the power-loop inductance can be reduced to 1.122 ^{o}C/W. PCB was used on the top side for interconnections to silver rods, which also allows the power supply and gate driver integration. With the stacked-die architecture, the footprint can be reduced to 70% for a double-sided cooling module, and the junction-to-case thermal resistance can be reduced to 0.079 ^{o}C/W. Fig. 2-38 summarizes all the embedded packages in this chapter.

	Packages	L_{power} (nH)	R_{thJC} (^{o}C/W)	R_{on} (mΩ)	$I_{leakage}$(mA)	Features
	Single-Sided Cooling: Single Device Package	0.562×2 + traces > 2	0.153	12.5	< 3	One Device With All Pin Connections
	Single-Sided Cooling: Half-Bridge Module	1.122	0.099	11	< 3	Driver Integration
	Double-Sided Cooling: Half-Bridge Module	1.347	0.079	11.5	< 3	Smallest R_{thJC}

Fig. 2-38. Summary of the embedded packages in Fig. 2-5, Fig. 2-14, and Fig. 2-30.

Chapter 3 Junction-to-Case Thermal Resistance Measurement of the Embedded Packages

3.1 Introduction of the R_{thJC} Measurement for GaN HEMTs

As discussed in the second chapter, embedded packages have been developed for GaN HEMTs. In the meantime, experimental verification of the thermal simulations is also key to ensuring a package development's success. The major challenge of measuring the R_{thJC} of a GaN package is the lack of accurate techniques to determine the switch's junction temperature, T_J.

Although techniques for direct measurement of T_J have been developed [52, 53], a more widely practiced technique for measuring T_J is through one of the switch's temperature-sensitive electrical parameters (TSEPs) [54-59], such as the threshold voltage (V_{th}), gate leakage current (I_g), drain current (I_d), or on-resistance (R_{on}). For Si and SiC power switches, the temperature dependence of any of the TSEPs is strong and well-characterized. Furthermore, one can follow the IEEE JESD51-14 standard [60] to accurately measure the R_{thJC} of the package. However, the common TSEPs of a GaN HEMT lack sufficient sensitivity or stability due to the charge-trapping effect [23, 24] from switching action. In [61, 62], the researchers recently fabricated GaN HEMT switches with two gate pads. They showed that the gate end-to-end or gate-to-gate electrical resistance, R_{g2g}, can be used as a reliable TSEP. However, because they did not fabricate packages for their switches, they did not apply the technique to measure R_{thJC}.

In this chapter, in Section 2, the methodology of the R_{thJC} measurement technique is introduced. Two techniques were combined to improve the accuracy: (1) using R_{g2g} as the TSEP and (2)

making multiple thermal resistance measurements with stacked layers of a thermal interface material (TIM). The stacked-TIM technique was employed to reduce inaccuracy in determining the package case temperature. Then, in Section 3, a standard wire-bonding package using the eGaN chip in Chapter 2 was first fabricated to verify the R_{thJC} measurement technique. R_{g2g} of the package was a sensitive and stable parameter for measuring T_J. Then, a procedure is presented for determining the package R_{thJC} by extrapolating thermal resistance data measured at different layers of TIM. Validation of the procedure is demonstrated from measurements obtained using two different TIMs and the results of FEA thermal simulations. Then, the embedded packages discussed in Chapter 2 were also tested for R_{thJC} to verify their thermal performances. Finally, Section 4 summarizes the proposed R_{thJC} measurement technique for GaN HEMT packages.

3.2 R_{thJC} Measurement Methodologies

3.2.1 Junction Temperature Determination

As discussed in the previous section, TSEPs are commonly used for determining the junction temperature of power switches. To compare the proposed R_{g2g} as a TSEP with the common TSEPs of Si and SiC switches, threshold voltage (V_{th}), forward voltage drop (V_{sd} or V_F), and on-resistance (R_{on}) of the packaged GaN HEMTs were also characterized. V_{th} was the gate-source voltage measured at I_D = 10 mA. V_{sd} (V_F) was the voltage drop across the switch when operating in the third quadrant at 10 mA. R_{on} was measured at V_{GS} = 6 V and I_D = 40 A by a curve tracer. The three major factors considered in the comparison were: sensitivity, immunity to electron trapping, and online capability. For a fair comparison of the sensitivity, all the units of the TSEPs were converted to mV/^{o}C. The raw and converted results are shown in Table 3-1. The TSEP of V_{th} is the least sensitive. A shift in V_{th}, as high as 0.5 V, was also observed upon switching, and this is likely the

result of electron trapping or hole accumulation/depletion. This issue makes V_{th} an unreliable TSEP for measuring T_J. Since GaN HEMTs have no built-in body diodes, V_{sd} is similar to V_{th} in the HEMT structure, and thus is also influenced by electron trapping. R_{on} is the most sensitive TSEP and is also capable of online T_J measurement. However, it can be influenced by electron trapping during switching actions. The TSEP of R_{g2g} has good sensitivity. Furthermore, it is immune to electron trapping because it is simply the resistance of a copper trace in the switch structure. Thus, it is also a good TSEP for online measurement.

Table 3-1. Comparison of different temperature-sensitive electrical parameters.

TSEP	V_{th}	V_{sd} (V_F)	R_{on}	R_{g2g}
Raw Sensitivity	0.2 mV/°C	0.35 mV/°C	13.75 mΩ/°C	4.7 mΩ/°C
Converted Sensitivity in mW/°C	0.2 mV/°C	0.35 mV/°C	0.55 mV/°C	0.24 mV/°C
Immunity to Electron Trapping	No	No	No	Yes
Online T_J Capability	No	No	Yes	Yes

3.2.2 Stacked-TIM Technique

Another requirement for accurate measurement of R_{thJC} is accurate measurement of the case temperature, T_C. The procedure prescribed in the JEDEC standard suggests making a hole or a groove in the heatsink for embedding a thermocouple. However, the non-uniform distribution of the case temperature and a large temperature gradient between the case and heatsink makes it challenging to accurately measure the case temperature. Therefore, the transient dual interface measurement (TDIM) technique was proposed in [63] to avoid the T_C measurement error. With this technique, R_{thJC} is determined by finding the point of deviation between two transient cooling curves or structure-function plots measured using different interface materials between the

package and the heatsink. However, the transient heat flow inside the package may differ from the steady-state heat flow. So, the TDIM result is not an accurate measure of R_{thJC}, which is defined under a thermal steady-state condition. Furthermore, the TDIM result is influenced by subjective decisions, e.g., offset correction and determination of the deviation location in the structure-function plots [64].

To remove the influence of T_C measurement on the steady-state R_{thJC} measurement, this work introduces the stacked-TIM technique. The technique involves making multiple thermal resistance measurements with varying numbers of layers of a TIM stacked between a package and a heatsink. Fig. 3-1(a) is a schematic showing a GaN package clamped to a heatsink with a few layers of a TIM in between. A buffer layer, which can be a TIM layer, is placed on top of the heatsink. A thermocouple is embedded between the buffer layer and the TIM stack. To ensure good thermal contact and minimal temperature measurement error, the thermocouple bead should be small, at least five times smaller than the buffer layer thickness. The thermocouple measures the temperature of the bottom surface of the TIM stack, labeled as T_{TIM}.

As the package is heated to a thermal steady state from the power dissipated by the channel, T_{TIM} is measured by the thermocouple, and T_J is determined from R_{g2g} steady-state thermal resistance from the switch junction to the bottom surface of the TIM stack, R_{thJTIM} is found by:

$$\mathcal{R}_{thJTIM} = \mathcal{R}_{thJC} + \mathcal{R}_{thCTIM} = \frac{T_J - T_{TIM}}{P} , \tag{3-1}$$

where R_{thCTIM} is the case-to-TIM thermal resistance. By varying the number of layers in the TIM stack or the total thickness, t, of the stack, a plot of R_{thJTIM} versus t is obtained, like the one depicted in Fig. 3-1(b). At $t = 0$, $R_{thJTIM} = R_{thJC}$, and R_{thJC} can be obtained by extrapolating the

data plot to the y-axis. Because of the heat-spreading effect in the TIM stack, R_{thJTIM} (t) is a nonlinear function. Thus, one needs a nonlinear fitting curve of the data points to guide the extrapolation.

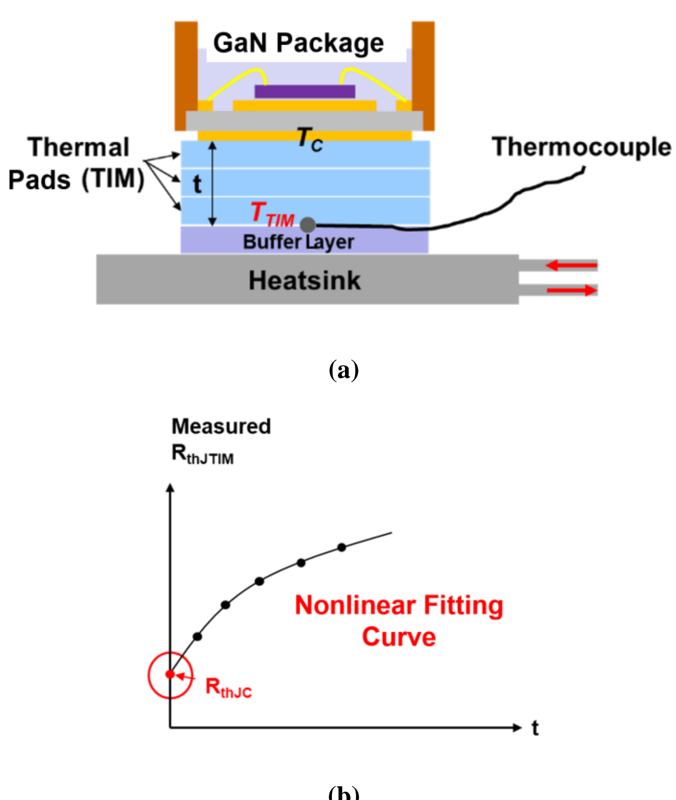


Fig. 3-1. (a) Schematic of the measurement setup with the stacked-TIM technique; and (b) depiction of R_{thJTIM} versus t plot with the nonlinear fitting curve for extracting R_{thJC}.

Fig. 3-2(a) and (b) show a simplified thermal model for finding an analytical expression for the fitting curve. Assuming a heat-spreading angle, θ, in the TIM stack, R_{thCTIM} in Eq. (1) is derived to be:

$$\mathcal{R}_{thCTIM} = \frac{1}{k} \cdot \int_0^{t0} \frac{\mathrm{d}t}{(x_1 + 2cot\theta \cdot t)(y_1 + 2cot\theta \cdot t)} , \qquad (3\text{-}2)$$

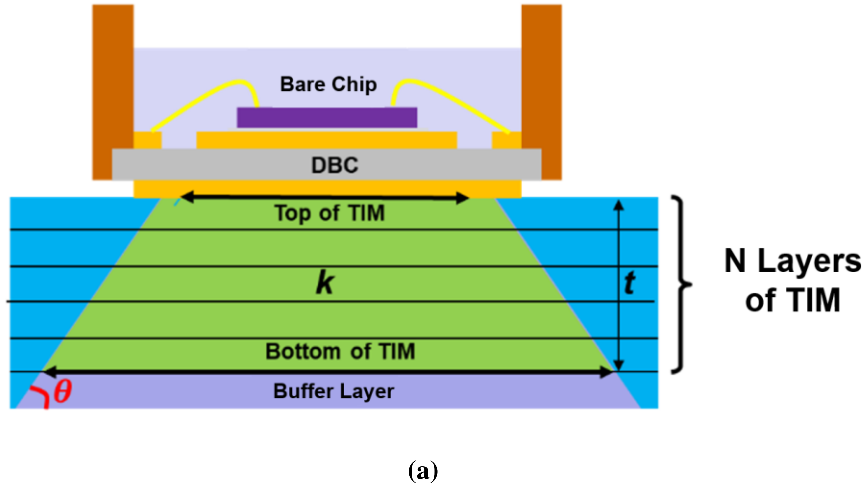
where k is the thermal conductivity of the TIM material, t_0 is the total thickness of the TIM stack, and (x_1, y_1) is (width, length) of the TIM area in direct contact with the package case. After the definite integration, R_{thJTIM} becomes:

$$\mathcal{R}_{thJTIM} = \frac{1}{k(y_1 - x_1)} \cdot \ln\left(\frac{t + \frac{x_0}{2cot\theta}}{t + \frac{y_0}{2cot\theta}} \cdot \frac{y_0}{x_0}\right) + \mathcal{R}_{thJC} \ , \tag{3-3}$$

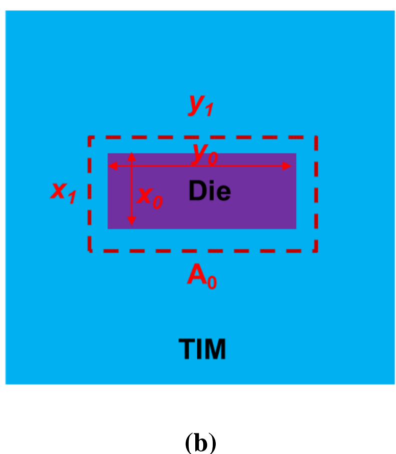
Thus, the nonlinear behavior of the R_{thJTIM} (t)fitting curve follows a natural log. And, the two unknowns, R_{thJC} and θ, can be obtained by fitting the data points to Eq. (3). However, the analytical function is cumbersome for data fitting. To simplify the following discussion, heat spreading is set at θ=45°, a reasonable assumption in a homogeneous substrate. Now, Eq. (3) becomes:

$$\mathcal{R}_{thJTIM} = a \cdot f(t) + \mathcal{R}_{thJC} \ , \tag{3-4}$$

where $a = \frac{1}{k}\frac{1}{y_0 - x_0}$, and $f(t) = \ ln \ \left(\frac{2t+x_0+2 \cdot t_{DBC}}{2t+y_0+2 \cdot t_{DBC}} \cdot \frac{y_0+2 \cdot t_{DBC}}{x_0+2 \cdot t_{DBC}}\right)$. (x_0, y_0) is (width, length) of the chip. The only unknown in Eq. (3) is $\mathcal{R}_{thJC}$, which can be readily obtained by fitting the data points to Eq. (4).



(a)



(b)

Fig. 3-2. A simple thermal model for deriving an analytical expression for the nonlinear fitting curve: (a) Cross-sectional view of heat spreading in the TIM stack; and (b) top view showing the dimensions of the die and the package case.

Fig. 3-3 is a flow chart summarizing the procedure for determining $\mathcal{R}_{thJC}$ by using R_{g2g} as the TSEP to measure T_j and the stacked-TIM technique to avoid inaccurate T_C measurement. In the chart, n is the number of layers of TIM in the TIM stack, $T_{TIM\#n}$ is the temperature at the bottom of the TIM stack with n number of layers, and $R_{thJTIM\#n}$ is the thermal resistance from junction to the bottom surface of the TIM stack with n number of layers.

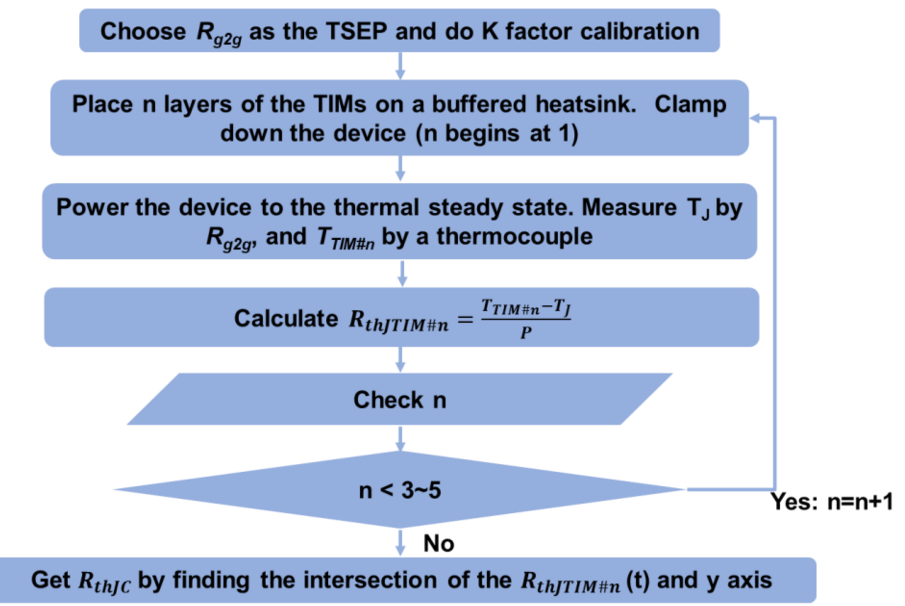
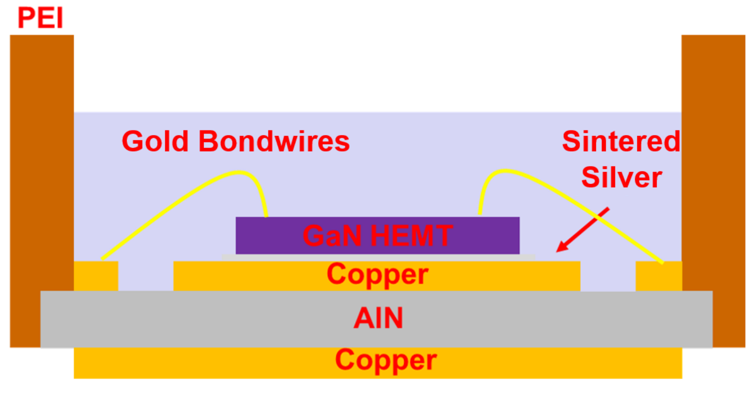


Fig. 3-3. A procedure for improved measurement of R_{thJC} of a GaN HEMT package using R_{g2g} as the TSEP and stacked-TIM technique to avoid inaccurate measurement of the case temperature.

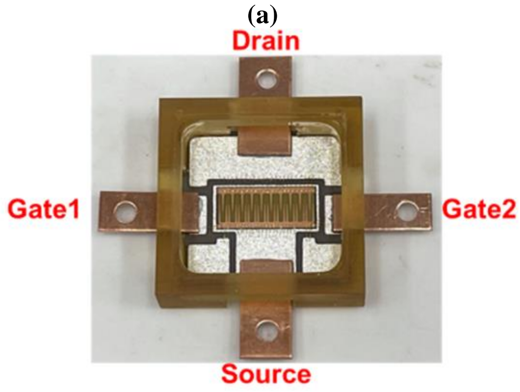
3.3 R_{thJC} Measurement of GaN HEMT Packages

3.3.1 A Custom Wire-Bonding GaN HEMT Package

The GaN HEMT chosen for this study is GaN Systems's Schottky type *p*-GaN gate HEMT rated for 650 V and 150 A with the part number GS-065-150-1-D. The die has two gate pads connected internally. Fig. 3-4(a) is a schematic of the cross-section of the package and (b) is the top view of a completed package. The GaN die was attached by silver sintering to a patterned DBC substrate with a silver surface finish, and a 2-mil gold wire connected the three terminals (gate, source, and drain) to the substrate. Copper leads were soldered to the DBC substrate for external connections. The housing for mechanical support was made of Duration® polyethyleneimine (PEI) from Mitsubishi Chemical Advanced Materials. The space inside the housing was filled with silicone (Nusil-2188 from Avantor) for insulation and protection.



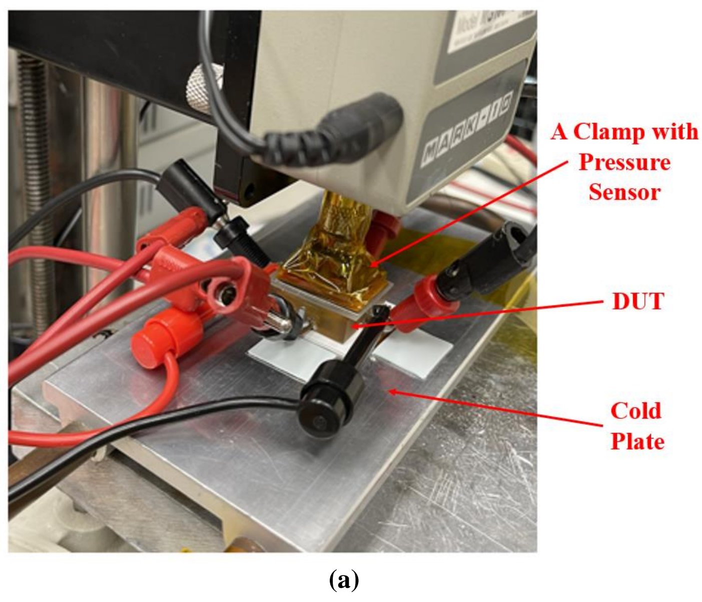
(a)



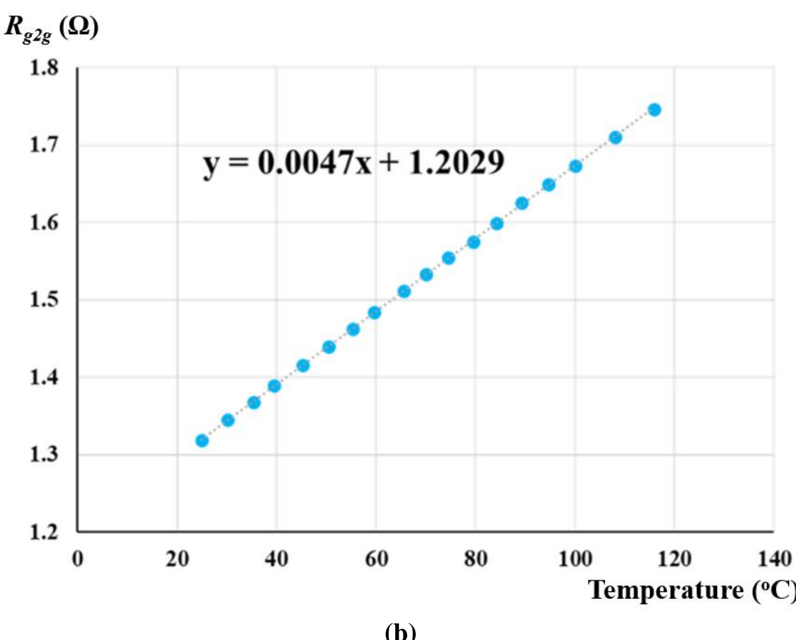
(b)

Fig. 3-4. (a) Schematic of the package cross-section; and (b) top view of a custom wire-bonding GaN package.

The measurement procedure described in the flow chart in Fig. 3-3 was used to determine the R_{thJC} of the GaN HEMT package in Fig. 3-4. The two gate leads of the package shown in Fig. 3-4(b) were purposely added for ease of characterizing R_{g2g} as a TSEP. Fig. 3-5(a) shows the experimental setup. The package was clamped to a hotplate with two layers of a TIM and a thermocouple in between. The gate-to-gate electrical resistance was measured by the four-point probe method at a constant current of 50 mA. The hotplate was heated from room temperature to 120 ^{o}C at increments of 5 ^{o}C, and R_{g2g} was recorded after the package temperature reached a steady-state at each increment. Fig. 3-5(b) is R_{g2g} versus temperature obtained on one packaged die. The dashed line is a linear fit to the data. Measurements on five different dice packaged in the same way showed a 3% sample-to-sample variation in R_{g2g}.



(a)



(b)

Fig. 3-5. (a) Overview of calibration setup for TSEP determination of the package in Fig. 3-4; and (b) R_{g2g} versus temperature calibration result of the package in Fig. 3-4.

The measurement procedure described in the flow chart in Fig. 3-3 was used to determine the $\mathcal{R}_{thJC}$ of the GaN HEMT package in Fig. 3-4. Since the result should be independent of the type of TIM used, the measurements were carried out using two types of TIM: TIM_A (TG-A1250

from t-Global Technology) of 0.5 mm thick and TIM_B (TG-A6200) of 0.5 mm thick. With each type, a layer serving as the buffer was first laid down on a water-cooled plate. Then, a K-type thermocouple bead of 0.1 mm in diameter was placed at a location directly beneath the chip center, followed by layers of the TIM and the package under test. To ensure good thermal contact, the stacked structure was clamped together under pressure suggested for each specific type of TIM.

For each TIM, five measurements were taken at a thermal steady state, one for each layer of the TIM added to the TIM stack. The self-healing power was controlled to keep the same T_J in all the measurements. Plotted in Fig. 3-6 are the measured $\mathcal{R}_{thJTIM}$ in red and blue circles versus t from the test runs with TIM_A and TIM_B, respectively. The thickness, t, of the TIM stack is equal to the number of layers, n, multiplied by the thickness of each layer. Each set of data points was fitted to Eq. (4). The dashed lines in the figure are the fitted nonlinear curves. The measured junction-to-case thermal resistance, R_{thJC}, at $t = 0$, was found to be 0.100 $^oC/W$ using TIM_A and 0.124 $^oC/W$ using TIM_B, a difference of 24%.

To further validate the measurement procedure, thermal simulations by FEA in an ANSYS Workbench under Steady-State Thermal Analysis were run for each of the measurement configurations and the R_{thJC} of the package. The points plotted in red and blue crosses in Fig. 3-6 are the simulated R_{thJC} with TIM_A and TIM_B, respectively. The simulated and measured points nearly overlap with each other. The simulated R_{thJC} is 0.121 $^oC/W$, which is also in good agreement with the two experimental values.

The difference between the two values of extracted R_{thJC} may partly be attributed to the displacement of the thermocouple bead off the designated location and the nonuniform temperature distribution in the buffer layer. A separate FEA thermal simulation showed that if the thermocouple was misplaced by 1 mm, the extracted R_{thJC}, would be off by 12%. Another

contribution to the difference may come from inaccurate or imprecise temperature measurements. Using a thermocouple with an ultra-small bead would most likely improve the accuracy of the R_{thJC} measurement.

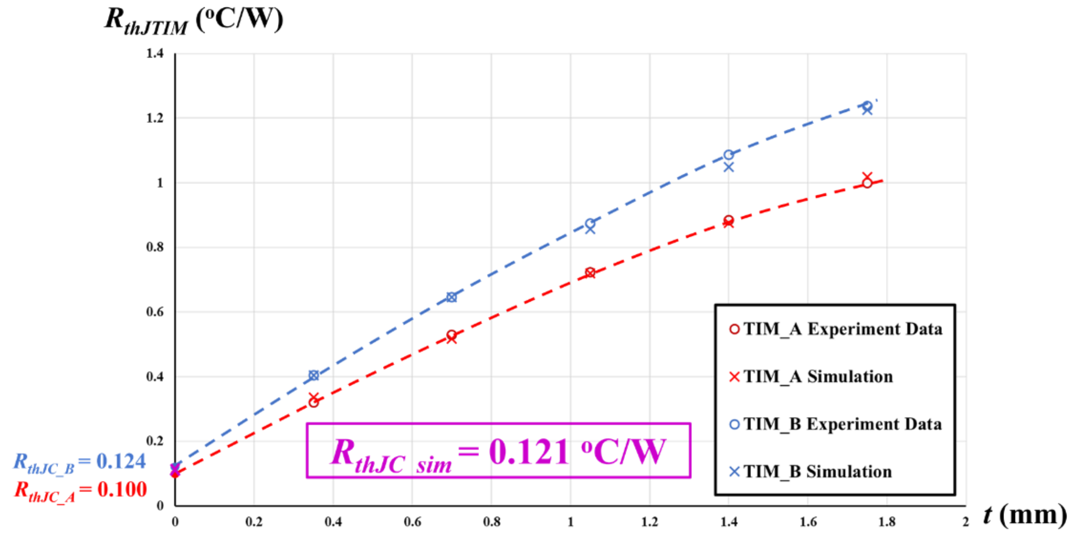
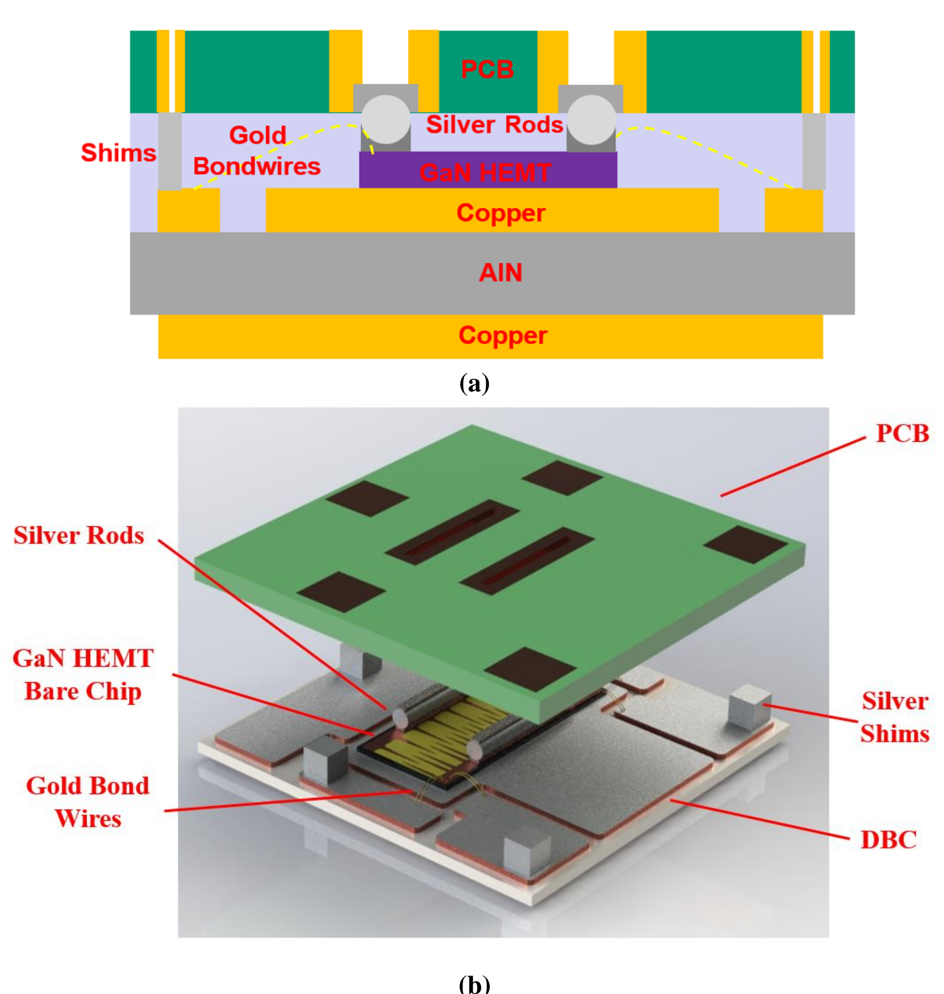


Fig. 3-6. Plots of the measured (red and blue circles) and simulated (red and blue crosses) junction-to-TIM thermal resistances with each TIM type. The dashed lines are the fitted curves of the experimental data by using Eq. (3-4). The intercepts of the fitting curves on the y-axis are the experimentally determined R_{thJC}.

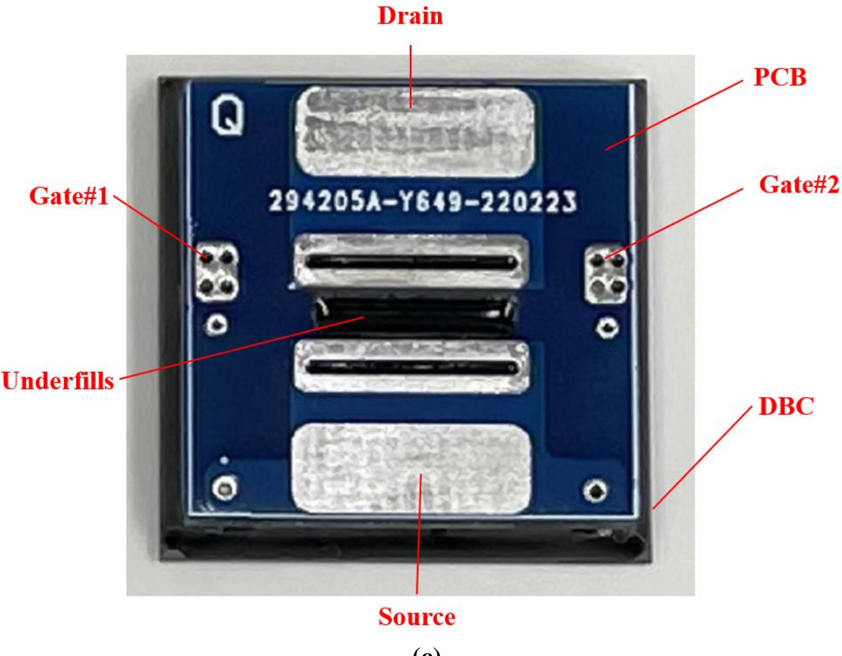
3.3.2 R_{thJC} Measurement of the Single-Sided Cooling GaN HEMT Package

To experimentally test the R_{thJC} of the embedded package described in Chapter 2.3.1, a simplified single-sided cooling embedded GaN HEMT package is designed using the same GaN HEMT bare die and packaging methodology. Fig. 3-7(a) is the cross-sectional view of the package with a single chip. The die was sintered on a DBC substrate. Since gate connections would not influence its thermal resistance, for this simplified package, the gate pads were connected to copper patterns on DBC substrates using bond wires. Four additional bond wires connected the source

pad to the substrate to avoid the backgate effect. Silver rods were still used as interposers to connect the source and drain pad. Silver shims were used to adjust the height. The rods and shims were soldered to the die's bonding pads by high-lead solder. The top side of the rod interposers was soldered to the PCB's plated slots by lead-free solder. Underfills (ME-531) were used to encapsulate the package. The 3D model of the package is shown in Fig. 3-7(b). And its top view is shown in Fig. 3-7(c).



(b)



(c)

Fig. 3-7. Simplified single-sided cooling package: (a) cross-section view; (b) 3D view; and (c) top view of a completed package.

Following the same R_{thJC} measurement procedure discussed in Section 3.2, the simplified single-sided cooling embedded package in Fig. 3-7 is first heated up for K factor calibration. Fig. 3-8 shows its R_{g2g} versus T_J plot. In the R_{thJC} measurement process, four layers of TIM were used to fit the R_{thJTIM} versus t (TIM thickness) curve shown in Fig. 3-9. According to the curve fitting, R_{thJC} is 0.087 ^{o}C/W. This value is also very close to the FEA simulation result, which is 0.099 ^{o}C/W.

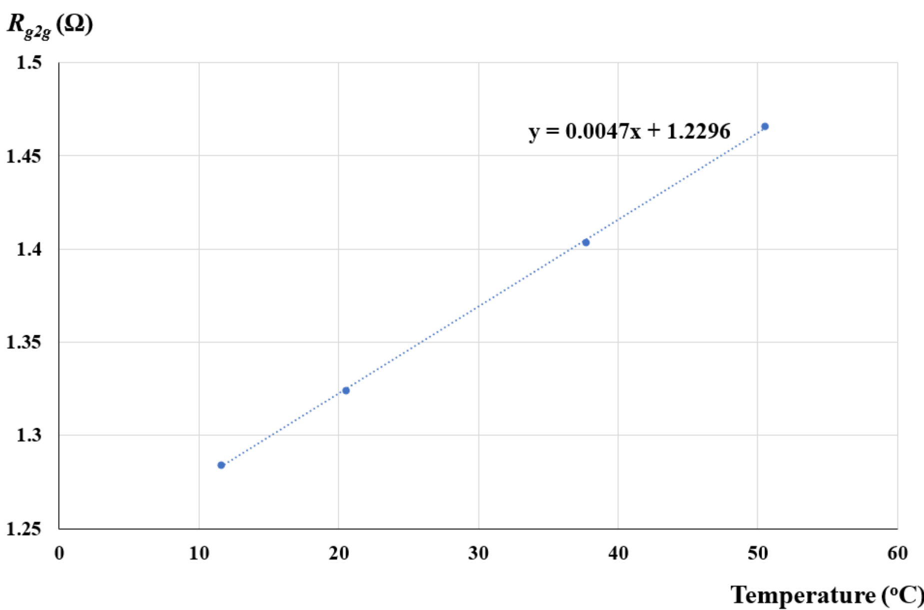


Fig. 3-8. R_{g2g} versus temperature calibration result for the simplified single-sided cooling package in Fig. 3-7.

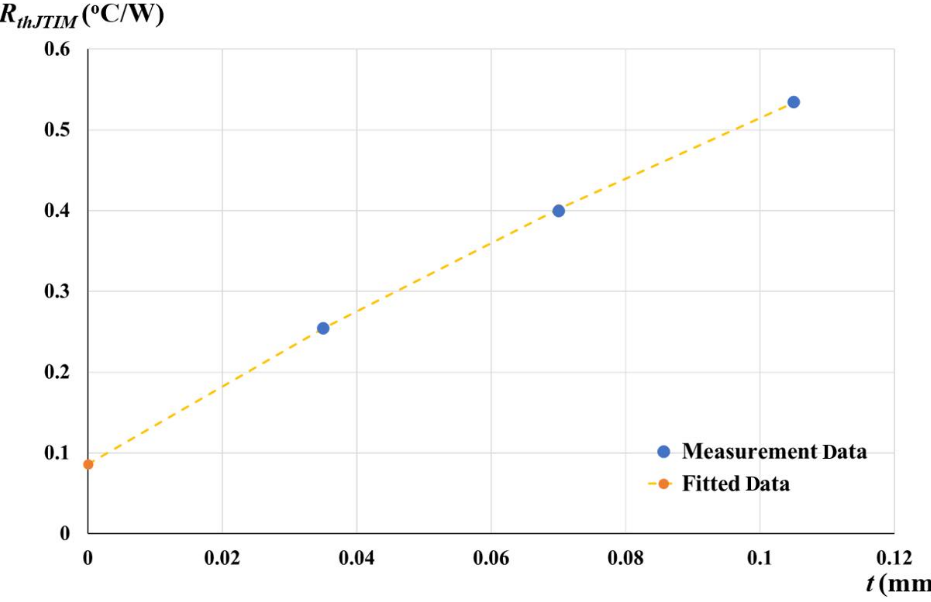


Fig. 3-9. The plot of the measured junction-to-TIM thermal resistances for the simplified single-sided cooling package in Fig. 3-7. The dashed line is the fitted curve of the experimental data by using Eq. (3-4). The intercepts of the fitting curves on the y-axis are the experimentally determined R_{thJC}.

3.3.3 R_{thJC} Measurement of the Double-Sided Cooling GaN HEMT Package

The double-sided cooling GaN HEMT package developed in Chapter 2.3.2, Fig. 2-30 was also tested for R_{thJC}. Due to the limitation of only one water cooling plate, it is hard to measure its R_{thJC} directly. In Fig. 3-10, the R_{thJC} of the double-sided cooling module can be regarded as junction-to-top-case thermal resistance (R_{thJTC}) and junction-to-bottom-case thermal resistance (R_{thJBC}) in parallel. R_{thJTC} and R_{thJBC} can be measured separately using the technique discussed in Section 2.

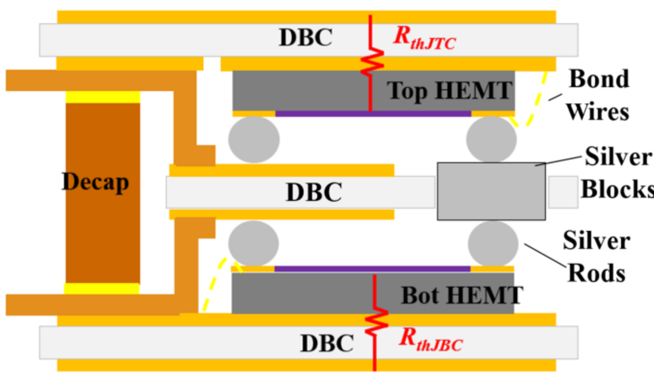


Fig. 3-10. Simplified thermal resistances in the double-sided cooling GaN HEMT package in Fig. 2-30.

Before the R_{thJTC} and R_{thJBC} measurement, K factor calibration for both the top and bottom chips was done, and the result is shown in Fig. 3-11(a) and (b). The measurement procedure described in Fig. 3-6 was used to determine the values for R_{thJTC} and R_{thJTC} of the double-sided cooling GaN HEMT package in Fig. 2-30.

In the measurement process, four layers of TIM were used to fit the junction-to-top-TIM thermal resistance, $R_{thJTTIM}$ and junction-to-bottom-TIM thermal resistance, $R_{thJBTIM}$ versus t (TIM thickness) curve shown in Fig. 3-11(a) and (b). According to the fitting, R_{thJTC} is 0.143 ^{o}C/W, and R_{thJBC} is 0.160 ^{o}C/W. Since these two thermal resistances are in parallel, the total R_{thJC} can be calculated to be 0.077^{o}C. This value is also very close to the FEA simulation result, which is 0.079 ^{o}C/W.

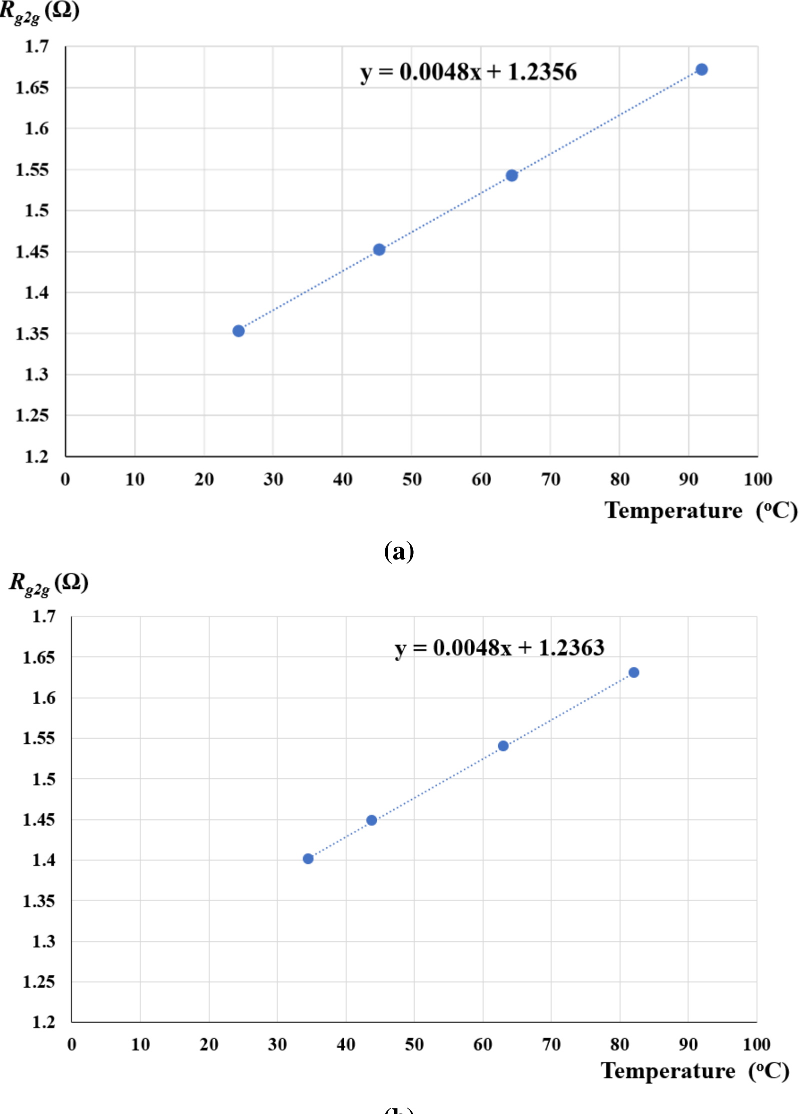


Fig. 3-11. (a) R_{g2g} versus temperature calibration result for the top-side GaN chip in the double-sided cooling package in Fig. 2-30; and (b) R_{g2g} versus temperature calibration result for the bottom-side GaN chip in Fig. 2-30.

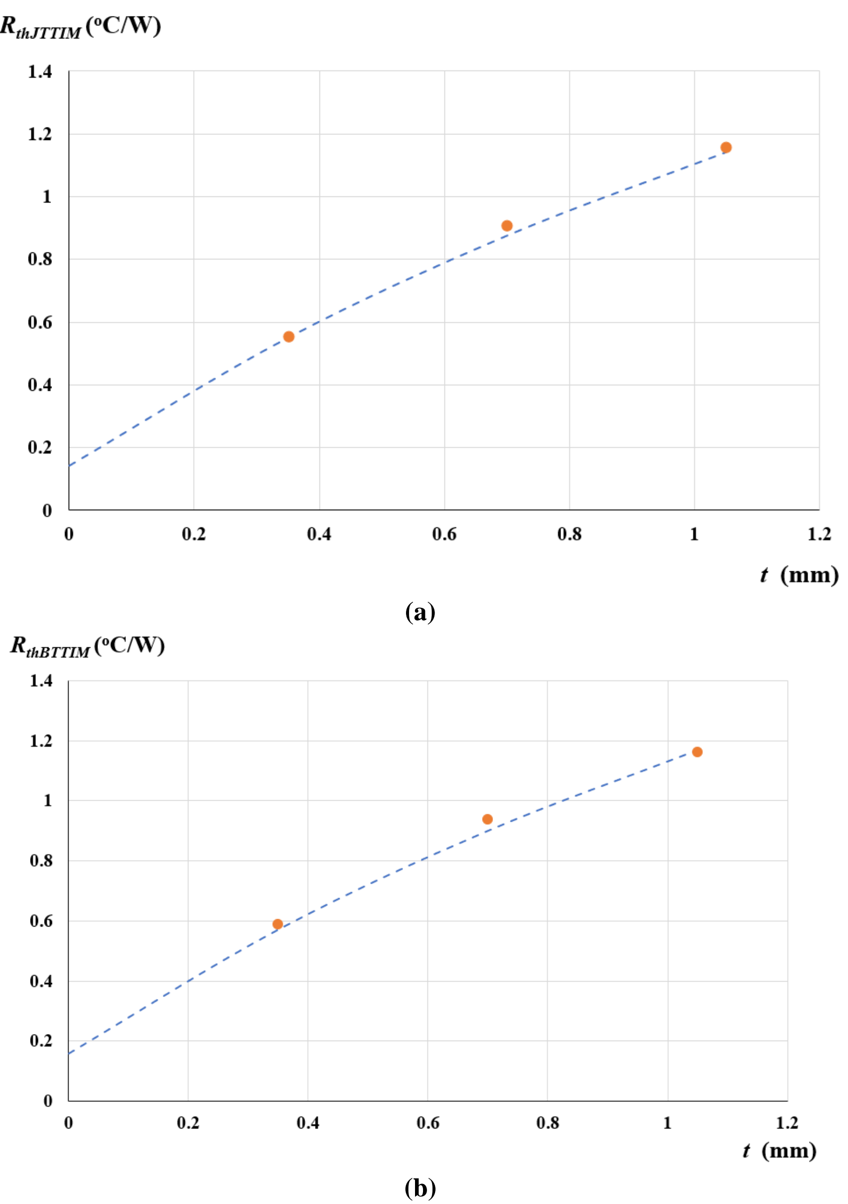


Fig. 3-12. (a) The plot of the measured junction-to-top-TIM thermal resistance ($R_{thJTTIM}$) of the package in Fig. 2-30; and (b) the plot of the measured junction-to-bottom-TIM thermal resistance, ($R_{thBTTIM}$) in Fig. 2-30. The dashed lines are the fitted curves of the experimental data by using Eq. (3-4). The intercepts of the fitting curves on the y-axis are the experimentally determined R_{thJTC} and R_{thJBC}.

3.4 Summary

This chapter has introduced a procedure to improve the accuracy of measuring the junction-to-case thermal resistance (R_{thJC}) of GaN HEMT packages. The procedure uses a GaN HEMT with two gate pads for accurate T_J measurement by utilizing the gate-to-gate electrical resistance (R_{g2g}) as the TSEP, with immunity to charge trapping and online measurement capability. The procedure also avoids direct case-temperature (T_C) measurement, which is inaccurate due to poor thermocouple/heatsink contact. Instead, the temperature at the interface between two thermal interface materials is measured. By varying the thickness of one TIM, e.g., through stacking multiple layers together, the junction-to-TIM thermal resistance, R_{thJTIM} versus the TIM stack thickness, t, is measured. Then, with the help of an analytical equation for the dependence of R_{thJTIM} on t, R_{thJC} can be determined by curve fitting and extrapolation to $t = 0$. The measurement procedure was tested using two different types of TIM on a custom wire-bonding package of an eGaN (650 V, 150 A) HEMT and embedded packages introduced in Chapter 2. The measurement results and the FEA simulation results are very close.

Chapter 4 Reliability Evaluation of the Embedded Packages

4.1 Introduction of Reliability Evaluation of GaN HEMT Packages

The long-time reliability of power switch packages is always an essential concern for power electronics packaging engineers. Although the embedded packages of the latest GaN HEMT chips developed in Chapter 2 show benefits over prior small parasitic inductances and low junction-to-case thermal resistance, their reliability still needs to be verified for high-power applications. The power cycling test is one of the reliability tests for power switch packages [25-27]. It not only provides temperature stress per cycle within a short period but also simulates the real application and stresses the package interconnections [65-67]. Therefore, the reliability of embedded packages introduced in Chapter 2 can be evaluated by this method.

However, most power cycling tests have been carried out on traditional Si and SiC MOSFET packages [68-70]. There are few power cycling tests reported for GaN HEMT packages. One of the reasons is that online monitoring of the GaN HEMT junction temperature is difficult. As discussed in Chapter 3, when the GaN HEMT packages are powered on during the test, traditional TSEPs would be unstable because of electron trapping. Some studies used the on-resistance (R_{on}), voltage drop from source to drain (V_{SD}), and gate-source voltage (V_{GS}) at a fixed gate current as TSEPs for determining GaN HEMT's T_J. However, all these TSEPs are unstable when electron trapping exists. Also, the current rating of the packages evaluated in these studies is below 30 A. For the embedded packages developed in Chapter 2, the target continuous current is at least 75 A

current rating (half of the bare die rating). The higher operating current would add high stress to package interconnections, which is an essential quality to evaluate.

In this chapter, the power cycling test setup for GaN HEMT embedded packages is first discussed in Section 2, including the LabVIEW program, test circuit design, and embedded package sample preparation. Then, the online T_J monitoring is achieved by using gate-to-gate resistance R_{g2g}, as discussed in Chapter 3. In Section 3, the power cycling test results are presented, and an FEA simulation is done to predict the failure mechanism. Finally, in Section 4, the results are summarized.

4.2 Design of GaN HEMT Power Cycling Test

4.2.1 Test Circuit Diagram and LabVIEW Control Program Design

Fig. 4-1 shows the circuit diagram of the power cycling test. A current source is used in this setup to control the operating current. To shorten the loop inductance, multiple decoupling capacitors are added. To simplify the test setup, the package under test (high voltage GaN HEMT embedded package) is always on, and the whole system is controlled by a control switch (low-voltage Si MOSFET). Since the control switch is in series with the DUT, it would also be heated and cooled during the test. To avoid the possibility that the controlled switch was damaged before being involved with the DUT, two commercial Si MOSFETs (CSD18511KCS) from Texas Instruments with R_{on} = 2.6 mΩ for each MOSFET were put in parallel. In this way, the power loss generated in each control switch is only 6% in the DUT. Also, to cool both the DUT and the controlled switches, the height of the DUT was set to be the same as the controlled switch.

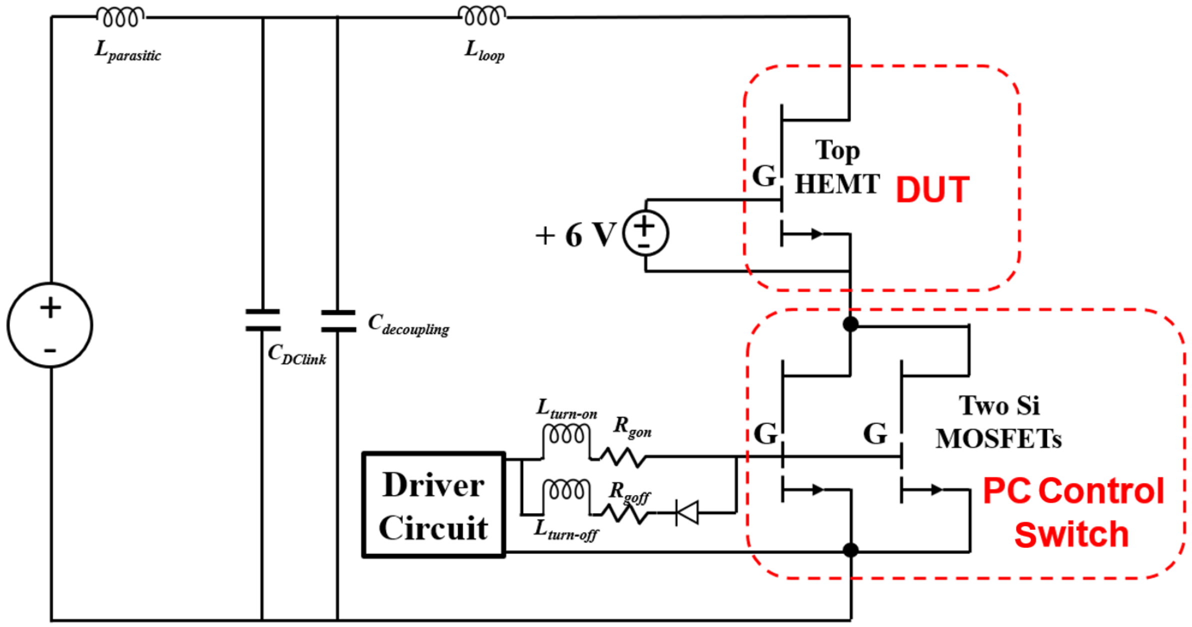


Fig. 4-1. Circuit diagram of power cycling test.

Fig. 4-2(a) shows the control signal of the control switches and Fig. 4-2(b) shows the power generated in the DUT. Since the DUT is always on, the system is powered by the current source at the set current when the control switches are turned on. As a result, T_J increases, and the R_{on} of the DUT also increases. Since the current is kept the same by the current source, the power generated by the DUT also increases during the on-time, as shown in Fig. 4-2(b). When T_J reaches the desired value, the control switches turn off, large DC-link capacitors absorb the current in the loop inductor, and the DUT cools down. The temperature profile is shown in Fig. 4-2(c).

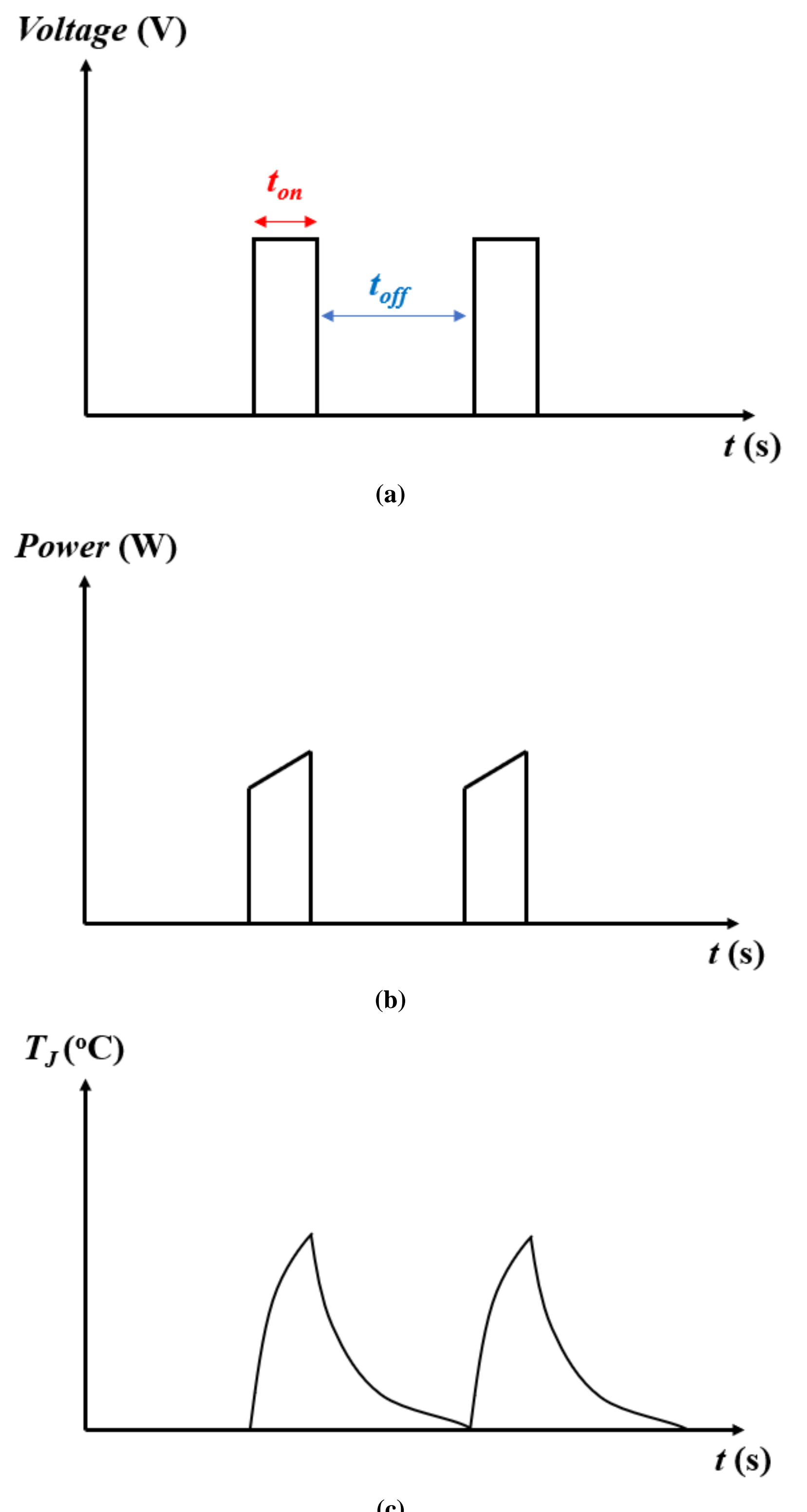


Fig. 4-2. In the power cycling test: (a) the signal applied to the control switches; (b) power generated by the DUT; and (c) the temperature profile of the DUT.

As for the detailed setup design, according to the JEDEC standard [71], the typical power cycling evaluation test conditions are shown in Table 4-1. Test condition B was selected because its minimum temperature is close to room temperature (25 ^{o}C) and the temperature difference (ΔT) is as high as 100 ^{o}C. The heating current is half of the bare chip rating, which is 75 A. As for the cooling system, a water-cooling plate with a chiller is used. The heat transfer coefficient is around 5800 W/m^{2}K.

Table 4-1. Typical power cycling evaluation test conditions.

Test Condition	Nominal $T_{cycle(min)}$, (°C)	Nominal $T_{cycle(max)}$, (°C)
A	25	+100
B	25	+125
C	10	+100
D	10	+125
E	40	+100

To monitor the T_J of the DUT during operation and to control the on/off based on T_J value, R_{g2g} (discussed in Chapter 3) was used as a TSEP. It is measured using the four-point probe method and a 50-mA isolated current source. A voltage probe acquires the voltage across R_{g2g} in the data acquisition (DAQ) device, NI USB-6211 from National Instruments, as shown in Fig. 4-4. The R_{g2g} is calculated and compared with the R_{g2g} at room temperature (25 ^{o}C) and the R_{g2g} at 125 ^{o}C. If the measured R_{g2g} is lower than R_{g2g} (@25°C), the DAQ device will send a 10-V turn-on signal to the controlled Si MOSFETs. Then the system starts heating, and the T_J of DUT increases. When the measured R_{g2g} is higher than R_{g2g} (@125°C), the DAQ device will send a 0-V turn-off signal to the controlled Si MOSFETs. Furthermore, the system is turned off, and the T_J of the DUT decreases. Fig. 4-3 shows the control logic block diagram.

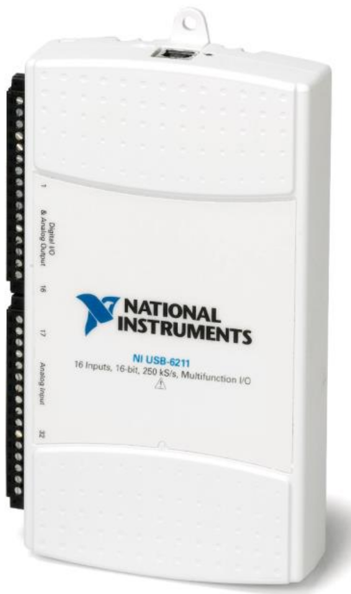


Fig. 4-3. Data acquisition (DAQ) device, NI USB-6211from National Instruments.

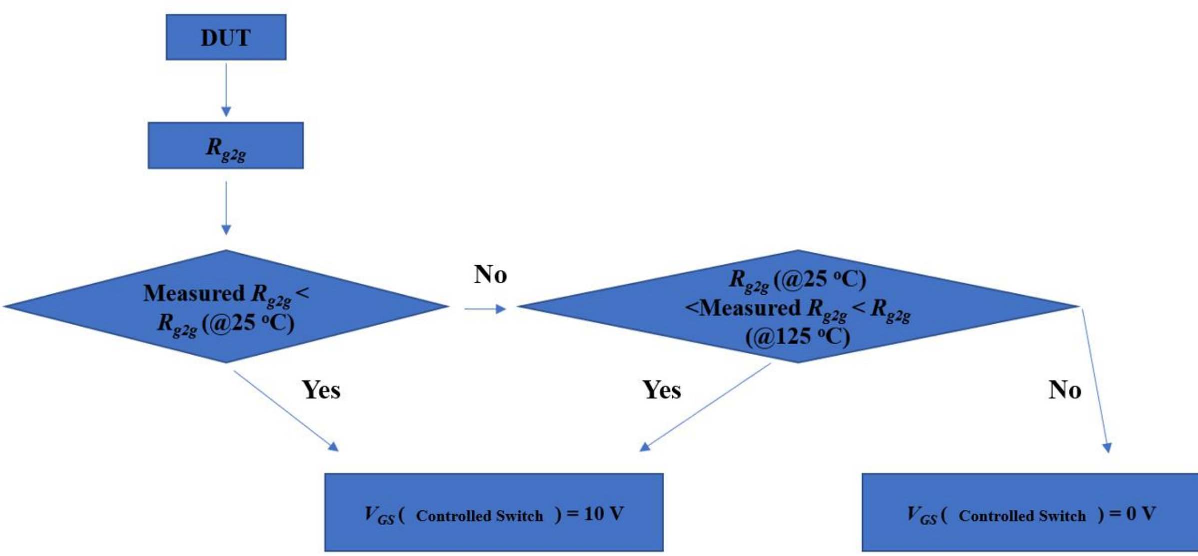


Fig. 4-4. LabVIEW program control logic diagram for the power cycling test in Fig. 4-1.

4.2.2 Power Cycling Sample Preparation, PCB Test Board Design, and Assembly

The embedded GaN HEMT package selected for this work is from Chapter 3, Fig. 3-7. It is a simplified PCB-DBC hybrid package with rod interposers for drain and source interconnections. Three samples were prepared for the power cycling test. In order to compare the embedded packages with commercial wire-bonding packages, three wire-bonding modules were designed using the same GaN HEMT bare dice. First, the bare dice were sintered on the etched substrates at 250 ^{o}C. Then, the interconnections to the gate, drain, and source pads were achieved by 2-mil gold bond wires. Assuming a 2-mi gold bond wire can stand 4 A, 18 bond wires were applied on the drain and source bonding pads. Finally, the copper tabs and silver shims were soldered to the DBC patterns. The housing was made of Duration® PEI from Mitsubishi Chemical Advanced Materials. Moreover, the package was encapsulated by silicone elastomer (Nusil R-2188). One of the wire-bonding packages is shown in Fig. 4-5. The two fabricated single-sided cooling embedded packages and two wire-bonding packages are shown in Fig. 4-6.

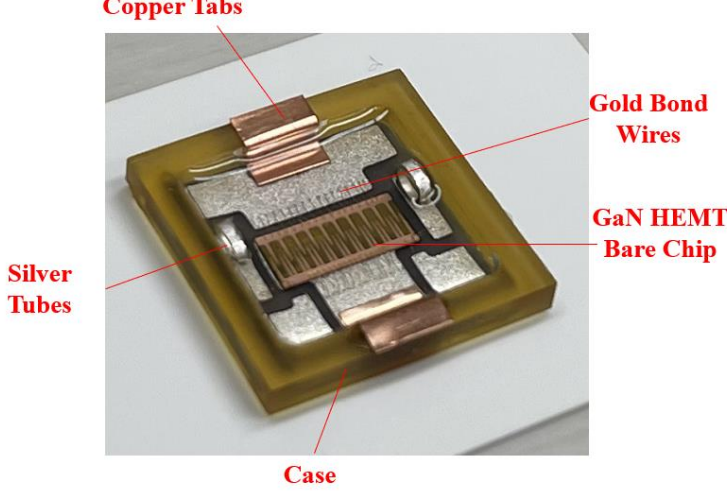


Fig. 4-5. Fabricated wire-bonding GaN HEMT package.

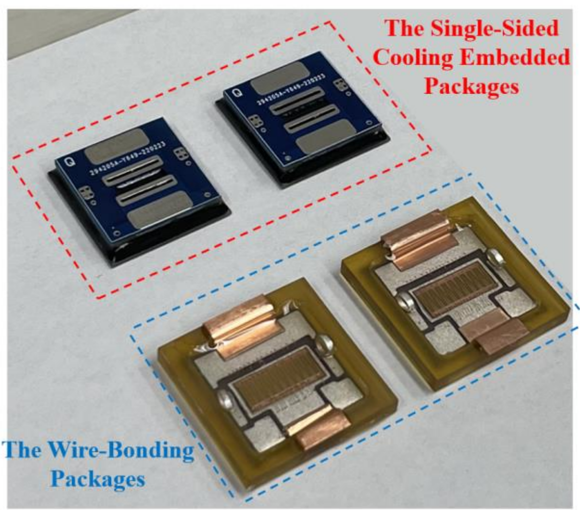


Fig. 4-6. Fabricated two GaN HEMT embedded packages and wire-bonding packages.

Meanwhile, a PCB test board was designed using Altium Designer. Besides the DUT and controlled switches, two 0.001-Ω sensing resistors were used in parallel to sense the current. The components were soldered to the board. The PCB layout is shown in Fig. 4-7. The first set of pins, P1, P2, P3, and P4, are for measuring R_{g2g} using the four-point-probe method. P5 and P6 are the nodes for the V_{GS} of the DUT. +6 V is applied to P5 and P6 to fully turn on the DUT. P7 to P10 are the nodes for driving the controlled switches. P11 and P12 are for sensing the V_{DS} across DUT. P13 and P14 are for sensing current through the DUT.

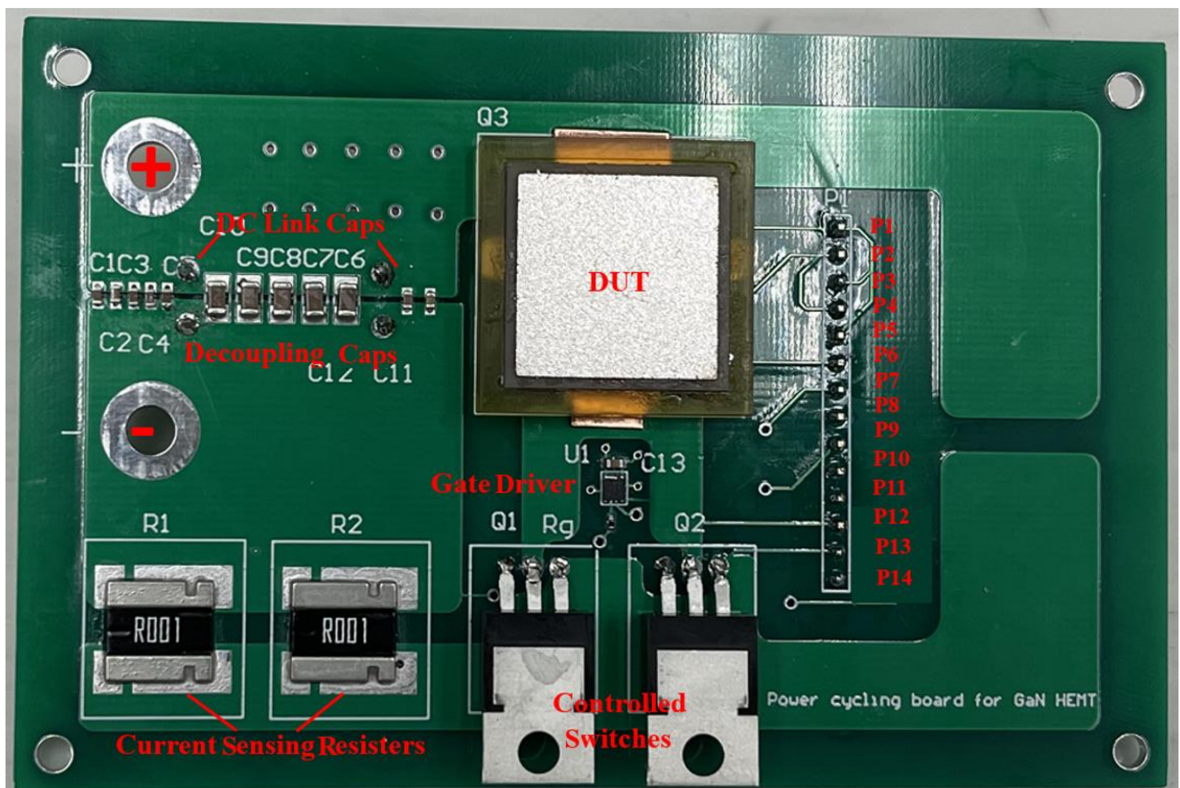


Fig. 4-7. The fabricated power cycling test board of the circuit diagram in Fig. 4-1.

4.3 Power Cycling Test

After assembly, K factor calibration was done using the same test setup. Fig. 4-8 shows the front panel of LabVIEW for K factor calibration. And the setup was clamped to a hot plate and heated to different temperatures. After K factor calibration, k and b values can be obtained.

The test board was later clamped to the water-cooling plate shown in Fig. 4-9. There were two layers of TIMs between the DUT's case and the water-cooling plate. A thermocouple bead was inserted into the middle point between these two TIM layers to monitor the TIM's temperature. This temperature is close to the case temperature. Fig. 4-10 shows the front panel of LabVIEW for the power cycling test. After inputting the desired cycle start temperature, the cycle ending temperature, and number of cycles to stop, the main cycle switch was turned on and the power cycling test was begun. The control switch signal, junction temperature, and case temperature were

monitored while the cycling test was running. After every 1,000 cycles, the on-resistance, R_{on}, was measured and recorded.

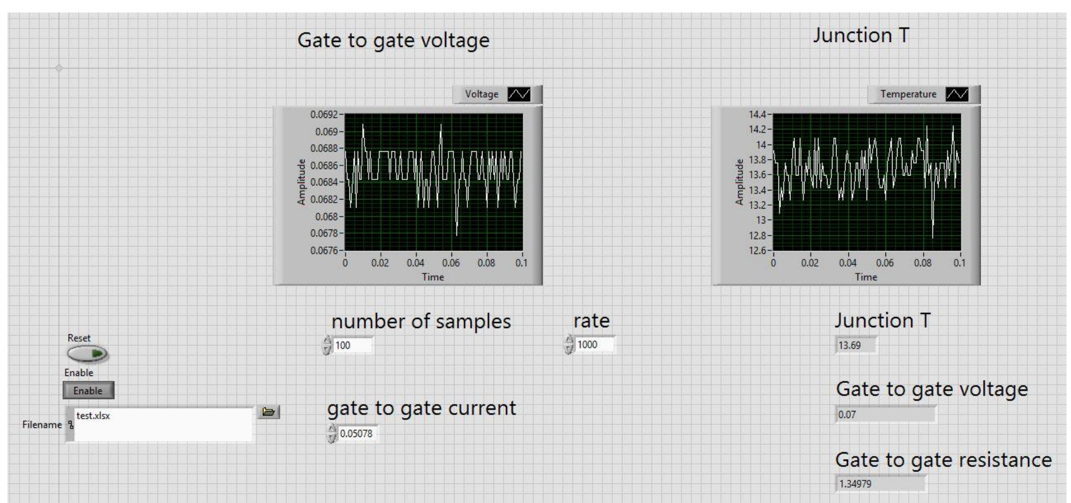


Fig. 4-8. LabVIEW front panel for K factor calibration.

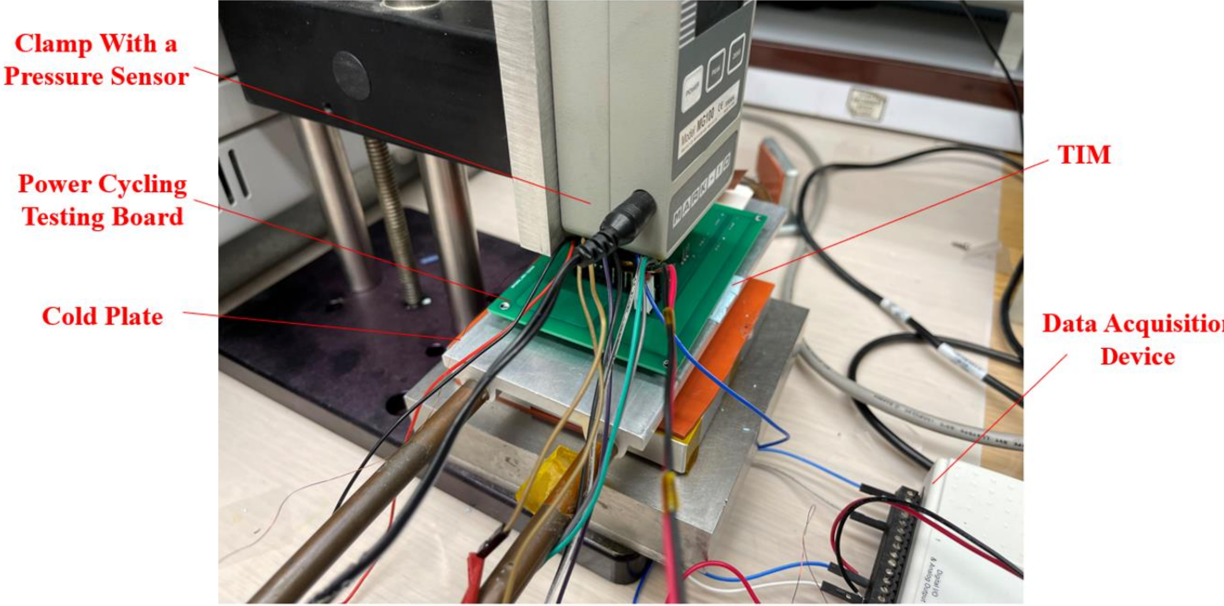


Fig. 4-9. Power cycling setup with a clamp and a water-cooling plate.

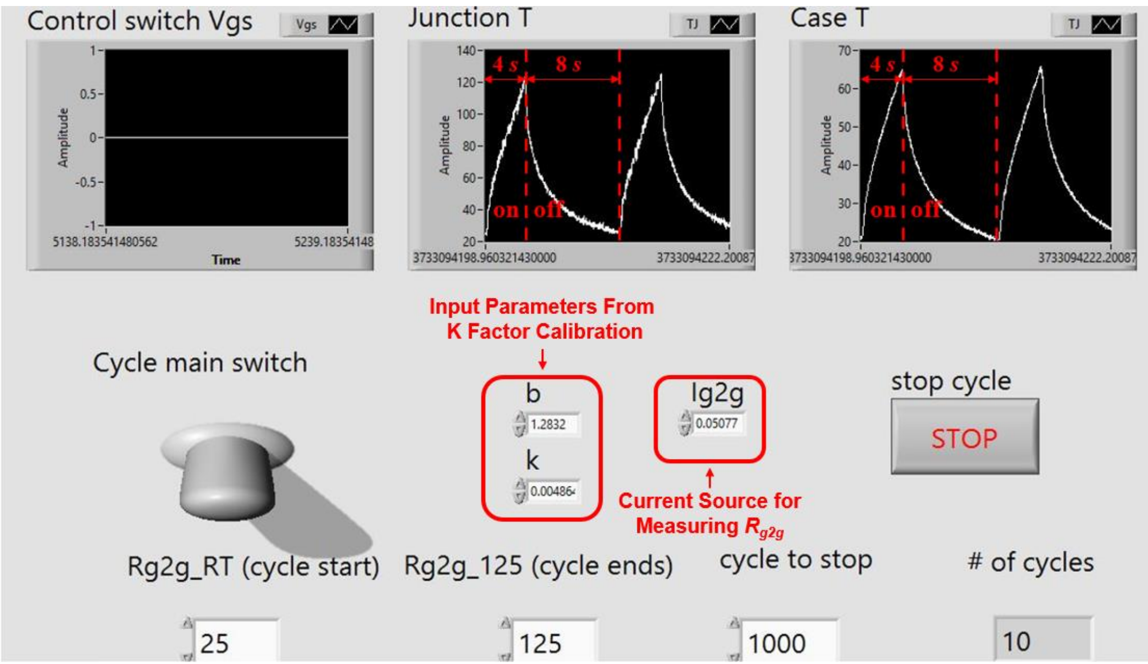


Fig. 4-10. LabVIEW front panel for power cycling test.

Fig. 4-11(a) shows R_{on} versus numbers of power cycles and (b) shows R_{thJTIM} versus numbers of power cycles of the single-sided cooling embedded packages. One sample withstands 26,064 cycles, and its R_{on} increases by 34%. The other sample withstands 23,855 cycles, and its R_{on} increases by 40%. Both samples lost gate connection after cycling. It is assumed that the reason both samples failed is that the gate bond wires failed.

For wire-bonding packages, unfortunately, at I = 75 A, two packages with 18 bond wires were not able to survive even one power cycle. As shown in Fig. 4-12, all 18 of the bond wires lost connection to the switch's drain pad. The possible reason is that the contact resistances between the gold wires and DBC substrate are not negligible. When conducting high current (75 A), the local bonding spots between gold wires and DBC were heated up and burned. So, all the bonds failed.

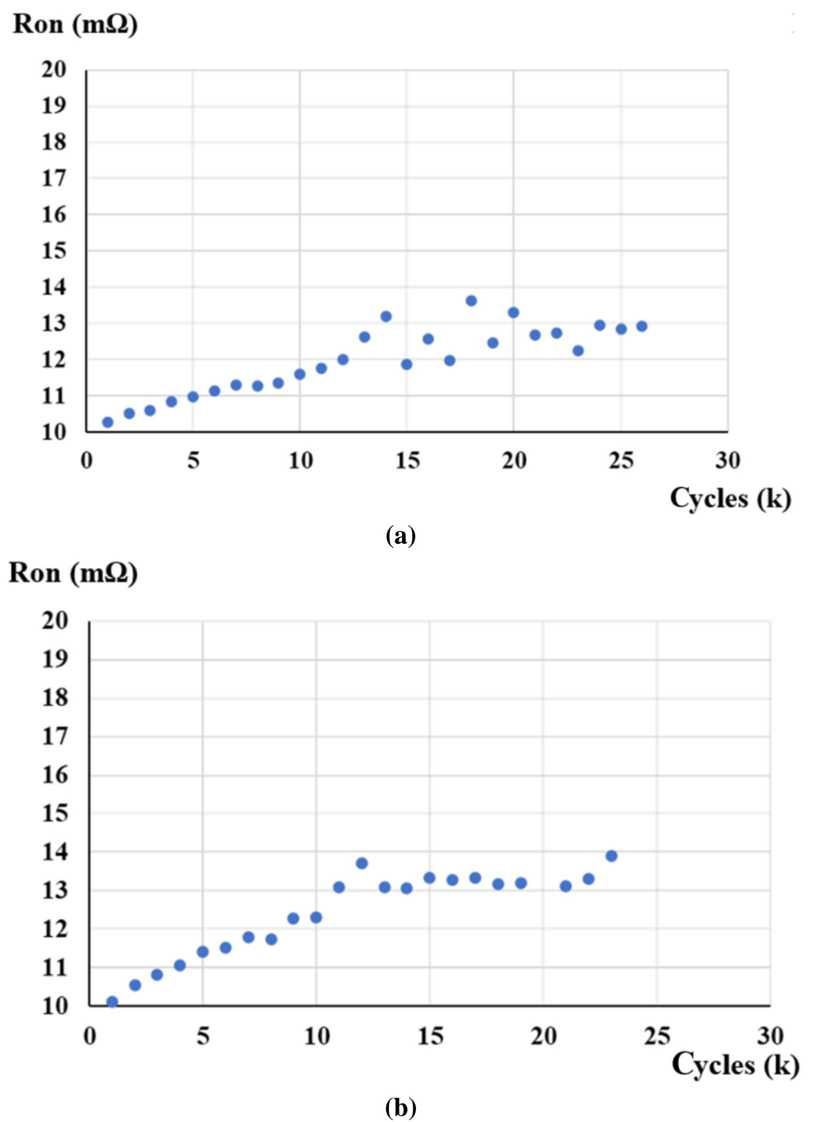


Fig. 4-11. (a) R_{on} versus numbers of cycles for the single-sided cooling embedded package sample 1 in Fig. 4-6; and (b) R_{on} versus numbers of cycles for the single-sided embedded package sample #2 in Fig. 4-6.

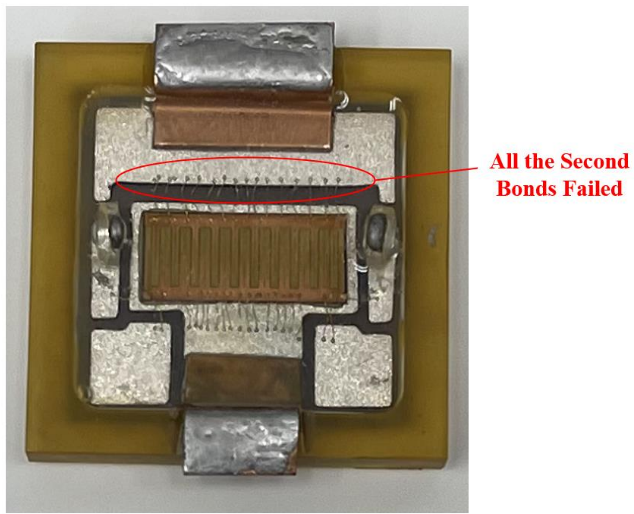


Fig. 4-12. Failed wire-bonding package after conducting 75 A for 0.1 s.

4.4 Summary

In this section, the power cycling test setup for GaN HEMT packages was designed and assembled. Online monitoring T_J was achieved using R_{g2g} as the TSEP discussed in Chapter 3. Using the LabVIEW program with a PCB testing board, the embedded package discussed in Chapter 3 was cycled from 25 ºC to 125 ºC with I = 75 A. The embedded packages were able to survive over 23,000 cycles. The failure mechanism is the gate bond wire. As for wire-bonding packages using wire-bonding for drain and source interconnections, they cannot survive even one cycle. Compared to wire-bonding packages, the embedded packages have more solid interconnections for high-current operation.

Chapter 5 Conclusion and Future Work

5.1 Conclusion

This work proposed embedded packaging techniques for a 650-V, 150-A, 10-mΩ GaN HEMT to achieve high density, power loop parasitic inductance smaller than 1.5 nH, and junction-to-case thermal resistance, R_{thJC} within 0.12 °C/W. To further verify the thermal resistance of the proposed embedded packages, junction-to-case thermal resistance measurement techniques were introduced by using gate-to-gate resistance, R_{g2g}, as a TSEP for junction temperature determination, and stacked-TIM technique to avoid case temperature measurement error. To study the reliability of the proposed embedded GaN HEMT packages, a power cycling test setup was designed and fabricated. The proposed embedded packages survived over 23,000 power cycles at heating current, I = 75 A. However, the wire-bonding package was damaged under the same circumstances after heating up at I =75 A.

5.1.1 Embedded Package Development for GaN HEMTs

The single GaN HEMT package (PCB-interposer-on-DBC) was first developed in Chapter 2.3 and demonstrated the feasibility of the embedded package solution. However, the pins and the termination add 2 mΩ resistance (total 14 mΩ) and around 1 nH parasitic inductance to the package. Then in Chapter 2.4, the embedded packaging concept was extended to a GaN HEMT half-bridge module with the same PCB-DBC hybrid structure. Silver rods replaced pins for drain and source interconnections. A decoupling capacitor was also integrated into the PCB to optimize power-loop inductance. The PCB-DBC hybrid half module achieves 11-mΩ on-resistance, 1.122-

nH power-loop inductance, and 0.099 °C/W junction-to-case thermal resistance. The module was also tested in a DPT circuit. The waveforms showed that embedded GaN HEMT packages have a clean waveform, less voltage, and lower current spikes with *dv/dt* around 40 V/ns. Finally, in Chapter 2.5, a double-sided cooling (DSC) half-bridge module was designed, fabricated, and characterized to further increase package density and improve thermal management. The DSC half-bridge module utilized the silver rod interposer discussed in Chapter 2.4. In addition, two dice were placed face to face, and a third DBC substrate was introduced for insulation. Compared to the PCB-DBC hybrid half module, the DSC half module has 30% less footprint and 20% less simulated junction-to-case thermal resistance.

5.1.2 Junction-to-Case Thermal Resistance Measurement and Reliability Assessment

To experimentally verify the thermal performances of the proposed embedded GaN HEMT packages, a junction-to-case measurement technique for embedded GaN HEMT packages was introduced in Chapter 3. The gate-to-gate resistance was used to determine junction temperature and the stacked-TIM technique was used to avoid errors in case temperature measurement. To verify the measurement, a custom wire-bonding package was fabricated. Its junction-to-case thermal resistance was measured by two different TIMs. The two measured levels of R_{thJC} were found to be within 24% of each other. The measurements were also compared with FEA simulated results, and excellent agreements were observed.

The junction-to-case thermal resistance of the embedded packages discussed in Chapter 2 was also measured using the proposed technique. For the single-sided cooling embedded package, the measured R_{thJC} is 0.087°C/W, which is close to the FEA simulation result (0.099°C/W) found in

Chapter 2. For the DSC half-bridge package, the measured R_{thJC} is 0.077°C/W. Again, it is close to the FEA simulation result (0.079°C/W).

5.2 Future Work

This work mainly focuses on developing and characterizing embedded packaging technologies for high-power GaN HEMTs. To further evaluate the reliability of the embedded packages for GaN HEMTs, the work can be extended in the following aspects.

1. Thermo-mechanical simulation using FEA can be applied to the embedded packages. By using the ANSYS Workbench simulation tools, the thermo-mechanical stresses can be simulated. The weakest points can be identified by analyzing the whole package structure and thermo-mechanical stresses. Then, FEA simulation can also be applied to temperature cycling and power cycling tests by simulating strain energy per cycle.
2. After FEA simulation, it is also significant to do reliability tests, including temperature cycling tests. By heating up and cooling down the whole embedded package structure, the stresses would accumulate inside the package for each cycle. As a result, the embedded packages could be cycled to failure. By knowing how many cycles the packages can survive, one can evaluate the reliability of the embedded packages. Also, together with FEA simulation, a lifetime model of the embedded packages can be developed.
3. After evaluating the reliability of the embedded packages, it is also interesting to integrate power supplies, bus bars, and gate drivers in the single-sided cooling embedded module. A converter can be further demonstrated using the embedded packages and compared with the converter that uses commercial switches.

Appendix A: Packaging and Characterization of GaN HEMTs for High-Temperature Applications

A.1 Introduction of High-Temperature Packaging and Characterization of GaN HEMTs

As discussed in Chapter 1, GaN HEMT's theoretical temperature limitation can be as high as 400 ^{o}C. However, very few studies reported on the high-temperature capability of packaged GaN HEMTs.

Section 2 of this appendix introduces two high-temperature GaN HEMT package designs for static and dynamic characterization. The two high-temperature packages were also fabricated. In Section 3, the fabricated packages were tested at temperatures up to 250 ^{o}C to determine the effects of temperature on their static and dynamic characteristics. Finally, Section 4 summarizes the whole chapter.

A.2 High-Temperature GaN HEMT Package Design and Fabrication

A.2.1 Wire-Bonding GaN HEMT Package With a Nitrogen Atmosphere

Fig. A-1 is a cross-sectional view of the wire-bonding GaN HEMT package with a nitrogen atmosphere. This package is for static characterization at 250 ^{o}C. Low-temperature, pressure-less silver sintering was selected for attaching the chip to a silver-coated DBC substrate. This is because the silver-sintered die-attach, once formed, can support the chip working reliably at junction temperatures up to 760 ^{o}C [72]. In addition, ball-and-wedge bonded 2-mil gold wire was

chosen for its high bond strength on the copper surface finish, current rating, and chemical stability for interconnection to the gate, source, and drain pads.

Condensed matter for chip encapsulation was avoided due to a lack of reliable, high-temperature potting materials on the market. To prevent the oxidation of copper on the chip surface at elevated temperatures, the interconnected chip was placed in a housing filled with nitrogen gas. The housing was made of Duration® PEI from Mitsubishi Chemical Advanced Materials because of its availability at low cost, ease of machining, and excellent insulating properties with a high heat deflection temperature of 216 ^{o}C. For a quick check on its high-temperature stability, the material was heated on a hot plate at 250 ^{o}C for an hour and no noticeable appearance changes were observed. Access to the three terminals of the switch was through silver leads soldered on the substrate using a high-lead (Pb) solder paste and fed out of the housing. A high-temperature silicone, NuSil R-2188, which has an operating temperature of up to 250 ^{o}C, was chosen to seal the housing onto the DBC substrate and fill the gaps between the terminal leads and the housing.

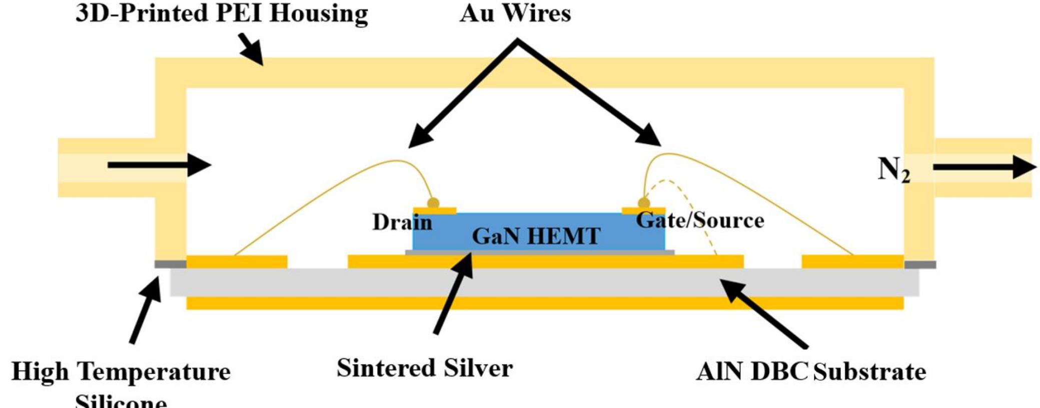


Fig. A-1. Cross-sectional schematic of the wire-bonding GaN HEMT package with nitrogen atmosphere.

Fig. A-2 shows the fabrication process of the high-temperature package. First, a 40-µm thick nanosilver paste (from NBE Technologies, LLC) was printed on an etch-patterned DBC substrate, followed by attaching the eGaN chip and sintering at 250°C for 15 minutes. The copper pads on the top surface were oxidized after sintering. To clean it off, the assembly was dipped in a diluted hydrochloric acid (HCl) solution for a few seconds, which effectively removed the oxidized copper. Then, 2-mil gold wires were ball-bonded onto the chip pads and wedge-bonded onto the DBC substrate to complete the interconnection. Next, silver leads were soldered on the substrate by reflowing a high-lead solder paste in a nitrogen-filled chamber to prevent second-time oxidation. The interconnected chip and substrate were then placed inside a 3D-printed PEI housing with gas inlet and outlet ports on its two ends and slots at the bottom for lead to feed through. The final step in the fabrication involved sealing the housing along the edges of the DBC substrate as well as the gaps between the leads and the housing. Sealing was done with the Nusil silicone by curing in a vacuum chamber to minimize trapped bubbles.

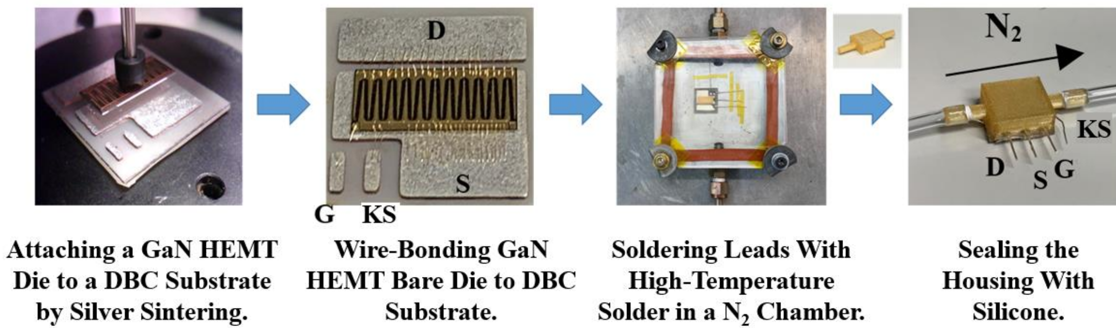


Fig. A-2. Fabrication steps of the wire-bonding GaN HEMT package with nitrogen atmosphere Fig. A-1.

A.2.2 Surface-Mounted GaN HEMT Package With Silver Rod Interposers

Fig. A-3 shows the 3D view of the surface-mounted GaN HEMT package with silver rod interposers. This package is for dynamic characterization at 250 °C. So, it is essential to shorten the parasitic inductances in the package. To better demonstrate the design structure, the cross-sectional view is shown in Fig. A-4. First, silver sintering was used to bond the bare die to a silver-coated AlN DBC substrate, for die attachment. Second, for interconnection to the drain and source, 1-mm diameter silver rods were attached to the drain pad and source pad with high-temperature solder (Sn10/Pb88/Ag2). The silver rods were conducting current vertically, and their parasitic inductance can be ultra-small (<0.1 nH). Third, for interconnection to the gate pads, two parallel 2-mil gold bond wires were used to help reduce parasitic inductance and a short silver tube was utilized for termination. To get rid of common source inductance and improve the switching performance, a second source (SS), also called kelvin source (KS), was added. The package is a flip-chip configuration and can be simply used as a surface-mounted device. To avoid the backgate effect, the source pad was connected to the DBC substrate by four bond wires. High-temperature silicone elastomers Nusil R-2188 encapsulated the package. A parasitic-related schematic is shown in Fig. A-5. The parasitic inductances of the package were simulated using an ANSYs Q3D extractor, and the thermal resistance was simulated by COMSOL Multiphysics. The result is shown in Table A-1.

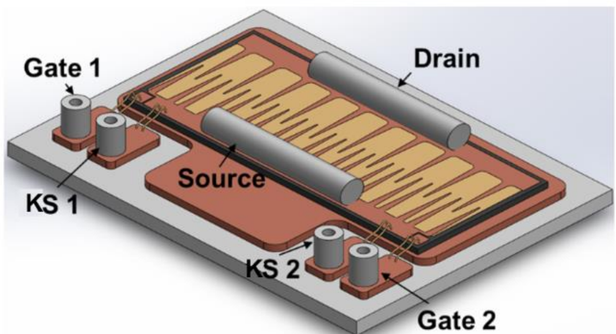


Fig. A-3. 3D model of the design for surface mount GaN HEMT package with silver rod interposers.

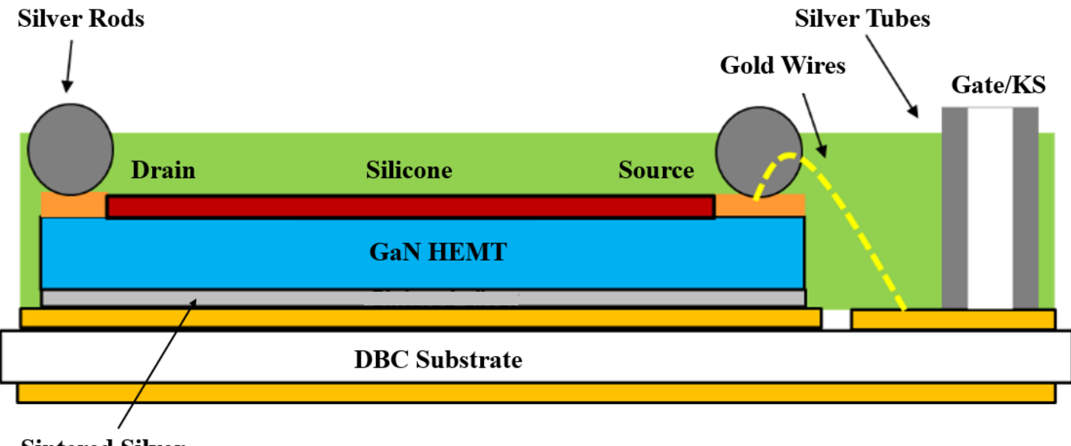


Fig. A-4. Cross-sectional view of the surface mount GaN HEMT package with silver rod interposers in Fig. A-3.

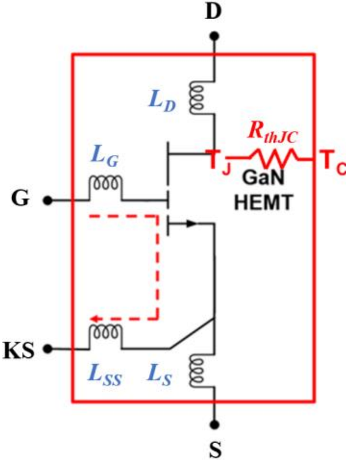


Fig. A-5. Schematic of the parasitic inductance of the surface-mounted GaN HEMT package with silver rod interposers in Fig. A-3.

Table A-1. Summaries of the parasitic inductances and thermal resistance for the surface-mounted GaN HEMT package with silver rod interposers in Fig. A-5.

	L_D or L_2 (nH)	L_G (nH)	L_{SS} (nH)	R_{thJC} (°C/W)
Simulated Parasitic Inductances	**0.09**	**1.577**	**1.555**	**0.153**

The fabrication process is shown in Fig. A-6. The bare die was attached to the substrate by nanosilver paste and sintered at 250 °C for 15 minutes. Gold bond wires were then bonded from the gate's bonding pads, and the source bonding pads were bonded to the silver-coated DBC substrate. After wire bonding, two silver rods were attached to the drain and source pads by high-temperature solder. The silver tube is also attached to the DBC pattern using high-temperature solder. They were soldered in a nitrogen chamber at 320 °C to avoid copper oxidation. Finally, the package was put in a Teflon box and encapsulated with Nusil R-2188.

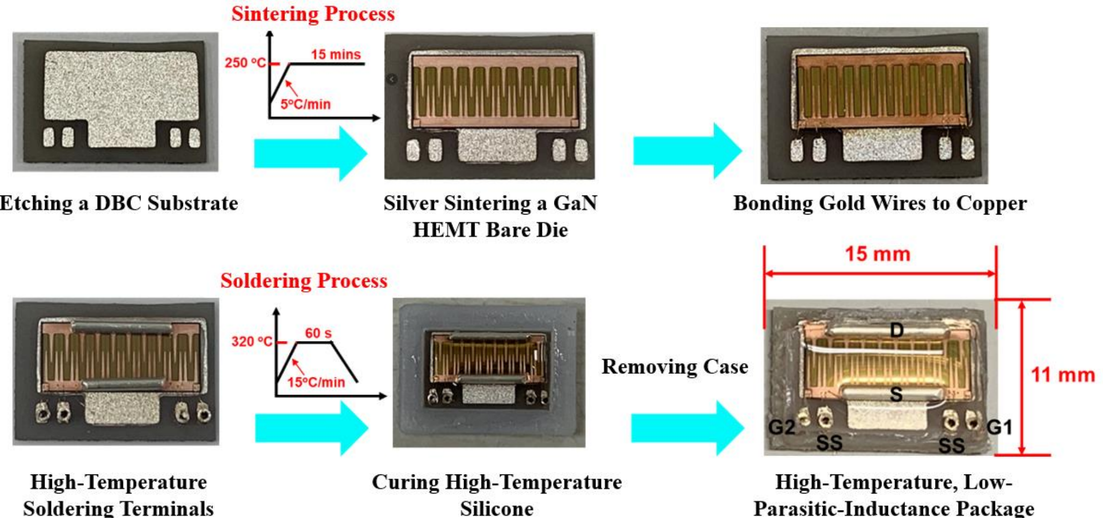


Fig. A-6. The fabrication process of the surface-mount GaN HEMT package with silver rod interposers.

A.3 High-Temperature Characterization of GaN HEMT Packages

A.3.1 High-Temperature Static Characterization

The wire-bonding GaN HEMT package with nitrogen atmosphere in Section 2.1 illustrates high-temperature static characterization. Fig. A-7 shows the setup for characterizing the wire-bonding GaN HEMT package on a curve tracer. To heat the package, a resistive heater was clamped to the DBC substrate with thermal grease in between to ensure good thermal contact between the two. The entire assembly was sufficiently compact for mounting directly on the curve tracer. Temperature monitoring was done by placing a thermocouple in contact with the bottom copper layer of the DBC substrate. This temperature was taken as the case temperature. Encapsulation was achieved by flowing nitrogen gas through the housing at a rate of 180 bubbles per minute. Since the nitrogen was at room temperature, there was a concern about its cooling effect on the chip, which would lower the chip or junction temperature below the case temperature. To calibrate the junction temperature, a package was fabricated using a nonfunctional chip. The dummy package is shown in Fig. A-8. The only difference between the functional and the dummy package was that a thermocouple was fixed on the surface of the dummy die. Following the same testing protocols used for the functional package, the two thermocouples in testing the dummy package recorded the temperature differences between the case and the junction. Table A-2 lists the differences. At low case temperatures (below 100 ^{o}C), the differences were negligible. The maximum temperature difference, with the junction temperature being lower, was only 8 degrees at 259 ^{o}C case temperature. The temperature calibration in Table 14 was used to correct the junction temperatures in the test of the functional package. In the following section, the temperatures referred to are the corrected junction temperatures.

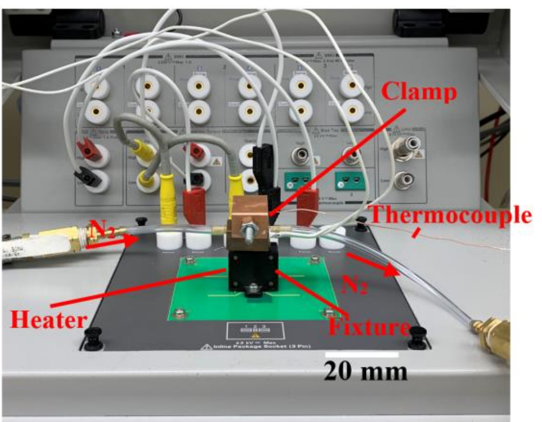


Fig. A-7. Setup for measuring the static characteristics of the GaN HEMT package in Fig. A-2 up to 250 °C.

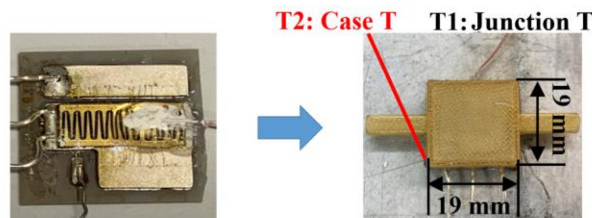


Fig. A-8. Left: Dummy package substrate showing a thermocouple affixed on top of a nonfunctional chip; right: after sealing the interconnected substrate inside a PEI housing in Fig. A-2.

Table A-2. Calibration of the temperature difference between junction and case.

Junction Temperature (T_J/°C)	Case Temperature (T_C/°C)	Temperature Difference (ΔT/°C)
50.6	50.6	0
102.3	102.3	0
150.4	154.4	4
205	210	6
251	259	8

Shown in Fig. A-9 are plots of the transfer characteristics of the packaged GaN HEMT measured at different junction temperatures, from 25 °C to 250 °C. The drain current, I_D, was reduced significantly at high temperatures. This is consistent with an analytical model proposed by others [73-75], which shows that the temperature dependence of the current comes mainly from carrier mobility. Since the mobility decreases with temperature, so does the drain current. Fig. A-9 is a plot of the threshold voltage, V_{th}, versus temperature. The threshold voltages were extracted

from Fig. A-9 using the ELR method in [76]. V_{th} gradually decreased with increasing temperature to a total of about 30% drop at 250 ^{o}C. This phenomenon was also reported in [77, 78]. Although the percentage of decrease may be small; given the already low threshold voltage of the eGaN HEMT at room temperature, one would need to take extra care in designing the gate-driver circuit to avoid false turn-on when using the eGaN HEMT in high-temperature applications.

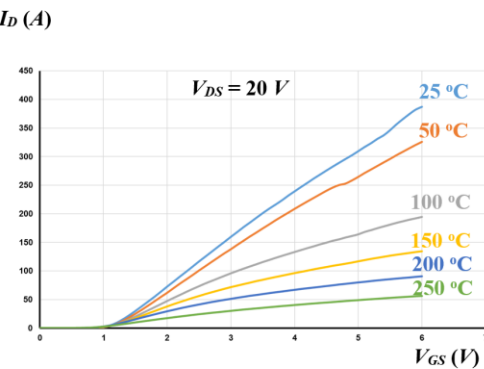


Fig. A-9. I_D - V_{GS} transfer characteristics at different temperatures (V_{DS} = 20 V) for the package in Fig. A-2.

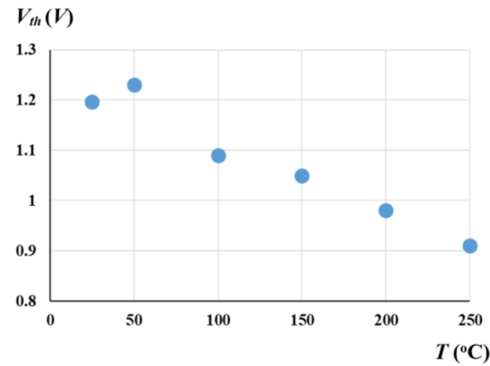


Fig. A-10. Threshold voltage vs. temperature of the GaN HEMT packaged in Fig. A-2.

Fig. A-11 shows three sets of output characteristics of t..he packaged eGaN HEMT measured at V_{GS} = 2, 4, and 6 V, respectively, and for each V_{GS}, at the different junction temperatures. For a given VGS, the eGaN HEMT's saturation voltage V_{sat} and saturation current Isat decreased with increasing temperature. This phenomenon was also observed in [79, 80]. I_{sat} is reduced to 67 A,

which is only about 45% of its room temperature current rating. The on-resistance (R_{on}) of the eGaN HEMT at different temperatures were determined from the I_D-V_{DS} curves at V_{GS} = 6 V, I_D = 40 A. Plotted in Fig. A-13 are curves of the R_{on} versus drain current at various temperatures. R_{on} was reduced below 25% of the value at room temperature. The reduction is likely caused by lower carrier mobility at a higher temperature. Consequently, the eGaN HEMT's current handling capability would have to be significantly de-rated for use at high temperatures. Finally, shown in Fig. A-13 is a plot of the leakage current I_D measured at V_{DS} = 400 V versus temperature. For the measurements, V_{GS} was set at -4 V, which is recommended for protecting the eGaN HEMT. The leakage current was relatively low at temperatures below 150 ^{o}C but rose rapidly beyond that temperature. One would have to consider its impacts on efficiency and thermal management when using the eGaN HEMT at high temperatures.

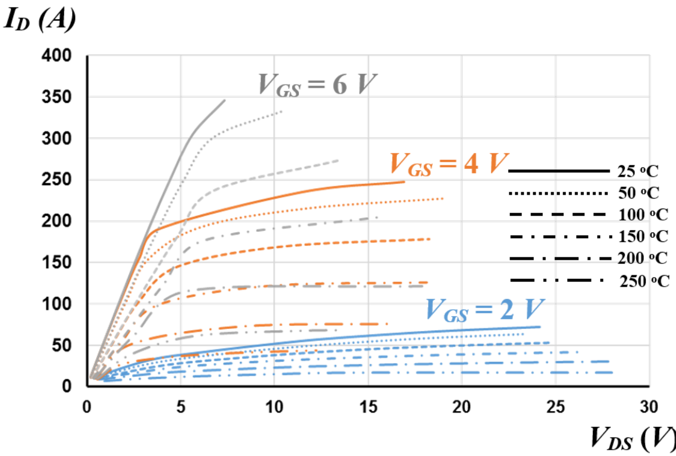


Fig. A-11. I_D - V_{DS} curves at different temperatures of the package in Fig. A-2.

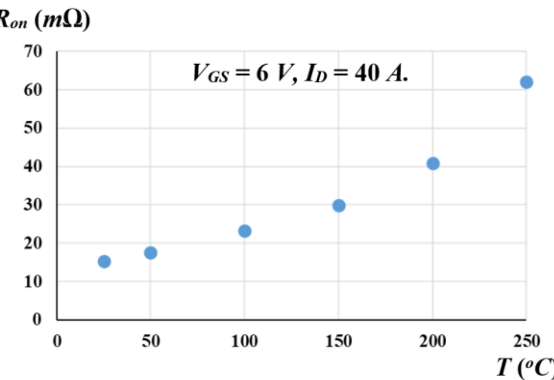


Fig. A-12. Packaged GaN HEMT on-resistance ($R_{on_package}$) vs. junction temperatures of the GaN HEMT package in Fig. A-2.

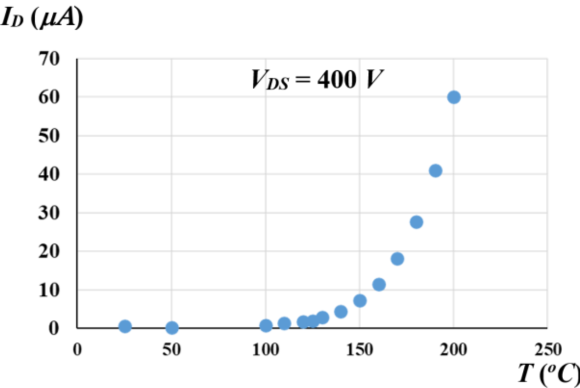


Fig. A-13. The plot of the leakage current, I_D at V_{DS} = 400 V vs. temperature of the GaN HEMT package in Fig. A-2.

A.3.2 High-Temperature Dynamic Characterization

The purpose of the surface-mounted GaN HEMT package with silver rod interposers in Chapter 2.2 was for high-temperature dynamic characterization. To get high-temperature dynamic performance, a double pulse test (DPT) setup was built for high-temperature characterization. Fig. A-14 shows the schematic for the DPT. Two pulses are sent to the DUT in a clamped inductive load circuit. By building current by the DC-bus capacitor in the first pulse, the DUT's switching transients can be captured under the desired voltage and current at the end of the first pulse and beginning of the second pulse. The high-temperature DPT setup is shown in Fig. A-14. In order to

test eGaN HEMT at high temperatures, a metal heater was attached to the other side of the DBC on the DUT, using thermal tape. A K-type thermocouple was also attached to the bottom side of the DBC to monitor the temperature. When the setup reaches a thermal steady state, the junction temperature (T_J) is the same as the case temperature (T_C) measured by the thermocouple. To test up to 250 ^oC, the eGaN HEMT was clamped to the top side of the PCB and utilized mechanical contacts to avoid solder-melting issues at high temperatures. Also, the gate driver for the DUT was placed on the bottom side of the PCB to avoid heating up from the heater. When the DUT was heated to 250 ^oC and reached a thermal steady state, the temperature of the driver was measured at about 125 ^oC (within the normal operating range).

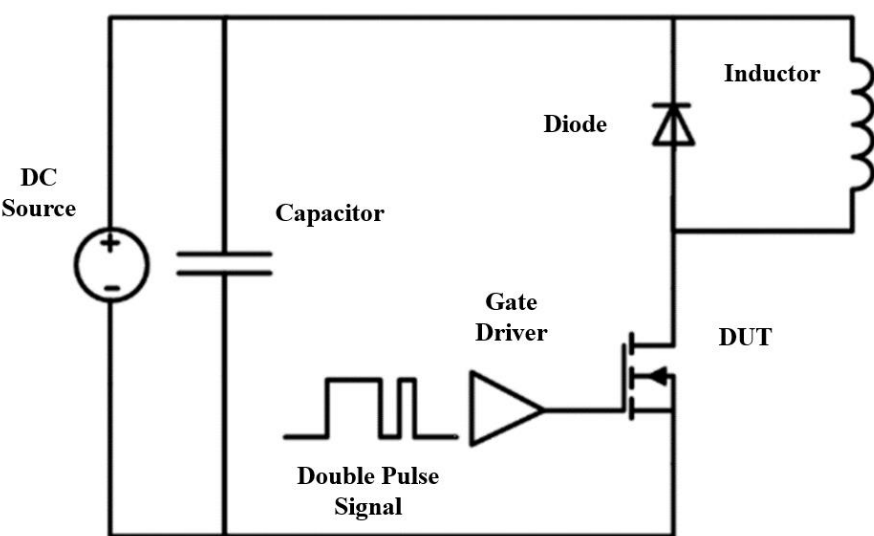


Fig. A-14. The schematic of DPT for the high-temperature test.

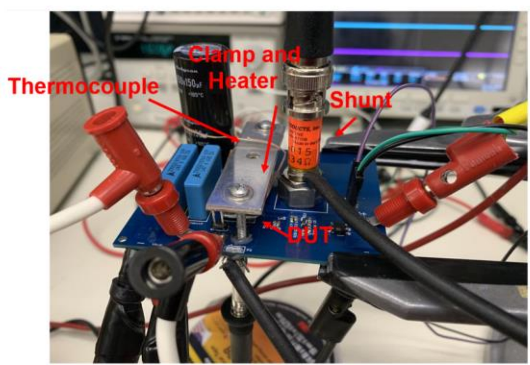


Fig. A-15. The overview of high-temperature DPT setup for the packaged GaN HEMT in Fig. A-6.

The DUT was characterized at different temperatures, 25 ^{o}C, 50 ^{o}C, 100 ^{o}C, 150 ^{o}C, 200 ^{o}C, and 250 ^{o}C. Although the eGaN HEMT's rating is 650 V, 150 A, the DUT was switched at 400 V and 40 A to avoid saturation at 250 ^{o}C. An overview of the switching waveforms for 250 ^{o}C is shown in Fig. A-16. The *dv/dt* was 38.09 V/ns, and the voltage overshoot was around 25% for the first pulse and 50% for the second pulse. The switching loss was calculated at different temperatures, and the result is shown in Fig. A-17.

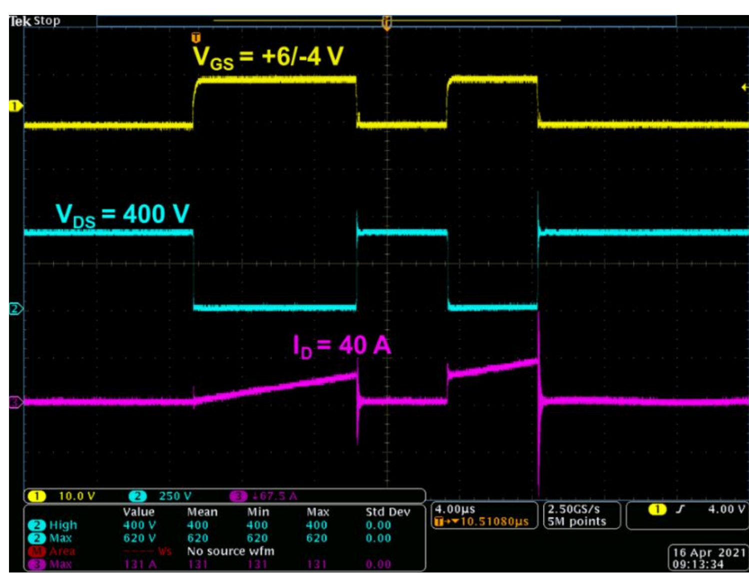


Fig. A-16. The DPT waveform @ 400 V, 40 A, and 250 ^{o}C for the GaN HEMT package in Fig. A-6.

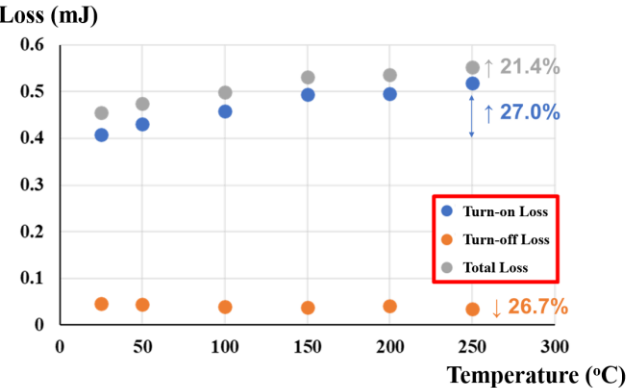


Fig. A-17. Switching loss versus temperature at different temperatures of the GaN HEMT package in Fig. A-6.

A.4 Summary

Two high-temperature packages were developed in this chapter. A wire-bonding GaN HEMT package with nitrogen atmosphere is for static characterization at high temperature. And, the surface-mounted GaN HEMT package with silver rod interposers is for dynamic characterization with much lower parasitic inductances. In the high-temperature test, a resistive heater was attached to the DBC substrate to heat the eGaN HEMT. Both packages survived multiple heating/cooling cycles between room temperature and 250 °C as they underwent static testing on a curve tracer and dynamic testing on a DPT board. As for static characterization, compared to the characteristics at room temperature, at 250 °C, the threshold voltage was reduced by about 30 %, the saturation current was down below 45% of the rated current, and the leakage current was increased by hundreds of times. As for dynamic characterization, the turn-on loss increased 27%, while the turn-off loss decreased 26.7% from room temperature to 250 °C.

These findings suggest that if the eGaN HEMT were to be used in a high-temperature power converter, one would need to significantly de-rate its current-handling capability, exert extra care in designing its gate-driver circuit to avoid false turn-on, and employ aggressive thermal management options to cool the lossy eGaN HEMT. Also, for eGaN HEMTs, zero voltage turn-on would help reduce the total switching loss at high temperatures.

References

[1] M. Carlowicz. (2021). *2021 Continued Earth's Warming Trend*. Available: https://earthobservatory.nasa.gov/images/149321/2021-continued-earths-warming-trend

[2] P. Fonta, "The "Paris agreement" on climate change: An opportunity for cement sector to further reduce its CO 2 emissions," in *2017 IEEE-IAS/PCA Cement Industry Technical Conference*, 2017, pp. 1-8: IEEE.

[3] F. Harvey, "Joe Biden could bring Paris climate goals 'within striking distance,'" *The Guardian,* 2020.

[4] M. Viser, S. M. Kim, and A. Linskey, "Biden plans immediate flurry of executive orders to reverse Trump policies," *Washington Post,* vol. 7, 2020.

[5] (2021). *Fast Facts on Transportation Greenhouse Gas Emissions*. Available: https://www.epa.gov/greenvehicles/fast-facts-transportation-greenhouse-gas-emissions#:~:text=According%20to%20the%20Inventory%20of,U.S.%20GHG%20emissions%20in%202019.

[6] (2019). *Electric Vehicle Benefits and Considerations*. Available: https://afdc.energy.gov/fuels/electricity_benefits.html#:~:text=Hybrid%20and%20plug%2Din%20electric%20vehicles%20can%20have%20significant%20emissions,when%20in%20all%2Delectric%20mode.

[7] (2017). *Electrical and Electronics Technical Team Roadmap*. Available: https://www.energy.gov/sites/default/files/2017/11/f39/EETT%20Roadmap%2010-27-17.pdf

[8] M. Hajlasz, "Gold free contacts to AlGaN/GaN heterostructures," 2018.

[9] J. Millan, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE transactions on Power Electronics,* vol. 29, no. 5, pp. 2155-2163, 2013.

[10] (2021). *AEC-Q101 Qualified 650V GaN FET in TO-247 (source tab) - TP65H050WSQA*. Available: https://www.transphormusa.com/en/document/datasheet-tp65h050wsqa/

[11] X. Huang, W. Du, F. C. Lee, Q. Li, and W. Zhang, "Avoiding divergent oscillation of a cascode GaN device under high-current turn-off condition," *IEEE Transactions on Power Electronics,* vol. 32, no. 1, pp. 593-601, 2016.

[12] Q. Song, R. Zhang, J. P. Kozak, J. Liu, Q. Li, and Y. Zhang, "Failure mechanisms of cascode GaN HEMTs under overvoltage and surge energy events," in *2021 IEEE International Reliability Physics Symposium (IRPS)*, 2021, pp. 1-7: IEEE.

[13] P. Xue, L. Maresca, M. Riccio, G. Breglio, and A. Irace, "Investigation on the short-circuit oscillation of cascode GaN HEMTs," *IEEE Transactions on Power Electronics,* vol. 35, no. 6, pp. 6292-6300, 2019.

[14] T. Oka and T. Nozawa, "AlGaN/GaN recessed MIS-gate HFET with high-threshold-voltage normally-off operation for power electronics applications," *IEEE Electron Device Letters,* vol. 29, no. 7, pp. 668-670, 2008.

[15] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, and I. Omura, "Recessed-gate structure approach toward normally off high-voltage AlGaN/GaN HEMT for power electronics applications," *IEEE Transactions on electron devices,* vol. 53, no. 2, pp. 356-362, 2006.

[16] Y. Cai, Y. Zhou, K. J. Chen, and K. M. Lau, "High-performance enhancement-mode AlGaN/GaN HEMTs using fluoride-based plasma treatment," *IEEE Electron Device Letters,* vol. 26, no. 7, pp. 435-437, 2005.
[17] B. Lu, O. I. Saadat, E. L. Piner, and T. Palacios, "Enhancement-mode AlGaN/GaN HEMTs with high linearity fabricated by hydrogen plasma treatment," in *2009 Device Research Conference*, 2009, pp. 59-60: IEEE.
[18] O. Hilt, A. Knauer, F. Brunner, E. Bahat-Treidel, and J. Würfl, "Normally-off AlGaN/GaN HFET with p-type Ga Gate and AlGaN buffer," in *2010 22nd International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2010, pp. 347-350: IEEE.
[19] X. Hu, G. Simin, J. Yang, M. A. Khan, R. Gaska, and M. Shur, "Enhancement mode AlGaN/GaN HFET with selectively grown pn junction gate," *Electronics Letters,* vol. 36, no. 8, pp. 753-754, 2000.
[20] Y. Uemoto *et al.*, "Gate injection transistor (GIT)—A normally-off AlGaN/GaN power transistor using conductivity modulation," *IEEE Transactions on Electron Devices,* vol. 54, no. 12, pp. 3393-3399, 2007.
[21] (2022). *GN001 Application Note - An Introduction to GaN Enhancement-mode HEMTs*. Available: https://gansystems.com/wp-content/uploads/2022/03/GN001_An-Introduction-to-GaN-E-HEMTs_220308.pdf
[22] K.-Y. R. Wong *et al.*, "A next generation CMOS-compatible GaN-on-Si transistors for high efficiency energy systems," in *2015 IEEE International Electron Devices Meeting (IEDM)*, 2015, pp. 9.5. 1-9.5. 4: IEEE.
[23] J. Chen, M. Hua, J. Jiang, J. He, J. Wei, and K. J. Chen, "Impact of Hole-Deficiency and Charge Trapping on Threshold Voltage Stability of p-GaN HEMT under Reverse-bias Stress," in *2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2020, pp. 18-21: IEEE.
[24] F. Yang, C. Xu, and B. Akin, "Characterization of threshold voltage instability under off-state drain stress and its impact on p-GaN HEMT performance," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 9, no. 4, pp. 4026-4035, 2020.
[25] C. Durand, M. Klingler, D. Coutellier, and H. Naceur, "Power cycling reliability of power module: A survey," *IEEE Transactions on Device and Materials Reliability,* vol. 16, no. 1, pp. 80-97, 2016.
[26] L. Lorenz, "Semiconductor power devices: Physics, characteristics, reliability [book review]," *IEEE Power Electronics Magazine,* vol. 6, no. 1, pp. 86-87, 2019.
[27] J. Lutz, "Packaging and reliability of power modules," in *CIPS 2014; 8th International Conference on Integrated Power Electronics Systems*, 2014, pp. 1-8: VDE.
[28] (2021). *IGO60R070D1-600V CoolGaN™ enhancement-mode Power Transistor*. Available: https://www.infineon.com/dgdl/Infineon-IGO60R070D1-DataSheet-v02_11-EN.pdf?fileId=5546d46265f064ff016685f053216514
[29] (2020). *LMG341xR050 600-V 50-mΩ Integrated GaN Fet Power Stage With Overcurrent Protection*. Available: https://www.ti.com/lit/ds/symlink/lmg3411r050.pdf?ts=1650388616132&ref_url=https%253A%252F%252Fwww.google.com%252F
[30] T. Hung, S. Chiang, C. Huang, C. Lee, and K. Chiang, "Thermal–mechanical behavior of the bonding wire for a power module subjected to the power cycling test," *Microelectronics Reliability,* vol. 51, no. 9-11, pp. 1819-1823, 2011.

[31] A. Ostmann, "Evolution and future of embedding technology," in *IMAPS/NMI workshop" disappearing die–embed your chips*, 2016.
[32] S. Savulak, B. Guo, and S. Krishnamurthy, "Three-phase inverter employing PCB embedded GaN FETs," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 1256-1260: IEEE.
[33] E. Hoene, A. Ostmann, and C. Marczok, "Packaging very fast switching semiconductors," in *CIPS 2014; 8th International Conference on Integrated Power Electronics Systems*, 2014, pp. 1-7: VDE.
[34] Y. Pascal, D. Labrousse, M. Petit, S. Lefebvre, and F. Costa, "PCB-embedding of power dies using pressed metal foam," in *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2018, pp. 1-8: VDE.
[35] A. B. Sharma *et al.*, "PCB embedded power package with reinforced top-side chip contacts," in *2016 6th Electronic System-Integration Technology Conference (ESTC)*, 2016, pp. 1-5: IEEE.
[36] J. L. Lu, D. Chen, and L. Yushyna, "A high power-density and high efficiency insulated metal substrate based GaN HEMT power module," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 3654-3658: IEEE.
[37] A. B. Jørgensen, S. Bęczkowski, C. Uhrenfeldt, N. H. Petersen, S. Jørgensen, and S. Munk-Nielsen, "A fast-switching integrated full-bridge power module based on GaN eHEMT devices," *IEEE Transactions on Power Electronics,* vol. 34, no. 3, pp. 2494-2504, 2018.
[38] B. Li, X. Yang, K. Wang, H. Zhu, L. Wang, and W. Chen, "A Compact Double-Sided Cooling 650V/30A GaN Power Module With Low Parasitic Parameters," *IEEE Transactions on Power Electronics,* vol. 37, no. 1, pp. 426-439, 2021.
[39] C. Ding, H. Liu, K. D. Ngo, R. Burgos, and G.-Q. Lu, "A Double-Side Cooled SiC MOSFET Power Module With Sintered-Silver Interposers: I-Design, Simulation, Fabrication, and Performance Characterization," *IEEE Transactions on Power Electronics,* vol. 36, no. 10, pp. 11672-11680, 2021.
[40] Y. Jin *et al.*, "Next generation eWLB (embedded wafer level BGA) packaging," in *2010 12th Electronics Packaging Technology Conference*, 2010, pp. 520-526: IEEE.
[41] H.-D. Chang *et al.*, "Development and characterization of new generation panel fan-out (P-FO) packaging technology," in *2014 IEEE 64th Electronic Components and Technology Conference (ECTC)*, 2014, pp. 947-951: IEEE.
[42] B. Sun, R. Burgos, D. Boroyevich, S. Bala, and J. Xu, "10 kw high efficiency compact gan-based dc/dc converter design," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 6307-6313: IEEE.
[43] H.-C. Chiu, L.-Y. Peng, C.-W. Yang, H.-C. Wang, Y.-M. Hsin, and J.-I. Chyi, "Analysis of the back-gate effect in normally OFF p-GaN gate high-electron mobility transistor," *IEEE Transactions on Electron Devices,* vol. 62, no. 2, pp. 507-511, 2014.
[44] H. Zhang, S. Yang, and K. Sheng, "GaN-on-Si lateral power devices with symmetric vertical leakage: The impact of floating substrate," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2018, pp. 100-103: IEEE.
[45] (2018). *GN002 Application Note - Thermal Design for GaN Systems' Top-side cooled GaNPX®-T packaged devices*. Available: https://gansystems.com/wp-

content/uploads/2018/10/GN002_Thermal-Design-Guide-for-Top-Side-Cooled-GaNpx-T-Devices_Rev-181030.pdf
[46] Y. C. Yeo *et al.*, "Solder joint encapsulation and reliability using dippable underfill," in *2010 12th Electronics Packaging Technology Conference*, 2010, pp. 710-714: IEEE.
[47] G. Bai, "Low-temperature sintering of nanoscale silver paste for semiconductor device interconnection," Virginia Polytechnic Institute and State University, 2005.
[48] G. Q. Lu, X. Liu, S. Wen, J. N. Calata, and J. G. Bai, "Strategies for improving the reliability of solder joints on power semiconductor devices," *Soldering & surface mount technology,* 2004.
[49] J. N. Calata, J. G. Bai, X. Liu, S. Wen, and G.-Q. Lu, "Three-dimensional packaging for power semiconductor devices and modules," *IEEE transactions on advanced packaging,* vol. 28, no. 3, pp. 404-412, 2005.
[50] J. Yin, Z. Liang, and J. D. van Wyk, "High temperature embedded SiC chip module (ECM) for power electronics applications," *IEEE transactions on power electronics,* vol. 22, no. 2, pp. 392-398, 2007.
[51] A. Grassmann *et al.*, "Double sided cooled module concept for high power density in HEV applications," in *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2015, pp. 1-7: VDE.
[52] L. Kang, H. Wen, Q. Bu, and W. Liu, "Design and Evaluation of GaN-based Over-Temperature Protection Circuit," in *2019 International Conference on IC Design and Technology (ICICDT)*, 2019, pp. 1-4: IEEE.
[53] (2022). *LMG342xR030 600-V 30-mΩ GaN FET With Integrated Driver, Protection, and Temperature Reporting*. Available: https://www.ti.com/lit/ds/symlink/lmg3422r030.pdf?ts=1650383790179&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FLMG3422R030
[54] J. Joh, J. A. Del Alamo, U. Chowdhury, T.-M. Chou, H.-Q. Tserng, and J. L. Jimenez, "Measurement of channel temperature in GaN high-electron mobility transistors," *IEEE Transactions on Electron Devices,* vol. 56, no. 12, pp. 2895-2901, 2009.
[55] L. Zhang, P. Liu, S. Guo, and A. Q. Huang, "Comparative study of temperature sensitive electrical parameters (TSEP) of Si, SiC and GaN power devices," in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2016, pp. 302-307: IEEE.
[56] M. Wu *et al.*, "Accurate measurement of channel temperature for AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices,* vol. 65, no. 11, pp. 4792-4799, 2018.
[57] M. H. Hedayati, J. Wang, H. C. Dymond, D. Liu, and B. H. Stark, "Overtemperature Protection Circuit for GaN Devices Using a di/dt Sensor," *IEEE Transactions on Power Electronics,* vol. 36, no. 7, pp. 7417-7428, 2020.
[58] Y. Shan, W. Gao, Z. Huang, W. Kuang, Z. Wu, and B. Zhang, "Test Methods and Principles of Thermal Resistance for GaN HEMT Power Devices," in *2020 21st International Conference on Electronic Packaging Technology (ICEPT)*, 2020, pp. 1-4: IEEE.
[59] K. Sharma, K. M. Barón, J. Ruthardt, and I. Kallfass, "Characterisation of the junction temperature of gallium-nitride power devices via quasi-threshold voltage as temperature sensitive electrical parameter," in *The 10th International Conference on Power Electronics, Machines and Drives (PEMD 2020)*, 2020, vol. 2020, pp. 932-936: IET.

[60] (2010). *TRANSIENT DUAL INTERFACE TEST METHOD FOR THE MEASUREMENT OF THE THERMAL RESISTANCE JUNCTION-TO-CASE OF SEMICONDUCTOR DEVICES WITH HEAT FLOW THROUGH A SINGLE PATH*. Available: https://www.jedec.org/standards-documents/docs/jesd51-14-0
[61] A. Cutivet *et al.*, "Characterization of dynamic self-heating in GaN HEMTs using gate resistance measurement," *IEEE Electron Device Letters,* vol. 38, no. 2, pp. 240-243, 2016.
[62] B. M. Paine, T. Rust, and E. A. Moore, "Measurement of temperature in GaN HEMTs by gate end-to-end resistance," *IEEE Transactions on Electron Devices,* vol. 63, no. 2, pp. 590-597, 2016.
[63] B. Siegal, "An alternative approach to junction-to-case thermal resistance measurements," *Electronics Cooling,* vol. 7, pp. 52-57, 2001.
[64] D. Schweitzer, H. Pape, L. Chen, R. Kutscherauer, and M. Walder, "Transient dual interface measurement—A new JEDEC standard for the measurement of the junction-to-case thermal resistance," in *2011 27th Annual IEEE Semiconductor Thermal Measurement and Management Symposium*, 2011, pp. 222-229: IEEE.
[65] U. Scheuermann and P. Beckedahl, "The road to the next generation power module-100% solder free design," in *5th International Conference on Integrated Power Electronics Systems*, 2008, pp. 1-10: VDE.
[66] S. Haumann, J. Rudzki, F. Osterwald, M. Becker, and R. Eisele, "Novel bonding and joining technology for power electronics-Enabler for improved lifetime, reliability, cost and power density," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 622-626: IEEE.
[67] E. Özkol, F. Brem, C. Liu, S. Hartmann, and A. Kopta, "Enhanced power cycling performance of IGBT modules with a reinforced emitter contact," *Microelectronics Reliability,* vol. 55, no. 6, pp. 912-918, 2015.
[68] A. Ibrahim, J.-P. Ousten, R. Lallemand, and Z. Khatir, "Power cycling tests in high temperature conditions of SiC-MOSFET power modules and ageing assessment," in *CIPS 2016; 9th International Conference on Integrated Power Electronics Systems*, 2016, pp. 1-6: VDE.
[69] R. Schmidt, R. Werner, J. Casady, B. Hull, and A. Barkley, "Power cycle testing of sintered SiC-MOSFETs," in *PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2017, pp. 1-8: VDE.
[70] T. Ziemann, U. Grossner, and J. Neuenschwander, "Power cycling of commercial SiC MOSFETs," in *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2018, pp. 24-31: IEEE.
[71] *Power Cycling*, June 2016.
[72] M. Koelink, "Ag-sintering as an enabler for thermally demanding electronic and semiconductor applications," *EE Power,* 2017.
[73] J. Xia, Y. Ruixia, Z. Zhengping, Z. Zhiguo, and F. Zhihong, "Analytical model and simulation for AlGaN/GaN high electron mobility transistor," in *2011 International Conference on Internet Computing and Information Services*, 2011, pp. 359-361: IEEE.
[74] M. Huque, S. Eliza, T. Rahman, H. Huq, and S. Islam, "Temperature dependent analytical model for current–voltage characteristics of AlGaN/GaN power HEMT," *Solid-State Electronics,* vol. 53, no. 3, pp. 341-348, 2009.

[75] M. Li and Y. Wang, "2-D analytical model for current–voltage characteristics and transconductance of AlGaN/GaN MODFETs," *IEEE Transactions on Electron Devices,* vol. 55, no. 1, pp. 261-267, 2007.

[76] A. Ortiz-Conde, F. G. Sánchez, J. J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, "A review of recent MOSFET threshold voltage extraction methods," *Microelectronics reliability,* vol. 42, no. 4-5, pp. 583-596, 2002.

[77] R. Hao *et al.*, "Normally-off p-GaN/AlGaN/GaN high electron mobility transistors using hydrogen plasma treatment," *Applied Physics Letters,* vol. 109, no. 15, p. 152106, 2016.

[78] P. Dherbécourt, O. Latry, and A. El Oualkadi, "Temperature effects of GaN HEMTs on the design of power converters," in *Third International Conference on Computing and Wireless Communication Systems, ICCWCS 2019*, 2019: European Alliance for Innovation (EAI).

[79] M. A. Khan *et al.*, "GaN based heterostructure for high power devices," *Solid-State Electronics,* vol. 41, no. 10, pp. 1555-1559, 1997.

[80] A. Anwar, S. Wu, and R. T. Webster, "Temperature dependent transport properties in GaN, Al/sub x/Ga/sub 1-x/N, and In/sub x/Ga/sub 1-x/N semiconductors," *IEEE Transactions on Electron devices,* vol. 48, no. 3, pp. 567-572, 2001.