ESD protected SiGe HBT RFIC Power Amplifiers

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(ABSTRACT)

Over the last few decades, the susceptibility of integrated circuits to electrostatic discharge (ESD) induced damages has justified the use of dedicated on-chip protection circuits. Design of robust protection circuits remains a challenging task because ESD failure mechanisms have become more acute as device dimensions continue to shrink. A lack of understanding of the ESD phenomena coupled with the increased sensitivity of smaller devices and time-to-market demands has led to a trial-and-error approach to ESD-protected circuit design. Improved analysis capabilities and a systematic design approach are essential to accomplish the challenging task of providing adequate protection to core circuit(s).

The design of ESD protection circuitry for RFIC's has been relatively slow to evolve, compared to their digital counterparts, and is now emerging as a new design challenge in RF and high-speed mixed-signal IC development. Sub-circuits which are not embedded in a single System-on-Chip (SOC), such as RF Power amplifiers (PAs), are of particular concern as they are more susceptible to the various ESD events.

This thesis presents the development of integrated ESD protection circuitry for two RFIC Power Amplifier designs. A prototype PA for 2.4 GHz Wireless Local Area Network (WLAN) applications was redesigned to provide protection to the RF input and the PA Control pins. A relatively new technique known as the *L-C tank* approach was used to protect the RFinput while a standard *diode ring* approach was used to protect the control line. The protection techniques studied were subsequently extended to a completely protected three-stage PA targeting 1.9 GHz Digitally Enhanced Cordless Telephone (DECT) applications. An on-chip shunt-L-series-C input matching network was used to provide ESD protection to the input pin of the DECT PA. A much more area efficient (as compared to the diode ring technique) *Zener* diode approach was used to protect the control and signal lines. The PA's RF performance was virtually unaffected by the addition of the protection circuits.

Both PAs were designed in a commercially available 0.5 μm SiGe-HBT process. The

partially protected WLAN PA was fabricated and packaged in a 3mm x 3mm Fine Pitch Quad Flat Package FQFP-N 12 Lead package and had a measured ESD protection rating of ± 1kV standard Human Body Model (HBM) ESD test. The simulated DECT PA demonstrated +1.5kV/-4kV HBM performance.

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Chapter 1

Introduction

The last few decades have witnessed remarkable growth in the wireless communications market which has led to the dramatical increase in the demand for integrated circuits operating in the RF/microwave regime. During this time, the technology has undergone profound changes. Future evolutions of wireless technology will offer more bandwidth, security and reliability, making them ideal for multimedia, video-conferencing, e-commerce and other complex applications. Widely anticipated applications for wireless technology include: wireless internet access, video on demand, personal data assistants (PDAs), position location and navigation in automobiles, mobile e-commerce, wireless computer peripherals and customized personal information services available anytime, anywhere [1] [2]. The expansion of such services is accompanied by the demand for low-cost, wireless transceivers.

Low cost, smaller size and increased cost efficiency have led to the trend of miniaturization and integration in circuit design. RF/monolithic microwave integrated circuits (RFICs and MMICs) have revolutionized the RF/microwave industry and have made the concept of wireless System on a Chip (SOC) a reality. The advantages of RFICs compared to hybrid printed circuit approaches are [3]:

- Higher reliability
- Reproducibility
- Higher performance

- Smaller Size
- Lower Cost (particularly packaging and assembly cost)

However, due to the difficulties involved in implementing high performance on-chip passive components, as well as reduced voltage headroom and lower breakdown voltages of active devices, ultimate levels of wireless SOC integration remain a major challenge. On-chip inductors in BiCMOS/CMOS technology typically have Quality (Q) factors ranging from 5 to 30 as compared to several 100s for off-chip inductors. The low Q factor of on-chip inductors remains a bottleneck in the integration of high performance RF sub-circuits such as Power Amplifiers (PAs) in single-chip systems (e.g. in silicon). As a result, PAs typically require off-chip baluns, capacitors and inductors to match to 50 Ω systems as shown in [4] [5].

In a mobile environment, a relatively small battery is typically the source of power for the entire system, so a major consideration of wireless circuit design is to minimize the power consumption. PAs are the core of the RF transmitter front end, amplifying the signal to an appropriate level as specified by the overall system link budget. The PA is typically the most power hungry circuit in the RF portion of the system and it is therefore critical to maximize PA efficiency. Finally, the overall cost of the RF front end must be minimized, which not only includes the fabricated ICs themselves, but their packaging, handling, testing, etc.

1.1 RFIC Technology Comparison

Gallium-Arsenide (GaAs) has historically been the preferred technology for PAs because of its intrinsically higher low-field electron mobility, transistion frequency (f_t[1]) and breakdown voltage. The semi-insulating GaAs substrate also helps in developing high-Q passive elements. Due to higher bandgap energies and mobilities, GaAs PAs have higher gain even at lower operating voltage. The higher gain translates into improved Power Added Efficiency (PAE) as compared to Si or SiGe PA's. Table 1.1 summarizes the key relative differences between Si and GaAs for RF applications [6].

[1]The theoretical frequency at which the short circuit current gain of the CE mode transistor drops to 0dB.

Table 1.1: Comparison of fundamental material properties of Si and GaAs Technology.

Properties	**Silicon**	**GaAs**
Breakdown Field (V/cm)	$\approx$ 3x10^5	$\approx$ 4x10^5
Low-field Electron Mobility (cm^2/V-sec)	$\approx$ 1500	$\approx$ 8500
Thermal Conductivity ($watt/cm$-$°C$)	$\approx$ 1.45	$\approx$ 0.45
1/f Noise Corner Frequency (Hz)		
BJT/HBT	$10 - 10^3$	$10^4 - 10^6$
MOSFET/MESFET	$10^3 - 10^5$	$10^6 - 10^8$
Substrate Resistivity (Ω-cm)	10^3	10^8

Even though GaAs has a number of advantages over Si, it also has some disadvantages which needs to be considered. The thermal conductiviy of GaAs is about 4 times lower than that of Si. This is a particularly difficult challenge for GaAs ICs as the power which must be dissipated is typically higher than that of Si ICs. Thermal management issues is a major consideration with regards to the ruggedness of the GaAs PAs. Stability and reliability have also been areas of major concern in GaAs technology [7] [8].

Recent advancements in Si-based RFICs, particularly the advent of SiGe Heterojunction Bipolar Transistors (HBTs), offers a significant challenge to GaAs HBT technology. The unity current gain frequency (f_t) of SiGe HBTs have reached a level comparable to GaAs technology. In fact SiGe HBTs have been demonstrated with f_ts beyond 350 GHz [9]. GaAs technology still has a significant performance advantage due to the higher low-field mobility which improves the minimum noise figure [10], but this is not a major concern in PA design. Meanwhile, the availability of PNPs and FETs in Si and SiGe technologies offer increased functionality in PA circuits. SiGe technology also offers a potential cost advantage over GaAs due to compatibility with existing Silicon fabrication infrastructure. Finally, a high level of integration can be achieved in SiGe ICs which in turn reduces the packaging complexity.

A summary of the advantages of SiGe technology over other technologies is given below:

- Size and power consumption are critical to mobile applications. For a given f_t, a SiGe HBT would require only about a third of the collector current as

compared to a Si BJT [6]. Also since MOSFETs historically have lower g_m per mA as compared to BJTs/HBTs, the current required to obtain the same f_t is larger [11].

- Breakdown voltages of SiGe HBTs are about twice those of Si BJTs for same f_t. As far as RF CMOS technology is concerned, the breakdown voltage as well as the maximum operating voltage are limited due to thin oxide breakdown and hot-carrier effects [12].

- HBTs have better noise performance since they have higher current gain (β) and f_t as compared to BJTs. The base resistance of a SiGe HBT can also be lower than the Si BJT counterpart. CMOS devices typically have higher minimum noise figure as compared to bipolar devices when biased at the same current density [13].

- By optimizing the *Ge* profile in the base of a HBT, much higher *Early voltage* V_A can be obtained than in BJTs. This results in higher r_o which maximizes gain and also helps in improving stability. The short-channel RF-MOSFETs have much lower r_o than SiGe HBTs due to increased channel-length modulation effects.

- HBTs have higher current gain than conventional BJTs as a result of which improved linearization by feedback is possible. Cancellation of the base-emitter heterojunction capacitance improves the intermodulation performance of HBTs as compared to MESFET and HEMT. This results in excellent linearity data as reported in [14].

Due to the advantages of SiGe HBTs, such as higher current gain, early voltage, breakdown voltage and transit frequency f_t, reduced base resistance as well as better transport properties of the base, performance approaching GaAs technologies can be achieved. Therfore SiGe technology was selected for the circuit designs in this work.

1.2 Need for ESD protection

Electrostatic Discharge (ESD), which is a major subset of Electrical Overstress (EOS), is a major reliability issue in ICs. EOS and ESD together account for more than 60 %

of failures in Si ICs [15]. As semiconductor devices have scaled to smaller dimensions and ICs have become more complex, the potential for destructive ESD events has became more serious. The problem of ESD protection is dealt with on a number of levels such as incorporating on-chip protection circuits, properly grounding the chip handling equipments and properly training personnel involved with wafer and package handling, in order to minimize the potential for ESD-related failure. However, once an IC is packaged and shipped, on-chip protection mechanisms are the major means of protection against ESD damage [16].

More recently, there has been a tremendous demand for increasing the electrostatic discharge (ESD) robustness of Radio Frequency Integrated Circuits (RFICs) in wireless communications applications, since such products, typically handheld, are much more prone to ESD-induced damages. On the other hand, ESD protection structures introduce parasitic effects that can adversely affect the performance of the core circuitry. Providing sufficient ESD protection for the RFICs in wireless systems without excessively degrading the performance poses a major design and reliability challenge. ESD protection for digital ICs is relatively mature; however, ESD protection of RF circuits is still in its infancy and is a topic of significant research and development [17] [18]. No standard methodologies exist yet for RF ESD protection. Standalone PA's are of particular concern since they are currently not embedded in large System on Chips (SOC), but are more likely to be packaged in separate PA modules.

1.3 Objective and Overview of Thesis

This work focuses on the development of integrated ESD protection circuitry that does not adversely impact the performance and cost of high performance RFIC power amplifiers. Specifically, this thesis involves the development of an ESD protection strategy in a state-of-the-art commercial SiGe technology for two, 3-stage power amplifiers, designed for 2.4 GHz Wireless Local Area Network (WLAN) and 1.9 GHz Digitally Enhanced Cordless Telephone (DECT) standards, respectively. The designs feature ESD protection schemes optimized for RF performance that protect the PAs from standard Human Body Model (JESD22-A114-B [19]) and Machine Model (JESD22-A115-A [20]) ESD events. However, these schemes can be straightforwardly extended to PA designs for other applications.

The first power amplifier, designed for 2.4 GHz Wireless Local Area Network (WLAN) applications, was partially protected (RF input and control lines only) while the second PA, designed for DECT standard was fully protected (input, output, control and supply lines). Different ESD protection schemes were used, and their advantages/disadvantages are explained in detail in the forthcoming chapters. The circuits were designed using a commercial $0.5\mu m$ SiGe-HBT process with high Q on-chip inductors. The PAs were packaged in a lead free 3mm PQFP (Plastic Quad Flat Package) 12 lead package.

This chapter has provided a brief discussion on some of the different technologies available in the market for PA design. Chapter 2 details the phenomena of ESD and also discusses some of the commonly used ESD characterization schemes such as Human Body Model and Machine Model in detail. Chapter 3 discusses the basics of power amplifier design and presents the design of a baseline WLAN PA which was redesigned with ESD protection circuits. Chapter 4 covers the design and simulation of the partially ESD protected WLAN power amplifier, and presents the measured results for the fabricated protoype. Design and simulation of the fully ESD protected DECT PA is presented in Chapter 5. A comparative analysis of the ESD schemes used for the two PAs is also presented in Chapter 5. The thesis concludes with a discussion of future research directions building on this work.

Chapter 2

Electrostatic Discharge

2.1 Background

Electrical overstress (EOS) includes high-energy events such as electrostatic discharge (ESD), electromagnetic pulses, lightning, and reversal of power and ground pins, which can cause catastrophic damage to integrated circuits. As a result of the high voltages involved, large electric fields and high current densities in small devices can lead to thermal damage and breakdown of insulators in ICs. By definition, EOS is *"the exposure of a component to a current or voltage beyond its maximum rating"*. ESD represents the largest subset of EOS. ESD is the *"rapid, spontaneous transfer of electrostatic charge induced by a high electrostatic field"* [21]. The duration of an EOS event may be anywhere from less than one nanosecond to one millisecond or longer. Long EOS events can lead to blown metal lines, latch up, and void formation in silicon due to local heating [16]. Such phenomena lead to either degraded performance or total failure of the circuit. Determining if the failure was specifically caused by ESD is a difficult task.

Although the field of RF circuit design has benefited from advances in IC technologies (in particular, Si-based technologies such as SiGe BiCMOS and RF CMOS), the design of ESD protection circuitry for RFIC's has been relatively slow to evolve and is a topic of significant research and development [22]. The rapid rate of technological advancement has reduced the time available for protection circuit design and development. It is therefore becoming more and more important to design protection

circuits that can be transferred into newer (next generation) technologies with little modification. Hence it is critical to understand the phenomena of ESD to ensure that the protection circuit design can be scaled or transferred with minimal impact on ESD and RF performance.

This chapter begins with an overview of ESD phenomena. The chapter then focuses on the characterization of ESD robustness based on voltages, currents and duration of the pulses. Classical ESD characterization has been performed using tests designed to model specific scenarios such as human handling, machine handling, or field induction. The most common industrial models used to test ESD performance of ICs are the Human-Body Model (HBM) [23] and the Machine Model (MM) [20]. Finally, another characterization technique called the Charge Device Model (CDM) [24] [25] is briefly discussed.

2.2 ESD Phenomena in Integrated Circuits

When two objects at different electrostatic potentials are brought into close proximity such that their electric field lines interact, transfer of electrostatic charges between the two objects can occur. This process is called electrostatic discharge or ESD. ESD events relevant to ICs have a relatively short duration of about 150 ns, and can generate very high voltage and current transients (up to a few kilovolts and a few tens of amperes). ESD is essentially a charge-driven mechanism as the event occurs because of charge imbalance [26]. ESD represents the transient discharge of static charge which may arise due to human handling or contact with machines. The theory behind the generation of these transient discharges have been presented in detail in previous works [27].

Electronic components that are susceptible to ESD damage are generally referred to as *ESD sensitive devices*, also known as $ESDS$ elements [28]. To help prevent damage to such devices, dedicated on-chip ESD structures must be incorporated to protect the core circuit against ESD stresses. The ESD protection performance level, referred to as *ESD robustness*, is determined by the ESD failure threshold voltage, $ESDV$ (expressed in units of volts or kilovolts), of an IC component.

There are three principal sources of ESD in IC manufacturing and handling environ-

ments. The first and the most common source is human handling. A human body can charge up to 20kV by walking across a carpet. This voltage is discharged to ground through an IC when the person touches the pins of the IC (assuming there exists a path to ground). Even though, the amount of energy involved is relatively small (as an ESD event lasts for very short period of time), it may be large enough to cause damage given the very small dimensions of the IC. The duration of discharge is typically about 150ns, with currents ranging from 1A to 10A depending on the conditions. The second source of ESD occurs in handling and testing systems. Such pieces of equipment can pick up charge due to improper grounding, which can then be transmitted to the IC during machine handling. The accumulated charge may be higher than in the cases of human handling. Hence the discharge is a high magnitude but short duration current pulse. The third source of ESD is the charging of the IC itself when it comes in contact with highly charged surface or material during transport. When the IC comes in contact with a grounded surface, the charge is discharged resulting in failure due to the large currents flowing in the IC. Each of the above mentioned ESD mechanisms, along with the methods used to test an IC's sensitivity to them, will be discussed in detail in this chapter.

Even though ESD is fundamentally caused by electrostatic potential, the energy dissipation and damage is due to the current flowing through the IC during the discharge. Hence, ESD protection structures should be designed so as to withstand high current levels. ESD robustness is typically stated in tems of an $ESDV$; however this is not a complete description as the above mentioned discharge models can result in different $ESDV$ for the same circuit.

2.3 ESD Protection Methods

ESD protection methods for ICs can be considered to be either *external* or *internal* chip protection schemes. External ESD protection methods include storing chips in shielded containers and handling them in static free environments. On the other hand, internal methods require integration of on-chip protection devices, which are intended to provide an explicitly robust path for ESD strikes between any pair of pins [29]. The protection circuit generally discharges the ESD strike by providing a low impedance path to ground, thereby shunting most, if not all of the transient away

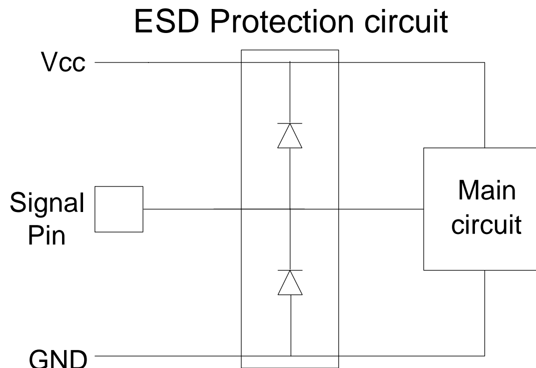


Figure 2.1: A Simple ESD protection circuit (After [30]).

from the sensitive core circuit(s). The protection circuit should also clamp the pad voltage to a sufficiently low level during the duration of the ESD event.

A typical on-chip protection circuit is placed between the signal pin and the main circuit, as shown in Figure 2.1 [30]. In this case, the diodes shunt excessive positive or negative voltage applied to the signal pin towards GND or Vcc, respectively, diverting the ESD strike from reaching the main circuit. The complexity of the protection system increases with the number of pins to be protected. It should be noted that an ESD protection circuit need not necessarily be based on diodes; depending on the available technology, it may be composed of various devices such as thick field oxide (TFO) clamps, silicon controlled rectifiers (SCRs), Medium-Voltage Triggered SCRs (MVTSCRs), spark-gaps, or transistors [31]. TFOs and SCRs fall under the category of *breakdown based* clamps. A TFO clamp consists of an NMOS transistor (used in grounded gate configuration) with a TFO gate which is tied to the drain. The trigger NMOS is usually a thin field oxide device and hence its drain needs to be protected using a resistor. SCRs do not have such triggering mechanisms and hence require higher voltages for triggering. Also SCRs take a finite time ($\sim$1ns) to latch up which makes them too slow for many applications [32]. MVTSCRs are formed by adding a bridging N+ region between the N-well and the P-epitaxial layer. As the N^+/P-epi junction has a lower breakdown voltage than the N-well/P-epi junction, the MVTSCR has a lower triggering voltage as compared to the normal SCR [33].

Ideally the protection system must not affect the input/output signal under normal operating conditions. However, the ESD protection devices present unwanted para-

sitic capacitances and resistances to the signal path, which can have an adverse effect on the performance of high speed and RF circuits. In particular, at RF frequencies, the parasitics associated with the ESD structures can lead to impedance mismatches, causing reflection of signals and degraded power transfer between signal pin and the core circuit.

Historically, the design of ESD protection circuits in RF systems has been an empirical, trial and error process in which several variations of a particular circuit are laid out, processed, packaged and tested on a pass/fail basis. This approach is time consuming and must be repeated as technologies evolve. However, advancements in CAD software and better device modeling have made the simulation of ESD events in integrated circuit designs practical. Such simulations can help predict a circuit's current-voltage response to an ESD stress event, allowing designers to evaluate the capabilities of protection circuits without costly and time-consuming fabrication, packaging, and testing cycles.

2.4 Characterizing ESD in Integrated Circuits

In order to characterize the susceptibility of a fabricated IC to ESD damage, the IC must be tested in the laboratory using stimuli which accurately mimic realistic ESD events. Actual ESD stresses can occur during wafer fabrication, packaging, testing, or any other time the circuit comes in contact with a person or machine. The most common industrial tests to measure ESD robustness are the Human-Body Model (HBM) [34] and the Machine Model (MM) [35], which are classified based on the charge storage mechanism. The human-body model, also known as the finger model, generates a pulse similar to that generated by a electrostatically charged human directly touching the pins of an IC. On the other hand, the machine model generates an oscillatory input pulse comparable to a pulse generated when a charged metal part comes in contact with an IC pin. A typical HBM and MM tester (ORYX 700) is shown in Figure 2.2. The models will be discussed further in the following sub-sections.

Some of the other techniques used for ESD characterization include: the Charge Device Model (CDM) [24] [25]; field-induced, field-enhanced [37] and capacitive-coupled

Figure 2.2: ORYX 700 HBM/MM ESD Tester (from [36]).

[38] models; and a relatively new technique called Transmission Line Pulsing (TLP) [39]. TLP will be specifically addressed in the Future work section of this thesis.

2.4.1 Human Body Model

The Human Body model has historically been the primary means of qualifying ESD reliability, as it is simple to conduct and has been accepted industry-wide over a number of years under JEDEC (formerly Joint Electron Device Engineering Council) standard JESD22-A114-B [19], MIL-STD-883F [23] and the ESD Association Standard 5.1 [34]. The HBM model is very simple to implement and relatively insensitive to parasitics such as stray capacitance and excess lead inductance. Figure 2.3 shows a schematic of a HBM and MM test circuit. For the HBM test, a 100 pF capacitor C_c (models the human body standing capacitance) is pre-charged to a given voltage V_c and then discharged through a 1500 Ω resistor R_c (models the human body resistance) into an I/O pin of a circuit, with another pin (usually a supply or ground pin), tied to ground. In this model, parasitic elements are represented by the series lead

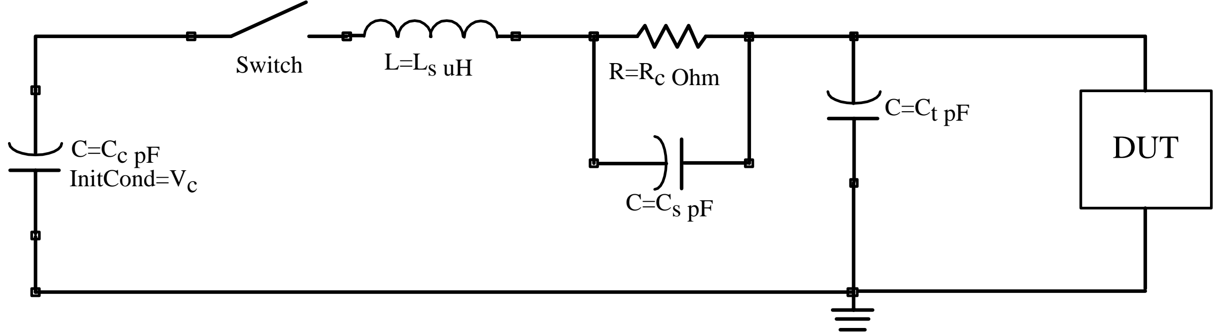


Figure 2.3: Circuit model for HBM and MM. Capacitor C_c is charged to test voltage V_c and then discharged through the resistor R_c to the *DUT* by closing the switch.

inductance L_s which determines the rise time along with the resistor R_c and R_{DUT}. R_{DUT} denotes the dynamic resistance of the device under test. C_s is the parasitic stray capacitance of R_s and the interconnect, C_t is the parasitic capacitance of the test board. A simple description of the HBM current waveform can be obtained from [40].

$$I = V_c C_c \frac{\omega^2}{\sqrt{a^2 - \omega^2}} \exp\left(\frac{-R}{2L_s} t\right) \sinh\left(\sqrt{a^2 - \omega^2}\right) t \ . \tag{2.1}$$

with $a = \frac{R}{2L_s}$, $\omega = \frac{1}{\sqrt{L_s C_s}}$, $a > \omega$ and $R = (R_c + R_{DUT})$ is the total resistance of the discharge circuit. From this equation, the risetime can be estimated as

$$t_{rise} = \frac{2L_s}{R} \ . \tag{2.2}$$

According to the MIL-STD-883F method 3015.7 specification [23], for a waveform with a rise time of $10ns$ ($t_{rise} = 10ns$), L_s is required to be about $7.5\mu H$. The decay time for a standard HBM waveform is therefore about $150 \pm 20ns$ (Figure 2.4). Table 2.1 shows the waveform specification for different voltage levels as specified by the JEDEC standard [19]. I_{peak} represents the current flowing through the resistor during a HBM strike, which is approximately $V_s/1500$. Before the actual HBM test is conducted using the DUT, a current waveform verification procedure is performed, replacing the DUT first with a short and then with a 500Ω load to make sure that the specifications in Table 2.1 are met.

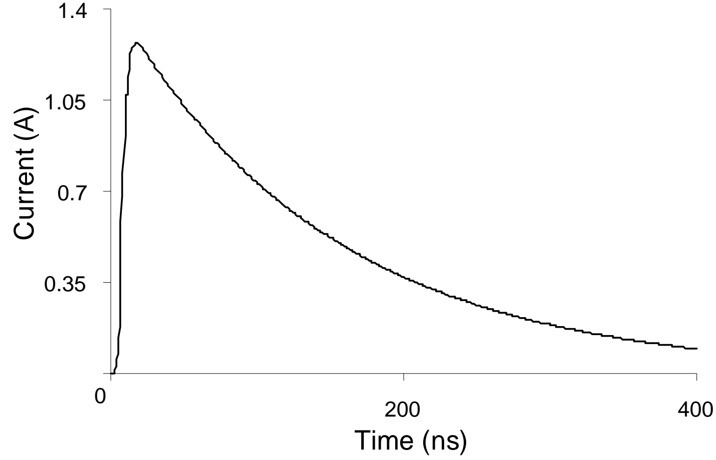


Figure 2.4: Output current waveform for V_c=2000 V, C_c=100 pF, R_c=1500 Ω, L_s=7.5 μH, C_s=1 pFand C_t=10 pF.

Table 2.1: Waveform Specification for HBM Pulse.

Voltage Level (V)	**I_{peak} for Short** I_p (A)	**I_{peak} for 500 Ω** I_{pr} (A)	**Rise Time for Short** t_r (ns)	**Rise Time for 500 Ω** t_{rr} (ns)	**Decay Timer for Short** t_d (ns)	**Ringing Current** I_R (A)
250	0.15-0.19	N/A	2.0-10	N/A	130-170	15% of I_{ps}
500	0.30-0.37	N/A	2.0-10	N/A	130-170	15% of I_{ps}
1000	0.60-0.74	0.37-0.55	2.0-10	5.0-2.5	130-170	15% of I_{ps}
2000	1.20-1.48	N/A	2.0-10	N/A	130-170	15% of I_{ps}
4000	2.40-2.96	1.5-2.2	2.0-10	5.0-2.5	130-170	15% of I_{ps} and I_{pr}
8000 (optional)	4.80-5.86	N/A	2.0-10	N/A	130-170	15% of I_{ps}

Human body model testing is conducted in accordance with the ESD Association standard [34]:

- Each I/O pin is tested individually with respect to each power supply pin. It is permissible to group the power supply pins together. All other pins [except the one being tested and the grounded pin(s)] are left open.
- Each power supply pin is individually tested with respect to other power supply pin(s). All other pins (except the one being tested and the grounded power supply pin or set of pins) are left open.
- Three positive (positive test voltage applied to the pin under test) and three negative (negative test voltage is applied to the pin under test) zaps repeated in sequence are required with an interval of 1-s between consecutive zaps.

In addition to above mentioned specifications, the MIL-STD-883F added one more specification for HBM testing [23]:

- Each I/O pin is tested individually with respect to other I/O pin(s). All other pins (except the one being tested and the combination of all input and output pins that are grounded) are left open.

Usually finer voltage steps than those given in Table 2.1 are used to obtain an accurate failure voltage. A simple test verification technique or a complete functionality verification test may be performed to validate $ESDV$. If one of the sample fails, the testing is repeated at the next lower voltage level. Samples which passed a lower voltage stress level are permitted to be used for testing at a higher ESD stress voltage; however, it is advisable to use new sample of devices to avoid cumulative damage effects. If none of the devices fail, the failure threshold is based on the highest step passed and the device is classified based on Table 2.2 [19] [23].

2.4.2 Machine Model

Another widely used ESD test scenario uses the Machine Model (MM) [20] [35]. Originating in Japan as the result of trying to replicate a worst-case HBM event, the

Table 2.2: HBM ESD Failure Threshold Classification.

Class	**Threshold Level**
0	$ESDV < 250V$
$1A$	$250 \leq ESDV < 500$
$1B$	$500 \leq ESDV < 1000$
$1C$	$1000 \leq ESDV < 2000$
2	$2000 \leq ESDV < 4000$
$3A$	$4000 \leq ESDV < 8000$
$3B$	$ESDV \geq 8000$

MM focuses on the type of discharge stresses which may occur in automated assembly lines. The basic circuit model for the MM is the same as that for HBM shown in Figure 2.3. However, the discharge capacitor C_c is increased to $200pF$ and, R_c is ideally set to 0Ω, i.e. the capacitor is discharged directly into the component [41]. In this case, the $200pF$ capacitor is discharged into the DUT via a parasitic resistance of a few ohms and a series inductance of about $1\mu H$. The resulting current waveform shows a decaying oscillatory response (Figure 2.5), with a rise time on the order of a few nanoseconds. Because of the small series resistance, the parasitic inductances and capacitances of the tester, along with the dynamic impedance of the DUT, have a much larger impact on the shape of the pulse, causing difficulty in reproducing the test environment. The MM waveform's sensitivity to DUT and the test board, makes pin-to-pin reproducibility extremely difficult, particularly in ICs with large pin counts.

The dependence of the output waveform on L_s is also shown in Figure 2.5. There is a drastic variation in rise time and peak current of the waveform when the series inductance (L_s) is changed from 0.5 μH to 2.5 μH. The MM current can be described by [42]:

$$I = V_c C_c \frac{\omega^2}{\sqrt{\omega^2 - a^2}} \exp\left(\frac{-R}{2L_s} t\right) \sin\left(\sqrt{\omega^2 - a^2}\right) t \ . \tag{2.3}$$

where $a = \frac{R}{2L_S}$ and $\omega_0 = \frac{1}{\sqrt{L_S C_S}}$ and $a > \omega_0$. When $a < \omega_0$ the above equation becomes:

$$I = V_c \sqrt{\frac{C_c}{L_s}} \exp\left(\frac{-R}{2L_s} t\right) \sin\left(\frac{t}{\sqrt{L_s C_c}}\right) \ . \tag{2.4}$$

where $R = (R_c + R_{DUT})$ is the total resistance of the discharge circuit, including

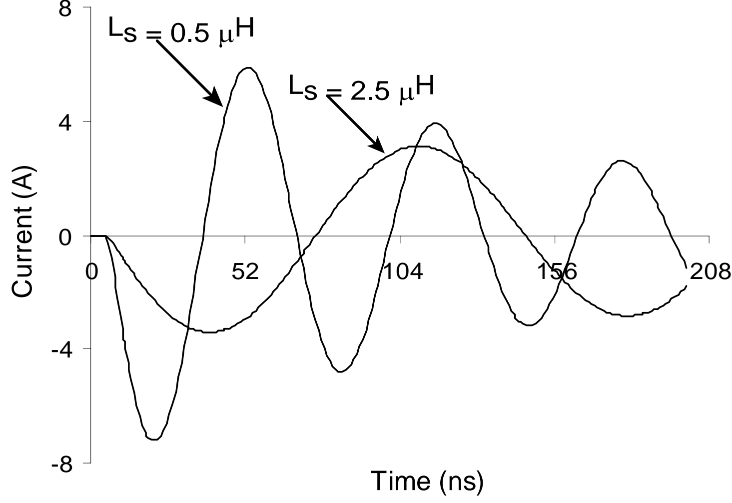


Figure 2.5: Short-circuit MM output current waveform for V_c=400 V, C_c=200 pF, R_c=5 Ω, C_s=1 pF and C_t=10 pF.

the load resistance (R_{DUT}). The current (I) has a complex characteristic with an amplitude given by $V_c\sqrt{\frac{C_c}{L_s}}$. The dependence on L_s can be clearly seen. The oscillating part of the waverform is explained by the sine term and both C_c and L_s determine the frequency of oscilaltion. The damping is determined by the series resistance and the inductance. If R_{DUT} does not meet the condition

$$R_{DUT} < 2\sqrt{\frac{L_s}{C_c}} - R_c \ . \tag{2.5}$$

then the damping term dominates and the current does not oscillate. For a specific value of L_s and R_{DUT}, if the above condition is not met, the current waveform essentially becomes that of the HBM.

As mentioned earlier, it is important to note that the threshold voltage is a sensitive function of the inductance of the system. A higher inductance value is less severe and may lead to confusing MM results when analyzing data using different test systems. Roozendaal, *et al.* [42] demonstrated the variation of $ESDV$ due to tester parasitics for the same IC tested using seven different testers. Although all the testers met the MIL-STD specification, they were not identical. Table 2.3 shows the waveform specification for a MM as specified by the JEDEC standard [20]. Because of the problems due to parasitic impedances, especially when trying to maintain pin-to-pin

Table 2.3: Waveform Specification for MM Pulse.

Voltage Level (V)	**Positive $\mathbf{I}_{peak}$ for Short** (A)	**Positive $\mathbf{I}_{peak}$ for 500 Ω** I_{pr} (A)	**Current at 100 ns for 500 Ω** I_{100} (A)	**Maximum Ringing Current** I_R (A)	**Resonance Frequency for Short** $\frac{1}{t_{fr}}$ (MHz)
100	1.5-2.0	N/A	N/A	I_{psl} x 30%	11-16
200	2.8-3.8	N/A	N/A	I_{psl} x 30%	11-16
400	5.8-8.0	I100 x 4.5	0.29±20%	I_{psl} x 30%	11-16
		max			

Table 2.4: MM ESD Failure Threshold Classification.

Class	**Threshold Level**
A	$ESDV < 200V$
B	$200 \leq ESDV < 400$
C	$ESDV \geq 400$

compatibility across a test board, JEDEC came up with a more stringent standard which includes the calibration through a 500Ω load (See Table 2.3). By calibrating the load set at 0 Ω as well as 500 Ω, the parasitics can be properly identified and compensated. However, it is important to understand the effect of parasitics on IC ESD behavior. The development of better calibration methods has been found to be expensive (requiring high frequency oscilloscopes, probes etc.) and can result in longer periods of equipment downtime.

Table 2.4 specifies the device failure threshold for the MM [20]. Due to the higher current level in MM, the pass MM thresholds for commercial IC's are typically very low as compared to those for HBM.

HBM and MM tests represent two different forms of the same discharge mechanism. In both cases, an externally charged object is discharged through the IC. Even though the failure modes are similar, the severity of damage varies drastically between the two tests. As far as the DUT is concerned, HBM and MM are considered as current sources. Hence it would be more appropriate to measure failure in terms of peak current rather than voltage.

A comparitive analysis between Human Body Model and Machine Model [40] shows

that HBM has a bandwidth of 2.1 MHz centred around 500kHz and MM has a bandwidth of 12 MHz with a centre frequency of 7 MHz. Because of the higher frequency of the MM waveform, its pulse duration is smaller, which may be less than the time required to trigger the protection circuit.

2.4.3 Charge Device Model

The HBM and MM ESD events are the result of external injection of charge into an IC. However, the Charge Device Model (CDM) ESD event is due to voltage build-up internal to the chip itself. The increased usage of automated manufacturing and testing equipment has led to environments conducive for CDM type discharges. Originally described by Bossard, Chemelli and Unger [24] [25], the CDM event is considerably faster than the HBM and MM event making it harder to model and is more sensitive to parasitics. Currently there are two implementations of the CDM test: the *field inducer test* or *non-socketed test* method [43]; and the *socketed test* method [44]. The *field-induced* test works on the principle of charging the chip and bringing a grounded pin close but not in contact with the chip's pin. Depending on the voltage and the distance between the pins, air discharge (arcing) results. This test closely replicates an actual ESD zap. However, the current-time distribution is not well controlled and also this approach depends significantly on the environment.

The socketed version is similar to HBM as shown in Figure 2.6. In this case, the discharge is controlled by a relay S2, which does not exactly replicate the physical event but can produce similar electrical reponse. The packaged IC is placed with its pins extending upwards. Charge is applied via the switch S1 and resistor R to one of the pins. S1 is then opened. A capacitor is formed between the packaged chip and the metal plate which stores the charge until switch S2 is closed. The discharge then takes place through the probe capacitance C_d, inductance L_d and resistance R_d. L_d needs to be minimized in order to obtain pulses $<$ 1ns which typical of CDM type discharges.

A major drawback of the CDM test method is that the parasitic elements in the discharge path siginificantly affect the discharge waveform. There also exist mechanical complexities in charging the ICs as it is important to avoid any damage occuring during the charging process. In addition, very expensive oscilloscopes with bandwidths

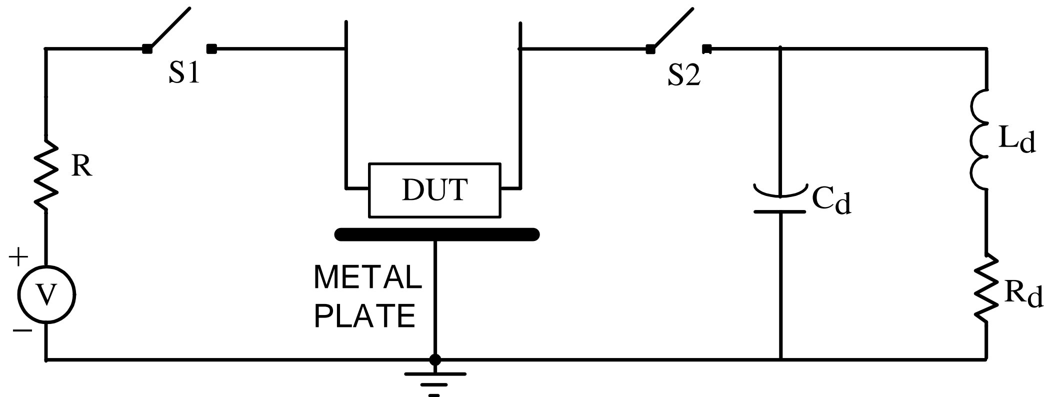


Figure 2.6: Equivalent Circuit for a Charged Device Model Test (After [40]).

in excess of 2GHz are required to monitor the discharge pulses. Consequently there is as yet no well defined CDM test standard.

The test methods described above are the principal ones currently used in the IC industry. A number of other methods have been developed for measuring the ESD performance in specific applications such as military or automotive [45]. Circuits in such applications tend to encounter more hostile environments and must be able to withstand much higher ESD stress conditions. These conditions are not reproduced by the standard HBM/MM testers.

2.5 Failure criteria

The standard method used to detect ESD damage is electrical testing. Typically, the leakage current for the stressed pin at its operating bias voltage after an ESD event is selected as the failure criterion by the ESD testers. The standards specify the allowable leakage and the leakage measurement conditions. However, a single type of test or figure of merit is not sufficient to guarantee robustness against different ESD failures. The nature of ESD makes it extremely difficult to set a fixed failure criterion. The selection of the failure criteria has a major influence on the ESD failure threshold. Not all instances of ESD damage result in a short circuit at the pin under test. The severity of the damage may vary resulting in large differences in the post-stress leakage measurements [46]. It is possible for a circuit to pass one type of test,

such as Human Body Model, while failing another, such as Machine Model [47]. It is even possible for a circuit to survive one level of a test while failing at a lower level of the same test. One particular case where a circuit passed HBM stresses less than 1kV and greater than 2kV up to 6kV, but failed at stresses between 1kV and 2kV due to interaction with the internal chip layout is described in [48]. In this case, a simple ESD protection circuit as shown in Figure 2.1 was used to protect a DRAM cell. Five clock buffers existed between the supply (V_{dd}) and ground lines (V_{ss}). One (or two) out of the five clock buffer SCR's was triggered on at lower stress levels ($< 1.5kV$ HBM) (this could most likely be due to the series metal resistance of supply lines) while at higher stress voltages ($> 2kV$), all five of the clock buffers triggered thereby avoiding the failure.

It has been shown that the leakage current at a particular stress level is directly linked to the $ESDV$ [40] and a monitor of leakage current can be used to characterize ESD behavior. However, for a reliable evaluation, the stressed IC should be subjected to a comprehensive *functional* test to make sure that it meets the product specification for performance. Thus, it should be emphasized that the type of IC being tested should be carefully considered before selecting the failure criteria.

2.6 Summary

This chapter has provided useful information about the ESD phenomena, internal and external methods of ESD protection and major issues involved in characterization of the ESD performance in IC's. The correlation between the different characterization schemes was discussed briefly. The increasing ESD sensitivity due to shrinking technologies and reduced susceptibility to human handling has led to ongoing development of newer testing standards. The next chapter sheds light on the basics of RF power amplifier design and goes on to discuss the design of a baseline PA. Chapters 4 and 5 form the core of this thesis discussing the design of the WLAN and DECT Power Amplifiers with integrated ESD protection circuitry along with subsequent simulations and measurement results.

Chapter 3

Power Amplifier Design

The Power Amplifier (PA) is a key component in the front end of an RF transmitter. Power amplifiers are used to amplify the signal being transmitted to an appropriate power level such that it can propagate over a required distance through the wireless channel. In the process, the PA should not introduce excessive signal distortion and should also be designed to minimize power consumption. The PA's control mechanism should be as simple as possible and its dimensions (die area) should be minimized. There is a well-known tradeoff between linearity and efficiency, the two important requirements for a PA. To amplify the signal to the required level, there must be some power consumed, but in order to maximize efficiency, the power consumption needs to be minimized. Hence a compromise should be reached between these two opposing requirements in the PA design.

This chapter will briefly discuss some of the commonly used parameters to quantify an RF PA, such as Power Added Efficiency (PAE), drain efficiency, and linearity measures such as 1-dB compression point, intermodulation distortion, input intercept point, adjacent channel power ratio, and Error Vector Modulation. This chapter will also discuss some of the the many different classes of operation of PA's based on the tradeoff between linearity and efficiency. Finally, the chapter will discuss the baseline PA design which is the starting point for the ESD protected design discussed in the subsequent chapters.

3.1 Efficiency

Efficiency is a critical factor in PA design. Three definitions of efficiency are commonly used [49]. *Drain efficiency* (η) is defined as the ratio of RF output power (P_{RFout}) to DC input power (P_{dc}):

$$\eta = \frac{P_{RFout}}{P_{dc}} \ . \tag{3.1}$$

Power Added Efficiency (PAE), the most commonly used metric, includes the RF drive power by subtracting it from the output power.

$$\text{PAE} = \frac{P_{RFout} - P_{RFin}}{P_{dc}} \ . \tag{3.2}$$

PAE can become less than unity for very low gains. In order to avoid this anomaly, the overall efficiency is defined as:

$$\text{Efficiency} = \frac{P_{RFout}}{P_{RFin} + P_{dc}} \ . \tag{3.3}$$

3.2 Linearity

Amplifier linearity plays an important role in the design of communication systems. Linearity is characterized using several different techniques depending upon the application. Some of the typical characterization measures are discussed briefly in the following sub-sections.

3.2.1 1-dB Compression Point ($\mathbf{P}_{1-dB}$)

Power amplifiers are typically saturating or compressing in nature. When operating in the linear region, the gain of the component is constant at a given operating frequency. However, as the input power is increased beyond a particular value, the gain decreases. The input 1-dB compression point (P_{1-dB}) is defined as the input signal level that causes the gain to drop by 1-dB [50]. The output power at this point is the output 1-dB compression point ($P_{1-dB,out}$). As shown in Figure 3.1, the output

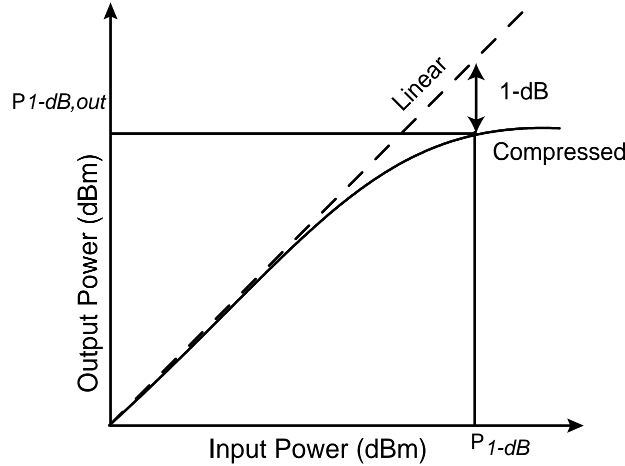


Figure 3.1: Definition of 1-dB Compression Point (after [50]).

level falls 1-dB below its extrapolated linear value at the 1-dB compression point. Typically the gain decreases rapidly beyond this point.

3.2.2 Intermodulation distortion

Non-linearities in an amplifier give rise to two types of signals: harmonics and intermodulation distortion (IMD). IMD consists of the distortion products occuring due to mixing of any two harmonic frequencies. Intermodulation distortion is usually measured with an RFinput signal composed of two sinusoidal tones (ω_1 and ω_2) of equal amplitudes but closely spaced frequencies (two-tone test) such that

$$\omega_2 - \omega_1 = \Delta\omega << \omega_c \ ,$$

where ω_c is the carrier frequency. Due to non-linear effects in the amplifier, the resulting RF output consists of various intermodulation products (in addition to the amplified version of the two fundamental tones and their harmonics. see Figure 3.2). Another measure of linearity is the ratio of fundamental to intermodulation power [also called carrier to intermodulation ratio (C/I)].

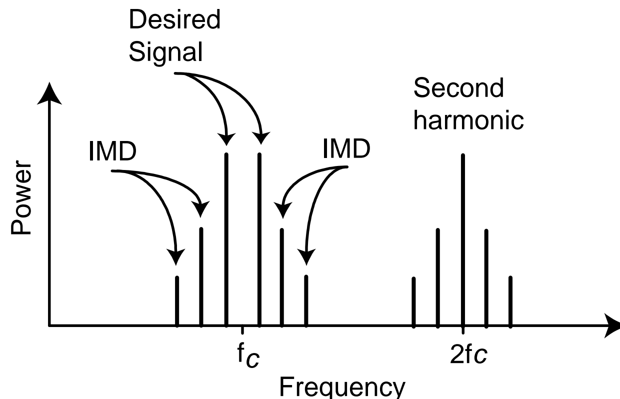


Figure 3.2: Distortion products in a RF Power Amplifier (after [51]).

3.2.3 Intercept point

Of all the intermodulation products, the third order intermodulation (IM3) products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are of particular concern as they appear in the vicinity of the fundamental tones ω_1 and ω_2 (the difference between ω_1 and ω_2 is small). The point where the fundamental response and the third-order spurious response intersect is known as the third order intercept point (IP3) [51]. In most practical cases, the amplitudes of the fundamental linear term as well as the third order intermodulation products compress well before reaching this point. In those cases, the intercept point is measured by extrapolating the fundamental and IM3 output characteristics (see Figure 3.3). IP3 serves as a better measure of linearity in comparison to the intermodulation products themselves as it can be specified independent of the power level [52].

3.2.4 Adjacent Channel Power Ratio

Adjacent channel power ratio (ACPR) characterizes how the main channel power spills over into the adjacent channels due to the nonlinearity of the PA. ACPR is widely used with modern digitally modulated systems. Basically ACPR is the ratio of power of the signal in the adjacent channel to the power of the signal in the channel carrying the modulated signal (see Figure 3.4. Usually ACPR is measured in terms of dB with respect to peak carrier power (dBc).

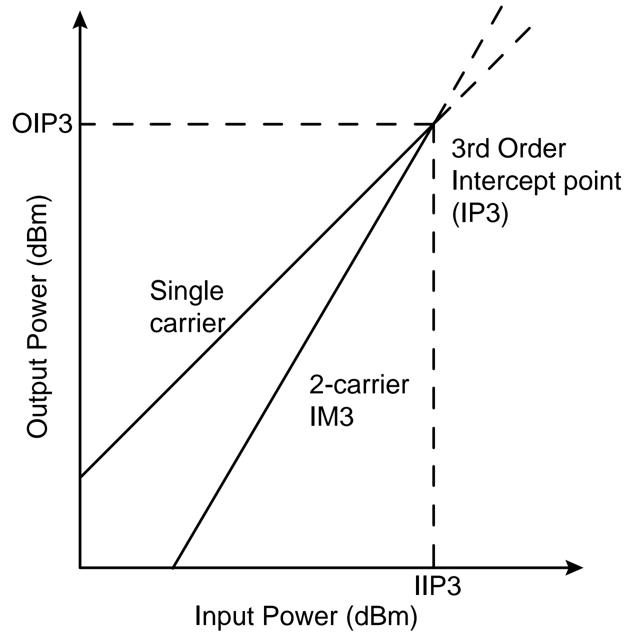


Figure 3.3: Single carrier and two-carier IM3 Power Amplifier Characteristic (after [52]).

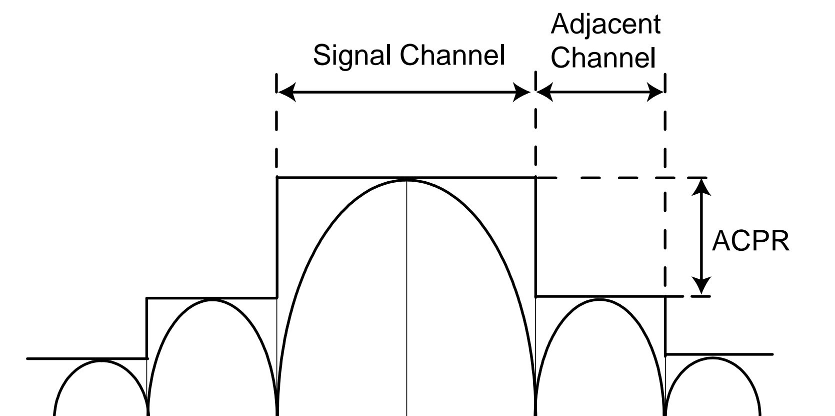


Figure 3.4: Spectral mask showing adjacent channel power.

3.2.5 Error Vector Magnitude

The 1-dB Compression Point alone is not an accurate measure of linearity for PAs as it is primarily a voltage domain function and the voltage limiting characteristic may be gradual or more abrupt. Real communication systems use complex waveforms which involve significant time varying voltage fluctuation [53]. For example, an OFDM signal contains voltage excursions that are five times greater than its average value (14-dB power ratio) while a single sinusoidal carrier has a peak-to-average ratio of about $\sqrt{2}$ (3-dB power ratio). Consequently a linear PA needs to be "backed off"; the average output power of the PA should be lower than its linear power-handling capabilities so that the voltage excursions do not push the PA into compression.

Error Vector Magnitude (EVM) is another measure of nonlinearity which better characterizes how the signal detection process is affected due to the non-linearities of the transmit PA. As shown in Figure 3.5, EVM is the scalar distance between the desired and actual (measured) constellation points. Expressed another way, EVM represents the residual noise and distortion remaining after an ideal version of the signal has been removed [54].

$$EVM = \sqrt{(I - I_{actual})^2 + (Q - Q_{actual})^2} \ , \tag{3.4}$$

where I and Q are the quadrature components of the measured signal, and I_{actual} and Q_{actual} are the quadrature components of the reference signal.

3.3 PA Classification

PAs consume significant power and scaled up versions of small-signal amplifiers are fundamentally incapable of providing high efficiency. Hence, other approaches must be considered which involve tradeoffs among linearity, power gain, output power and efficiency.

Power amplifiers may be classified into several categories, depending on their operating bandwidth (broadband and narrow band), and whether they are intended for *constant-envelope* or *linear* operation [55]. The class of operation is basically deter-

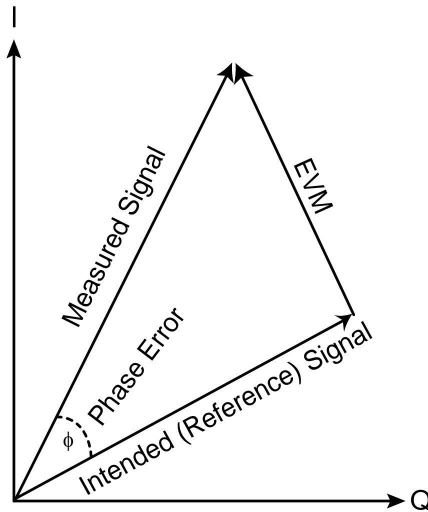


Figure 3.5: Illustration of Error Vector Magnitude (after [54]).

mined by the operating point (also called the Q-point) on the load-line drawn on the output IV characteristics of the power transistor(s). Alternatively, class of operation can be specified in terms of the conduction angle (α) which is a measure of the time during which the transistor(s) is (are) conducting (ON). Some of the common classification of PAs are discussed briefly in the following sub-sections.

3.3.1 Class A Amplifier

A transistor is generally assumed to be linear if it operates in the region of operation between cutoff and saturation (triode in FETs). Linear operation will result if an amplifier is biased at the exact midpoint of the linear region, providing the RF drive signal never exceeds the boundary values (cutoff and saturation voltage). In principle, a perfectly sinusoidal input signal will result in a perfectly sinusoidal output current without any harmonics. Such an amplfier is said to be a class A amplfier.

Ideally a class A amplifier can be considered to be linear for a limited range of input drive. In reality, the linear region contains weak non-linearities which become more evident as the signal drive level increases. Finite variation of β with collector current (I_c) in bipolars will result in non-linearities; in FETs there is a fundamental non-linearity due to the square law relationship between input voltage and drain current

(I_d). These non-linearities generate significant harmonic content in case of Class A operation. However, a reactive matching network (typically used to transform the 50 Ω antenna load to the optimum load resistance which the transistor wants to see) can act as a filter attenuating the generated harmonics thus giving a cleaner output signal [52].

The operating point of a Class A amplifier is the center of the active region (the signal level should not push the transistor into cutoff or saturation). Figure 3.6 shows the operating point (Q-point) of a class A amplifier on a current/voltage transfer characteristics. Since the transistor is always in active region, the device is always conducting (even when there is no RF signal). Thus the transistor is constantly drawing current which represents continous loss of power. In other words, the conduction angle of the Class A amplfier is 2π (See Figure 3.7). As a result, Class A amplifiers have the lowest efficiency of all classes of operation. On the other hand, the transistor is biased at the center of the active region and hence these PAs have very good linearity. As a result, it is advisable to use Class A amplifiers in cases where linearity is a stringent requirement but power consumption (efficiency) is less of an issue. It can be shown that the theoretical maximum efficiency of a Class A PA is always $\leq$ 50% [51]. In an inductorless system with resistive loading, the output voltage cannot rise beyond the supply voltage and hence the efficiency is limited to a theoretical maximum of 25% [56]. Class A RF Power amplifiers are typically used as low-level driver amplifiers [51] where the power consumption is a very small portion of the total power consumption.

3.3.2 High Efficiency amplifiers

This section deals with "reduced conduction angle", high-efficiency RF power amplifiers. Biasing the active device to a low quiescent current and allowing the RF signal to drive the device into cut-off is a traditional method of making high efficiency RF amplifiers. However, the reduction of conduction angle alone is not sufficient to obtain useful improvement in efficiency. By providing suitable impedance terminations at harmonics of the signal frequency, considerable improvements in efficiencies can be obtained. This section discusses on some of the commonly used high-efficiency amplifiers.

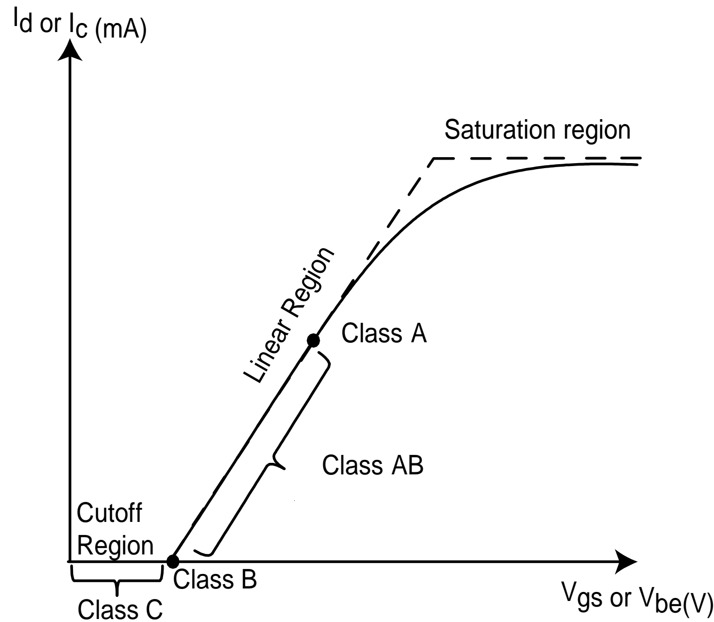


Figure 3.6: Q-point of Class A, AB and B type amplfiers. Dotted line represents an ideal response. Solid line shows the more realistic weakly non-linear response.

Class B

Class B amplifiers are much more efficient than Class A amplifiers. For medium and high power applications, Class B is generally used. In a Class B amplifier, there are generally two transistors, one drives the current into the load while the other draws the current out of the load. Hence this configuration is generally called a "push-pull" configuration. From the Q-point perspective, the two transistors are biased just at their turn-on voltages as shown in Figure 3.6. The two transistors are driven 180° out of phase so that each one is active for half of a cycle and cutoff during the other half of the cycle. Moreover, as the devices are biased at the edge of turn-on, there is no current flow with no applied signal, thus Class B attempts to maximize the efficiency. The conduction angle of a Class B amplifier is π (see Figure 3.7).

In the ideal case, the efficiency of a Class B amplifier can approach a maximum of 78% [51]. In practice, as the drain/collector voltage swing is less than maximum and due to additional losses in the circuit, PAE of Class B implementations may reach as high as 63% [57]. However, *Crossover distortion* occurs when the signal is transferred from one device to the other which degrades the linearity of the PA [58]. Due to lack

of high-speed p-type devices in most bipolar and FET technologies prohibits the use of push-pull configuration.

Class AB

Class AB operation falls between Class A and Class B (see Figure 3.6). For example, the push-pull concept (with improved efficiency as compared to a Class A architecture) can be used, while at the same time improving the linearity (as compared to a Class B architecture) by minimizing *crossover distortion.* As shown in Figure 3.7, the conduction angle α is greater than π (pure Class B) but less than 2π (pure Class A). Thus each device conducts for a slightly longer period of time, which smooths out the output voltage waveform during the crossover period. This approach can therfore provide linearity closer to class A and efficiency closer to class B. Depending on the linearity and efficiency requirements, the designer can choose the bias point appropriately (closer to threshold for higher efficiency or closer to the centre of the load line for better linearity). RF PAs in Class AB architectures have been widely reported in the literature, with efficiencies ranging between 30% to 60% [59],[60].

Class C

In a Class B amplifier, each transistor is biased at threshold and conducts for half a cycle. In a classical class C amplifier, the transistor is biased below threshold (See Figure 3.6) so that the transistor is active for less than half of the RF cycle. Because of this biasing strategy, the efficiency is increased, since the device is on for less than half of the cycle [the conduction angle is less than π (See Figure 3.8)], but the linearity is significantly degraded. The efficiency can be increased theoretically to a maximum of 100% if the conduction angle goes to $0°$. Of course this causes the output power to decrease to 0 since no current is being delivered to the load. A compromise of, for example, $\alpha = 150°$ can result in a PAE of 85% [61]. Such a PA can be used in applications with constant envelope modulation schemes where linearity is not a major concern.

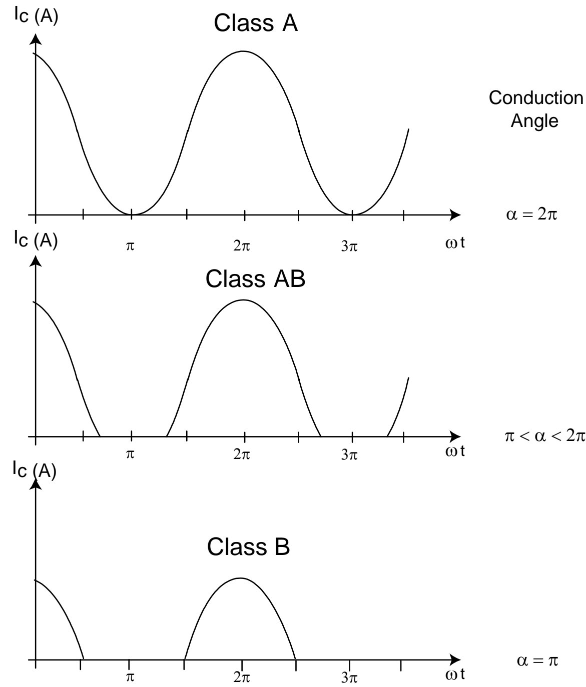


Figure 3.7: Conduction angle relations for Class A, B and AB Power Amplifiers.

Class D

A typical class D PA uses two or more transistors as *switches* to generate a square-wave voltage at its drain/emitter. This waveform is then applied to a network consisting of a load resistance and series tank circuit. The two transistors switch the LCR resonator between DC and ground for alternate half cycles. The frequency at which the transistor is switched is assumed to be equal to resonant frequency of the LCR circuit. Figure 3.8 shows the current and voltage waveforms for a class D configuration. The current remains a sinusoid without any DC offset due to the resonator and the series blocking capacitor present at the output of the PA. As a result, each transistor conducts for half a cycle, and the required output sinusoidal wave results from superimposing the two half-cycle sine waves. Since the switching waveform is ideally a square wave, no power is dissipated in the switch; current is drawn only through the "on" transistor resulting in an ideal Class D efficiency of 100 %. One notable aspect of Class D is that efficiency is not degraded by the presence of reactance in the load (assuming that the Q-factor of the inductor and capacitor of the series tank circuit

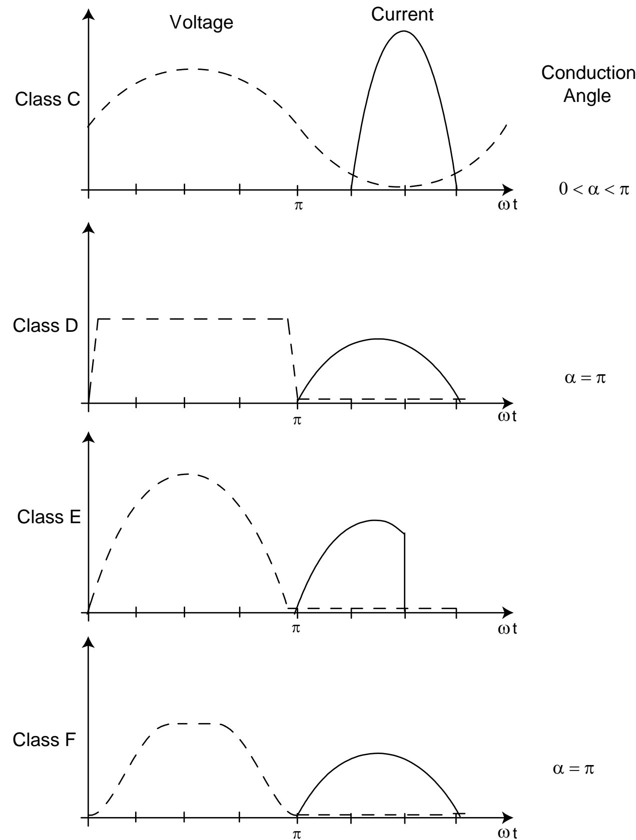


Figure 3.8: Current and Voltage Waveforms for non-linear PAs (after [49]).

is high). Some of the issues with a Class D design are the losses due to transistors in saturation, drain/collector capacitance, and switching speed. For a MOS device, the power loss is directly proportional to $\frac{V_{DD}^3}{2}$ [62], and increases in proportion to the operating frequency.

Class E

Class E employs a single transistor operated as a switch shunted by a capacitor. In addition to this shunt capacitor, a series passive load network (LCR) is also connected across the transistor. As with the Class D amplifier case, the Q-factor of the resonator is assumed to be high enough to force a pure sinewave current (due to the flywheel effect) into the LCR branch. The DC voltage is supplied through a high-reactance choke. Two currents combine to flow into the switch-capacitor combination; the dc

supply current and the sinusoidal resonant current in the LCR branch. When the switch (transistor) is ON, the collector is shunted to ground, current through the capacitor is also zero. When the transistor is OFF, the collector voltage waveform is produced by charging of the shunt capacitor. When switch changes from OFF to ON, the charge in the capacitor is rapidly discharged. Figure 3.8 shows the voltage and current waveforms for a Class E amplifier. The key point of operation is the near instantaneous transfer of current from the transistor to capacitor when the switch opens. The current and the voltage never coexist and hence there is theoretical 100% efficient conversion of DC to RF. MOSFET Class E amplifiers have been used as high-efficiency, high frequency switching amplifiers with power levels up to 1kW [63].

Class F

The Class F amplifier is one of the oldest techniques available to improve efficiency. This approach uses harmonic resonators in the output network to shape the output waveforms. A class F amplifier is nothing but a class B amplifier designed using an odd harmonic trap[1] connected between the supply and the active device. This configuration gives better performance than with an inductive choke which is limited by its Q-factor. The transistor output is connected to a load via a high Q resonator, so as to provide open-circuit terminations at higher odd harmonics. Figure 3.8 shows the voltage and current waveform a class F configuration. Since the devices are biased in Class B operation, the current waveform will be a half-sinusoidal waveform. The voltage waveform appears to have a square-wave like appearance due to the quarterwave even-harmonic short, coupled with the clamping effect occuring near the turn-on region of the transistor. Alternatively in an inverse class F configuration, the voltage is approximately a half sine wave and current is approximately a square wave. Squaring up of the sinewave can be improved by adding higher order odd harmonic traps which lead to an ideal class D amplifier. At any instant of time the voltage and current are not present simultaneously and hence the theoretical maximum efficiency is again 100 %. [64] and [65] discuss the harmonic generation and manipulation mechanisms to optimize class F performance.

[1] An odd harmonic trap is a quarterwave transmission line stub which when connected appropriately has the advantage of being an open circuit at the fundamental and presents a short circuit at successive even harmonics.

To summarize, linearity and efficiency are two opposing requirements in PA design. The Class A amplifier is considered linear within a limited range of input drive. Class AB, B, C and F amplifiers are classified as high-efficiency amplifiers, and use the active device as a controlled current source. These classes improve the efficiency by reducing the conduction angle and driving the active device into cut-off region for a portion of each cycle. Another approach to improve the efficiency of PAs is to use the active device as a switch (since ideally a switch disipates no power). Class D and E amplifiers operate based on this approach. There are a number of other approaches to power amplifier design such as Class S, Doherty, Chireix outphasing amplfier which are beyond the scope of this thesis − for further information, the reader is directed to [52] [51].

Class AB amplifiers provide the flexibility of providing either good linearity by biasing them close to Class A operation or high efficiency by biasing them close to Class B region of operation. The baseline design is a 3-stage SiGe PA designed for WLAN 802.11 b/g applications. Based on the requirements of a linear PA design, the three stages of the PA were biased in Class AB operation but closer to a Class A bias point in an attempt to improve the linearity. This design was then extended to design the completely ESD protected PA targeted for DECT application, and the bias point was moved closer to Class B operation in order to improve the overall efficiency of the PA. Some of the approaches used for the design, and a discussion on the baseline PA will be provided in the following sections.

3.4 Design Approach

An important priority in the baseline PA design is to achieve the specified gain at the required output power over the desired frequency band. In order to achieve the required output power, linearity and matching, design decisions including the choice of device technology, multi-stage design and the use of tuned matching networks were made. Each of these techniques will be discussed in the following sub-sections.

3.4.1 Device Technology

Chapter 1 presented a discussion of GaAs, Si and SiGe technologies and their relative advantages and disadvantages. GaAs technology has historically offered advantages that offset its higher cost relative to Silicon-based technologies. However, advances in the silicon industry have resulted in SiGe devices that are now able to compete directly with GaAs devices. SiGe HBTs have potential cost advantages compared to GaAs and also allow for RF/mixed-signal integration with standard CMOS technology. SiGe HBTs offer higher early voltage, breakdown voltage and g_m (as compared to Silicon BJT's) and comparable f_t (as compared to GaAs devices). Given these advantages, SiGe HBT technology was chosen for the PA designs in this project.

3.4.2 Multi-Stage Design

The linear WLAN PA has a high gain requirement (30 dB); consequently a multistage design is indicated since the desired gain cannot be obtained using a single stage. The optimum drive level at the input of the PA is about -10dBm. Therefore the first stage of the PA could be small, while the required output power (20 dBm) necessitates large output stages. A multistage PA is needed with devices, increasing in size through each of the stages. A major restriction on the PA is that its power consumption increases while efficiency decreases as multiple stages are added. The transistors in the SiGe technology used, provided an average power gain of about $8 \sim 10$ dB per stage. Thus an optimum value of three stages was chosen which allows to meet the gain specification by gradually increasing the size along the stages and also place a reasonable limit on the DC power consumption.

3.4.3 Tuned Design

The well-known maximum power transfer theorem is not strictly relevant in power amplifiers (especially in designing an output circuit). One reason is that it is not straightforward to define impedances in a large-signal environment. Furthermore, assuming it is possible to arrange for a conjugate match, only half of the power available at the output of the transistor can be transferred to the load, which is

highly unacceptable in many cases. In general, a PA is designed to deliver the specified amount of power into a load with the highest achievable efficiency based on power gain and linearity [55]. Acceptable gain and linearity can be achieved using the LC tuned circuits which also help in tuning out the capacitances that reduce the f_t of the transistors.

3.4.4 Off-Chip matching

Although the maximum power transfer theorem is not strictly relevant in designing the output circuit of a power amplifier, it is very important in designing the input circuit. Driving PAs at large signal levels present a serious design challenge and hence an input impedance match to the driving source is critical. As far as the output of the PA is concerned, the antenna rarely presents a nominal load to the PA, because its impedance is influenced by the environment. Furthermore, the transistor wants to see a load impedance other than that of the antenna in order to obtain maximum gain, and hence a matching network is also needed at the output of the PA. The same argument could be extended for interstage matching as the output of one stage of a PA would require a load impedance different from the input impedance offered by the succeding stage.

The Q factor represents the loss of a tuned L-C circuit. For an ideal parallel LC resonant circuit, the Q is infinite, and therefore no current needs to be supplied by an external source since the structure will resonate with an initial excitation. However, in reality, Q's are finite and the circuit will lose some amount of energy (current) during each cycle due to the losses in the parasitic resistive components of inductor and capacitor. The realizable range of values of Q for off-chip components ($100 \sim 1000$) is much higher than the Q-factor of available on-chip components ($5 \sim 25$). Off-chip components have much lower parasitic loss and hence the amount of current that needs to be replenished is also low.

3.5 Baseline Power Amplifier Design

This work focuses on the development of ESD protection circuitry which can be directly integrated into high-performance RFIC PAs with minimal impact on RF performance and cost. The baseline amplifier (see Table 3.1 for detailed PA specification) was designed by M/A-COM (Lowell, MA) to target WLAN 802.11 b/g applications, with a high gain of 30 dB for output power ranges of 18 dBm to 22 dBm. All three stages of the amplifier were biased Class AB, but the 1st stage was biased closer to Class A in order to obtain higher linearity (at the expense of efficiency). The allowable supply voltage range varies from 1.5 to 3.6 V; maximum current drawn is less than 200 mA with a standby leakage current of 3 μA. The PA chip is fabricated using a commercial 0.5 μm SiGe-HBT process with high Q on-chip inductors and was packaged in a 3mm Fine Pitch Quad Flat Package FQFP-N 12 lead package. Figure 3.9 shows the functional board level block diagram of the power amplifier. The input, output and interstage matching were performed off-chip using microstrip transmission lines and capacitors based on performance advantages and cost related benefits. Input (RF_{in}), Output (RF_{out}), Control lines (V_{en}), Supply lines (V_{cc1} and V_{cc2}) and the three stage grounds(Gnd_1,Gnd_2 and Gnd_3) require ESD protection.

The baseline PA was redesigned to provide protection to only RF input and control lines. The protection techniques were later extended to provide protection to supply and RF output of the PA. The design of the partially protected and fully protected PAs are discussed in the succeeding chapters.

3.6 Summary

This chapter has provided a brief overview on some of the important concepts in power amplifier design, and discussed the design requirements for the baseline power amplifier which was later redesigned to provide ESD protection. The next two chapters deal with the specific design techniques used for the full ESD protection of a SiGe HBT power amplifier. Simulation and measurement results are presented for a fabricated prototype partially protected power amplifier.

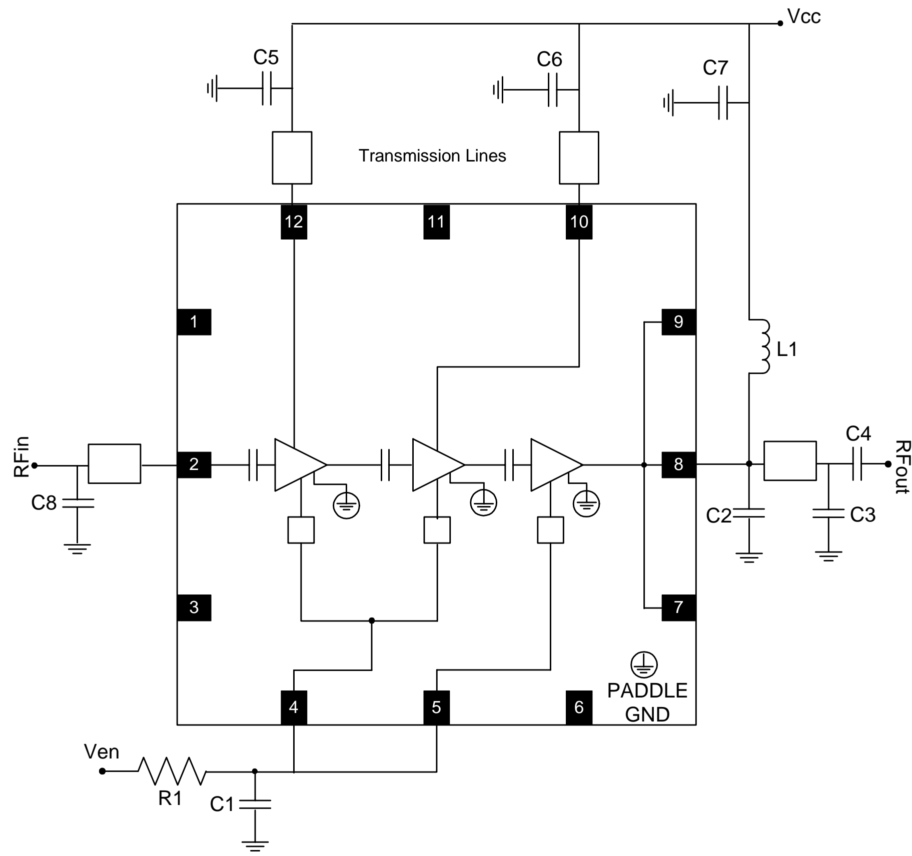


Figure 3.9: Functional Schematic of the 2.4GHz WLAN Power Amplifier.

Table 3.1: WLAN Power Amplifier Specification.

Parameter	Specification	Units
Frequency	$2.4 \sim 2.5$	GHz
Gain	30	dB
Input VSWR	1.6:1	–
1-dB Compression	26.5	dBm
Bias Voltage	$1.5 \sim 3.5$	V
Current	200	mA
Off Current	3	μA
Isolation	< -40	dB
Harmonics $2f_o, 3f_o$	-30	dBc
Linear Output Power @ 3% EVM	18	dBm

Chapter 4

Partially Protected WirelessLAN PA

The goal of this research was to design a completely ESD protected SiGe HBT Power Amplifier. This is a significant advancement in the current state of the art of PA's, as no PAs with integrated ESD protection structures have been published to date in the literature. Recently more Si/CMOS PAs have been reported [66] [67].

In this chapter the SiGe PA design for 2.4GHz WLAN applications is enhanced with partial ESD protection. The different ESD protection schemes used are discussed in detail. Small signal and large signal simulations of the PA design are presented. Measured results are then shown, including the PA's performance under standard HBM and MM tests.

4.1 Partially protected PA chip

A package level block diagram of the partially protected PA is shown in Figure 4.1. In this design, only the RF_{in} and the control pins ($V_{en1,2}$ and V_{en3}) were protected on the prototype WLAN PA (refer to Section 3.5). Widths and lengths of the metal traces were extracted from the layout and their parasitic contributions were modeled by approximating them as transmission lines using appropriate microstrip substrate models. Subsequent simulation results incorporate the effects of these interconnect

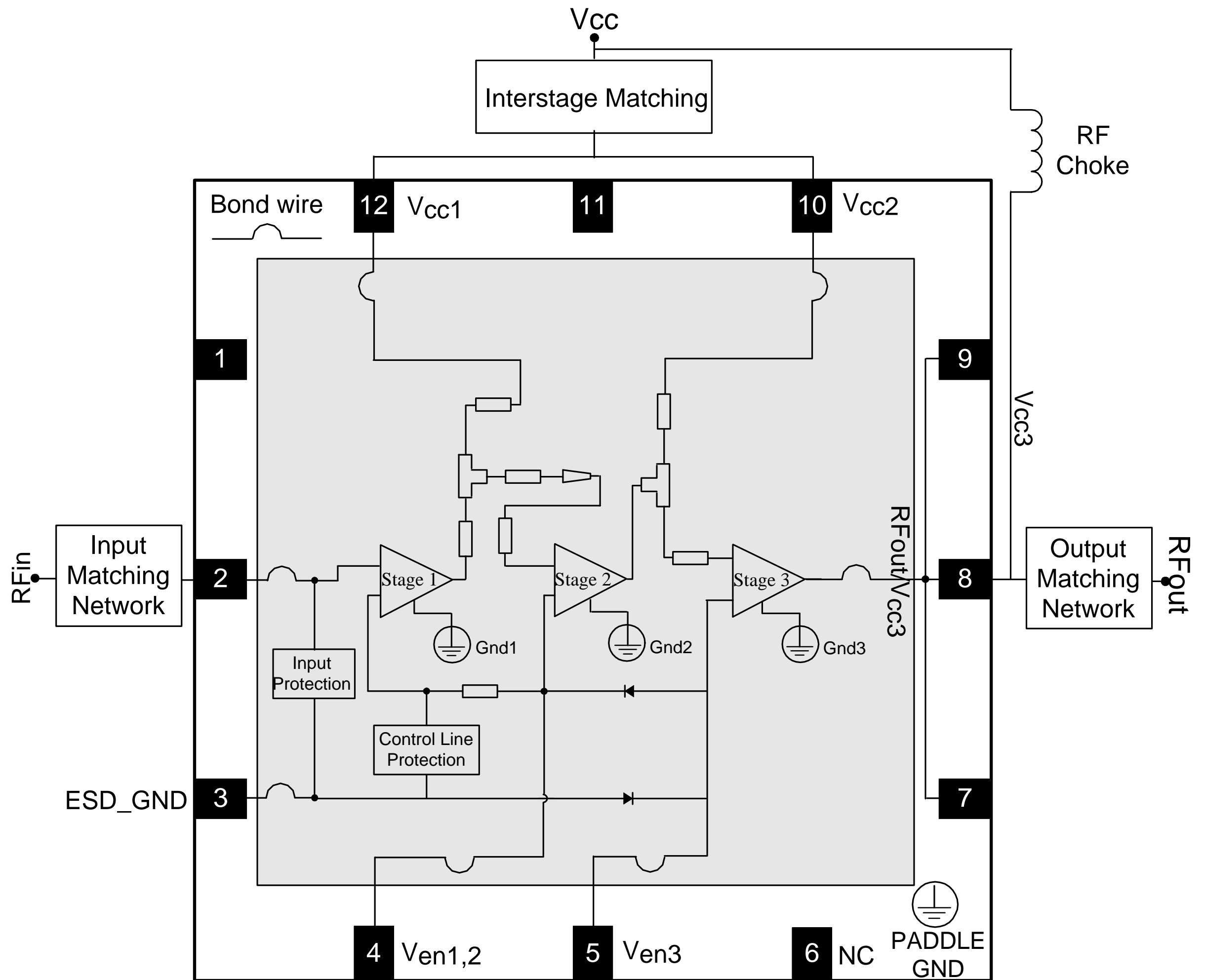


Figure 4.1: Block diagram of the partially protected 2.4GHz WLAN Power Amplifier. Microstrip transmission lines represent the parasitics of the laid out traces.

parasitics. Four separate ground pads were used, one each for the three stages, and one common ground pad for the input and control pin protection circuit, in order to minimize coupling of RF signals between the stages and also to the ESD ground (ESD_Gnd). The ground pads of the three stages of the PA were connected to *Paddle* ground, whereas the ESD_Gnd was assigned a separate ground pin. Since the input protection circuit was connected between the input pin and ESD_Gnd, separating the ground pin from the main stage grounds minimizes leakage of RF signals from the 2nd and the 3rd stage into the 1st stage. The control signals (V_{en}) for the first two stages were tied together, while the third stage had a separate control pin. In order to isolate the three stages, separate power supply pins (V_{cc1}, V_{cc2}) were used for the first two stages. To minimize the pin count, the third stage supply pin (V_{cc3}) was allowed to share a pin with RF_{out} on the chip level. This also facilitates the use of an off-chip high-Q choke. Interstage matching (both stage1-stage2 and stage2-stage3), as well as input and output matching networks were realized off-chip for the reasons specified in Section 3.4.4. The design of the RF Input and control line protection schemes will be discussed in the following sub-sections.

4.2 ESD Protection Schemes

As mentioned earlier, only the *RFinput* (RF_{in}) and the control ($V_{en1,2}$ and V_{en3}) pins were protected in this PA design. In Chapter 5, a fully ESD protected version building on this work will be described. The *diode ring* approach (as described by [31]) was initially used for protecting the control pins; this was later replaced by the *Zener* approach. An *LC tank* approach (as demonstrated for 5.2 GHz LNA in [68]) was used to provide protection at the *RFinput.* The LC tank approach was later modified such that, apart from protecting the *RFinput,* it could be used to replace the off-chip input matching network by an on-chip shunt-L-series-C matching network.

4.2.1 ESD diodes

Chapter 2 provided a brief introduction into using diodes for ESD protection. Since diodes are robust for ESD protection purposes, it is critical to understand the behavior of diodes from this perspective.

An ideal diode will have a current in forward bias described by the Shockley equation

$$I_D = I_s \left[e^{\left(\frac{V_D}{V_t}\right)} - 1 \right] \ , \tag{4.1}$$

where I_s is the *reverse saturation current*, V_D is the forward bias voltage and V_t is the thermal voltage given by $\frac{kT}{q}$ (26mV at 300K). For $V_D \gtrsim V_t$, the factor of 1 can be neglected. The diode in forward bias is also characterized by its series resistance R_S. Therfore, the voltage supported by a diode is given by

$$V_D = V_t \bullet \ln \left(\frac{I_D}{I_s} \right) + I_D R_S \ . \tag{4.2}$$

During an ESD event, the current flowing through the diode will be large and hence the $I_D R_S$ drop needs to be considered. In addition, the forward (turn-on) voltage decreases as the temperature is increased:

$$V_{on}(T_1) = nE_{go} + \left(\frac{T_1}{T_0} \right) \left[V_{on}(T_o) - nE_{go} \right] \ , \tag{4.3}$$

where $E_{go} = 1.206V$ (bandgap voltage of Si at 0K) and n is the diode ideality factor; T_1 and T_o are the new and the original temperatures.

The diode performance varies significantly based on the technology used. For example, the well formation in a CMOS process can make the diodes in a CMOS process a three terminal device. In many processes, a diode is actually a PNP transistor with either the base connected to the emitter or collector. Due to transistor action, this can be both detrimental or beneficial from an ESD perspective.

Cascaded Diodes

If ideal diodes are cascaded in series, the cut-in voltage V_{on} (the minimum voltage above which the diode begins appreciable current conduction) increases linearly with the number of diodes in series. However, some processes have non-ideal, transistor-based collector-base (CB) junction diodes (a transistor with its base shorted to the emitter). In reality the cut-in voltage of a cascaded CB diode does not scale linearly. Due to the transistor current gain effect, there is a reduction in the cut-in voltage of the next stage. This action is repeated at every stage. Thus the sum of voltages in

a cascade of transistor-based diodes is smaller than that in the case of ideal diodes. The cut-in voltage of two identical cascaded diodes is given by:

$$\ln \frac{I_1}{I_s} = \frac{qV_1}{nkT} \ ,$$

$$\ln \frac{I_2}{I_s} = \frac{qV_2}{nkT} = \ln \frac{I_1}{(\beta+1)I_s} = \ln \frac{I_1}{I_s} - \ln(\beta+1) \ ,$$

$$V_2 = V_1 - \frac{nkT}{q} \ln(\beta+1) \ , \tag{4.4}$$

where I_1,V_1 and I_2,V_2 represent the forward current and cut-in voltages of the cascaded diodes. Thus the transistor action opposes linear buildup of forward voltage. It is also found that increased temperature during an ESD event further reduces the forward voltage [31].

Cascading diodes increases the effective cut-in voltage, but also the total series resistance. During an ESD event, the current flowing through the diodes will be large and hence the series resistance needs to be considered. In order to keep the ideal diode chain resistance constant, the diode area must be scaled up by a factor equal to the number of diodes (n) in the chain. This increases the chain area by a factor of n^2. The negative aspect of transistor based diodes is the non-linear increase in the cut-in voltage; as a result more diodes may be needed in the cascaded structure. On the other hand, with real diodes the resistance in the forward path becomes less than that of an ideal cascaded chain.

Once the diode turns on, only a small voltage is required to increase the current through it. In other words, the AC or dynamic resistance of the forward biased diode is small. The dynamic resistance can be calculated by

$$R_n = R_d \left(1 + \frac{1}{(\beta+1)^{n-1}}\right) \ , \tag{4.5}$$

where R_d is the individual diode resistance and R_n is the total resistance of the chain of n diodes. For small β, the diode chain's resistance decreases drastically, while for large β, the chain resistance approaches that of a single diode. An ideal diode chain, on the other hand, has series resistance of nR_d. In a CB diode, the effective resistance is somewhat between R_d and nR_d. Hence in a CB diode chain, it is not necessary to

Table 4.1: ESD Diode Capacitance.

	Capacitance @ 0V, f =2.45GHz		
	Area (μm^2)	C (simulated) (pF)	C (measured) (pF)
Zener	50x30	2.46	2.112
CB	20x20	0.329	0.393

scale the diode chain area by n^2 to maintain the chain resistance but to a smaller degree as indicated by Eq. 4.5. Thus CB diodes seem to be better suited for creating series cascaded diodes. The next sub-section discusses about the diodes available in the design kit.

4.2.2 Diodes in the available technology

The available fabrication technology supports two non-scalable ESD diode structures (*Zener based* and *HBT based CB junction* diodes) that have been qualified against the HBM test. The different diode structures were laid out separately and a sawed wafer section (unpackaged) was probed using GSG RF probes. Dynamic and Static I-V measurements were then performed using a pulsed I-V analyzer (Accent DIVA D265). As the probe pads add considerable loss to the measurements (because they act as large shunt capacitors) open and short circuited pad structures were also laid out and the parasitic effects of the pad structures were de-embedded from the measurements. The results show that *Zener based* diodes have a breakdown voltage of about 7V while the HBT based CB junction diodes have a breakdown voltage of about 21V. All diodes have a cut-in voltage (V_{on}) of approximately 0.7V. Figure 4.2 shows that the diodes have relatively low on resistance in the forward biased region. Small-signal measurements show that the CB diode has the lowest diode capacitance (refer to Table 4.1) which is attributed to its smaller size. Hence the CB diodes were used for control line protection which is detailed in the next section.

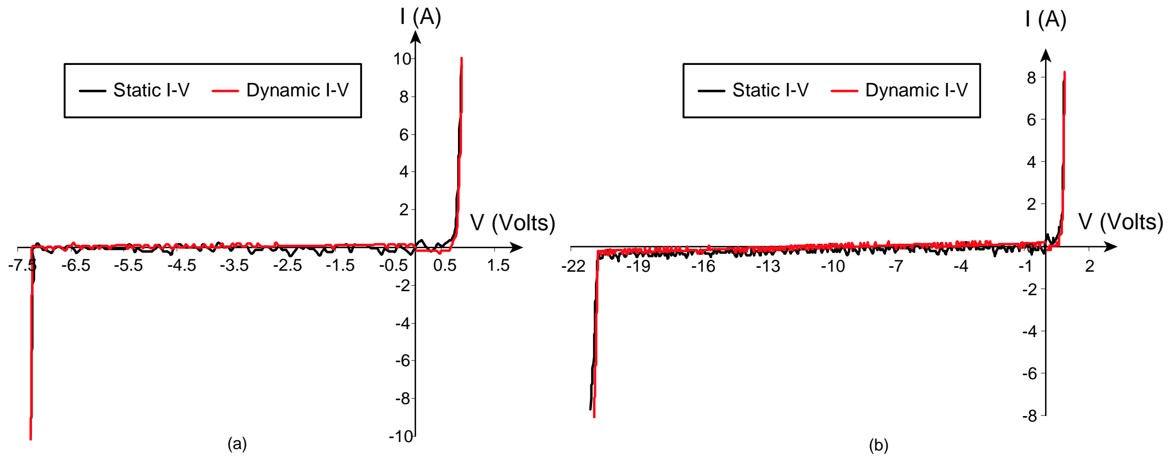


Figure 4.2: (a) Zener based and (b) CB based diode Static and Dynamic I-V characteristics.

4.2.3 Control line protection schemes

Figure 4.3(a) shows the diode ring approach [31] used to protect the stage1 and stage2 control line ($V_{en1,2}$ - refer Figure 4.1 for location of circuit). The following factors were considered in the construction of the diode ring:

- The maximum voltage difference between the two supplies being clamped;
- Temperature of operation; and
- Burn-in requirements;

The voltage difference (ΔV) between supplies ($V_{en1,2}$ and ESD_Gnd) is the most important factor in determining the number of diodes needed in the cascade clamp (forward biased series diodes) of the diode ring. The number of diodes should prevent actuation of the ring during normal (non-ESD) operation (1.6 $\sim$ 3V). Under normal operating conditions, the diodes operate in reverse biased operation, and hence the leakage through the diodes should be minimized. 5 diodes were used in this case, each with $V_{on} \simeq 0.7V$ [$5 \times 0.7 = 3.5V > 3$V (maximum supply voltage)]. The diode ring should also provide protection against *positive* and *negative* ESD events (refer to Section 2.4.1). For a positive ESD strike, the cascade clamp in the diode ring starts conducting once the control voltage increases to a value sufficient to turn

on all the diodes in the string, thereby protecting the core circuit. There will be a slight voltage excursion (due to diode series resistances) for a short period of time (few ns). For a negative strike, the reverse biased diode in the ring turns on at its V_{on} thereby preventing the strike from reaching the PA. The size of the diodes used for protecting control pin(s) is important, as the total capacitance at the pin must be charged/discharged during PA cycling. CB junction diodes were therfore used in the diode ring because of their minimal size (20x20μm^2) and lower capacitance (0.393pF). The diodes available in the design kit were non-scalable and hence parallel pairs of diodes were actually used in the ring in order to reduce the equivalent resistance of the diodes thereby reducing the voltage overshoot. However this does have the drawback of increased capacitance on the control pin.

A two-diode approach [31] was used to protect the stage3 control pin (V_{en3}). In this approach the diode D1 [diode connected between V_{en3} and $V_{en1,2}$ in Figure 4.3 (b)] transfers any positive ESD strike on V_{en3} pin to $V_{en1,2}$. The diode ring present on $V_{en1,2}$ pin subsequently gets triggered, thereby averting the strike. This technique is slightly better for negative ESD strikes as the diode D2 (the diode connected between V_{en3} and ESD_GND) transfers negative ESD strikes directly to ESD_GND.

The above mentioned methods can be used for protecting the RF-input/output. However, the total diode capacitance can impact the RF performance. It may be difficult to absorb the capacitance into the input matching network as the junction capacitances of the diode vary with voltage. It is interesting to note that only the diode's forward bias characteristics are utilized to protect the core circuit from an ESD strike. Hence, if the diode ring approach is used, the protected device becomes indifferent to the polarity of ESD strike. Either the reverse biased diode (for negative strike) or string of diodes (for positive strike) turn-on once the voltage on the pin exceeds it normal operating voltage by V_{on}. The same argument holds for the two-diode approach.

4.2.4 RF Input Protection

ESD currents typically have a lower frequency spectrum as compared to the desired RF signals. Therefore a protection circuit can be designed that essentially acts like a low pass filter. The basic electrical component with such a characteristic is an

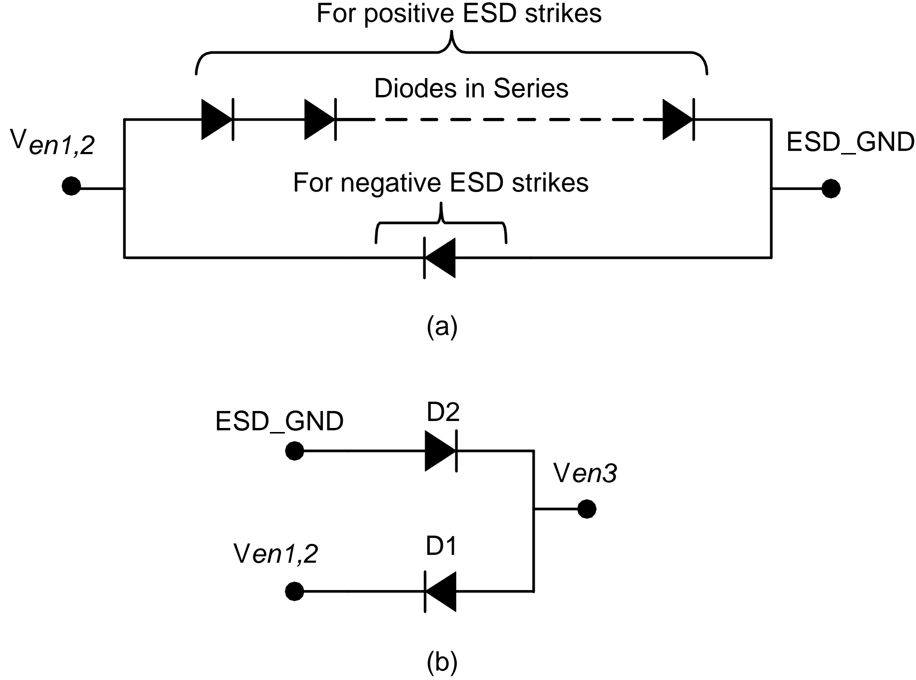
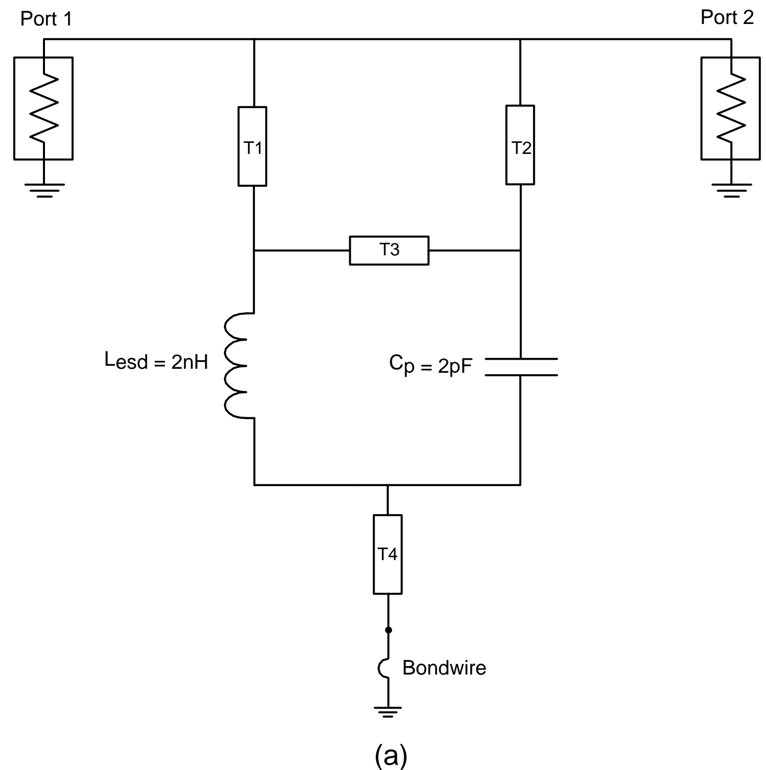


Figure 4.3: (a) Diode ring approach and (b) Two diode approach for Control line Protection.

inductor. Therefore, an on-chip shunt inductor at an RF port can divert ESD strikes to ground. While a normal ESD protection structure adds parasitics to the device, this inductor can be designed to tune out the parasitics at the port [68]. On the other hand, the inductor acts like a shunt path to ground at ESD frequencies. An external capacitor may be added to obtain a more realizable value of on-chip inductance. Figure 4.4 shows the LC tank scheme used to protect the RFinput pin of the PA. The on-chip inductor (L_{esd}) was used to tune out the parasitic capacitance at the input of the PA; an external capacitor C_p was added to minimize the value of the inductor. An optimum value of inductance (2 nH) and capacitance (2 pF) was chosen after considering the trade-offs between their sizes, the series loss added and bandwidth requirements. Transmission lines T1, T2, T3 and T4 are included to account for the parasitics due to the metal lines and lossy Si substrate. The figure also shows the series loss ($< 1dB$) introduced by the tank circuit, which could be compensated by tuning the external matching network.

There are a number of important factors to be considered while designing the tank circuit. The transmission loss of the low pass circuit must be as low as possible so that



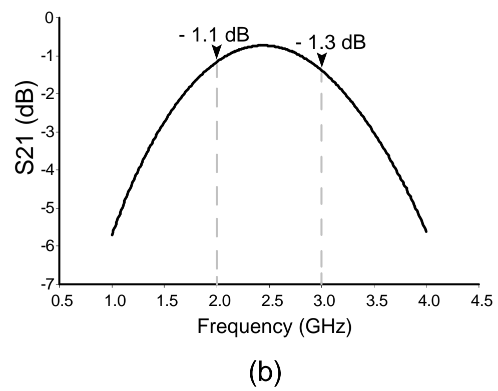


Figure 4.4: (a) Circuit used to simulate the loss in the tank circuit. (b) Simulated loss in the tank circuit over a frequency range of 1 - 4GHz.

the circuit does not significantly degrade the RF input/output signal levels. Inductors with a higher Q-factor will reduce the transmission loss. However, the Q-factor should also be low enough so as to provide sufficient bandwidth. In an ideal case ($Q = \infty$), the inductor shunts an ESD strike instantaneously thereby pulling the pad voltage to zero. The effect of finite Q causes some voltage overshoot. The parasitic resistance of the inductor represents the on-resistance of the protection circuit (inductor) during an ESD event. Hence this resistance must be minimized from an ESD standpoint.

4.3 Simulation Results

4.3.1 Small-signal simulation

Figure 4.5 shows the small-signal simulation results for the partially protected SiGe PA. All simulations were performed using Agilent Advanced Design System (ADS) version 2003C [69]. The S_{11} and S_{22} are < -20dB, indicating a well-matched input and output. The series loss added due to the LC tank was compensated for by slightly re-tuning the external input matching network. The Rollett Stability factor (commonly known as the *k-factor)* curve shows that the PA is unconditionally stable as k is always greater than unity. However, *k-factor* analysis is only valid for single-stage amplifiers where external matching is performed using passive circuits. The intermediate stages in a multistage PA are terminated using active networks and, hence, *k-factor* analysis is not an accurate measure of stability. However, considering the multistage PA as a single two port network and analyzing its overall *k-factor* provides a necessary but not a sufficient condition for stability. The μ_load (denoted as mu_load) and μ_source (denoted as mu_source) stability measurements denote the geometrically derived load and source stability factors, ie., the distances from the center of the Smith chart to the nearest unstable-input (μ_source) or output (μ_load) stability circle. According to [70], having $\mu_load > 1$ and $\mu_prime > 1$ are the two necessary and sufficient conditions for unconditional stability of a 2-port network. μ_load and μ_prime curves are >1 indicate that the nearest unstable input or output lies outside the Smith chart. Thus, the PA is unconditionally stable over a wide range of frequencies.

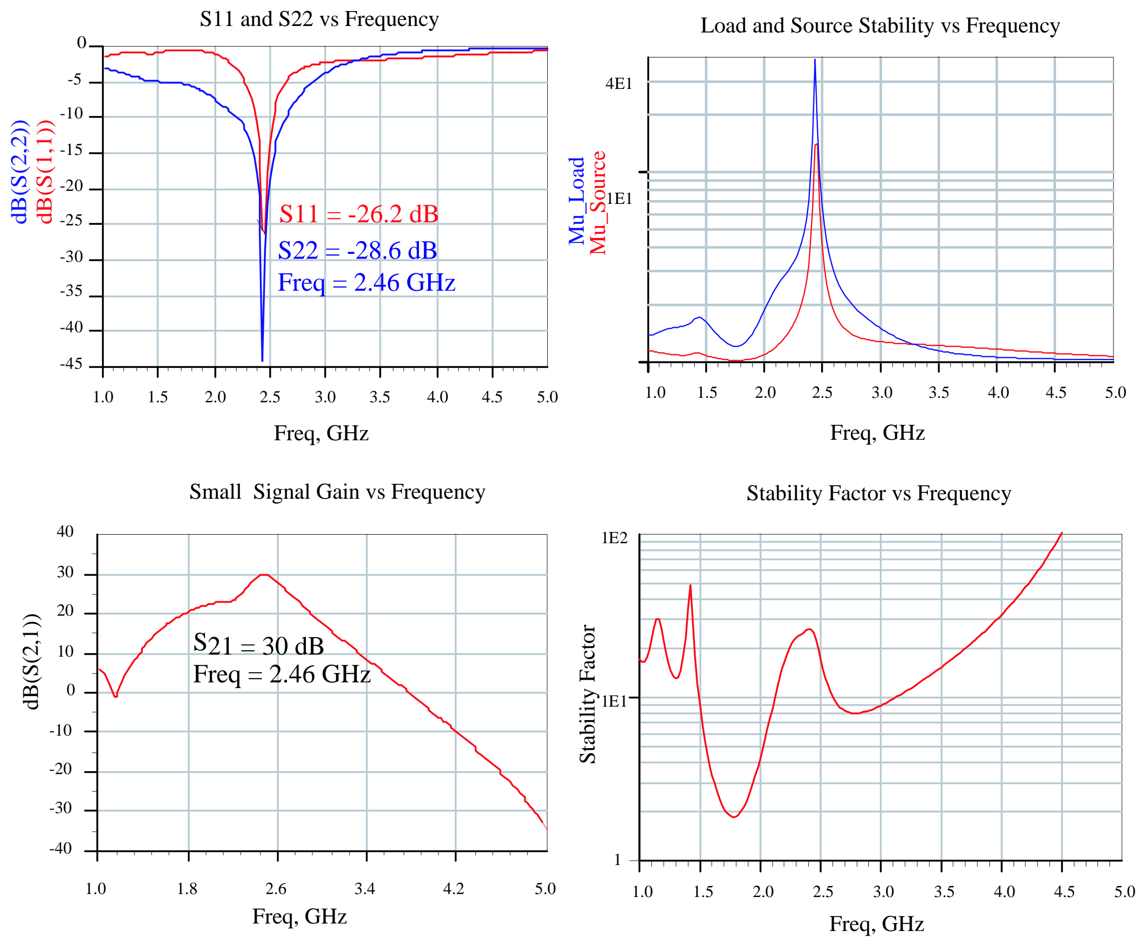


Figure 4.5: Small signal simulation results for the partially protected SiGe HBT PA.

4.3.2 Large-signal simulation

Large signal simulation results are shown in Figure 4.6. The optimum region of operation of the PA design is around -8 dBm input power. At this point, the gain is around 30dB. *1-dB Compression Point* (see Section 3.2.1) ($P_{1-dB,out}$ = 24 dBm) alone is not an accurate measure of linearity (refer Section 3.2.5 for further details), so *Error Vector Magnitude* simulations were performed to verify that the addition of ESD diodes did not excessively degrade the linearity of the PA. The PA's EVM was 5.3% at moderate output powers. The PA also has a Large-signal *Return loss* (20 dB) consistent with small-signal simulation results, which shows a conjugately matched input. The low PAE (13%) was a result of the backed off (by about 8dB) operation of the PA (refer to Section 3.2.5 on reasons for backed off operation).

4.4 Measured results

A photograph of the partially protected PA board is shown in Figure 4.7. The test setup used for performing small signal measurements is shown in Figure 4.8. Figure 4.9 shows the Small signal and Sweep power measurements made using an HP 8510C Network Analyzer. A 20dB attenuator was used to protect the network analyzer since the PA has a very high gain. An HP3631A DC power supply was used to provide the supply (V_{cc}) and control (V_{en}) voltages for the PA. An Agilent 34401A multimeter was used to measure the total current drawn by the PA. There was an error in the layout of a bias resistor in one of the stages which decreased the operating voltage of the main transistor. Because of this design error, the PA provided only about 15 dB small-signal gain at these operating voltages. The control voltage had to be increased to 4V to obtain a gain of 25 dB which was still lower than the specified gain. All of the measurements on the partially protected power amplifier were performed with a supply voltage of 3.3V and a control voltage of 4V. The small signal S_{11} and S_{22} results show that the input match is slightly shifted from the design operating frequency, which may also be due to the layout error.

The large-signal measurement test setup is shown in Figure 4.10. Isolator1, with a 50Ω termination, is used to protect the signal generator from any reflected power. The second circulator (Isolator2) is used to prevent reflected power from reaching the

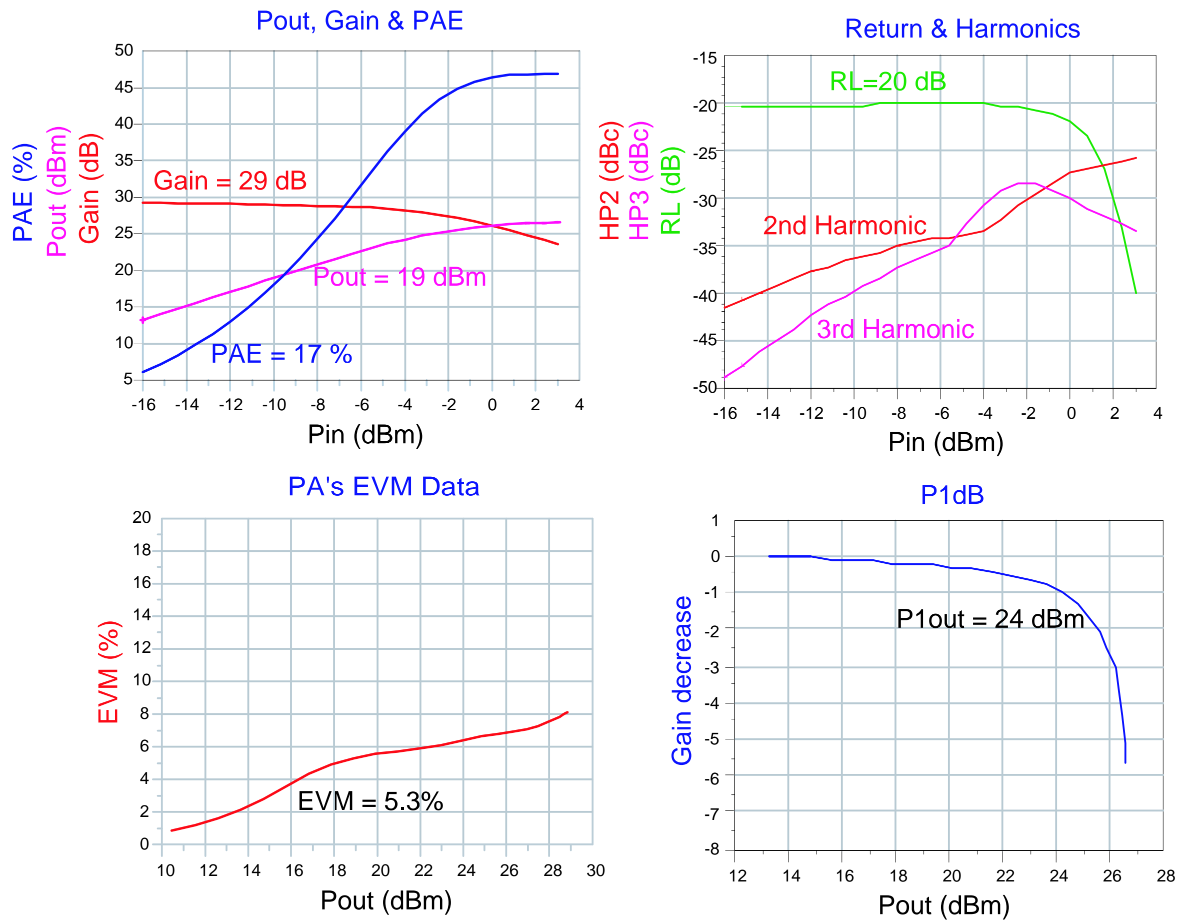


Figure 4.6: Large Signal Simulation results for the partially protected SiGe HBT PA. Values highlighted are for Pout=19dBm.

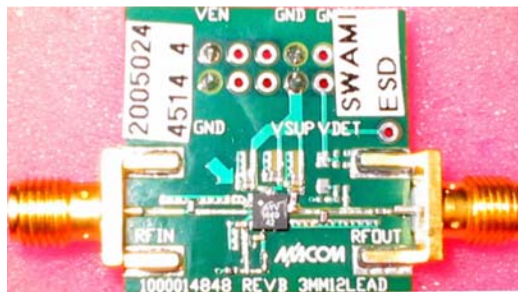


Figure 4.7: Partially protected SiGe HBT Power Amplifier board.

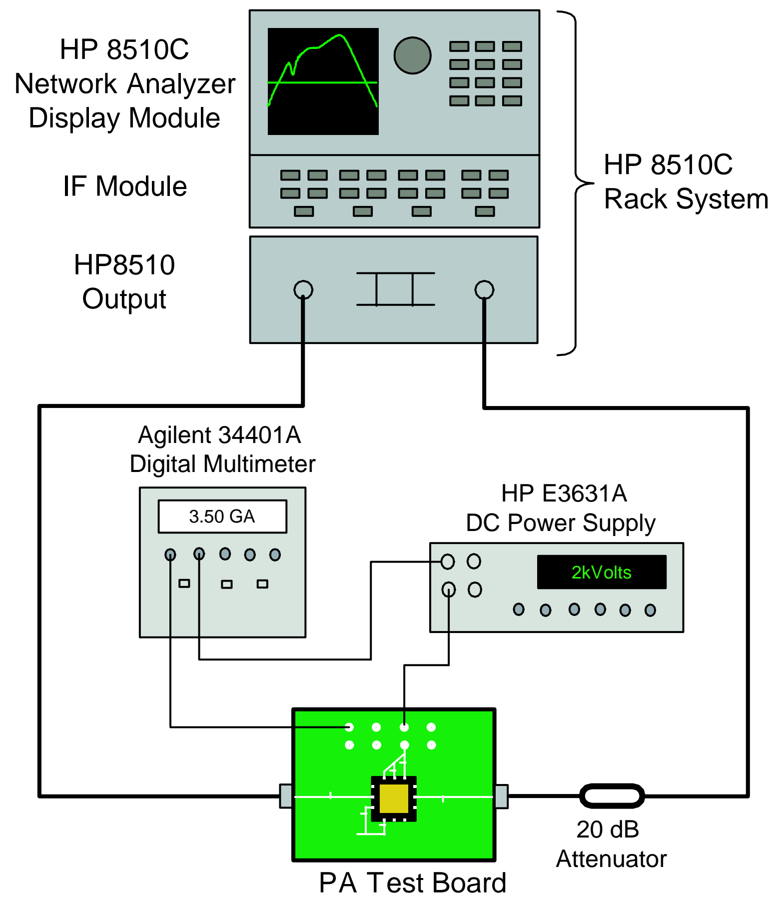


Figure 4.8: Experimental set-up for measuring small-signal S-parameters.

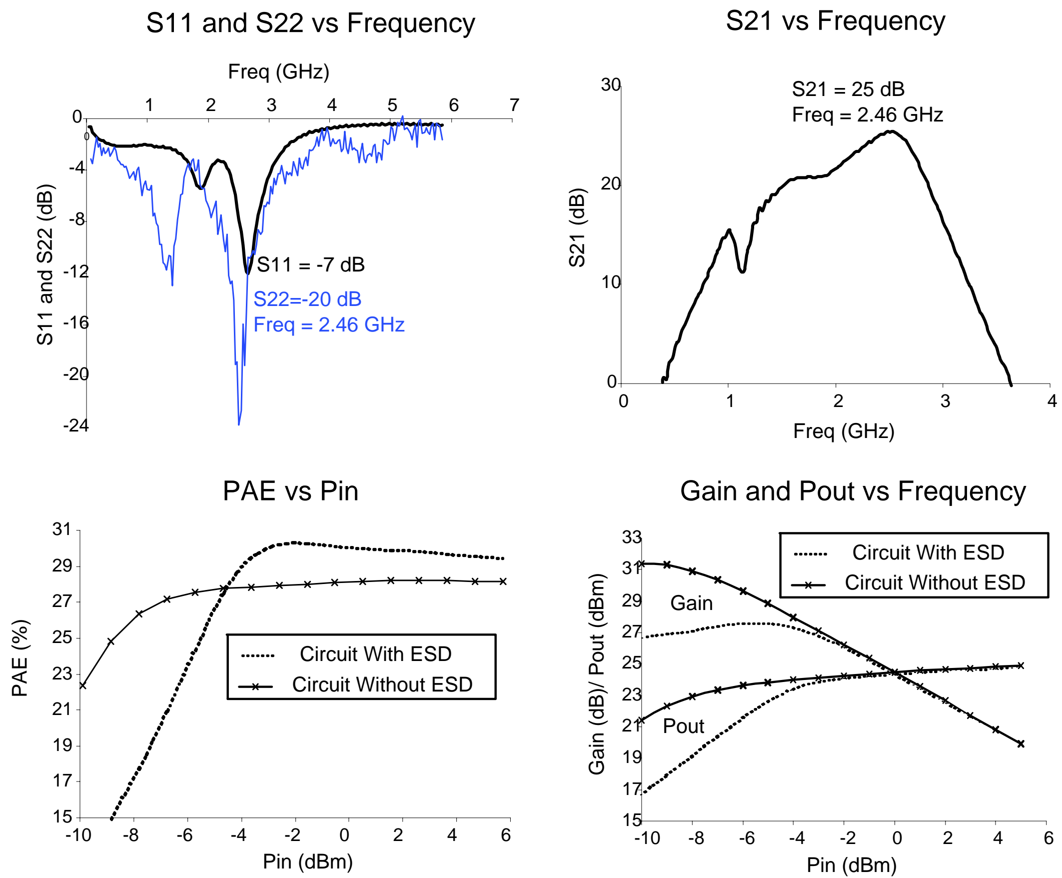


Figure 4.9: Small signal and sweep power measurements.

input power meter. A low pass filter is used at the output of the PA to filter out the harmonics generated. Gain and P_{out} analysis shows a clear 3 dB difference between the circuit with and without ESD protection circuit at the operating power levels which may be due to the design error.

4.4.1 ESD Compatibility

The circuit was tested for its ESD compatibility using a standard HBM and MM tests in accordance with MIL-STD-883F method 3015.7 specification [23] at M/A-COM, Lowell, MA. Appendix A describes the detailed testing procedure used for HBM ESD testing. ESD test was performed up to $\pm$1kV using a standard HBM ESD tester. A comprehensive RF performance test was performed before and after the ESD testing in order to estimate the $ESDV$ of the PA. Figure 4.11 shows that the measured RF output power (for a range of samples) remains virtually the same before and after a $\pm 1000V$ HBM test, indicating that the ESD strike was successfully averted from the core circuit by the LC tank present in the input and the diodes present in the control line.

The PA did not pass the 250V MM test and a study of the pin resistances indicate that the first stage blocking capacitor had failed due to the ESD strike. This indicates that either (or both) of the protection circuits (LC tank and/or Diode ring) did not provide a sufficient path to ground for the ESD strike. Recall that the protection circuits are connected to a common ESD_Gnd pad. As ESD strikes can occur between any two pin combination, for cases when the ESD_Gnd is left floating, the LC tank or/and the diode ring do not provide sufficient grounding for the ESD strike. Hence, for a 250V MM test, the pad voltage increased beyond the breakdown voltage of the first stage capacitor (approximately 30V).

In the fully protected version of the PA (to be discussed in Chapter 5), the ESD_GND was connected to *Paddle* ground. The *Paddle* provides a continuous path to ground for the ESD strike irrespective of whether the ESD_Gnd is properly grounded. This will be discussed further in the following chapter.

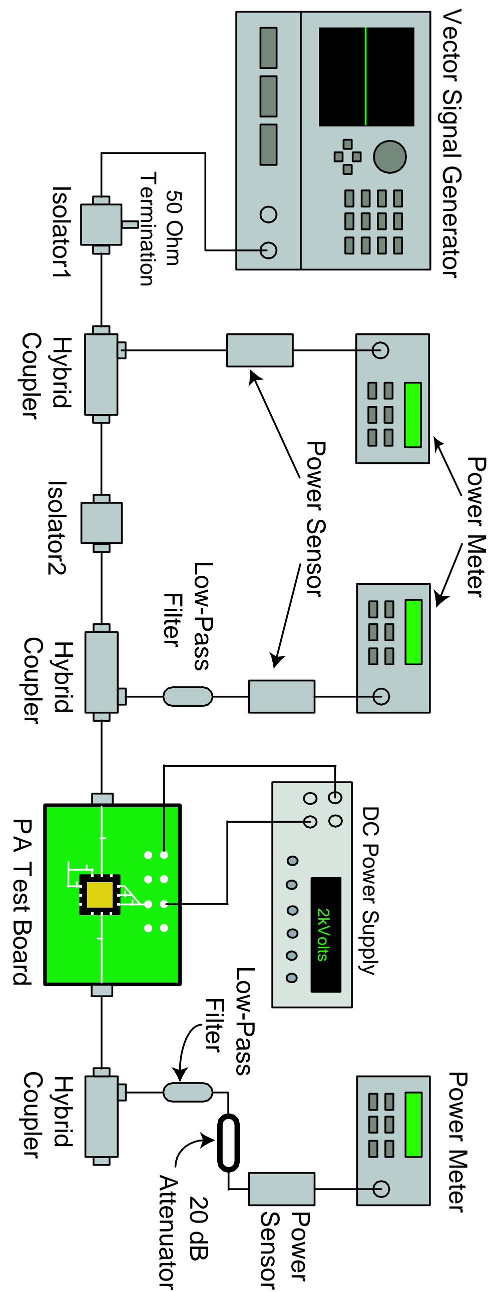


Figure 4.10: Experimental set-up for measuring large-signal performance.

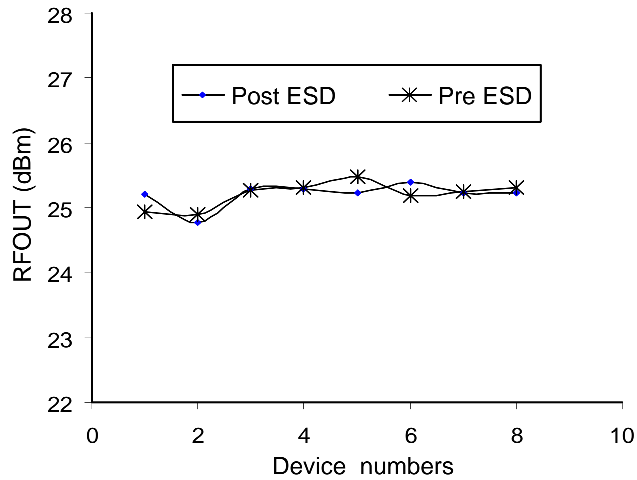


Figure 4.11: Measured RF performance pre/post ±1kV HBM test.

4.5 Summary

This chapter discussed the different ESD protection schemes that were used to protect the input and control lines of the prototype PA design. Large signal and small signal simulation results show that all the PA's RF specification were met. Measured results plotted in the end show that the circuit has an $ESDV$ of $\pm 1kV$ Human Body Model. The next chapter focuses on the design of a completely protected PA for Digitally Enhanced Cordless Technology (DECT) applications. The ESD protection schemes used for protecting the WLAN PA were extended in order to provide protection to RF_{out} and power supply lines. Simulations comparing the performance of the PA with and without ESD protection are presented.

Chapter 5

Fully Protected DECT PA

As discussed in the previous chapter, the incorporation of ESD protection structures into RFICs requires careful RF/ESD circuit co-design. By accurately accounting for the presence of the ESD protection structure, the designer can take advantage of the associated parasitic loading in the design of the circuit. In this chapter, some of the techniques used in the protection of the WLAN PA described in Chapter 4 have been extended to the design of a completely protected PA. The baseline amplifier design in this study originated from M/A-COM, Roanoke, VA. The design techniques involved in fully ESD protecting a SiGe PA designed for Digitally Enhanced Cordless Telephone (DECT) application are described in detail below. Small and large-signal performance simulations of the PA design with and without ESD protection are compared, and the effect of the different ESD protection schemes on the PA performance is discussed in detail.

5.1 Design Goals

5.1.1 DECT Specification

The Digitally Enhanced Cordless Telephone (formerly called Digital European Cordless Telephone), or DECT, standard employs 10 channels of 1.728 MHz each, along with time-division multiplexing (TDMA) of users (up to 12) within each channel in order to increase system capacity. Figure 5.1 shows the basic frequency allocation

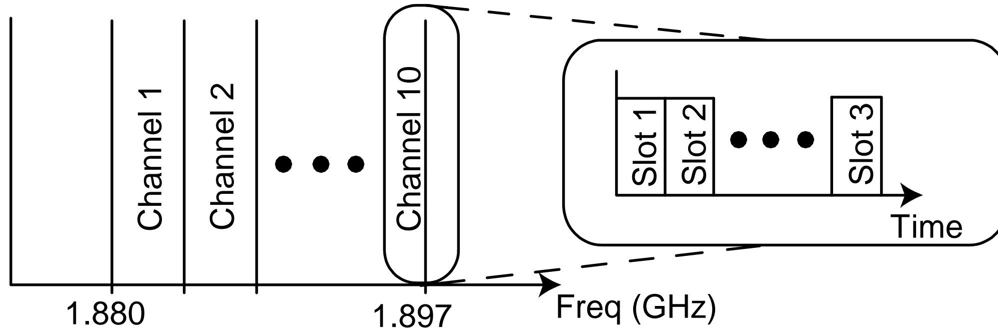


Figure 5.1: Basic Frequency allocation for DECT (after [58]).

for DECT. The key specifications for a DECT PA are the power output levels and time domain transmit masks. DECT uses Gaussian Frequency Shift Keying (GFSK) modulation scheme. Since power efficiency is also a key concern, the linearity requirements can be relaxed compared to WLAN standards. The output power levels vary from approximately ∼19 dBm (80 mW) to 24 dBm (250 mW) [71].

5.2 DECT Power Amplifier Design

The DECT PA features a high gain of 26dB for output power ranging from 24 dBm to 28 dBm and a good Power Added Efficiency (PAE) of about 43% at 1.8-2.0GHz. All three stages of the amplifier are biased Class AB (first stage is slightly more class A to obtain higher linearity) so as to increase the overall efficiency. The allowable supply voltage range varies from 1.6 to 4V; maximum current drawn is less than 400 mA with a standby leakage current of $3\mu A$. The PA chip is to be fabricated using a commercial $0.5\mu m$ SiGe-HBT process with high Q on-chip inductors. It is to be packaged in a 3mm Plastic Quad Flat Package (PQFP) 12 lead package. Table 5.1 shows the detailed design specifications of the PA. In this design, the RF Input (RF_{in}), RF Output (RF_{out}), Control lines (V_{en}), Supply lines (V_{cc1} and V_{cc2}) and the three stage grounds (Gnd_1,Gnd_2 and Gnd_3) require ESD protection.

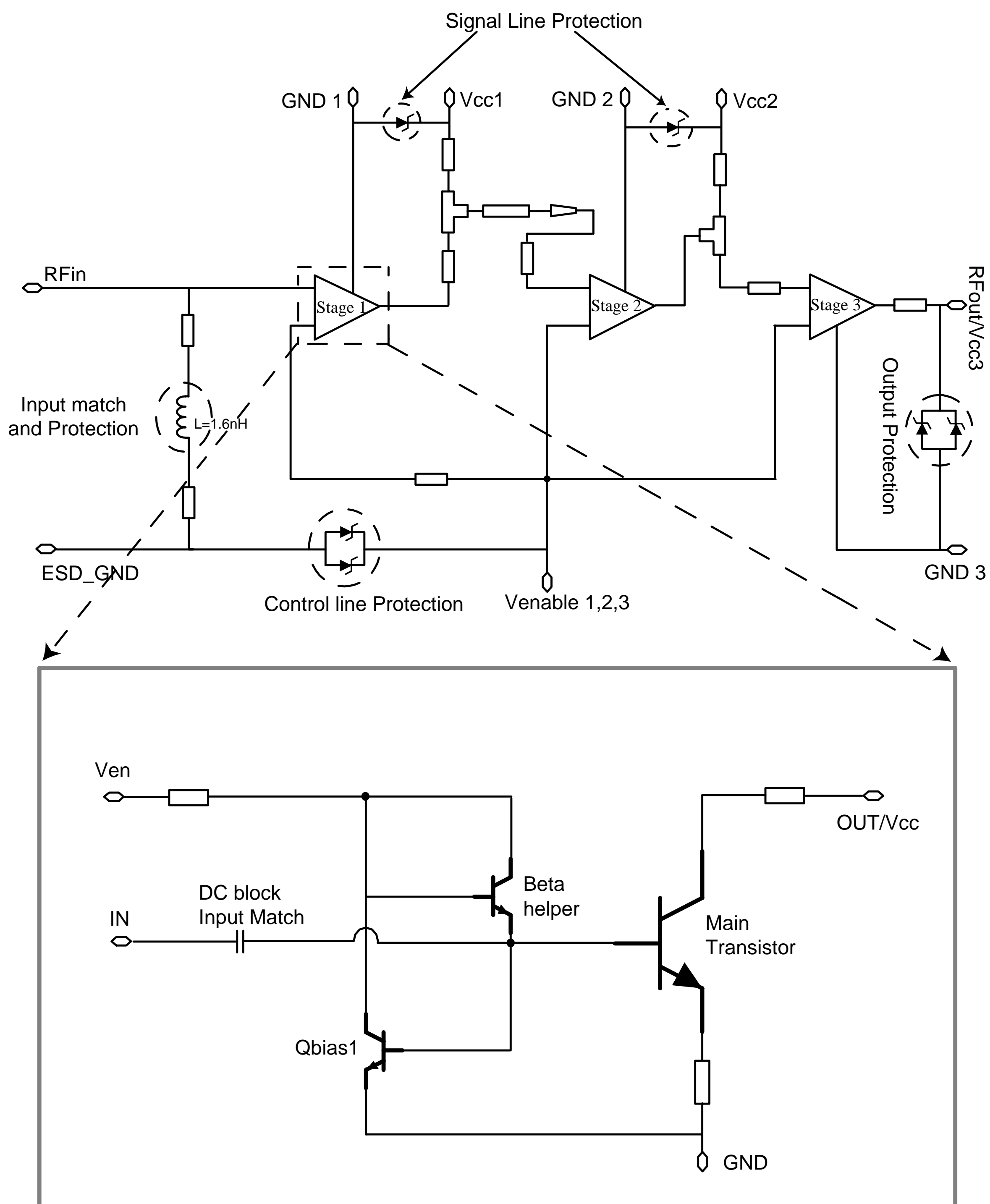


Figure 5.2: Completely protected DECT PA chip. The inset shows one of the PA stages. Microstrip transmission lines represent the parasitics of the laid out traces.

Table 5.1: DECT Power Amplifier Specification.

Parameter	**Specification**	**Units**
Frequency	$1.8 \sim 2.0$	GHz
Gain	27	dB
Output Power	$24 \sim 28$	dBm
Input Return Loss	15	dB
PAE	> 40	%
Bias Voltage	$1.6 \sim 3.0$	V
Current	< 400	mA
Off Current	3	μA
Isolation	< -40	dB
Harmonics		
$2f_o$	-35	dBc
$3f_o$	-40	dBc

5.3 Completely protected PA chip

Figure 5.2 shows the chip-level schematic of the completely protected DECT PA design. The interstage (Both Stage1-Stage2 and Stage2-Stage3) and output matching (not shown in figure) networks are realized off-chip for performance and cost savings. The input (RF_{in}), output (RF_{out}), control (V_{en}) and supply line (V_{cc1} and V_{cc2}) protection schemes are highlighted in the schematic. Parasitic effects of the interconnect traces were modeled using microstrip transmission lines in the same manner as described earlier for the partially protected PA. In order to prevent undesired coupling between the different stages, each stage has separate ground pins which are connected together on the package level to the *Paddle* ground. A separate ESD_GND pin was used to provide a common ground for the input and control signal protection circuits on the chip level so as to isolate the protection circuit from the main RF circuit. However, unlike the partially protected PA design in Chapter 4 (where the ESD_GND was connected to a separate pad on the package), all the ground pins (including ESD_GND) were connected at the package level to a common *Paddle* ground. The rationale for this will be discussed later in this chapter.

The inset in Figure 5.2 shows the schematic of the first stage of the PA including biasing schemes. The biasing is done using a simple current mirror with beta helper

circuit [72].

5.4 ESD Protection Schemes

The RF/ESD co-design is divided into two sections: (1) Control and supply lines; and (2) Input/Output protection. It should be noted that the completely protected PA design was expected to fit in the same die area as the partially protected version discussed in Chapter 4. Therefore, the *Zener diode* approach was used for protecting the control, supply lines and RF_{out} in order to minimize die area. The capacitances of the diode on the output lines were absorbed by the external output matching components. A slightly modified version of the L-C tank approach used in Section 4.2.4 was used to protect RF_{in}.

5.4.1 Control and Supply line protection

For this design, the *Zener diode* approach was utilized for protecting the control and the bias lines. This approach uses just one reverse biased Zener diode (as opposed to a string of diodes used in Section 4.2.3) as shown in Figure 5.3(a) between the voltage line and ground. This approach utilizes both forward and reverse bias characteristics of the diode, unlike the diode string approach, which utilizes only the forward characteristics of the diodes. Available Zener diodes were used because of their lower reverse breakdown voltages. These diodes are slightly bigger (50x30μm^2) as compared to the CB diodes available in the design kit and hence have a larger capacitance (2.112pF). It is interesting to note that this approach is more immune to stronger negative HBM pulses. For a positive ESD strike the diode breaks down at about 7V, providing a slight overshoot for a very short period of time (few ns). For a negative strike, the Zener turns on at its forward V_{on} providing a much lower voltage overshoot. To make the device indifferent to the positive and negative ESD strikes, one can either design Zener diodes with comparatively lower breakdown voltages (which is typically not an option for IC designers with a given process) or use the diode string approach. However, the single Zener approach is more area efficient as compared to the diode string approach, especially given that there is more than one control line to protect in this design. Two diodes were used in parallel to protect the control pins ($V_{en1,2,3}$) (See

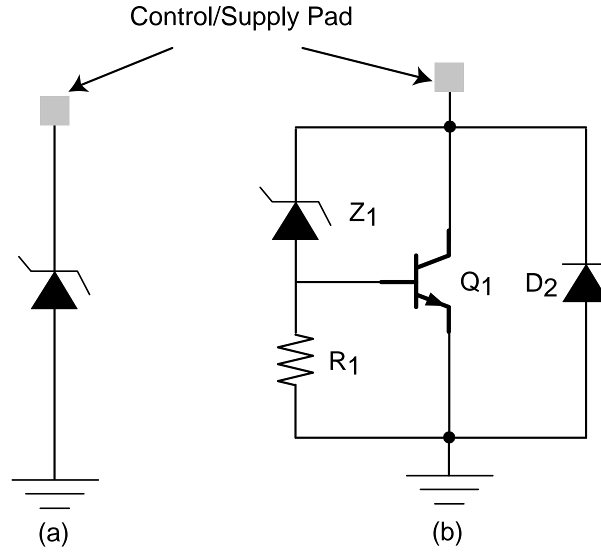


Figure 5.3: (a) Zener approach. (b) Zener based clamp.

Figure 5.2). Even though this increases the total capacitance on the pin, this reduces the effective voltage overshoot during an ESD event since the dynamic resistance of the diodes is reduced.

An alternate approach considered was the Zener based clamp shown in Figure 5.3(b) [73] which could be used to provide protection to a higher voltage level. Here, the Zener Z_1 is broken down during an ESD event and current flows through the resistor R_1 to ground. For severe ESD strikes, dissipating all the energy through the Zener is not practical. A vertical NPN transistor such as Q_1 shown in the figure is preferred. The resistor R_1 is used to bias the base-emitter junction of the vertical NPN transistor (Q_1), which then takes the majority of the ESD energy away from the Zener and provides the main discharge path. The size of Q_1 totally depends on the amount of ESD protection level desired. For the case where the control/supply pad is negative with respect to the pad, the diode D_2 provides the main conducting path. A CB junction based diode is preferred for D_2 as compared to a Zener because of the smaller size and reduced parasitic capacitance. This approach increases the effective area of the protection structure and hence the parasitic capacitance also increases. Due to area constraints, this approach was not used for protecting the control and supply lines of the SiGe HBT DECT PA design.

5.4.2 Input/Output protection

The L-C tank approach discussed in Section 4.2.4 was modified to provide input matching. In this case, a shunt-L series-C network was used to provide input matching thereby eliminating the need for external matching networks. However, this approach was not extended to protect the RF_{out} port. RF_{out} and V_{cc3} share the same set of pins which would then need to be split apart in order to use the L-C tank or shunt L-series C approach. This would also introduce more loss in the RF output path. Further, an on-chip RF choke and a shunt inductor were needed for output matching which increases the effective area of the overall PA.

An alternative approach that was investigated to protect RF_{out} was the use of an on-chip RF-choke to provide a shunt path for the ESD strike to V_{cc3} from where the protection circuit for supply pin would take over and suppress the ESD strike. However, the size of the required inductor was excessively large for on-chip implementation, since it was operating as the RF choke. Also, the output blocking capacitor would have to be implemented off-chip (or separate protection will have to be provided for the output blocking capacitor) as it would be directly in the path of an ESD strike on the output pin, if it were implemented on-chip. Also, the size of the 3rd stage transistor was very large and hence provided a comparatively lower resistive path for the ESD strike as compared to the large choke with increased parasitics (as a result of lower Q). Thus, a considerably large amount of the ESD current preferred to sink through the 3rd stage transistor as opposed to choosing the choke to V_{cc3}.

The Zener clamp based approach discussed in the previous section is also not particularly effective in protecting output as RF_{out} and V_{cc3} shared the same pin. The transistor Q_1 [see Figure 5.3 (b)] which is connected directly to the RF_{out} must be quite small in order to reduce the leakage, whereas it needs to be large enough to provide a direct path for ESD. Hence the Zener clamp approach was not used to protect the output. The protection of the RF output circuitry was realized using a simple shunt protective Zener diode (two parallel diodes were used in order to reduce the dynamic resistance), and the capacitance of the loading diodes was is incorporated into the output match design.

5.5 Simulation Results

5.5.1 Small-signal simulation

Figure 5.4 shows a comparison of the small-signal simulations of the PA without protection circuitry and those of the completely protected PA. As mentioned in Section 4.3.1, ADS version 2003C was used to perform all simulations. The S_{11} and S_{22} curves show that the RF input remained well matched ($S_{11} \sim$ -13dB) and there is a slight improvement in the small signal gain ($S_{21} \sim$ 30dB) despite a degradation in output matching ($S_{22} \sim$-7dB). The stability simulations were performed considering the three stage PA as a single two port network. The stability factor is always greater than unity which indicates that the PA is unconditionally stable over frequency ranges between 0-6 GHz. The increase in the μ_source and μ_load stability factor values indicate that there may be additional isolation provided by the zener diodes between the supply lines of each stages

5.5.2 Large-signal simulation

Figure 5.5 shows a comparison of the large-signal simulations of the protected and unprotected versions of the DECT PA design. Recall, the output protection circuit has two parallel Zener diodes in order to reduce the voltage overshoot during an ESD event. Because of this, there exists excess leakage in the last stage, and hence the total current consumed by the protected PA is slightly more than that of the unprotected version. Even though there is a slight increase in the total current consumption, there is little degradation in the PAE of the PA. The optimum operating point of the PA is around -2 dBm (input power), where the gain is around 28 dB. The protected PA appears to have better second and third harmonic levels than the original unprotected version. The better harmonic performance may be due to the additional harmonic trapping provided by the capacitance of the Zener diodes present between the supply lines of each of the stages, but this needs to be verified experimentally

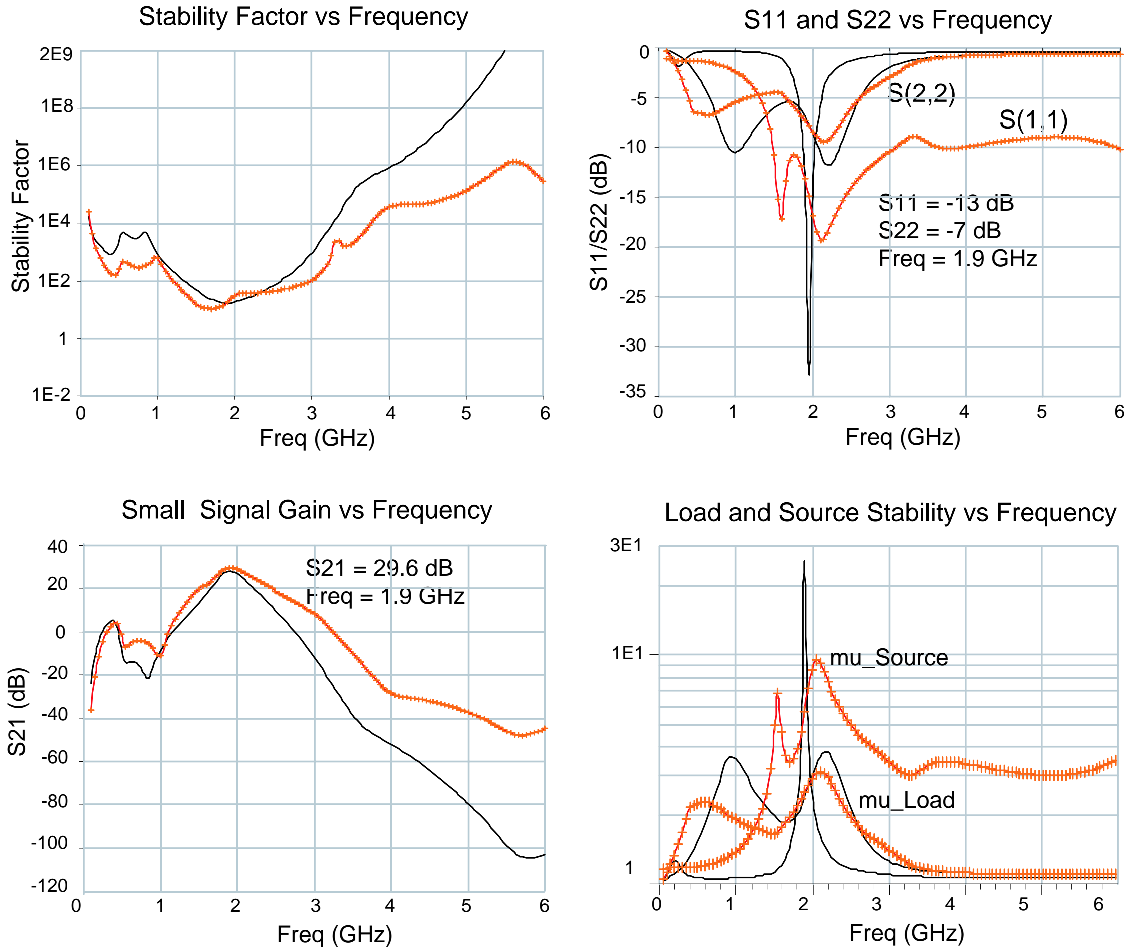


Figure 5.4: Small Signal Simulation comparison between PA without ESD protection (solid lines) and completely protected PA (lines with X's). The S-parameter data listed in the figures is for the Fully-protected PA.

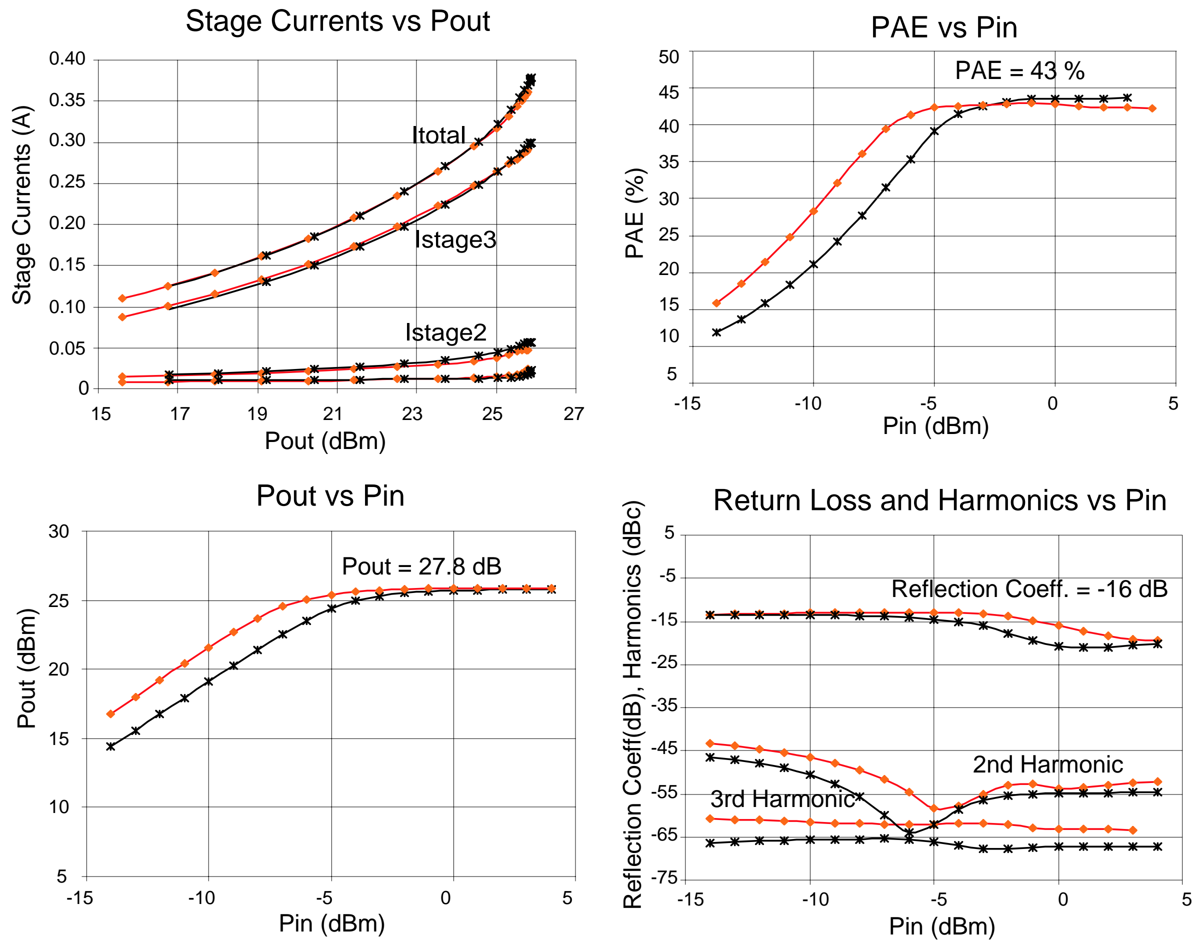


Figure 5.5: Large-signal Simulation comparison between PA without ESD protection (solid lines) and completely protected PA (lines with diamonds). The parameters highlighted are for the protected PA at a Pin = 0 dBm.

5.5.3 ESD Transient event simulation

Figure 5.6 shows the transient simulation response of the completely protected SiGe PA for standard HBM and MM ESD pulses. The circuit's response to +1.5kV, –4kV HBM and 350V MM pulses (with respect to the package PADDLE) are shown in Figure 5.6. For a positive HBM ESD strike on V_{cc} pin, the voltage rises to a maximum of 12V for a few nanoseconds and settles to a low value within 20μs. For a similar ESD strike on V_{en} and RF_{in} pins, the protection structures limit the voltage overshoot to a lower value. The final settling voltages in the cases of strikes on the V_{en}, V_{cc} and RF_{out} pins are around 7V, which is the reverse breakdown voltage of the Zener. As mentioned earlier in Section 5.4.1, the simulations show that the protection structure provides better protection for negative ESD strikes as compared to positive strikes. Even for a –4kV HBM strike, the voltage overshoot is limited to a lower value for strikes on 'RF_{out}', 'V_{en}' and 'V_{cc}'. It is interesting to note is that the L-C tank circuit, which provided the least voltage overshoot for a positive HBM strike, seems to provide the maximum voltage overshoot in case of a negative HBM strike. This is due to the fact that for a positive strike on the RF_{in} pin, the ESD pulse has two paths to ground – either a very high impedance path looking into the blocking capacitor of the first stage, or a much lower resistive path through the inductor. The ESD current prefers the least resistive path (through the inductor) thereby reducing the voltage overshoot to a very low value. During a negative strike, the pulse looks at two comparable resistances; one looking up into the emitter of the first stage transistor and the other that of the inductor. Hence the current tends to divide among the two path causing a higher voltage overshoot. However, the surge on RF_{in} lasts only for a very short period of time. In case of the MM strike, the voltage rises to much higher values as compared to HBM. The surge due to strikes on V_{en} and RF_{out} are similar. This is due to the fact that similar Zener diodes are used to protect both the V_{en} and RF_{out} and hence, the dynamic impedance looks similar thereby making the voltage overshoot comparable.

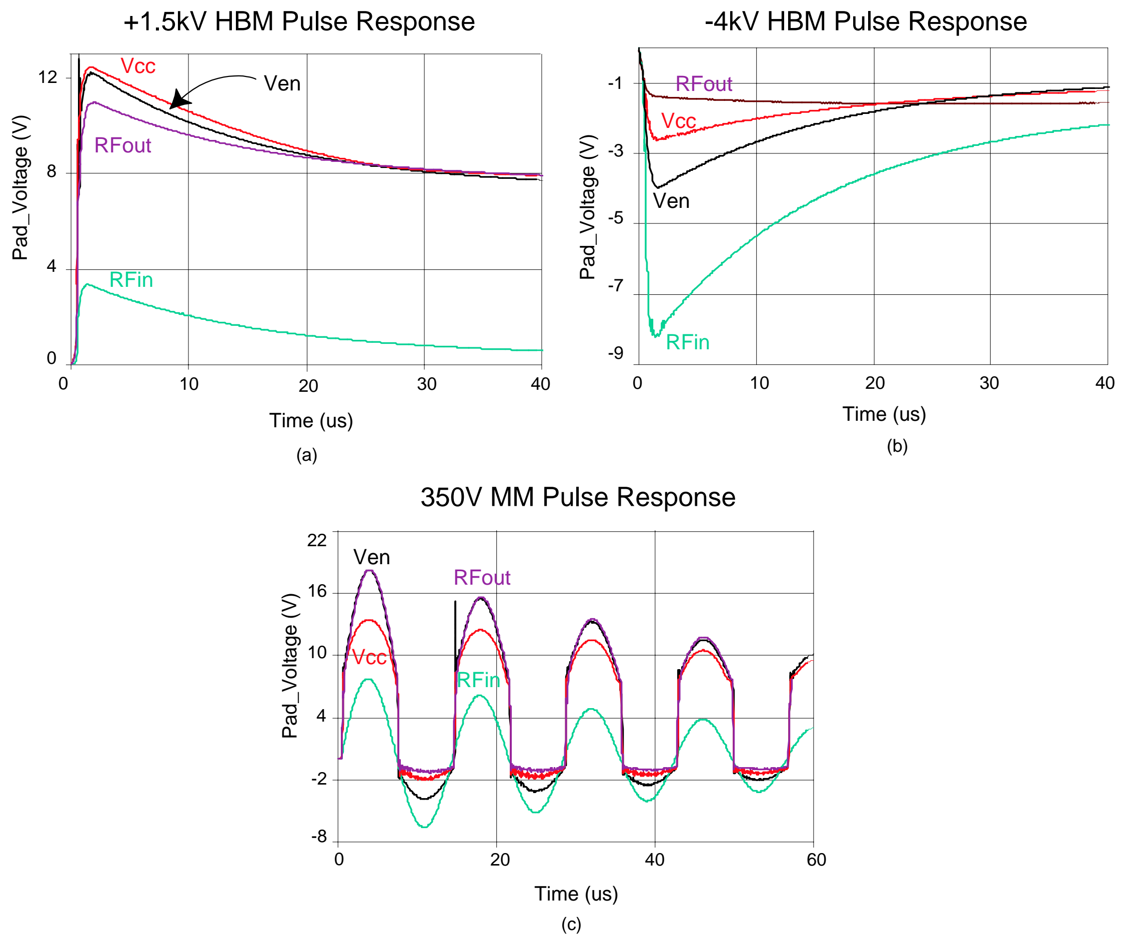


Figure 5.6: Pad Voltages during (a) +1.5kV HBM Pulse, (b) -4kV HBM Pulse, and (c) 350V MM Pulse with respect to Paddle ground.

5.6 Summary

This chapter has discussed in detail the design of the completely ESD protected DECT PA. A Zener diode approach was used (as opposed to the diode ring approach used in the WLAN PA design in Chapter 4) for protecting the control and supply lines in order to maintain a small die area. An on-chip input matching network was incorporated using a shunt-inductor, which also provided ESD protection to RF input. A Zener diode was used to protect the RF output/V_{cc3} line. Comparisons of large-signal, small-signal simulations for the protected and the unprotected versions of the PA show that the performance of the PA is virtually unaffected by the incorporation of the protection circuits. Transient response to HBM and MM pulses show that the PA can withstand HBM pulses of -4 kV to +1.5 kV and MM pulses of up to 350V. The design is being laid out for fabrication in a commercially available SiGe HBT Power technology in the near future.

Chapter 6

Conclusion and Future work

The continuous scaling down of semiconductor device dimensions in the IC industry guarantees that the importance of ESD protection will continue to grow. Methods to protect sub-micron devices must be considered along with other manufacturing issues because a product with high susceptibility to ESD-induced damage will not be widely accepted. RFICs in mobile applications are exposed to a variety of ESD events and hence demand increased ESD robustness. As a result, dedicated on-chip protection circuits are being designed to protect standalone sub-circuits such as RF Power Amplifiers. These sub-circuits are more prone to ESD events as they are generally packaged in separate modules as opposed to being integrated into large SOCs with overall I/O and power supply. The objective of this thesis was to develop robust, integrated ESD protection circuitry for low cost, high performance RF power amplifiers. This chapter summarizes the significant findings of this work and suggests future research directions.

6.1 Conclusion

A simple but effective protection-circuit design methodology was outlined for protecting the RF input and control pins of a SiGe HBT Wireless LAN Power Amplifier. The *L-C tank* approach was used to protect the input while a standard *diode ring* approach was used for protecting the control lines. These protection techniques were extended with little modification to protect a three-stage power amplifier designed

for Digitally Enhanced Cordless telephone application. The *diode ring* approach was replaced by an area efficient Zener diode approach for control supply lines and the On-chip shunt L-series C input matching network was used to provide protection to the input pin of the PA. Both the PA's were designed in a commercial 0.5 μm SiGe-HBT process. The WLAN PA was fabricated and packaged in a lead free 3mm Fine Pitch Quad Flat Package (FQFP-N) 12 Lead package. Standard HBM ESD test measurements on the WLAN PA show that the protection circuits are capable of protecting the PA from -1kV to +1kV HBM pulses. The simulated DECT PA demonstrates that excellent performance can still be achieved while at the same time provide +1.5kV to -4kV HBM ESD protection. The design is being laid out for fabrication in the near future.

6.2 Future work

As mentioned above, the fully protected DECT PA design is being laid out for fabrication in a commercially available SiGe HBT Power technology. The most immediate and important future work is the packaging and testing of the fully-protected PA for its ESD robustness as well as RF performance. When the circuit is available for testing, the test setups shown in Figures 4.8 and 4.10 can be used to measure the RF performance. An ESD test plan as described in Appendix A should be devised for performing the HBM and MM pulse tests.

Although this work represents progress on specific ESD protection schemes for RF Power Amplifiers such as L-C tank approach and Zener approach, the ESD testing schemes used (HBM and MM) are relatively old and have many limitations. This work focused on the HBM and MM standards as they are the only schemes which are currently accepted in the industry. However, a newer characterization method known as Transmission line Pulsing (TLP) is currently becoming popular as it overcomes some of the limitations of HBM and MM. Another interesting protection technique which can be considered for future broadband ESD protection scheme is the T-coil approach, which will be discussed later in this section.

6.2.1 Transmission Line Pulsing Model

There are many limitations to using the traditional models discussed in Chapter 2 to characterize ESD protection performance. The double exponential (refer to equations 2.1 and 2.4) and oscillating pulses of the standard ESD testers make it extremely difficult to determine the exact working of the device during an ESD event [40]. If the current is varying over the pulse duration, so will the voltage. This makes accurate current and voltage acquisition very complicated during HBM and MM events. Thus the traditional HBM and MM tests are used to characterize the device with a *ESDV* and a simple "pass or fail" response.

A relatively new testing method known as the transmission line pulsing (TLP) uses a different approach to characterize ESD. TLP captures the transient I-V curve of a stressed device by sampling each current level so briefly that actual damage is not caused to the device. TLP uses a very short pulse measurement system which is useful to provide to both electrical operating analysis and electrical damage signature (*EDS*). Since TLP uses a flat top pulse, both the current through the device and the voltage across the DUT can be accurately measured to provide Current-Voltage (I-V) characteristics. Moreover, TLP also allows leakage measurements to be performed after each pulse as compared to HBM or MM tests where the DC leakage of the DUT can be measured only at the beginning and the end of the stress. These leakage measurements help in determining the pulse current capability of each individual protection structure. The I-V and the leakage data on a device are defined together as the Electrical Damage Signature (*EDS)* [74]. The *EDS* not only allows determination of the overall robustness of a protection circuit but also helps in locating the weakest point [pin(s)] of the circuit as TLP allows leakage and I-V measurements to be performed after zapping each pin.

Two types of TLP testers (Constant Current TLP Tester and Constant Impedance TLP tester) are currently in use. Figure 6.1 shows the circuit schematic of a constant current TLP tester. As the name suggests, this method provides a constant current to the DUT for the duration of the pulse. In this method [75] [76], a 50 Ω coaxial cable is first charged up to a voltage corresponding to the current desired in the line. The low inductance discharge relay is then closed generating a square voltage pulse, which travels down through a 50 Ω coaxial line to the DUT. One end is terminated

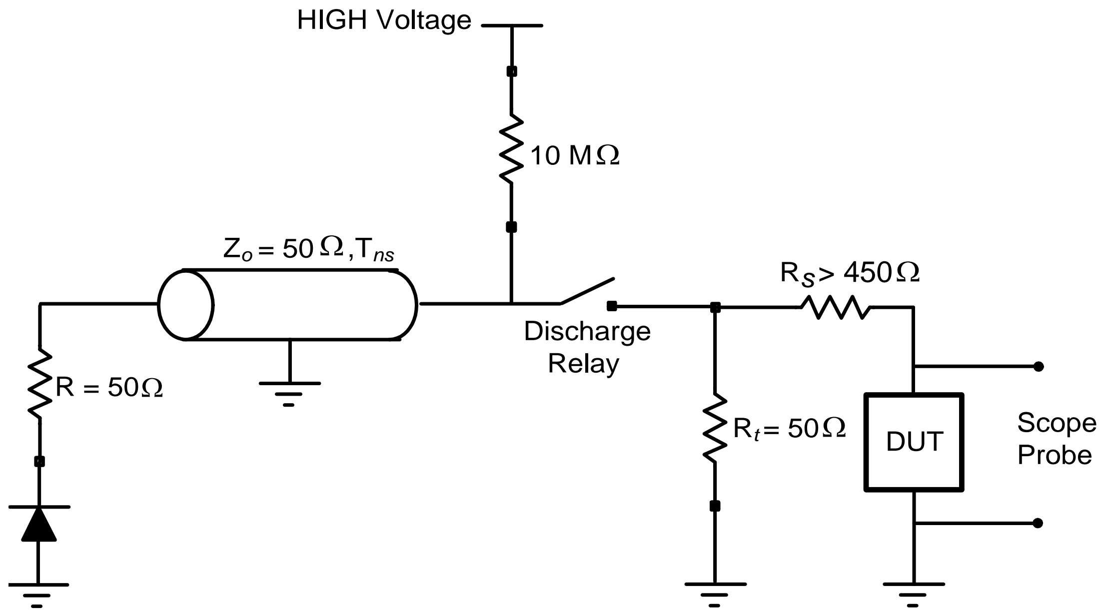


Figure 6.1: Constant Current TLP Tester Schematic (after [31]).

with a diode-resistor arrangement to absorb any reflected energy that would be applied to the DUT otherwise. During conduction, the DUT will have a relatively low resistance value. For optimum termination in order to minimize pulse distortion due to reflections and for applying a constant current to the DUT, R_s needs to be $\geq$ 500 Ω [77]. The terminating resistor (R_t) is chosen appropriately so that the parallel combination of R_s and R_t is 50 Ω. Amplitude, duration and rise time are the three important aspects of the TLP waveform (Figure 6.2) to reproduce the damage seen by a HBM ESD event.

In practice, generating a clean TLP waveform is very difficult due to the parasitic elements in the measurement and test setup. The parasitics generate considerable distortion and oscillation which must be reduced or eliminated. In a realistic TLP pulse, the oscillating voltage waveform complicates the measurement. This potentially leads to a false estimation of $ESDV$ for the device.

The correlation between TLP-generated failures and classical ESD model-generated failures [79] [80] shows that HBM pulses with an exponential decay time of 150 nsec should theoretically require a rectangular pulse of 75nsec to provide equivalent energy at the same peak currents. ESD designers have been currently using TLP systems

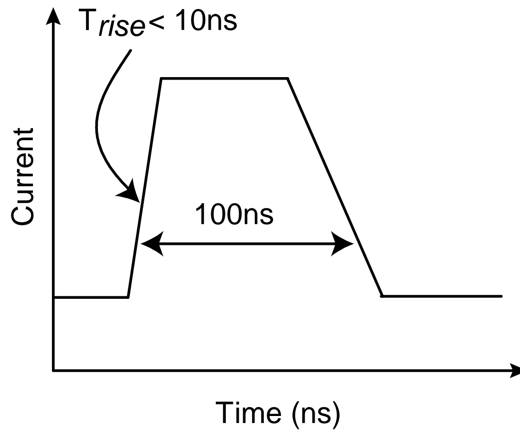


Figure 6.2: Constant Current TLP Tester Waveform (after [78]).

with rectangular pulse widths of 75-200 nsec with rise times ranging from 1-40nsec. According to [81], correlation between TLP pulse and HBM test pulse can be remarkably close if their rise times are comparable. This leads to the possibility that TLP will be used as a industry accepted test method sometime in the near future.

With regards to the fully protected RF PA, the TLP system could be useful in locating the weakest pin(s). Even though information about the breakdown voltage of each components supported by the design kit is provided by the vendors, those breakdown voltages are not completely reliable in case of a transient ESD event which lasts for a very short period of time. By conducting TLP tests with a rectangular pulse of 75nsec (in order to correlate with HBM) on the PA, the *EDS* data obtained can be used to determine the performance of the transistors and capacitors during an ESD event and accurately determine the corresponding HBM *ESDV* of failure for each component. Also, the leakage measurements performed after each pulse can help in determining any latent defects in the PA.

6.2.2 T-Coil ESD Protection Networks

The LC tank approach and the Zener diode approach used to protect the input and the output of the fully protected RF PA respectively cannot be used to provide broadband ESD protection. The LC tank protection circuit used at the RF input of the PA will not be effective for high frequency ESD events such as CDM, field-induced model or

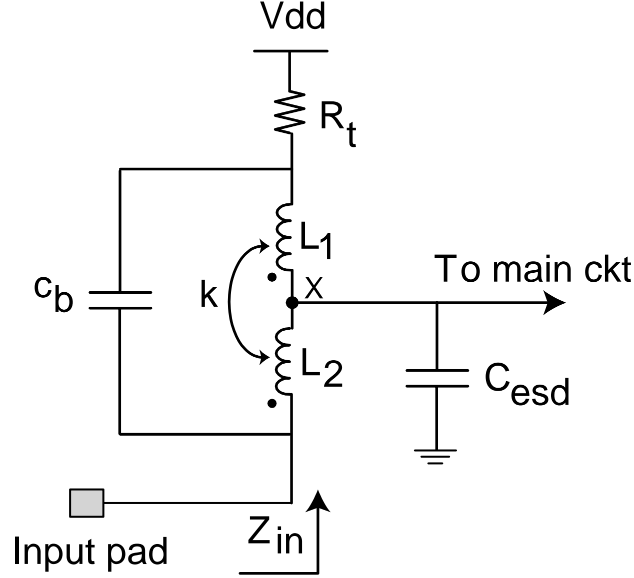


Figure 6.3: T-Coil network (after [17]).

capacitively-coupled model. In order to provide effective protection for those ESD events and also provide broadband ESD protection, a new protection structure known as T-coil approach [17] [18] can be used.

T-Coil ESD protection networks provide a 70% increase in RF bandwidth over the L-C tank approach. T-coils also display a purely resistive input impedance that is independent of the frequency (Z_{in}=R_t). As shown in Figure 6.3, the network consists of two coupled inductors L_1 and L_2 with a coupling coefficient of k and a bridge capacitance C_b. R_t denotes the on-chip terminating load resistor. At low frequencies, L_1 and L_2 shunt the input to R_t, while at higher frequencies C_b shunts the input to R_t. It can be shown that for Z_{in} to remain purely resistive, the following condition will have to be satisfied:

$$L_1 = L_2 = \frac{C_{esd}R_t^2}{4}\left(1 + \frac{1}{4\varsigma^2}\right) \ , \tag{6.1}$$

where ς is the damping factor of the network.

The T-coil network can also be used at the output. When an addition resistor was added in series with L_1 and L_2, to account for the effect of output impedance, the voltage at node X remains unchanged as long as the input is driven by a source

impedance equal to R_t. Therefore the series resistance of the T-coil does not translate to signal loss. T-Coil structures offer a promising, broadband input and output ESD protection structure design suited for broadband RF amplifiers. T-coils provide broad bandwidth, good impedance matching and low midband loss.

The *ESDV* of the PA can also be increased by using large sized ESD protection structures. These protection structures can effectively replace the capacitance C_b. T-Coil network provides the required RF bandwidth and negligible loss irrespective of the size (parasitic capacitance) of the protection structures. However, the structure is potentially large and could be used only at the RF input/outputs.

Appendix A

ESD testing

The partially protected prototype PA was ESD tested with standard HBM pulses in accordance with MIL-STD-883F method 3015.7 specification [23] at M/A-COM, Lowell, MA. As shown in Figure A.1, comprehensive functionality test was performed before and after the ESD testing in order to ascertain whether the device has successfully passed the ESD zap. Table A.1 shows the device pin specification and their functionality. As only the RF input and control lines were protected in the prototype PA, only pins 0 to 4 were ESD zapped. Even though MIL standard provided the flexibility of grouping similar supply pins together (reduces the number of tests required) for ESD testing, the control pins (pin 3 and 4) were left separate for better ESD analysis purposes in case of a failure.

Table A.2 shows the ESD test plan. Only one pin was zapped (and one pin grounded) at any instant during the ESD test. Remaining pins were left floating. 24 samples were ESD tested for HBM pulses at ±300V, ±600V and ±1kV. Table A.3 shows the device serialization for the each test. Each test was performed on two different samples at different HBM voltages. Even though samples which passed a lower voltage stress level are permitted to be used for testing at a higher ESD stress voltage, new sample

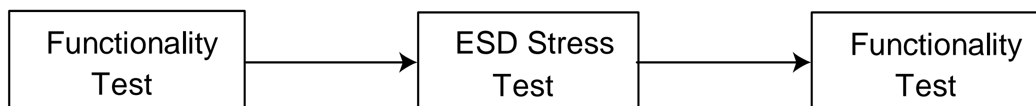


Figure A.1: Block diagram of the ESD test method.

Table A.1: Pin Specification for the prototype PA.

Device Pin	**Pin Name**
0	Paddle
1	ESD_GND
2	RFin
3	$V_{en1,2}$
4	V_{en3}
5	N/C
6	N/C
7	RFout/V_{cc3}
8	RFout/V_{cc3}
9	RFout/V_{cc3}
10	V_{cc2}
11	N/C
12	V_{cc1}

Table A.2: ESD test plan.

Test Number	**Grounded Pin**	**Zapped Pin (One at a time)**
1	1	0, 2, 3, 4
2	2	0, 1, 3, 4
3	3	0, 1, 2, 4
4	4	0, 1, 2, 3

of devices were used to avoid cumulative damage effects. All 24 samples passed ESD testing. Measured RF performance of 8 samples tested at HBM stress level of ±1kV shown in Chapter 4, Figure 4.11 indicate that the PA can withstand upto ±1kV HBM stress.

Table A.3: Deviice Serialization for ESD testing.

Test Number	**± 300V HBM**	**± 600V HBM**	**±1kV HBM**
1	1,2	3,4	5,6
2	7,8	9,10	11,12
3	13,14	15,16	17,18
4	19,20	21,22	23,24

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