Heteroepitaxial Germanium-*on*-Silicon Thin-Films for Electronic and Photovoltaic Applications

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ABSTRACT

Developing high efficiency solar cells for lower manufacturing costs has been a key objective for photovoltaic researchers to drive down the levelized cost of energy for solar power. In this pursuit, III-V compound semiconductor based solar cells have steadily shown performance improvement at approximately 1% (absolute) increase per year, with a recent record efficiency of 46% under concentrator and 32% under AM0. However, the expensive cost has made it challenging for III-V solar cells to compete with the mainstream Silicon (Si) technology. Novel approaches to lower down the cost per watt for III-V solar cells will position them to be among the key contenders in the renewable energy sector. Integration of such high-efficiency III-V multijunction solar cells on significantly cheaper and large area Si substrate has the potential to address the future LCOE roadmaps by unifying the high-efficiency merits of III-V materials with low-cost and abundance of Si. However, the 4% lattice mismatch, thermal mismatch, polar on non-polar epitaxy makes the direct growth of GaAs on Si challenging, rendering the metamorphic cell sensitive to dislocations.

The focus of this dissertation is to investigate heterogeneously integrated 1J GaAs solar cells on Si substrate using germanium (Ge) as an intermediate buffer layer that will address mitigation of defects and dislocations between GaAs active cell structure and Ge "virtual" substrate on Si. The all-epitaxial molecular beam epitaxy (MBE)-grown thin (<1 μm) hybrid GaAs/Ge "virtual" buffer approach provided 1J GaAs cell efficiency of ~10% on Si, as compared with cell structures with thick 3 μm GaAs buffers. Solar cell results were further corroborated with material analysis to provide a clear path for the reduction of performance

limiting dislocations. The thin "Ge-on-Si" virtual buffer was then investigated comprehensively to understand the impact of the heterostructure on device performance. The growth, structural, morphological, and electrical transport properties of epitaxial thin-film Ge, grown by solid source MBE on Si using a two-step growth process, were investigated. High-resolution x-ray diffraction analysis demonstrated ~0.10% tensile strained Ge epilayer, owing to the thermal expansion coefficient mismatch between Ge and Si, and negligible epilayer lattice tilt due to misfit dislocations at the Ge/Si heterointerface. Micro-Raman spectroscopic analysis further corroborated the strain-state of the Ge thin-film on Si. Cross-sectional transmission electron microscopy revealed the formation of a 90° Lomer dislocation network at the Ge/Si heterointerface, suggesting the rapid and complete relaxation of the Ge epilayer during growth. Atomic force micrographs exhibited smooth surface morphologies with surface roughness < 2 nm. Hall mobility measurements, performed within a temperature range of 77 K to 315 K, and the modelling thereof indicated that ionized impurity scattering limited carrier mobility in the thin Ge epilayer. Additionally, capacitance- and conductance-voltage measurements were performed after fabricating the metal-oxide-semiconductor capacitors (MOS-Cs) in order to determine the effect of epilayer dislocation density on interfacial defect states (D_{it}), bulk trap density, and the energy distribution of D_{it} as a function of temperature for electronic device applications. Deep level transient spectroscopy was used to identify the location (within the Ge bandgap) of electrically active trap levels; however, no significant trap levels were detected. Finally, the extracted D_{it} values were benchmarked against previously reported D_{it} data for Ge MOS devices, as a function of threading dislocation density within the Ge layer. The results obtained in this work were found to be comparable with other Ge MOS devices integrated on Si via alternative buffer schemes. The understanding gained from this comprehensive study of Ge-*on*-Si will help optimize the 1J GaAs on Si via thin Ge buffer approach, to enable a future of high efficiency low cost solar cells for terrestrial applications.

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GENERAL AUDIENCE ABSTRACT

The global energy landscape is projected to change remarkably in the coming decades with dwindling carbon based resource reserves and escalating energy demands, necessitating large-scale adoption of cleaner alternatives, such as solar energy. However, for widespread commercial and domestic adoption of photovoltaics, the cost of solar generated electricity must become competitive with non-renewable resources such as oil or coal. Thus, achieving high efficiency solar cells and driving down cell costs are key research objectives of the photovoltaic (PV) community in order to become more self-sufficient in the energy sector. In this pursuit, III-V compound semiconductor-based solar cells have steadily outperformed all other PV technologies, but cost-prohibitive for terrestrial deployment. Si is the undisputed standard in the PV industry; thus, to make a significant step forward in the pursuit of high efficiency solar cells, a promising approach will be to integrate the superior properties of compound semiconductors with the mature technology of Si. This research systematically investigates the integration of high efficiency III-V cells with low cost, abundant Si substrates via a germanium (Ge) layer to unify the performance merits of III-V cells with the cost benefits and superior mechanical and thermal properties of Si. Concurrently, Ge has also emerged as a strong candidate to boost transistor performance at low operating voltages, primarily owing to its superior carrier mobility and ease of integration into mainstream Si process flow. This research further delves into the structural and electrical properties of the Ge on Si structure. Overall, this research demonstrates the feasibility of the use of Ge directly integrated on Si for high efficiency solar cells and low-power electronic devices.

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Chapter 1

Introduction

1.1 Motivation for III-V on Silicon Solar Cells

The global energy landscape is projected to change remarkably in the coming decades with dwindling carbon based resource reserves and escalating energy demands. The looming energy crisis coupled with increasing evidence of climate change will necessitate large-scale adoption of cleaner alternatives, such as solar energy. Solar energy has immense potential to reduce climate change, curtail consumer expenditure, and generate jobs. In fact, if solar modules were 20% efficient at turning solar energy into power, we would only need to cover a land area about the size of Spain to power the entire Earth renewably in 2030. However, for widespread commercial and domestic adoption of photovoltaics, the levelized cost of solar generated electricity must become competitive with sources such as oil or coal.

III-V compound semiconductor based multijunction solar cells have been the most successful technology for delivering the highest photovoltaic conversion efficiency in niche applications in space and under concentration (Fig. 1.1). The performance of single-junction (1J) Si solar cells has almost saturated at ~26%, with the most recent accomplishment of 26.3% efficiency [2]. In contrast, III-V solar cells have steadily shown performance improvement, with the most recent world record efficiency of 46% at 508 suns for a bonded four-junction GaInP/GaAs/GaInAsP/GaInAs solar cell [2]. Despite achieving the highest conversion

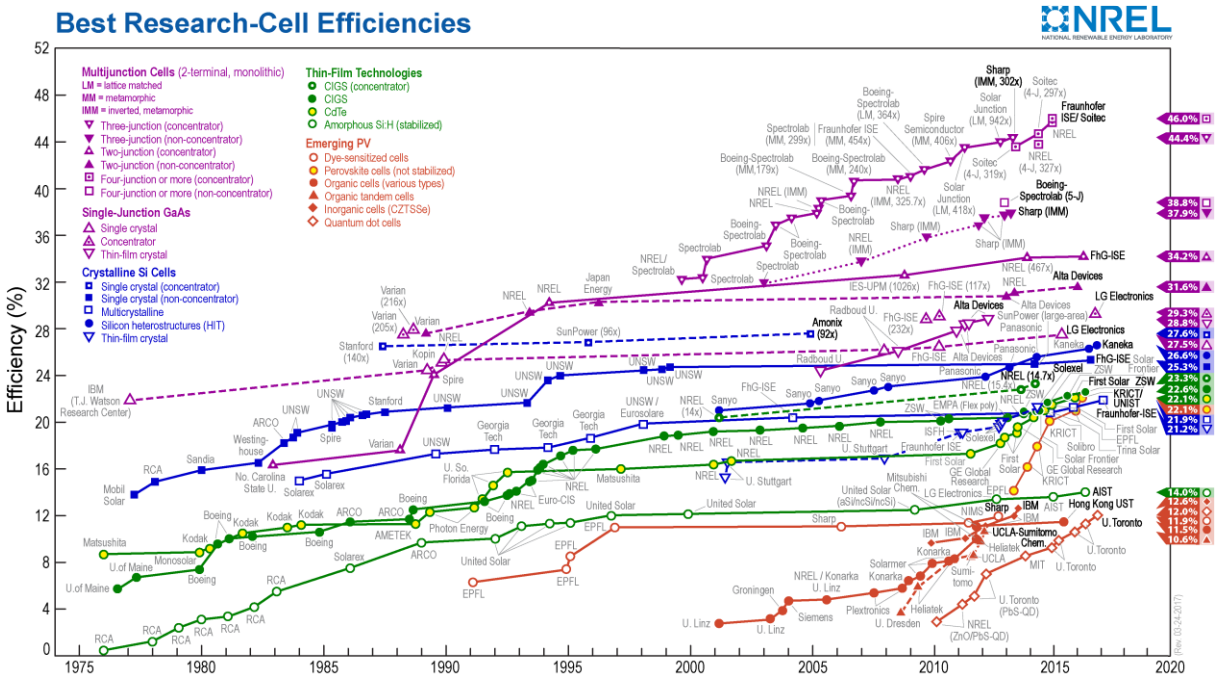

Figure 1.1: Conversion efficiencies for research cells, from 1976 to the present, for a range of photovoltaic technologies, NREL 2017 [1].

efficiency amongst all competing photovoltaic technologies, their expensive cost has been the major impediment in their large-scale deployment for terrestrial applications. The dominance of Si solar cells and their plummeting prices in recent years have made it challenging for high efficiency III-V solar cells to make a strong commercial impact. One of the most significant cost contributors to the bill of materials for III-V solar cells is the cost of the starting substrate. Germanium (Ge) is often the material of choice for bottom subcell and substrate for these high efficiency tandem multijunction cells (i.e., InGaP/GaAs/Ge), due to its close lattice match to GaAs and InGaP materials, used in the junctions above, and its low bandgap of 0.66 eV. In addition, Ge or GaAs substrates are typically used for subsequent III-V solar cell growth, and these are not only smaller in diameter, but also significantly more expensive than Si substrates. Therefore, successful integration of III-V solar cells on Si substrate can offer a great promise for lowering the future levelized cost of energy by unifying the high efficiency merits of the III-V materials with the low-cost and abundance of the Si substrate. In addition to the economic benefits associated with the larger area and low cost of Si substrate, Si also offers higher

thermal conductivity and superior mechanical strength in comparison to GaAs or Ge substrates. The research on integrating III-V compound semiconductor materials on Si substrate for photovoltaic application was initiated in 1980s. The fundamental challenges of GaAs on Si epitaxy lay in the 4% lattice mismatch between GaAs and Si, the growth of a polar compound semiconductor on non-polar Si, and the large difference (63%) in thermal coefficient between GaAs and Si, which leads to the photoactive region being sensitive to dislocations, anti-phase boundaries and thermal cracking. A promising approach for this heterintegration is the introduction of a thin Ge epilayer between the Si substrate and the GaAs subcell, thereby creating a virtual "Ge-*on*-Si" template for subsequent lattice matched GaAs cell growth. This approach decouples two challenges, viz. that of lattice mismatched growth and polar on non-polar epitaxy, at separate interfaces. Moreover, the Ge-*on*-Si template can be further extended to develop a hybrid Ge-Si active junction below the GaAs cell, where the Ge layer serves as the emitter in a bottom Si sub-cell. Hence, the succesful integration of low defect density Ge thin film on Si will enable the realization of high efficiency low cost III-V solar cells on large area Si substrate. Furthermore, in the past decade, the integration of thin Ge or its compound SiGe on Si has received widespread attention in the semiconductor research community as Ge was rediscovered as the material of choice to maintain device performance for future technology nodes.

1.2 Emergence of Electronics and Photonics with Germanium

Since its first experimental demonstration in 1959 [3], Si-based Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET) has remained the driving force for the semiconductor industry in the last five decades. Although the working principle of the MOSFET has remained the same, the physical dimensions have been continually reduced to double the number of transistors on a chip every two years following Moore's Law [4]. This exponential decrease in transistor dimensions resulted in increase in microprocessor performance over technology

generations. However, the conventional device dimension scaling could not continue forever, primarily due to increased power consumption and the impact of supply voltage scaling on device performance.

As scaling reached sub-100nm regime, more non-silicon elements were introduced to Si technology at every generation. At the 90 nm node, carrier mobility, μ, was increased through the implementation of uniaxial strain on the Si channel using Silicon-Germanium (SiGe) source/drains and silicon nitride (Si_3N_4) stressor layer, thereby enhancing PMOS and NMOS transistor drive current, respectively [5]. At the 45 nm node, a metal gate and a scalable high-κ gate dielectric (i.e., HfO_2) was used to further enhance transistor drive current by increasing oxide capacitance, C_{ox}, while reducing the off-state leakage current, an issue that plagued the semiconductor industry with silicon dioxide (SiO_2) dielectric scaling [6]. At the 22 nm node, a novel Fin Field-Effect-Transistor (FinFET) design was implemented, yielding more gate control and thus better device performance at lower gate voltages [7]. Currently in production are 14 nm transistors, which implement a taller fin design to aid with increased drive current and allow continued die area shrinkage [8]. In this pursuit, Intel reported the 14 nm node transistor density to be approximately 38 million transistors per millimeter squared [9].

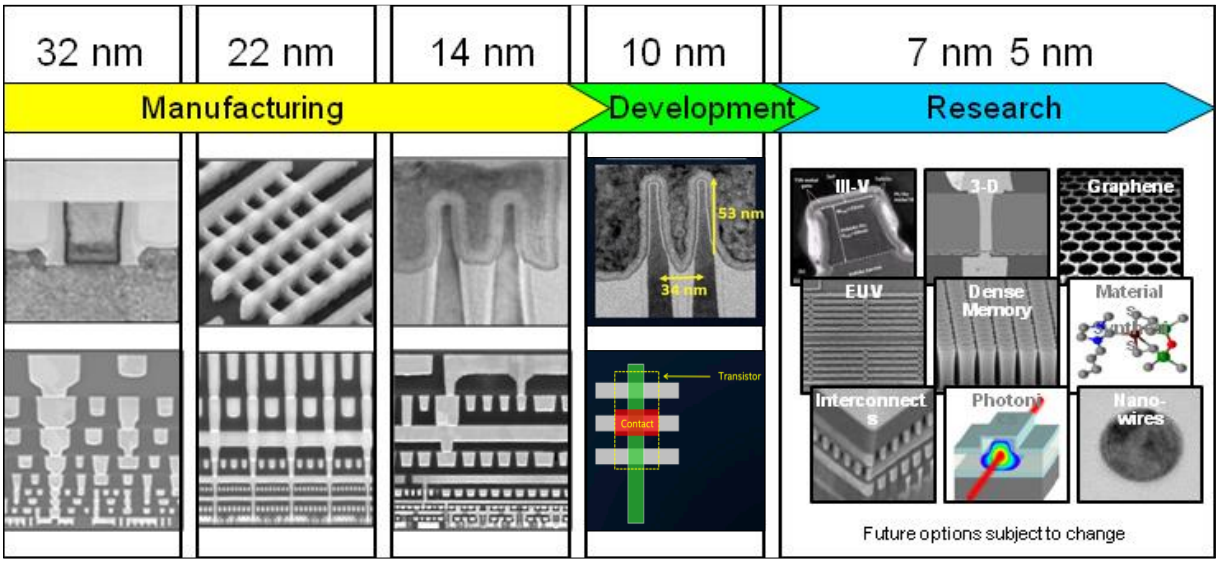

Figure 1.2: Silicon research and development pipeline, Intel 2015-2017 [9].

Industry giants such as Intel, IBM and Applied Materials have suggested the introduction of a SiGe channel for 7 nm node and beyond [10]. Fig. 1.2 shows the evolution of the Si-based MOSFET in the last decade, from the 32 nm node down to the 14 nm node, and the projected future of these devices for smaller nodes. As traditional performance increase begins slowing down, novel materials and device architectures will become necessary to boost transistor performance. According to the 2015 ITRS, III-V, Ge, carbon nanotube, and 2D materials are examples of such channel materials under consideration for future nodes [11].

Ge is particularly of great interest as channel material, owing to its high bulk hole and electron mobilities and ease of integration into mainstream Si process flow. The fundamental physical properties of Ge are compared with Si and several other III-V semiconductors in consideration are given in Table I. Ge has a smaller effective mass (m_e) for electrons and also a smaller effective mass in the heavy hole (m_{hh}) and light hole (m_{lh}) bands compared to Si. Bulk mobilities in Ge are 2.8× and 4.2× higher for electrons and holes, respectively, as compared to

Parameters	**InSb**	**InAs**	**Ge**	**GaSb**	**$In_{0.53}Ga_{0.47}As$**	**Si**	**InP**	**GaAs**
Electron effective mass (m_e/m_0)	0.014	0.023	1.59 0.0815	0.041	0.041	0.98 0.19	0.08	0.063
Hole effective mass: (m_{hh}/m_0) (m_{lh}/m_0)	0.43 0.015	0.41 0.026	0.33 0.043	0.4 0.05	0.051	0.49 0.16	0.6 0.089	0.51 0.082
Electron mobility (cm^2/Vs)	77,000	40,000	3900	3000	12,000	1400	5400	8500
Hole mobility (cm^2/Vs)	850	500	1900	1000	300	450	200	400
Dielectric Constant	16.8	15.15	16.2	15.7	12.5	11.7	12.5	12.9
Bandgap (eV)	0.18	0.36	0.66	0.726	0.74	1.12	1.35	1.42
Lattice mismatch to Si (%)	19.3%	11.6%	4.2%	12.1%	8.1%	0%	8.1%	4.05%

Table 1.1: Basic parameters of common semiconductor channel materials [12].

those of Si. A smaller effective mass and higher carrier mobility in Ge can potentially lead to higher drive currents in Ge MOSFETs than in Si MOSFETs. Furthermore, its low bandgap of 0.66 eV makes Ge a suitable candidate for low-power devices operating at low supply voltage (≤ 0.5 V) while still mitigating leakage from band-to-band tunnelling and thermionic emission that would otherwise plague very low-bandgap materials.

With the boom in computational power, enabled by the shrinking size of transistors, interconnect bottlenecks for both interchip and intrachip communication are projected to be major impediments to energy-efficient performance scaling. As nanotechnology provides increased circuit densities in smaller nodes, the RC delay increases leading to increase power density of Si devices (Fig 1.3). This is especially seen in parallel computing applications where the ability to communicate within a single chip of multiple components decreases as the density of components increases. Therefore, there is a pressing need for large bandwidth, low-resistance interconnects in exa-scale computing applications, as copper-based electrical interconnects become inefficient in meeting essential bandwidth requirements. With hyperscaling of processors, it will become increasingly challenging to transmit signals electrically while maintaining low power consumption, low delay, and a high signal-to-noise ratio. A promising approach to address these limitations is the integration of photonic devices with Si technology. The indirect bandgap of Si limits the realization of Si-based photonic devices; hence, the hybrid integration of Ge and III−V materials-based optoelectronic devices with traditional Si CMOS technology would revolutionize technology needs in the near future.

On material compatibility, Ge covers all CMOS prerequisites. Furthermore, Ge has been demonstrated to work as the active material in modulators, lasers and photodetectors. Thus, Ge is suggested as the most suitable material capable of conforming to the CMOS standards and

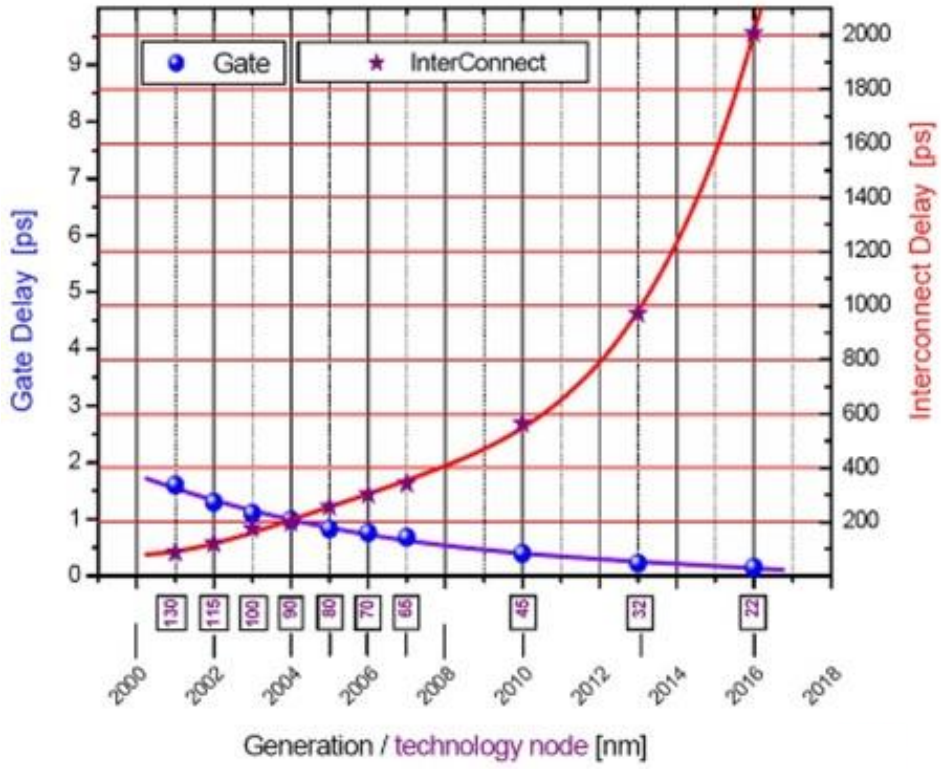

Figure 1.3: Increasing trend in RC interconnect delay with decreasing technology node, Applied Materials. [13]

be a light emitter for photonic integration. Researchers have focused on the development of Ge-based electronic and optoelectronic devices, including: (i) Ge lasers on Si for on-chip integrated photonics [14,15]; (ii) high-speed and high-sensitivity Ge photoreceivers on Si for optical data communication [16,17]; (iii) Ge-based MOSFETs for low-power logic [18,19]; (iv) Ge-based CMOS integrated circuits [20]; and (v) Ge-based quantum well FinFETs [21-23] for next-generation high-speed, low-power logic applications. However, two major challenges must be dealt with before Ge can be considered as a viable replacement as a future channel material; the device-quality heterogeneous integration of Ge on Si substrate and the development of a suitable gate stack for Ge.

1.3 Integration of Ge on Si substrate: Challenges and Approaches

To bring Ge based alternative channel into high-volume production, it must be made compatible with modern Si manufacturing process. Moreover, to lower levelized cost of solar

power, we must integrate high efficiency III-V solar cells grown on Ge onto large area Si substrates. The most challenging semiconductor growth issue is that of Ge's lattice constant being 4.2% larger than that of Si. As a result of the lattice mismatch, Ge epitaxy on to Si substrate results in the relaxation of the Ge film via the formation of misfit dislocations at the heterointerface. These dislocations can propagate close to the surface and deleteriously impact device performance by reducing both carrier mobility and carrier lifetime while increasing junction leakage. In solar cells, diclocations in the active region act as carrier recombination centers and limit current, and thus conversion efficiency in the device. In addition to the lattice mismatch, there is also a significant thermal mismatch between Ge and Si, due to the large difference in the thermal expansion coefficients of Ge (6.1×10^{-6}/K) and Si (3×10^{-6}/K) [24]. The thermal strain developed due to this large thermal mismatch can lead to macroscopic cracks in the device. To overcome these challenges several integration approaches have been pursued by Ge researchers, including wafer bonding, graded buffers, metamorphic buffers, substrate patterning and selective area growth, shallow trench isolation (STI) structures, and nanocontact epitaxy. Here we discuss some of these routes that have been pursued in order to heterogeneously integrate Ge onto Si substrate, as well as their shortcomings.

The graded Si_xGe_{1-x} buffer approach seeks to introduce the 4.2% lattice mismatch between Ge and Si substrate (x=1) gradually rather than abruptly with the goal of producing high-quality Ge films above the buffer (x=0). Relaxation occurs continuously during growth, and mismatch strain is alleviated by the strain-relieving glide of threading dislocations, allowing for the threading dislocations present in the initial low-Ge composition layers to suppress the nucleation of additional dislocations in the higher-Ge composition layers. Currie et al. [25] demonstrated epitaxial Ge films with threading dislocation density (TDD) as low as 2.1×10^6 cm^{-2}, on the order of bulk Ge substrates. This particular graded Si_xGe_{1-x} buffer growth involved a chemical-mechanical-planarization (CMP) step at 50% Ge grading, to prevent dislocation

pile-up due to a blocking of the threading dislocation glide, a complication observed in thicker grades to high Ge concentration. However, the Si_xGe_{1-x} buffer was 12 μm thick, which adds to overall process cost; had thermal mismatch induced cracks due to thick buffer layer; and had *rms* roughness of 24.2 nm, which was too rough for device definition. Though *rms* roughness of SiGe buffers can be controlled by low temperature growth and very gradual grading, these buffers suffer from large thickness and thermal strain related cracks in device layers. Loh et al. [26] demonstrated a Ge epilayer with TDD of 5×10^5 cm^{-2} and *rms* roughness of 1.4 nm using only a 160 nm thick buffer layer. The composite buffer consisted of a 30 nm $Si_{0.8}Ge_{0.2}$ buffer layer, followed by a 30 nm Ge seed layer grown at low-temperature, and then capped with a smooth 100 nm Ge epitaxial layer grown at high-temperature. However, despite the progress in developing optimal Si_xGe_{1-x} buffers, this approach fails in that it does not provide suppression of parallel conduction nor effective device isolation. The Si_xGe_{1-x} buffer bandgap, which lies between that of Ge and of Si (0.66 eV to 1.12 eV), provides additional higher conductivity paths not ideal for suppression of parallel conduction and fails to ensure electrical isolation of devices.

Germanium-on-insulator (GeOI) approach offers the heterogeneous integration of Ge onto Si substrate through the incorporation of a high bandgap oxide buffer, which allows suppression of parallel conduction as well as effective device isolation. There are various ways to form GeOI wafers, most popular methods being thermal oxidation of SiGe layers and wafer bonding of donor Ge wafers onto SOI wafers. The wafer bonding approach, commercially known as Smart Cut™ technology has been able to achieve *rms* roughness of less than 2Å and estimated TDD below 10^6 cm^{-2}, thus offering excellent Ge surfaces for device definition. Despite the fact that the GeOI approach helps achieve high-quality Ge surfaces and succeeds where the Si_xGe_{1-x} buffer fails, namely eliminating parallel conduction as well as device isolation, the major shortcoming of the GeOI approach lies in the large thermal mismatch between the Ge layer and

the oxide layer. Standard CMOS process and integration typically involve multiple thermal annealing steps, but these devices suffer from thermal instability at high temperatures. Moreover, CMOS applications see usage in microprocessor logic, where high thermal budget are induced as a result of regular computing usage. Ge bonded to an SiO_2/Si wafer faces thermal issues due to the thermal coefficient of SiO_2 being 5.6×10^{-7}/K [27] whereas that of Ge being 6.1×10^{-6}/K [25]. As a result of this large thermal strain, it is possible for cracks to propagate through repeated exposure to high thermal budgets and deleteriously affect device performance, or causing complete failure of GeOI devices.

Nanocontact epitaxy utilizes elastically strain-relaxed Ge nanodots without misfit dislocations as seed crystals for defect free Ge growth. Very high density of Ge nanodots (NDs) are grown epitaxially on the Si substrate with limited contact between the NDs and the Si substrate through nanowindows in an ultrathin SiO_2 film. NDs fabricated by this method are elastically strain relaxed with lattice constants that are almost the same as that of the bulk material. A second layer of Ge is grown to flatten the growth surface, and then a final Ge layer is grown to obtain a highly crystalline and smooth film. Typically, the resulting Ge films possess *rms* surface roughness of ~0.4 nm and etch pit densities of 10^4 to 10^5 cm^{-2}. However despite fewer misfit dislocations, the complex growth process leads to appearance of stacking faults in the material, as well as extended defects due to coalescence of NDs. [28]

These heterointegration methods, albeit innovative, continue to encounter myriad challenges that hinder large scale adoption of Ge devices in the semiconductor industry. On the contrary, the direct epitaxy of Ge layer on Si remains by far the most cost effective path for Ge integration on Si process platform and necessitates a comprehensive study of the structural, morphological and electrical properties of the Ge-*on*-Si heterostructure.

1.4 Thesis Objective and Organization

The objective of this research is to investigate the viability of direct Ge-*on*-Si heteroepitaxy by MBE for (i) integration of III-V solar cells on Si and (ii) alternate channel material; by systematically and comprehensively studying the carrier transport properties, oxide-semiconductor heterointerface characteristics and structural defects that influence electrical performance of the monolithic Ge-*on*-Si heterostructure. The thesis detail the impact of this material stack used as buffer layer in the heterogenous integration of single junction (1J) GaAs solar cells on Si, and compare this approach with the direct epitaxy of GaAs cells on Si substrate. To further understand the findings, the research work devoted to this will study the growth and characterization of thin Ge on Si, in addition to the electrical and interfacial properties of the material stack, to understand its potential for low-power electronic applications.

This thesis is organized in to seven chapters. ***Chapter 2*** presents the experimental techniques related to growth and material characterization used throughout this research, including the basic principles of MBE and various surface and material characterization methods. ***Chapter 3*** presents the experimental techniques related to electrical characterization of solar cells and MOS capacitors used in this research, and includes a brief synopsis on the operating principles of MOS capacitors. ***Chapter 3*** also presents experimental techniques related to carrier mobility investigation in this heterostructure and fundamentals of the theoretical modeling of these measured mobility values. ***Chapter 4*** presents the use of Ge-*on*-Si heterostructure as a metamorphic buffer for integration of GaAs solar cells on Si substrate. In this chapter, we investigate the performance of 1J GaAs cells grown on Si using two different all epitaxial III-V/IV buffer approaches as an alternative to III-V cells grown on expensive and smaller diameter Ge or GaAs substrates. The initial approach is the direct epitaxy of GaAs cells on Si

using a thick GaAs buffer while the second approach is the introduction of the Ge/Si heterostructure investigated above underneath a thin GaAs buffer, thereby creating a virtual "Ge-*on*-Si" template for subsequent GaAs growth. ***Chapter 5*** presents a comprehensive investigation of the structural and optical properties of Ge directly integrated on to Si. The epitaxial Ge-*on*-Si heterostructure was examined using various material characterization methods, including atomic force microscopy, Raman spectroscopy, X-ray reciprocal space maps (RSMs), photoluminescence spectroscopy and transmission electron microscopy to determine the crystal quality, strain relaxation, defect density, and abruptness of the epitaxial Ge layer**.** ***Chapter 6*** presents the electrical characterization of the Ge-*on*-Si heterostructures. To assess the electrical quality of the Ge epilayer, Hall mobility measurements are performed and the experimental data is fit via theoretical consideration of the scattering processes in Ge in order to isolate the dominant scattering processes limiting carrier mobility. MOS capacitors are fabricated using the Ge-*on*-Si heterostructure to study its interfacial properties. Deep-level transient spectroscopy (DLTS) is also used to measure electrically active trap levels within the epitaxial Ge film. Extracted performance parameters are then benchmarked against previously published Ge MOS data to investigate the viability of Ge-*on*-Si channels. Lastly, ***Chapter 7*** summarizes the conclusion of this work and presents the prospects for future avenues of research and investigation based upon this thesis' current findings.

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Chapter 2

Experimental Methodology: Material Synthesis and Characterization

2.1 Molecular Beam Epitaxy: Growth of Group IV and III-V Epilayer and Heterostructures

All structures studied in this thesis were grown by solid-source MBE, a technique to grow crystalline thin films epitaxially, in ultrahigh vacuum (UHV) with precise control of thickness, composition and morphology. Under MBE growth conditions, thermal evaporation of high-purity, elemental liquid or crystalline sources generates a molecular beam of neutral atoms or molecules that is directed towards a growth substrate. To optimize the flux of material impinging on the growth surface and maintain a consistent growth environment, the growth chamber is kept under UHV with residual gas pressure below 10^{-9} Torr in the reactor chamber during growth. Such strict vacuum conditions increases the mean-free path of the constituent atomic or molecular species, thereby minimizing collisions between beam particles and the background vapor and promoting high-purity, low-defect epitaxy. A combination of oil-free roughing, turbo, ion, and cryogenic pumps are typically employed to generate the UHV environment critical for MBE growth.

Fig. 2.1 shows a schematic diagram for a typical MBE reactor chamber [1]. In addition to using various pumping systems to maintain the UHV background, several measures are taken

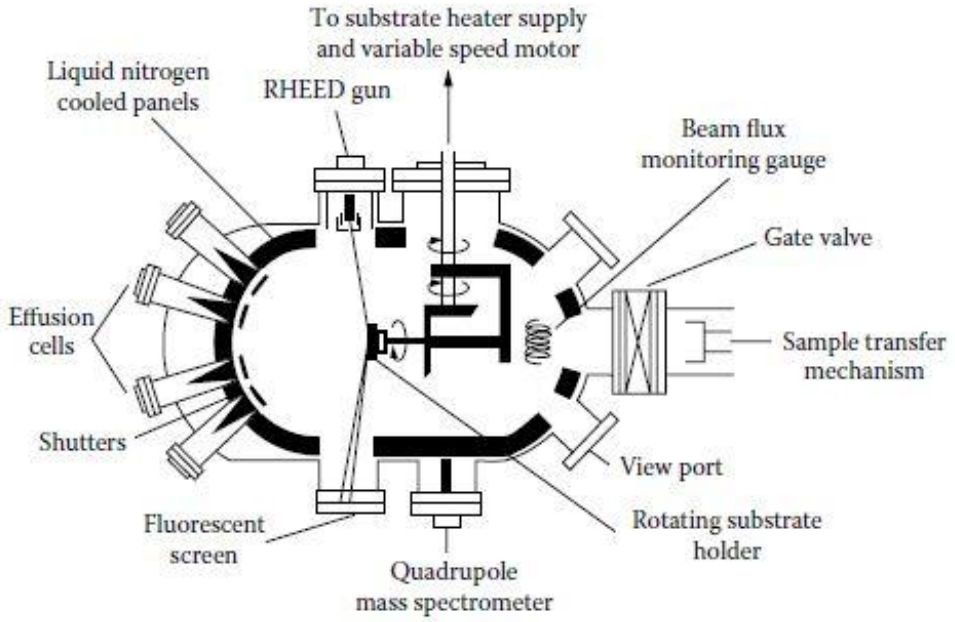

Figure 2.1: Schematic representation of typical MBE reactor chamber [1]

prior to growth to minimize residual atomic species contamination. system to atmosphere. Further, baking of the individual effusion or cracking cells for each elemental species also aids in degassing the required growth materials and minimizing contamination. Additionally, as can be seen in Fig. 2.1, the walls of the growth chamber are cooled using a cryogenic (liquid N_2) shroud to minimize any undesirable flux generation from atomic or molecular species coating the reactor's walls [2]. Similarly, components such as shutters and heaters are machined from highly stable, non-reactive and low-vapor pressure materials, e.g., tantalum (Ta), molybdenum (Mo), or pyrolytic boron nitride (PBN). Substrate wafers undergo several degassing steps prior to growth, including: (i) an 180^{o}C, three-hour long bake in a loading chamber to remove moisture from the substrate surface, substrate holder, and intro-chamber; (ii) a 300-400^{o}C (depending on the substrate material) two- hour long bake in a buffer chamber to degas higher-temperature surface contamination before transferring to the growth chamber; and (iii) a high temperature oxide desorption in order to remove surface native oxides formed under ambient atmospheric conditions, thereby generating a pristine starting surface for epitaxy.

At this stage, thin-film epitaxy proceeds by heating of the effusion or cracking cells (shown in Fig. 2.1 mounted opposite to the substrate) and generation of an elemental flux whose exposure time on the growth surface is actively controlled by individual motorized shutters. The flux levels required during growth are routinely calibrated prior to substrate loading using an ion gauge (shown in Fig. 2.1 behind the substrate holder) to measure the beam-equivalent pressure (BEP) of each source for a given source temperature. In order to ensure film composition and thickness homogeneity across the growth surface, the substrate holder is typically rotated at a speed of six to eight revolutions per minute (*rpm*).

In-situ surface monitoring is performed using reflection high-energy electron diffraction (RHEED) to monitor oxide-desorption and epitaxial growth. Electron beams nearly parallel to the growth surface are reflected on a phosphorous-coated screen, with the low angle of incidence limitng electron penetration into the sample to several surface monolayers, thereby only generating diffraction patterns of the two-dimensional surface lattice. This surface reconstruction in reciprocal space is known as a RHEED pattern [1]. Streaky RHEED patterns are obtained when ideal 2D, layer-by-layer (Frank-van der Merwe) growth is obtained [1]. In the case of island-like growth (known as Volmer-Weber growth), spotty RHEED patterns can be observed. In addition to surface monitoring, RHEED can also be used to precisely determine growth rate [1]. This is because RHEED intensity oscillation frequency is proportional to the epitaxial monolayer thickness [1]. With this relationship, a linear relation between the growth rate and BEP can be generated.

2.2 Atomic Force Microscopy (AFM): Surface Morphology Characterization

Atomic force microscopy (AFM) is a scanning probe microscopy (SPM) technique that can achieve angstrom-level vertical resolution during surface morphology characterization. As described in Fig. 2.2, an extremely sharp tip (3-6 μm tall pyramid with 15-40 nm end radius)

attached to a cantilever is passed over a sample surface, resulting in a vertical deflection or force exerted upon the cantilever [1]. This reaction of the probe to the forces that the sample imposes on it is measured by way of a laser diode, calibrated to the cantilever's top surface prior to measurement, wherein the reflected beam from the cantilever surface is incident upon a four-quadrant photodiode. As the cantilever moves across the sample, the deflection of the cantilever results in deflection of the position of the reflected beam on the photodiode with respect to its initial position. This, in turn, is translated into a measure of the vertical movement

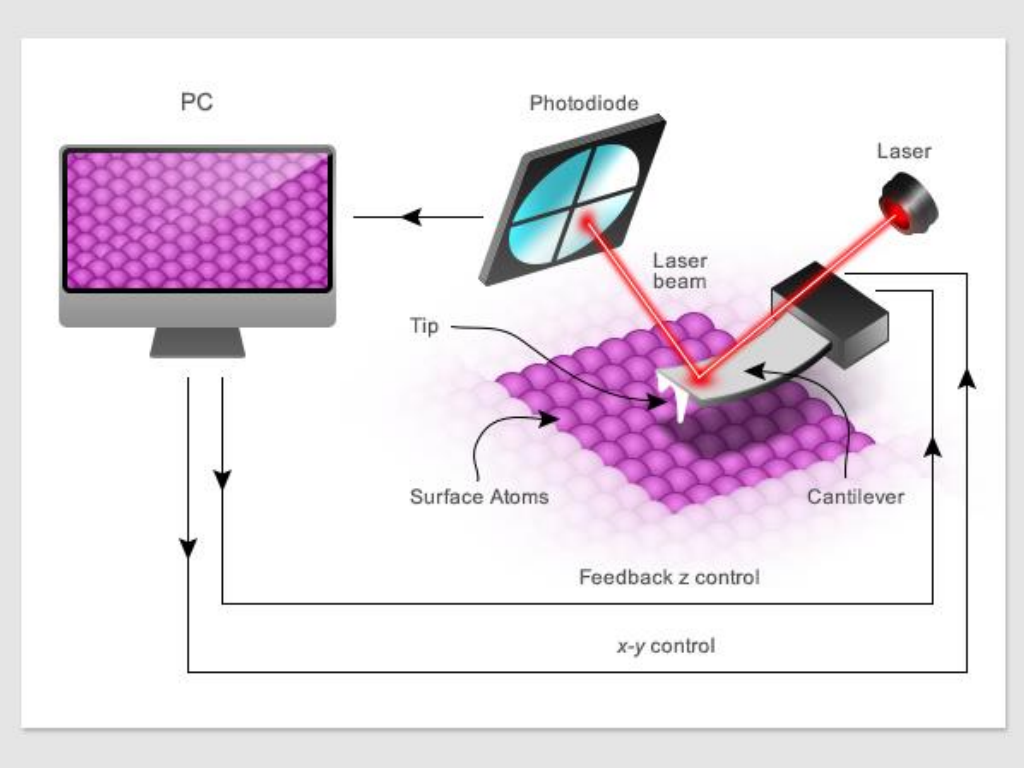

Figure 2.2: Atomic force microscopy setup, including laser diode and four-quadrant photodiode for measuring vertical displacement, the cantilever and probe tip.

of the cantilever and thus the height and topography of surface features on the sample. AFM setups may have a piezoelectric feedback system integrated into the sample mounting stage to maintain a constant force on the cantilever tip as it scans the sample surface. For a given sample, forces that are measured in AFM can include mechanical contact force, van der Waals forces, capillary forces, chemical bonding, electrostatic forces, magnetic forces, Casimir forces, solvation forces, etc.

2.3 Raman Spectroscopy: Thin Film Strain-State Analysis

Raman spectroscopy is a second-order (two-photon) optical measurement technique suitable for the characterization of strain in semiconductor thin films and superlattices. When photons are scattered by an atom or molecule, most photons are elastically scattered (Rayleigh scattering), such that the scattered photons have the same energy (frequency and wavelength) as incident photons. However, a small fraction of the scattered photons (approximately 1 in 10 million) are in-elastically scattered by an excitation, with the scattered photons having a frequency different from, and usually lower than, that of the incident photons (Raman scattering) [3]. The source of these additional scattering frequencies are the vibrational modes, i.e., phonon modes in a crystal, of the sample material. If the emitted radiation is of lower frequency than the incident radiation, then it is called Stokes scattering, whereas, if emitted radiation is of higher frequency, then it is called anti-Stokes scattering. Due to Stokes radiation being correlated with an increase in vibrational energy of the sample, and the fact that at room temperature most materials are in their lowest vibrational state, Stokes radiation is generally more intense than anti-Stokes radiation. Moreover, the vibrational, or phonon modes, that contribute to scattering are also correlated with the scattering geometry. In the case of back scattering from a (001) surface, such as the micro-Raman measurements performed in this thesis, the longitudinal optical (LO) phonons are polarized along the $\hat{z}$ direction, whereas the transverse optical (TO) phonons are polarized along the $\hat{x}$ and $\hat{y}$ directions. Consequently, under (001) back scattering collection geometries, only LO phonon modes contribute to the detected scattered spectra. Furthermore, under strain, the normally degenerate phonon modes will be lifted, resulting in a change in the LO phonon mode frequency and thus a change in the observed Raman frequency [4]. Fig. 2.3 shows a typical micro-Raman spectroscopy setup, in which an Ar laser is filtered, polarized, and focused on a sample surface through a confocal microscope down to a spot size of approximately 1 μm [5]. The scattered light from the sample

is collected through the microscope (known as a back scattering collection geometry) and directed into a double pre-monochromator, after which it enters the spectrometer prior to being detected by either a multichannel or CCD detector. As the back scattered light passes through the pre-monochromator and spectrometer, the position of the gratings and the width of the slits in both equipment determine the resolution and intensity of the detected spectral peak. In cases where the scattered intensity is low, a photomultiplier tube may be included in the measurement setup prior to the detection stage. In this thesis, a JY Horiba LabRam HR800 micro-Raman system equipped with a 514.32 nm Ar laser excitation source was used to measure the relaxation state of Ge thin films, and further corroborated by x-ray diffraction measurements.

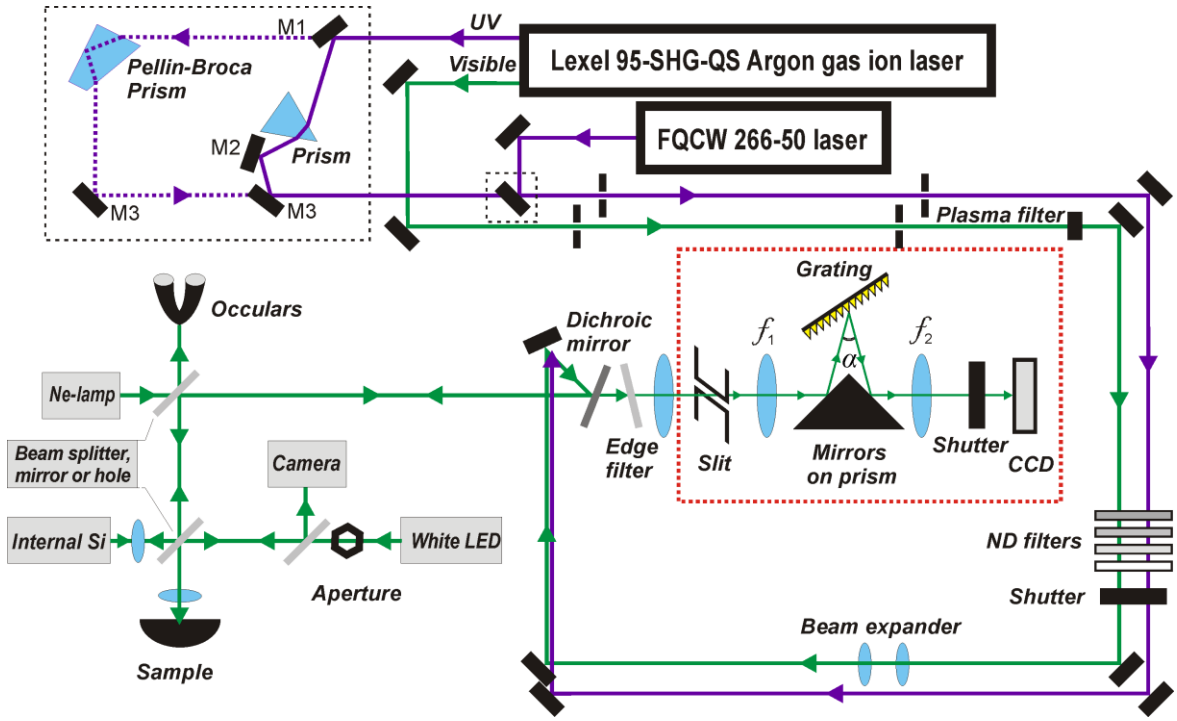

Figure 2.3: Micro-Raman Spectroscopy experimental setup

2.4. X-ray Diffraction: Thin Film Strain and Structural Analysis

High-resolution X-ray diffraction (HR-XRD) is a critical tool for structural characterization and determination of strain relaxation properties in heteroepitaxial layers. Fig. 2.4 shows a typical HR-XRD system, including: (i) an X-ray source (usually a copper (Cu) tube) that produces a broad spectrum, divergent beam of X-rays; (ii) a four-bounce Bartels

monochromator that restricts the beam to a specific wavelength (energy) and angular divergence; and (iii), the sample and scintillation detector placement, including the rotation axes for both. For rocking curve measurement, the sample is rotated about the ω-axis, resulting in a spectrum containing peaks of various intensity, width, and angular position that directly correspond to the epitaxial layers present in the sample and their structural properties. These spectra are then used to analyze the strain relaxation properties and structural quality of the sample.

X-ray crystallography is built on the real and reciprocal space geometric equivalence for angular diffraction, using the Bragg and Laue equations, respectively. Fig. 2.5 shows the Bragg

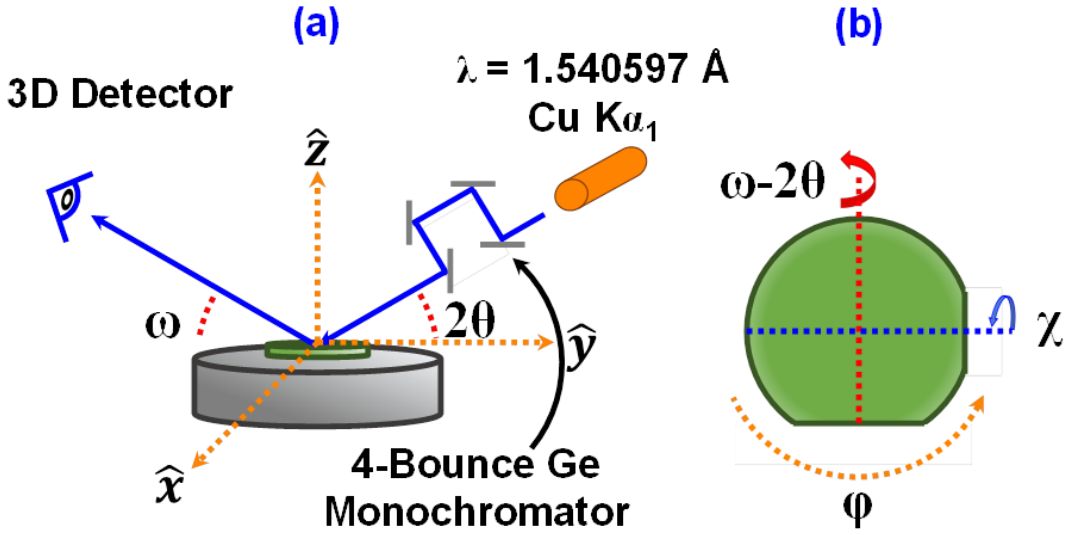

Figure 2.4: **(a)** Conventional high-resolution X-ray diffraction setup, including a Cu tube X-ray source, 4-bounce Ge monochromator, multi-axis sample stage, and 3D detector. **(b)** Sample surface showing the angular axes rotated during rocking curve and reciprocal space map measurements.

diffraction conditions for incident X-rays in a uniformly flat, periodic crystal structure wherein the spacing between crystal planes is given by d [1]. If the incidence and reflection angles are equal to θ, then the path difference, Δ, between two parallel X-ray beams, a and b, is equal to $2d\sin\theta$. In this case, the condition for constructive interference becomes $\Delta = n\lambda$, where n is an

integer and λ is the X-ray wavelength (1.540597 Å in this thesis). Thus, the Bragg diffraction condition is given by [1]:

$$2dsin\theta_B = n\lambda$$

where n is the order of reflection, θ_B is the Bragg angle, d is the inter-atomic plane spacing, and λ is the X-ray wavelength, as previously defined. The equivalent Laue equation for reciprocal space is given by [1]:

$$d\ (h,k,l) = \frac{a}{\sqrt{h^2 + k^2 + l^2}}$$

where a is the crystal's lattice spacing and (*hkl*) define the indices of the atomic plane under investigation in reciprocal space. Equating these equations, the Bragg angle, θ_B (*hkl*), for an atomic plane specified by the (*hkl*) indices can be rewritten as:

$$\theta_B\ (hkl) = \sin^{-1}\frac{\sqrt{h^2 + k^2 + l^2}}{a}$$

The detailed strain relaxation analysis for diamond and zinc-blende semiconductors requires the recording of reciprocal space maps (RSMs), which consist of several hundred rocking curves taken at incrementally different ω center points in order to graph a two-dimensional

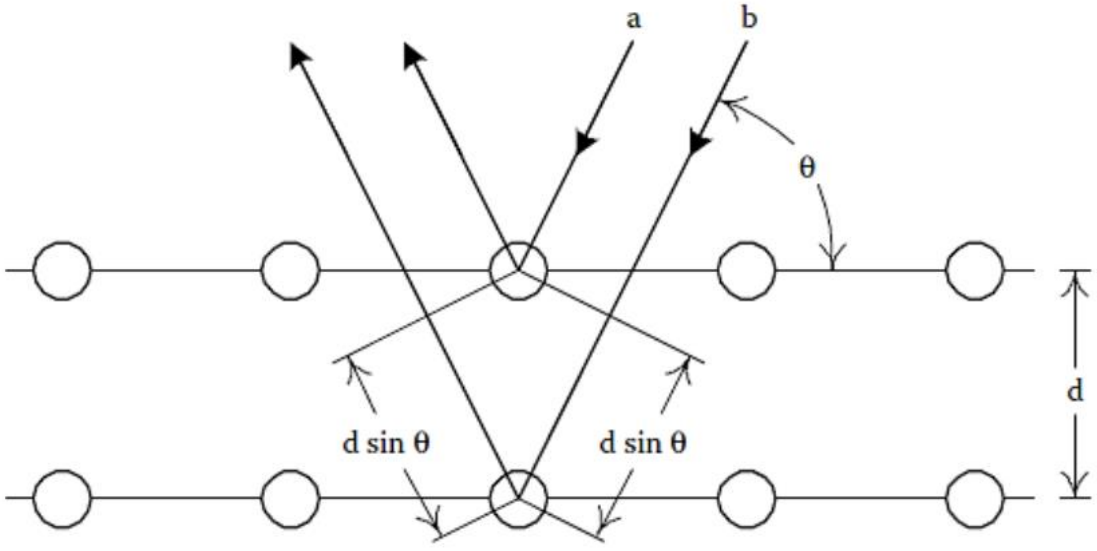

Figure 2.5: Schematic diagram of the Bragg diffraction condition for a single crystal, periodic structure.

map (*ω-2θ*) of the diffraction angles (vs. intensity) present in the sample. Because of asymmetric dislocation relaxation along the two orthogonal [110] and $[1\bar{1}0]$ directions, the in-plane lattice constants $a_{[110]}$ and $a_{[1\bar{1}0]}$ could be different. To account for this during measurement, the incident X-ray beam is aligned with each orthogonal <110> in-plane direction in order to measure the anisotropy in strain relaxation in the sample, should any exist. Using Bragg's law, the in-plane, $a_{\parallel}$, and out-of-plane, $a_{\perp}$, lattice constants for each layer can be determined from the asymmetric (115) and symmetric (004) RSMs, respectively. Subsequently, the relaxed lattice constant, a_r, and epitaxial strain, ε, of each layer can be determined using [6]:

$$a_r = \frac{2v}{1+v} a_{\parallel} + \frac{1-v}{1+v} a_{\perp}$$

$$\varepsilon = \frac{a_r - a_s}{a_s}$$

where ν is the Poisson ratio of each epilayer and a_s is the lattice constant of the substrate.

Fig. 2.6 shows a schematic representation of symmetric (004) and asymmetric (115) RSMs plotted according to *q* vector. The *q* vector of each epilayer in the schematic consists of two components, q_x and q_z, corresponding to the angular splitting between *ω* and *2θ*, respectively, in real space. As shown in the diagram, different strain states and degrees of relaxation can result in different positions of the reciprocal lattice point (RLP) for each epilayer, including fully strained (pseudomorphic), fully relaxed (metamorphic), partially relaxed, or tilted (α) [7]. In the case of an ideal, fully relaxed epilayer without tilt, the (115) RLP will lie on a line of relaxation that intersects the (004) axis at an angle of 15.8°. On the other hand, a fully strained

epilayer's (115) RLP will lie on a strain line that connects it via the (001) directed axis to its virtual substrate.

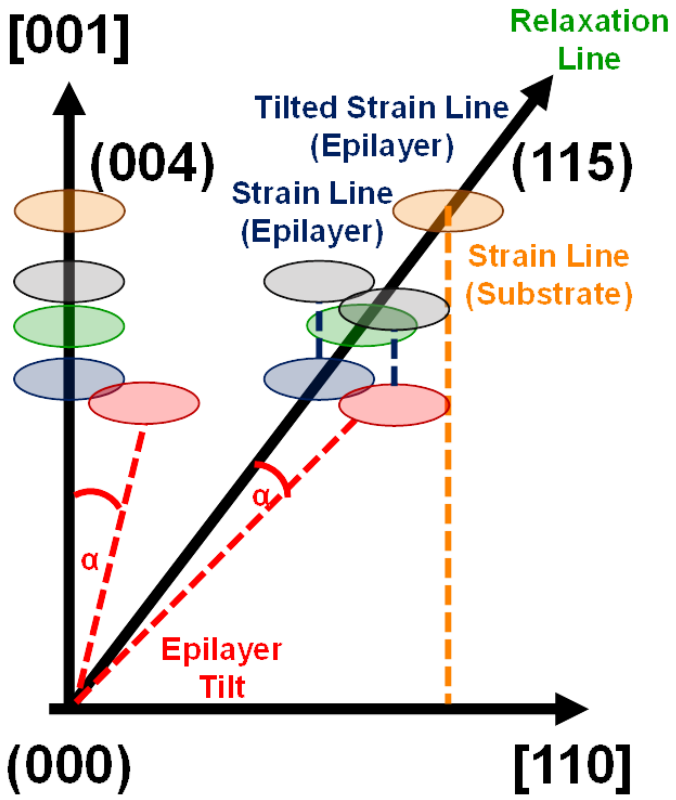

Figure 2.6: Reciprocal space schematic highlighting the sample orientations in real space as well as the crystallographic orientations in reciprocal space. The epitaxial layers of interest (blue shows virtual substrate strain template, and green shows strained layer) are shown under two different conditions: no epitaxial tilt (the virtual substrate strain template is oriented along the sample normal and full relaxation lines) and small epitaxial tilt (deviation away from the sample normal and full relaxation lines introduces an 'artificial error' in the measured strain relaxation properties).

2.5. Transmission Electron Microscopy (TEM): Defect and Structural Analysis

High-resolution transmission electron microscopy (HR-TEM) is an excellent technique to characterize the long- and short-range structural quality of samples as well as defect propagation in the sample, and the coherence and abruptness of heterointerfaces. In order to

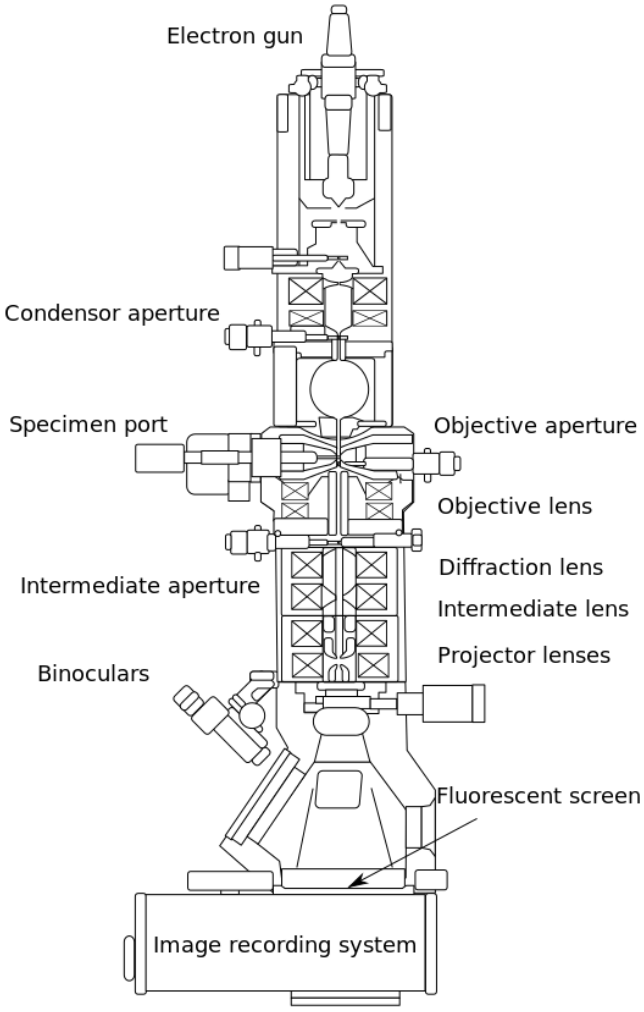

Figure 2.7: Schematic diagram of a conventional transmission electron microscope.

apply TEM imaging to semiconductor samples, electron transparent foils of thin film cross sections are prepared. Foils with thicknesses approximately 100 nm or less are necessary for transmission through the sample of incident, high-energy electrons at the sample surface. Typical accelerating voltages used during TEM imaging vary from 100 KeV up to 1 MeV, depending on the instrument. Fig. 2.7 shows a schematic diagram for a conventional TEM instrument [8]. High-energy electrons are collimated using magnetic condenser lenses and then focused on to the sample surface. Due to the high-energy nature of the electron beam and the extremely thin thickness of the sample, electrons are transmitted through the sample and scatter elastically or in-elastically with host atoms. In crystalline semiconductor samples, this leads to

Bragg diffraction for those electrons that scatter elastically in the sample. The diffracted beam is then brought into focus at the focal plane for the objective lens. In diffraction imaging mode, the first intermediate lens is focused on the back focal plane of the objective lens and the resulting diffraction pattern from the sample is magnified and projected by a combination of the intermediate and projection lenses. The diffraction spot pattern displayed on the phosphorous screen corresponds to different diffraction vectors, g, which are used to index and align the electron beam to a particular diffraction condition and assist in generating the final TEM micrograph. After diffraction alignment, inverted sample image is formed by the objective lens. An aperture located at the back focal plane of the objective lens is used to select a singular diffraction condition for image formation, resulting in either a bright-field image if g = [000] or a dark-field image if a different g vector is selected. Magnification is enhanced by increasing the accelerating voltage of the electron beam. Additional signals can be collected from the electrons that scatter in-elastically through the sample. In such cases, the transfer of energy from the incident electron beam to the host atoms generates X-rays as electrons in the host atoms undergo radiative relaxation. As the energy separation between orbitals is different for different atoms, collection of the X-rays generated through in-elastic electron transmission is used to determine the elemental composition of the sample. This technique is known as energy-dispersive spectroscopy (EDS). Specimen preparation is an important aspect of the TEM analysis. For most electronic materials, a common sequence of preparation techniques includes ultrasonic disk cutting, mechanical polishing, dimpling, and ion-milling. Dimpling is a preparation technique that produces a specimen with a thinned central area and an outer rim of sufficient thickness to permit ease of handling. Ion milling is traditionally the final form of specimen preparation, in which charged argon ions are accelerated to the sample surface by the application of high voltage. The ion impingement upon the specimen surface removes material as a result of momentum transfer.

2.6. Photoluminescence Spectroscopy: Study of Optical Properties

Photoluminescence (PL) spectroscopy is a valuable non-destructive, contactless measurement technique used for probing semiconductors, and investigating their optoelectronic properties. In performing such measurements, a laser with above-bandgap photon energy is used for photo-excitation of electron-hole pairs in the sample. The radiative recombination of the optically-pumped excess carrier population results in emission characteristics that are directly correlated with the electronic transitions in the sample. In addition to being used for determining the bandgap of electronic materials, PL spectra can yield a vast array of material information, such as: (i) surface, interface, and impurity levels; (ii) defect levels; (iii) material quality, given, as material quality decreases, the probability of non-radiative recombination increases; (iv) doping concentrations; (v) free- and bound-exciton recombination and binding energies; and (vi), strain or relaxation in thin-film strained-layer epitaxy [9].

Fig 2.8 shows a conventional micro-photoluminescence (μ-PL) measurement system, including a laser excitation source, filters to remove unwanted wavelengths, choppers to modulate the excitation beam for lock-in detection, a cryostat for cryogenic (liquid N_2 or He_4)

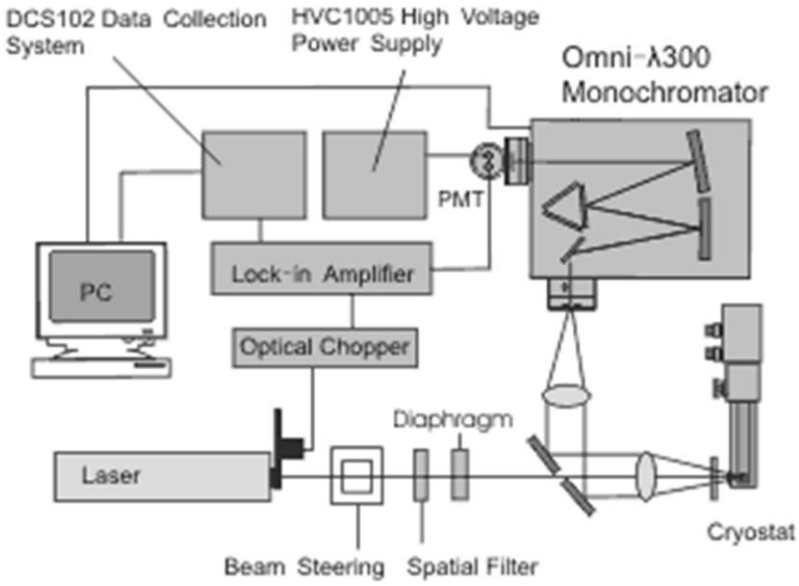

Figure 2.8: Low temperature micro-photoluminescence spectrometer setup

sample measurement, a single or double grating monochromator, and detector (typical cooled to improve the signal-to-noise ratio) [10]. In such a setup, the spectral (energy) resolution is limited by the focal length of the monochromator and the detection range is determined by the monochromator grating. For the μ-PL measurements performed in this thesis, a 700 nm Ti:Sapphire laser source and a thermoelectric cooled InGaAs detector were used for optical pumping and detection, respectively.

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Chapter 3

Experimental Methodology: Electrical characterization techniques

3.1. Performance analysis of Solar Cells

3.1.1. Current-Voltage (I-V) Measurement

The performance of individual solar cells is commonly characterized in terms of the open circuit voltage (V_{oc}), the short circuit current (I_{sc}), and the fill factor (FF). The most fundamental technique of solar cell characterization and performance evaluation is the measurement of cell efficiency. Light I-V measurement provides a direct tool for evaluating the sunlight to power conversion efficiency of a solar cell. Furthermore, the impact of parasitic series resistance (R_s) and shunt resistance (R_{sh}) can also be gauged by light I-V measurement analysis. On the other hand, dark I-V measurements provide insight into the series and shunt resistance of the device and could help identify process induced shunt mechanisms (such as metal deposition providing a shunt path due to incorrect alignment across the mesa edge, defects and dislocations in the epitaxial layers etc.). To gain better understanding of a solar cell's operation, one can extract diode parameters such as the reverse saturation current (I_o), which is strongly dependent on the temperature; and ideality factor (n), which provides insight about various radiative and non-radiative recombination mechanisms, from the light or dark I-

V characteristics. The ideality factor (n) describes how closely the diode's behavior matches that predicted by theory, which assumes the p-n junction as an infinite plane with no recombination processes occurring within the space-charge region. The reverse saturation current (I_0) is a measure of leakage of carriers across the p-n junction in reverse bias. This leakage is a result of carrier recombination in the neutral regions on either side of the junction. Using a single diode model, the current-voltage relationship under illumination is given by the analytical expression [1]:

$$I = I_L - I_0 \left\{ \exp\left[\frac{q(V+IR_s)}{nkT}\right] - 1 \right\} - \frac{V+IR_s}{R_{sh}} \qquad (3.1)$$

where I_L is the light generated current, n is the ideality factor of the junction, and k is the Boltzmann constant with kT/q having the value of 0.02586 V at 300 K. For a cell in which the shunt resistance, R_{sh}, is large and does not have to be taken into consideration, it is possible to derive an expression describing the correlation between remaining parameters. Defining the characteristic resistance, R_{ch}, of a cell as the ratio V_{oc}/I_{sc}, and the thermal voltage, V_{th}, as nkT/q, allows the definition of normalized resistances and voltages. A normalized series resistance, r_s, is defined as R_s/R_{ch} and a normalized open circuit voltage, v_{oc}, as V_{oc}/V_{th}. For the case where both R_s, and R_{sh} both have negligible effect upon cell performance, a simple but very accurate expression for the fill factor is derived as [2]:

$$FF_0 = \frac{v_{oc} - \ln(v_{oc}+0.72)}{1+ v_{oc}} \qquad (3.2)$$

accurate for $v_{oc} > 10$. For cases where R_{sh} is large enough to be neglected but R_s plays a significant role, the fill factor must be corrected to [2]:

$$FF_s = FF_0(1 - 1.1r_s) + \frac{r_s^2}{5.4} \qquad (3.3)$$

where r_s is the normalized series resistance, and valid for $r_s < 0.4$, and FF_0 described in Eqn. 3.2. Parasitic shunt resistance also reduces the fill factor. For the case where both series and shunt resistances are important, the fill factor is given by [2]:

$$FF = FF_s\left(1 - \frac{v_{oc}+0.7}{v_{oc}}\frac{FF_s}{r_{sh}}\right) \quad (3.4)$$

where r_{sh} is the normalized shunt resistance (R_{sh}/R_{ch}), and FF_s is described by Eqn. 3.3. This expression gives good accuracy provided that (r_s + 1/r_{sh}) < 0.4. The accuracy is improved if one (or both) of r_s and 1/r_{sh} is small.

Illumination of Air mass 1.5 spectrum (AM1.5) is used for terrestrial cells and Air mass 0 (AM0) is used for characterizing space cells. Four point probe is commonly used in I-V measurement to remove the effect of probe/cell contact resistance. The cell efficiency is given by [1]:

$$\eta = \frac{I_{sc}V_{oc}FF}{P_{in}}\ (\%) \quad (3.5)$$

where I_{sc} is the short circuit current, V_{oc} is the open circuit voltage, P_{in} is the incident power and FF is the fill factor defined as [1],

$$FF = \frac{P_{max}}{V_{oc}I_{sc}} \quad (3.6)$$

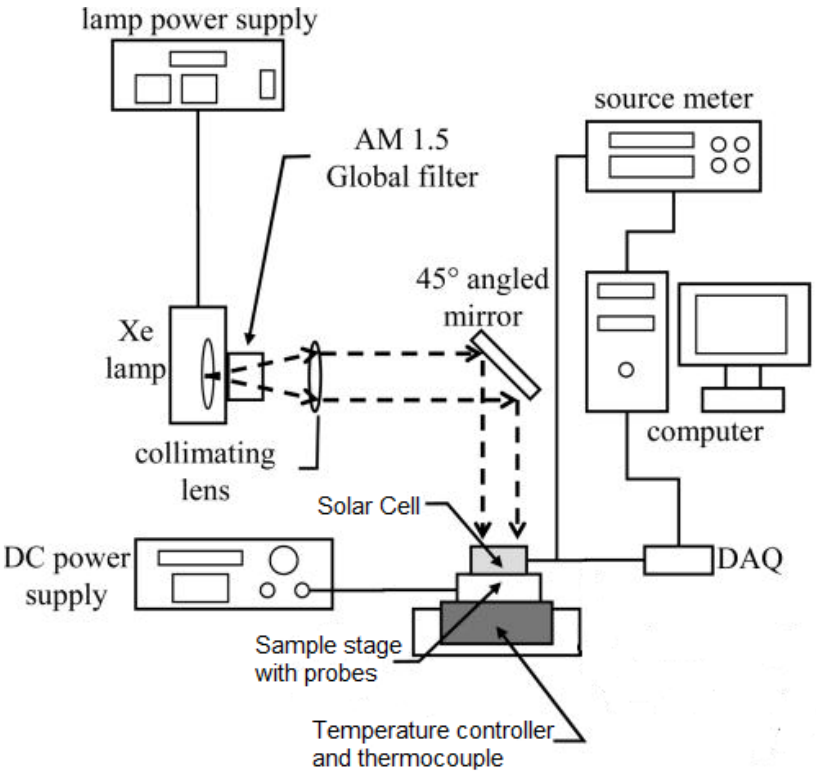

Figure 3.1: Typical I-V measurement setup for Solar cells under AM 1.5 G illumination

where P_{max} is the maximum output power of the solar cell.

Fig. 3.1 shows a typical setup for I-V measurement of solar cells. Measurement systems require prior calibration with standard cells for a given illumination spectrum.

3.1.2 Quantum Efficiency (QE) and Reflectance Measurement

Quantum Efficiency (QE) is defined as the ratio of number of carriers collected by the solar cell to the number of photons of a given energy incident on the solar cell. QE may be measured either as a function of wavelength or as energy. If all photons of a certain wavelength are absorbed and the resulting minority carriers are collected (converted), then the quantum efficiency at that particular wavelength is unity (100%). QE for photons with energy below the band gap is zero. QE analysis provides key insight into the cell design. Especially, for multijunction solar cells, short-circuit current density (J_{sc}) could be extracted from individual subcells using QE measurements and aid in current-matching. Fig. 3.2 describes a typical QE measurement setup. The QE system has specific filters and light biasing capability to do QE measurements on individual subcells in a multijunction cell. The external quantum efficiency

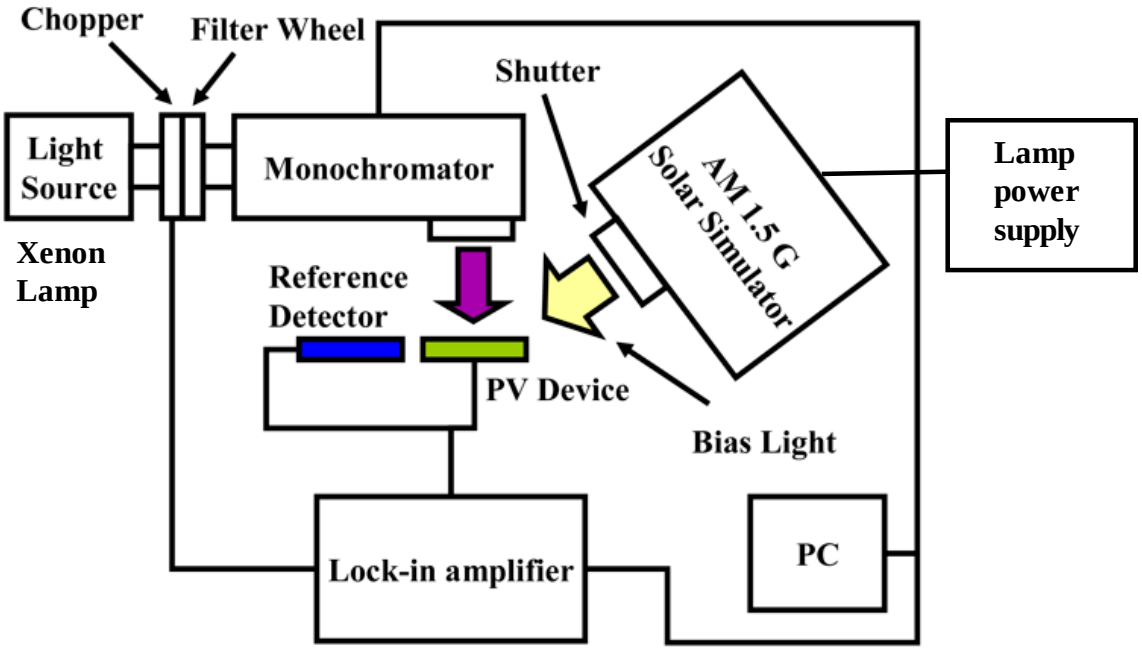

Figure 3.2: Quantum Efficiency and Reflectance Measurement Setup for AM 1.5 G Spectrum.

(EQE) of a solar cell includes the effect of optical losses such as transmission and reflection, whereas internal quantum efficiency (IQE) refers to the efficiency with which photons that are not reflected or transmitted out of the cell can generate collectable carriers. By measuring the reflection and transmission of a device, the EQE curve can be corrected to obtain the IQE curve, given by [1]:

$$IQE = \frac{EQE}{1-Reflectance}. \quad (3.7)$$

3.2. Carrier Transport investigation techniques

3.2.1. Hall Effect Measurement

Hall effect measurements are invaluable for characterizing both low- resistance and high-resistance semiconductor materials, and determining various material parameters, including: carrier mobility, carrier concentration (n), Hall coefficient (R_H), resistivity, magnetoresistance (R_B), and carrier conductivity type (N or P). The Hall effect can be observed when the combination of a magnetic field through a sample and a current along the length of the sample create an electrical current perpendicular to both the magnetic field and the current, which in turn creates a transverse voltage perpendicular to both the field and the current. The underlying principle is the Lorentz force: the force on a point charge moving with velocity v due to electromagnetic fields (electric field ε and magnetic field B), given by:

$$\vec{F}_{Lorentz} = q\left(\vec{\varepsilon} + \vec{v} \times \vec{B}\right). \quad (3.8)$$

The first step in determining carrier mobility is to measure the Hall voltage (V_H) and corresponding Hall coefficient ($R_H(B)$) by forcing both a magnetic field perpendicular to the sample (B) and a current through the sample (I). This combination creates a transverse current. The resulting potential (V_H) is measured across the device. Accurate measurements of both the sample thickness (t) and its resistivity ($\rho(B)$) are also required. The resistivity is determined using either a four-point probe or the van der Pauw measurement technique. With these known

parameters, the Hall mobility of electrons (μ_n) and their carrier concentration (n) can be calculated by [3]:

$$\mu_n = \frac{1}{nq\rho(B)} = \frac{|V_H t|}{BI\rho(B)} \tag{3.9}$$

and

$$n = \frac{r_H}{qR_H(B)} = \frac{IB}{q|V_H|} \tag{3.10}$$

where q is the electronic charge, B is the applied magnetic field, and r_H is the Hall factor. Hall voltages and van der Pauw voltages can be as low as a few millivolts, so the recommended test technique involves a combination of reversing source current polarity, sourcing on additional terminals, and reversing the direction of the magnetic field. Fig 3.3 describes a typical Hall Effect measurement setup comprising of a bipolar constant-current source, high input impedance voltmeter, permanent magnet or electromagnet, and temperature controlled sample holder.

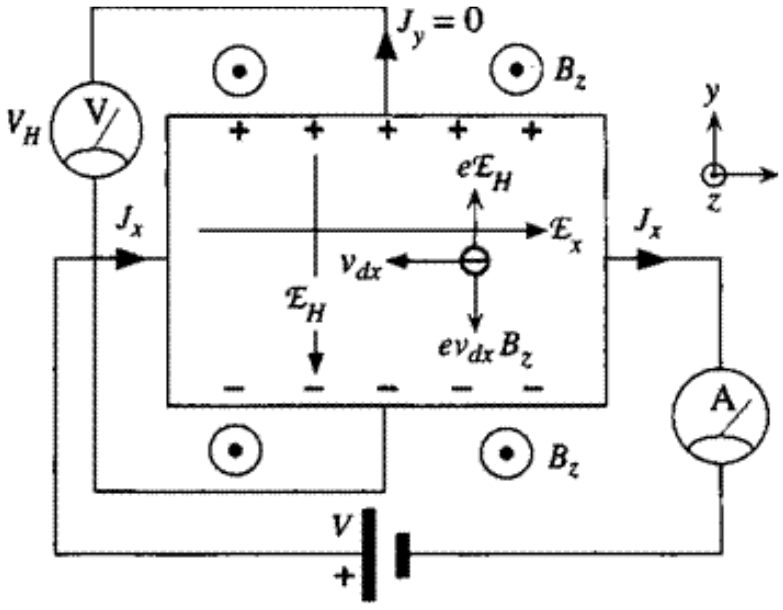

Figure 3.3: Basic experimental setup for Hall measurement for carrier mobility and free carrier concentration determination

3.2.2. Scattering Mechanisms and Carrier Mobility

In this thesis, theoretical approach of transport phenomena in semiconductors is considered using the Boltzmann transport equation. The transport equation expresses the dependence of the distribution of charge carriers ($f(k,r,t)$) under weak external forces as the net effect of two competing processes; the change in f due to transport phenomena under the action of the external force, and the change in f due to random collisions between carriers, quantified as [4]:

$$\frac{df}{dt} = \left(\frac{\partial f}{\partial t}\right)_t + \left(\frac{\partial f}{\partial t}\right)_c. \tag{3.11}$$

In steady state transport phenomena, we may assume $\frac{df}{dt} = 0$, thus the above equation concurrently becomes:

$$\left(\frac{\partial f}{\partial t}\right)_t + \left(\frac{\partial f}{\partial t}\right)_c = 0. \tag{3.12}$$

The relaxation time approximation assumes that all collision processes involved are elastic and can be expressed in terms of a unique relaxation time. Elastic scattering requires that the change of carrier (electron or hole) energy during the scattering process must be small compared to the energy of carriers (electron or hole, respectively), and the relaxation time is a scalar quantity. Typical examples of elastic scattering processes include the scattering of electrons or holes by longitudinal acoustical phonons, ionized impurities, and neutral impurities in a semiconductor. It must be noted that the relaxation time τ may be a function of temperature and energy, depending on the type of scattering mechanisms involved, as will be discussed later. The relaxation time approximation enables the linearization of the Boltzmann transport equation such that the collision term ($(\frac{\partial f}{\partial t})_c$) is expressed in terms of the ratio of the perturbed distribution function ($f - f_0$) and the relaxation time (τ). This approximation allows one to obtain analytical expressions for different transport coefficients in semiconductors. The collision term in the Boltzmann transport equation represents internal relaxation mechanisms

related to the collision of charged carriers with different scattering sources in a semiconductor under the influence of external forces. Under elastic scattering conditions, the non-equilibrium distribution function (f) decays exponentially with time to its equilibrium value (f_0) after removal of external force, the time constant of which is essentially the relaxation time or collision time. These scattering mechanisms are responsible for the charged carriers to reach steady-state condition when external forces are applied to the semiconductor, and to return to the equilibrium condition when external forces are removed. Hence, the transport properties of a semiconductor depend strongly on the various scattering mechanisms.

The electrical conductivity of an *n*-type semiconductor is expressed in terms of electron mobility (μ_n) and electron concentration (n_0) and electronic charge (q) as:

$$\sigma_n = n_0 q \mu_n. \tag{3.13}$$

Assuming the validity of Matthiessen's rule, the total electron mobility (μ_n) is given by [3]:

$$\mu_n^{-1} = \sum_i \mu_i^{-1} \tag{3.14}$$

where μ_i is the electron mobility due to the i-th scattering mechanism. Now, electron mobility (μ_i) in Eq. 3.9 for each individual scattering process can be defined in terms of the conductivity effective mass (m^*) and the relaxation time (τ) as follows [4]:

$$\mu_i = \frac{q<\tau_m>^i}{m^*}. \tag{3.15}$$

where $<\tau_m>^i$ is the average momentum relaxation time for the i-th scattering mechanism, which is given by [4]:

$$< \tau_m >^i = \frac{4}{3\sqrt{\pi}} \int_0^\infty \tau_m^i (z) z^{2/3} \exp(-z)\, dz\,, \tag{3.16}$$

where z is the electron energy in k_BT.

In this thesis, the dominant scattering mechanisms assumed to govern carrier transport in Ge thin-films are: (i) acoustical phonon scattering; (ii) optical phonon scattering; (iii) ionized

impurity scattering; (iv) neutral impurity scattering; and (v) dislocation scattering, the treatment of each is discussed in *Chapter 6*.

3.3. Interface Characterization Techniques

The study of semiconductor surfaces is critical since most practical problems concerning the reliability and stability of semiconductor devices boils down to the semiconductor's surface conditions, especially in regard to the oxide/semiconductor heterointerface. Capacitance-voltage (C-V) and conductance-voltage (G-V) measurements on metal-oxide-semiconductor capacitors (MOS-C), are useful in the quantification of MOS interface quality by the extraction of standard metrics including flatband voltage, doping level, fixed charge density, effective oxide thickness, metal work function, and interface trap density. The interface trap density (D_{it}) is a key metric to quantitatively measure the quality of the oxide/semiconductor heterointerface.

3.3.1. Ideal Capacitance-Voltage Characteristics

Understanding ideal MOS-C theory is important to exploring semiconductor surface physics and critical before discussing metric extraction. An ideal MOS-C is defined where: (i) there are no interface traps nor trapped oxide charges and therefore, the only free charge carriers are those that are intrinsic to the semiconductor and those that exist in the metal, of opposite polarity to the semiconductor's charges; (ii) the dielectric oxide is a perfect insulator with infinite resistivity; (iii) the difference between the metal's work function ϕ_M and the semiconductor's work function ϕ_S is 0. In understanding MOS-C behavior, we will consider a *p*-type bulk semiconductor throughout this chapter. Three modes exist for an ideal MOS-C under bias conditions: accumulation, depletion, and inversion. The energy-band diagrams for a *p*-type semiconductor MOS-C for the accumulation, depletion, and inversion modes are shown below in Fig. 3.4(a), 3.4(b), and 3.4(c), respectively. The corresponding device

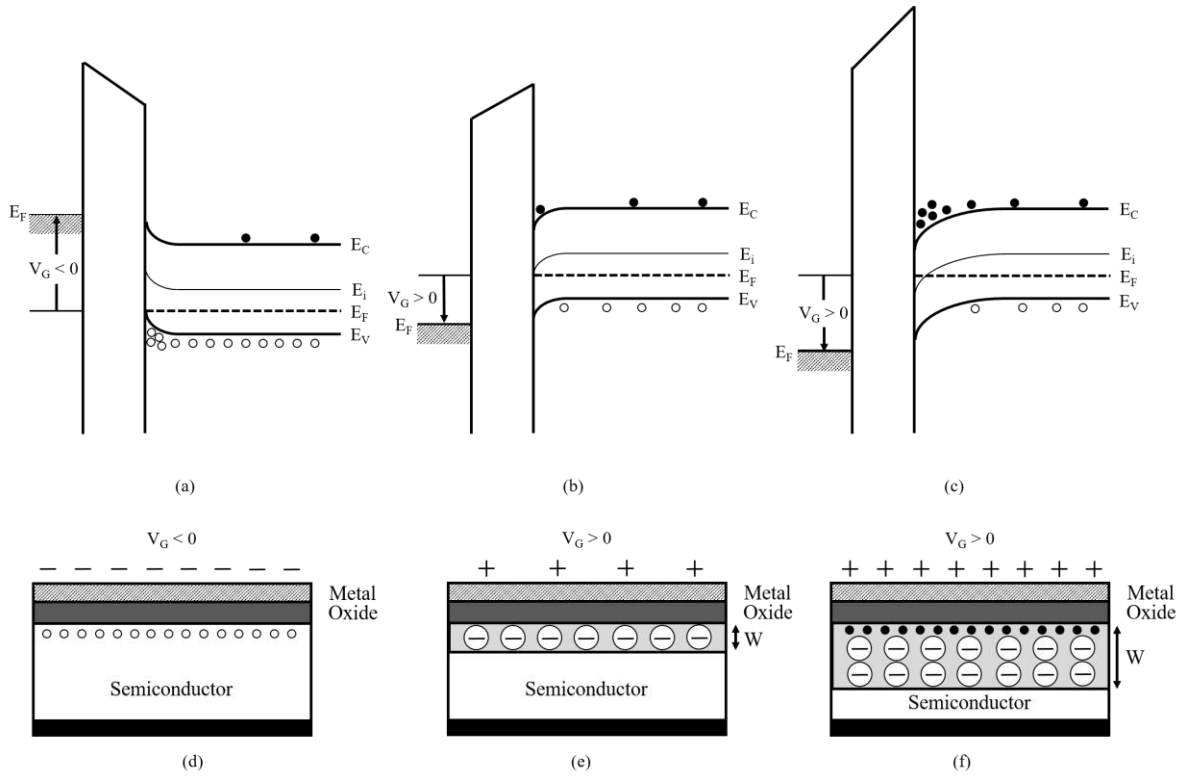

Figure 3.4: Energy-band diagrams of ideal p-semiconductor MOS-C for the modes of **(a)** accumulation, **(b)** depletion, and **(c)** inversion. Schematics for same MOS-C for the modes are shown as **(d)** accumulation, **(e)** depletion, and **(f)** inversion.

schematic for each mode are also shown in Fig. 3.4(d), 3.4(e), and 3.4(f), respectively. For the *n*-MOS-C under the accumulation mode, a negative bias ($V_G < 0$) is applied to the gate. The valence band edge (E_V) bends up toward the Fermi energy level (E_F), as shown in Fig. 3.4(a). This upward bending results in an accumulation of majority carriers (holes) at the semiconductor surface, as clearly reflected in Fig. 3.4(d). When a positive bias is applied ($V_G > 0$) to the gate, the bands begin to bend downward and majority carriers (holes) are depleted, as shown in Fig. 3.4(b). As seen in Fig. 3.4(e), a depletion layer forms (the lighter grey layer underneath the oxide layer denoted with W), the semiconductor surface begins to look more negative as ionized acceptor ions begin to appear. The MOS-C thus enters depletion mode. When larger positive gate bias is applied, the bands bend even more downward and the intrinsic Fermi level (E_i) now crosses E_F, as shown in Fig 3.4(c). Minority carriers (electrons) appear at

the semiconductor surface, resulting in an inverted surface and thus, the MOS-C enters inversion mode. In inversion mode, as shown in Fig. 3.4(f), the depletion layer from Fig. 3.4(e) becomes larger as more ionized acceptor ions and electrons begin to appear, resulting in a highly negative semiconductor surface.

Capacitance-voltage characteristics demonstrate the effect of a direct-current (DC) bias voltage sweep with an alternating-current (AC) voltage of various frequencies on the capacitance of the semiconductor surface. In an ideal *p*-type semiconductor MOS-C, as mentioned in the previous section, negative gate bias results in an accumulation of holes at the semiconductor surface. This large accumulation of holes results in a very large capacitance in series with the oxide capacitance, C_{ox}, which results in a net capacitance of simply C_{ox}, as shown in the C-V curve of an ideal *n*-MOS-C in Fig. 3.5. The capacitance remains independent of further applied gate voltage until the gate bias on the MOS-C approaches $V_G = 0$, which in an ideal MOS-C is assumed to be the flatband condition, where the surface potential, $\psi_s = 0$, as pointed out in Fig. 3.5. In this flatband condition, there is a distinct capacitance called the flatband capacitance, C_{FB}, which can be described as [5]:

$$C_{FB} = \frac{\varepsilon_s \varepsilon_{ox}}{\varepsilon_s t_{ox} + \varepsilon_{ox}\sqrt{k_B T \varepsilon_s / N_A q^2}} \tag{3.17}$$

where ε_{ox} and ε_s are the permittivity of the oxide and the semiconductor, respectively, k_B is the Boltzmann constant, T is the temperature, N_A is the acceptor concentration, q is the electronic charge, and t_{ox} is the oxide thickness. From flatband condition to the bias condition where $\psi_s = \psi_{Bp}$, which is defined to be the Fermi potential with respect to midgap, in depletion mode. In this regime, the depletion capacitance C_D comes into play and is defined as [4]:

$$C_D = \frac{\varepsilon}{W} \tag{3.18}$$

where W is the width of the depletion layer, given by [4]:

$$W = \sqrt{\frac{\varepsilon_s^2}{C_{ox}^2} + \frac{2\varepsilon_s V}{qN_D}} - \frac{\varepsilon_s}{C_{ox}} \tag{3.19}$$

where N_D is the intrinsic donor concentration and V is the applied voltage. From Eq. 3.19, W is directly proportional to applied bias V, thus, with increasing gate voltage, the depletion width grows. Depletion capacitance, C_D, inversely proportional to W, becomes smaller in response to increasing gate voltage, and becomes significant in overall series capacitance, causing a drop in overall capacitance. Beyond the bias condition where $\psi_s = \psi_{Bp}$, the MOS-C enters weak inversion and the MOS-C begins to display two different phenomenon, which is affected by the frequency of the supersetted AC voltage. ψ_{Bp} is defined below [5]:

$$\psi_{Bp} = \frac{k_B T}{q} \ln\left(\frac{N_A}{n_i}\right). \tag{3.20}$$

The first phenomenon explains MOS-C behavior when an AC voltage bias of low frequency is applied. At low frequencies, the recombination-generation rates of minority carriers are able to follow the small-signal variation, which enables charge exchange in the inversion layer and minority carriers appear at the semiconductor surface [5]. From the weak inversion to strong inversion regime (defined as $\psi_s = 2\psi_{Bp}$) the semiconductor surface begins to see increasing accumulation of minority carriers. In addition, at $\psi_s = 2\psi_{Bp}$, the semiconductor enters strong inversion, and gate bias voltage $V_G = V_{TH}$, which is defined as the threshold voltage. V_{TH} is given by [4]:

$$V_{TH} = \frac{\sqrt{2\varepsilon_s q N_A (2\psi_{Bp})}}{C_{ox}} + 2\psi_{Bp}. \tag{3.21}$$

In this inversion regime, the increase in the capacitance associated with minority carriers leads to dominance of C_{ox} in the overall series capacitance, similar to accumulation regime. This is visible in the C-V characteristic, where after the initial dip in overall capacitance, the capacitance begins to increase as more minority carriers populate the semiconductor surface, for low frequency applied bias.

The second phenomenon describes MOS-C behavior when a high frequency AC voltage is applied. In this situation, the thermal recombination-generation rates of the minority carriers

cannot follow the small-signal variation, which results in no accumulation of minority carriers at the semiconductor surface. Instead, the depletion width grows, and associated depletion capacitance becomes smaller with increasing gate voltage until the depletion width reaches maximum (W_{max}) and capacitance reaches minimum at C_{min}, shown by high frequency curve in Fig 3.5. C_{min} is given by [5]:

$$C_{min} = \frac{\varepsilon_{ox}\varepsilon_s}{\varepsilon_s t_{ox} + \varepsilon_{ox} W_{max}} \tag{3.22}$$

where W_{max} can be expressed as [5]:

$$W_{max} \approx \sqrt{\frac{4\varepsilon_s k_B T \ln\left(\frac{N_A}{n_i}\right)}{q^2 N_A}}. \tag{3.23}$$

It must be noted that all equations derived in this section are only relevant for ideal p-semiconductor MOS-Cs. However, simply replacing N_D for N_A and vice versa will yield the parameters of interest for n-semiconductor MOS-Cs.

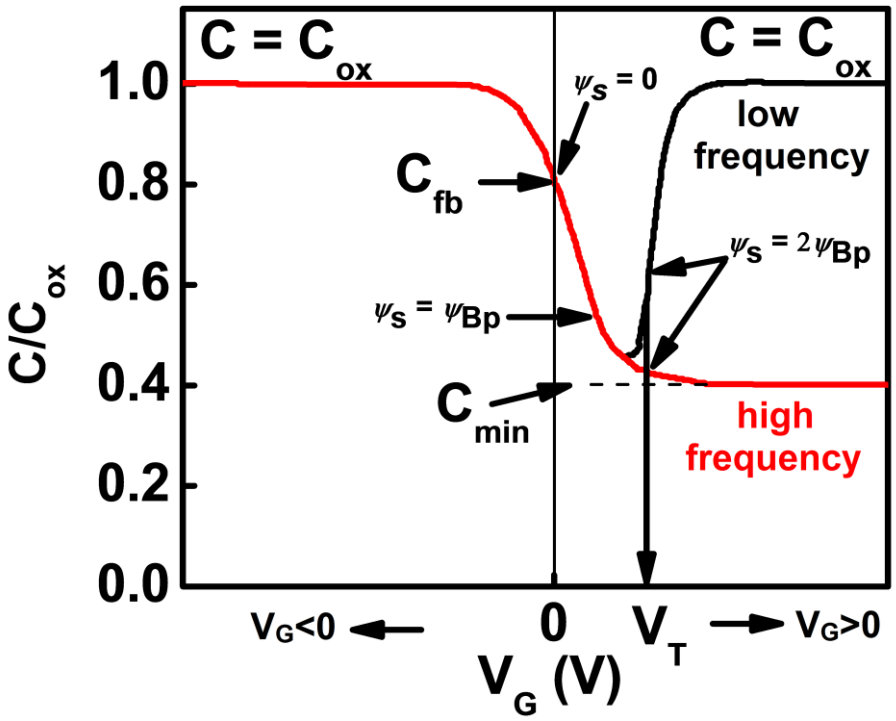

Figure 3.5: Capacitance-voltage curves of ideal *p*-semiconductor MOS-C where the black line represents MOS-C behavior for low frequency AC voltage and the red line represents the MOS-C behavior for high frequency AC voltage.

3.3.2. Non-idealities and their effect on Capacitance-Voltage curves

We have explored ideal MOS-Cs thus far; however, non-idealities are often introduced during the growth of an oxide layer on a terminated single-crystal semiconductor surface for the case of practical MOS-Cs. These non-idealities exist in the form of trap levels and charges, and affect ideal MOS-C characteristics. The four types of traps and charges are:

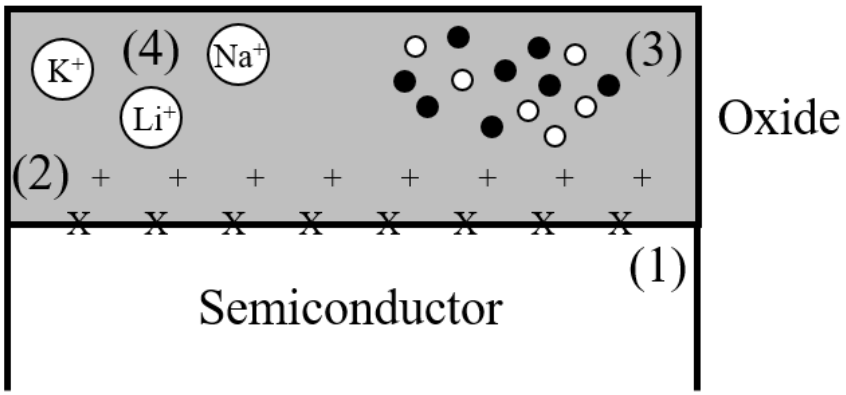

Figure 3.6: Traps, charges and their approximate location within the oxide where the numbers are as mentioned below.

(1) Interface trapped charges (Q_{it}, N_{it}, D_{it}): Positive or negative charges that exist at the oxide/semiconductor heterointerface. They originate from structural defects, oxidation-induced defects, metal impurities, or other defects caused by radiation damage or other bond breaking processes [4,5]. These are states within the semiconductor's forbidden bandgap and are in electrical communication with the underlying semiconductor [5, 6].

(2) Fixed oxide charges (Q_f, N_f): Positive charges near the oxide/semiconductor heterointerface, whose density of charges depends on oxidation ambient and temperature, cooling conditions, and the semiconductor's orientation [6]. Unlike interface trap charges mentioned above, fixed oxide charges are not in electrical communication with the underlying semiconductor [5, 6].

(3) Oxide trapped charges (Q_{ot}, N_{ot}): Positive or negative charges due to carriers (i.e. holes or electrons, respectively) being trapped in the oxide [5,6]. These carriers are trapped by mechanisms such as radiation, avalanche injection, hot-carrier injection, etc [5,6].

(4) Mobile oxide charge (Q_m, N_m): Charges that exist in the oxide due to ionic impurities such as Na^+, Li^+, K^+, and H^+ [6]. They are mobile within the oxide under bias-temperature stress conditions [5].

A schematic of the above-mentioned traps and charges and their approximate location within the oxide is shown in Fig 3.6. We now discuss the associated capacitances for these traps and charges, and how to model them in the different C-V modes. Fig. 3.7 summarizes the different modes of MOS-C operation and capacitances that are in effect at each mode for p-semiconductor MOS-C:

Here, C_p, C_b, C_n, and C_{it} are the capacitances associated with holes, bulk substrate, electrons, and interfacial traps. Essentially, all modes are exactly as described in section 3.2.1 with the exception of the depletion mode. Interfacial traps contribute a capacitance C_{it} that is in parallel with the bulk capacitance, C_b. We can also see that C_{ox} is present in all modes of operation of the MOS-C. The effect of interfacial traps on C-V curves will be discussed in a later section.

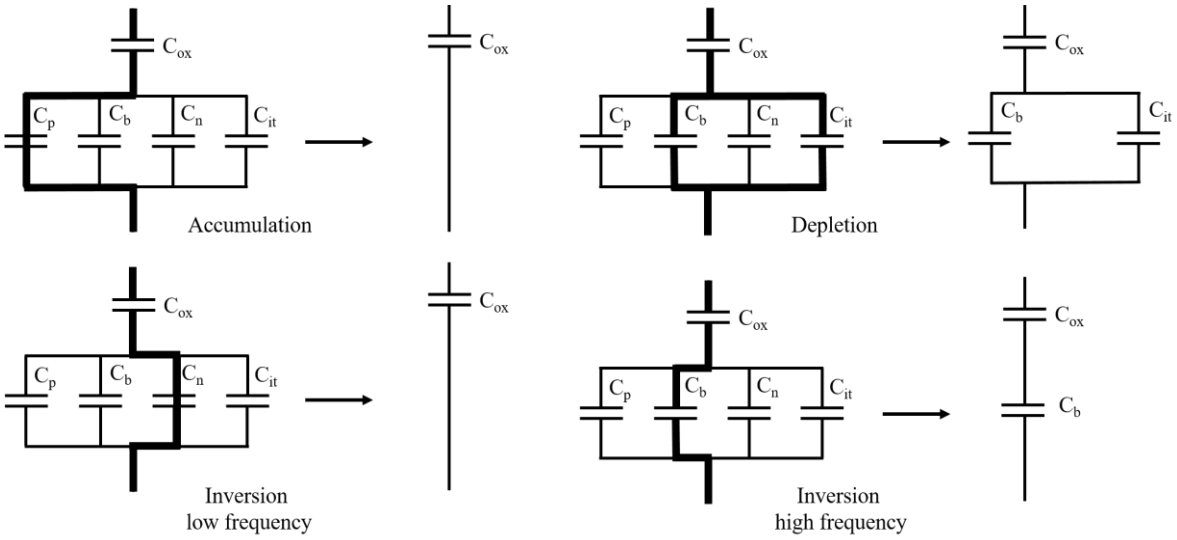

Figure 3.7: Effective capacitances at several modes in p-semiconductor MOS-C Capacitance-Voltage measurements.

3.3.3. Maserjian Extraction Method of Oxide Capacitance C_{ox}

The oxide capacitance, C_{ox} plays an important role in the extraction of various important parameters used to quantitatively, and qualitatively gauge the quality of the oxide/semiconductor heterointerface. The method used in experimentally extracting C_{ox} from measured C-V curves in this thesis is called the Maserjian et al. method [7]. The governing equation is [7]:

$$\frac{1}{C_{hf,acc}} = \frac{1}{C_{ox}} + S\left|\frac{d(\frac{1}{C_{hf,acc}^2})}{dV}\right|^{1/4} \tag{3.24}$$

where $C_{hf,acc}$ is the high frequency accumulation capacitance and S is a constant. Plotting $1/C_{hf,acc}$ versus $(d(1/C_{hf,acc}^2)/dV)^{1/4}$ and then linearly fitting data points yields a straight line with y-intercept on the $1/C_{hf,acc}$ line equivalent to $1/C_{ox}$. Fig. 3.8 shows an example of the Maserjian method extraction of C_{ox}. Experimental data points, shown in blue, are extracted from high-frequency C-V measurements and then fit linearly, in red, which is then extrapolated to obtain the y-intercept. The y-intercept, encircled in black, is equivalent to $1/C_{ox}$.

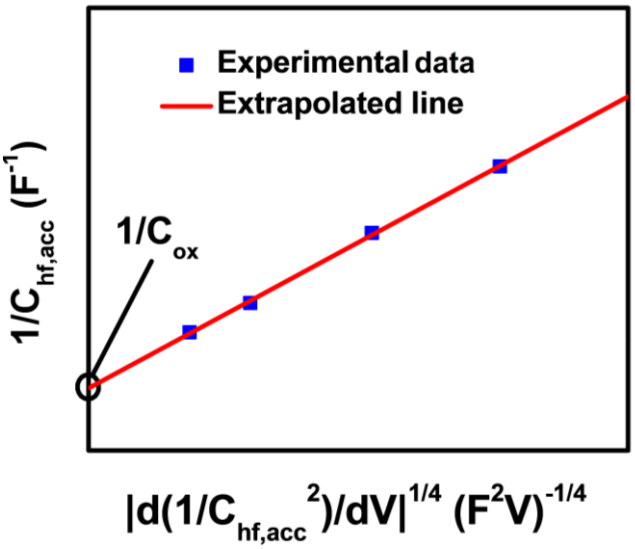

Figure 3.8: Maserjian method for extraction of C_{ox} from high frequency C-V data. The encircled y-intercept gives C_{ox} value.

3.3.4. Extraction of Flatband Voltage V_{FB}

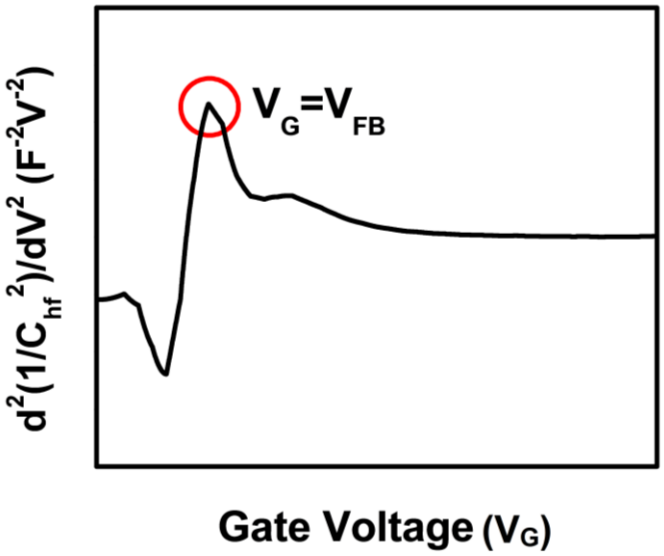

Figure 3.9: Hillard et al. [8] method for extraction of V_{FB} (encircled in red) from high frequency C-V data.

Another parameter of interest that will help extracting information about device non-idealities is the flatband voltage V_{FB}. The method implemented here, as discussed by Hillard et al. [8] requires plotting $d^2(1/C_{hf}^2)/dV^2$ against V_G, where C_{hf} is the high-frequency C-V data, which in this thesis used the 1 MHz C-V curve. The double differential curve has a sharp peak that coincides with $V_G = V_{FB}$. Fig. 3.9 shows an example of the application of this method to determine V_{FB}.

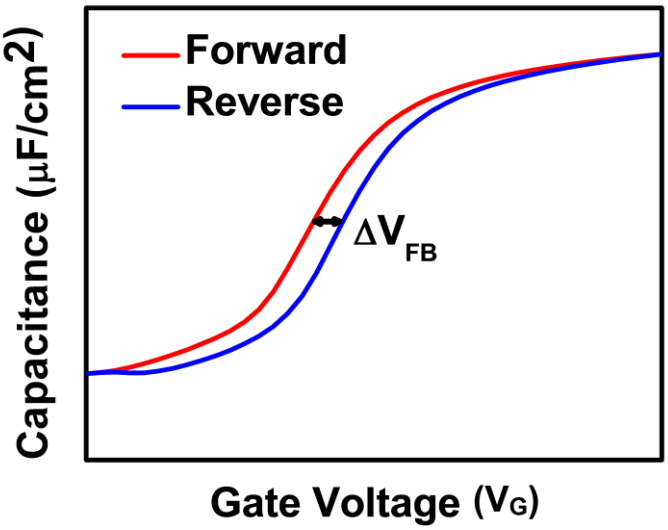

Figure 3.10: Hysteresis (ΔV_{FB}) between forward sweep (red curve) and reverse sweep (blue curve) in a high frequency C-V curve.

3.3.5. Extraction of Oxide Trapped Charge Density N_{ot}

With knowledge of both C_{ox} and V_{FB}, oxide trapped charge density N_{ot} information can be obtained. When performing a high frequency forward and reverse V_G sweep, the C-V curve shows a shift in V_{FB} (ΔV_{FB}) between the two sweeps, known as hysteresis, as demonstrated in Fig 3.10. With knowledge of ΔV_{FB}, N_{ot} can be calculated using [6]:

$$N_{ot} = \frac{\Delta V_{FB} C_{ox}}{q}. \tag{3.25}$$

3.3.6. Extraction of Doping Concentration

The extraction of doping concentration in the bulk semiconductor is based on an iterative approach called the maximum-minimum capacitance technique. In this technique, the doping density N can be derived using the following formula [6]:

$$N = \frac{4\varphi_F}{4\varepsilon_s \varepsilon_0 A^2} \frac{C_{inv}^2}{(1-\frac{C_{inv}}{C_{ox}})^2} \tag{3.26}$$

where C_{inv} is the minimum capacitance measured from the high frequency C-V curve, ε_s is the permittivity of the semiconductor, ε_0 is vacuum permittivity, A is gate electrode area, C_{ox} is the oxide capacitance, and φ_F is the Fermi surface potential, also dependent on N and given by:

$$\varphi_F = \frac{k_B T}{q} \ln(\frac{N}{n_i}) \tag{3.27}$$

where k_B is the Boltzmann constant, T is temperature, q is electronic charge, and n_i is the intrinsic carrier concentration of the semiconductor. Since φ_F depends on N, N can be iteratively found by continuously plugging in different values into Eq. 3.26, which is then plugged into Eq. 3.27. N is thus found by comparing the difference between the N plugged in the first equation (3.26), and the N derived using the second equation (3.27).

3.3.7. Extraction of Interfacial Trap Density D_{it}

Interface traps, located at the oxide-semiconductor heterointerface, are in electrical communication with the underlying semiconductor, hence their influence on C-V curves is

readily noticeable. To that end, interface trap density, D_{it} is a key metric in quantitative evaluation of oxide-semiconductor interface quality, which determines performance in a MOS device. Fig. 3.11 shows the effect of D_{it} on high and low frequency C-V curves measured. For the high frequency case, interface traps cannot follow the AC probe frequency and thus do not contribute to the capacitance. However, they still follow the slow varying DC signal, and as the gate voltage is swept from accumulation to inversion, Q_{it} contributes to the gate charge.

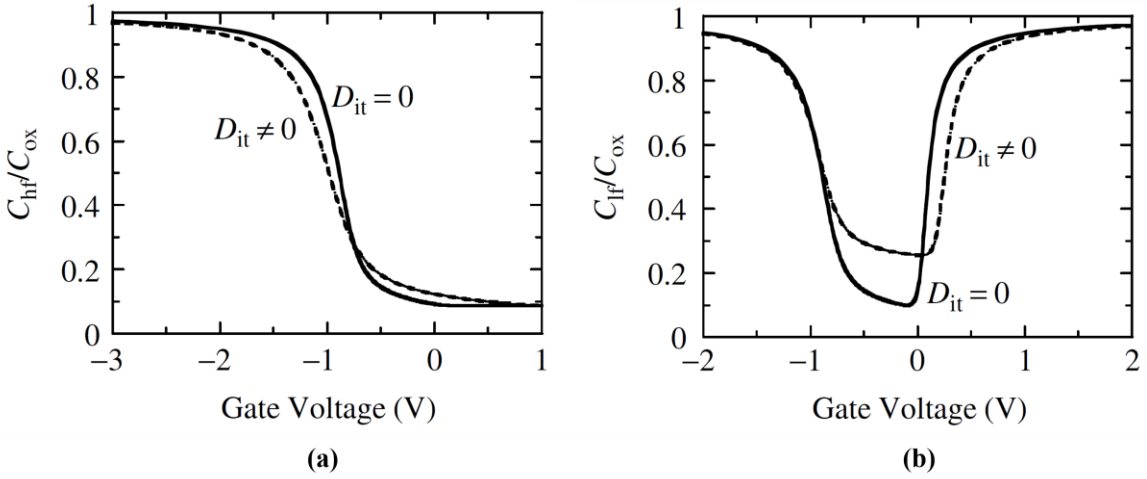

Figure 3.11: Theoretical normalized capacitance with (dashed line) and without (solid line) the contribution of D_{it} for (a) high frequency and (b) low frequency [3].

Thus, the effective gate charge becomes $Q_G = -(Q_s+Q_{it})$, meaning both semiconductor surface and interface traps must be charged [5]. As a result, the high frequency C-V curve stretches out along the gate bias axis. For low frequency AC signals, interface traps respond to both the AC and DC signals, and contribute a capacitance C_{it}, resulting in stretch out along gate voltage, as well as a larger minimum capacitance C_{min}.

Various methods are used to extract D_{it} including the quasi-static method, Terman method, Gray-Brown and Jenq method, charge pumping, conductance method, and several others [14]. The method that will be employed in this thesis for D_{it} extraction is the conductance method, because it is the most sensitive method to measure D_{it} and is also the most comprehensive method, yielding D_{it} in both depletion and weak inversion regimes of the band gap [6,9].

3.3.7.1. Overview of the Conductance Method

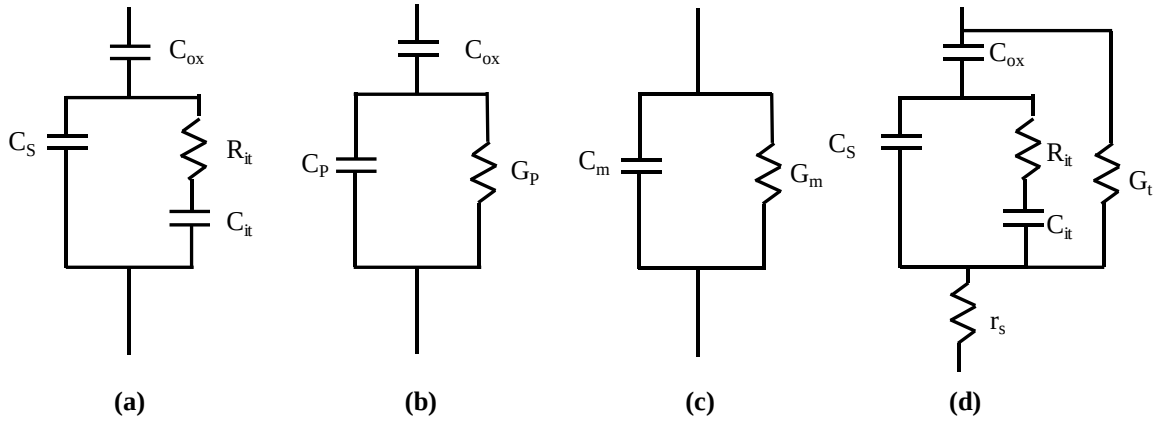

Figure 3.12: Equivalent circuits for the conductance method; **(a)** MOS-C with interface trap time constant $\tau_{it} = R_{it}C_{it}$, **(b)** simplified circuit of **(a)**, **(c)** measured circuit, **(d) (a)** with included series resistance r_s and tunnel conductance G_t.

The equivalent circuit of a MOS-C that is used in the conductance method is shown in Fig. 3.12(a), where C_S is the semiconductor capacitance, C_{ox} is the oxide capacitance, C_{it} is the interface trap capacitance, and R_{it} is the resistance representing the lossy process of carrier capture-emission. The circuit in Fig. 3.10(a) is simplified to the circuit shown in Fig. 3.12(b) to yield C_p and G_p, which are the equivalent parallel capacitance and conductance. C_p and G_p are given by the following equations [6]:

$$C_p = C_s + \frac{C_{it}}{1+(\omega\tau_{it})^2} \tag{3.28}$$

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln[1 + (\omega\tau_{it})^2] \tag{3.29}$$

where $C_{it} = q^2D_{it}$, $\omega = 2\pi f$ (f being measurement frequency) and $\tau_{it} = R_{it}C_{it}$. However, capacitance meters assume the MOS-C to consist of the parallel combination of measured capacitance, C_m, and measured conductance G_m. Therefore, a practical form of G_p/ω will include C_m and G_m and is given by [6]:

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2(C_{ox}-C_m)^2} \tag{3.30}$$

Eq. 3.24 assumes negligible series resistance, r_s. Accounting for r_s and tunnel conductance G_t, we obtain the complete circuit of the MOS-C, shown in Fig. 3.12(d). Including the contribution of r_s and G_t parameters, the derivation of G_p/ω yields [6]:

$$\frac{G_p}{\omega} = \frac{\omega(G_c - G_t)C_{ox}^2}{G_c^2 + \omega^2(C_{ox} - C_c)^2} \tag{3.31}$$

where C_c and G_c are the corrected capacitance and conductance, respectively, when r_s is not negligible, and can be derived using the following equations [7]:

$$C_c = \frac{C_m}{(1 - r_s G_m)^2 + (\omega r_s C_m)^2} \tag{3.32}$$

$$G_c = \frac{\omega^2 r_s C_m C_c - G_m}{r_s G_m - 1} \tag{3.33}$$

G_t can be determined from Eq. 3.24 when $\omega \rightarrow 0$. The derivation of r_s is done using the following equation [6]:

$$r_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \tag{3.34}$$

where G_{ma} and C_{ma} are measured conductance and capacitance, respectively, in accumulation.

3.3.7.2. Accounting for Surface Potential

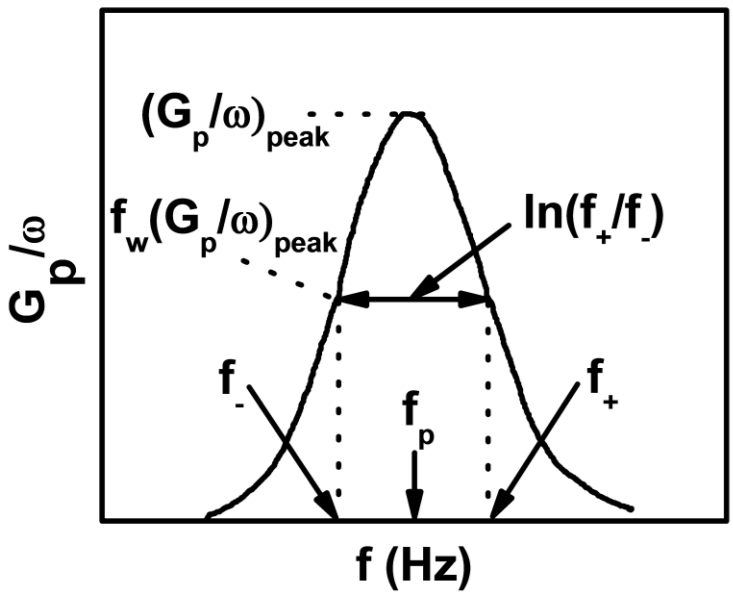

Figure 3.13: Conductance peak analysis for D_{it} extraction while accounting for surface potential fluctuation.

Conductance is measured as a function of frequency ω and plotted as G_p/ω. G_p/ω has a peak (maxima) at $\omega = 1/\tau_{it}$ and at that maximum, $D_{it} \approx 2.5G_p/q\omega$ [6]. In addition to obtaining D_{it}, τ_{it} can also be obtained from the ω at the peak G_p/ω location on the ω-axis. However, experimental G_p/ω curves are typically much broader than theoretical curves as predicted by Eq. 3.29 due to surface potential fluctuations that are a result of non-uniform oxide and interface trap charge distribution as well as doping density [6]. Thus, a more accurate extraction of D_{it} takes into account this peak broadening. Brews showed that with a single MOS conductance curve, some fitting parameters, and very little calculation, it is possible to accurately extract D_{it} while accounting for surface potential fluctuations [10]. Fig. 3.13 shows a G_p/ω curve where, by accounting for the width of the curve, interfacial broadening σ_s is considered in the derivation of D_{it} [10].

To find σ_s, an estimate of the width of the peak of the conductance curve is taken into account with $f_w(G_p/\omega)_{peak}$, or some fraction of $(G_p/\omega)_{peak}$. Here, $(G_p/\omega)_{peak}$ is the max value of the conductance curve and f_w is some arbitrarily chosen fraction. G_p/ω is a function of the parameter $\xi = \omega\tau$, where ω is radian frequency and τ is the capture time for a majority carrier

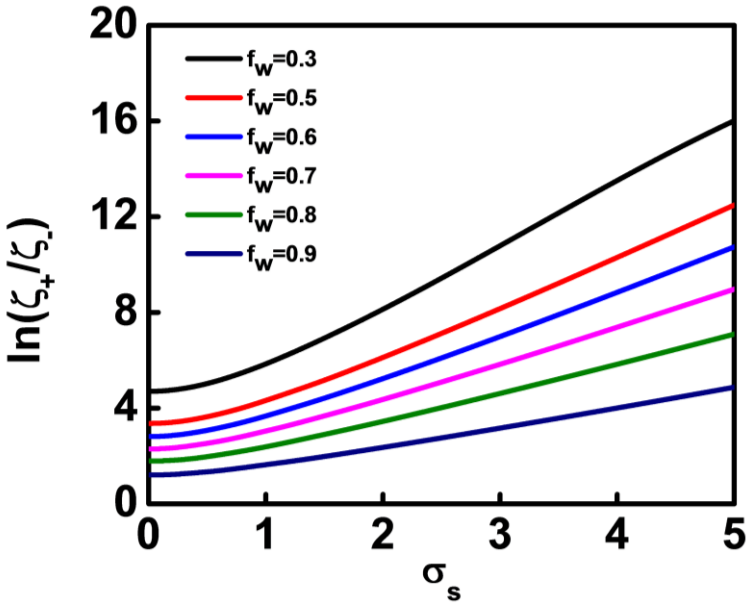

Figure 3.14: Experimental width parameter $ln(\xi_+/\xi_-)$ as a function of interfacial broadening parameter σ_s for various fractions of conductance curve width f_w [10].

by interface traps [9]. Because the influence of surface potential on peak broadening is considered, the width of the curve is an important parameter. Thus, there must be two points for this parameter (i.e. ξ_+ and ξ_-) and the width of the curve is simply $ln(\xi_+/\xi_-)$. To correlate the parameter ξ with a G_p/ω vs. f curve, $ln(\xi_+/\xi_-)$ is equivalent to $ln(f_+/f_-)$, where f_+ and f_- are the upper and lower bound of frequencies that correspond to $f_w(G_p/\omega)_{peak}$. Once $ln(\xi_+/\xi_-)$ is found, it is fit against various f_w values to yield σ_s, as shown by Fig. 3.14.

Once σ_s is determined, the ratio f_d can be determined, which is defined as:

$$f_d = \frac{(\frac{G_p}{\omega})_{peak}}{qAD_{it}} \tag{3.35}$$

where q is electronic charge, and A is device area. Therefore, with all known parameters, D_{it} can be derived as:

$$D_{it} = \frac{(\frac{G_p}{\omega})_{peak}}{qAf_d}. \tag{3.36}$$

The correlation between f_d and σ_s is described in Fig. 3.15.

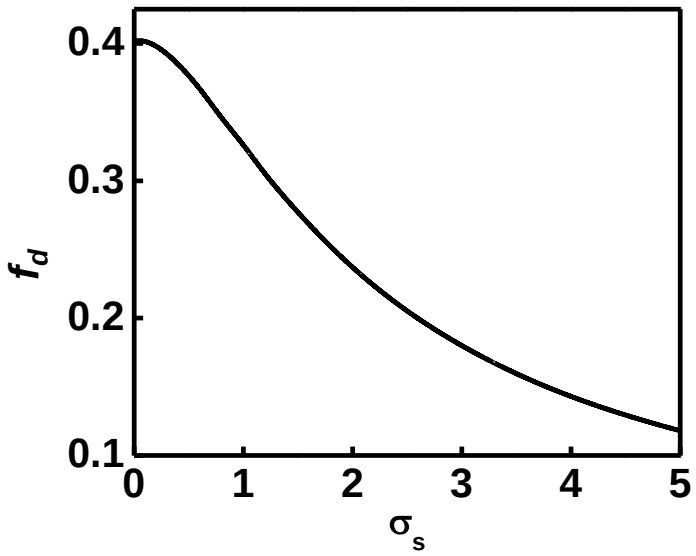

Figure 3.15: Plot of ratio f_d vs. interfacial broadening parameter σ_s. f_d can be used to determine D_{it} [10].

Once D_{it} is extracted, each data point obtained, which is a function of frequency, can be plotted as a distribution across the bandgap using the characteristic trapping time relation [11]:

$$\tau = \frac{1}{2\pi f} = \frac{1}{\sigma v_{th} n_i} \exp(-\frac{E_t - E_i}{k_B T}) \quad (3.37)$$

where τ is the characteristic trapping time, f is the measurement frequency, σ is the trap capture cross section, v_{th} is the carrier thermal velocity, n_i is the semiconductor intrinsic carrier concentration, E_t is the trap energy level, E_i is the midgap energy level, k_B is the Boltzmann's constant, and T is temperature.

3.3.7.3. Conductance Method: Determining Fermi-level Efficiency

Apart from the extraction of D_{it}, another application of the conductance method is its role in Fermi-level efficiency (FLE) method [9]. The FLE method utilizes contours of the conductance (G_P/ω) peaks extracted from the conductance method, and allows for the parametrization of conductance peaks as a function of both gate voltage and frequency. It allows for the tracing of the Fermi-level displacement as a function of gate voltage (V_G), where the ease of change in this Fermi-level position or band bending is a reflection of the trap density levels at the oxide-semiconductor heterointerface [12]. FLE is defined as follows [12]:

$$FLE = \frac{d\phi_s(V_G)}{dV_G} = \ln\left(\frac{f_2}{f_1}\right)\left(\frac{k_B T/q}{V_1 - V_2}\right) \ (\%) \quad (3.38)$$

where $\phi_s(V_G)$ is the semiconductor band bending with respect to gate voltage bias V_G and f_1 and f_2 are frequencies at which G_p/ω conductance peaks occur under voltage bias V_1 and V_2, respectively. The steeper the Fermi level trace, the higher the *FLE* and gate voltage control of the MOS device is better, suggesting good quality heterointerface.

3.3.7.4. Low-temperature Extension of the Conductance Method for Complete D_{it} Mapping

The conductance method is one of the most sensitive and comprehensive techniques to measure D_{it} in MOS-Cs, but when performed at room temperature, the technique becomes limited in its scope for low-bandgap materials such as Ge. Unlike Si, low-bandgap materials have short characteristic time constants for the capture/emission processes of carriers through interface traps. As a result, room temperature C-V and G-V measurements do not reflect the typical interface trap behavior of Ge MOS-Cs due to weak-inversion responses and thermal generation of minority carriers in Ge [13]. As the conductance method was originally developed for Si MOS-C devices and does not take into account minority carrier interaction, application of the conventional conductance method at room temperature can often lead to both under- and overestimation of D_{it} by more than an order of magnitude in low bandgap materials [13]. From Eq. 3.37, it can be seen that trap energy level is dependent on variables such as temperature, σ, v_{th}, and n_i. The last three variables are typically not more than a magnitude in difference from semiconductor to semiconductor, which implies that the trap time constants is relatively similar from semiconductor to semiconductor. For all semiconductors at 300 K, it is impossible to see D_{it} at the band edges. Therefore, in order to obtain a distribution of D_{it} throughout the entire forbidden gap, it is necessary to probe the MOS-C using a wide range of temperatures, including low temperatures down as low as 77 K for select semiconductors such as Ge.

3.4. Deep-Level Transient Spectroscopy: Investigation of Trap Levels in Semiconductor Bulk

Deep Level Transient Spectroscopy (DLTS) is an efficient and powerful method used for sensing and characterizing deep level impurities in semiconductors. DLTS is a capacitance transient thermal scanning technique, operating in the high frequency (MHz) range. It uses the capacitance of a pn junction or Schottky barrier to probe the charge state of a deep centre in

the semiconductor. DLTS technique is highly sensitive, rapid, can cover a broad range of trap levels, and is able to distinguish between majority- and minority-carrier traps [3]. DLTS can also give the trap concentration, energy and capture rates for both kinds of traps. Thus, DLTS allows complete characterization of trap levels in the space charge region of a bulk semiconductor. Fig. 3.16 describes the process of DLTS measurement and energy band diagram of the sample under bias.

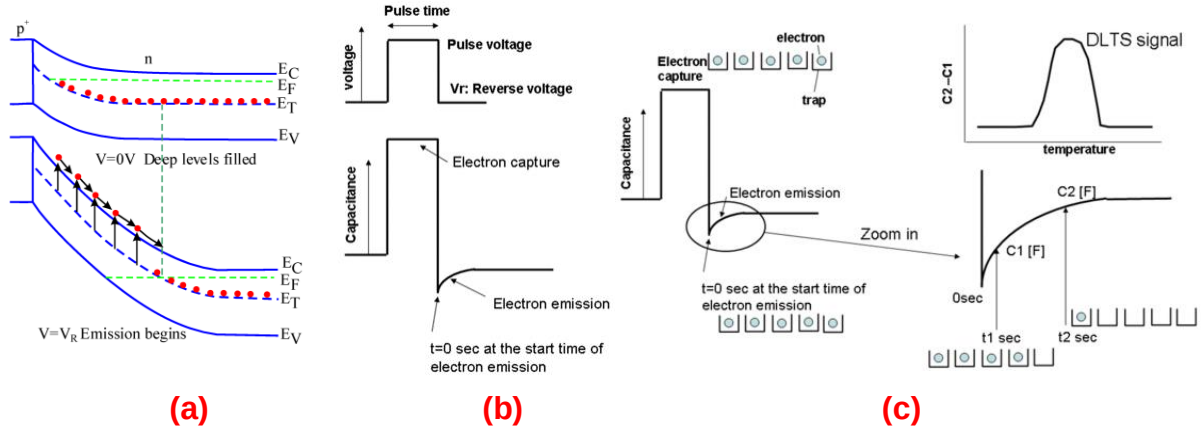

Figure 3.16: **(a)** Energy band diagram of a p^+n junction with an electron trap energy level E_T at zero applied bias (above) and steady reverse bias (below). **(b)** Applied bias pulse in DLTS measurement (above) and obtained capacitance signal (below). **(c)** Procedure to obtain DLTS signal during charge carrier and charge emission processes.

In the space charge region of a Schottky barrier or a pn-junction, traps can be filled or emptied by varying the applied voltage bias. At a high reverse bias voltage, a large number of traps are raised above the Fermi level, and emit their charge by thermal excitation (Fig. 3.16 (a)). When a low reverse bias voltage is applied, most deep trap centers are located below the Fermi level and are rapidly occupied by capture of a charge carrier. The change of the charge state of the trap centers is observed in the capacitance transient [15]. The measured capacitance (Fig. 3.16 (b)) is given by:

$$C(t) = C_0[1 - \frac{N_T}{2N_D}\exp(-\frac{t}{\tau})]\,, \qquad (3.39)$$

where C_0 is the capacitance at reverse bias, N_D is donor concentration, t is time, N_T is the total density of deep states and τ is the time constant given by:

$$\tau = \frac{1}{(e_n + e_p)} \tag{3.40}$$

e_n and e_p being the electron and hole emission rates, respectively, which determine the density of filled traps n_T, in a pn junction with total density of traps N_T, given by:

$$n_T = \frac{e_p}{e_n + e_p} N_T \, . \tag{3.41}$$

Having a set of the emission rate and corresponding measurement temperature, an Arrhenius plot allows for the deduction of trap activation energy for the thermal emission process. The trap emission rate for an electron is given by:

$$e_n = \sigma_n v_{th} N_c \exp\left(-\frac{E_c - E_T}{k_B T}\right) \tag{3.42}$$

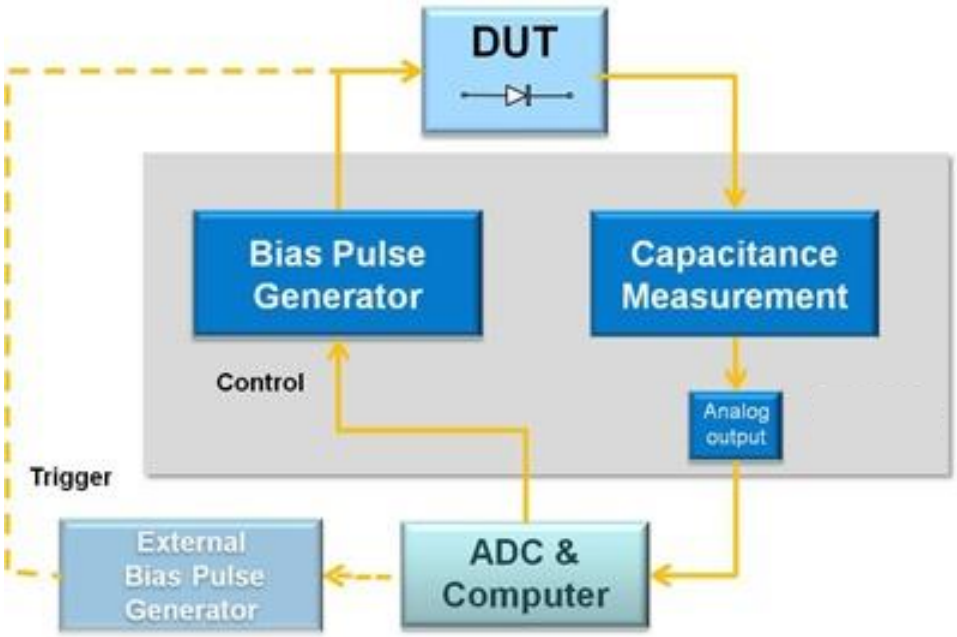

Figure 3.17: Typical DLTS measurement setup

where σ_n, is the electron capture cross-section, v_{th} is the thermal drift velocity of electrons, N_c the effective density of states, E_C-E_T the energy position of the trap center from the conduction band edge, k_B is Boltzmann's constant and T is temperature.

Traps in the upper half of the band gap respond to electrons in the conduction band and traps in the lower half respond to holes in the valence band. In case of pn-junctions, both types of traps can be investigated in the same device due to the presence of both types of carriers simultaneously. On the contrary, in a Schottky barrier structure, only majority carriers are present. Thus, in order to investigate trap centers in the whole band gap, n and p-type material require separate investigation. Fig. 3.17 describes a typical setup for DLTS measurement, including a high frequency capacitance meter, a pulse generator, an ADC block and measurement computer, and a temperature controlled sample stage. Low temperature measurements allow detection of shallow traps in the semiconductor. The DLTS technique is instrumental in determining a majority of properties of defects such as structure, introduction rates, introduction mechanism, thermal stability of the defects, etc.

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Chapter 4

Impact of Buffer Architecture on the Performance of Heterogeneously Integrated III-V-on-Si Solar Cells

In *Chapter 1*, we discussed how the successful monolithic integration of high efficiency III-V cells on low cost, abundant Si substrates would enable the unification of the performance merits of III-V cells with the cost benefits and superior mechanical and thermal properties of Si. In this *Chapter*, we investigate the performance of 1J GaAs cells grown on Si using two different all-epitaxial III-V/IV buffer approaches as an alternative to current III-V cells grown on expensive and smaller diameter Ge or GaAs substrates. The initial approach is the direct epitaxy of GaAs cells on Si using a thick GaAs buffer and understanding the required base thickness to compensate for dislocations propagating into the active region. The second approach is to introduce a thin Ge epilayer between the Si substrate and GaAs buffer, thereby creating a virtual "Ge-*on*-Si" template for subsequent GaAs growth. This approach decouples two challenges, viz. that of lattice mismatched growth and polar on non-polar epitaxy, at separate interfaces. Moreover, the Ge-*on*-Si template can be further extended to develop a hybrid Ge-Si active junction below the GaAs cell, where the Ge layer serves as the emitter in a bottom Si sub-cell. The aim of this work is to elucidate the role of the Ge epilayer and to

enable thinner III-V-on-Si solar cell structures, reducing manufacturing cost while preserving the electrical performances of these devices.

4.1. MBE Growth of Solar Cell Structures

Fig. 4.1 shows the different cell structures studied in this work, of which Sample A and Sample B use a 2 µm GaAs buffer grown directly on Si, whereas Sample C is comprised of a 144 nm Ge intermediate layer with a 750 nm GaAs buffer on top. All structures were grown on Si substrates offcut 4-6° towards the <110> direction, thus creating a double stepped interface for anti-phase domain (APD) free GaAs growth on non-polar Si (or Ge), in a dual chamber MBE system. Migration enhanced epitaxy (MEE) was used to nucleate GaAs in Samples A and C but not in Sample B, where only low temperature GaAs nucleation was performed. In Sample C, a two-step LT/HT growth process enabled two-dimensional growth at low temperatures, forming a template for subsequent smooth, high quality Ge layer growth at high temperature with fewer threading dislocations. Growth temperatures were varied from a minimum of 400°C for GaAs nucleation up to 530°C at the surface. Multiple annealing steps were included in each buffer growth to annihilate dislocations propagating into the active cell region, which adversely affect the cell performance.

The active 1J n-on-p GaAs cell in Sample A has a 2 µm base with $1x10^{17}$ doping concentration at 1 µm/hour growth rate, in comparison to a 1.5 µm base region in Sample B and Sample C with same doping concentration but grown at 0.5 µm/hour. Be and Si were used for the p and n-type dopant sources across all samples. The $Al_xGa_{1-x}As$ composition was modified from $Al_{0.25}Ga_{0.75}As$ in the back surface reflection layer to $Al_{0.71}Ga_{0.29}As$ in the window layer to accommodate a large bandgap window with reduced broad-spectrum absorption. Growth temperature was closely monitored in the back surface reflector (BSR) and window layer to mitigate the effect of difference in Ga and Al ad-atom mobilities. After completion of each

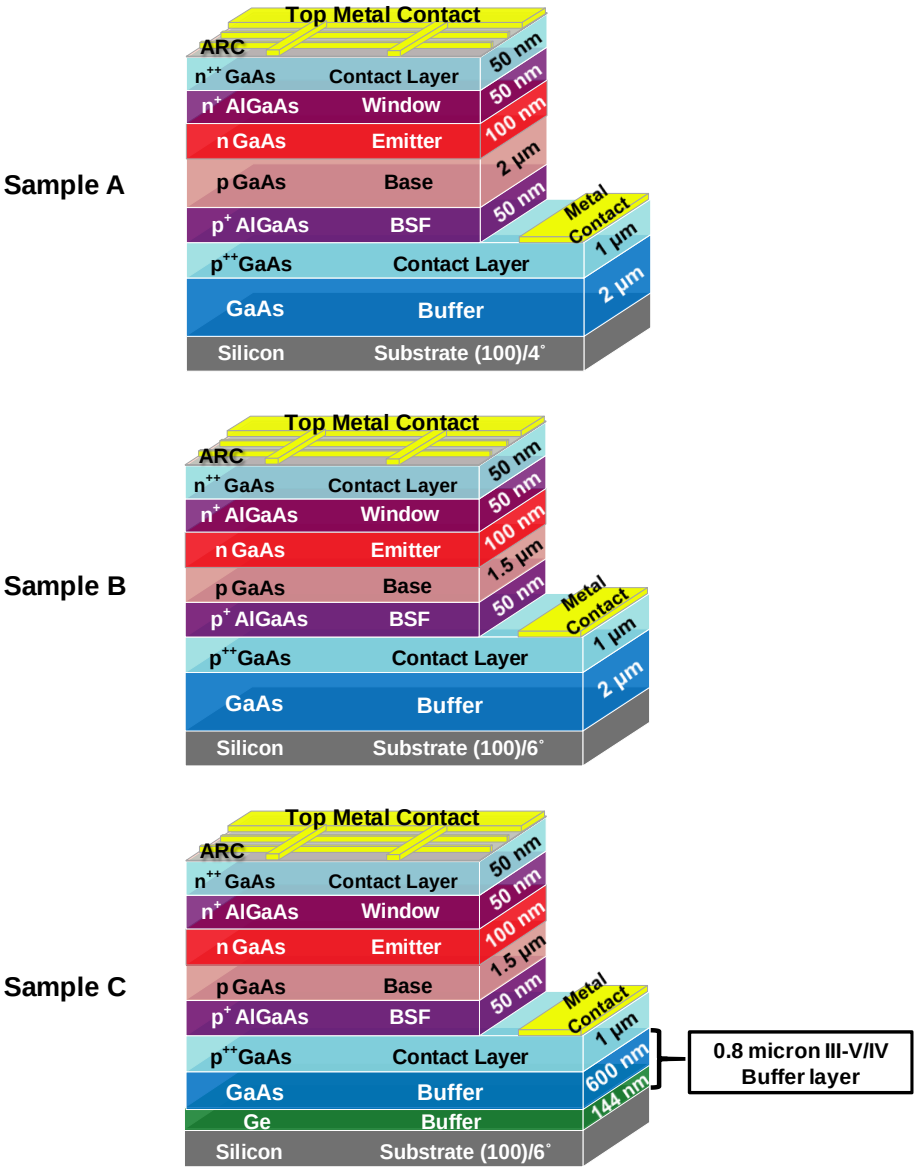

Figure 4.1. Schematic diagrams of the solar cell structures with different buffer architectures.

growth, the samples were gradually cooled down to prevent any thermal cracking prior to unloading for characterization and fabrication. Subsequently, the grown material stacks were characterized for structural defects and surface roughness, described in the following section.

4.2. Material Characterization of Solar Cell Structures

The use of Al in the BSR and window layer increases surface roughness, and hence surface recombination velocity (SRV) of minority carriers in the 1J active cell, due to the low ad-atom

mobility of Al and its subsequent clustering. The use of an offcut substrate further increases susceptibility of the cell surface to roughness. The surface roughness of the top GaAs contact layer of each sample was studied. As shown in the AFM micrographs in Figure 6.2, for a scan size of 20×20 μm^2 the RMS roughness measured was 9.02 nm for Sample A, 17.1 nm for Sample B and 3.17 nm for Sample C. This suggests that, despite the lower thermal budget given to atoms during surface reconstruction in Sample C and a 6˚ offcut substrate, the low temperature Ge nucleation and MEE assisted GaAs nucleation on Ge preserves a significantly smoother surface through the cell growth. On the contrary, Sample B suffers from high surface roughness, which can be contributed to the absence of MEE during GaAs nucleation on offcut Si. Comparing Samples A and C, it was found that the Ge intermediate layer reduces surface roughness, which would result in a lower SRV in the III-V cell. Moreover, the X-ray rocking

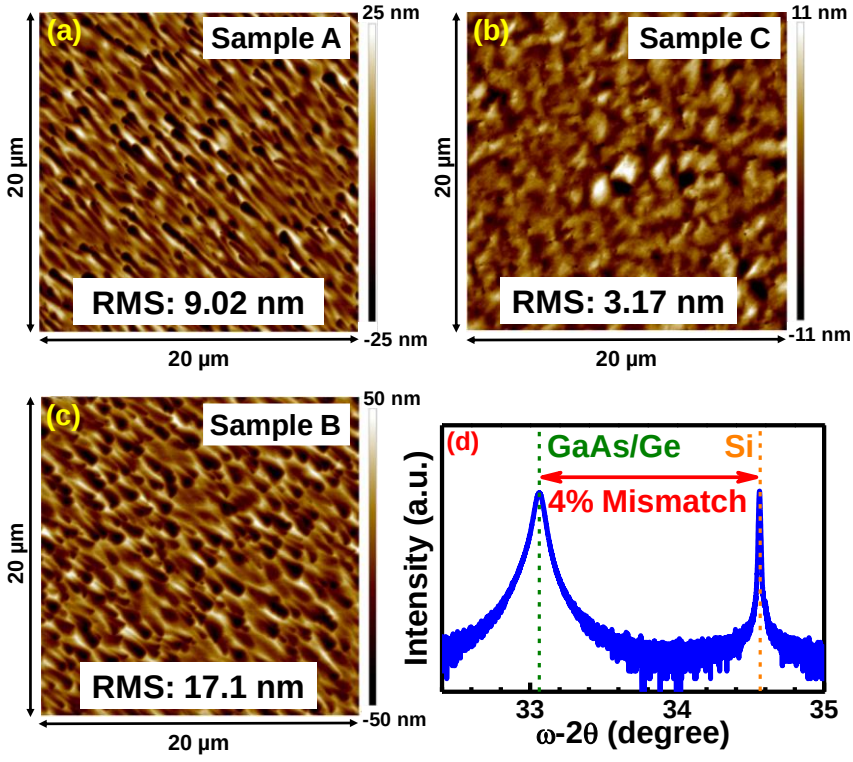

Figure 4.2. (a-c) AFM micrographs indicating surface roughness of GaAs top contact layer for each sample, respectively, and **(d)** (004) X-ray rocking curve of Sample C to show the metamorphic nature of the composite GaAs/Ge buffer.

curve from Sample C, seen in Fig. 4.2 (d), shows a fully relaxed GaAs/Ge peak alongside the Si substrate peak, indicating successful Ge-*on*-Si epitaxy and enabling a virtual Ge template for the subsequent GaAs buffer. Cross-sectional TEM micrographs of Samples A, B and C, shown in Fig. 4.3, revealed APD-free growth, thus indicating that substrate offcut suppressed the initiation of inversion domain boundaries at the III-V/IV interface. The low resolution X-TEM images of the entire device stack show low propagation of misfit induced defects into the active device beyond the GaAs buffer layer. Despite its significantly reduced thickness, the hybrid III-V/IV buffer in Sample C can be seen to effectively minimize threading dislocations from the lattice mismatched Si-Ge heterointerface.

Energy-dispersive X-ray spectroscopy (EDS) elemental mapping helps corroborate the GaAs/Ge buffer quality on Si. Fig. 4.3 (d) shows a three-element overlay of Ge, Si, and As, where the red corresponds to As content, blue corresponds to Ge content, and green corresponds to Si content. Three distinct, uniform color regions corresponding to GaAs (red),

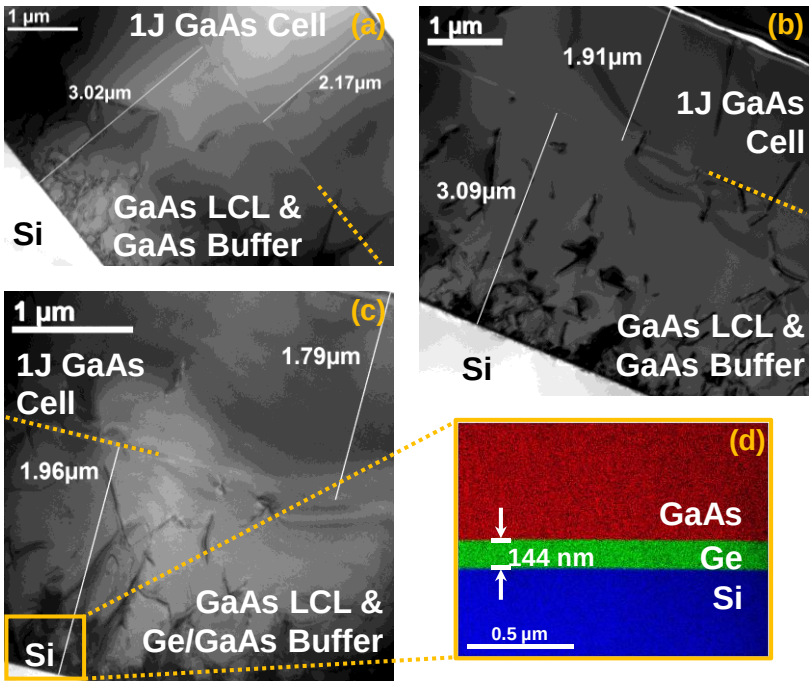

Figure 4.3. **(a-c)** Low magnification TEM micrographs of each sample, respectively, and **(d)** EDS elemental map of the composite GaAs/Ge buffer layer interfaces in Sample C.

Ge (blue) and Si (green) layers are clearly visible with no evidence of interdiffusion at the interfaces, which would have been indicated by a mixing of colors in the EDS map. Several dislocations that migrate into the buffer can be seen to annihilate, likely caused by thermal annealing during growth. Furthermore, no micro-twins or stacking faults were observed, demonstrating good crystal quality across samples. To investigate the electrical performance of grown cells, devices were fabricated on each sample and their conversion efficiency parameters measured.

4.3. Device Fabrication of Solar Cells

Solar cells were fabricated from all three samples using previously in-house developed process at the Micro and Nano Fabrication Facility at Whittemore Hall, Virginia Tech. These devices were all-front contact, enabled by the lateral conduction layer grown above buffer layers, to avoid carriers from travelling through the highly dislocated buffer regions. The fabrication process began with solvent cleaning, native oxide removal in dilute NH_4OH, followed by four levels of lithography and PVD metallization of contacts. MgF_2/ZnS based Anti-Reflection Coating (ARC) was deposited using KJ Lesker PVD-250 tool, after top GaAs

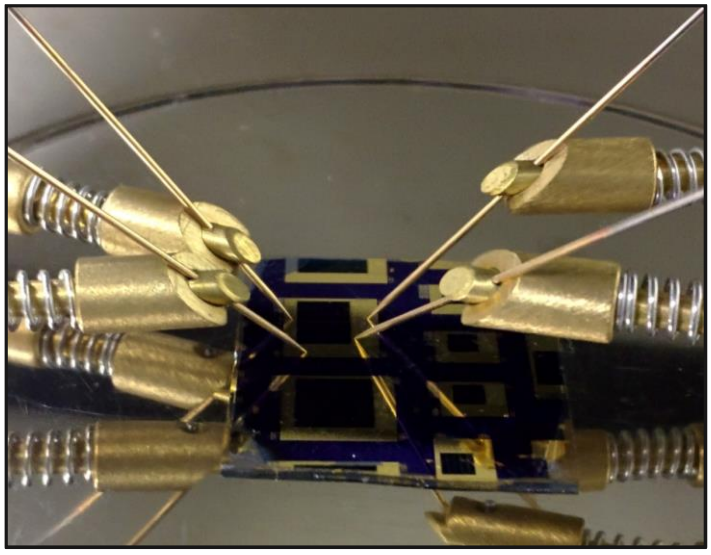

Figure 4.4: Fabricated Solar Cells being probed for Electrical measurements

cap etch. To better understand the effect of defects in the active region, cells of dimensions (0.5 cm × 0.5 cm) and (0.2 cm × 0.2 cm) were processed on Samples B and C. Details of this fabrication process has been previously reported [2]. The fabricated cells were then probed under simulated solar spectrum to measure their electrical performance (Fig. 4.4).

4.4. Electrical Characterization of Fabricated Solar Cells

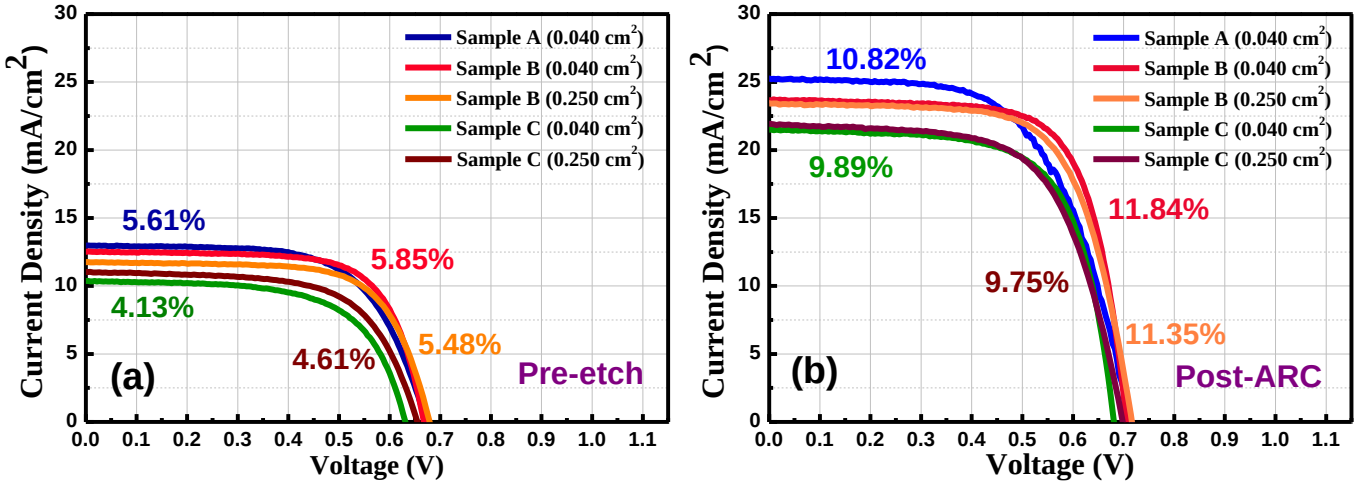

Figure 4.5. I-V characteristics with cell efficiency indicated of Samples A, B and C **(a)** before etching out the top contact layer, **(b)** after etch and ARC deposition of the same

Current-voltage (I-V) characteristics of the fabricated solar cells are measured on an Oriel SOL 2A 150W solar simulator equipped with AM1.5G filter. QE measurements of these cells were also performed on a Newport IQE200 series QE system which utilizes a xenon lamp and has the capability to measure the IQE, EQE and reflectance over the entire solar spectrum starting from 300 nm – 1800 nm using a Si/Ge detector. Fig. 4.5(a) and (b) depict the I-V characteristics of fabricated cells under AM 1.5 G conditions at both pre-cap etch and post ARC deposition stages, respectively, and Table 4.1 enlists critical performance parameters for the latter. The V_{oc} can be observed to be strongly limited due to dislocations in the photo-active junction. The J_{sc} increases by 100% after etching and ARC deposition due to a lack of contact-layer photon adsorption and minimized reflection from the cell surface. Cell performance is limited by threading dislocations into the base region, as is corroborated from the EQE graph

Sample #	Cell Area (cm^2)	Voc (V)	Jsc (mA/cm^2)	Fill Factor (%)	Efficiency η (%)
Sample A	0.040	0.715	25.232	59.98	10.82
Sample B	0.040	0.705	23.684	70.86	11.84
Sample B	0.250	0.716	23.420	67.70	11.35
Sample C	0.040	0.680	21.493	67.60	9.89
Sample C	0.250	0.698	21.880	63.83	9.75

Table 4.1. Output performance parameters for different cell sizes on each sample after anti-reflection coating deposition.

in Fig. 4.6, which shows a flat spectral response for higher energy photons between 475 nm to 675 nm, but drops steadily for higher wavelengths. The impact is less severe for the low wavelength regime (<700 nm) likely because during cell growth, GaAs emitter is grown after the GaAs base, therefore the additional thickness and thermal budget help annihilate dislocations and restrict their propagation in the direction of the growth, as evident from the cross-sectional TEM micrograph of Fig. 4.3. Peak IQE was found to be ~84% for Sample A,

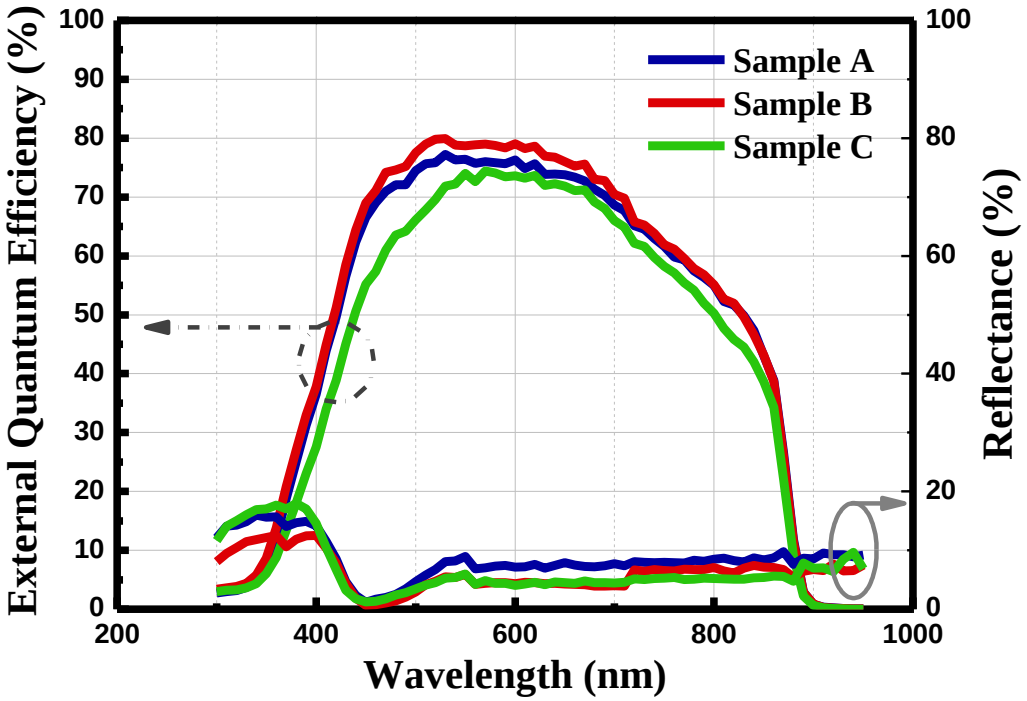

Figure 4.6. External quantum efficiency (EQE) and Reflectance of samples with incident light spectra

~85% for Sample B, and ~79% for Sample C; much smaller than that for GaAs cells grown on GaAs substrate (~90%). The high surface roughness in Sample B does not translate into lower electrical performance, corroborating the inference that dislocations reaching the active cell layers limits conversion efficiency in all grown cells. Smaller area (0.040 cm^2) cells, expected to be less sensitive to defects, corroborate with slightly higher efficiencies. Overall, there is high uniformity between output parameters of cells of both sizes. Sample A suffers from high series resistance losses that limit its fill factor, likely stemming from a reduced lifetime of minority carriers in its thicker base, as the fabrication process is consistent across all cells. On the contrary, shunt resistance is found to be very high in Sample A and significantly smaller in Sample C, which further reduces the V_{oc} value. This is potentially caused by a higher density of dislocations in Sample C, which serve as leakage path for carriers in the active cell.

The single diode model was employed in extraction of diode parameters i.e. saturation current (I_0) and ideality factor (n) of the measured solar cells under illumination and at 300 K to analyze the junction quality. Table describes the extracted parameters of each solar cell sample of same size (0.040 cm^2) including measured parasitic series (R_s) and shunt (R_{sh}) resistances under AM 1.5G illumination.

Sample #	V_{oc} (V)	I_{sc} (mA)	FF (%)	R_s (ohms)	R_{sh} (ohms)	Ideality Factor *n*	Diode Current I_0 (mA)
Sample A	0.715	1.0093	59.98	152.51	29919	1.76	$1.52x10^{-7}$
Sample B	0.705	0.9473	70.86	69.43	35674	1.57	$2.71x10^{-8}$
Sample C	0.680	0.8597	67.60	79.10	23397	1.84	$5.35x10^{-7}$

Table 4.2: Measured and extracted parameters of the light I–V curves of 0.040cm^2 area solar cell samples using the one-diode model

The ideality factor for all solar cell samples lie between 1 and 2, indicating competing recombination processes with the ideal diode. This deviation from the ideal diode is a direct result of imperfections in the fabricated structures, which influence field distribution within the active layer, and lead to a reduction in the effective voltage (V) in the form of a higher ideality factor. Sample A has an ideality factor greater than that of Sample B, indicating higher number of recombination centers within the active region, most likely due to additional dislocations in the thicker base region. Sample B and C have the exact same active cell structure, hence the higher ideality factor in Sample C arises from higher defect density in active cell due to a thinner dislocation-filtering buffer. Overall, it appears that the diode ideality factor depends upon thickness and defect density of the active layer.

The reverse saturation current (I_0) is related to the loss of photo-generated charge carriers at defects due to recombination. These recombination mechanisms can be broadly classified as surface and bulk recombination [3]. Bulk recombination depends on defect density and thickness, under constant surface area of the active layer. Thus, with higher defect density and/or thicker active layer the bulk recombination dominates over the surface recombination. Between Sample A and Sample B, the observed increase in the I_0 is primarily due to increased bulk recombination. For Sample A with thicker active layer, total number of defects in the active layer increases, leading to a larger bulk recombination of photo generated charge carriers. Comparing I_0 between Sample B and Sample C, we can see higher recombination at bulk defects in Sample C with less than half the dislocation-filtering buffer thickness in Sample A, which leads to one order increase in the saturation current. Throughout the electrical characterization of these solar cells, we observe that despite the drastic reduction of buffer thickness in Sample C, the Ge virtual substrate formation ameliorates its impact on cell performance. We also observe that a thinner active cell leads to lower recombination loss of

charge carriers and lower diode ideality factor, both of which are favorable characteristics of a solar cell.

Sample C, with a 900 nm buffer as opposed to a 2 µm buffer in Samples A and B, provides competent results; inferring that the 144 nm Ge intermediate layer enables a very thin buffer layer in this promising approach for designing high efficiency GaAs cells on Si. If we were able to better control the defects in our thin buffer layer stack, we can expect to see higher efficiency GaAs solar cells on Si with reduced material cost and improved thermal stability. We have demonstrated a novel design for the monolithic integration of III-V solar cells on Si utilizing an intermediate Ge layer, which can serve both as a buffer layer or an active layer to realize a hybrid Ge-Si bottom sub-cell. This virtual "Ge-*on*-Si" template, must be optimized to minimize threading dislocations from the lattice-mismatched interface, and requires further investigation of its structural and electrical properties. The following *Chapters* encompass a comprehensive study of the properties of this Ge-*on*-Si heterostructure.

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Chapter 5

Growth and Structural Properties of Germanium-*on*-Silicon Thin-Films

Chapter 4 has demonstrated the use of Ge thin –film on Si to integrate 1JGaAs solar cells on Si. We observe that the introduction of Ge enables a thin buffer for heterointegration; however, the cell performance has tremendous room for improvement. For better understanding of the limiting factors and ways to optimize cell performance, we now investigate the thin Ge-*on*-Si heterostructures. We have also seen in *Chapter 1* that Ge is an attractive candidate for next-generation high speed and low-power devices. There remains the need to integrate Ge on to established Si platform, as the integration of large-diameter, bulk Ge wafers with the current CMOS process is cost-prohibitive. Various methods of integration of Ge devices onto Si platform were discussed, along with the challenges or shortcoming of these methods. The direct integration of thin Ge films onto Si substrate, also provides a cost-effective route for the monolithic integration of Ge electronics on Si platform.

To evaluate the viability of the above-mentioned approaches, thin Ge films were grown on Si and the heterostructures characterized for their material properties and electrical performance. A major objective of this study was to understand the effect of the significant lattice mismatch

and thermal mismatch between Ge and Si, on the characteristics of this heterostructure. This chapter presents the investigation of structural properties of the heterointegrated Ge-*on*-Si thin film platform. To that end, the strain relaxation properties of the Ge-*on*-Si heterostructure were investigated by triple axis x-ray diffraction and micro-Raman spectroscopy. Surface roughness, which affects carrier mobility by increasing surface scattering, was evaluated via AFM. Cross-sectional and plan-view TEM (PV-TEM) analysis was used to evaluate the structural and defect properties of the epitaxial Ge-*on*-Si heterostructures. Photoluminescence (PL) measurements were also performed to evaluate the film's optical quality and compare it to that of bulk Ge and Ge grown on GaAs.

5.1. MBE growth of Ge-*on*-Si heterostructure

In this chapter, Ge thin film was grown on a (100)/4˚ offcut Si substrate *in-situ* using solid-source MBE, utilizing separate Ge and III-V growth chambers connected via an ultra-high vacuum transfer chamber. The undoped epitaxial ~135 nm Ge layer was grown employing a two-step, low temperature-high temperature growth process incorporating several annealing stages. This two-step growth process for Ge has been previously reported [1] to achieve device-quality Ge films with low surface roughness, good crystalline quality and minimal intermixing between the Ge and Si layers. The Ge growth temperature was in the range of 250˚C to 400˚C, after initial Si oxide desorption at 900ºC to obtain a smooth starting substrate. The low temperature growth initiation facilitates the preservation of a highly ordered, two-dimensional growth surface, whereas subsequent high temperature growth and annealing phases provide additional thermal budget for the growing Ge film to relax via dislocation annihilation and dislocation glide. As a result, the Ge epilayer is expected to exhibit enhanced crystallinity and a smooth surface morphology.

5.2. Surface Roughness of Ge-*on*-Si via AFM

Surface morphology is understood to play a key role in electronic, optoelectronic, and photovoltaic device applications due to the direct correlation between surface roughness and device properties (e.g., surface scattering-induced mobility degradation, minority carrier surface recombination velocity, etc.). Correspondingly, the ability to accurately quantify material surface morphology via AFM provides a useful metric for the evaluation of growth and fabrication processes. In this work, the surface morphology and *rms* roughness of an MBE grown Ge-*on*-Si thin film was measured via AFM, as shown by the representative micrographs in Fig. 5.1(a) and 5.1(b) (10 µm x 10 µm and 1 µm x 1 µm scan sizes, respectively). The *rms* roughness of the as-grown Ge epilayer was found to be less than 2 nm despite the 4% lattice mismatch between Ge and Si, suggesting that the low temperature Ge nucleation aids in maintaining a smooth, two-dimensional (2-D) surface reconstruction throughout the growth. This conclusion is further reinforced by the lack of observable island formation in the short-

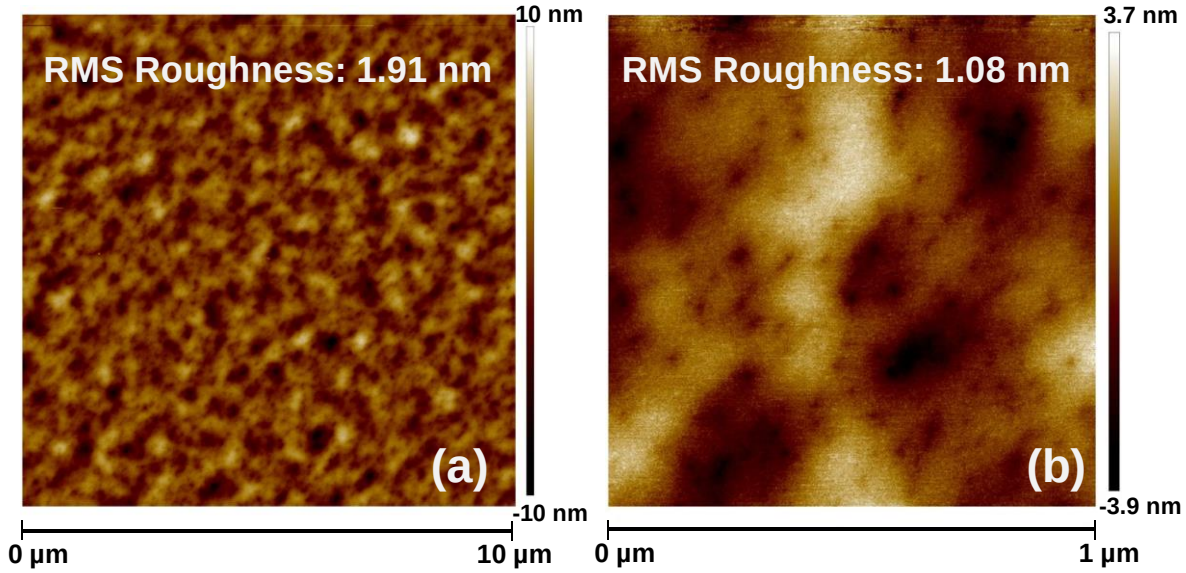

Figure 5.1: AFM micrographs of the epitaxial Ge-*on*-Si heterostructure for **(a)** 10 µm x 10 µm and **(b)** 1 µm x 1 µm scans, exhibiting RMS surface roughness < 2 nm

range (1 µm x 1 µm) AFM micrograph. The structural quality of this lattice-mismatched Ge epilayer is later investigated in detail using TEM and XRD analysis.

5.3. Strain Analysis of Ge-*on*-Si via Micro-Raman Spectroscopy:

Elastic strain effects in thin film semiconductors due to lattice mismatch or thermal coefficient mismatch can cause mechanical curling, fracture, and even device failure. Cracking in solar cells is a prevalent issue, and strain in buffer layers must be closely monitored to avoid any cracks in the cell structure grown on top. Raman spectroscopy has been widely used to measure in-plane strain in films *via* the shift of Raman vibrational modes. Peak shifts in Raman spectroscopy thus provide a convenient method for the non-destructive assessment of strain in a system. To that end, micro-Raman spectroscopy was employed in order to determine the residual strain (if any) in the epitaxial Ge thin-film grown on Si. It is worth noting that the penetration depth of the optical excitation source is expected to be less than 20 nm in Ge [2], thus the collected Raman spectra are representative of the Ge epilayer (~135 nm) and suitable for the subsequent strain-state analysis. Fig. 5.2 compares representative Raman spectra acquired from the Ge thin-film grown on Si (in green) and an n-type (100) Ge substrate (in yellow), highlighting the fundamental un-strained Ge Raman line at 300.83 cm^{-1}. Additionally, the inset shows the fitted Raman spectrum for the Ge-*on*-Si epilayer, clearly identifying the experimentally observed Ge-*on*-Si peak position ($\omega_{Ge\text{-}on\text{-}Si}$ = 300.40 cm^{-1}) and its corresponding wavenumber shift with respect to the bulk Ge phonon mode. The in-plane biaxial strain in the Ge epilayer was estimated from the shift in phonon vibration mode ($\Delta\omega$) relative to bulk Ge, using the relation:

$$\Delta\omega = -b\varepsilon_{\parallel} ,$$

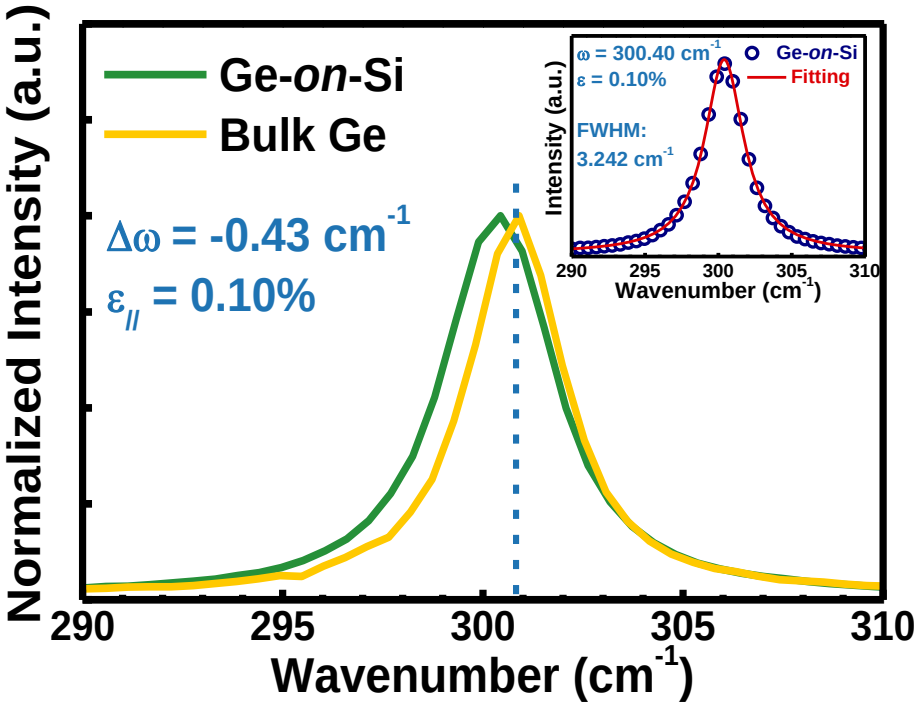

Figure 5.2: Raman spectra of the 135 nm Ge-*on*-Si thin-film and a bulk Ge substrate. The shift in the FWHM centroid indicates a slightly tensile-strained Ge epilayer.

where b is a material parameter dependent on the material's phononic and elastic constants. Using the reported literature value of b = 415 cm^{-1} for Ge [3], a tensile strain of $\varepsilon_{//}$ = 0.10% was deduced in the Ge-*on*-Si epilayer for the observed Raman shift and was believed to be caused by the difference in thermal expansion coefficients of Ge and Si. Moreover, for single-crystal Ge, only one active phonon mode contributes to Raman scattering in the (001) back scattering measurement orientation. One can find from Fig. 5.2 that a singular active phonon mode was indeed observed. Additionally, the low full width at half maxima (FWHM ~ 3.24 cm^{-1}) of the measured Ge-*on*-Si phonon mode suggests a highly ordered film [4]. To confirm the Raman-derived strain-state of the epitaxial Ge-*on*-Si film, high-resolution x-ray diffraction measurements were used to independently analyze the structural properties of the Ge epilayer.

5.4. Structural Quality of Ge-*on*-Si via X-ray Diffraction Analysis

High-resolution x-ray diffraction has been commonly used to study epitaxial lattice mismatch, epilayer mosaicity, ternary alloy composition, strain relaxation, epilayer thickness, and superlattice periodicity in semiconductor heterostructures [5,6]. In this work, the relaxation state of the Ge epilayer and its crystalline quality were investigated using symmetric (004) and

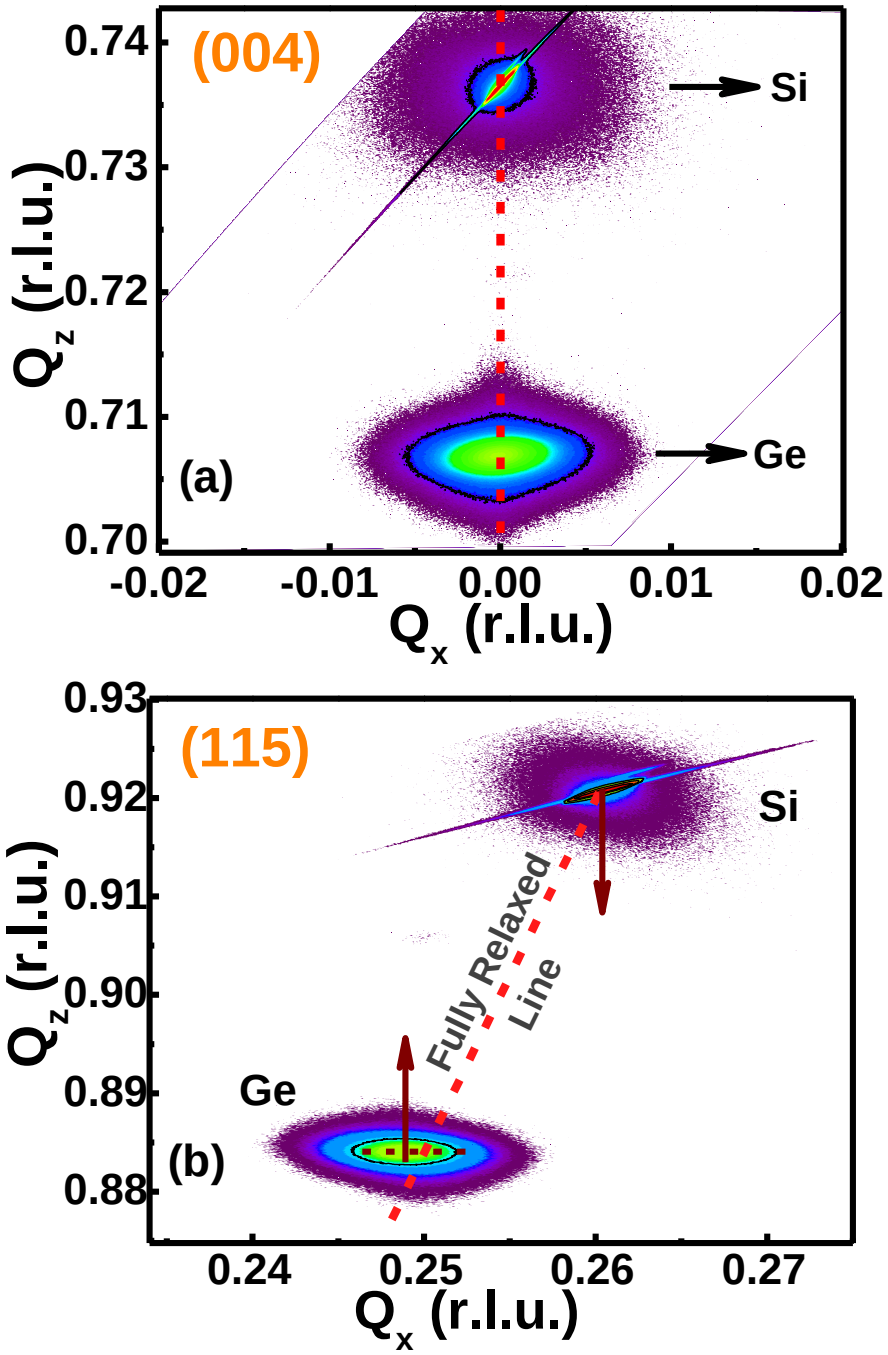

Figure 5.3: (a) Symmetric (004) and **(b)** asymmetric (115) RSMs of Ge-*on*-Si. . No lattice tilt was observed, as shown by the alignment in Q_x of the Ge and Si RLPs in the (004) RSM. The asymmetric (115) RSM indicates the presence of residual stress in the Ge epilayer.

asymmetric (115) RSM analysis, as shown in Fig. 5.3(a) and 5.3(b), respectively. As can be readily seen in the symmetric (004) RSM shown in Fig. 5.3(a), the Ge reciprocal lattice point (RLP) was found to be aligned (in Q_x) with the RLP of the Si substrate, indicating minimal lattice tilt within the Ge epilayer. Additionally, the in-plane and out-of-plane lattice constants of Ge were calculated using the asymmetric (115) and symmetric (004) RSMs respectively, and methods outlined in literature [7]. Utilizing the experimentally derived lattice constants, the relaxation state of the Ge epilayer was determined with respect to the Si substrate, indicating that the as-grown Ge-on-Si thin-film was ~99% relaxed. Upon further inspection of the asymmetric (115) RSM (Fig. 5.3(b)), the (115) Ge RLP was found to be distinctly shifted towards lower Q_x, deviating from the vector (pointing towards (000) in reciprocal space) indicative of full epilayer relaxation. These results suggest the presence of low levels of residual stress in the Ge epilayer, corroborating the Raman analysis discussed above. The observed tensile strain in the Ge epilayer can be linked to the thermal expansion coefficient mismatch between Ge and Si, resulting in residual epilayer strain following high temperature Ge-*on*-Si growth [8]. Finally, minimal Ge RLP mosaicity in both (004) and (115) RSMs further confirmed the crystalline quality of the Ge/Si heterostructure. Additional insight into the relaxation mechanisms at the Ge/Si heterointerface and the defect distribution within the Ge epilayer was provided by cross-sectional and plan-view TEM analysis.

5.5. Defect Analysis of Ge-*on*-Si via TEM

Transmission Electron Microscopy was used to analyze the propagation of defects through the Ge layer, as device performance is sensitive to threading dislocations into the active region of the material stack, which act as recombination centers and provide leakage path to charge

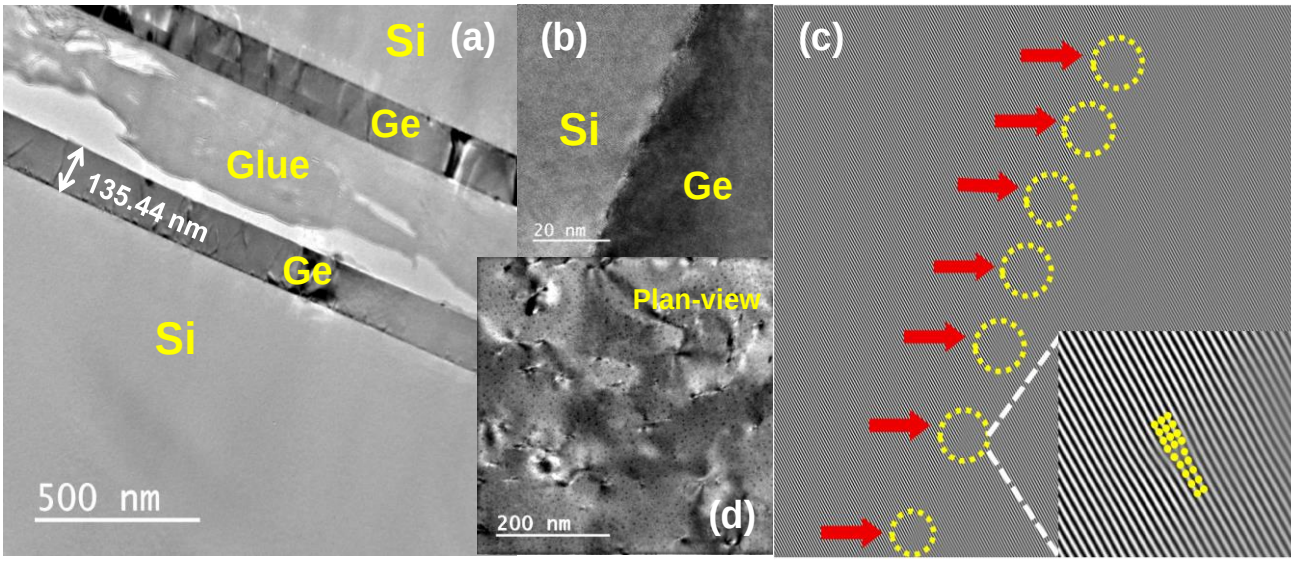

Figure 5.4: (a) Cross sectional TEM micrograph of the Ge-*on*-Si heterostructure. **(b)** High-resolution TEM micrograph of the Ge/Si heterointerface revealing interfacial misfit dislocations, which upon further analysis were found to be 90˚ Lomer dislocations **(c)**. **(d)** Plan view TEM micrograph highlighting threading dislocations present in the Ge epilayer.

carriers. Fig. 5.4(a) shows a representative low-magnification TEM micrograph of the as-grown Ge/Si heterostructure, consisting of approximately 135 nm of unintentionally doped Ge epitaxially grown on (100)/4° Si, whereas Fig. 5.4(b) shows a high magnification TEM micrograph corresponding to the Ge/Si heterointerface. The abrupt and uniform nature of the Ge/Si interface suggests minimal atomic intermixing occurred during epilayer growth. Moreover, the low magnification TEM micrograph in Fig. 5.4(a) shows limited propagation of defects from the heterointerface towards the Ge surface, which is especially critical for transistor channel applications. Additionally, the recorded TEM micrographs revealed two distinct strain relaxation mechanisms: (i) a periodic array of 90˚ Lomer misfit dislocations (MDs) with separation varying from 5.8 nm to 12.1 nm, as clearly seen in Fig. 5.4(c); and (ii), a network of TDs visible from the plan-view TEM micrograph shown in Fig. 5.4(d). Atomistic modelling of Lomer dislocation arrays at the Ge/(001)Si heterointerface by Dornheim et al [9] showed that full relaxation of misfit strain in the [110] direction implies a separation of 9.6 nm between two Lomer dislocations. In a compressively strained material system, wherein the Ge

epilayer lattice constant (5.658 Å) is larger than the Si substrate lattice constant (5.431 Å), the MD is associated with an extra half-plane of atoms inserted within the substrate, as can be seen in the reconstructed HR-TEM image of the (111) planes shown in the bottom-right inset of Fig. 5.4(c). The MDs at the Ge/Si heterointerface allow for partial strain relaxation and are understood to aid in reducing threading dislocation propagation through the Ge layer. Moreover, the pure edge nature of 90˚ Lomer dislocations implies that they do not have a tilt component, as was corroborated by the (004) RSM shown in Fig. 5.3(a). Fig. 5.4(d) shows a representative PV-TEM micrograph of the Ge/Si heterostructure, from which a TDD of ~10^{10} cm^{-2} was determined. It is important to note that PV-TEM captures a set of threading dislocations, each of which has a component of its line vector perpendicular to the image plane. These dislocations may bend out of the image plane prior to reaching the top surface, and therefore have little influence over carrier transport or inversion behavior close to the Ge surface. The effect of propagating defects on carrier transport is modelled in *Chapter 6*, followed by an investigation into their electrical trapping characteristics.

5.6. Optical Properties of Ge-*on*-Si via Photoluminescence Spectroscopy

Ge photoluminescence has been studied for several decades, [10-13] predominantly at low temperatures, in order to develop Ge-based photodetectors [14] and optical sources [15] for the realization of on-chip photonics. In this work, PL was used to investigate the optical properties of the as-grown Ge-*on*-Si heterostructure as well as the influence of film dislocations on these properties. Previously, Haynes and Nilsson [12] reported a direct transition emission feature at 0.8 eV for a 120 µm Ge sample measured at room temperature. More recently, Lieten *et al.* [13] studied the various phonon-assisted transitions in doped and un-doped bulk Ge between 7 K and 400 K. At 7K, Lieten and co-workers observed intense luminescence peaks at 0.73 eV, 0.71 eV, and 0.702 eV, which were attributed to phonon-assisted exciton recombination

involving transverse acoustic (TA), longitudinal acoustic (LA) and transverse optical (TO) phonons, respectively, in the [111] direction. Fig. 5.5(a) shows the PL spectrum of bulk n-type ($N_D \sim 3x10^{17}$ cm^{-3}) Ge at room temperature highlighting the dominant phonon-assisted indirect

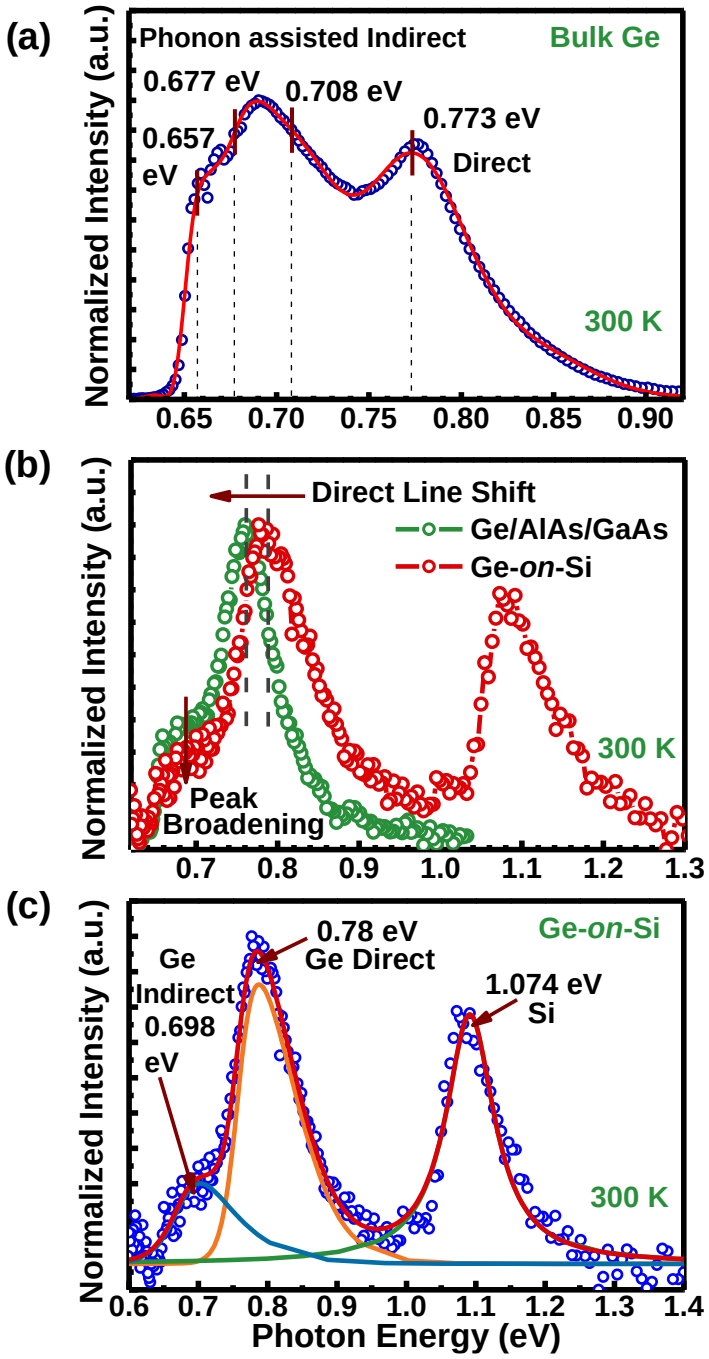

Figure 5.5: (a) PL peaks of bulk n-type Ge showing direct and indirect transitions, **(b)** Comparison of Ge-*on*-Si PL spectrum with Ge epilayer grown on GaAs using AlAs buffer **(c)** de-convoluted PL spectrum of Ge-*on*-Si sample showing the different optical transitions.

transition peaks as well as the singular direct transition emission feature. Similarly, Fig. 5.5(b) compares the PL spectra taken from the epitaxial Ge-*on*-Si structure and an almost lattice-matched Ge/AlAs/GaAs heterostructure. Lastly, Fig. 5.5(c) shows the de-convoluted PL spectrum from the as-grown Ge-on-Si heterostructure revealing both Ge- and Si-related spectral features. One can find from Fig. 5.5(a) that two broad phonon-assisted indirect recombination peaks (0.677 eV and 0.708 eV) were observed, whereas the direct-gap emission feature expected at 0.8 eV was blue-shifted to 0.786 eV due to the bandgap narrowing effect [16]. Conversely, the PL spectrum recorded from the Ge-*on*-Si heterostructure (Fig. 5.5(c)) revealed three major luminescence peaks: (i) a phonon-assisted indirect transition peak from the Si substrate at ~1.07 eV; (ii) a strong direct transition peak in Ge at 0.78 eV; and (iii) a weak, broadened indirect transition peak in Ge at 0.7 eV. The indirect peak at 0.7 eV is partially cut off due to detector limits, and cannot be resolved completely. Any weak signal detected below 0.6 eV in the Ge-*on*-Si sample was due to a second order diffraction from the Si peak, and disappeared when a long pass filter was used to remove any signal from Si.

In this *Chapter*, we investigated the structural characteristics of the Ge-*on*-Si heterostructure and observed a ~0.1% tensile strained stack, with high defect density threading dislocations from the mismatched interface but no observed lattice tilt. In *Chapter 6*, we probe this heterostructure to study its electrical properties, which will determine the performance of photovoltaic and electronic devices employing this Ge-*on*-Si stack.

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Chapter 6

Electrical Properties of Germanium-*on*-Silicon Thin-Films

In this *Chapter*, we electrically characterize the MBE grown Ge-*on*-Si heterostructure and seek to understand the effect of structural defects on these properties. To assess electrical quality of the Ge epilayer, Hall mobility measurements were performed as a function of temperature. The experimental mobility data were then fit via theoretical consideration of the scattering processes in Ge in order to isolate the dominant scattering processes limiting carrier mobility. Carrier mobility in the Ge layer determine the motion of carriers through this epilayer, critical for improved solar cell currents and transistor current. Low- and room-temperature multi-frequency C-Vand G-V measurements were performed in order to analyze the interfacial quality of the atomic layer deposited (ALD) Al_2O_3/Ge MOS interfaces. The extracted interface trap density (D_{it}) values were benchmarked against previously published Ge MOS D_{it} data as a function of film dislocation density. Lastly, DLTS was used to measure electrically active trap levels and the trap response times within the epitaxial Ge film. Obtained results in this *Chapter* highlight the viability of the Ge-*on*-Si direct integration path for next-generation

energy efficient germanium electronics, and compound semiconductor solar cells grown on Si via thin Ge buffer.

6.1. Carrier Mobility and Scattering Processes in Ge-*on*-Si:

Carrier mobility, and its dependence on temperature, are key figures of merit for the direct integration of Ge-based electronics on Si. Correspondingly, in order to assess the electrical quality of the Ge-*on*-Si thin-film, temperature-dependent Hall mobility measurements were performed and analyzed to extract carrier mobility and carrier concentration. Subsequent theoretical treatment of the measured data was employed to model relevant scattering mechanisms and determine their influence on carrier transport. To this end, the carrier density (n) and mobility (μ_n) of an n-type semiconductor was determined from the measured Hall coefficient ($R_H(B)$) and the resistivity ($\rho(B)$) using the relations described in *Chapter 3* (Eq. 3.2-3.3). Fig. 6.1 shows the measured μ_n and sheet carrier concentration (N_s) as a function of temperature. The measured electron mobility was found to weakly depend on temperature,

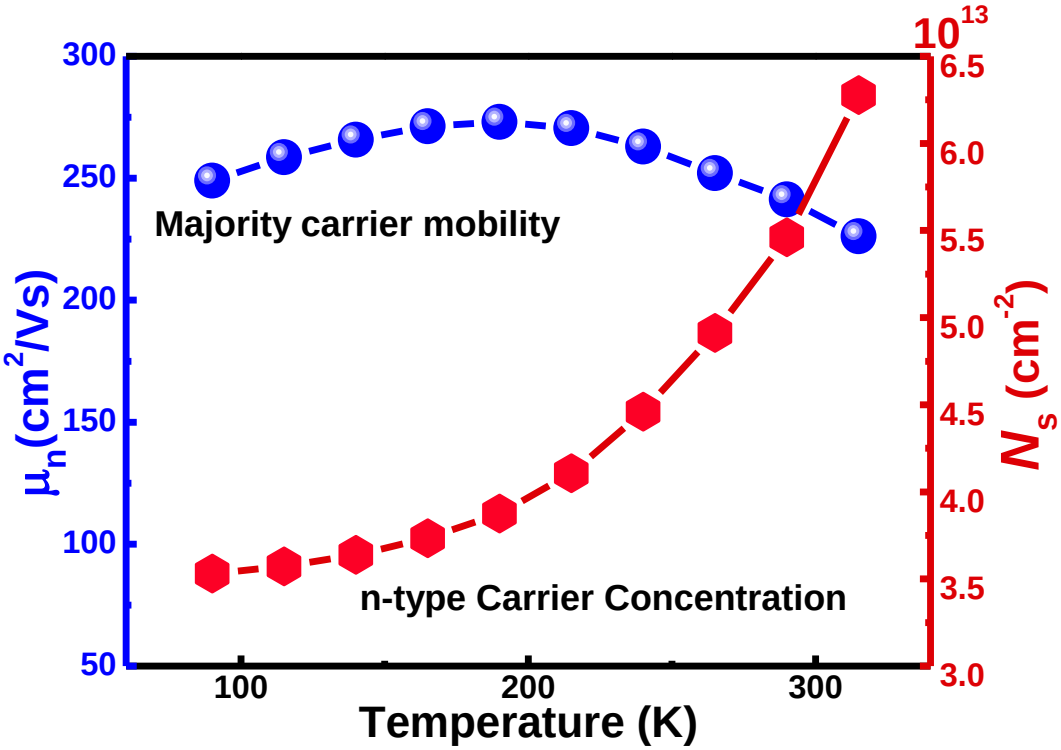

Figure 6.1: Mobility and sheet carrier concentration of epitaxial thin 135 nm n-type Ge-*on*-Si.

exhibiting decreases at both high and low temperatures. Such behavior has been previously observed in heavily doped semiconductors, due to the reduced contribution of lattice scattering component to carrier mobility [1]. Despite the absence of a dopant source during growth, a sheet carrier concentration of 5.46×10^{13} cm^{-2} (bulk concentration ~4.5×10^{18} cm^{-3}) was measured in the Ge epilayer. Moreover, the high free carrier density at low temperatures (< 100 K) reveals the shallow nature of the donor-like impurities. The p-type Si substrate has a resistivity of 1 to 5 Ω-cm, and the *p-n* junction formed enables electrical isolation of the Ge layer from the substrate in these measurements.

Theoretical treatment of the experimental transport data employed Boltzmann's transport equation to model epilayer carrier mobility as a function of scattering mechanism and measurement temperature. Accordingly, the relaxation time approximation was used to describe the dominant scattering mechanisms including: (i) acoustical phonon and optical phonon scatterings; (ii) ionized impurity scattering; (iii) neutral impurity scattering; and (iv) dislocation scattering. The calculated carrier mobility assumes the validity of Matthiessen's rule and the total mobility is obtained following Eq. 3.7-3.9, described in *Chapter 3*.

Table 6.1: Mobility expressions for various scattering processes in Ge.

Scattering mechanisms	Mobility (μ)	Reference No.
Optical deformation potential scattering	$\mu_{ODP} = 6.4\times10^{-5}\left(\frac{C_l}{E_A^2}\right)\left[\frac{exp\left(\frac{\theta}{T}\right)-1}{T^{1/2}\,\theta}\right]\left(\frac{m_0}{m^*}\right)^{5/2}$	[2-5]
Acoustic deformation potential scattering	$\mu_{ADP} = 3.17\times10^{-5}\left(\frac{C_l}{E_A^2}\right)T^{-3/2}\left(\frac{m^*}{m_0}\right)^{-5/2}$	[3,6]
Dislocation Scattering	$\mu_{dis} = \frac{2^{6.5}a_0}{\sqrt{\pi}m_{hh}^{1/2}q^3N_{dis}}\lambda^{-1}(k_BT)^{3/2}$	[7,8]
Ionized impurity scattering	$\mu_{ion} = \frac{\sqrt{2}\varepsilon_0^2\varepsilon_S^2(2k_BT)^{3/2}}{N_I q^3 m^{*1/2}\ln\left[1+\left(3\varepsilon_0\varepsilon_S k_BT/q^2N_I^{1/3}\right)^2\right]}$	[1,9]
Neutral impurity scattering	$\mu_n = \frac{1}{20}\frac{m_n q^3}{N_N\kappa\hbar^3}$	[10,11]

Table 6.2: Parameters used for calculating the mobility in Ge and corresponding References.

Parameters	Germanium	Reference No.
Lattice Constant, a_0 (Å)	5.6579	[12,13]
Optical Phonon Debye Temperature, ϑ (K)	382	[12,13]
Deformation Potential, E_A (eV)	9.5	[12,13]
Average Longitudinal Elastic Constant, C_{ll} (dyne/cm^2)	12.60 x 10^{11}	[12,13]
C_l (dyne/cm^2)	1.503 x 10^{12}	[12,13]
Effective mass of electron, m_n, m^* (kg)	0.22 x m_0	[12,13]
Debye Screening Length, λ (m)	$\sqrt{\varepsilon_0 \varepsilon_s k_B T / N_e q^2}$	--------
Vacuum Permittivity, ε_0 (Fm^{-1})	8.85 x 10^{-12}	--------
Relative Permittivity, ε_S	16.1	[14]
Dielectric Constant, κ	16.1	[14]
Boltzmann Constant, k_B (JK^{-1})	1.38 x 10^{-23}	--------
Reduced Planck Constant, $\hbar$ (Js^{-1})	1.056 x 10^{-34}	--------

Table 6.1 and **Table 6.2** summarize the mobility expressions and material parameters associated with each scattering mechanism, respectively, as taken from literature.

Fig. 6.2 shows the calculated mobility as a function of temperature for various scattering processes following the procedures previously outlined. Scattering by ionized impurities is modelled upon the semi-classical solution for the long-range Coulomb field induced at an ionized impurity center in the lattice, developed by Conwell and Weisskopf [9]. The scattering potential due to a neutral shallow level impurity center is described by a square well potential which becomes a dominant scattering source for carriers at low temperatures [11]. Consequently, neutral impurity scattering mobility varies indirectly with temperature *via* the neutral impurity density, N_N. Lastly, the effect of dislocations on carrier mobility can be understood by the introduction of acceptor centers along a dislocation line, which capture electrons from the conduction band of the n-type Ge [7,8]. The resulting potential field around these charged dislocation lines scatter the conduction electrons and reduce electron mobility. Here, N_{dis} denotes the concentration of threading dislocations. The $T^{3/2}/\lambda$ dependence of the mobility shows competition between a number of high thermal energy carriers and screening

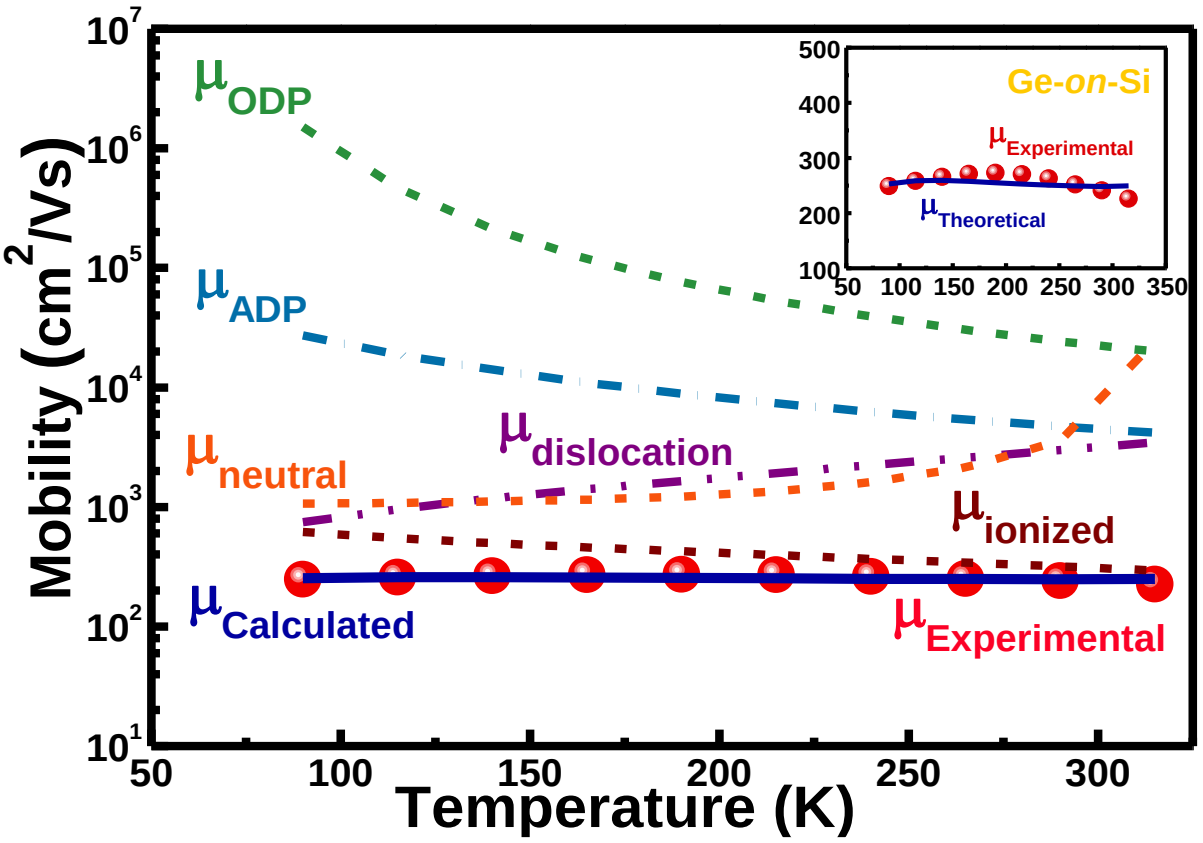

Figure 6.2: Measured electron mobility of Ge-*on*-Si epilayer as a function of temperature along with the theoretical calculated mobility from individual scattering mechanisms. The calculated and measured mobilities show good agreement, as can be seen more clearly in the inset.

of the scatter source (charged dislocations). Fitting of the measured mobility data to this dislocation scattering model indicates a dislocation density of 7×10^{9} cm^{-2} influencing carrier mobility in the Ge-*on*-Si structure, slightly lower than the 10^{10} cm^{-2} TDD extracted from the PV-TEM micrograph in Fig. 5.4(d). The total calculated mobility compared to that measured *via* Hall shows comparable mobility values well within limits of error (< 2.2% *rms* fit error); however, the model was found to overestimate electron mobility at higher temperatures (>300 K). One possible cause for the quantitative disagreement between the calculated and experimental curves in Fig. 6.2 are additional scattering sources not accounted for by the proposed model, such as inter-valley and electron-electron scattering. Additionally, the carrier mobility was found to be limited by ionized impurity scattering due to the high unintentional doping concentration (~10^{18} cm^{-3}) in the Ge epilayer, particularly at higher temperatures.

Neutral impurities and dislocations appear to limit electron mobility only at low temperature when there is less screening by ionized donors. Previous research revealed that ionized impurity scattering and acoustic deformation potential (ADP) scattering dominate Ge mobility [2,12]; however, due to the high density of impurities and the presence of dislocations in the Ge-*on*-Si structure, ADP no longer strongly influences the carrier mobility. Moreover, as compared to ionized impurity scattering, dislocations introduced into the Ge epilayer upon lattice-mismatched heteroepitaxy were found to have less of an impact on carrier mobility under the high substrate doping conditions.

6.2. Ge-*on*-Si MOS Capacitor Characteristics:

It is generally understood that the oxide-semiconductor interface plays a critical role in determining the inversion characteristics of a MOS-C device. Consequently, MOS capacitors have proven invaluable in providing insight into the quality of the oxide/semiconductor heterointerface as well as the bulk semiconductor material. By conducting C-V and G-V measurements on MOS-C structures, standard metrics including flat-band voltage (V_{FB}), doping level (N_D or N_A), fixed oxide charge (N_{OT}), equivalent oxide thickness (EOT), effective work function (φ_{eff}), and interface trap density (D_{it}) can be extracted. Extraction of these parameters therefore allows for a quantitative assessment of the quality of the oxide/semiconductor interface.

6.2.1. MOS Capacitor Fabrication

P-type MOS capacitors were fabricated on the epitaxial n-type Ge-*on*-Si heterostructure using an Al_2O_3–based composite high-κ gate stack, in order to investigate the Ge epilayer's interfacial and bulk trap densities. Fabrication of the devices began with a 60s solvent degrease using acetone, isopropanol, and deionized (DI) water, followed by a 60s native oxide removal in dilute (1:10) hydrofluoric acid. A high-quality, native GeO_x interfacial passivating layer was

then formed by thermal oxidation at 450°C for 10 minutes in an O_2 ambient. Immediately afterwards, a 4 nm Al_2O_3 gate oxide was deposited at 250 °C using a Cambridge NanoTech ALD system with trimethylaluminum and DI water as precursors for Al and oxygen, respectively. The 250 nm Al gate electrodes 250 nm Al Ohmic contacts were subsequently deposited using a Kurt J. Lesker PVD250 electron beam deposition chamber. Fig. 6.3 shows a cross-sectional schematic of fabricated MOS-C device.

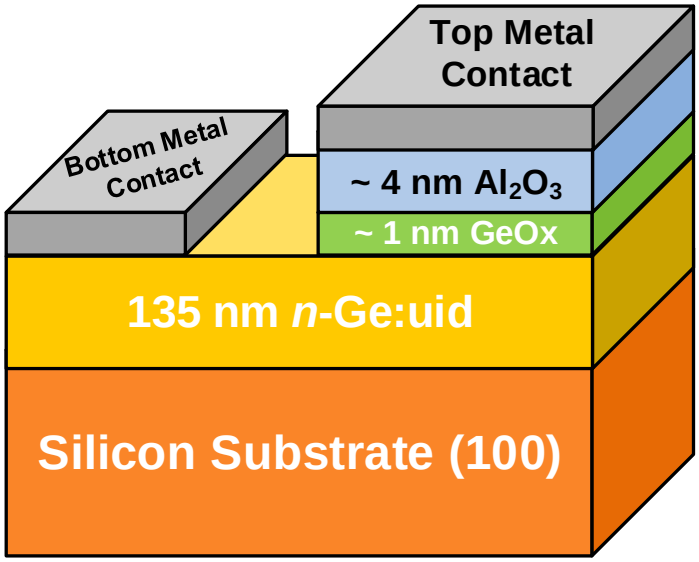

Figure 6.3: Ge-*on*-Si MOS capacitor structure.

To evaluate the electrical characteristics of the fabricated MOS-C devices, low- and room-temperature multi-frequency C-V and G-V were performed using an HP4284A precision LCR meter with frequencies ranging from 1 kHz to 1 MHz. Accurate measurements were obtained with the removal of series resistance (r_s), as discussed in *Chapter 3* (Eq. 3.24-3.26).

6.2.2. MOS Capacitor Measurement and Analysis

Fig. 6.4 describes the temperature-dependent C-V characteristics from a representative Ge *p*-MOS-C, in the temperature range of 292 K and 77 K. The C-V measurements demonstrate an increasing suppression of minority carrier- and/or D_{it}-induced inversion response for decreasing temperatures. A plausible reason for the persistence of low-frequency minority carrier inversion at 77 K are near-surface mid-gap traps in the depletion layer that create

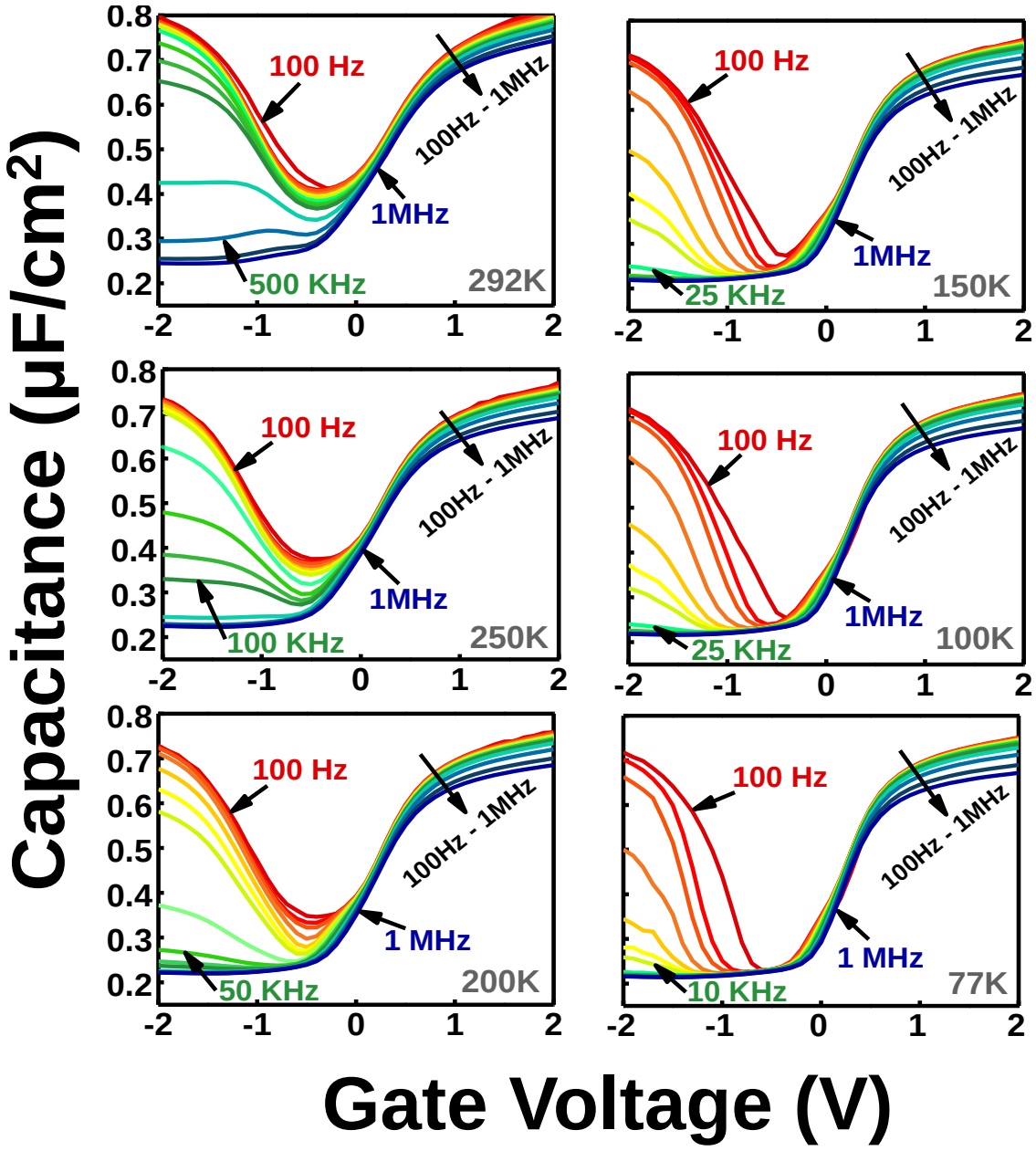

Figure 6.4: Capacitance-voltage characteristics of a representative Ge-*on*-Si MOS capacitor measured from 292 K to 77 K as a function of frequency, indicating the frequency (in green) at which inversion response begins to appear in the device.

electron-hole (*e*-*h*) pairs and provide the necessary population of minority carriers (holes) to create an inversion layer at negative bias [15]. This is investigated later *via* DLTS. Alternatively, interface traps and fixed oxide charge could also mediate *e*-*h* pair generation or induce a permanent inversion layer, thereby providing a supply of minority carriers at low temperatures [15,16]. Equivalent oxide thickness (*EOT*) of ~ 3.47 nm was derived for the

Al_2O_3/GeO_x gate stack at 292 K. A moderate V_{FB} shift (~ 0.28 V) was observed across all temperatures, which was attributed to the high unintentional doping in the Ge epilayer, as reported previously [17]. Limited interface states induce stretch out in the C-V curves, and a frequency dispersion of 2.8% per decade at 292 K was also observed. Additionally, high frequency C-V measurements taken at 292 K exhibited a signature of mid-gap interface trap response.

Trapped oxide charge density and hysteresis were also measured as a function of temperature, as shown in Fig. 6.5. One can find from Fig. 6.5 that the Ge MOS-Cs demonstrated a hysteresis of 323 meV at 292 K, which reduced to 250 meV at 250 K before increasing to 308 meV at 77 K (f = 100 kHz). The experimentally observed hysteresis was attributed to bulk oxide traps as opposed to insufficient dangling bond passivation at the oxide/Ge heterointerface [18,19]. From the measured C-V hysteresis, N_{ot} was extracted using the Maserjian method, which takes into account carrier quantization in the accumulation regime, using Eq. 3.18, described earlier

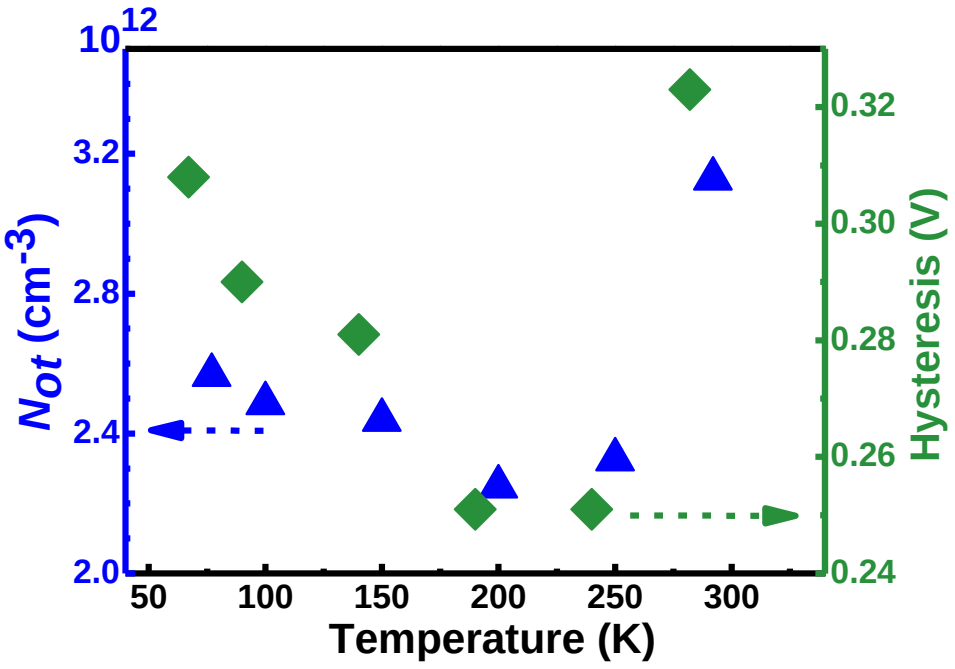

Figure 6.5: Extracted trapped oxide charge density and corresponding hysteresis in a representative Ge-*on*-Si MOS capacitor as a function of measurement temperature.

[20]. The extracted N_{ot} values were found to parallel the C-V hysteresis behavior over the range of investigated temperatures, peaking at ~3×10^{12} cm^{-3}.

Fig. 6.6 shows the conductance contours corresponding to G-V sweeps measured between 77 K and 292 K, qualitatively highlighting the FLE of the fabricated Ge MOS-Cs. The Fermi level trace (dotted black line) at each measurement temperature follows the conductance peak under different frequency and bias conditions, and its slope demonstrates how efficiently the FL is

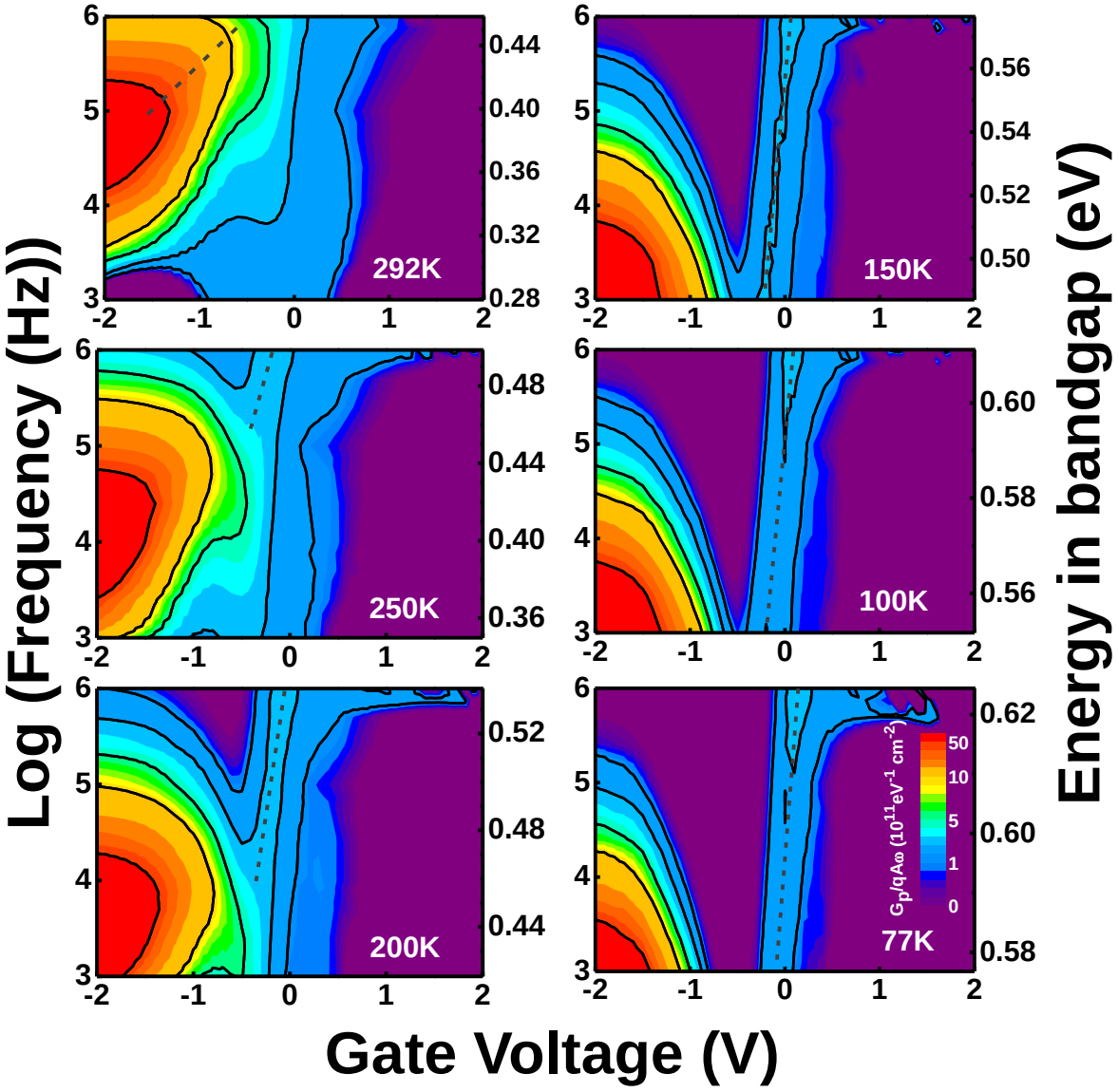

Fig 6.6: Conductance contours of a representative Ge-*on*-Si MOS capacitor measured from 292 K to 77 K, indicating steeper fermi level trace at lower temperatures. All figures follow the scale shown in 77K plot.

biased throughout the bandgap. The magnitude of the conductance peak within the depletion region was found to reduce significantly at decreased temperatures, as indicated by the gradual constriction of the blue region in Fig. 6.6. This indicates a reduction in D_{it}, which is directly proportional to the magnitude of conductance peaks, with decreasing temperature.

FLE is quantitatively defined as the derivative of surface FL position $E_f(V_G)$ or band bending at the semiconductor surface $\varphi_s(V_G)$ with respect to gate bias V_G, and was calculated within the depletion region using the relation [21]:

$$FLE = \ln\frac{f_2}{f_1}\frac{kT/q}{V_1 - V_2}\ (\%)\ ,$$

where f_1 and f_2 are frequencies at which the G_p/ω conductance contours peak under gate bias V_1 and V_2, respectively, k is the Boltzmann constant, T is temperature, and q is the elementary charge. The frequency at which the conductance peak occurs is associated with the trap energy

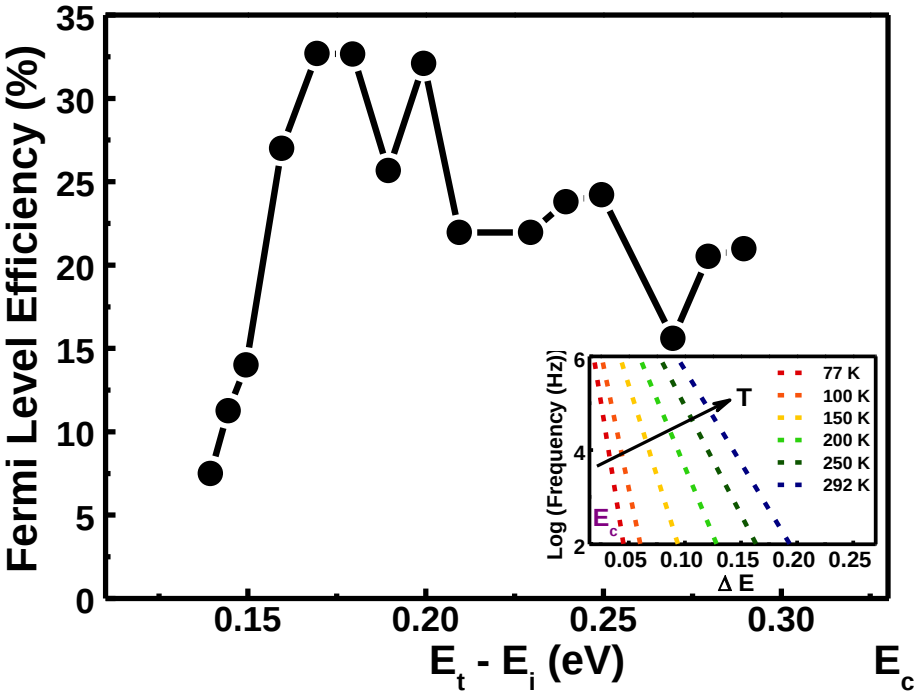

Figure 6.7: FLE as a function of energy of the Ge-*on*-Si MOS capacitor showing a decline in FLE close to the midgap. Inset shows Ge bandgap energy ranges accessible at various measurement temperatures (77 K- 292 K) for frequencies from 100 Hz to 1 MHz.

within Ge bandgap, and consequently with FLE using the characteristic trapping time equation [15]:

$$\tau_n = \frac{1}{2\pi f} = \frac{\exp(\Delta E/_{kT})}{\sigma_n v_{th} N_c}$$

where τ_n is the characteristic trapping time constant for electrons, f is the measurement frequency, σ_n is the trap state capture cross section, ΔE is the energy level of the trap state from the conduction band edge, v_{th} is the thermal velocity of electrons, N_c is the density of states in the conduction band of Ge, k is the Boltzmann's constant, and T is temperature. σ_n was assumed to be a constant value [22] of 10^{-16}cm^{-2} for Ge MOS capacitors [23]. By using the characteristic trapping time equation, FLE is plotted as a function of trap energy E_t away from midgap E_i, in Fig. 6.7. A peak FLE of 32.7% was extracted about 0.17 eV away from the midgap (E_i) indicating good FL modulation with gate biasing (V_G), but declined sharply close to the midgap. This behaviour indicates an increased density of interface states close to the mid bandgap region, which is corroborated later with the extracted D_{it} distribution. Conductance contours extracted from G-V measurements performed at temperatures ranging from 77 K to 292 K were utilized in the calculation of FLE, as each temperature allows the sampling of a limited region of the Ge bandgap, indicated in the inset of Fig. 6.7.

Fig. 6.8 shows the extracted D_{it} as a function of energy within the bandgap for representative Ge MOS-Cs on Si. The variable temperature measurement scheme (292 K to 77 K) allows for a more accurate extraction of D_{it} due to the suppression of the weak inversion response observed in low bandgap materials. Additionally, the lower temperatures (and higher frequencies) allow for the extraction of D_{it} closer to the band edge. D_{it} was calculated using the conductance method (accounting for surface potential) [15,24] following:

$$D_{it} = \left(\frac{G_p}{\omega}\right)_{max} [f_D\ (\sigma_S)\ qA]^{-1}\ ,$$

where $(G_p/\omega)_{max}$ is the maximum parallel conductance G_p normalized over angular frequency ω, q is the electric charge, $f_D(\sigma_s)$ is the universal function of standard deviation for band bending σ_s, and A is the capacitor area. For low bandgap materials, D_{it} values extracted from room temperature C-V measurements are overestimated due to the temperature-dependent supply of minority carriers to the inversion layer, which, in turn, contributes to higher conductance

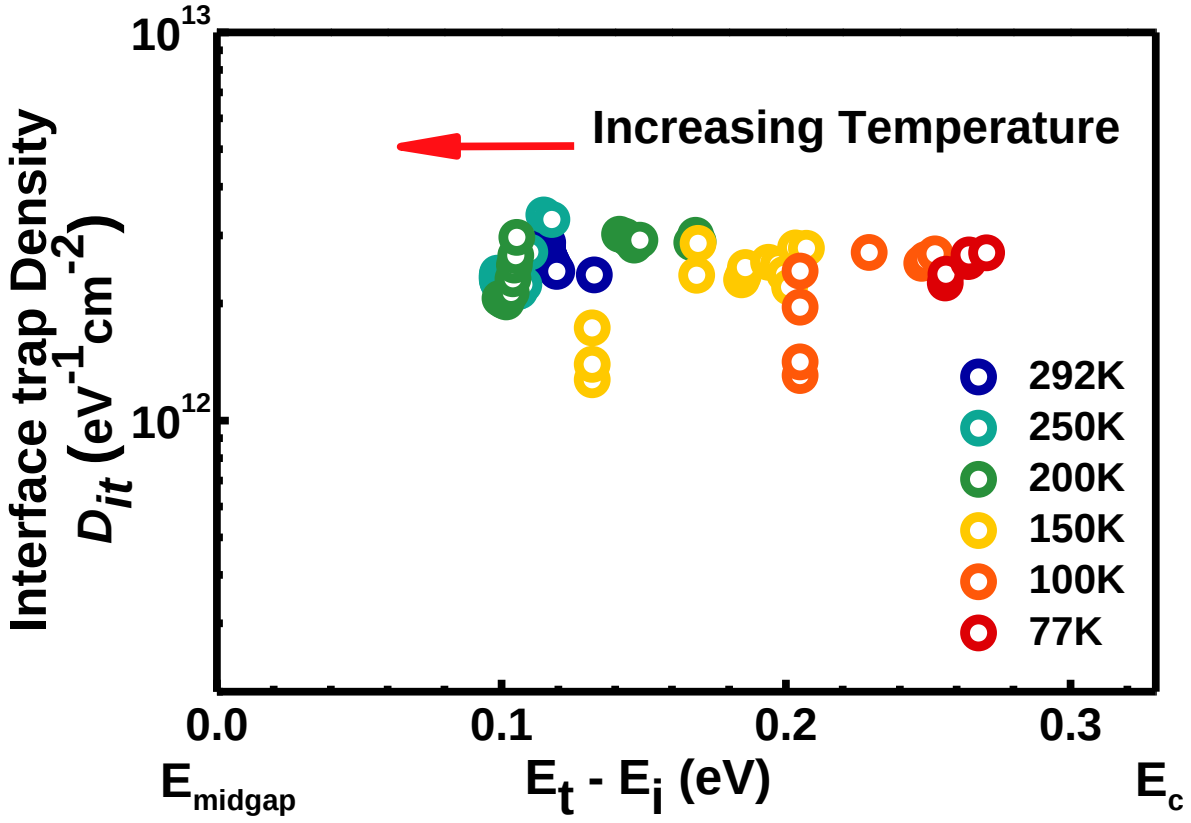

Figure 6.8: Extracted D_{it} values at different temperatures plotted with trap energy level from midgap for Ge-*on*-Si MOS capacitor.

[22,23]. In this work, a peak D_{it} of 3.38x10^{12} cm^{-2} eV^{-1} was observed approximately 0.115 eV away from the midgap, E_i, whereas a minimum D_{it} of 1.27x10^{12} cm^{-2} eV^{-1} was observed approximately 0.13 eV away from E_i. We observe a denser distribution of interface states closer to the mid bandgap region, reflected by the lower FLE in this energy range discussed earlier. These obtained D_{it} values, an important parameter for transistor performance, are later benchmarked against previously published D_{it} values for various Ge MOS devices.

6.3. Ge-*on*-Si Deep-Level Trapping Characteristics:

Previously, we demonstrated that although a dense network of dislocations running through the Ge film is observed *via* TEM, ionized impurity scattering remains the dominant scattering mechanism for large epilayer doping concentrations (~10^{18} cm^{-3}). Moreover, despite AFM analysis revealing a smooth surface morphology with low *rms* roughness, it is imperative to investigate the ability of threading dislocations to reach the epilayer surface, thereby acting as charge trapping centers and inhibiting the inversion response of the MOS structure. Deep level transient spectroscopy (DLTS) is a powerful junction capacitance tool for space-charge based devices, frequently used to study depth, type (acceptor or donor), density, and activation energy of electrically active trap centers within a semiconductor. Fig. 6.9 shows the DLTS response for the Ge-*on*-Si MOS structures for three different voltage steps with a long filling pulse duration (1 ms) to ensure that the traps are completely filled. DLTS measurements were

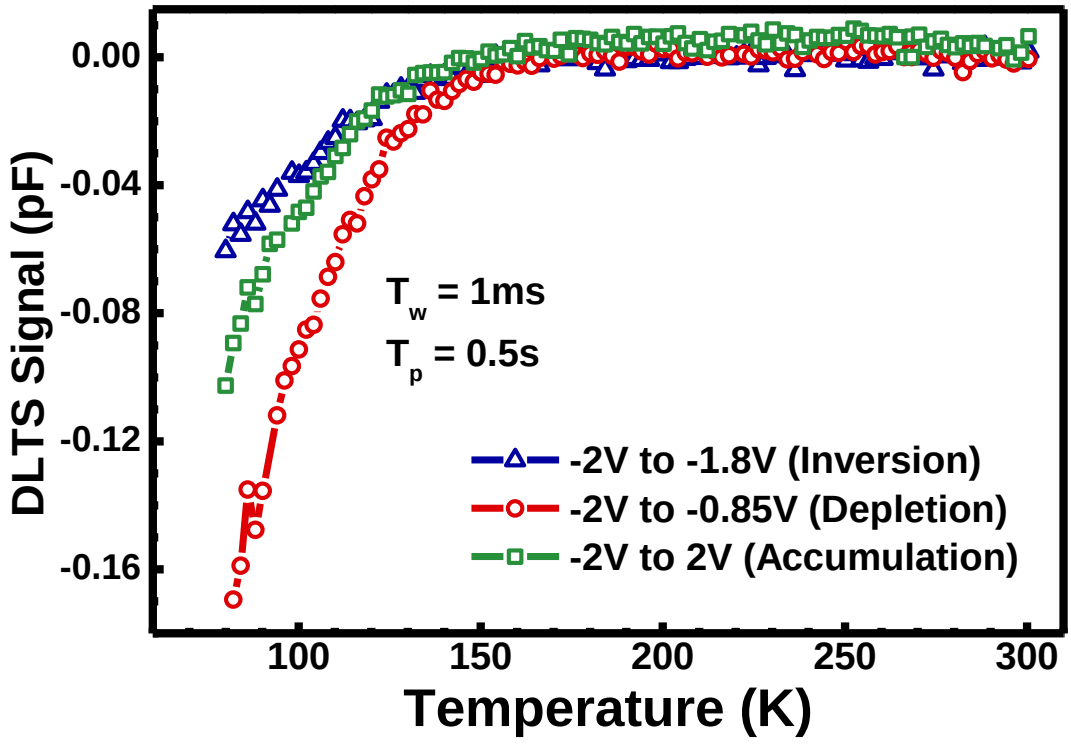

Figure 6.9: DLTS spectra taken from a representative Ge-*on*-Si MOS device for three voltage steps at emission rate of 3000 sec^{-1}

performed over a temperature range of 80 K - 300 K, and curves represented in Figure 5.10 are for an emission rate of 3000 sec^{-1}. The quiescent reverse bias pulse is -2 V (V_R) while the filling pulse (V_{FILL}) biases the capacitor in accumulation (2 V), depletion (-0.85 V) and inversion (-1.8 V). All DLTS spectra are observed to be dominated by a peak at 77 K, conceivably induced by D_{it} but free of bulk trap related peaks. The absence of measured trap levels in this temperature range (80 K to 300 K) demonstrates that, if in existence, the density of electrically active bulk traps is much lower than the interface trap density found by the previously shown CV methods, and these trap centers can be sensed at much lower temperatures, beyond the scope of this work.

6.4. Ge-*on*-Si MOS Capacitor D_{it} Benchmarking

Interface trap density, a key metric in MOS device performance, has been previously shown to have a direct correlation with threading dislocation density (*TDD*). Moreover, it has been

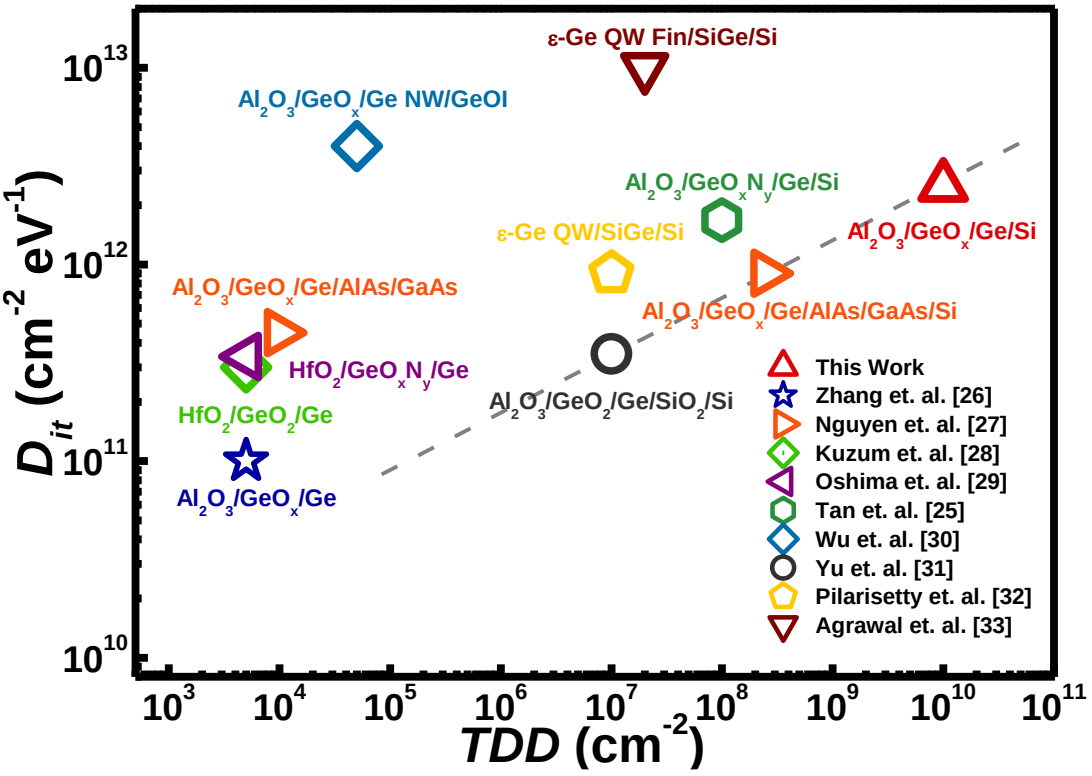

Figure 6.10: Benchmarking of obtained D_{it} to that previously reported for various Ge MOS devices as a function of *TDD*.

reported that both D_{it} and *TDD* were directly reduced *via* high-temperature thermal cycle annealing [25]. Fig. 6.10 shows a collection of room temperature D_{it} values measured for Ge MOS devices as a function of *TDD*, including the work reported herein. The previously published data use a variety of gate oxides and substrates, which could affect both the reported D_{it} and *TDD* values [25-33]. Hence, the device structure is indicated alongside each data point. An interesting pattern emerges for Ge devices on Si using different epitaxial integration schemes and an Al_2O_3/GeO_x gate stack: an almost linear increase in D_{it} with increasing *TDD*. This suggests that reducing the dislocation density in the Ge/Si stack will directly benefit the oxide-semiconductor heterointerface quality of fabricated MOS devices. Bulk Ge devices can be observed to benefit from the lowest D_{it} due to the absence of lattice mismatch-induced dislocations propagating through to the inversion surface. Lower interface states within bandgap will also help reduce surface recombination velocity in solar cells employing this heterostructure as active junction. Furthermore, from Fig. 6.10, a representative D_{it} value for Ge-*on*-Si MOS-Cs studied in this work can be found to be on par with that from other Ge devices integrated on Si *via* buffer techniques [27,32,33] or insulator layers [30].

In this *Chapter*, we observe that the high threading dislocation density reported in *Chapter 5* does not affect carrier transport in Ge epilayer. We also observe anomalous inversion behaviour of Ge-*on*-Si MOS-Cs although DLTS measurements down to 80 K do not detect electrically active traps in the semiconductor. The benchmarking of Ge-*on*-Si D_{it} values show potential of the heterostructure in development of field effect transistors. Consequently, this comprehensive study of the structural and electrical properties of directly grown epitaxial Ge-*on*-Si provides a pathway for the development of Ge-based electronic, optoelectronic, and photovoltaic devices on Si. The understanding of this heterostructure allows us to optimize the Ge epilayer to develop high efficiency GaAs solar cells on Si with a thin Ge intermediate buffer layer. *Chapter*

7 summarizes the results obtained in this research and various approaches to take this work further.

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Chapter 7

Conclusion and Future Prospects

7.1. Summary

The objective of this thesis was to investigate the performance of GaAs solar cells integrated on Si using a thin Ge buffer layer. In this pursuit, the structural, electrical and interfacial properties of the Ge-*on*-Si heterostructure were studied to analyze the limitations of this direct integration approach. This *Chapter* summarizes the findings and future prospects of this work.

A novel design for monolithically integrated of GaAs solar cells on Si utilizing an intermediate Ge layer was demonstrated, where the Ge epilayer can serve both as a buffer or an active layer to realize a hybrid Ge-Si bottom sub-cell. Introduction of this group IV epilayer facilitated a thin buffer system to mitigate mismatch induced defects within the buffer layer and produce ~10% conversion efficiency in subsequent active GaAs junction. Furthermore, our approach utilizing the MEE of polar III-V semiconductors on offcut Si substrates resolves two fundamental challenges of surface roughness and inverse domain boundary formation in these solar cells. The GaAs cells grown on Ge-*on*-Si platform via a < 1 µm thin buffer showed comparable performance with other GaAs junctions grown on Si with > 2 µm thick buffer

layers. To enable higher efficiency of active junctions on the Ge-*on*-Si integration approach, we studied the Ge-*on*-Si heterostructure to probe the structural and electrical properties of this buffer.

High-quality epitaxial Ge was grown on Si substrate via solid-source MBE. The crystallinity, surface morphology, epitaxial Ge relaxation state, and optically excited photoemission were investigated in order to evaluate the material properties of the thin 135 nm Ge epilayer on Si. Atomic force microscopy revealed a smooth surface morphology and demonstrated a surface roughness of ~2 nm. Relaxation in the Ge epilayer was found to occur via defect formation as well as the formation of Lomer 90˚ misfit dislocations at the Ge/Si heterointerface. X-ray diffraction analysis confirmed the presence of ~1% residual tensile stress in the as-grown Ge epilayer, which was further corroborated by micro-Raman spectroscopy. The majority carrier mobility and density were measured as a function of temperature and modelled in accordance with different scattering mechanisms in Ge. Ionized impurity scattering was found to limit carrier mobility in the unintentionally doped n-type Ge layer. Further assessment of the epitaxial Ge-on-Si thin-film was made by analyzing the MOS behavior of fabricated p-MOS capacitors, yielding interface and oxide trap densities in the epitaxial Ge-on-Si MOS structure. A peak FLE of 32.7% was extracted between the midgap and conduction band edge in Ge, corresponding to the low D_{it} value of 1.3×10^{12} cm^{-2} eV^{-1}. Additionally, deep-level transient spectroscopy was used to independently probe trap levels close to the Al_2O_3/Ge heterointerface, but no bulk trap levels were detected. Finally, the extracted D_{it} values were benchmarked against previously reported D_{it} data for Ge MOS devices as a function of threading dislocation density within the Ge layer. The results obtained in this work were found to be comparable with other Ge MOS devices integrated on Si via alternative buffer schemes.

Thus, this research demonstrates the feasibility of the Ge/Si material system for applications in low power, high-performance CMOS logic. This virtual "Ge-*on*-Si" platform, upon optimization to minimize threading dislocations from the lattice mismatched interface, indicates a promising future for monolithically integrated, low-cost and high-efficiency III-V-on-Si photovoltaics.

7.2. Avenues for Future Research

In order to leverage the research results discussed above and fully exploit the advantages of Ge/Si-based electronic and photovoltaic devices, additional research must be done in the following areas:

(1) In *Chapter 5* we observe from PV-TEM that the Ge epilayer has a TDD of 10^{10} cm^{-3} which is detrimental to solar cell performance, and could be the root of anomalous inversion behaviour at low temperature in Ge-on-Si MOS devices. The dislocation density minimization in the Ge thin film needs to be addressed. Several annealing schemes during and after Ge growth including thermal cycle annealing, pulsed laser annealing, excimer laser annealing etc. can be explored for this purpose. Solar cells can be grown on these annealed buffer structures and their performance evaluated against presented research.

(2) In *Chapter 6,* we observe high unintentional doping in Ge epilayer, which limits carrier mobility and shifts flatband voltage in the MOS Capacitors. Higher carrier mobility is one of the driving factors for using Ge in electronic devices but ionized impurity scattering limits this advantage. The high V_{FB} is undesirable as it makes it more difficult for the gate metal to invert the channel by requiring increased gate voltage to deplete the extra charges because of the high doping. Reduced carrier scattering is also

desirable in solar cells. Hence, Ge epilayers with much smaller doping concentration must be investigated for MOS devices and solar cells on Si.

(3) Another promising approach that can be pursued for integrating GaAs solar cells on Si via Ge buffer is the introduction of thin AlAs/GaAs underneath the Ge virtual substrate. Proof-of-concept composite Ge/AlAs/GaAs dislocation filtering buffers on Si demonstrate reduction in threading dislocation density by three orders, compared to direct Ge on Si. The thin and semi-transparent AlAs/GaAs buffer also allows for an active Si subcell. Moreover, there is potential of leveraging AlAs buffer layer as a sacrificial layer to facilitate epitaxial lift-off of III-V cells from Si substrate, which could substantially lower the burden on number of reclaimed substrate reuses (often requires CMP) and make this technology commercially attractive.

(4) Further *EOT* scaling and reduction of D_{it} will be necessary to exploit the potential of Ge as an alternative material to Si, thereby driving device current required for high-performance electronics. To help scale *EOT*, the implementation of high-κ gate dielectrics such as HfO_2 will be necessary. Implementation of plasma oxidation for a relatively thick layer of HfO_2 to reduce gate leakage, but the usage of very thin Al_2O_3 and GeO_x to maintain a competitive *EOT*, may be a possible solution to both scale EOT as well as demonstrate low D_{it} values. Low D_{it} values will aid in further Fermi-level unpinning, and allow for better tunability of V_{TH} using different work function metals.

(5) The root cause of the anomalous inversion behavior observed in MOS-Cs implementing Ge-*on*-Si heterostructure would need to be analyzed. As DLTS measurement at 80 K and above could not provide results of consequence, lower temperature DLTS measurements should be performed to detect extremely shallow traps in the bulk semiconductor.