An Investigation of Fundamental Frequency Limitations for HF/VHF Power Conversion

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Abstract

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The volume reduction in power converters over the past several decades can chiefly be attributed to increases in switching frequency. It is to be expected that the trends towards miniaturization will maintain steady pressure to keep this pace of increasing switching frequencies of power converters. However certain fundamental limits in high frequency power conversion are being reached as frequencies are being pushed deeper into the megahertz range, inhibiting substantial further increases.

The work reported in this dissertation is intended to systematically investigate the fundamental frequency limitations, identify some of the solutions for HF/VHF power conversion and to provide guidelines and tools to optimize the performance of power converters by maximizing frequency.

A number of multi-megahertz power converters are examined to evaluate the present status and future trend of HF/VHF power conversion. An interesting trend between power level and frequency is observed. A general limitation about the power level and frequency, independent of design details, is derived from the physics of the semiconductor devices, which determines the upper bound of the power levels as frequency increases.

A 250 MHz DC-DC power converter (derived from the Class E power amplifier) is analyzed and demonstrated with discrete components, which again verifies the trend between power level and frequency. The power losses in the semiconductor devices are discussed, and optimization criteria for minimizing the power losses of the devices, are discussed. By relating the power losses to the semiconductor materials' properties, a

methodology for selecting proper materials is identified for high frequency and high efficiency power conversion.

The frequency scaling effects of passive components, still dominating the volume of the modern power converter, is analyzed. A generic multi-disciplinary methodology is developed to analyze and maximize frequency and performance of passive components in terms of power density and efficiency. It is demonstrated how the optimum frequency can be identified, and how power conversion efficiency deteriorates beyond this optimum under a fixed maximum temperature.

Power loss measurement is becoming more challenging as higher frequency and higher efficiency power conversion. To achieve an accurate power loss measurement in a high frequency, high efficiency power electronics system or component, limitations of electrical measurement are identified, and various calorimetric methods are surveyed. Calorimetric methods are more accurate due to the direct heat loss measurement. An advanced calorimetric system is proposed, analyzed, and tested, demonstrating about 5% error in total losses up to 25W.

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To my father Bingyan & mother Lamei

and

My wife Xiaoyan & sons

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Chapter 1 Introduction

1.1. Background

Two of the most important performance criteria accompanying the application-driven trends in DC-DC power convertsion today are power density and efficiency. Higher frequencies and higher levels of integration are necessary to increase power density. It is predicted that power densities of about 20 W/cm^3 to 30 W/cm^3 will appear around 2015 and switching frequencies 5 to 10 times higher than those of today are necessary to achieve these goals, according to the survey in [6].

The rationale behind pushing power converter switching frequencies has historically been connected to the desire to reduce the volumes of the electromagnetic passive components, i.e. transformers, inductors and capacitors. An evolution of modular telecommunications power conversion units over a ten-year period is shown in Fig. 1.1 [2]. During that period the switching frequencies have gradually risen from the 75-kHz range to the 1-MHz range, which resulted in substantially reduced physical sizes of passive components.

In principle, a higher frequency means that the circuit needs to process a proportionally smaller amount of energy during each cycle for the same amount of power. The sizes of energy storage and transfer components such as filters, resonant tanks, AC-decoupling capacitors, snubbers, power transfer transformers, depending to some degree on the frequency operation, will scale down as the frequency increases. There are several exceptions to this rule, for instance the presence of DC or low frequency harmonics (i.e. a boost inductor with a large DC bias), or other limits on dimensional downscaling, such as voltage isolation thicknesses and safety requirements, (i.e. transformers having HV windings), turns and turns-ratio trade-offs, required cooling surfaces, mechanical or packaging limits, among others.

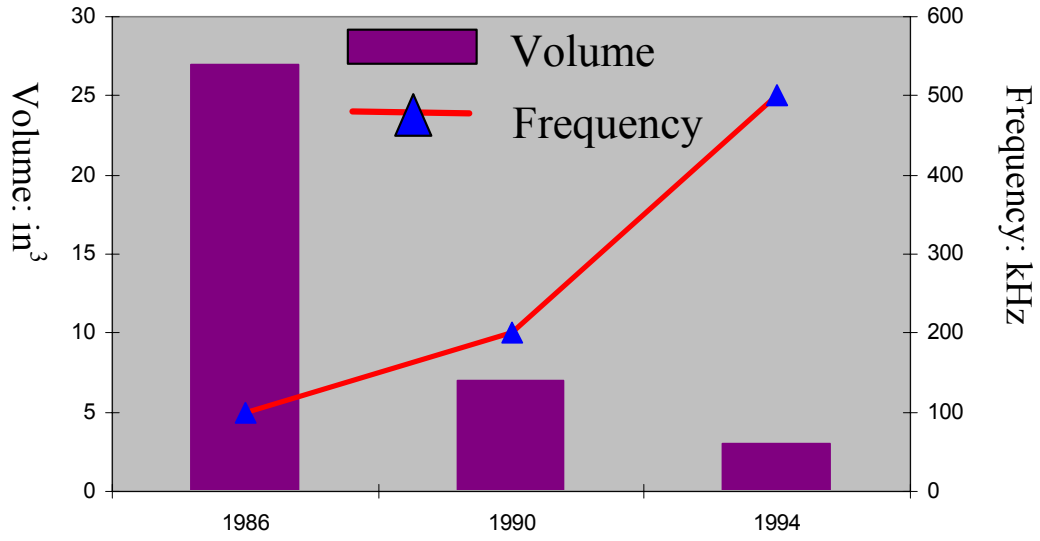


Fig. 1.1 Size evolution of modular telecom power conversion units [2].

Today the power densities of DC-DC power converters are being driven higher by the application demands more than ever. It is unlikely that demands for smaller volumes, squeezed into lower profiles over smaller circuit real-estate, with better performance, lower cost and, above all, higher efficiencies will relax anytime soon. Over the past several decades, raised frequency has been the dominant factor that enabled dramatic power density increases [1][2]. It is to be expected that these trends towards miniaturization and higher levels of integration will also maintain steady pressure to keep this pace of increasing switching frequencies of power converters.

1.2. Limitations of HF/VHF Power Conversion

1.2.1. Introduction

Power converters are moving towards much higher power densities and lower profile to accommodate the available real-estate, volume and profile requirements and cost factors while improving or maintaining efficiency. And more recently there has been more demand for power converters to provide greatly improved transient response to

meet the needs of fast switching loads. All these present more and more stringent challenges to power electronics engineers, though a series of improvements in technology with circuits, materials, packaging and switching frequency have already led to unprecedented gains in power densities, efficiency, transient response and reliability of power converters over last decades [1].

1.2.2. Monolithic Integration and Converters-On-a-Chip

The continued miniaturization of power converters by pushing switching frequencies up to multi-MHz (even up to hundreds of MHz) ranges, could eventually lead to the ultimate realization of on-chip power conversion. The implementation of power converter-on-chip may be required with functional integration of the devices, controls, magnetics and capacitors. This represents the key research challenge for integration into chip scale package, which will result in the actual mixing integration of analog, digital, and RF or power circuitry on the same packaging structure. There are several advantages to VHF power conversion as described below:

- ✓ Firstly, a miniaturized power converter can be easily placed closer to the load to reduce voltage drops due to interconnect resistances and inductances. This can also facilitate the power requirements of high current, rapidly changing load demanded by the microprocessors and new generation ICs in the future-computer and in telecom applications.

- ✓ Secondly, higher operation frequency of the monolithic power converter can improve the transient response, which is especially beneficial to the voltage regulator module in the microprocessor. Note that today, the push for higher frequencies is not only from the standpoint of reducing size, but also for improvements in the transient response. In the VRM application, a moderate compromise of efficiency seems to be acceptable if transient response can be improved sufficiently [1].

- ✓ Thirdly, a higher operation frequency facilitates tighter voltage regulation required in modern microprocessors and new generation ICs with smaller filters.

- ✓ Fourthly, monolithic power converters can easily be distributed all across the system to supply different loads, as opposed to having external power converters [4]. This enables another level of single-chip and on-chip power conversion. Power supplied from a board-mounted module or regulator module can be further broken down into smaller chip-like solutions to optimize the power management. For applications such as mobile phones, this can be important for various voltage levels required within the chip [4].

- ✓ Finally, minimization of the areas occupied by fully integrated power converters is critical in ultimately reducing the production cost.

1.2.3. Modeling and Design

Improvements in converter performances, size, weight and cost along with the increasing switching frequency have been achieved mainly through the technological advances and improvements in devices, materials, components and circuit designs, packaging techniques, and better thermal management. Therefore the efforts to achieve higher power density while maintaining or improving efficiency by means of pushing switching frequencies involves coupled multi-disciplinary issues in electrical, thermal, mechanical, and material properties of the components and packaging. However, it is also important to note that further advances are becoming more limited since certain fundamental limits in high frequency power conversion are being reached as the switching frequency is becoming higher and higher. These fundamental frequency limitations should be identified and understood for future high-frequency high-efficiency power conversion technologies.

1.2.4. Semiconductor Device Technologies

Every major increase in frequency would have been impossible without the advances in power semiconductor device technologies. From the original mercury arc devices to the present mainly silicon-based devices, the technology has seen a device volume reduction of 3~4 orders of magnitude – depending somewhat on power level [3]. Semiconductor devices capable of operating up to GHz range are already available thanks to the continued advancement of the technology. The evolution and future trend of power semiconductor devices are shown in Fig. 1.2. Accompanying the advances in semiconductor devices is the simultaneous increase of the switching frequencies [1]. Fig. 1.3 shows the progression of increases in switching frequencies concurrent with evolution of semiconductor technologies.

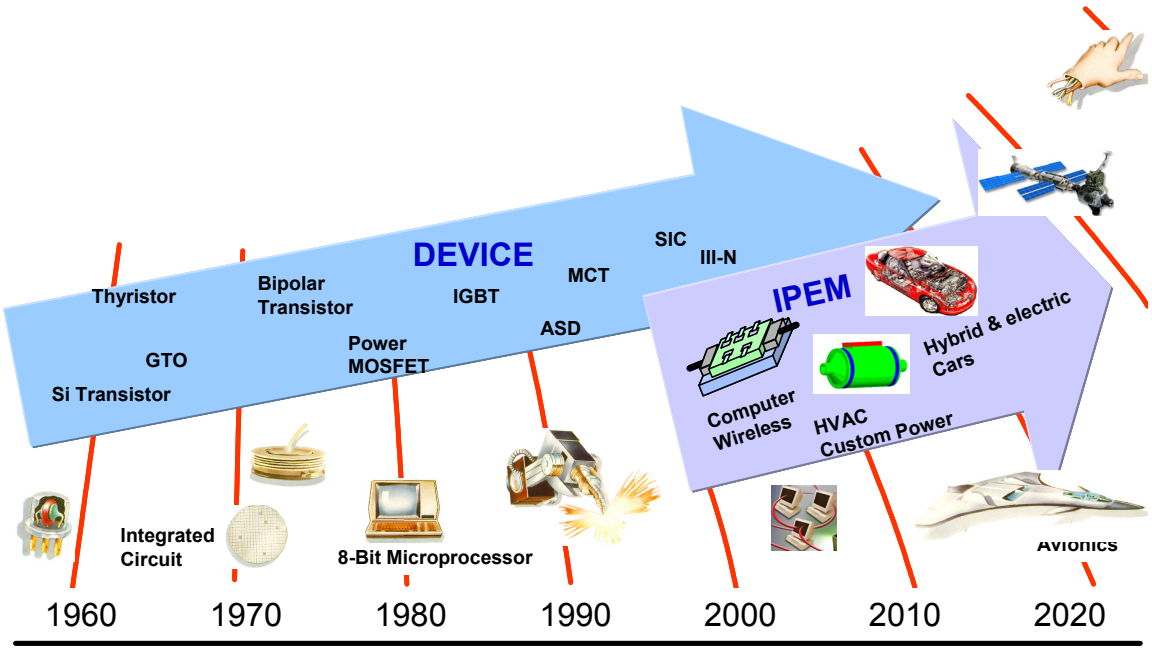


Fig. 1.2 Evolution of power semiconductor devices.

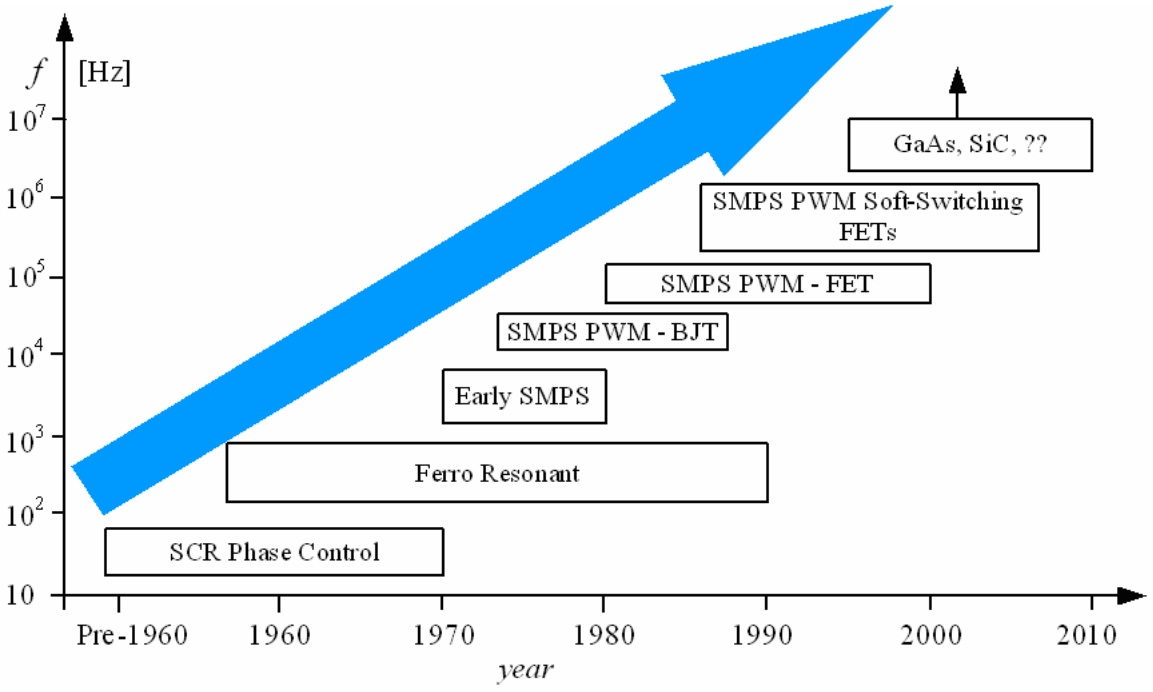


Fig. 1.3 Frequencies of different power supply technologies used in power conversion vs. time.

Notably, the introduction of the power MOSFETs in the early 1980's pushed switching frequencies into hundreds of kHz, then into MHz ranges with the applications of soft-switching techniques that later took advantage of the parasitic components in the circuitry [5] by means of functional integration. Modern device technologies are steadily bringing us closer to radio frequency power conversion at hundreds of MHz, even up to GHz, with continuous scaling, i.e., shrinking size (gate length), radical improvements in processing technology and development of new device structures (such as RF MOSFETs or MESFETs) [29].

Despite the fact that 3~4 orders of magnitude volume reduction have already been achieved in power semiconductor devices that can operate up to GHz frequencies under certain conditions, most power converters still operate well below the low megahertz range today and only an order of magnitude reduction in the overall volume has been achieved over the past 50 years [3]. This reflects some of the challenges peculiar to higher frequency power conversion. Clearly, there are limiting factors that seem to inhibit

further increases in switching frequencies. Exactly what they are and where the limit lies are not well understood, and not so clear.

1.2.5. Circuit Toplogies and Control Strategies for VHF Power Conversion

Load-Range Requirements

Firstly, power converters must operate efficiently over a wide load range from a variable input voltage. However, existing circuit topologies and control strategies commonly used at low frequencies become unsuitable when used at such high frequencies (tens of MHz ~ hundreds of MHz). The operation of conventional PWM DC-DC power converters becomes limited due to very short transition times. The resonant, soft-switching techniques are essential for operation in the HF/VHF ranges. Moreover, appreciable circuit parasitic values must be cleverly exploited to reduce power losses. This approach is effective for full load conditions, however, the circulating current losses are typically unacceptable in systems that must operate efficiently over a wide load range.

Output Regulation

Output regulation represents another challenge for VHF frequency operation. Controlling and regulation methods employed in conventional power converters are no longer suitable for VHF power converters. In order to ensure efficient operation and required regulation under wide load range and variable input, a new system structure is required to overcome these difficulties, such as the structure proposed in [18][19]. It is comprised of many cellular switching power converters to increase the total power level. The output regulation can be implemented by adjusting the number of the operating converter cells according to the variable load and input. In this way every operating cell in the structure will always operate at an optimum operating point so that maximum efficiency can be maintained even under light conditions. The control circuitry can be implemented in digital micro-controllers.

Converter Dynamics

Moreover, converter dynamics and control circuit implementation complexities escalate at higher switching frequencies. Therefore , innovative circuit topologies and control circuitries are needed to solve these problems and make power converters operate efficiently at HF/VHF.

1.2.6. Device Characteristics for future HF/VHF conversion technologies

Power semiconductor devices with high speed and low loss must be developed in order to achieve a dramatic increase in switching frequency and still allowing acceptable efficiencies. The frequency-dependent losses of the power devices in the power converters, including gate drive losses and switching losses, increase as functions of frequency. Switching loss is associated with switching when both voltage and current are changing and energy exchanges taking place with drain-source capacitances that are discharged during every cycle. To reduce this loss, soft-switching techniques are often employed. For example ZVS (zero-voltage-switching) can virtually eliminate the losses associated with the drain-to-source capacitance.

Gate drive loss is the result of energy transfer induced by charging and discharging the gate capacitance of power devices. Gate drive loss increases almost linearly with switching frequency. This loss often becomes a limiting factor for high frequency operation. To reduce the loss, the energy can be recovered and reused in subsequent cycles by employing resonant gate drivers. Thus, the desired characteristics of future devices for high switching frequency are smaller gate capacitances and resistances.

Conduction loss is proportional to the on-resistance of the devices. Lower on-resistance of the devices will result in lower conduction losses. However as frequency is pushed higher, the conventional power devices are approaching their performance limitations imposed by their material properties. The inherent design trade-off lowering ON-resistance AND reducing capacitance in a power device, should be optimized for high speed and high efficiency operation. The power-frequency products of

semiconductor devices also limit the achievable power densities. Thus a future HF/VHF power conversion technology will require further advances in the device technologies. Novel structure and wide band-gap semiconductor devices, such as silicon carbide and gallium nitride devices, as well as novel silicon devices like a super junction FETs, are under way for breaking through the device limitations [6] to achieve the low gate capacitances and resistances while maintaining reasonably low on-resistances.

1.2.7. Passive Components

Compared to the performance improvements in the power devices, it is clearly the inadequate performance of passive components where we must turn our attention to. In seeking equal or greater benefit by reducing volumes of passive components more commensurate with those of the power devices, radical increases in operating frequencies are required. Unfortunately, no major breakthroughs have been achieved in the passive materials for high frequency operation, and passive components still dominate the volumes of power converters.

Magnetic components

In the continued efforts to minimize power converter volume, the miniaturization of energy storage and transfer passive components is usually the most difficult obstacle, especially for magnetic components. At lower switching frequencies, the passive components dominate the volumes of power converters. The losses associated with capacitive components or magnetic components are small for low frequencies. But at higher frequencies, the losses become the most important consideration. For most ferrite materials, core losses increase dramatically with frequency in the megahertz range because the eddy current losses, hysteresis losses and HF copper losses increase with frequency. The rapid increases of core losses offset the volumetric utilization and inhibit the increase of switching frequency due to efficiency or thermal constraints. The permeabilities of ferrites also depend on frequency. As a result, higher switching frequencies do not always lead to smaller sizes of magnetic components.

However, the trend to smaller magnetic components at higher frequencies has driven many new research efforts to develop new magnetic materials and fabrication techniques [7][8] to optimize the high frequency performance. The thin-film or micro-fabricated magnetic components usually operate below 10 MHz at present. But the permalloy, ferrite polymer compounds and other materials appear to be promising for higher frequency operation [9]. Most of the thin-film magnetic materials to date have been restricted to low power conversion and limited current handling capability. This suggests that in order to increase current handling capability and power level, magnetic materials with high resistivity, low coercivity, and high saturation magnetization are required along with the capability of being deposited in multi-layers. It is interesting to note that some soft magnetic materials with such features have been addressed in a 3.3- to 1.1-V, 7A dc-dc converter at frequencies beyond 10 MHz [10]. On the other hand, if the operation frequency of the power converter can be increased sufficiently, the magnetic components can be implemented without magnetic cores due to low inductance required. This provides an opportunity to integrate the magnetic components on silicon wafer, allowing further integration with power devices and control circuitry within a single silicon die. Silicon-integrated magnetics should achieve reasonable component size and quality-factor Q with some improved fabrication techniques such as micromachining techniques proposed in [11][12].

Therefore, in order to achieve dramatic reductions in magnetic components sizes, either new magnetic materials that do not suffer frequency-dependent loss limitation are required, or the operating frequencies of power converters must be sufficiently high so that air-core magnetics can be employed effectively.

Capacitive components

Compared to the semiconductor devices and the magnetics, capacitor technologies are already suitable for frequencies of 10 MHz and beyond through advanced manufacturing techniques and new materials. This has primarily been stimulated by the improvements in ceramic capacitors with high values of capacitance per unit volume, ultra-low ESL and ESR. Ceramics can potentially take the lead in this regard, particularly

with the recent advent of new materials and multilayer ceramic capacitors, which have demonstrated production capacitance scalability (> 10 μF). Capacitor development for the future will focus on smaller grain size of dielectrics to allow thinner dielectric processing. A new evolving "nanostructure multilayer" capacitor technology mentioned in [13], getting inorganic high dielectric constant coatings built up by interleaving electrodes in a multilayer construction, shows a great potential for HF/VHF power conversion. Typical examples of such materials are $ZrTiO_3$, TiO_2 and $CaTiO_3$, which are 0.1 – 10 μm thick and contain 100 – 10000 layers.

Ultimately, the dielectric materials are also limited due to their frequency-dependent properties, i.e., the dielectric constant, a complex quantity, that changes with frequency. A higher switching frequency leads to the increased losses including dielectric loss and Ohmic loss, and derated performance of a capacitor. In order to achieve higher frequency operation with higher efficiencies, better materials are required to reduce capacitor dissipation factor by 1/3 to 1/10 and increase capacitor energy and power densities 2 to 10 times those available today [13].

1.2.8. Packaging and Integration Techniques

High frequency conduction losses [14] and increased contact resistances in conductors or interconnections, due to the skin effects, proximity effects or the distributed effects at HF/VHF, become more pronounced, resulting in distorted performances and reduced efficiency. Radiation leakage and losses become more severe, thermal noise must be accounted for, and new scaling laws come into effect. Therefore, higher levels of integration and packaging techniques are critical to minimize these adverse effects physically. Merely extending conventional packaging could bring about modest improvements in electromagnetic characteristics, enabling higher frequencies as a result of better discrete layout, tighter packing of components, smaller parasitic planning of interconnections, better heat-sinking, lower profile and modular construction. But it is not enough to achieve the order of magnitude improvement that is really needed [3]. A more aggressive packaging approach is necessary to develop higher levels of integration.

A number of technologies, such as the Metal Post Parallel Plate Structure (MPIPPS), Buried Power Technology, Power Overlay Technology, and Flip Chip on Flex Technology, have been developed to allow lower inductance interconnection structures, better thermal management and flat integrated packages. To be one of the promising candidates in this field, it is essential to develop a 3D integrated system approach in the form of a highly Integrated Power Electronics Modules to incorporate electromagnetic integration of passive components, non-wire-bond power stage integration, advanced materials and thermal management – and eventually advanced power semiconductor devices for the further development of power conversion.

1.2.9. Thermal Management

More advanced and more efficient thermal management will also be required to effectively remove the heat through smaller surface areas to satisfy the increasing demand for faster, smaller, lighter, cheaper and more reliable HF/VHF power converters. The average power densities and heat dissipation rates have increased nearly two-fold in the last decade. The common cooling techniques such as heat sink and heat pipe technologies will no longer be capable of meeting the thermal management demands of future systems. It is obvious that more aggressive thermal management techniques are required to handle the increased heat loads at this level of integration. There are many technologies emerging but the most promising in the near future are liquid cooling, refrigeration and spray cooling. Other technologies include embedded micro-heat pipes, micro- or mini-channel heat sinks, and micro-machined air-jet array impingement, among others [20], to name but a few.

1.2.10. Measurement Issues

The measurements of the electrical quantities are becoming more challenging with the power converters advancing into higher frequencies, higher efficiency, and smaller volume. For high frequency signal and highly distorted signals, conventional

measurement equipments are no longer suitable due to their limited bandwidth and dynamic frequency response limitations. The interferences from high dv/dt or di/dt signals, the intrusion of probes or oscilloscopes into the circuits, among others, all contribute to aberrations of the measurements. Among these, accurate power loss measurements are becoming increasingly difficult as frequency and efficiency are being pushed higher.

In summary, the implementation of HF/VHF power converters is limited by many coupled multi-disciplinary issues in electrical, mechanical, thermal, material properties. These fundamental frequency limitations include:

- Circuit topology and control strategy;
- Power semiconductor device technology;
- Energy storage and transfer capabilities of passive components;
- Packaging, interconnection, and integration techniques;
- Thermal management;
- Measurements.

1.3. Objective of this Study

The objective of this thesis is to systematically investigate the fundamental frequency limitations for HF/VHF power conversion technology. The main aim is to provide necessary tools for analysis and design towards optimizing power density and efficiency by maximizing frequency. The necessary guidelines will be provided to identify the fundamental reasons of the limitations. Since the investigation involves complex and coupled multi-disciplinary issues coupled in various ways, a good qualitative insight into the frequency scaling effects and the tradeoffs between different performance functions is indispensable in understanding the HF/VHF performances in order to optimize the design. The dissertation is arranged as follows:

1.3.1. Chapter 2: HF/VHF Power Conversion Technology Review and Discussion

In this chapter numerous multi-megahertz switching converters, that were demonstrated successfully in the literature, are reviewed, trends are recognized and some conclusions are drawn from these trends. The topologies and power conversion technologies suitable for high frequency operation (> 10 MHz) are described. The implementations and main features of these converters are summarized. In regards to the development of HF/VHF power conversion, the trade-offs between the power level and the operating frequency are identified and illustrated. A general relation about the power-frequency limit is derived from the physics of the semiconductor devices, which show how the ultimate limitations depend on the material properties of the semiconductor devices in the converters.

1.3.2. Chapter 3: Analysis and Design of RF Class E DC-DC Power Converter

In this chapter the DC-DC power converter derived from Class E power amplifier is analyzed. The operating principles and designs of this kind of converter are described in detail. The Class E DC-DC converter is a promising option for operating at radio frequencies and beyond due to its excellent soft switching characteristics. A prototype 250 MHz power converter is designed and implemented with discrete surface mount components along with the experiment results. A theoretical guideline is discussed about how to optimize the semiconductor devices to reduce power losses incurred in the device and improve the efficiency for HF/VHF power conversion. A criterrion for comparison, the product of on-resistance and input capacitance of device, is identified in terms of semiconductor material properties for high frequency and high efficiency power conversion.

1.3.3. Chapter 4: Fundamental Frequency Limitations of Passive Components for HF/VHF Power Conversion

The frequency scaling limitations of integrated passive components are discussed in this chapter. As mentioned earlier, increasing frequency has been the primary approach for reducing passive component volumes. It is also a well known fact that at some frequency no further advantage is obtained, and yet it is unclear where this 'optimum' frequency (or limit) lies. This chapter addresses this question. A methodology is developed to theoretically analyze the complex multi-disciplinary interplay of design parameters, to maximize frequency whilst optimizing performance of integrated passive components for power conversion in terms of efficiency and power density. Among others the materials, thermal management, packaging and in-circuits functions are considered. The performances of integrated planar magnetic components and capacitive components in terms of power density and power conversion efficiency are evaluated as a function of frequency scaling. The analysis demonstrate how the methodology can be used to identify the most optimum power conversion frequency for a given set of specifications, circuit function, selection of materials and packaging technology and limitations, and thermal constraints.

1.3.4. Chapter 5: Power Loss Measurement Techniques for HF/VHF power conversion Applications

Finally, measurement techniques are discussed for high frequency applications. Emphasis is placed on power loss measurement techniques, including electrical and thermal techniques, along with their advantages and disadvantages. The electrical power loss measurement techniques are limited by their large errors even with highly sophisticated digital equipment. In theory higher accuracy is possible by measuring loss directly. Calorimetric methods provide the means for measuring losses directly and consequently, it is considered to be the most promising method available for accurate power loss measurement. This method has the advantage of being able to measure the power losses under normal operating conditions and being independent of electrical

quantities of the device under test. A calorimeter suitable for accurate power loss measurement is proposed and described in this chapter. The measurement system is based on the principle of direct measurement of heat flux. It can implement temperature control and can measure heatsink-mounted components such as active IPEMs, passive IPEMs, and integrated magnetics. A prototype is built and the calibration result of this calorimeter demonstrated about 5% error in total losses.

Chapter 2 HF/VHF Power Conversion Technology Review and Discussion

2.1. Introduction

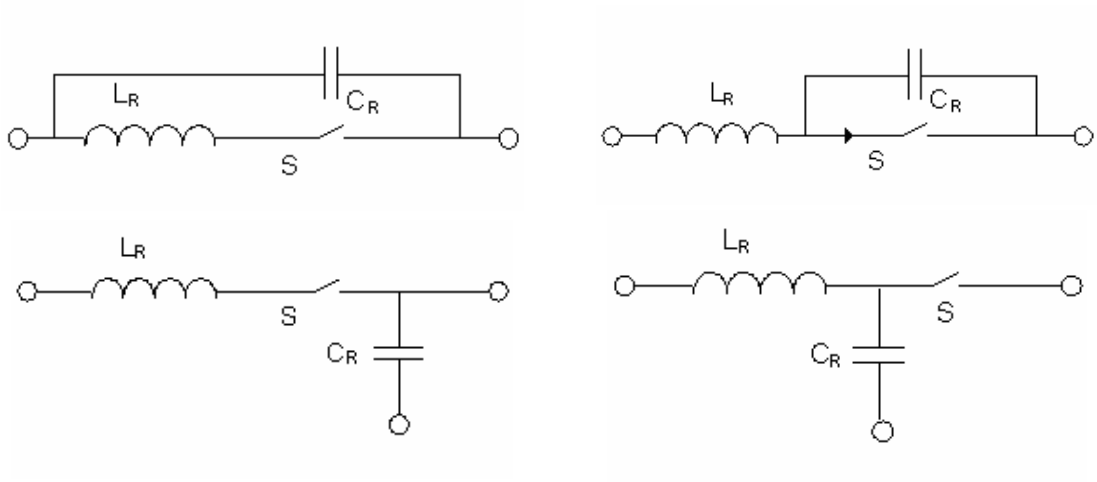
To examine how switching frequencies in power converters are being pushed higher and higher, some published literature that discuss power converters having switching frequencies of 10 MHz and beyond are reviewed in this chapter.

Since 1970's, there have been major efforts from researchers to achieve high power density and faster transient response of DC-DC converters by increasing switching frequency. High efficiency and high switching speed are of critical importance to achieve the design objectives in these high frequency DC-DC power converters. As a result new techniques and converter topologies have emerged to realize high frequency operation, such as ZCS and ZVS resonant switching techniques [30], and of RF Class E resonant converters [31][32]. The availability of devices and new VLSI processes have enabled DC-DC converters operating beyond 10 MHz [33][34][35]. Efforts to operate these circuits beyond 10 MHz have been plagued with a number of problems, limiting the overall conversion efficiency and power density of converters.

Basically, HF/VHF DC-DC power converters can be implemented in two ways. One is the improvement of conventional PWM converters such as Buck converters, Boost converters and Flyback converters. The other method is the introduction of new topologies and architectures such as Class E converters. These two kinds of methods are described below.

2.2. Resonant switching techniques in conventional converters

One of the fundamental limitations towards increasing the frequency of conventional PWM power converters is the presense of parasitic elements in the circuit. There are two ways to deal with this problem. The first is to minimize the parasitic elements in the circuit. However, it is impossible to reduce the parasitics beyond a minimum level, e.g. for offline converters [36]. Another approach is to use resonant switching techniques to employ the parasitics to the circuit's advantage and include the parasitics in the circuit design. Popular methods using this technique are zero-voltage switching (ZVS) and zero-current switching (ZCS). The basic structures of resonant switch are shown in Fig. 2.1.



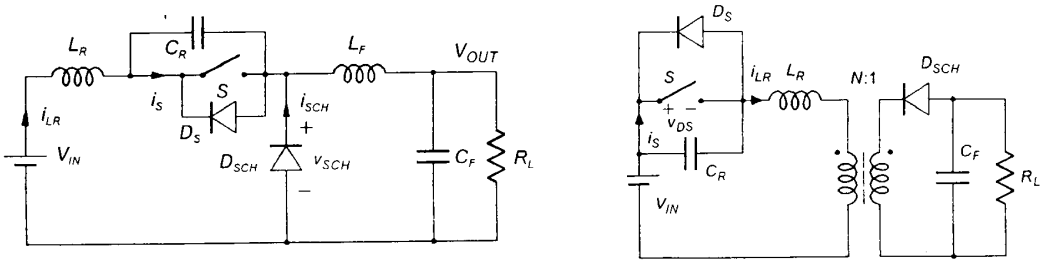
(a) Zero-current switching (b) Zero-voltage switching

Fig. 2.1 Basic structures for soft resonant switching

The essence of ZVS is to shape the drain-to-source voltage waveforms of devices so they become zero prior to turning on. The ZCS technique shapes the device's current waveform so that the device is turned off when its current is zero [30]. Thus the resonant switching techniques allow very low switching losses and permits efficient operation at increased frequencies. ZCS is somehow limited to the lower megahertz range since this

technique can not solve the problem of switching loss associated with capacitive discharge at turn-on [30].

There has ever been intensified efforts on resonant converters to operate in the 2 – 20 MHz range in the mid to late 1980's [1][37]. In [37] Buck and Flyback ZVS quasi-resonant converters (QRC's) were presented. The experimental results of Buck ZVS QRC (Fig. 2.2a) showed switching frequencies from 6.6 MHz at 25 W to 16.7 MHz at 2.5 W and 80% efficiency at full load. However, a high voltage stress in the order of 8 times the input voltage for a 7:1 load range, was applied to MOSFET. The experimental Flyback ZVS QRC in Fig. 2.2b operated from 3 MHz at 20 W with V_{in} = 45 V to 13 MHz at 5 W with V_{in} = 60 V, V_{out} = 5V. Efficiency of the converter was typically 70%.



(a) Buck ZVS QRC (b) Flyback ZVS QRC

Fig. 2.2 Basic circuit diagram of ZVS QRC in [37].

In summary, the ZVS technique is suitable for very high frequency operation. However high voltage stress made single-ended ZVS converters unsuitable for wide load range applications.

2.3. High speed switching devices in conventional Converters

Conventional MOSFET-based converters may operate at frequencies as high as 10 MHz by using novel switching techniques such as ZVS or ZCS. But increasing operating frequencies above 10 MHz for such converters necessitates new advanced power semiconductors with high speed and low losses. Incorporation of such new devices

into conventional power converters for high frequency operation has been successfully demonstrated in the literature as described below.

High speed GaAs vertical field-effect transistors (VFETs) with less than 2ns switching have been incorporated in 10 MHz, PWM Boost and Buck 5 W power converters that demonstrated good efficiency (>85%) and very high power densities (500 W/in^3) [33]. Benefits of GaAs VFETs over silicon MOSFETs include: 10-to-1 improvement in switching speeds, and reductions in specific resistances and device capacitances. GaAs VFET lacks the parasitic diode of a MOSFET, reducing reverse recovery losses. The two drawbacks of the device technology at present are its normally-on characteristics caused by depletion mode operation and technological immaturity.

In [38] a PWM boost converter with an operating frequency of 10 MHz was implemented with GaAs's HBT's in hybrid form for a portable wireless transmitter to meet the requirements of smaller size and higher bandwidth. Power efficiency at 1 W with 74% efficiency was reported in this literature.

Gallium Arsenide (GaAs) MESFET power switches like MESFET and Schottky barrier rectifiers applied in Buck [39], Boost [40], Cuk [43], Flyback [44] DC-DC converters have allowed switching frequencies up to 100 MHz, even up to 250 MHz [42]. The primary advantages for using GaAs over silicon are low ON resistance, low voltage, fast switching speed, and semi-insulating substrate [39]. This mainly comes from intrinsically higher electron mobility of GaAs (5000 cm^2/Vs for GaAs, 600 cm^2/Vs for silicon with 10^{17} cm^{-3} doping density) and higher energy bandgap. Since the on-resistance to input capacitance factor $R_{on}C_{iss}$ is inversely proportional to the electron mobility, GaAs switches are expected to provide much lower power losses than silicon switches [41].

A 40 MHz to 100 MHz step down 10 V to 5 V (8 V) converter using GaAs power MESFET was demonstrated with an output power of 2.6 Watts and power efficiency of 77% at 40 MHz in [39]. A prototype based on hybrid circuit technology was implemented on an alumna subtrate with 1 A – 15 V X-band power MESFET, an X-band

MESFET based gate driver, a 110 nH – HF ferrite based very low loss inductor and various DC decoupling chip capacitors. Experimental results of the converter are shown in Fig. 2.3. If a MESFET power transistor with 0.5 Ohm ON state resistance instead of 4 Ohm in the prototype was used, more than 85% efficiency could be achieved at 100 MHz.

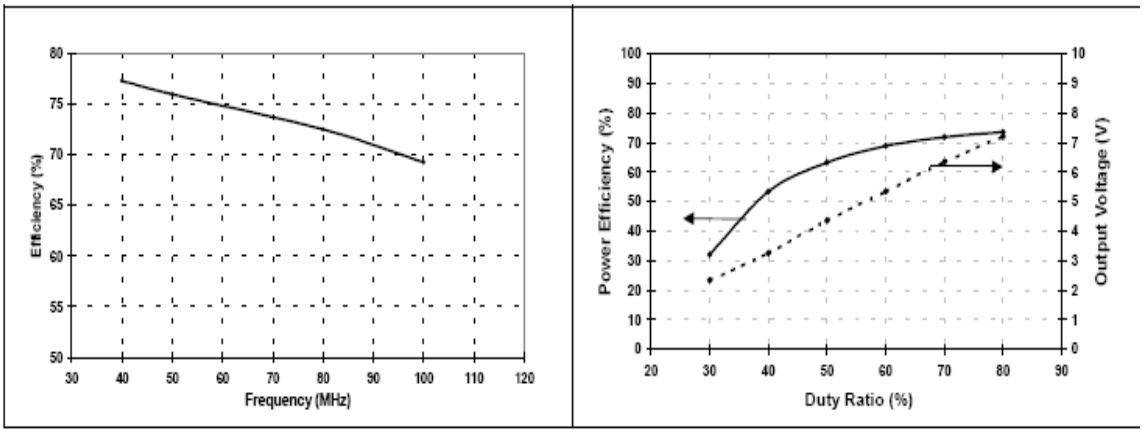


Fig. 2.3 Experimental results of Buck in [39]**.**

A GaAs-based 5 V/10 V – 2 W Boost converter operated at 100 MHz was presented in [40] with 69% efficiency with small passive components: a 23 nH planar inductor (4×4 mm^2) and a 47 nF surface mount capacitor (1×2 mm^2). The hybrid technology prototype Boost converter was assembled on a 10 mil Alumina substrate. A 0.7 μm technology 2 A-12 V commercial MESFET, a 150×150 μm 27 V Schottky rectifier and a gate driver were carefully mounted with very tight interconnection ribbons in order to avoid parasitic oscillations.

Two principal limitations of high switching frequencies (>20 MHz) DC-DC converters are: relatively small breakdown voltage of HF switches, and HF losses of passive components. Novel large gap III-V power devices such as heterojunction bipolar transistors (HBTs), high electron mobility transistors and the hetrojunction isolated gate FETs should be investigated for potential use. Concerning passive components, especially ferrite based inductors, the limitations are related to the limited cut-off frequency of UHF ferrite materials (generally < 300 MHz). It should be interesting to

investigate RF techniques by using Transmission Line based components like BALUNs in order to replace conventional inductors and transformers. Also a smart power monolithic technology, that involves the gate drivers and the power devices, would allow us to avoid the effect of the parasitic inductances and reduce the size of the circuit [41][43]. A more compact design should be possible by using MMIC technology.

A simplified comparative theory in [42] highlighted the intrinsic advantages of GaAs over conventional silicon devices for very high frequency applications. Taking into account the maturity and reliability, cut-off frequency of higher than 20 GHz, GaAs MESFET/HEMT devices constitute a real solution for converters operating up to hundreds of MHz like the modulated power supply RF amplifiers. The feasibility of ultrahigh frequency DC-DC converters using GaAs power switches opened new perspectives in the power electronics domain in terms of compact size and speed.

2.4. Monolithically integrated conventional power converters by VLSI

High switching frequency is the key design parameter that enables full integration of a high efficiency power converter. By evolving to higher switching frequencies, values of inductors and capacitors are reduced to values that are suitable for integration. Due to tight area constraints, integrated capacitors and inductors above certain values are not acceptable for integration. On the other hand, the VLSI process technology allows us to integrate both active and passive devices of power converters onto the same die. In a typical nonintegrated converter, significant energy is dissipated by the parasitic impedances of the interconnects among the nonintegrated devices (inductors, capacitors, power transistors, and PWM circuitry). An integrated converter on a chip can potentially lower the parasitic losses as the lengthes of interconnects between different components are reduced. Additional energy savings can be realized by utilizing advanced deep submicrometer fabrication technologies with lower parasitic impedances [46][47][48].

Full integration of power converters is challenging because monolithic magnetics technology can't provide high quality inductors. Integrated inductors usually have poor parasitic impedance characteristics: low Q-values and low self-resonant frequencies, which can degrade efficiency of power converters. Therefore new magnetic materials or improved fabrication techniques are required to achieve the desirable characteristics. New integrated microinductor technology using CoZrTa with relatively small parasitic impedances and higher cut-off frequencies (> 3GHz) has been reported in [52]. Therefore on-chip integration of active and passive components of power converters permits switching frequencies higher than typical switching frequencies found in conventional converters. Examples of on-chip integrated DC-DC power converters are illustrated below.

The SiGe BiCMOS process is well suited for portable wireless applications due to its significant advantages: high speed, low noise figure, excellent linearity, and less dependence of speed upon high field strength and supply voltage. It has been successfully applied in a DC-DC power converter for wireless applications. A DC-DC converter design for on-chip integration with a WCDMA power amplifier has been presented in [35] to increase transmitter efficiency and improve battery life. The synchronous rectifier (SR) Buck converter was implemented in IBM's 0.35 μm SiGe BiCMOS 6HP process. Simulation results show an average efficiency of 78.8% over power amplifier operating conditions and a peak efficiency of 86%. The converter was optimized for operation at 88.7 MHz. The inductor value (9.1 nH) is small enough to be integrated on-chip, however the series resistance of on-chip inductors (1 ~ 2 Ω) is too large for power conversion applications. Therefore output inductor and capacitor are implemented off-chip [35] in the converter.

Similarly a 100 MHz two-phase interleaved SR Buck converter was implemented by the use of 0.18 μm SiGe BiCMOS process for wireless applications, but with high quality integrated passive devices [45]. The inductor quality factor limits the efficiency of converter. The inductor quality factor is limited by metal line resistivity, capacitive

coupling to the substrate and magnetic coupling to the substrate. The metal line resistance is lowered by removing the first few internal turns of the spiral inductor, which do not contribute too much to the total inductance. By use of thick electroplated copper layer after the 5th layer of Cu metallization and far above the substrate, a high quality factor inductor was implemented [45].

On-die switching DC-DC converters can be fabricated in existing CMOS (80 nm – 180 nm) [47] [51] for future microprocessor power delivery. As pointed out in [51], increasing input voltage to VRM (voltage regulator module), and moving the VRM closer to the microprocessor by integrating it either in the package or the die itself alleviates some problems associated with low voltage, high current distribution networks. In fact, integrating the DC-DC converter onto the same die as a microprocessor can improve energy efficiency, enhance the quality of voltage regulation, and decrease the number of I/O pads dedicated for power delivery on the microprocessor die. Furthermore, reliability of voltage conversion circuitry can be enhanced, area can be reduced, and overall cost can be decreased by using an integrated circuit technology [46].

Comprehensive circuit models of the parasitic impedances of monolithic switching DC-DC converters were presented in [47][48] to analyze the frequency dependent efficiency characteristics of the Buck converter as switching frequency is increased to permit full integration. An optimum circuit configuration with maximized efficiency was derived from this model. The effects of scaling the active and passive devices and the related switching and conduction losses on the total power characteristics of a buck converter were examined. The independent variables of the proposed model in [47] are the switching frequency and inductor current ripple. An estimation of efficiency from the analytical model is within 2.4% of the simulation results at the target design point. An efficiency of 88.4% at switching frequency of 477 MHz was demonstrated by simulation for voltage conversion from 1.2 V – 0.9 V volts while supplying 9.5A current. The area occupied by the converter is 12.6 mm^2 assuming an 80 nm CMOS technology. By including gate voltages and tapering factors of MOSFETs as independent parameters in the model proposed in [48], estimation of efficiency is now within 0.3% of circuit

simulation. An efficiency of 84.1% at 102 MHz was achieved by simulation for voltage conversion from 1.8 V to 0.9 V assuming 0.18 μm CMOS technology.

In order to achieve the desirable efficiencies at such high frequencies, MOSFET power dissipation reduction techniques were applied to improve the efficiency based on the parasitic circuit models of the monolithic Buck converter (Fig. 2.4) in [47][48]and [51].

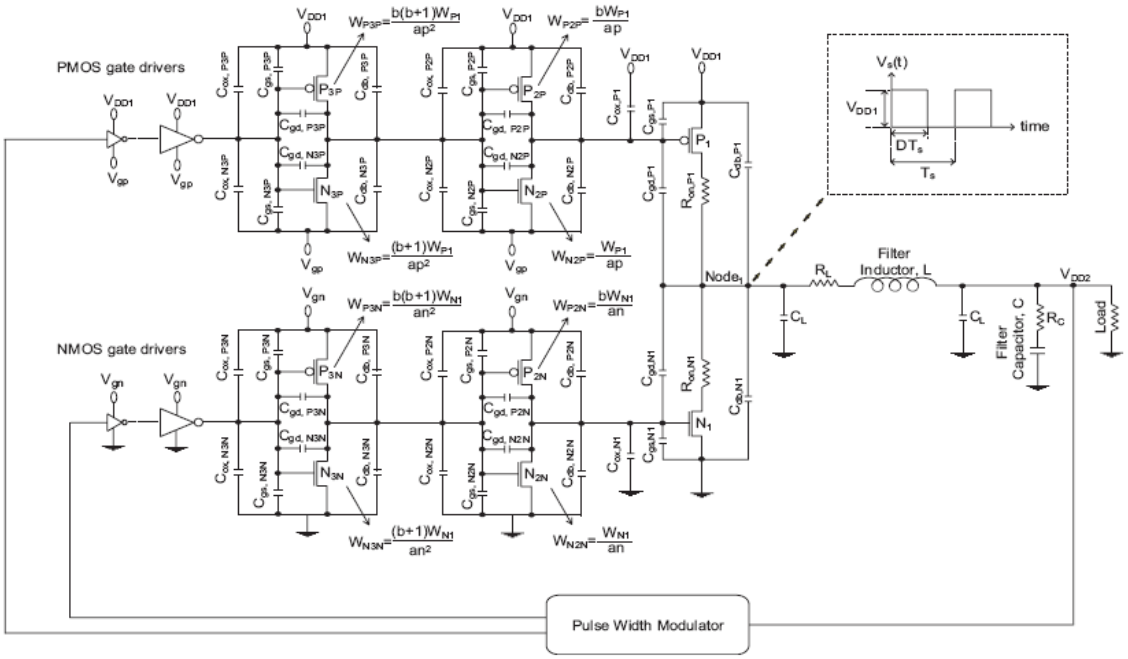


Fig. 2.4 Parasitic impedances and transistor geometric sizes of Buck converter.

Firstly, an optimum MOSFET channel width exists that minimizes the total MOSFET related power, due to the fact that increasing MOSFET width reduces the conduction losses while increasing the switching losses.

Secondly, the impact of tapering factor on maximum efficiency is also analyzed [48]. As shown in Fig. 2.5, at a certain range of tapering factor, dynamic switching losses dominate the total losses. The efficiency increases with higher tapering factor in the range dominated by switching losses. After peak efficiency is reached, increasing short-circuit losses in the power MOSFET gate drivers begin to dominate. Hence, efficiency degrades

with further increasing tapering factor. The optimum tapering factors are 10 and 16 for the full-swing and low swing circuits, respectively [53].

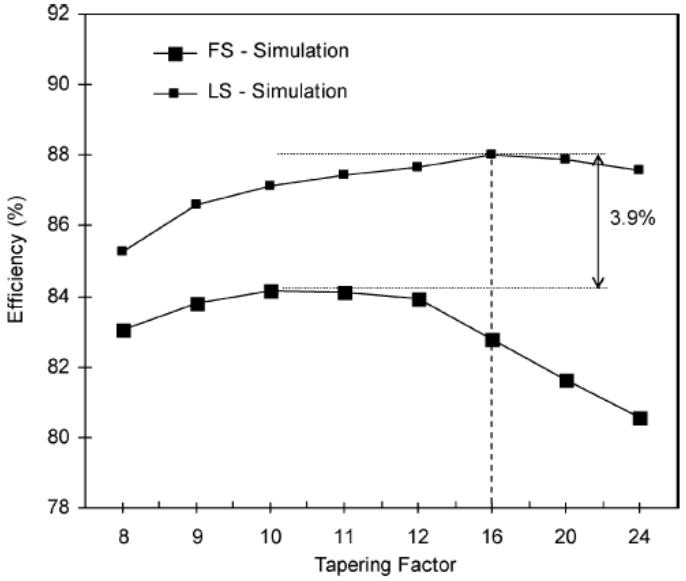


Fig. 2.5 Maximum efficiency with low-swing (LS) and full-swing (FS) Buck converters vs. tapering factors.

Another technique to improve the efficiency, involving low swing MOSFET gate driving, was investigated in [48] [53] to improve the efficiency of a DC-DC converter. The total power dissipation of the low swing buck converter is reduced by 24.5% as compared to the full swing maximum efficiency configuration, resulting in 3.9% higher in efficiency than that of full swing DC-DC converter (Fig. 2.5). Energy recycling drivers or ZVS switching can also be employed to reduce switching losses, as illustrated in [51].

DC-DC converter efficiency is strongly dependent on the switching frequency, so that it is clearly a primary design variable in the analysis. The efficiency was analyzed over some frequency range varying the circuit configuration. The maximum efficiency circuit configurations determined by the model was simulated, verifying the circuit operation and performance characteristics. The global maximum efficiency with a full-swing converter was 84.1% based on a tapering factor of 10. The switching frequency of maximum efficiency configuration is 102 MHz.

The integrated 4-phase Buck DC-DC converters implemented in a 90 nm CMOS technology were demonstrated with off-chip air-core inductors in [49] and [50]. At 480 MHz operating frequency the measured efficiency was 72% for a voltage conversion from 1.8 V – 0.9 V while supplying 0.5 A load current in [49]. The efficiency of 80%-87% at switching frequency of 100 to 317 MHz was demonstrated in [50] for a voltage conversion from 1.2-0.9V while supplying 0.3A output current.

2.5. New architecture DC-DC converters derived from Class E power amplifier

This new family of high switching frequency DC-DC converter has emerged since 1980's [54][55][56]. The name "Class E" comes from switching mode RF power amplifier circuits [57][58]. The idea of Class E DC-DC converter was first published by Gutmann in 1980 [54]. As the switching frequency increases to VHF range, the conventional converters with square waveforms become limited mainly due to short transition times and parasitics. On the other hand, the DC-DC converter derived from the Class E power amplifier provides a promising option for operation at microwave frequencies due to its excellent soft switching characteristics. The Class E DC-DC converter uses the same principles as the class E power amplifier. It is based on sinusoidal waveform operation and the zero voltage switching technique.

The switching-mode Class E power amplifier is employed as the resonant inverter due to its high efficiency and simplicity. The rectifier should offer high efficient and high frequency rectification. The underlying principle of Class E operation is to shape the voltage and current waveforms of the switch so that two waveforms are displaced in time from each other. Matching networks can be added to provide both the required voltage-current waveform displacement and the necessary impedance transformation between the rectifier and inverter. When Class E conditions are met, the power dissipation during the switching transitions will be minimized. The parasitics of semiconductor device and passive components can be incorporated into circuit design. Applications of this RF circuit design principle to high frequency DC-DC power converters have been reported in

[56][59][60][61]. With the advanced semiconductor devices and processing technologies available now, high-efficiency operation becomes possible at hundreds of MHz.

The experimental results for a 10 MHz 5 W 25 V to 5 V converter constructed using RF bipolar switch and a Schottky rectifier verified the basic design approach in 1980 [56] and indicated that efficient load and line regulation could be provided with narrow band frequency control. An efficiency of 68% was obtained and it was predicted that 75% efficiency could be obtained with better optimization of inductor Q. Later in 1988 a converter prototype operating at 22 MHz was demonstrated (Fig. 2.6). It consisted of a self-oscillating, ZVS inverter section that fully utilized internal MOSFET capacitances. Output voltage was regulated by narrow band frequency control, implemented with reverse biased varactor diodes in the gate circuit. A peak efficiency of 78% was obtained for 50V nominal input and 5V output.

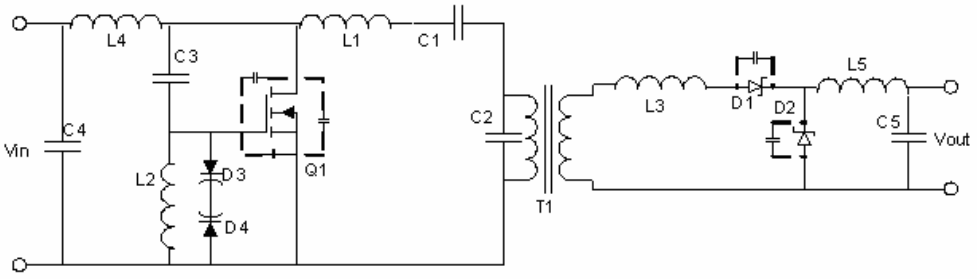


Fig. 2.6 Schematic of DC-DC converter operating at 22 MHz.

In the work reported in [59] a 4.5 GHz DC-DC power converter was investigated, the highest frequency DC-DC converter reported to date. The converter consisted of a switching-mode Class E power amplifier and diode rectifiers (Fig. 2.7). The Class E amplifier was implemented using transmission lines instead of lumped elements. The output power of the Class E amplifier could be shared by two half-wave rectifiers using a 3-dB hybrid as shown in Fig. 2.7. The two DC outputs could be connected in series or in parallel, giving more choices for output voltage or current value. The overall efficiency of 64% was achieved for a 87 Ω load with an output 2.15 V. The output power of the Class E power amplifier could be coupled through a 10 dB directional coupler to a single rectifier circuit. A conversion efficiency of 49% across a 135 Ω load was mentioned in [59]. The fact that the converter was realized without any discrete magnetic components

provided potential for planar, compact and low-profile realization. The approach was amenable to monolithic integration, which would enable very small overall dimensions.

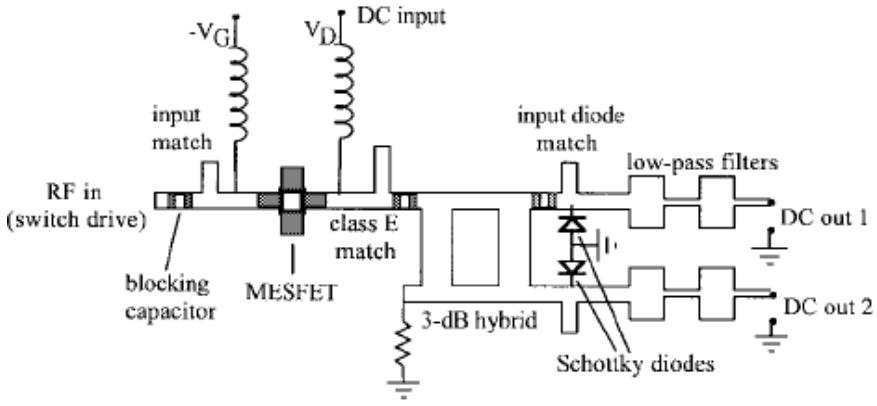


Fig. 2.7 Layout of 4.5 GHz DC-DC converter.

The Class E DC-DC converter was shown in [60] to be an excellent candidate for on-chip switching converters because of high efficiency at high switching frequencies. A 200 mW, 800 MHz integrated Class E DC-DC was designed using a 0.6 μm CMOS process. A 22 nH spiral inductor was designed on the Metal 3 layer. The 50 pF resonant capacitor was implemented with a pair of parallel poly silicon plates. An integrated feedback controller with a VCO was used for output voltage regulation. The layout of the inverter without its choke inductor, synchronous class E rectifier without output low-pass filter inductor and capacitor, VCO, and delay circuit were designed. It was pointed out in this paper that a complete integration could be accomplished by using the second harmonics class E inverter, which didn't need a larger inductance for a choke coil [62].

Class E DC-DC converter can be implemented using discrete components, as described in [61]. The experimental evaluation of prototype with cells operating at 100 MHz was demonstrated (Fig. 2.8). Output power ranged from 2.5 W to 6 W, with an average efficiency greater than 77.5%. An underlying feature of the design approaches presented in this paper was that the energy conversion and regulation functions were partitioned in ways that were compatible with the effective implementation of ultra-high frequency circuit designs and techniques.

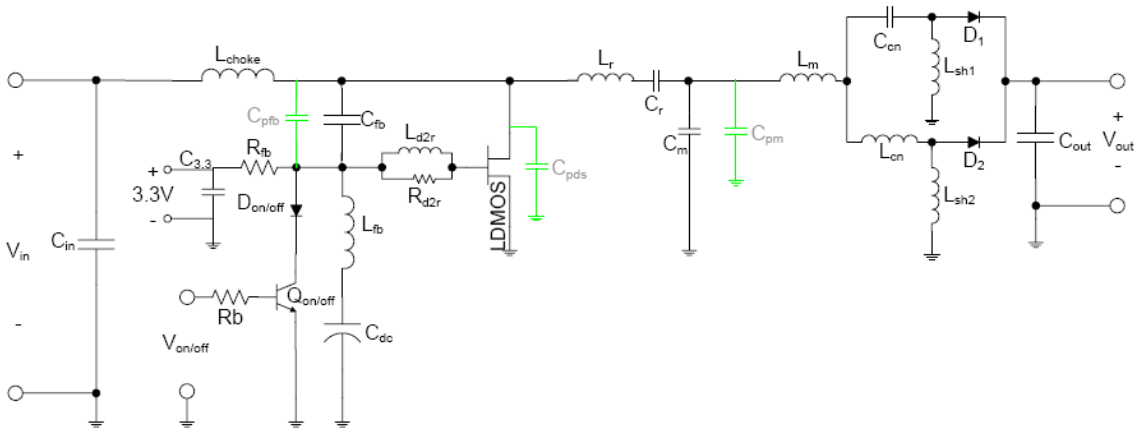


Fig. 2.8 Switching DC-DC power converter at 100 MHz.

2.6. Trends of Power Level with Increasing Frequency

Numerous megahertz switching converters have been reviewed in the previous section. The topologies, techniques for improving efficiency, and implementation techniques are all described along with their main performance features. The implementations of high frequency power converters can be basically classified into two categories in terms of topologies and system architectures:

- Improvements of conventional PWM converters such as Buck -, Boost -, and Flyback -converters and others through :
  - Resonant switching techniques;
  - High-speed semiconductors to replace conventional MOSFETS in the converters;
- New topologies and architectures suitable for high frequency operation such as Class E DC-DC converters.

In terms of processing technologies, there are four kinds of ways to implement power converters:

- Discrete implementation;

- Hybrid integration techniques;
- Monolithically integration by VLSI;
- Distributed implementation based on microwave theory.

The selected multi-megahertz converters are listed in Table 2.1.

Table 2.1 Summary of multi-megahertz power converters.

f	Power	Efficiency	Topology	Implementation	Device/Process	Demo/Simulation	Dimension/power density
10 MHz	5W	68%	Class E	Discrete	MOSFET	Demo	-
10 MHz	10 W	70%-80%	Buck, Flyback	Discrete	MOSFET	Demo	-
22 MHz	50 W	78%	Class E	Discrete	MOSFET	Demo	0.5″×4.16″×2.61″
50-250 MHz	3 W	60%-80%	Boost	Hybrid	MESFET	Demo	10 × 20 mm^2
63 MHz	1 W	~70%	Flyback	Discrete	HFET	Demo	-
100 MHz	6 W	77.5%	Class E	Discrete	LDMOSFET	Demo	-
100 MHz	50 mW	-	2-phase Buck	Monolithic	0.18μm BiCMOS	Simulation	-
100-477 MHz	-	80%-88%	Buck	Monolithic	0.18μm/80nm CMOS	Simulation	12.6 mm^2
100-317 MHz	270 mW	80%-87%	4-phase Buck	Integrated	90nm CMOS	Demo	1.26 mm^2(inductor not included)
480 MHz	450 mW	72%	4-phase Buck	Integrated	90nm CMOS	Demo	-
800 MHz	200 mW	72%	Class E	monolithic	0.6 μm CMOS	Simulation	-
4.5 GHz	50-120 mW	49%-64%	Class E	Distributed	MESFET	Demo	14×7×0.05 cm^3

The relationship between the power levels and frequencies of the converters previously described is depicted in Fig. 2.9. And the plot of efficiency vs frequency is shown in Fig. 2.10. It is clearly shown that there is a trend towards decreased power level when the switching frequency increases. It seemed reasonable to suppose that there is an ultimate limit for the trade-off between the power level and the frequency of a converter. Considering the the components constituting a converter, it is reasonable to conclude that it is the capabilities of power semiconductor devices in the converter that ultimately determines its power level. Therefore, the power-frequency limits of the semiconductor devices should be considered thereafter to identify the trade-off existing between the power and the frequency.

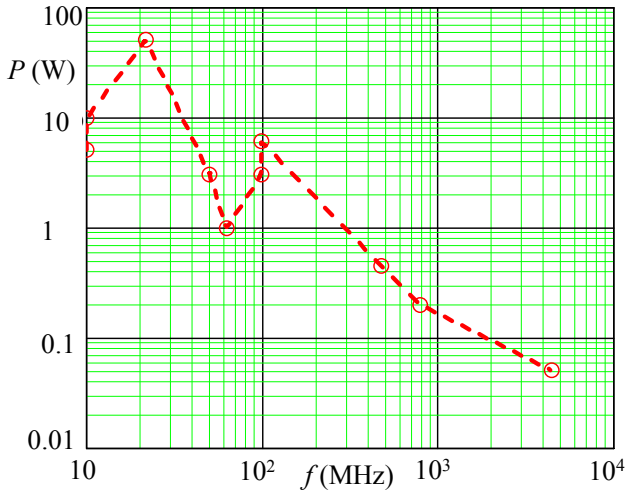


Fig. 2.9 Power level vs frequency for selected converters.

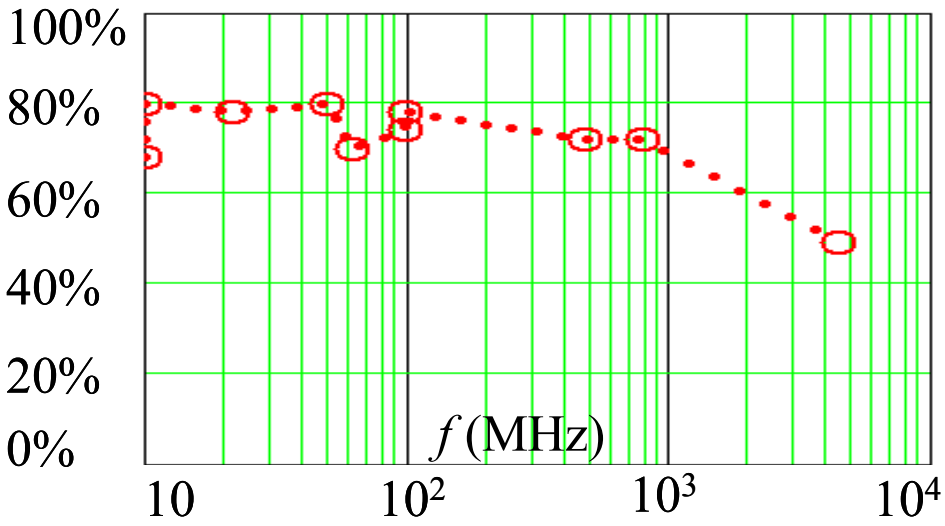


Fig. 2.10 Efficiency vs frequency for selected converters.

The power-frequency product of the power devices should be derived in a manner that makes it independent of design details. The objective here is to derive a general relation about the power-frequency limit that show the performance limits independent of a converter-specific design and demonstrate its use in evaluating future designs and developments. This is to establish upper bounds on the performance by developing a highly idealized and simplified device model whose performance is not likely to be

surpassed by that of any attainable design, no matter how optimized or cleverly conceived.

Firstly, for a semiconductor junction with a doping density N, the maximum voltage is given by [63]

$$V_{\max} = \frac{\varepsilon_s E_{bk}^{\ 2}}{2Nq} \tag{2.1}$$

where ε_s : dielectric constant of the semiconductor;

q : the electron charge;

E_{bk} : breakdown electric field.

The maximum current per gate width flowing through the device is given by

$$I_{\max} = dqNv_s \tag{2.2}$$

where d : thickness of the channel;

v_s : the saturated drift velocity of an electron.

For practical applications, the maximum applied voltage is usually kept to be about one-half of $V_{\max}$ to provide an adequate safety margin. This is the same for the maximum current through the device. So the maximum power per unit gate length is:

$$P_{\max} = \frac{1}{2} \cdot \frac{1}{2} V_{\max} \cdot \frac{1}{2} I_{\max} = \frac{\varepsilon_s E_{bk}^{\ 2} v_s d}{16} \tag{2.3}$$

The maximum allowable operation frequency is the cut-off frequency f_T of the device, given by

$$f_T = \frac{1}{2\pi\tau} = \frac{1}{2\pi} \frac{v_s}{L_g} \tag{2.4}$$

L_g : gate length.

Finally the power-frequency product is derived from (2.3) and (2.4) as

$$P_{\max} f_T = \frac{\varepsilon_s}{32\pi} \frac{d}{L_g} (E_{bk} v_s)^2 \tag{2.5}$$

d/L_g is the form factor of the device, typically in the range of 3~5.

Therefore, the power-frequency product mainly depends on the product of E_{bk} and v_s, which agrees well with Johnson's figure of merit [64]. E_{bk} and v_s are the intrinsic properties of the semiconductor material. So the power-frequency product ultimately depends on the properties of semiconductor materials in the devices. This relationship effectively verify the empirical relationship $P \propto f^{-1}$ for the power-frequency product of the present Si-based devices [3][108][111].

The simple analysis above is a reasonable explanation for a trade-off between power level and frequency existing in power converters. For given semiconductor material, the energy transfer rate per second must decrease with increasing frequency, eventually limiting the realization of high density power converter through increasing frequency. Though raised frequency has been the dominant factor that enabled dramatic power density increases over the past, it doesn't mean that power density improvement could be always achieved by pushing the frequency, under the conditions of given semiconductor materials. The power density would be decreased because of dramatically reduced power when the frequency is pushed beyond some limiting value, thus defeating our original objective for improved power density.

The larger power level can be achieved, in principle, by connecting devices in parallel within the frequency limits of the device, according to Johnson's figure of merit given below. The price paid is the decreased impedance level. In practice, power output may be limited more by the problems of cost, device uniformity, and circuitry [64].

$$\text{JFOM} = (P_m X)^{1/2} f_T = \frac{E_b v_s}{2\pi}$$

where X is the reactive impedance of device capacitance.

Due to this limitations mainly imposed by the semiconductor materials, it is necessary to develop other devices materials to achieve higher power and improve power density at higher frequency. The physical properties of major semiconductor materials are listed in Table 2.2. The calculated $(E_{bk}v_s)^2$ in the last row is normalized to that of Si.

Table 2.2 Physical properties of several semiconductor materials

	Si	GaAs	4H SiC	6H SiC	GaN
Bandgap E_G (eV)	1.1	1.4	3.2	3	3.4
E_{bk} (10^5 V/cm)	5.7	6.4	33	30	40
v_s (10^7 cm/s)	1	2	2	2	2.5
μ (cm^2/Vs)	1350	8500	610	340	1200
k (W/cm-K)	1.5	0.5	4.5	4.5	2.1
$(E_{bk}v_s)^2$	1	5	134	110	308

It can be seen that GaN and SiC take a tremendous advantage over conventional semiconductors Si and GaAs for high power and high frequency power conversion due to their larger breakdown field and higher saturated velocity. High saturation velocity means this material suitable for high frequency operation, whereas high breakdown field makes this material suitable for high voltage application. As a result, it is suitable for high power and high frequency operation. High thermal conductivity gives it extra advantage for high power applications.

Therefore GaN and SiC demonstrate high potential for the efforts to improve the power density by pushing frequency. Their distinguished physical properties give them much higher performance limits, compared with that of silicon-based power devices. Thus it is expected that research and development on novel materials, novel structures and packaging of power devices will help to relieve the current power-frequency limits imposed by silicon and raise the future power-frequency product to a higher level, so that higher power densities can be achieved in reality by pushing frequency.

Chapter 3 Analysis and Design of RF Class E DC-DC Power Converter

3.1. Introduction

In the previous chapter, many different techniques that have in the past been employed to achieve high frequency DC-DC power converter were summarized and described. In this chapter a RF Class E DC-DC power converter, which is suitable for operation at Very High Frequency (VHF) range, is described and demonstrated. The converter consists of a high frequency, high efficient Class E inverter, a resonant rectifier and an optional matching network as shown in Fig. 3.1.

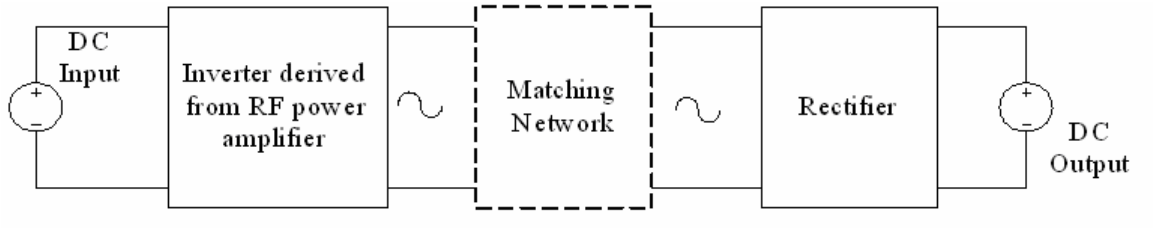


Fig. 3.1 Block diagram of proposed RF DC-DC converter.

The converter can be implemented by using discrete active and passive components because these components operating in RF ranges are now commercially available. It is more easily built and flexible in design for the purpose of investigating the frequency limitations of high frequency power conversion, compared with that of monolithic converter on a chip.

The operating principle of the circuit is described along with the derivations of the design equations. Effects of various circuit parameters on the performance of converter are analyzed in this chapter. The prototype of the converter is implemented based on the selected discrete components. Parasitic values of circuit board layout are extracted by

Ansoft Q3D. Experimental results are provided with analysis and discussions at the end of the chapter.

3.2. Analysis of Class E RF DC-DC converter

3.2.1. Operation principle of Class E inverter

The basic circuit of Class E inverter is shown in Fig. 3.2. It is also called a Class E power amplifier. The inverter meets the so-called Class E switching conditions: both the switch voltage v_{DS} and its derivate dv_{DS}/dt are zero when the switch SW turns on. The class E inverter consists of a switch SW, a shunt capacitor C_s, a series resonant circuit $L_r - C_r$, and a choke inductor RFC. The parasitic output capacitance of SW, choke parasitic capacitance and stray capacitances are included in C_s. The necessary capacitance can be provided by the overall shunt parasitic capacitance for high operating frequency.

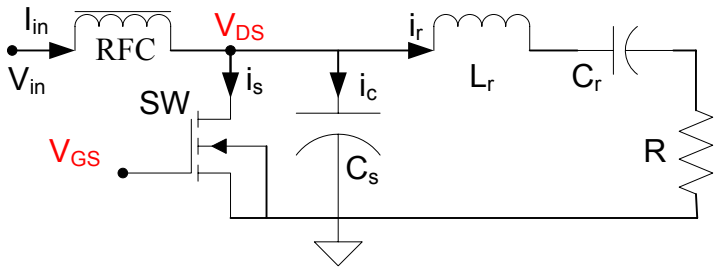


Fig. 3.2 Class E inverter.

The series resonant circuit $L_r - C_r$ is usually not tuned to the operating frequency f. To achieve zero-voltage switching turn-on of the switch, the operating frequency is greater than the resonant frequency $f_0 = 1/2\pi\sqrt{L_r C_r}$. Thus the resonant circuit has a net series reactance jX at operating frequency. It can be considered as a resonant circuit tuned to the operating frequency in series with a net reactance jX (see Fig. 3.3).

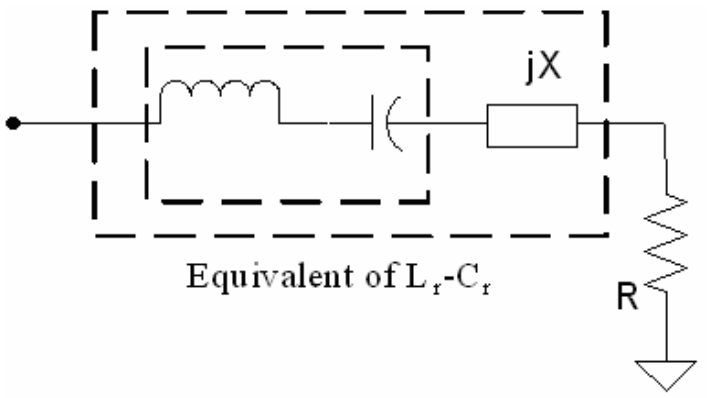


Fig. 3.3 Series resonant circuit.

The loaded quality factor Q is assumed be high (Q≥2.5) so that the sinusoidal current flows through the series resonant circuit [65][66]. The choke RFC has large enough inductance so that its ripple current is much lower than the dc component of the input current. Fig. 3.4 shows the waveforms of the inverter. The difference between input current, I_{in}, and resonant current, i_r, flows into C_s when the switch is open, and through the switch when it is closed. When the switch turns on, $v_{DS}(2\pi) = 0$ means no energy stored in C_s, yielding zero turn-on switching losses. When the switch turns on, $dv_{DS}(\omega t)/d(\omega t)\big|_{\omega t=2\pi} = 0$ means that the switch current starts from zero.

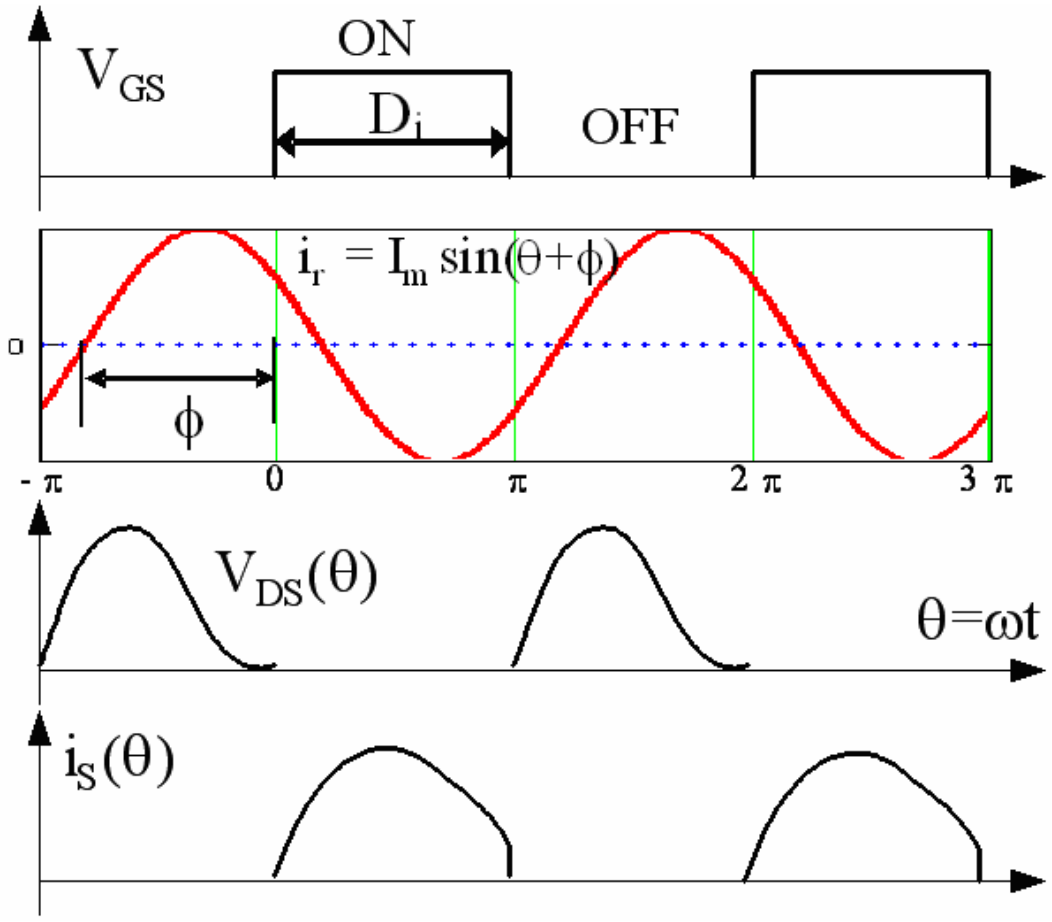


Fig. 3.4 Waveforms of Class E inverter.

Optimum operation, $v_{DS}(2\pi) = 0$ and $dv_{DS}(\omega t)/d(\omega t)\big|_{\omega t=2\pi} = 0$, can be achieved only at optimum load $R = R_{opt}$ [65]. If $R > R_{opt}$, the amplitude of i_r through the resonant circuit is lower than that for optimum operation, voltage drop across shunt capacitor C_s decreases, and the switch voltage v_{DS} is greater than zero at turn on. On the other hand, when $R < R_{opt}$, the switch voltage v_{DS} is less than zero at turn-on. Both cases ($R > R_{opt}$ and $R < R_{opt}$) result in turn-on switching losses. If an anti-parallel or a series diode is added to the switch, the switch can automatically turn on at zero voltage for $R \le R_{opt}$.

3.2.2. Circuit Analysis based on ideal operation

The analysis of the circuit is based on the following assumptions:

a) The active devices act as ideal switches whose on-resistance is zero, off-resistance is infinite, and switching times are zero.

b) The parasitic capacitances of the switches are included in the shunt capacitances and are independent of the switch voltages.

c) The current through the series resonant circuit is sinusoidal at the operating frequency.

d) The choke inductance is large enough that current through it is constant.

e) All passive elements in the circuit are ideal.

The analysis is performed in the interval $0 \le \theta \le 2\pi$, where $\theta = \omega t$ is the angular time. Based on the assumptions above, the current through the resonant circuit $L_r - C_r$ is assumed to be:

$$i_r = I_m \sin(\theta + \Phi) \tag{3.1}$$

where I_m is the amplitude and Φ is the initial phase of current i_r.

Refer to Fig. 3.2 and Fig. 3.4, and assume ON duty cycle of SW is D_i.

$$SW : \begin{cases} ON & 0 < \theta < 2\pi D_i \\ OFF & 2\pi D_i < \theta < 2\pi \end{cases}$$

According to Fig. 3.2,

$$i_s(\theta) + i_c(\theta) = I_{in} - i_r(\theta) \tag{3.2}$$

During the time interval $0 < \theta < 2\pi D_i$, the switch is on and $i_c = 0$.

$$i_s(\theta) = \begin{cases} I_{in} - I_m \sin(\theta + \Phi) & 0 < \theta < 2\pi D_i \\ 0 & 2\pi D_i < \theta < 2\pi \end{cases} \tag{3.3}$$

During the time interval $2\pi D_i < \theta < 2\pi$, the switch is off and $i_s = 0$.

$$i_c(\theta) = \begin{cases} 0 & 0 < \theta < 2\pi D_i \\ I_{in} - I_m \sin(\theta + \Phi) & 2\pi D_i < \theta < 2\pi \end{cases} \tag{3.4}$$

The voltage across the shunt capacitor C_s and switch SW is:

$$v_{DS}(\theta) = \frac{1}{\omega C_s} \int_{2\pi D_i}^{\theta} i_C(\theta) d\theta \Rightarrow$$

$$v_{DS}(\theta)=\begin{cases}0 & 0<\theta<2\pi D_i\\ \dfrac{1}{\omega C_s}\{I_{in}(\theta-2\pi D_i)+I_m[\cos(\theta+\Phi)-\cos(\Phi+2\pi D_i)]\} & \\ & 2\pi D_i<\theta<2\pi\end{cases} \tag{3.5}$$

For ZVS operation,

$v_{DS}(2\pi)=0\Rightarrow$

$$I_m=I_{in}\frac{2\pi(1-D_i)}{\cos(2\pi D_i+\Phi)-\cos(\Phi)} \tag{3.6}$$

The voltage slope of v_{DS} is:

$$\xi=\frac{dv_{DS}(\theta)}{d\theta}\Big|_{\theta=2\pi}=0\Rightarrow$$

$$\xi=\frac{I_{in}}{\omega C_s}\left[1-\frac{2\pi(1-D_i)\sin(\Phi)}{\cos(2\pi D_i+\Phi)-\cos(\Phi)}\right]=0\Rightarrow$$

$$tg\Phi=\frac{\cos(2\pi D_i)-1}{2\pi(1-D_i)+\sin(2\pi D_i)} \tag{3.7}$$

The average voltage across the choke inductor is zero, so the input voltage is equal to the average of v_{DS} :

$$V_{in}=\frac{1}{2\pi}\int_0^{2\pi}v_{DS}(\theta)d\theta\Rightarrow$$

$$V_{in}=\frac{I_{in}(1-D_i)}{\omega C_s}\frac{\pi(1-D_i)\cos(\pi D_i)+\sin(\pi D_i)}{\tan(\pi D_i+\Phi)\sin(\pi D_i)} \tag{3.8}$$

Thus the dc input resistance of the inverter is:

$$R_{dc}=\frac{V_{in}}{I_{in}}=\frac{(1-D_i)}{\omega C_s}\frac{\pi(1-D_i)\cos(\pi D_i)+\sin(\pi D_i)}{\tan(\pi D_i+\Phi)\sin(\pi D_i)} \tag{3.9}$$

Refer to Fig. 3.3, the series resonant circuit can be equivalent to the net reactance jX at the operating frequency. Due to the sinusoidal current through the series resonant circuit, the fundamental component of v_{DS} at operating frequency can be represented as (see Fig. 3.5)

$$v_{DS\_1}=v_x+v_R=V_x\cos(\theta+\Phi)+V_R\sin(\theta+\Phi)$$

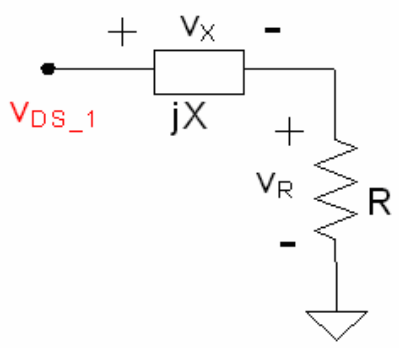


Fig. 3.5 Equivalent circuit of series resonant circuit at the operating frequency.

R is the load resistance of the inverter, which is driven by the sinusoidal current through the series resonant circuit. The voltage across the R is also given by

$$v_R(\theta) = RI_m \sin(\theta + \Phi) = V_R \sin(\theta + \Phi) \tag{3.10}$$

The amplitude of the fundamental component $v_R(\theta)$ can be also determined by the following Fourier integral with respect to phase Φ :

$$V_R = \frac{1}{\pi}\int_0^{2\pi} v_{DS}(\theta)\sin(\theta + \Phi)d\theta \Rightarrow$$

$$V_R = -V_{in}\frac{2\sin(\pi D_i)\sin(\pi D_i + \Phi)}{\pi(1 - D_i)} = R \cdot I_m \tag{3.11}$$

Similarly, the amplitude of $v_x(\theta)$ can be calculated as the following:

$$V_x = \frac{1}{\pi}\int_0^{2\pi} v_{DS}(\theta)\cos(\theta + \Phi)d\theta \Rightarrow$$

$$V_x = X \cdot I_m =$$

$$V_{in}\frac{1 - 2\pi^2(1 - D_i)^2 - 2\cos\Phi\cos(2\pi D_i + \Phi) + \cos 2(\pi D_i + \Phi)[\cos 2\pi D_i - \pi(1 - D_i)\sin 2\pi D_i]}{2\pi(1 - D_i)\cos(\pi D_i + \Phi)[\pi(1 - D_i)\cos\pi D_i + \sin\pi D_i]} \tag{3.12}$$

Until now the output power of the inverter can be derived from equation (3.11) as the following:

$$P_{out\_inv} = \frac{1}{2}V_R I_m \tag{3.13}$$

Substituting (3.6) and (3.11) into the equation above (3.13), then

$$P_{out\_inv} = V_{in} I_{in}$$

100% efficiency is achieved for an ideal inverter.

Using (3.6), (3.8) and (3.11), the following relationship can be derived:

$$\omega C_s R = \frac{2\sin(\pi D_i)\sin(\pi D_i + \phi)\cos(\pi D_i + \phi)[\pi(1-D_i)\cos(\pi D_i) + \sin(\pi D_i)]}{\pi^2(1-D_i)} \tag{3.14}$$

Using (3.6), (3.88) and (3.12), the reactance X can be obtained:

$$\omega C_s X = \frac{2\pi^2(1-D_i)^2 - 1 + 2\cos\Phi\cos(2\pi D_i + \Phi) - \cos 2(2\pi D_i + \Phi)[\cos 2\pi D_i - \pi(1-D_i)\sin 2\pi D_i]}{2\pi^2(1-D_i)} \tag{3.15}$$

Assuming the quality factor of the series-tuned circuit is Q, define

$$Q = \frac{\omega L_r}{R}$$

$$\Rightarrow L_r = Q\frac{R}{\omega} \tag{3.16}$$

The net reactance of series resonant circuit is

$$X = \omega L_r - \frac{1}{\omega C_r} \tag{3.17}$$

From (3.16) and (3.17)

$$C_r = \frac{1}{\omega}\cdot\frac{1}{QR_i - X} \tag{3.18}$$

Substituting (3.6) into (3.3), then differentiating (3.3) with respect to θ, the peak switch current can be obtained:

$$I_{S\_\max} = I_{in}[1 - \frac{\pi(1-D_i)}{\sin(\pi D_i)\sin(\pi D_i + \Phi)}] \tag{3.19}$$

When $\theta = \frac{3}{2}\pi - \Phi$ for $\theta < 2\pi D_i$

If duty cycle D_i is low, the peak switch current occurs at $\theta = 2\pi D_i$

$$I_{S\_\max} = I_{in}[1 + \frac{\pi(1-D_i)\sin(2\pi D_i + \Phi)}{\sin(\pi D_i)\sin(\pi D_i + \Phi)}] \tag{3.20}$$

In the same way, from (3.5) the peak switch voltage occurs at

$$\theta = 2\pi - \Phi + \arcsin[\frac{\cos(\Phi) - \cos(2\pi D_i + \Phi)}{2\pi(1-D_i)}] \tag{3.21}$$

The normalized peak switch current I_{S_max}/I_{in} and voltage V_{DS_max}/V_{in} versus duty cycle D_i is shown in Fig. 3.6. When $D_i = 0.5$, $I_{S\_max}/I_{in} = 2.862$, $V_{DS\_max}/V_{in} = 3.56$.

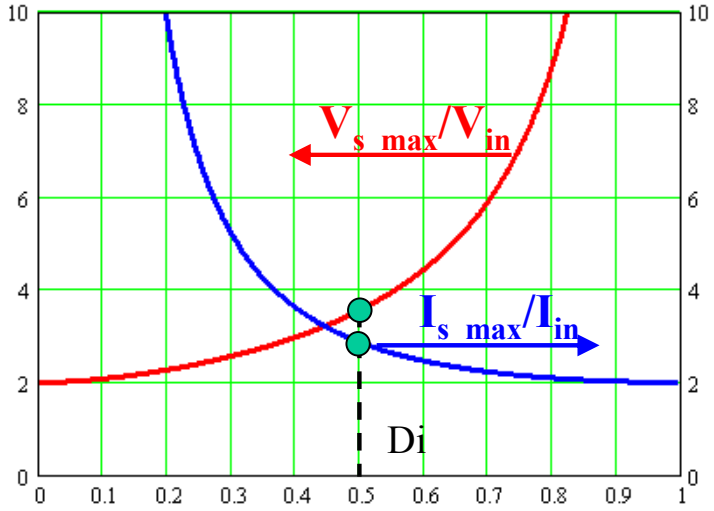


Fig. 3.6 Normalized peak switch current and voltage vs. duty cycle.

Power output capability of the inverter is defined as:

$$C_p = \frac{P_{out\_inv}}{V_{DS\_max} I_{S\_max}} \tag{3.22}$$

Therefore power output capability versus duty cycle can be plotted in Fig. 3.7.

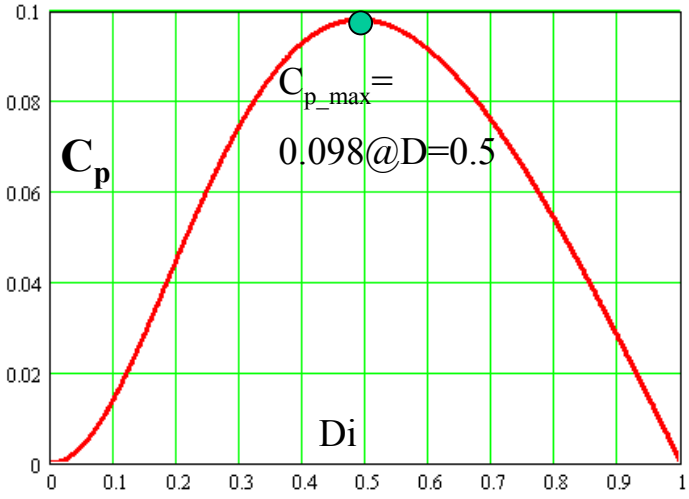


Fig. 3.7 Power output capability C_p vs Duty cycle D_i.

From (3.13) and (3.11), the output power is obtained as

$$P_{out\_inv} = \frac{2V_{in}^{\ 2}}{R}\left[\frac{\sin \pi D_i \sin(\pi D_i + \Phi)}{\pi(1 - D_i)}\right]^2$$

The normalized output power $P_{out\_inv} \Big/ V_{in}^{\ 2} R$ as a function of duty cycle is shown below (Fig. 3.8).

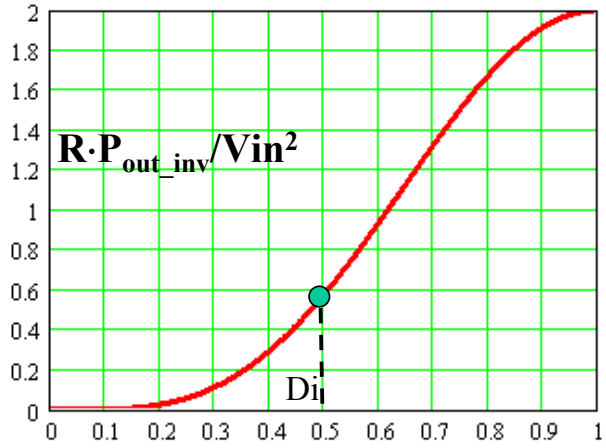


Fig. 3.8 Normalized output power vs duty cycle.

The duty cycle of the inverter can in fact be chosen arbitrarily, however, 50% duty cycle is the common choice, considering the factors below:

a. maximum power output capability is reached at this duty cycle;

b. optimum trade-off of the voltage stress and current stress of the active switch;

c. convenient for practical implementation and easily obtainable duty cycle value.

For the analysis above, assume $D_i = 0.5$ and $\xi = 0$, the following parameters can then be derived from the equations above:

From (3.7),

$$\tan(\Phi) = -\frac{2}{\pi} \tag{3.23}$$

$$\sin(\Phi) = \frac{2}{\sqrt{\pi^2 + 4}} \tag{3.24}$$

$$\cos(\Phi) = -\frac{\pi}{\sqrt{\pi^2 + 4}} \tag{3.25}$$

$$\text{Therefore, } \Phi = 147.52° \tag{3.26}$$

From (3.9) and (3.14)

$$R_{dc} = \frac{V_{in}}{I_{in}} = \frac{1}{\pi\omega C_s} = \frac{\pi^2 + 4}{8} R \tag{3.27}$$

$$\omega C_s R = \frac{8}{\pi(\pi^2 + 4)} = 0.1836 \tag{3.28}$$

From (3.11) and (3.12),

$$V_R = \frac{4}{\sqrt{\pi^2 + 4}} V_{in} = 1.074 V_{in} \tag{3.29}$$

$$V_x = \frac{\pi(\pi^2 - 4)}{4\sqrt{\pi^2 + 4}} V_{in} = 1.2378 V_{in} \tag{3.30}$$

Fundamental component of v_{DS} at operating frequency f is

$$\begin{aligned} v_{DS\_1} &= 1.074 V_{in} \sin(\theta + \Phi) + 1.2378 V_{in} \cos(\theta + \Phi) \\ &= 1.639 V_{in} \sin(\theta + 147.52° + 49.05°) = 1.639 V_{in} \sin(\theta - 163.43°) \end{aligned} \tag{3.31}$$

From (3.6), $I_m = I_{in} \dfrac{\sqrt{\pi^2 + 4}}{2}$ (3.32)

$$I_{S\_\max} = I_{in}[1 + \frac{\sqrt{\pi^2 + 4}}{2}] = 2.862 I_{in} \tag{3.33}$$

$$V_{S\_\max} = V_{in} 2\pi(\pi - \Phi) = 3.56 V_{in} \tag{3.34}$$

From (3.13), the output power is

$$P_{out\_inv} = \frac{V_R^{\,2}}{2R} = \frac{8}{\pi^2 + 4} \frac{V_{in}^{\,2}}{R} = 0.5768 \frac{V_{in}^{\,2}}{R} = \pi\omega C_s V_{in}^{\,2} \tag{3.35}$$

The output power is proportional to the frequency, the capacitance across the drain-source of the switch, and the squared input voltage.

From (3.15)

$$\omega C_s X = \frac{\pi^2 - 4}{2(\pi^2 + 4)} = 0.2116 \tag{3.36}$$

$$\frac{X}{R} = \frac{\pi(\pi^2 - 4)}{16} = 1.1525 \tag{3.37}$$

Therefore, the load network impedance of Class E inverter is

$$Z = R + jX = R(1 + jtg49.05°) = 1.526R \cdot e^{j49.05°} = \frac{0.28}{\omega C_s} e^{j49.05°} \tag{3.38}$$

Power output capability is:

$$C_p = \frac{P_{out\_inv}}{V_{S\_\max} I_{S\_\max}} = 0.098 \tag{3.39}$$

3.2.3. Practical considerations

The previous analysis is based on several simplifying assumptions, which are not always acceptable. Class E inverter significantly depends on the circuit parameters, such as choke inductance, load quality factor Q, nonzero active device ON resistance, or duty cycle. It is important to determine the effect of these factors on the circuit performance.

The ideal choke RFC, which has zero DC resistance and infinite reactance at operating frequency, is assumed in the previous analysis. Class E operation with a finite (and small) DC feed inductance is possible and sometimes desirable [67][68]. In practice, a very large inductance value (larger than normally required) for the RFC choke is inconvenient considering:

1. Size, weight and cost of RFC choke increases with inductance;
2. DC resistance is also large, increasing power losses;
3. Large number of turns may cause high parasitic capacitance.

Therefore a tradeoff in designing RFC is important. Inductance should be as low as possible, but still large enough to achieve the desired behavior and performance. A practical recommendation is that the inductance of RFC choke should ensure current ripple to be less than 10% of input DC current I_{in} [58][65].

$$\Delta i = \frac{V_{in}}{L}\frac{1}{2f} < 10\% I_{in} = 0.1\frac{V_{in}}{R}\frac{8}{\pi^2 + 4} \Rightarrow$$

$$\omega L_{RFC} > 55R \tag{3.40}$$

The real switch device in the inverter circuit has non-zero ON resistance, resulting in the switch conduction loss. Some previous papers have addressed the switch losses in the Class E power amplifier. A simple approximate method was firstly presented by Raab

and Sokal in 1978 to calculate the power losses introduced by the ON resistance R_{ds_on} for 50% duty cycle [69]. The power loss was then given by

$$\begin{aligned} P_{ds\_on} &= \frac{1}{2\pi}\int_0^{2\pi} i_s(\theta)^2 R_{ds\_on} d\theta \\ &= \frac{\pi^2+28}{2(\pi^2+4)}\frac{R_{ds\_on}}{R}P_{out\_inv} = 1.365\frac{R_{ds\_on}}{R}P_{out\_inv} \end{aligned} \tag{3.41}$$

The conduction losses in each Class E circuit component was derived and expressed as functions of duty cycle in [73]. The effect of duty cycle on power losses and the total efficiency was analyzed. However, the waveforms of the amplifier were not reformulated. Then a new analysis formulation was presented in [74] to analyze the effect of the ON resistance with a simple reformulation of the drain waveforms. The efficiency and optimum component values of a lossy Class E amplifier were solved with relatively simple calculations. The derivation is summarized in the following. However in most cases (3.41) is used to estimate the ON-resistance power dissipation due to its simplicity.

In the following analysis of 50% duty cycle, the effect of ON resistance of the switch will be considered.

$$v_{DS}(\theta) = \begin{cases} i_s(\theta)R_{ds\_on} & 0 < \theta < \pi \\ \dfrac{1}{\omega C_s}\{I_{in}(\theta-\pi) + I_m[\cos(\theta+\Phi)+\cos\Phi]\} + v_{DS\_0} & \\ & \pi < \theta < 2\pi \end{cases}$$

$$v_{DS\_0} = R_{ds\_on} i_s(\pi) = R_{ds\_on}(I_{in} + I_m \sin\Phi)$$

By applying Class E requirements $i_s(2\pi) = 0$ and $v_{DS}(2\pi) = 0$,

$$i_s(2\pi) = 0 \Rightarrow \sin\Phi = \frac{I_{in}}{I_m}$$

$$v_{DS}(2\pi) = 0 \Rightarrow \cos\Phi = -\frac{I_{in}}{I_m}\frac{2y+\pi}{2}$$

where $y = \omega C_s R_{ds\_on}$

Therefore, $tg\Phi = -\dfrac{2}{2y+\pi}$

When $\pi < \theta < 2\pi$,

$$v_{DS}(\theta) = \frac{I_{in}}{\omega C_s}[\theta - (y + \frac{\pi}{2})\cos\theta - \sin\theta + y - \frac{3}{2}\pi]$$

When $0 < \theta < \pi$,

$$i_S(\theta) = I_{in}[1 + (y + \frac{\pi}{2})\sin\theta - \cos\theta]$$

The average value of $v_{DS}(\theta)$ needs to be equal to the input voltage:

$$V_{in} = \frac{1}{2\pi}\int_0^{2\pi} v_{DS}(\theta)d\theta \Rightarrow$$

$$V_{in} = \frac{I_{in}}{2\pi\omega C_s}(2 + 3\pi y + 2y^2)$$

The power dissipation caused by the ON resistance can be calculated as:

$$P_{ds\_on} = \frac{1}{2\pi}\int_0^{2\pi} i_s(\theta)v_{ds}(\theta)d\theta \Rightarrow$$

$$P_{ds\_on} = R_{ds\_on}{I_{in}}^2(\frac{7}{4} + \frac{\pi^2}{16} + \frac{\pi}{4}y + \frac{2}{\pi}y + \frac{1}{4}y^2)$$

Therefore the output power of the inverter is:

$$P_{out\_inv} = P_{in} - P_{ds\_on} \Rightarrow$$

$$y^4(k + \frac{\pi^2}{4}) + y^3(3\pi k + \pi + \frac{\pi^3}{4}) + y^2(2k + \frac{9\pi^2}{4}k + \frac{\pi^2}{4} + \frac{\pi^4}{16})$$
$$+ y(3\pi k - \pi) + k = 0$$

where $k = \frac{P_{out\_inv}R_{ds\_on}}{{V_{in}}^2}$

It's interesting to note that the equation doesn't have positive roots above $k \approx 0.100152$. Thus the following requirement must be met in order to operate in the Class E mode [74]:

$$R_{ds\_on} < 0.100152\frac{{V_{in}}^2}{P_{out\_inv}}$$

And also from $P_{out\_inv} = P_{in} - P_{ds\_on} \Rightarrow$

$$R = 2(\sin\Phi)^2[\frac{1}{2\pi\omega C_s}(2 + 3\pi y + 2y^2) - R_{ds\_on}(\frac{7}{4} + \frac{\pi^2}{16} + \frac{\pi}{4}y + \frac{2}{\pi}y + \frac{y^2}{4})]$$

The amplitude of the voltage across the net reactance X is:

$$V_x = \frac{1}{\pi}\int_0^{2\pi} v_{DS}(\theta)\cos(\theta+\Phi)d\theta \Rightarrow$$

$$V_x = X \cdot I_m =$$

$$\frac{I_{in}}{\pi\omega C_s}[\pi\sin\Phi + \frac{\pi}{2\sin\Phi} + 4\cos\Phi + 2y\sin\Phi] \Rightarrow$$

$$X = \frac{\sin\Phi}{\pi\omega C_s}[\pi\sin\Phi + \frac{\pi}{2\sin\Phi} + 4\cos\Phi + 2y\sin\Phi]$$

Assume the ESR of resonant inductor L_r is r_L, the ESR of resonant capacitor C_r is r_C. The power losses in r_L and r_C are

$$P_{LC} = \frac{1}{2} I_m{}^2 (r_L + r_C) = \frac{r_L + r_C}{R} P_{out\_inv} \tag{3.42}$$

The power loss in the ESR r_{RFC} of RFC choke is

$$P_{RFC} = I_{in}{}^2 r_{RFC} = \frac{4}{\pi^2+4} I_m{}^2 r_{RFC} = \frac{8}{\pi^2+4}\frac{r_{RFC}}{R} P_{out\_inv} \tag{3.43}$$

Considering the effects of R_{ds_on}, r_L, r_C and r_{RFC}, the efficiency of Class E inverter is

$$\eta_{inv} = \frac{1}{1 + 1.365\frac{R_{ds\_on}}{R} + \frac{r_L + r_C}{R} + \frac{8}{\pi^2+4}\frac{r_{RFC}}{R}} \tag{3.44}$$

For a given R_{ds_on} and ignoring other parasitic resistances, an increase in load resistance leads to an increase in efficiency. But at the same time, the output power decreases, as seen from (3.35); RFC choke reactance increases, according to (3.40); the required shunt susceptance decreases based on (3.28), meaning that maximum frequency of the circuit is compromised.

If Q_{Lr} is the unloaded quality factor of L_r and Q_{Cr} is the unloaded quality factor of C_r, the ESR of L_r C_r is

$$r_L + r_C = \frac{\omega L_r}{Q_{Lr}} + \frac{1}{\omega C_r Q_{Cr}} = \frac{QR}{Q_{Lr}} + \frac{QR - X}{Q_{Cr}} \tag{3.45}$$

The power loss due to the ESR of inductor usually dominates the power loss due to the ESR of capacitor, so for an optimally operated Class E inverter when ignoring r_{RFC}, the efficiency given by (3.44) can be approximated as

$$\eta_{inv} = \frac{1}{1 + 1.365\frac{R_{ds\_on}}{R} + \frac{Q}{Q_{Lr}}} \tag{3.46}$$

The relationship between efficiency η_{inv} and the load quality factor Q is shown in Fig. 3.9 for different R_{ds_on}/R (assuming unloaded quality factor of inductor $Q_{Lr} = 170$). Fig. 3.10 shows the relationship between efficiency and the ratio R_{ds_on}/R for different load quality factor values.

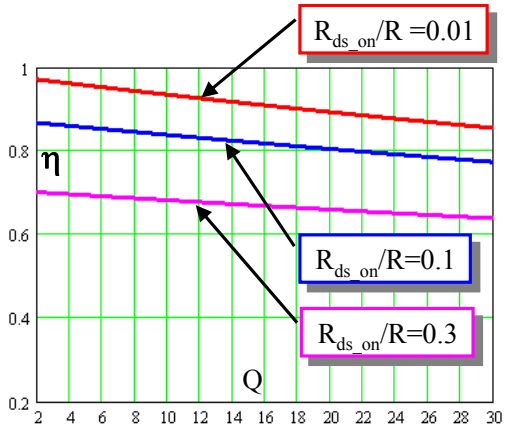


Fig. 3.9 Efficiency vs Q (D_i = 50%)

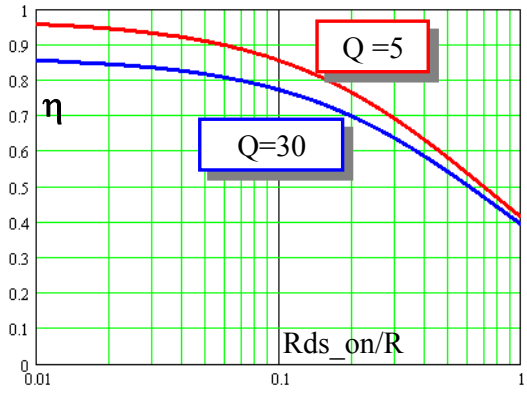


Fig. 3.10 Efficiency vs R_{ds_on}/R (D_i = 50%).

Lower Q leads to lower power dissipation in the circuit, thus the efficiency is increased. Efficiency decreases quickly with increasing ON resistance of the switch when the load is fixed.

A number of excellent Class E papers have been published to characterize the effects of Q. The analysis method proposed by Raab [72] assumes that the quality factor

Q of the resonant network is high enough that the current through L_r and C_r is essentially sinusoidal at the operating frequency. This method gives quite accurate results for $Q \geq 15$. Kazimierczuk and Puczko [66] provide a class E amplifier analysis at specific values of Q and D in the form of tabulation, but they didn't give continuous function design equations based on their tabular data. As a result, an accurate design is only available at any chosen tabulated value of Q. Avratoglou and Voulgaris [71] provided an analysis and numerical solutions as graphs but no tables of computed values and no design equations fitted to the numerical results. Precise design values cannot be read from the graphs. Sokal [70] provides accurate design equations fitted to tabulated values in [66] at 50% duty cycle. The relationship among output power P_{out_inv}, load R, Q, V_{in} and transistor saturation voltage V_{sat} is least-squares fitted to the data in Table 1 in [66], over the entire range of Q from 1.789 to infinity, within a deviation of ±0.15% by a second order polynomial function of Q. These equations are accurate and simple enough for designers to easily manipulate.

$$P_{out\_inv} = \frac{(V_{in} - V_{sat})^2}{R} 0.576801(1.001245 - \frac{0.451759}{Q} - \frac{0.402444}{Q^2}) \tag{3.47}$$

Hence:

$$R = \frac{(V_{in} - V_{sat})^2}{P_{out\_inv}} 0.576801(1.001245 - \frac{0.451759}{Q} - \frac{0.402444}{Q^2}) \tag{3.48}$$

The design equations for C_s and C_r are given below.

$$C_s = \frac{8}{\omega R \pi(\pi^2 + 4)}(0.99866 + \frac{0.91424}{Q} - \frac{1.03175}{Q^2}) + \frac{0.6}{\omega^2 RFC} \tag{3.49}$$

$$C_r = \frac{1}{\omega R} \frac{1}{Q - 0.104823}(1.00121 + \frac{1.01468}{Q - 1.7879}) - \frac{0.2}{\omega^2 RFC} \tag{3.50}$$

Therefore, the choice of Q involves a trade-off among competing evaluation criteria. Lower Q means wider operating bandwidth, higher harmonic content and lower power loss in the parasitic resistance of the resonant circuit.

3.2.4. Analysis of rectifier

Fig. 3.11 shows a Class E zero-voltage-switching rectifier which consists of a diode D_3, a shunt capacitor C_{rec}, and a low pass filter L_f-C_f. DC power is delivered to load R_L. The rectifier is driven by a sinusoidal current source i_r from the resonant tank in the inverter. The C_{rec} shapes the voltage across the diode so that diode turns on and off at low dv/dt, reducing the loss at both transitions. The diode junction capacitance and winding capacitance of the filter L_f are absorbed into the shunt capacitance C_{rec}. The low pass filter should ensure the output voltage ripple within acceptable limits.

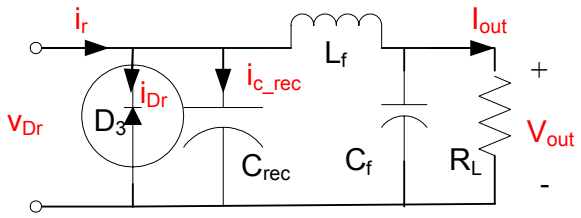


Fig. 3.11 ZVS rectifier

For convenience of analysis, assuming the current through L_f constant and equal to the output current I_{out}. The input current of the rectifier is:

$$i_r = I_m \sin(\theta + \Phi)$$

The diode has ON duty cycle Dr. The main operating waveforms are shown in Fig. 3.12.

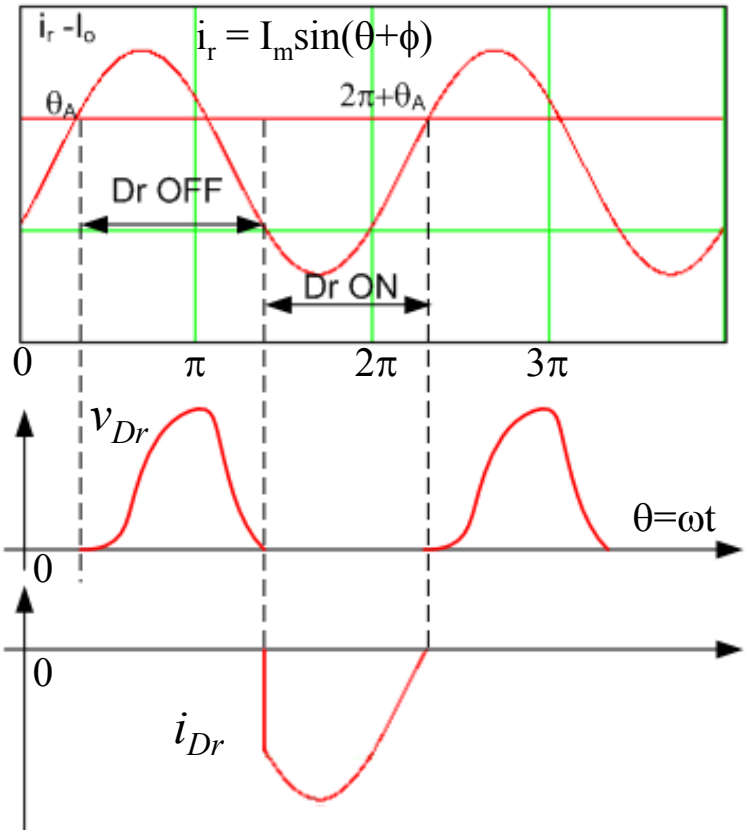


Fig. 3.12 Main waveforms of rectifier.

The current through the shunt capacitor C_{rec}:

$$i_{c\_rec}(\theta) = \begin{cases} I_m \sin(\theta + \Phi) - I_{out} & 0 < \theta \le 2\pi(1 - D_r) \\ 0 & 2\pi(1 - D_r) < \theta \le 2\pi \end{cases}$$

At $\theta = \theta_A$, $i_{c\_rec} = 0$

$$\Rightarrow \sin(\theta_A + \Phi) = \frac{I_{out}}{I_m}$$

$$\Rightarrow \theta_A = a\sin(\frac{I_{out}}{I_m}) - \Phi$$

When the diode is off, the voltage v_{Dr} across the diode is determined by the following expression:

$$v_{Dr}(\theta) = \frac{1}{\omega C_{rec}} \int_{\theta_A}^{\theta} i_{c\_rec}(\theta) d\theta = \frac{I_{out}}{\omega C_{rec}} [\frac{\cos(\theta_A + \Phi) - \cos(\theta + \Phi)}{\sin(\theta_A + \Phi)} - (\theta - \theta_A)]$$

The peak voltage across the diode can be determined by setting

$$\frac{dv_{Dr}(\theta)}{d\theta} = 0 \Rightarrow$$

$$V_{Dr\_\max} = \frac{I_{out}}{\omega C_{rec}}[\frac{2}{tg(\theta_A + \Phi)} - \pi + 2(\theta_A + \Phi)] \text{ when } \theta = \pi - \theta_A - 2\Phi$$

At the instant that the diode turns on, the voltage $v_{Dr}(\theta_A + 2\pi(1 - D_r)) = 0$

$$\Rightarrow tg(\theta_A + \Phi) = \frac{1 - \cos 2\pi D_r}{2\pi(1 - D_r) + \sin 2\pi D_r}$$

The average value of the voltage v_{Dr} should be equal to the output voltage V_{out}

$$V_{out} = \frac{1}{2\pi}\int_{\theta_A}^{2\pi+\theta_A} v_{Dr}(\theta)d\theta \Rightarrow$$

$$V_{out} = \frac{I_{out}}{2\pi\omega C_{rec}}\left[\frac{2\pi(1 - D_r) + \sin 2\pi D_r}{\tan(\theta_A + \Phi)} + 1 - \cos 2\pi D_r - 2\pi^2(1 - D_r)^2\right]$$

$$\Rightarrow \omega C_{rec} R_L = \frac{1}{2\pi}\left[\frac{2\pi(1 - D_r) + \sin 2\pi D_r}{\tan(\theta_A + \Phi)} + 1 - \cos 2\pi D_r - 2\pi^2(1 - D_r)^2\right]$$

$\omega C_{rec} R_L$ as a function of D_r is shown below (Fig. 3.13):

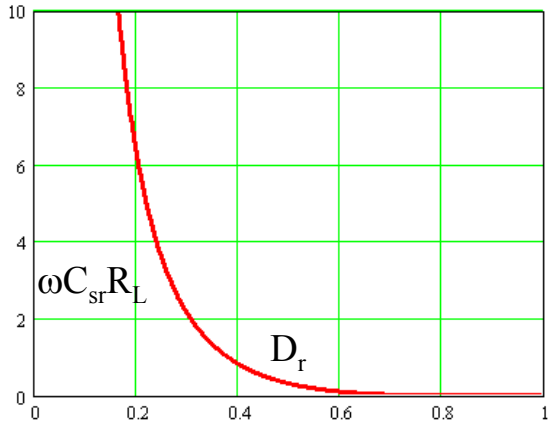


Fig. 3.13 $\omega C_{rec} R_L$ vs D_r .

The input power of the rectifier contains only the fundamental component due to the sinusoidal input current from the inverter. Therefore it is sufficient to determine the input impedance of the rectifier at the operating frequency. The input impedance of the rectifier is equivalent to an input resistance R_i in series with an input capacitance C_i (as shown in Fig. 3.14). The voltage $v_{Dr}(\theta)$ can be expanded into the Fourier series in such a

way that the sinusoidal component represents the voltage v_{Ri} across R_i , and the cosinusoidal component represents the voltage v_{Ci} across C_i at the frequency f .

The fundamental component of the voltage $v_{Dr}(\theta)$ can be expressed:

$$v_{Dr}(\theta) = v_{Ri} + v_{Ci} = V_{Rim}\sin(\theta + \Phi) - V_{Cim}\cos(\theta + \Phi)$$

where V_{Rim} and V_{Cim} are the amplitudes of fundamental components of voltages v_{Ri} and v_{Ci} across the equivalent input resistance R_i and C_i, respectively.

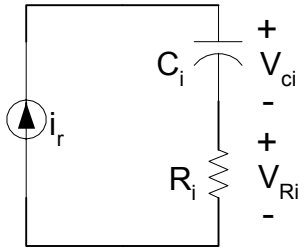


Fig. 3.14 Equivalent circuit of the rectifier

The V_{Rim} is given by

$$V_{Rim} = \frac{1}{\pi}\int_{\theta_A}^{2\pi+\theta_A} v_{Dr}(\theta)\sin(\theta + \Phi)d\theta$$

The equivalent input resistance R_i can also be derived as the following when neglecting the power losses.

Output power of the rectifier

$$P_{out} = {I_{out}}^2 R_L$$

Input power of the rectifier

$$P_{in\_rectifier} = \frac{1}{2}{I_m}^2 R_i$$

$$P_{out} = P_{in\_rectifier} \Rightarrow R_i = \frac{2{I_{out}}^2}{{I_m}^2} R_L = 2(\sin(\theta_A + \Phi))^2 R_L$$

The plot of $\frac{R_i}{R_L}$ versus D_r is shown in Fig. 3.15

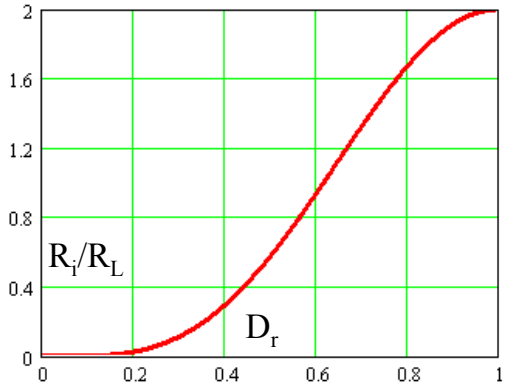


Fig. 3.15 R_i/R_L as a function of D_r.

Also $P_{out} = P_{in\_rectifier} \Rightarrow$

$$\frac{V_{out}}{V_{Rim}} = \frac{1}{2\sin(\theta_A + \Phi)}$$

The V_{Cim} is given by using Fourier formula

$$V_{Cim} = -\frac{1}{\pi}\int_{\theta_A}^{2\pi+\theta_A} v_{Dr}(\theta)\cos(\theta + \Phi)d\theta$$

Hence the input reactance of the rectifier at the operating frequency is given by

$$X_i = \frac{1}{\omega C_i} = \frac{V_{Cim}}{I_m}$$

Therefore the equivalent input capacitance of the rectifier is

$$\frac{1}{C_i} = \frac{1}{\pi C_{rec}}[\pi(1 - D_r) + \sin 2\pi D_r - \frac{1}{4}\sin 4\pi D_r \cos 2(\theta_A + \Phi) -$$

$$\frac{1}{2}\sin 2(\theta_A + \Phi)(\sin 2\pi D_r)^2 - 2\pi(1 - D_r)\sin(\theta_A + \Phi)\sin(2\pi D_r - (\theta_A + \Phi))]$$

Fig. 3.16 shows C_i/C_{rec} as a function of D_r. C_i/C_{rec} increases from 1 to infinity when D_r increases from 0 to 1.

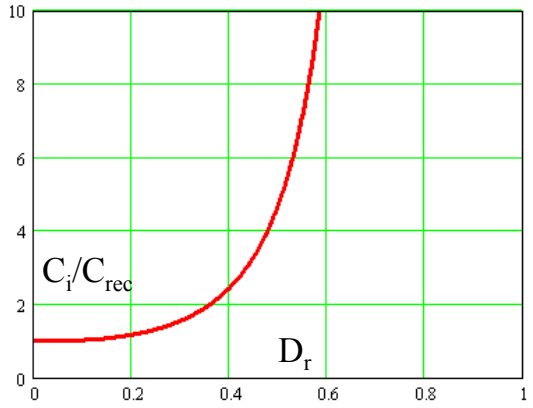


Fig. 3.16 C_i/C_{rec} vs D_r.

3.2.5. Resonant gate driver of Class E inverter

As the frequency increases, the power dissipation of gate drive becomes more significant. Because of the miller feedback effect of the gate-drain capacitance and the non-linearity of the device capacitance with drain-source voltage, the gate charge required to turn on a device is the best way to correctly predict the gate drive requirements. Two types of gate driver schemes are examined here: square-wave gate drive and sinusoidal resonant gate drive. The two driving schemes have different losses and current requirements for a given peak gate voltage and switching speed. The peak current requirements of each system are also different [75].

In the case of square-wave gate drive (Fig. 3.17), the energy stored in the gate capacitance during the charging process is determined as follows:

$$E_{gate} = \tfrac{1}{2} V_{gs} Q_g$$

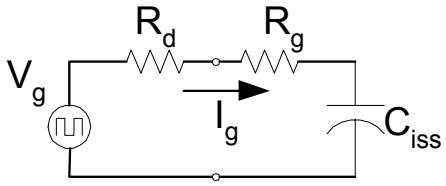


Fig. 3.17 Simplified equivalent gate drive circuit for the square wave drive.

The loss per switching cycle is two times E_{gate}, and given by

$$P_g = V_{gs} Q_g f_s$$

The time t_{on} that charges the gate capacitance to V_{gs} is determined by the time constant τ of the gate drive path. Typically, it takes a total time equal to 4τ to fully charge a capacitor up to V_{gs}.

$$t_{on} = 4\tau = 4(R_g + R_d)C_{iss}$$

The peak current in the gate drive is given by

$$I_{g\_peak} = \frac{V_{gs}}{R_d + R_g}$$

Thus the power requirement for the square-wave gate drive is independent of the switching speed, and the switching speed is ultimately limited by the gate resistance. Thus there is an intrinsic limit to how fast the gate can be charged, which becomes a factor as the frequency of operation increases [75].

In the case of sinusoidal resonant gate driver (Fig. 3.18), the input voltage is sinusoidal and the current is also sinusoidal if ignoring the non-linearity of the gate capacitance. Assuming that the required gate charge is Q_g and the sinusoidal gate drive signal has a frequency f_s, then the peak current needed to charge the gate from zero to V_{gs} during t_{on} is:

$$I_g = \frac{Q_g}{\int_0^{t_{on}} \cos(\omega_s t) dt} = \frac{Q_g \omega_s}{\sin(\omega_s t_{on})}$$

The peak voltage capability of the gates of the MOSFET will then clearly limit how fast one can switch the device with a resonant sinusoidal gate drive. The peak voltage across the gate of the device is given by

$$V_{gs\_peak} = \frac{V_{gs}}{\sin(\omega_s t_{on})}$$

Because the gate capacitance resonates with the resonant inductor L_d, the reactive impedance of the gate circuit is considered negligible. Thus the required input voltage is equal to

$$V_g = I_g (R_d + R_g)$$

and the power dissipation is:

$$P_g = \tfrac{1}{2} I_g^{\,2} (R_d + R_g)$$

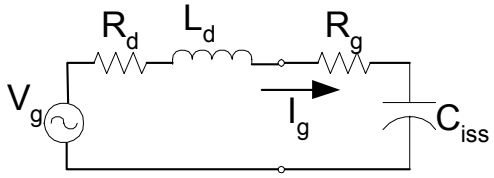


Fig. 3.18 Simplified equivalent resonant gate drive circuit

In contrast to the square-wave gate drive, the sinusoidal resonant gate drive is not limited in switching speed by the gate resistance, yet the power requirement is proportional to the resistances. By increasing V_g to increase the peak current I_g, the time it takes to reach a certain gate voltage can be reduced. The power loss of the gate drive can be reduced by reducing the drive resistance. Because in a resonant configuration, the energy stored in the gate gets stored for a half cycle in the resonant inductor and is recovered during the next half cycle. But with square-wave switching, the energy is always resistively dissipated.

In general the square-wave gate drive has more severe requirements than the resonant gate drive. The gate drive devices must be very fast and be capable of sourcing or sinking large currents. For example, to charge a 2000 pF capacitor in 10 ns to 10 V, total gate drive resistance must be equal to 1.25 Ω, the peak current is 8 A. For the sinusoidal gate drive, the peak gate current increases with frequency. The maximum current would occur at the highest operating frequency. For a given switching time, the highest operating frequency is when the switching time is a quarter of the switching period. Otherwise, the device never reaches either the fully on or the fully off condition. Thus the maximum frequency given a 10 ns switching time is 25 MHz. Under this worst case, the peak current is 3.14 A, less than that of the square-wave gate drive. Also the

lead inductance and leakage inductance can be absorbed into the resonant inductor L_d, but they have to be minimized for the square-wave drive [75].

Therefore the sinusoidal resonant gate driver is desirable to drive the switch in the Class E inverter due to the reduced losses and less severe requirements compared with square-wave gate driver. A self-oscillating resonant gate driver can be employed as described in [61][76][77][78][79]. The Class E inverter with a self-oscillating gate driver is shown in Fig. 3.19.

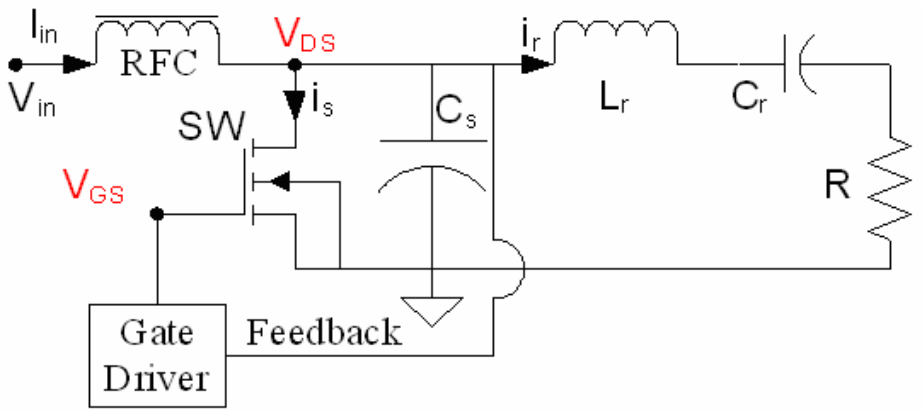


Fig. 3.19 Class E inverter with self-oscillating gate driver.

The design of feedback gate driver should satisfy the oscillation requirement at the desired operation frequency, i.e., $A(f)\cdot\beta(f)=1$ as shown in Fig. 3.20. Specific component values in the feedback circuitry are needed for operation at a desired frequency and to obtain the required phase shift between the input and output of the feedback network. The drain-source voltage v_{DS} is employed as the feedback signal. By properly shifting the fundamental component of the switch voltage v_{DS}, a sinusoidal gating signal is generated at the gate terminal to sustain the oscillation at the desired frequency.

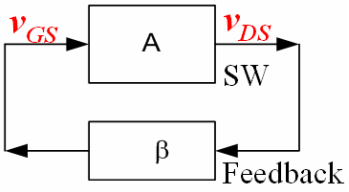


Fig. 3.20 General Feedback oscillation.

By referring to the operating waveforms of idealized Class E inverter shown in Fig. 3.21, the phase difference between the fundamental component of v_{DS} and the gate drive signal v_{gs} is 163.4°. The fundamental component v_{DS_fund} is already derived as shown in (3.31).

$$v_{DS\_fund}(\omega t) = 1.074V_{in}\sin(\omega t + \Phi) + 1.2378V_{in}\cos(\omega t + \Phi)$$
$$= 1.639V_{in}\sin(\omega t + 147.52° + 49.05°) = 1.639V_{in}\sin(\omega t - 163.43°)$$

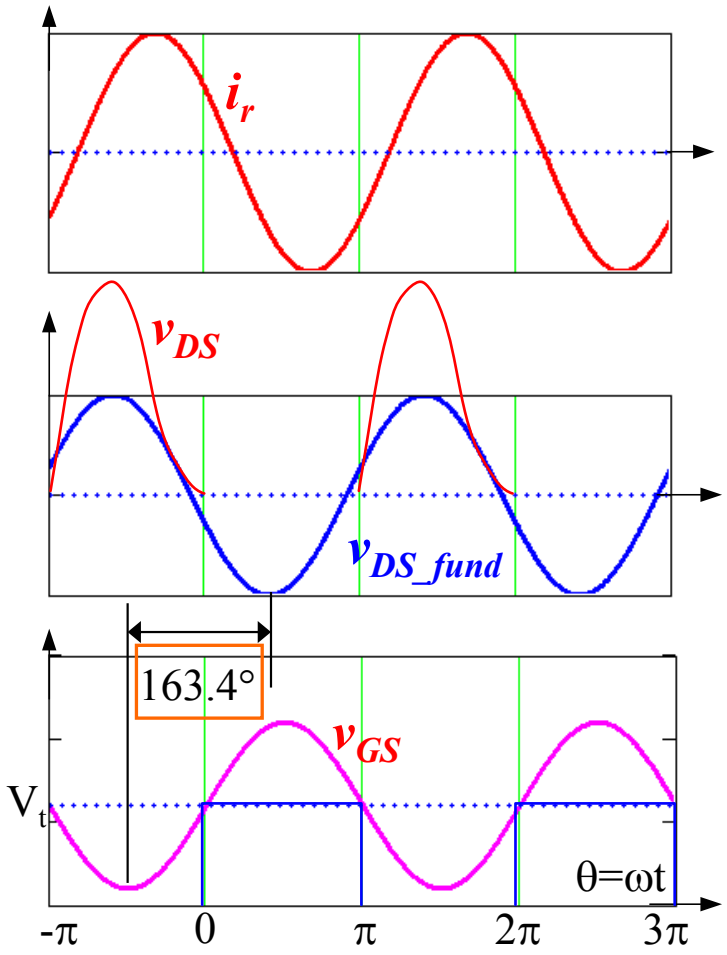


Fig. 3.21 Phase shift between gate signal and fundamental of drain-source voltage.

The sinusoidal gate driver signal can be expressed as follows:

$$v_{GS}(\omega t) = V_t + V_m \sin \omega t$$

V_t is the bias voltage applied to the gate, equal to the threshold voltage of the switch and keeping the duty cycle of the inverter at 50%. The basic feedback circuit can be implemented as in Fig. 3.22 to achieve the required phase shift. The amplitude of

fundamental component of v_{DS} is also attenuated to a value that ensures proper gate drive and is below the gate breakdown voltage ($V_{GS\_\max}$). The input impedance of feedback circuit at v_{DS} should be large enough to ensure that the operation of inverter is not significantly affected. Therefore a capacitor with small capacitance value is chosen for X_3 element in Fig. 3.22. Whether X_2 is an inductor or a capacitor depends on the other parameters in the feedback network and requirement to satisfy the oscillation.

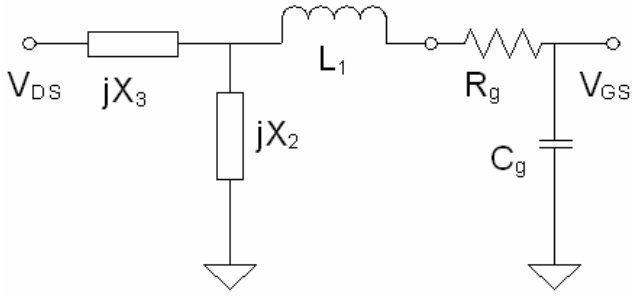


Fig. 3.22 Block diagram of basic feedback circuit.

Therefore a simplified feedback is proposed as shown in Fig. 3.23. The transfer function of the feedback circuit is given below. Element X_2 in Fig. 3.22 needs to be an inductor to meet the phase and amplitude requirement based on the circuit parameters. The frequency response of the transfer function V_{GS}/V_{DS_fund} is shown in Fig. 3.24. By properly adjusting the component values, the required amplitude and phase at the desired operating frequency can be obtained. The required phase 163.4° is obtained at 250 MHz as shown in Fig. 3.24. Resistor R_2 can be properly adjusted to set the magnitude and the precise frequency of oscillation. The function of L_1 and R_1 is to damp the second resonance apparent in the transfer function [61].

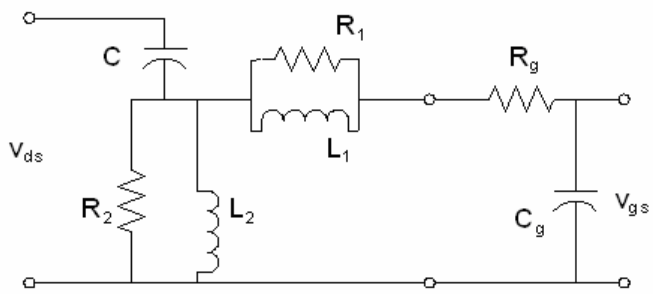


Fig. 3.23 Simplified feedback circuit.

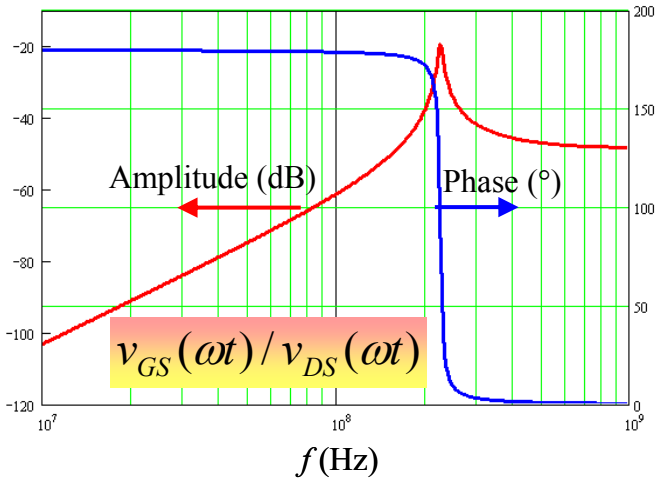


Fig. 3.24 Frequency response of V_{GS}/V_{DS_fund}.

$$\frac{V_{DS\_fund}}{V_{GS}} = \frac{\frac{L_2}{C_g} + \frac{L_1 + L_2}{C} - \omega^2 L_1 L_2 - \frac{1}{\omega^2 C C_g}}{\frac{L_2}{C_g}} + j\frac{\omega L_2 R_g - \frac{R_g}{\omega C}}{\frac{L_2}{C_g}}$$

$$= \frac{1.64 V_{in}}{V_m} \angle -163.4°$$

A simple control signal which starts and stops the operation of the inverter can be introduced as in [61] (Fig. 3.25). When control signal turns on the switch in the feedback circuit, the inverter stops operation due to low gate driving signal v_{GS}; When the switch in the feedback circuit is off, bias voltage V_{bias} charges C_{bias} through R_2. When the voltage v_{GS} exceeds the threshold voltage of the switch in the inverter, oscillation starts through the feedback network and keeps normal operation of the Class E inverter. Thus a control signal can be used to activate or terminate the inverter operation. During operation C_{bias} remains biased close to the threshold voltage of the switch in the inverter, keeping the duty cycle near 50%. Therefore, the voltage v_{GS} is a DC voltage superimposed with a sinusoidal voltage generated through the feedback network, which is exactly the desirable waveform as shown in Fig. 3.21. C_{bias} should be chosen for minimal impact on the feedback circuit.

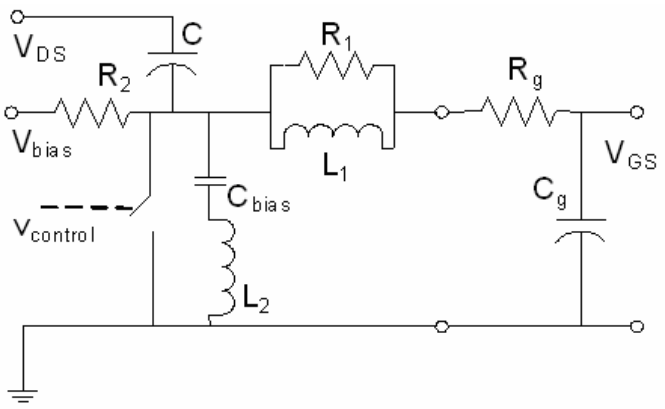


Fig. 3.25 Feedback oscillating gate driver.

3.2.6. Discussion of matching network between the inverter and rectifier

Now the complete DC-DC power converter derived from Class E power amplifier can be shown in Fig. 3.26. As stated in 3.2.1, in order to minimize the switching losses in the Class E inverter, the equivalent load of the inverter should satisfy the optimum load condition $R = R_{opt}$ or at least $R < R_{opt}$ to achieve zero-voltage turning-on in the switch. In many situations, the load of the inverter is different from the required optimum load. Therefore a matching network is required between the inverter and the rectifier to provide the impedance transformation.

There are several methods to design the matching networks [26][80]. At low frequencies (HF and VHF), the impedance matching network is usually achieved with lumped element circuits, usually if the circuit size is much smaller than the wavelength ($l < \frac{\lambda}{10}$). Distributed components are often used at higher frequencies where the component or circuit size is comparable with wavelength.

The rectifier can be equivalent to R_i in series with C_i at the operating frequency as previously stated in Analysis of rectifier. This means that the impedances to be matched

have reactive components. As a general rule, the reactive component of the load impedance must be compensated by a convenient reactance seen at the input of the matching network, so the transformed impedance is a purely resistive load.

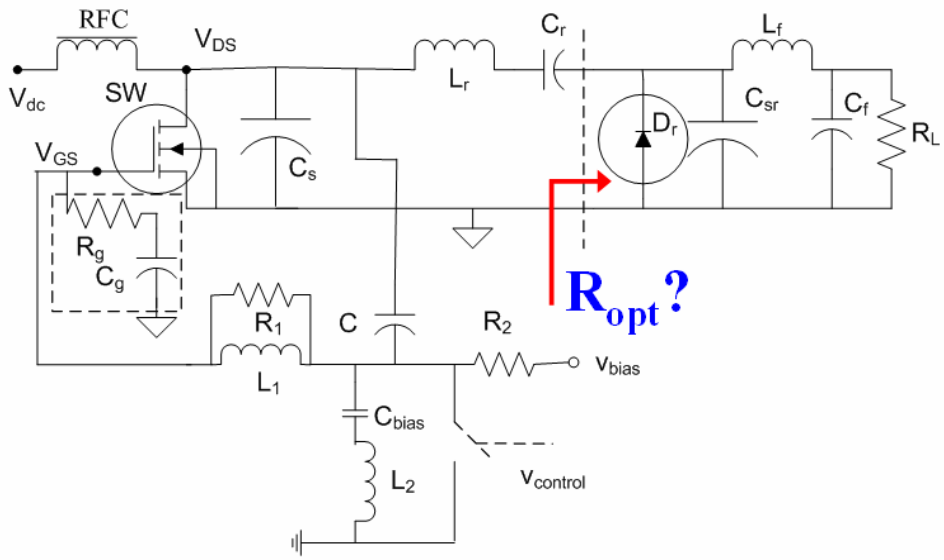


Fig. 3.26 RF DC-DC power converter.

When the required optimum load R_{opt} of the inverter is larger than equivalent resistance R_i of the rectifier, the matching network shown in Fig. 3.27 can be employed.

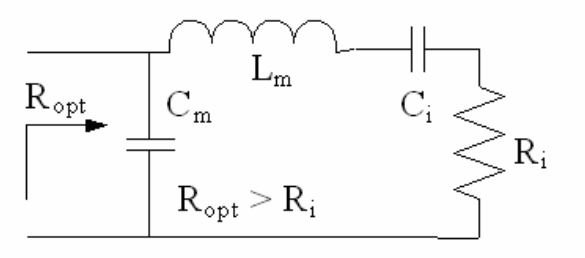


Fig. 3.27 Matching network for $R_{opt} > R_{pi}$.

The design equations are:

$$L_m = \frac{1}{\omega} R_i \sqrt{\frac{R_{opt}}{R_i} - 1} + \frac{1}{\omega^2 C_i}$$

$$C_m = \frac{1}{\omega} \frac{\sqrt{\frac{R_{opt}}{R_{pi}} - 1}}{R_{opt}}$$

If $R_{opt} < R_i$, firstly the series R_i - C_i is converted to a parallel resistance-capacitance combination as shown in Fig. 3.28. The following relations can be obtained:

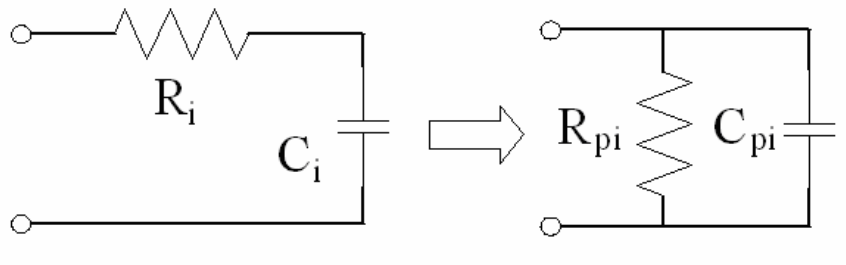


Fig. 3.28 Series combination conversion into parallel combination.

$$R_{pi} = R_i[1 + (\frac{1}{\omega C_i R_i})^2]$$

$$C_{pi} = \frac{C_i}{1 + (\omega C_i R_i)^2}$$

Then the parallel impedance can be converted into the optimum load R_{opt} by the L matching network as shown in Fig. 3.29.

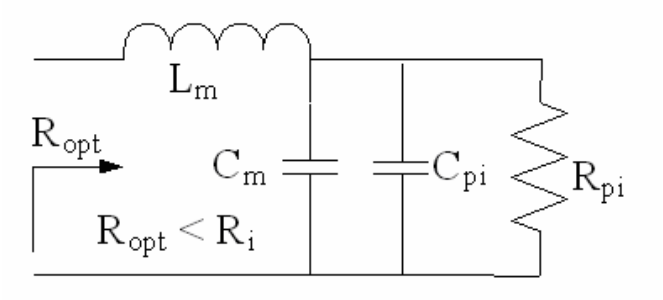


Fig. 3.29 Matching network for $R_{opt} < R_{pi}$.

The design equations are given by

$$L_m = R_{opt} \frac{1}{\omega} \sqrt{\frac{R_{pi}}{R_{opt}} - 1}$$

$$C_m = \frac{1}{\omega} \frac{\sqrt{\frac{R_{pi}}{R_{opt}} - 1}}{R_{pi}} - C_{pi}$$

The two-reactance matching network above is the simplest among the various matching techniques. However it has its own limitations in some cases such as: no

solution for some combinations of matched impedance; impractical values obtained (too large or too small values of capacitors and inductors); no design flexibility. In such situations the three-reactance matching networks can be used to realize the impedance transformation. Usually one of the impedance matching circuits can meet the design requirements with practical component values. Four-reactance matching networks allow exact impedance matching at two distinct frequencies and are appropriate for broadband impedance matching. When the operating frequency is sufficiently high (e.g. > 1GHz), the use of transmission-line sections as matching network becomes practical due to the short lengths required.

3.2.7. Experimental results and discussion

The implementation of the converter is referred to Appendix I. For the given specifications below: f =250 MHz, R_L =20 Ω, V_{out} =4.5 V, V_{in} =10 V, the component values of the circuit are listed in Table 3.1 (refer to Fig. 3.30).

Table 3.1 Component values of RF DC-DC power converters.

Component	Value	Part number
RFC	120nH	Coilcraft:1812SMS-R12
L_r	5nH	Coilcraft: A02T
L_1	5nH	Coilcraft: A02T
L_2	5nH	Coilcraft: A02T
L_f	120nH	Coilcraft:1812SMS-R12
C_{bias}	1nF ×2	ATC100B102
C_r	24pF×2	ATC100B240
C_f	10 nF	AQ125C103
C	0.5pF	AQ12EA0R5
R_1	200 Ω	Standard SMD
R_2	4.64 k Ω	Standard SMD
SW		L8711P
D_r		SL02

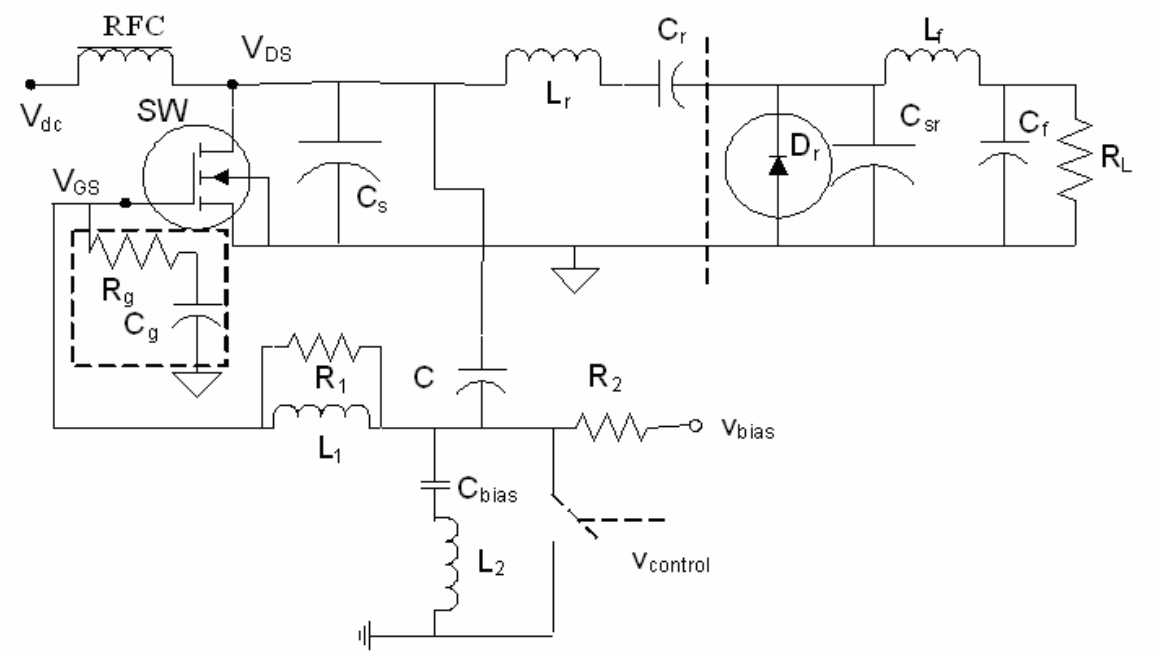


Fig. 3.30 The proposed RF DC-DC power converter.

The prototype is shown in Fig. 3.31. The dimension of the prototype is L×W×H = 3×2×0.4 (cm).

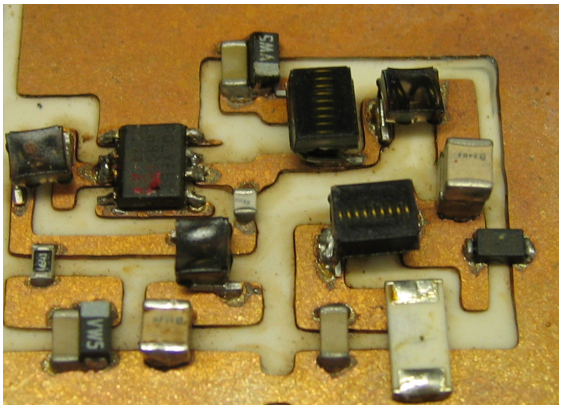


Fig. 3.31 Prototype of RF DC-DC power converter at 250 MHz.

When the input voltage is 10 V and load is 20 Ω, the measured drain-source voltage of the switch SW is shown in Fig. 3.32. The corresponding gate driver signal is measured as shown in Fig. 3.33, the output voltage is shown in Fig. 3.34.

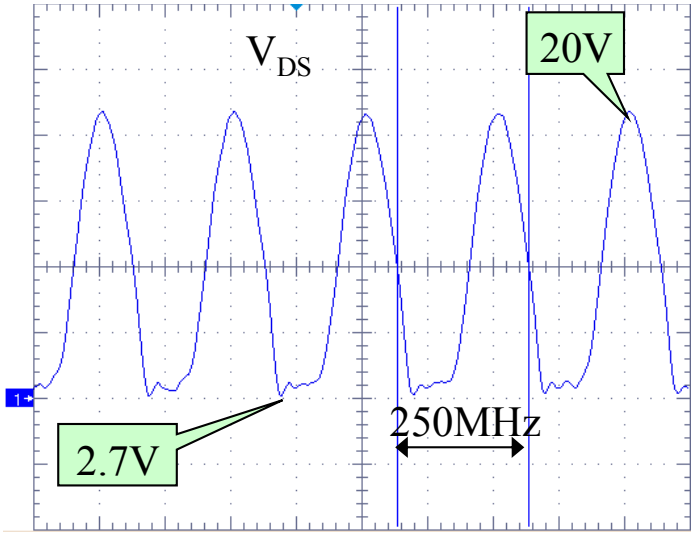


Fig. 3.32 Drain-source voltage of SW at 250 MHz operating frequency.

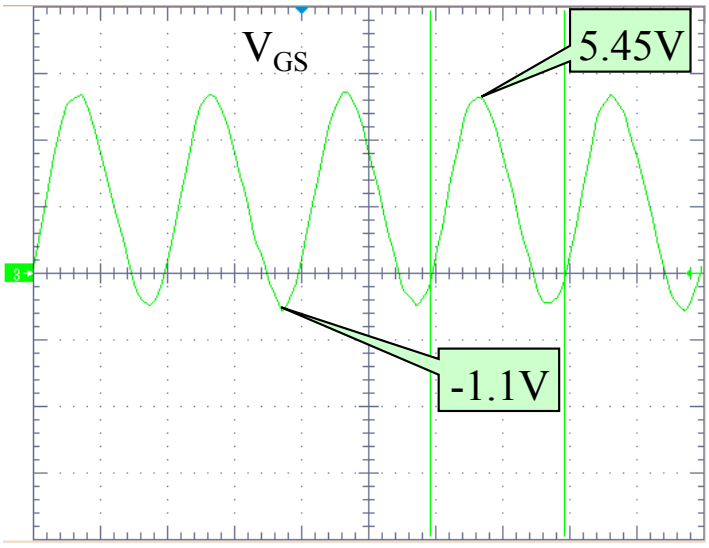


Fig. 3.33 Gate driver signal of SW in the DC-DC converter.

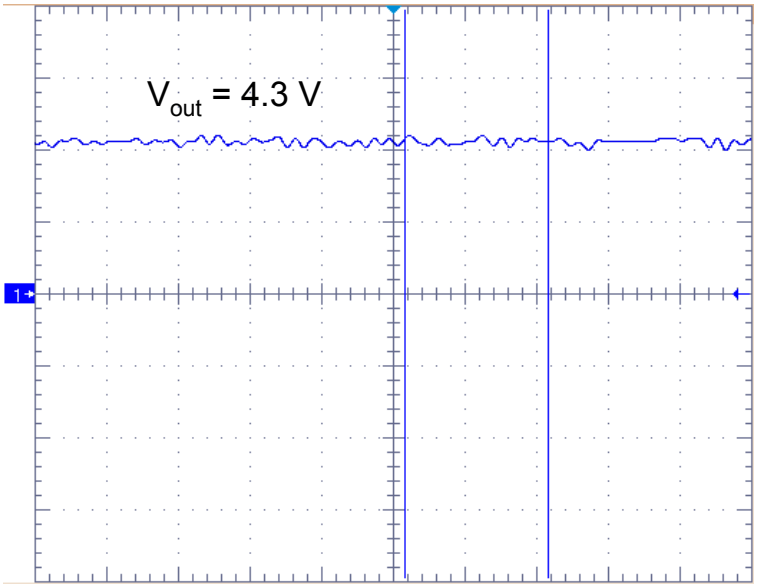
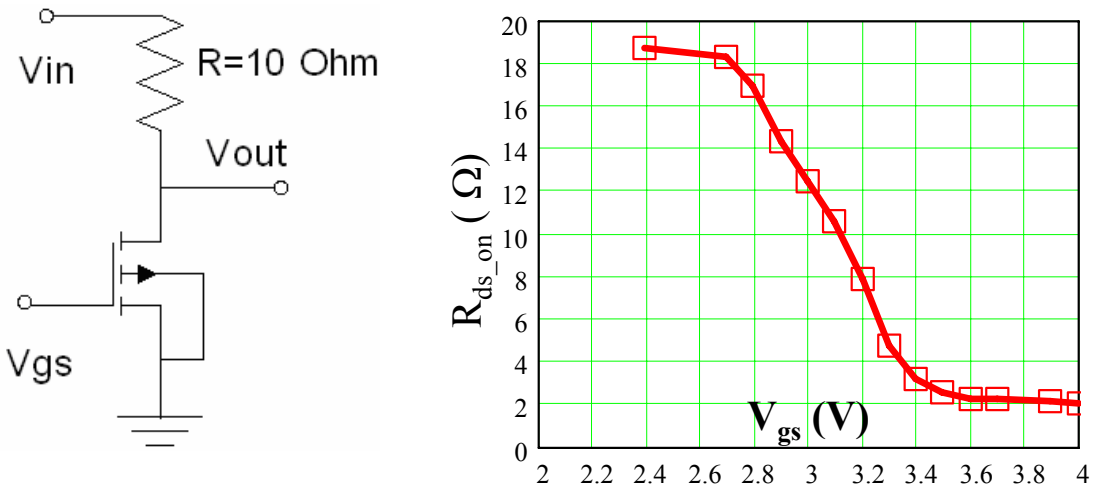


Fig. 3.34 Output voltage of the converter.

The switching frequency, 250 MHz, is significantly higher than those found in conventional DC-DC converters. This is the highest switching frequency implemented by discrete surface-mounted components. The output voltage across the load 20 Ohm is 4.28 V for 10 V, 0.2 A input. Only 46% efficiency is obtained for this prototype. By investigating the temperature distribution of the circuit board, the hottest part is located at the SW which dissipates most of the power. Based on the circuit shown in Fig. 3.35 (a) to test the ON-resistance of the LDMOS L8711P employed in the prototype, the relationship between ON-resistance and gate voltage is obtained in Fig. 3.35 (b). The bias voltage of the self-oscillating gate driver is set at V_{bias} = 2.6V to achieve 50% duty cycle. The ON-resistance of the SW corresponding to the bias voltage is about 18 Ω from Fig. 3.35 (b). ON-resistance of the switch can be reduced by increasing the bias voltage, but duty cycle is reduced at the same time, which results in lower efficiency and lower output power (Fig. 3.36). Therefore a better power device with lower ON-resistance should be chosen to improve the efficiency. It is expected that the efficiency could be increased up to around 70%.



(a) (b)

Fig. 3.35 R_{ds_on} of SW vs gate-source voltage.

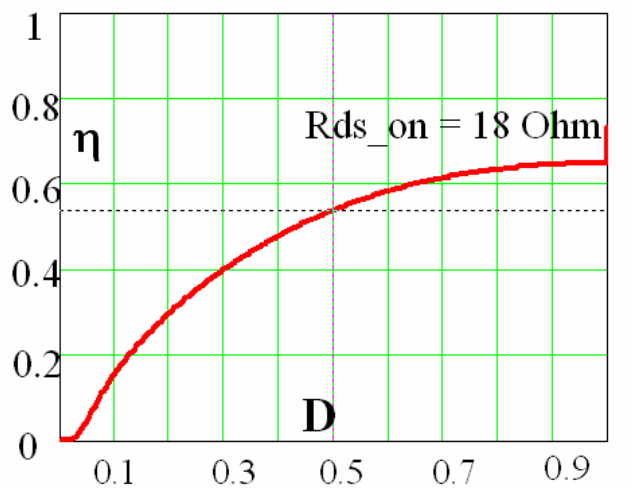


Fig. 3.36 Efficiency vs Duty cycle for 18Ω ON-resistance.

Another problem exists with the discrete passive components and interconnects in the circuit [83][92][93][94][95]. In reality, the passive components, especially the component in the resonant circuit, are not lumped. They are distributed along the transmission line on which is placed. The physical size of the passive components can result in significant errors in estimating the values of components when they are used at radio frequencies. The interconnects (or traces) between the components are in fact microstrip transmission lines. Thus all these effects contribute to the deviation of the designed circuit from the optimum operation condition. Take for example a look at the chip capacitor mounted as shown in Fig. 3.37. The copper traces on each side of the

capacitor act like a piece of microstrip line having characteristic impedance Z_0. The capacitor can be considered as a transmission line section (characteristic impedance Z_{0C}) along the vertical height h. The actual capacitive part lies in the middle of the structure shown in Fig. 3.37, which can also be represented by a transmission line model at RF frequencies. The equivalent circuit model for this configuration is shown in Fig. 3.38. This circuit model can be incorporated to analyze its effects on the performance of the converter. There are various configurations for the passive components in RF power converter. Each configuration and mechanical orientation has different parasitic parameters, which should be individually analyzed.

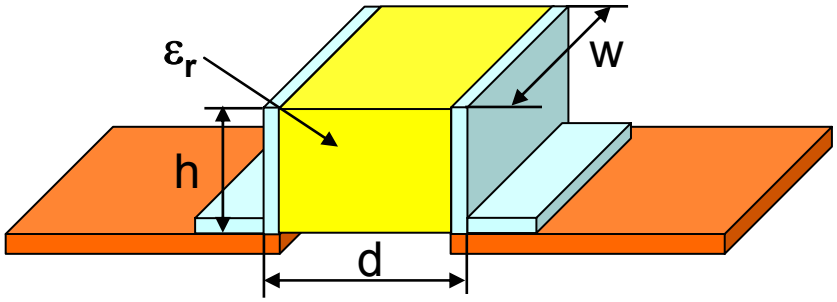


Fig. 3.37 Series mounting of a chip capacitor on the circuit board.

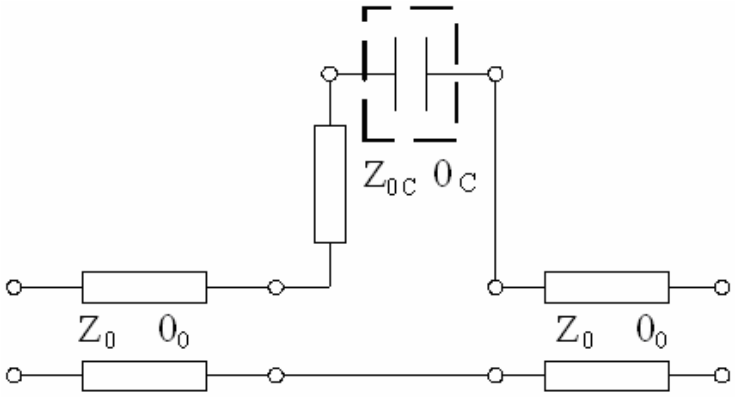


Fig. 3.38 Equivalent circuit model of structure above.

In order to improve the efficiency of RF DC-DC converter, it is important to employ a better LDMOS with lower ON-resistance in the future, which will significantly increase the efficiency. By operating at lower switching frequency, the efficiency of the power converter can be increased through reduced switching losses and reduced

distribution effects of the interconnects and passive components. More complete and complicated analysis of the converter would be required to consider the practical or nonlinear features of components in the circuit to obtain more desirable performance. For example, the nonlinear shunt capacitance in the Class E inverter should be included in the design procedure [96][97][98][99] to obtain optimum component values.

In summary, a 250 MHz, 2 W RF DC-DC power converter based on Class E inverter was demonstrated with discrete components in this chapter, with a power density about 14 W/in^3 for dimension L×W×H = 3×2×0.4 (cm). The relationship between the power level and the frequency of this converter follows the trend limited by the power-frequency product, as illustrated in Fig. 3.39.

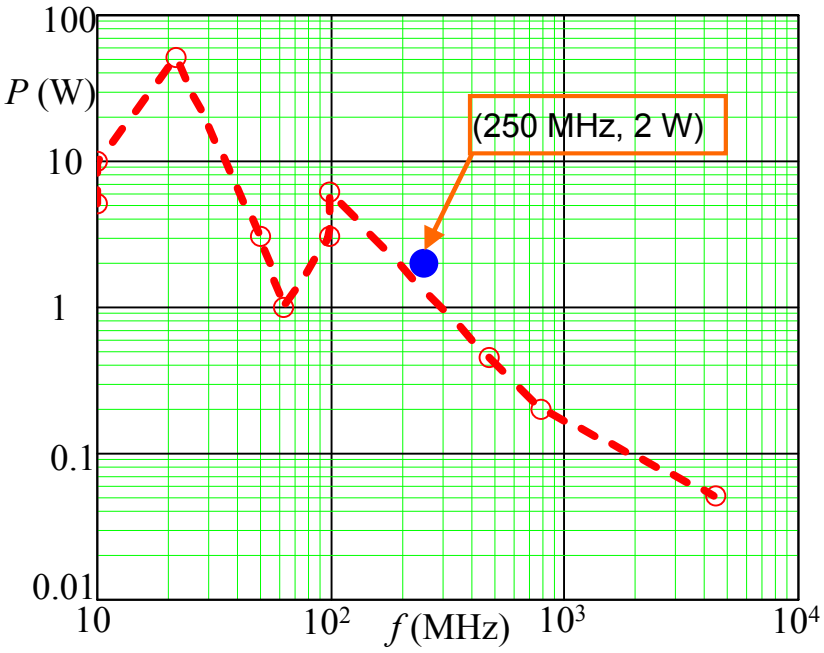


Fig. 3.39 Trend-line between power level and frequency of the selected converters.

The power device in the converter plays an important role in determining the overall efficiency. To minimize the power losses in the semiconductor devices, there have been concerted efforts to reduce the ON-resistance of the device. At present, several MOSFET devices achieve mΩ values of ON-resistances, but they are limited to low frequency applications. However for HF/VHF applications, it is necessary to not only

reduce the ON-resistance but the device capacitance as well for higher efficiency. ON-resistance can be reduced by increasing the device die area, but leading to a corresponding increase in the input capacitance of the device. For power devices, the conduction losses are directly proportional to ON-resistance. The switching power losses depend on the transition times which are proportional to the input capacitance of the device. Therefore, the efficiency of a power device may be represented by ON-resistance R_{on} and input capacitance C_{in}.

The total power loss in a power device is comprised of conduction losses and switching losses. Assuming the switching losses are mainly due to the charging and discharging of the input capacitance in a power device, then the total power loss is given by

$$P_{dis} = {I_{rms}}^2 R_{on} + C_{in} {V_G}^2 f$$

ON-resistance and input capacitance can be represented by their specific on-resistance and specific capacitance, respectively, as [100]

$$R_{on} = \frac{R_{on,sp}}{A}, \text{ and } C_{in} = C_{in,sp} \cdot A,$$

Both $R_{on,sp}$ and $C_{in,sp}$ are determined by the material properties and design rules of the device. So

$$P_{dis} = {I_{rms}}^2 \frac{R_{on,sp}}{A} + C_{in,sp} \cdot A \cdot {V_G}^2 \cdot f$$

The minimum power loss occurs when the conduction loss is equal to the switching loss. The minimum value of power loss is

$$P_{dis,\min} = 2 I_{rms} V_G \sqrt{f R_{on,sp} C_{on,sp}}$$

at a device area given by

$$A = \frac{I_{rms}}{V_G} \sqrt{\frac{R_{on,sp}}{C_{in,sp}}} \sqrt{\frac{1}{f}} = \frac{I_{rms}}{V_G} R_{on,sp} \sqrt{\frac{1}{R_{on,sp} C_{in,sp}}} \sqrt{\frac{1}{f}}$$

A conclusion can be made from equation above that in order to reduce power loss and improve the efficiency, it is necessary to minimize the product of $R_{on,sp}$ and $C_{in,sp}$. For

a given semiconductor material, $R_{on,sp}$ and $C_{in,sp}$ are also given. So the minimum power loss increases with increasing frequency f and gate drive voltage V_G. The optimum die area decreases with increasing frequency and gate drive voltage. On the other hand, when the switching frequency and gate drive voltage are given, the smaller the product of $R_{on,sp}$ and $C_{in,sp}$ is, the less the power loss is and the larger the die area is. Therefore, the best semiconductors for high frequency power conversion should exhibit small product of $R_{on,sp}$ and $C_{in,sp}$.

The product of $R_{on,sp}$ and $C_{in,sp}$ may be regarded as a criterion to evaluate the efficiency of a power device. In fact $R_{on,sp}$ and $C_{in,sp}$ can be expressed in terms of the material properties [100].

$$R_{on,sp} = \frac{4V_B^{\,2}}{\varepsilon_s \mu E_{bk}^{\,3}}, C_{in,sp} = \frac{\varepsilon_s E_{bk}}{2\sqrt{V_G V_B}}$$

where V_B is breakdown voltage, ε_s is the dielectric constant, μ is the carrier mobility, E_{bk} is the breakdown field. Then

$$R_{on,sp} C_{in,sp} = \frac{2V_B^{\,1.5}}{\mu E_{bk}^{\,2}\sqrt{V_G}}$$

$$P_{dis,\min} = \sqrt{\frac{8I_{rms}^{\,2} V_G^{\,1.5} V_B^{\,1.5} f}{\mu E_{bk}^{\,2}}}$$

$$A_{\min} = \sqrt{\frac{8I_{rms}^{\,2} V_B^{\,2.5}}{f\varepsilon_s V_G^{\,1.5} \mu E_{bk}^{\,4}}}$$

It can be seen that the product of $R_{on,sp}$ and $C_{in,sp}$ is inversely proportional to the product of μ and E_{bk}^2. The power loss will increase with increasing frequency, but decrease with the increasing product of μ and E_{bk}^2. Therefore in terms of materials, the best semiconductor devices should exhibit a large breakdown electric field and a large mobility, which leads to reduced power loss and die area.

In Table 3.2, the products of μ and E_{bk}^2 normalized to Si of several semiconductor materials are listed. Again GaAs, SiC and GaN power devices demonstrate less power losses than Si devices due to their better material properties. Among these semiconductor materials, the distinguished physical properties of GaN again give GaN-based power conversion technology extremely high potential for HF/VHF power conversion applications.

Table 3.2 Properties of several semiconductor materials

	Si	GaAs	4H SiC	6H SiC	GaN
Bandgap E_G (eV)	1.1	1.4	3.2	3	3.4
E_{bk} (10^5 V/cm)	5.7	6.4	33	30	40
v_s (10^7 cm/s)	1	2	2	2	2.5
μ (cm^2/Vs)	1350	8500	610	340	1200
k (W/cm-K)	1.5	0.5	4.5	4.5	2.1
$(E_{bk}v_s)^2$	1	5	134	110	308
μE_{bk}^2	1	8	15	7	44

Combined with the power-frequency limit described previously, it is clear that the first fundamental frequency limitations of HF/VHF power conversion ultimately depend on the material properties of the semiconductors employed in the power converters. The semiconductor materials with higher breakdown field, higher mobility and higher drift velocity are desirable for high efficiency, high power and high frequency power conversion. When the semiconductor material is given, the power-frequency product, and the product of specific ON-resistance and specific device capacitance are given. When ON-resistance is lowered, input capacitance of the device becomes larger, which means that device should operate at a lower switching frequency for keeping the efficiency but larger output power is possible. Operating at lower switching frequency, on the other hand, means reduced switching losses, and reduced parasitic effect and distributed effects of interconnects among the components. Therefore there are optimum power density and efficiency existing for some frequency range, beyond which the degraded power density and efficiency will occur. Consequently, it is necessary to develop devices from other materials in the future in order to maximize the power density and efficiency by pushing frequency.

Chapter 4 Fundamental Frequency Limitations of Passive Components for HF/VHF Power Conversion

4.1. Background

Over the past several decades the volume reduction in power converters can chiefly be attributed to increases in switching frequency. In keeping this trend towards miniaturization and higher levels of integration to improve the power densities of power converters (with present dielectric and magnetic materials), higher switching frequencies will be required while maintaining or improving the efficiency. In theory, an increased frequency of operation reduces the required amount of pulsed energy storage per cycle, thus reducing the volume occupied by the dominating magnetic and electric energy storage elements in power converters. At the same time it is very important to maintain a high efficiency when raising the switching frequency, without exceeding permissible temperature rises as the volume or cooling areas decrease.

Improvements in converter performance, size, weight and cost along with the increasing switching frequency have been achieved mainly through the technological advances and improvements in devices, materials, components and circuit designs, packaging techniques, and better thermal management. Therefore efforts to achieve higher power density while maintaining or improving efficiency by means of pushing switching frequencies involves coupled multi-disciplinary issues in electrical, thermal, mechanical, and material properties of the components and packaging [106][107].

Semiconductor device technology has been one of the major enablers for pushing switching frequencies. Device size has been reduced to a level where it is no longer the primary determining factor of packaging volume of a converter [3] at present. The

switching losses in the semiconductor devices have also been on a steady decline with the improvements in device technology, device types, driving and novel circuit techniques. Clearly devices don't impose the fundamental limitations inhibiting advances in power conversion technologies at the present stage, though there are still some limitations to future development, such as the power-frequency limits and power loss limitations with increasing frequency that were described in previous chapters.

Compared to the 3~4 orders of magnitude volume reduction and performance improvements in the power device, it is clearly the inadequate performance of passive components where we must turn our attention to. In seeking equal or greater benefit by reducing volumes of passive components more commensurate with those of the power devices, radical increases in switching frequency are required with today's materials. Unfortunately, no major breakthroughs have been achieved in the passive materials for high frequency operation and passive components still dominate the volumes of power converters. The dielectric materials in the capacitive components and the magnetic materials in the magnetic components are frequency-dependent and produce non-linear energy storage and power dissipation as a function of frequency. It is then also necessary to investigate the effects of these materials on power conversion performance of power converter as the switching frequency increases. At the same time developments and advances in new and improved magnetic and dielectric materials are necessary.

To keep up with the steps brought about by pushing switching frequency, improvements in packaging, thermal management, integration, EM characteristics, control and circuitry are all necessary. As the applications drivers continue to raise demands for reduced profile and increased power density there is also a tendency towards higher levels of integration and a tendency to push for higher frequencies. Yet, a three-dimensionally integrated power electronics technology must also be developed to address major issues and improve the characteristics of high frequency power converters. These technologies promise great potential in lowering interconnections impedances, improving thermal management and reducing profile [3][106][107][112]][113]. The technologies being developed include planar metallization to allow 3D integration of power devices

and control functions, the integration of passive components to increase power density, and advanced cooling strategies, as these dominate the volumes of power converters.

Given this background it is essential to explore the frequency scaling effects of integrated passive components for high frequency power conversion [101]-[105]. A methodology is developed to theoretically analyze and maximize frequency and performance of passive components for power conversion in terms of efficiency and power density, considering materials, thermal management, packaging and in-circuits functions among others. This is also an attempt to answer the question "what is the optimum power conversion frequency for a particular integrated passive component of a certain technology in my circuit, given all the specifications and the design freedom that I have?"

Apparently the investigation of frequency scaling effects in integrated passive components involves complex and coupled multi-disciplinary issues (see Fig. 4.1). Successfully addressing this issue will help to identify the tradeoffs between different performance functions and optimize the design.

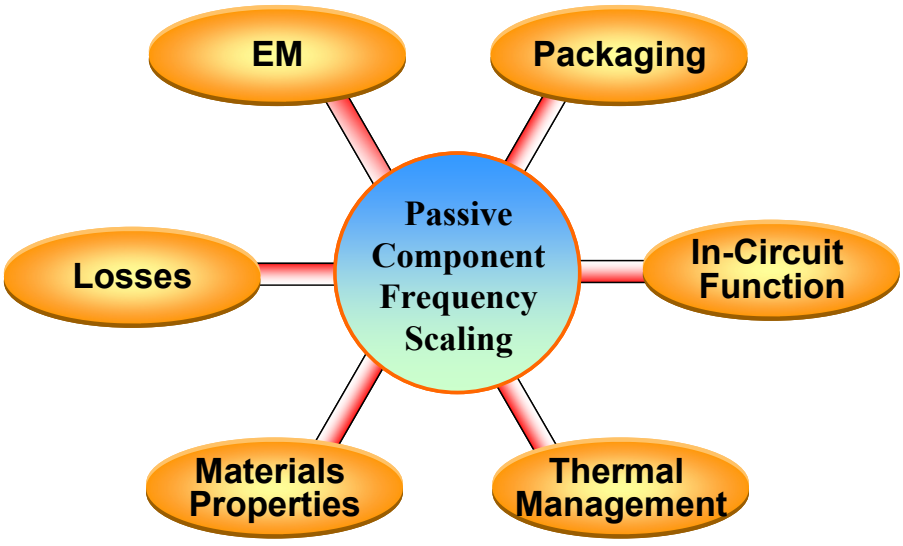


Fig. 4.1 Multi-disciplinary issues of passive component frequency scaling investigation.

4.2. Setting up the model

Definitions of parameters

Analyzing the effects of frequency scaling on passive components is a complex multi-disciplinary task, involving many issues such as packaging, materials properties, thermal-, electromagnetic-, and loss mechanisms and in-circuit functions. In order to develop a reasonable methodology for analyzing the performance as a function of all these parameters, it is necessary to constrain the problem in some ways and specify variables in others that will facilitate the analysis.

For this purpose, three kinds of parameters are defined in the analysis below. These are:

- inflexible constraints,
- discretized parameters and
- design variables.

The inflexible constraints are usually determined by specifications such as the rated nominal and boundary electrical values and relationships at the component terminals, the maximum temperature, operating limits and so on. During the design stage these parameters must remain fixed in strict adherence to these design specifications.

The next category, discretized parameters, involves a set of parameters that belong to slightly more relaxed constraints in the design. For instance, the design itself may not be limited to a specific packaging technology or materials. However, during the iteration in the design stage it may be convenient to stick to a specific manufacturing technoology implicitely owning its own set of limitations, or make a selection of materials that are available only in certain thicknesses, i.e. the thickness of magnetic or dielectric layers, thickness of copper, number of turns in a winding, the properties of available materials, real estate dimensions, profile, etc.

The remaining category allows continuous adjustment over a given range, such range having been set by one of the previous parameter categories. The performance of passive components can then be evaluated by the few remaining design variables over which the designer has most control, such as the operating frequency, various component dimensions or impedance ranges, among others.

Thermal Model

As switching frequency increases, the specific losses in the passive components materials rise exponentially, resulting in raised temperatures. The temperature is determined by how efficiently heat generated in the components is removed to the ambient. Each material used in constructing a capacitor or a magnetic component has a maximum temperature beyond which its performance will start to deteriorate, and in the worst instances, destroy the component. Hence the component temperature must be kept at or below the permissible values for proper operation and reliability. If the temperature is too far below the maximum value, then the component form factor has usually not been optimized. In other words, for a given component, there is only one optimum temperature, and this is a maximum.

In structures and configurations that comprise different materials sharing the heat flux, the optimum temperatures are assumed to be influenced by one another. The maximum temperature in the structure is then chosen such that the highest possible temperature is reached in each material (which may not be its individual optimum temperature), without exceeding the maximum temperature in any material. This means that the structure is designed so that the operating temperature of at least one material is optimized, and the temperatures of the remaining materials will be at or below their individual optima. In the analysis that follows the components are analyzed by themselves and the optimum temperature is associated with only one material. These temperatures can therefore be categorized under either the inflexible constraints or under the discretized parameters. The thermal limits imposed by the design specifications, for instance minimum ambient temperature or the maximum temperature of the coolant, are

considered to be inflexible design constraints, as the designer does not have control over them.

The model will be applied to an example of a packaging technology. In addition, the simplest components, having only one layer of dielectric or permeable material, and single layers of conductors, are treated. This severs only to illustrate the methodology, and it should be kept in mind that the model is completely extendable to other planar embodiments that are not limited in this way.

The passive components are considered to be in planar form as depicted in Fig. 4.2, with cooling structures such as heat sinks, heat spreaders, air flow or coolant, or other means for providing the cooling function. A single layer of dielectric or magnetic material is sandwiched between the copper layers. It is further assumed that the convection from the top surface is negligible in the analysis and the top surface is adiabatic. This is reasonable, because the upward heat flowing is relatively small in relation to the heat flowing downwards towards the cooling surface, especially in a hermetically sealed packaging or an encapsulated environment, which is usual in military, space and aerospace applications where spatial volume (or weight) is a luxury. It is further assumed that power dissipation is uniformly distributed in the copper layers and in the dielectric or magnetic material. This is not always true, but since we are aiming at high frequency applications, the real estate occupied by the component is very small, which also means that the temperature distribution on the cooling surface can be considered even as the thermal conductivities of the materials don't scale with the conceptual size reduction. Due to the large thermal conductivity of copper compared to the other materials, the temperature gradient inside the thin copper layer can also be neglected.

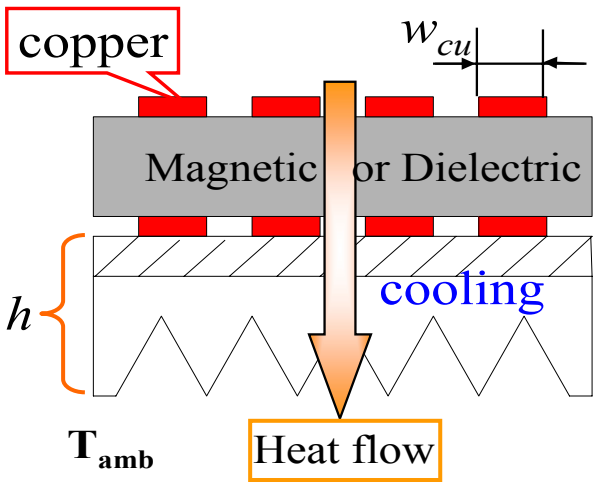


Fig. 4.2 Structure of the integrated planar passive components.

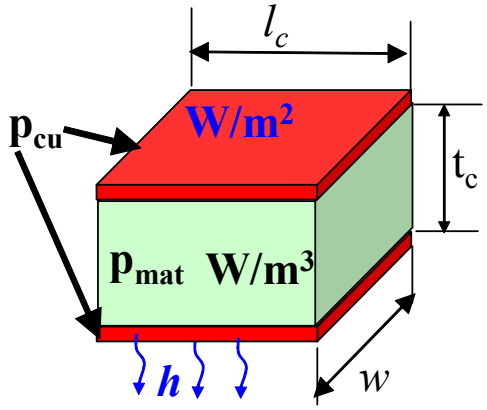


Fig. 4.3 Simplified thermal model of integrated passive components.

The structure of Fig. 4.2 can now be simplified to an even simpler model as shown in Fig. 4.3. Here p_{mat} [W/m^3] represents uniform volumetric losses in the dielectric or magnetic material, and p_{cu} [W/m^2] represents uniform copper losses per unit area, and h is equivalent to cooling effects (heat sink, air flow etc.). The maximum temperature T_{max} occurs at the topmost copper layer (x=0) (refer to Fig. 4.4). The differential equation governing the heat flow [114] is given as

$$\frac{\partial^2 T}{\partial x^2} + \frac{p_{mat}}{k_c} = 0 \qquad (4.1)$$

The boundary conditions are specified by

$$\frac{p_{cu}A_s + p_{mat}A_s t_c + p_{cu}A_s}{hA_s} = T\big|x = t_c - T_{amb} \qquad (4.2)$$

$$p_{cu} A_s = -k_c A_s \frac{\partial T}{\partial x} \Big| x = 0 \qquad (4.3)$$

The general solution to (4.1) is

$$T(x) = -\frac{p_{mat}}{2k_c} x^2 + C_1 x + C_2 \qquad (4.4)$$

From the boundary conditions,

$$C_1 = -\frac{p_{cu}}{k_c} \text{ and } \quad C_2 = \frac{p_{mat}}{2k_c} t_c^{\,2} + \frac{p_{cu}}{k_c} t_c + \frac{2p_{cu} + p_{mat} t_c}{h} + T_{amb}$$

Therefore the maximum temperature at $x = 0$ is

$$T_{\max} = \frac{p_{mat}}{2k_c} t_c^{\,2} + \frac{p_{cu}}{k_c} t_c + \frac{2p_{cu} + p_{mat} t_c}{h} + T_{amb} \qquad (4.5)$$

where k_c [W/m·°C] is the thermal conductivity of the dielectric or magnetic material, T_{amb} [°C] is the ambient temperature, t_c is the thickness of the dielectric or magnetic layer, and A_s is the surface area. Clearly, the maximum temperature is related to the power dissipation in the copper layer and dielectric or magnetic layer. It also depends on the thermal conductivity of the passive layer and its thickness.

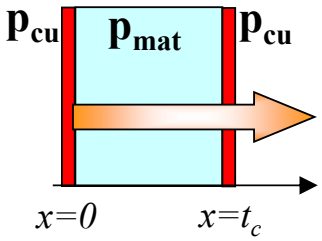


Fig. 4.4 Heat transfer of the simplified thermal model.

4.3. Performance of Magnetics as a function of frequency

Frequency Characteristics of magnetic material

When a magnetic material is subjected to a sinusoidal time-varying magnetic field it creates a phase shift between the flux density, B, and magnetic field intensity, H, due to magnetic losses. Therefore, the permeability of magnetic materials is a complex number having a real part corresponding to energy storage and an imaginary part representing losses [115]:

$$\mu_c = \mu_{real} - j\mu_{imag} \tag{4.6}$$

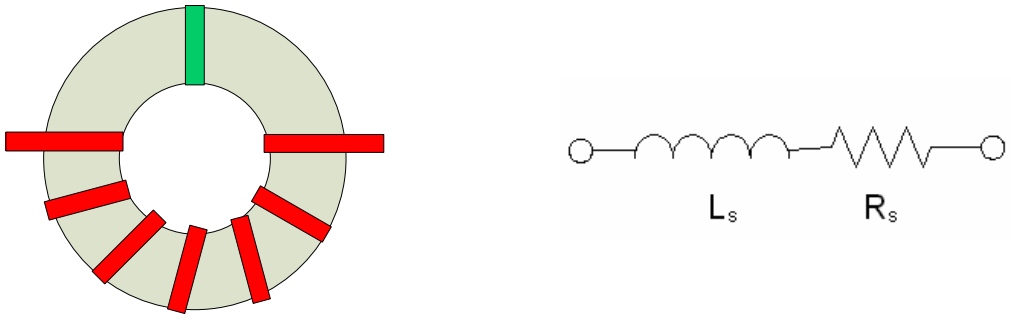
This is useful for predicting magnetic losses for power applications. Since an inductor under sinusoidal excitation dissipates some energy, its impedance is given by the series combination of a resistance R_s and inductance L_s under sinusoidal excitation:

$$Z = j\omega L_s + R_s = j\omega L_0 \frac{\mu_{real} - j\mu_{imag}}{\mu_0} \tag{4.7}$$

where L_0 is the air core inductance, R_s is related to the imaginary part of the complex permeability and represents the losses in the component. For a simple toroidal core with cross section, A_c, path length, l_c, and N turns of winding (Fig. 4.5), we have

$$L_s = \frac{\mu_{real}}{\mu_0} L_0 = \mu_{real} \frac{N^2 A_c}{l_c} \tag{4.8}$$

$$R_s = \frac{\omega\mu_{imag}}{\mu_0} L_0 = \omega\mu_{imag} \frac{N^2 A_c}{l_c} = \omega L_s \frac{\mu_{imag}}{\mu_{real}} \tag{4.9}$$



(a) Toroidal core inductor. (b) Series equivalent circuit.

Fig. 4.5 Toroidal inductor and its series equivalent circuit.

The values of equivalent series circuit parameters R_s and L_s can be measured directly by using an impedance analyzer [116]. Then the real and imaginary parts of the complex permeability can be obtained from (4.8) and (4.9) as functions of frequency.

The complex permeability is frequency-dependent [115][117]-[119]. A relaxation formula may be used to describe the frequency-dependent behavior of complex permeability as shown in (4.10).

$$\mu_{real} = \frac{\mu_{c0}}{1+(f/f_r)^2}$$

$$\mu_{imag} = \mu_{c0}\frac{f/f_r}{1+(f/f_r)^2} \qquad (4.10)$$

The loss tangent is given by

$$\tan\delta_m = \frac{\mu_{imag}}{\mu_{real}} \qquad (4.11)$$

where μ_{c0} is permeability at low frequency, f_r is cut-off frequency, which can usually be determined by measurement. Behavior of the real and imaginary part of the complex permeability is shown in Fig. 4.6.

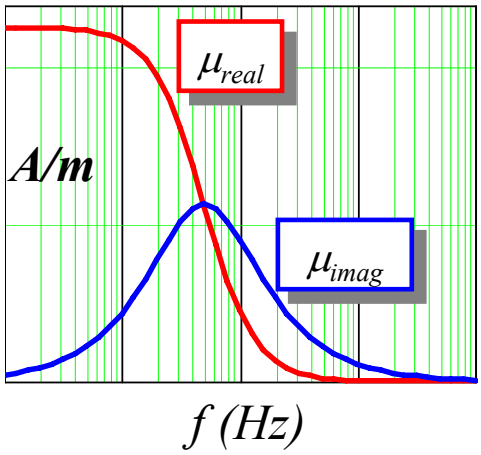


Fig. 4.6 Frequency dependency the complex permeability.

This simple theoretical model is in a good fit to the measurements [117][118][119] in some cases. However, it is only in good for some materials with single relaxation time. As pointed out in [120], the behavior of the complex permeability is interpreted as a superposition of two relaxation mechanisms: domain-wall motion and magnetic moment rotation [120]. Also three types of relaxation processes exist: a) electron diffusion; b)

diffusion of cations; c) single ion relaxation [115]. All these phenomena and other reasons such as grain-size dependence [117] can result in a distribution of relaxation time constant and inaccurate representation of the complex permeability with (4.10). So the modification of (4.10) is necessary to match the measured frequency characteristics of the specific magnetic core. Take 3F4 magnetic core for instance and referring to the measured complex permeability, for example, as given by Ferroxcube, the real and imaginary parts of the complex permeability are expressed as (4.12). Fig. 4.7 depicts their frequency-dependent characteristics.

$$\mu_{real} = \frac{\mu_{c0}}{1+(f/f_r)^4}$$

$$\mu_{imag} = 1.8\mu_{c0}\frac{(f/1.6f_r)^{2.5}}{1+(f/1.6f_r)^{4.5}} \qquad (4.12)$$

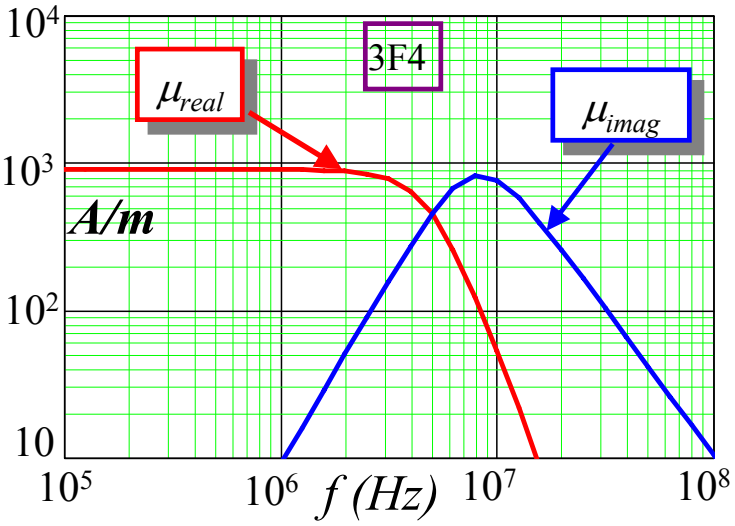
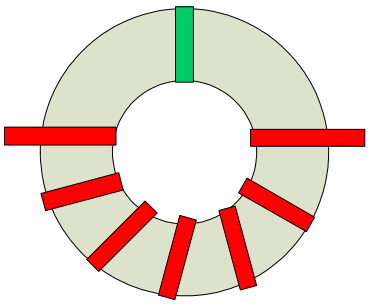


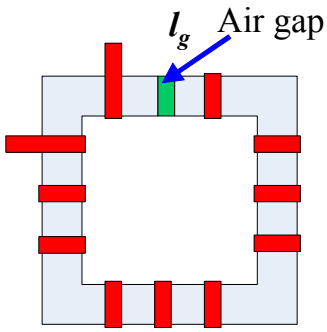
Fig. 4.7 Complex permeability of 3F4 as a function of frequency.

Performances analysis of magnetics as frequency increases

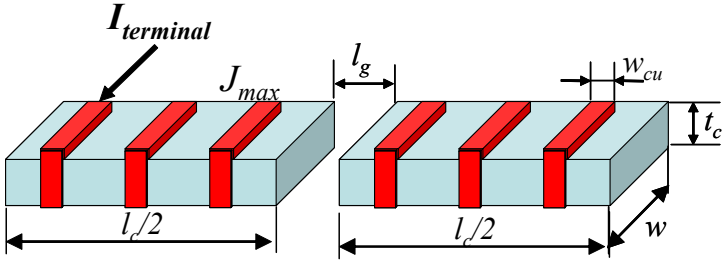
The integrated planar inductors in Fig. 4.8(a) to Fig. 4.8(c) are used as examples to maximize the power density and efficiency by varying frequency and dimension. The inductors can be implemented in several types as shown and can be simplified to the representation in Fig. 4.8(d).



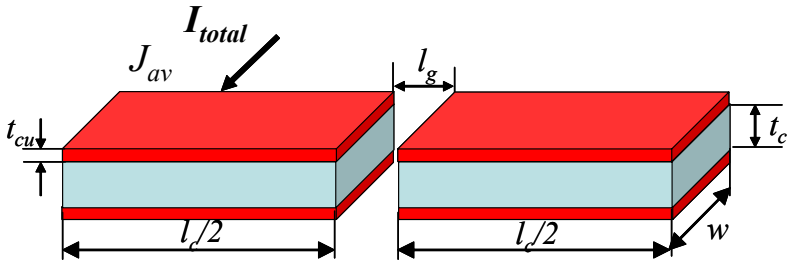
(a) Toroidal inductor.



(b) Integrated planar inductor.



(c) Integrated planar inductor.



(d) simplified model of integrated planar inductor.

Fig. 4.8 Various equivalent integrated planar inductors.

In these figures, l_g is the length of an air gap, l_c is the length of the magnetic core, w is the width of the core, t_c is the thickness of the core, t_{cu} is the thickness of the copper layer, J_{max} is the maximum current density in the copper winding, $I_{terminal}$ is the current through each winding, J_{avg} is the average current density in the copper plate, and I_{total} is the total current through the copper plate. If the number of winding is N, then

$$I_{total} = N \cdot I_{terminal} \quad (4.13)$$

$$I_{total} = J_{av} t_{cu} l_c \quad (4.14)$$

$$I_{terminal} = J_{\max} t_{cu} w_{cu} \quad (4.15)$$

Define the winding factor

$$k_{cu} = \frac{Nw_{cu}}{l_c} \tag{4.16}$$

Then substitute (4.14) and (4.15) into (4.13), we get

$$J_{av} = k_{cu} J_{\max} \tag{4.17}$$

From Ampere's law:

$$I_{total} = H_c l_c + H_g l_g = \frac{B_c}{\mu_c} l_c + \frac{B_g}{\mu_0} l_g \tag{4.18}$$

where μ_c is the permeability of the core, B_c is the magnetic flux density in the core, B_g is the magnetic flux density in the air gap.

The fringing factor k_f is defined to take into account the fringing effect in the air gap as

$$k_f = \frac{B_g}{B_c} \tag{4.19}$$

So from (4.18), (4.19) and (4.14),

$$B_c = \frac{J_{av} t_{cu}}{\frac{1}{\mu_c} + \frac{k_f}{\mu_0} k_g} = \mu_e J_{av} t_{cu} \tag{4.20}$$

where form factor k_g is defined as

$$k_g = \frac{l_g}{l_c} \tag{4.21}$$

The effective permeability due to the air gap is defined as

$$\mu_e = \frac{\mu_c}{1 + k_f k_g \frac{\mu_c}{\mu_0}} \tag{4.22}$$

$$\mu_e = \mu_{e\_real} - j\mu_{e\_imag} \tag{4.23}$$

The inductance of the inductor is expressed by

$$L = N^2 \frac{w \cdot t_c}{\frac{l_c}{\mu_{e\_real}}} = N^2 \mu_{e\_real} t_c k_w \tag{4.24}$$

Form factor k_w is defined as

$$k_w = \frac{w}{l_c} \tag{4.25}$$

The stored energy in the inductor is

$$E = \frac{1}{2} L I_{ter\min al}{}^2 = \frac{1}{2} N^2 \mu_{e\_real} t_c k_w (\frac{I_{total}}{N})^2 \Rightarrow$$

$$E = \frac{1}{2} \mu_{e\_real} t_c J_{av}{}^2 t_{cu}{}^2 w l_c \tag{4.26}$$

The energy per unit area is

$$E_s = \frac{E}{w l_c} = \frac{1}{2} \mu_{e\_real} J_{av}{}^2 t_{cu}{}^2 t_c = \frac{1}{2} \mu_{e\_real} J_{\max}{}^2 k_{cu}{}^2 t_{cu}{}^2 t_c \tag{4.27}$$

The total losses in the inductor consist of copper losses in the winding and magnetic losses in the core, both of these loss values are related to the maximum current density $J_{\max}$. The copper loss per unit area is

$$p_{cu} = \frac{\frac{1}{2} I_{ter\min al}{}^2 R_w}{l_c w} = \frac{J_{\max}{}^2 w_{cu}{}^2 t_{cu}{}^2 N w}{2 l_c w \sigma w_{cu} t_{cu}} = k_{cu} \frac{J_{\max}{}^2 t_{cu}}{2\sigma} \tag{4.28}$$

where σ is the electrical conductivity of copper.

The magnetic loss per unit volume in the inductor is given by

$$p_{mag} = \frac{\frac{1}{2} I_{ter\min al}{}^2 R_s}{vol} \tag{4.29}$$

Here $I_{ter\min al} = J_{\max} w_{cu} t_{cu}$, $R_s = \omega \mu_{e\_imag} N^2 \frac{w \cdot t_c}{l_c}$, $vol = l_c \cdot w \cdot t_c$, thus

$$p_{mag} = \frac{1}{2} \omega \mu_{e\_imag} k_{cu}{}^2 J_{\max}{}^2 t_{cu}{}^2 \tag{4.30}$$

The total power dissipation in the inductor should keep the temperature below the allowable maximum value according to (4.5). Substituting the copper loss density equation (4.28) and the magnetic loss density equation (4.30) into (4.5), the maximum current density $J_{\max}$ is derived as

$$J_{\max}{}^2(f,k_g)=\frac{T_{\max}-T_{amb}}{\frac{1}{2}(\frac{t_c{}^2}{2k_c}+\frac{t_c}{h})\omega\mu_{e\_imag}(f,k_g)k_{cu}{}^2t_{cu}{}^2+(\frac{t_c}{k_c}+\frac{2}{h})\frac{k_{cu}t_{cu}}{2\sigma_{cu}}} \quad (4.31)$$

The planar inductor shown in Fig. 4.8 is now taken as a case study. The design parameters are defined in Table 4.1. Some performance values, such as maximum current density, energy density, power density and efficiency can be derived and quantified as a function of frequency or dimension, which will be shown in the following parts.

Table 4.1 Definition of design constraints.

Inflexible constraints	Discretized constraints	Design variables
$T_{\max}=100°C$ $T_{amb}=25°C$	Thickness of core: $t_c=4$ mm	Frequency: f
	$h=10$ W/m^2-°C	Form factors: k_g, k_w
	Properties of magnetic material	Thickness of copper:
	Numbers of winding turns	($t_{cu}=10$ μm)

For the following example a 3F4 ferrite core is chosen, where $k_c=5$ W/m·°C, $\mu_{c0}=900\mu_0$, $f_r=5$ MHz. The complex permeability is shown in Fig. 4.7. Winding factor, $k_{cu}=N\cdot w_{cu}/l_c$, is also taken into account in the analysis and $k_{cu}=0.8$ in the example below. The fringing factor k_f is set to be 0.9 for the analysis.

According to (4.31), under such constraints conditions the maximum current density through the winding is plotted in Fig. 4.9. When the switching frequency increases, the losses in the inductor also increase. The current density then needs to be derated to keep the temperature rise, which is an inflexible constraint.

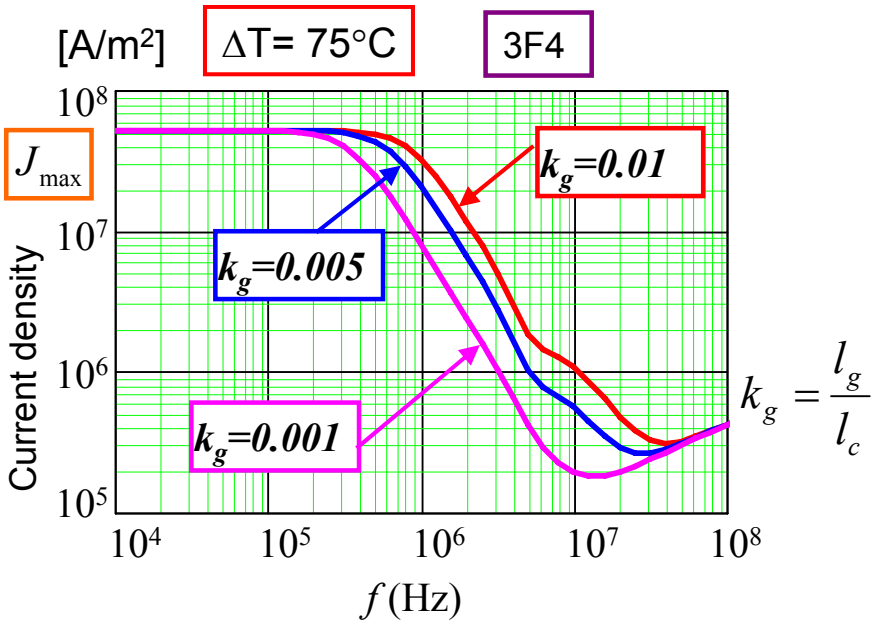


Fig. 4.9 Maximum current density as a function of frequency.

The energy density as a function of frequency is plotted for k_g = 0.01, 0.005 and 0.001 (Fig. 4.10). For a constant switching frequency, the relationship between the energy density and the form factor k_g is plotted in Fig. 4.11. Energy density is also derated as frequency increases. For any given frequency, there is a maximum energy density that depends on k_g.

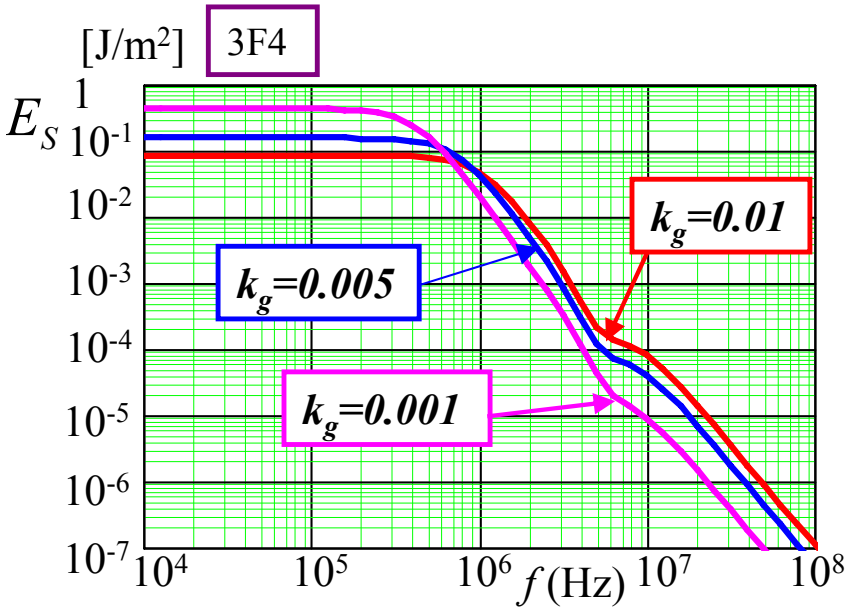


Fig. 4.10 Energy density as a function of frequency.

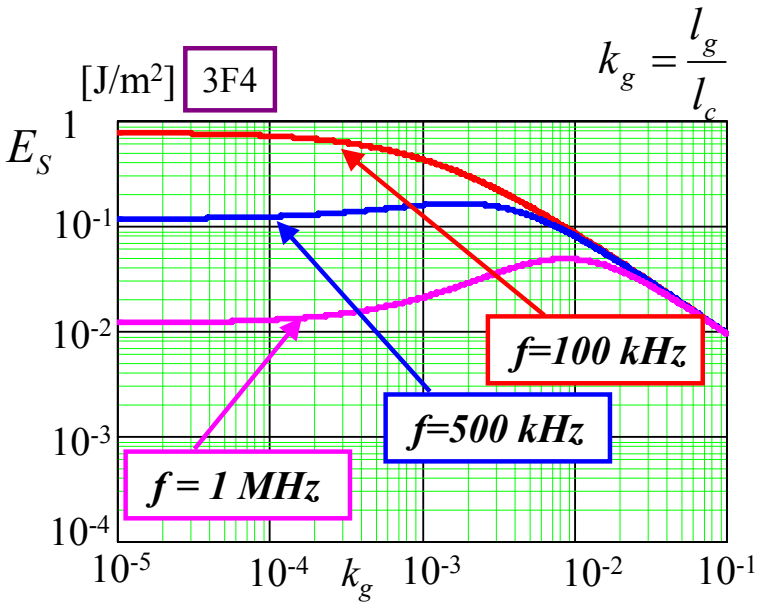


Fig. 4.11 Energy density as a function of k_g for different frequency.

The volumetric power density of the inductor is

$$P_V = \frac{E_s f}{t_c} \tag{4.32}$$

The volumetric power loss density is

$$P_{d\_V} = p_{mag} + \frac{p_{cu}}{t_c} \tag{4.33}$$

The power conversion efficiency is defined as

$$\eta = 1 - \frac{P_{d\_V}}{P_V + P_{d\_V}} \tag{4.34}$$

The power density P_V and power loss density P_{d_V} as a function of frequency are plotted in Fig. 4.12. Fig. 4.13 shows the relationship between the power density and the form factor k_g for the different switching frequencies. Power conversion efficiency as a function of frequency and form factor k_g is illustrated in Fig. 4.14 and Fig. 4.15, respectively.

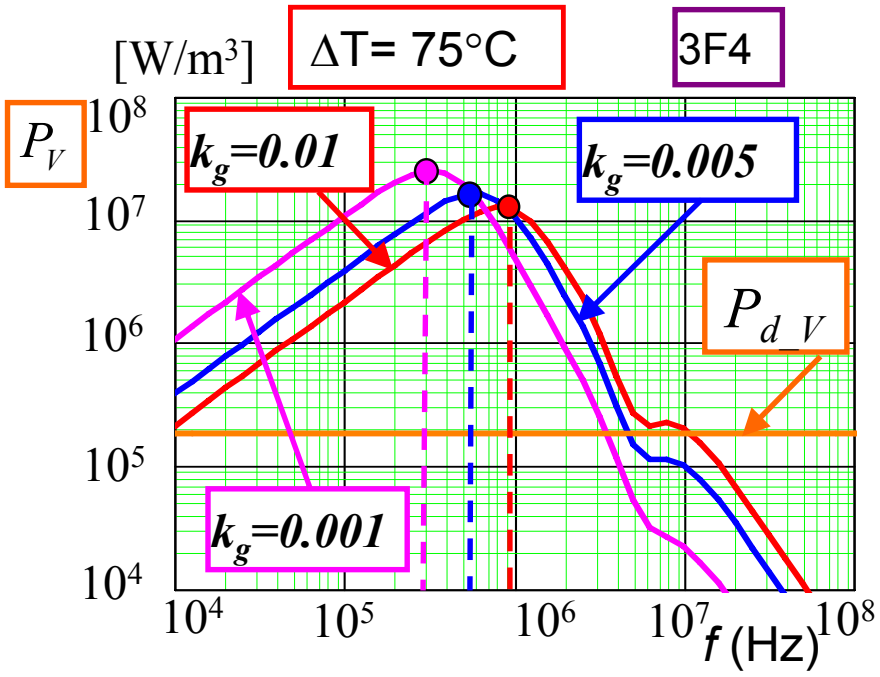


Fig. 4.12 Power density as a function of frequency.

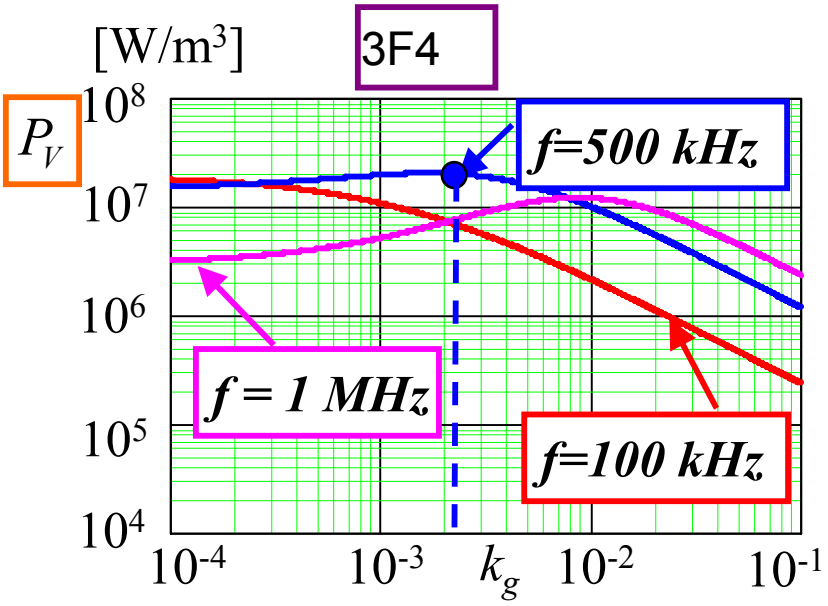


Fig. 4.13 Power density as a function of form factor k_g.

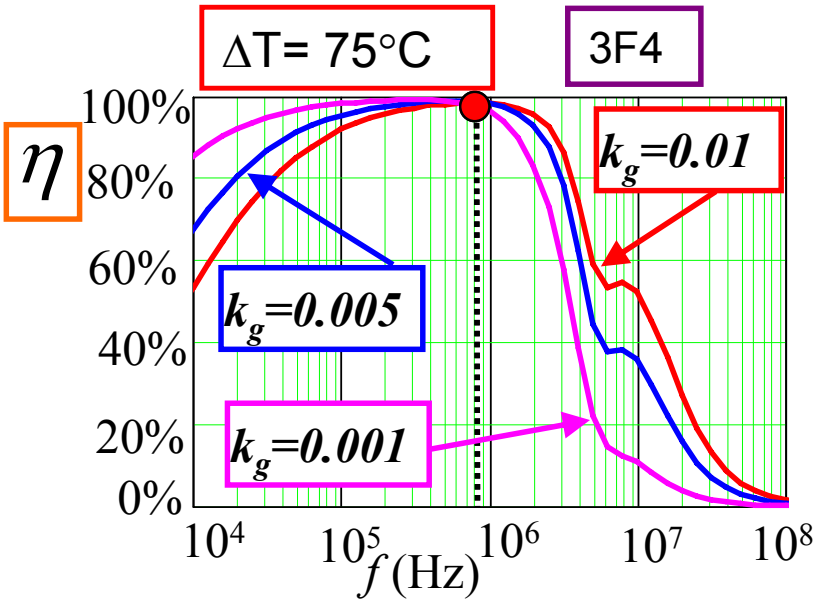


Fig. 4.14 Power conversion efficiency as a function of frequency.

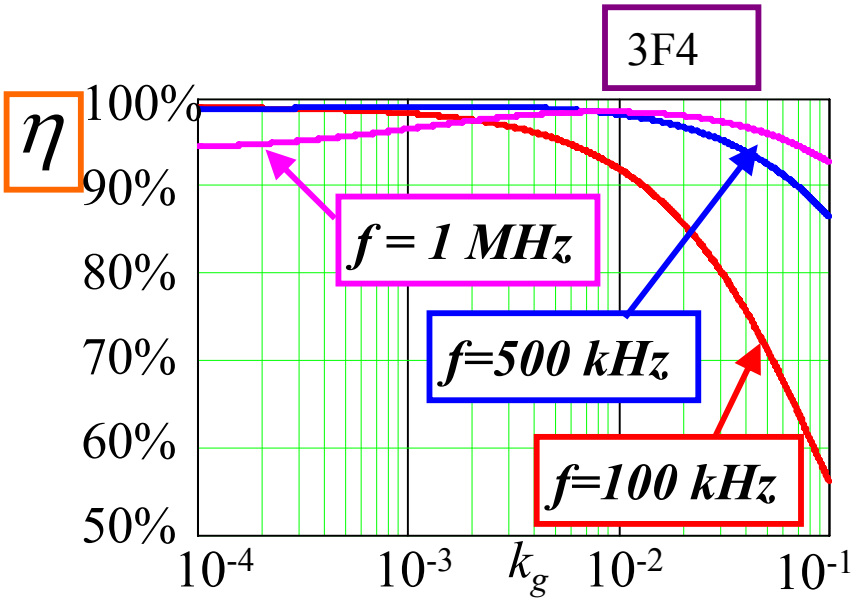


Fig. 4.15 Power conversion efficiency as a function of form factor k_g.

Some important conclusion can be drawn from the analysis above. For constant temperature rise, the power loss density P_{d_V} is kept constant, independent of frequency and form factor k_g (Fig. 4.12). A proper operating frequency point can be selected to achieve the maximum power density for constant k_g (Fig. 4.12), while maximizing the power conversion efficiency (Fig. 4.14). As shown in Fig. 4.12, when $k_g = 0.01$, the

maximum power density is achieved at 820 kHz and the power conversion efficiency reaches a maximum value 98.5%. When the operating frequency is given, the power density and power conversion efficiency can be maximized by selecting proper form factor k_g as shown in Fig. 4.13 and Fig. 4.15.

Form factor k_w doesn't play a role in determining the current density, energy density and power density in the previous analysis. It's mainly determined by the required inductance as (4.24). Assuming the inductance is inversely proportional to the frequency (thus maintaining a constant power throughput) and if the initial inductance at 100 kHz is 100 μH for 10 turns of windings, then the form factor k_w as a function of frequency based on (4.24) is illustrated in Fig. 4.16. The form factor k_w does not always decrease as a function of increasing frequency due to frequency-dependent permeability of the core.

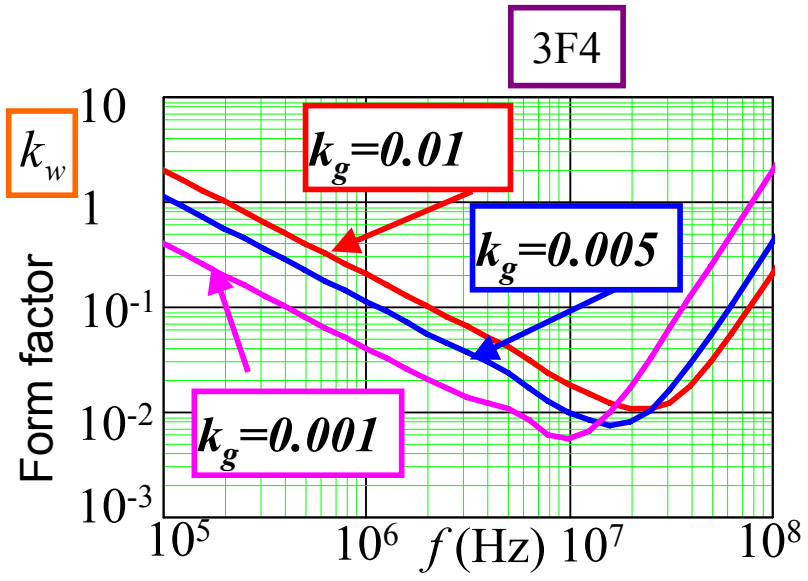


Fig. 4.16 Form factor k_w as a function of frequency.

4.4. Performance of Dielectrics in a Capacitor as a function of frequency

In this section, we consider an illustrative example of an integrated capacitor comprised of a pair of parallel copper plates separated by dielectric material. Again this simple structure was chosen for its simplicity, and because it gives direct insight into the effects of frequency scaling. More complicated, volume-efficient multi-layer capacitors can also be analyzed using the same technology.

The relative permittivity of dielectric material in the capacitor is a frequency-dependent complex quantity. The static dielectric constant is an effect of polarization under DC conditions. When the applied field, or the voltage across the parallel plate capacitor, is a sinusoidal signal, then the polarization of the medium under these AC conditions leads to an AC dielectric constant that is generally different from the static case. To understand and model the dynamic response of dipolar polarization is quite a complicated affair. Debye, however, rendered the problem tractable by what's known today as the so-called Debye equations [121][122][123]. The Debye equations, in (4.35), describe the behavior of the frequency dependence of the complex dielectric constant:

$$\varepsilon_r = \varepsilon_r' - j\varepsilon_r'' = \varepsilon_{r\infty} + \frac{\varepsilon_{rs} - \varepsilon_{r\infty}}{1 + j\omega\tau} \qquad (4.35)$$

where ε_r' is the real part and ε_r'' is the imaginary part, both being frequency dependent. $\varepsilon_{r\infty}$ is infinite relative permittivity as $\omega \to \infty$, typically equal to 1; ε_{rs} is static relative permittivity at DC condition; τ is the relaxation time, depending on the material, but typically for liquid and solid media it is in the gigahertz range.

Consider a capacitor, which has its dielectric medium between a pair of parallel plates (Fig. 4.17).

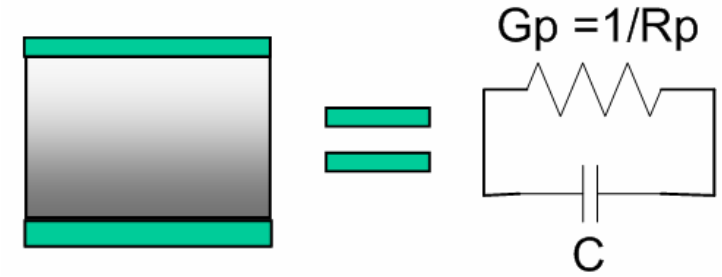


Fig. 4.17 A parallel plate capacitor.

The admittance, Y, i.e., the reciprocal of impedance of this capacitor is

$$Y = \frac{j\omega A\varepsilon_0\varepsilon_r(\omega)}{d} = \frac{j\omega A\varepsilon_0\varepsilon_r'(\omega)}{d} + \frac{\omega A\varepsilon_0\varepsilon_r''(\omega)}{d}$$

which can be written as

$$Y = j\omega C + G_p$$

where

$$C = \frac{A\varepsilon_0\varepsilon_r'}{d},\ G_p = \frac{\omega A\varepsilon_0\varepsilon_r''}{d}$$

The admittance of the dielectric medium is a parallel combination of an ideal, or lossless, capacitor, with a relative permittivity ε_r', and a resistance of $R_p = 1/G_p$. There is no real electric power dissipated in C, but there is indeed real power dissipated in R_p because

$$\text{Input power} = IV = YV^2 = j\omega CV^2 + \frac{V^2}{R_p}$$

Thus the real part ε_r' indicates capability of storage of electric field energy for non-magnetic dielectrics and represents the relative permittivity used to calculate the capacitance. The energy loss is determined by ε_r''. The imaginary part ε_r'' is the relative loss factor, known as Loss Factor in the literature. It should not be confused with Dissipation Factor or Loss Tangent $\tan(\delta)$. $\tan(\delta)$ is defined as:

$$\tan(\delta) = \frac{\varepsilon_r''}{\varepsilon_r'} \qquad (4.36)$$

(4.35) can be split for real (ε_r') and imaginary part (ε_r'') of the complex permittivity:

$$\varepsilon_r' = \varepsilon_{r\infty} + \frac{\varepsilon_{rs} - \varepsilon_{r\infty}}{1 + (\omega\tau)^2} \qquad (4.37)$$

$$\varepsilon_r'' = \frac{(\varepsilon_{rs} - \varepsilon_{r\infty})\omega\tau}{1 + (\omega\tau)^2} \qquad (4.38)$$

$$\tan(\delta) = \frac{\varepsilon_r''}{\varepsilon_r'} = \frac{(\varepsilon_{rs} - \varepsilon_{r\infty})\omega\tau}{\varepsilon_{rs} + \varepsilon_{r\infty}\omega^2\tau^2} \qquad (4.39)$$

The real part ε_r' decreases from its maximum value $\varepsilon_r'(0)$ to 1 at high frequencies. The imaginary part ε_r'' is zero at low and high frequencies but peaks when $\omega\tau = 1$ or when $\omega = 1/\tau$ (as shown in Fig. 4.18).

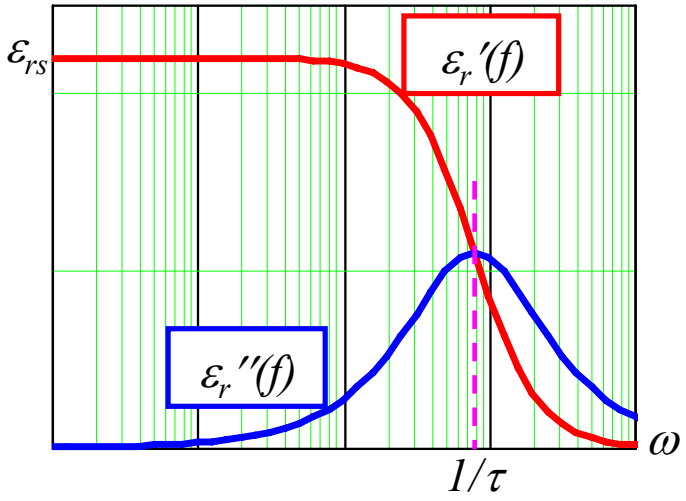


Fig. 4.18 relative permittivity as a function of frequency.

It can be interpreted as follows: At low frequencies the dipole moment of the polar molecules orients in the applied electric field. The real part is approximately constant and equal to ε_{rs}, and the imaginary part ε_r'' is close to zero, which includes the contributions from the dipolar, ionic, and electronic polarization mechanisms. At higher frequencies the dipole can no longer follow the directions of the external applied field. The dipoles are unable to reorientate with that field and the total polarization falls and only the ionic and electronic contributions remain. Thus, ε_r' and ε_r'' assume rather low values. However, at a specific frequency called resonance frequency ω_{res} ($\omega_{res}\tau = 1$), the efficiency of the reorientation process is at maximum, as the rate of change in direction of the applied field matches the relaxation time of dipoles. From the viewpoint of energy, the rate of energy storage by the field is determined by ω whereas the rate of energy transfer to molecular collisions is determined by $1/\tau$. When $\omega = 1/\tau$, the two processes, energy storage by the field and energy transfer to random collisions, are then occurring at

the same rate, and hence energy is being transferred to heat most efficiently. Thus ε_r'' related to the power dissipated in the dielectric medium peaks when $\omega = 1/\tau$ [121][122].

An implicit assumption made during the derivation of the Debye equations is that there is only one relaxation time. While this may be true for some crystalline solids, it is less likely to be so for amorphous solid such as a glass, where the random nature of the structure will likely lead to a distribution of relaxation times. In this case, a distribution of relaxation times is necessary to interpret the experimental data. The empirically-derived Cole-Cole equation is given to take this effect into account as (4.40) [122]-[124].

$$\varepsilon_r = \varepsilon_r' - j\varepsilon_r'' = \varepsilon_{r\infty} + \frac{\varepsilon_{rs} - \varepsilon_{r\infty}}{1 + (j\omega\tau)^{1-\alpha}} \qquad (4.40)$$

where α is a constant that has a value in the range $0 \le \alpha \le 1$. This fractional power law frequency-domain behavior is a striking characteristic. Nevertheless, the model correlates well with measured permittivities data for many materials.

The temperature-dependent characteristics of complex permittivity is mainly expressed through a temperature-dependent relaxation time $\tau = \tau_h \exp(H/kT)$. If the DC conductivity σ of the dielectric material is not negligibly small, then the conductivity σ will contribute to the imaginary part the complex permittivity [123].

$$\varepsilon_r = \varepsilon_r' - j(\varepsilon_r'' + \frac{\sigma}{\omega\varepsilon_0})$$

$$\varepsilon_r = \varepsilon_r' - j\varepsilon_r'' - j\frac{\sigma}{\omega\varepsilon_0} = \varepsilon_{r\infty} + \frac{\varepsilon_{rs} - \varepsilon_{r\infty}}{1 + j\omega\tau} - - j\frac{\sigma}{\omega\varepsilon_0}$$

In general dielectrics are grouped into three classes [125]: Class I dielectrics include ceramics with relatively low (ε_r'<15) and medium (ε_r':15~500) permittivity and dissipation factors of less than 0.003. Class II dielectrics are high-permittivity ceramics having values of ε_r' between 2000 and 20000 with $\tan\delta$ below 0.03. Class III dielectrics

contain a conductive phase that effectively reduces the thickness of the dielectric and results in very high capacitance. Their breakdown voltages are quite low, however.

The power losses in capacitors are attributable mainly to Ohmic losses in the plates, terminals and leads, and the dielectric losses. The dissipated power is distributed among the conducting elements and the dielectric, and the extent to which each contributes is also a function of frequency [126]. The dielectric loss is determined by the specific properties of the dielectric material. Each dielectric material has an associated loss factor or loss tangent, which is a common representation of the dielectric loss. This can be represented by a resistance R_{sd} which is in series with the capacitor, and expressed as

$$R_{sd} = \tan\delta \frac{1}{\omega C} = \tan\delta \frac{1}{2\pi f C} \qquad (4.41)$$

For the integrated planar capacitor with dielectric layer sandwiched between two copper plates as shown in Fig. 4.19, the current distribution is illustrated in Fig. 4.20.

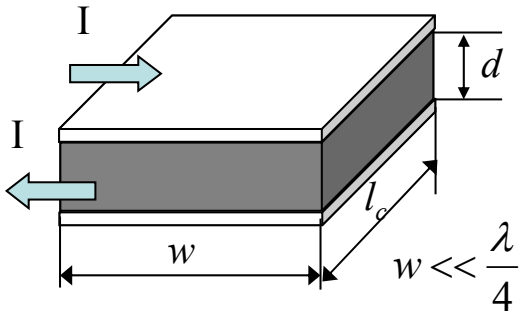


Fig. 4.19 Integrated planar capacitor with a pair of parallel plates.

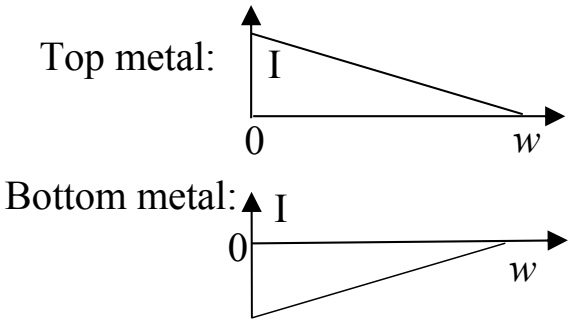


Fig. 4.20 Current distribution along the plates.

Assuming a sinusoidal current source with amplitude I, the current and current density are related by equation below:

$$I = J_{\max} l_c \delta_{skin}(f) \tag{4.42}$$

where $\delta_{skin}(f)$ is skin depth:

$$\delta_{skin}(f) = \sqrt{\frac{1}{\pi f \mu_{cu} \sigma_{cu}}} \tag{4.43}$$

and σ_{cu} is conductivity of copper. Corresponding to the current distribution shown in Fig. 4.20, the copper loss per unit area of the top or bottom copper plate is:

$$p_{cu} = \frac{1}{2 l_c w} \int_0^w (J_{\max} \frac{x}{w} l_c \delta_{skin})^2 \frac{dx}{\sigma_{cu} l_c \delta_{skin}} \Rightarrow$$

$$p_{cu} = \frac{{J_{\max}}^2 \delta_{skin}}{6 \sigma_{cu}} \tag{4.44}$$

The maximum temperature of the integrated capacitor (Fig. 4.19) due to the power losses in dielectric and copper plates is still presented by (4.5) based on the thermal model shown in Fig. 4.3. This equation is repeated below for this case:

$$T_{\max} = \frac{p_{diele}}{2k_c} d^2 + \frac{p_{cu}}{k_c} d + \frac{2p_{cu} + p_{diele} d}{h} + T_{amb} \tag{4.45}$$

where p_{diele} is the volumetric dielectric loss density, k_c is the thermal conductivity of the dielectric material, d is the thickness of dielectric layer.

The resistance R_{sd} in (4.41) represents the dielectric loss, so for a sinusoidal current excitation source with the amplitude I, the dielectric loss per unit volume is:

$$p_{diele} = \frac{\frac{1}{2} I^2 R_{sd}}{vol} = \frac{1}{2} \frac{{J_{\max}}^2 {\delta_{skin}}^2 {l_c}^2}{w \cdot l_c \cdot d} \tan\delta \cdot \frac{1}{\omega C} \Rightarrow$$

$$p_{diele} = \frac{1}{2} \frac{{J_{\max}}^2 {\delta_{skin}}^2 \cdot \tan\delta}{\omega C \cdot d} \cdot \frac{1}{k_w} \tag{4.46}$$

The energy stored in the capacitor is given by

$$E = \frac{1}{2}CV^2 = \frac{1}{2}CI^2\frac{1}{(\omega C)^2} = \frac{J_{\max}{}^2\delta_{skin}{}^2 l_c{}^2}{2\omega^2 C} \quad (4.47)$$

The energy per unit area is then

$$E_s = \frac{E}{w \cdot l_c} = \frac{J_{\max}{}^2\delta_{skin}{}^2}{2\omega^2 C \cdot k_w} \quad (4.48)$$

The volumetric power density is given by

$$P_V = \frac{E_s f}{d} \quad (4.49)$$

As we did before, let's assume that the capacitance is inversely proportional to the operating frequency, i.e., $C \cdot f = \text{constant}$, which means that the rate at which energy is transferred is constant. The inflexible constraints imposed on the following analysis include maximum temperature $T_{\max}$ at 85°C, and ambient temperature $T_{amb} = 25°C$; Those parameters that can be discretized include thickness of the dielectric layer, dielectric material properties, and the cooling coefficient $h = 10$ W/m^2-°C. Operating frequency f and form factor $k_w = w/l_c$ are variables that can be varied to analyze the performances of the integrated capacitor shown in Fig. 4.19.

For this example we selected a high-permittivity dielectric X5U with $\varepsilon_{rs} = 4400$, relaxation time $\tau = 0.2 \times 10^{-9}$ S, and the thermal conductivity $k_c = 1.5$ W/m-°C. The frequency-dependent complex permittivity is shown in Fig. 4.21. Assuming a specific capacitance value of 100 nF at 1 MHz, so $C \cdot f = 0.1$ (F·Hz). The surface area of the integrated capacitor is then given by (4.50). Fig. 4.22 shows the surface area as a function of frequency for two dielectric layer thickness values. It is clear that at first the surface area will become smaller with increasing frequency, but it will again become larger beyond some frequency because it then becomes necessary to derate the frequency-dependent real part of the permittivity.

$$A = \frac{C \cdot d}{\varepsilon_0 \varepsilon_r'} \quad (4.50)$$

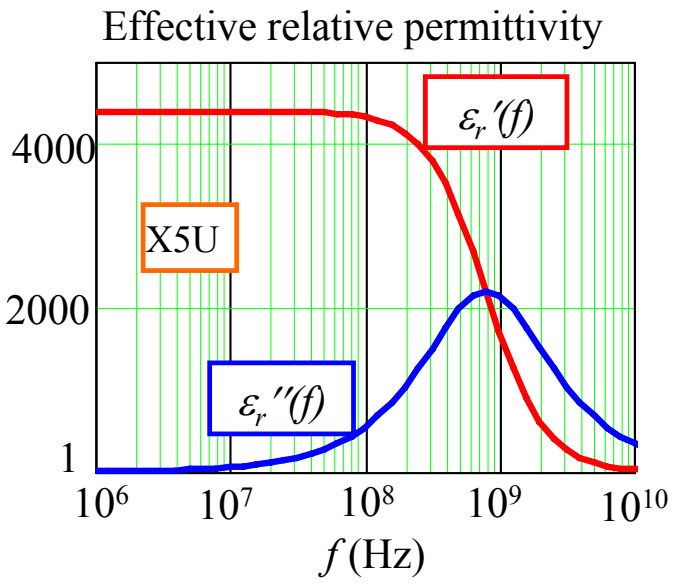


Fig. 4.21 frequency-dependent relative permittivity of X5U.

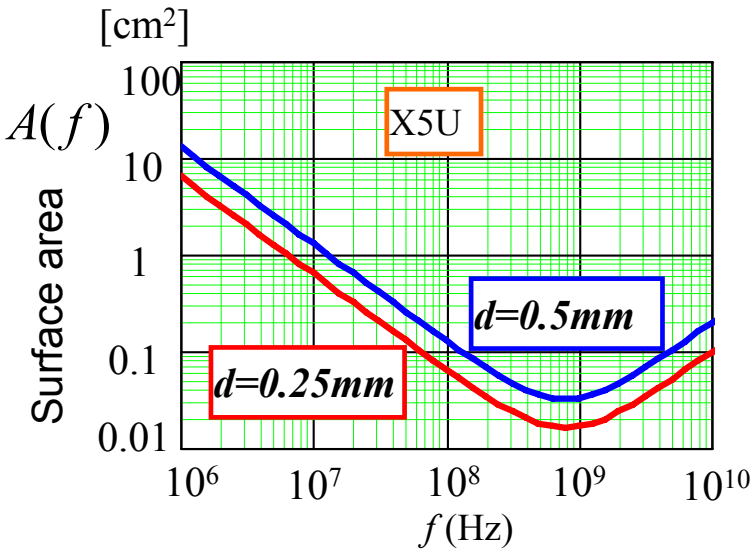


Fig. 4.22 Surface area changes with frequency.

From (4.44), (4.45) and (4.46), the maximum current density is derived as (4.51) and is plotted in Fig. 4.23 as a function of frequency.

$$J_{\max}{}^2(f,k_w)=\frac{T_{\max}-T_{amb}}{(\frac{d}{k_c}+\frac{2}{h})(\frac{\tan\delta\cdot\delta^2}{4\omega\cdot C}\frac{1}{k_w}+\frac{\delta}{6\sigma_{cu}})} \qquad (4.51)$$

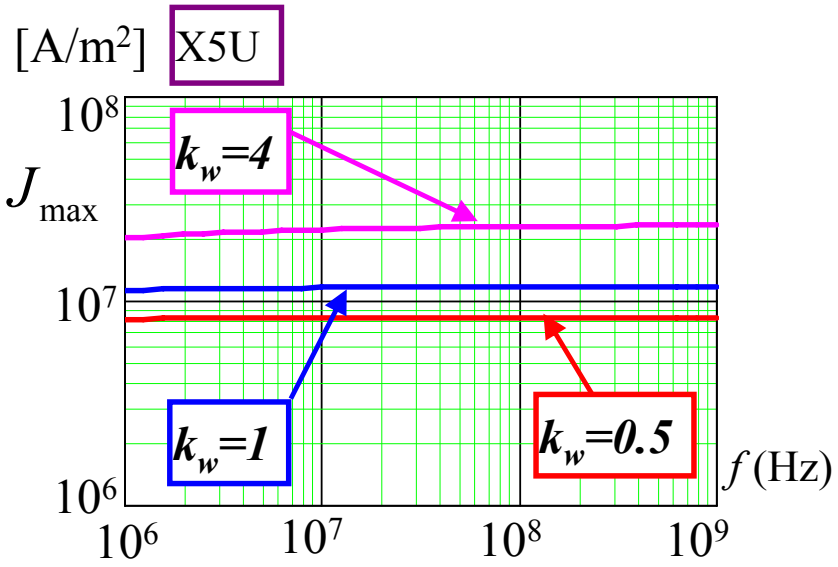


Fig. 4.23 Maximum current density through the cap as a function of frequency.

Then from (4.48) the energy density as a function of frequency is plotted in Fig. 4.24 for several form factors $k_w = \frac{w}{l_c}$. And the energy density versus the form factor $k_w = \frac{w}{l_c}$ is illustrated in Fig. 4.25. When the frequency increases, the stored energy density decreases. The energy density doesn't strongly depend on the form factor k_w.

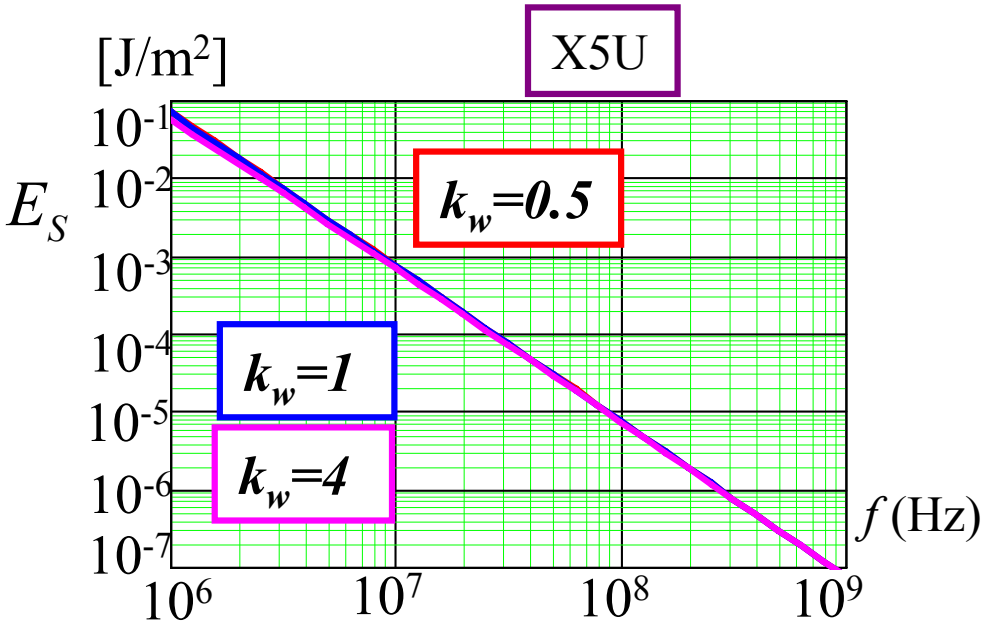


Fig. 4.24 Energy density vs. frequency.

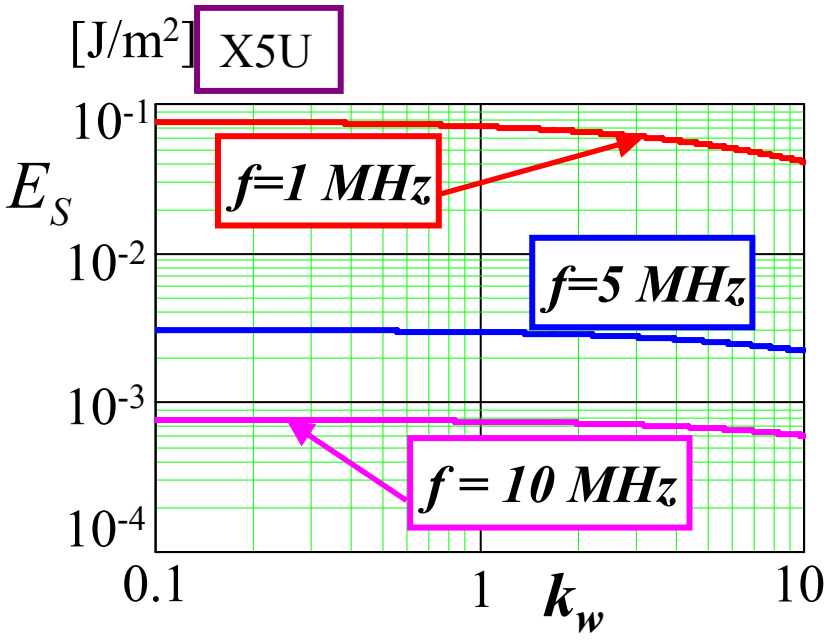


Fig. 4.25 Energy density vs. form factor k_w under different frequencies.

The total volumetric power loss density P_{d_V} can be derived from both the volumetric dielectric loss density (4.46) and the copper losses per unit area (4.44), given by

$$P_{d\_V} = p_{diele} + \frac{p_{cu}}{d} \qquad (4.52)$$

The power density P_V (4.49) of the integrated capacitor is illustrated in Fig. 4.26 as a function of frequency along with its power loss density P_{d_V}. Fig. 4.27 plots the power density as a function of form factor k_w. When the frequency increases, the power density decreases with a slope nearly -20 dB/dec. Under these conditions, the form factor k_w doesn't seem to play much role in this process. Power loss density is also kept constant for constant temperature rise, independent of frequency and form factor k_w.

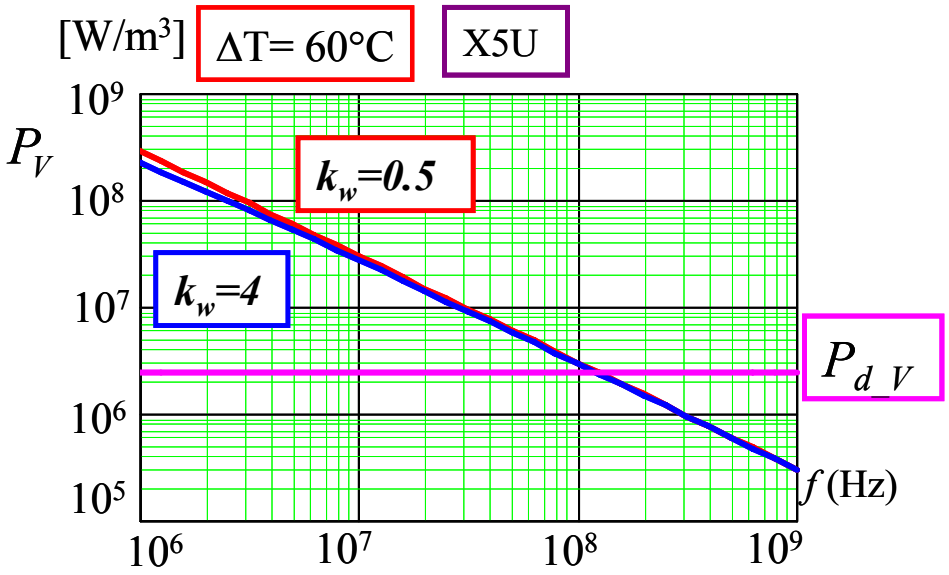


Fig. 4.26 power density as a function of frequency along with the power loss density.

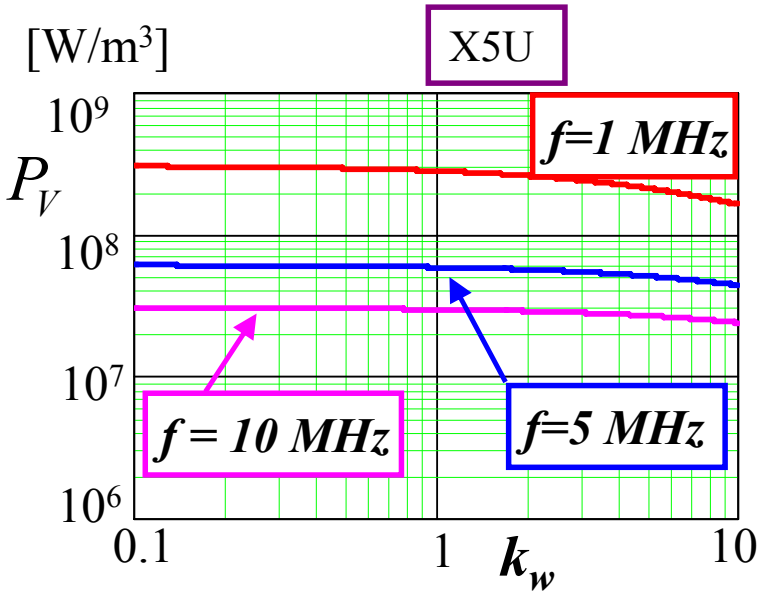


Fig. 4.27 power density as a function of form factor k_w.

The power conversion efficiency as a function of frequency, according to (4.34), is illustrated in Fig. 4.28. Fig. 4.29 plots the power conversion efficiency as a function of form factor k_w.

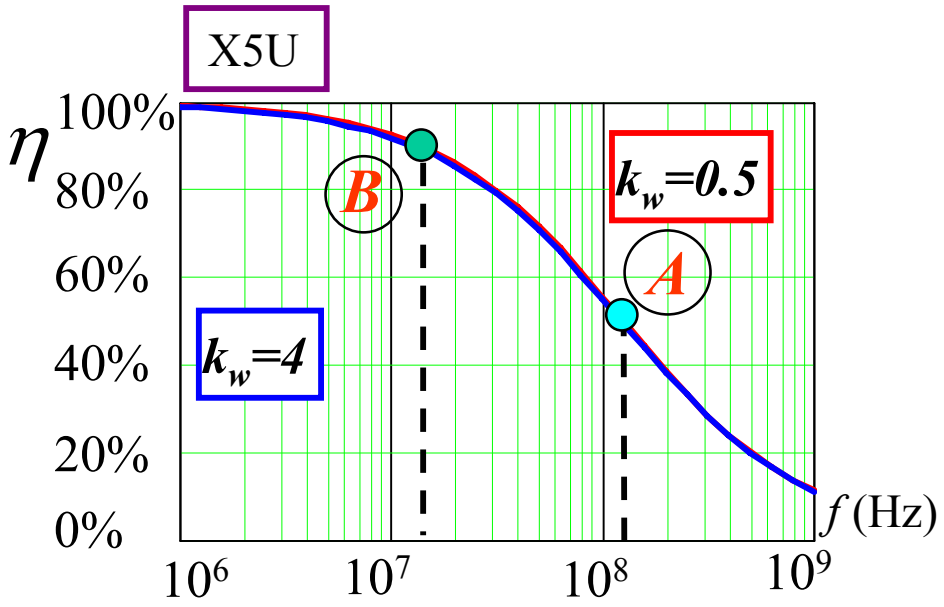


Fig. 4.28 power conversion efficiency vs frequency.

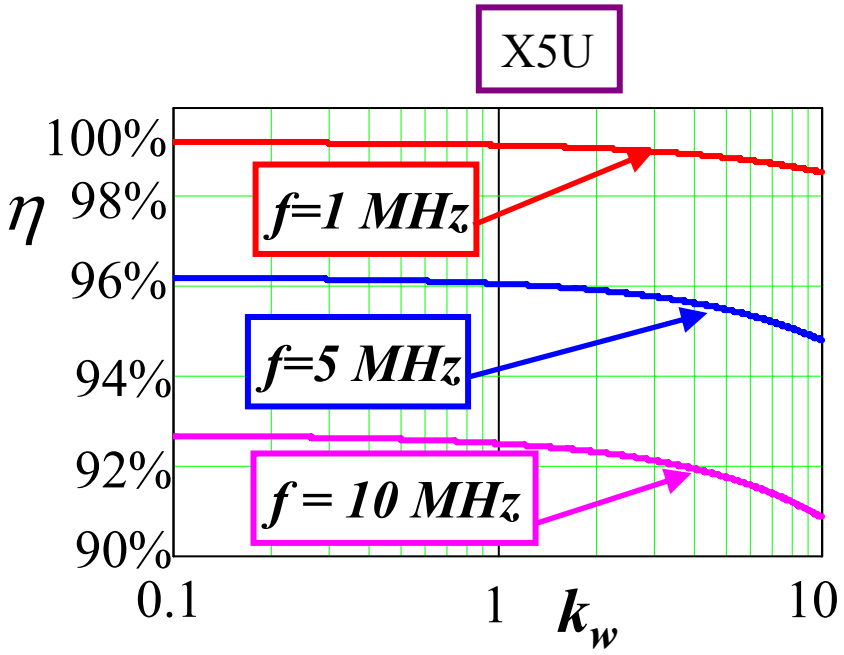


Fig. 4.29 power conversion efficiency as a function of form factor k_w.

As shown in Fig. 4.28 when the maximum temperature is fixed at 85°C, at point A when $k_w = 0.5$, energy lost per cycle exceeds the amount of energy stored per cycle at $f = 125$ MHz, i.e. that power conversion efficiency is below 50%. In order to ensure the

power conversion efficiency larger than 90% when $k_w = 0.5$, we learn here that the operating frequency should not exceed 13.6 MHz (at point B).

In our next analysis we have selected the low-permittivity dielectric Silicon Nitride (SiN). It has a static relative permittivity ε_{rs} of 7.8, relaxation time $\tau = 0.1\times10^{-11}$ S, and its thermal conductivity $k_c = 25$ W/m-°C. The frequency-dependent relative permittivity is shown in Fig. 4.30. The capacitance is again assumed to be inversely proportional to the frequency and the initial capacitance is set to a value of 1 nF at 100 MHz. The thickness of the dielectric layer $d = 100$ μm. The maximum temperature $T_{\max}$ is still 85°C for 25°C ambient temperature. The surface area as a function of frequency is plotted in Fig. 4.31. As before, the relationship between the power conversion efficiency and frequency or form factor k_w is derived, and shown in Fig. 4.32 and Fig. 4.33 respectively. For k_w=0.5, the power conversion efficiency is 50% at 24 GHz (point A in Fig. 4.32); the power conversion efficiency reaches 90% when the operating frequency is 1.9 GHz at point B in Fig. 4.32. It is clear that low permittivity dielectrics are more suitable for very high frequency operation due to its lower tangent loss, but at the expense of larger volume.

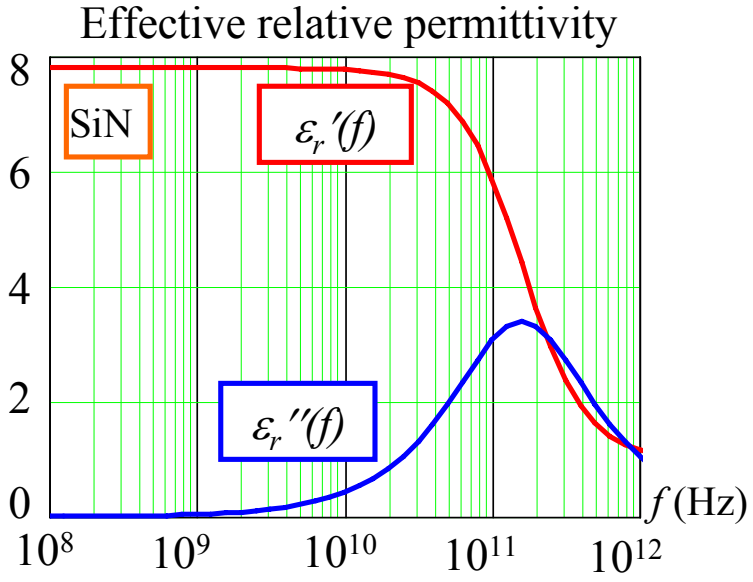


Fig. 4.30 relative permittivity as a function of frequency.

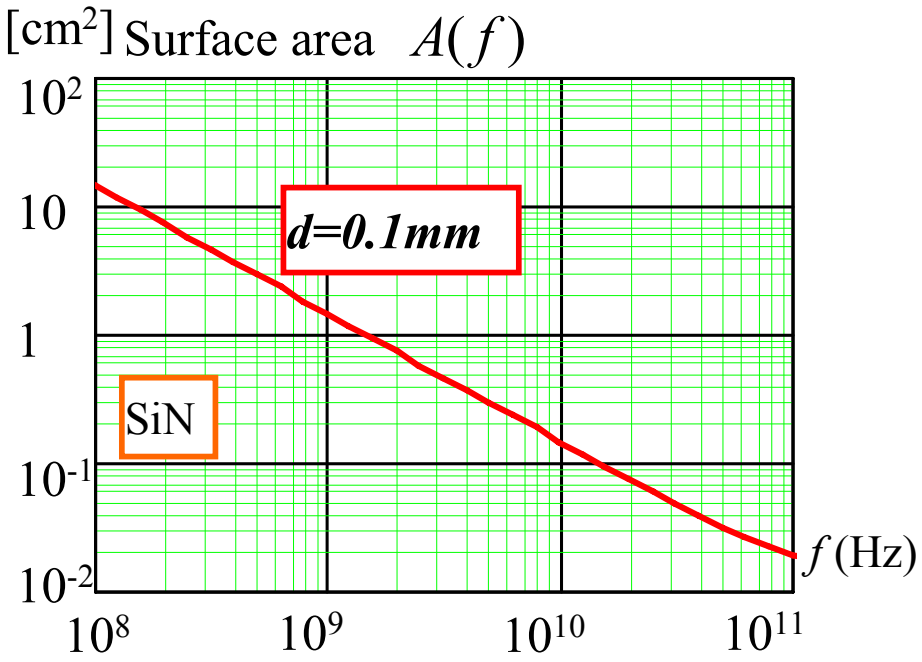


Fig. 4.31 surface area of capacitor as a function of frequency.

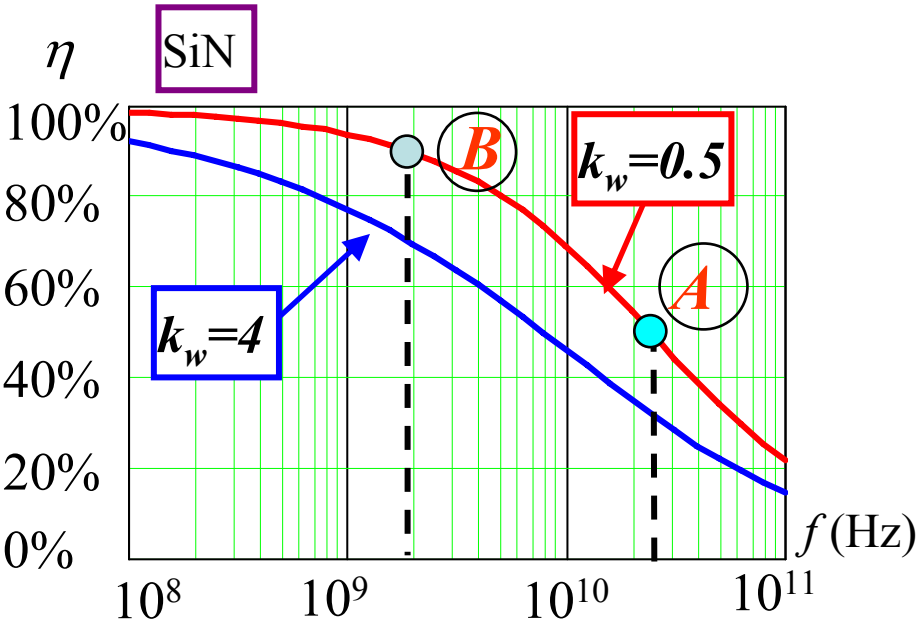


Fig. 4.32 power conversion efficiency vs frequency.

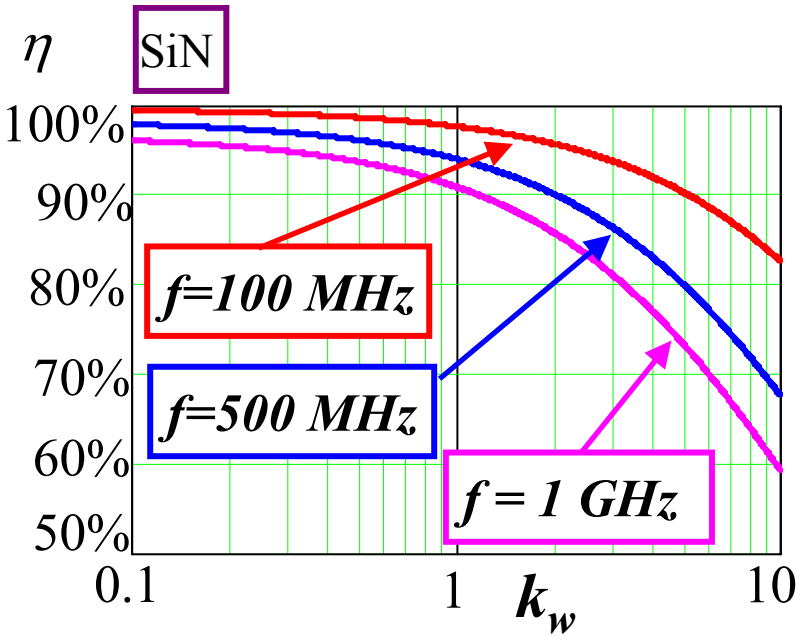
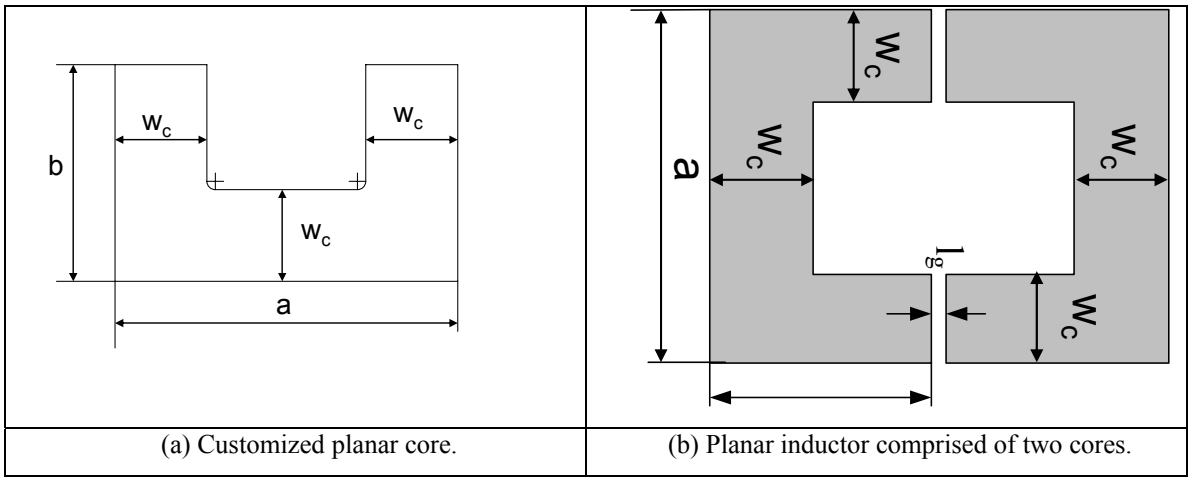


Fig. 4.33 power conversion efficiency as a function of form factor k_w.

4.5. Experimental Verification on Frequency Scaling Effects of Integrated Inductor

The purpose of this chapter is to verify the frequency scaling effects of the integrated magnetic components based on the model setup previously through the experiments. An integrated planar inductor will be made as the sample for the experiments. 3F3 is chosen as the magnetic material. The customized ferrite cores from Elna Magnetics Co. are chosen as the parts to make a planar integrated inductor. The shape of the customized planar ferrite cores PLT64/50/5 is shown in Fig. 4.34(a). The planar inductor is comprised of two ferrite cores, shown in Fig. 4.34(b).



(a) Customized planar core. (b) Planar inductor comprised of two cores.

Fig. 4.34 Customized planar core and the inductor under study.

The practical dimensions of the ferrite core in Fig. 4.34 are listed in Table 4.2. The width w_{cu} of the copper windings wrapped around the ferrite core is 6.5 mm. The number of the copper winding turns N is 20. The average magnetic path length is l_c = 256 mm.

Table 4.2 Dimensions of customized ferrite core

a	b	w_c	t (core thickness)	t_{cu}	w_{cu}
62 mm	48 mm	15 mm	5 mm	50 μm	6.5mm

The fabrication process of the sample is described in Appendix IV. After the processes as described in Appendix IV, the final inductor is shown Fig. 4.35, consisting of two ferrite cores.

Fig. 4.35 Inductor sample for experiment.

The impedance of the inductor is measured by impedance analyzer 4294A and shown in Fig. 4.36. The frequency-dependent permeability of 3F3 can be modified to match the measured impedance. The k_g can be obtained from (4.24), k_g = 0.0013. The fringing factor is chosen as k_f = 0.7. The winding factor k_{cu} = 0.47.

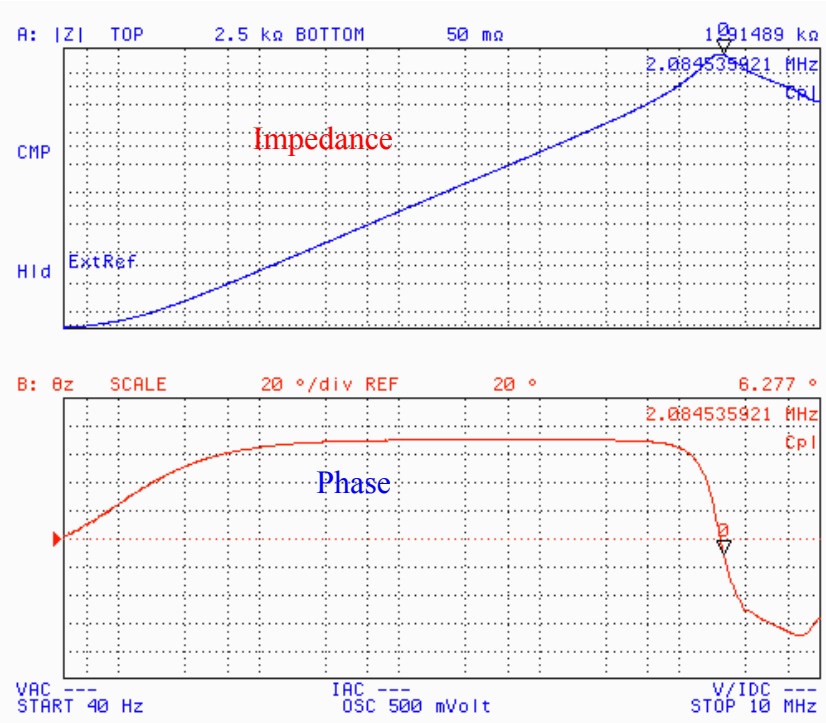
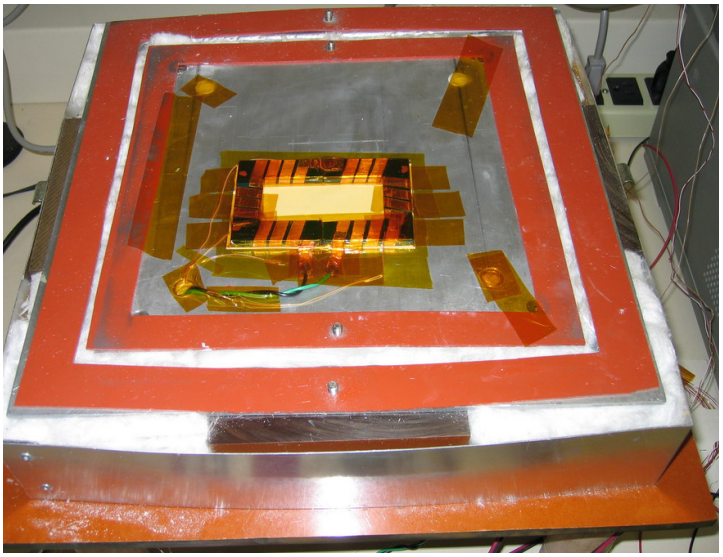
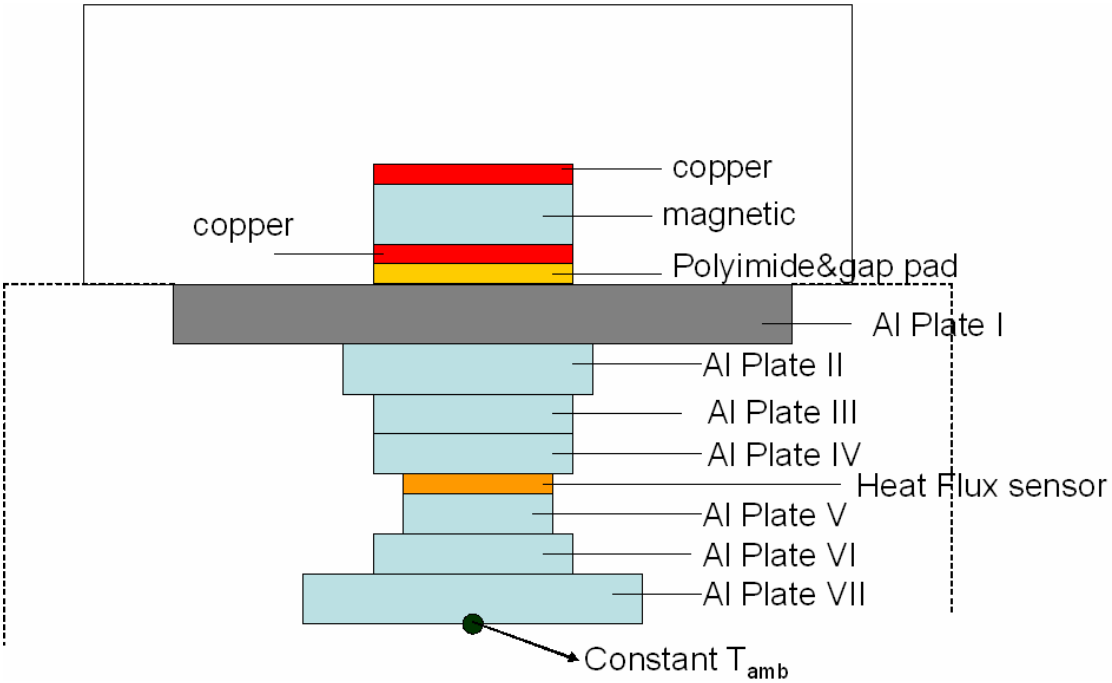


Fig. 4.36 Impedance characteristics of the inductor.

The planar inductor is put inside of the calorimeter chamber built in Chapter 5, as shown in Fig. 4.37. In order to prevent heat escaping from the top of the inductor, the top of the inductor is covered with thermal insulation material - fiber glass. The dimensions and thermal properties of all the parts in the Fig. 4.37 are shown in Table 4.3. The thermal contact resistances exist between surfaces. We cannot ignore thermal contact resistances, but they are very difficult to quantify. In the design process a 1 K-cm^2/W contact thermal resistance coefficient is assumed [127].



(a)



(b)

Fig. 4.37 Diagram of the planar inductor and the chamber.

Table 4.3 Dimension and properties of the parts in Fig. 4.37.

	Dimension (L×W×t) (mm)	Thermal Conductivity W/m-K
Plate VII	140×160×10	167
Plate VI	50×50×10	167
Plate V	26×30×10	167
HFS-4	26×30 ×0.23	3.5 (K/W)
Plate IV	50×50×10	167
Plate III	50×50×10	167
Plate II	80×80×10	167
Plate I	240×240×10	167
Gap Pad	96×62×0.25	3
Polyimide	Thickness:0.064 × 3	0.12
Magnetic layer	Thickness: 5	3
Copper layer	Thickness:50 μm	385

In the experiment, a sinusoidal waveform generated by Agilent 33120A waveform generator is amplified by power amplifier (AR amplifier Model 1000L) to the inductor inside the chamber. Differential probe P5205 measures the voltage across the input terminals of the inductor, TCP202 current probe records the current flowing into the inductor. And Data Acquisition Unit 34970A is used to record the measured temperatures and the output of the heat flux sensor HFS-4 inside the calorimeter (refer to Chapter 5). The experiment setup is shown in Fig. 4.38.

In order to verify the performances of the inductor as a function of frequency, experiments at several frequency points are carried out. In these experiments, the input power ($V_{max} \cdot I_{max}$) into the inductor is kept constant, with regard to the difficulty of controlling the power losses generated in the inductor to keep constant temperature rise. The power loss densities and efficiencies at several operating frequencies are identified. The Table 4.4 shows the measurement results. The measured data points are marked in Fig. 4.39, Fig. 4.40, Fig. 4.41 along with the theoretic curve predicted from the model. It

is clear that the measured results match the expected curve very well.

Table 4.4 Measurement results.

	f	P_V (W/m^3)	I_{max} (A)	V_{max} (V)	T_{max} (°C)	P_d (W)
Theory	1 MHz	3.5×10^5	0.35	244	72	9.9
Measured			0.35±3%	236±3%	75.6 ±2	10 ±5%
Theory	800 kHz	3.5×10^5	0.29	145	55	6.1
Measured			0.31±3%	136±3%	54.3 ±2	6.2 ±5%
Theory	700 kHz	3.5×10^5	0.44	190	45	3.8
Measured			0.43±3%	192±3%	44.5 ±2	3.6 ±5%
Theory	500 kHz	3.5×10^5	0.53	159	35	1.85
Measured			0.58±3%	146±3%	34.2 ±2	1.86 ±5%
Theory	400 kHz	3.5×10^5	0.6	142	31.1	1.1
Measured			0.67±3%	126±3%	31.9 ±2	0.94 ±10%
Theory	200 kHz	3.5×10^5	0.84	100	26.4	0.25
Measured			0.95±3%	88±3%	27 ±2	0.23 ±10%

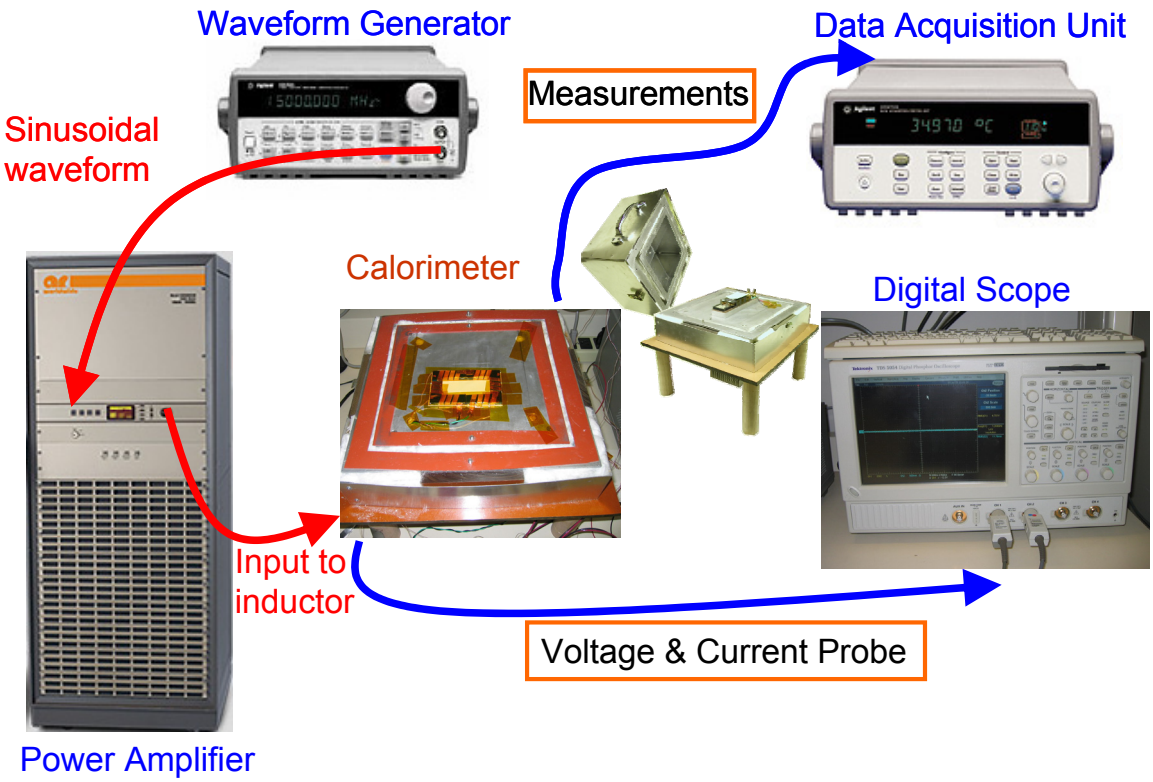


Fig. 4.38 Experiment setup.

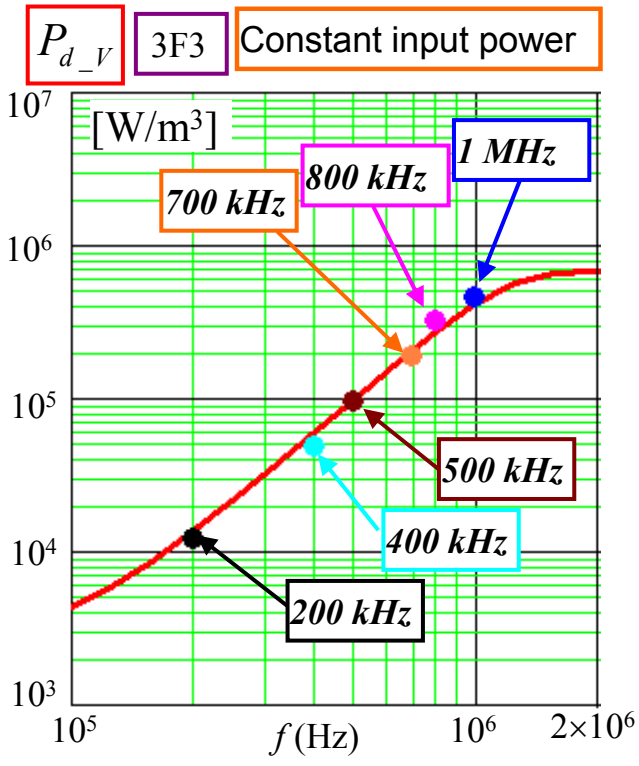


Fig. 4.39 Measured power loss density as a function of frequency.

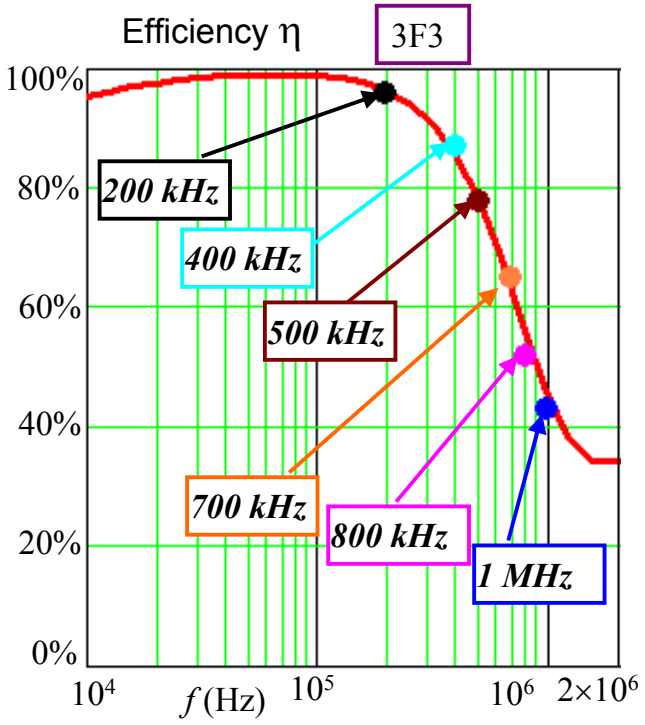


Fig. 4.40 Measured efficiency as a function of frequency.

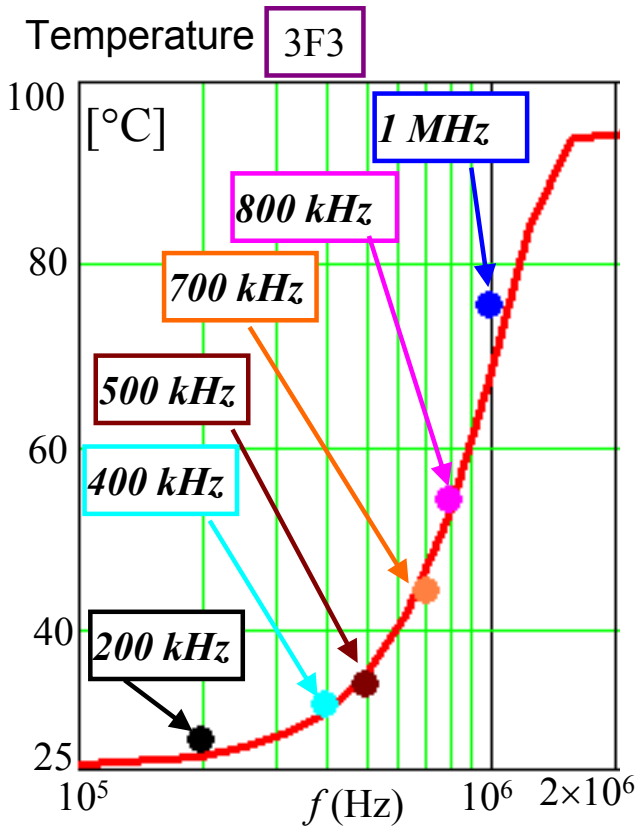


Fig. 4.41 Measured temperature vs frequency.

4.6. Summary

A generic multi-disciplinary model was developed in this chapter to analyze the performance of passive components in terms of power density and power conversion efficiency as a function of frequency scaling. The material characteristics, thermal management and temperature constraints, circuit specifications and packaging techniques are all incorporated into this model.

For magnetic components (single layer planar inductor in the examples), power density and power conversion efficiency can be optimized by selecting proper operation frequency or form factor during the design procedure. It was demonstrated how the optimum frequency can be identified, and how power conversion efficiency deteriorates beyond the optimum under a fixed maximum temperature. The analysis also shows how frequency dependencies of material properties are responsible for today's capacitor technologies being more suitable for high frequency operation than magnetic components.

Therefore for very high frequency operation, even at hundreds of megahertz, air-core magnetic components are necessary. But the price paid to it is the substantially raised volumes, defeating our original objective for reduced volume and increased power density.

It should be noted here that the self-resonant frequency of the passive components due to parasitic is not considered in the analysis. In practice, self-resonant frequency, depending on the structure and manufacturing technology, also plays a role in limiting the highest operation frequency.

Lastly, the examples demonstrate how the methodology can be used to identify the most optimum power conversion frequency for a given set of specifications, circuit function, selection of materials and packaging technology and limitations, and thermal conditions.

Chapter 5 Power Loss Measurement Techniques for HF/VHF power conversion Applications

5.1. Introduction

It is important to measure the high frequency signals accurately for the purpose of verifying design, characterizing and debugging the design if problems are found.

In previous chapter, a VHF DC-DC power converter was designed and it became necessary to visualize the converter to ensure its proper operation through the measurements. However the task of measuring at such high frequencies is really a big challenge for engineers. Accurate measurement of such high frequency signals requires very sophisticated instrumentation to acquire useful information about its operation. The instrument should have a bandwidth sufficiently beyond the highest frequency contained in signals being measured. This very sophisticated instrument must also be able to measure signals without interfering with the operation of the circuits and systems. Therefore it is necessary to use high performance current or voltage acquisition systems to obtain the current or voltage waveforms. Limited by bandwidth, interference or sensitivity, no suitable current sensing techniques [128] are available for this 250 MHz power converter at present. So only the voltage measurement is possible and a voltage probe is discussed and in Appendix II.

A model was established in Chapter 4 to investigate the performances of integrated passive components in terms of power density and efficiency by varying frequency or dimensions. It is clear that accurate determination of losses is required to validate the design and verify the model. Also accurate estimates of these losses in these integrated passive components are important to characterize their thermal behavior, which is driven by the demand for reducing volume, pushing frequency higher and

improving efficiency. The accurate measurement of losses, presenting many difficulties, can be approached by electrical measurement and calorimetric measurement.

It is realized that the losses measurement by electrical method could yield errors of 100% and more. It is well known that the measurement of high efficiency systems is difficult, and the difficulty increases as the efficiency increases. The effects of switching transients, non-linearity of components, high frequencies and so on make the accurate measurement of losses more difficult. Errors larger than 100% are not uncommon, even using very sophisticated digital instruments. Digital instruments are notoriously susceptible to EMI/RFI and the main sources of error include: sampling errors and phase shifts between channels; delays, parasitic effect introduced by probes; mismatched bandwidth; errors introduced by AD conversion. Therefore losses measurement by the electrical instruments is most suitable for pure DC and low frequency systems.

To overcome the limits of electrical measurement, the calorimetric method is an alternative for loss measurement since it is based on the heat effect caused by the power dissipation and independent of the electrical quantities in the systems. It is suitable for measurement under high frequency and non-sinusoidal conditions. Calorimetric method is the most popular and the most promising method to accurately measure losses in magnetic losses or dielectric losses. It can achieve high accuracy but be limited to steady state and be time-consuming.

5.2. Limitations of electrical measurements for power loss measurement

5.2.1. Background

The need of a quantitative knowledge of power loss in any power electronics system is self-evident. Driven by recent advances toward integration, higher operating

frequencies and improved efficiency in power electronics systems, accurate estimates of power losses is becoming more challenging and important to ensure proper thermal management and reliable operation. Although sophisticated numerical modeling methods are often available to predict power losses, validity of the models need to be verified experimentally, especially where complex loss mechanisms exist in some parts, for instance magnetic materials for power conversion.

Typically there are two kinds of techniques to measure the power losses:

- electrical methods;
- calorimetric methods.

The electrical measurement [131][132][133][134][135][136] uses the product of voltage and current, which gives an electrical quantity equivalent to power. Power measurement can be performed by measuring the voltage drop across the device and the current flowing through it using electrical instruments. In DC and low frequency AC circuits it is common to measure power directly by using analog electronic equipments: voltmeters for voltage measurements and ammeters for current measurements, or a combined measurement using a wattmeter. However for high frequency signal and highly distorted signals, such as pulse width modulation, conventional meters are no longer suitable because of their limited bandwidth and dynamic frequency response. Digital instruments have gained popularity for obtaining the required resolution. This kind of digital meter takes simultaneous samplings of voltage and current waveforms, digitizes these values, and provides arithmetic multiplication and averaging using digital techniques to obtain a power measurement. An appealing advantage of the electrical methods is that they are easy to perform and to reproduce a measurement. It is suitable for steady state as well as transient measurements. However, high di/dt and dv/dt's introduce serious RFI/EMI problems, since digital instruments are very sensitive to noise. The accuracy of digital measurement is also affected by the delays introduced between probes, phase shifts between sampling channels of digitizer, sampling errors and non-linearities of A/D converters. No instrument known to man can accurately record the

hard-switched output voltage waveforms when dv/dt is very high [137]. Therefore the electrical measurement methods are most suitable for pure DC or low frequency systems.

Loss measurements in power electronics systems become especially difficult for components or systems having high power conversion efficiencies. The conventional output-input electrical method can produce very large errors, regardless of the technique used for measuring input and output power, because a considerable error always exists when two nearly equal numbers are measured and subtracted in such a high efficiency system.

For example, 1 kW converter with an efficiency η=93%, input power P_{in}=1000 W, output power P_{out}=930 W, $P_{loss} = P_{in} - P_{out}$=70 W, and assuming $P \propto V \cdot I$, and a ±1.5% error distribution in voltage and current measurement for the input and output power, then the maximum error of loss measurement can be ±57.9 W with respect to nominal 70 W. In other words under these idealistic conditions the absolute percentage error of loss is 83%. If the efficiency increases to 95%, the maximum error percentage can be 117% (Fig. 5.1)! Clearly, there is a high degree of inaccuracy, which makes the loss figure totally unacceptable. In order to achieve a maximum absolute error of 5% in the total loss measurement using this method, an error as small as 0.09% in each of the voltage and current measurements is required. Such a small error is difficult to achieve, even employing the most sophisticated metering instruments.

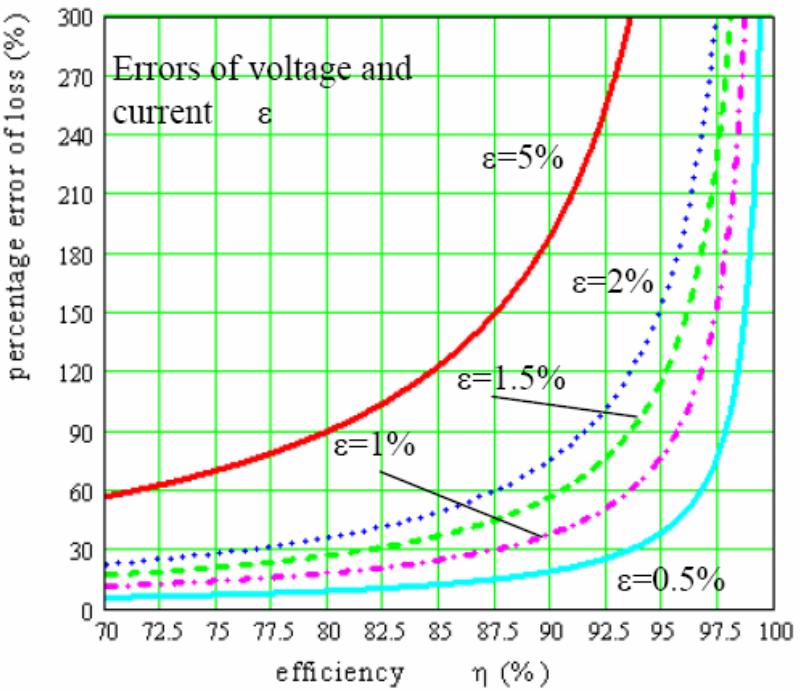


Fig. 5.1 Percentage error of loss measurement vs efficiency for given error of voltage and current.

Note that measurement uncertainties are usually expressed in terms of a standard uncertainty, which is evaluated by either statistical methods or an assumed probability distribution. Since definitions of measurement uncertainty are often subjective and even unique among different standards, the discussion herein will focus more on the independent sources of error than their interpretations and distributions.

5.2.2. Direct Wattmeter Measurement [139]

In this method the traditional electromechanical wattmeter has been used to directly make measurements of the electrical power of device under test. At higher frequencies the wattmeter accuracy becomes quickly deteriorated, especially when voltage and current waveforms are non-sinusoidal and contain high frequency harmonics. Usually this kind of wattmeter has low bandwidth and poor frequency response, therefore it is only applicable to DC and low frequency sinusoidal measurement, and unsuitable for high frequency and non-sinusoidal conditions.

5.2.3. Digital Measurement Techniques

Today digital instruments, especially digital oscilloscopes, are some of the most widely used measuring tools in power electronics systems. Estimating losses digitally is based on the high frequency sampling of voltage and current waveforms. For periodical power signals with voltage $v(t)$ and current $i(t)$, having a period of T, determine the average power P_0 of

$$P_0 = \frac{1}{T}\int_0^T v(t)\cdot i(t)dt \qquad (5.1)$$

The voltage and the current waveforms are simultaneously sampled at a sampling rate $f_s = 1/T_s$, and converted to digital values. The instantaneous power is the product of the digital values. If $v(t)$ and $i(t)$ are the instantaneous samples of the voltage and current at time $t_i = iT/N$, then the average power P_0 can be approximated by

$$P_d = \frac{1}{N}\sum_{n=0}^{N-1} v(t_i)i(t_i) \qquad (5.2)$$

where N is the number of samples used in the average.

High-speed digital acquisition of voltage and current data using modern digitizers along with PCs makes this technique a powerful tool for power loss measurement. This method has been used for high frequency magnetic core loss measurement [157][158]. In [157] an automated measurement system for core loss characterization, under sine wave or square wave voltage excitation, is presented (see Fig. 5.2). The core loss of a toroidal core in a temperature-controlled chamber is obtained by computing the mean of the product between primary current (through current-sensing resistor or current probe) and open circuit secondary voltage referred to the primary over an integer number of acquired cycles. Under sinusoidal excitation, the core loss is given by

$$P = \frac{1}{T}\int_0^T v(t)i(t)dt = VI\cos\theta \qquad (5.3)$$

where θ is phase angle between voltage and current. The percentage error in the loss measurement due to uncertainty in the phase is obtained as

$$f(N,\theta)=\frac{\Delta P}{P}=\tan\theta\cdot\Delta\theta\times 100\% \qquad (5.4)$$

The phase error per data sample, $e=360°/N$, causes a maximum phase difference error $\Delta\theta=2e$, where $N=f_s/f_0$ denotes the ratio of sampling rate to excitation frequency. Fig. 5.3 shows the percent error involved in core loss measurement versus phase angle for different sampling number N over a cycle.

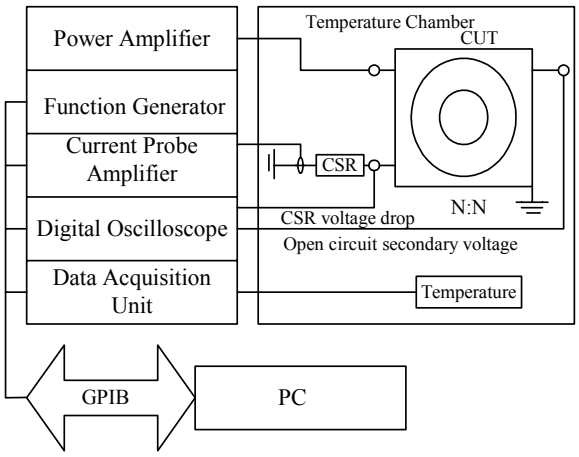


Fig. 5.2 Automated measurement system for core loss.

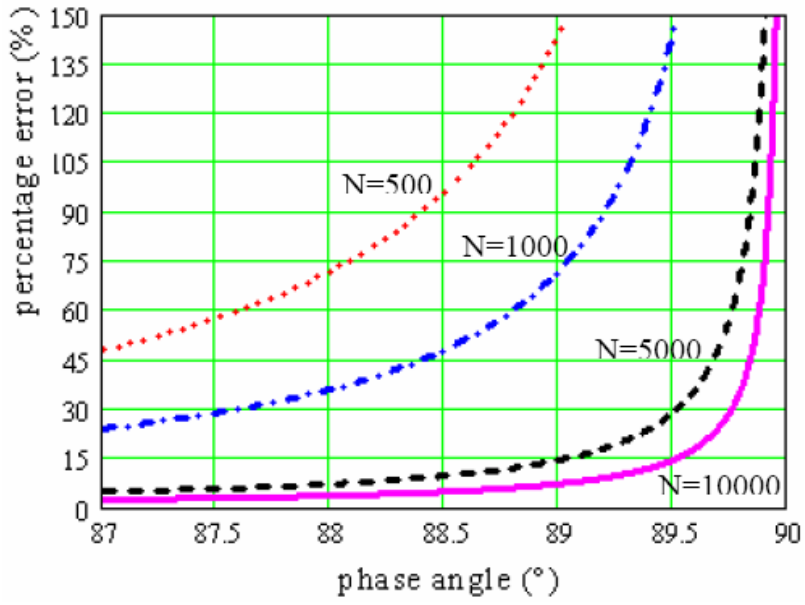


Fig. 5.3 Percentage error caused by sampling uncertainty in phase angle versus phase angle for different N.

Fig. 5.3 illustrate that when θ is close to 90° the percent error can be quite large, even for high sampling rate. The graph shown in Fig. 5.3 represents the maximum percentage error in the loss estimate due to the limited phase resolution only. If the amplitude error caused by the resolution of the digitizer and the delay introduced between current and voltage waveforms due to the probe and the cable are considered, the error will be larger [158].

A computer-based data acquisition system coupled with a digital oscilloscope to create a virtual instrument for instantaneous and average power measurements on resistors, capacitors, AC/DC power converters and BJT inverters is described in [159]. The same technique was adopted in [160] to measure the power loss of transformer. This kind of instrument shows good accuracy for operating frequencies up to 100 kHz. However, when a digital oscilloscope is used for measuring losses in high frequency switching power devices, large errors may occur [161][162[163][164]. During high-speed measurements, parasitic parameters that exist within the measurement system introduce significant aberrations into the measured waveforms. Firstly, different propagation delays due to the physical construction of voltage and current probes are noticeable for MHz signals [165]. Although compensation and correction are recommended to reduce these delays, it is pointed out in [165][166] that compensation alone is not sufficient for overshoots and distortions introduced by probes and cables, especially when the probe's input capacitance is of the same order of magnitude as the capacitance of the device under test. Secondly, the bandwidth and risetime of oscilloscope/probe system also affect measurement accuracy. The equations used to approximate scope/probe system rise time and bandwidth [167] are:

$$\text{System risetime} \approx \sqrt{\text{tr}_{\text{probe}}^2 + \text{tr}_{\text{scope}}^2} \qquad (5.5)$$

$$\text{System bandwidth} \approx \frac{0.4}{\sqrt{\text{tr}_{\text{probe}}^2 + \text{tr}_{\text{scope}}^2}} \qquad (5.6)$$

Table 5.1 shows how the ratio of source bandwidth to system bandwidth affects amplitude attenuation of the measured waveforms. As seen from this table, for reasonable

accuracy Probe/Scope system bandwidth should always be 3 to 5 times larger than measured signal bandwidth.

Table 5.1 SOURCE BANDWIDTH VS. SYSTEM BANDWIDTH

Ratio of Source Bandwidth to Probe/Scope System Bandwidth	Risetime Slowing Amplitude Attenuation
1:1	41%
1:2	12%
1:3	5%
1:5	2%

Finally the ground lead and probe input capacitance could adversely affect the accuracy of measurement by inducing high frequency resonance. Common mode noise may also intrude the measurement system through the ground lead. Susceptibility to RFI/EMI is therefore another important source of uncertainty.

5.3. Review of Calorimetric method for loss measurement

5.3.1. Introduction

In theory higher accuracy is possible by measuring loss directly. Since the total power losses dissipate as heat, the effect caused by the heat can be measured to determine the losses. This can be achieved by calorimetric methods. Consequently, calorimetric method based on direct loss measurement provides a more accurate measurement technique. Calorimetric methods have been widely used in power electronics to measure the power losses of magnetic components [138]-[142], capacitors [143], switching semiconductors [144][145], power converters [146] and electrical machines [137][147]-[155]. Consequently, the calorimetric principle is the most promising of the methods available for accurate power loss measurements [155][156]. This method has the advantage of being able to measure the power losses under normal operating conditions

and being independent of electrical quantities of the device under test. Disadvantages are that it is usually limited to steady state and that the measurement procedure is time-consuming.

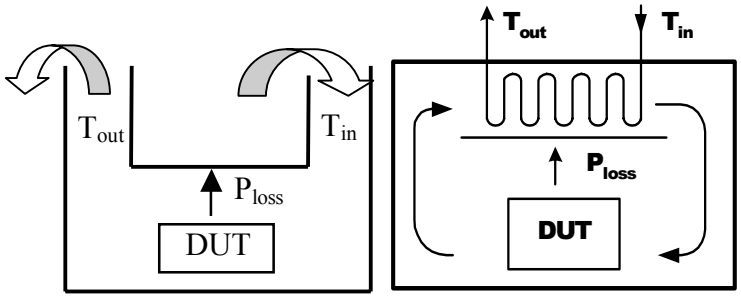
The electrical methods discussed above are all based on indirect loss measurements. Consequently, good accuracy is not easily achieved. Calorimetric methods provide the means for measuring losses directly and are therefore expected to have better accuracy. In addition, they are less dependent on electrical peculiarities of the devices being tested. One challenge is then to measure losses of power electronics modules, components or sub-systems under actual operating conditions.

5.3.2. Basic Principle of Operation

The calorimetric method is essentially aimed at measuring the P_{loss} which the DUT (device under test) dissipates as heat within a measurement chamber. If the heat is completely absorbed by the coolant surrounding the DUT, under steady state the power dissipated by the DUT can be calculated, from measured values of the mass flow rate ($\dot{m}$) and temperature rise (ΔT) of the coolant, as follows:

$$P_{loss} = \frac{c_p \cdot m \cdot \Delta T}{dt} = c_p \cdot \dot{m} \cdot \Delta T \qquad (5.7)$$

where c_p is the specific heat of the coolant. The calorimeter can take an open or closed form as in Fig. 5.4.



a) open type calorimeter; b) closed type calorimeter.

Fig. 5.4 Types of calorimeter.

The open type calorimeter exchanges heat directly with the surrounding air, whereas the primary coolant is circulated in a closed loop inside the closed type calorimeters that require heat exchangers to remove the heat. The closed type calorimeter is much more accurate than the open type [147].

Some calorimeters based on the equation above have been presented in [140][141] for transformer loss measurement and in [154] for loss measurement of electrical machines. In [140], the transformer is placed in thermal contact with a calorimeter block having known mass and specific heat values. Assuming that the system is isolated from the environment, the transformer loss can be calculated based on an energy increment of the block, which is a product of the mass, specific heat and temperature rise of the block in a specific time interval. However, in practice the calorimeter block and transformer are not perfectly isolated from the environment. It is therefore necessary to compensate for the energy that leaks to the surrounding through insulation and through transformer leads. The thermal connection between two bodies is also critical since the error caused by poor thermal contact can't be compensated.

In [141], the coolant of dielectric fluid FC40, is circulated in the closed cooling system, which consists of the reservoir, pump and, cooling coils near an adiabatic calorimeter tube (Fig. 5.5). A delta-T thermocouple pile is used in this system for a temperature difference measurement and a flow meter for measuring the flow rate. It is important to maintain a constant flow rate through the chamber, minimize the heat leakage through the walls of the chamber and control the temperature of the FC-40 fluid in the reservoir.

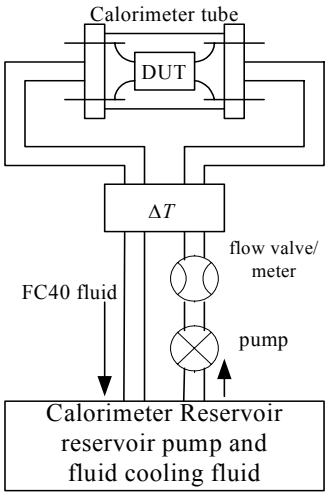


Fig. 5.5 Block diagram of calorimeter illustrated in [141].

5.3.3. Open-type Balance Calorimeter

A single chamber calorimeter was demonstrated by Turner et al. [20] for the measurement of losses in a 5.5 kW induction motor. This open type calorimeter uses air as the coolant and loss measurement is based on the balance method. Determination of the unknown losses takes place in two parts — the DUT test and the balance test. Essentially, the input power in the balance test is adjusted until the coolant temperature rise is the same as the value obtained during the DUT test. This method eliminates the need to measure the specific heat, coolant flow rate. However, the cooling fluid has to keep the same properties (such as temperature, relative humidity, pressure, and flow rate.) in the two tests. In [20] a worst-case accuracy of 1.45% was reported at full load. The DUT test and the balance test lasted between 6 and 8 hours. This simple balance calorimetric technique has also been successfully implemented for measuring the losses of power electronic systems in permanent magnetic machines [137] and magnetic components in power converters [139] with good accuracy.

The balance calorimeter is easy to implement. However it is time-consuming. It is difficult to maintain the same measurement conditions for both tests. Generally, expensive equipment and advanced control are required to maintain the same airflow,

temperature and humidity between two tests. As described in [152][153], an improved calorimeter with advanced computer control was designed. Air temperature, humidity, pressure and volume flow rate are accurately measured with high precision instruments and are provided as feedback signal to computer to correct the difference between two tests. Thus very good accuracy is achieved, but at the expense of complicated control, large and complex configuration, and cost. Due to the high repeatability and accuracy, there is no further need for the balance test once calibrated. An accuracy within as little as 0.2% was reported for a loss measurement of a 30 kW induction motor.

Another balance calorimeter presented by Turner is an open type double chamber calorimeter (DCC) [168] shown in Fig. 5.6. The DCC can perform a motor test and a calibration test simultaneously. The ratio of the measured losses to the reference heat losses is proportional to the ratio of the respective air temperature rise. Since the same air is used for both tests, errors are reduced by removing the uncertainty of air's thermal properties between tests. Also the DCC simplifies the calorimeter operations and shortens the test time, but it doubles the chamber size. An overall accuracy of ±15 W was obtained in [168] for 1 kW losses in a 7.5 kW machine, and ±2% error based on the 600 W total losses was reported in a flow calorimeter [169], a variation of DCC technique with labyrinth structure to improve mixing of the air, shown as in Fig. 5.7.

The DCC method is an improved technique, which reduces the testing time compared with the balance test of the single chamber. However, the problem of different heat leakage between two chambers still exists. Once again there is no guarantee that the airflow conditions inside two chambers are similar.

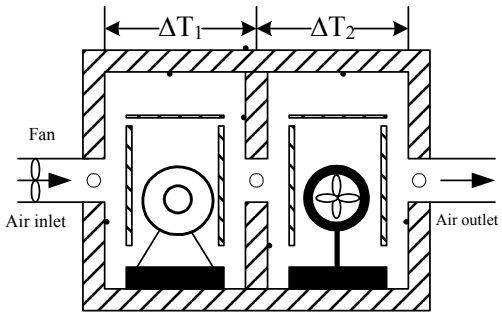


Fig. 5.6 Block diagram of DCC in [168].

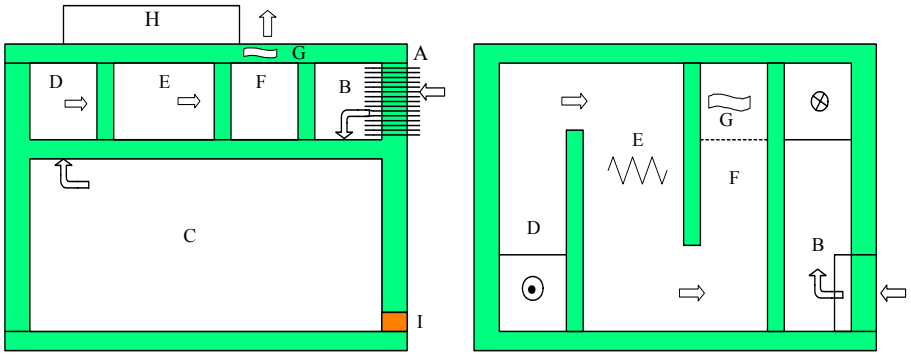


Fig. 5.7 Flow calorimeter

a) front view cross section; b) cross-section view of the labyrinth from the top.

A: temperature equalizer; B: inlet room; C: test room;

D: outlet of test room; E: reference heater; F: outlet of reference heater;

G: regulated fan; H: supply, control and readout; I: cable feed through.

5.3.4. Double-jacketed, Closed Type Calorimeter

As mentioned before, it is very important to minimize the heat leakage through the chamber walls and other parts of the calorimetric chamber. The concept of a double-jacket calorimeter was presented by P.D. Malliban in [147][148][149]. This is essentially a closed type calorimeter that directly measures the power losses according to the basic equation mentioned above, but a second thermally insulating enclosure is introduced to prevent the heat leakage through the walls, and also to ensure that all heat from the DUT is completely absorbed by the coolant. Therefore, the power lost through the chamber walls can be set less than the required absolute accuracy P_{acc}. In theory, the heat leakage in the closed type calorimeter shown in Fig. 5.4(b) can be eliminated if the temperature inside the calorimeter is the same as that of ambient. Thus, a significant improvement in the accuracy of losses measurement is possible by spending half of the time that is typically required by balance calorimeter. The schematic of the double-jacketed calorimeter is depicted in Fig. 5.8.

The outer insulating enclosure isolates the calorimeter from the ambient. The air gap temperature T_e is controlled to be equal to the temperature T_i inside the calorimeter. To

ensure that power loss through the inner calorimeter walls is less than required absolute accuracy P_{acc} the following relation should be satisfied:

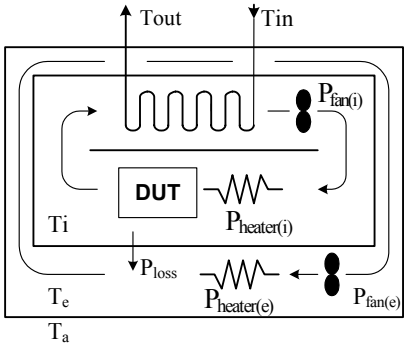


Fig. 5.8 Schematic of double-jacket calorimeter.

$$\left|T_i - T_e\right| < P_{acc} R_{th(cal)} \qquad (5.8)$$

where $R_{th(cal)}$ is the thermal resistance of the inner walls.

Although the calorimeter of [147] was originally designed to test a motor up to 1.1 kW, it can also be used to perform tests on a 2.2 kW induction motor [148]. An air/water heat exchanger placed inside the chamber is used to absorb the heat dissipated by the test motor and DC fans are used to force air through the heat exchanger. A water tank is located above the calorimeter. The flow rate is measured by weighing the water at fixed intervals of time and is adjusted by throttling the valve. The insulating wall and motor support structure were carefully designed to reduce the heat leakage. Heaters and fans were evenly placed in the air gap to ensure uniform temperature distribution on the surface and to avoid local cold or hot spots. With special attention paid to the potential sources of error and improved design, 0.5 W accuracy on a full scale of 300 W was achieved by using this calorimeter. It is claimed in [148] that an accuracy of 0.1 W over 200 W is possible with smaller and more accurate calorimeters.

A calorimetric wattmeter (shown in Fig. 5.9) constructed at Aalborg University is also a double-jacketed closed-type calorimeter [155][156]. It consists of two concentric thermally insulated boxes. The surfaces of the inner test chamber are coated with glass fiber and epoxy. It is equipped with an internal heating system that serves the dual

purposes of creating a desired test temperature and for calibration. An array of 68 light bulbs in the air gap regulates the surface temperatures to minimize the heat flux through the walls. These bulbs also lead to faster response by radiating the heat to the surface. A gear pump controls water flow rate and a flow meter senses the flow rate. A refrigeration unit combined with a heater before the inlet controls the inlet coolant temperature. The heat dissipated from the DUT is absorbed by the flowing water through the heat exchanger. Numerous temperature sensors are installed in the measurement system for measuring temperatures in different locations. A PC with LabViewTM is used to control, regulate and store all the data. An empirical formula was presented to compute the inlet temperature and mass flow in advance by using a predicted value of the power loss as an input. This calorimeter can measure power losses in the range of between 1W and 50W with an error of less than ±0.2% at full load. The physical size of the DUT was 200×200×300 mm, but could be up to 1000×1000×700 mm for measuring losses of between 200~1500 W.

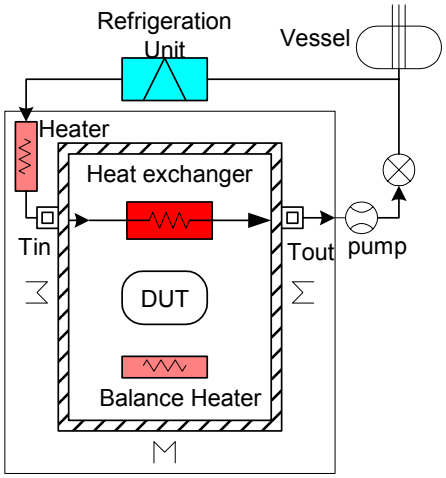


Fig. 5.9 Diagram of calorimetric wattmeter designed in [155].

These tests demonstrate that the implementation of a double-jacketed enclosure in the calorimeter could increase the accuracy considerably by active control of the air gap temperature and by implementing automatic computer control.

5.3.5. Calorimeter Based on Heat-flux Sensor

A simple and accurate apparatus for measuring the losses in a magnetic component is presented in [138] (Fig. 5.10). A heat flux sensor is embedded inside a pedestal on which the DUT is mounted. A liquid-cooled base plate serves as the heat exchanger. The heat passing through the sensor generates a temperature difference between the two sides of the sensor. The temperature difference is proportional to the heat flux through the sensor and is converted to a voltage signal. A heat spreader distributes the heat over the sensor area. The apparatus is designed such that almost all the heat generated in the DUT passes through the heat flux sensor. Accuracy of the instrument depends on how well this condition is satisfied.

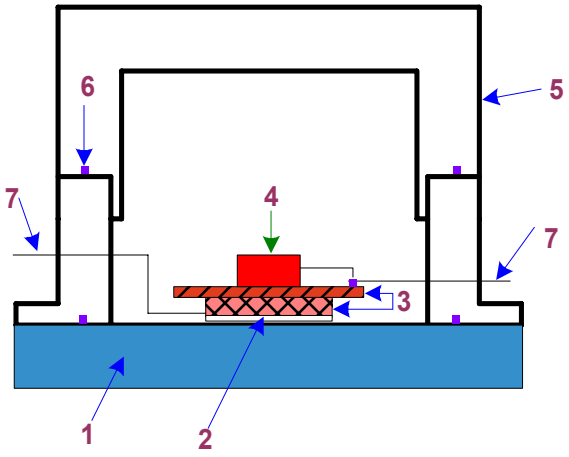


Fig. 5.10 Schematic of calorimeter based on heat flux sensor.

1: aluminum base plate; 2: heat flux sensor; 3: heat spreader;

4: DUT; 5: aluminum cover; 6: fitting; 7: lead wires.

The liquid-cooled base plate allows most of the heat to flow downwards through the heat flux sensor. The chamber is evacuated to minimize convection heat loss and inside surfaces are polished to minimize the radiation heat loss through the cover. Factors that affect the measurement accuracy were analyzed by using thermal analysis software. The apparatus is suited for measuring power losses of relatively small components to within ±5% error. This method is easier to implement and operate in comparison with the calorimetric methods described above. It doesn't need a liquid bath or a liquid flow system and the thermal time constants are significantly shorter.

5.3.6. Summary

From the discussion of various calorimeters above, it's clear that every method has its own features and advantages.

The open type calorimeter uses air as coolant, thus eliminating the risk of leaking fluids. The cooling system is very simple, however, properties of air such as density and specific heat are easily affected by ambient temperature, pressure and humidity. Air as coolant is also more prone to uneven temperature distributions inside the chamber. Therefore the open type calorimeter is unsuitable for a direct calorimetric measurement. Although the balance calorimeter and the DCC calorimeter facilitates the applications of the calorimetric method by eliminating the need for direct measurements of air density and flow rate, problems such as heat leakage between two tests or chambers and great temperature gradients still exist. These problems were addressed in [152], but at the expense of significant increase in complexity and cost.

For the closed type calorimeter water or another fluid is used as coolant. The density and specific heat of such coolants can be determined more accurately and are not affected much by the changes in the environment. The volume and flow rate can also be determined easily. Since the density and specific heat of such coolants are much larger than those of air, the volume flow rate is much smaller for a given power loss, resulting in smaller duct sizes and slower flow velocities. This method may therefore be used for a direct calorimetric measurement or a balance test with better accuracy than that of the open type calorimeters. Active temperature control by adding another insulating enclosure and automatic computer control increases the measurement accuracy considerably. However, liquid coolant and a heat exchanger are needed in the closed cooling system, making this system complex and expensive.

The dry calorimeter based on heat-flux sensor is an effective and simple construction. Fewer accessories are required compared to the other calorimeters, and the testing time can be reduced because of small time constants.

5.4. Proposed calorimeter for loss measurement

A new dry calorimeter with a heat flux sensor, but combining the features of the double-jacketed, closed-type calorimeter, is presented for measuring power loss of the active IPEMs, passive IPEMs and other integrated modules [170]. The DUT (device under test) is placed in an air-tight chamber. The temperature difference between two polished covers in the apparatus is controlled in order to reduce the heat escape caused by convection and radiation. A heat flux sensor placed under the highly conductive pedestal senses the total heat generated in the DUT. A pair of thermoelectric modules is introduced to cool the DUT and control the operating temperature of the DUT. The heat sink, TE modules and heat flux sensor together therefore replace the liquid cooling systems that characterize the other calorimetric measuring methods. Compared with the conventional cooling systems, thermoelectric modules have advantages such as the absence of any moving parts, no need for coolant, no position-dependent, small size, high reliability, and easy for control. The proposed calorimeter is easy to setup and operate, losses up to 25 W can be measured with an expected error of less than 5%.

5.4.1. Introduction

A schematic diagram of the proposed calorimeter is shown in Fig. 5.11. The DUT is mounted on a thermally conductive aluminum plate (plate I), under which a heat flux sensor is mounted for sensing the overall heat generated in the DUT. Another aluminum plate (plate II) is mounted beneath the heat flux sensor as a heat spreader. Below the plate II are two thermoelectric (TE) modules well contacted with the heat sink. During operation, the TE modules keep the temperature of plate II at a constant value, so the TE modules are used to direct the heat flow through the heat flux sensor. The value of power loss in the DUT can be obtained from the output voltage of the heat flux sensor. Two highly polished aluminum covers minimize the radiation. Heaters are mounted on the outer cover for the temperature control so that the temperature difference between two covers can be reduced to minimize the heat escaping via the two covers. Fiberglass fills

the space between the two covers and surrounds the whole chamber. This apparatus is designed so that all the heat generated in the DUT flow through the heat flux sensor. The accuracy of the apparatus depends on how well this requirement is met.

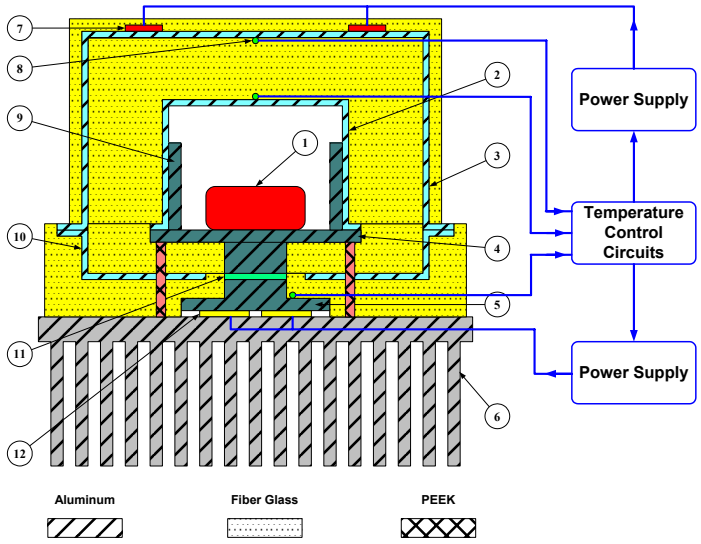


Fig. 5.11 Schematic of the proposed calorimeter.

1: DUT; 2: Inner Al cover; 3: Outer Al cover; 4: Al Base Plate I;

5: Al Base Plate II; 6: Heat sink; 7: Heater; 8: Thermocouple;

9: Fins; 10: Insulated material; 11. Heat flux sensor; 12: TE module.

Heat flux sensor

This sensor measures the rate of thermal energy flow per unit area (heat flux). In the proposed apparatus, the sensor is placed between two aluminum plates with good thermal contact. When heat flows through the sensor, a small temperature difference develops across the multi-junction thermopile. Each thermocouple pair of the thermopile produces a voltage proportional to heat flux. The total voltage across the thermopile is the sum of these voltages and indicates the direction and magnitude of heat flux. The sensor has the following advantages:

- low profile
- low thermal resistance
- easily attached to curved and flat surfaces
- wide temperature range
- fast response time

- conveniently interfaces with voltmeters or recorders

There are two types of heat flux sensors to choose from. One is HFS-4 from Omega. The other one is BF-03 produced by Vatell Corporation .Some information of the two sensors is listed in Table 5.2. HFS-4 was chosen as the heat flux sensor in our proposed calorimeter.

Table 5.2 Date of heat flux sensors

Model	Sensitivity $mV/(W/cm^2)$	Response time (sec)	Thermal Resistance $K/(W/m^2)$	Thickness (mm)	Size (mm)	Manufacturer
HFS-4	20.62	0.7	0.00352	0.23	35×28.6	Omega
BF-03	50	0.9	0.0008	0.2	51×51	Vatell Corp.

To take full advantage of the low thermal resistance of the heat flux sensor, it should be mounted so that there is a good thermal contact between the sensor and the test surface. A concerted effort should be made to prevent any air bubbles, dirt, or water from becoming trapped between the sensor and the test surface. So the sensor should be mounted on a smooth, clean, dry surface. A thin, uniform layer of the paste should be applied to the sensor and then press the sensor gently to test surface. Use the smallest amount of paste possible. Not only is excess paste messy, but also it can slow the response time of the sensor.

Thermoelectric modules

A thermoelectric module is a semiconductor-based electronic component that functions as a small heat pump. Four basic physical phenomena are related to the operation of thermoelectric devices: The Seebeck effect, the Peltier effect, the Thomson effect, and the Joule effect. The Seebeck effect means that the voltage is generated when a temperature change is maintained between the two sides of a TEC. The Peltier effect is the heating or cooling effect observed when an electrical current is passed through two dissimilar junctions. The Thomson effect is heating or cooling effect in a homogeneous conductor observed when an electrical current is passed in the direction of a temperature gradient. This effect plays a negligible role in the operation of practical thermoelectric

modules. The Joule effect is the heating effect observed in a conductor as an electrical current is passed through the conductor.

A typical TE module consists of two ceramic plates with several P-type and N-type semiconductor elements connected electrically in series and thermally in parallel (as shown in Fig. 5.12). The thermal model of the TE module is shown in Fig. 5.13, where T_H is the temperature of the hot side of the TE, T_C is the temperature of the cold side of the TE, V and I are input voltage and input current applied to the TE module, respectively [171]. Q_C is the absorbed heat in the cold side, Q_H is the released heat in the hot side, and P_e is the electric power supplied to the module.

$$Q_H = P_e + Q_C \tag{5.9}$$

$$P_e = VI \tag{5.10}$$

$$V = S_M \times (T_h - T_c) + I \times R_M \tag{5.11}$$

$$Q_c = S_M \times T_c \times I - 0.5 \times I \times R_M - K_M \times (T_h - T_c) \tag{5.12}$$

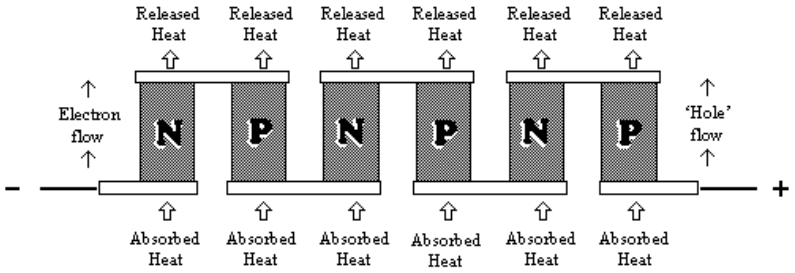


Fig. 5.12 Schematic of a TE module.

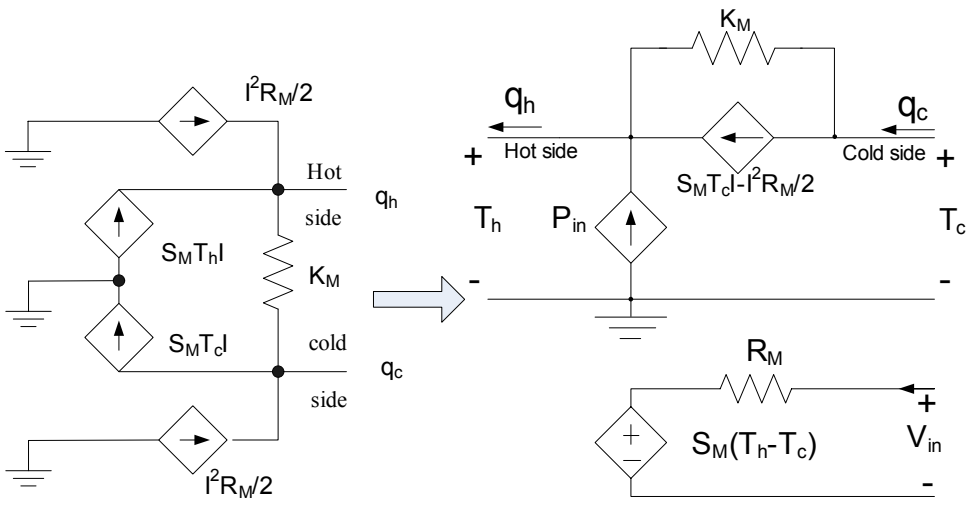


Fig. 5.13 Equivalent thermal model of TE module.

where S_M is the Seebeck coefficient of the module (V/K), R_M is the module's resistance (Ω), K_M is thermal conductance of module (W/K).

By applying a low voltage DC power source to a TE module, heat will be moved through the module from one side to the other, so one side becomes cold while the other is heated. By varying the power to the TE module, TE module can be used to adjust and control the heat flow and temperature. Two identical TE modules CZ1-1.4-127-1.14, electrically in series and thermally in parallel, are used as cooler in the proposed calorimeter to stabilize the temperature of the base plate II. The specifications for the CZ1-1.4-127-1.14 are as follows: I_{max} =8 A, Q_{max} = 78 W, V_{max} = 16.1 V, ΔT_{max} =79 ºC. The heat pumping capacity of the TE module significantly depends on the heat sink, which must be capable of dissipating both the heat pumped by the module as well as the heat losses generated as a result of supplying electrical power to the module. In the proposed apparatus, an air-forced convection heat sink is employed to ensure TE module's performance.

5.4.2. Thermal analysis of the proposed calorimeter

A simple thermal model of the proposed apparatus is shown in Fig. 5.14. The thermal model of the TE module is included, where T_C is the cold side temperature and T_h

is the hot side temperature, I is the input current applied to the TE modules. The heat generated in the DUT flows downwards through the thermal resistance R_{p1} of the base plate I, thermal resistance R_{fs} of the heat flux sensor, thermal resistance R_{p2} of the base plate II, and through the TE modules and heat sink (R_{hs}) into the environment. A small portion of the heat generated in the DUT escapes through the two covers (thermal resistance R_{io}) into the ambient air.

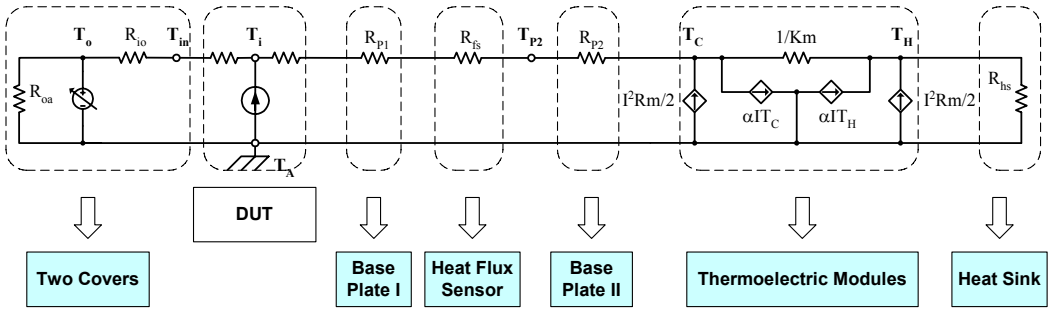


Fig. 5.14 Complete thermal model of the proposed calorimeter.

All of the heat flux that doesn't pass through the flux sensor contributes to the measurement errors. There are two main heat leakage paths in the proposed apparatus: One is the heat leakage through the two covers and the other one is the conducted heat along any power leads which connects the DUT to an external source.

Heat leakage through the two covers

The space between the inner cover and outer cover is full of thermal insulation material (fiber glass). The heat leakage consists of conduction leakage and radiation leakage. The radiation heat leakage is negligible. The heat leakage through the two covers can be expressed as:

$$q_{lc} = \frac{(T_{in} - T_o)}{R_{io}} \qquad (5.13)$$

where T_{in} is the average temperature of the inner cover, T_o is the average temperature of the outer cover, and R_{on} is the thermal resistance between two covers. If the temperature difference between the two covers can be reduced, then the heat leakage through the two covers will also be minimized. In the proposed measurement system, heaters mounted on the outer cover are controlled to keep the temperature of the outer

cover close to that of the inner cover. By monitoring and controlling $\Delta T_{io} = T_i - T_o < 1°\,\mathrm{C}$, the heat leakage will be less than 0.24 W for the proposed calorimeter.

FEM thermal simulation results were obtained to compare the influence of heaters on the heat leakage through the covers. Dimensions of the covers are listed in the Table 5.3. The simulation results for the proposed calorimeters in Fig. 5.15 are shown in Table 5.4. Without heaters on the outer cover, the temperature difference between the inner cover and the outer cover is about 8.7°C, and the heat leakage through the two covers is about 2.18W. When heaters are mounted on the surface of the outer cover, the temperature difference between the two covers can be reduced to about 0.75°C, and the heat leakage through the two covers is then only about 0.19W. Therefore the measurement error of the calorimeter is greatly reduced when the temperature control is introduced between the two covers. Therefore the measurement error is greatly reduced when the temperature control is introduced between the two covers.

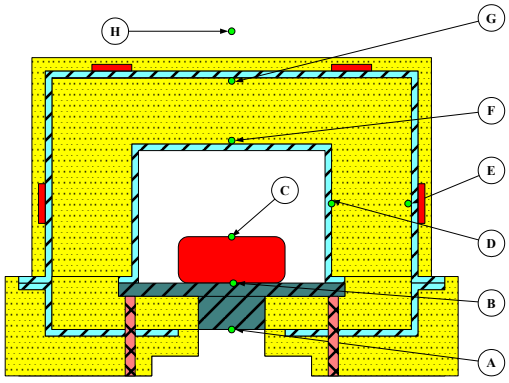


Fig. 5.15 Locations of temperature points of the calorimeter in the thermal simulations.

Table 5.3 Dimensions of the covers.

	Diameter (mm)	Height (mm)	Thickness (mm)
Inner cover	200	150	5
Outer cover	270	180	5
Base cover	270	40	5

Table 5.4 Simulation results of the apparatus

		Temperature (°C)	
		Without Heaters Control	With Heaters control
A	Base Plate I Bottom	36.0	36.0
B	Base Plate I Top	42.4	43.7
C	Device Top	127.3	129.4
D	Inner Cover Side	48.9	49.8
E	Outer Cover Side	40.1	49.0
F	Inner Cover Top	48.4	49.6
G	Out Cover Top	40.1	48.9
H	Ambient	25.0	25.0

Heat leakage along the power leads

The heat leakage through thermocouple wires and power leads must also be calculated to estimate the error of the measurement system. In [140], the conduction heat loss along the wires is calculated assuming that the wire is cooled by natural convection. To calculate the heat leakage through the wires, a steady-state thermal model of the power leads is presented, as shown in Fig. 5.16. T_i is the temperature of the wire's high temperature end. T_{1i} (i is from 1 to n) is temperature in the power leads. T_{2i} (i is from 1 to n-1) is temperature on the insulation surface of the power leads. The thermal resistance R_{1i} of the metal wire with length of dx is

$$R_{1i} = \frac{dx}{k_w \pi a^2 / 4} \qquad (5.14)$$

and the thermal resistance R_{2i} of the insulation of the power lead with the length of dx is

$$R_{2i} = \frac{\ln\left(\frac{a+2b}{a}\right)}{2k_i \pi dx} \qquad (5.15)$$

where k_w is the thermal conductivity of the metal wire, k_i is the thermal conductivity of the insulation, a is the dimension of the metal wire, b is the thickness of the insulation. The convection thermal resistance R_{3i} of the power lead with the length of dx is

$$R_{3i} = \frac{1}{h_c \pi (a+2b) dx} \tag{5.16}$$

where

$$h_c = Nu\left(\frac{k_a}{(a+2b)}\right) \tag{5.17}$$

Nu is the Nusselt number, k_a is the thermal conductivity of air. Nusselt number can be calculated based on the empirical formula as the following:

$$Nu = C \cdot (G_r \cdot P_r)^m \tag{5.18}$$

where G_r is Grashoff number and P_r is Prandtl number.

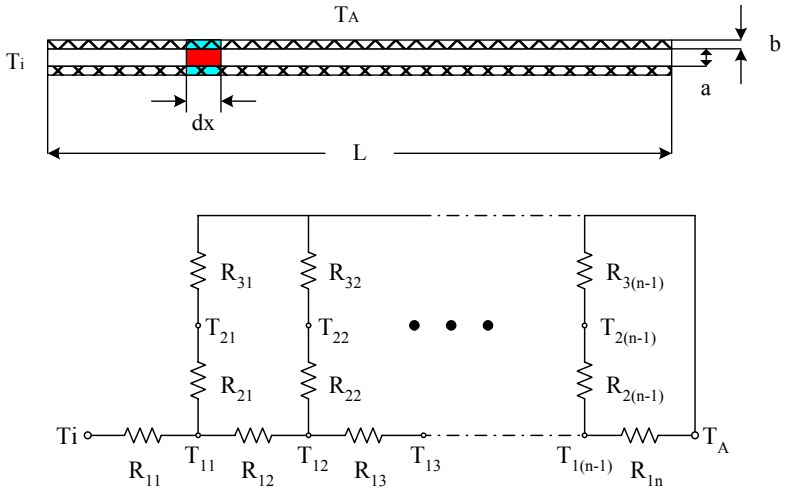


Fig. 5.16 Thermal model of the power leads into the calorimeter.

Take an example, consider an insulated wire with *L=0.2 m, a=1.09 mm, b=1 mm, n=100, K_i=0.1 W/(m·°C), T_i=55 °C, T_A=25 °C*, we get R_{total}=168 °C/W from the thermal model above. The heat leakage along the wire is then:

$$q_w = \frac{T_i - T_A}{R_{total}} = 0.18W \tag{5.19}$$

Also the analytical equation to calculate the heat leakage along the leads can be derived as the following. Considering the energy balance on the wire with the length of dx, we can get

$$-k_w A_c \frac{dT}{dx}|_x = -k_w A_c \frac{dT}{dx}|_{x+dx} + h_{eq} P dx (T - T_a) \quad (5.20)$$

then,

$$\frac{d^2 T}{dx^2} - \frac{h_{eq} P}{k_w A_c}(T - T_a) = 0 \quad (5.21)$$

where $h_{eq} = \dfrac{1}{\dfrac{a}{h_c(a+2b)} + \dfrac{a \ln(a+2b/a)}{2k_i}}$, which combines the thermal resistance of the insulation layer and the convection resistance around the insulation layer; $P = \pi a$, $A_c = \dfrac{\pi a^2}{4}$.

Assuming the power lead loses heat from the end of the lead, the temperature distribution and the total heat leakage along the wire can be obtained:

$$\frac{T - T_a}{T_i - T_a} = \frac{\cosh[m(L-x)] + (h_{eq}/mk_w)\sinh[m(L-x)]}{\cosh mL + (h_{eq}/mk_w)\sinh mL} \quad (5.22)$$

$$q_w = \sqrt{h_{eq} P k_w A_c}\,(T_i - T_a)\frac{\sinh mL + (h_{eq}/mk_w)\cosh mL}{\cosh mL + (h_{eq}/mk_w)\sinh mL} \quad (5.23)$$

where $m^2 = \dfrac{h_{eq} P}{k_w A_c}$.

Some results are shown in figures (Fig. 5.17 ~ Fig. 5.19) below. The following conclusions are made: The heat loss of the wire increases with increasing wire diameter, and increases with the length of the wire when the wire's length is small. But when the length of the wire is beyond a critical value, the heat loss will almost remain constant. Note that the insulation of the wire may actually increase the heat loss released from the wire as a function of insulation thickness until heat loss reaches a maximum value at a critical radius, beyond which the heat loss will start decreasing.

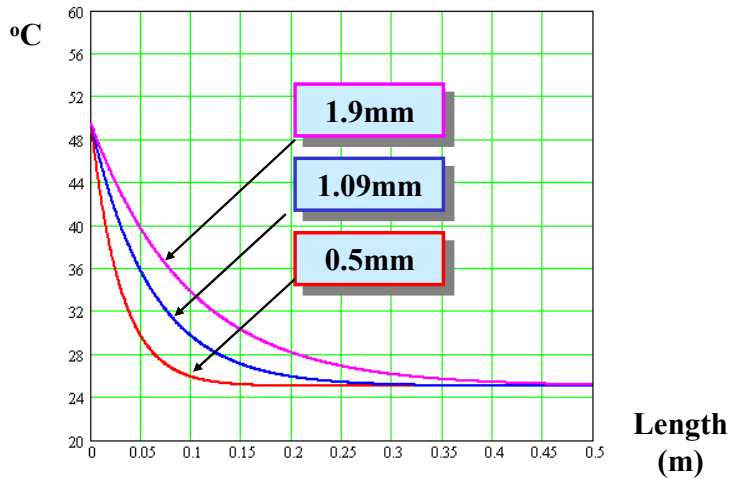


Fig. 5.17 Temperature distribution for 3 diameters of the wire: 0.5 mm, 1.09 mm, and 1.9 mm when b=1 mm.

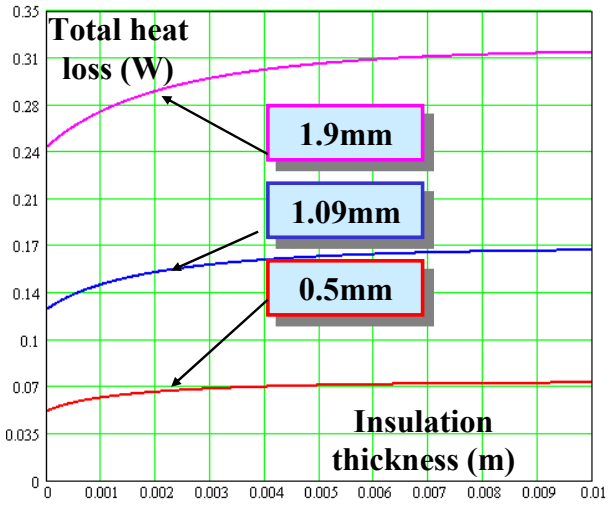


Fig. 5.18 Total heat loss for 3 diameters of wire: 0.5 mm, 1.09 mm, and 1.9 mm.

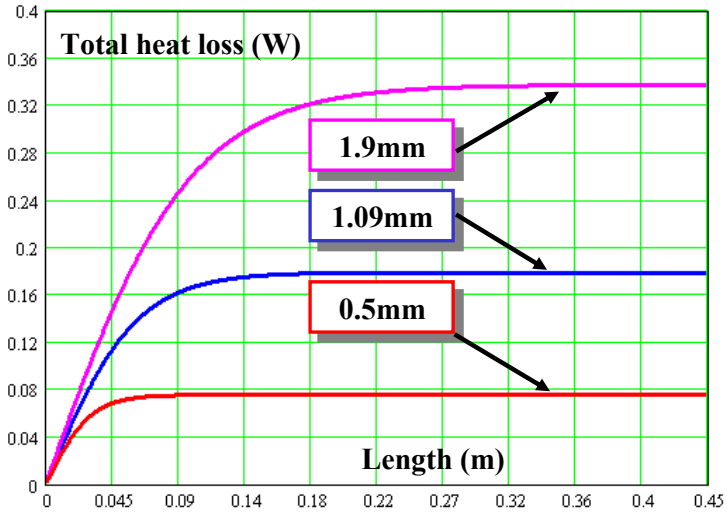


Fig. 5.19 Heat leakage as a function of length for given diameters: 0.5 mm, 1.09 mm, and 1.9 mm when b = 1 mm.

In the conventional analysis of the heat loss along the wire where the effect of convection is neglected and only the conduction heat transfer along the axial direction is considered, the result is $q_w = 0.05$ W. This shows that the heat leakage along the wires is underestimated by the conventional analysis.

5.4.3. Calibration and experiment

The design process of the calorimeter is described in Appendix III. Fig. 5.20 shows the prototype calorimeter.

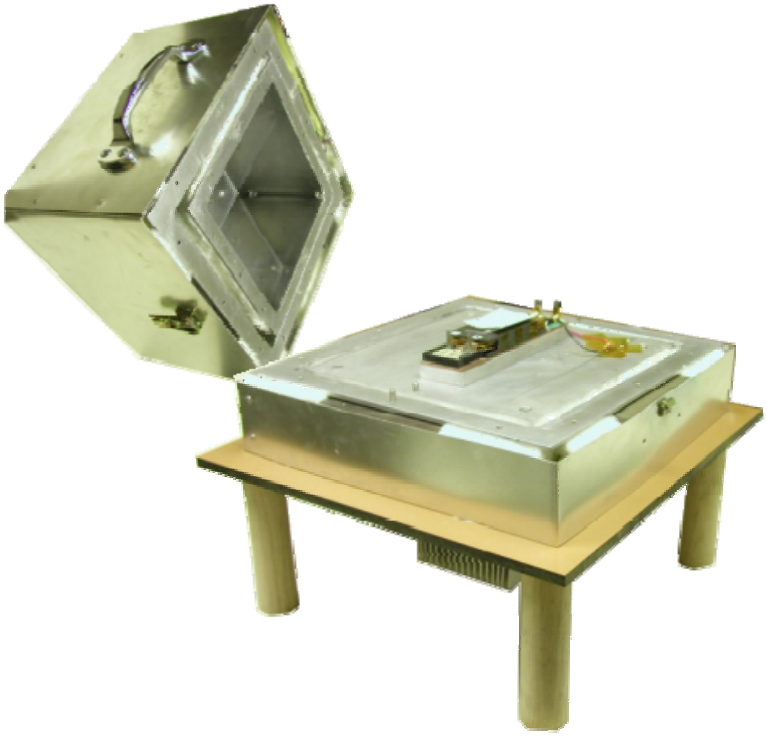


Fig. 5.20 Prototype of the proposed calorimeter.

Calibration was performed by using a power resistor in place of the DUT and subjecting it to a known DC power. The resistor was chosen for its ability to maintain high accuracy over a wide temperature range. The measured power loss of the resistor as a function of the heat flux sensor output in mV is given in Fig. 5.21. The calculated power losses based on the sensor's sensitivity are also plotted on the same graph. The measured and calculated power losses are given in Table 5.5. The figures and tables show good agreement with the calculated results.

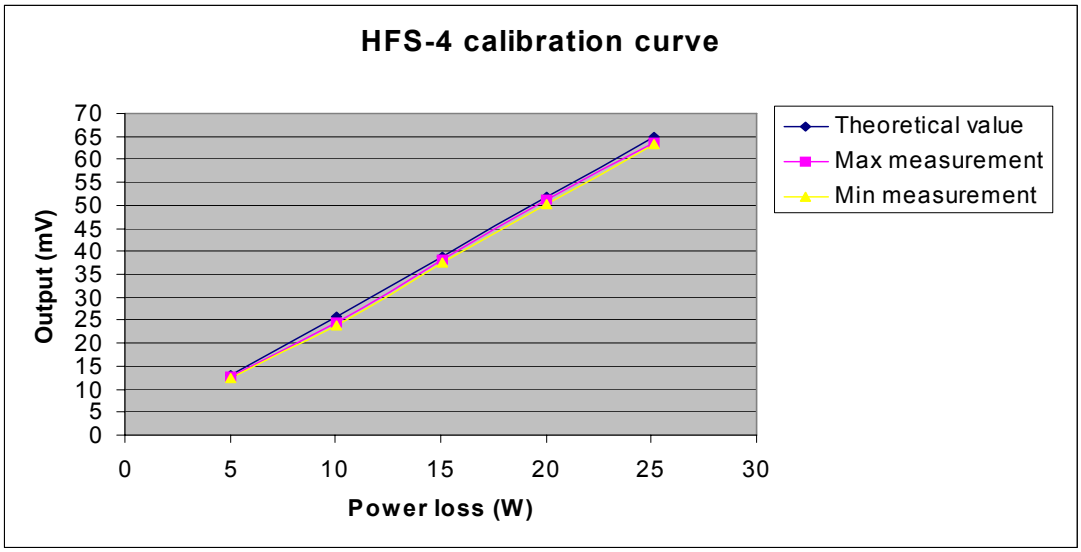


Fig. 5.21 Comparison between measured results and theoretical values.

Table 5.5 Calibration results

Input power (W)	Theoretical (mV)	Measured Max value	Measured Min value	Min error	Max error
4.99±1.5%	12.89	12.84	12.32	3.88%	4.44%
10.04±1.5%	25.9	24.6	23.8	5.02%	8.10%
15.07±1.5%	38.95	38.2	37.44	1.92%	3.88%
20.02±1.5%	51.75	51.36	50.4	0.75%	2.6%
25.11±1.5%	64.9	63.48	63.2	2.2%	2.62%

5.5. Summary

Various power loss measurement techniques, including electrical and calorimetric methods, are reviewed along with their advantages and disadvantages. The limits of electrical power loss measurement techniques are analyzed. They are not suitable for high efficiency systems due to the difficulty extracting losses from two nearly equal numbers. Also electrical measurement methods are not suitable for high frequency signals due to larger errors introduced by measuring equipments and interferences from the environments.

A simple dry type calorimeter for accurate power loss measurements was developed, analyzed, tested and herein presented. Compared to other calorimetric methods, it does not need a complex liquid cooling system. A heat flux sensor and thermoelectric modules in the apparatus, in combination with simple control circuits, make this structure compact and simple to use. The apparatus is easy to set up and very cost-effective. Factors affecting the accuracy of the calorimeter were identified and considered in its design and practical development. Double polished aluminum covers with temperature difference control minimize the heat leakage through the covers, and the inner test chamber is air-tight to minimize the heat leakage. Empirical calibration verifies that the apparatus has an acceptable accuracy. The calorimeter is also suitable for other low power losses measurement applications.

Chapter 6 Conclusion and Future Work

6.1. Conclusion

This thesis is an attempt to investigate the fundamental frequency limitations for HF/VHF power conversion technology in order to optimize the power density and efficiency as the frequency is pushed higher and higher. Major emphasis is placed on fundamental investigations with regards to: power conversion structures, semiconductor devices, passive components, and power loss measurement techniques. The major accomplishments and conclusion are summarized below:

- The existing state-of-the-art HF/VHF power conversion technologies were briefly reviewed, focusing on their topologies, power levels, frequency levels, dimensions, and implementation techniques. The trend of power levels and frequencies is extracted to estimate the future development of HF/VHF power conversion. Raising the frequency is a common method for increasing power density. When frequency increases beyond a certain range or value, the dimension of power converters begin to increase again due to the complex interplay of design trade-offs, thus degrading the power density. A fundamental limit responsible for the trade-off between the power and frequency ultimately depends on the physical properties of the semiconductor materials, i.e., critical breakdown field and saturated drift velocity. It is this fundamental limitation being imposed by the semiconductor devices that determines the upper bound of power level as frequency increases. Semiconductor materials with higher breakdown field and drift velocity have larger power-frequency products. This indicates that in order to optimize the power density in the future as frequency increases it is necessary to apply new materials with higher breakdown field and drift velocity into the semiconductor devices, besides the

advances in other constituent technologies.

- A DC-DC power converter (derived from the RF Class E power amplifier), which is very suitable for VHF power conversion and that dominates the higher end of the frequency scale, is analyzed with a detailed discussion and derivation of design equations. A 250 MHz prototype (implemented using discrete surface-mounted components) is demonstrated along with the experiment results, which achieves the highest frequency among the discrete power converters ever found in the literature.

- Power losses, including conduction loss and switching loss, in the semiconductor devices can be represented by ON-resistance and device capacitance. The smaller the product of ON-resistance and device capacitance is, the higher the efficiencies of HF power architectures can be. In order to improve the efficiency of power conversion system, the product of ON-resistance and device capacitance should be minimized. By relating the product to the intrinsic material properties, the power loss can be reduced by using semiconductor materials exhibiting a larger breakdown field and a larger mobility whilst the die area is also reduced. When the semiconductor material is given, the minimum power loss in the device will increase with increasing frequency, leading to lower efficiency of the system. And the device die area at which the minimum power loss occurs is reduced with switching frequency.

- A generic multi-disciplinary model was constructed and then used to analyze the performances of passive components (i.e. power density and power conversion efficiency) as functions of frequency. For magnetic components, there is an optimum frequency (or frequencies) at which the power density and power conversion efficiency is maximized, and beyond which the reverse is true. It was demonstrated how this optimum frequency (or frequency limit) can be identified, and how power

conversion efficiency deteriorates beyond the optimum under a fixed maximum temperature. Therefore further increases in operating frequencies to improve power density are not always beneficial in terms of power density. The frequency scaling investigation of passive components (capacitors and magnetics) shows how frequency dependencies of material properties are responsible for high frequency operation. The method can be extended to identify the most optimum power conversion frequency for a given set of specifications, circuit functions, selection of materials and packaging technology, and thermal conditions.

- Using the results from the fundamental limitations of the power devices and passive components in the power converter, the power density and efficiency as a function of frequency scaling is plotted in Fig. 6.1. It is clear that pursuing high frequency alone doesn't necessarily lead to improved power density and efficiency. Some compromises must be made between different requirements with respect to specific applications.

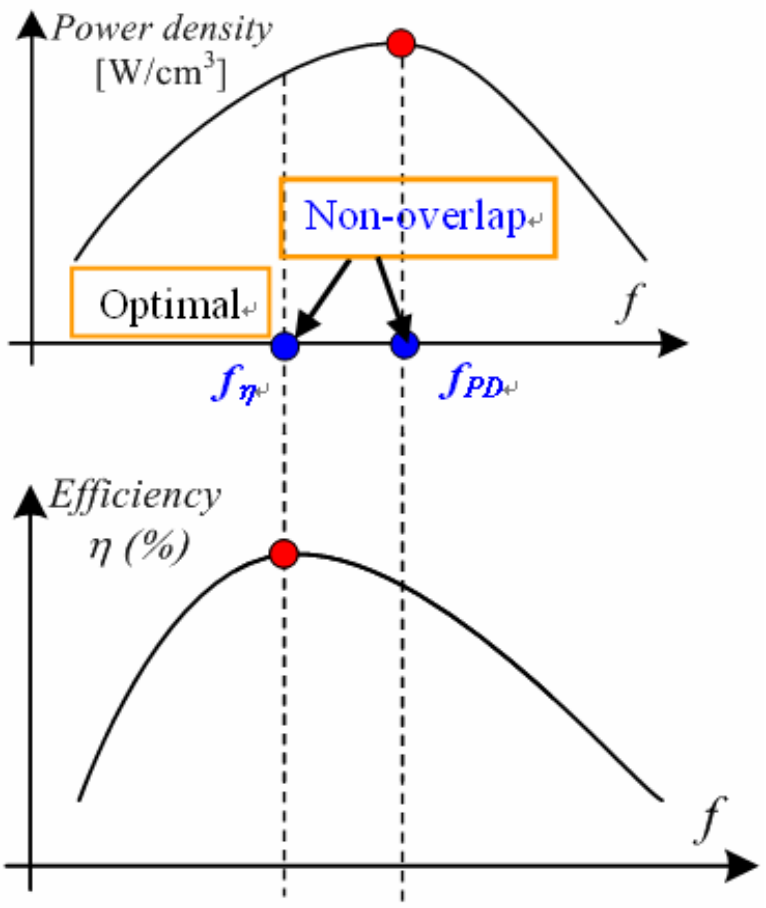


Fig. 6.1 Power density and efficiency variation with switching frequency.

- The limitations of electrical loss measurement techniques are analyzed, exhibiting large error for high-efficiency, high-frequency power electronics system. Various calorimetric methods for loss measurement are reviewed, demonstrating reduced errors due to the direct measurement of thermal heat flux. A new advanced calorimetric measurement system for accurate power loss measurement is proposed, analyzed and tested. Compared to other calorimetric methods, it does not need a complex liquid cooling system. A heat flux sensor and thermoelectric modules, in combination with simple control circuits, make this system compact and easy to use. It has the ability to measure heatsink-mounted components such as IPEMs, passive IPEMs and integrated magnetics. The calibration of the calorimetric system demonstrates about 5% error in up to 25 W total

losses.

6.2. Future work

The investigation of fundamental frequency limitations for HF/VHF power conversion is a quite broad, complex and systematic subject, requiring knowledge from many different disciplines in the different fields related to power electronics system. In order to continue pushing the trend towards miniaturization of power converter, the other fundamental limitations in packaging, integration, interconnects and thermal management technologies should be further investigated, identified and optimized for optimum performances of the power converter. The guidelines and design tools demonstrated in the dissertation can be extended to the future work as the follows.

(1) Evaluation of new semiconductor devices for HF/VHF power conversion.

New semiconductor devices with better material properties than those of silicon should be evaluated in the power converter for their performances in terms of power level, efficiency, frequency, power density.

(2) Further improvement of Class E RF DC-DC power converter for better efficiency and power density.

Class E RF DC-DC power converter demonstrates promising potential for VHF power conversion. It is necessary to apply new devices and new control strategies (such as the multi-switching cell concepts) in a higher level of integration techniques to achieve higher efficiency, increased power and higher power density.

(3) Optimization of power density or efficiency through the optimization of passive and active components by frequency selection at the system level design stage.

Based on the present available high frequency power devices, magnetic materials and dielectric materials, evaluate some frequency ranges for optimum power density or efficiency at different power levels. If necessary, investigate the feasible frequency range for the applications of air core magnetic components.

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Chapter 1 & 2:

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Appendix I Implementation of RF DC-DC power converter

The DC-DC converter with Class E inverter and Class E rectifier is supposed to be implemented with discrete components and operate at $f = 250MHz$. In such high frequency circuitry, it is critical to select proper components that can operate under this frequency. Grounding and proper placement of switching components are also crucial to achieve the desirable performance.

A. Component selection of the circuitry – LDMOSFET and passive components

A wide variety of active devices is currently available for use in RF applications. Traditionally, RF power transistors have been built using Si bipolar technology, although GaAs power transistors area also available. Recently, laterally diffused metal-oxide-semiconductor (LDMOSFET) transistors have been proven to be very popular for these applications [81].

LDMOSFET is a modified n-channel MOSFET specifically designed for both high frequency and power amplifier applications. The significantly reduced parasitic capacitances, especially the miller feedback capacitance, make it suitable for high frequency applications. They have superior RF performance compared to bipolar transistors and are highly cost-effective compared to their GaAs counterparts. Most MESFETs are deletion-mode devices and require a negative gate bias. Therefore LDMOSFET is a better candidate over GaAs MESFET for switching applications in the proposed RF DC-DC power converter.

LDMOS is especially useful at UHF and lower microwave frequencies because direct grounding of its source eliminates bond-wire inductance. LDMOS devices allow the breakdown voltage to be above 80V while maintaining good frequency performance,

opening the door of high power and high frequency operation to bulk-Si technology. Also LDMOS technology is compatible with CMOS process and passive components [82], providing the potential for the integrated implementation.

Some key parameters of several LDMOS devices are listed in Table A. 1. L8711P from Polyfet is chosen as the switching device in the prototype due to its low cost and easy availability from vendors.

Table A. 1 Comparison of several LDMOSFETs.

Part	Vendor	f (GHz)	$V_{(BR)DSS}$ (V)	P_{D_max} (W)	Rds_on (Ω)	C_{oss} (pF)	C_{iss} (pF)
PD57018S	ST	1	65	31.7	0.72 (V_{gs}=10V, I_d=1.25A)	21	34.5
MRF284LSR1	Motorola	2	65	87.5	0.3 (V_{gs}=10V, I_d=1A)	23	43
MRF6522-70R3	Freescale	1	65	159	0.15 (V_{gs}=10V, I_d=1A)	47	130
L8711P	Polyfet	1	36	60	0.4 (V_{gs}=20V, I_d=8A)	40	50

Discrete passive components are employed in the prototype of RF DC-DC converter. In comparison to the distributed elements, they have the advantage of smaller size, lower cost, smaller interaction effects between discrete components and wider bandwidth characteristics in this frequency range although discrete passive components exhibit lower quality factor Q [83].

Components for applications in resonant, matching and filter sections are required to meet the requirements of high Q, high self-resonant frequency and low parasitic values. RFC choke in the circuit need higher current-handling capability and lower dc resistance values.

As there are few magnetic materials that can be applied in such high frequency range, air-core inductors are selected in the converter. RF air core inductors from Coilcraft® are found to be very suitable for RF application. They feature tight inductance tolerance and thermal stability, which can often eliminate the need for circuit tuning. They have high SRF (Self-resonant frequency) in the order of GHz. The product of inductance and SRF for smaller value inductors is as large as 24 nH – GHz, whereas for

large value inductors (100 nH) the product is as large as 120 nH – 1 GHz. The mini spring air core inductors from Coilcraft have inductance from 2.5nH to 43 nH with SRF ranging from 12.5 GHz to 1.2 GHz. For large inductance, for example, 120 nH midi spring air core inductor has SRF at 1.1 GHz. These air core inductors are in form of surface mount and provide extremely high Q over a wide frequency range. For example, mini spring air core inductors from Coilcraft can achieve a minimum Q-value of 100. Fig. A 1 shows the variation of Q as a function of frequency [84]. The inductors with the current rating of 4 A are also available.

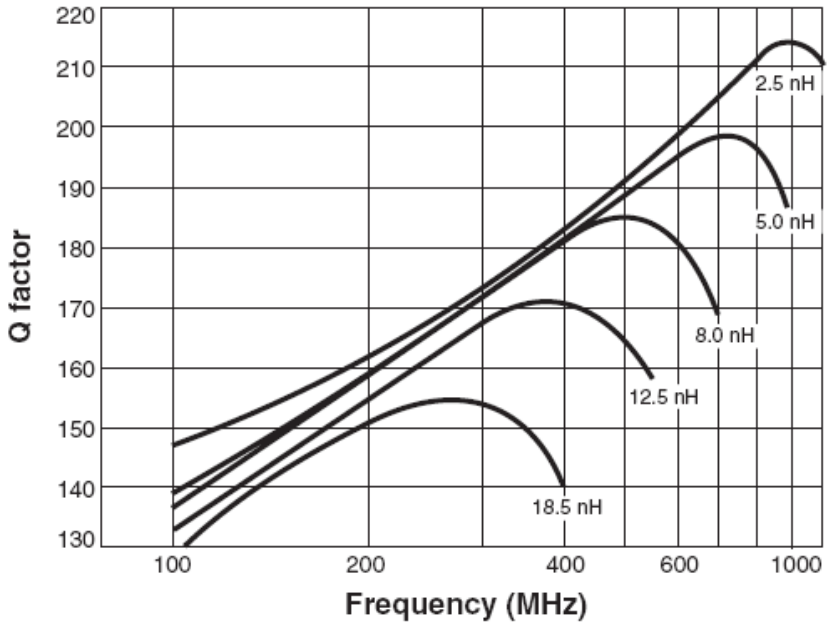


Fig. A 1 Typical variation of Q vs frequency for mini spring air core inductors from Coilcraft.

When selecting a capacitor, one should consider several parameters including capacitance value, tolerances, the quality factor Q, ESR, SRF, voltage rating, current rating, temperature coefficient, and cost [83]. A typical range for RF applications is from 0.1 pF to 1 μF. All discrete capacitors at radio frequencies have both resistance and inductance. Series resistance in a capacitor is determined by knowing the Q of the capacitor at the operating frequency. When a capacitor is represented by a series combination of capacitance C and resistance R_s, the quality factor Q is defined as $Q = \frac{1}{\omega C R_s} = \frac{1}{2\pi f C R_s}$. The chip capacitors from ATC and AVX are available for RF applications, featuring high Q, low ESR/ESL, high SRF, low noise and ultra stable

performance. Fig. A 2 shows typical measured Q values of ATC series 100B chip capacitors. For a 22 pF capacitor, the Q is around 100 at 1GHz. Fig. A 3 shows typical ESR values for ATC series 100B chip capacitors. For a 22 pF capacitor, ESR is about 0.06 Ohm at 500 MHz.

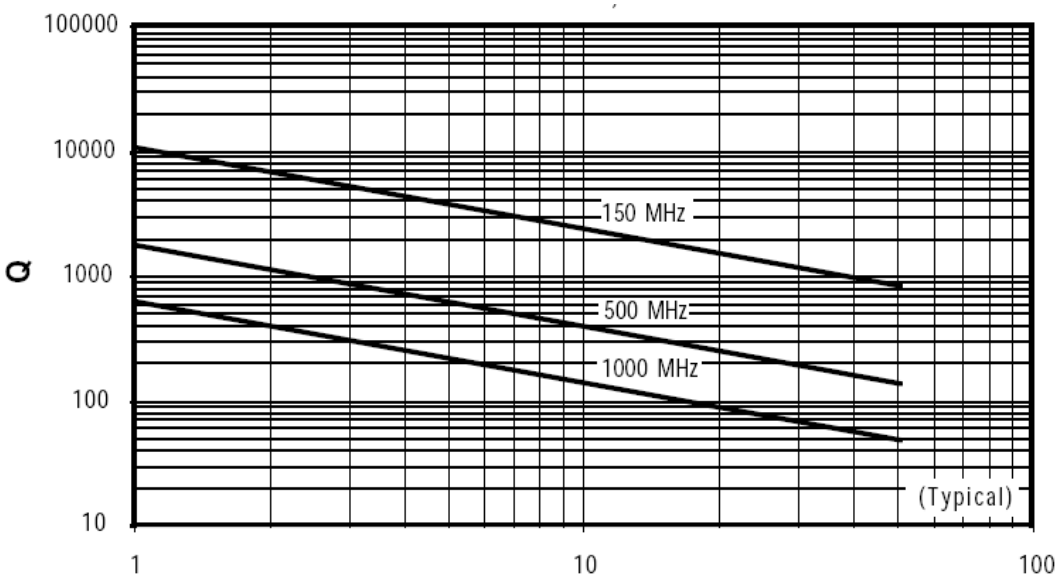


Fig. A 2 Typical variation of Q vs capacitance of ATC chip capacitors.

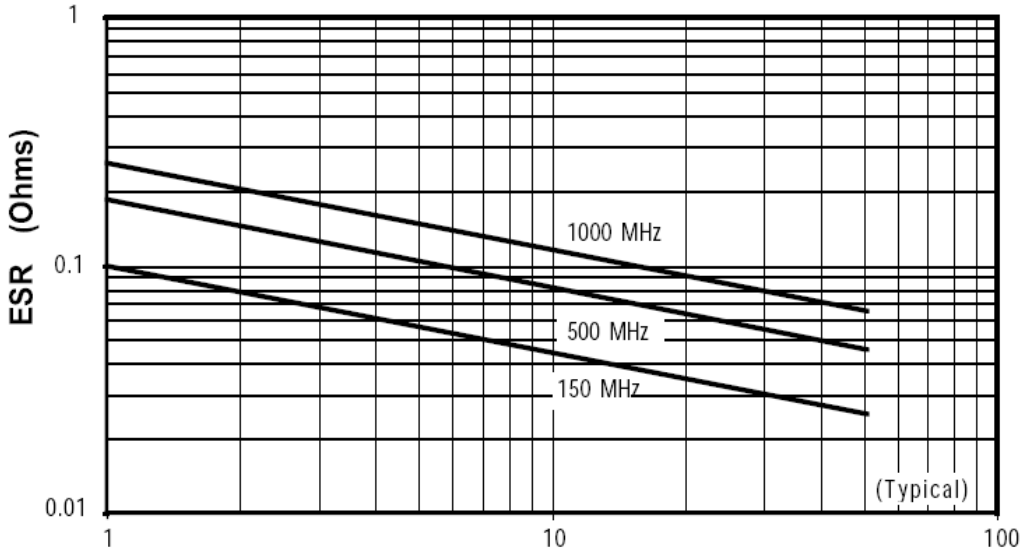


Fig. A 3 ESR vs capacitance of ATC chip capacitors.

B. Layout and parasitic extraction

The implementation of proper layout in switching converters is essential to the successful operation of the converters. The importance of a good layout in the VHF ranges cannot be overstated. The layout factors can affect the performance of the switching converter. The considerations that affect the circuit board layout include: radiated electromagnetic interference (radiated EMI), conducted EMI, stability, efficiency and operational longevity. It is really a critical challenge to layout the RF circuit board. However the knowledge about the layout fundamentals for switching circuits makes the efforts much easier.

Switching power converter has large current pulses with very sharp edges flowing within the circuit. These current pulses have the greatest effect on the creation of EMI, particular attention should be paid to place the components of these loops. Fig. A 4 shows these current loops for the proposed RF power converter.

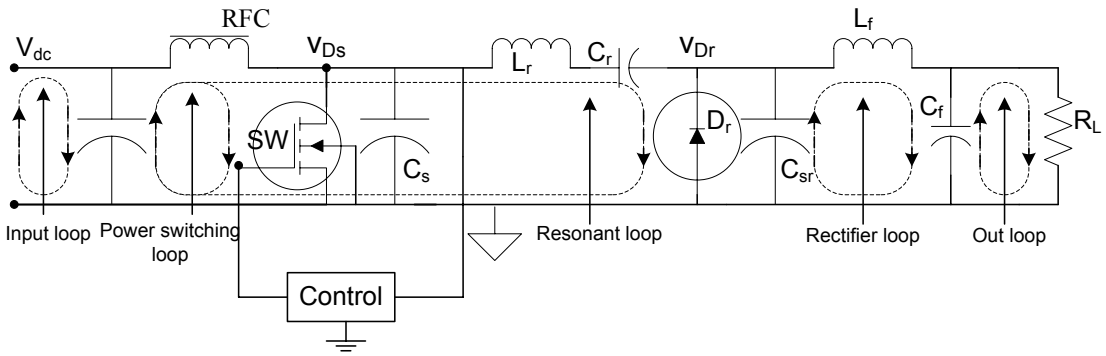


Fig. A 4 Major current loops in the switching RF DC-DC power converter.

Five loops are listed in the figure above. They are:

1. Power switching loop.
2. Resonant loop.
3. Rectifier loop.
4. Input source loop.
5. Output load loop.

The current flows in both input and output loops are composed of DC elements with some AC ripple current. These AC components are the elements that generate conducted EMI. The input and output loops do not result in problems most of the time

because the AC pulses are filtered by the input filter and output filter capacitors respectively. This means that the high frequency noise problems created by these two loops are less than the other three AC loops. The output voltage ripple is caused by the charging and discharging of the output capacitors. Therefore it is helpful to minimize the effect of ESR and ESL by making the traces between the filter capacitor and the load as short and wide as possible. An adequate capacitor value, in parallel with power source, is required at the input terminal. Besides, to prevent the spike voltage from feeding back to the power line, some isolated installation is desirable, for example, a small inductor.

On the other hand, the power switching loop, resonant loop and rectifier loop are entirely AC. They have high peak currents and very sharp edges (di/dt). Simultaneously, there are high rates of dv/dt occurring within these loops. As a result these loops are very noisy and deserve extraordinary attention. These loops should be laid out to have very small circumferences and be implemented with short, wide traces. Smaller circumference dictates less efficient antenna, reducing the radiated RF energy. The inductance and resistance exhibited by a trace is inversely proportional to its width. Wider trace not only causes lower voltage drop around the loop, thus less RF radiation, but also provides better heatsinking for the power devices. So the loop traces should be as wide as possible.

For the layout considerations, care must be taken to make sure the components that make up each of the three loops close to each other. In this way the dynamic high currents remain in the converter's power section. Therefore C_{in}, RFC and SW (Fig. A 4) should be close to each other. Also C_{in}, L_r, C_r and D_r should be close. By using short, wide traces, the tight layout can be achieved to reduce radiation, improve efficiency, reduce ringing and prevent interference to quieter parts of the circuit.

The stray capacitance at the nodes where voltage changes quickly should be minimized. The size of such nodes should be kept small by using wide, short traces. At the same time, EMI emanated from those nodes is reduced. The nodes V_{DS} and V_{Dr} in Fig. A 4 are identified as nodes where voltage quickly changes. The stray inductance in the circuit branches with quickly changing current also should be minimized. The inductance

in series with SW and D_r can indeed cause a problem because current through them changes abruptly. These series inductance include stray inductance from leads as well as inductance in the ground return path. Note the current through the resonant tank $L_r - C_r$ undergoes quick change due to very high switching frequency. Thus the stray inductance of these branches must be minimized.

The ground serves as a common point of the reference for the circuit, which is a very important function. Therefore, to place the ground carefully is crucial since improper grounding layout will cause instability in the circuitry. Usually there are two types of grounds existing within the switching power converter: high current loop power ground and low level control ground. The control ground should be isolated from the noisy power ground. Two separate ground paths can be routed. The power ground should be made with short and wide traces to minimize the inductance and resistance. Connecting the two grounds at one point ensures that no noisy current circulates within the control ground. The connection between these two grounds can be relatively narrow, as virtually no currents flows via that path.

A large ground plane can be placed on PCB back side and around high current traces to reduce EMI. The ground plane acts as a shield to prevent some RF energy from radiating to the environment [85]. These large conductor areas traps radiated EMI and dissipate them within eddy current created by RF energy. Furthermore, the ground plane on the back gains thermal characteristics to keep the PCB at a lower temperature (comparing to no planes).

According to the characteristics of RF power converter, the key points on designing PCB layout are summarized in the following:

1. Power ground is separated from control ground, but connected at a point.

2. Noisy loops (power switching loop, resonant loop, rectifier loop) should be kept tight to reduce ringing and radiation.

3. Minimize stray capacitances at nodes V_{DS} and V_{Dr} with high dv/dt.

4. Minimize stray inductance, especially branches SW , D_r and resonant tank.

Based on these principles, the practical PCB layout of the RF DC-DC converter is shown in Fig. A 5.

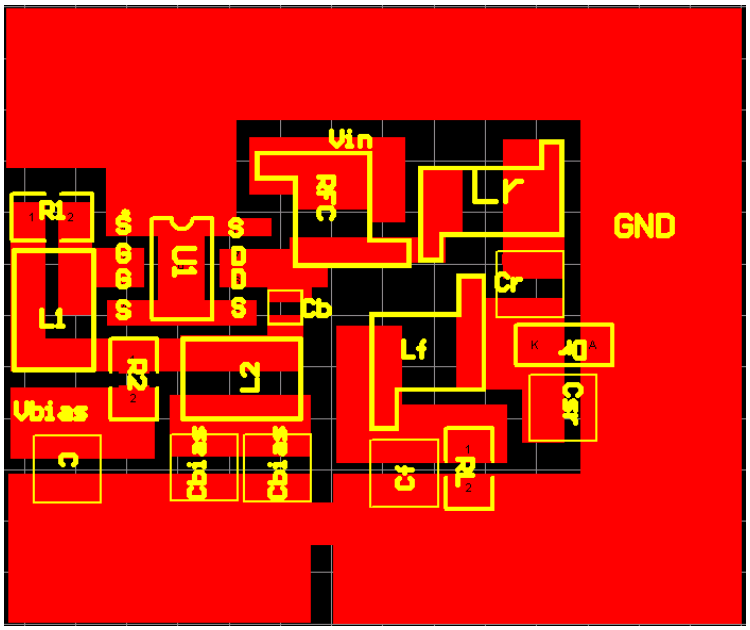


Fig. A 5 Practical layout of RF DC-DC power converter.

In order to evaluate the layout design and estimate the parasitic effects on the circuit, it is necessary to determine the parasitics of the circuit layout. In the following section the extraction of the layout parasitic is described.

Software Maxwell Q3D Extractor is chosen as the tool to calculate the parasitic elements. Maxwell Q3D Extractor is interactive software package that can be used to electrically characterize 3D interconnect structures such as those found in connectors, Printed Circuit Boards (PCBs) [86]. This software can be used to solve for the circuit parameters such as capacitance matrices, partial inductance and resistance matrices based on the theory of partial element equivalent circuit (PECC) [87]. Lots of successful applications of Q3D Extractor in parasitic extraction can be found in some literatures [88][89][90][91].

The process for extracting the parasitic matrices is summarized below. In order to setup the 3D geometrical model in Q3D Extractor, firstly the practical 2D PCB layout generated is saved as an Autocad file. Then this 2D profile can be converted into 3D structure based on the information of practical geometry in Autocad and saved as ACIS file *.sat. The ACIS file is exported into the Q3D Extractor as a 3D model which has the same dimensions as the practical ones. After specifying material properties for each object, identifying the conductors, specifying source excitations and setting up the solution settings, all the necessary parasitic parameters in the circuit can be generated. Only the important circuit board parasitics are listed in Table A. 2 (refer to Fig. A 6). The results show small parasitic capacitances and inductances of the layout which have negligible effects on the performance of the circuit.

Table A. 2 Key parasitics in the circuit board.

	DS	Dr	Gate
Parasitic cap (refer to GND)	0.069 pF	0.057 pF	0.047 pF
Parasitic inductance	0.17 nH	0.04 nH	0.014 nH

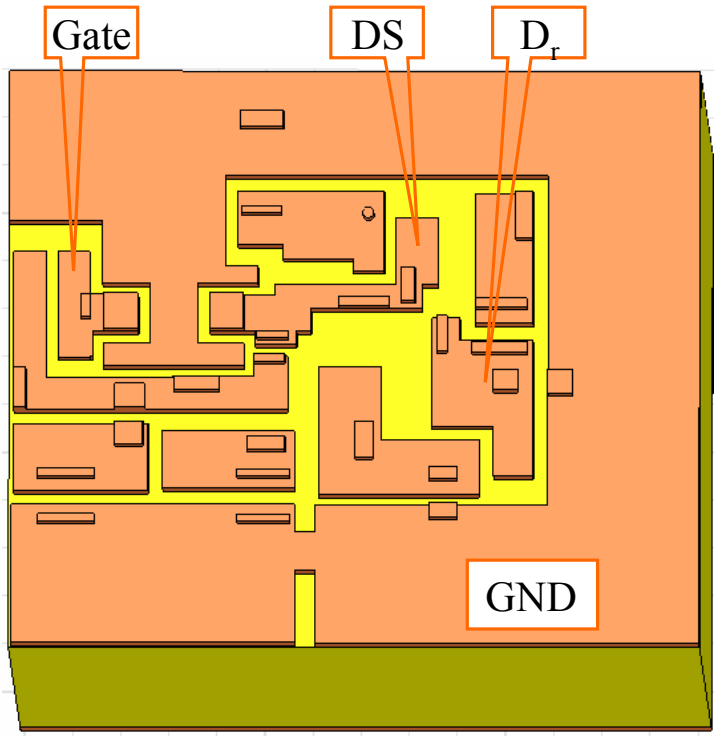


Fig. A 6 Model of 3D circuit layout in Q3D.

Appendix II Voltage measurement probe

TDS5104 digital oscilloscope manufactured by Tektronix® is chosen as a measurement platform to measure the waveform in the RF DC-DC converter (refer to Fig. 3.30). The key features of the oscilloscope include up to 1 GHz bandwidth and 5 GS/s real time sampling rate. The input impedance of the channel is 1 MΩ ± 1% in parallel with 18 pF ± 2 pF or 50 Ω ± 2.5%.

The commercially available probe - the high impedance passive probe P5050 10×, 500 MHz is often used to measure the voltage waveform. It is necessary to look at the frequency characteristics of this probe when it is used for high frequency measurement. This typical 10× probe uses an RC network at the probe tip to form a 10:1 voltage divider with the scope input impedance and the cable capacitance. The RC probe tip network is approximately a 10 MΩ resistor in parallel with a 11.1 pF capacitor. The probe cable has a characteristic impedance made as high as possible with a typical value being 170 Ω. Since the probe is not terminated in its characteristic impedance at the scope, there will be some reflections at higher frequencies and the resultant ringing and spurious response. Another problem with this probe is that the input capacitance of 11.1 pF becomes fairly low impedance at frequencies above 50 MHz. At 50 MHz, 11.1 pF has a capacitive reactance of about 300 Ω. The frequency characteristics of the input impedance of probe 5050 is shown in Fig. A 7 [129], which clearly shows that the probe is not suitable for voltage waveform measurement in the 250 MHz DC-DC power converter.

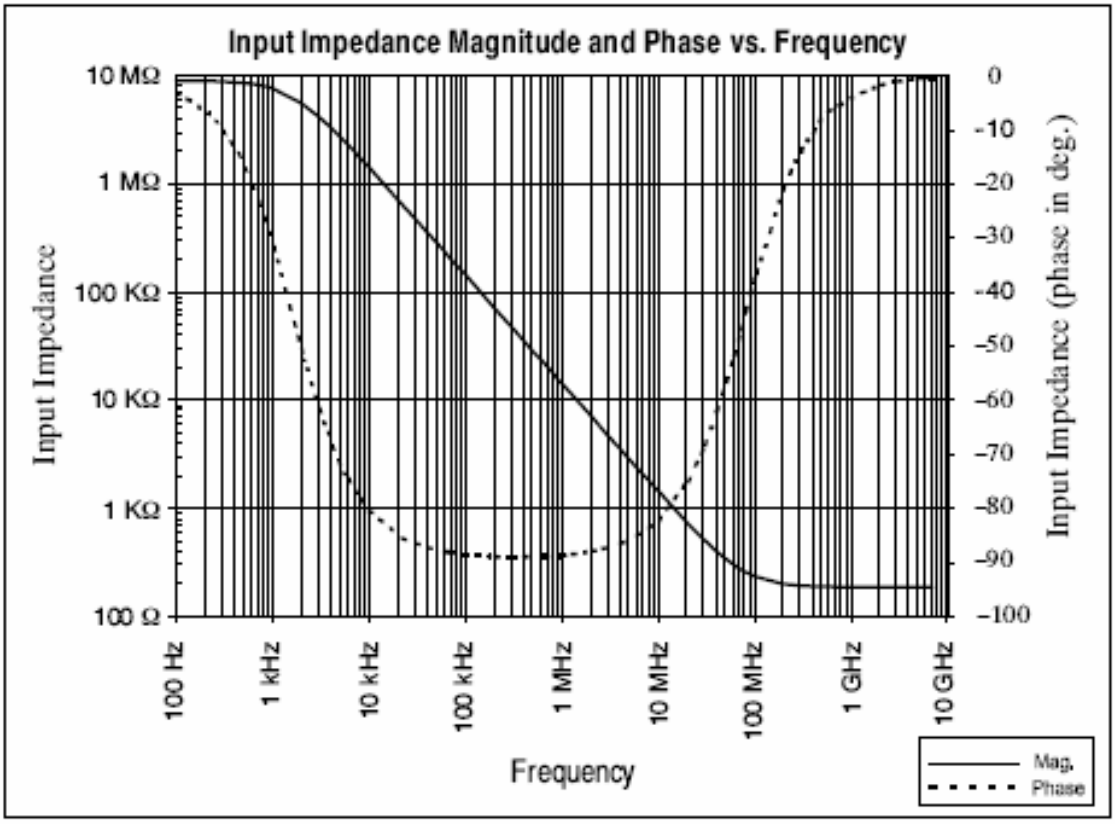


Fig. A 7 Frequency response of input impedance of probe 5050.

Since the input impedance of the scope TDS5104 can also be selected at 50 Ohm, a coaxial cable having 50 Ohm characteristic impedance is chosen to construct a probe. The cable is terminated at the scope end, so the input impedance looking into the input end of the cable is 50 Ohm over a wide range of frequencies. A resistor R_{in} is added in series with the cable to form a voltage divider and set higher input impedance (as shown in Fig. A 8).

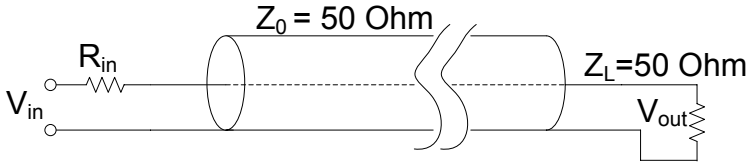


Fig. A 8 Probe made by coaxial cable.

The input impedance is now $R_{in} + Z_0$ and the divider ratio is given by $\frac{V_{out}}{V_{in}} = \frac{Z_0}{R_{in} + Z_0}$. If a 10:1 probe is needed R_{in} must be 450 Ohm and input impedance is

500 Ohm. It should be noted that the parasitic capacitance C_{in} of R_{in} should be minimized. If assuming C_{in} in parallel with R_{in}, there exists a corner frequency $\frac{1}{2\pi R_{in} C_{in}}$ below which the probe behaves like a voltage divider composed of Z_0 and R_{in}. Above the corner frequency, the divider ratio approaches unity. So a high quality resistor R_{in} is necessary. For typical resistor designs, this corner frequency ranges between 300 to 500 MHz for a 450 Ohm resistor. If there is a mismatch between the cable characteristic impedance and the scope, a reflection is generated which travels back on the cable. The probe tip resistor 450 Ohm is also not a match for the cable. So in order to mitigate the resultant reflections at the probe tip, a 50 Ohm resistor can be connected between the center conductor and the shield of the coaxial cable as shown in Fig. A 9. The input impedance looking into the cable is now 25 Ohm. So the probe has a divider ratio of 20:1 probe if R_{in}=475 Ohm. The input resistance of the probe is still 500 Ohm. In fact 500 Ohm input impedance of this probe is resistive over a wide frequency range and greater than that of probe 5050 above 50 MHz [130].

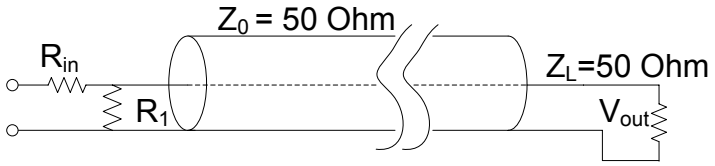


Fig. A 9 Improve probe made by coaxial cable.

This kind of passive probe is well suitable for low impedance circuits. The input impedance should be much higher than the impedances encountered in these circuits. If it is not the case, the circuit would not likely function in the first place. In this case, high performance commercial probes such as active probes (e.g. P6202) should be resorted to at the expense of high cost.

Appendix III Design of the proposed calorimeter

Based on the thermal model analysis of the calorimeter in 5.4.2, it is essential to minimize the heat leakage through the two covers. Aside from the heaters necessary for controlling the temperature of the outer cover, other design considerations are also required to achieve this goal. These considerations include:

- to provide a high degree of thermal insulation
- to minimize heat flow escaping from the system to the surrounding
- low thermal resistance path from the DUT to the TE module
- control circuits for TE module to direct heat flow and keep operating temperature close to the practical case
- control circuits for heaters on the outer cover
- minimizing the thermal expansion stress between different materials
- various temperature measurements for control and monitoring
- flexibility and ease of operation.

The surface temperatures are measured with K type thermocouples. Monolithic thermocouple amplifiers with cold junction compensators IC AD595 (Fig. A 10) amplifies the output voltages of the thermocouples. These thermocouples should be evenly and reliably mounted on the surfaces. One thermocouple is installed on every outer surface of the inner cover and outer cover. On the top surface of the base plate I, four evenly distributed thermocouples are mounted. Four thermocouples are also installed on the surface of base plate II for the purpose of controlling TE module. The controllers for heaters and TE modules are shown below in Fig. A 11 and Fig. A 12, respectively.

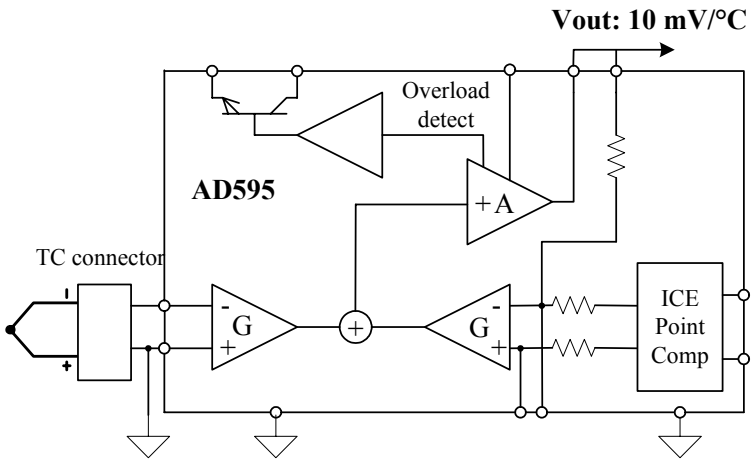
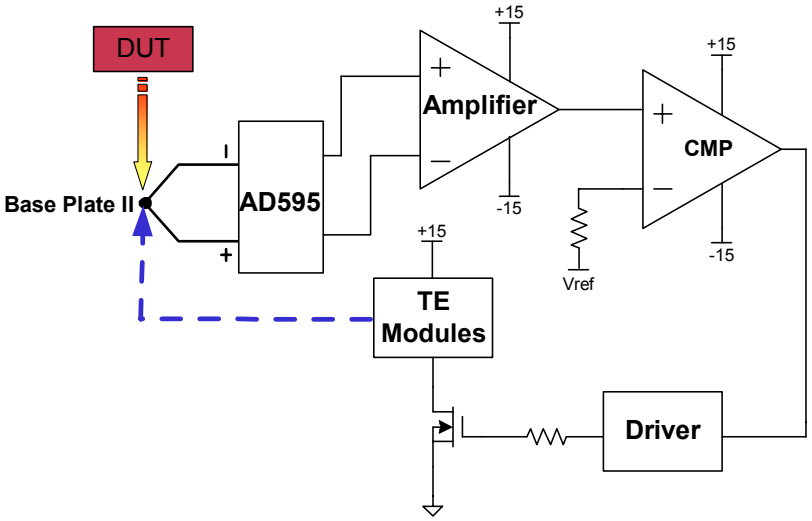
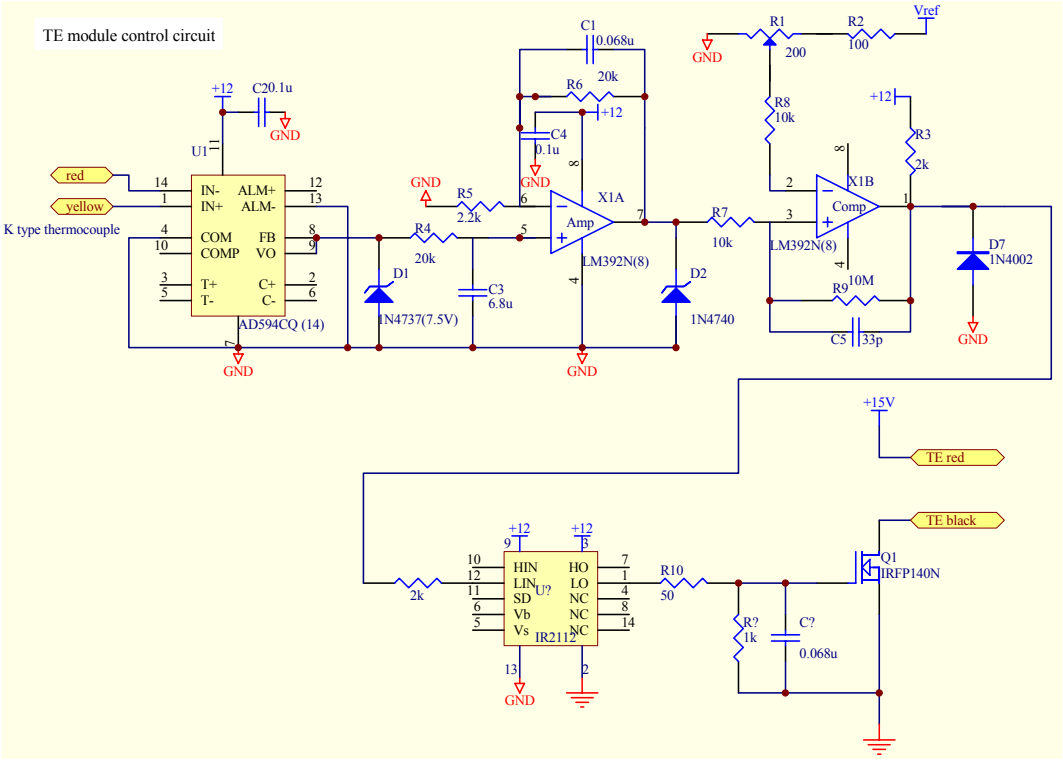


Fig. A 10 Functional block diagram of AD595.

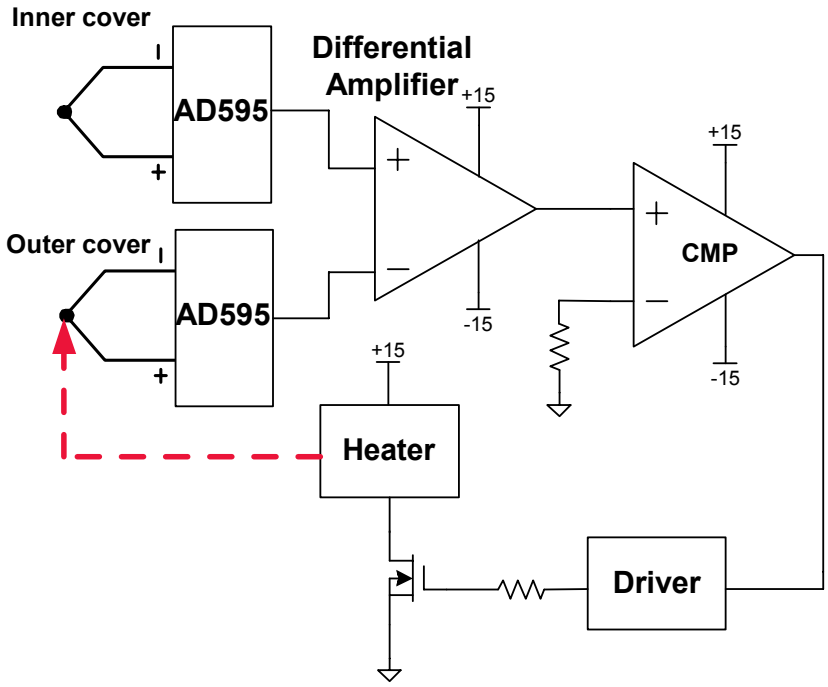


(a) Functional block diagram.

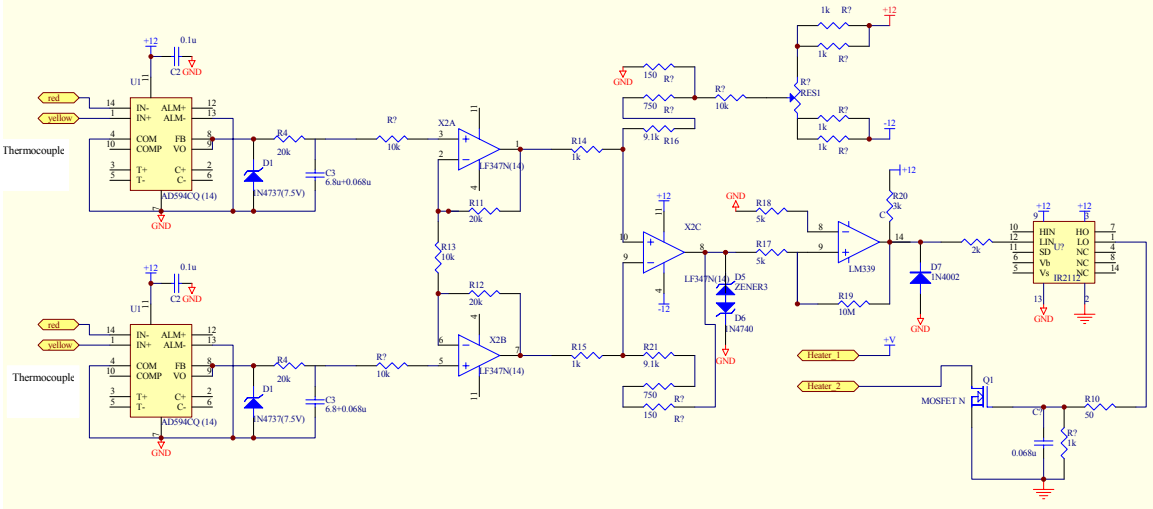


(b) Circuit schematic.

Fig. A 11 Controller for TE modules.



(a) Block diagram.



(b) Circuit schematic.

Fig. A 12 Temperature difference controller for the two covers.

The proposed calorimeter is in the form of two concentric boxes. The internal box is the test chamber and should be in good contact with the base plate I. Internal surfaces of the inner cover and outer cover are highly polished to reduce the radiation heat leakage. A fiberglass material with a thermal conductivity of 0.033 W/m·K fills the space between the two covers, which can effectively prevents the heat from escaping. The external surfaces of the outer cover are coated with an additional layer of fiberglass to ensure more uniform temperature distribution across the whole outer cover. Fig. A 13 shows a schematic diagram of the apparatus.

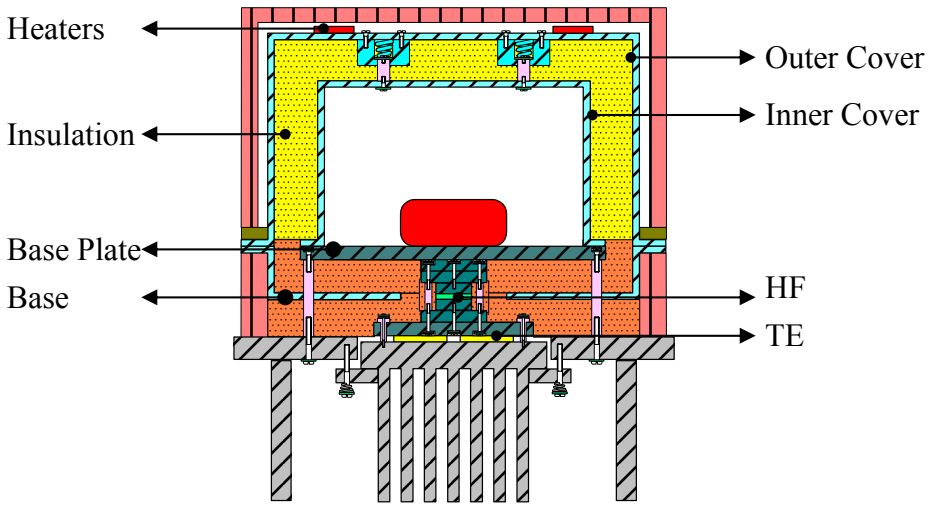


Fig. A 13 Mechanical schematic of the calorimeter.

Two power resistor heaters are uniformly distributed on each of the external surfaces of the outer covers. The mounting surfaces of the heaters were coated with thermally conductive grease and then bolted to the cover. Four spring-loaded connectors are arranged in a symmetrical pattern between the two covers so as to provide uniform pressure when the two covers rest on the base plate and base cover (as shown in Fig. A 14). The maximum load of each spring in the design is 23.7 lb. Aside from the stainless steel screws and the Zinc-plated springs, other parts of the connector are good thermal insulators for minimizing the heat loss through the connector. With this design the inner cover and outer cover are mechanically connected, and easily removable. The pressure caused by the spring compression helps to increase the contact between inner cover and base plate I.

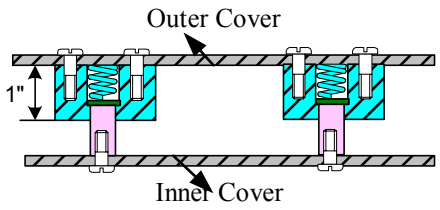


Fig. A 14 Spring connection between two covers.

In order to ensure a low thermal resistance path from DUT downward to TE module, aluminum is used as the heat plates. All the aluminum plates were therefore machined flat. Since the coefficients of thermal expansion (CTE) of the aluminum plates, heat flux sensor and TE modules are different, the heat sink and the aluminum plate just above the TE module were bolted together using the spring-loaded stainless steel screws to effectively minimize the thermally induced mechanical stress induced by mismatched CTE's. This construction was repeated for the heat sink and base frame together (Fig. A 15).

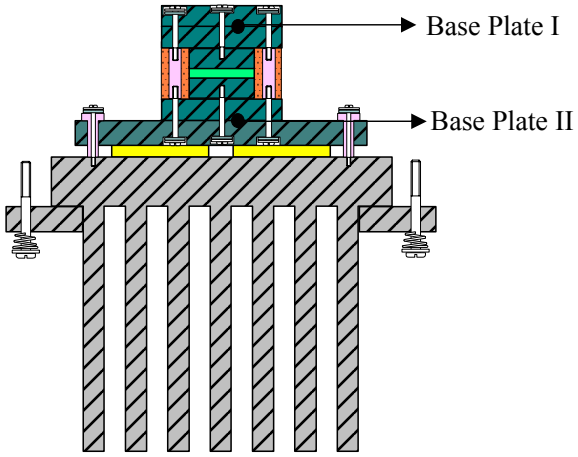


Fig. A 15 Illustration of reducing thermal stress.

A soft layer of silicone gasket between the inner cover and base plate seals it air tight. Any power leads and signal wires necessary for the operation of the DUT can be connected via four airtight feed-through connectors on the base plate I. The supporting legs of the calorimeter should have good mechanical strength and thermal insulation. Adjustable draw latches are installed to clamp the upper part and the lower base part together.

Appendix IV Fabrication processing of the integrated inductor

In order to obtain the practical integrated inductor as described in design process of 4.5, the fabrication processes below are required to follow.

1. Rounding the 12 sharp edges of the ferrite core by sander machine.

2. Cleaning: cleaning is always critical to the success of fabrication. Clean the ferrite core by Actone at first, then alcohol; finally rinse the ferrite core with DI water, and dry it.

3. Coating the ferrite core with the solder mask as insulation layer between the ferrite core and windings. The solder mask is the combination of one part ENTHONE® DSR-3241 B and four part ENTHONE® DSR-3241 A. After the coating of each side, place the sample on the hot plate for 20 minutes at 80 °C.

4. Baking the ferrite core coated with the solder mask inside the heat oven to harden the solder mask in preparation for the sputtering. The baking process is illustrated in Fig. A 16. The sample after this process step is shown in Fig. A 17.

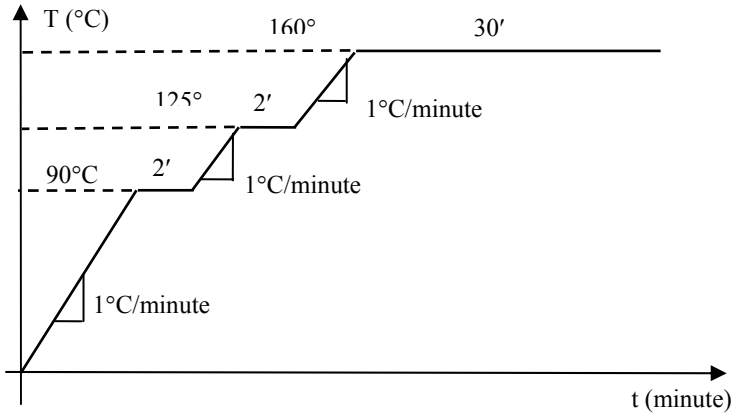


Fig. A 16 Baking process for hardening the solder mask.

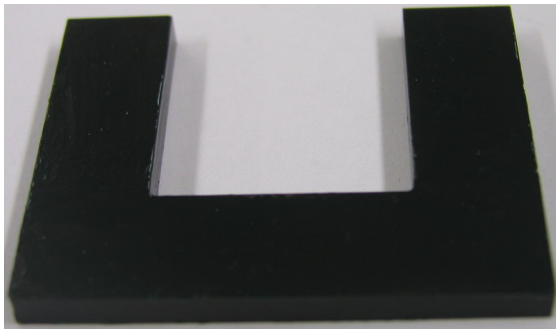


Fig. A 17 Sample after solder mask.

5. Sputtering the sample.

It is better to clean the surfaces of the ferrite core after the step above before sputtering. The two sides of the sample are required to be sputtered. Before the sputtering of copper layers, Ti layer is firstly sputtered to each side of the sample. Ti sputtering process lasts for about 15 minutes. After sputtering Ti on each side, then sputter Cu on both sides of the sample. Cu sputtering process lasts for 15 minutes plus another 15 minutes, i.e., totally 30 minutes. The sputtering step is a long process for about 12 hours because of 2~3 hours pumping time at the beginning of each sputtering. The sample after Cu sputtering is shown in Fig. A 18. The empirical relationship between the sputtering time and the thickness is listed in Table A. 3.

Table A. 3 Relationship between sputtering time and thickness.

	30 minutes
Ti	50 – 60 nm
Cu	500 – 600 nm

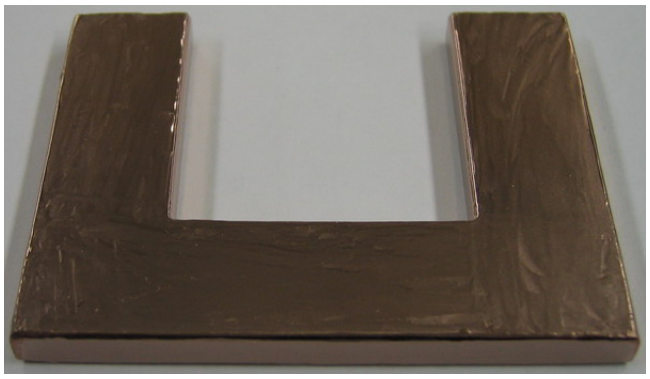


Fig. A 18 Sample after Cu sputtering.

6. Cu Electroplating of the sputtered sample.

The Cu electroplating process is to increase the thickness of the designed metallization layer. The normal plating current density is 20 mA/cm^2 and 25 μm thickness is achieved under this current density after one hour. The current is set at 1.1 A according to the total surface area of the sample. The plating lasts 2 hours to obtain 50 μm thickness of Cu layer.

Fig. A 19 shows the picture of the samples after electroplating.

Fig. A 19 Samples after electroplating.

7. Etching: The Kapton in width of 6.5 mm is wrapped around the ferrite core to develop the winding pattern of the inductor, as shown in Fig. A 20. Then put the sample in the developer as shown in Fig. A 21 to remove the unnecessary copper. This etching process lasts about 10 minutes. After washing with water, put the sample into the Ti etching solution (1 Ti etchant TFT: 20 DI water) for about 5 minutes to remove Ti layer.

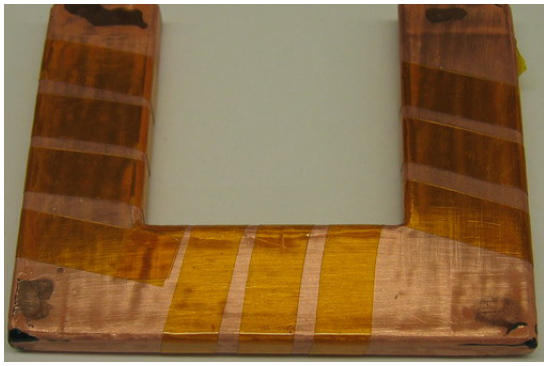


Fig. A 20 Winding Pattern of the inductor.

Fig. A 21 Developer machine for removing copper.

Now the sample is ready for making inductor.

Vita

The author, Chucheng Xiao, received his B.S. and M.S. degree from Huazhong University of Science and Technology, Wuhan, China in 1995 and 1998, respectively. From July 1998 to June 2001, he worked as an engineer in the Power Electronics Institute of Dongfang Electronics Co., China. Since August 2001, he has been working towards his Ph. D degree at Center for Power Electronics Systems (CPES), Virginia Polytechnic Institute and State University. His research interests include high frequency high power density DC-DC power converters, thermal management and measurement of power electronic systems, integrated current sensing techniques and integration of passive components.