DESIGN CONSIDERATIONS OF A THIRTY-KILOWATT, THIRTY-KILOHERTZ, FULL-BRIDGE INVERTER FOR APPLICATION IN A VERY-LOW-FREQUENCY COMMUNICATIONS SYSTEM

by

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This author wishes to thank those closest to him for their patience and friendship. People who take me as I am, accepting my faults which are many with my assets which are fewer in number. Perhaps my best quality is my extreme loyalty to those people. For now and forever I am at your service.

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CHAPTER ONE

INTRODUCTION

1.1 Thesis Statement

This thesis presents the design and development of a state-of-the-art, thirty-kilowatt, thirty-kilohertz, full-bridge, static inverter module. Bipolar junction transistors are utilized as the power switches within the inverter unit. Sixteen modules may be combined via vector summation to provide a sinusoid synthesis technique applicable to a one-half-megawatt, very-low-frequency transmitter for a submarine communications system.

1.2 Very-Low-Frequency Communications

The United States Navy presently operates communications transmitters. These transmitters operate in the 15 to 30 kilohertz frequency range at power levels up to 2 megawatts. The communications stations, which are to a large extent technologically outdated, suffer from high energy costs. In addition, the stations are difficult and costly to maintain. The cited drawbacks have provided an incentive for the U.S. Navy to explore current switching power conversion technology as an avenue toward more compact, more efficient, less costly communications transmitters. [2]

Very-Low-Frequency communications typically involve the use of Frequency-Shift-Keying. FSK is a form of pulse-coded modulation where the instantaneous output frequency

of the FM system is switched between two or more values [7]. Such systems operate into a very high Q antenna which presents a reactive load to the transmitter. Reactive phase angles of twenty degrees or more are not uncommon [3].

At the heart of a transmitter such as that discussed in the previous paragraphs is the power amplifier. For this particular project, a voltage-fed bridge inverter, operating in the clamped mode, forms the individual building block for the power amplifier. Sixteen modules collectively comprise the power amplifier with each module converting a DC input voltage to an AC quasi-square wave output voltage.

A time sequence of quasi-square waves is summed and converted into a single stepped sinusoidal waveform by connecting the secondaries of eight inverter bridge modules' output transformers in series. The concept of vector summation is then used to combine two such outputs with a relative phase angle between the two waveforms. The resultant amplitude of the vectorially summed sinusoid is a product of the two input waveforms and their phase angle difference. Vector summation is an attractive candidate for the required task as high efficiency, low distortion, and improved fault tolerance result during the process of converting the DC input power to AC output power [2].

1.3 Historical Background of Power Inversion Techniques

Historically, the conversion of a DC power input to an AC power output was performed by conversion of electrical energy into mechanical energy and then back to electrical energy. A motor-generator set could be used as an example of this early conversion process. Such methods of power inversion were, at best, costly, cumbersome and inefficient.

Starting with the introduction of high power Silicon Controlled Rectifiers (SCRs), static inverters were developed. Until recently, static high power processing had largely been the domain of thyristors (SCRs). Thyristors were utilized because of their durability and high power ratings. Such devices do, however, have disadvantages. While they can easily be gated "on" to the conduction state, a commutation network is generally required at turn off to interrupt the current flow through the switch. Exact requirements of reapplied voltage or dv/dt must be adhered to in order to insure satisfactory turn off. The additional circuitry increases the size, complexity, cost, and power loss of the resulting power conversion unit. Power converters containing thyristors as the switching components are generally limited to low frequency operation (less than 5 kilohertz) due to the device's slow switching speed and requirement for some means of commutation [5].

Recently developed ultra-high-power bipolar junction transistors have replaced thyristors in several high-power (less than 1000V, 500A) high-frequency chopper and inverter applications. The incentive for conversion to power BJTs has been the great progress made in the knowledge of and manufacture of these components. The new devices have shown improvements in the areas of characteristics, such as voltage and current ratings, yields, and durability. In conjunction with these improvements there has been a reduction in parameter spreads. The technology has lead to the emergence of new products to rival and compete with other types of fast reliable power switches presently available to the designer [6]. While the new transistor power devices cannot be obtained with the same voltage and current ratings as their previous counterparts, (thyristors with voltage ratings of 3500 Volts or current ratings of 2000 Amperes are available) the inherent simplicity of their use has made transistors an economical and popular alternative to SCRs. There are two immediately foreseeable advantages to the use of BJTs. First, the circuit complexity and topology may be reduced because there is no need for complex commutating networks which, in turn, makes the power bipolar transistor relatively easy to turn off. Second, the frequency of operation can be expanded from

the one to two kilohertz region to the range of fifty kilohertz for additional reductions in the size, weight, and cost of circuit components, especially the magnetics [1].

Power transistors do offer exciting performance advantages over Silicon Controlled Rectifiers. Most notably they are capable of higher switching speed which is a necessary requirement for a thirty-kilohertz inverter project. A power transistor is not, however, as rugged a switch as a thyristor. The load line shaping must be performed carefully to reduce voltage and current stresses during switching and hence to improve switch reliability. In fact, optimization of switching characteristics is a central issue to the proper design of the inverter module [6].

Two more critical issues which must be addressed in the consideration of design trade offs are the careful design of the base drive and protection against overloads such as might occur during a shoot-through or short circuit condition. These two factors and the previous switching characteristics will be discussed in depth in the following chapters.

1.4 The Focus of Past and Present Research

Some of the previous work on high-power, high-frequency, full-bridge inverters has occurred at Virginia

Tech. Initially, work by C. Peng, Dr. F. C. Lee, and Dr. D. Y. Chen led to the development of a base drive circuit and prototype thirty-kilohertz, three-kilowatt inverter module under contract with Batelle Columbus Laboratories. The primary goals of the investigation were "to design and construct base drive circuits for a full-bridge transistor power inverter circuit and to determine a necessary snubber circuit (stress limiting circuit) for the power transistors of the inverter." [8] Presently, work is being performed on a full-bridge transistor power inverter capable of the same operating frequency at ten times the previous power level or thirty kilowatts. The base drive circuit is radically different from the previously constructed module. While the new inverter module uses a conventional polarized snubber arrangement, additional care and caution are required to protect the devices within the bridge from stress related failures at the more extensive power levels of thirty kilowatts.

Westinghouse Electric Corporation has also developed high-power inverters. [3] Indeed Westinghouse has a full bridge inverter for VLF use in the 27-60 kilohertz frequency range with an output power of twenty-five kilowatts. The devices (Westinghouse D7ST) used in Westinghouse's full-bridge inverter are identical to the power devices

used in the present inverter module. The present project at Virginia Tech differs in that here a bridge inverter is developed that operates in the clamped mode. The clamped mode, which shall be explained shortly, offers the advantage of sourcing the load continuously from a low impedance.

Additionally, the bridge inverter constructed here uses a Darlington configuration for the individual switch elements. This configuration offers superior gain over single device architectures and allows the use of a lower power base drive circuit.

1.5 Inverters, Definition and Theory

It would be unwise to progress further without some definition and theory relating to the operation of single phase inverters in general. While it is assumed the reader has some knowledge of rudimentary inverter design, a review of pertinent topics is included. The following discussion relates to figures 1.5.1 and 1.5.2. A full-bridge inverter (Fig. 1.5.2) is more complex than its push-pull or parallel inverter counterpart (Fig. 1.5.1). The bridge inverter contains two times the number of switches as the parallel structure. Each device in the bridge is only required to block slightly over the supply voltage because of the arrangement of the transistorized switches. Second, since a center tapped transformer is

not used in the bridge inverter configuration; it has a simpler transformer requirement. By comparison in the parallel arrangement the bipolar junction transistor which is off must sustain the supply voltage as well as an equivalent induced voltage in half of the primary of the center tapped output transformer. For this inverter project two times the supply voltage of three-hundred volts plus a safety margin of fifty volts would have required a transistor with a sustaining voltage of six-hundred and fifty volts so that the parallel inverter configuration was not a viable alternative.

The disadvantages of the full-bridge inverter are not trivial. First, the upper two transistors require isolated base drives to function properly. Second, any asymmetry in the conduction interval of one diagonal pair of devices as opposed to the other pair may cause saturation of the output transformer. Third, the switching aid networks in the bridge or totem pole configuration often incite undesirable interactions; consequently these networks require more attention in design and analysis than the network required by a single device [9]. Finally, the parallel structure utilizes half as many transistors to perform a power processing task identical to that of a bridge inverter.

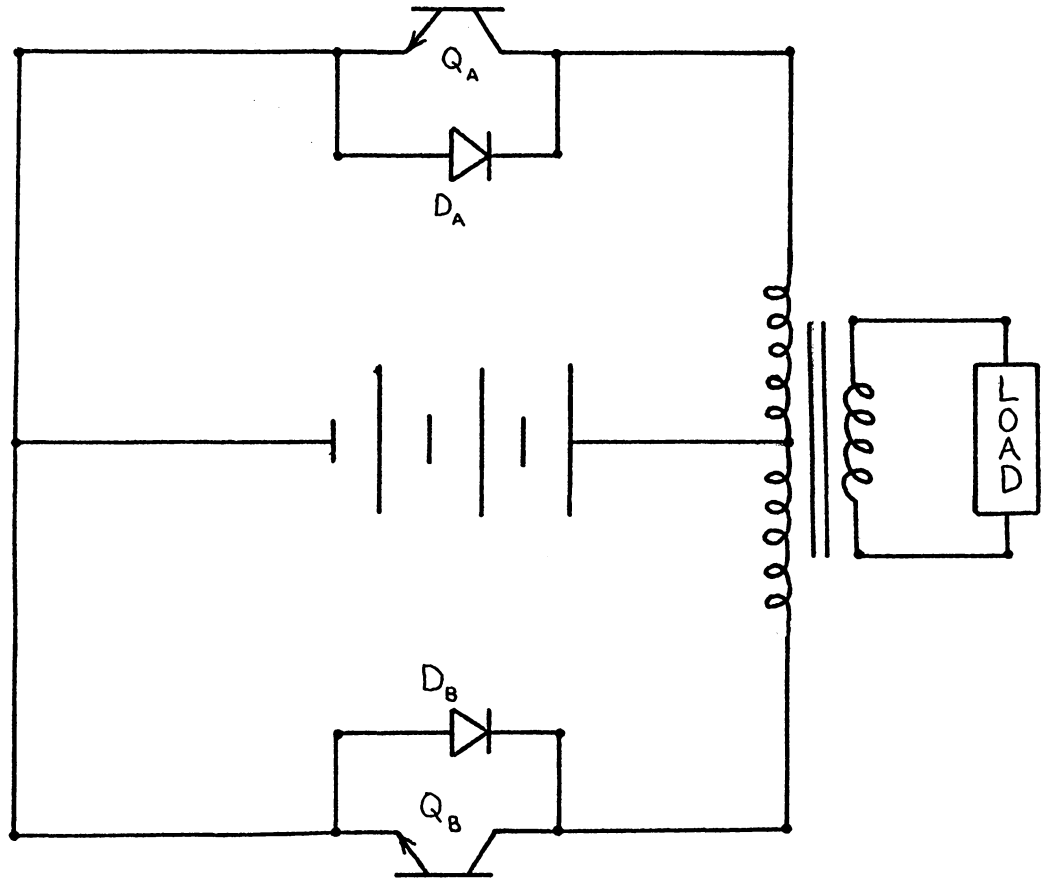


Figure 1.5.1 Parallel or Push-Pull Type Inverter Structure

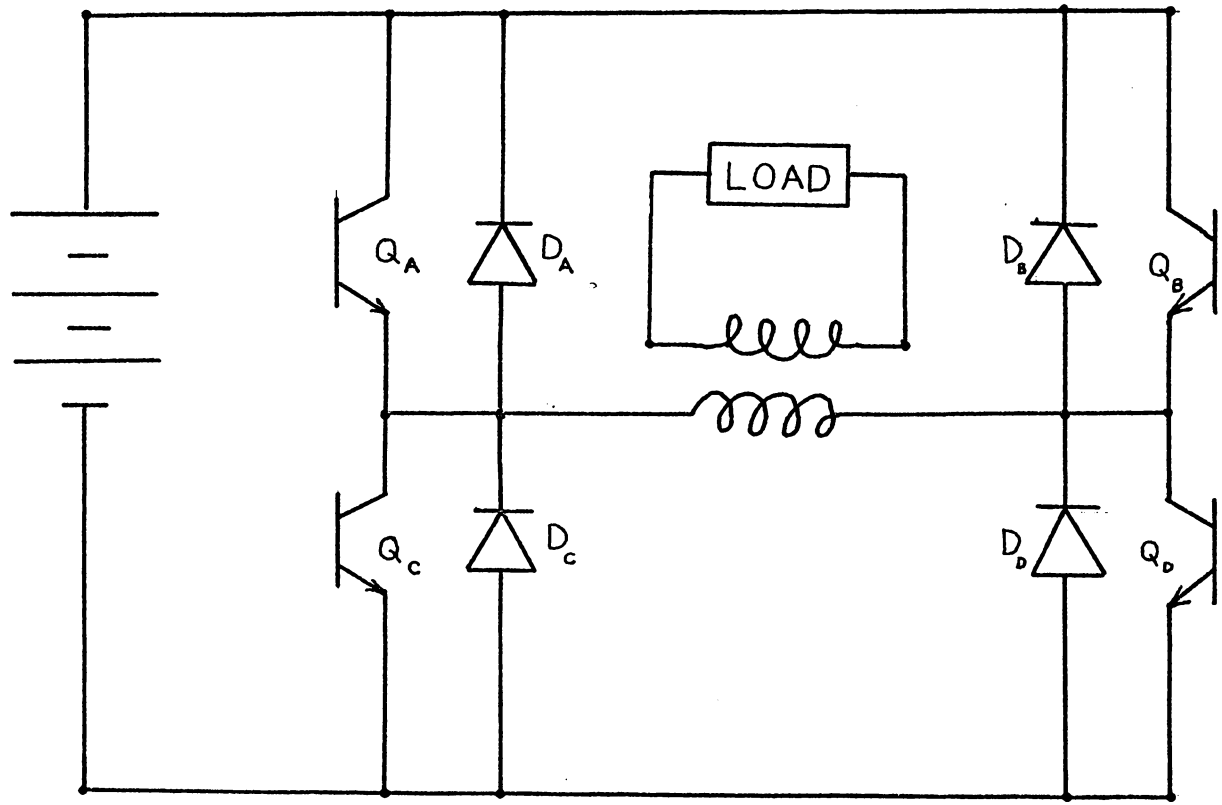


Figure 1.5.2 Full Bridge Inverter Structure

In Fig. 1.5.2 the bridge inverter is shown along with Fig. 1.5.3a and 1.5.3b which are timing diagrams for the switches in the bridge. The first timing diagram operates the switches of the bridge in the "straight inverter" mode. The conduction intervals of Q_A and Q_D are identical, ignoring storage time effects as are the conduction intervals of Q_B and Q_C. The output voltage waveform for straight inverter operation is shown below the timing diagram 1.5.3a.

To operate the bridge in the clamped mode the diagonal pair drive waveforms (Q_A,Q_D) and (Q_B,Q_C) are offset. Essentially, transistor Q_A turns on and off earlier than transistor Q_D. During the portion of conduction overlap of transistors Q_A and Q_D the secondary voltage of the output transformer is positive. It remains positive after the drive waveform has been removed from switch Q_A until all the stored charge is removed from the device. At this point any leakage or stray inductance in the primary or a reactive load will cause current to continue to flow (due to energy storage) through the transformer primary. The output transformer primary is shorted by transistor Q_D and the anti-parallel diode D_C. After the bipolar junction transistor Q_A has been off sufficiently long to ensure that storage time

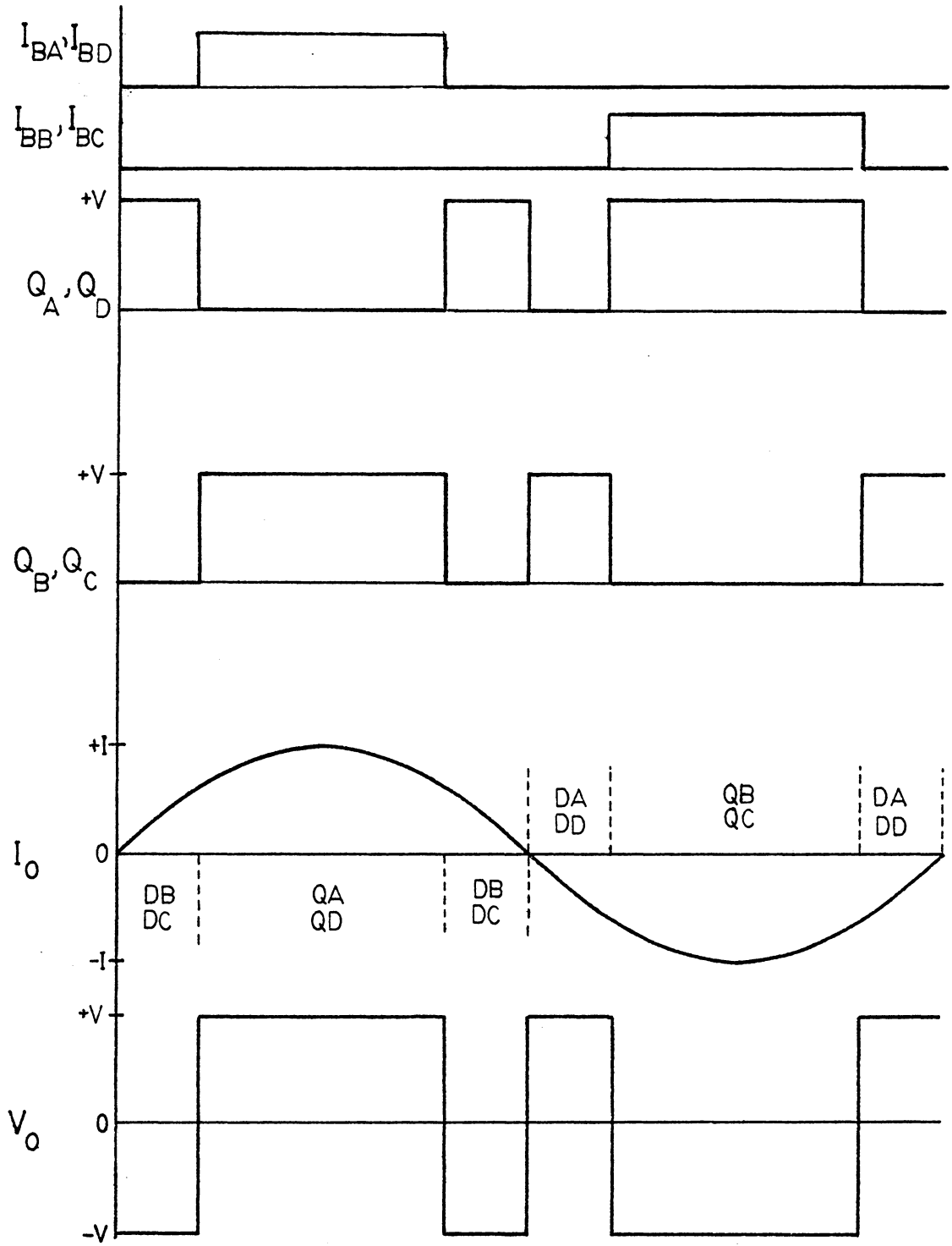


Figure 1.5.3a Full Bridge Inverter Waveforms Straight Inverter Mode Operation

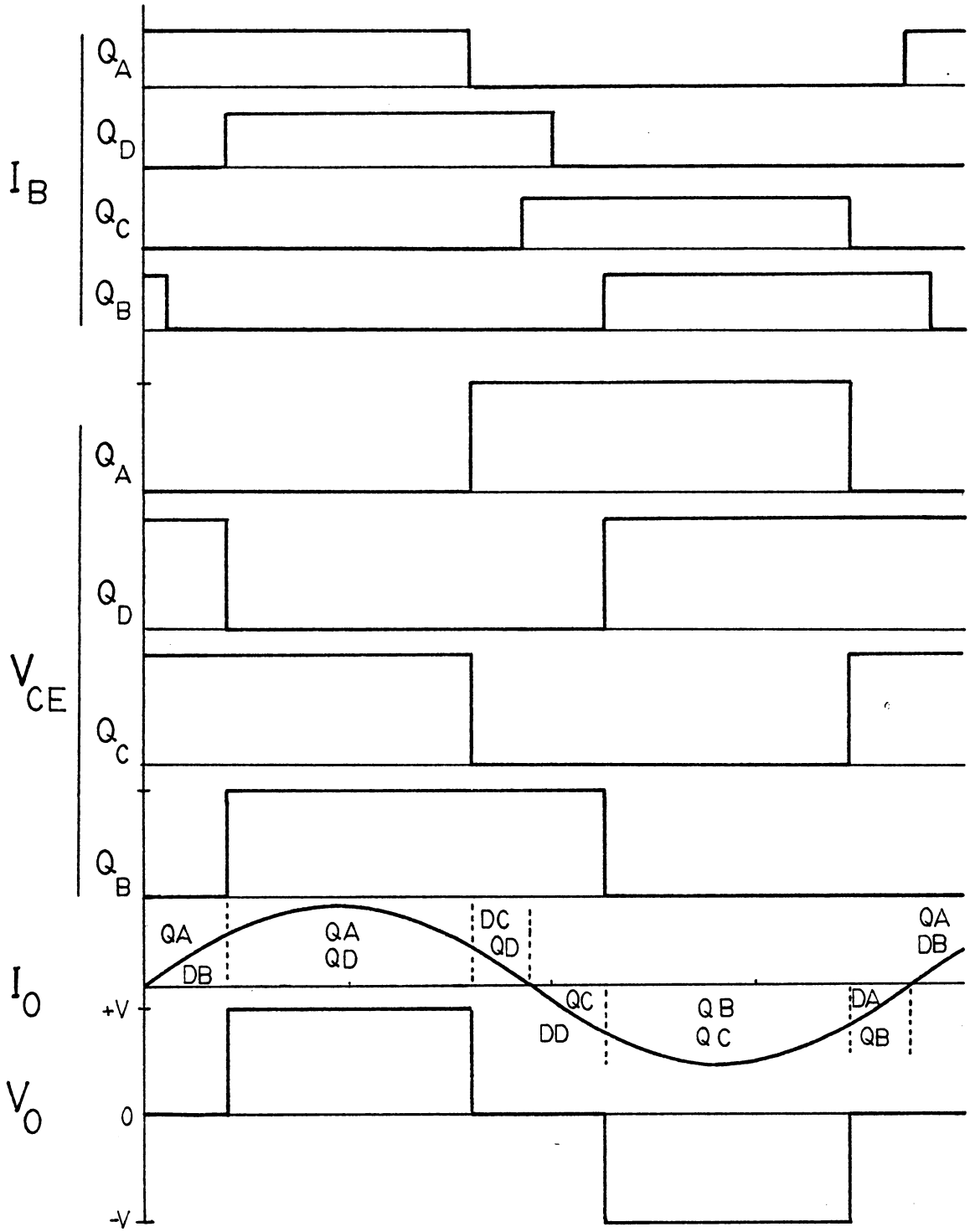


Figure 1.5.3b Full Bridge Inverter Waveforms
Clamped Mode of Operation

effects have concluded, device Q_C is turned on. At this point device Q_D may still be conducting. It is likely at high frequencies of operation that the drive waveforms to transistors Q_A and Q_B or transistors Q_C and Q_D will overlap but this presents no problem to proper bridge operation. It is, however, necessary to delay the turn on of device Q_C long enough so that device Q_A and Q_C do not conduct simultaneously. The temporary short across the supply could damage both devices. Similar statements apply to devices Q_B and Q_D. The negative output voltage appears at the terminals of the secondary when device Q_D is turned off sufficiently long to reduce stored charge and device Q_B is turned on. It is quite apparent that operation in the clamped mode allows the current and voltage to be phase shifted through the secondary of the output transformer without serious side effects in the primary power circuit. The clamped mode is thus very appropriate for reactive loads such as those the transmitter might be required to drive. [1,2]

1.6 Method of Study

For the conclusion of this introduction the method of study is discussed as it applies to the implementation of the full-bridge inverter module. In the initial stages of inverter development, a single device

was tested to specify an appropriate power switch and drive scheme. The selection of a device includes the selection of essential components such as those in the snubber network. Resistor-Capacitor, Resistor-Capacitor-Diode, and Resistor-Capacitor-Active clamp networks were developed and compared for voltage snubbering capabilities. Once a discrete Darlington configuration had been chosen, various combinations of single and dual reverse drive networks were tested to minimize BJT storage time. This work is discussed further in the third chapter of this thesis.

The second phase of study involved half-bridge inversion. A single diagonal pair of devices was operated to determine the various conduction intervals of the transistors. This half-bridge operation is explained more completely within the testing results of the fourth chapter.

The third and final phase of development has been the operation of the bridge inverter as a full bridge in the straight inverter and clamped mode. During this time interval logic and protection circuits were developed to prevent shoot-through destruction of the devices within the bridge. These circuits are discussed in the fourth chapter which specifies the components of the thirty-kilowatt inverter module.

CHAPTER TWO

THE TRANSMITTER CONFIGURATION EMPLOYING VECTOR SUMMATION

2.1 Introduction

It is the purpose of this chapter to discuss the vector summation scheme and how it relates to the design goals of high efficiency, low distortion, and fault tolerance. The specific scope is to define the individual DC to quasi-squarewave conversion modules, examining their efficiency and distortion content. From the addition of eight individual modules a DC to stepped-sinusoidal inverter is synthesized. The total harmonic content of this resultant inverter is optimized by Fourier analysis and the system is defined in block diagram format. The modular approach is examined for its tolerance to system faults with the possibility of on-line correction of serious module failures within the system. Finally, all design requirements are considered on the basis of their effectiveness and reliability.

2.2 The Power Amplifier-Switched Mode Techniques

The power amplifier's fundamental purpose is to multiply the amount of energy in the input signal. This amplification insures the proper transmission of the information contained within the input signal over long

distances or through varying media (such as salt water) both of which attenuate the signal energy. High efficiency, low cost, fault tolerance, low distortion, and system reliability are major design considerations of the solid state VLF transmitter power supply.

For example, amplifier-type inverter circuits operating in Class B or Class C push-pull could provide signal gain [6]. The high power dissipation of the transistors operating in the linear region, however, would make such a choice impractical for any high power design. Conversely, the switched mode or Class D amplification is well suited to designs requiring high power gain. Switched mode amplification is a means of achieving very high efficiencies. The transistors are switched alternately between cutoff and saturation. As a result of the low saturation voltage of the transistor, the conduction losses are small even at high values of collector current. The resulting input power to output power conversion efficiency employing switched mode techniques significantly lowers the energy costs [6,10].

2.3 The Power Amplifier-Vector Summation Approach

Figure 2.3.1 and 2.3.2 which can be referenced to Hammond and Henry's previous work provide an excellent pictorial perspective of the vector summation approach.

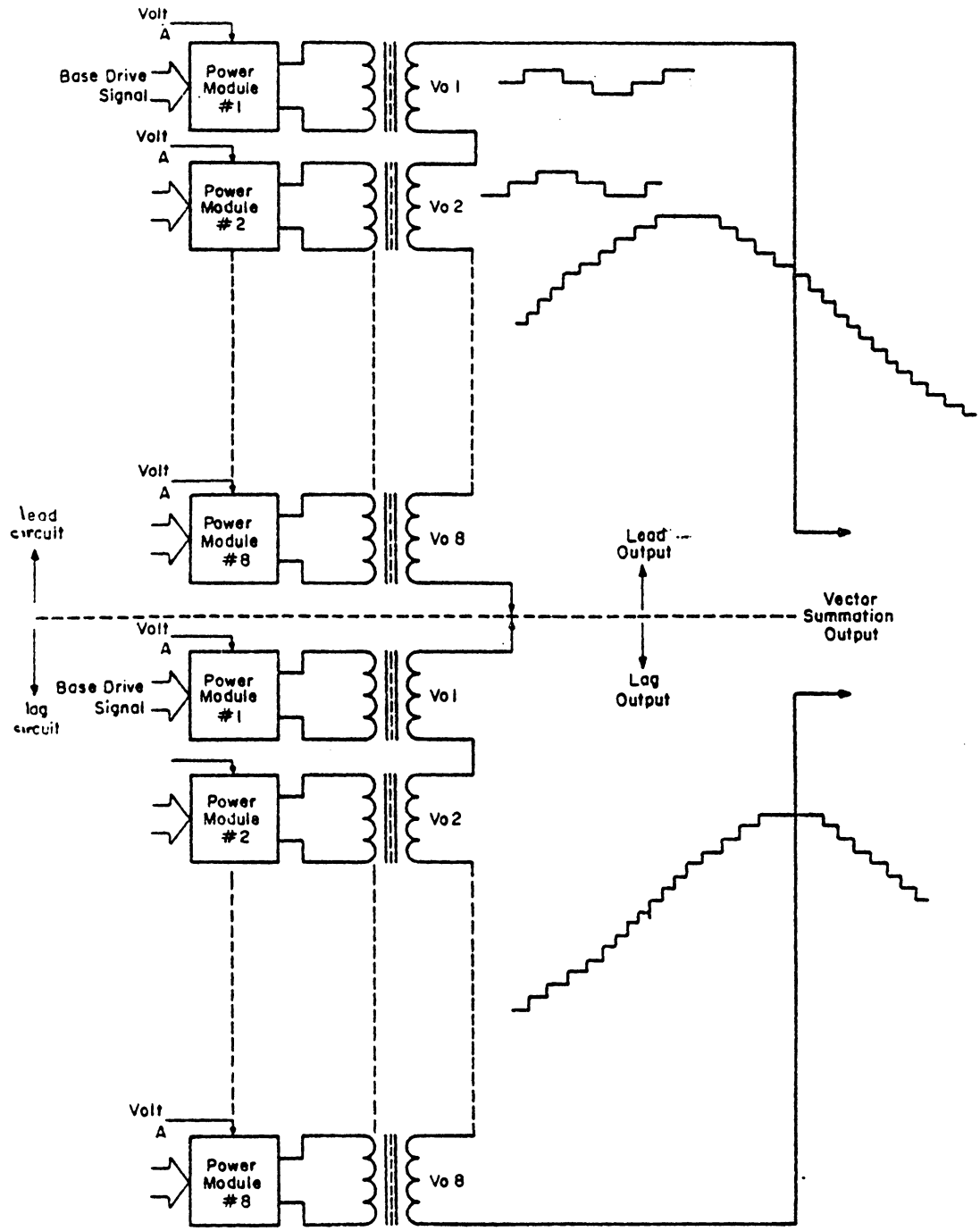


Figure 2.3.1 Sixteen Bridge Inverter Modules Employed in a Lead/Lag Vector Summation Scheme [2]

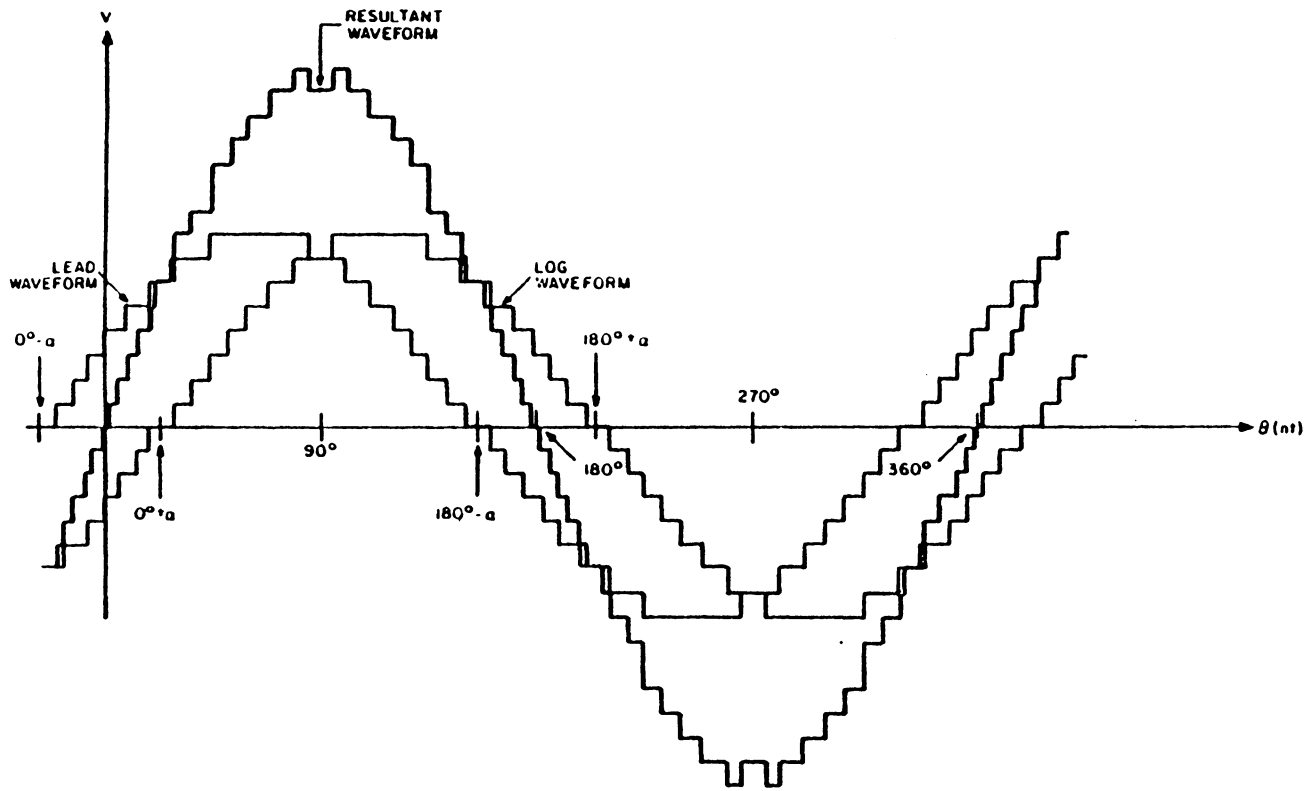


Figure 2.3.2 Resultant Stepped Sinusoidal Waveform Generated from Lead and Lag Waveforms [2]

Sixteen inverter power modules (Fig. 2.3.1) are employed to produce a substantially higher power sinusoidal output. The output voltage ($+V_{DC}$, $-V_{DC}$, or 0) for all sixteen DC to quasi-square modules is identical in magnitude to any of the others. Eight bridge-driven power transformers are connected in series in two separate phases. Each waveform is identified as belonging either to the lead phase or to the lag phase. The vectorial addition of two sinusoids separated by a phase angle 2α (Fig. 2.3.2) can be written:

$$V_{RESULTANT} = V \cos(\omega t) + V \cos(\omega t + 2\alpha) \qquad (2.3.1)$$

Alternately, suppose that zero time occurs at α so that the equation can be rewritten as:

$$V_{RESULTANT} = V \cos(\omega t - \alpha) - V \cos(\omega t + \alpha) \qquad (2.3.2)$$

Using simple trigonometry identifies the equation becomes:

$$V_{RESULTANT} = 2V \cos \alpha \cos(\omega t) \qquad (2.3.3)$$

Thus it can be seen that the resultant waveform is of the same frequency as the two individual parts with new magnitude $2V \cos \alpha$, which varies as a function of the angle α.

2.4 Vector Summation - Generating the Stepped Sinusoidal Output

Figures 2.4.1 and 2.4.2 show two possible methods of obtaining a stepped sinusoidal waveform [6]. In Figure 2.4.1 the individual quasi-squarewaves have progressively shorter durations to form the peak of the sinusoidal waveform. In Figure 2.4.2 each quasi-squarewave has an identical duty ratio so that the peak is formed by shifting the phase of the individual steps. This second method of obtaining the sinusoid is more desirable from the standpoint that each module processes the same amount of power. The case where some modules conduct for very short periods is prone to distortion. The current waveforms for inverters operated at very light duty cycles may not be the same as the current waveforms in inverter modules operated at moderate duty ratios. This difference may be the result of parasitic elements or snubber components. By no means are these the only two possible causes of additional distortion.

A Fourier analysis of a single quasi-square waveform portion of the stepped sinusoid provides equation 2.4.1:

$$v(t) = \sum_{\substack{n=1 \\ n \text{ odd}}}^{\infty} \frac{4V}{n\pi} \cos \phi \sin(n\omega t) \qquad (2.4.1)$$

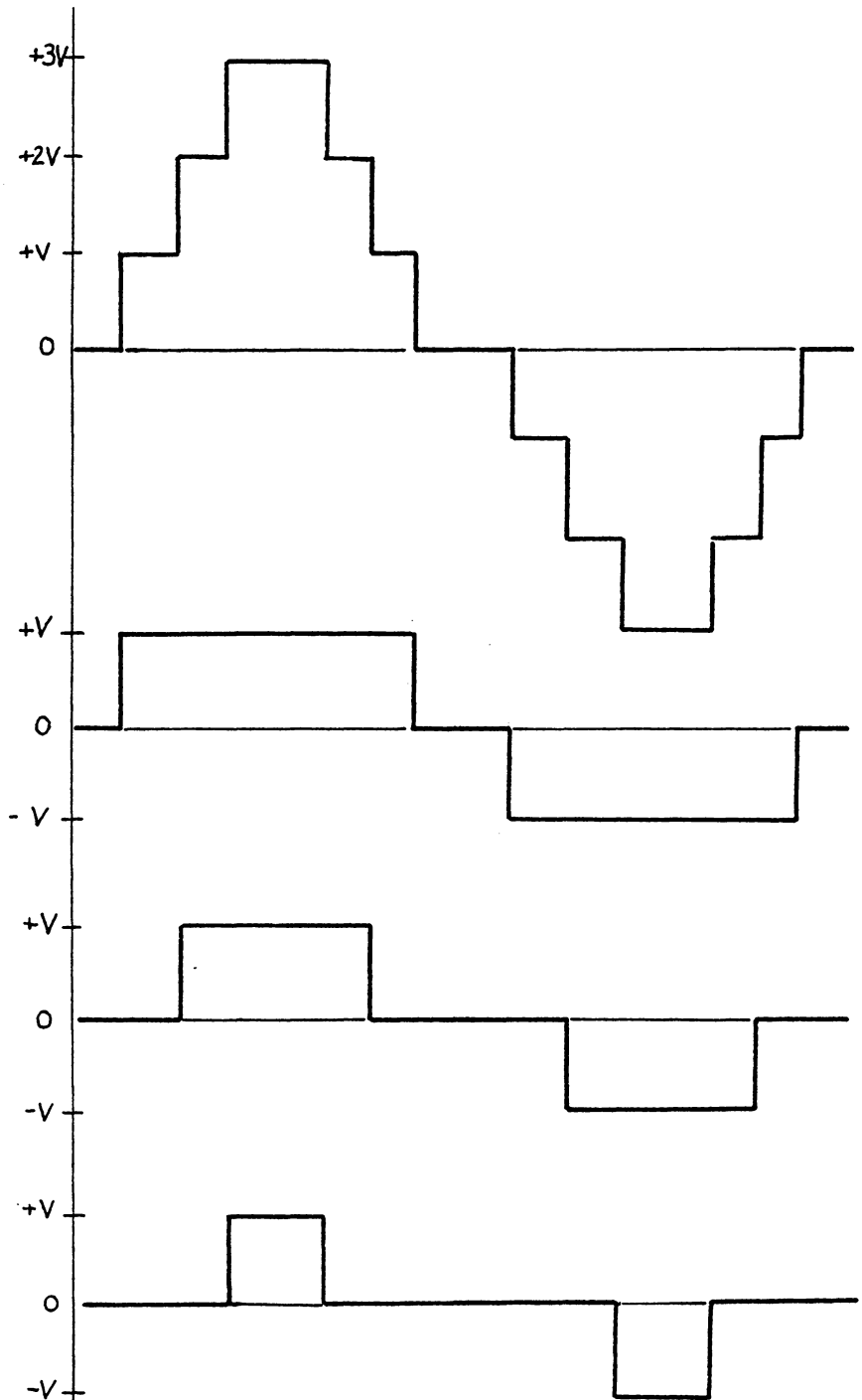


Figure 2.4.1 Stepped-Sinusoidal Voltage Generation Using Three Inverter Outputs with Different Duty Ratios

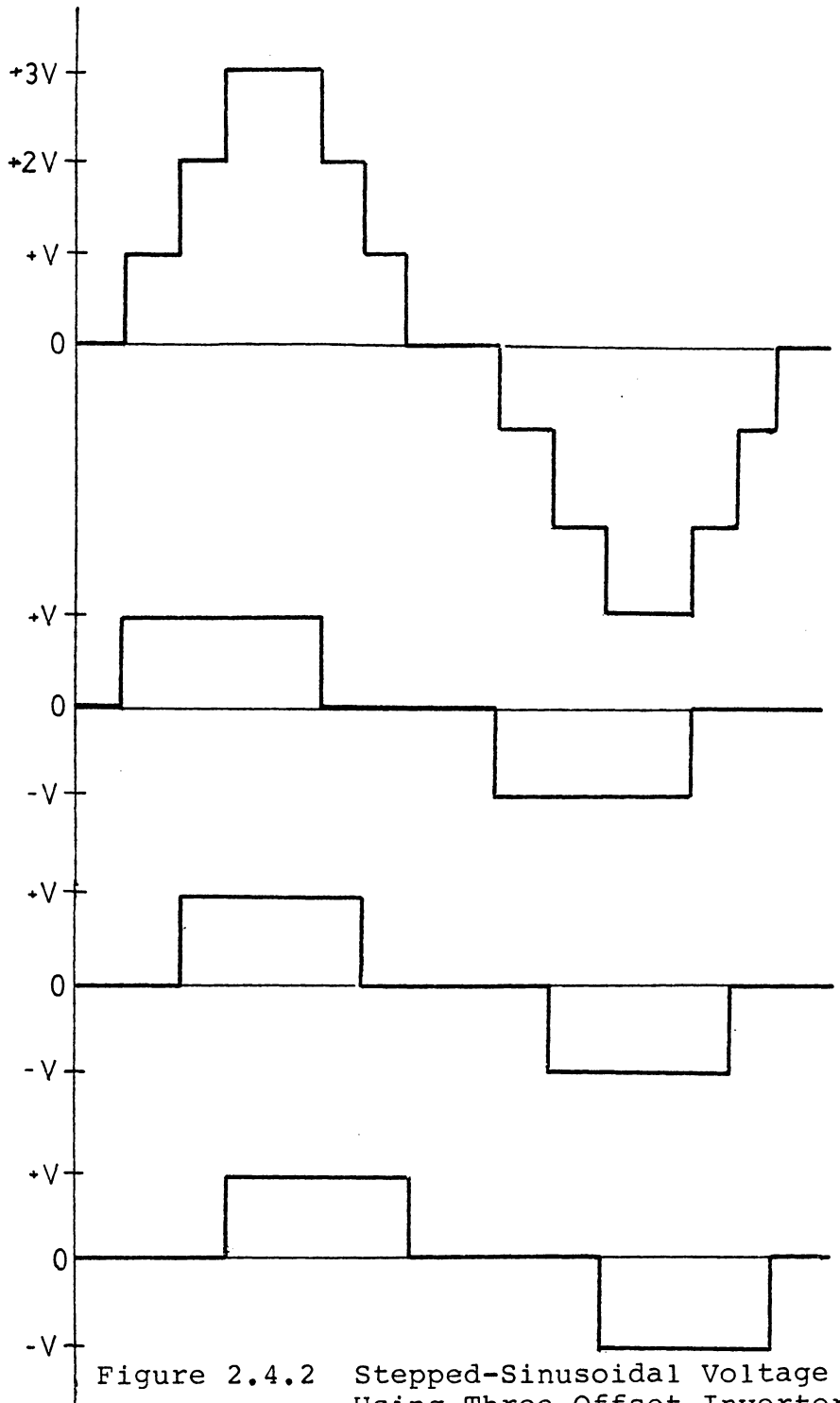


Figure 2.4.2 Stepped-Sinusoidal Voltage Generation Using Three Offset Inverter Outputs with Identical Duty Ratios

The evaluation of v(t) leaves the conclusion that the magnitude of the fundamental and all odd order harmonics is affected by the dwell angle or zone of zero output voltage (see Fig. 2.4.3). The waveform because of its symmetry contains only odd order harmonics and a graph is presented showing the relative magnitudes of the fundamental versus the third and fifth harmonics [6].

2.5 Harmonic Distortion - Optimizing the Stepped Sinusoidal Waveform

The entire amount of higher frequency components compared to the magnitude of the fundamental as a ratio is called total harmonic distortion. The equation for T.H.D. is shown below where

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} A_n^2}}{A_1} \qquad (2.5.1)$$

and A_n represents the magnitude of the n^{th} frequency Fourier component of the waveform [6].

As mentioned initially, a Fourier analysis is required to optimize the distortion content of the resultant stepped sinusoidal waveform. In Figure 2.5.1 different stepped waveforms are shown with an indication of their respective THD. The THD of a stepped sinusoid varies as a function of step size

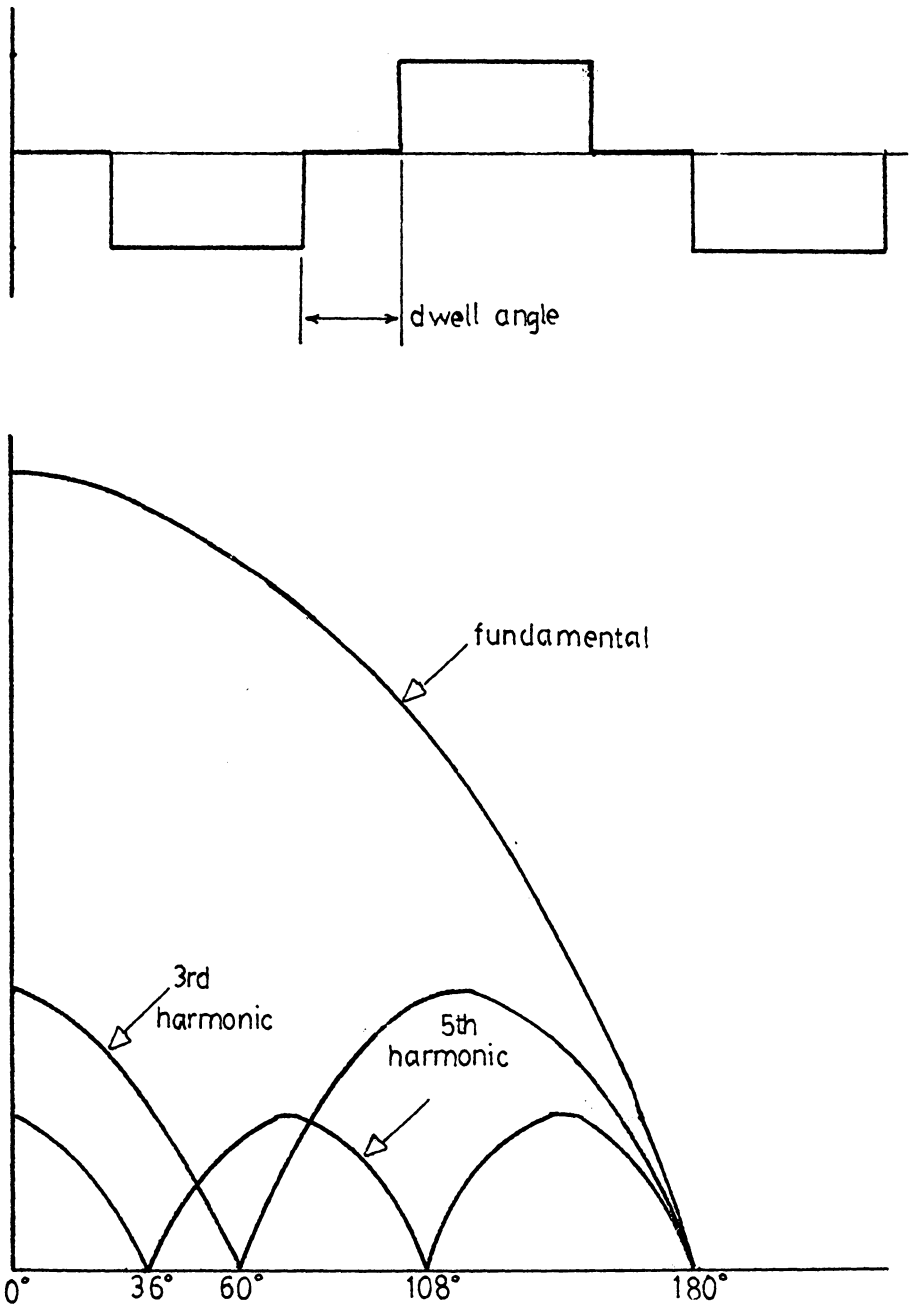


Figure 2.4.3 Relative Magnitudes of the Fundamental, Third, and Fifth Harmonics as a Function of the Dwell Angle [6]

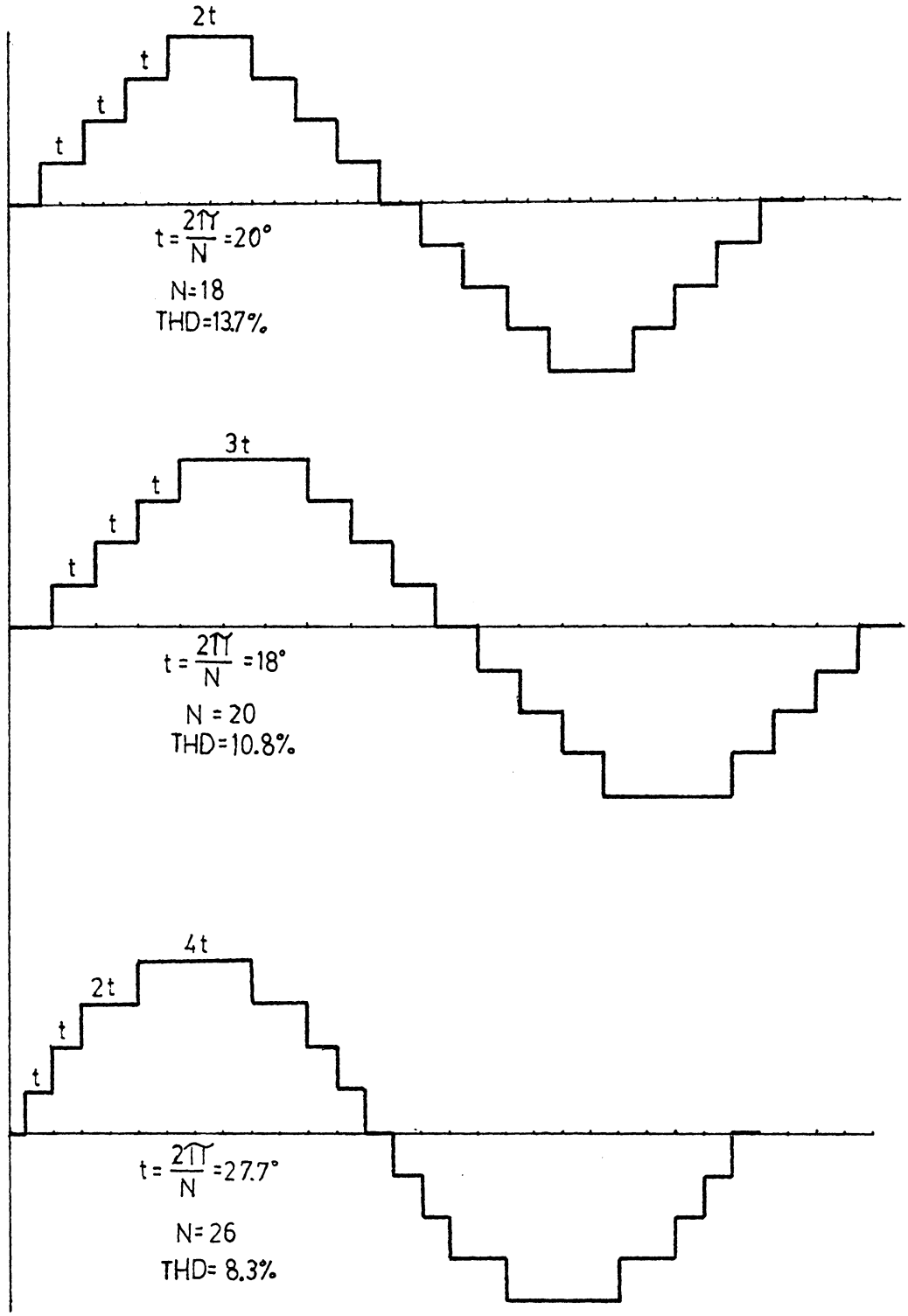


Figure 2.5.1 Total Harmonic Distortion for Three Stepped-Sinusoidal Waveforms [6]

and the total number of steps. For the communications transmitter with its eight step waveform (see Figures 2.5.2a and 2.5.2b) the general equation for the Fourier expansion is given by Equation 2.5.2

$$v(t) = \sum_{\substack{n=1 \\ n_{odd}}}^{\infty} \frac{4V}{n\pi} (\cos n\alpha + \cos n\beta + \cos n\Delta + \cos n\gamma + \cos n\varepsilon + \cos n\Omega + \cos n\lambda + \cos n\tau) \sin n\omega t \qquad (2.5.2)$$

This equation can be used in conjunction with equation (2.5.1) to calculate the total harmonic distortion as a function of the angles α, β, Δ, ε, Ω, λ and τ. The result of these calculations is shown in Table 2.5.1 [2]. Often it is not necessary to minimize all of the higher order distortion terms especially in this case where the antenna acts like a low pass filter. Using (2.5.1) and (2.5.2) for the third harmonics produces equation (2.5.3):

$$\text{Harmonic Distortion} = \frac{\sqrt{(\frac{4V}{3\pi})^2 (\cos 3\alpha + \cos 3\beta + \cos 3\Delta + \cos 3\gamma + \cos 3\varepsilon + \cos 3\Omega + \cos 3\lambda + \cos 3\tau)^2}}{\frac{4V}{\pi} (\cos \alpha + \cos \beta + \cos \Delta + \cos \gamma + \cos \varepsilon + \cos \Omega + \cos \lambda + \cos \tau)} \qquad (2.5.3)$$

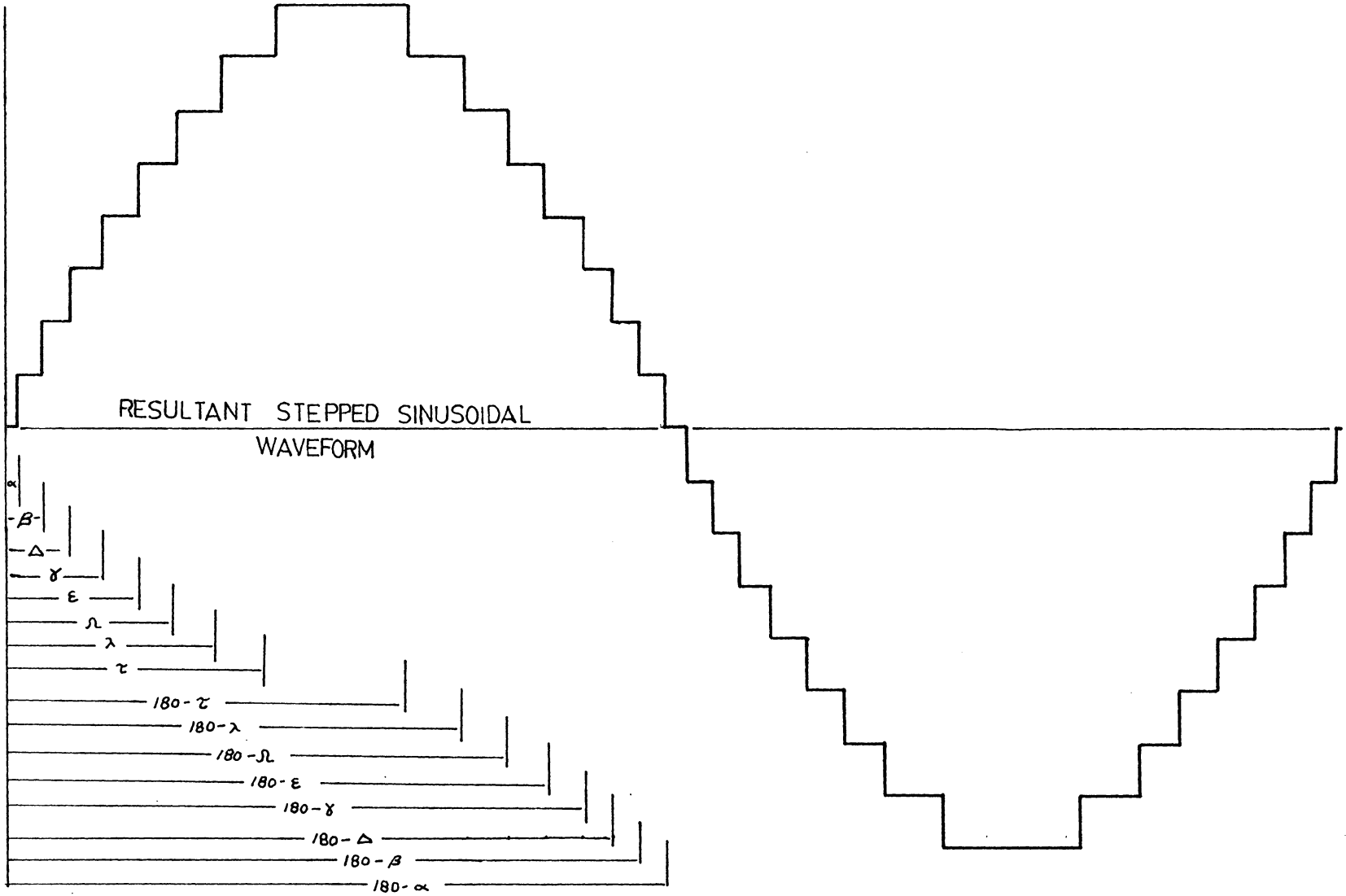


Figure 2.5.2a Stepped-Sinusoidal Output as a Function of the Angles (α, β, Δ, γ, ε, Ω, λ, τ)

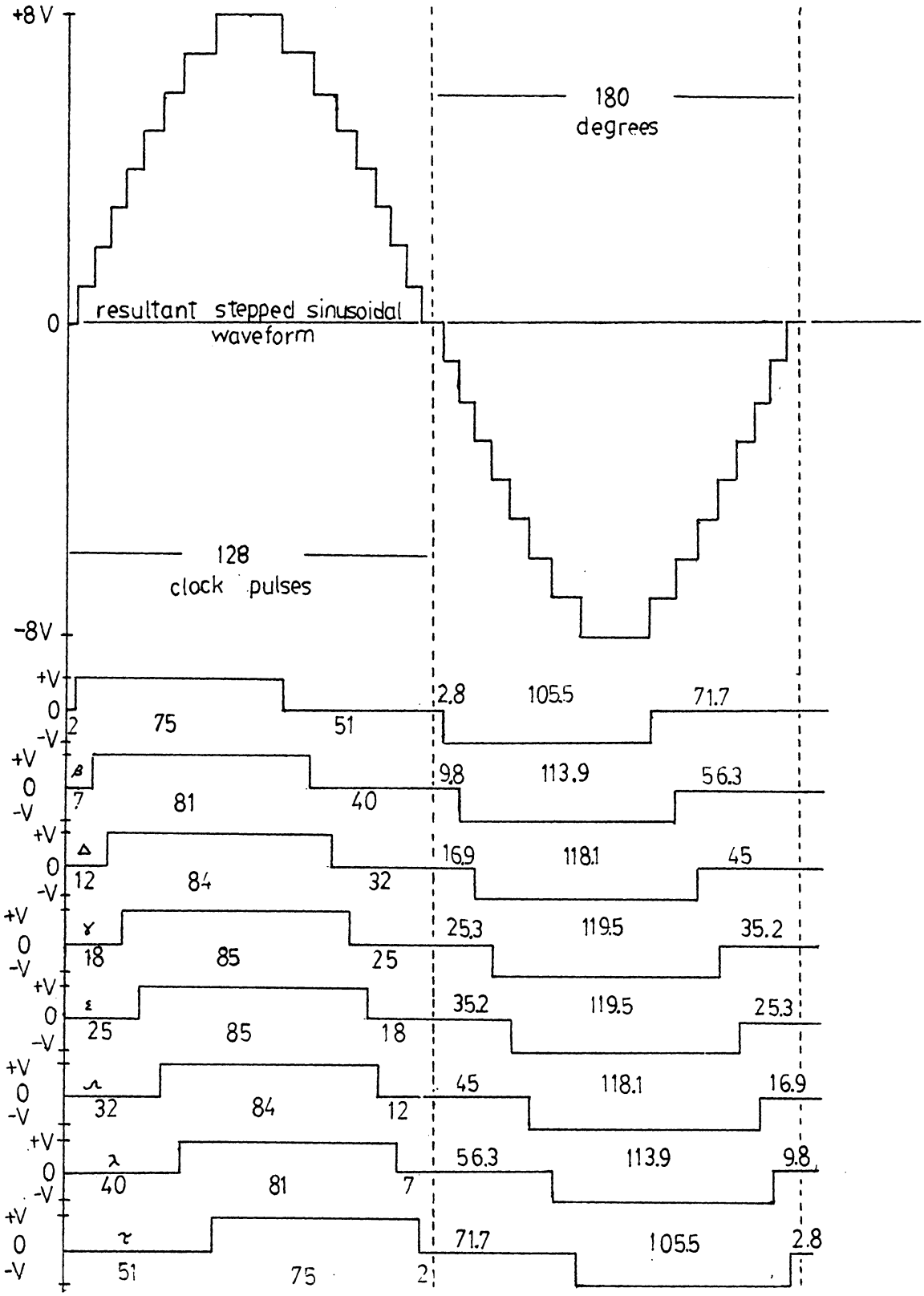


Figure 2.5.2b Synthesis of the Stepped-Sinusoid Employing Eight DC to Quasi-Squarewave Inverters [1]

Table 2.5.1

Quasi-Squarewave Voltage Step	Turn on Angle (Degrees)	Turn Off Angle (Degrees)
1	$\alpha = 3.6^{\circ}$	$180 - \tau = 110.4^{\circ}$
2	$\beta = 10.8$	$180 - \lambda = 125.7$
3	$\Delta = 18.2$	$180 - \Omega = 136.6$
4	$\gamma = 25.9$	$180 - \varepsilon = 145.8$
5	$\varepsilon = 34.2$	$180 - \gamma = 154.1$
6	$\Omega = 43.4$	$180 - \Delta = 161.8$
7	$\lambda = 54.3$	$180 - \beta = 169.2$
8	$\tau = 69.6$	$180 - \alpha = 176.4$

The eight quasi-squarewave inverter outputs are summed using the method of Figure 2.4.2 so that each waveform has approximately the same duty ratio. "This method of sinusoid generation results in a range of positive and negative duty ratios of 28% to 32%." [2] Digital control is employed to implement the appropriate drive signals to the individual modules. "The number shown on each step of the stepped sinusoidal waveform (Fig. 2.5.2a) and the quasi-square waveform (Fig. 2.5.2b) indicates the time length of each step, in the unit of a clock pulse (to the digital control circuit). A complete cycle of the sinusoidal waveform is divided into 256 clock pulses and, therefore, the frequency of the sinusoid is $1/256^{th}$ of the clock frequency." It will be noted that each clock pulse is equivalent to $2\pi/256$ or 1.41 degrees so that angle α is now 2.81^{o}, β is now 9.84^{o}, Δ is now 16.9^{o} and so forth. (See Table 2.6) The difference between these values and the optimized distortion content values is caused by the digital clock requirement. Recall that the clock is 256 times the output frequency so that for an output frequency of 25 KHz this requires the use of a 6.4 MHz clock. Now suppose that the completely optimized values are used so that each clock pulse is $.1^{o}$ in duration. This would require a clock 3600 times the output frequency,

Table 2.6

Quasi-Squarewave Voltage Step	Turn On Angle (Clock Pulses)	(Degrees)	Turn Off Angle (Clock Pulses)	(Degrees)
1	2	2.81	77	108.28
2	7	9.84	88	123.75
3	12	16.88	96	135
4	18	25.31	103	144.84
5	25	35.16	110	154.69
6	32	45.00	116	163.12
7	40	56.25	121	170.16
8	51	71.72	126	177.19

For the same 25 KHz output frequency a 90 MHz clock would be required. This sort of clock rate would be quite impractical in normal digital control logic due to individual gate delays, addressing times, and other timing criteria. As a consequence of the trade off between optimized distortion and a reasonable clock rate, the turn on and turn off times of the inverter modules are altered slightly.

2.6 Base Drive Generation for the Inverter Modules

The digital controller must implement 64 base drive logic signals appropriate to each of four power transistors in two phases of eight inverter modules [1]. Since each output cycle of the system is divided into 256 clock periods, it is convenient to employ 256 × 8 Read Only Memories (ROMs) to store the information germane to the production of the output waveform. (See Fig. 2.6.1) Normally a total of eight ROMs would be required for the lead and lag phases of modules. One ROM would generate the drive signals for eight Q_A switches, one would provide the Q_B switches' drive signals, and the other two ROMs would store the Q_C and Q_D drive signals. An identical set of four ROMs would yield the drive signals for the devices in the lag phase. The clamped mode operation requires equivalent drive signals for each switch pair Q_A and Q_D

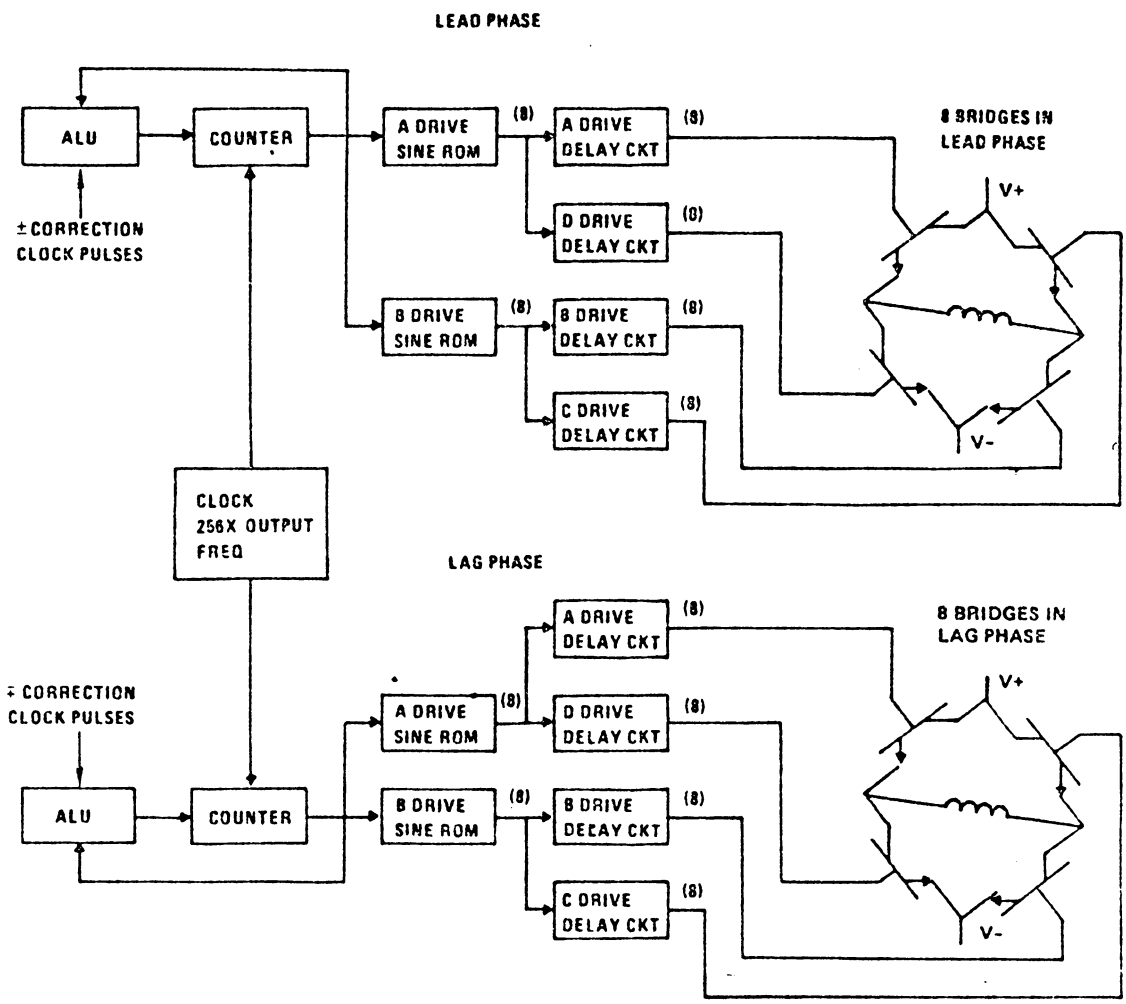


Figure 2.6.1 LEAD/LAG Base Drive Signal Generation 2

(Q_B and Q_C) with the signal for $Q_D(Q_C)$ time shifted with respect to the signal for switch $Q_D(Q_B)$. In this case then only four ROMs total are required with the output of each ROM generating a set of drive signals and a delayed set of drive signals. Each pair of ROMs is addressed by a counter sharing a common clock with the counter that addresses the pair of ROMs in the other phase. In order to provide the phase correction α to vectorially sum the lead and lag outputs together a number of clock pulses is added to the lead addressing counter and subtracted from the lag addressing counter. There is no phase shift in the summed sinusoidal output during corrections because the separate lead and lag stepped waveforms are shifted forward and backward in time, respectively [2].

Base drive generation using ROMs and a system clock provides a great deal of system versatility. The inverters within the power amplifier can be operated with the phase shifts shown earlier to provide a stepped sinusoidal output. Another possibility is to replace the base drive ROMs so that all the inverters act in phase to produce a squarewave or quasi-squarewave output. Normally the transmitter (operating in Class D) would be coupled with a high Q resonant antenna as the loading element.

The antenna acts as a low-pass filter so that a large sinusoidal current would flow into the load antenna only at the resonant frequency [2].

2.7 Fault Tolerance Techniques Applied to the Power Amplifier

Additional flexibility is available from the power amplifier due to its unique construction from several smaller inverter modules. Each of the individual modules is connected through its transformer secondary to every other module.

"The load current through the transformer secondary winding of each of the cascaded inverters depends on the resultant output voltage and the load condition which could be resistive (load current in phase), capacitive (load current leading output voltage), or inductive (load current lagging). Therefore, the transformer secondary current can have any phase with respect to the secondary winding voltage....The direction of the primary current depends on the direction of the secondary current." [1]

At this point the designer might hypothesize what would happen to the secondary load current i.e. the transmitter output if a particular inverter bridge module malfunctioned. Such a study is an investigation of the systems' tolerance to faults in the individual modules.

The failure can occur so that the bridge inverter's primary appears shorted in both directions, shorted in one direction and high impedance in the other direction, or open circuited in both directions. These failure modes would be coupled to the type of switch failure occuring in the power processing circuitry connected to the primary. A short of a power transistor or anti-parallel diode would have the effect of causing a high current the next time a power switch on the same side of the bridge were turned on. This would open the fuse or circuit breaker protecting the dc power supply connected to the bridge. On the other hand, if a power transistor were to fail so that it appeared as an open circuit, ultimately the output transformer would saturate due to the dissymmetry of the current flowing through the primary. The resulting saturation of the transformer's core would be coupled with a reduced impedance and high current that would again cause the mechanism (fuse or circuit breaker) protecting the bridge power supply to open [2].

The case where the bridge primary appears as an open circuit is more serious than that where the primary is shorted. The open circuit reflected toward the secondary would evoke an increase in distortion of the output sinusoid. It is probable that even in this case the secondary of the faulted bridge's output transformer would

saturate once every half cycle of the stepped sinusoidal output voltage. Coupling this fact with the antenna's low-pass filtering action might reduce the severity of the waveform degradation caused by the open circuited primary in the faulted bridge module.

Suppose the design engineer connected ten bridge inverters to one another through their secondaries rather than the required eight. The possibility would exist of correcting faults in one or two modules while the extra two modules (normally not employed) would replace the failed modules. The primaries of modules containing failed parts must be shorted to insure that they have a minimal effect on secondary load current. Similarly the primaries of modules not presently in use must also be shorted. When the failure occurs, the failed module's primary is shorted, its base drives are removed and applied to an on-line replacement module. The short on the primary of the replacement module is removed so that its operation becomes identical to that of the recently failed inverter bridge [2].

2.8 Vector Summation - A Recapitulation

In summary the vector summation approach through the use of independent inverter modules offers a large

amount of control adaptability. Different outputs may be obtained by employing different base drive ROMs. The output frequency can be changed by increasing or decreasing the system clock. For example to go from 25 KHz to 30 KHz requires the clock frequency to be increased from 6.4 MHz to 7.68 MHz. The amplitude of the resultant output can be changed by varying the phase angle α separating the lead and lag phases. With 16 modules, the peak resultant output can be varied as the function $16 * V_{DC} * \cos \alpha$ between 0V and $16 * V_{DC}$.

CHAPTER THREE

DEVICE AND DRIVE SELECTION

3.1 Introduction

Appropriate power switch selection is a crucial phase in the development of a high power, full-bridge inverter. With this view in mind, a substantial portion of this thesis is dedicated to increasing the designer's understanding of the costs and benefits associated with the switching devices chosen for this project. The device selection also includes the drive requirements and the choise of suitable switching and or snubbering components which will prevent failures due to stresses such as surpassing the maximum voltage ratings, occurence of second breakdown phenomena, or exceeding the switch's power dissipation limits.

3.2 The Choice of a Power Switch - FETs

Initially both FETs and bipolar junction transistors were considered for use within the power switching unit of the inverter bridge. Field Effect Transistors were considered because their switching time is considerably faster than bipolars (ten nanoseconds is typical) [12,13]. The speed advantage of the FET at turn off is a result of the lack of stored charge within the device. To turn a FET off merely requires the discharge of the gate capacitance. In addition to high frequency performance, the FET has a high

input impedance which allows the designer to use simplified low power drives.

Nevertheless, power FETs were not chosen because the highest power FET switch then available was a 450 Volt, 11 Ampere device requiring the designer to parallel perhaps ten devices within the inverter module to reach the thirty-kilowatt design goal. While paralleling several FETs is not an impossible task, there is a possibility of large current imbalances at turn on and turn off between devices. Even if gate-source capacitances could be controlled within 1% of each other, a difference of five nanoseconds or so in the application of drive to two devices might turn one FET completely on while the other power FET remained turned off. For this reason it would have been impractical to parallel ten FETs for each power switch in the bridge [14].

3.3 The Choice of a Power Switch - Darlington BJTs

Instead of choosing a power FET, bipolar junction transistors in the Darlington configuration were employed in the inverter. The effective switching device created by the combination of a driver transistor and power transistor has characteristics similar to a single BJT with a current gain that is, to a first approximation, equivalent to the product of the individual transistor's betas [11].

3.4 Darlington Transistors - G.E. D67DE

Two types of Darlington configuration were chosen for final consideration as the power switching unit in the bridge inverter module late in September of 1981. The first type, a GED67DE power Darlington exists as a prefabricated package. It had excellent characteristics including a high current gain and short device storage time. Unfortunately, at the time the transistors were chosen, the GE device was fabricated with an anti-parallel diode with a large reverse recovery time (about 4 μsec). This is the time interval during which the upper Darlington package in a bridge or totem-pole configuration would appear as a short to the lower Darlington package. Such a reverse conduction time period would be unacceptable during the turn on of the lower switch when a short circuit current would flow in the diode and lower switch from the power source [14].

3.5 Darlington Transistors - Westinghouse D7ST-D60T

The second type of Darlington power switch tested was a discrete combination of the Westinghouse D7ST power transistor and a drive transistor. Initially, the Westcode WT3300 was used as the drive transistor; however, ultimately the Westinghouse D60T was employed as the driver. The

expected overall gain of the discrete combination could be expected to be about the same or slightly less than that for a prefabricated Darlington. The discrete Darlington composed of the Westinghouse D7ST and D60T was chosen as the best design solution since an extremely fast, soft reverse recovery diode (Westinghouse R502) with a reverse recovery time of 300 nanoseconds could be used in conjunction with the discrete pair. This diode did not provide a reverse conduction path for a long enough period of time to damage or stress the power transistors in the bridge [14].

3.6 D.C. Gain of the Darlington Configuration

There are several advantages to the utilization of the Darlington as a power switch. Figure 3.6.1 is a diagram of two transistors, Q1 and Q2, with their various currents defined. The total collector current (I_C) is the sum of the individual collector currents (I_{C1} and I_{C2}). These currents can be reexpressed via the following equations:

$$I_C = I_{C1} + I_{C2} \tag{3.6.1}$$

$$I_{C1} = \beta_1 I_{B1} + (\beta_1 + 1) I_{CO1} \approx \beta_1 I_{B1} \tag{3.6.2a}$$

$$I_{C2} = \beta_2 I_{B2} + (\beta_2 + 1) I_{CO2} \approx \beta_2 I_{B2} \tag{3.6.2b}$$

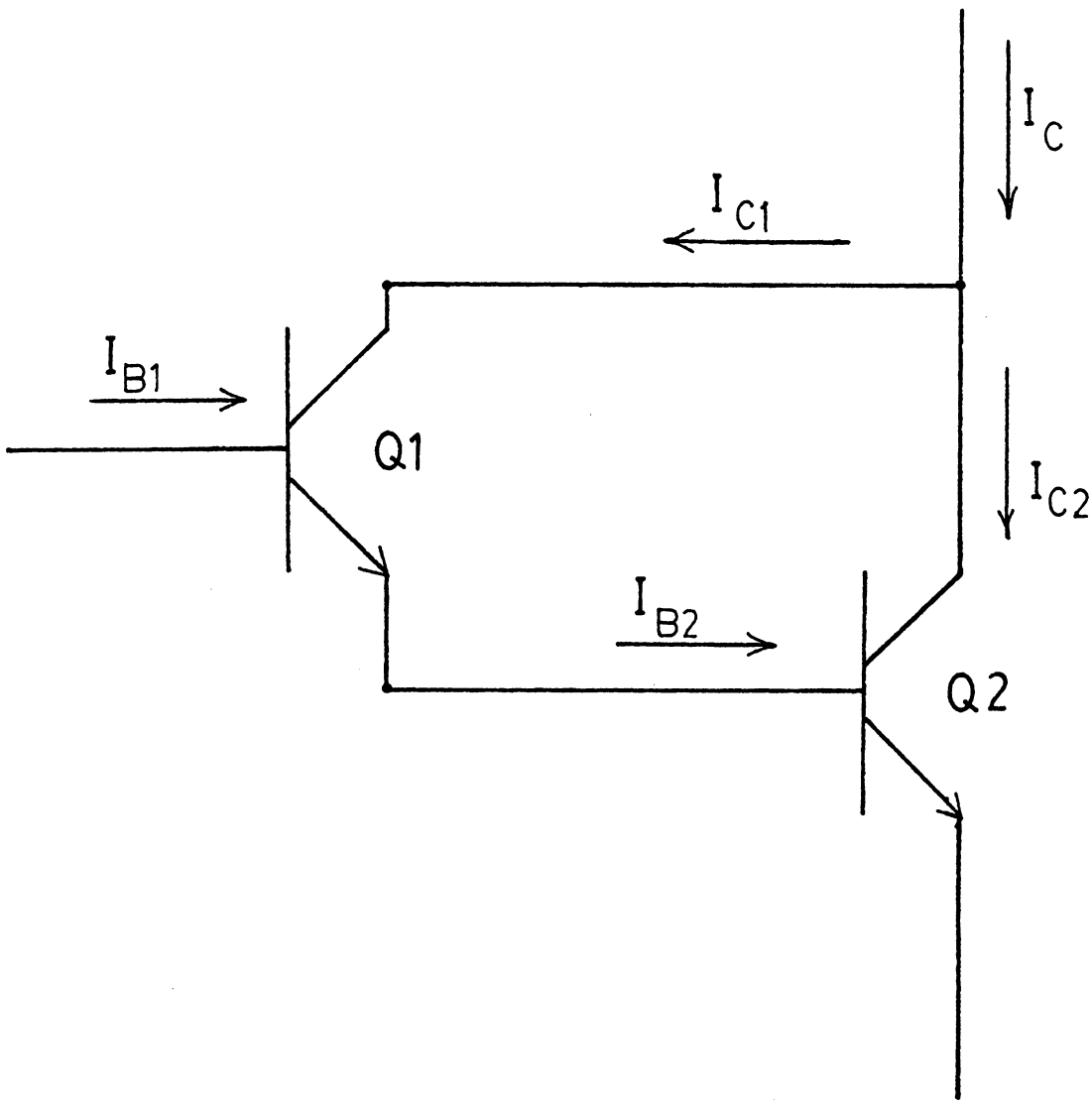


Figure 3.6.1 Darlington Configuration of Two NPN Transistors

$$I_C = \beta_1 I_{B1} + \beta_2 I_{B2} \tag{3.6.3}$$

$$I_{B2} = \frac{I_{C1}}{\alpha_1} = (\frac{\beta_1 + 1}{\beta_1}) I_{C1} = (\frac{\beta_1 + 1}{\beta_1}) \beta_1 I_{B1} = (\beta_1 + 1) I_{B1} \tag{3.6.4}$$

$$I_C = \beta_1 I_{B1} + \beta_2(\beta_1 + 1) I_{B1} = (\beta_1 + \beta_2 + \beta_1\beta_2) I_{B1} \tag{3.6.5}$$

$$\frac{I_C}{I_{B1}} = \beta_1 + \beta_2 + \beta_1\beta_2 \equiv \beta_{OVERALL} \tag{3.6.6}$$

The d.c. gain of the Darlington pair is slightly greater than the product of the d.c. gains for the individual transistors. In the case where Q1 was the D60T driver transistor and Q2 was the D7ST power transistor β_1 could be as high as 30 since operation is at a very low collector current (see Fig. 3.6.2 @ I_C = 10 - 30A) while β_2 might be 10 [15,16].

Several factors would act to reduce the transistors' d.c. current gains. First, the driver device data shown in Figure 3.6.2 is for a device operating at the interface between the quasi-saturation and linear region. As the driver device in the Darlington configuration is driven into

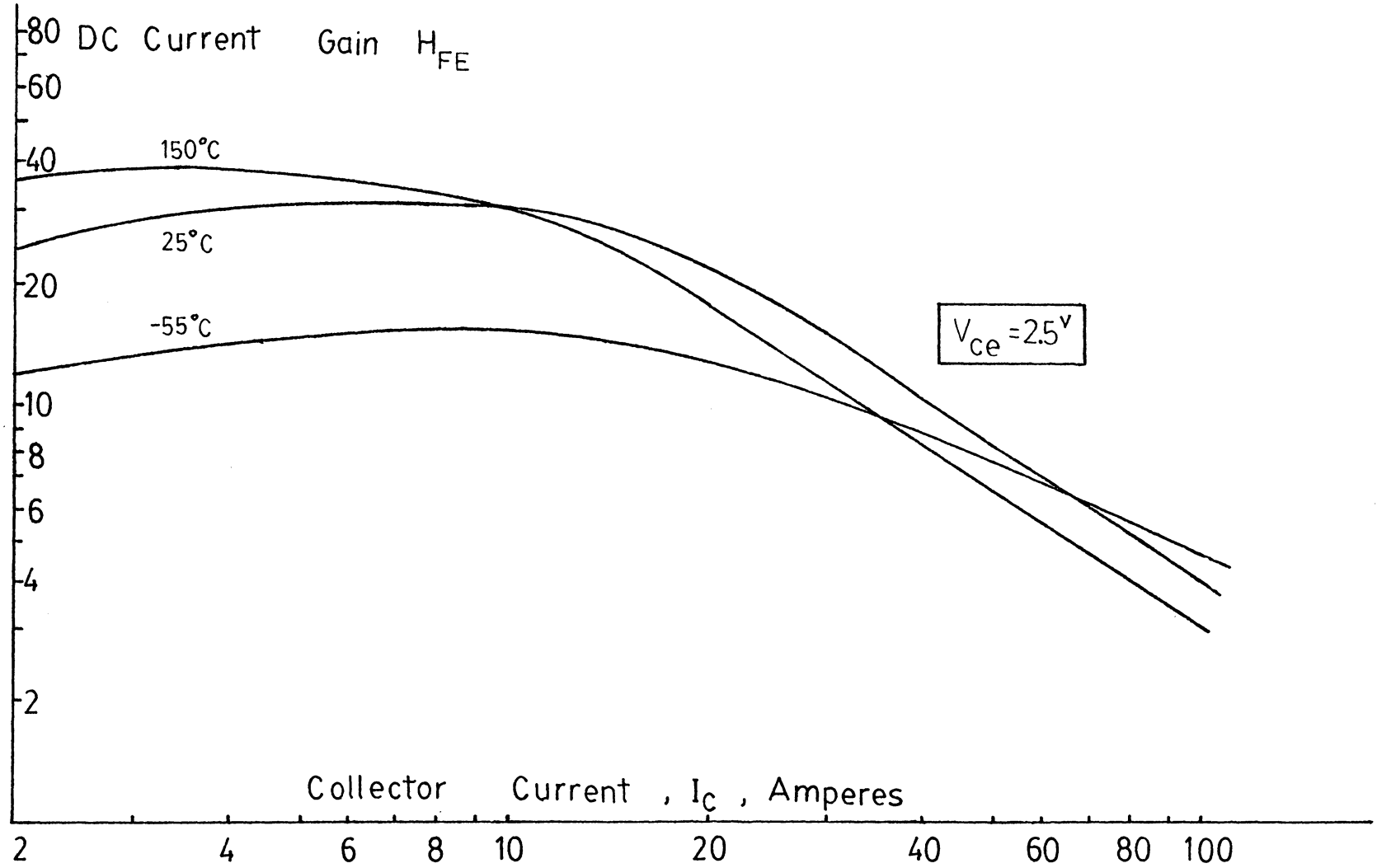


Figure 3.6.2 D.C. Current Gain Versus Collector Current for the D60T Driver Transistor [15]

the hard saturation region of operation ($V_{CD} \leq .5V$) the d.c. current gain would fall considerably below that calculated via the graph of current versus d.c. gain. The reduced gain as the power transistor passes through quasi-saturation into the deep-saturation state is explained by the effective base width modulation of the device [4]. In Figure 3.6.3 the collector-emitter voltage is shown as a function of collector current with a fixed base current. Note that for a collector-emitter voltage of three-tenths of a Volt and base current of six Amperes that the collector current is forty Amperes. In this case the forced d.c. gain would be given by equation 3.6.7a forced d.c. gain is used since the device is operating under hard saturation conditions.

$$\beta_f = \frac{I_C}{I_B} = \frac{40}{6} = 6.7 \qquad (3.6.7a)$$

Now compare the forced gain for a collector-emitter voltage of one and one-half volts and a base current of six Amperes. The collector current (I_C) is

$$\beta_f = \frac{I_C}{I_B} = \frac{53}{6} = 8.8 \qquad (3.6.7b)$$

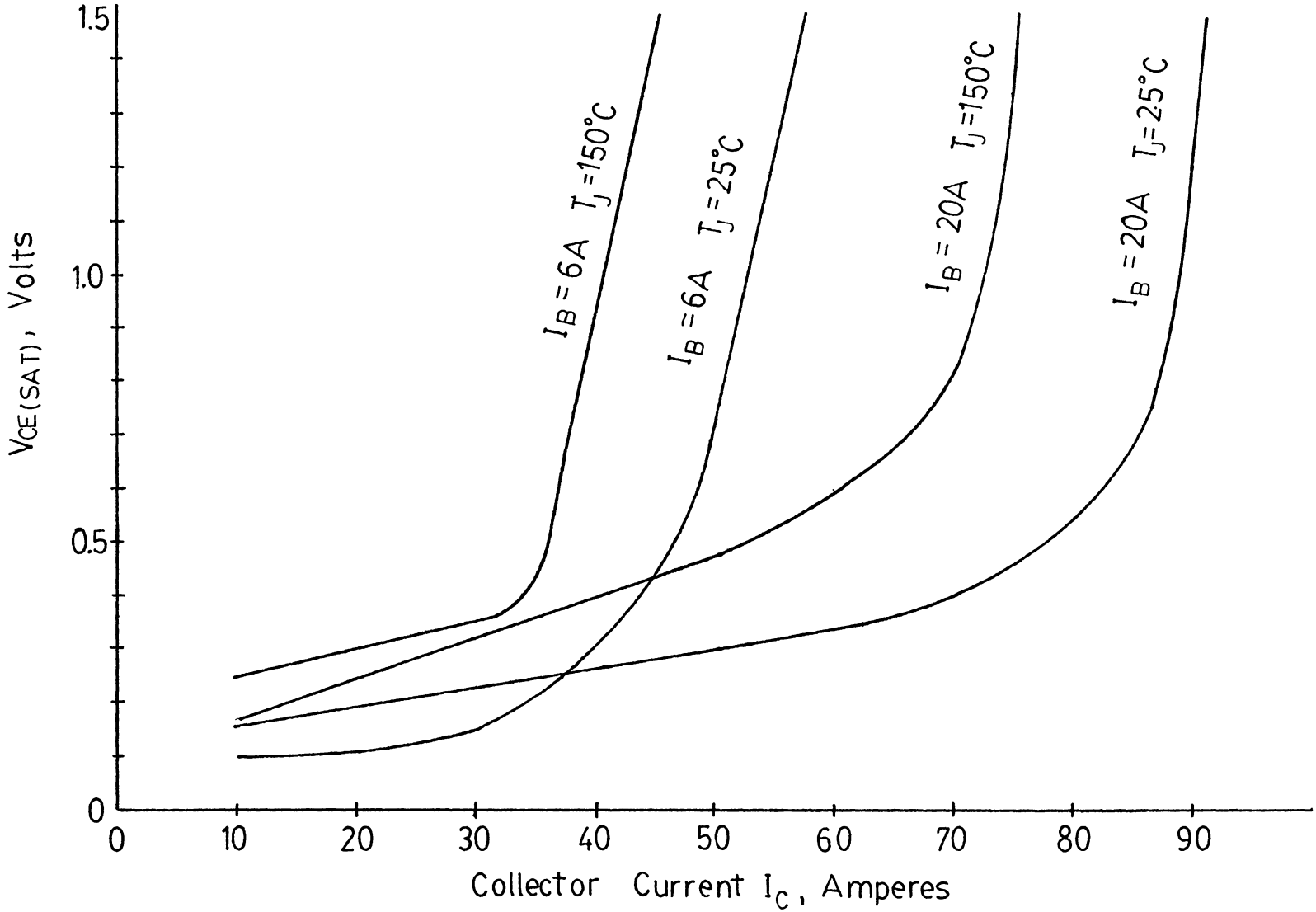


Figure 3.6.3 Collector-Emitter Saturation Voltage as a Function of Collector Current for D60T [15]

approximately fifty-three Amperes for a forced gain higher than that previously calculated. It is likely that the forced gain is less than or equal to eight in this application since the collector current of the D60T should be less than thirty Amperes and the measured base current is approximately four Amperes [15,16].

The second gain reduction would occur because the data for the D7ST (Q2 in this case) is given at a collector-emitter voltage of two and one-half volts. The collector-emitter potential of the power device is equivalent to that of the driver device and the base-emitter voltage of the power device combined. In this case V_{CE} would be less than one and one-half volts so that the power device's gain would be reduced but not as significantly as if it were completely saturated.

3.7 Darlington Configuration Utilizing Leakage Stabilization Resistances

Generally the Darlington configuration is employed with several resistances which also have the effect of reducing the overall gain but which provide a functional path for device leakage currents to flow [4]. Observing Figure 3.6.1 it can be seen that the leakage current from transistor Q1 is injected entirely into the base of transistor Q2. This would yield the external appearance of a high

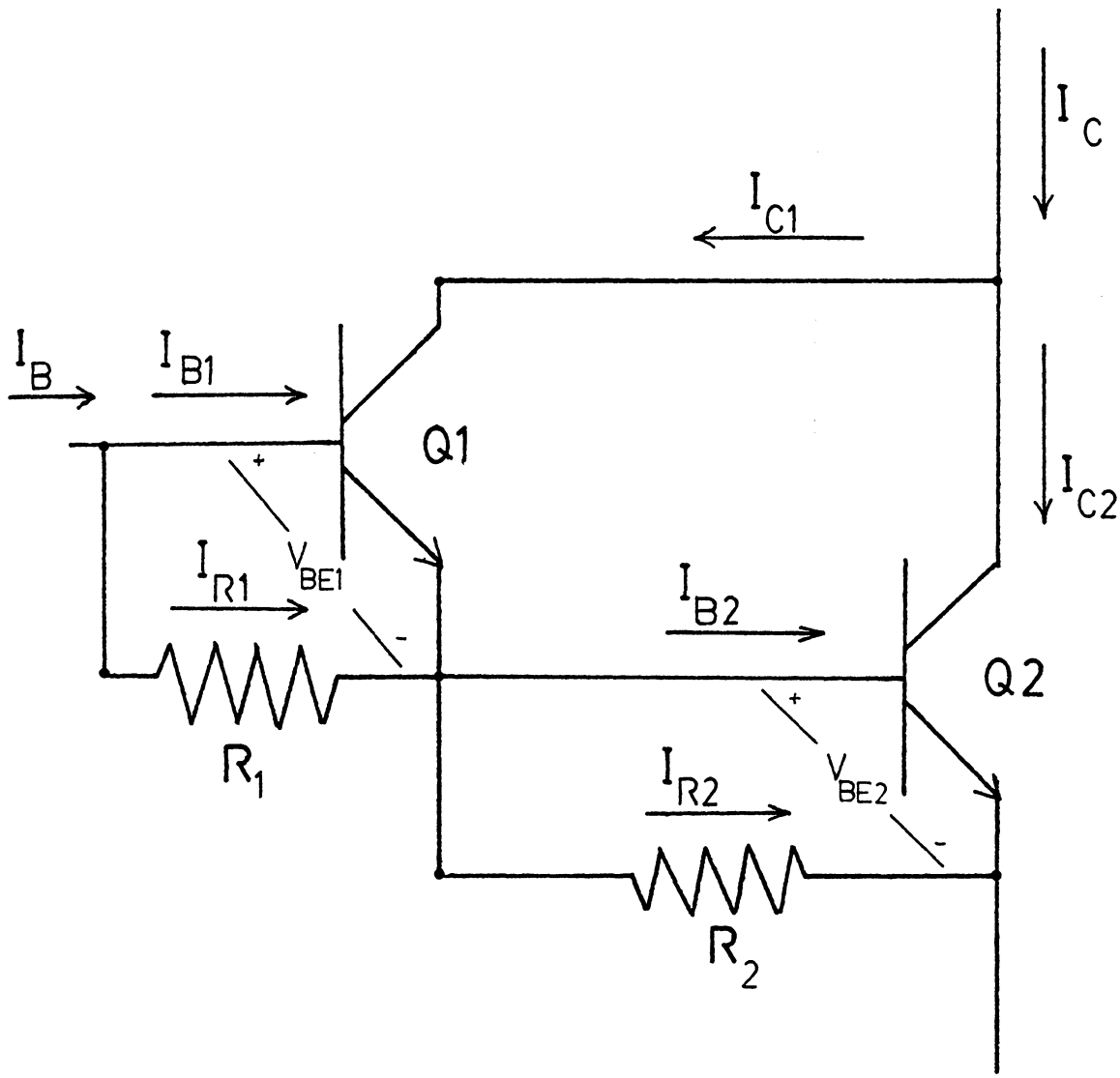


Figure 3.7.1 Darlington Configuration with Stabilization Resistances R_1 and R_2

leakage current because the transistor Q2 would amplify the initial leakage current in addition to supplying its own component to the total leakage current. In Figure 3.7.1 the resistance R_2 provides an alternative path for the leakage current. The way in which the addition of resistances R_1 and R_2 affect the d.c. gain of the Darlington pair may be calculated with reference to Figures 3.6.1 and 3.7.1. The following equations provide an estimate of the gain deviation caused by the R_1, R_2 pair. Repeating the equations (3.6.1)-(3.6.3) for Figure 3.7.1 and

$$I_C = I_{C1} + I_{C2} \qquad (3.6.1)$$

$$I_{C1} = \beta_1 I_{B1} \qquad (3.6.2a)$$

$$I_{C2} = \beta_2 I_{B2} \qquad (3.6.2b)$$

$$I_C = \beta_1 I_{B1} + \beta_2 I_{B2} \qquad (3.6.3)$$

adding the new equations (3.7.1)-(3.7.5) yields the desired result.

$$I_{B2} = (\beta_1 + 1) I_{B1} - \frac{V_{BE2}}{R_2} + \frac{V_{BE1}}{R_1} \qquad (3.7.1)$$

$$I_C = \beta_1 I_{B1} + \beta_2 \quad (\beta_1 + 1) I_{B1} - \frac{V_{BE2}}{R_2} + \frac{V_{BE1}}{R_1} \qquad (3.7.2)$$

$$\frac{I_C}{I_{B1}} = \beta_1 + \beta_1\beta_2 + \beta_2\left(1 - \frac{V_{BE2}}{R_2 I_{B1}} + \frac{V_{BE1}}{R_1 I_{B1}}\right) \qquad (3.7.3)$$

$$I_{B1} = I_B - \frac{V_{BE1}}{R_1} \qquad (3.7.4)$$

Replacing I_{B1} in (3.7.3) with the expression in (3.7.4) and solving for I_C/I_B concludes with equation (3.7.5)

$$\beta_{OVERALL} \quad \frac{I_C}{I_B} = \left[\beta_1 + \beta_1\beta_2 + \beta_2\left(1 - \frac{V_{BE2}}{R_2 I_B} + \frac{V_{BE1}}{R_1 I_B}\right)\right]\left(1 - \frac{V_{BE1}}{R_1 I_B}\right) \qquad (3.7.5)$$

This is the new expression for $\beta_{OVERALL}$ the effective d.c. current gain of the transistor pair. For an estimate of the old and new effective beta values for the resistances R_1 and R_2, the base-emitter voltages, V_{BE1} and V_{BE2}, the total base current I_B and the d.c. current gains β_1 and β_2 are provided below

$$R_1 = 30\Omega$$

$$R_2 = 11\Omega$$

$$V_{BE1} = V_{BE2} = 1^{VOLT}$$

$$I_B = 4 \text{ Amperes}$$

$$\beta_1 = \beta_2 = 10$$

The values for R_1, R_2, V_{BE1}, V_{BE2}, and I_B are taken directly from the circuit but β_1 and β_2 are only estimates which may appear somewhat arbitrary. Using these values the calculated overall betas without and with stabilization resistors are 120 and 118.8 respectively.

In summary the primary advantage of the Darlington power switch over single device power switches is the high gain which allows the designer to control a large output power with a lower power base drive. In the Westinghouse inverter project where a single transistor was utilized as the power switch the total current supplied by the base circuit was as much as twenty-six Amperes for a collector current of fifty Amps [3]. Part of the current supplied by the base circuit (about twenty Amps) flowed into the collector circuit through the base-collector diode of a Baker Clamp so that this portion of the current would not add to the power losses of the base drive. On the other hand, even with only the remaining six Amperes flowing into the base-emitter junction with an output of fifty Amperes the effective gain would be eight which is much less than the gain of a Darlington pair. In this project a base current

of four Amperes was adequate for current levels of one hundred and twenty-five Amperes [3].

3.8 Darlington Configuration's Collector-Emitter Saturation Voltage

A second advantage to using the transistors Q1 and Q2 as a direct coupled pair is related to the overall saturation voltage V_{CE2}. As previously stated, the collector-emitter voltage of the output device (V_{CE2}) is the sum of Q1's collector-emitter voltage (V_{CE1}) and Q2's base-emitter voltage (V_{BE2}) from Kirchoff's laws. As a result the driver transistor Q1 can be saturated but the power transistor Q2 remains in the quasi-saturated state due to its higher voltage drop from collector to emitter. It is advantageous to keep Q2 out of deep saturation so that its storage time is reduced. In equation (3.8.1) the limiting factor is V_{BE2} which is weakly dependent on base current I_{B2}. Conversely, the

$$V_{CE2(SAT)} = V_{CE1(SAT)} + V_{BE2} \qquad (3.8.1)$$

base current (I_{B2}) is strongly dependent on the base-emitter voltage (V_{BE2}). From one device to another the base-emitter voltage will exhibit very little parameter dispersion so that the potential V_{BE2} establishes a firm lower limit for the collector-emitter voltage (V_{CE2}) [4].

3.9 Storage Time Effects of the Darlington Configuration

The storage time of a Darlington configuration is usually long due to the fact that it stems from the storage time of a highly saturated driver and a quasi-saturated power device. It may be shorter than, the same as, or longer than the storage time of an identical power device operating in the saturated state. The storage time depends largely on the base and collector currents existing immediately prior to turn off both of which will be determined by the circuitry surrounding the transistor. Several circuit techniques exist to alleviate or shorten storage time effects in the Darlington configuration. Herewith is an explanation of the effects and some possible remedies. The definition of storage time is that time interval following the removal of forward base current (possibly simultaneous with the application of reverse base current) during which the device continues to operate with little or no change in collector current due to stored charge in the transistor. It makes sense, therefore, that following the removal of positive drive from the driver of the Darlington configuration the collector current of the driver would not change significantly during its storage time. It would still provide the same level of injection into the base of the power device. The power device would

be unable to turn off until this injection had subsided and thus the power transistor's storage time effect would not even begin to any considerable extent until the driver device's storage time had ended. This is exactly the case and can cause significant problems if the designer fails to consider or acknowledge this fact [4].

Several factors are involved in the reduction of storage time. The leakage stabilization resistances may also be used to supply low impedance paths through which excess charge can flow and be dissipated. The forced gain under which the driver operates may be increased by reducing the base current for a reduction in device storage time. The designer must be careful that the reduction in base current does not allow either device to pull out of saturation to the extent that power dissipation in the devices would be higher than maximum ratings.

3.10 Drive Methods - Employing a Negative Reverse Current

Application of a negative bias voltage to the effective base-emitter junction of the Darlington pair can increase the rate at which stored charge is evacuated from the devices. A standard figure of comparison is the ratio of reverse to forward current versus the device storage time [4]. Increasing the ratio or magnitude of reverse

base current to forward current accomplishes a significant reduction in storage time initially but usually becomes ineffective at reducing the storage time for high ratios. When a large amplitude reverse current flows with a corresponding high di_B/dt rate from the base, carriers are rapidly depleted from the base-emitter junction. The remaining charge is largely stored in the collector and base-collector regions. From the point in time where charge is depleted from the base-emitter junction to the time when all regions are free of excess charge the transistor will act like a slow diode undergoing reverse recovery so that the collector current decays very gradually. This phenomenon is commonly referred to as the current tailing problem during turn off. With this type of operation the device experiences simultaneous high current and high voltage during switching. Large power losses must occur within the device. The possible consequences are thermal instability, excessive power disspation, or the occurance of reverse bias second breakdown all of which can destroy the power switch. This should not imply that a fast reverse bias current is not necessary for fast proper turn off; it is meant only as a precautionary note regarding high reverse base currents [4].

There are several ways in which the negative bias at turn off can be applied to the two devices forming the Darlington. The first type of dual reverse drive turn off involves the use of negative bias on both base-emitter junctions (see Fig. 3.10.1a). The second type of single reverse drive turn off utilizes a diode connected anti-parallel to the base-emitter junction of Q1 (see Fig. 3.10.1b) to provide a path for current from the base of the power device Q2. This path is necessary because the driver device cuts off before much of the charge has been removed from the power device. Without the diode or the resistance, R_1, the only method of charge removal from the power device would be largely internal recombination which is a very graduate process. The presence of the diode insures that the reverse potential is applied to the power device after the driver turns off.

3.11 Drive Methods - A Comparison

Both methods of turn-off were compared on the D60ST-D7ST transistor pair hence the oscilloscope photographs shown on the next several pages provide some interesting results for the readers' perusal. The first two photographs (Figs. 3.11.1a and 3.11.1b) show the collector current, reverse base current and collector-emitter voltage for a single reverse drive and dual reverse drive

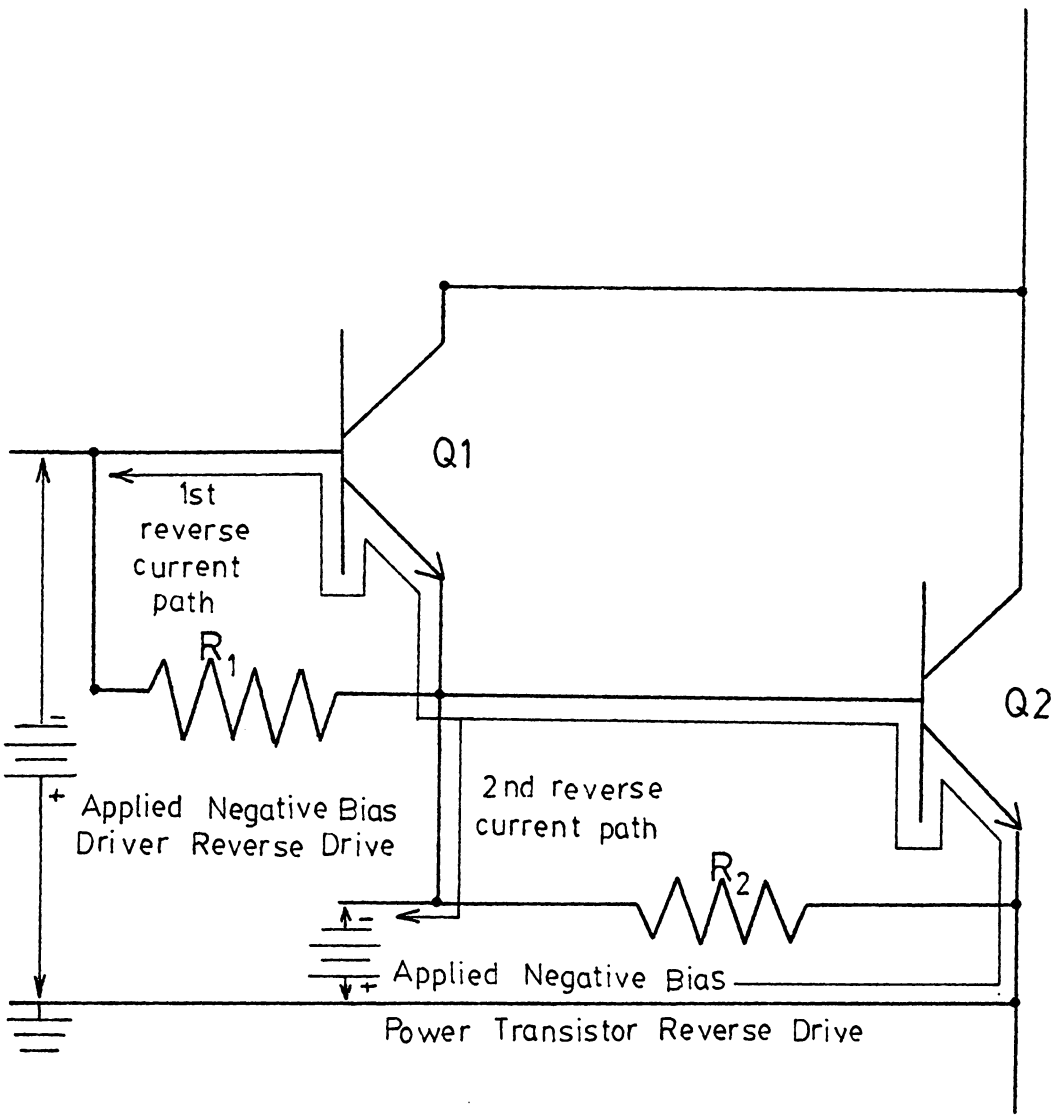


Figure 3.10.1a Dual Reverse Drive

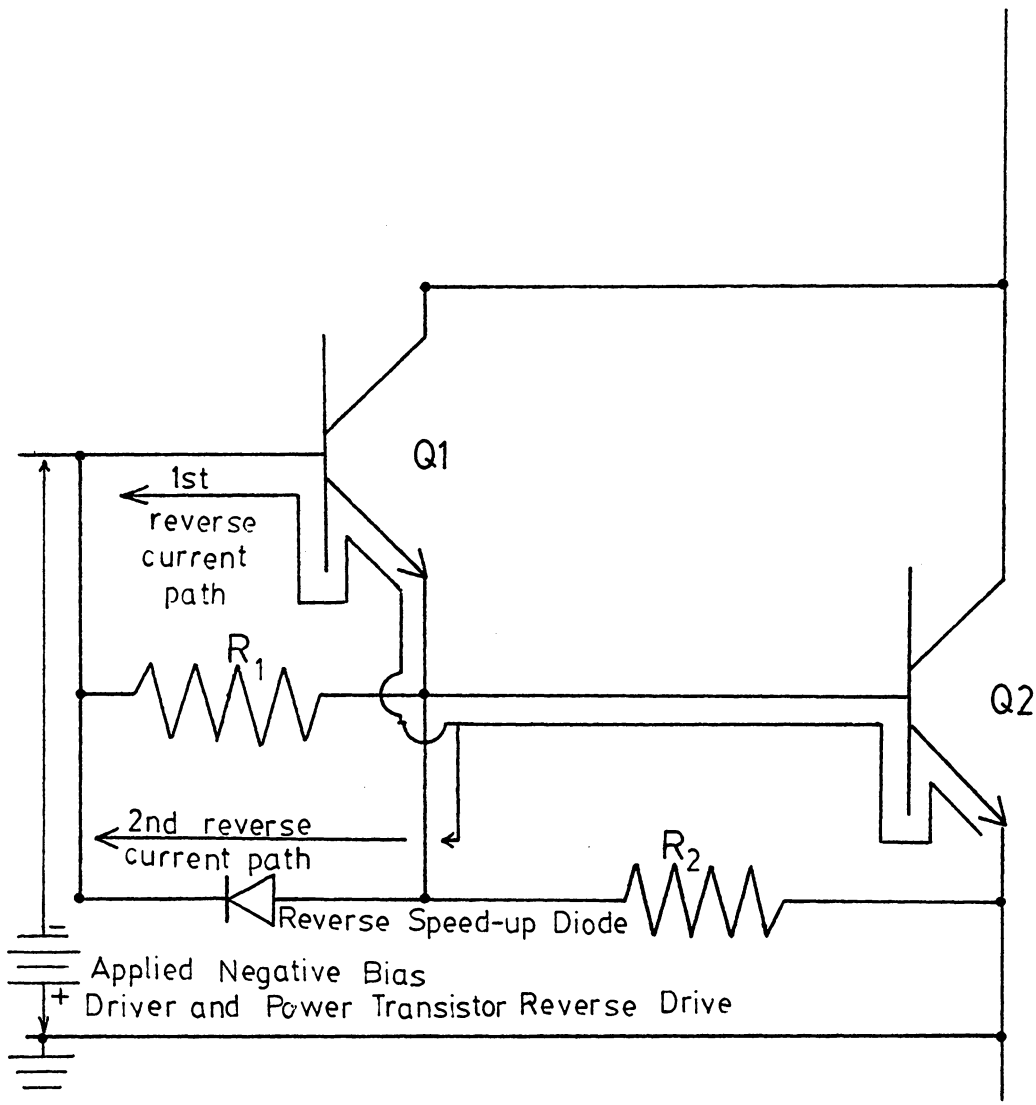
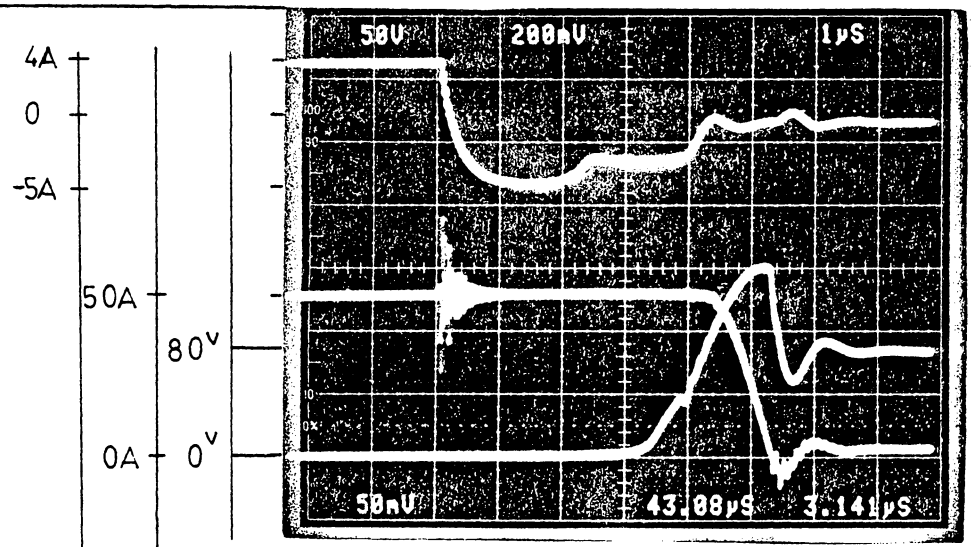
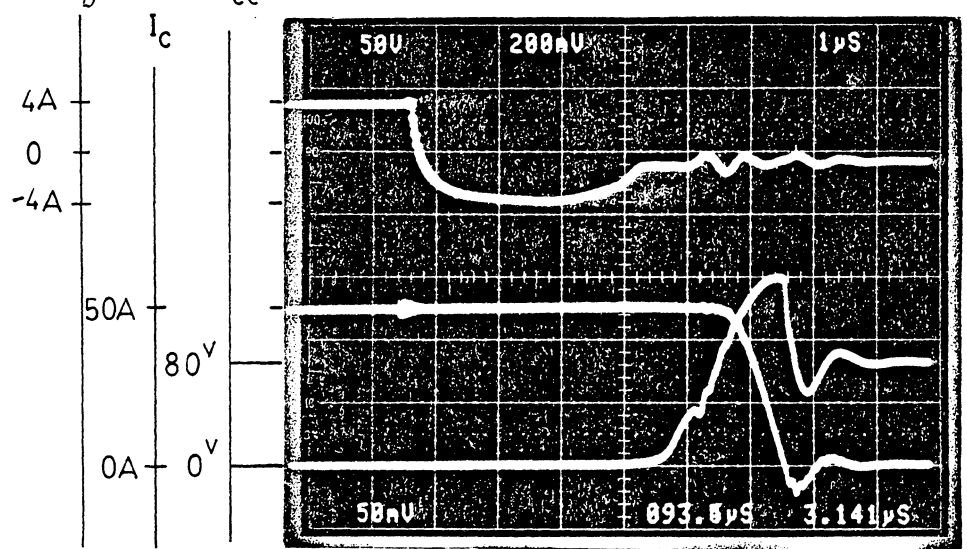


Figure 3.10.1b Single Reverse Drive
(with speed-up diode)



(a) SINGLE REVERSE DRIVE



(b) DUAL REVERSE DRIVE

Storage Time Comparison

(a) $T_S = 4.4\ \mu s$ (b) $T_S = 5.2 \mu s$

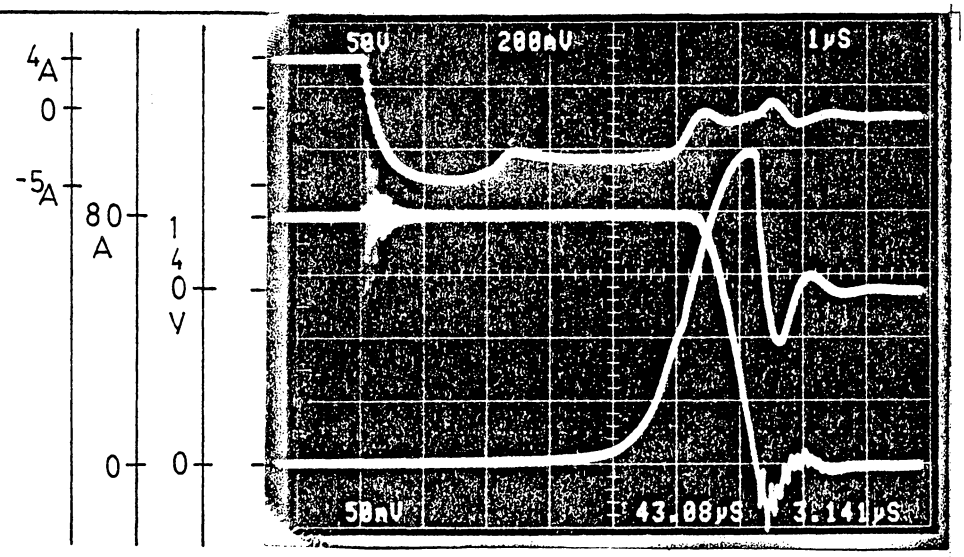
Figure 3.11.1 Single versus Dual Drive T_S Comparison (50 Amperes I_C)

respectively. The first photo (Fig. 3.11.1a) resulted in a storage time of 4.4 microseconds for a collector current of fifty Amperes and a collector-emitter voltage of eighty Volts. A forward drive current of four Amperes was employed so that upon application of reverse drive the D60T device was very saturated. The reverse bias potential of seven Volts applied to the two devices resulted in a reverse base current of five Amperes. Seven Volts were chosen as the applied voltage since it was the maximum voltage which the emitter-base junction of the power device could sustain without avalanching.

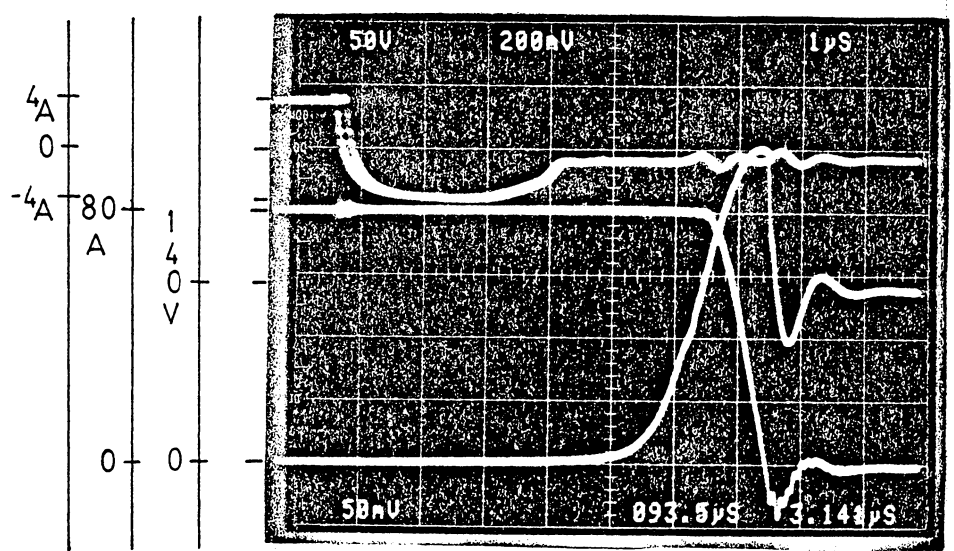
There are two distinct reverse current levels during the storage time. The primary level which lasts for 2.4 microseconds corresponds to the interval when charge is removed from the driver device and the power device. The reverse current path during this interval is through the emitter-base junctions of the two transistors (review Fig. 3.10.1b). The smaller secondary reverse current level which occurs as the driver turns off conforms to the removal of charge from the power device through the reverse speed-up diode. Note that the secondary current level lasted approximately 2 microseconds indicating that the contributions to the overall storage time was roughly the same for both devices.

The second photograph (Fig. 3.11.1b) for a dual reverse drive exhibits a 5.2 microsecond storage time which is slightly greater than the single reverse drive storage time. All the conditions were identical to those employed in the single reverse drive circuit; however, in this case, the seven Volt negative bias voltage was applied to both base-emitter junctions at turn off. The reverse current measured at the base of the driver transistor was not as negative as the reverse current obtained using a single reverse drive; this is possibly because the drive was not great enough when applied to both transistors since both reverse currents were provided by the same negative bias source. The end result was a much longer storage time for the driver device.

Photographs taken at higher collector current (Figs. 3.11.2a and 3.11.2b) indicated that it is the time interval of the secondary reverse current (power transistor storage time) which expands in duration as the total collector current is increased. This implies that the power device becomes more deeply saturated as the current level is increased. Furthermore, the power device must be more saturated because the drive device collector current constitutes a greater portion of the total collector current which it, in turn, injects into the base of the power device



(a) SINGLE REVERSE DRIVE



(b) DUAL REVERSE DRIVE

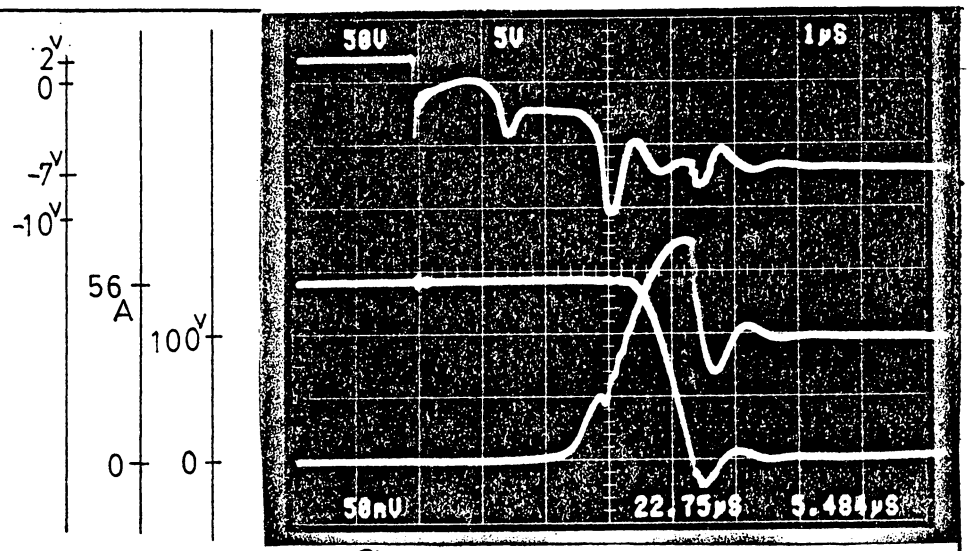
Storage Time Comparison

(a) $T_S = 5.4\mu s$ (b) $T_S = 5.8\mu s$.

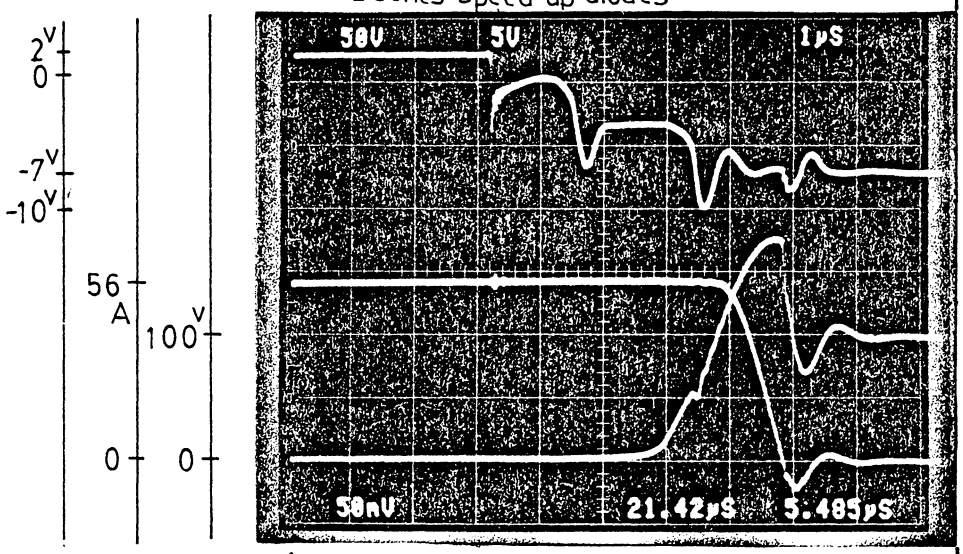
Figure 3.11.2 Single versus Dual Drive T_S Comparison (80 Amperes I_c)

D7ST. Again the photographs at collector currents of eighty Amperes show that the storage time is shorter for a single reverse drive with speed-up diode. In this case 5.4 microseconds compared to 5.8 microseconds for the dual reverse drive. Difficulty in obtaining a relatively short storage time utilizing a dual reverse drive led to the choice of the more conventional single drive with a speed-up diode.

The choice of a single drive scheme provided a good compromise between drive complexity and fast device turn off. Additionally, the designer has some flexibility in the number of anti-parallel diodes employed in the single drive Darlington configuration. The speed-up diode turns on as the driver device turns off and provides a negative bias of a diode drop to the driver's base-emitter junction. Increasing the number of anti-parallel diodes placed in series increases the reverse bias providing a more dynamic turn off of the driver transistor. The internal construction of the transistor makes it a somewhat distributed device so that larger reverse bias voltages prevent dv/dt turn on of the central portion of the transistor. Several empirical measurements with two and three speed-up diodes are presented (Figs. 3.11.3a, 3.11.3b, 3.11.4a, and 3.11.4b). The results of these comparisons indicate a choice of two anti-parallel diodes would minimize the Darlington devices'



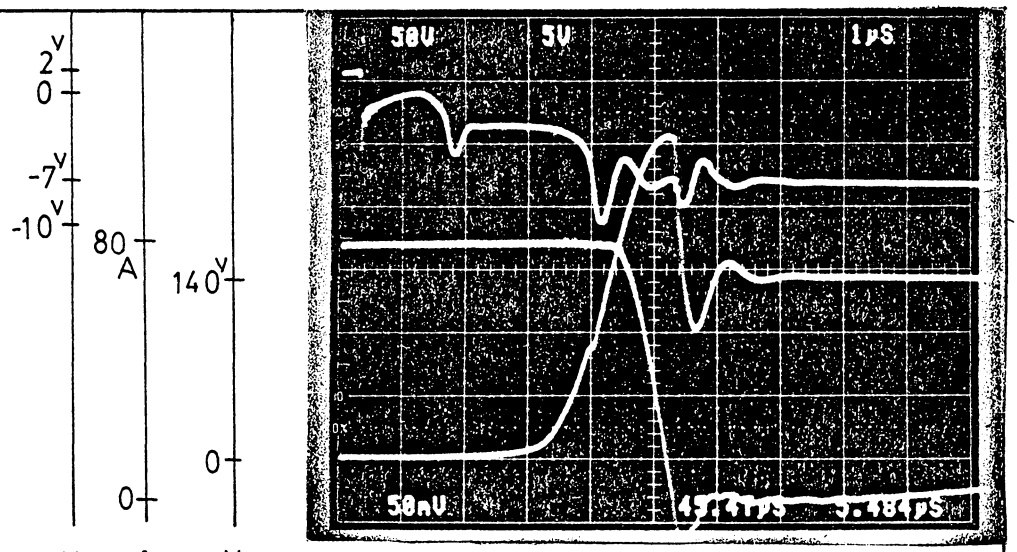
(a) Single reverse drive
2 series speed-up diodes



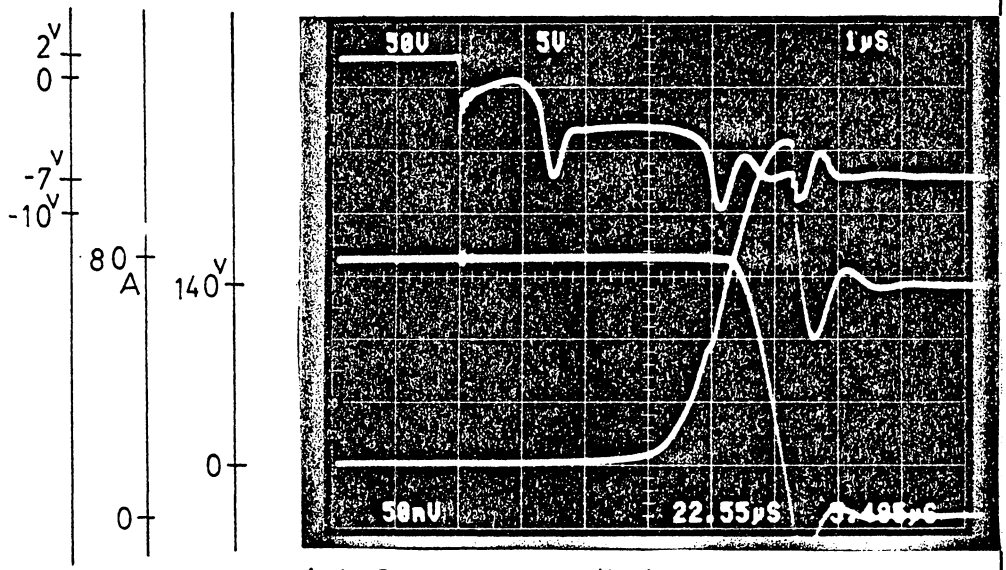
(b) Single reverse drive
3 series speed-up diodes

Storage Time Comparison
(a) T_S= 3.4μs (b) T_S=3.5μs

Figure 3.13.3 Single Drive, Series Speed-up Diodes
Storage Time Comparison (56 Amperes)



(a) 2 speed-up diodes



(b) 3 speed-up diodes

Storage Time Comparison
(a) T_S = 4μs (b) T_S = 4.3μs

Figure 3.13.4 Single Drive, Series Speed-up Diodes
Storage Time Comparison (80 Amperes)

storage time effects. The storage time comparison for one, two, and three series speed-up diodes at a collector current of eighty Amperes produced storage times of 5.4, 4, and 4.3 microseconds respectively.

3.12 The Base Drive Circuit

The base drive circuitry and components specified for each Darlington power switch are shown in Figure 3.12.1 and Table 3.12.1. At the extreme left of Figure 3.12.1 the optical coupler HP2601 provides conductive isolation between the logic functions and the transistors' base drives which are d.c. coupled to the power circuit. An optical isolator was employed instead of more bulky, less efficient transformer methods. The initial opto-coupler used, an MCL 611 proved to be much less noise immune than the Hewlett Packard isolator finally chosen. The major differences between the two couplers were in the method of internal isolation and the type of output devices employed. The General Instrument part contained an internal Schmidt Trigger circuit and an open collector transistor output [19]. On the other hand, the HP2601 utilized an internal Faraday shield and a Schottky transistor output device [20]. These characteristics combined to provide the HP product with superior response time and noise immunity.

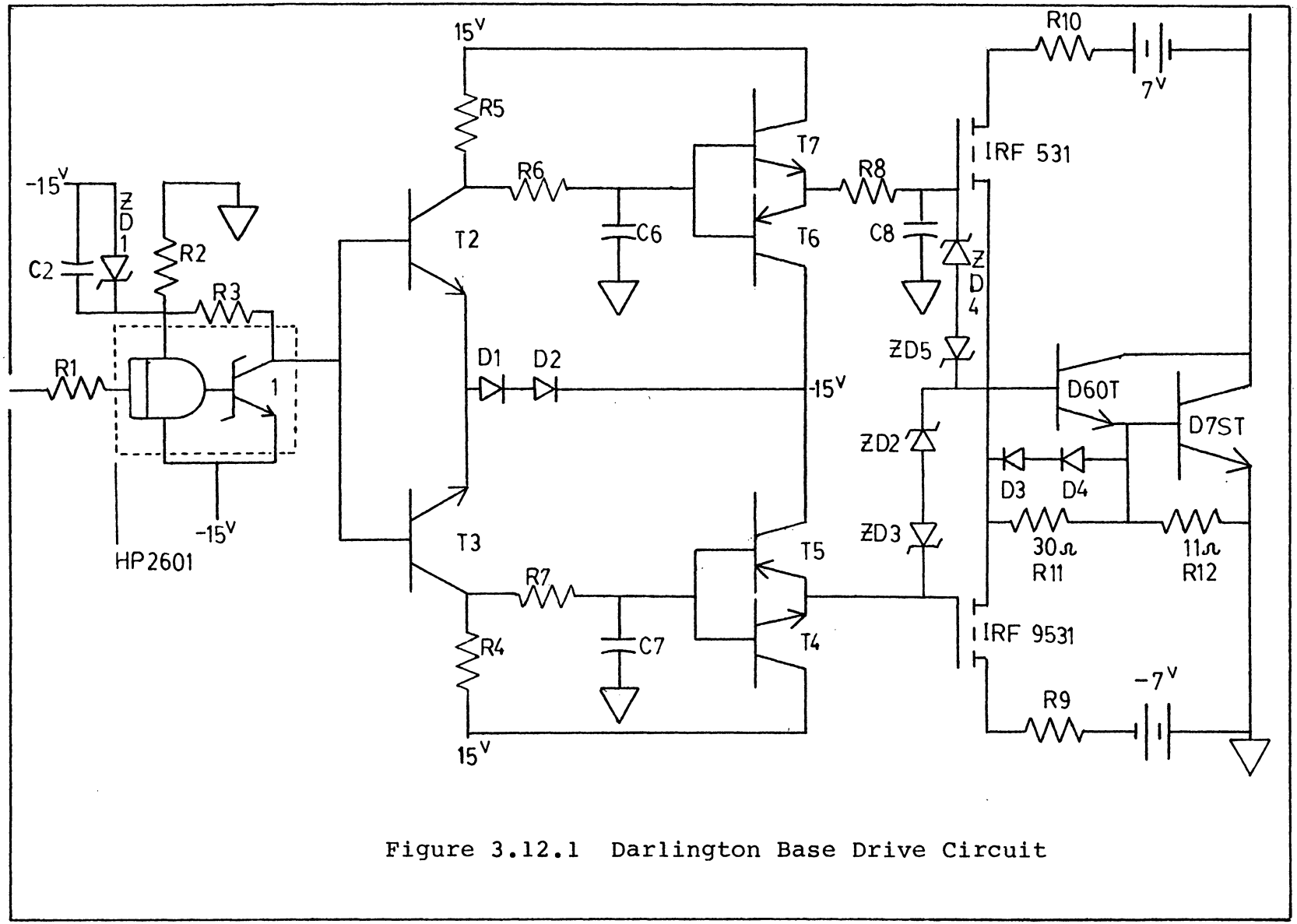


Figure 3.12.1 Darlington Base Drive Circuit

TABLE 3.12.1

Component Values for the Darlington Base Drive Circuit
(All resistances are rated ¼ Watt, 5% unless otherwise specified)

R1	360Ω	HP2601 OPTOCOUPLER	
R2	180Ω	ZD1	4.7^{V} Zener Diode
R3	510Ω	C2	22 ufd 25^{V} tantalum
T2,T3	TCG 161	npn switching transistor	
R4,R5	1.8 kΩ	½ Watt	
R6,R7	1.6 kΩ		
C6,C7	87.6 pfd		
T4,T7	mm5262	npn switching transistor	
T5,T6	mm3726	pnp switching transistor	
R8	680Ω		
C8	130 pfd		
Zd2,Zd3,Zd4,Zd5		18^{V} Zener Diode 1N4746A	
R9	½Ω	1 Watt	
R10	11/6	24 Watts (6 11Ω 4 Watt noninductive resistors)	
D1,D2	Rectifier Diodes		
D3,D4	Fast Recovery Diodes	A114F	
R11	30Ω	1 Watt	
R12	11Ω	4 Watts	

A 4.7 Volt zener diode network (ZD1, C2, R2) is used to provide the supply voltage for the optical coupler so that the unloaded output voltage varies between negative ten and negative fifteen Volts. The open collector output of the Schottky transistor (pulled up through a 510 Ohm resistor R3) is coupled into the bases of identical npn switching transistors connected to the positive fifteen volt supply through the resistors R5 and R4. In turn the outputs of the transistors T2 and T3 are low pass filtered using the networks (R6,C6) and (R7,C7). The diodes D1 and D2 ensure that the transistors T2 and T3 remain off when the output of the optical coupler is negative fifteen Volts. In addition the diodes increase the noise margin of the transistors.

The transistor pairs (T7,T6) and (T5,T4) are complementary emitter followers. Initially two stages of emitter followers were used to provide current gain. The high gain provided substantial amplification for circuit noise created by switching transients in the power circuit. To alleviate this problem the number of current amplifier stages was reduced to a single stage for the forward and reverse drives. The resistor-capacitor network at the output of (T6,T7) coupled with the internal capacitance of the FET IRF531 provides a slower voltage rise at the gate of the FET at

turn on. In this case a compromise must be reached between the requirements of a fast turn on for the Darlington pair and oscillations caused by stray inductance in the forward drive current path. The zener diodes (ZD4,ZD5) and (ZD2, ZD3) provide transient protection to the gates of the FETs. Transient voltages of twenty Volts between the gate and the source can cause pinholes in the silicon oxide insulating layer. The zener diodes provide a low impedance conductive path to voltages greater than 18.7 Volts. Finally the power resistor R10 and resistor R9 perform current limiting in the output circuit of the base drive. R9 with a value of 1/4 ohm more appropriately damps oscillations excited by stray reactances at turn off while R10 and the internal resistance of the FET IRF531 provide a means of controlling the forward current and, therefore, the forced gain B_f. The photographs (3.12.2 and 3.12.3) show the measured base-emitter voltage and base current provided by the drive circuit. These photographs were taken at several collector current levels so that the magnitude and duration of the reverse current varies. It should be noted that the forward and reverse drive are arranged in a symmetrical push-pull arrangement. Either the n-channel FET IRF531 will be on providing forward drive or the p-channel FET IRF531 will be on providing reverse drive to the Darlington pair.

The photographs taken at low collector current levels (Fig. 3.12.2) have reverse currents which are very sharp and short in duration. Under the initial application of negative bias (see Figs. 3.12.3 and 3.12.4) the measured voltage at the base-emitter terminals remains positive. During this time interval the forward current falls and reverses finally reaching a peak value of negative ten Amperes. The time rate of change of the base current from t_0 to t_1 (Fig. 3.12.3f) is approximately negative twenty Amperes per microsecond so that the di/dt effect multiplied by a stray inductance of perhaps one hundred nanohenries lessens the applied reverse bias voltage drop across the 1/4 ohm damping resistor (Rg) and the drop across the p-channel FET($R_{DS(on)}$ = .25 ohms) becomes significant so that the applied reverse bias is reduced by five Volts. As the driver transistor begins to turn off from t_1 to t_2 the reverse current begins to decrease quite rapidly causing a di/dt of positive twenty Amperes per microsecond so that the applied reverse drive is temporarily increased causing an increase in the measured reverse bias on the base-emitter of the Darlington. During the interval t_2 to t_3 the secondary reverse current begins to flow through the emitter-base junction of the power stage and the speed-up diodes and once again, the voltage drop across R9 and the FET become

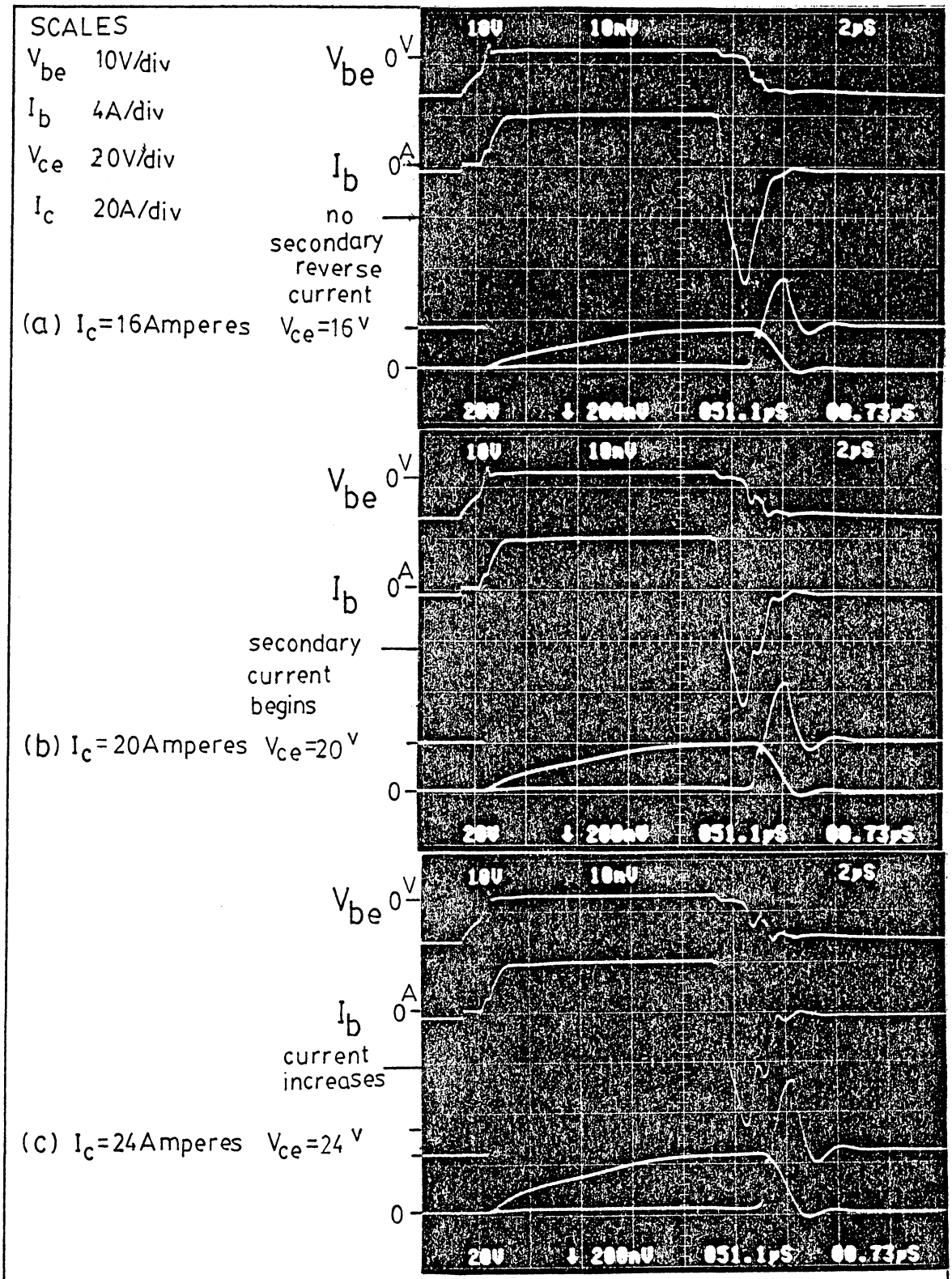


Figure 3.12.2 Base Emitter Voltage & Base Current

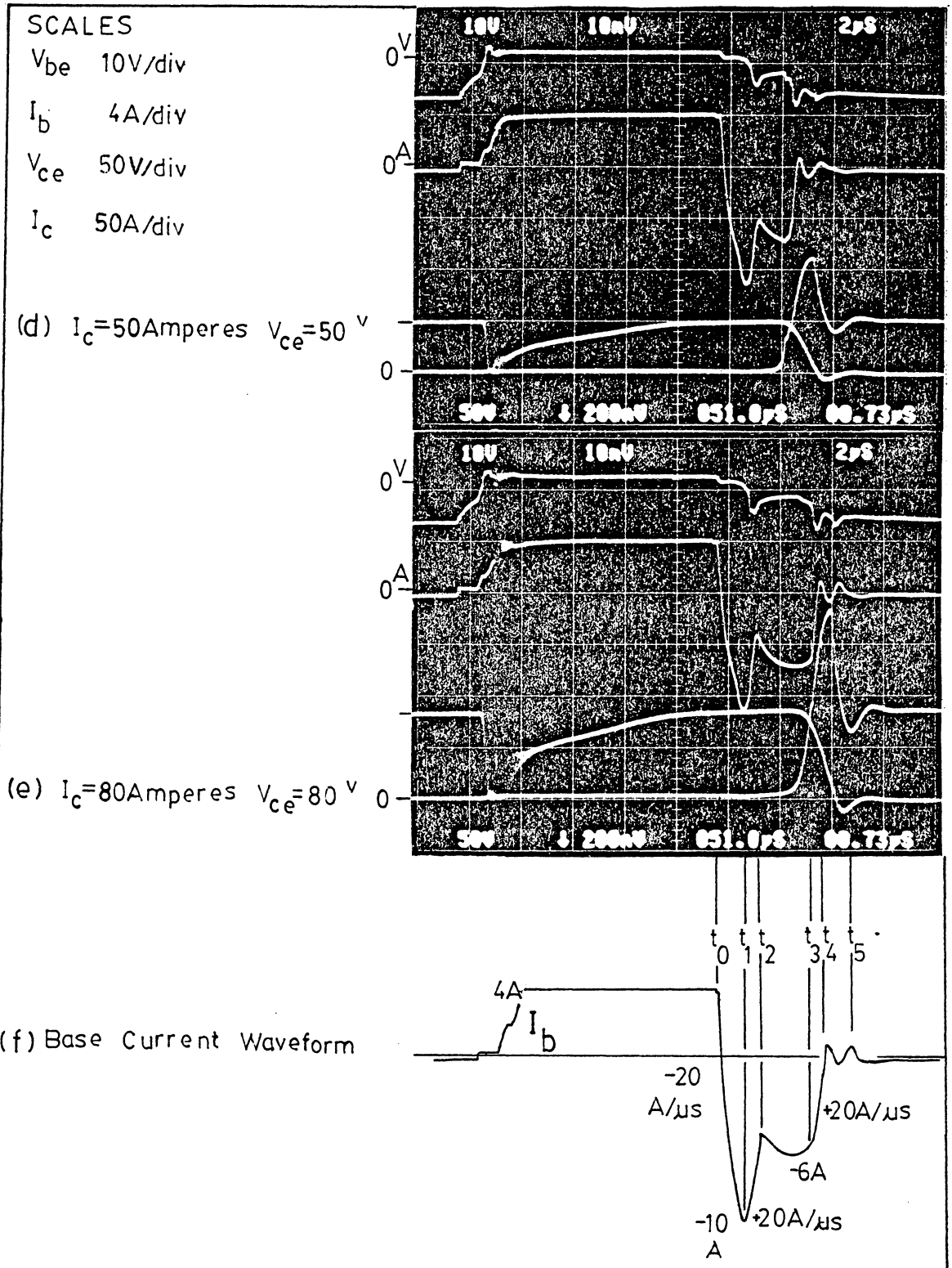


Figure 3.12.3 Base Emitter Voltage & Base Current

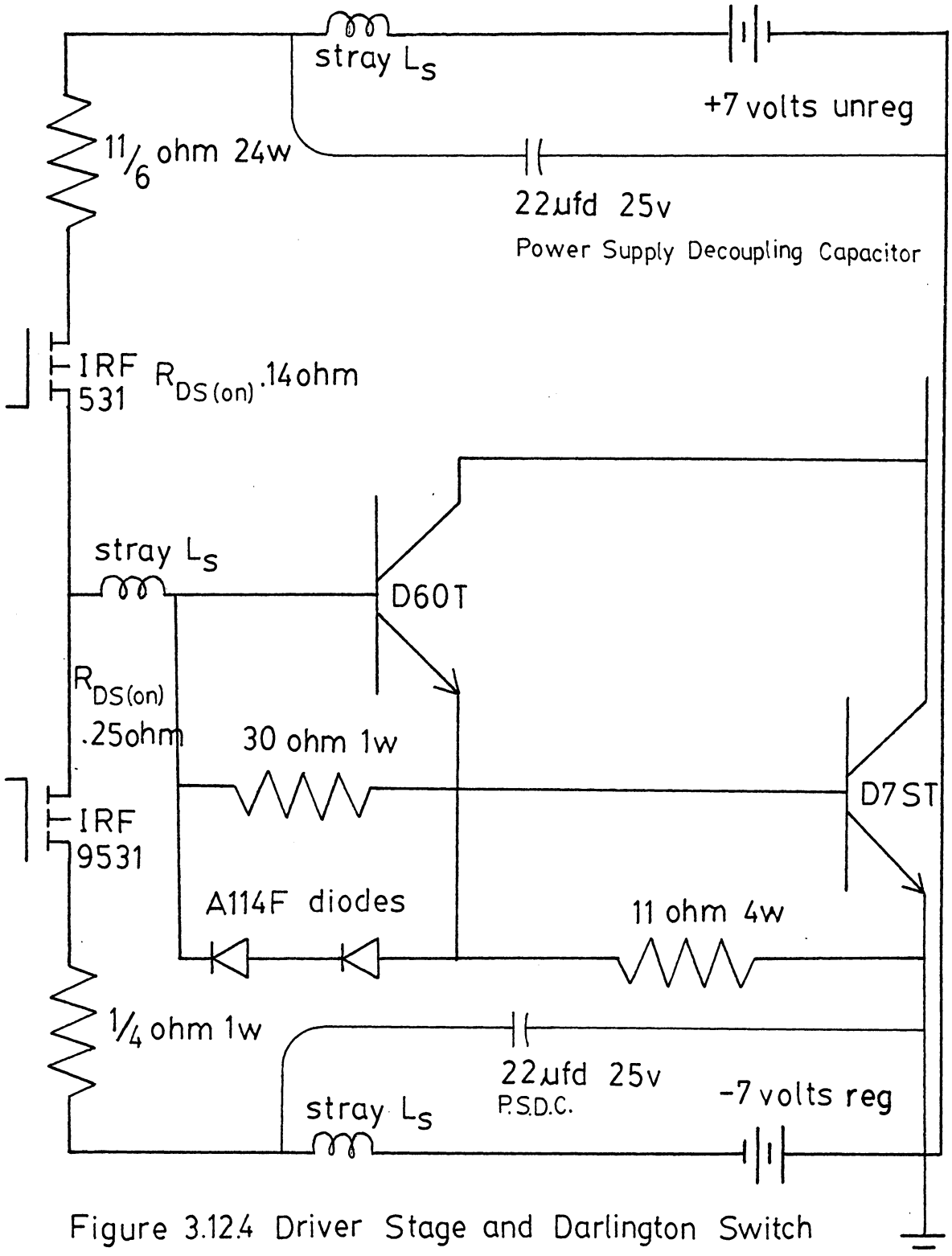


Figure 3.12.4 Driver Stage and Darlington Switch

important. As the power device D7ST turns off from t_3 to t_4, the reverse current decreases quite rapidly causing a similar di/dt induced increase in the reverse bias as that caused when the driver turns off. The end result is a second temporary increase in the reverse bias measured at the base-emitter terminals of the Darlington pair. Finally at t_5 the two transistors are turned completely off, applying the full reverse bias voltage of seven Volts to the two devices. A small reverse current of about half an Ampere flows through the anti-parallel speed-up diodes and the base-emitter leakage stabilization resistor of the power device.

The photographs taken at the higher collector currents of fifty and eighty Amperes (Fig. 3.12.3) provide the same sort of information as the low current photographs. In addition, they provide some visualization of when the storage time of the power device begins to become significant. At approximately twenty Amperes (Fig. 3.12.2) the secondary current level begins to appear indicating the presence of stored charge in the power device. At fifty Amperes (Fig. 3.12.3) the two devices forming the Darlington contribute equally to the storage time and at eighty Amperes the power device D7ST has a much greater storage time than the drive device D60T.

3.13 Switching Stress - The Snubber Network

The circuit component selection would be incomplete without some form of stress relief network. Snubbers, as they are more commonly referred to, provide several tangible benefits in switching circuits. Farraro enumerates a list of five prevalent snubber functions in power switching [18]. First, the networks are capable of transferring the energy loss during switching away from the power device. Second, snubbers are useful for overvoltage suppression especially the extreme voltage transients created when the current through an inductive reactance is interrupted or switched. Third, snubbers are employed to limit the rate of rise of voltage and current. Fourth, secondary breakdown can be avoided since the snubber circuits insure that the device is kept within the safe operating area. Finally, snubber networks help to abate noise and electromagnetic interference normally generated in the power circuit.

Three different types of snubbering were compared for the bridge inverter circuit application. Several papers call attention to the pitfalls involved in applying polarized snubbers in the full-bridge configuration [4,9]. In this case, however, both polarized Resistor-Capacitor-Diode and non-polarized Resistor-Capacitor circuits were tested on a single Darlington power switch. Additionally, a Resistor-

Capacitor-Active Voltage Clamp circuit was developed for consideration as the stress relief network. The RC portion of the circuit would control the voltage rise during turn-off while the voltage clamp would clip the voltage transients at a present level. Both parts of the network would transfer the switching power losses at turn off away from the Darlington. Figure 3.13.1 shows the fairly simple network used to test the RC and RCD snubbers.

At turn off, the inductive nature of the load maintains the current flow into the power device. The load current is commutated from the power switch to the reverse free wheeling diode only after the collector emitter voltage V_{CE} rises slightly above the supply voltage level. When the diode begins to conduct, the current through the power switch begins to decrease. Generally, however, the collector emitter voltage continues to rise due to stray inductance in the power circuit. The stray inductance, which can be as small as ten nanohenries or as large as several microhenries, can cause substantial voltage overshoot at the terminals of the power switch. This voltage overshoot obtains its maximum value at the inflection point of the falling collector current. By placing a capacitor or the series combination of a diode and a capacitor in parallel with the power device, the total current flowing into the

power switch-snubber combination remains the same as without the snubber. Nevertheless, the capacitor acts to limit the rate of rise of collector-emitter voltage and acts to shunt current from the transistor since its current is proportional to the time rate of change of the collector-emitter voltage. This means that the transistor will not experience simultaneous high voltage and high current during turn off and this is the underlying principle behind the operation of the snubber network. The determination of element values for a snubber circuit is often empirical and, in this case, Figures 3.13.2a, 3.13.2b, and 3.13.2c provide a comparison of the snubbering abilities of both RC and RCD snubbers for three different values of capacitance. The RCD circuit can be analyzed to explain the different portions of each waveform. The equivalent circuits are provided (Fig. 3.13.3) from the optimum snubber circuits paper of Pearson and Sen [9].

Initially, there are three basic portions of the turn off voltage waveform. The first portion begins when the transistor is switched off. The time derivative of the collector voltage is linear and so is the current through the snubber capacitor. When the collector voltage reaches the supply voltage level, the free wheeling diode is forward biased and begins to conduct. Starting at this point

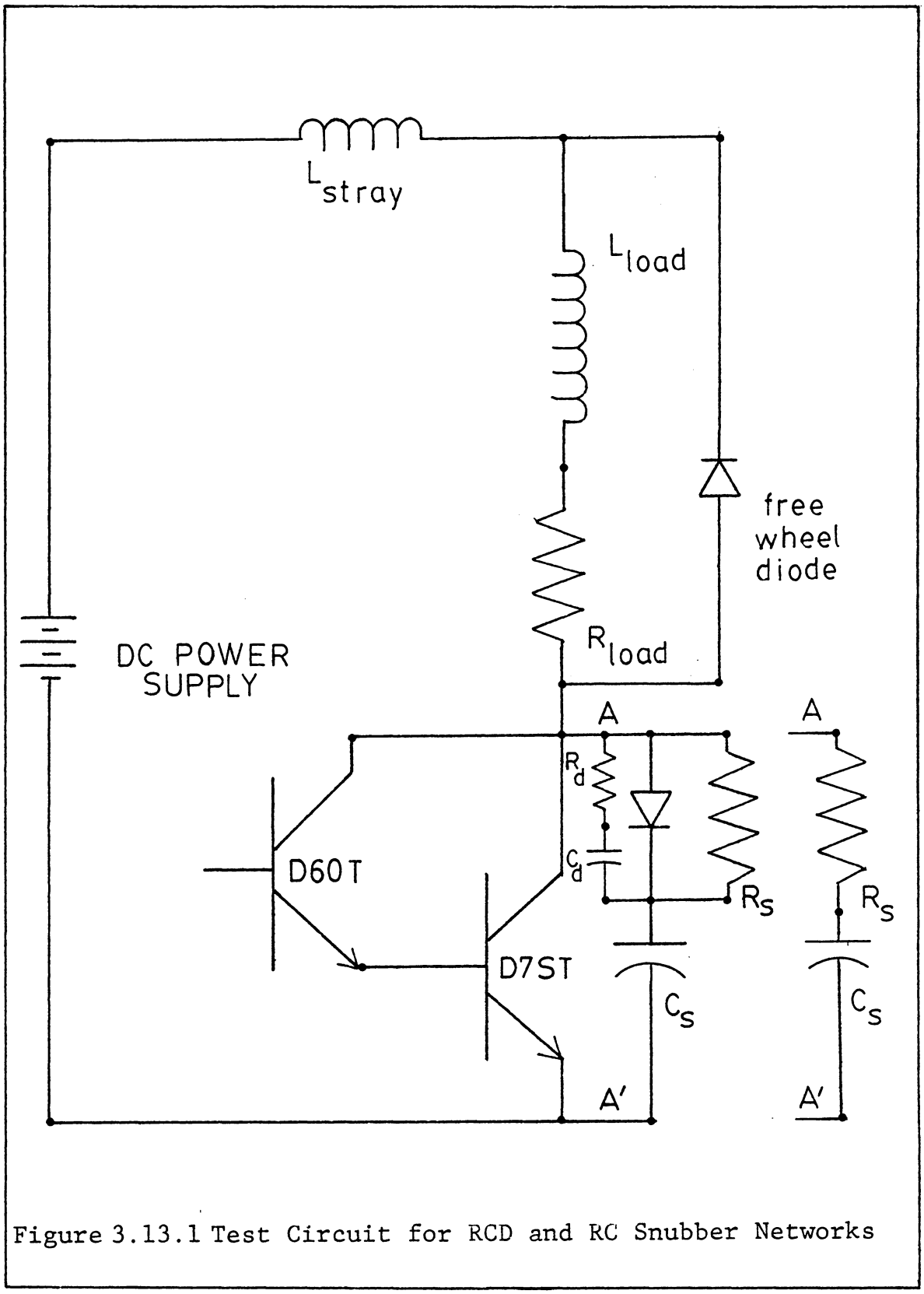


Figure 3.13.1 Test Circuit for RCD and RC Snubber Networks

ELEMENT VALUES

$R_{Snubber} = 50\,\Omega$

$C_{Snubber} = .3\,\mu fd$

Diode = 70hfl

ENERGY STORAGE

$\frac{1}{2}CV^2 = E$

$V = 100^V$ $E = 1.5 \times 10^{-3}$ Joules

$V = 200^V$ $E = 6 \times 10^{-3}$ J

$V = 300^V$ $E = 13.5 \times 10^{-3}$ J

POWER DISSIPATION of R_S

$\frac{1}{2}CV^2F = E \times$ Frequency $= P$

Frequency = 30 kilohertz

$V = 100^V$ P = 45 Watts

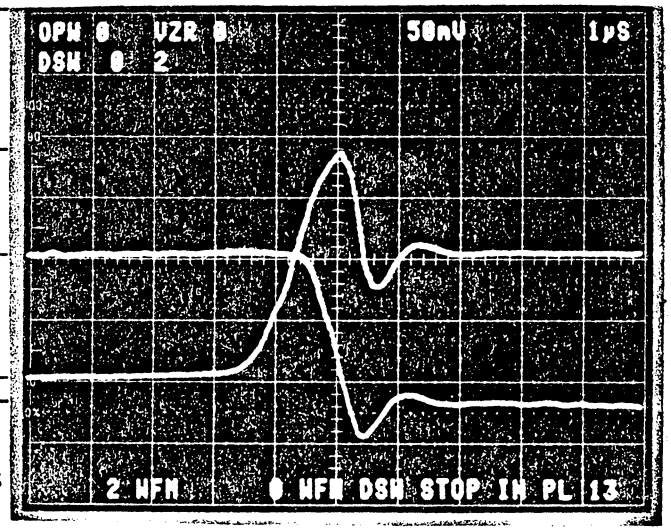
$V = 200^V$ P = 180 W

$V = 300^V$ P = 375 W

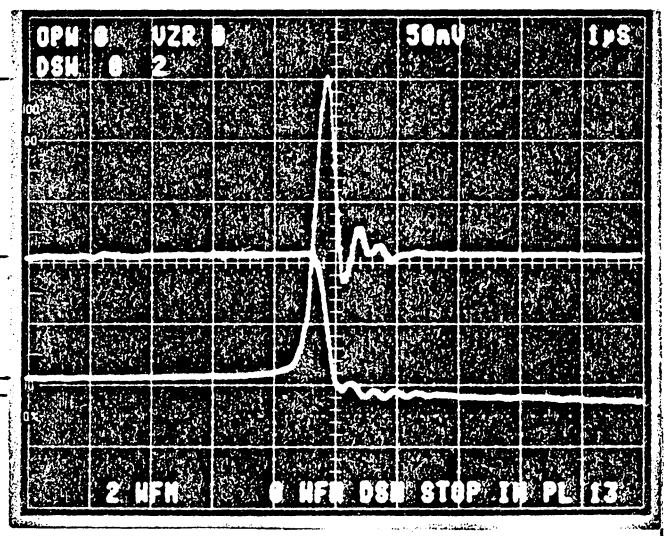
SCALES

Current 20 Amps/div

Voltage 50 Volts/div



(a) Resistor-Capacitor-Diode



(b) Resistor-Capacitor

Peak Voltage	V_{ce}
(a) 180^V	(b) 250^V

Figure 3.13.2a RCD&RC Snubber Networks ($C_S = .3\mu fd$)

ELEMENT VALUES

$R_{Snubber} = 50$

$C_{Snubber} = 0.2\,\mu fd$

Diode = 70 hfl

ENERGY STORAGE

$\frac{1}{2} C V^2 = E$

$V = 100^V \quad E = 1 \times 10^{-3} J$

$V = 200^V \quad E = 4 \times 10^{-3} J$

$V = 300^V \quad E = 9 \times 10^{-3} J$

POWER DISSIPATION of R_s

$\frac{1}{2} C V^2 \times F = E \times Freq = P$

Frequency = 30 kh_z

$V = 100^V \quad P = 30$ Watts

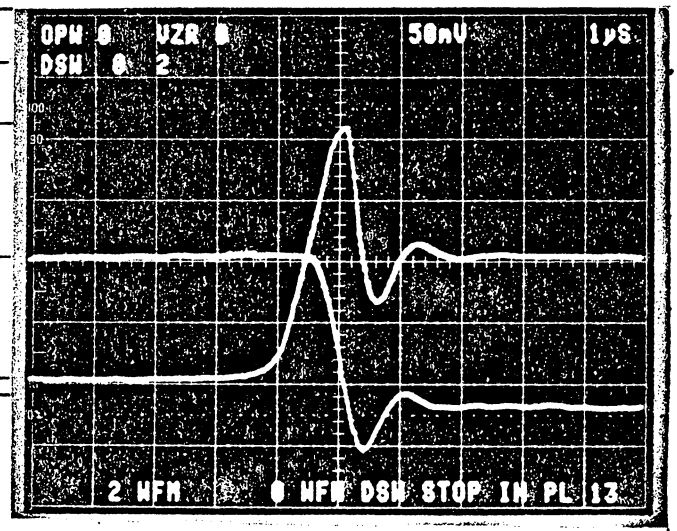
$V = 200^V \quad P = 120$ W

$V = 300^V \quad P = 250$ W

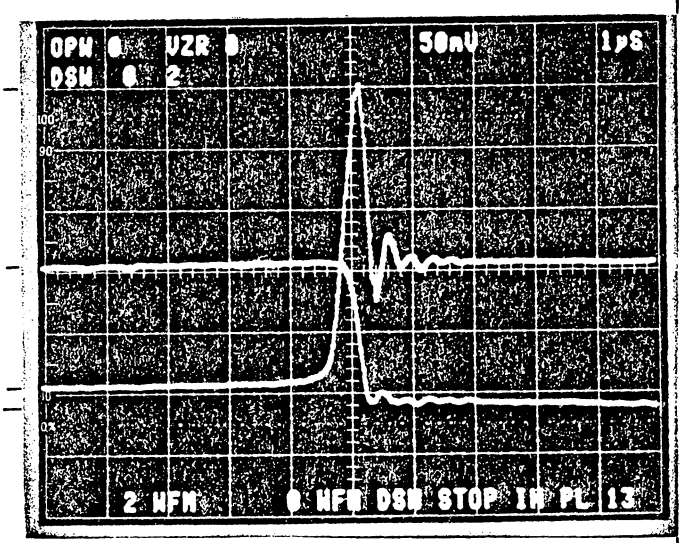
SCALES

Current 20 Amps/div

Voltage 50 Volts/div



(a) Resistor-Capacitor-Diode



(b) Resistor-Capacitor

Peak Voltage	V_{ce}
(a) 210^V	(b) 250^V

Figure 3.13.2b RCD&RC Snubber Networks (C_S=.2μfd)

ELEMENT VALUES

$R_{Snubber} = 50\,\Omega$

$C_{Snubber} = 0.1\,\mu fd$

Diode = 70 hfl

ENERGY STORAGE

$\frac{1}{2}CV^2$ E

$V = 100^V$ $E = 5 \times 10^{-4}$ J

$V = 200^V$ $E = 2 \times 10^{-3}$ J

$V = 300^V$ $E = 4.5 \times 10^{-3}$ J

POWER DISSIPATION of R_S

$\frac{1}{2}CV^2 \times F = E \times Freq = P$

Frequency 30 kh_z

$V = 100^V$ P = 15 Watts

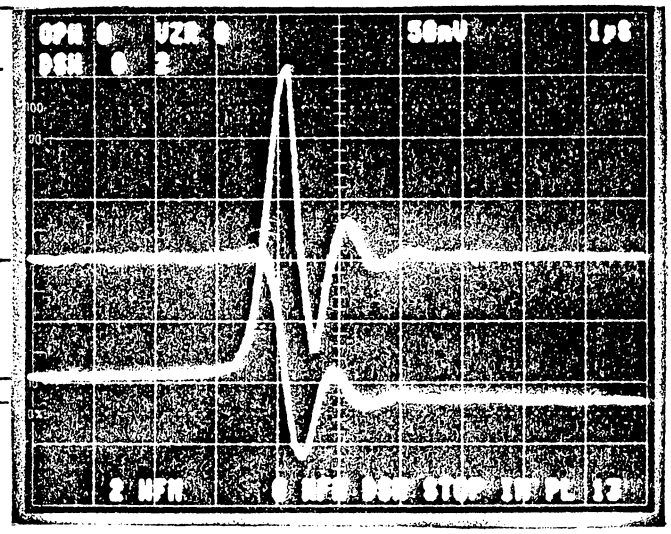
$V = 200^V$ P = 60 w

$V = 300^V$ P = 125 w

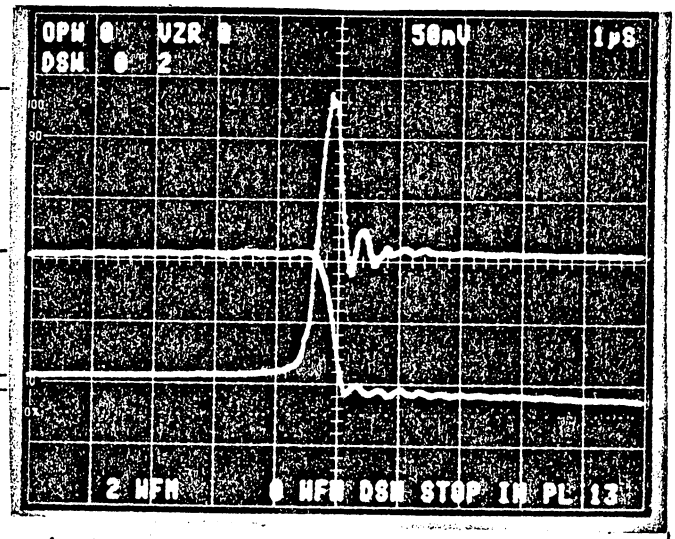
SCALES

Current 20 Amps/div

Voltage 50 Volts/div



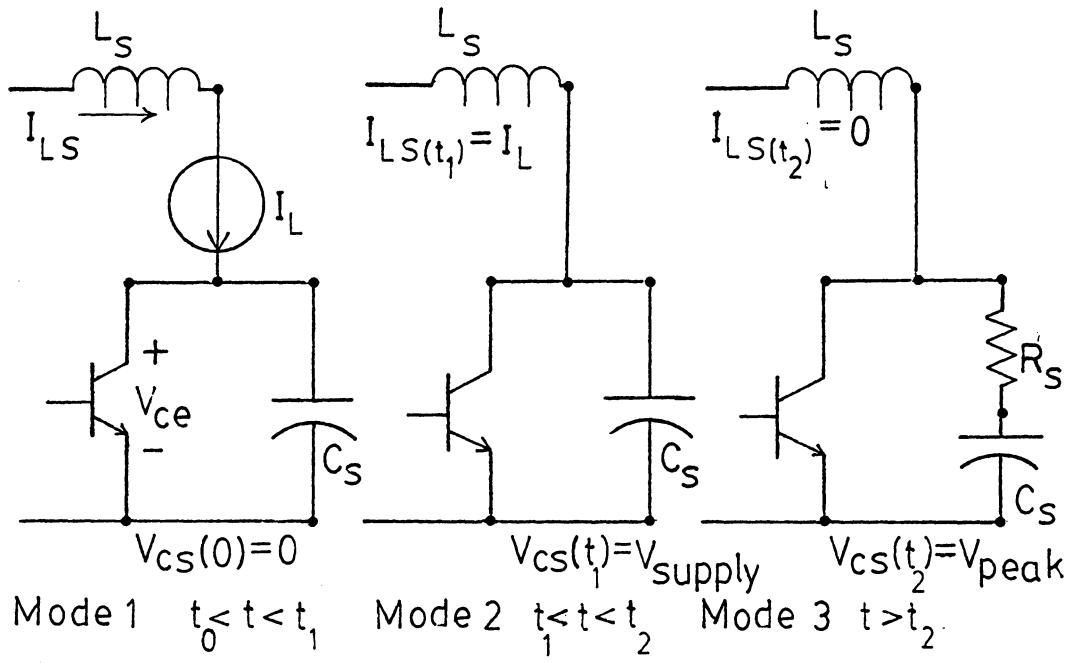
(a) Resistor-Capacitor-Diode



(b) Resistor-Capacitor

Peak Voltage V_{ce}	
(a) 260^V	(b) 240^V

Figure 3.13.2c RCD&RC Snubber Networks $C_S = .1\,ufd$



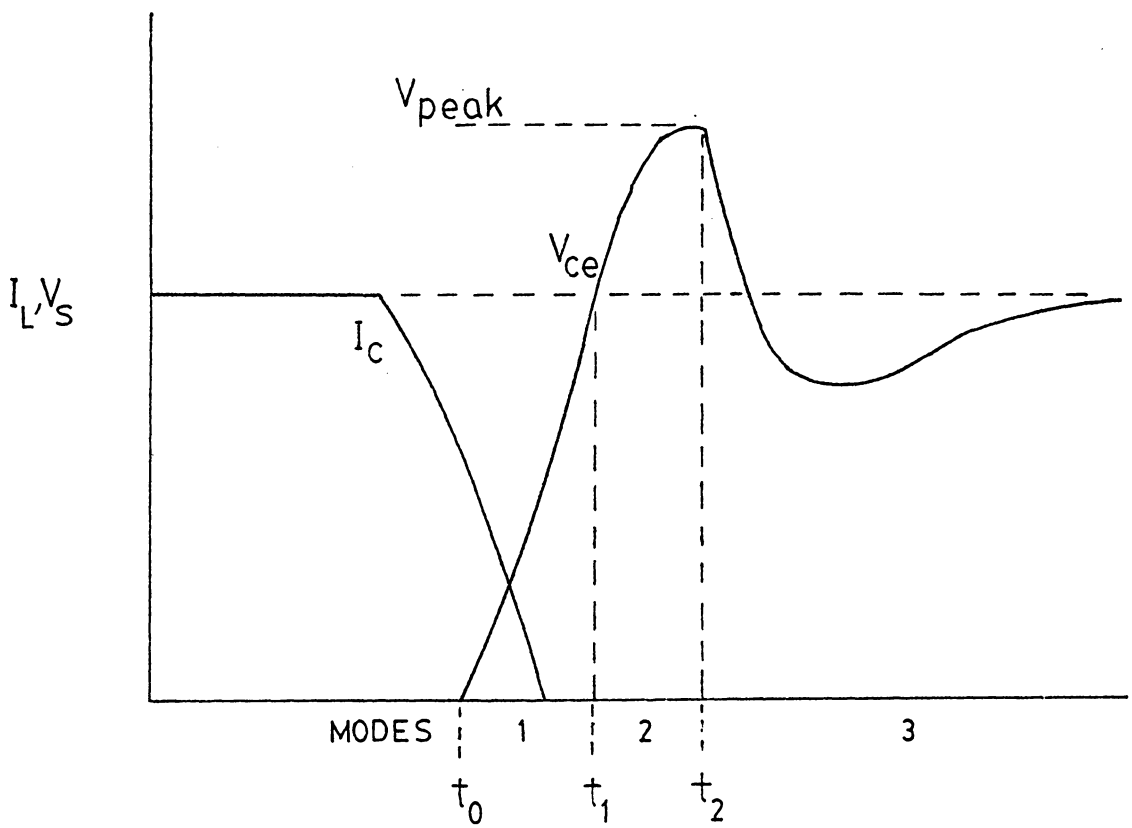


Figure 3.13.3 Resistor-Capacitor-Diode Equivalent Circuits

($t = t_1$) the snubber capacitor voltage is charged like an LC circuit with an initial current equal to the full load current through the stray inductance L_s and an initial capacitor voltage equal to the supply voltage. The equations 3.13.1 - 3.13.8 describing the circuit are shown below:

$$V_{SUPPLY} = L_s \frac{di_L}{dt} + \frac{1}{c_s} \int i_L dt + V_{cs}(0)$$

$$0 = L_s \frac{d^2 i_L}{dt^2} + \frac{1}{c_s} i_L \qquad (3.13.2)$$

$$i_L = A \cos \omega t + B \sin \omega t \quad \text{where } \omega = \frac{1}{L_s C_s} \qquad (3.13.3)$$

$$i_L(0) = i_L \qquad V_{CS}(0) = V_{SUPPLY} \qquad (3.13.4)$$

$$i_L = i_L \cos \frac{1}{L_s C_s} t \qquad (3.13.5)$$

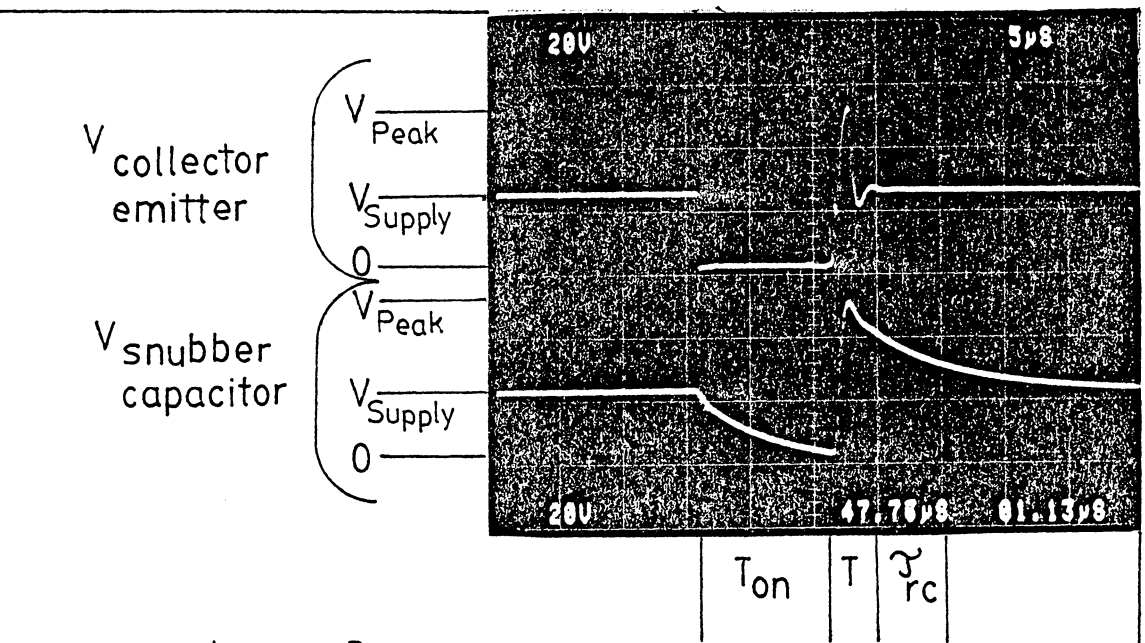
$$V_{CD} = V_{CAPACITOR} = \frac{1}{C_s} \int i_L \cos \frac{1}{L_s C_s} t \, dt + V_{CS} \qquad (3.13.6)$$

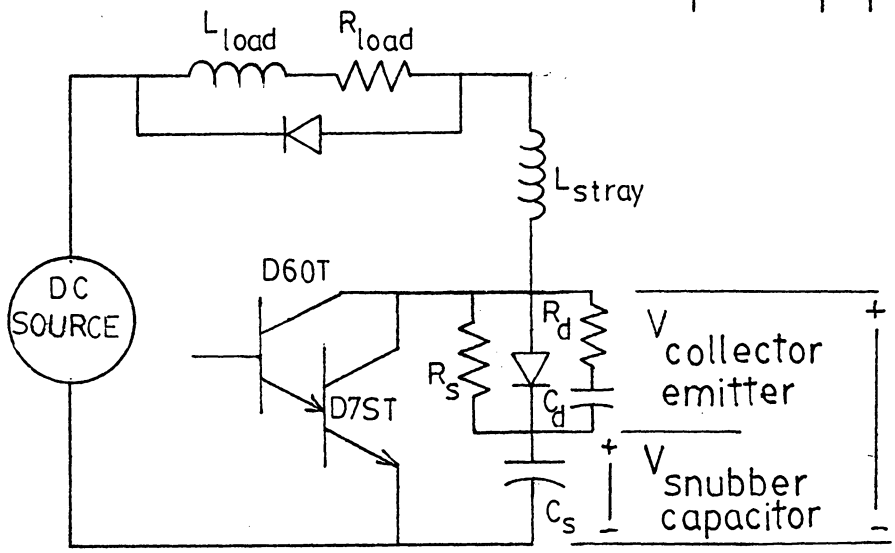
$$V_{CE} = V_{SUPPLY} + \frac{L_s}{C_s} i_L \sin \frac{1}{L_s C_s} t \qquad (3.13.7)$$

$$V_{CE_{PEAK}} = V_{SUPPLY} + \frac{L_s}{C_s} i_L \qquad (3.13.8)$$

The peak voltage the capacitor reaches is given by equation 3.13.8. When the peak voltage is reached, the current in the diode feeding the capacitor falls to the zero magnitude since the capacitor current leads the capacitor voltage by a phase of ninety degrees. As the current through the diode attempts to reverse, the stored charge in the pn junction diode is evacuated and the diode regains its reverse current blocking capabilities. The snubber capacitor voltage (see Fig. 3.13.4) which is equal to V_{PEAK} decays gradually back to the supply voltage through the snubber resistance $R_{SNUBBER}$. The collector-emitter voltage decays much more rapidly since its value is tied to the potential caused by the variation of collector current through the stray inductance L_s of the power circuit.

It should be worth noting, at least in passing, that two components which appear in Figures 3.13.1 and 3.13.4 were not discussed in the ideal behavior of the RCD snubber. These two components, R_D and C_D, are placed in parallel with the snubber diode and act to suppress voltage transients generated when the snubber diode turns off (see Figures 3.13.5a and 3.13.5b).





$T_{on} = 10\mu s$

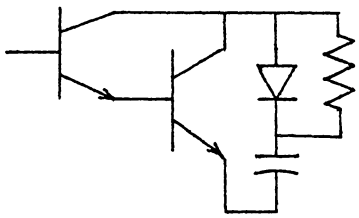
$T = 3\mu s$

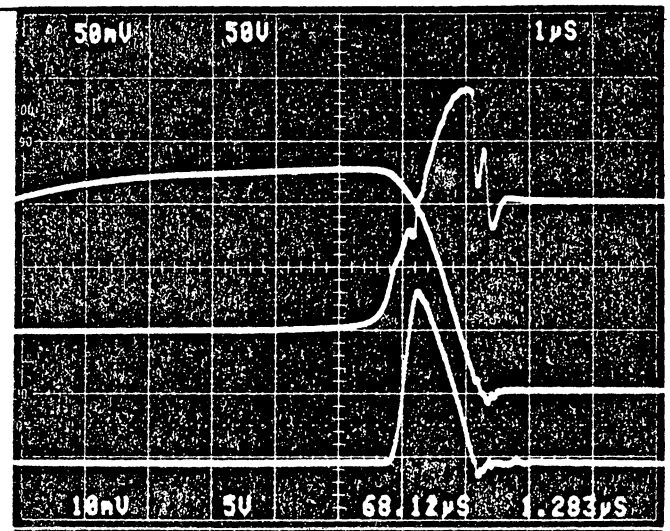
$\tau_{rc} = R_s \times C_s = 25 \times .22 = 5.5\mu s$

Energy Stored in $C_s = \frac{1}{2} C_s V(t)^2$ (AT SOME TIME t)

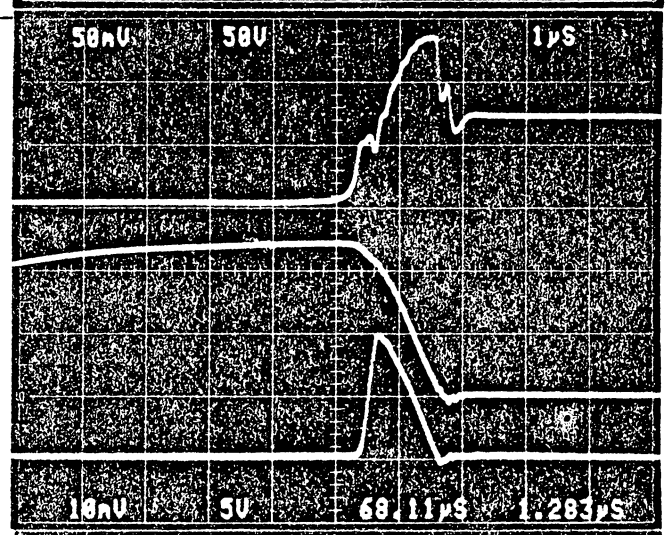
Figure 3.13.4 Capacitor Voltage Variation (during the switching interval)

(c) V_{ce} 100^{V} I_{load} 70^{A}



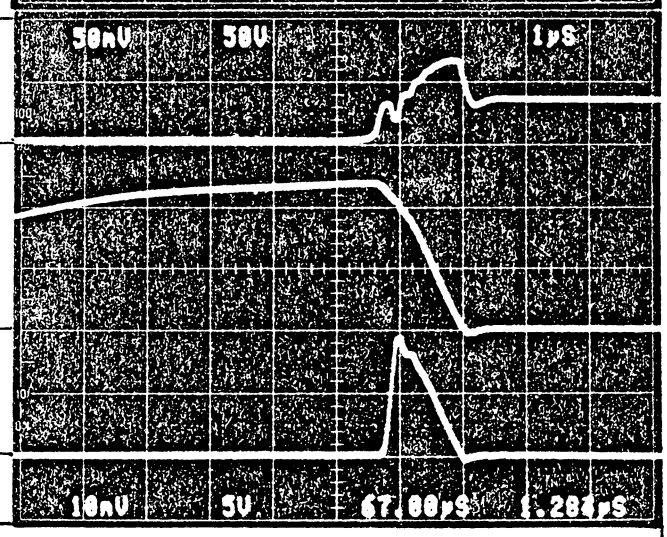


(b) V_{ce} 70^{V} I_{load} 50^{A}



(a) V_{ce} 30^{V} I_{load} 24^{A}

V_{ce}



SCALES

V_{ce}	50^{V}/div	I_{load}	10^{A}
I_{load}	$10,20,20^{A}$/div	I_{diode}	10^{A}
I_{diode}	$10,20,20^{A}$/div		

Figure 3.13.5a RCD Snubber without R_D & C_D

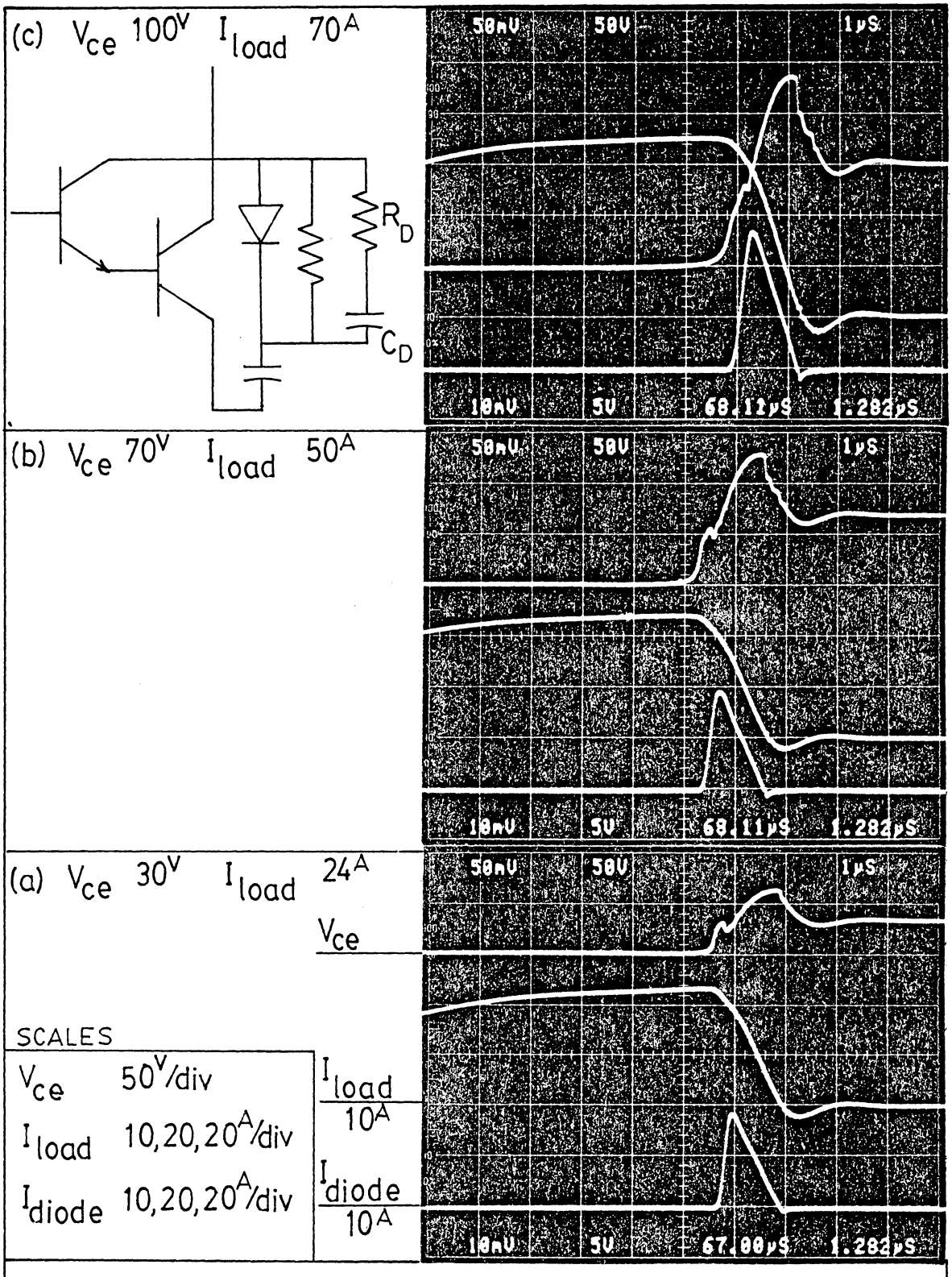


Figure 3.13.5b RCD Snubber with R_D & C_D

Recall that when the capacitor voltage reaches its peak value the diode supplying current to the snubber capacitor turns off. Without the additional elements, R_D and C_D, the interruption of current through the stray inductance in the collector circuit incites a sudden voltage drop in the collector-emitter voltage (Fig. 3.13.5a). At higher currents and voltages this mechanism has the potential to initiate dv/dt turn on of the transistor.

Now observing Figure 3.13.5b the addition of the elements, R_D and C_D, does not prevent the diode from turning off but they do provide a temporary alternate path for the stray inductances' current. An an end result, the collector-emitter voltage decays gradually instead of falling sharply.

The theoretical behavior described in the previous paragraphs shows good correspondence with the data collected. Table 3.13.1 provides the different values calculated for the stray inductance from the photographs (Figs. 3.13.2a, 3.13.2b, and 3.13.2c). The method of calculating the inductance was to employ equation 3.13.8 with the value of the peak voltage, supply voltage, and snubber capacitor taken from the individual photos. By solving 3.13.8 the stray inductance was determined to be on the order of one microhenry.

TABLE 3.13.1

Stray Inductance Calculation

$$(3.13.8)\quad V_{PEAK} = V_{SUPPLY} + \frac{L_{STRAY}}{C_{SNUBBER}} I_{LOAD}$$

$$L_{STRAY} = \frac{V_{PEAK} - V_{SUPPLY}}{I_{LOAD}}^{2} \times C_{SNUBBER}$$

V_{PEAK}	V_{SUPPLY}	I_{LOAD}	$C_{SNUBBER}$	CALCULATED L_{STRAY}
184^{V}	100^{V}	48^{A}	.35μF	1.072μH
188^{V}	100^{V}	48^{A}	.30μF	1.008μH
197^{V}	100^{V}	48^{A}	.25μF	1.021μH
210^{V}	100^{V}	48^{A}	.20μF	1.050μH
230^{V}	100^{V}	48^{A}	.15μF	1.100μH
260^{V}	100^{V}	48^{A}	.10μF	1.11 μH

In Figures 3.13.2a - 3.13.2c the energy stored in the snubber capacitor and the power dissipation of the snubber resistances were calculated. The energy stored in the capacitor is proportional to the peak voltage which is in turn inversely proportional to the size of the capacitor. The major tradeoff involves the peak voltage experienced by the snubber capacitor and transistor versus the power requirements of the snubber resistance. During the turn off phase the capacitor charges to the peak voltage given by 3.13.8. The energy stored in the capacitor at this point is provided by equation 3.13.9 (see Fig. 3.13.14).

$$E_{STORED} = \frac{1}{2} C_s V_{PEAK}^2 \qquad (3.13.9)$$

After the peak voltage has been reached it decays via the snubber resistance back to the supply voltage level. Equation 3.13.10 shows the amount of energy transferred to the snubber resistor.

$$E_{TRANSFERRED_1} = E_{STORED\ INITIAL} - E_{STORED\ FINAL} \qquad (3.13.10)$$

$$E_{TRANSFERRED_1} = \frac{1}{2} C_s V_{PEAK}^2 - \frac{1}{2} C_s V_{SUPPLY}^2 \qquad (3.13.10a)$$

The snubber capacitor maintains this voltage until the transistor is turned on again at which point the snubber capacitor voltage decays to zero. The energy transferred to the snubber resistor during this period is given by 3.13.11:

$$E_{TRANSFERRED_2} = E_{STORED\ INITIAL} - E_{STORED\ FINAL} \qquad (3.13.11)$$

$$E_{TRANSFERRED_2} = \frac{1}{2} C_s V^2_{SUPPLY} - \frac{1}{2} C_s (0)^2 \qquad (3.13.11a)$$

The total energy transferred to the snubber resistance is the sum of the two energy transfers. This energy dumping by the capacitor is repetitive so that the power dissipation is the multiplication of the energy and the switching frequency (see equation 3.13.12).

$$P_{R_S} = \frac{1}{2} C_s V^2_{PEAK} \times \text{Frequency} \qquad (3.13.12)$$

In summary the three figures for the RC and RCD snubbers (3.13.2a - 3.13.2c) show that the .3 microfarad capacitor in the polarized snubber performs the best overvoltage suppression but at the cost of a large power dissipation in the snubber resistor (375 watts at 30 KHz and 300 Volts). The lower valued snubber capacitors do not

transfer as much energy away from the power switch or suppress the voltage transient but their power dissipation is more reasonable.

Since there was no clear cut choice of a superior RC or RCD snubber, a combination of an active voltage clamp and a non-polarized resistor capacitor snubber was tested.

3.14.1 Active Voltage Clamp Circuit

Figure 3.14.1 displays the schematic diagram for an active voltage clamp utilizing an International Rectifier series 450 power FET. Since a resistor-capacitor snubber network can provide adequate current shunting of the transistor at turn off but is inadequate for transient voltages, a combination of the two circuits could prove to be ideal in this application.

The principle of operation of the FET voltage clamp circuit is quite straight forward. When the voltage transient magnitude exceeds three hundred and fifty Volts, the zener diode reference network begins to conduct current. Soon the gate to source potential measured across the thirty ohm resistance R1 surpasses four Volts and the n channel FET (IRF 450) turns on. At this point the low impedance path provided by the seven and one-half ohm power resistor, R_{CLAMP}, and the drain to source resistance of the FET

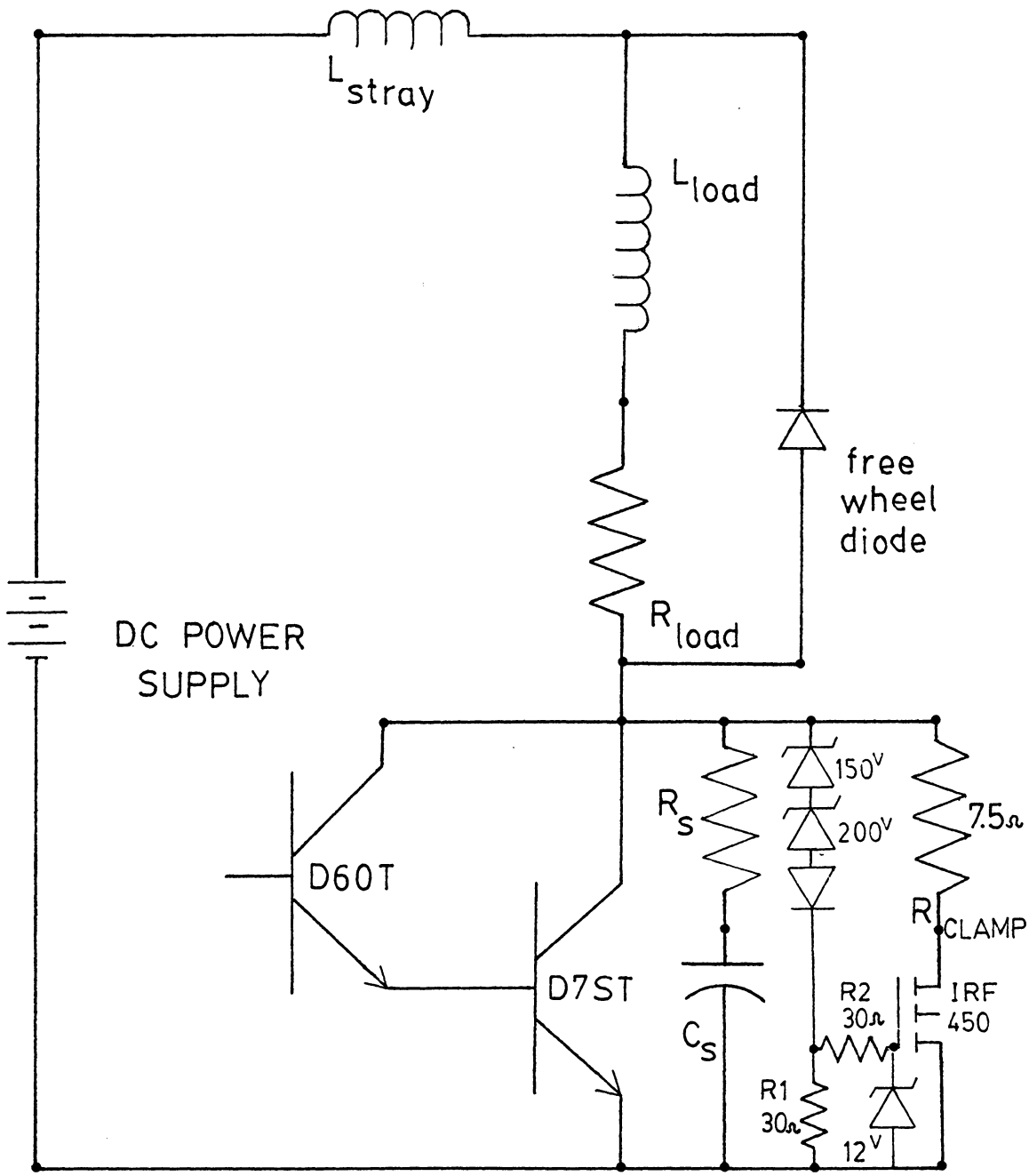


Figure 3.14.1 Active Voltage Clamp Test Circuit

($R_{DS(on)}$ = .4 ohm) causes a high current of about forty-five Amperes to flow through the FET for a brief duration of time (see Fig. 3.14.2). Although the FET is only rated for a continuous current of ten Amperes, the low duty cycle prevents the FET power switch from being stressed beyond manufacturers' specifications. Equations 3.14.1 - 3.14.4 are the results of testing the voltage clamp circuit with a source voltage of two hundred and fifty Volts and a collector current of eighty Amperes. The clamp circuit appears to act properly although some high frequency oscillations result during its interval of operation.

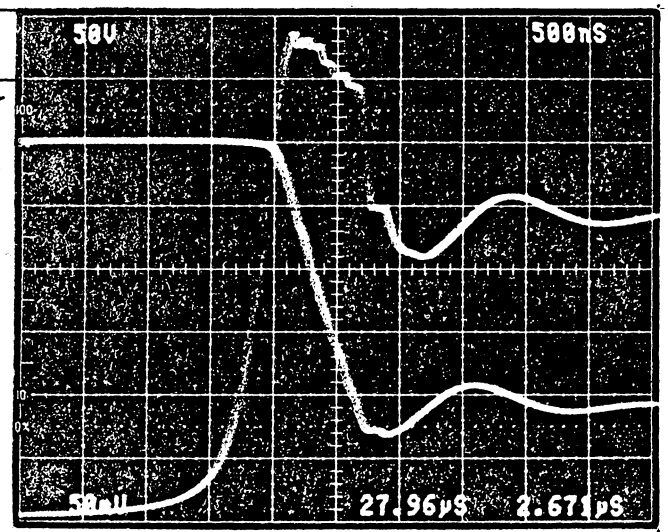
$$T_{ON_{\text{CLAMP CIRCUIT}}} = 700 \text{ nanoseconds} \qquad (3.14.1)$$

$$T_{SWITCHING\ CYCLE} = \frac{1}{F_{SWITCHING}} = 33.3 \text{ microseconds} \qquad (3.14.2)$$

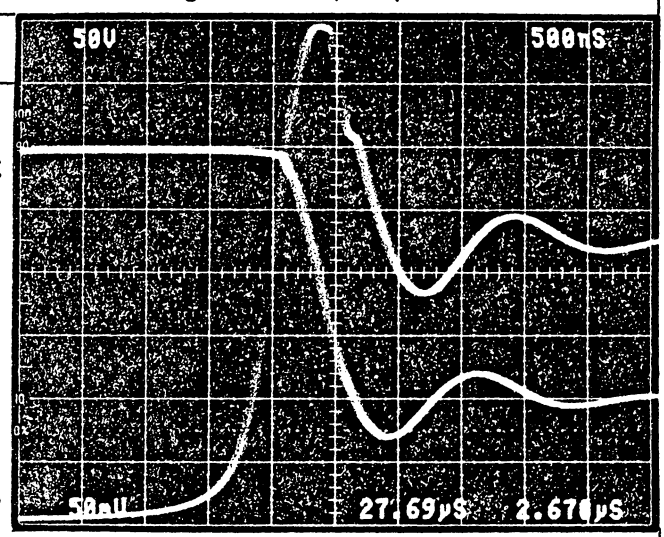
$$\text{Duty Cycle} \quad D.C. = \frac{T_{ON}}{T_{SWITCHING}} \times 100 = \frac{700 \times 10^{-9}}{33.3 \times 10^{-6}} \times 100 = 2.1\% \qquad (3.14.3)$$

Average Power Dissipation

$$P_{D_{AVE}} = P_{D_{(T_{ON})}} \times D.C. = (45) \times (18) \times .021 = 17.0 \text{ Watts} \qquad (3.14.4)$$



(a) Voltage Clamp Operation



(b) Unclamped Voltage Transient

SCALES

I_c 20A/div

V_{ce} 50V/div

OPERATING CONDITIONS

Freq = 30 kh_z , Voltage = 250V, Current = 80A

(T_{clamp} = 700 ns ÷ T = 33.3μs) = 2.1% Duty Cycle

Figure 3.14.2 Results For Voltage Clamp Circuit

This chapter has completely specified the switching devices, their configuration, and the method employed to drive the transistors. The last topic which was the topic of how to aid the devices during switching to insure their safe repetative operation remains unsettled. In Chapter Four operation of the Darlington power switches in the full bridge configuration may lead to the emergence of a superior snubbering technique. There are, as previously stated, differences in the operation of the switches individually and operation in the totem pole or bridge configuration.

CHAPTER FOUR

FULL-BRIDGE INVERTER MODULE

4.1 Introduction

The fourth chapter appropriately deals with the design and configuration for the entire inverter bridge module. The inverter module system is defined on a global level at which point six very important design considerations will be addressed. The first topic concerns the input filtering requirements. The input power supply to the thirty-kilowatt, thirty-kilohertz inverter module should be capable of supplying and accepting large amounts of power quickly (fast response time). A second task was to develop a logic circuit to operate the full bridge in the clamped mode. Timing is critical in this instance as any error in the drive signals to the bridge inverters' base drives can cause a shoot-thru condition to occur. The possibility of a short circuit leads to the third objective; implementation of an over-current protection circuit. The protection function is performed through the combination of an input choke, resistive current shunt and a peak current sensing circuit. A fourth task was to interface the base drives, logic circuit, protection circuit and the power switches in the bridge. Some considerations of noise generation and suppression were carried out. Finally, the

last two requirements involved snubber circuit interactions in the full bridge and false turn on due to dv/dt effects. Both problems are present in the inverter module, hopefully not to the point that such problems are insurmountable.

Until now the development work involved testing a single Darlington power switch; however, with this rather extensive chore completed (see Chapter 3) the more important objective of full bridge operation was assailed. Initial testing was performed by operating a diagonal pair of switches in a half bridge configuration. This operation helped to qualitatively explain the different phases of circuit behavior observed within the full bridge inverter.

4.2 Inverter Module Configuration

Figure 4.2.1 exhibits the inverter module in quasi-block diagram format. Conceptually, the inverter is composed of five separate subsystems which include; the power source, the base drive logic circuit (Fig. 4.3.1), the over-current protection circuit (Fig. 4.4.1), the base drive circuits (Fig. 3.12.1), and the bridge inverter power circuit (Fig. 4.5.1). Each subsystem provides a very distinct function for the inverter system.

The first subsystem contains the d.c. power source which has a variable output capability. The source is

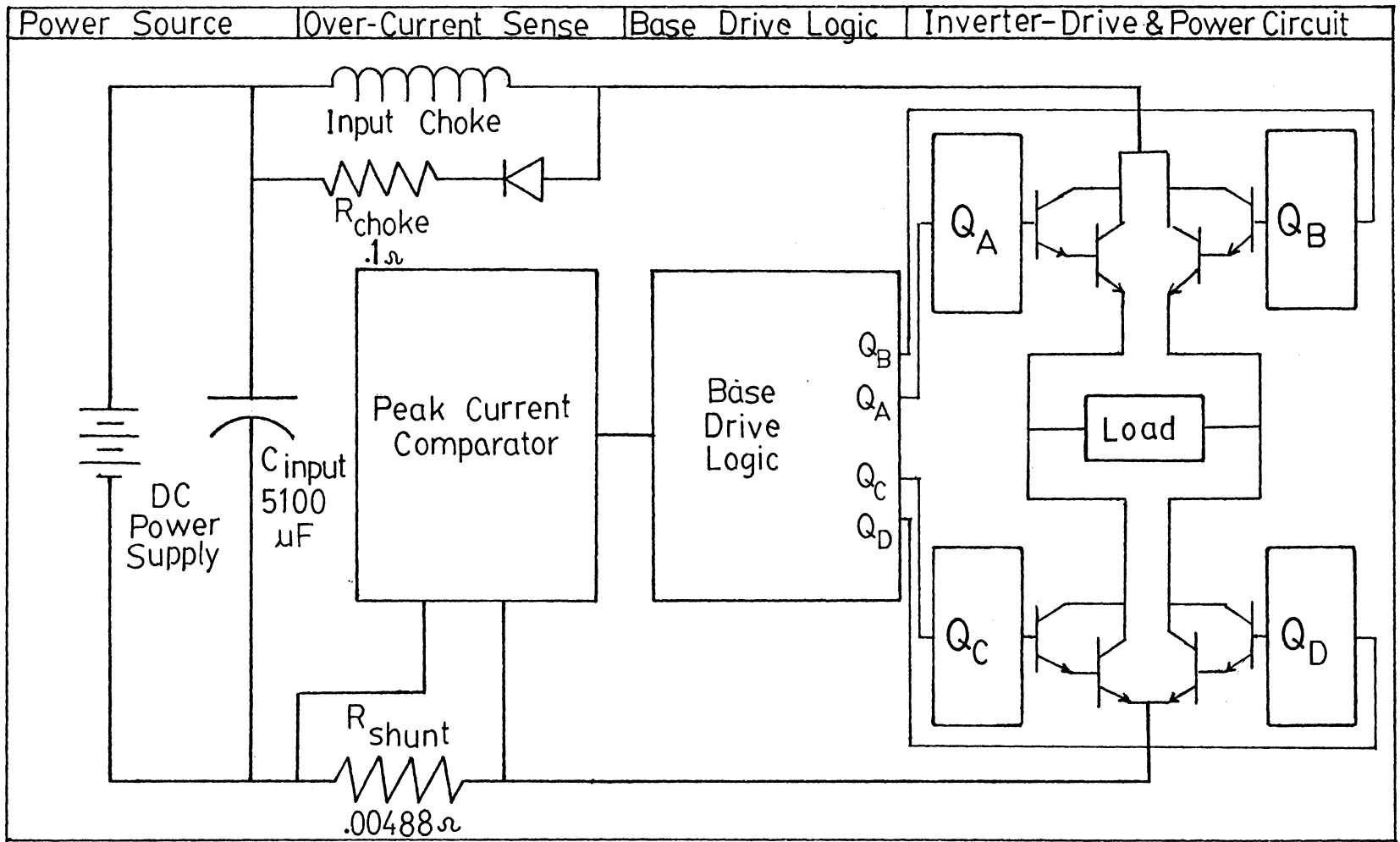


Figure 4.2.1 BLOCK DIAGRAM OF INVERTER MODULE

coupled with a fifty-one hundred microfarad capacitor to provide high energy storage. There are several reasons for the capacitor. The first reason is that generally a full-bridge inverter utilizes anti-parallel diodes around the power switches to furnish bidirectional current flow capabilities. The bidirectional current capability in turn supplies a path for inductive currents or for regeneration back into the power source. Often the source is incapable of sinking these currents so that some form of independent storage mechanism is required i.e. a capacitor. A second reason for utilizing a capacitance at the input is to supply the instantaneous demands of the inverter's load. Since the value of capacitance is so great (5100μF), it is capable of storing about one and one-half coulombs of charge. This charge can furnish a current of one hundred and fifty Amperes for a time period of ten milliseconds.

In practice, the capacitance was placed as close as physically possible to the inverter circuit to decouple any stray inductance in the power leads to the d.c. source. This increases the effectiveness of the capacitor at handling switching load demands.

4.3 Base Drive Logic

The logic circuit subsystem is an inherently simple circuit (see Fig. 4.3.1). Three dual monostable multivibrators

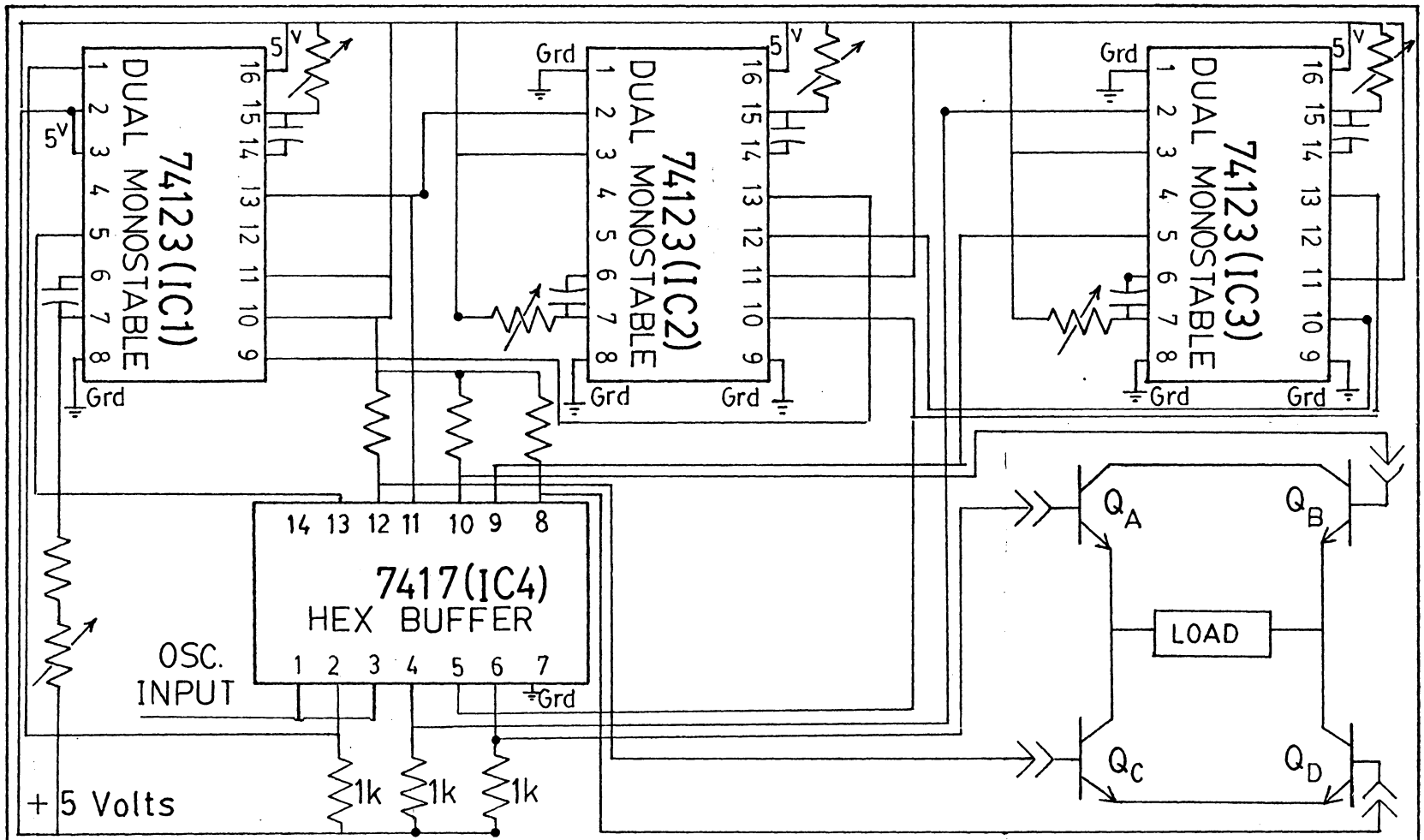


Figure 4.3.1 BASE DRIVE LOGIC SCHEMATIC

DESIGN& DRAWING BY P.D. WESEL
DATE 9-1-83

(dual one shots) are interconnected to provide the four outputs to the base drives of the inverter bridge. The two outer integrated circuits (IC2 and IC3) provide the four individual drive signals for the transistor. The inner integrated circuit furnishes the capability of delaying the Q_D signal relative to the Q_A signal (Q_B signal relative to the Q_C signal) so that the inverter can be operated in the clamped mode (see Fig. 4.3.2).

Beginning at the input, an oscillator squarewave is fed into pins 1 and 3 on IC4 which is a hex buffer circuit. The two outputs (pins 2 and 4) are then connected into two inputs on IC1 and IC3 (pins 1 and 2). The Q_A drive signal is rising-edge triggered and the Q_C drive signal is falling-edge triggered so that each output occurs 180^o out of phase with the other. The two one shots' RC time constants are adjustable in length so that the duty cycle of the Q_A and Q_C waveforms can be changed.

Both the Q_A and the Q_C signals are used as the triggering inputs to IC2 (pins 10 and 2). The two one-shots on IC2 are rising-edge triggered and initiate small positive delays in the Q_A and Q_C signals. These outputs are returned to IC3 and IC1 where they are used as inputs (pins 10 and 9 respectively). The Q_D and Q_B signals are then delayed in time with respect to the Q_A and Q_C signals. All the outputs

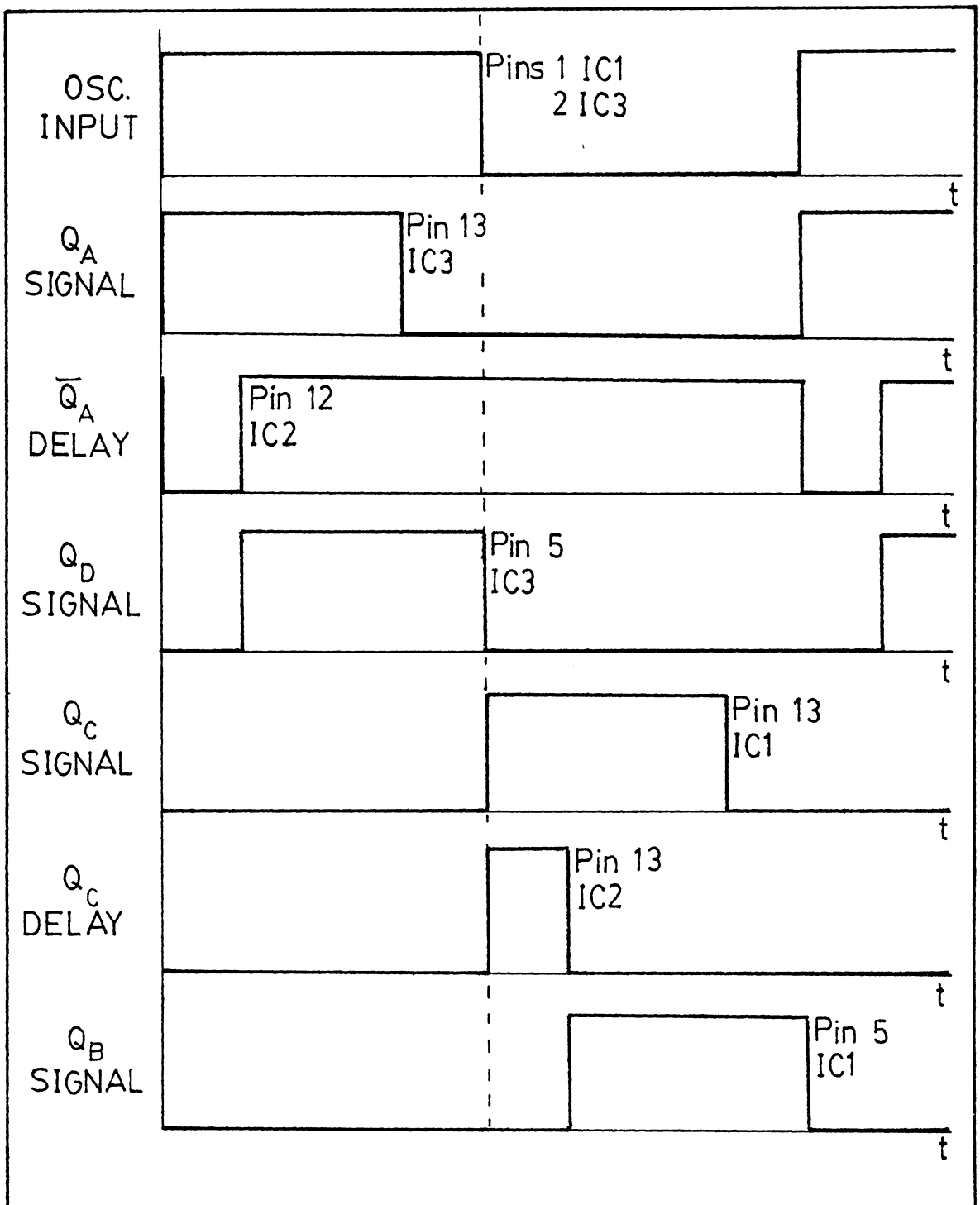


Figure 4.3.2 TIMING DIAGRAM
BASE DRIVE LOGIC

are buffered through IC4 before being attached to the base drive circuits of the bridge inverter. Finally, assuming the one shots are not triggered falsely by spurious noise, it is impossible for the logic signals to the power switches, Q_A and Q_C (Q_B and Q_D), to overlap reducing the risk of shoot-thru. It should be noted, however, shoot-thru considerations are not eliminated because of device storage time effects.

4.4 Over-Current Protection

The over-current protection system is composed of a resistive current shunt, peak current sensing circuit (see Fig. 4.4.1), and an input choke. The current shunt converts a high value current to a low voltage measurement. The shunt used in this instance has a resistance of .00488 ohms so that a current of one hundred Amperes would translate into a voltage drop of one-half Volt across the shunt. Allowable power dissipation for this particular current shunt is one hundred Watts meaning it can sustain switched currents up to two hundred Amperes. The output of the shunt is low-pass filtered and connected to the inverting input of an operational amplifier.

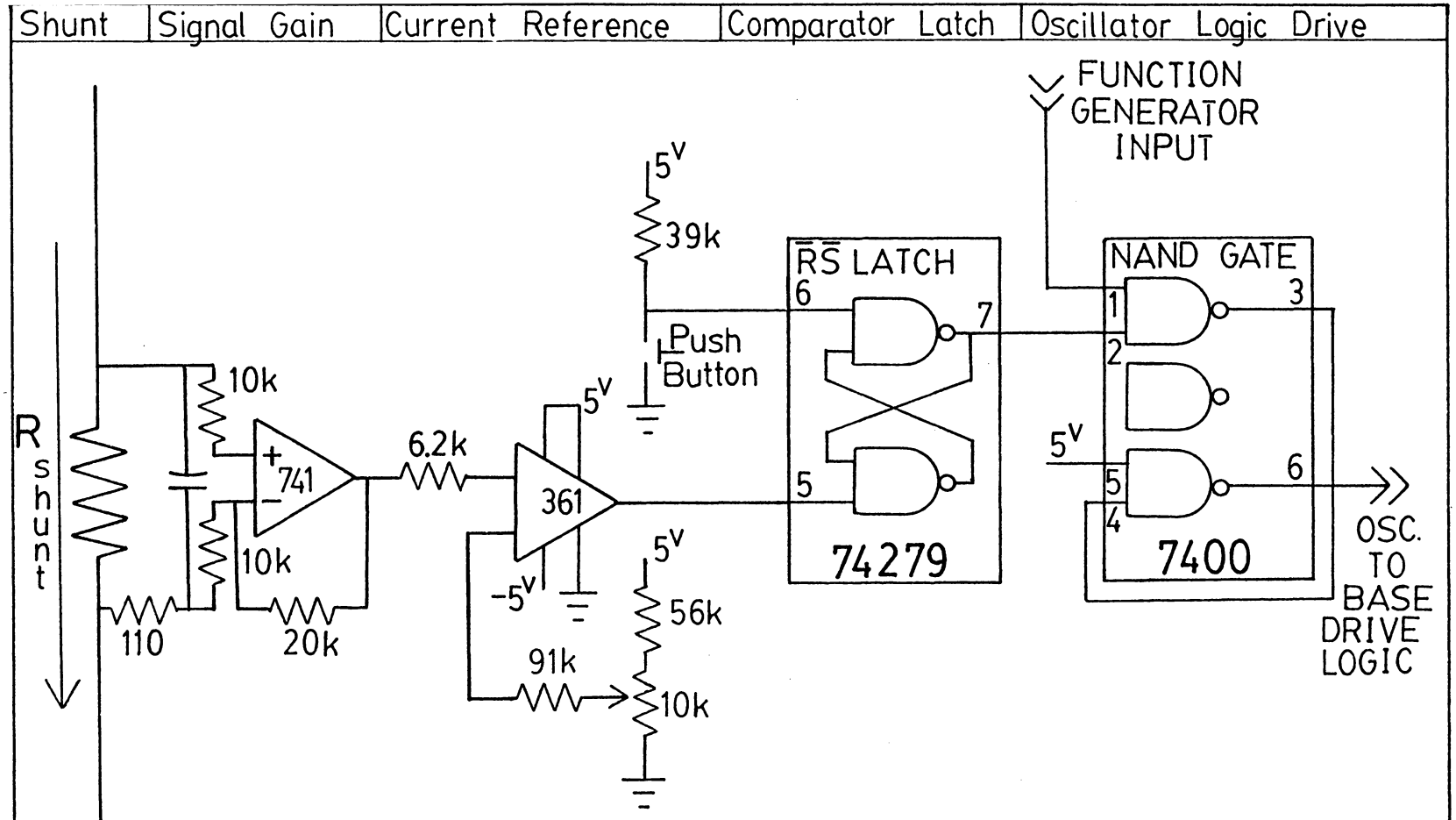


Figure 4.4.1 OVER-CURRENT PROTECTION SCHEMATIC

DESIGN & DRAWING BY PD WESEL

DATE 9-1-83

A few factors should be mentioned here. First, it was desirable to place the shunt in the return path to the power supply from the inverter (simply for mechanical reasons). It was also advantageous to ground the emitters of the lower two Darlington BJT power switches in the bridge for measurement purposes and noise elimination in the lower two base drive circuits. For these reasons the measured potential across the shunt was negative and the op-amp provided inversion of the current signal as well as amplification.

A second consideration was the choise of an appropriate gain level for the inverting op-amp. Since five Volt supplies were utilized it was not practical to substantially amplify the output of the sunt ($-.5^{V}$ at 100 Amperes). The chosen gain varied between two and four depending on the current level of bridge operation. Initially, a very fast operational amplifier was used in the circuit (TL081 for example); however, due to the reverse recovery current spike the op-amp was susceptible to high frequency switching noise. Instead a slower standard 741 op-amp was employed. Since the typical slew rate of the 741 is about half a Volt per microsecond, the gain was reduced to two so that the protection circuit could operate with reasonable response time at the higher currents.

The amplified current shunt signal was compared with a voltage reference using a high speed comparator (LM 361) The National chip contained internal buffering and level shifting from the bidirectional op-amp supply (±5 Volts) to TTL levels of zero and five Volts. The comparator's output was in turn latched using a TI74279 quad $\bar{S}\bar{R}$ latch circuit. Only a single $\bar{S}\bar{R}$ latch was used with the $\bar{R}$ input coming from the reference comparator and the $\bar{S}$ input provided by a pull up resistor with a push button swtich to ground. Finally, two "nand" gates were used in a 7400 TTL package as a single "and" gate. The latched comparator signal and a function generator oscillator were combined.

Under normal operation the voltage drop caused by current flowing through the shunt would not be sufficient to trip the protection circuit. In the case where two switches in the same leg of the inverter bridge simultaneously conducted the resulting short circuit and high current would surpass the preset protection level and the output of the comparator would go low causing the latch to change state. The oscillator input to the base drive logic would be instantaneously interrupted and held at the low level so that the base drives would apply reverse bias to all four power switches.

The input choke (see Fig. 4.4.2) performs the valuable task of limiting the time rate of rise of the current under short circuit conditions providing the protection circuit with time to react. Since the protection circuit is not capable of instantaneous reversal of the applied drive to the Darlington switches the input inductance would prevent the simultaneous catastrophic application of high current and high voltage to the switches.

Under short circuit conditions the current would rise rapidly inducing an L di/dt potential drop across the inductor. In practice the input inductance was supplied by a large air core inductor for which an order of magnitude estimate of five microhenries was determined from the L/R time constant of the bridge. Therefore, if the supply voltage was three hundred Volts and a short occurred it would take over three microseconds for the current to reach the two hundred Ampere level.

The .1 ohm resistor in the free wheeling path provides a more substantial potential drop across the inductor during the phase when all four switches in the bridge are off and the inductor current loops through the free wheeling diode. The higher potential drop hastens the decay of current through the inductor and resets the flux.

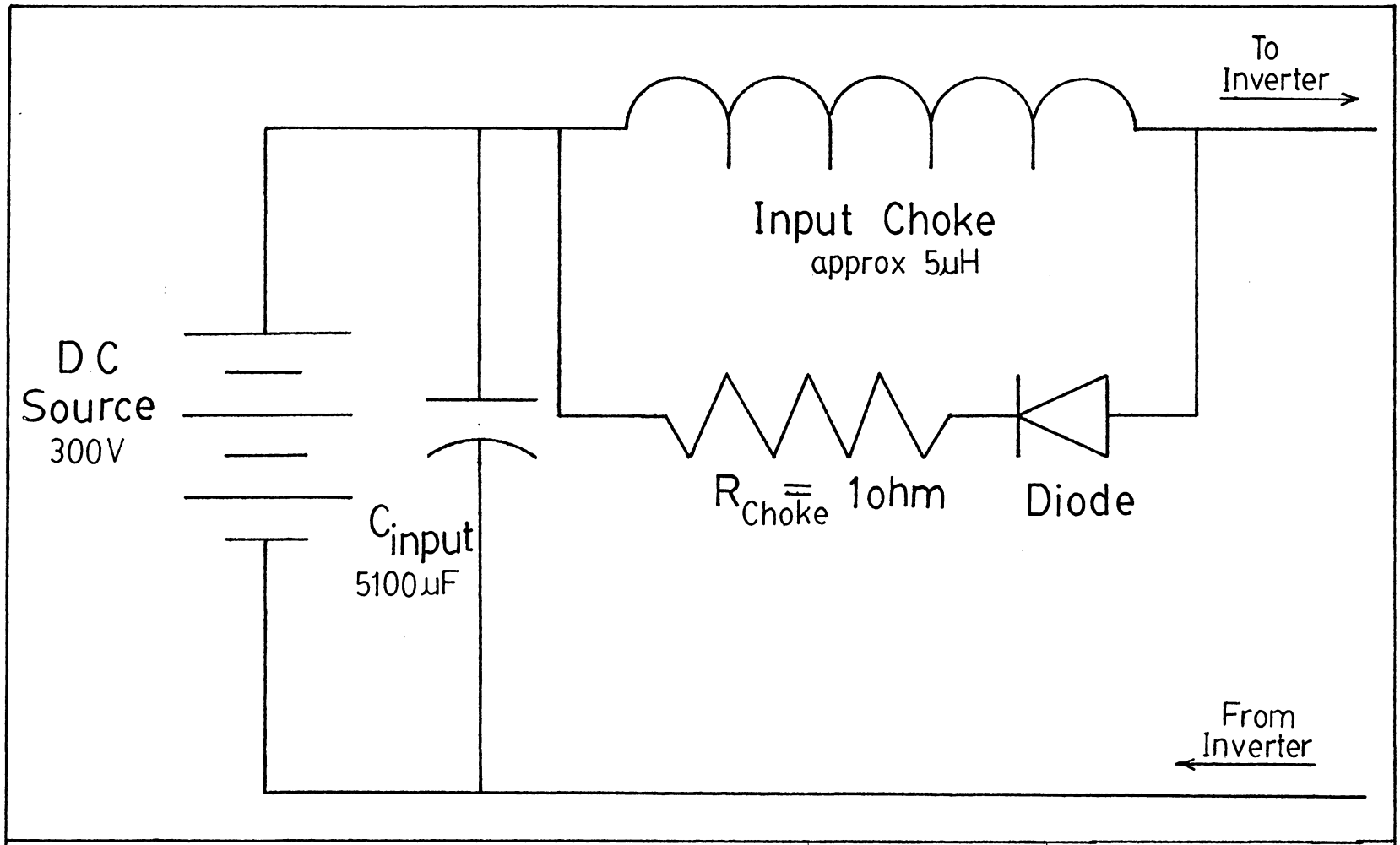


Figure 4.4.2 PROTECTION INPUT CHOKE CIRCUIT

4.5 Inverter Power Circuit - Half Bridge Operation

Since the base drive circuit subsystem was previously discussed in section twelve of the third chapter the only major subsystem left to be discussed is the inverter bridge power circuit. This discussion is accompanied with results from bridge operation. Also, the previously mentioned dv/dt effects and snubbering interactions in the bridge need to be dealt with.

Figure 4.5.1 is a schematic diagram for the bridge power circuit with an intermediate valued RCD snubber and the optional active voltage clamp circuits. Each power switching unit contains twelve elements not including the active voltage clamps. These elements are subdivided into three categories. The Darlington switch itself is composed of two transistors (D60T and D7ST), two leakage stabilization resistances (30 ohms and 11 ohms), and two reverse speed-up diodes. The snubber network consists of a resistor, diode and a capacitor along with a second resistor and capacitor parallel to the snubber diode. Finally, each Darlington power switch is coupled with a Westinghouse R502 fast recovery diode in order to provide bidirectional current capabilities.

Physically the upper two power switches were electrically connected through their aluminum heat sinks.

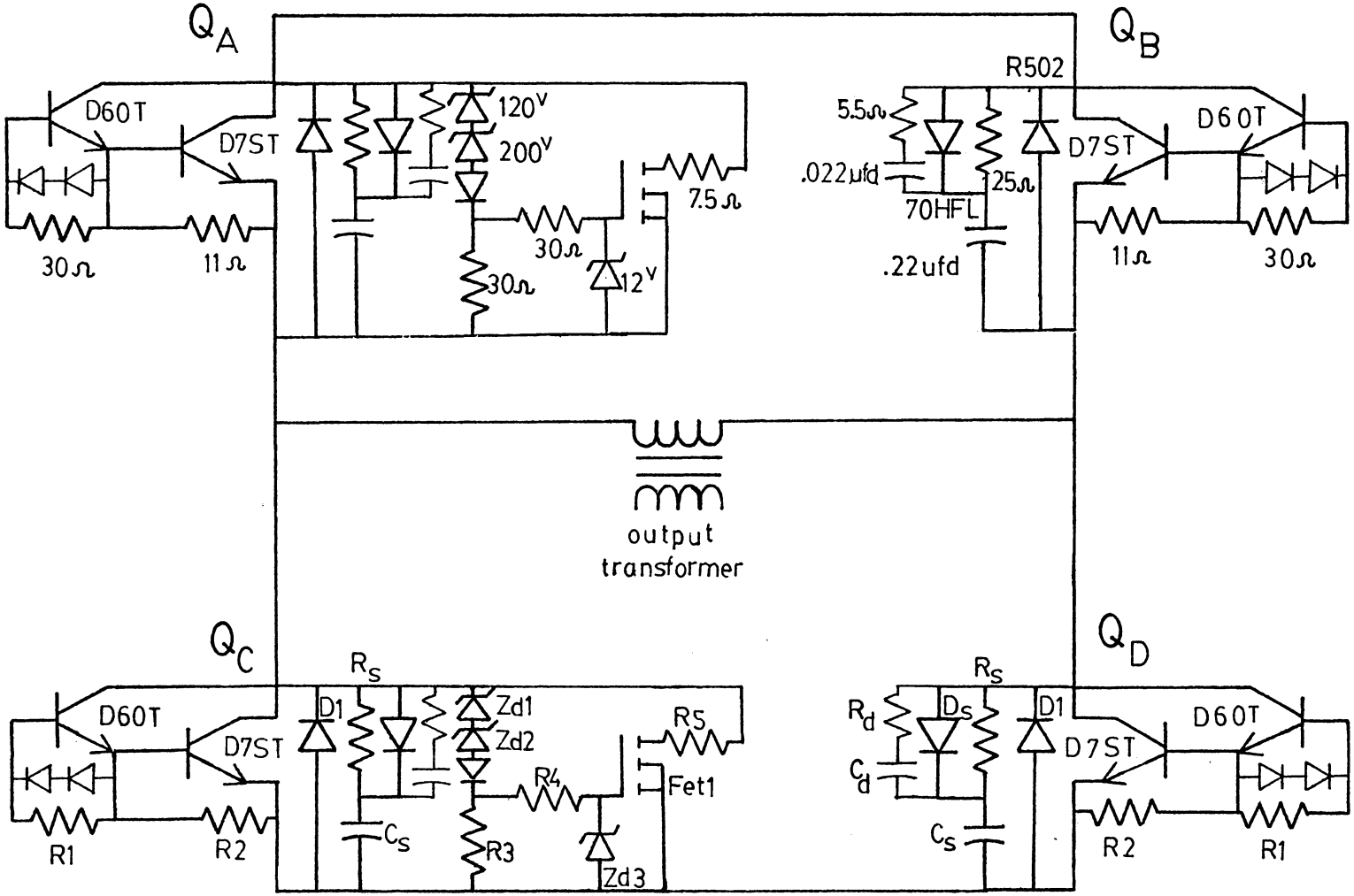


Figure 4.5.1 INVERTER POWER MODULE CIRCUIT DIAGRAM

The bottom two switches were also connected electrically by placing their heat sinks together. The D60T and R502 are both stud mount devices which required that the sinks be drilled and tapped to accomodate them. The D7ST transistor, on the other hand, is a hockey puck type device which conducts only when compressed between two conducting surfaces.

Any parasitic elements would be most prevalent in the connections of the upper devices to the lower devices and the connection of all four switches to the load or output transformer. In construction, the circuitry was placed as symmetrically as possible so that each conductive path through the inverter was identical.

Initially, the bridge was operated, without the active voltage clamp, in the half bridge configuration so that only the upper left hand switch (Q_A) and the lower right hand switch (Q_D) conducted. Operating these two devices with the offset drive waveforms of the clamped mode provided some interesting results (see Fig. 4.5.2). The collector-emitter voltage of the Q_A device and the load current are shown in Figure 4.5.2. The Q_A and Q_D drive signals were both approximately ten microseconds in length with the Q_D signal occuring about four microseconds after the Q_A signal starts.

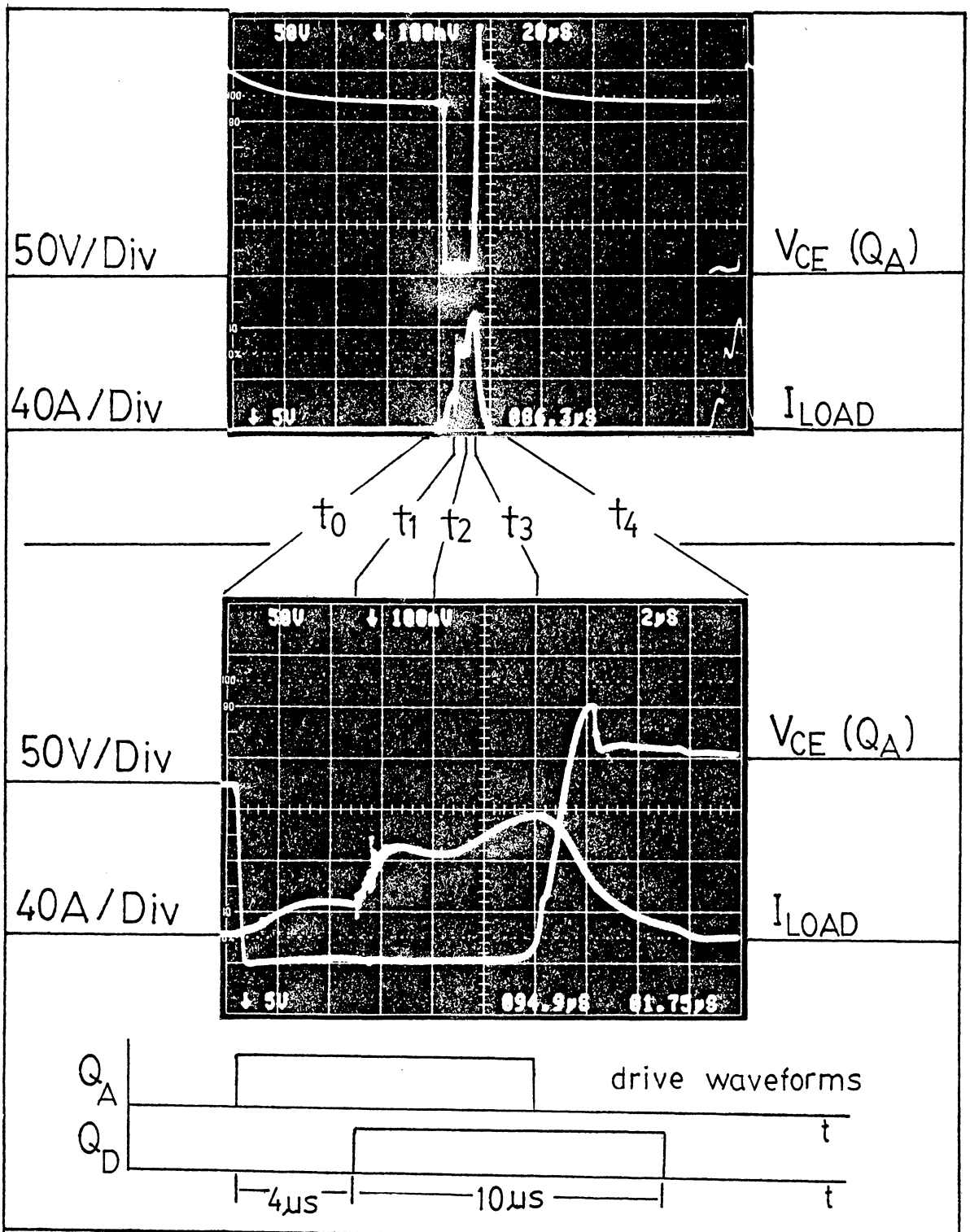


Figure 4.5.2 HALF-BRIDGE OPERATION (170^V, 100^A)

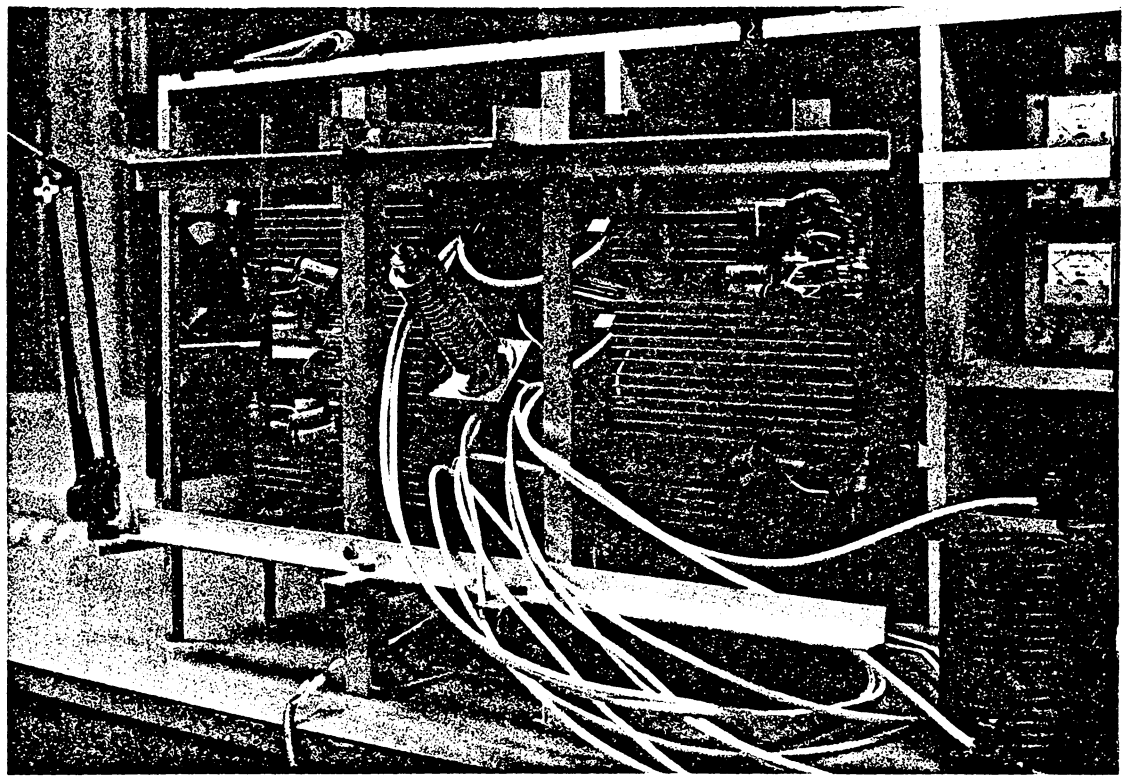


Figure 4.5.2a Breadboard of the 30kW Transistorized Inverter Module

The load current from t_0 to t_1 was characterized by the charging of the Q_D snubber (see Fig. 4.5.1a). An additional current component would flow through Q_A to charge the snubber of Q_C as well but would not flow through the load to do so.

At t_1 the Q_D device was turned on and the load current oscillated slightly and then rose with an LC oscillation due to the input inductance and the snubber capacitor of Q_C (see Fig. 4.5.1b). The capacitor C_s of device Q_C continues to charge because of the increasing voltage across the load. The load potential maintains a forward bias on Q_C's snubber diode until the resonating LC circuit causes the current through the diode to attempt to reverse. At this point, corresponding to t_3 on Figure 4.5.2 the full source voltage of one hundred and seventy Volts is applied to the load.

Between t_3 and t_4, Q_A is switched off first and four microseconds later Q_D is turned off. When the Q_A swtich turns off, the load current begins to decay through the still conducting Q_D switch and the anti-parallel diode of Q_C (see Fig. 4.5.1c). The Q_D switch turns off with eight Amperes or so of the original one hundred Ampere peak current is flowing through the anti-parallel diodes of Q_B and Q_C back into the source.

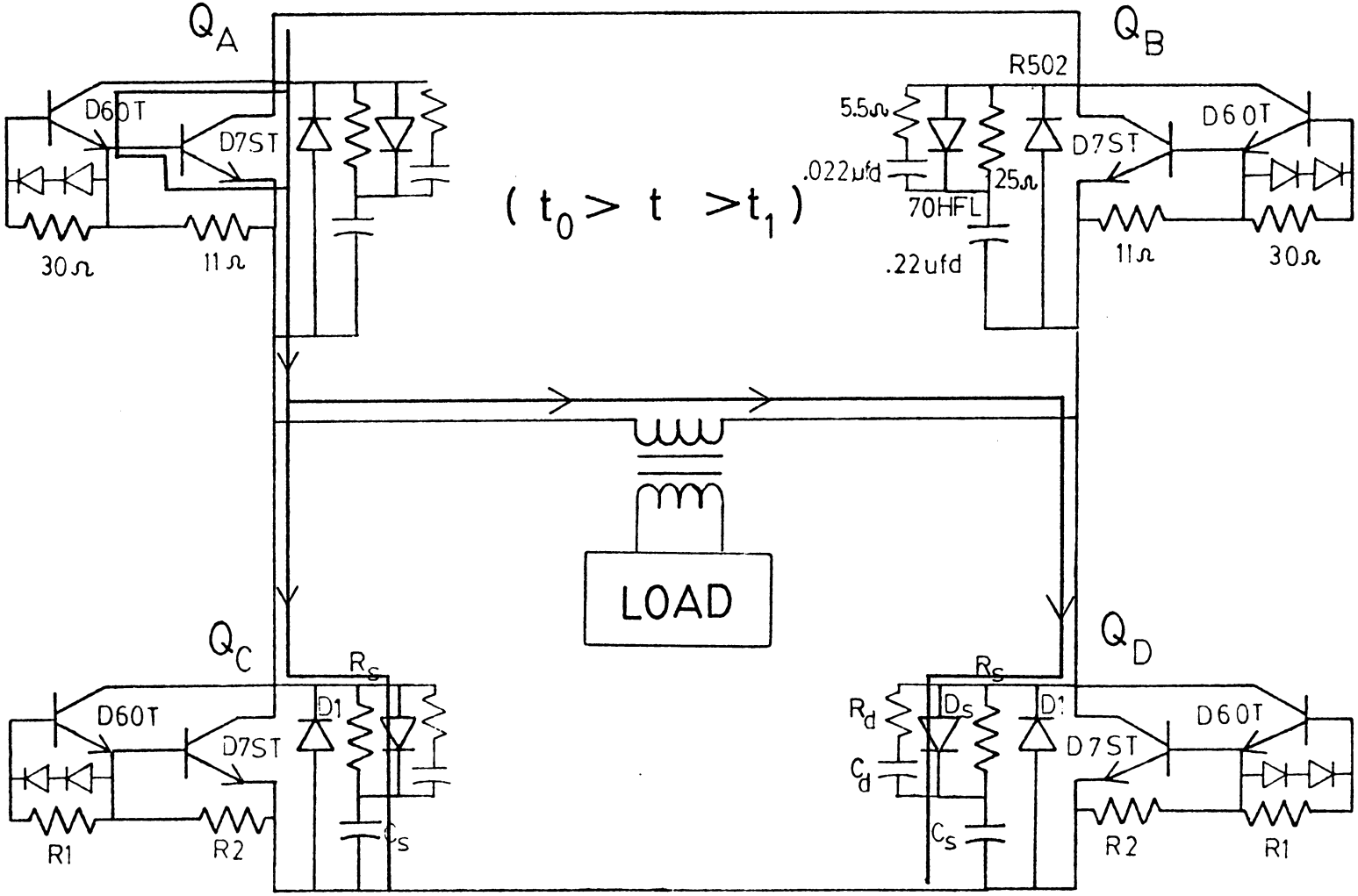


Figure 4.5.1a INVERTER POWER MODULE CIRCUIT DIAGRAM

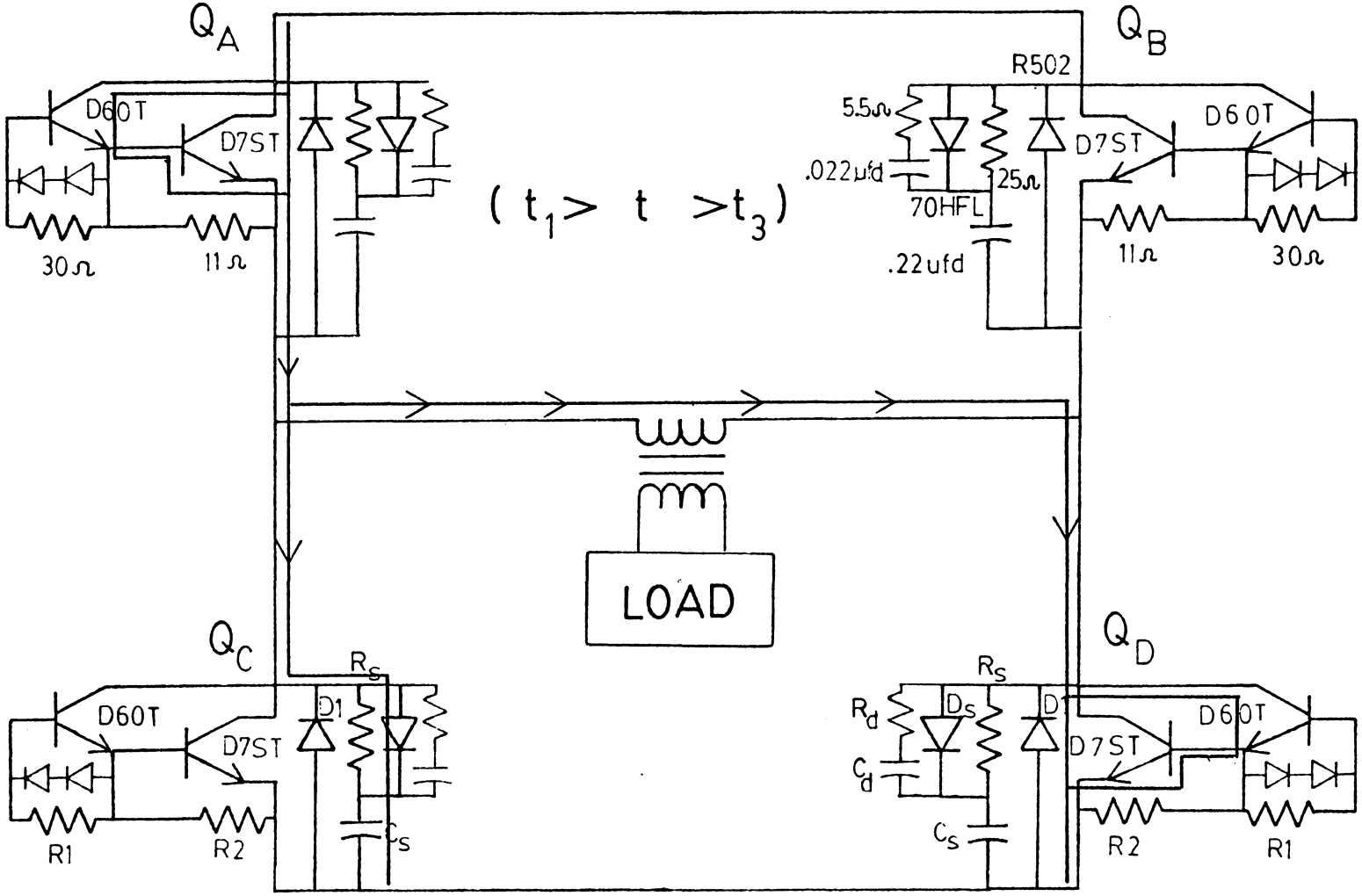


Figure 4.5.1b INVERTER POWER MODULE CIRCUIT DIAGRAM

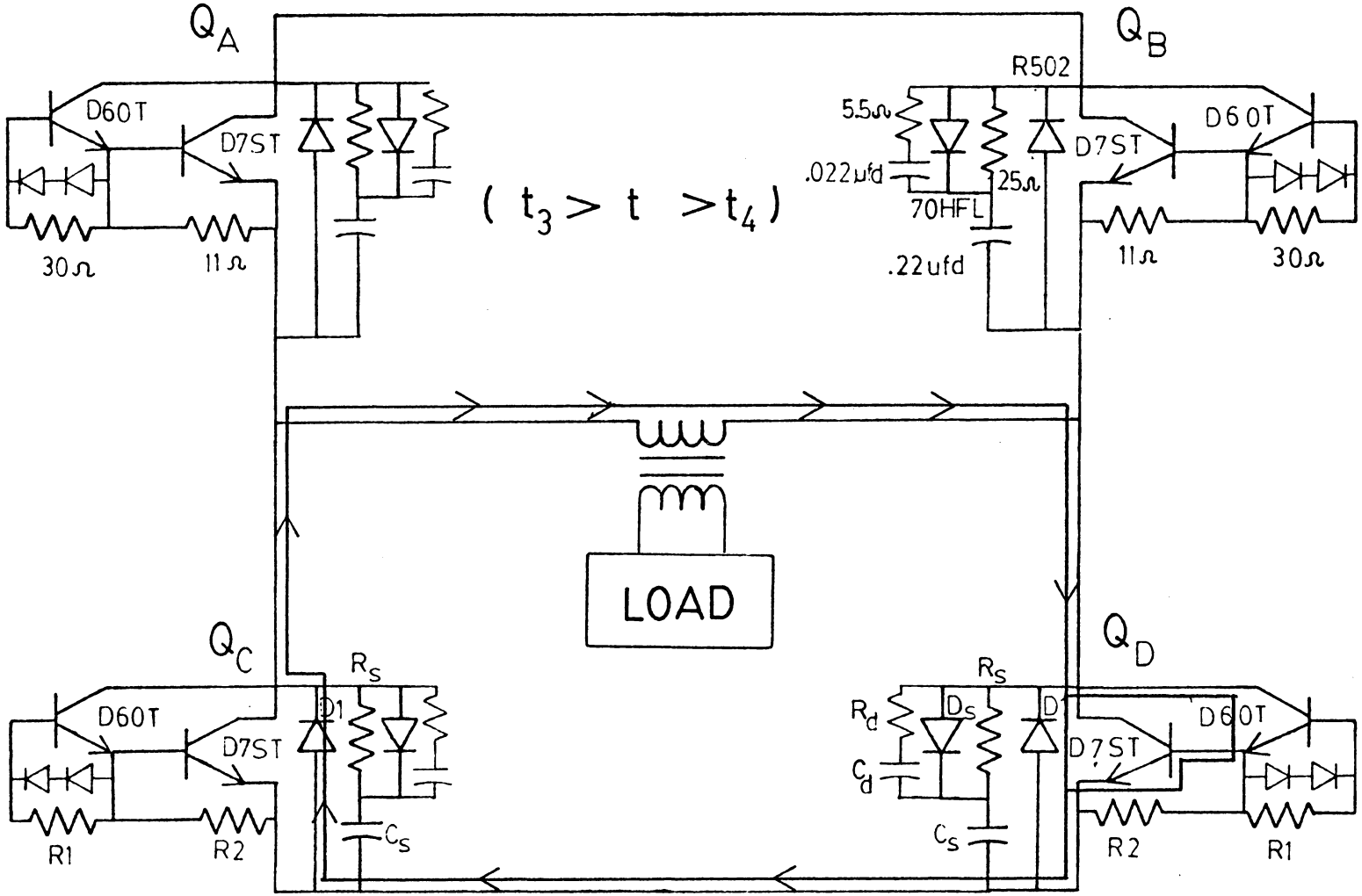


Figure 4.5.1c INVERTER POWER MODULE CIRCUIT DIAGRAM

4.6 Inverter Power Circuit - Full Bridge Operation

In the previous half-bridge clamped mode of operation the upper device turned off first requiring the switch to block the entire source voltage. This is one of the characteristics of clamped mode techniques as opposed to straight inverter operation where both devices turn off at the same time and equally share the supply voltage.

The device turning off first does no under high current conditions in addition to blocking the full source voltage. This is more commonly referred to as "hard" turn off. The power switch turning off later does so under a lower collector current and is required to block little or none of the voltage. Figures 4.6.1 through 4.6.4 furnish some detailed waveforms of full-bridge clamped mode operation at 250^{V} and 80^{A}. The first set of photographs show the same devices as for half-bridge operation (Q_A and Q_D). Each switch's collector-emitter voltage is shown with respect to both the load current and the source current through the input choke. Because Figure 4.6.1 can only supply a broad prospective of how the collector-emitter potential of the "hard" turn off device Q_A and the "soft" turn off device Q_D varies. Figures 4.6.2 and 4.6.3 supplement the information in Figure 4.6.1 on more expanded scales.

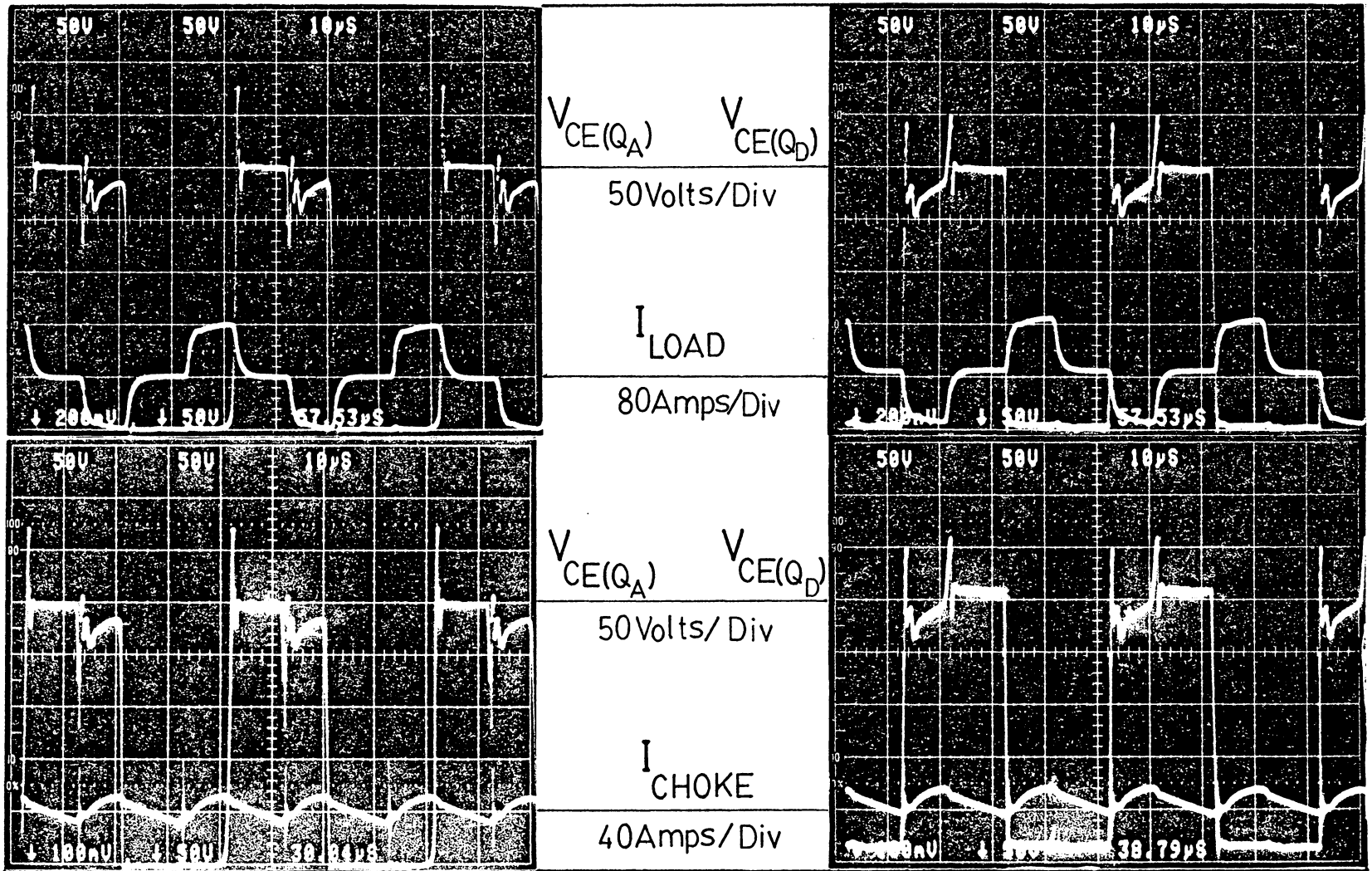


Figure 4.6.1 Full-Bridge Operation, Clamped Mode (250^{V}, 80^{A})

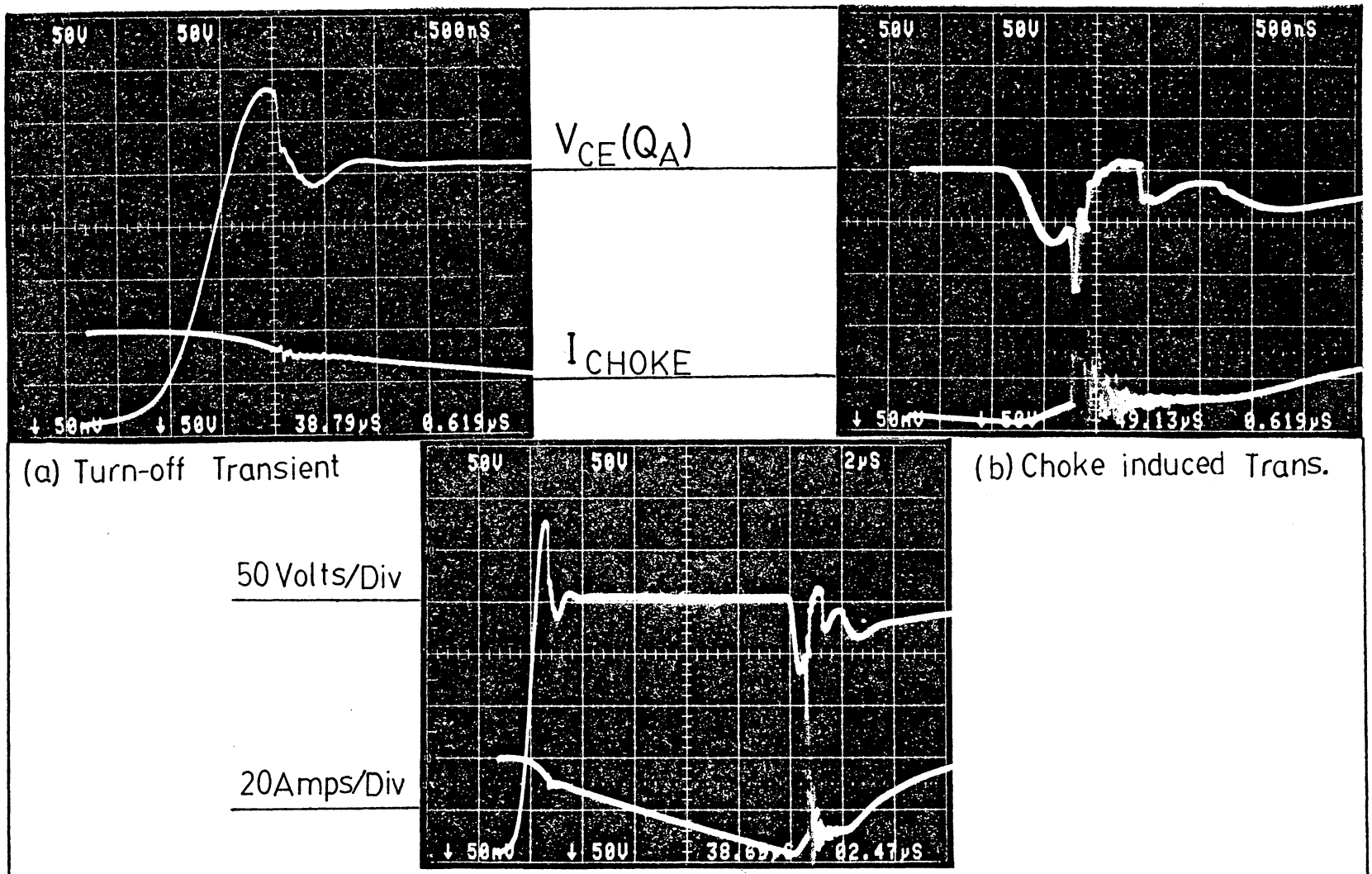


Figure 4.6.2 Collector Emitter Potential of Q_A at Turn Off (Hard)

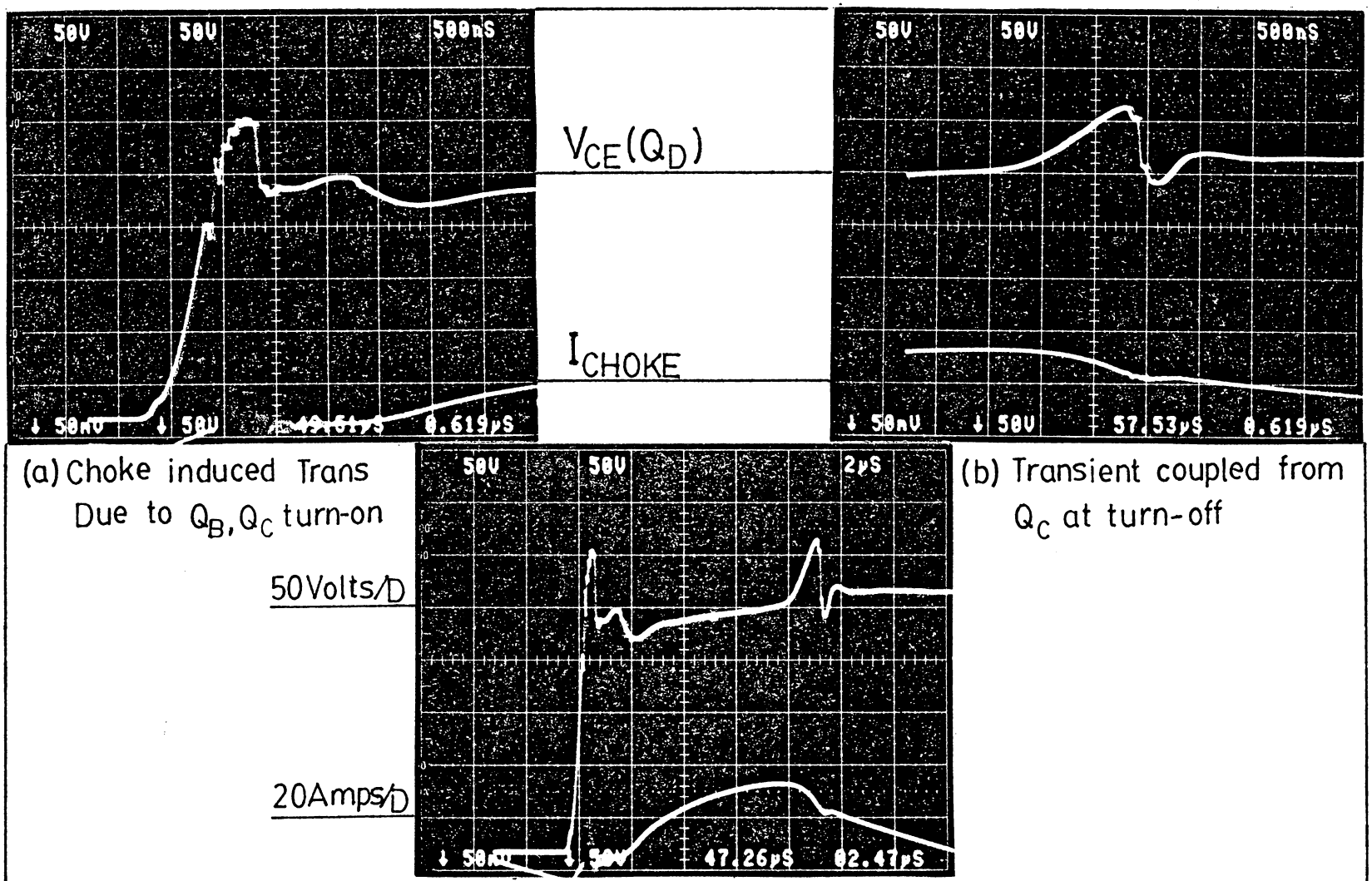
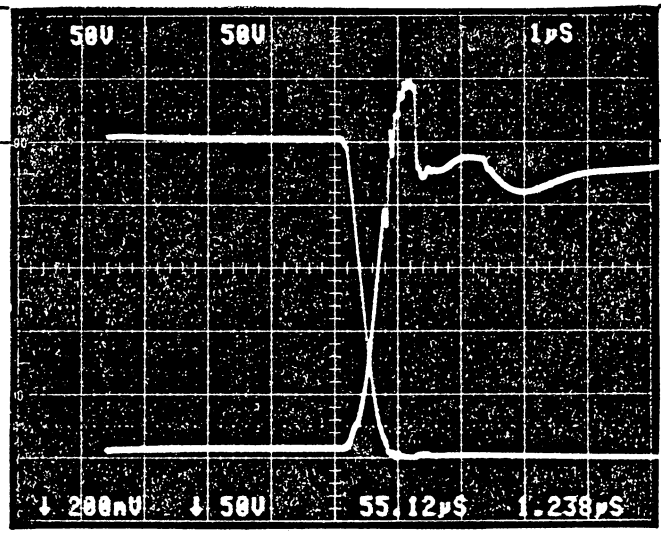
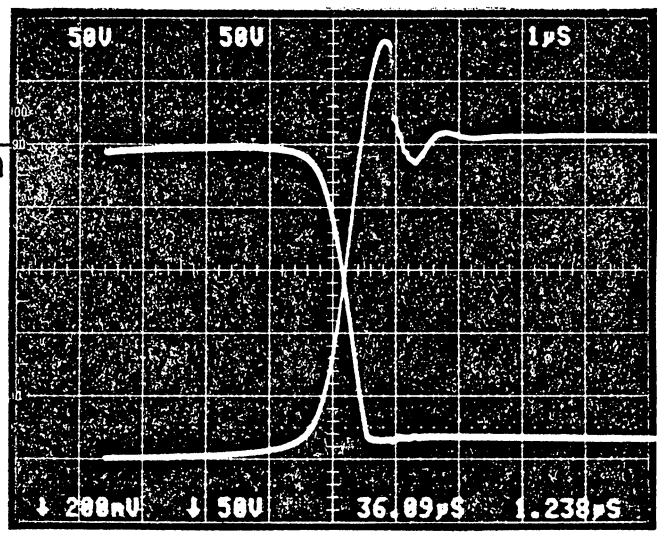


Figure 4.6.3 Collector-Emitter Potential of Q_D at Turn-Off (Soft)



$V_{CE}(Q_B)$
Turn-on

$V_{CE}(Q_D)$
Rising to Source



$V_{CE}(Q_C)$
Falling from Source

$V_{CE}(Q_A)$
Turn-off

SCALES

V_{CE} 50 Volts/Div

Figure 4.64 Voltage Crossover Waveforms (between Q_A, Q_D & Q_C, Q_B)

Starting with Figure 4.6.1 and 4.6.2 the "hard" turn off at Q_A has a more significant voltage transient than Q_D. Recalling the ideal behavior for the RCD snubber network in section thirteen of Chapter Three, transistor Q_A turns off in a similar fashion. Initially, Q_A's snubber capacitor is charged linearly to the supply voltage at which point Q_A continues to charge due to stray circuit inductance in a resonant fashion. Looking at the upper left hand photograph in Figure 4.6.2 gives an expanded view of this phenomena. After the peak voltage is reached the snubber diode current of Q_A attempts to reverse and snaps the diode off resulting in the rapid decrease of the collector-emitter potential. The small RC snubber around the snubber diode damps the later portion of the V_{CE} waveform. On both the center photograph and the photo in the upper right hand corner of Figure 4.6.2 there is a second fluctuation of Q_A's collector-emitter potential. Since Q_A is turned off first and blocks the entire source voltage, any change in the source voltage will be reflected in the potential of Q_A. What is occurring in this case is the turn on of Q_C followed by the turn on of Q_B. As these devices turn on the load current and simultaneously the choke current increase causing an L di/dt induced drop in the voltage applied to the bridge. The potential across Q_A once again

varies in a resonant manner but in this case the voltage is clamped by the d.c. supply and cannot rise significantly above the source.

Looking at Figures 4.6.1 and 4.6.3, there are two voltage transients in the "soft" turn off Q_D waveform. Explaining the cause of these two different transients is slightly involved. As stated earlier, the "soft" turn off device blocks little or no applied voltage at turn off. It is only when the upper device Q_B turns on that the collector-emitter voltage of Q_D will rise. This voltage also rises in a manner analogous with the RCD behavior explained in Chapter Three. One thing to note is that the first transient associated with Q_D (Fig. 4.6.3) is induced in a similar fashion to the second transient associated with the "hard" turn off device Q_A. As the other pair of power switches (Q_C followed by Q_B) are turned on, the current rises sharply and the input choke prevents the full source voltage from being applied to the load. As the rate of rise of load current levels off, the voltage applied to the device Q_D and also the load rises toward 250 Volts ($V_{SOURCE} = 250^V$).

The second transient shown in the upper right hand photograph of Figure 4.6.3 occurs when Q_C turns off. Q_C is located horizontally to Q_D in the bridge. As Q_C turns

off experiencing hard turn off, the path including the load inductance is clamped by Q_B and the anti-parallel diode of Q_A. Thus in an idealistic sense Q_C and Q_D must experience the same potential variation because they are connected to a common circuit node i.e. the load is shorted by Q_B and anti-parallel diode D_A.

Figure 4.6.4 shows the change in potential across the legs of the bridge inverter. The upper photograph is the transistion where device Q_B is turning on and device Q_D having been previously turned off is required to block the full source potential less whatever voltage is dropped across the input choke. The lower photograph is the transistion where Q_A turns off. It does so under high current conditions and the voltage Q_C directly beneath Q_A falls since Q_D is still conducting. As the potential on Q_C falls Q_A rises to block the full supply voltage.

4.7 Turn-On Phenomena in the Full-Bridge

Normally the reverse recovery of the anti-parallel diodes in the bridge and of the free wheeling diode anti-parallel to the input choke could be potentially destructive to the transistors in the bridge during turn on. However, due to the extremely fast soft reverse recovery of the diodes used (Westinghouse R502) this problem was eliminated in the bridge inverter [5].

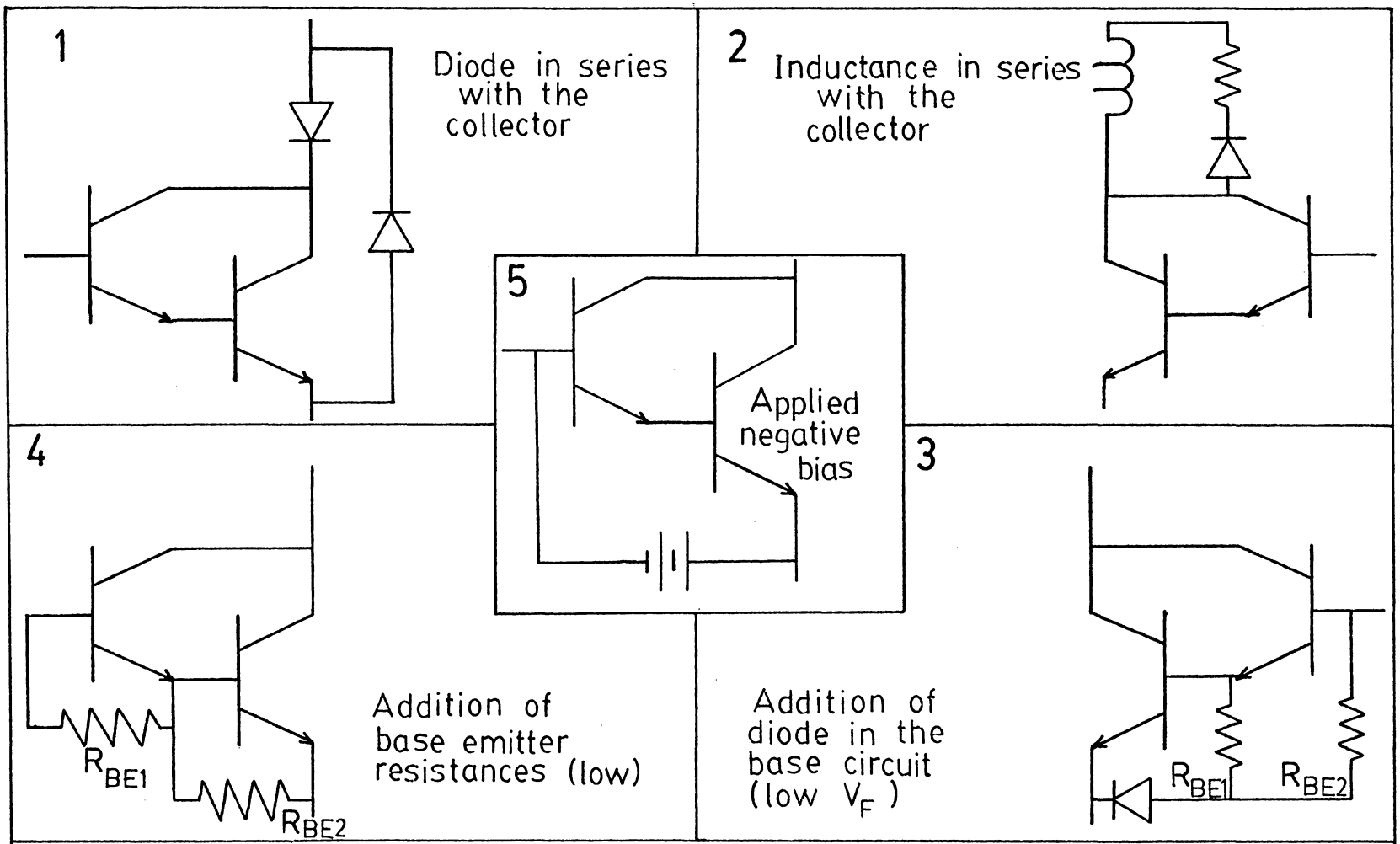


Figure 4.7.1 Five Methods of Suppressing dV/dt Turn-on

A second possible difficulty at turn on is caused by the snubber capacitor dumping current through the Darlington pair at turn on. A quick calculation shows that this current would be no more than about fifteen Amperes. ($V_{CAP} = 300^{V}$ $R_{SNUBBER}$ - 25 is 12^{A}). In this case the additional snubber current would not constitute a serious threat to the devices in the bridge.

By far the most serious problem to be dealt with in the full bridge inverter is the dv/dt initiated turn on of the BJTs. This spurious turn on problem is related to the feedback capacitance C_{ob} associated with all power transistors and the problem is aggravated by several bridge characteristics. The faster the device turns on the greater the dv/dt and corresponding regenerative current from the collector into the base circuit. Additionally since the bidirectional switches of the bridge are rather imperfect the current flows entirely through the transistor in the forward direction but is shared by both the anti-parallel diode and the Darlington in the other. Because of the transistor's reverse conduction it contains a larger store of charge than when in a totally quiescient state and this charge can supply the temporary currents necessary to reinitiate turn on. Finally because Darlington power switches were utilized the higher gain makes it far easier

for a small feedback current to turn the switch back on [5, 19].

Redoutey has suggested five possible methods of lessening dv/dt effects (see Fig. 4.7.1), three of which were utilized to some extent in the full-bridge inverter [4]. The first technique used is the placement of a small resistance parallel to the base-emitter junction. This has the effect of shunting any collector to base capacitive current away from the device. Recall that resistances were added to the Darlington earlier for leakage current stabilization purposes. A slight conflict occurs because the resistance also allows the transistor to conduct in the reverse mode through the resistor and the collector base diode [4].

If reverse currents are not allowed to flow through the transistor by placing a diode in series with the collector the dv/dt problem is curtailed. dv/dt effects are must less pronounced when the transistor is isolated from reverse condition [4].

A low voltage drop diode (Schottky for example) can also be placed parallel to the base emitter junction in series with the base-emitter resistance. Once again this limits the transistor's reverse conduction and dv/dt susceptibility. The potential drop must be low or the effect of the base-emitter resistance is cancelled and the transistor operates as if neither component were present [4].

The fourth way to prevent dv/dt turn on is to reverse bias the emitter-base junction of the power switch. This lessens the effective capacitive feedback current when a sudden change in collector-emitter potential occurs. Also the reverse bias source provides a more desirable path for these feedback currents since the emitter is at a higher potential than the base [4].

Finally, a protective choke in series with the collector (such as the input choke used here) prevents dv/dt effects. Additionally the choke limits turn on switching stress. The manner in which the inductance works is to share any sudden changes in potential when a switch in the bridge is turned on [4].

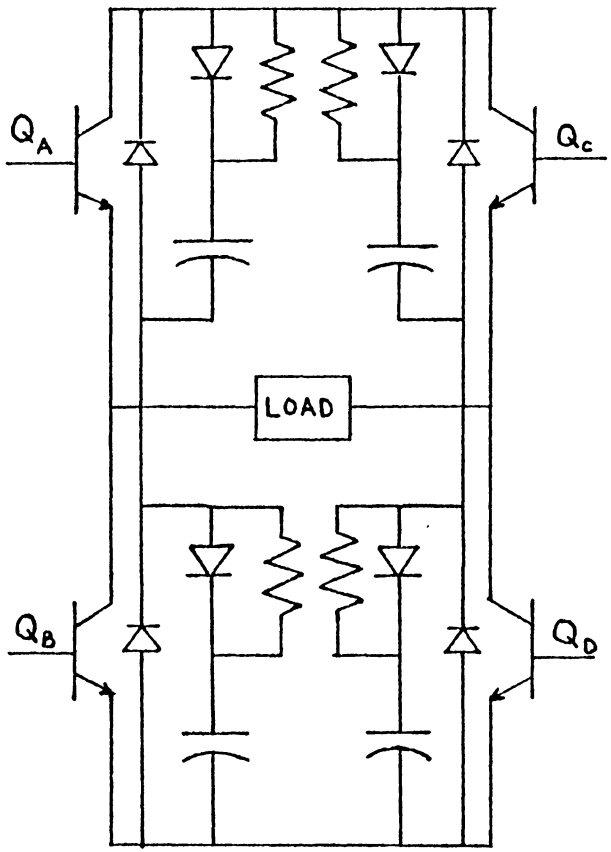
In this project a thirty ohm resistor was placed in the base-emitter circuit of the driver and an eleven ohm resistance was employed parallel to the power transistor's base-emitter junction. Second, a reverse bias potential of seven Volts was applied to the two devices during their turn off interval. Finally, an input choke was connected to the source effectively in series with the upper two switches of the bridge.

4.8 Snubber Network Interactions

Snubber interaction is a problem which is often overlooked in bridge design. To clarify what constitutes a

snubber interaction suppose one transistor's snubber capacitor discharges as another charges so that the total potential across the two networks is constant. If one of the power switches is then turned on the potential variation across the other switch's snubber capacitor can induce a dv/dt generated high current through the capacitor and the device which is turning on (see Fig. 4.8.1). This reciprocal interaction is especially prevalent when polarized RCD snubbers are utilized in a bridge or totem pole configuration.

Figure 4.8.2 displays photographs of the inverter power switch collector-emitter voltages (each shown relative to the forty Ampere load current). The snubbering technique employed was a polarized RCD snubber with a .3μF capacitor. Operating in the clamped mode at one hundred and fifty Volts the waveforms show that Q_A's (Q_B's) collector-emitter voltage rises or falls in opposition with Q_C's (Q_D's) collector-emitter voltage. Looking at the waveforms on the left in Figure 4.8.2 the key points to note are those when no load current is flowing. Immediately after the load current falls to zero the charge across the snubber capacitors begins to change with an RC time constant, i.e. the switches, Q_A and Q_C, attempt to share in blocking the applied source voltage. Then in the region directly



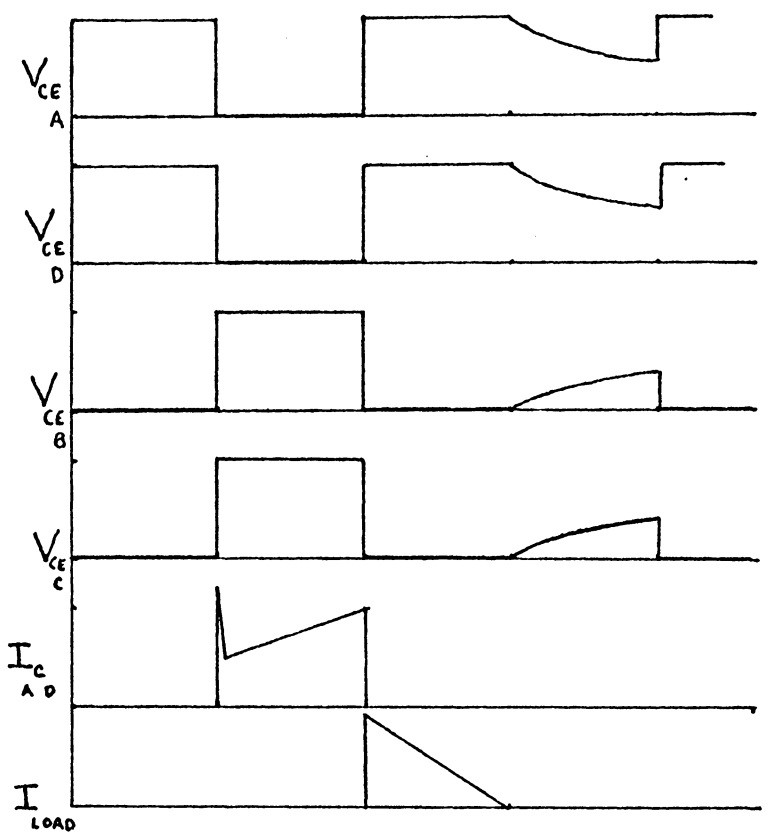


Figure 4.8.1 Snubber Circuit Interaction

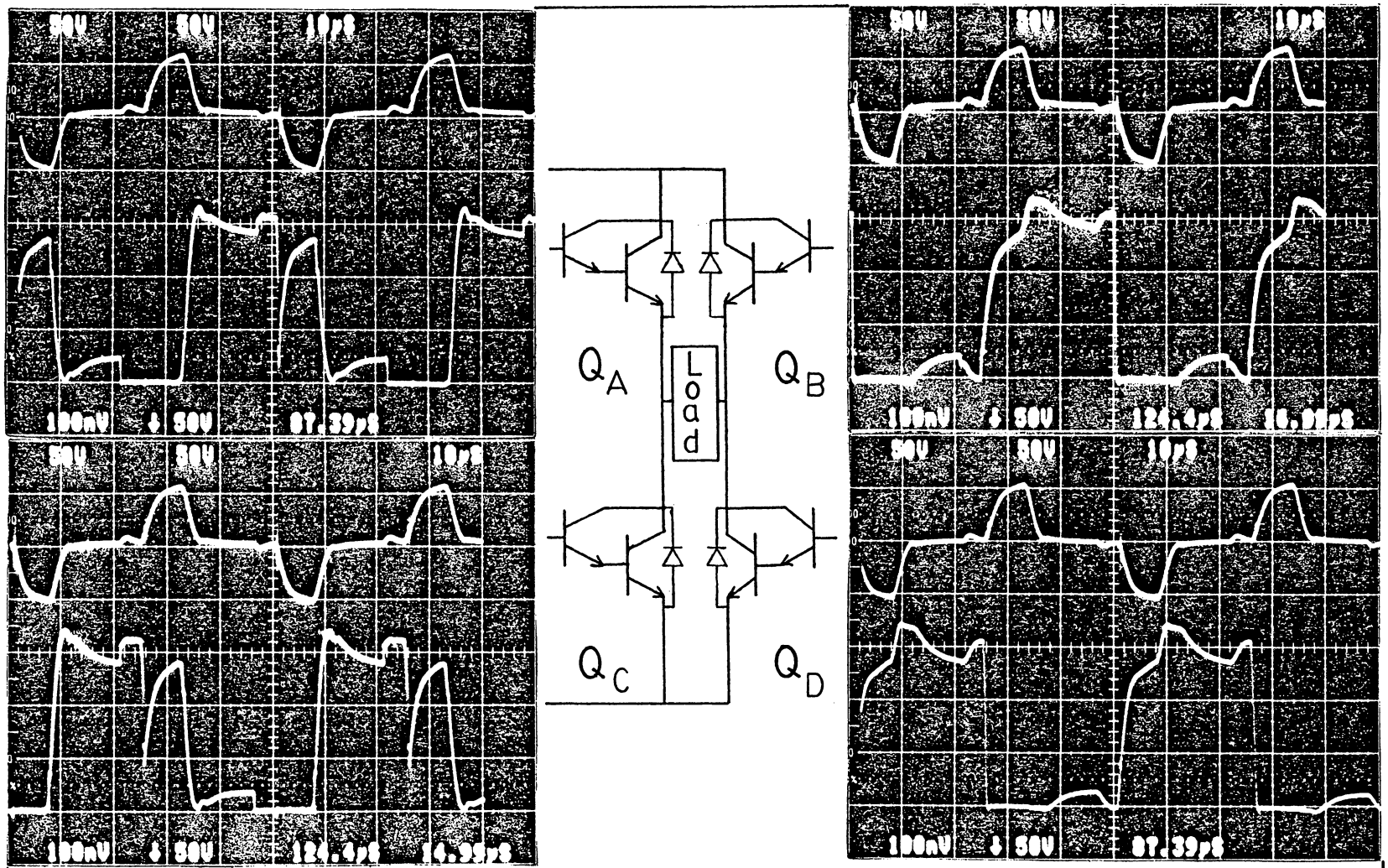


Figure 4.8.2 Full-Bridge Inversion With Snubber Interaction

preceding load current conduction that is characterized by a small hump in the current transistor Q_A is turned on. The voltage variation across the snubber capacitors of Q_A and Q_C is abrupt because Q_A is turned on first. Recall the drive waveforms are offset for Q_D and Q_B in the clamped mode. The instantaneous change in capacitor voltage is translated into a high current through transistor Q_A which is turning on. The small current flowing through the load is caused by Q_B's snubber discharging back through the load.

Empirically it is observed that one pair of switches (Q_B and Q_D) do not experience instantaneous dv/dt's. In addition looking back at Figure 4.6.1 where an RCD snubber was also employed with a .1μF capacitor the interaction problem is not present. Thus the snubber problems may be reduced by choosing components of an appropriate value.

4.9 Achievement of Our Goal

Figure 4.9.1 provides a photograph of the bridge operating at 270 Volts and 110 Amperes. In practice this was near the highest level obtained without switch failures. Twice while operating in the 270 Volt, 120 Ampere region D7ST power transistors were destroyed. In one instance it was the two soft turn off devices which were destroyed. While not mentioned earlier the devices which turn off last operating in the clamped mode have a storage time which may

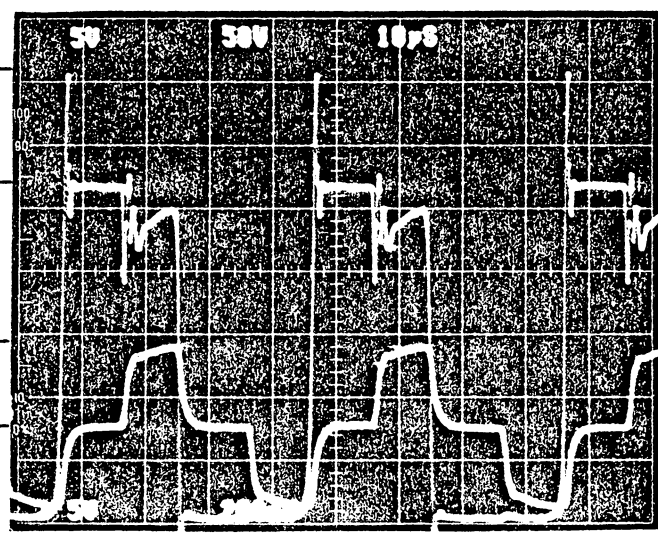


Figure 4.9.1 Full Bridge Operation
(27kh$_z$, 270Volt, 110Amps)

be 20% greater than the hard turn off device's storage time (5.5 microseconds versus 4.5 microseconds). This is caused by the fact that charge is swept out of the collector-base regions much faster operating under high collector currents than lower valued ones. The asymmetry of device storage times for clamped mode operation can severely complicate operation at high frequencies.

In a second instance a single D7ST device on the hard turn off side of the bridge failed when operating the full bridge at a high power level with the active voltage clamp circuit mentioned in Chapter Three. Perhaps in this case the abrupt dv/dt generated on the falling edge of the voltage clipped transient caused a brief false turn on related failure.

As a conclusion for this chapter the bridge-inverter was tested thoroughly in half bridge and full bridge operation. A comprehensive design of base drives, base drive logic, over-current protection and switching aid networks took place. dv/dt turn on and snubbering interaction were discussed in relation to our experience with these problems in the inverter.

CHAPTER FIVE

CONCLUDING REMARKS AND RECOMMENDATIONS

The author hopes that this thesis has provided some keen incite into the realm of high power inverter technology. Problems such as switching speed and storage time effects encountered in device and drive selection are not restricted to inverters or bipolar junction transistors. Still later the dv/dt and snubbering interactions confronted in full-bridge operation will be confronted in most state-of-the-art, high-frequency, high-power conversion circuits especially those required to switch power levels as high as thirty-kilowatts with switching frequencies approaching thirty-kilohertz.

Parasitic behavior within the circuit becomes important as stray inductance begins to cause severe transient voltages. The reverse recovery of the anti-parallel diodes in the bridge may not be a severe problem at low frequencies. At high frequencies the repetitive nature of the reverse recovery current can cause overheating and degradation or failure of components.

The experienced designer must learn to deal effectively with each application. Generally there are no hard and fast rules applicable to every high-power project. There are no perfect switches either. For example, FETs are being constructed. FETs do not have the storage time problems

associated with BJTs because they are unipolar devices. Yet most power FETs do have a built in anti-parallel diode which causes reverse recovery problems. On the other hand, the BJTs used here have storage time problems especially operating in the clamped mode at thirty-kilohertz. The storage time of the Darlington power switches was observed to be between four and six microseconds. Clamped mode operation at high frequencies does not allow much dead time for clearing the stored charge. The maximum dead time between conduction of Q_A and Q_C (Q_B and Q_D) was about five or six microseconds depending on how close to thirty-kilohertz the inverter was operated. Shoot-through destruction occurred if the storage time of all the power switches was not minimized.

The advantages of utilizing d.c. to quasi-squarewave inverter modules to synthesize a stepped sinusoidal output are notable. Low distortion andharmonic content coupled with high reliability is obtained. Each module is very efficient and this high efficiency is reflected in the resulting d.c. to sinusoidal system. An LC filter is not required to smooth the output as the antenna of the transmitter performs this function.

Full-bridge inverters have some distinct advantages and disadvantages relative to other forms of inversion. The simple output transformer, low voltage applied to the transistors and ease of filtering are favorable factors. On

the other hand the complications posed by the switching aid networks, the isolated base drives and risk of simultaneous conduction are not desirable. Some precautionary measures were taken to deal with these problems. The base drive circuits were optically coupled and isolated. Logic function design was performed carefully to lessen the possibility of shoot-through and components were arranged in a short symmetrical layout to prevent unnecessary voltage transients. An over-current protection circuit was implemented in a closed loop fashion from the power stage to the base drives.

Within the bridge the Darlington transistor proves to be an excellent switch coupling reliability and performance. The designer must overcome ambiguities associated with snubber design. Substantial effort is required to insure the switching elements safe operation.

The major goal of this project was to develop a thirty-kilowatt, thirty-kilohertz, full-bridge inverter module and it is reasonable to ask how the end product stacked up against this goal. In answer to this the inverter module developed here is implemented in the full-bridge configuration. It is also quite capable of thirty kilohertz operation but the output power level achieved was only about sixteen kilowatts. While the design goal of thirty-kilowatts has not been achieved never the less the development and investigation has been thorough. Investigation suggests that straight inverter operation may be more

desirable than clamped mode operation at high frequencies due to the physical limitation of the power devices. The asymmetry of switch storage time coupled with the shorter available dead time to reduce stored charge in the clamped mode will continue to cause difficulties.

The author hopes both that this project has been informative to his reader and that the project will evolve into a useful stage in the development of a high power VLF transmitter. The question of the technique used to obtain this goal is left open. Either lower power modules operated in the clamped mode or high power modules operated in a straight inverter fashion are recommended.

FOOTNOTES

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DESIGN CONSIDERATIONS OF A THIRTY-KILOWATT, THIRTY-KILOHERTZ, FULL-BRIDGE INVERTER FOR APPLICATION IN A VERY-LOW-FREQUENCY COMMUNICATIONS SYSTEM

by

Philip David Wesel

ABSTRACT

A thirty-kilohertz thirty-kilowatt full bridge inverter design is presented. The inverter module forms an integral part of a very-low-frequency transmitter for a submarine communications application. Device selection and drive selection as well as testing data for inverter clamped mode of operation are presented.