3. FUNDAMENTAL VOLTAGE BALANCING ANALYSIS FOR FLYING CAPACITORS

3.1 INTRODUCTION

In this chapter, fundamentals of the proposed soft-switching multilevel inverter for active power filter applications are investigated and discussed with the voltage balancing for flying capacitors. Voltage balancing in the flying capacitor multilevel inverter (FCMI) is very important in maintaining the voltage balancing between the flying capacitors for a safe operation. This means that the flying capacitor voltage should be stable at any operational conditions. For that purpose, the inverter theoretically requires the symmetric switching of control signals with a phase shifting. In spite of the symmetric control scheme, a voltage unbalance of the flying capacitor in practical implementations may be observed due to unequal parameters of the inverter caused by 1) different IGBT tolerance, 2) different dv/dt, 3) different value of C_f, etc [D33].

In this study, voltage balancing of the flying capacitor as well as the DC link capacitors under soft-switching operations is characterized through both simulation and experimentation.

3.2 FUNDAMENTAL ISSUES OF VOLTAGE BALANCING

3.2.1 Flying Capacitors

A voltage balance of a flying capacitor means that the two inner devices can then be clamped like that of the conventional two-level inverter. However, voltage unbalances may be

observed under the different component behaviors and packaging techniques in practical circuits, in spite of the self-balancing of the capacitor voltage at a given switching cycle.

Fig. 3.1 shows the capacitor voltage waveform of the single-phase inverter under soft-switching operations. As expected, the capacitor voltage divergence is observed at simulation, because of the reasons mentioned above. Unlike the single-phase inverter, a three-phase inverter will be kept at a more stable clamping voltage, because the flying capacitor voltage fluctuates only every 60° cycle.

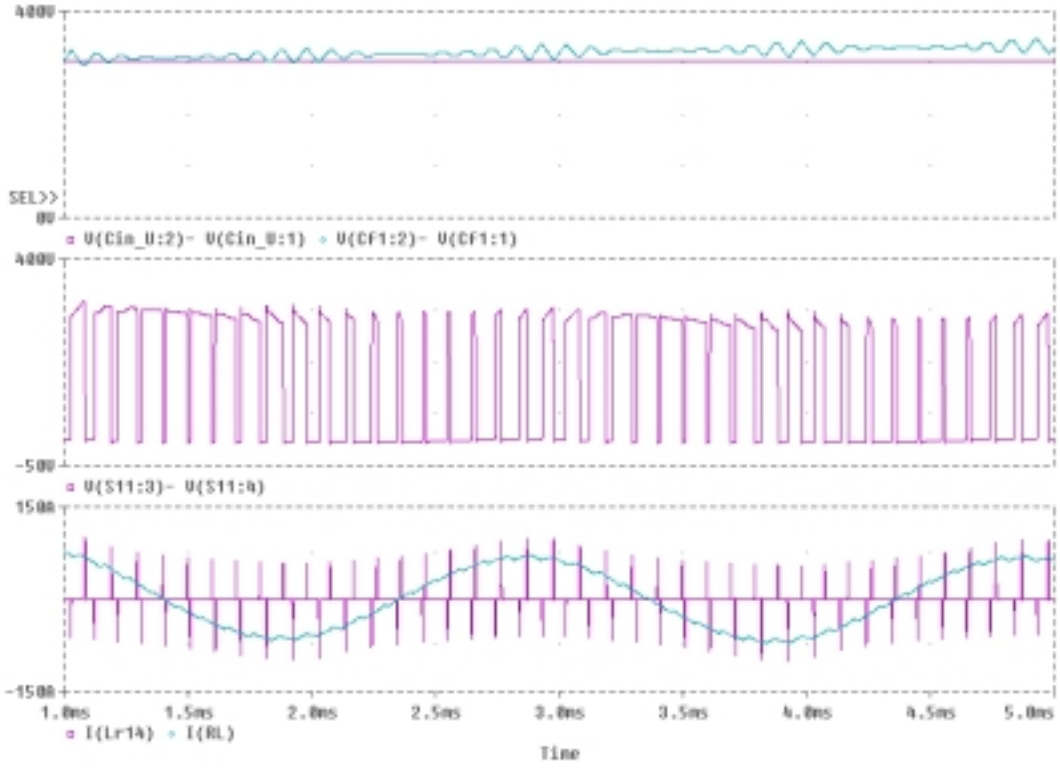


Fig. 3.1 Unbalanced flying capacitor waveforms under soft-switching operations.

3.2.2 DC Link Split Capacitors

In general, an auxiliary resonant commutate pole (ARCP) topology [C4] has a limitation of voltage balancing among their split capacitors because of the fluctuation of the floating center-tap potentials. Such a fluctuation of dc link voltage causes a difficulty in the auxiliary circuit control. Although the proposed inverter is similar to an ARCP soft-switching circuit structure, the inverter can overcome the limitation of the voltage balancing problem between the dc link capacitors using self-balancing. For validation, simulations as shown in Fig. 3.2 were performed to verify the self-balancing of a dc link capacitor. The ripple voltage of the capacitor under pulse-width-modulation (PWM) switching was observed to be constant during the period of a load current frequency. The result indicates that the voltage across the dc link capacitor was self-balanced over a fundamental cycle, without any additional control scheme.

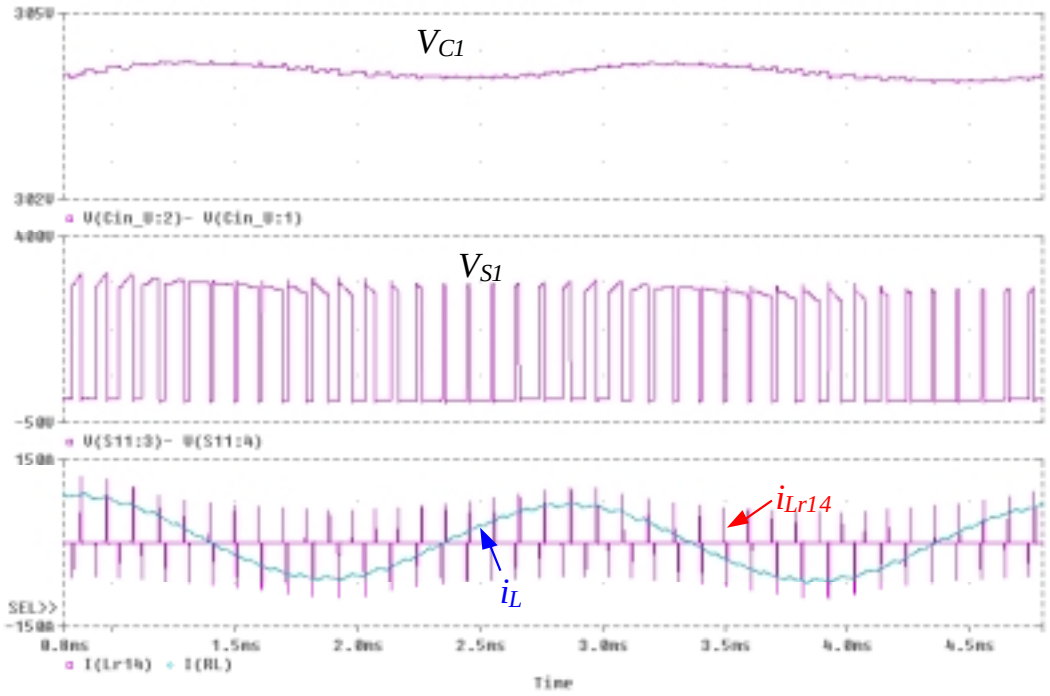


Fig. 3.2. Self-balanced waveforms of a dc link capacitor under PWM switching.

3.2.3 Voltage Synthesizing

It is well known that the voltage synthesizing method in the FCMI influences the voltage balancing of the flying capacitors. With an independent control between switching cells, the FCMI has an attractive feature of control flexibility that has multiple switching patterns. It results in better performance of the inverter by optimizing the switching pattern. Recently, an optimum switching pattern was studied for solving the voltage balance problem. The attempts in [E16] and [E17] have been started with each switching state producing the same output voltage but different directions of the current in the flying capacitor. The flying capacitor can be balanced regardless of the load current. However, in a practical system, in conjunction with the voltage synthesizing, the voltage control loop is required to maintain a charge balance between flying capacitors.

3.3 Analysis Of Main Circuit And Its Modulation

Considering the fundamentals of voltage unbalance and voltage synthesis in the FCMI, solution strategies for the fundamental problems are introduced and analyzed in the following.

3.3.1 Circuit Analysis

A half-bridge 3-level flying capacitor inverter as shown in Fig. 3.3 consists of two two-level switching cells; the inner loop cell ($C_f \rightarrow S_2 \rightarrow S_3$) and outer loop cell ($C_1 \rightarrow S_1 \rightarrow C_f \rightarrow S_4 \rightarrow C_2$). These cells are controlled by different modulation indexes, d_1 and d_2, at a given switching frequency under their phase shifting. In order to characterize voltage balancing at the steady-state, the current through the flying capacitor should be averaged to zero during each cycle. The stability will be guaranteed under any conditions if the average capacitor current is zero.

Assume that the load current is constant during a switching cycle; the capacitor current is expressed as:

$$i_{cf}(t) = (d_1 - d_2) \cdot i_L(t) \tag{3-1}$$

where, d_1 and d_2 are the instantaneous duty cycle of switch pairs, S_1-S_3 and S_2-S_4, respectively. If $i_{cf}(t) = 0$, or $d_1 = d_2$, the steady-state stability over a fundamental cycle is satisfied with $< i_{cf} > = 0$. For the safe operation of the inverter, the dynamic voltage balancing in the transient state is very important. In this regard, the voltage balancing is analyzed and discussed for self-balancing in the start-up condition. The output voltage is as follows:

$$\begin{aligned} V_{AN} &= V_{S3} + V_{S4} \\ V_{AO} &= V_{AN} + V_S/2 \end{aligned} \tag{3-2}$$

where, $V_{S3} = (1 - d_1) \cdot V_{cf}$, $V_{S4} = (1 - d_2) \cdot V_{cf}$. The variation of the output voltage reflects the output current ripple so it influences the variation of the flying capacitor current. Thus, the capacitor current variation is expressed as:

$$\Delta i_{cf}(t) = \Delta i_L(t) \cdot (d_1 - d_2) \tag{3-3}$$

From (3-3), it can be concluded that the capacitor current variation is a function of the load current variation and switching functions of the two cells. In addition, the flying capacitor voltage is characterized with the time response of the capacitor voltage when the switching action is activated. Prior to switching, the voltage has zero value. The flying capacitor current can be expressed as below. The flying capacitor current can be assumed as follows,

$$\Delta i_{cf}(t) = (V_S/2 - V_{Cf}(t)) \cdot K \tag{3-4}$$

where, K is the conductance at the harmonic frequency. From (3-4), the capacitor current can be derived from the flying voltage variation as:

$$(\frac{V_S}{2} - V_{Cf}(t)) \cdot K = C_f \cdot \frac{dV_{Cf}(t)}{dt} \tag{3-5}$$

$$V_{Cf}(t) + \frac{C_f}{K} \cdot \frac{dV_{Cf}(t)}{dt} = \frac{V_S}{2} \tag{3-6}$$

Solving for V_{Cf}, the capacitor voltage is expressed as:

$$\begin{aligned} V_{Cf}(s) + \frac{C_f}{K} \cdot s \cdot V_{Cf}(s) &= \frac{V_S}{2} \\ V_{Cf}(s) &= \frac{V_S}{2} \cdot \frac{1}{(1 + \frac{C_f}{K} \cdot s)} \end{aligned} \tag{3-7}$$

From (3-7), it is concluded that the dynamic of the flying capacitor voltage has a typical first order characteristic. Fig. 3.4 shows the capacitor voltage dynamics under different initial voltages at start-up. The voltage reaches the final value of $V_S/2$ at steady state. The voltage rising is corresponding to the time constant associated with a given flying capacitor capacitance and trans conductance, C_f/K. As expected, both results of the numerical simulation and Pspice simulation indicate that the flying voltage achieved self-balancing at transient state.

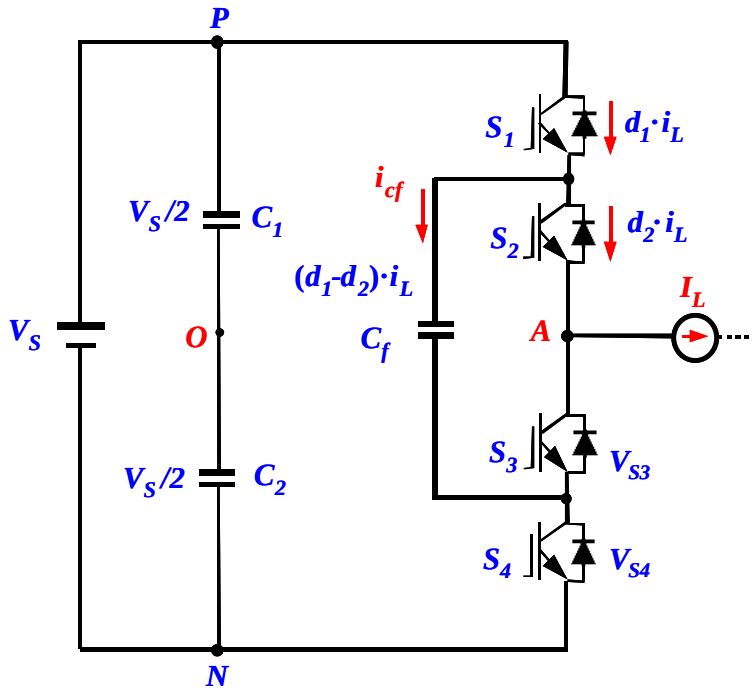
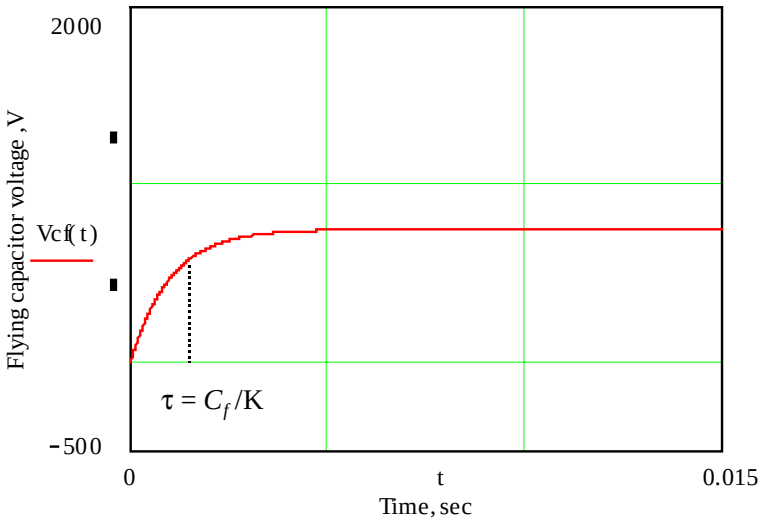
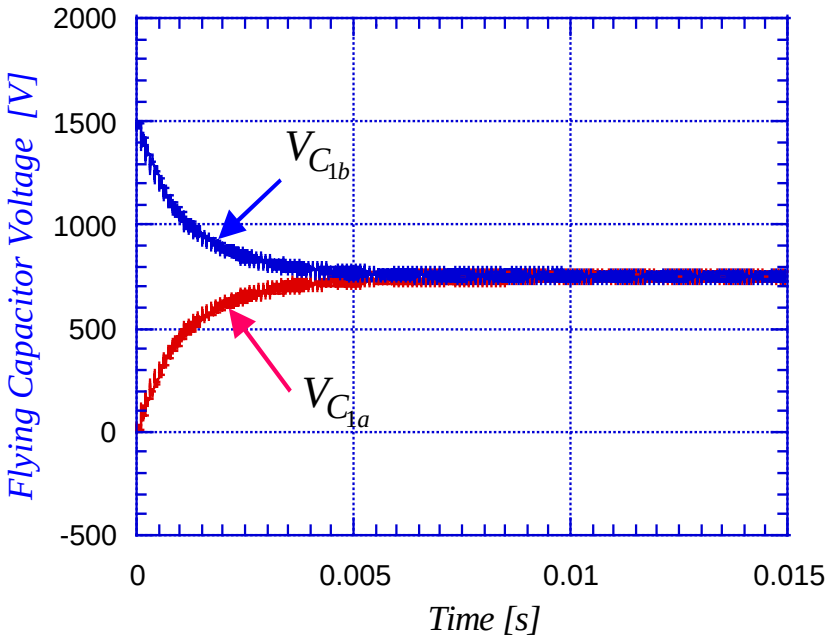


Fig. 3.3. Configuration of a half-bridge 3-level inverter with a flying capacitor.



(a) Numerical calculation



(b) P-spice simulation

Fig. 3.4. Simulated capacitor voltages at start-up.

On the other hand, the voltage across the flying capacitor depends on the capacitance of the capacitor and the ripple current through the capacitor. Assume that the load current is constant during each switching cycle.

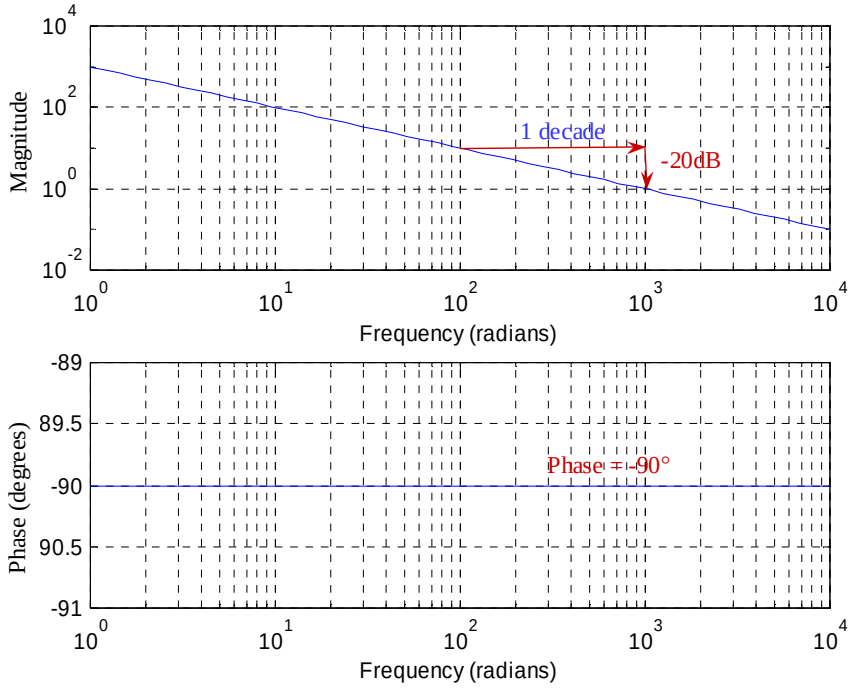
$$\Delta i_{Cf} = m(t) \cdot \Delta I_L = C_f \frac{dV_{cf}}{dt} \tag{3-8}$$

Thus, the transfer function of the flying capacitor can be expressed.

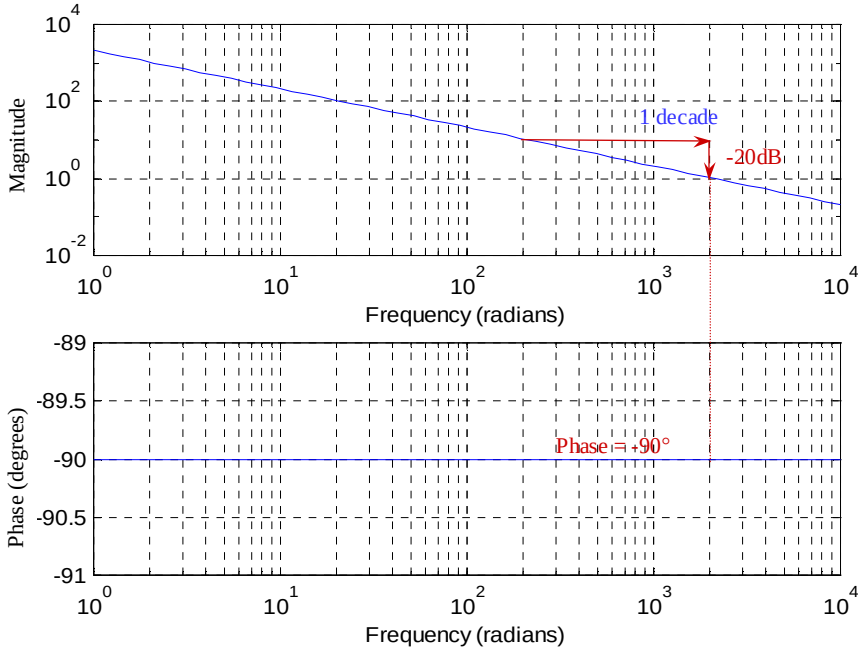
$$\frac{V_{Cf}(s)}{d(s)} = \frac{I_L}{s \cdot C_f} \tag{3-9}$$

It is concluded that the behavior of the flying capacitor voltage acts as an integrator. So the equivalent circuit looking V_{cf}(s) /d(s) is a buck converter. Since the transfer function has an

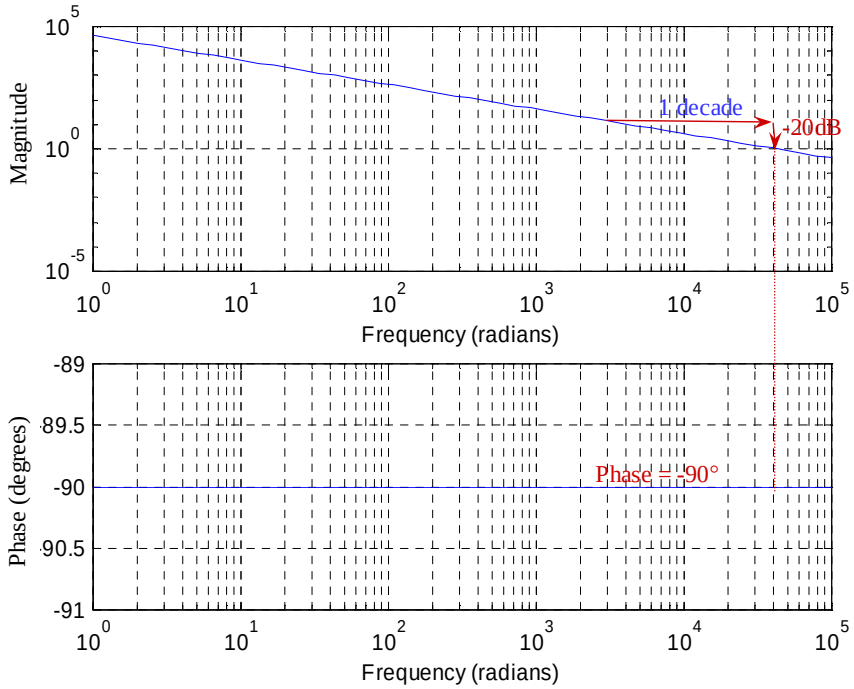
integral term, the *s* is only raised to the first power. If the load current and modulation are constant, the frequency responses of the capacitor voltage under different parameters can be plotted as shown Fig.3.5. The Bode diagrams compose of two curves for the open-loop transfer function. The *x*-axis of both curves represents the significant frequency. The *y*-axis of the first curve represents the magnitude of the transfer function, and the y-axis of the second curve is the phase (degree). The gain Bode plot in Fig. 3.5 consists of a straight line falling at –20dB/decade. It crosses the 0-dB axis at 1000 rad/sec. Also a first order integral shifts the phase -90° independent of frequency. In order to shift a phase margin from -90°, a feedback controller is required. Depends on the capacitance of the frying capacitor and the load current, the different zero crossing frequencies are obtained from the frequency response of the transfer function in (3-9); C_r = 1000μF and I_L = 1A for Fig. 3.5(a), C_r = 470μF and I_L = 1A for Fig. 3.5(b), and C_r = 470μF and I_L = 20A for Fig. 3.5(c).



(a) C_f = 1000 μF and I_L = 1A



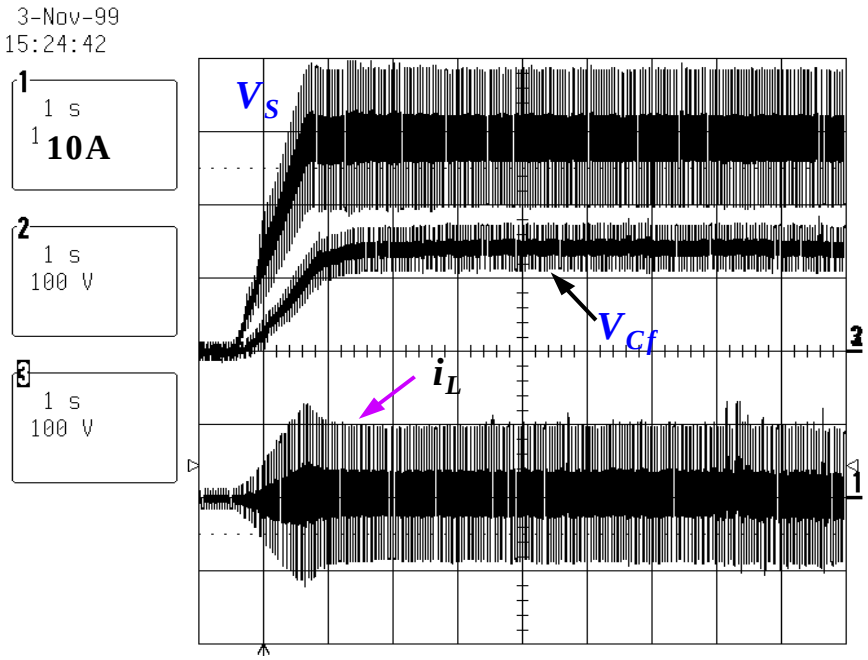
(b) C_f = 470 μF and I_L = 1A



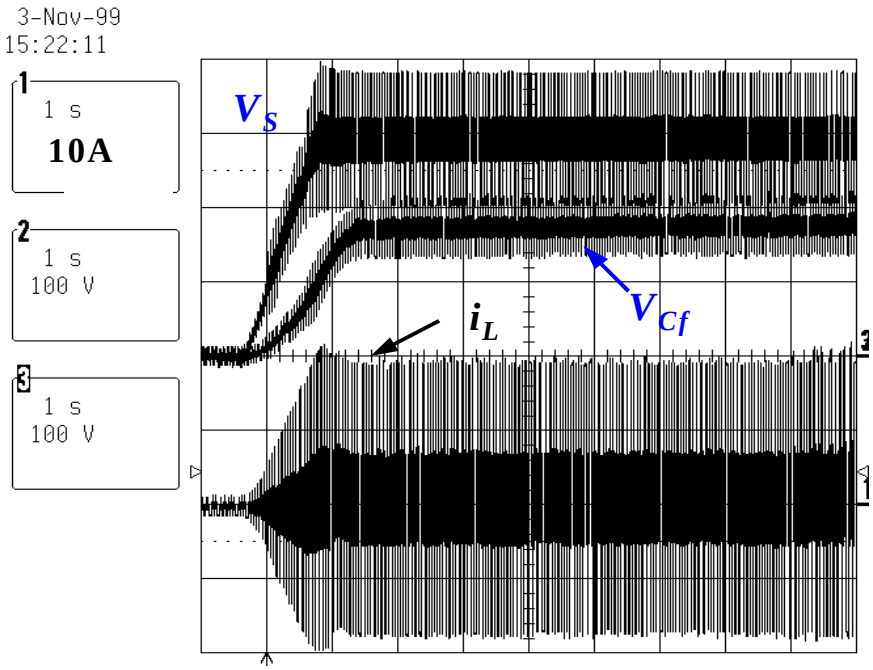
(c) C_f = 470 μF and I_L = 20A

Fig. 3.5 Bode plots of the flying capacitor voltage with open-loop.

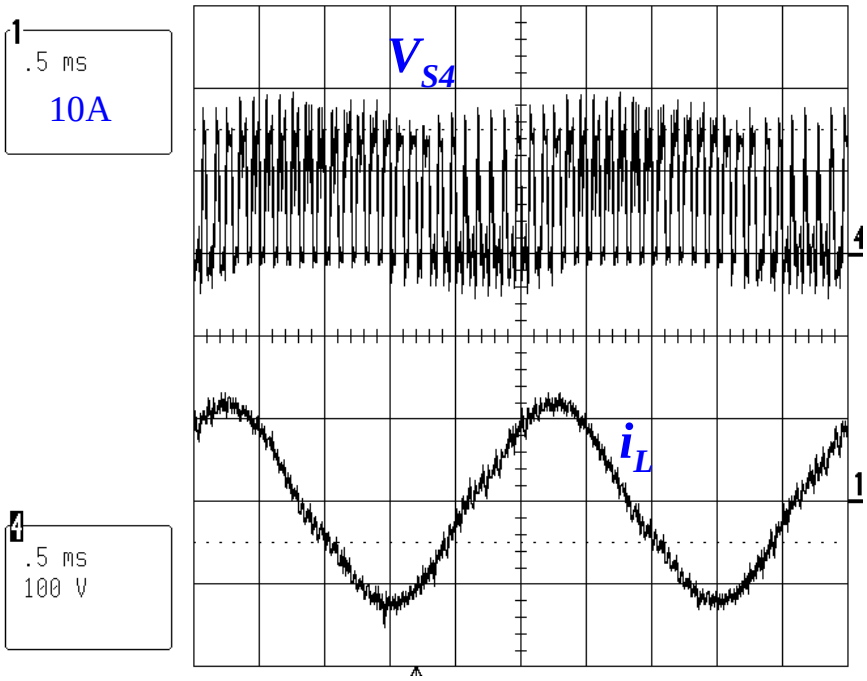
Fig. 3.6 shows experimental voltage and current waveforms of the inverter under different load current conditions. In the case of Fig. 3.6(a), the voltage waveform of the flying capacitor is balanced through both start-up and steady state conditions. The flying capacitor of 470μF is used for the test. However, during the high current case in Fig. 3.6(b), an unbalanced waveform was observed at steady state. The flying voltage V_{Cf} is diverged during inverter operation. The voltage unbalance, as shown in Fig. 3.6(c), influences voltage fluctuation of the switch cell. Furthermore, this can result in a voltage greater than the rates during long periods of operation. As a result, an unbalanced voltage was observed to occur at conditions other than startup. In order to avoid voltage unbalance being diverged, an appropriate scheme of feedback control is required.



(a) Balanced case at a load current of 10 A (V_{Cf} = Vs/2)



(b) Unbalanced case of a load current of 20 A ($V_{Cf} > Vs/2$)



(c) Voltage unbalance waveforms of the main switch

Fig. 3.6. Experimental waveforms of the flying capacitor at start-up conditions.

3.3.2 Voltage Synthesizing Modulations

Unlike the diode flying multilevel inverters, the voltage synthesizing of FCMIs has more switching states at a given voltage level. Table 3-1 represents the possible switching states and their corresponding output voltages of a half-bridge single-phase three-level inverter as shown in Fig. 3.3. In the switching modulation pattern, there are two possible vector sequences for half of the dc source voltage. In regard to switching states that produce the same output voltage but different current direction through the flying capacitor, the capacitors can be balanced regardless of the load current. Such multiple state redundancies provide control flexibility for the voltage balancing of the flying capacitors [E17].

Fig. 3.7 shows a single-phase 3-level inverter for active power filter applications. The circuit consists of eight IGBT switches and two flying capacitors. The topside switches, S_{1a}, S_{2a}, S_{1b}, and S_{2b}, are complementarily turned on and off with bottom-side switches, $\overline{S}_{1a}$, $\overline{S}_{2a}$, $\overline{S}_{1b}$, and $\overline{S}_{2b}$. These switches are independently controlled. Thus, there are sixteen available switching states from four independent switches. For simplification, it is assumed that all switches are ideal operations and the flying voltage between flying capacitors is constant as $v_{cf1} = v_{cf2} = v_{dc}/2$ during a cycle. The switching states of a single-phase 3-level active filter are given in Table 3-2. The output voltage has five voltage levels during each cycle. Unlike Table 3-1, there are a number of redundant switching states to ensure a given output voltage.

Table 3-1. Switching states of a half-bridge single-phase three-level inverter.

Switching States				**Flying Capacitor Current (i_{Cf})**	**Output Voltage V_{AO}**
S_1	**S_2**	**S_3**	**S_4**		
1	1	0	0	0	V_S
1	0	1	0	- i_{Cf} (discharging)	V_S /2
0	1	0	1	i_{Cf} (charging)	V_S /2
0	0	1	1	0	0

* S_1/S_4 and S_2/S_3 are complementary states

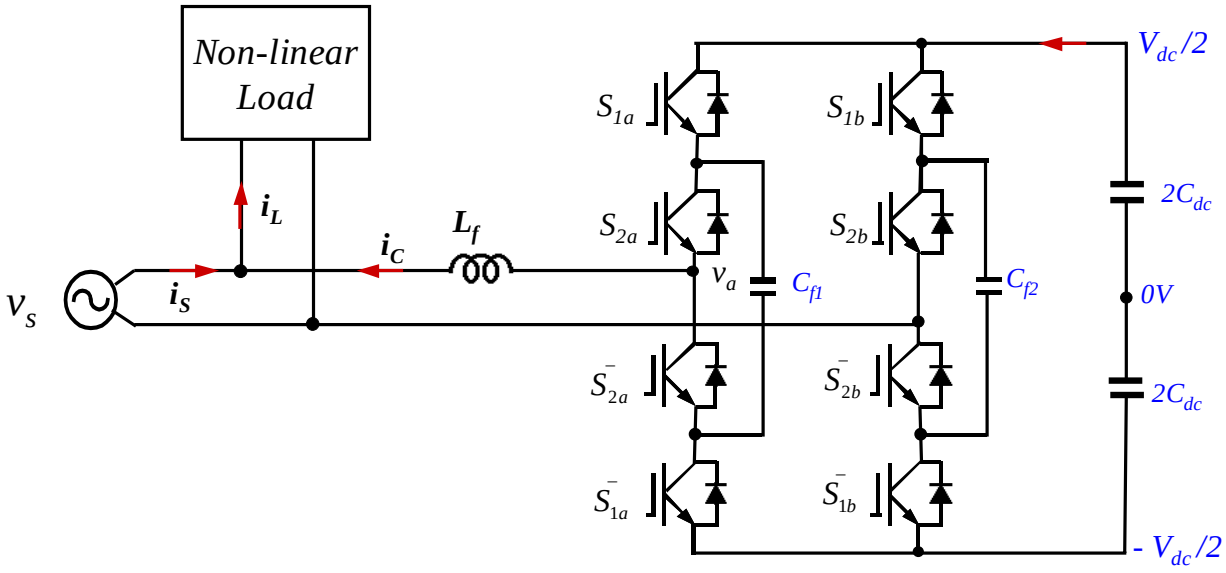


Fig. 3.7. Single-phase 3-level active power filter with flying capacitors.

Table 3-2. Possible switching states of a single-phase 3-level active filter.

Possible switching states				Output voltage related to capacitors	Output voltage
S_{1a}	S_{2a}	S_{1b}	S_{2b}	v_{ab}	v_{ab}
0	0	0	0	0	0
0	0	0	1	$-v_{Cf2}$	$-v_{dc}/2$
0	0	1	0	$-v_{dc}+v_{Cf2}$	$-v_{dc}/2$
0	0	1	1	$-v_{dc}$	$-v_{dc}$
0	1	0	0	v_{Cf1}	$v_{dc}/2$
0	1	0	1	$v_{Cf1}-v_{Cf2}$	0
0	1	1	0	$v_{Cf1}+v_{Cf2}-v_{dc}$	0
0	1	1	1	$v_{Cf1}-v_{dc}$	$-v_{dc}/2$
1	0	0	0	$-v_{Cf1}+v_{dc}$	$v_{dc}/2$
1	0	0	1	$-v_{Cf1}-v_{Cf2}+v_{dc}$	0
1	0	1	0	$-v_{Cf1}+v_{Cf2}$	0
1	0	1	1	$-v_{Cf1}$	$-v_{dc}/2$
1	1	0	0	v_{dc}	v_{dc}
1	1	0	1	$-v_{Cf2}+v_{dc}$	$v_{dc}/2$
1	1	1	0	v_{Cf2}	$v_{dc}/2$
1	1	1	1	0	0

3.4 CHARACTERISTICS OF THE FLYING CAPACITORS

A distinguishing characteristic of the FCMI is that the flying capacitor voltage is required to be stable at any operation condition. It guarantees the voltage stability of the inverter. With voltage stability, the capacitor voltage is subjected to the variation of the load current, even when the average of the current is zero. Thus, the current and voltage ripple of the capacitor is analyzed in this section. As mentioned above, FCMI control signals need an equal duty cycle with a 180° phase shifting for the two-cells. For effective analysis, the rms current can be derived from the load current together with the duty cycle for a given switching frequency.

$$\begin{aligned} i_{Cf(rms)}(t) &= i_L(t)\cdot\sqrt{2\cdot(1-d(t))} && \text{for } d>0.5 \\ i_{Cf(rms)}(t) &= i_L(t)\cdot\sqrt{2\cdot d(t)} && \text{for } d<0.5 \end{aligned} \tag{3-10}$$

where $i_{Cf(rms)}$ is the instantaneous rms current through the flying capacitor, which is solved over the switching cycle. The $i_L(t)$ is the load current and the $d(t)$ is the duty cycle of the two cells and determined by the modulation index $m(t)$ as:

$$\begin{aligned} i_L(t) &= I_a\cdot\sin(\omega_m t+\theta) \\ d(t) &= \frac{1+m(t)}{2} \\ m(t) &= M\cdot\sin(\omega_m t) \end{aligned} \tag{3-11}$$

where i_a is the peak load current, ω_m is the load current frequency, M is the duty amplitude, and θ is the power factor angle. For simplification, the capacitor current is expressed as:

$$i_{Cf(rms)}(t) = i_L(t)\cdot\sqrt{1-|M|} \tag{3-12}$$

From (3-12), it can be concluded that the current through the flying capacitor dominates the load current and modulation index. Also, the maximum rms current occurs when pure reactive power is transferred.

Fig. 3.8 shows the relationship between the normalized capacitor current vs. duty ratio at a load current frequency of 500Hz. As a result, the duty ratio increases, the capacitor current ripple decreases, even the load power factor angle varies. For the voltage ripple of the flying capacitor, assume that the capacitor has a stable energy balance for charging and discharging modes. The ripple voltages are derived as:

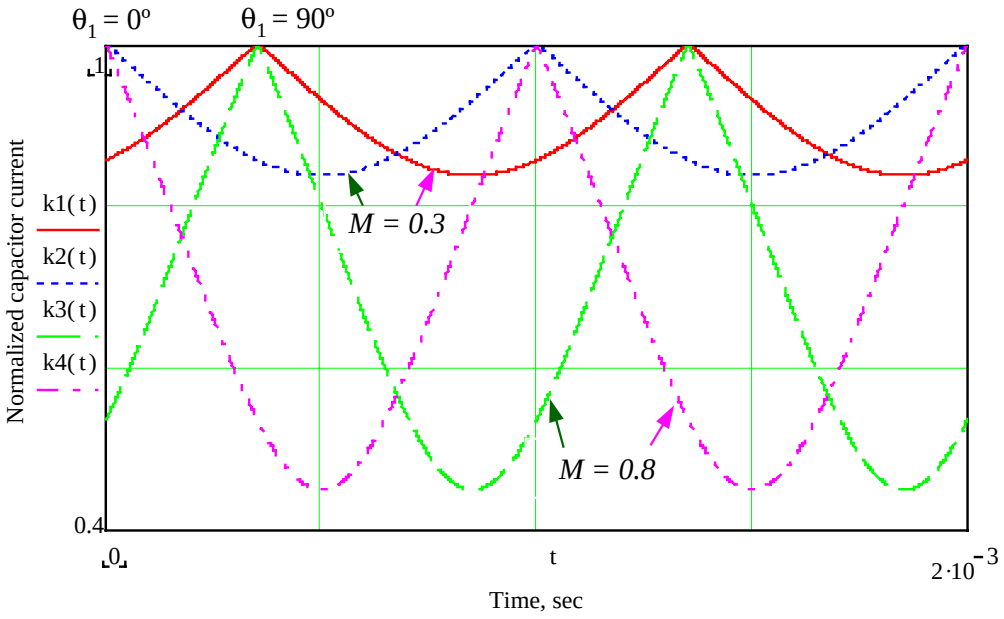


Fig. 3.8. Normalized capacitor current vs. duty ratio at a load frequency of 500 Hz.

$$\Delta V_{Cf} = \frac{i_{Cf\,(rms)}}{C_f \cdot f_s} \tag{3-13}$$

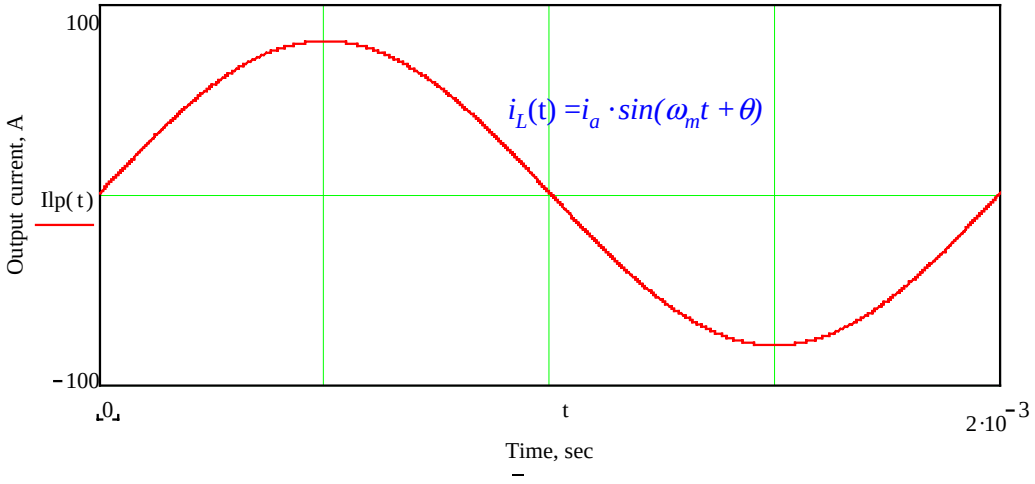
where f_s is the switching frequency. By replacing $i_{cf(rms)}$ with the function of the load current, the voltage ripple amplitude is expressed as:

$$\Delta V_{Cf} = \frac{i_L(t)}{C_f \cdot f_s} \cdot \frac{1-|M|}{2} \tag{3-14}$$

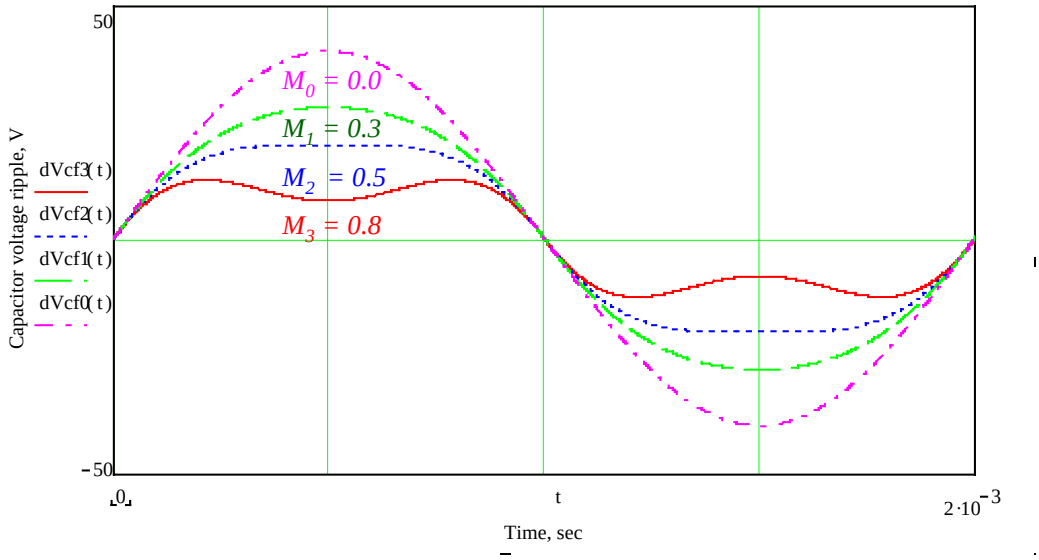
For the dc current applications, letting $i_L(t) = i_o$ in (3-14), the voltage is expressed as:

$$\Delta V_{Cf} = \frac{i_o}{C_f \cdot f_s} \cdot \sqrt{1-|M|} \tag{3-15}$$

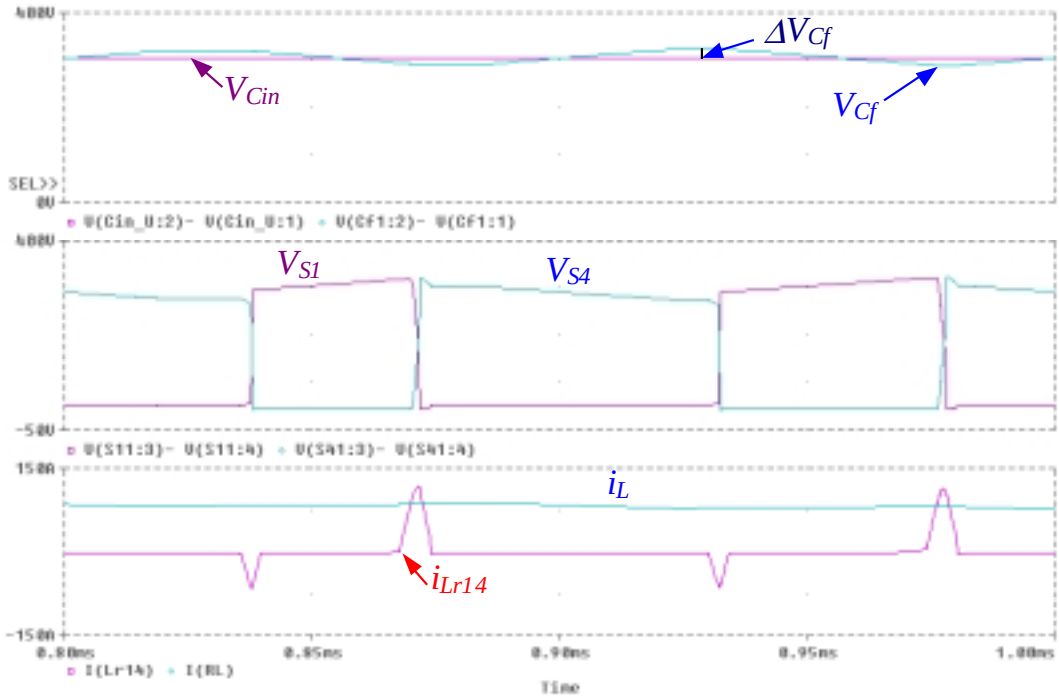
where, i_o is the current source. For validation, the flying capacitor current and voltage characteristics as shown in Fig. 3.9 are simulated by the numerical calculation at the same condition as shown in Fig. 3.8. Using (3-13), the voltage ripple of the flying capacitor was calculated under different conditions, C_f = 200 μF and C_f = 1000 μF, respectively. With an 80A load current and 12 kHz switching operation, the voltage ripple comparison of flying capacitors are summarized in Table 3-3. As a result, the voltage ripple decreases as the duty ratio increases. Fig.3.10 shows the relationship between the ripple voltage and modulation index under different flying capacitances. The voltage ripple can be reduced as the capacitance increases.



(a) Load current of 80 A



(b) Capacitor ripples voltage vs. duty ratio at a load current 80 A

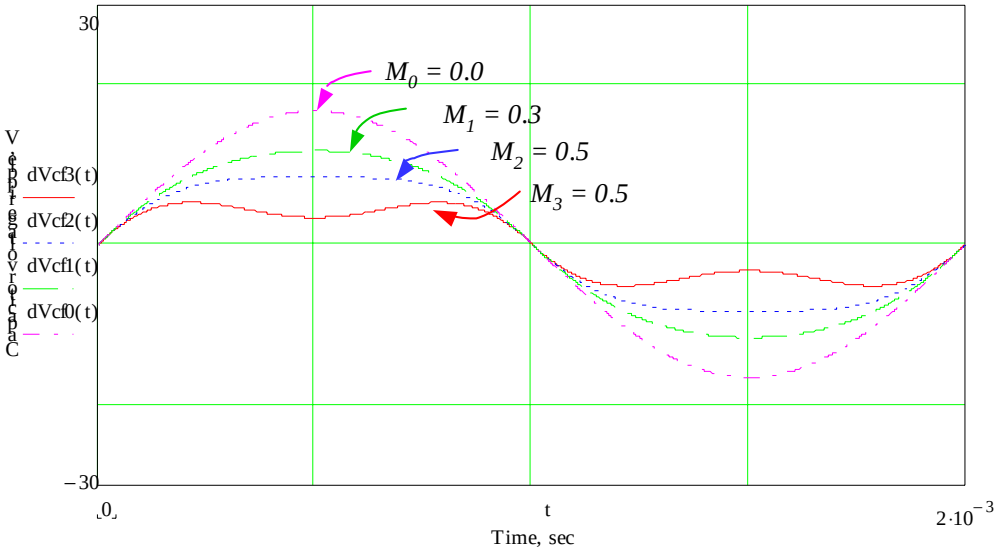


(c) Ripple voltage of the flying capacitor under PWM switching

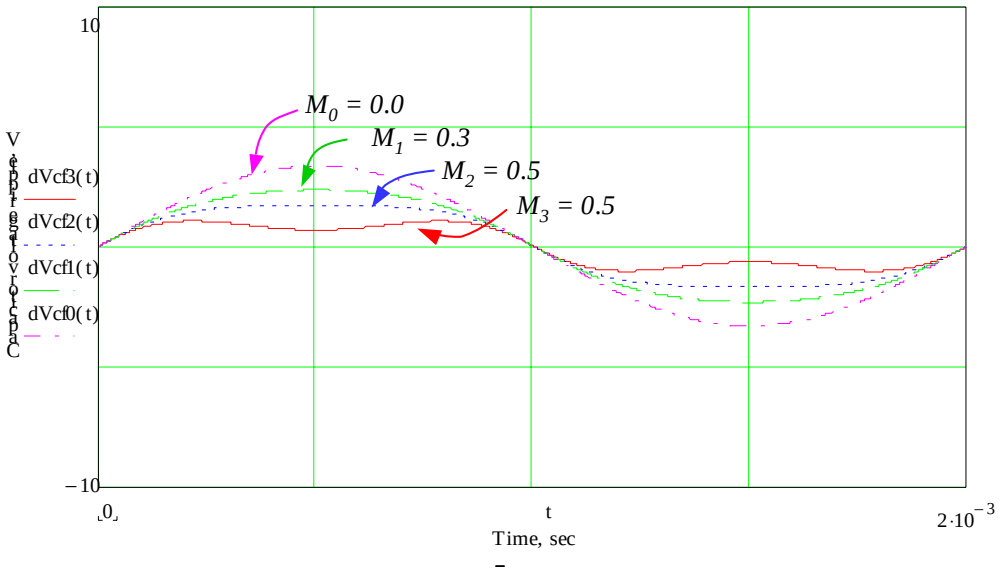
Fig. 3.9. Current and voltage waveforms of flying capacitor.

Table 3-3. Voltage ripple comparison under different flying capacitors.

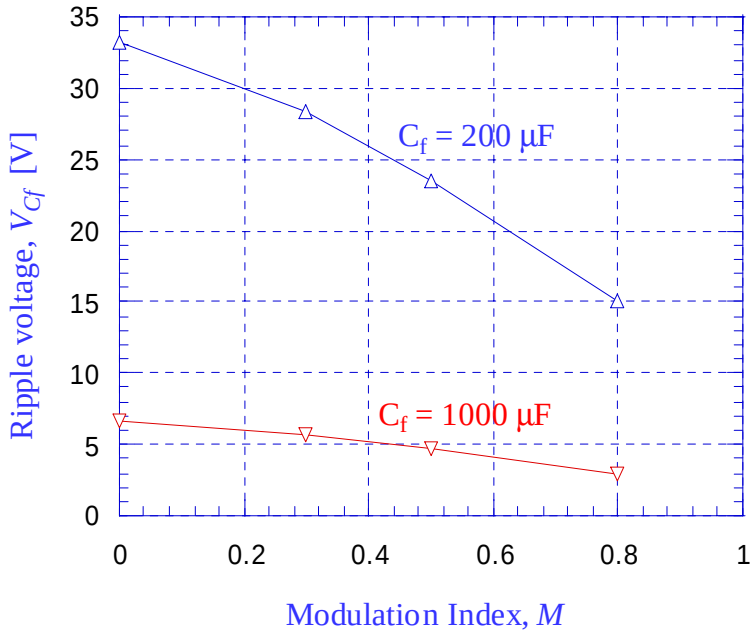
C_f	Modulation Index	ΔV_{Cf}	Conditions
200 μF	M = 0.0	33.3 V	I_S = 80 A f_S = 12 kHz
	M = 0.3	28.4 V	
	M = 0.5	23.5V	
	M = 0.8	15.0V	
1000 μF	M = 0.0	6.7 V	I_S = 80 A f_S = 12 kHz
	M = 0.3	5.7 V	
	M = 0.5	4.7V	
	M = 0.8	3.0 V	



(a) C_f = 200 μF



(b) C_f = 1000 μF



(c) Ripple voltage versus modulation index

Fig. 3.10. Relationship between the ripple voltage and modulation index.

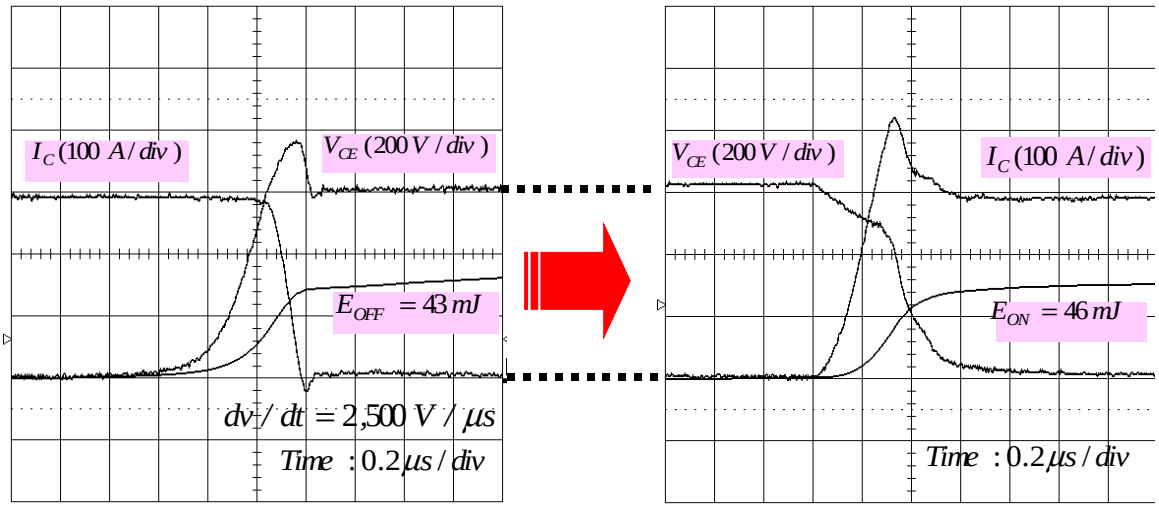
3.5 CHARACTERISTICS OF SNUBBING CAPACITORS

It is well known that the ZVT inverters need snubbing capacitors to place the resonant circuitry in parallel with the main switches. They reduce the turn-off loss and turn-off dv/dt of the device. In general, a larger size capacitor can reduce the turn-off loss and dv/dt. However, the extra energy stored in the resonant capacitor needs to be discharged during turn on. So, the capacitor size should be optimized so that both turn-on and turn-off losses are reduced. The rate of change of voltage across the resonant capacitor can be expressed as

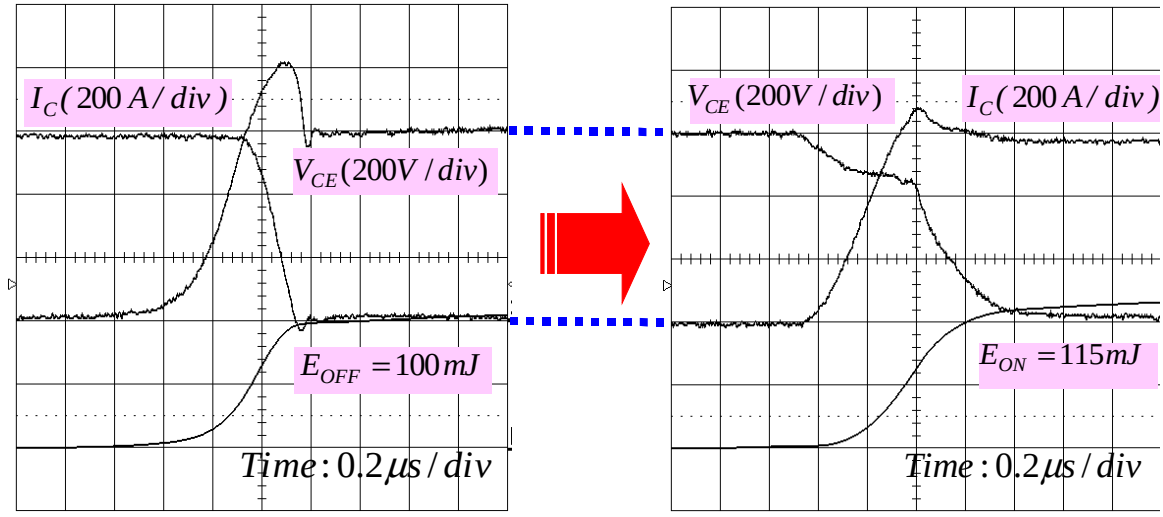
$$\frac{dV_{CE}}{dt} = \frac{I_{sw}}{C_r} \tag{3-16}$$

where, V_{CE} is the collect-emitter voltage, and I_{sw} is the device current, which equals to the load current, I_L, during switching.

In a conventional hard-switching scheme, the characteristics of an IGBT are usually studied based on the turn-on and turn-off losses shown in Fig. 3.11. The IGBT turn-on causes a reverse recovery in the freewheeling diode and a large current spike. For turn-off losses, the charges stored in the base of the IGBT cause a current tail at turn-off. This tail increases turn-off losses and also increases a deadtime between the conduction of two devices in the chopper leg. The following experimental waveforms indicate the total losses of the IGBT and diode during switching. Fig. 3.11(a) & (b) show the voltage, current and switching energy waveforms of IGBT during turn-on and turn-off under hard switching. During turn-off, dv/dt of 2,500 V/μs and switching energy of 43 *mJ* were obtained at a load current 300 A, and 100 *mJ* for 600 A. Under turn-on, di/dt of 1,100 A/μs and switching energy of 46.0 *mJ* at 300 A, and 115 *mJ* for 600 A were obtained.



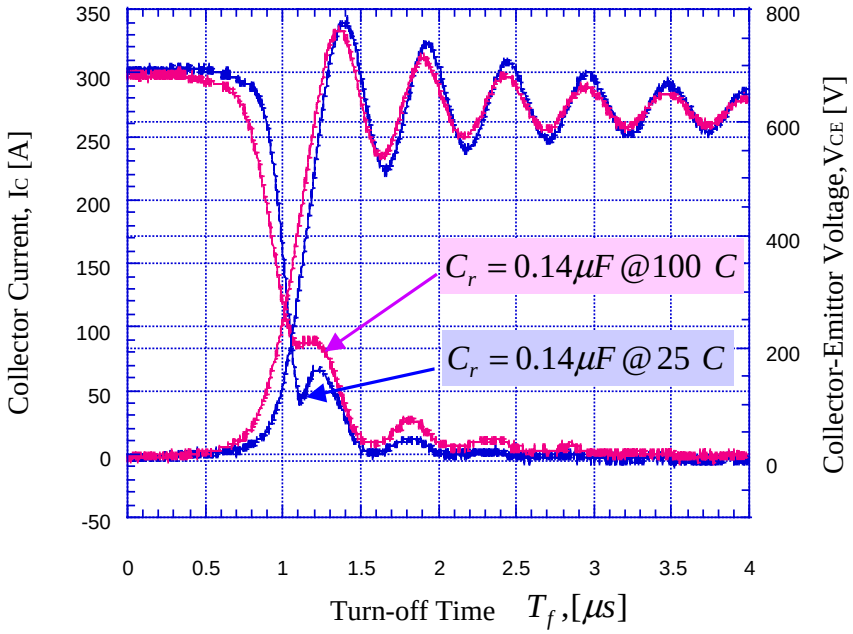
(a) Hard-switching: I_{SW} = 300 A



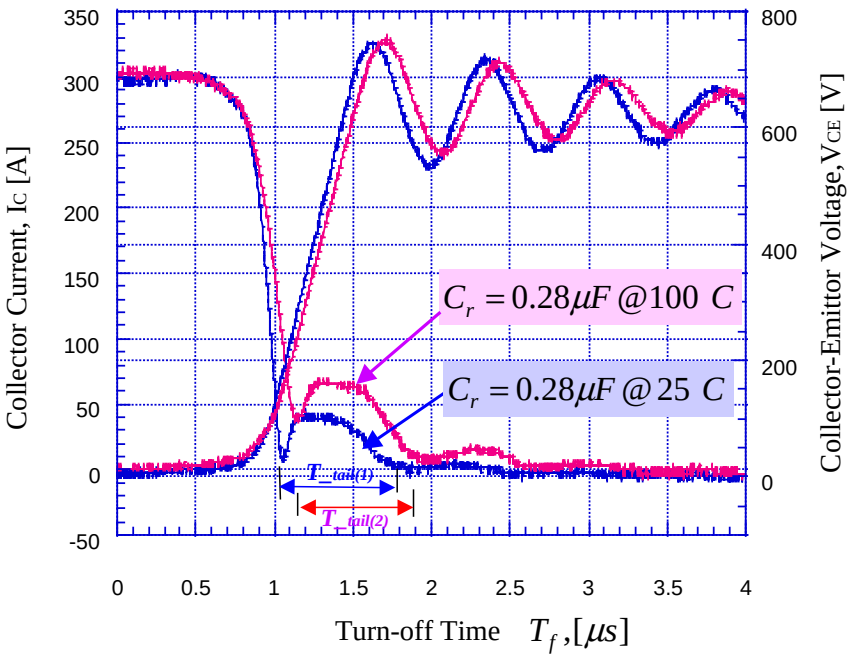
(b) Hard-switching: I_{SW} = 600 A

Fig. 3.11. Experimental waveforms of the current and voltage of the IGBTs under hard-switching.

Fig. 3.12 shows experimental turn-off current and voltage waveforms of the IGBT under different snubbing capacitors and temperatures, with C_r = 0.14 μF and C_r = 0.28 μF at 25 °C and 100 °C, respectively. With low dv/dt, switching losses eventually is decreased. The dv/dt rate of 580 V/ μs under C_r = 0.28 μF in Fig. 12(b) is much less than the 2.5 kV/μs that was obtained in the hard-switching condition. The turn-off loss under soft switching was reduced by four times as compared to the hard-switching condition.



(a) C_r = 0.14 μF



(b) C_r = 0.28 μF

Fig. 3.12. Soft-switching characteristics of IGBT under different snubbing capacitors.

Fig. 3.13 shows a typical dv/dt versus snubbing capacitors corresponding to load current variations. It is very clear that the rate of dv/dt depends on the snubbing capacitor value. To determine the resonant capacitor, the value of dv/dt is preferred to be less than 1,000 [V/μs]. Although a higher value of the capacitor reduces turn-off loss, it makes an inductor design more difficult because there should be an energy balance between the inductor and the capacitor during charging and discharging, which takes place during the switching transients.

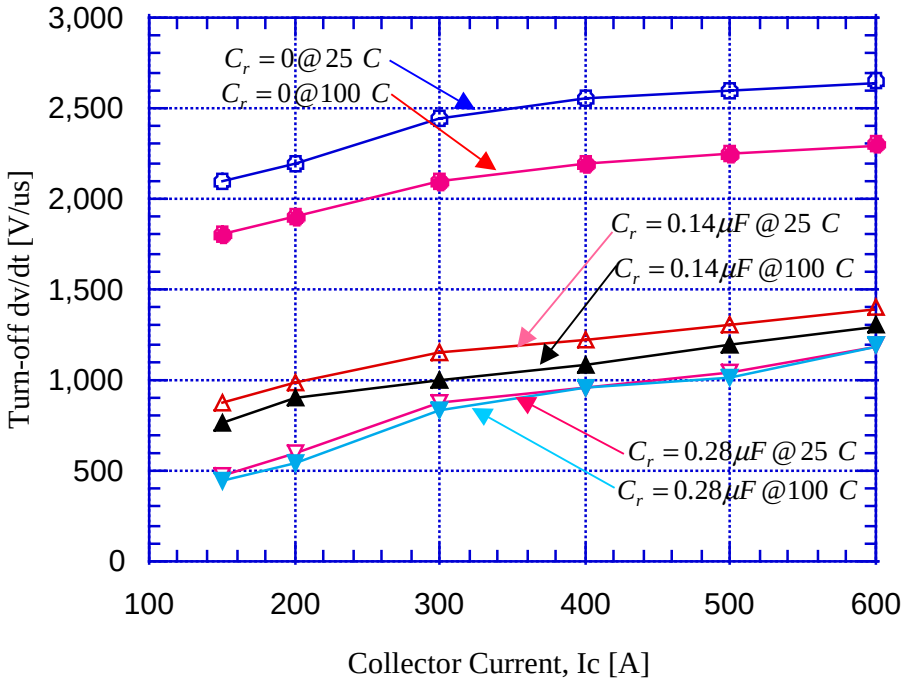
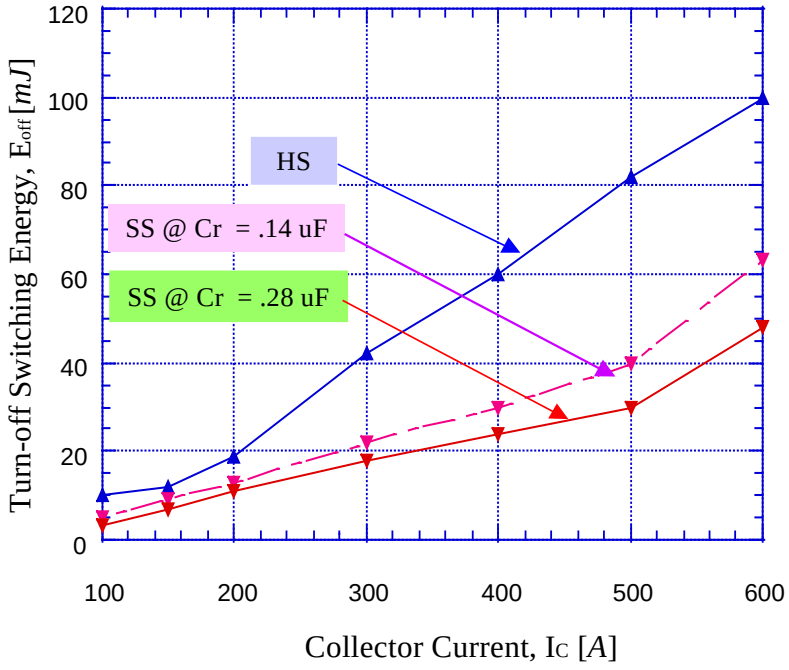


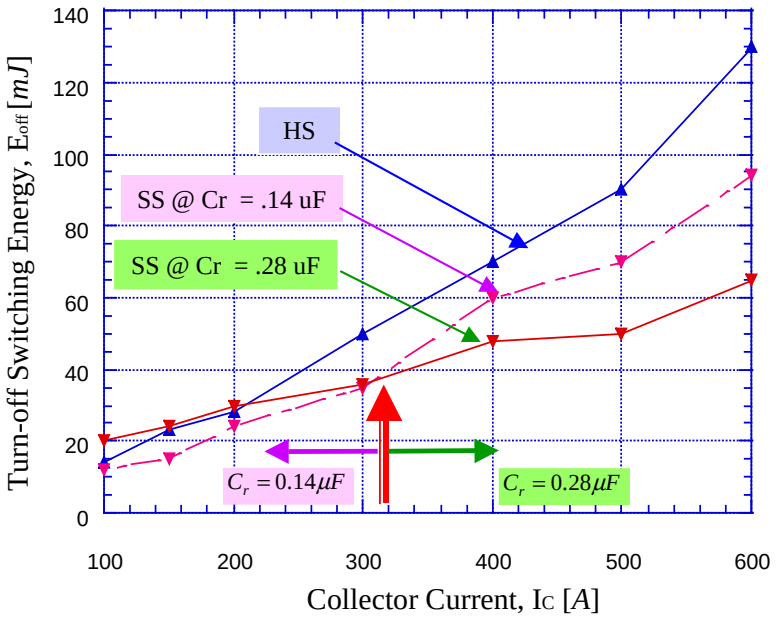
Fig. 3.13. Turn-off dv/dt comparisons corresponding to snubbing capacitors.

Fig. 3.14 shows turn-off switching energy comparison of the IGBT between hard and soft-switching schemes under different snubbing capacitors. From experimental results, it is obvious that the turn-off switching loss can be reduced by a larger snubbing capacitor at 25 °*C*, but not at high temperatures because of the large failed current. The average turn-off switching losses corresponding to the load current and temperatures under different snubbing capacitors can be chosen from these curves at the expected operating current.

Furthermore, such snubbing capacitors partly influence voltage unbalance between the flying capacitors caused by different dv/dt ZVT operations, in conjunction with conduction voltages of series connected IGBTs. To identify their voltage balance, simulation was performed through a P-spice program. As we expected, simulation results show a great sensitivity to device and circuit characteristics.



(a) T_j = 25 °C



(b) T_j = 100 °C

Fig. 3.14. Turn-off switching energy comparisons under hard- and soft-switching conditions.

3.6 CHARACTERISTICS OF DC LINK CAPACITORS

For unbalanced voltages between flying capacitors, it is very important to determine the size of a dc link capacitor capable of instant storage power. Although the size of their capacitances determines the voltage ripple of the active filter, it should be properly selected. Thus, effects on the dc link capacitor ripple of the active filter are investigated. Such a study provides a solution for optimal capacitance calculation of the capacitor.

Fig. 3.15 shows the configuration of a three-level active power filter with flying capacitors. For simplification, it is assumed that the switches have ideal operation without any voltage drop. The voltage equations can be derived from the main circuit.

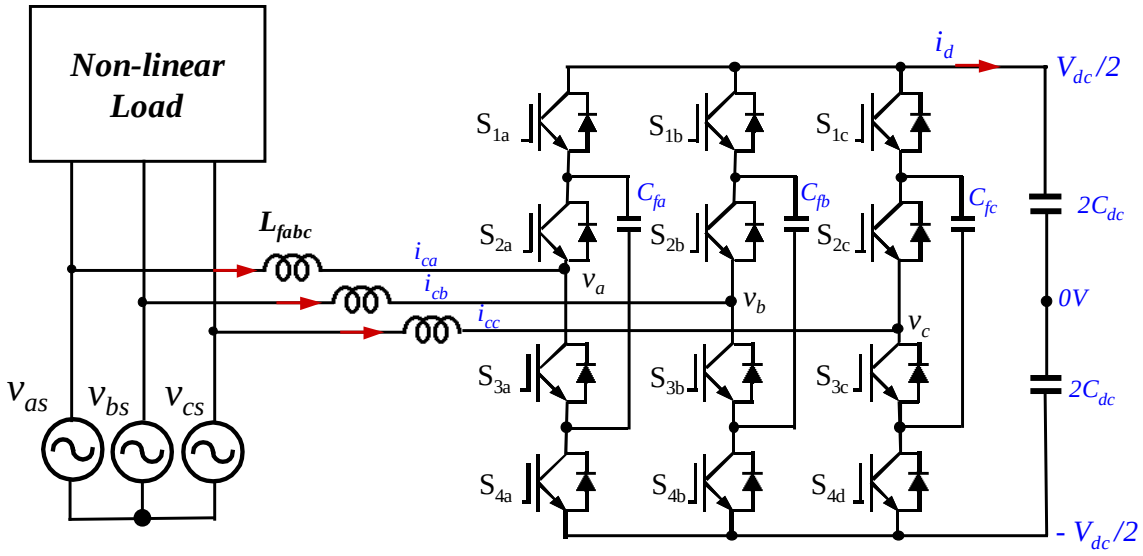


Fig. 3.15. Configuration of a three-level active power filter with flying capacitors.

In addition, it is assumed that three-phase voltage sources are balanced without voltage distortion. The source voltages for each phase be defined as follows

$$\begin{aligned} v_{as} &= V_m \sin(\omega t) \\ v_{bs} &= V_m \sin\left(\omega t - \frac{2\pi}{3}\right) \\ v_{cs} &= V_m \sin\left(\omega t + \frac{2\pi}{3}\right) \end{aligned} \tag{3-17}$$

where, V_m is the peak voltage for power sources.

$$\begin{aligned} v_{as} &= L_{fa}\frac{di_{Ca}}{dt} + v_a \\ v_{bs} &= L_{fb}\frac{di_{Cb}}{dt} + v_b \\ v_{cs} &= L_{fc}\frac{di_{Cc}}{dt} + v_c \end{aligned} \tag{3-18}$$

where L_{fa}, L_{fb}, and L_{fc} are the inductances of the interfacing inductors to the utility and let $L_{fa} = L_{fb} = L_{fc} = L_f$. And v_a, v_b, and v_c are the ac voltages in the front of the converter. These voltages can be determined by the switching function as:

$$\begin{aligned} v_a &= x_a \cdot \frac{V_{dc}}{2} \\ v_b &= x_b \cdot \frac{V_{dc}}{2} \\ v_c &= x_c \cdot \frac{V_{dc}}{2} \end{aligned} \tag{3-19}$$

where x_a, x_b, and x_c are switching functions between each leg. Using these equations, the dc link current can be calculated by summing three current paths.

$$i_d(t) = i_{Ca}\frac{x_a+1}{2} + i_{Cb}\frac{x_b+1}{2} + i_{Cc}\frac{x_c+1}{2} \tag{3-20}$$

Of course, it is assumed that there is no neutral line. This means that the total current to be compensated for current harmonics should be zero under balanced load conditions.

$$i_{Ca} + i_{Cb} + i_{Cc} = 0 \tag{3-21}$$

On the other hand, the switching functions can be expressed as

$$\begin{aligned} x_a &= \frac{2}{V_{dc}}\left(v_{as} - L_f\frac{di_{Ca}}{dt}\right) \\ x_b &= \frac{2}{V_{dc}}\left(v_{bs} - L_f\frac{di_{Cb}}{dt}\right) \\ x_c &= \frac{2}{V_{dc}}\left(v_{cs} - L_f\frac{di_{Cc}}{dt}\right) \end{aligned} \tag{3-22}$$

Therefore, the total dc current through the dc link capacitors can be expressed as.

$$i_d(t) = \frac{i_{Ca}}{2}\left(\frac{2}{V_{dc}}\left(v_{as} - L_f\frac{di_{Ca}}{dt}\right)+1\right) + \frac{i_{Cb}}{2}\left(\frac{2}{V_{dc}}\left(v_{bs} - L_f\frac{di_{Cb}}{dt}\right)+1\right) + \frac{i_{Cc}}{2}\left(\frac{2}{V_{dc}}\left(v_{cs} - L_f\frac{di_{Cc}}{dt}\right)+1\right) \tag{3-23}$$

Since the sum of the three currents is zero, the dc current can be arranged as:

$$\begin{aligned} i_d(t) &= \frac{1}{V_{dc}}\left[\left(i_{Ca}\cdot v_{as}\right)+\left(i_{Cb}\cdot v_{bs}\right)+\left(i_{Cc}\cdot v_{cs}\right)\right] - \frac{1}{V_{dc}}\left[\frac{L_f}{2}\cdot\frac{d}{dt}\left(i_{Ca}^2+i_{Cb}^2+i_{Cc}^2\right)\right] \\ &= \frac{1}{V_{dc}}\left[P - \frac{L_f}{2}\cdot\frac{d}{dt}\left(i_{Ca}^2+i_{Cb}^2+i_{Cc}^2\right)\right] \end{aligned} \tag{3-24}$$

where,

$$P = (i_{Ca} \cdot v_{as}) + (i_{Cb} \cdot v_{bs}) + (i_{Cc} \cdot v_{cs}) \tag{3-25}$$

From (3-23), we can find the voltage ripple of the dc link voltage associated with the dc capacitors as:

$$\Delta V_{dc} = \Delta i_d(t) \cdot C_{dc} \tag{3-26}$$

where, $\Delta i_d(t)$ is the current ripple through the dc capacitor. The current ripple interacts with the current of the flying capacitor.

3.7 INTERACTION BETWEEN FLYING CAPACITORS AND DC CAPACITOR

When a flying capacitor multilevel inverter is applied to an active power filter, it is necessary to identify the interaction between flying capacitors and dc bus capacitor during reactive power compensation. This is because the main topology consists of many reactive capacitor elements. Since the stored energy in the dc bus capacitor flows through each flying capacitor, it is necessary to investigate the charge current flow for the capacitors.

Unlike inverter applications, the flying capacitors in an active filter circuit not only acts as a flying circuit to provide a neutral voltage sharing between main switches, but also absorbs or supplies reactive power to assist harmonic filtering during reactive power compensation. To explain the interaction between these capacitors, assume that the compensating current is negative and the flying capacitors are clamped to $v_{Cf1} = v_{Cf2} = V_{dc}/2$, while the dc capacitor discharges for harmonic current injection. Table 3-4 depicts the power flows of the capacitors during reactive power compensation.

Table 3-4. Power flows between flying capacitors and dc capacitor during reactive compensation.

Valid switching states				Output voltage	Power flow (flying capacitors)		Power flow (DC link capacitor)	Harmonic current injection
S_{1a}	S_{2a}	S_{1b}	S_{2b}	v_{ab}	v_{Cf1}	v_{Cf2}	v_{dc}	I_C
1	0	0	0	$- v_{Cf1} + v_{dc}$	Charging	No	Discharging	Negative
1	1	0	0	v_{dc}	No	No	Discharging	Negative
1	1	0	1	$-v_{Cf2} + v_{dc}$	No	Charging	Discharging	Negative
0	0	1	1	0	No	No	No charging	Negative

Fig. 3.16 shows the operation circuits of the active power filter during reactive power compensation. Even the power flows depend on the switching modulation techniques, reactive power compensation involves positive and negative current directions. For simplification, three possible modes are related to reactive power compensation for negative current operations of I_C, two charge modes for C_{f1} and C_{f2}, respectively, and only one flying mode of the flying capacitors. Fig. 3.16 (a) and (b) show the charge current flows to the flying capacitors. To get a terminal voltage, $v_{ab} = V_{dc}/2$, the dc capacitor C_{dc} discharges and one of flying capacitors charges during charging mode. The voltage can be expressed as follows.

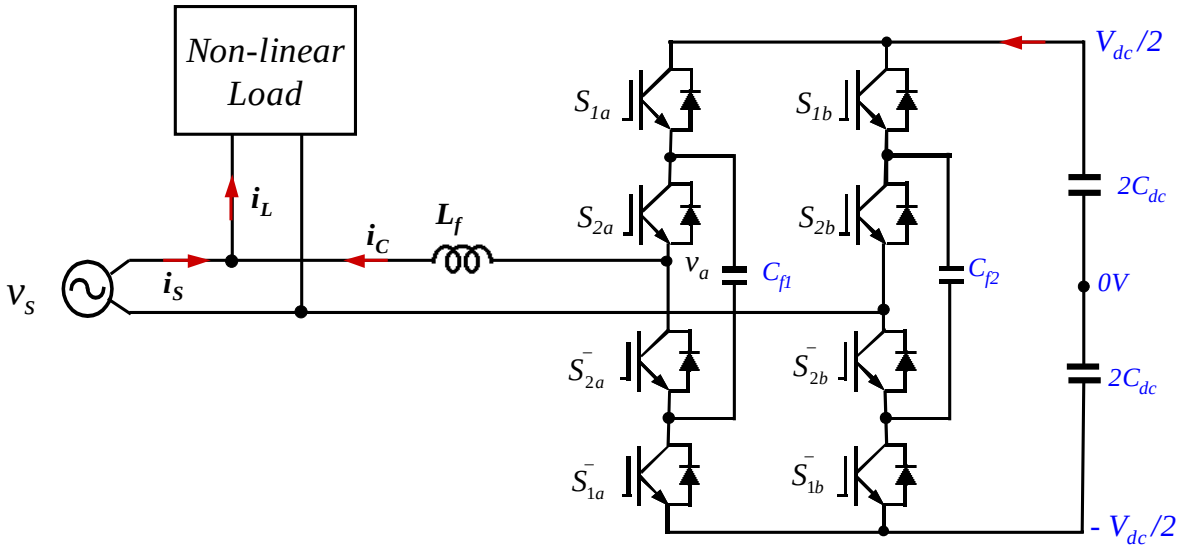
$$\begin{aligned} \frac{dv_{Cf1}}{dt} &= \frac{d_{2a} - d_{1a}}{C_{f1}} i_{dc} \\ \frac{dv_{Cf2}}{dt} &= \frac{d_{2b} - d_{1b}}{C_{f2}} i_{dc} \\ \frac{di_C}{dt} &= \frac{di_{dc}}{dt} = \frac{v_{ab} - v_S}{L_f} = \frac{V_{dc} - v_S}{2L_f} \end{aligned} \tag{3-27}$$

where, i_{dc} is the dc current through the dc capacitor and is the same as the compensating current of $i_{C.}$ Also d_{1a}, d_{2a}, d_{1b} and d_{2b} are instantaneous switching intervals per cycle. On the other hand, to get the terminal voltage $v_{ab} = V_{dc}$ as shown in Fig. 3.16(c), the four main switches, $S_{1a,}$ S_{2a}, S_{1b}, and S_{2b}, are turned on. During this interval, the dc current is linearly decreasing and discharging the dc bus capacitor C_{dc}, and compensating the harmonic current in the load. Fig. 3.16(d) shows the dc voltage mode during negative current. The dc voltage directly provides power for the reactive power compensation without any flying capacitor paths.

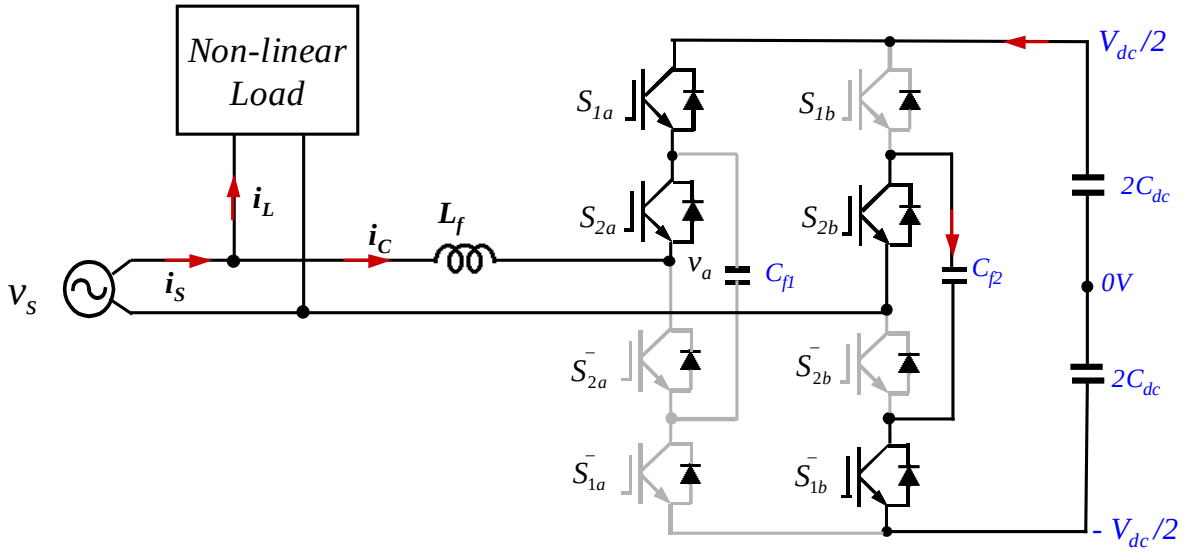
Providing that the capacitance of dc capacitor C_{dc} is high enough, it can be assumed that the conducting time, (d_{1a} – d_{1b}) is very short time intervals, compared to that of the line frequency. Thus, the capacitor voltage is practically constant. From these relationships between the charging mode and flying mode, the power input to the compensation is given by

$$P_{com\_in} = n \cdot v_S \cdot I_C \tag{3-28}$$

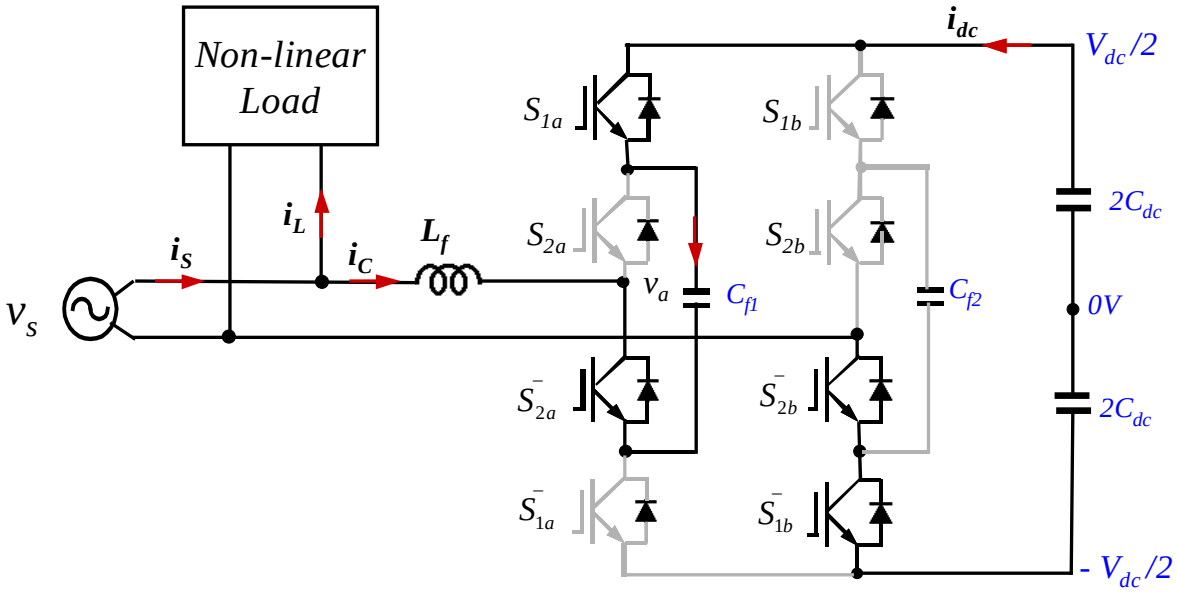
where, n is the number of phases.



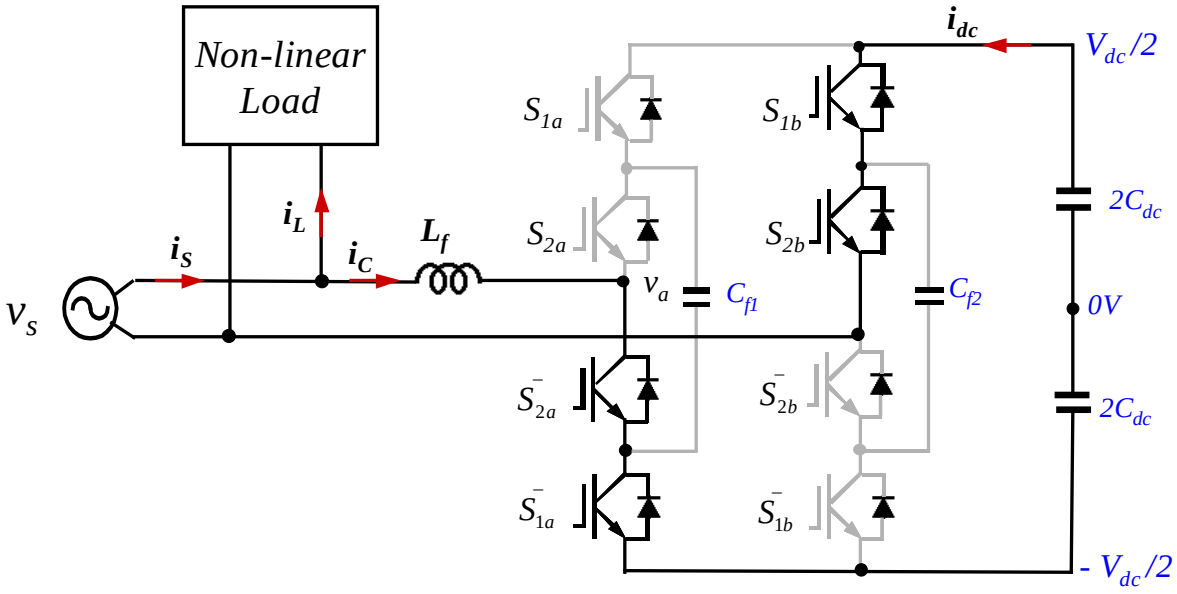
(a) Charging mode for C_{f1}



(b) Charging mode for C_{f2}



(c) Flying mode



(d) Dc voltage mode

Fig. 3.16 Power flow of the capacitors during reactive power compensation.

3.8 CONCLUSION

This chapter has studied fundamentals of voltage balancing for flying capacitors used in the proposed inverter. The various aspects associated with the voltage balancing were investigated to identify their safe operation in depth. In addition, the voltage balance issues between flying capacitors are discussed and identified through simulation and experimental results. In the behavior of the flying capacitor voltage, since the transfer function has an integral term, the *s* was only raised to the first power. The gain Bode plot had a straight line falling at –20dB/decade. It crossed the 0-dB axis at 1000 rad/sec. Also a first order integral shifted the phase -90° independent of frequency.

Furthermore, the interaction between the flying capacitors and dc link capacitor during reactive power compensation was analyzed. This provides the design guideline of an active power filter using flying capacitors. The following results were obtained from this study.

- Identification of the fundamentals of voltage unbalance between flying capacitors, dc link split capacitors,
- Analysis of the clamping mechanism with flying capacitors,
- Voltage synthesizing modulation for the charging balancing between the flying capacitors,
- Characteristics and dynamics of flying capacitors under various operations, and
- Interaction between the flying capacitors and dc capacitor during reactive power compensation.

To overcome the fundamental limitations associated with voltage unbalance between flying capacitors, it is necessary to control the unbalanced capacitor voltage by adding or subtracting in proportion to the unbalanced portion. The control scheme needs a closed-loop to compensate for the control signal to the main switch. The control algorithm will be discussed in Chapter 4.