CHAPTER VI

Development of Flip Chip on Flex Structure for Packaging Integrated Power Electronics Modules

Integrated power electronics modules (IPEMs) are envisioned as integrated power modules consisting of power semiconductor devices, power integrated circuits, sensors, and protection circuits for a wide range of power electronics applications, such as inverters for motor drives and converters for power processing equipment. Integration in power electronics is a rather complex process due to incompatibility of materials and processing methods used in fabrication, and due to the high energy levels these components must handle. Innovative 3-D integration technologies rather than planar integration approach are desired to be developed in order to meet the system requirements. Packaging involves the solution of electrical, mechanical and thermal problems. As a result, packaging of IPEM requires a multidisciplinary effort, encompassing the areas of materials, power semiconductor devices, fabrication processes, circuits and control, magnetics, thermal design and analysis, packaging, computer aided design integration, manufacturing as well as application considerations.

This chapter is focused on designing and fabricating a reliable and high performance packaged IPEMs eliminating the usage of wire bond in the process. We have developed a three-dimensional approach, termed flip chip on flex (FCOF), for packaging high-performance IPEMs. The new concept is based on the use of solder joint (D^2BGA chip scale package), not fine aluminum bonding wires, to interconnect power devices. This packaging approach has the potential to produce modules having superior electrical and thermal performance and improved reliability. We have demonstrated the feasibility of this approach by constructing half-bridge converters (consisting of two IGBTs, two power diodes, and a simple gate driver circuitry) which have been successfully tested at power levels over 30 kW.

6.1 Introduction

In this section, we introduce the converter topology we use in our work and briefly summary the advantages and advancement of three-dimensional multilayer power packaging.

6.1.1 Converter Topology

A review of high-power converter topologies shows two families of widely used phase leg structures [1]. One, as shown in Figure 6.1 (a), is the phase leg composed of two active switches and a diode anti-parallel with each of them. It can be used in AC/DC, DC/AC, and DC/DC converters, such as boost rectifier, voltage source inverter (VSI), and full/half-bridge converter. The other commonly used structure, shown in Figure 6.1 (b), is a phase leg that consists of two active switches with diodes in series with each of them. It can be configured as buck rectifier or current source inverter to perform AC/DC and DC/AC conversions. These two topologies can be called basic switching cells. These switching legs, together with driver circuits which can perform signal power amplification, level shift, isolation, protection and diagnostic functions, would make a switching cell that can perform as a generic computer-controlled power electronic building block. We chose a one-phase leg topology, shown as the shaded area in Figure 6.1 (a), as the power stage of an elementary IPEM module.

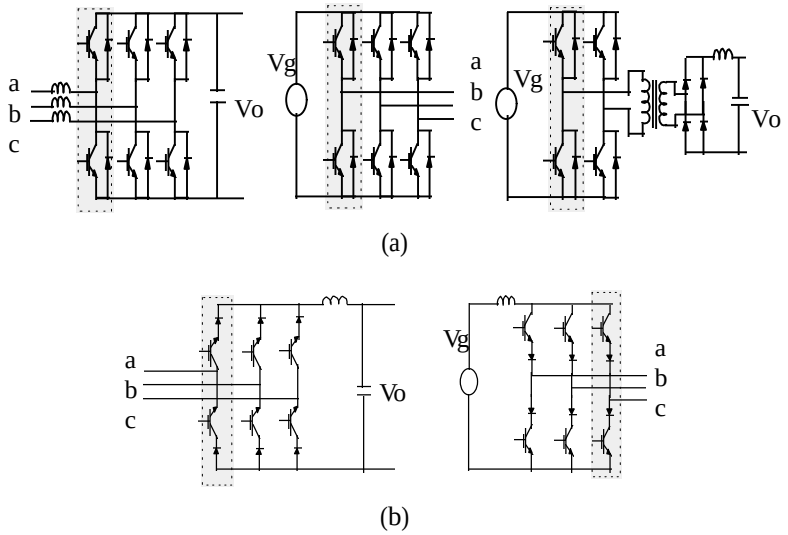


Figure 6.1. Converter topologies

6.1.2 Three-Dimensional Multilayer Power Packaging

From an electrical design point of view, traditional power modules are normally quite simple; however, these modules are often extremely difficult to fabricate due to high voltages and large currents, as well as thermal management and realibility considerations associated with the high power modules. The basic concept of multilayer package is to sandwich the semiconductor devices between a top and a bottom layers so that the interconnections between

the devices go to a different plane, thus eliminating wire-bonds. Investigations of the electrical parasitic effects and the thermal management associated with commercially available planar wire-bonded IGBT modules as well as three-dimensional module structures [1-4.] have shown that a multi-layer three-dimensional design has the following advantages over the conventional planar (wire-bond) design:

- The substrate does not need to allocate the conductor traces for bonding wires; the whole real estate can be utilized efficiently at high power level.
- Both the bottom and top layers have a large copper layer serving as a ground plane, the mutual coupling effect will reduce the conductor trace inductance, thus reducing mutual inductance between the devices as well. Most importantly, the negative and positive terminal leads are located in different planes allowing the implementation of the laminated terminal design, which cannot be implemented in a wire-bond design. The laminated structure of a three-dimensional design would significantly reduce the termination inductance, which is a major concern in a wire-bond module.
- The wire-bond parasitic effects as well as mechanical stress and fatigue are removed.
- The closed packaging of gate passive components and capacitors will effectively protect the devices.
- Thermal management can be improved by double sided cooling.

Just because of the benefits of a three-dimensional multilayer design, several new technologies for fabrication multilayer power modules are under development by the module manufacturers and research institutes [5-6] in the area of power electronics. New technologies that are under development to eliminate wire bonds typically employ spin-coating or tape-casting for laying down dielectric, dry or wet etching for opening up the contact pads and thin film deposition or plating for interconnecting devices. Other available techniques for device interconnections include gold stud-bumps and pressure contact assembly on the device pad [7-9]. General Electric researchers have developed the thin-film power overlay technology for packaging power devices; they use thin-film deposition followed by electroplating processes for device interconnections[6]. Recent power modules developed at Semikron contain spring-loaded metal strips that form electrical contacts on power devices by mechanical force [10]. Ferreira *et al.* proposed a packaging concept involving multiple layers of electromagnetic materials and switching function layers [11]. Linden *et al*. developed a power circuit substrate and packaging

technology combining multichip module-laminated (MCM-L) technology with Insulated Metal Substrate (IMS) technology [12]. All of these technologies have yet to prove their manufacturability, reliability, and cost effectiveness.

Consequently, we can conclude that, in a packaging protocol for power electronics modules, a three dimensional structure would be significantly more efficient than the conventional planar wire-bond approach. However, in a three-dimensional packaging structure, device interconnects would also need to be realized in a vertical interconnection technique. Solder joint interconnects could be specially suited for vertical interconnects, which has been widely used in IC packaging. In the following sections, we describe the three-dimensional flip chip on flex package structure, discuss the martial issues and fabrication process, and report the electrical and reliability results of the packaged modules.

6.2 Flip Chip on Flex Package Structure Design and Description

A flip chip on flex (FCOF) package was proposed [13] to construct integrated power electronics modules (IPEMs). The feasibility of this packaging approach is demonstrated by constructing half-bridge power modules (in two different phases) consisting of two switches (MOSFETs or IGBTs), two power diodes a few gate driver circuit components. The first phase of the module fabrication is intended for evaluation of this solder joint power chip interconnection approach while the second phase is focused towards fabrication of integrated power modules with significant integration of gate driver circuitry.

6.2.1 First phase module

The detailed specification of the first phase power module is as following:

Configuration:	Half-bridge inverter module including gate drives and bus snubber capacitor as shown in Figure 6.2.		
Power semiconductors:	Power MOSFETs (2)	80 V, 20 A	50 mm^2/die
	Free-wheeling diodes (2)	80 V, 10 A	25 mm^2/die
Bus Snubber Capacitor:	200 nF, 80 V		
Gate Drive Circuitry:	Surface-mount on separate PWB substrate, 20 x 20 mm/switch		

Power Terminals:	Lateral copper tabs with bus power terminals in parallel plate configuration
IPEM Baseplate:	Galvanically isolated, with maximum thermal conductivity
Baseplate dimensions	50 mm x 75 mm

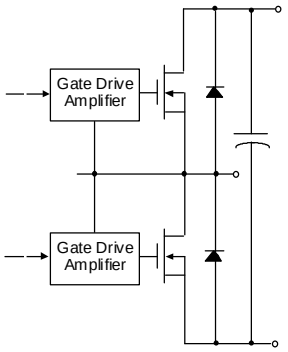


Figure 6.2. The configuration of the first phase power module.

The chip-scale packaged power devices we introduced in chapter V enable the realization of three-dimensional packaging of integrated power electronics modules. Most commercially available power devices (IGBTs, diodes) are vertical structures and, in order to realize high integration and maximize heat-transfer efficiency, a three-dimensional multilayer structure is selected where the power devices are sandwiched between two metallic layers. The proposed IPEM structure extends flip chip and flex circuitry technologies to power electronics packaging and takes advantages of these two technologies. Figure 6.3 (a) and (b) show the IPEM circuit and IPEM structure layers, respectively. The bottom layer of this structure, an insulated metal substrate (IMS), is used for attaching power chips. The substrates are etched and patterned into the desired pattern. The IMS substrate serves three purposes: providing a major thermal path for power devices; providing an electrical path and complete the electrical layout; and supporting the robust assembly of the module. The top layer of the structure is a doubled-sided flexible copper-clad laminate, which is an adhesiveless composite of polyimide film bonded to copper foil. Chip scale packaged MOSFETs and diodes are flip chip attached to the top flex substrate. That is, solder joints are used to connect the power chips to the flexible substrate. The devices can be encapsulated (optional) with thermally conductive underfill polymer materials to reduce the thermo-mechanical stresses imposed on the solder joints and help dissipate and distribute heat.

Gate drivers are built on separate PWB substrate using surface mount components. Surface mount snubber capacitor is chosen which is attached to the backside of the top flex substrate.

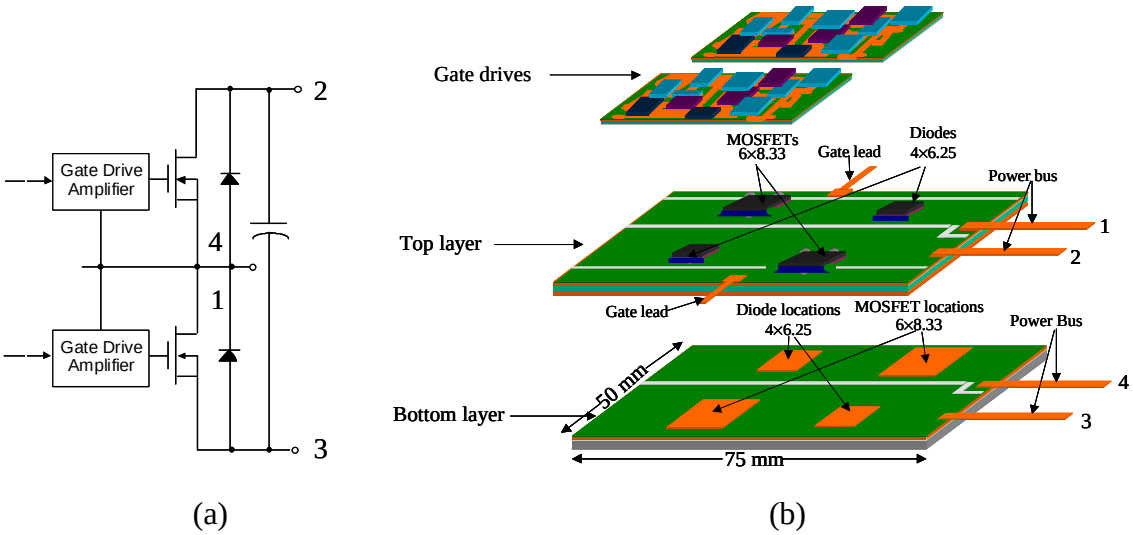
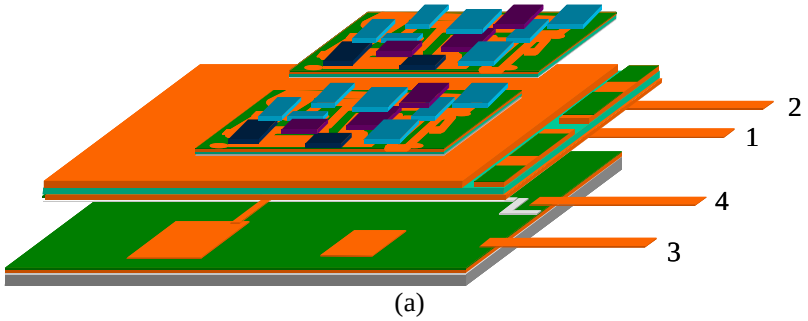
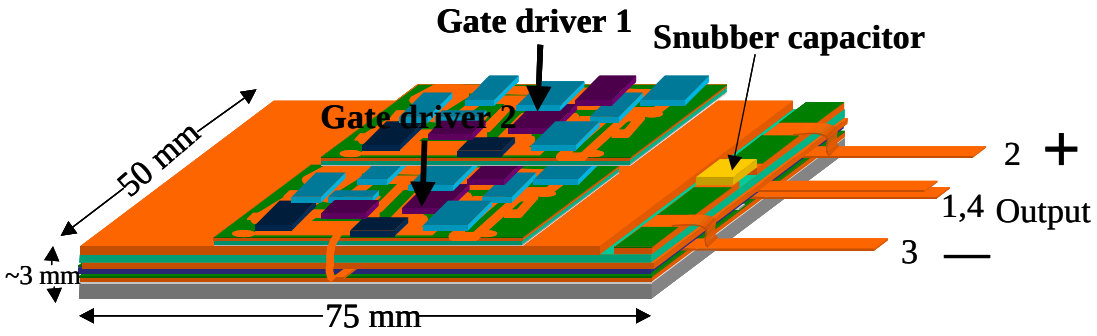


Figure 6.3. (a) IPEM circuit and (b) schematic IPEM structure layers.

In order to complete the electrical path and maximize heat-transfer efficiency, the top layer is flipped during the assembling process with the backside of the power devices (Drain for MOSFET and Cathode for diode) soldered to the bottom layer. Figure 6.4 (a) shows the schematic structure of the IPEM before assembly and Figure 6.4 (b) shows fully assembled IPEM. The two drivers are attached on top of the flex substrate using adhesive. Also the surface mount snubber capacitor is soldered to the top flex substrate and connected to the two power buses. Again, the gap between the top and the bottom layer can be encapsulated (optional) with thermally conductive encapsulant to reduce the thermo-mechanical stresses imposed on the die attach solder joint, prevent moisture, dust, and any corrosive chemicals from reaching the power devices as well as solder joints and help dissipate and distribute heat. Figure 6.5 is the cross-sectional view of the packaged IPEM detailing the power chip interconnection structure.



(a)



(b)

Figure 6.4. Schematic structure of the IPEM; (a) before assembly, but the top layer is flipped and ready for attachment; (b) after assembly of top and bottom layers and the two gates drivers and snubber capacitor.

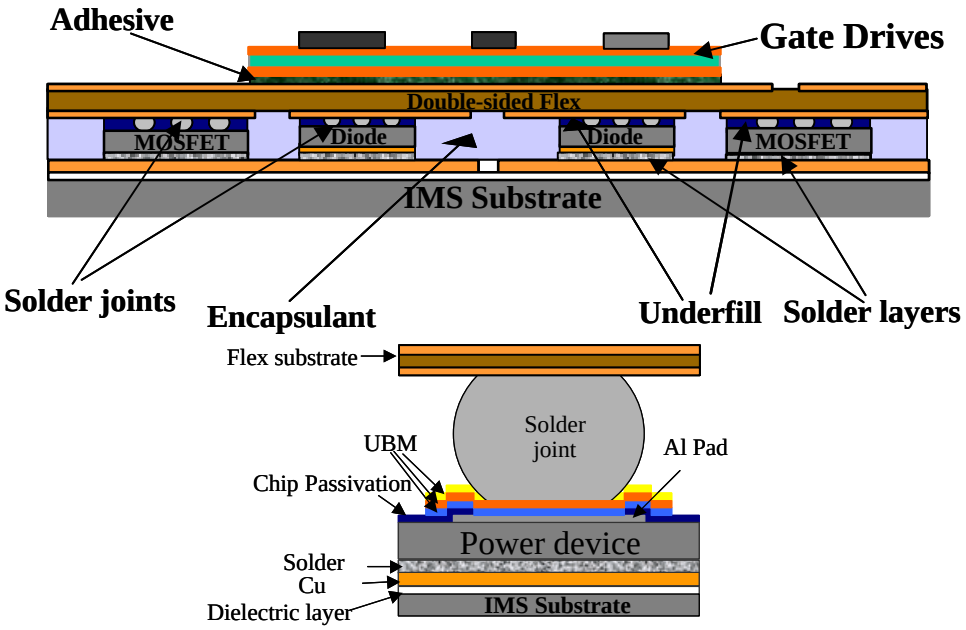


Figure 6.5. Cross-sectional view of the packaged IPEM.

6.2.2 Second phase module

For the second phase power module, we used IGBT devices (IGBT ratings: 1200 V, 70 A) and want integrate the gate drivers directly into the package instead of using separate boards. Figure 6.6 shows the circuit diagram of the second phase FCOF-IPEM. In this design, the power stage structure is same as the first phase one, only that gate drivers were built on the backside of the top flex substrate directly and the flex substrate can be folded and more components can be included.

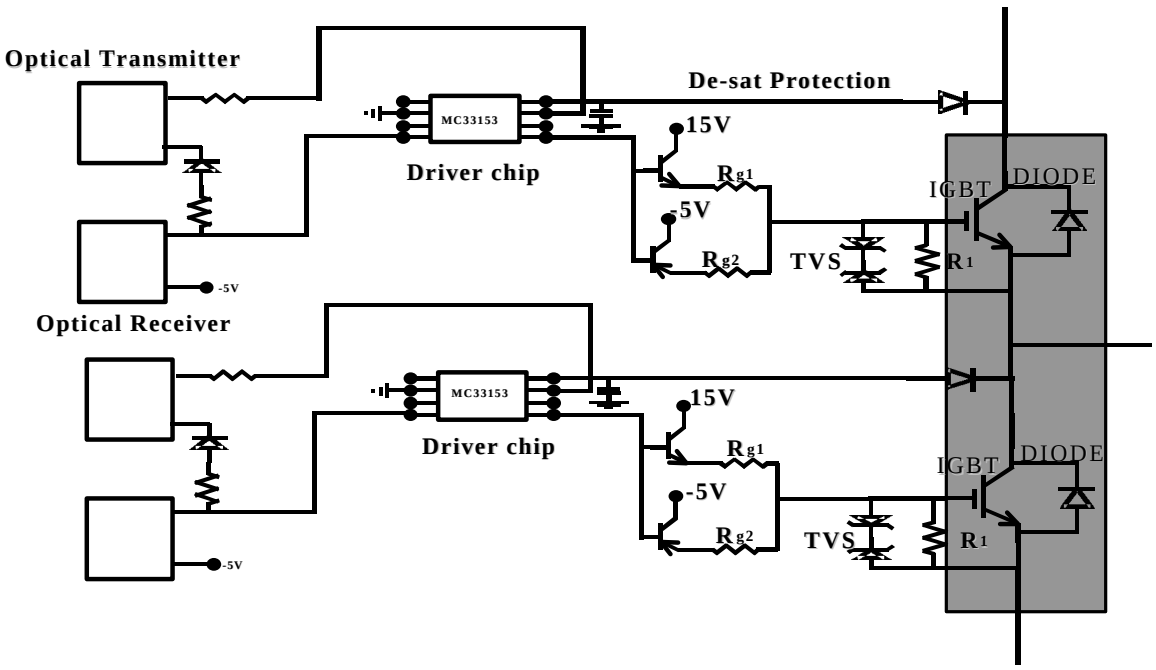
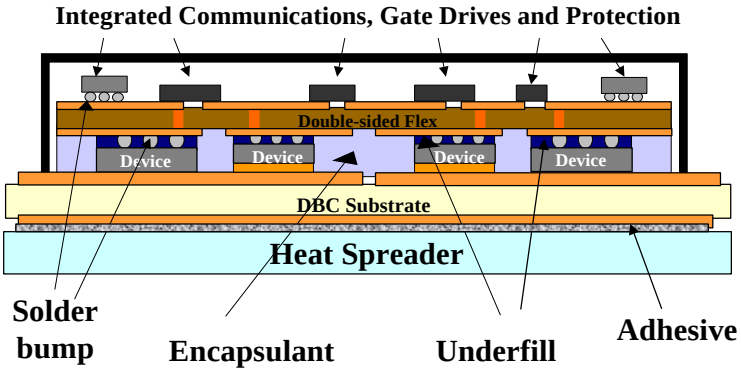
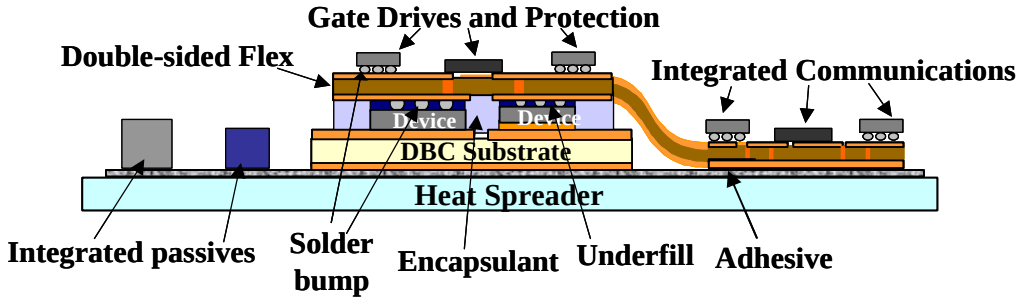


Figure 6.6. Circuit diagram of the second phase FCOF-IPEM with simple gate driver and control circuitry.

Figure 6.7 illustrates the proposed second phase IPEM structure. This time a direct-bond copper (DBC) substrate is used for attaching power chips instead of IMS since IGBT power devices have higher power and they generate more heat. The DBC substrate serves three purposes: providing a thermal path for flip-chip devices; providing an electrical path and complete the electrical layout; and supporting the robust assembly of the module. The top layer of the structure is a doubled-sided flexible copper-clad laminate, which is an adhesiveless composite of polyimide film bonded to copper foil. For improved reliability, triple-stacked high standoff hourglass-shaped solder joint is used to connect the power chips to the flexible substrate with a circuit pattern for gate-drive components. The devices are encapsulated with thermally conductive underfill polymer materials to reduce the thermo-mechanical stresses imposed on the solder joints and improve thermal management. Finally, gate drivers and control circuits are built on top of the flex circuitry using either flip chip or surface mount technology. If there is not enough space for putting all the necessary gate drivers and control circuit components on top of the flex, the flex can be bended and extended down to the heat spreader and thus more space is available, as shown in Figure 6.7 (b). Also we can put integrated passive components on the spreader.



(a)



(b)

Figure 6.7. Schematic FCOF structure of an integrated power electronics module built by CSP power devices.

6.3 Materials Design and Selection

Thermal management, reliability, current-handling capabilities and manufacturability are the major issues addressed in the materials selection process. It is very important to improve the thermal conductivity of power electronic packages, thus we can reduce power device operating temperatures for a given power level. In this way, devices may be placed closer together (thus improving power density), thermal cycling fatigue should be reduced (by reducing the magnitude of temperature change), and thermal stresses should be reduced (by decreasing thermal expansion strain). Superior thermal management requires the availability of materials with high thermal conductivity and thermal capacitance. Reliability is related to thermal management, CTE of materials, flexibility of the substrates and structure of the package. Current-handling capability is directly associated with the thickness of the metal layers and interconnection. The FCOF package is a structure incorporating materials with different properties. It contains silicon power chips, gate driver and control circuitry, solder joints, underfill material, thermally conductive encapsulation material, flexible substrate and bottom substrate (DBC or IMS).

The melting temperatures of the solders, the bumping process compatibility, manufacturability, and reliability are the major factors that influence the choice of solder compositions. Temperature hierarchy must be preserved at all times during the assembly processes to ensure structural integrity of the solder bump interconnect. Solder composition also has a significant influence on solder bump reliability. Eutectic Sn96.5/Ag3.5 solder has excellent characteristics and has shown great reliability improvement over eutectic lead-tin solder [14, 16]. As we discussed in Chapter II and III, the chip interconnection structure of FCOF package can be either single barrel-shaped solder joint or stacked solder joint. For single solder joint, either eutectic lead-tin solder or eutectic silver-tin solder is preferred. For a triple-stacked solder joint, which consists of inner cap (adjacent to die), middle solder ball and external cap. The inner cap is either Sn96.5/Ag3.5 alloy with a melting temperature of 221°C or Sn63/Pb37 with a melting temperature of 183°C. In the middle is Sn10/Pb90 solder, whose melting temperature is 268°C. The external cap is eutectic solder (Sn63/Pb37) with a melting temperature of 183°C.

The interposer of the structure is double-sided, copper-clad laminate, which is an adhesiveless composite of polyimide film bonded to copper foil. This copper-clad is commercially available. This laminate has excellent handling characteristics for fabrication, outstanding dimensional stability, excellent assembly performance over a wide range of processing temperatures, low thermal expansion coefficient, excellent thermal resistance for high-temperature assembly processes and is compatible with conventional oxide treatments and wet chemical plated-through-hole desmear processes. The thickness of both the polyimide film and copper foil is 2 mil. However, the copper sheet on the power device side is thickened to 5 mil by electroplating to increase current-carrying capacity. The pattern of Cu traces is formed by photolithography and chemical etching. After processing, the substrate retains very good bend and crease flexibility.

Underfills are used primarily to improve the reliability of the flip chip interconnection systems. These materials fill the gap between the chip and substrate around the solder joints reducing the thermal stresses imposed on the solder joints. The cure time and temperature of the underfill is a major factor in the selection of an underfill material for a flip chip interconnection system. Since the underfill process follows the flip-chip bonding step, cure temperatures lower than the melting point of the solder joint is necessary. The glass transition temperature of the

underfill material should be well above the service temperatures of the module. Other factors, which influence the performance of an underfill, are its CTE, elastic modulus and adhesion to the interconnection system materials. The CTE of the underfill material must match those of the solder joint as closely as possible [15]. High elastic modulus underfill materials are preferred. With an elastic modulus close to that of the solder, the underfill forms a quasi-continuum with the joints, thus reducing the stress rise associated with the sharp contact angle between the solder and the die and substrate [15]. Good adhesion of the underfill material to the substrate and the die generally improves the reliability of the interconnection system. Several underfill materials have been investigated. These materials and relevant properties are listed in Table 6.1 [16-18]. Underfill material D is the preferred material for the structure since this material has lower CTE, high elastic modulus and furthermore it is thermally conductive. It has a T_g of 120°C and it has superior adhesion to Cu foil and the commonly used IC passivation materials, including polyimide. This underfill material is a fast-curing compound, with a cure time of 15 minutes at 150°C.

Table 6.1. Properties of various packaging materials.

Materials	Elastic Modulus (Gpa)	CTE (ppm/°C)	Thermal Conductivity (W/m·K)
Silicon	112	4.1	136
Underfill A	3.6	50	X
Underfill B	3.1	35	X
Underfill C	5	29	X
Underfill D	11	23	3.14
Thermally conductive adhesive	11	23	3.14
Flex substrate	4.1	20	X
Solder	16	25	51
Copper	123	17	390
DBC AlN	>600	7	180

Thermally conductive encapsulation material is used mainly to improve thermal management. High thermal conductivity materials are desirable. CTE, elastic modulus, T_g, adhesion and cure conditions are also important factors in the selection of the thermally conductive encapsulant. The material fills the gap between the flex and bottom DBC substrate and encapsulates the power devices. In this way, the heat generated by the power chips is dissipated in three dimensions thus improving thermal management. Just like the underfill

materials, thermally conductive encapsulant can also protect the power chips since they are embedded in it. Furthermore, this filling material can support the flex substrate and the driver and control circuit, reduce the load on the power dies and solder bumps and distribute stresses. Finally, excellent adhesion of the filling material to the substrates and considerably high elastic modulus improves the reliability of the module and make it more robust. The thermally conductive encapsulant has a low-viscosity and low-stress adhesive. Its T_g is 100°C. It cures in 15 minutes at 150°C.

The selection of the bottom substrate is critical. First, it should have high current handling capability. Secondly, it must have excellent thermal conductivity. Thirdly, its coefficient of thermal expansion ideally should be closely matched to the power devices. Lastly, it should have good mechanical and physical properties. The first selection for a high-performance ceramic substrate material is Aluminum Nitride (AlN). AlN exhibits a unique combination of thermal conductivity, electrical resistivity, thermal expansion and strength characteristics that match the needs for packaging, and cannot be achieved by either alumina (Al_2O_3) or beryllia (BeO). Compared to alumina, AlN has 10-15 times greater thermal conductivity, 50-75% greater bending strength and most importantly, a coefficient of thermal expansion close to silicon. Beryllia, on the other hand, possess more than half the thermal conductivity of copper and thus is used for applications demanding both thermal dissipation and electric isolation. However, BeO is brittle and is considered hazardous material to work with due to the toxic nature of BeO dust. AlN provides more than three times the bending strength of BeO, it can be sintered at a lower temperature and it is nontoxic. As a result, in the FCOF IGBT module design, we have used commercially available Direct Bond Copper (DBC) on AlN substrates where 25 mil thick AlN is sandwiched between 10-12 mil thick Cu plates on both sides (See Appendix A for detailed introduction to DBC).

The other materials selection includes investigation of available metals, metallic alloys or metal matrix composites (MMCs) as heat sink, which will maximize heat removal, minimize thermal fatigue and improve reliability. We have paid special attention to composite materials with thermal conductivity and thermal coefficient of expansion matched to that of silicon. For example, copper or aluminum metal matrix composites, fabricated by reaction synthesis processes, have a great potential due to their high thermal conductivities (the processing techniques can produce clean, low thermal resistant matrix/dispersoid interfaces) and tailored

thermal expansion coefficients. However, MMC heatspreaders are significantly more expensive than copper baseplate, and consequently, for a low-cost package design, we have selected thick copper baseplate as the heatspreader for FCOF modules.

6.4 Fabrication Process and Issues

6.4.1 Flip Chip on Flex Module Fabrication Process Design and Description

The flip chip on flex module fabrication basically consists of chip scale package fabrication, gate driver fabrication and IPEM assembling. The detailed fabrication steps of the designed IPEM are shown in Figure 6.8. The CSP fabrication is a true wafer-level packaging, which can reduce cost and improve production capability. The UBM is deposited after screening the devices and those bad devices can be eliminated from the following processes. The UBM (typically Ti/Cu/Au or Cr/Cr-Cu/Au) is deposited by sputtering technique. Considering that power devices do not require high solder joint density and pitch and high diameter solder joints are preferred in order to handle high current, the lowest cost solder bumping approach-stencil printing is selected. After dicing the solder bumped devices, we have essentially obtained chip scale power package (D^2BGA package). At this stage, high power/burn-in test can be conducted on those CSPs either using standard test sockets which are available in IC packaging or soldering them to a tester using lower temperature solder. Next, the CSPs are flip-soldered to the patterned top flex substrate. Flux and other contaminations are cleaned and then a thermally conductive underfill material may be introduced (optional) into the gap between the packages and substrate to enhance mechanical adhesion and reliability by distributing stresses caused by the mismatched coefficients of thermal expansion between the chip and substrate. After flip chip bonding, the top layer is flipped and the backsides of the power chips are soldered on to the prepared bottom IMS substrate. Thermal conductive encapsulant is filled in the gap between the top and bottom layers to make the package robust, help distribute and dissipate heat and improve the package reliability. Gate drivers are built separately using surface mount technology. Finally the gate drivers are attached on the top layer using adhesive and the snubber capacitor is soldered on top of the flex substrate and connected to the power buses. After the module is completed, it is tested for functionality and performances.

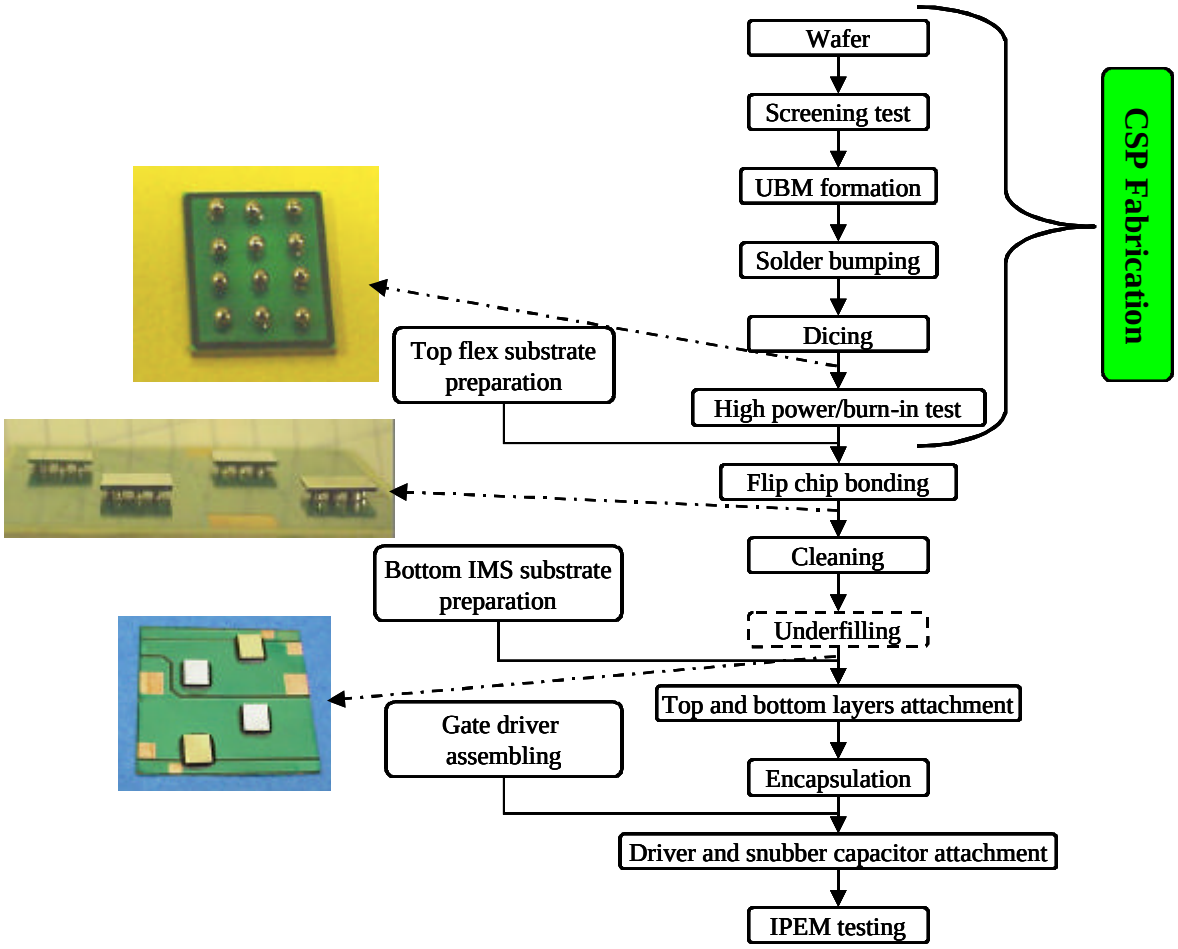


Figure 6.8. FCOF-IPEM fabrication process flowchart and similar pictures for corresponding steps for IGBT case.

Solder bumping process for both conventional barrel-shaped solder joint and high standoff hourglass-shaped solder joint has been described in Chapter II. Please refer to Chapter II for details.

Top flex substrate preparation: The top flexible substrate is a double-sided, copper-clad. One side is the power stage layout and the other side is a simple snubber capacitor attachment layout (in the case of driver and controller integration, the other side of the flex is the layout of driver and control circuit). The copper sheet on the power device side is thickened to 5 mil by electroplating. Figure 6.9 shows the top flex substrate process steps. The patterns of Cu traces are formed by photolithography and chemical etching. Solder mask is used to define solder joint locations. Power buses and gate leads are soldered to the pads using high temperature solder (Pb95Sn5).

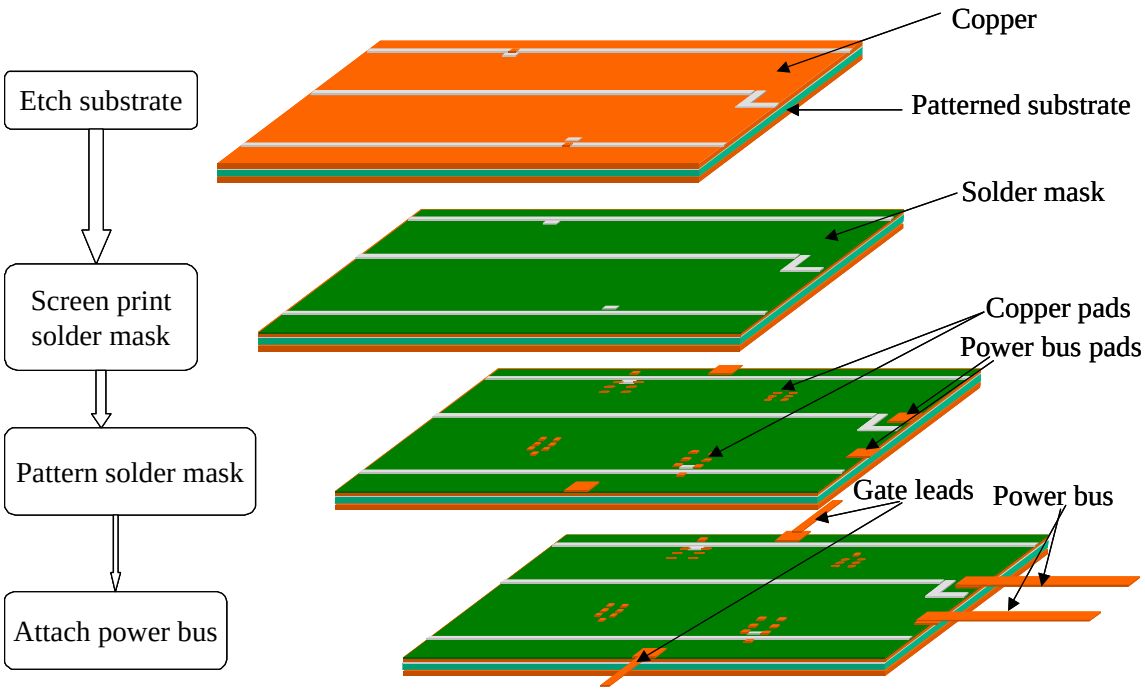


Figure 6.9. Top flex substrate preparation.

Underfiling: After the chip-scale packaged devices are flip-soldered to the top patterned flexible substrate and cleaning. A thermally conductive underfill material is introduced into the gap between the packages and substrate to enhance mechanical adhesion and reliability by distributing stresses caused by the mismatched coefficients of thermal expansion between the chip and substrate. During underfill, the assembly is placed on a hot plate with 90 °C. Underfill is placed around two chip sides in an "L" pattern. After some time, the gap is completely filled and then the underfill is cured.

Bottom IMS/DBC substrate preparation: IMS substrate is selected due to the fact that it is lost cost and has excellent current handling capability and acceptable thermal conductivity. Figure 6.10 illustrates bottom IMS substrate preparation process. The bottom DBC substrate has 12 mils thick nickel-plated copper. To get fine resolution and avoid undercut, electrochemical-etching technology is used (see Appendix B for details). After etching, a photoimagable solder mask was applied with conventional screen-printing. Photolithography allowed definition of openings in the solder mask around all the chip site pads and surface mount footprints on the substrates. This also offers the alignment mark for the top and bottom layers attachment. Power buses are soldered to the pads using high temperature solder (Pb95Sn5).

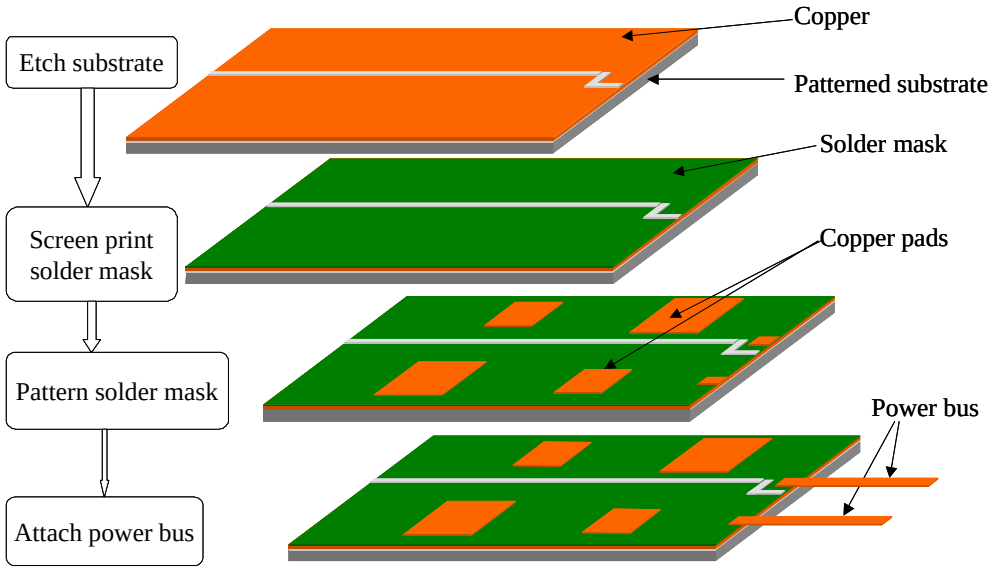


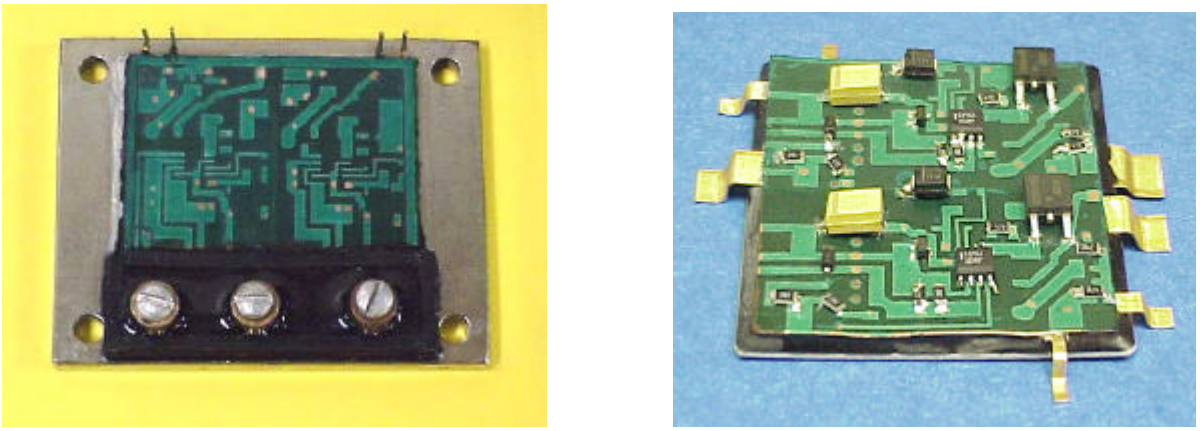
Figure 6.10. Bottom IMS substrate preparation.

Top and bottom layer attachment: During the top and bottom layer attachment, solder paste is first applied on the pads of bottom IMS. The top layer is flipped with the backside of power devices face down and then it is placed above the bottom assembly with the backside of power chips sitting in the solder mask openings of the patterned bottom IMS substrate. After this, the assembly is put in reflow oven for reflow. As a result, the top and bottom layers are attached together.

For the second phase module, driver and control circuit components are placed on top of flex. Then the bottom DBC substrate is placed under the whole top plate assembly with the backside of power chips sitting in the solder mask openings of the patterned DBC substrate. After this, the assembly is put in reflow oven for reflow. Thus both the top driver and control circuit components and the bottom substrate are reflowed at the same time. As a result, driver and control circuits are built on top of flex layer and the backsides of power chips are soldered to the patterned DBC substrate. Finally, the gap between the bottom and top substrate is encapsulated using the thermally conductive adhesive and then fully cured.

The three-dimensional packaging approach enables the fabrication of low profiled and high-density power modules. Figure 6.11 shows the packaged IGBT modules. The dimension of a typical FCOF half-bridge power stage module is 2"×2"×0.5" and 2"×2"×0.15" for Figure 6.11 (a) and (b), respectively. Compared with the state-of-the-art half-bridge power modules (typical dimensions of 3.7"×1.34"×1.2"), the volume of the half-bridge FCOF power module is reduced

by 65% and 90%, respectively. These modules were tested up to 800 V and 90 A for their functionality using switching test. Figure 6.12 shows the witching waveforms of FCOF IGBT power modules.



(a) (b)

Figure 6.11. Prototypes of FCOF IGBT power modules: (a) half-bridge power stage module; (b) half-bridge power module with simple integrated gate driver.

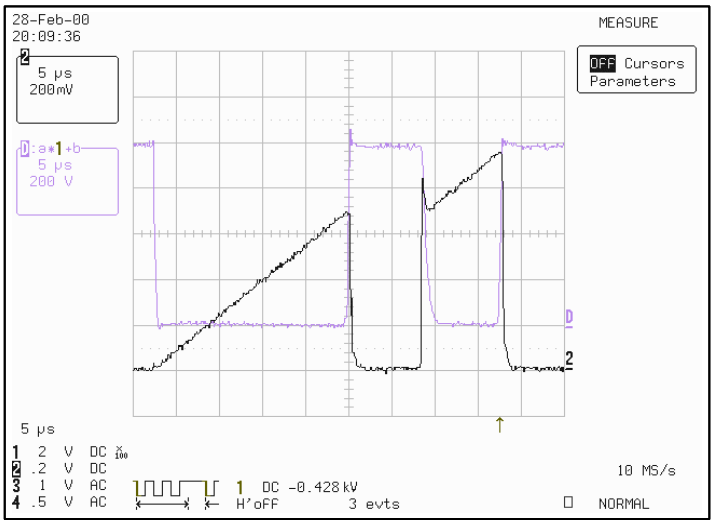


Figure 6.12. Switching waveforms of FCOF IGBT power modules.

6.4.2 Fabrication Issues

We can see from the above section that the flip chip on flex approach of packaging IPEM involves several steps. For each step, we analyze the related potential issues, such as fabrication risks, potential problems, equipment availability and possible solutions. Table 6.2 lists the major processing steps and the issues.

Table 6.2. Steps and issues of FCOF processing

Step Description	Issues
UBM formation	Availability of solderable power die from commercial manufacturers
	Established UBM technology for IC industry, such as IBM-C4
	Requires optimized deposition of UBM (wetability, adhesion, low stress, low resistance) if done in-house
Solder bumping	Well established in IC industry; wafer-level solder bumping is available; Equipment available; standard solder balls available; established standard
	Local CTE mismatch between solder joint and silicon chip
	Selection of a solder that is applicable in automotive application and with reduced fatigue characteristic at high and low temperature extremes
	Requires optimization of solder deposition and reflow parameters to make sure solder joint uniformity and void free if done in-house
High power/burn-in test	Known-good-die solution for power MCM packaging
	Standard testing socket available in IC packaging
	Requires building in-house tester if solder area array is not standard
Top flex substrate preparation	Accurately alignment of front and back side pattern if double-sided layout is needed and if the alignment requirement is high
Flip chip bonding	Flip chip bonder is commercially available; self-alignment effect of solder bonding
	Alignment accuracy for in-house manual pick-up and place machine
	Global CTE mismatch between substrate and silicon chip
	Optimized solder joint geometry and selection of substrate for improved solder joint reliability
	Requires optimization of reflow parameters to achieve reduced voids or void-free bonding
Underfilling (optional)	Selection of an underfill materials that has high service temperature, high insulation, good adhesion to power device passivation layer and substrate, and also preferably thermally conductive
	Bubble-free underfilling
Bottom IMS substrate preparation	Challenges of etching thin conductor widths and spacing on thick copper
	Electrochemical etch can be used to prevent undercutting
Top and bottom layer attachment	Alignment accuracy for manual alignment
	Die attach solder selection to obey temperature hierarchy
	Optimized reflow process to minimize die attach void content
	CTE mismatch between IMS and silicon
Encapsulation	Selection of an encapsulant that has low curing temperature, high service temperature, high insulation, good adhesion to top and bottom substrates, and also preferably thermally conductive
	Bubble-free encapsulation
Gate driver assembling	Surface mount
Driver and snubber capacitor attachment	Selection of epoxy with low curing temperature and high service temperature

6.5 Electrical Performance

In this section, the electrical performance of the FCOF power modules are reported and compared with that of wire bond power devices and modules. Commercial packaged IGBT device from vendor in the form of TO-247 package, wire bond module and FCOF power modules consisting of two CSP IGBTs, two CSP diodes were evaluated using both static tests and dynamic tests. For all of the above mentioned devices and modules, the same IGBT die and diode (if used) are used which we bought from the same vendor.

6.5.1 Static performance

SONY Tektronix 371 programmable high power curve tracer is used to conduct the static tests. The test condition is: pulse width is 250 μs, duty cycle lower than 0.5%. Five samples of each kind of device and module (Commercial packaged IGBT, D^2BGA IGBT, FCOF module and wire bonded module) were tested. The IGBT die we used is high speed IGBT. Its I_C versus V_{CE} curve is almost linear in the active region, thus we can define the amount of change in V_{CE} by the amount of change in the collector current I_C as on-state resistance R_{on}. Figure 6.13 shows voltage drop for different packages at I_c=90 A and I_c=35 A and Table 6.3 are typical static characteristics for different packages. We can see that D^2BGA IGBT has the lowest voltage drop and on-state resistance, highest forward transconductance. Compared with the commercial packaged IGBT, the $V_{CE(sat)}$ and R_{on} of D^2BGA IGBT are improved by about 20% and 30% respectively. When they are built in FCOF module, because of the resistance of connections, circuit tracks and external power bus, the voltage drop and on resistance is increased. The wire-bond module we built has more wire-bonds and much wider leads than the commercial IGBT device, thus it has lower $V_{CE(sat)}$ and R_{on} than the commercial packaged IGBT.

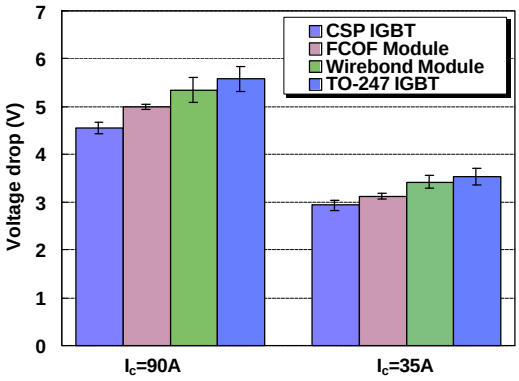


Figure 6.13. Voltage drop for different packages at I_c=90 A and I_c=35 A.

Table 6.3. Typical static characteristics of various power devices and modules.

	BV_{CES} (V) (I_C≈2 mA) (V_{GE}=0 V)	V_{GE} (V) (I_C≈2mA) (V_{CE} = V_{GE})	$V_{CE\ (sat)}$ (V) (I_C≈35 A) (V_{GE}=15 V)	$V_{CE\ (sat)}$ (V) (I_C≈90 A) (V_{GE}=15 V)	Ron (mΩ) (I_C≈90 A) (V_{GE}=15 V)	g_{fs} (S) (I_C≈90 A) (V_{CE}≈10 V)	$I_{C(on)}$ (A) (V_{GE}=15) (V_{CE}≈10 V)
TO-247 IGBT (Data sheet)	>1200	6	3.1	X	X	X	170
TO-247 IGBT (Test data)	>1300	6	3.51	5.66	38.5	30	158
Wire bond module	>1300	6	3.37	5.34	35.1	31	163
CSP IGBT	>1300	6	2.92	4.52	26.3	34	211
FCOF module	>1300	6	3.15	5.06	31.6	33	185

6.5.2 Switching performance

The switching characteristics for IGBTs are: switching times; switching energy; stray inductance (Ls). Ls is the package inductance between the bonding pad on the die and the external electrical connection. This inductance slows down the turn-on of the IGBT by an amount that is proportional to the di/dt of the collector current. For power module, stray inductance is self-inductance and mutual inductance of die bonding, circuit tracks and leads. Stray inductance causes turn-off overvoltage spikes and the turn-on voltage drops. During switching, the collector current changes rapidly and this high di/dt induces voltage transients across the stray inductances inside the packages. That is, V_L=L*di/dt. High voltage overshoot could result in a peak voltage exceeds the rating of the devices. Switching losses can be divided into turn on losses and turn off losses. In case turn on losses occur, the reverse recovery behavior of free wheeling diode is essential. The transient intervals of switching on and off are characterized by dynamic tests. Two different test setups were used. For the first several modules, a pulse-switch tester was used. Figure 6.14 shows the test circuit. The packaged FCOF power modules were tested for their functionality and performance. The highest test voltage and current available were 640 V and 50 A. The packaged FCOF modules passed 640 V and 50 A tests at both room temperature and 85°C. In order to evaluate the performance of FCOF package, packaged IGBT device in TO-247 form and commercially available wire-bond power module (half-bridge module, consists two IGBTs, two diodes. Note: the IGBT in this

commercial wire bond module could be different from those in the FCOF module and TO-247 IGBT device, but the IGBT in the latter two are same) and were also tested using the exactly same setup. For comparison, we used external packaged diode as the free-wheeling diode for all the three packages.

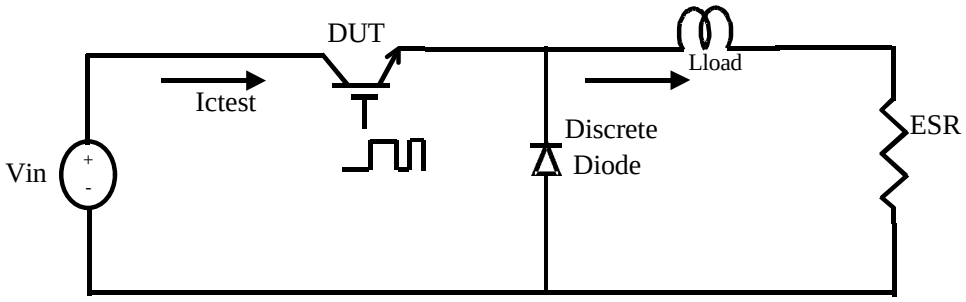


Figure 6.14. Pulse-switch test circuit.

Test results showed that the overshoot voltages vary for different packages. The FCOF package has the lowest overshoot, TO-247 IGBT device is next and wire-bond module has the highest overshoot voltage. Figure 6.15 shows the peak voltages and their overshoot percentages of the bus voltage (640 V) for the three packages. P1 is commercial wire-bond power module, P2 is TO-247 IGBT device and P3 is FCOF module. The FCOF has about 17% voltage overshoot, while TO-247 and the commercial module has about 28% and 32% overvoltage, respectively. Figure 6.16 shows the switching waveforms of the three configurations.

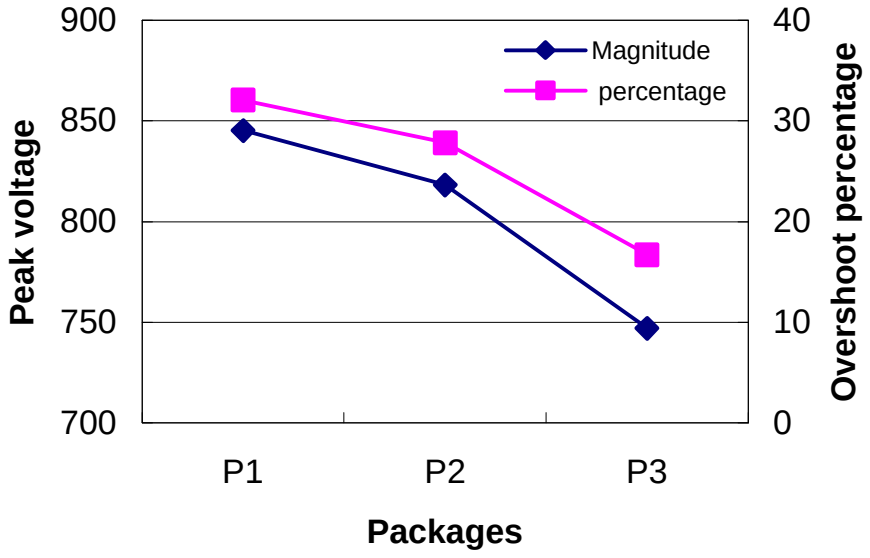


Figure 6.15. Peak voltages and overshoot percentages for the three packages.

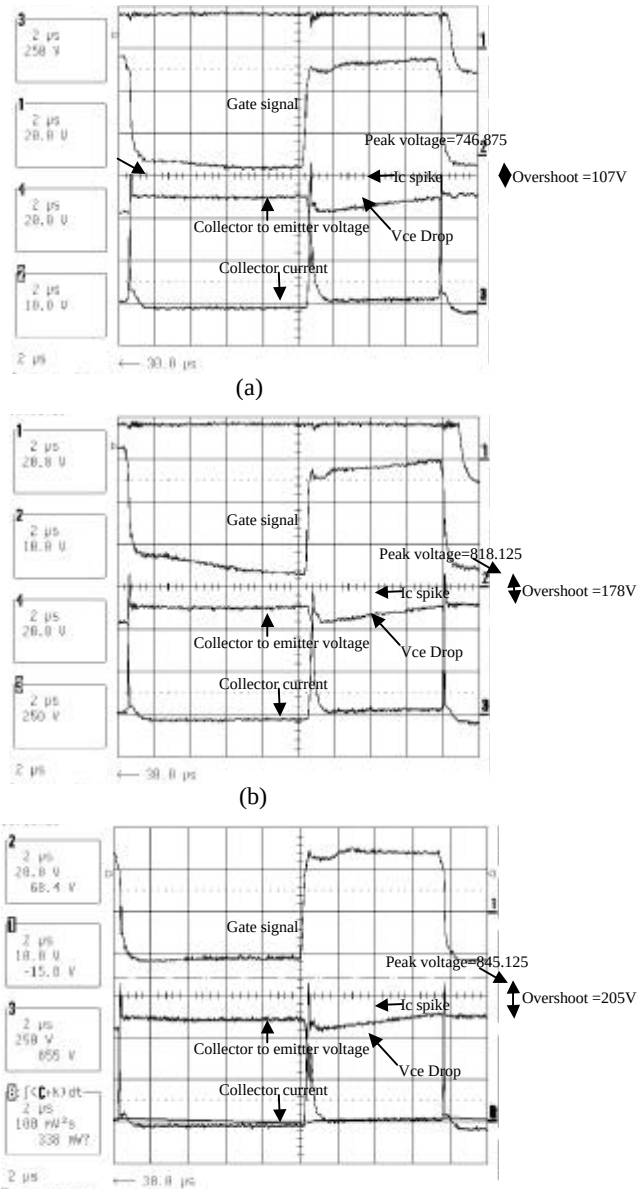


Figure 6.16. Switching waveforms of (a) FCOF module; (b) TO-247 IGBT device; (c) commercial wire-bond module.

For the recently fabricated modules, a new test setup was used. Figure 6.17 illustrates the test circuit. Gate resistor of R_g=24Ω was used. Commercial packaged IGBT in form of TO-247, FCOF module and in-house made wire bonded module are tested for comparison of their performances. The voltage is measured between the two terminals of the under test IGBT and the switch current is sensed at the emitter terminal as shown in Figure 6.17. Table 6.4 gives the test results and Figure 6.18 shows the switching waveforms of FCOF module and commercial packaged IGBT. The FCOF module has the lowest overshoot, commercial wire-bond packaged

IGBT device is next and wire-bond module has the highest overshoot voltage. The FCOF module has about 8.6% voltage overshoot, while a commercial IGBT device and an in-house processed wire-bond IGBT module have about 13.2% and 14% voltage overshoot, respectively. FCOF package greatly reduces device stresses. Also, because FCOF module has lower resistance and inductance than the other two packages, its turn-on time is shorter accompanied by lower turn-on loss.

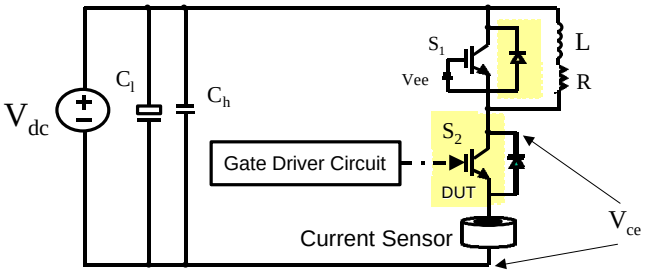
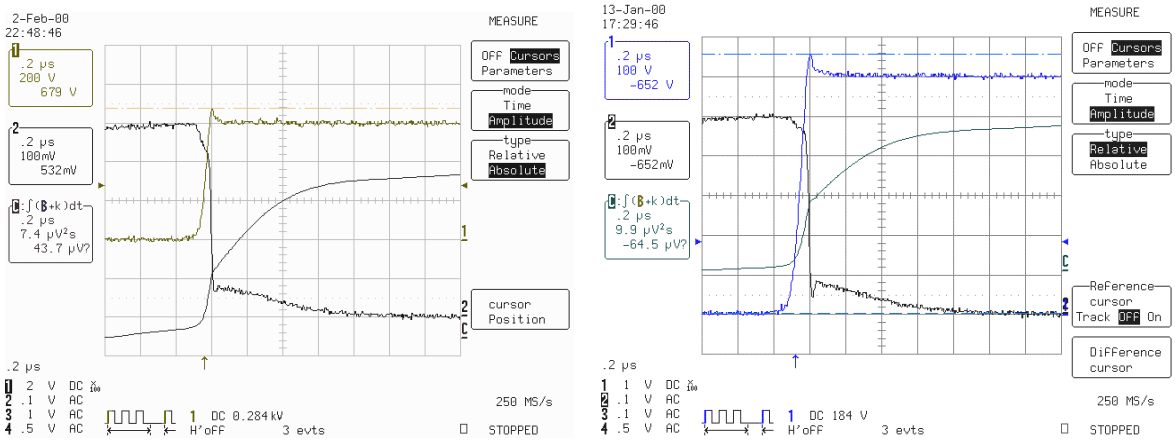


Figure 6.17. The dynamic test circuit.

Table 6.4. Dynamic test results of various power devices and modules at V=600V, I=50A

	t_{rise} (μs)	E_{on} (mJ)	T_{fall} (μs)	E_{off} (mJ)	$V_{CE(overshoot)}$ (V)
TO-247 IGBT (Test data)	0.43	6.72	0.9	2.87	79
Wire bond module	0.42	6.55	1	3.39	84
FCOF module	0.34	5.97	1	3.45	52



(a) (b)

Figure 6.18. Turn-off switching witching waveform of (a) Commercial packaged IGBT and (b) FCOF module.

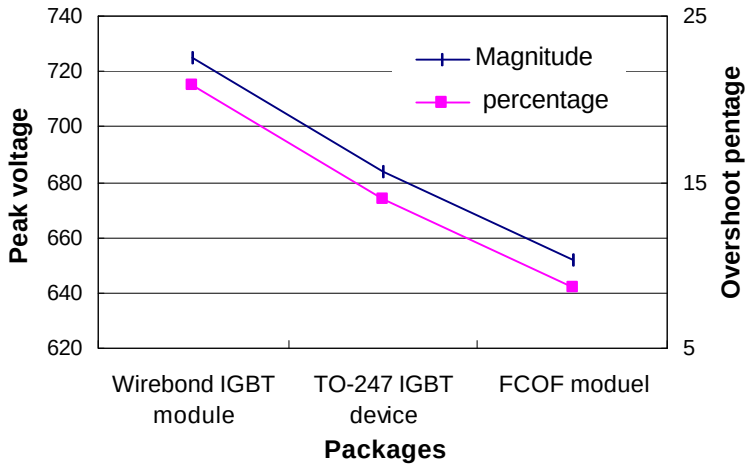


Figure 6.19. Peak voltages and overshoot percentages for different packages.

The turn-off overvoltage spikes and the turn-on voltage drops come from parasitics inside the packages. During switching, the collector current changes rapidly and this high di/dt induces voltage transients across the stray inductances inside the packages. That is, $V_L=L*di/dt$. For packaged device, the stray inductance is the package inductance between the bonding pad on the die and the external electrical connection. This inductance slows down the turn-on of the IGBT by an amount that is proportional to the di/dt of the collector current. For power module, stray inductance is self-inductance and mutual inductance of die bonding (L_{Si} for IGBT and L_{Di} for diode), circuit tracks (L_{Ti}) and leads (L_{Li}). Figure 6.20 illustrates the parasitic elements of a typical half bridge power module.

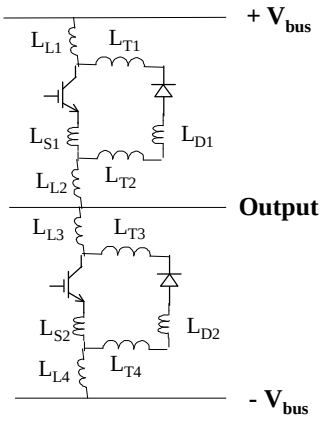


Figure 6.20. Parasitic elements of a half bridge power module.

High voltage overshoot could result in a peak voltage exceeds the rating of the devices. High voltage rating devices not only add additional cost, but also result in high conduction losses

and thus low overall efficiency. From Table 6.4 and Figure 6.18, we can see that FCOF module has lower parasitics than wire-bond module. Study shows that the performance of power modules is affected significantly by the inductance of the leads [3]. The FCOF modules we tested have longer leads than commercial module though we could make them shorter. The TO-247 IGBT device has the shortest leads. However, the total stray inductance of TO-247 IGBT device is still higher that of the FCOF module. This indicates that the parasitics of die bonding and circuit tracks inside the FCOF package are much lower than those of commercial module and discrete device. This is expected since the length of solder bump is about 2% of the length of wire bond. Furthermore, due to the three-dimensional packaging structure, the FCOF package has lower profile and offers an additional degree of freedom for minimizing track inductance.

6.6 Thermal Consideration

In conventional one-dimensional wire-bonded planar packaging, there is no thermal path on the wire-bonded face of the device. In order to get the heat out of the device; the die is always soldered to the copper conductor layer, resulting in a unidirectional thermal dissipation. The common methods of cooling in commercially available power modules have already reached their limit and to further improve thermal performance, the waste heat has to be dissipated more efficiently [19-21]. The stacked solder bumps in Cavity-down flip chip on flex and D^2BGA chip-scale packages as well as FCOF module are thick and they occupy a large portion of the power chip area. They help extract heat from the devices. In the FCOF module, the power chips are backbonded to the bottom DBC substrate, which has high thermal conductivity. Designs have been proposed which combine a solder backside die bond with solder bumps to give extremely low thermal resistance-on the order of 0.4 °C/W for chips joined directly to a water-cooled plate in a MCM [22-23]. This would give a power capability of over 100W per chip [24]. Furthermore, the interior space between the top and bottom substrates and the stacked solder bumps provide an additional area for thermal management. When this volume is filled with a solid (or non-flowing liquid) dielectric, additional thermal spreading from the power devices and solder bumps to the rest of the module structure occurs, reducing thermal resistance. The edges of the module are then also available as a possible thermal dissipation path. Therefore, three-dimensional heat dissipation can be realized, as show in Figure 6.21.

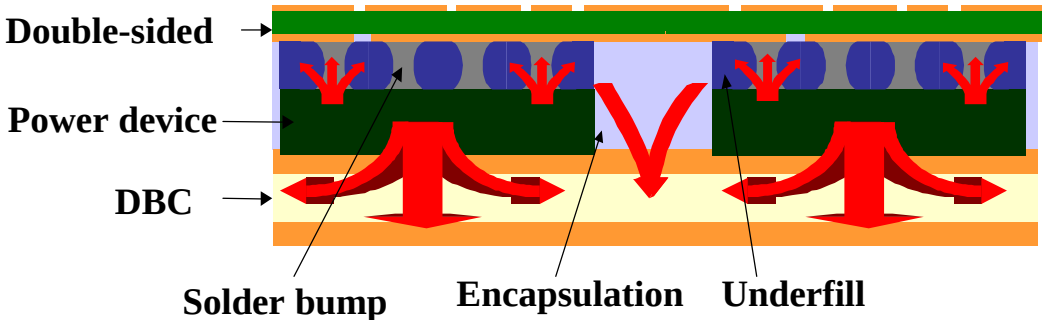


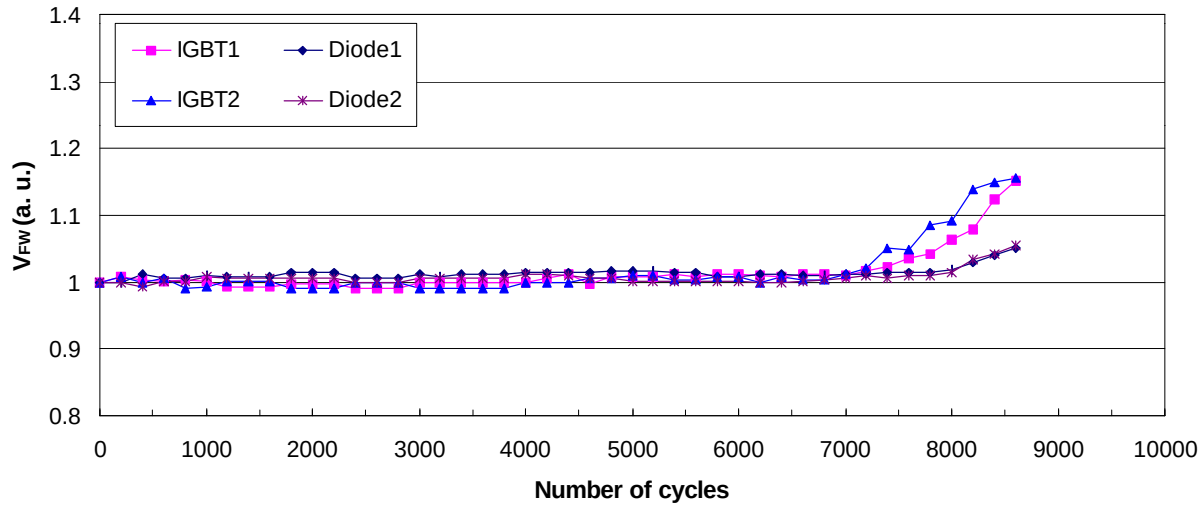
Figure 6.21. Three-dimensional thermal paths of FCOF module.

6.7 Reliability Assessment

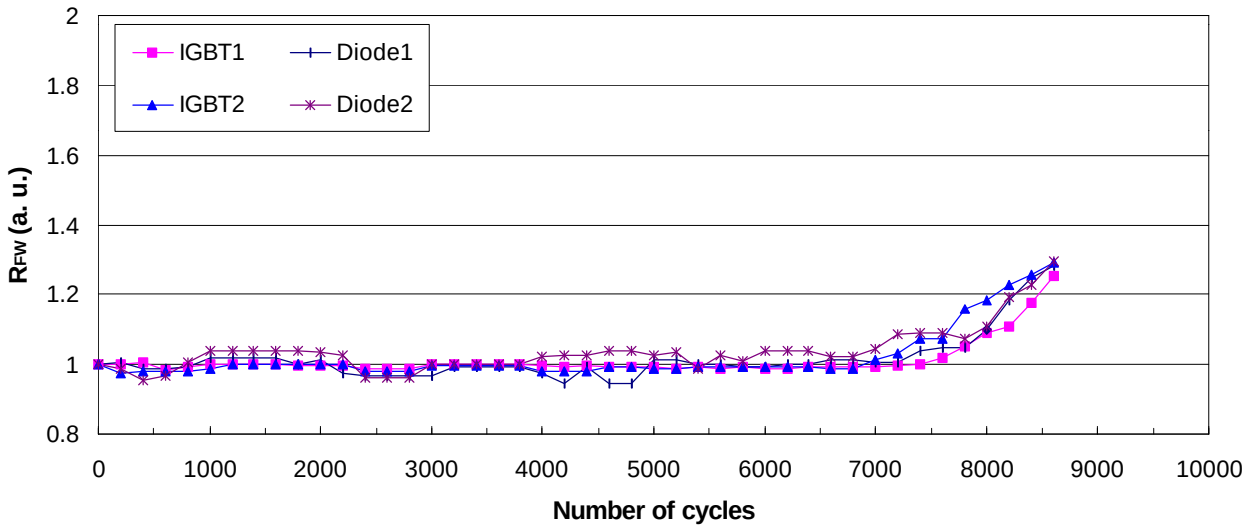
For flip chip on flex IPEM, failure is likely to happen at two locations. One is the front chip interconnection-solder joint. The other is the back side of chip-die attach solder layer. Thermal stresses in solder joints caused by CTE mismatch between top substrate and silicon are the main causes of failure in solder joint interconnections. For the die attach solder layer, fatigue failure is also caused by the CTE mismatch between IMS/DBC substrate and silicon.

As we discussed in Chapters 3 and 4, an optimized solder joint geometry for device interconnection, a compliant substrate, and underfilling materials reduce the shear strain and thus improve solder joint reliability. Thermal cycling test were conducted on flip chip on flex power modules as well as commercial wire bonded IGBT power modules to evaluate thermal fatigue lifetime. If we assume that thermal fatigue failure is the dominant failure mechanism for the designed IPEM operated in field environment, we can project the reliability of the FCOF IPEM. The changes of collector emitter voltage drop ($V_{CE(sat)}$) of IGBT devices and/or forward voltage (V_F) of diodes, noted as V_{FW}, as well as the slope of the forward characteristics (dV/dI), noted as R_{FW}, were used as the evaluation criteria. When V_{FW} and R_{FW} increase 20%, we regard the test samples fail. After every 200 thermal cycles, the modules were systematically tested. Figure 6.22 and Figure 6.23 show the typical V_{FW} and R_{FW} changes of the two IGBTs and two diodes in a FCOF power module and a commercial wire bonded power module, respectively, as a function of the number of cycles. The values of the forward voltage for IGBTs and MOSFETs were normalized for comparison purposes. From Figure 6.22 and Figure 6.23, we can see that fatigue lifetimes of all the configurations obtained from V_{FW} criterion are significantly different from those obtained from R_{FW} criterion, with R_{FW} criterion being more sensitive. It seems that FCOF modules have higher fatigue life than wire bonded power module, but this is not conclusive since

our reliability data on commercial wire bonded power module is limited. After the V_{FW} and R_{FW} of the IGBTs and diodes in commercial power module had obvious increases, their forward curves were distorted, as shown in Figure 6.24. However, the shape of the forward curves of IGBTs and diodes in FCOF power module was still normal after V_{FW} and R_{FW} had evident increases.

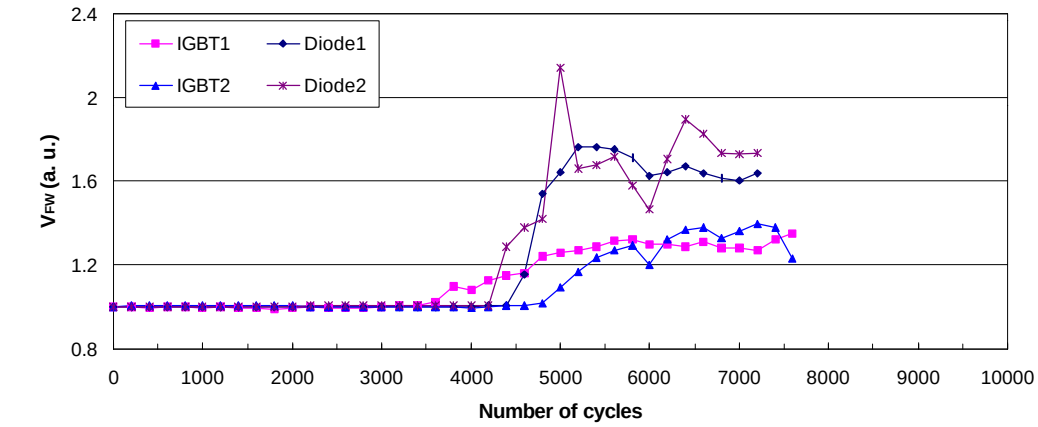


(a)

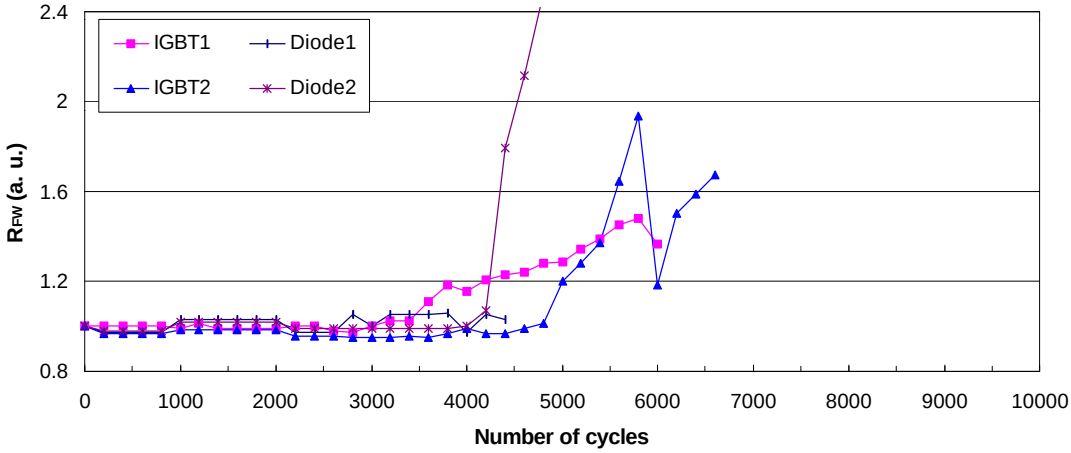


(b)

Figure 6.22. Typical (a) forward voltage and (b) resistance changes of the two IGBTs and two diodes in a FCOF power module versus number of thermal cycles.

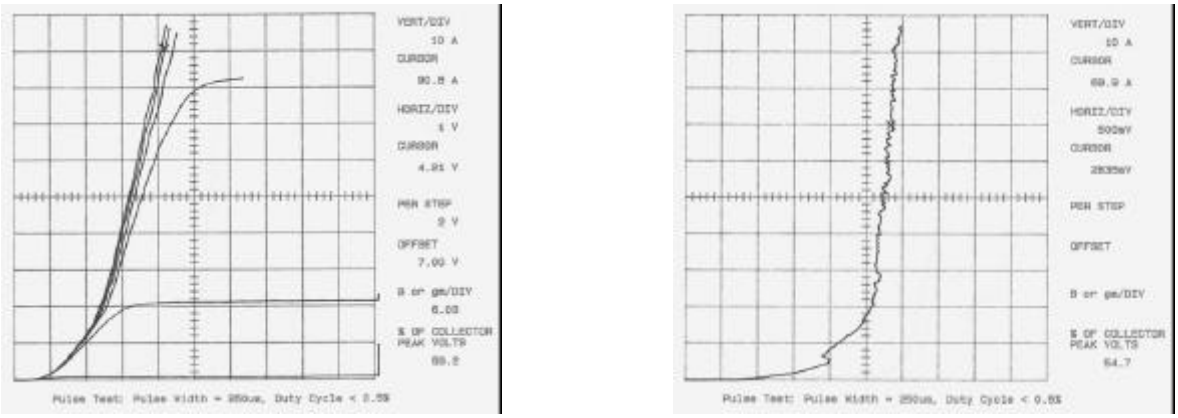


(a)



(b)

Figure 6.23. Typical (a) forward voltage and (b) resistance changes of the two IGBTs and two diodes in a commercial wire bonded power module versus number of thermal cycles.



(a) (b)

Figure 6.24. Distorted forward curves of IGBTs and diodes in commercial power module after forward drops have obvious increase; (a) IGBT; (b) diode.

Similar to high standoff hourglass-shaped solder joint interconnected chip-scale power packages, we believe die attach solder fatigue failure is the dominant failure mechanism in FCOF modules. Figure 6.25 shows C-SAM image of the interface between IGBT solder joint and flex substrate in a FCOF power module. We can see that there is no obvious crack at the interface between solder joint and flex substrate. Figure 6.26 shows failed commercial wire bond power module. We did not notice evident wire bond failure in the failed module, but there was obvious wire bond heel necking and power bus connection fatigue failure, as shown in Figure 6.26 (a) and (c). Furthermore, broken wire bond residues left by manufacture process were observed, as shown in Figure 6.26 (c).

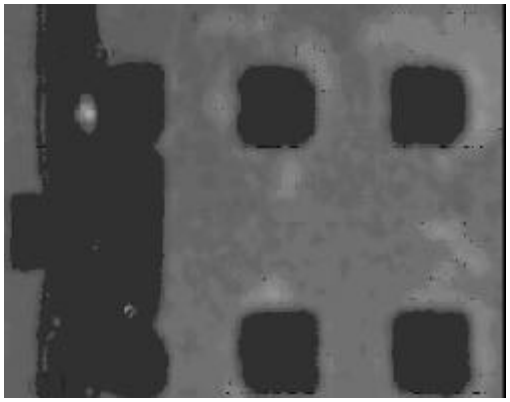
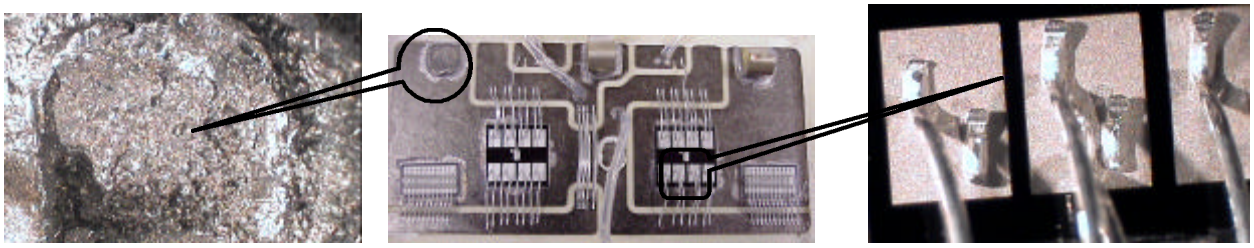


Figure 6.25. C-SAM image of the interface between IGBT solder joint and flex substrate in a FCOF power module.



(a) (b) (c)

Figure 6.26. Failed commercial wire bond power module; (a) Output lead failure; (b) overview of failed open module; (c) Wire bond heel necking and wire bond residue left by manufacture process.

6.8 Summary

A three-dimensional multichip power module structure has been developed by using solder bumped power chips. Several versions of FCOF module have been built and tested up to 800 V and 90 A for functionality. This three-dimensional structure not only makes power

module miniature possible, but also offers better electrical performance both by eliminating the wire-bonds and minimizing track inductance. The FCOF module has reduced parasitic inductance by 40% to 50% over conventional wire bond power module. Three-dimensional heat dissipation could be achieved in this FCOF structure. Temperature cycling test showed that this FCOF module is quite reliable and is potentially more reliable than wire bond power modules.

6.9 References

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