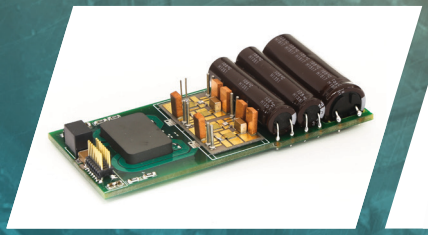
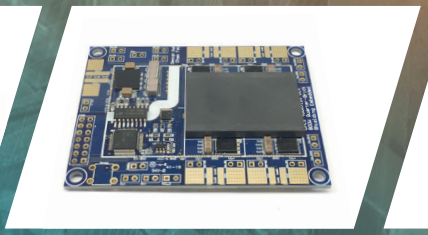
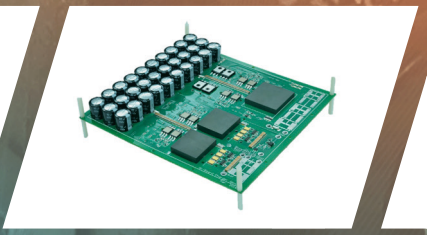
CPES

Center for Power Electronics Systems

Annual Report 2017







VirginiaTech

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Introduction

The Center for Power Electronics Systems (CPES) was established as a National Science Foundation Engineering Research Center (ERC) in 1998, and since then has become world-renowned for its research and education/outreach programs. The power electronics program was first initiated in 1977 under the name PERG (Power Electronics Research Group). Later, in 1983, the program was renamed to VPEC (Virginia Power Electronics Center) when it became a university center. In 1987, VPEC became a Technology Development Center (TDC) of Virginia's Center for Innovative Learning (CIT).

The CPES mission is to provide leadership through global collaborative research and education in creating advanced electric power processing systems of the highest value to society. Specifically, CPES is dedicated to improving electrical power processing and distribution that impact systems of all sizes—from battery-operated electronics to vehicles to regional and national electrical distribution systems. On the lower-power side, CPES has continued to make notable technological advancements. Many of these new technologies have arisen through the CPES Power Management Consortium (PMC), which has experienced immense growth over the years. Additionally, CPES has a keen interest to support and grow the development and integration of higher-power electronics at the power grid level. CPES intends to further explore these technologies by increasing its research efforts in this area.

In early 2017, Virginia Tech announced the Energy Innovation Initiative, which will significantly expand its research and education program in power and electronics systems. The idea is to broaden the programs towards power-electronics-based innovations in all forms of generation, transmission, distribution, and consumption of electrical energy. The university and its partners are planning up to $15 million as start-up support, and has appointed CPES to lead this effort.

Moreover, despite the ever-changing times, the CPES Industry Consortium has continued to thrive, and government funding has been strong amidst the shifting political climate. In order to keep up with the increasing research demands, CPES has been growing its graduate student population. With more students and new research endeavors, the prospects of CPES are bright and alive with excitement.

From Fred C. Lee

Fred C. Lee
CPES Director

Dear friends:

I first set foot on this land of opportunity in 1969 with the idea of pursuing an advanced degree in the field of electrical engineering. At Duke University, I was blessed to meet a great teacher and my life-long mentor, Professor Thomas G. Wilson, who introduced me to the wonderful world of power electronics. Upon graduation from Duke, I had a brief tenure in the aerospace industry in Los Angeles; then I decided to switch to an academic career. I was fortunate to arrive at this "Hokie" nation. My wife Leei and I immediately fell in love with its beautiful campus, set in the midst of the Blue Ridge Mountains. It was such a welcome contrast to the massive city of Los Angeles and the hustle and bustle of freeway traffic.

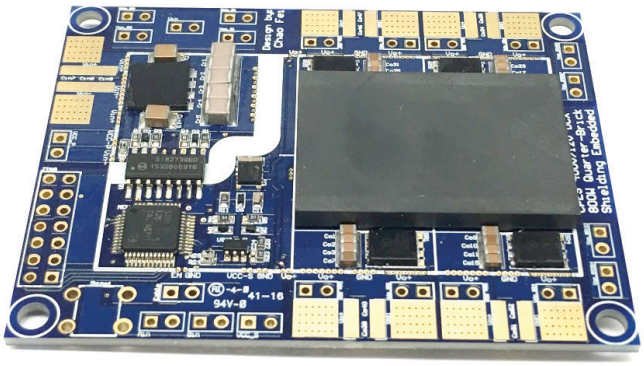
As you know, when you love your work and enjoy the place you live, time flies. This year marks the fortieth anniversary of my arrival in Blacksburg. During the past four decades, I have been blessed with the opportunity to work with many talented faculty members, staff members, and graduate students. They have touched my heart, challenged my intellect, and shaped my life in every way imaginable.

My special thanks go to Dushan Boroyevich for his unwavering friendship and support that I can always count on, a true partner in research and in management of CPES for the past three decades; to Teresa Shaw for her incredible energy and dedication, and her incredibly big heart and ability to forgive and forget; to Prof. Dan Chen for his partnership and support in getting the power electronics program off the ground; to Prof. Daan Van Wyk for his kindness and infinite wisdom; to Drs. Bo Cho, Ray Ridley, Ming Xu, Paolo Mattavelli, Qiang Li, and many other extremely talented faculty members who worked closely with me; to Linda Long and Ann Craig for their rigorousness and discipline in financial matters that kept me out of trouble, especially during NSF ERC time; to Beth Tranter for her incredible effort for making CPES a model ERC in education and outreach programs; the list goes on.

I am extremely proud of my students for their accomplishments in their respective workplaces. They are the source of my pride. I also have had the great fortune to work with brilliant visiting professors and scholars from all over the world. Last but not the least, I am very thankful for the privilege to work with so many highly esteemed global corporations through the Center's Industry Partnership program. It is their generous donations of money and precious time that have set our Center apart to become an envy among our peers.

The time has come for me to pass the helm of CPES to Dr. Dushan Boroyevich, who has been the Center's Co-Director for the past 20 years, to lead the Center into its future. As to my own future, I will stay at Virginia Tech as an emeritus professor, and continue working with my colleagues and supervising graduate students on a part-time basis.

I want to take this opportunity to thank all of you for your generous support for the past 40 years, and to share with you some of my reflections over the past four decades.



A high frequency dc-dc converter.

Highlights of PERG/VPEC/CPES

Four Decades of Developments

A humble beginning

I was hired in 1977 with the expectation that I would fix a broken electric car that was a gift to the EE Department from a local utility company. Instead of fixing the car, together with colleagues at Virginia Tech, I secured a DOE grant and built a new EV drive using the first generation of giant bipolar transistors and a permanent magnet brushless DC motor. Since then, this drive system has been in the mainstream of EV propulsion. In 1979, Professor Dan Chen was hired by the EE Department. Dan Chen and I formed a small research group and named it PERG, Power Electronics Research Group. One notable PERG project was a collaboration with the Naval Ocean Systems Center that demonstrated the first transistorized cascade multilevel inverter for powering the very-low-frequency transmitter amplifier for submarine communication. This technology was eventually commercialized for medium-voltage motor drives in the '90s by Robicon, a Westinghouse spin-off and now a subsidiary of Siemens.

In the intervening four decades, the world has undergone a series of transformational changes on many fronts, such as information technology, industry automation, infrastructure technology, and the electrification of all forms of transportation systems. In each of these cases, the field of power electronics has played a critical role in enabling the changes in these important industries, which have profoundly changed the world we live in.

Virginia Tech began its power electronics program at a time when only a handful of universities in the country offered such a program. The timing couldn't have been better. With strong institutional support, the small research group that started as PERG has been on the cutting edge of these technology trends, and has made great strides as each trend became a force in the marketplace.

Fred Lee (left) in the early years of power electronics research at Virginia Tech.

Virginia Power Electronics Center (VPEC)

VPEC became the new name of PERG in 1983. At the same time, the Industry/University Partnership Program was established, which had the goal of developing a research agenda that meets industry needs while allowing industries to profit from the Center's research and perspectives. In the subsequent years, two faculty members, Professors Bo Cho and Vatché Vorpérian, were hired under VPEC. The Center was well-positioned to be on the verge of the explosive growth of computer and communication industries.

VPEC pioneered the concept of soft switching and was awarded the first zero-voltage switching patent in the world. In the following years, the Center developed a series of soft-switching technologies, known as quasi-resonant, multi-resonant and soft-switching PWM, with over 20 related patents awarded. These techniques enabled a dramatic reduction in switching losses, stresses, noise, and EMI. These soft-switching technologies have become the core technologies of the power electronics equipment currently used in information technology (IT), military, aerospace, commercial, and industrial applications; resulting in much improved

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reliability, energy efficiency, and reduced system size and cost.

In 1987, VPEC was selected through a competitive process as one of Virginia's Technology Development Centers under the Virginia Center for Innovative Technology (CIT), with the mission of promoting economic development in the State of Virginia. During this year, Dr. Ray Ridley was hired upon his graduation to serve as VPEC's Assistant Director.

> *"Virginia Tech began its power electronics program at a time when only a handful of universities in the country offered such a program.* ***The timing couldn't have been better."***

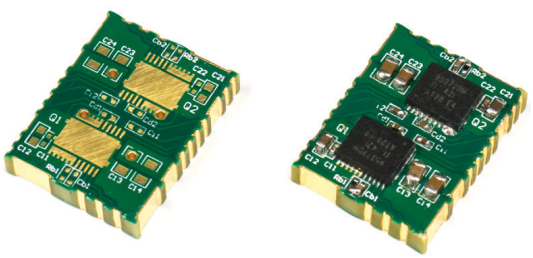
High-power infrastructure technologies

High-power infrastructure technologies were identified as a new research thrust at the Center when Professor Dushan Boroyevich rejoined VPEC in 1990 as faculty, after earning his Ph.D. at VPEC in 1986. The Center began its effort to develop high-power technologies aimed at applications related to advanced infrastructure development, such as large power systems for mainframe computers, the manned Mir Space Station, and transportation systems that included electric vehicles, more-electric aircraft, and ships. The Center received multiple grants from IBM, NASA, DOD, DOE and the Navy. This high-power program was elevated to a higher level when Professor Alex Huang joined the Center in 1994.

The Center devoted significant efforts towards Power Electronics Building Blocks (PEBB) under an ONR-funded program, with an emphasis on developing highly integrated modular functional building blocks to facilitate system-level integration. This concept has taken off in earnest and has now become common practice for a wide range of high-power applications. VPEC's efforts in PEBB development eventually culminated in the next big move.

CPES (Center for Power Electronics System) was established in 1998, as an Engineering Research Center (ERC) under the National Science Foundation, with the vision of developing integrated power electronics modules (IPEMs) to facilitate system-level integration in a manner similar to the way integrated circuits are used in microelectronics. The Center consists of Virginia Tech (the lead institution), University of Wisconsin-Madison, Rensselaer Polytechnic Institute, North Carolina A&T State University, University of Puerto Rico-Mayaguez, and an industrial consortium of 96 corporate partners. The multi-institutional collaboration resulted in the development of advanced integration technologies for various forms of IPEMs with demonstrated improvements in electrical and thermal performance that are suitable for automation.

The rapid adoption of the Intelligent Power Module (IPM), a concept similar to IPEMs, has been steadfast, and IPMs are now used in every electric hybrid vehicle, as well as in over 60 percent of small variable-speed motors. The adoption of the IPEM approach in the IT industry began in earnest in the early 2000s. One example of IPEM technology is DrMOS, an integration of power MOSFETs with drivers and control, which is widely used in power supplies for the IT industry. The multi-phase voltage regulators (VRs) used to power Intel processors was originated by CPES. We have subsequently generated over 25 related U.S. patents that address key areas such as power delivery architecture, modularity and scalability, control and sensing, integrated magnetics, and advanced packaging and integration. Today, every microprocessor incorporates multiphase VRs, which can also be found in high-end



Multiphase VRs.

graphics processors, memory devices, telecommunications networks, and all forms of mobile electronics.

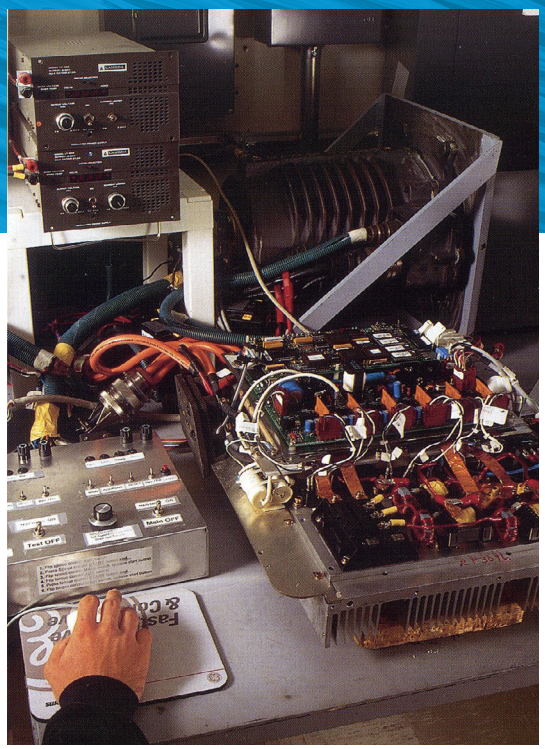
During this period, a slew of exceptionally talented people were added to the CPES faculty team, including Professors Daan Van Wyk, Khai Ngo, Ming Xu, Fred Wang and Rolando Burgos, further strengthening our capability in circuit design, magnetics, electronics packaging, and system integration for a wide range of applications.

The Center was cited by NSF as the model Engineering Research Center (ERC) for its Industry Collaboration and Technology Transfer Program and Education and Outreach Program. There have been programs that emulate these in both Europe and in Japan.

Post-ERC era

Since its graduation from the NSF ERC program in 2008, CPES has clearly demonstrated fiscal sustainability with increasing commitment from industry partnerships. The key factor for this growing industry support was the creation of the Principal Plus Membership and the Intellectual Property Protection Fund (IPPF) within the Center's Industry Partnership program. This expansive program enables industry members to sponsor graduate fellowships and provides them the opportunity for directed research in areas of mutual interest, with the ability to access IPs generated through this fellowship program on a royalty-free, non-exclusive basis. The program has grown dramatically since its founding.

The Center structures the industry-funded graduate fellowships into three clusters to enhance synergy and teamwork among graduate students. These three clusters, also referred to as mini-consortiums, include: Power Management (PMC), High Density Integration (HDI), and Wide-Bandgap High-Power Converters and Systems (WBG-HPCS).The primary research objective of this industry-funded fellowship program is to develop precompetitive technologies to be shared among all participating members. The Industry Partnership program is designed to complement the industry-sponsored contract research, which is usually aimed at supporting industry to commercialize the technology generated under the industry fellowship program.



PNGV Electric Vehicle Testbed.

Numerous technology transfer activities have taken place as the result of this two-pronged approach, which is unique among our peer institutions and deemed a particular strength. It was during this post-ERC era that professors Paolo Mattavelli and Qiang Li were added to the Center faculty.

Industry partnership program

Since its inception in 1983, more than 215 corporations worldwide have benefited from the Center's research output and intellectual properties. This strategy is unique and has been the backbone of the Center's various programs, which encompass education, research, outreach, industry collaboration and technology transfer. The partnership program has enabled the Center to devote its research to forward-looking technologies over the past 35 years. To date, the partnership program has generated over $31M in gift support, along with numerous industry-funded contract research projects. In 2016 alone, our members have generated $2.5M in gift funds with over 40 Industry-funded graduate fellowships. Membership support is essential to providing a stable cash flow for the operation of a soft-money based center of this size, which includes five tenure-track members, 50 graduate students and 7 staff members. The Center

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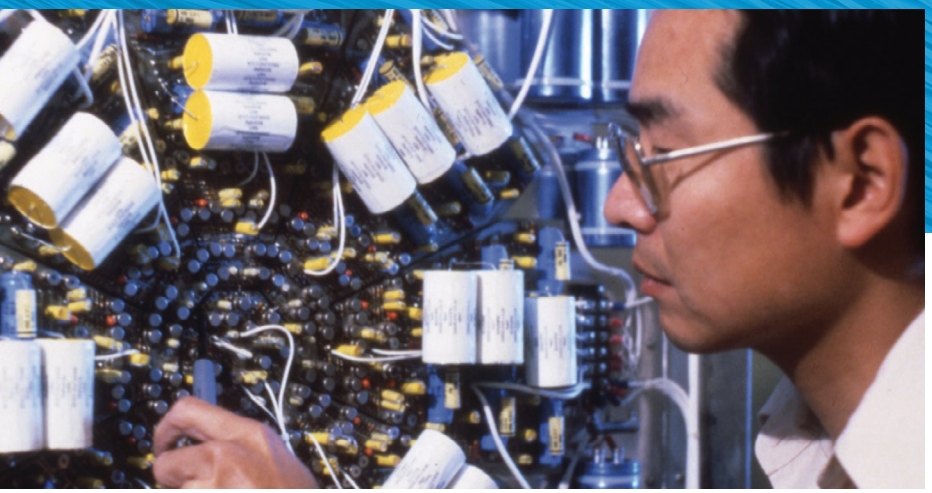


Fred C. Lee with nondestructive second breakdown tester for power semiconductor devices.

also hosts and supports 10-15 visiting professors and scholars annually.

The grand challenge

Now the world is facing the pressing need and the grand challenge of building a sustainable energy future with a large penetration of renewable energy sources into our aged electrical grids. There is enormous potential in the development of power electronics, which is to be driven by emerging technologies such as the changing power grid structure, an intergrid of future electronic energy networks, offshore wind power, multilevel cascade converters for interconnection of DC and AC grids, high-voltage DC transmission, solid-state transformers in traction and smart grids, large battery storage, and new control technologies. For CPES to continue playing the leading role in this revolutionary future, the Center has to re-position itself to establish a global alliance with government agencies, industries and universities. This forward-looking vision comes from my colleague Professor Dushan Boroyevich, who has been serving as the Center Co-Director for the past 20 years. Now it is time for me to pass the helm to Dr. Boroyevich to materialize this grand vision. This grand vision is supported by the administration with strong commitment in the form of additional faculty positions and other resources. As to my future, I will remain a member of this team. I am looking forward to this bold move and I am eager to support it.

In closing

The Center could not have been on this path of steady growth for the past four decades without our numerous talented and dedicated graduate students, faculty members, and staff. Over the last four decades, the Center has graduated over 150 PhD students and 170 MS students. Many of them are serving as leaders in their chosen fields. A significant number of them chose to found their own enterprises, of which two start-ups are now publicly-held companies.

In addition, the Center has hosted over 150 visiting professors and scholars. The Center has also published over 3100 technical papers, theses, and dissertations and 18 volumes of the CPES book series. The Center has filed over 280 invention disclosures and has been awarded 103 U.S patents. Besides its highly successful industry partnership program, the Center has performed more than 875 government- and industry-funded sponsored research projects and raised over $150 million of research funding.

In hindsight, I am glad that I chose the field of power electronics and an academic career. I am most privileged and fortunate to be able to work with this wonderful team, which has received strong support and commitment from this great institution, Virginia Tech, to which I have devoted almost my entire career.

"Ut Prosim - That I may Serve"

—Fred C. Lee
CPES Director

Continuing the challenge

How to change the world, Fred Lee style

Fred, Fred C. Lee, 李澤元 , Dr. Lee: Tens of thousands of people around the world, who know the meaning of the words "power electronics," from students to presidents, know about Virginia Tech because they know about Dr. Lee. How did this come about? It is really quite simple. Just 40 years of unwavering focus on quality: in high-frequency power conversion research, in graduate student education, and in effective technology transfer to industry.

Secondary breakdown, multi-level, resonant, power MOSFET, soft-switching, quasi-resonant, multi-resonant, zero-voltage, zero-current, soft-transition, off-line, PFC, current-mode control, subsystem interaction, minor loop-gain, forbidden zones, PEBB, DPS, VR, multi-phase, IPEM, coupled inductors, EMI, integrated magnetics, POL, GaN … The arcana of the fast-changing field of high-frequency power conversion are rich and often baffling, yet a source of great excitement and pride for power electronics engineers and so inextricably associated with Fred's name. The technologies that Fred C. Lee has pioneered result in much-improved reliability, energy efficiency, and reduced system size and cost of power conversion systems, impacting most aspects of human life, ranging from personal computing and mobile devices to military, aerospace, commercial, industrial, and renewable energy applications. For example, POL converters incorporating many ideas generated by CPES power every "smart gadget" today.

Fred firmly believes that engineering research in academia has a very clear mission: to educate graduate students in an open and sharing environment and to transfer any useful results to industry as fast as possible. In pursuit of quality, we search the globe for the best and hardest working minds, and provide them with the best academic power electronics lab in the world, where they generate and share knowledge, without walls or barriers. Then, it is again simple: just basic circuits, semiconductors, magnetics, modeling and control, and understanding their interplay through theory, simulations, and building hardware from scratch. And every single person in the lab has to attain this deep and intuitive understanding, and build the hardware from the scratch, and make the best presentation every week, and …

Understanding! There are no problems, just challenges, and challenges are easy to overcome if you understand. And Fred is forever challenging us to understand. All of his students and co-workers recall months of trying to explain to Dr. Lee their new ideas and constantly being challenged, even about basic assumptions and concepts. Finally, in frustration, you are not sure if you are completely incapable of understanding anything, or if you got stuck with the advisor and supervisor, who just doesn't get it? Until you accidentally overhear Fred telling to someone else: "This is the best idea I've seen in a long time; you should use it!" You finally feel good, but don't relax. There are many new challenges, for many new months, and many years. Fred has served as major advisor to more than 150 graduate students and has published with them over 1000 papers. He is one of the top three best-cited authors among 2.5 million engineering authors in the world!

Papers are never enough, however. How to transfer this knowledge to industry in a more immediate and tangible way? Fred has always thought that having research contracts with industry is great: they provide major resources for significant inventions with a large group of students. But, they also constrain the distribution of knowledge and limit the impact on society. It would be much better if we could have one contract with all the companies in the world that work in our technology field. So, across 30 years, Fred has developed a globally unique model of university-industry partnership that challenges the companies to provide continuous support and guidance for specific research objectives that produce beneficial results shared by everyone. This expansive program enables industry members to sponsor graduate student research, and provides to industry the opportunity for directed research in areas of long-term interest, with the ability to use and share the IP. Just 80 companies now and more than 200 in the last 30 years.

Fred is tough, Fred is demanding, Fred is competitive and can be brash, but you can always count on him to do the right thing in the end. We are all delighted that Fred will continue to serve us, Virginia Tech, and the world, and that we all will continue to be challenged by him.

Just 40 years of relentless pursuit of quality in the open and sharing environment. Everything else is a distraction: fishing, boating, travel, cars, sports, start-ups, money, administration … It is all great to try, get excited, have fun, have something to talk about … and then focus back on power supplies, graduate students, industry partnerships, and family:

It's hard to say, but we love you Fred!

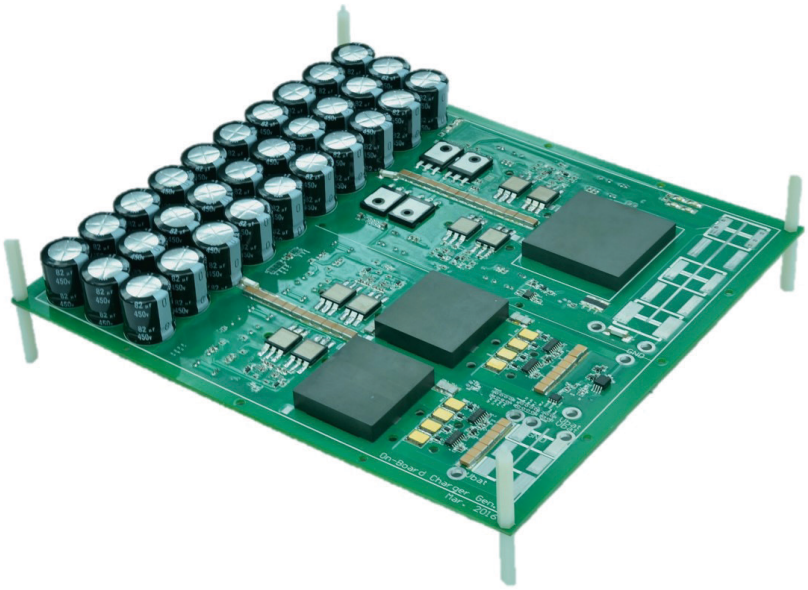
—db

Thanks from all of CPES!

Leading the way

Cutting edge advancements

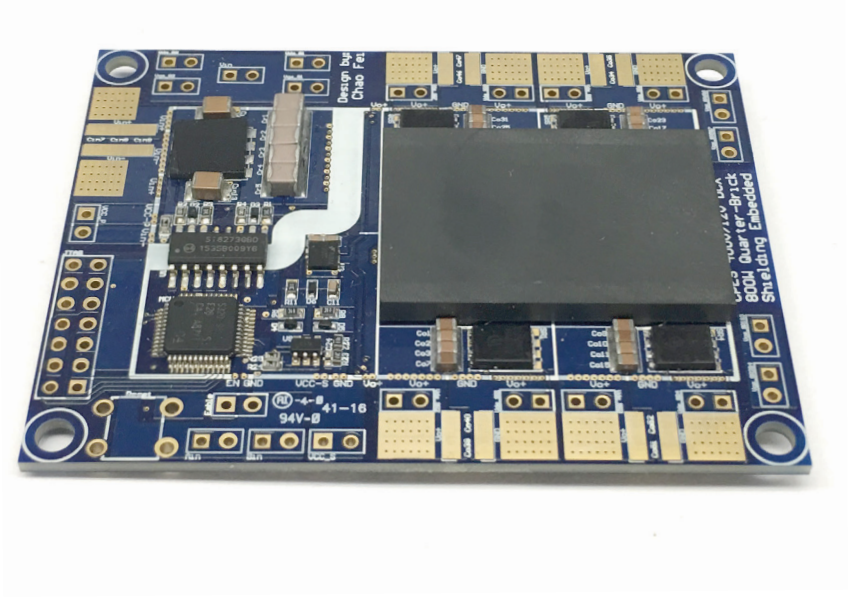
High Frequency High Density WBG-Based 6.6 kW Bidirectional On-Board Charger



A wide bandgap (WBG) devices based 6.6 kW bidirectional on-board charger (OBC) system is recently developed for plug-in electrical vehicles (PEVs). With proposed novel variable dc-link voltage system architecture, high frequency soft switching operation, and PCB winding-based integrated magnetics, the OBC system achieves over 96% peak efficiency in the entire battery charging profile while the state-of-the-art product can only achieve 94% peak efficiency in a narrow loading range. At the same time, its power density is 37 W/in^3 which is 3~5 times better compared to the best industrial practice. Furthermore, the inductors and transformers are integrated with PCB winding which simplify the labor intensive manufacturing process significantly and make the whole system ready for manufacturing automation.

800 W 400 V/12 V LLC Converter

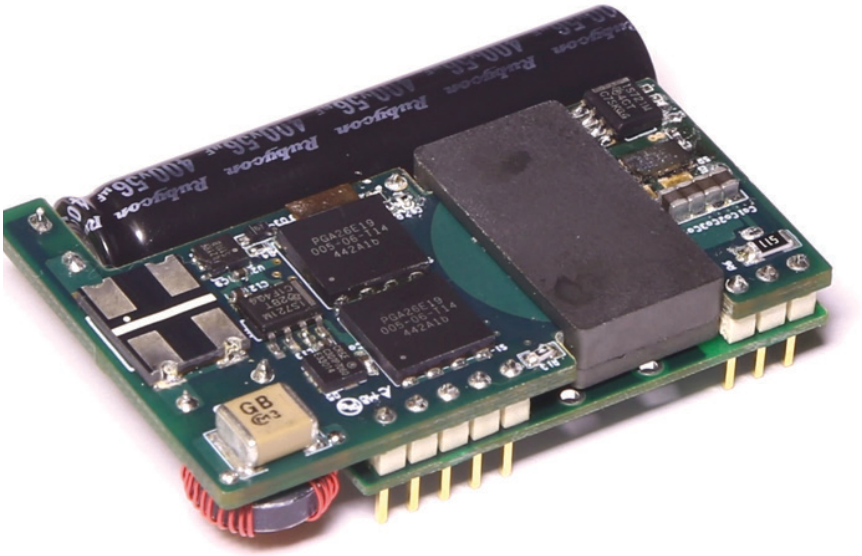
This is an 800 W 400 V/12 V LLC Converter, operating at 1 MHz with GaN devices. It achieves a peak efficiency of 97.6%, which is the highest efficiency demonstrated at such high switching frequency. This converter employs a novel matrix transformer structure which integrates 4 transformers into 1 magnetic core. With those techniques, the converter achieves a power density of 900 W/in^3 and satisfies the quarter-brick footprint requirement. This is the first prototype meeting iNEMI's requirement for the dc-dc converter of the future data center architecture.



Leading the way

Cutting edge advancements

High Density High Efficiency Adapter



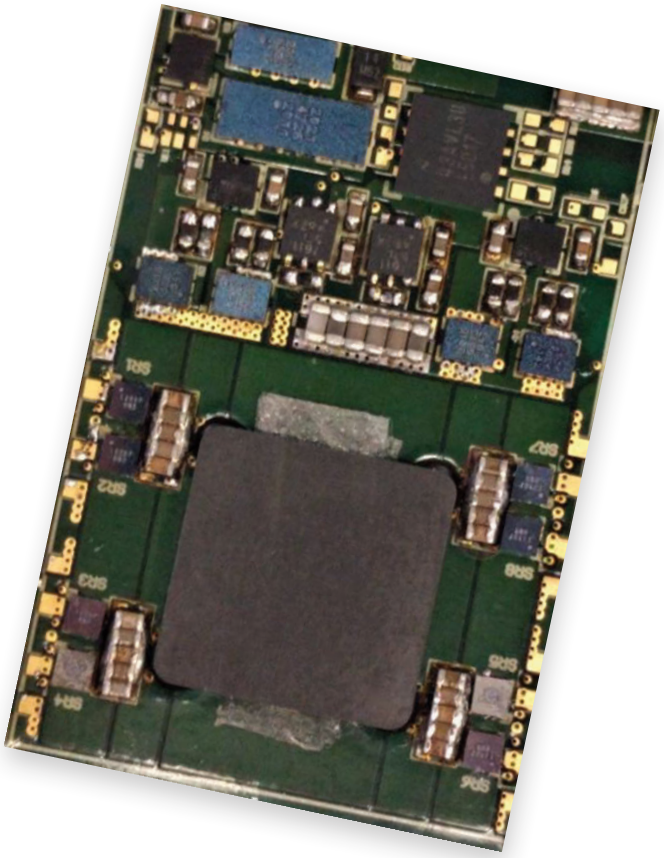
One of the biggest power supplies markets, in both volume and revenue, is the ac-dc adapter/charger for consumer electronics. The market is projected to surpass $8 billion in 2015 and reach $9 billion by 2018; with much of this growth being driven by smart phones, tablets, and a number of emerging applications. The adapter is strongly driven by efficiency and power density for all forms of portable electronics. Most adapters only operate at relatively low frequencies (<100 kHz), with state-of-the-art efficiency up to 91.5%. However, low-frequency operation limits the adapter power density to 6-9 W/in^3. The emerging GaN device is deemed a game-changing device in this particular application, with improved efficiency and significant size reduction.

To realize the full benefits of GaN, a number of issues have to be addressed carefully, including soft-switching topology selection, high-frequency magnetics, control, packaging, gate drives, and thermal management. The research team at CPES successfully demonstrated that the GaN-based adapter design is capable of operating at 1-2 MHz frequencies with an improved efficiency up to 93.5%. Subsequently, a power density of 25 W/in^3, which is a three-fold improvement over the state-of-the-art product, was successfully demonstrated at 45 W and 65 W levels. The adapter is designed with transformer windings fully integrated into the printed circuit board (PCB), which is well-suited for automation during manufacture, and therefore, this will bring significant cost reduction with large scale in manufacturing.

48/1 V Sigma Converter

Efficient power delivery architectures are gaining more attention in the design of future generations of data centers and telecom power supplies to minimize the ever increasing trend of power consumption. 48 V voltage regulator modules (VRMs) have been used in telecom applications for many years, a recent study indicated that 48 V VRMs, instead of 12 V VRMs, is deemed a more efficient and cost effective architecture for data center applications as well.

In this work, a high efficiency, high power density power conversion was accomplished using a one-stage quasi-parallel power architecture known as sigma converter. The proposed power delivery architecture shares the power between two converters connected in series from the input side and parallel connected from the output side, thus, rather than other well-established two-stage solutions, higher efficiency is always obtained. In the proposed 48 V sigma converters, a high efficiency unregulated LLC converter operating as a dc-dc transformer (DCX) was used to deliver the majority of the power, leaving a smaller portion flowing through a less efficient buck converter for output voltage regulation purposes. With the aid of GaN devices and high performance magnetic materials, the LLC-DCX, operating at switching frequency of 1 MHZ, was established using a PCB winding matrix transformer configuration integrating 4 transformers in one core structure. PCB winding inductor and GaN devices were used to build the buck converter responsible of output voltage regulation. This module has achieved an efficiency 93.5% at 1 V output and power density of 420 w/in^3, setting a new record.

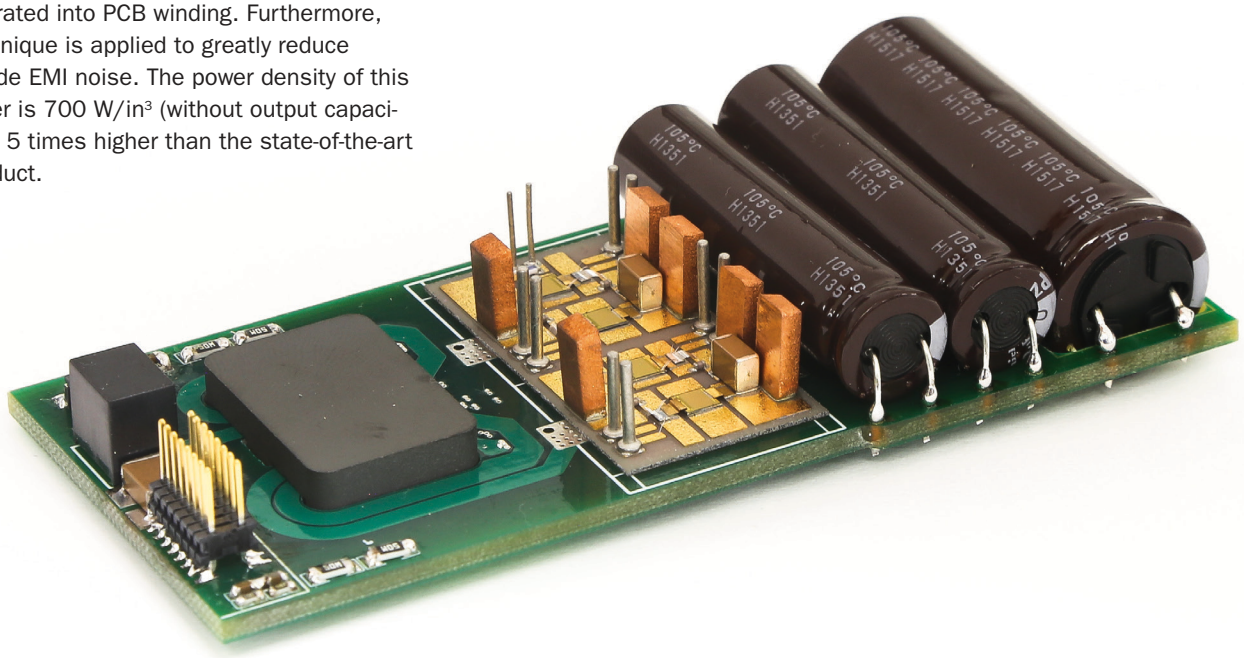


Leading the way

Cutting edge advancements

High Efficiency High Density 1 kW GaN-Based PFC with Integrated Magnetics

A 1 kW PFC converter is developed for server power supply. With a full bridge GaN device module packaged by CPES, the switching frequency is above 1 MHz. With such high switching frequency, the efficiency can still achieve 99%. With coupled inductor technique, it is the first time that the 1 kW inductor can be integrated into PCB winding. Furthermore, balance technique is applied to greatly reduce common mode EMI noise. The power density of this PFC converter is 700 W/in^3 (without output capacitor), which is 5 times higher than the state-of-the-art industry product.



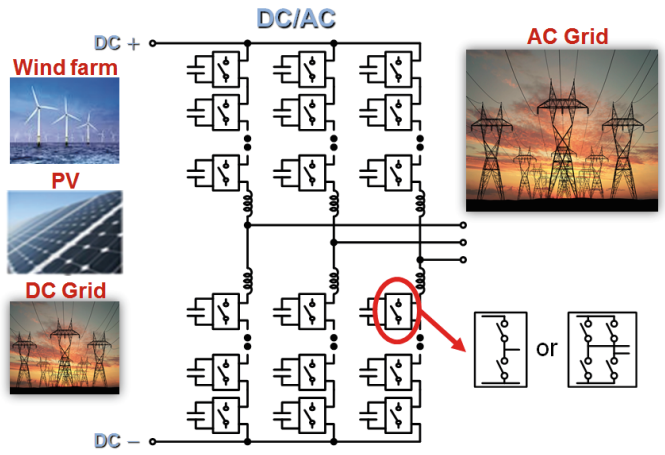
The Medium-Voltage Impedance Measurement Unit (MV IMU)

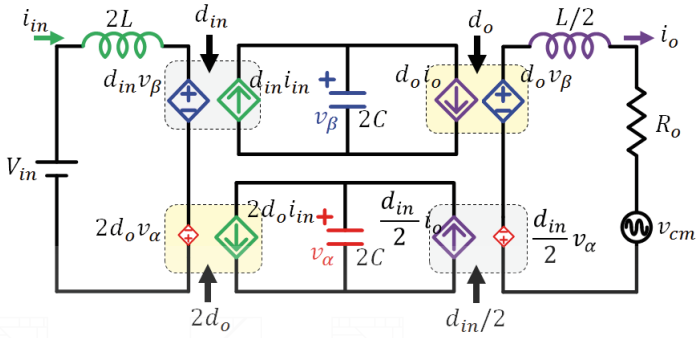
The impedance measurement unit (IMU) developed for the U.S. Office of Naval Research is capable of characterizing in-situ impedances of medium-voltage shipboard power systems (both MVAC and MVDC) in the frequency range from 0.1 Hz to 1 kHz, necessary for system stability assessment. It features a power electronics building block (PEBB) modular concept developed using remarkably powerful 10 kV SiC MOSFET modules, and can significantly aid design of the advanced U.S. Navy shipboard platforms with contemporary all-electric architecture. The IMU aligns well with the ESRDC goals to ensure the United States' superiority in electric systems for critical applications, and is seen as necessary and unprecedented technology to develop cutting-edge MVDC systems that feature high reliability and survivability without compromising stability. The IMU itself is an electronics power converter, and its built-in impedance measurement capability, both developed in CPES, most likely present the first ever successful engineering attempt to measure medium-voltage system impedances using modern silicon carbide-based power electronics converters.

Leading the way

Cutting edge advancements

Decoupled aß Model of Modular Multilevel Converters (MMCs)



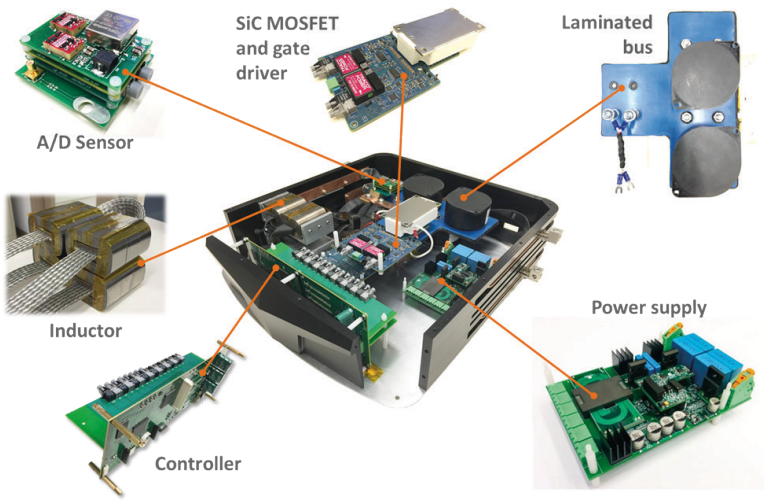


The modular multilevel converter (MMC) is widely adopted in high-voltage applications because of its simplicity and modularity. However, in current practice, a rather large capacitor is required to store line-frequency related circulating energy.

Recently, a state-plane analysis was proposed to decouple the circulating energy into two orthogonal components. Based on this state-plane analysis, a decoupled αβ model of the MMC was proposed. The proposed model accurately explains the flow of delivered power and circulating power. Based on this model, the method of eliminating circulating powers are clearly delineated from that of the delivered power for the first time. Up to 90% of capacitor bank reduction can be realized using the suggested method of control.

Power Electronic Building Blocks (PEBB)

The 100 kW SiC-based power electronics building block, dubbed PEBB 1000, features high scalability and modularity. This feature allows numerous power conversion topologies to be implemented by series and parallel connections of numerous blocks (PEBBs) in order to achieve practically any required current and voltage level. SiC-PEBBs 1000 will enable, for the first time, the notion of a high power density PEBB-only integrated power system benefitting from the system and commercial advantages featured by the PEBB modular concept, and from the exceptional power processing capabilities offered by SiC semiconductors. Advanced hierarchical control under development for PEBB 1000 will allow for ultra-high scalability of more than 1000 PEBB nodes per converter. Rated at 100 kW, PEBB 1000 truly is a one-of-a-kind power electronics converter, boasting a smart-gate driver with integrated Rogowski current sensor for outstandingly fast short-circuit protection, advanced current control, and high common-mode noise rejection, all provided at 100 kHz of switching frequency.



Statistics

$153M+
Research expenditures

225
Companies have belonged to the CPES Industry Consortium

153
PhD degrees awarded

103
Patents awarded

25
Startup companies founded by CPES alumni

294
Visiting professors, students, and industry engineers

2
National Academy of Engineering members

20,000
Square feet of space

887
Research projects sponsored by government and industry

2880
Conference and journal papers

176
Master's degrees awarded

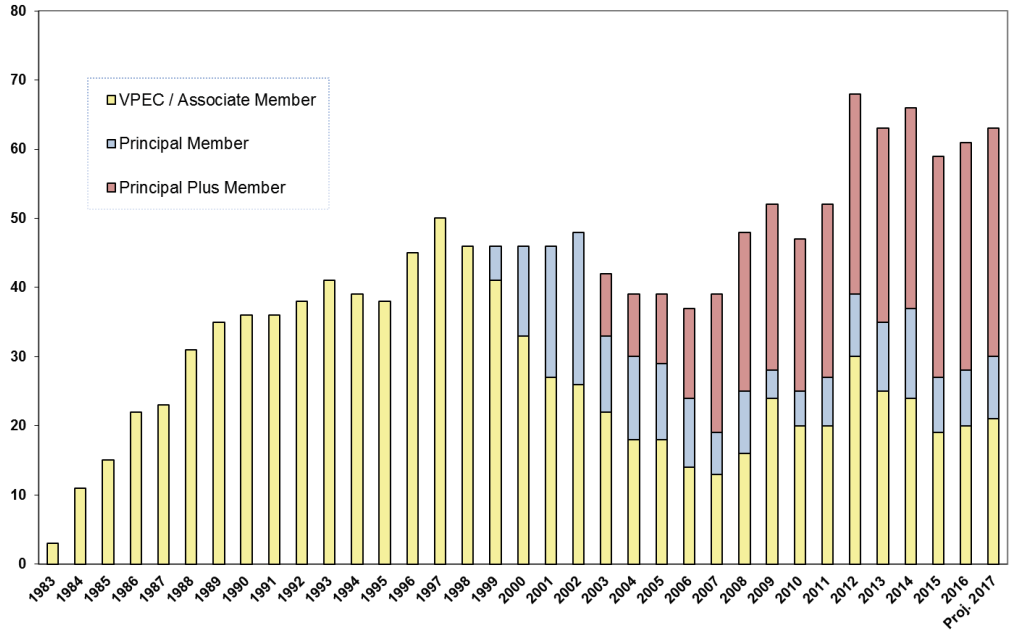
286
Invention disclosures filed

15
CPES alumni in academia

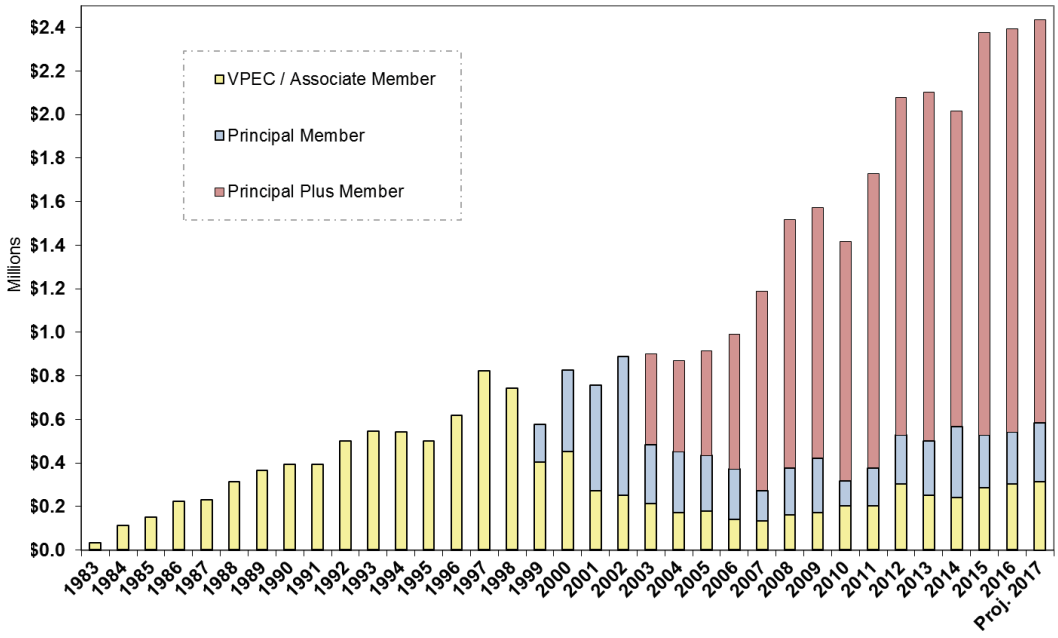
38
Countries with technical exchange

3
IEEE Fellows

CPES Membership Company Growth



Industry Membership Funding Growth



Overview

CPES Industry Consortium

The CPES industrial consortium is designed to cultivate connectivity among researchers in academia and industry, as well as create synergy within the network of industry members.

The CPES connection provides the competitive edge to industry members via:

- *Access to state-of-the-art facilities, faculty expertise, top-notch students*
- **$5M+** *Leveraged research funding of more than $5.0 million per year*
- *Industry influence via Industry Advisory Board*
- *Intellectual properties with early access for Principal Plus and Principal members via CPES IPPF (Intellectual Property Protection Fund)*
- *Technology transfer made possible via special access to the Center's multi-disciplinary team of researchers, and resulting publications, presentations, and intellectual properties*
- *Continuing education opportunities via professional short courses offered at a significant discount*
- *Option to send engineers to work with CPES researchers on campus via the Industry Residence Program*

The CPES industrial consortium offers the ideal forum for networking with leading-edge companies and top-notch researchers and provides the best mechanism to stay abreast of technological developments in power electronics.

MEMBERSHIP STRUCTURE

Principal Plus Members

Annual contribution - $50,000

Principal Plus Members gain tangible benefits via research collaboration with CPES as a member of one of the mini-consortia on focused research—PMC (Power Management Consortium), HDI (High Density Integration), or WBG-HPCS (Wide Bandgap High-Power Converters & Systems). Companies interested in more than one focused research areas may join another mini-consortium for an additional annual contribution of $50,000 each. In addition to all the benefits offered to Principal and Associate Members, Principal Plus Members have easy access to cutting-edge IPs via CPES IPPF (Intellectual Property Protection Fund).

Principal Members

Annual contribution - $30,000

Principal Members are well positioned to influence and guide CPES as Industry Advisory Board (IAB) members. Principal Members also have cutting-edge IP advantage via automatic IPPF (Intellectual Property Protection Fund), in addition to all the benefits offered to Associate Members.

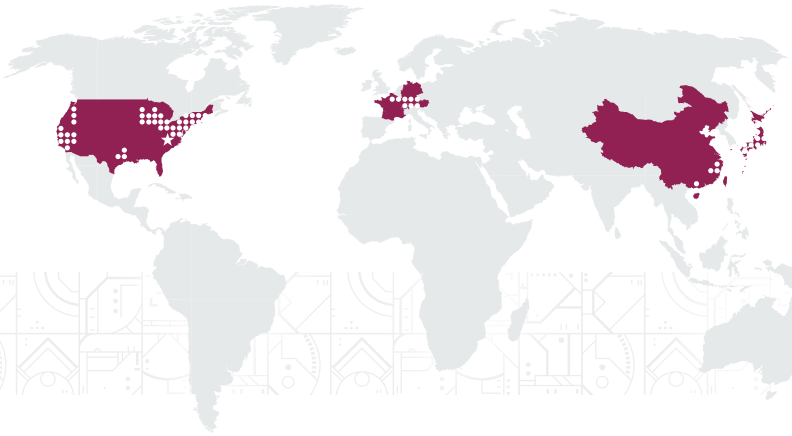
Associate Members

Annual contribution - $15,000

Associate Members gain the competitive edge, not only through easy access to CPES research results, researchers, and state-of-the-art facilities, but also opportunities for technical exchanges via the Industry Residence Program and continuing education via CPES short course to stay abreast of new technologies. Companies participating in the Industry Residence Program must be actively engaged in collaborative research with the Center in technical areas that are of mutual interest, to be determined jointly with CPES faculty host.

Affiliate Members make in-kind hardware/software donations to CPES equivalent to $10,000 per year. Their contributions must be relevant to CPES research. Membership participation at this level requires Center Director approval.

CPES



Industry members
February 2016–February 2017

Principal Plus Members

3M Company
ABB, Inc.
Alstom Transport
Altera – Enpirion Power
Chicony Power Technology Co., Ltd.
Crane Aerospace & Electronics
CRRC Zhuzhou Institute Co., Ltd.
Delta Electronics
Dialog Semiconductor
Dowa Metaltech Co., Ltd.
Eltek
Emerson Network Power/Vertiv
GE Global Research
GE Power Conversion, Inc.
General Motors
Groupe SAFRAN
Huawei Technologies Co., Ltd.
Infineon + International Rectifier
Integrated Device Technology, Inc.
Intel
Inventronics (Hangzhou), Inc.
Keysight Technologies
Linear Technology
Lockheed Martin Corporation
Murata Manufacturing Co., Ltd.
Navitas Semiconductor
NextEV
Nissan Motor Co., Ltd.
NXP Semiconductors
ON Semiconductor
Panasonic Corporation
Rockwell Automation
Silergy Corporation
Sonos, Inc.
Sumitomo Electric Industries, Ltd.
Texas Instruments
United Technologies Research Center

Principal Members

AcBel Polytech, Inc.
Fairchild Semiconductor Corporation
Flextronics
LG Electronics
Macroblock, Inc.
Mercedes-Benz R&D N. America
NR Electric Co., Ltd.
Siemens Corporate Technology
Toshiba Corporation
ZTE Corporation

Associate Members

Analog Devices
Calsonic Kansei Corporation
China Nat'l Elec. Apparatus Res. Inst.
Crown International
Cummins, Inc.
Dell
Dyson Technology Ltd.
Eaton Corporation, Innovation Center
Efficient Power Conversion
Ford Motor Company
Fuji Electric Co., Ltd.
Halliburton Energy Services, Inc.
Johnson Controls, Inc.
LiteOn Technology Corporation
Maxim Integrated Products
Microsoft Corporation
Richtek Technology Corporation
Robert Bosch GmbH
Shindengen Electric Mfg. Co., Ltd.
Tesla Motors
Toyota Motor Corporation
Toyota Motor Engineering & Manufacturing North America, Inc.
United Silicon Carbide, Inc.

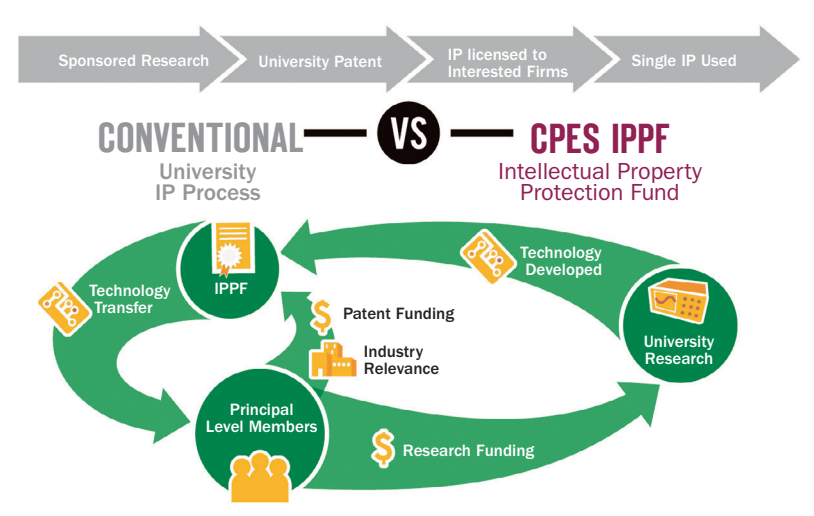
Affiliate Members

ANSYS, Inc.
CISSOID
DfR Solutions
EGSTON GmbH
Electronic Concepts, Inc.
Mentor Graphics Corporation
NEC TOKIN Corporation
OPAL-RT Technologies
Plexim GmbH
Powersim, Inc.
Rohde & Schwarz
Simplis Technologies, Inc.
Synopsys, Inc.
Taiyo Yuden Co., Ltd.
Tektronix, Inc.
Transphorm, Inc.
Vesta System
VPT, Inc.

Intellectual Property Protection Fund

IPPF is a unique IP access mechanism that provides extraordinary IP advantage to all Principal-level members. IPPF is available automatically, at no additional cost, to Principal Plus and Principal members. IPPF members meet quarterly with inventors to discuss invention disclosures and jointly decide which technologies to protect, with patenting costs covered by IPPF.

Once a technology is protected, IPPF members are granted a royalty-free, non-exclusive, non-transferable license to use the technology. IPPF is applicable only to technologies developed by CPES-VT researchers under the CPES industry consortium.




Industry
Academia
Government
CPES
Mini-Consortiums
WBG-HPCS
HDI
PMC

Mini-Consortium Program

The CPES mini-consortium program provides a unique forum for creating synergy among industries and defining new research directions to meet future industry needs. The formation of the mini-consortium allows CPES to pool resources and focus on developing precompetitive technologies to address common challenges, and sharing the research results among mini-consortium members.

Mini-consortium members are enrolled in CPES as Principal Plus Members, with annual contributions of $50,000. They gain tangible benefits via research collaboration with CPES as a member of one of the mini-consortia on focused research:

- **PMC** (Power Management Consortium)
- **HDI** (High Density Integration)
- **WBG-HPCS** (Wide Bandgap High-Power Converters and Systems)

Companies interested in more than one focused research area may join another mini-consortium for an additional annual contribution of $50,000 each.

Power Management Consortium (PMC)

In 1997, at the request of Intel, CPES established a VRM mini-consortium to address the issue of power management for future generations of microprocessors, targeting sub-1 volt and 100-200 amps current. As a result of this focused research, the CPES team developed a multi-phased voltage regulator module (VRM). Instead of paralleling power semiconductor devices to meet the current demand and efficiency requirements, the research team proposed to parallel a number of mini-converters. By paralleling the mini-converters and phaseshifting the clock signal, the team was able to both cancel the significant part of the output current ripple and increase the ripple frequency by N times, where N is the number of channels paralleled. This resulted in significant demonstrated improvement—specifically:

- 4 times improvement in transient response
- 10 times reduction in output filter inductors
- 6 times reduction in output capacitors
- 6 times improvement in power density

The new generation of Intel's microprocessor is operating at a much lower voltage and higher current, with a fast dynamic response in order to implement the sleep/power mode of operation. This mode of operation is necessary to conserve energy, and to extend the operation time for battery-operated equipment. The challenge for the voltage regulator module in this case is to provide a precisely regulated output with fast dynamic response in order to transfer energy as quickly as possible to the microprocessor. Today, every Intel processor is powered by such multiphased VRMs developed by CPES.

Power Management Consortium (PMC) is an outgrowth of the early VRM mini-consortium initiated in 1997. The goal is to extend its research scope with a focus on developing precompetitive technologies in the areas of power management for distributed power system architectures, EMI/EMC, power quality, ac-dc converters, dc-dc converters, POL converters in applications including microprocessors, tablets, notebooks, desktops, servers, data centers, networking products, telecom equipment, solid state lighting, battery chargers, transportation, renewable energy, and other industrial and consumer electronic applications.

The PMC mini-consortium has accumulated a wealth of knowledge and made significant contributions to the power management industry. Since its inception, the program has been supported by more than 30 major semiconductor and power supplies companies. PMC currently has 24 members. In the past year, seven new members joined the PMC: Dialog Semiconductors, Integrated Device Technology, Lockheed Martin, Navitas Semiconductor, NextEV, NXP Semiconductors, and Silergy Corporation.

The PMC places a significant emphasis on developing high-efficiency, high-power density switch-mode power supplies based on recent developments in wide bandgap (WBG) power devices such as Gallium Nitride (GaN) devices and Silicon Carbide (SiC) devices. This emphasis is highly leveraged with the recent DOE award of "PowerAmerica." CPES is a partner in this multi-industry, multi-university collaboration program for a period of five years. The CPES role is to work with the wide bandgap (WBG) manufacturing industry to explore potential applications and impacts of GaN and SiC devices to power conversion technologies.

Our WBG-based research will use several test beds to demonstrate the benefit of GaN-based power converters:

a. High frequency adapter with 40 W/in^3 power density and above 94% efficiency.

b. High frequency 1 kW single phase PFC with 700 W/in^3 power density and 99% efficiency.

c. High frequency 1 kW 400 V/12 V unregulated LLC converter with 900W/in^3 power density and 98% efficiency.

d. High frequency 3 kW 400 V/48 V isolated dc-dc converter with above 98% efficiency and 1000 W/in^3 power density.

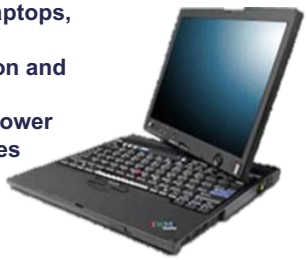
e. High frequency 48 V/1 V voltage regulator for server application with above 93% efficiency and 400 W/in^3 power density.

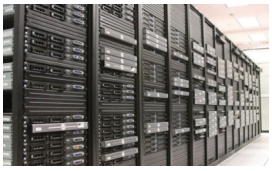
f. High frequency 6.6 kW bidirectional on-board charger (OBC) for plug-in electric vehicles (PEVs) with above 96% efficiency and 37 W/in^3 power density.

g. High frequency 25 kW battery charger with above 97% efficiency and 50 W/in^3 power density.

WORK SCOPE

- High performance VRM/POL converters
- High efficiency power architectures for laptops, desktops, and servers
- High frequency magnetics characterization and design
- High-efficiency and high-power density power supplies with wide bandgap power devices
- Digital control
- EMI
- Solid state lighting
- Power management for PV system
- Power management for battery system





PARTICIPANTS

PMC Members

3M Company
Altera – Enpirion Power
Chicony Power Technology Co., Ltd.
CRRC Zhuzhou Institute Co., Ltd.
Delta Electronics
Dialog Semiconductor
Eltek
Emerson Network Power/Vertiv
Huawei Technologies Co., Ltd.
Infineon + International Rectifier
Integrated Device Technology, Inc.
Intel
Inventronics (Hangzhou), Inc.
Linear Technology
Lockheed Martin Corporation
Murata Manufacturing Co., Ltd.
Navitas Semiconductor
NextEV
NXP Semiconductors
ON Semiconductor
Panasonic Corporation
Silergy Corporation
Sonos, Inc.
Texas Instruments

Research Team *February 2016 – February 2017*

Faculty

Fred C. Lee
Qiang Li

Graduate Students

Syed Bari
Chao Fei
Junjie Feng
Rimon Gadelrab
Dongbin Hou
Yi-Hsun (Eric) Hsieh
Xiucheng Huang
Zhengrong Huang
Bin Li
Chen Li
Virginia Li
Zhengyang Liu
Yadong Lyu
Ruiyang Qin
Yuchen Yang
Shishuo Zhao

Visiting Scholars

Weijing Du
Minfan Fu
Yan-Cun (Daniel) Li
Rong Xu
Biao Zhao

Leveraged with Government Funding from:

PowerAmerica
ARPA-E

High Density Integration (HDI)

HDI was created in 2011 as a mechanism for CPES and industry members to address emerging or long-term challenges in power electronic integration. While it is supported primarily by CPES memberships, it also leverages sponsored research with major industries such as ABB, Alstom, Boeing, GE, Group Safran, MKS, Nissan, Raytheon, Rolls-Royce, and Toyota, as well as with government agencies including the ARPA-E, NSF, DARPA, DOE, ONR, U.S. Army, and the U.S. Air Force. The tradeoffs among reliability, efficiency, cost, electromagnetic compatibility, power density, and speed are explored as new materials, components, circuits, and applications emerge.

The commercialization of wide-bandgap semiconductors as Silicon Carbide (SiC) and Gallium Nitride (GaN) has shifted switching frequency beyond tens of megahertz, power rating beyond megawatts, and junction temperature beyond 250° C. Ancillaries, characterization metrology, modeling method, packaging process, and manufacturing paradigm need to be transformed.

Unique high-temperature packaging technology is an example of CPES's fulfillment of these critical needs to the future powerelectronic industry. HDI has developed die-attach materials that can be processed at low temperatures, yet are reliable at the temperature of the wide-bandgap junction. Processes have been developed to encapsulate ultra-thin planar packages with polymer having high glass transition temperature and dielectric strength.

Magnetic materials with low core loss density have been synthesized from magnetic metals for additive manufacturing of high-frequency magnetic components. Inductors have been integrated into the converter package as a substrate to achieve power density approaching 1 kW/in^3. Over-molding magnetic materials have been synthesized for integrating energy storage and protection functions.

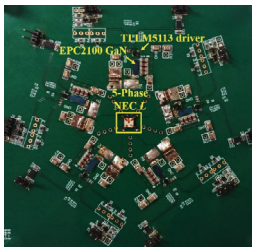
Techniques to decouple the noise loops have been identified to enable high dv/dt commutation in wide-bandgap environments. Design methodologies have been documented for high-temperature capacitors, power buses, protection, sensing, digital control, etc. New breeds of gate drivers, sensors, active filters, and passive filters have been demonstrated in a wide range of products, from power adapters to power-electronic building blocks. Significant improvement in power density, efficiency, and signal integrity are expected thanks to the adoption of the technological advances.

HDI tasks are scoped to advance wide bandgap systems, magnetic components, and module integration.

This current scope of work includes the following topics:

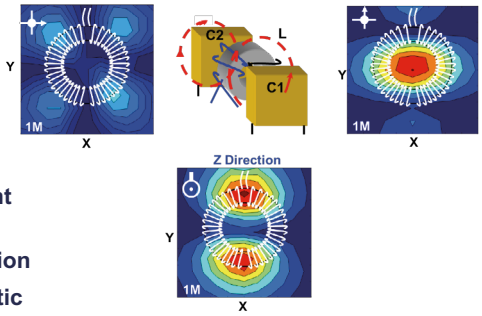
- **Wide Bandgap Systems**
  - Active dv/dt Control of 600 V GaN Switches
  - Characterization of Wide Bandgap Semiconductor switches up to highest voltage and temperature
  - High-Density Laptop Adaptor
  - Integrated Multi-Phase Voltage Regulators in Small Portables
- **Magnetic Components**
  - Additive Manufacturing of Magnetic Components
  - Magnetic Structures with High Energy Density
  - Over-Molding of Encapsulating Magnetics
  - Low-Profile Magnetic Substrate
  - Weakly Coupled Coils with Low Stray Field for Wireless Power
  - Integration of and Field Interaction in Common-Mode and Differential-Mode Filters
  - Integrated Multi-Phase Inductor for Voltage Regulator for Small Portables
  - PCB-Integrated Magnetics for High-Efficiency, High-Density Front-End Power Supply
  - Characterization of High-Power Inductors and Materials
- **Module Integration**
  - Reliability Measurement of Large-Area Sintered Silver Joints
  - Current Sensor Integrated with SiC MOSFET Module
  - High-Efficiency, Diode-Less 1.2 kV SiC MOSFET Half-Bridge Module
  - Integration of Magnetic Dice into Power Module

WORK SCOPE



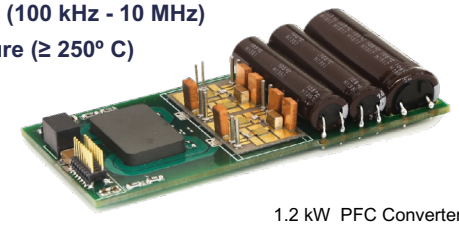
20 MHz 5-Phase Integrated Voltage Regulator

- Wide bandgap devices
- Material and component characterization
- Active module integration
- High frequency magnetic integration
- Converter integration
- Wide power range (10 W - 100 kW)
- High frequency (100 kHz - 10 MHz)
- High temperature (≥ 250° C)



Field Coupling among EMI Filter Components

Gate Driver for 3.3 kV 400 A Full SiC MOSFETs



1.2 kW PFC Converter

PARTICIPANTS

HDI Members

ABB, Inc.
Alstom Transport
Crane Aerospace & Electronics
Delta Electronics
Dowa Metaltech Co., Ltd.
GE Global Research
General Motors
Groupe SAFRAN
Huawei Technologies Co., Ltd.
Lockheed Martin Corporation
Nissan Motor Co., Ltd.
Sumitomo Electric Industries, Ltd.
Texas Instruments
United Technologies Research Center

Leveraged with Gifts from:

ABB, Inc.
LG Electronics

Leveraged with Government Funding from:

PowerAmerica
ONR
ARPA-E
DOE

Research Team *February 2016 – February 2017*

Faculty

Dushan Boroyevich
Rolando Burgos
Fred C. Lee
Qiang Li
Guo-Quan Lu
Khai Ngo

Research Faculty

Zhiyu Shen
Xuning Zhang

Graduate Students

Christina DiMarino
Shan Gao
Yingying Gui
Nidhi Haryani
Dongbin Hou
Xueyu (Sharon) Hou
Qian Li
Ming Lu
Alinaghi (Ali) Marzoughi
Zichen Miao
Sungjae Ohn
Bingyao Sun
Keyao Sun
Jun Wang
Qiong Wang
Kuangzhe Xu
Yi (Yasmine) Yan
Yue Xu
Yuchen Yang

Visiting Scholars

Yan-Cun (Daniel) Li

Wide Bandgap High-Power Converters & Systems (WBG-HPCS)

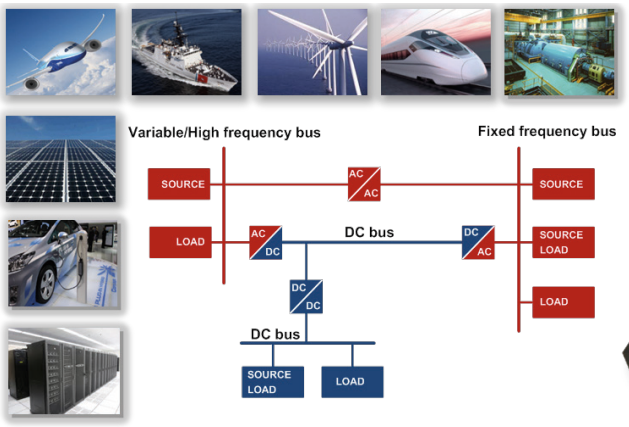
This CPES mini-consortium program provides a unique forum for creating synergy among the power industry and defining new research directions to meet future energy needs. The WBG-HPCS mini-consortium allows CPES to pool resources and focus on developing pre-competitive technologies to address common challenges, and sharing the research results among mini-consortium members. The main objective of the WBG-HPCS mini-consortium is to expand CPES's expertise in autonomous electric power systems (already established for transportation and IT) into the area of renewable energy integration and grid power electronics applications based on WBG power devices, while providing competitive research and education in that area.

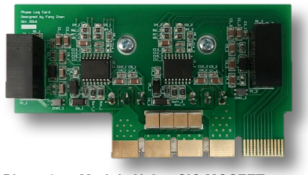
The current research directions of the WBG-HPCS mini-consortium comprise four different topics listed below with corresponding sub-topics. Additionally, a WBG-HPCS system testbed structure is planned to be designed and built in the near future for experimental validation purposes.

This current scope of work includes the following topics:

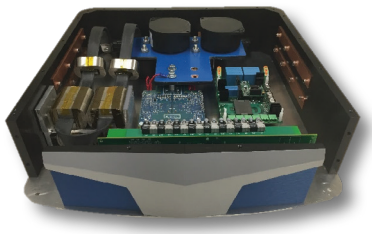
- **High-Power WBG-Based Power Converters**
  - Evaluation and design of Si-based and SiC impact on modular multilevel converters for MV drives
  - High frequency control of modular multilevel converters in ac-dc and dc-dc mode
  - Design of SiC-based modular multilevel converters with 1.7 kV, 3.3 kV, and 10 kV devices (package, gate-drive, PEBB, converter, system)
- **WBG-Based Power Electronics Technology**
  - Characterization of MV SiC devices
  - Design and evaluation of SiC-based SST
  - Design of high-efficiency SiC-based ECC-G2, single-phase to LVDC
  - Static and dynamic nonlinear droop control for LVDC distribution systems
- **Renewable Energy Integration**
  - Design of Si-based multilevel ECC for grid-tied applications (ac-dc + dc-dc)
  - Impact of PV inverters at distribution and transmission level
- **Stability and Dynamic Interactions in Power Converter Systems**
  - Virtual synchronous machine modeling and converter control for grid-tied inverters
  - SiC-based Impedance Measurement Unit (IMU); design and testing
  - Evaluation of dynamic interactions between multiple high-voltage STATCOM in the transmission system
  - Stability assessment and interactions of utility-scale PV inverters in medium-voltage distribution systems

WORK SCOPE

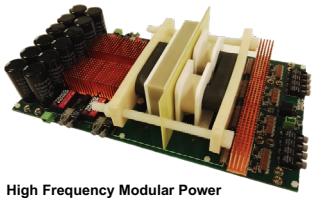




Phase-Leg Module Using SiC MOSFETs to Connect AC and DC Power Distribution Systems



100 kW, 1 kV SiC MOSFET based PEBB unit



High Frequency Modular Power Conversion from Medium Voltage AC to Low Voltage DC

- High-power WBG-based power converters
- WGB-based power electronics technology
- Renewable energy integration
- Stability and dynamic interactions in power converter systems

PARTICIPANTS

WBG-HPCS Members

ABB, Inc.
Delta Electronics
GE Power Conversion, Inc.
Huawei Technologies Co., Ltd.
Keysight Technologies
Rockwell Automation

Leveraged with Gifts from:

ABB, Inc.
United Technologies Research Center
PowerHub
Dominion

Leveraged with Government Funding from:

PowerAmerica
ONR

Research Team *February 2016 – February 2017*

Faculty

Dushan Boroyevich
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Fred C. Lee
Qiang Li

Research Faculty

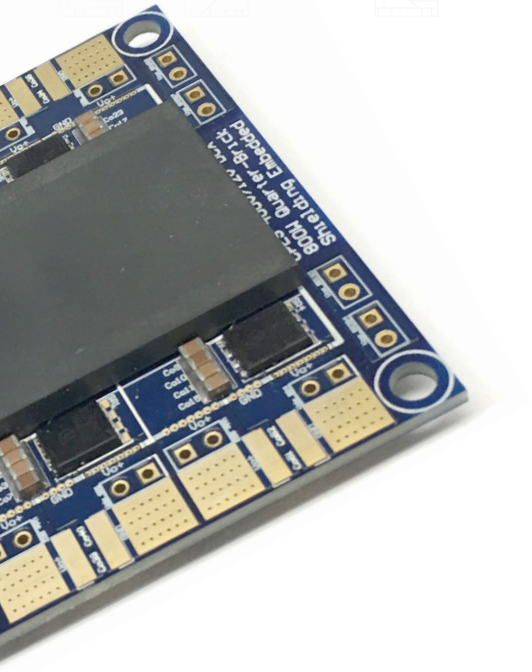
Igor Cvetkovic
Zhiyu Shen

Graduate Students

Fang Chen
Yi-Hsun (Eric) Hsieh
Zhengrong Huang
Chen Li
Chi Li
Yadong Lyu
Alinaghi (Ali) Marzoughi
Sungjae Ohn
Niloofar Rashidi Mehrabadi
Ye Tang
Jun Wang
Jianghui Yu
Shishuo Zhao

Visiting Scholars

Zeng Liu
Xiaolong Yue

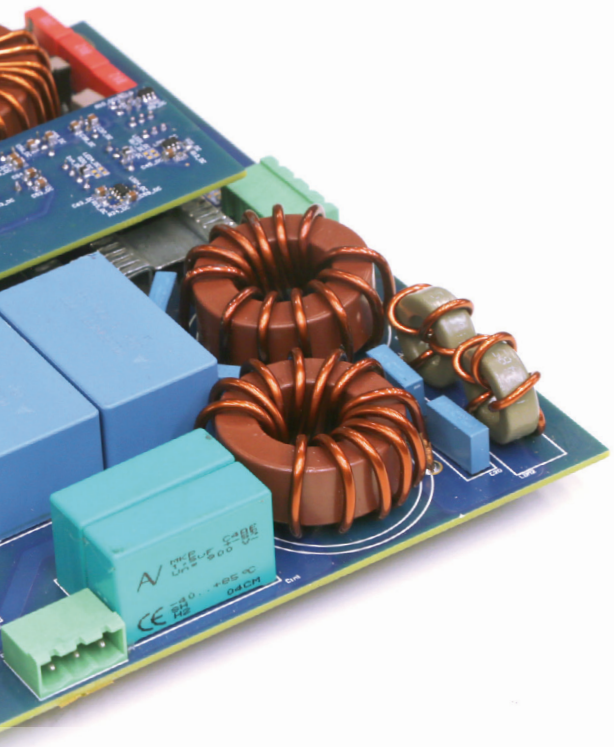


Research

In its effort to develop power processing systems to take electricity to the next step, CPES has cultivated research expertise encompassing five technology areas: (1) power conversion technologies and architectures; (2) power electronics components; (3) modeling and control; (4) EMI and power quality; and (5) high density integration.

These technology areas target applications that include: (1) power management for information and communications technology; (2) point-of-load conversion for power supplies; (3) vehicular power converter systems; and (4) high-power conversion systems.

In 2016, CPES sponsored research totaled approximately $2.4 million. The following abstracts provide a quick insight to the current research efforts.



Application Areas

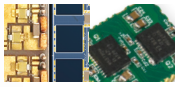
Power Management for Computers, Telecommunications, & Others

Vehicular Power Converter Systems

Point-of-Load Conversion

High-Power Conversion Systems

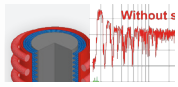
Technology Areas



Power Conversion Topologies & Architectures

Power Electronics Components

Modeling and Control



EMI and Power Quality

High Density Integration

Sponsored Research

Integrated GaN-based power supplies and active gate-drive control for 500 kHz, Three-Phase GaN-based Inverters

Sponsored by: SAFRAN

October 1, 2010 – September 30, 2016

The main objective of the latest phase of the industrial collaboration with SAFRAN (Phase V, 2015–2016), saw this project made use of the EMI modeling and filter design procedures developed in the past year to support the design of integrated power supplies for gate-drive and avionics applications operating in harsh environment in terms of dv/dt transients and also high temperature. Specifically, the project developed an integrated 2 W, dual-output gate-drive power supply for a half-bridge 650 V GaN HEMT phase-leg, featuring a PCB-embedded transformer, and GaN devices operating at 1–2 MHz to achieve a power density of 90 W/in^3, and a minimum input-output capacitance of 1.5 pF for maximum dv/dt immunity. It also developed an integrated 30 W, 28 V dual-output avionic power supply for wide-input-voltage range (10–80 V) applications, featuring a PCB-embedded transformer, and GaN devices operating at 1 MHz to achieve a maximum power conversion efficiency of 95%, and a minimum efficiency of 88% under light load conditions. Under a third throughst, the project developed a novel active gate-driver circuit to control the dv/dt voltage slew rate during the turn-on and turn-off transients of 650 V GaN e-HEMT devices, demonstrating a 6–12 dB attenuation in the EMI noise generated in the 10–30 MHz region. The concept was validated on a three-phase voltage-source inverter (VSI) operating at 500 kHz and 1 kW prototype constructed using the GaN devices in question and the active gate-driver.

Strategies for Wide Bandgap, Inexpensive Transistors for Controlling High Efficiency Systems (Switches)

Sponsored by: ARPA-E, ADEPT Program (Advanced Research Projects Agency Energy, Agile Delivery of Electrical Power Technology) Sub–Awardee of: HRL

March 6, 2014 – March 7, 2017

With the sponsorship of ARPA-E, CPES has partnered with HRL Laboratories to demonstrate ultra-high efficiency, low-cost power modules for future 1.2 kV, 100 A, vertical gallium-nitride (GaN) devices under development at HRL. These devices, expectedly capable of commutation speeds in the 100–200 V/ns range, will minimize switching losses to the extent where system efficiencies of >99% are expected at the power converter level.

In its first year, CPES has developed several ultra-low parasitic inductance package concepts using ribbon topside interconnections for the GaN devices and Flex PCB for the gate-terminals, with which it has reduced this parasitic component to less than 3 nH. Similarly, the module design has targeted the minimization of the parasitic capacitances to ground as an EMI containment strategy. Several prototypes of the power module using 1.2 kV, 90 A, SiC MOSFET devices were built and demonstrated to validate the module design. An advanced module concept utilizing ribbon bonding for the power terminals and a flex PCB for the gate-loop of the power module attained ultra-minimized parasitic components. During its second year the project developed a gate-driver unit for the corresponding power module, using an impedance-based channeling technique to divert the EMI noise generated from the sensitive control circuitry on the board, being capable of operating under harsh electromagnetic environments generated by the fast switching of these devices, typically in the 50–100 V/ns. The gate-drive was extensively tested and demonstrated with the module in continuous operation using a boost dc-dc converter configuration for this purpose. On its third year, the project has focused on the switching evaluation of the GaN vertical devices developed from HRL, which allowed CPES to demonstrate the switching of the first 800 V, 2 A vertical GaN FET in the world in December 2016.

Thermal-Electrical-Mechanical Modeling of IGBT Module Failure Modes

Sponsored by: Huazhong University of Science and Technology

August 8, 2014 – July 31, 2017

Insulated Gate Bipolar Transistors (IGBT) are one of the major players in modern power conversion, especially for medium and high power applications. The reliability of these devices remains to be a major concern, topic which Huazhong University of Science and Technology (HUST) has been studying jointly with Techsem Semiconductor Co., and now is interested in pursuing jointly with CPES. The primary goal of this research will be to investigate the possible failure modes of commercial IGBTs, including:

1. Module layout and its influence on the electric field and thermal distribution;
2. Wire bond structure and its impacts on the internal current distribution;
3. Direct Bond Copper (DBC) substrate preparation and its reliability;
4. Thermal interface material (TIM) selection and its influence on the module reliability;
5. Encapsulation of high voltage IGBT modules.

SiC-PEBB Modules for Next Generation MVDC Integrated Power Systems – Development of the SiC-Based PEBB 1000

Sponsored by: Office of Naval Research

August 1, 2014 – February 28, 2017

This project has developed 1 kV Silicon Carbide (SiC) based power electronics building block (PEBB) modules, named PEBB 1000. These SiC-PEBBs have truly enabled, for the first time, the notion of a high power density PEBB-only integrated power system for future Navy ships, profiting doubly from the system and commercial advantages featured by the PEBB modular concept, and from the power processing advantages offered by SiC semiconductors. As such, power density, efficiency, high control bandwidth, modularity, voltage and current scalability, reconfiguration flexibility, simplicity, and the potential for low-cost commercial off-the-shelf technology become a factual reality. For demonstration and evaluation purposes, two PEBB 1000 units have been developed by CPES to evaluate the performance of the PEBB in ac-dc, dc-ac and dc-dc applications. This will allow for a comprehensive assessment of the PEBBs, converters, and their system-level impact. In a parallel effort funded by ONR, GE Global Research has developed the PEBB 6000 unit using 10 kV SiC MOSFET power modules from Powerex, using CREE devices, which will enable the comprehensive evaluation of the SiC-PEBB integrated power systems for future Navy ships. The first PEBB 1000 prototype was fully tested in March 2016, and converter level tests are expected to follow soon thereafter.

High Power Solid State Circuits

Sponsored by: Office of Naval Research

Sub–Awardee of: ABB

May 1, 2015 – October 31, 2016

The main goal of the team at CPES, Virginia Tech, has been to develop a power converter concept with current limiting capability that can effectively withhold its stored energy during fault conditions. The converter has a modular structure being capable of scaling up its operation in both voltage and current by the series and parallel connection of its modules. At the system level, the main goal will be to demonstrate the current-limiting capability of the converter both under fault and overload conditions, demonstrating as well potential to expand the safe operating area of the system by sharing the limited load current among multiple power converters. Lastly, coordination aspects among power converters with current-limiting function and solid state circuit breakers will be investigated in order to formulate the system level circuit protection scheme. To this end, CPES has carried out in record time, the design, modeling, simulation, construction, and testing of the modular (PEBB-based) power converter concept rated at 1 kV dc, 45 kW. Accordingly, system level simulations were conducted to evaluate the current-limiting functionality both during faults and overload conditions, which have been fully verified experimentally under shortcircuit conditions. The converter, a unit based on the PEBB 1000 SiC module of three-phase modular configuration, was tested in both inverter and rectifier modes, demonstrating how under faults it could not only withhold its energy stored from feeding the fault event, but it could also control, limit, and extinguish the fault current in the dc bus, being capable of resuming normal operation and reinstating the regulation of the dc bus at 1 kV immediately after the clearing of the fault.

Developing the Future of Wide Bandgap Power Electronics Engineering Workforce – Wide Bandgap Generation (WBGen) Fellowship Program

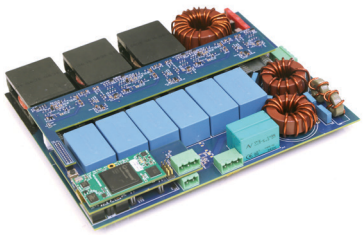
Sponsored by: Department of Energy

January 1, 2015 – July 31, 2021

The goals of the proposed project are first to train the next generation of U.S. citizen power engineers with WBG power semiconductor expertise, thus aiding in fulfilling the future workforce needs in this field; second, to broaden the range of WBG-based power electronics by conducting research and development on high-efficiency grid apparatus and high-efficiency electrical power systems; and third, to enhance the power engineering curriculum by formalizing WBG-oriented design procedures for power electronics components and systems that can effectively integrate the inherent, challenging material characteristics of these devices, which have effectively rendered design procedures for silicon (Si) based power electronics obsolete.

This project expects to graduate 10 MS students during its 5 years of execution, fund the first two years of 10 PhD students, and fund the first year of 5 additional MS and PhD students. In this period of time, 3–5 PhD students will expectedly graduate from Virginia Tech having passed through the proposed traineeship, and 5–10 more will do so in the following years. In all, a total of 45 graduate student assistantships will expectedly have been granted throughout the five years of the WBGen program. This will not only have an immense impact on the success of the WBG research programs at Virginia Tech, but will consequently spring immeasurably positive effect on the power engineering workforce over the next 5 to 10 years. Furthermore, the DOE and DOD laboratory and industrial partnership established in the traineeship will also benefit significantly from the interaction with the participating graduate students, cementing what are already strong relationships between the partners, CPES, and CPE, into a solid network of power engineering training, research, and development.

So far, four WBGen fellows have joined the program, establishing partnerships with ABB Inc., General Motors (GM), United Technologies Aerospace Systems (UTAS), HRL Laboratories, and the National Renewable Energy Laboratory (NREL).



SiC Inverter.

Modular Inverter

Sponsored by: United Technologies Aerospace Systems (UTAS)

March 1, 2016 – June 30, 2017

In this phase of the ongoing collaboration with UTAS, CPES has developed an extreme efficiency three-phase voltage source inverter in three-level T-type configuration using SiC devices, achieving an outstanding 99.4% for 5 kW high speed motor drive applications in aerospace electrical distribution systems. Meeting a specific form factor, and with a total loss budget of 30 W, CPES developed an optimization procedure to design the three-phase inverter in question. A first unit has

been demonstrated so far, which successfully passed its power quality and EMI qualification tests. A second inverter unit will be built in 2017 to demonstrate their parallel operation capability, which enables them to jointly drive a higher power electrical motor without requiring any communication between the inverter units or modules. This project follows the successful results obtained in the previous phase of the collaboration with UTAS where CPES developed a high efficiency (97.5%) ac-dc, two-stage power converter module with high-frequency galvanic isolation rated at 230 V ac, 28 V dc, and 1.25 kW, using a Vienna-type front-end ac-dc converter, and an LLC-type dc-dc converter.

Investigation of High Efficiency Single-Phase AFE Converter

Sponsored by: United Technologies Research Center

September 1, 2016 – April 30, 2017

The objective of this project is to demonstrate an ultra-high efficiency single-phase AFE converter for ACS applications utilizing state-of-the-art WBG power semiconductors, with a power rating of 8 kW. The converter design will consider the inclusion of input and output filters to comply with applicable harmonic and EMI standards, but the experimental testing of the EMI filters will be addressed during a prospective second phase of the project. The AFE converter will use an existent digital controller developed at CPES for testing purposes. Two converter concepts have been developed using SiC and GaN power semiconductors, demonstrating efficiencies in the 99.5% range.

Highly Integrated Wide Bandgap Power Module for Next Generation Plug-In Vehicles

Sponsored by: Department of Energy
Sub–Awardee of: General Motors Corporation

March 1, 2016 – February 16, 2018

The objective of the project is to research, develop, and demonstrate a highly integrated wide bandgap (WBG) power module targeting the next Generation plug-in vehicles. The power module proposed will be functionally and mechanically optimized for GM's traction inverter architecture. The resulted voltage source inverter will achieve or exceed DOE's specific power, power density, and cost targets of 14.1 kW/kg, 13.4 kW/L, and $3.3/kW, respectively, while operating more efficiently. A full scale power module will be completed.

Next Generation Electric Machines Program

Sponsored by: Department of Energy
Sub–Awardee of: General Electric Global Research

October 6, 2016 – December 30, 2018

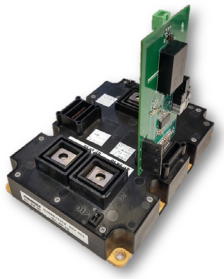
This project will conduct research to address the development of a medium voltage SiC-based motor drive with the GE GRC team. Virginia Tech will develop a technical approach and gate-driver circuit for the series connection of 1.7 kV SiC MOSFET devices. Comparative analysis of SiC switches using low voltage devises in a series versus high voltage devices will be completed. In its first year of execution, CPES has already developed a successful active-control mechanism to achieve the unrestricted series connection of SiC MOSFET power devices.

Electric Ship Research and Development Consortium

Through Florida State University (Lead) and Office of Naval Research

August 1, 2016 – July 31, 2017

CPES will continue supporting ONR's mission by participating as a member of the ESRDC, a multi-university consortium led by Florida State University. Within this framework CPES will work on the demonstration of PEBB 1000 based power converters and systems, for which it will develop an updated version of the PEBB 1000 unit built with 1.7 kV SiC MOSFET devices. It will continue working on the impedance measurement unit (IMU) previously developed for ONR using 10 kV SiC MOSFET devices, a multi-megawatt converter capable of operating from 4,160 V ac and 6,000 V dc networks, to measure the terminal impedances at interfaces of interest with the purpose of assessing the stability conditions of the electrical system. The main focus of this work will be to improve its electromagnetic compatibility (EMC), necessary to operate with the fast-switching 10 kV devices in place. Lastly, CPES will support the electric ship design, modeling, and simulation effort within ESRDC by integrating the modeling of power electronics systems taking into consideration parametric and model-form uncertainties into the process, with which improved and optimum designs will become feasible using the PEBB models developed.



10 kV Gate Driver.

Gate Driver for Gen3 10 kV, 240 A SiC MOSFET Power Modules

Sponsored by: Office of Naval Research

August 1, 2016 – July 31, 2017

The objective of this project is to design and test an integrated gate driver unit for Gen3 10 kV, 240 A SiC MOSFET power modules recently developed by CREE under ONR sponsorship. The gate driver unit will be capable of handling voltage slew rates of 100 V/ns, and will have an insulation capacity of 20 kV, featuring current-based short circuit protection, active Miller clamping, soft shutdown functionality, as well as under and overvoltage protection. To this end an integrated Rogowski current sensor will be adopted, which will provide a full current measurement capability for the module. The use of on-board FPGAs will provide the means for fast and expedient communication between the gate driver unit and its corresponding system controller.

Electromagnetic Interference (EMI) Mitigation and Containment in SiC-Based Modular UPS for Industrial Applications

Sponsored by: Department of Energy through PowerAmerica Institute

July 1, 2016 – June 30, 2017

ABB Corporate Research and the Center for Power Electronics Systems (CPES) at Virginia Tech will jointly pursue the efficiency and power density improvement of industrial UPS units. Within a broader scope, the ABB will adopt SiC MOSFET/Schottky barrier diode power module technology to replace existing Si IGBT solutions, while CPES will develop an EMI mitigation and containment strategy including the design of all EMI filters. Specifi-

cally, CPES has conducted a topology selection for the UPS module, which has resulted in a three-level back-to-back ac-ac converter configuration with an additional three-level dc-dc converter acting as battery charger. With the use of CPES-developed modulation and control schemes, the EMI emissions of the unit have been significantly reduced, effectively mitigating this type of interference. After concluding the initial design phase, CPES is currently testing the SiC-based hardware under construction using 1.2 kV three-level SiC modules in neutral-point-clamped (NPC) configuration. The full converter is expected to be tested in the summer of 2017. The specifications of the UPS module in question are: 100 kW, 480 V, 460 A, and 60 Hz.

Control of Modules of Parallel SiC Switching Cells

Sponsored by: Toyota Motor Engineering Manufacturing NA, Inc.

August 15, 2014 – March 31, 2016

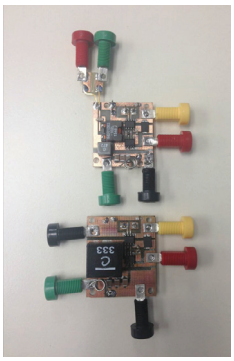
The objective of the project is to develop a gate driver/controller that would commutate a large number of paralleled SiC MOSFETs reliably, as well as balance the performance of the dies with respect to power or thermal distributions. Development of guiding principles for the design and fabrication of a power module of such paralleled MOSFETs will also be achieved.

Constant-Flux Magnetics for Power Conversion

Sponsored by: National Science Foundation

November 15, 2012 – April 30, 2016

At least 30% of the volume in commercial inductors store no or negligible energy. The "constant-flux" concept improves energy density by filling the available volume with as much magnetic (core) materials as practically feasible, then dispersing the windings to shape the distribution of magnetic flux, e.g., to distribute magnetic flux uniformly. In this project, guiding principles will be developed from the structural and field standpoints to realize the constant-flux concept. Performance metrics, such as inductances, capacitances, and quality factor will be modeled, quantified, and compared with the corresponding benchmarks.



Buck converter with tunable LLC filter.

Tunable Energy Efficient Electronics (TE3)

Sponsored by: DARPA

December 1, 2015 – November 30, 2018

In modern defense systems, the processing of electrical power to a suitable voltage level and frequency is a key factor in achieving high performance, light weight, improved reliability, and high efficiency. A majority of defense applications often require power processors to operate with a fluctuating source, load, or environment. Passive components with added tunability are sought to provide adaptability to different circuit conditions. They will add a major leap in size optimization, controllability and circuit design strategies. This project is going to design and make tunable power inductors, transformers, capacitors, and current sensors to reduce weight of power passives and increase power handling capacity. TE3-based dc-dc power converter system will be designed for achieving high power density and efficiency with adaptability to fluctuations in source, load, and environment.

Power Integration by Multifunctional Molding

Sponsored by: National Science Foundation

August 1, 2015 – July 31, 2017

Power modules are employed in electronic systems to lower part count, improve reliability, and reduce cost. The type of power module addressed herein comprises a complete dc-dc switched-mode converter in one package. Power switches, gate drivers, sensors, controllers, lead frames, and filter inductor are integrated into one building block that is encapsulated in molding compound. A 50 W module with efficiency exceeding 90% would fit into a volume of 1.5 x 1.8 x 0.6 cm^3.

While the filter inductor is known to be undesirably bulky, the unused space filled up by the molding compound might actually be larger than the inductor's volume. Power density would be improved significantly if the molding compound also stores energy so that, with appropriately designed winding, the module case also functions as the inductor. Such power integration by multifunctional molding has not been demonstrated so far because of two reasons. First, magnetic materials are usually kept away from a switching loop for fear that the increase in stray magnetic field would adversely affect a converter's operation. Second, an encapsulant with significant relative permeability (20–30) is difficult to synthesize using low temperature and low or no pressure.

The objective of the research is to integrate the energy-storage function into the encapsulating case of the power module, thereby reducing material usage and possibly simplifying the manufacturing process. Fundamental contributions are anticipated in materials and electrical engineering, education, and application. Encapsulation material that integrates mechanical/chemical (protective) and electrical (energy storage) functions is to be synthesized using low temperature and low pressure. Multi-magnetics modules (MMM) with unexplored electromagnetic properties and design methodology are to be devised to take advantage of such material. Operability of power-electronic converters are to be assessed the presence of magnetic media. Converter topologies are to be synthesized to leverage the field couplings inside an MMM. All fundamental advances are to culminate in a manufacturing process of multi-magnetics modules with less materials and cost, possibly.

Resonant Cross-Commutated Buck Converter

Sponsored by: Texas Instruments

Resonant current generated in one phase of two interleaved buck converters is injected into the switched node of the other phase to turn on the active switch at zero voltage over wide load range, and to turn off the synchronous switch at near-zero current at nominal load. This idea is applied to an interleaved two-phase buck converter with output voltage regulated by extended duty ratio. The rms current in the resonant inductors is kept below 0.4 I_o at half load by utilizing

resonance between L_r and C_r. The expectations were validated by a 2 MHz prototype with 12 V input, 3.3 V at 20 A output, and peak efficiency of 93.5%.

Modeling of Coupled Inductors with Plate Core

Sponsored by: Texas Instruments

The magnetic component is the most bulky part in the bias power supply module. Planar structures have been widely used in order to lower the profile and improve the power density. The plate-core coupled inductors consist of multilayer pcb windings sandwiched by two core plates which reduce the fabrication cost thanks to the simple structure. The inductors with winding layers sandwiched between two core plates are studied in this paper in order to model the magnetic field and self-inductance with finite core dimensions, very non-uniform flux patterns, and large fringing flux. The proportional-reluctance, equal-flux (PREF) model is developed to find the magnetic field by dividing the reluctance into several tubes that carry the same amount of flux. The methodology enables calculation of inductance, winding loss, coupling coefficient, and core loss. An improved equivalent circuit is developed from the modeling results to include the impact from current phase-shift and dynamic behavior. The model is verified by coupled-inductor prototypes.

Ocean Wave Energy Harvesting

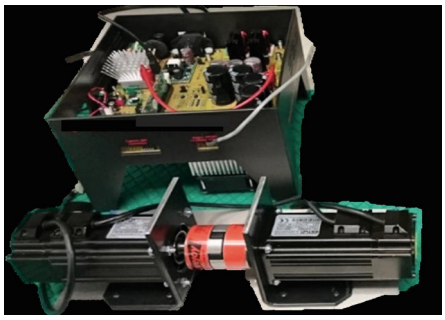
Sponsored by: Center for Innovative Technology Commonwealth Research Commercialization Fund (CIT CRCF) and in conjunction with the Center for Energy Harvesting Materials and Systems (CEHMS) at Virginia Tech

July 1, 2016 – June 30, 2017

Ocean wave energy potential in the US was 64% of the total electricity generated from all sources in 2010. Over 53% of the US population lives within 50 miles of a coast, so ocean waves offer exceptional opportunity. For wave energy generation equipment alone, the annual worldwide market is over $150B. However, ocean wave energy harvesting remains in relative infancy globally. One of the most important challenges is the power takeoff (PTO) mechanism, the machinery that converts kinetic energy of the waves into electricity.

The objective of this project is to develop and commercialize innovative ocean wave energy harvesting technology with high efficiency and reliability. We aim to solve the fundamental challenge of wave energy harvesting by converting irregular up-and-down motion of the ocean waves into unidirectional rotation of the electrical generator. Our solution integrates perfectly with the strict requirements of the power grid with a modular, isolated, bidirectional dc-dc converter and dc-ac power converter. Our multidisciplinary team has the required expertise in mechatronics, design, dynamics, control, and power electronics.

This proposal will develop an innovative power takeoff mechanism "mechanical motion rectifier" that is totally different from and superior to all existing wave power takeoff methods. By converting the irregular, oscillatory motion into regular, unidirectional rotation, our solution will solve the fundamental challenge of ocean wave energy harvesting. Wave energy is concentrated at low frequencies and low velocities, which makes efficient conversion extremely difficult and limits the options for efficient power takeoff technology (PTO). The power takeoff is the mechanism to convert the mechanical energy into electricity. In a major review article, Dr. O'Falcao states that the power takeoff mechanism "is possibly the single most important element in wave energy technology, and underlies many (possibly most) of the failures to date." Direct-drive linear PTOs that use linear electromagnetic generators require heavy, bulky permanent magnets; these systems have extremely low conversion efficiency in low speed reciprocating motion. Indirect-drive PTOs use hydraulic fluid as an intermediate step, which causes efficiency loss, system complexity, and low reliability. Our proposed PTO marries the advantages of direct- and indirect-drive PTO methods, with much higher energy conversion efficiency, enhanced reliability, and unmatched compactness.



Ocean wave pulse energy take-off (PETO).

Efficient and Reliable Power Takeoff for Ocean Wave Energy Harvesting

Sponsored by: Department of Energy and in conjunction with the Center for Energy Harvesting Materials and Systems (CEHMS) at Virginia Tech

March 1, 2016 – February 28, 2017

Our objective is to revolutionize ocean wave energy harvesting by designing, prototyping, and validating an innovative power takeoff (PTO) with a novel mechanical motion rectifier mechanism and unique power electronics to improve the energy conversion efficiency and thus the power output by 25% (Metric I) and reduce the failure rate by 50% (Metric II). Our PTO is based on a "mechanical motion rectifier" (MMR) that converts the irregular up-and-down (or back-and-forth) wave motions into unidirectional rotation of the electrical generator. Moreover, innovative power electronics, which we name "Pulsed Energy Takeoff (PETO)," will seamlessly integrate the PTO power and the grid. The proposed MMR based PTO is an entirely new concept that marries the advantages of direct- and indirect-drive PTO methods with much higher energy conversion efficiency, enhanced reliability, unmatched compactness, and elimination of hydraulic components.

We plan to achieve the 25% power output per unit cost through increase of the mechanical and electrical efficiency. By converting the oscillatory wave motion into unidirectional rotation of the generator using the "mechanical motion rectifier" and highly efficient ball screw, we can significantly reduce the impact force, efficiency loss, and bulk mass that appear in traditional PTO designs.

The proposed power electronics will collect more power than a passive power takeoff, yet permit the power electronics to be rated at a safe level consistent with the system's 25% improvement in power rating. Temperature rise at semiconductor junctions will be limited to a level consistent with the system's 50% improvement in failure rate. Note that while ac-dc converters are available commercially, an ac-dc converter will be designed and fabricated in the project to ensure flexibility in system integration.

Our goal will be validated through the design, modeling, optimization, and manufacturing of 20-100 kW PTO prototypes with active power electronics. After lab tests on the efficiency and accelerated-life failure rate, we will evaluate the system-level performance through ocean test in the Atlantic Ocean near Hampton Roads, VA. We expect a targeted system of 50 kW PTO will have a cost of $100k-$150k. Working at 50% capacity it annually produces 219,000 kWh of electricity, with cost recovery in 4-5 years.

High Density High Efficiency Adapter

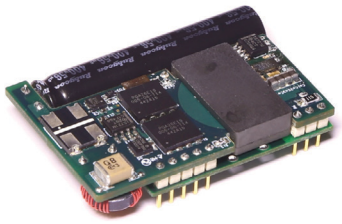
Sponsored by: Department of Energy through PowerAmerica Institute

February 1, 2015 – June 30, 2016

The adapter is highly driven by efficiency and power density for all forms of portable electronics. The adapter below 65 W power level is chosen for the demonstration for its potential economic impact, with wide range applications covering a large section of mobile devices, including tablet, notebook, and many other portable electronics equipment. Today, most of the adapters are only operating at relative low frequency (<100 kHz) with the state-of-the-art efficiency up to 91.5%. However, the low frequency operation limits the adapter power density at 6-11 W/in^3.

High efficiency and high frequency are the catalysts for size reduction. The emerging GaN device, with much improved figures of merit, opens the door for an operating frequency well into the MHz range. To realize the full benefits of GaN, a number of issues have to be addressed carefully, including soft- switching topology selection, high-frequency magnetics, control, packaging, gate drives, and thermal management. We have successfully demonstrated that the GaN-based adapter design is capable of operating at 1-2 MHz frequencies with an improved efficiency up to 94%. Subsequently, a power density of 25-30 W/in^3, which is a three-fold improvement over the state-of-the-art product, was successfully demonstrated at 45 W and 65 W levels. In this MHz adapter design, we have implemented a number of unique features:

- A flyback with active clamp circuit is applied to recycle the transformer leakage energy and, thus, realize soft-switching for the primary switches which brings over 90% reduction of switching losses. This enables the circuit to operate at 1-2 MHz while achieving high efficiency. The noise associated with high di/dt and dv/dt are also significantly reduced.
- 6-layer PCB based high-frequency transformer design to enable high power density.
- Common-mode noise is significantly reduced using the patented transformer shielding technique. The shielding provides more than 20 dB common-mode EMI reduction across the full frequency range (150 kHz~30 MHz), thus reducing the EMI filter to a single-stage filter.
- With the exception of the EMI filter and bulk energy storage capacitor, everything can be fully automated in the manufacturing process.



45 W adapter prototype.

High Frequency GaN Converters for Distributed Power Systems

Sponsored by: Department of Energy through PowerAmerica Institute

February 1, 2015 – June 30, 2016

The ever increasing demand for high-efficiency and high-density switch-mode ac-dc power supplies includes but is not limited to computers, telecommunication, data centers, electrical vehicle battery chargers, PV inverters, numerous industrials, and aerospace applications. Collectively, these products consume more than 10% of the total electric power. In the proposed effort, we will use high voltage GaN devices for the server power supplies to push its frequency 20 fold, from today's 50-100 kHz to 1-5 MHz. As a result, the power density of the frontend converter can be dramatically increased from today's 30-50 W/in^3 to 100-150 W/in^3. Furthermore, it is envisioned that the front-end power processing to be fully modularized. In this manner, a customized power system can be synthesized by using simple modular building blocks such as multi-phase power factor correction (PFCs), and high voltage dc-dc converters and dc-dc transformers (DCXs) for input/output isolation. These front-end converters are followed with already standardized multi-phase distributed Point-of-Load (POL) converters. In Year 1 of this program, we have successfully developed a 1 kW, 1-3 MHz critical mode PFC with 99% peak efficiency and more than 200 W/in^3 power density. A PCB integrated coupled-inductor has also been proposed for this PFC circuit to further improve its power density and achieve balance control on the circuit parameters to greatly reduce common mode EMI noise. For the dc-dc stage, we have developed a 1 kW, 1 MHz 400 V/12 V DCX with PCB winding based matrix transformer. It achieves 97% peak efficiency and 700 W/in^3 power density.

This high density DCX will be further improved to meet the specifications proposed by iNEMI for future dc datacenters with on-board 380 V/12 V modules. (Recently, the International Electronics Manufacturing Initiative (iNEMI) at the behest of IBM and other server manufacturers undertook a project to develop an industry standard for dc-dc converters. This converter is used to step down 380 V directly to 12 V and is placed directly on the motherboard). Compared to today's ac datacenter, the dc datacenter with an on-board 380 V/12 V module will bring at least 7% improvement in system efficiency.

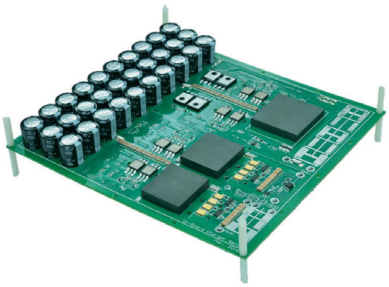
High Efficiency High Density GaN- Based 6.6 kW Bidirectional On-board Charger for Plug-in Electric Vehicles (PEVs)

Sponsored by: Department of Energy

Sub-Awardee of: Delta Products Corporation

October 1, 2014 –September 30, 2017

This project involves the development of a



6.6 kW On-board Battery Charger.

lightweight, compact and highly efficient bidirectional on-board charger (OBC) for plug-in electric vehicles (PEVs). PEV hereafter refers to plug-in hybrid electric vehicles (PHEV) and battery electric vehicles (BEV).

Due to the reverse recovery problem of Si semiconductors, a Si-based bidirectional OBC is typically implemented with two separate modules: a charger and an inverter. However, by adopting Wide bandgap semiconductors, including both Gallium Nitride (GaN) and silicon sarbide (SiC), one single converter is able to process power in both directions, resulting in a much smaller and lower cost system. In addition, due to the superior performance of wide bandgap semiconductors, the converter switching frequency can be pushed to as high as 500 kHz, reducing 30%~50% of the total system volume while in the meantime achieving 1%~2% efficiency improvement over its Si counterparts.

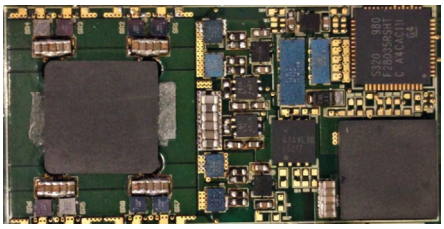
In this project, CPES developed a new two stage bidirectional on-board charger structure. The first stage is a two-phase interleaved PFC working at critical conduction mode with 300 kHz switching frequency per phase. All the fast switches can achieve zero voltage switching (ZVS), resulting in small switching loss. The second stage is a CLLC resonant converter featuring a symmetrical resonant tank. ZVS is also achieved and the switching frequency is pushed to 500 kHz. In order to deal with the wide battery voltage range, a variable dc-link voltage structure is proposed. By allowing the dc-link voltage to track the battery voltage, the gain range of the resonant converter is reduced significantly. Therefore, the switching frequency range is kept narrow and the best efficiency is maintained within the entire battery voltage range. In addition, all the magnetic components of the OBC is implemented using PCB winding, including transformer and inductor for the resonant converter and the coupled inductor for the PFC stage. As a result, manufacture automation and good parasitic control are achieved. A 6.6 kW two stage OBC prototype is demonstrated with 96% efficiency over the entire battery voltage range and 37 W/in^3 power density, both of which are far beyond the current industry practice.

Research of High-Efficiency High Density Power Conversion Architecture

Sponsored by: Huawei Technologies Co., Ltd.

August 19, 2015 – February 19, 2017

This project will develop a high frequency (>MHz) 48 V/1 V power module. A high efficiency, high power density power conversion was accomplished using a one stage quasi-parallel power architecture called a sigma converter. The proposed power delivery architecture shares the power between two converters connected in series from the input side and parallel connected from the output side, thus, rather than other well-established two stage solutions, higher efficiency is always obtained. In the proposed 48 V sigma converters, a high efficiency unregulated LLC converter operating as a dc-dc transformer (DCX) was used to deliver the majority of the power leaving smaller portions flowing through a less efficient buck converter for output voltage regulation purposes. With the aid of GaN devices and high performance magnetic materials, the LLC-DCX, operating at switching frequency of 1 mHz, was established using a PCB winding matrix transformer configuration integrating 4 transformers in one core structure. PCB winding inductors and GaN devices were used to build the buck converter responsible for output voltage regulation.



Sigma converter.

In the first year of this project we have successfully developed a (45-55 V)/1 V – 80 A sigma converter with power density of 420 W/in^3 and peak efficiency of 93.4%.

DC Data Center with High Frequency Isolation

Sponsored by: Department of Energy through PowerAmerica Institute

July 1, 2016 – June 30, 2017

The power required to support the computing infrastructure in large data centers can reach up to several tens of MW. However, less than half of this power is actually delivered to the computing load. The rest of the power is dissipated in power conversion, distribution, and cooling. Therefore, a more efficient power architecture and conversion are urgently needed.

With traditional ac data center power architecture, multi-megawatts power are taken from the high-voltage lines and converted to 480 V ac (line to line)/277 V ac (line to neutral) through a bulky 60 Hz transformer. A series connected UPS supply power to PDU (Power Distribution Unit). The 277 V ac output voltage is then stepped down to 208 V ac through a PDU 60 Hz transformer and distributed to the PSU (Power Supply Unit) cabinet level. These various stages of power conversion together are responsible for 21% loss of the total system power.

In this project, we propose to eliminate the 480 V ac power distribution bus. Instead, we will use high frequency solid-state transformers (SST), in a cascade configuration, to directly step down 4.16 kV ac to 380 V dc with single stage conversion. This configuration has a minimum power conversion stage and totally eliminates the bulky 60 Hz transformer. The proposed approach potentially can save up to 10% of the energy consumption in the data centers. Furthermore, the proposed power architecture is not only suitable for data centers, it also can be used for a broad range of applications, such as EV charge stations, energy storage systems, PV farms, and other micro-grids related applications.

Research of High-Efficiency High-Density 110 V/24 V Power Module

Sponsored by: CRRC Zhuzhou Institute Co., Ltd.

July 1, 2016 - August 30, 2017

The rail transportation systems, especially those new-generation high-speed rails, have great demands on high-efficiency high-density power modules. On these trains, the specific power module needs to provide a 24 V dc

output (maximum 8 A load) to power various IC chips. The input is a 110 V battery whose terminal voltage is roughly regulated, which can vary from 64 V to 160 V in practical applications.

A two stage solution, consisting of a buck converter followed by an LLC converter, is proposed for the target application to achieve 97% efficiency. The whole system will be controlled by a microcontroller and can fit into a quarter-brick footprint.

22 kw On-Board Bidirectional Battery Charger

Sponsored by: LG Electronics, China R&D Center

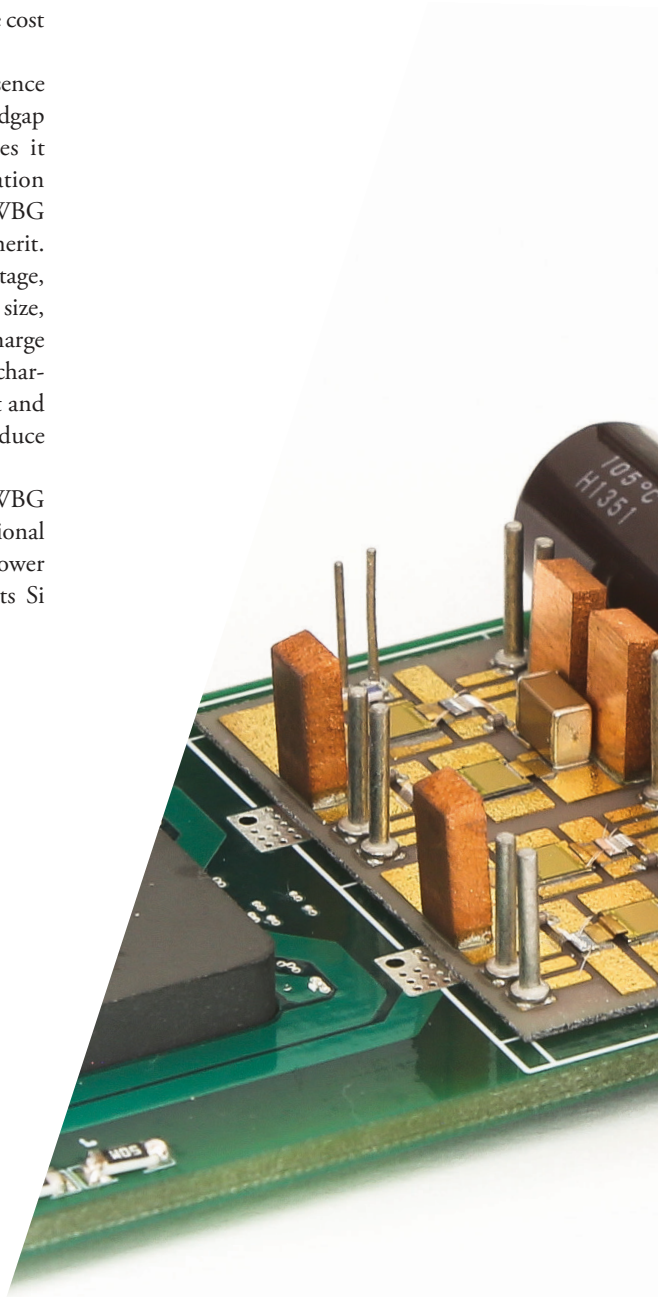
November 1, 2016 – October 31, 2017

Due to the concerns regarding the increasing fuel cost and air pollution, plug-in electric vehicles (PEV) or plug-in hybrid electric vehicles (PHEV) draw more and more attention. PEVs and PHEVs have rechargeable batteries that can be restored to full charge by plugging to an external electrical source. One crucial challenge of PEV's commercialization is the demand of a lightweight, compact, and efficient on-board charger system. The state-of-the-art on-board charger products are majorly Si-based, which operate at less than 100 kHz switching frequency, and haveonly 3~12 W/in^3 power density and at most 92~94% efficiency.

In addition, there's a growing demand for bidirectional power flow of on-board chargers so that the power in the battery can be used to support grid or standalone loads. However, for conventional Si based chargers, due to the severe reverse recovery charge of Si devices, a SiC Schottky diode instead of Si MOSFET needs to be used. As a result, reverse power flow becomes impossible. Usually, another separate converter is used to handle the discharging process. Apparently, this lowers down the power density and increases the cost of the whole system significantly.

Compared with Si devices, the absence of reverse recovery charge in wide bandgap (WBG) devices (GaN and SiC) makes it possible to achieve bidirectional operation with one single converter. In addition, WBG devices have a much better figure of merit. For a given resistance and breakdown voltage, WBG devices require a much smaller die size, which can translate into smaller gate charge and junction capacitance. Both of these characteristics are able to shorten the current and voltage transition interval and thus reduce switching loss.

The target of this project is to use WBG to develop a three phase 22 kW bidirectional battery charger with at least 3x the power density improvement compared with its Si based counterparts.



Intellectual Property

U.S. Patents Awarded

14-097
Two-Stage Multichannel LED Driver with CLL Resonant Circuit
By Xuebing Chen, Daocheng Huang, Qiang Li, Fred C. Lee
U.S. PATENT: 9,544,956
Issued: January 10, 2017

13-008
Electrical Power System Stability Optimization System
By Sheau-Wei Fu, Kamiar Karimi, Marko Jaksic, Bo Zhou, Bo Wen, Paolo Mattavelli, Dushan Boroyevich
U.S. PATENT: 9,471,731
Issued: October 18, 2016

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I^2 Average Current Mode (ACM) Control for Switching Power Converters
By Yingyi Yan, Fred C. Lee, Paolo Mattavelli
U.S. PATENT: 9,343,964
Issued: May 17, 2016

12-131
Optimal Trajectory Control for LLC Resonant Converter for Soft Start-Up
By Weiyi Feng, Fred C. Lee
U.S. PATENT: 9,318,946
Issued: April 19, 2016

12-152
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By Weiyi Feng, Fred C. Lee, Shu Ji
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Issued: March 1, 2016

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17-062 (Combine with 16-057)
12/6/2016
Resonant Topologies with Coupling and Load Independent Resonance for Wireless Power Transfer Applications
Junjie Feng, Minfan Fu, Qiang Li, Fred C. Lee
[Patent application sponsored by IPPF]

17-016
8/26/2016
Soft-Switching Techniques for Three-Phase AC/DC Converters
Zhengrong Huang, Zhengyang Liu, Fred C. Lee, Qiang Li, Furong Xiao
[Patent application sponsored by IPPF]

17-015
8/26/2016
A Novel Bi-Directional Two-Stage AC/DC Converter with Variable DC-link Voltage and Integrated PCB Winding Transformer for Wide Output Voltage Range Applications
Bin Li, Zhengyang Liu, Fred C. Lee, Qiang Li
[Patent application sponsored by IPPF]

16-115
4/12/2016
Multiphase Coupled and Integrated Inductors with PCB Winding for PFC Converters
Yuchen Yang, Mingkai Mu, Fred C. Lee, Qiang Li
[Patent application sponsored by IPPF]

16-110
4/8/2016
Method and Apparatus for Current/Power Balancing
Zichen Miao, Yincan Mao, Khai Ngo, Chi-Ming Wang
[Patent application sponsored by TEMA]

16-109
4/1/2016
Matrix Transformer and the Winding Structure
Chao Fei, Fred C. Lee, Qiang Li
[Patent application sponsored by IPPF]

16-094
2/24/2016
High-Frequency Circulating Current Injection Control for High-Speed Switch-Based MMC
Jun Wang, Rolando Burgos, Dushan Boroyevich
[Patent application sponsored by IPPF]

16-062
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Fang Chen, Rolando Burgos, Dushan Boroyevich
[Patent application sponsored by IPPF]

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Method and Apparatus to Improve Power Device Reliability
Yincan Mao, Zichen Miao, Khai Ngo, Chi-Ming Wang (TEMA)
[Patent application sponsored by TEMA]

16-057
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Junjie Feng, Qiang Li, Fred C. Lee
[Patent application sponsored by IPPF]

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[Patent application sponsored by TEMA]

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1/20/2016
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[Patent application sponsored by TEMA]

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9/15/2015
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Fang Chen, Rolando Burgos, Dushan Boroyevich
[Patent application sponsored by IPPF]

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Jongwon Shin, Khai Ngo
[Patent application sponsored by TEMA]

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7/27/2015
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Yadong Lyu, Fred C. Lee, Qiang Li
[Patent application sponsored by IPPF]

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7/13/2015
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Khai Ngo, Lujie Zhang, Zichen Miao
[Patent application sponsored by IPPF]

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[Patent application sponsored by IPPF]

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2/2/2015
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Fred C. Lee, Xiucheng Huang, Qiang Li
[Patent application sponsored by IPPF]

15-068
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Xiucheng Huang, Fred C. Lee, Qiang Li
[Patent application sponsored by IPPF]

15-067
1/26/2015
New Current Mode Control Based on Charge Control Concept
Syed Bari, Fred C. Lee, Qiang Li
[Patent application sponsored by IPPF]

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Virginia Li, Pei-Hsin Liu, Qiang Li, Fred C. Lee
[Patent application sponsored by IPPF]

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Optimal Battery Current Waveform for Bidirectional PHEV Battery Charger
Lingxiao Xue, Paolo Mattavelli, Dushan Boroyevich
[Patent application sponsored by IPPF]

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Mingkai Mu, Sizhao Lu, Yang Jiao, Fred C. Lee
[Patent application sponsored by IPPF]

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Yipeng Su, Dongbin Hou, Fred C. Lee, Qiang Li
[Patent application sponsored by IPPF; CIP to 13-169]

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Syed Bari, Fred C. Lee, Qiang Li, Pei-Hsin Liu
[Patent application sponsored by IPPF]

14-075
1/6/2014
Compact Inductor Employing Redistributed Magnetic Flux
Khai Ngo, Han Cui
[Patent application sponsored by IPPF]

14-066
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Pei-Hsin Liu, Fred C. Lee, Qiang Li
[Patent application sponsored by IPPF]

14-065
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Xiucheng Huang, Weijing Du, Qiang Li, Fred C. Lee
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14-053 (includes 14-147)
10/16/2013
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Jun Wang, Rolando Burgos, Dushan Boroyevich, Bo Wen
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Yipeng Su, Qiang Li, Fred C. Lee, Wenli Zhang
[Patent application sponsored by IPPF]

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Zhiyu Shen, Marko Jaksic, Paolo Mattavelli, Dushan Boroyevich, Jacob Verhulst, Mohamed Belkhayat
[Patent application sponsored by NNS]

13-166
6/13/2013
System and Method for Impedance Measurement Using Series and Shunt Injection
Zhiyu Shen, Marko Jaksic, Paolo Mattavelli, Dushan Boroyevich, Jacob Verhulst, Mohamed Belkhayat
[Patent application sponsored by NNS]

13-085
1/4/13
V^2 Control with Capacitor Current Ramp Compensation using Self-Calibrated Lossless Capacitor Current Sensing
Yingyi Yan, Pei-Hsin Liu, Fred C. Lee
[Patent application sponsored by IPPF]

13-032
9/12/12
Transformer Shielding Technique for Common-Mode Noise Reduction in Isolated Converters
Yuchen Yang, Daocheng Huang, Qiang Li, Fred C. Lee
[Patent application sponsored by IPPF]

12-130
5/18/12
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Pei-Hsin Liu, Fred C. Lee, Yingyi Yan, Paolo Mattavelli
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12-122
4/23/12
Common input voltage control and output power maximum power point tracking (MPPT) for Sub-panel converters with series outputs
Xinke Wu, Zijian Wang, Fred C. Lee, Feng Wang
[Patent application sponsored by IPPF]

12-044
10/7/11
Energy Storage for PFC by EV Motor/Generator
Khai Ngo, Hui Wang
[Patent application sponsored by IPPF]

12-024
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Dong Dong, Dushan Boroyevich, Paolo Mattavelli
[Patent application sponsored by IPPF]

Invention Disclosures

17-072
1/10/2017
Embedded Screen for Containing Common-Mode Current within a Power Module
Christina DiMarino, Mark Johnson, Dushan Boroyevich, Rolando Burgos

17-062
12/6/2016
Resonant Topologies with Coupling and Load Independent Resonance for Wireless Power Transfer Applications
Junjie Feng, Minfan Fu, Qiang Li, Fred C. Lee

17-059
11/21/2016
Cooler with EMI-Limiting Inductor
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17-016
8/26/2016
Soft-Switching Techniques for Three-Phase AC/DC Converters
Zhengrong Huang, Zhengyang Liu, Fred C. Lee, Qiang Li, Furong Xiao

17-015
8/26/2016
A Novel Bi-Directional Two-Stage AC/DC Converter with Variable DC-link Voltage and Integrated PCB Winding Transformer for Wide Output Voltage Range Applications
Bin Li, Zhengyang Liu, Fred C. Lee, Qiang Li

17-004
7/11/2016
Cooler with EMI-Limiting Inductor
Khai Ngo, Han Cui, Chi-Ming Wang (TEMA)

17-001
7/5/2016
Method of Increasing AC/DC Voltage Gain of Three-Phase Critical Conduction Mode Converter
Qiong Wang, Xuning Zhang, Zhiyu Shen, Rolando Burgos

16-115
4/12/2016
Multiphase Coupled and Integrated Inductors with PCB Winding for PFC Converters
Yuchen Yang, Mingkai Mu, Fred C. Lee, Qiang Li

16-110
4/8/2016
Forced Unbalanced Method to Reduce Transient Current Unbalance in Semiconductor Power Switches
Zichen Miao, Yincan Mao, Khai Ngo, Chi-Ming Wang (TEMA)

16-109
4/1/2016
Matrix Transformer and the Winding Structure
Chao Fei, Fred C. Lee, Qiang Li

16-108
3/29/2016
Design of Modular Multilevel Converter in AFE Mode with Minimized Passive Elements Installed
Alinaghi Marzoughi, Rolando Burgos, Dushan Boroyevich

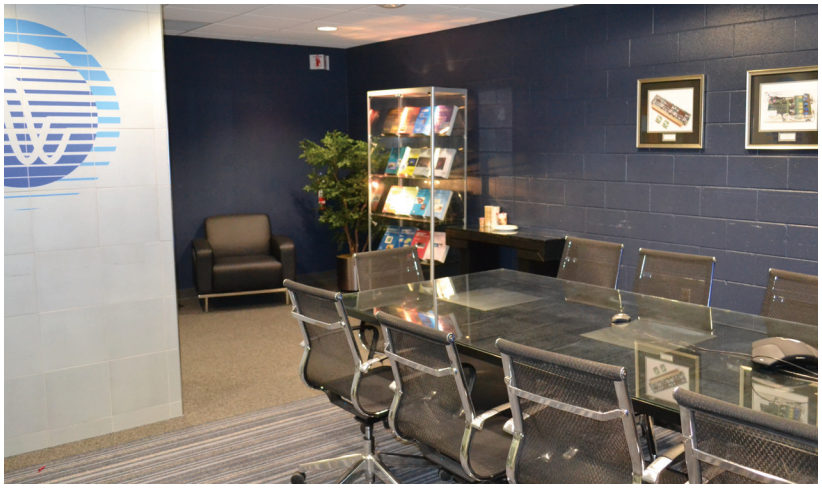
16-107
3/29/2016
Capacitor Voltage Ripple Minimization in Modular Multilevel Converter Based on Average Model Theory
Alinaghi Marzoughi, Rolando Burgos, Dushan Boroyevich

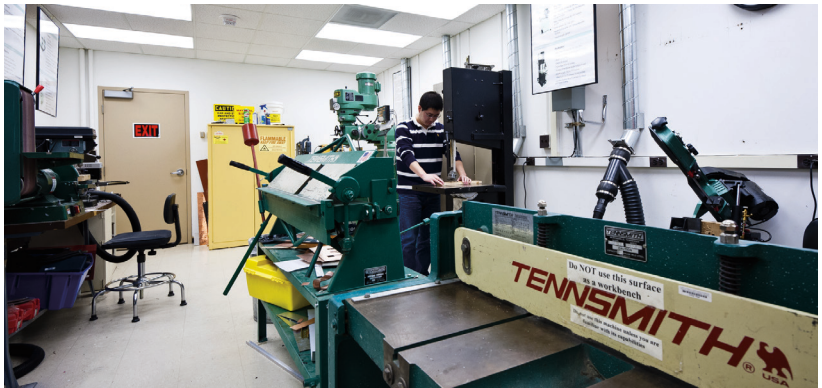
16-094
2/24/2016
High-Frequency Circulating Current Injection Control for High-Speed Switch-Based MMC
Jun Wang, Rolando Burgos, Dushan Boroyevich

Virginia Tech Facilities

Introduction

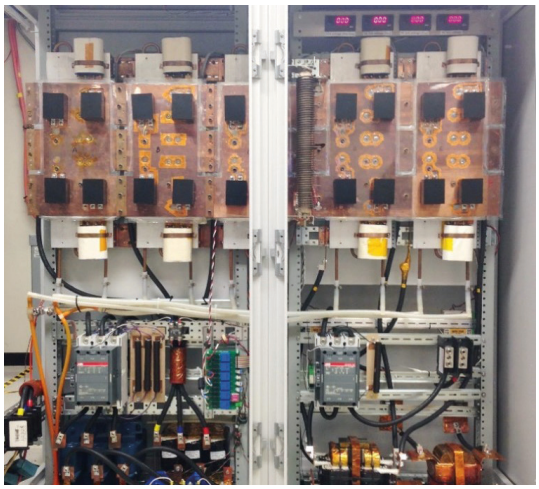
The Center headquarters are located at Virginia Tech, occupying office and lab facilities encompassing more than 20,000 sq ft of space in one building. Research space at CPES-VT includes an electrical research lab, an integrated packaging lab, and computer lab. In addition to the headquarters labs and offices, a research library, and a large conference room with voice and video conferencing capabilities supporting remote site course instruction as well as interaction among CPES collaborators are maintained. Interactive collaboration is routinely facilitated through conference calls, WebEx online conferencing, student and faculty exchanges, and face-to-face research project review meetings.

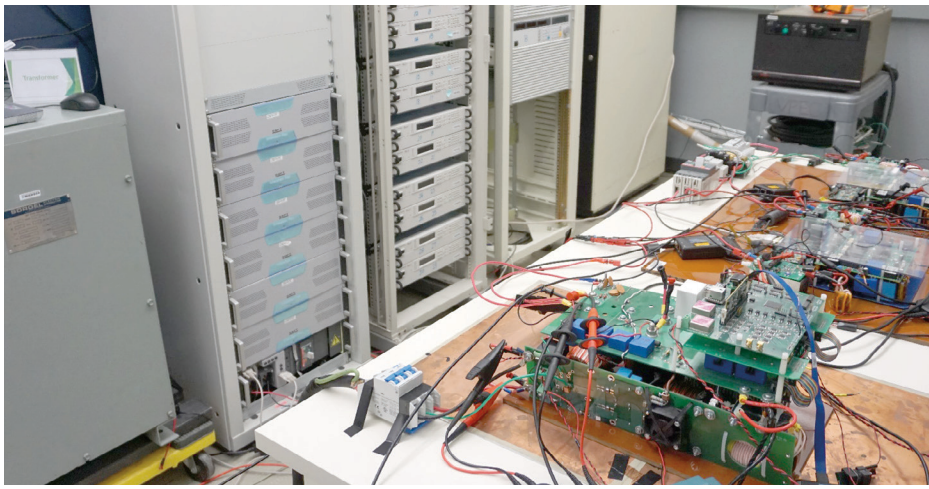




Electrical Research Laboratory

The electrical research laboratory is equipped with state-of-the-art tools and equipment for development of power electronic circuits and systems of all sizes from sub-volts, sub-watts to 6 kV, 1 MW. It also includes PWB manufacturing equipment, an EMI chamber, a clean room and a mechanical shop. New this year is a state-of-the-art curve tracer that is capable of characterizing up to 10 kV and 1500 A. Each student bench is equipped with Dell computers with an i7 core and up to 16 GB of RAM for running complex simulations. Standard instrumentation includes: GHz oscilloscopes, multi-channel function generators, electronic loads, network, spectrum, impedance, logic, and power analyzers, thermal sensors, and ac-dc bench supplies of all sizes. Specialized test room equipment includes: thermal imaging, thermal cycling chambers, Hi-Pot tester, 3D magnetic field scanner, EMI/EMC analyzer, large and small dynamometers, automatic circuit board routing equipment, magnetic core loss testing, programmable and variable loads, and liquid cooled heat-exchanger.





Integrated Packaging Lab

The Integrated Packaging (IP) Lab supports all CPES students, faculty, visiting scholars, and sponsors for their advanced needs in power electronics packaging research. The lab was established to create and evaluate alternative approaches to the design and manufacture of Integrated Power Electronics Modules (IPEMs) and provide the state-of-the-art electronic manufacturing and assembly equipment. The IP lab itself has installed a sealed ceiling and HEPA filtration to create over 1,600 square feet of class 10,000 cleanroom space, and the addition of a dark room for photolithography processing. It has the capability to produce FR4, DBC, and thick film hybrid substrates, perform metallization using RF sputtering thin film deposition and electro/electro-less plating, and develop substrate patterns by virtue of laser ablation machining, chemical metal etching, and screen printing. The IP lab also has the ability to mount bare dies and SMT components using high precision pick-n-place machine, solder reflow belt furnace, and convection reflow oven. The advanced vacuum solder reflow system provides another technical solution for die-attachment in a flux-less, void-less process. The wire bonding machines equipped in the IP lab provide interconnect options of heavy aluminum wire bonding, gold wire ball bonding, and aluminum/gold ribbon bonding for manufacturing IPEMs. For accurate and controlled dispensing of adhesives and encapuslants, an automated precision dispensing system and a spin coater have been added in the lab. In addition, the IP lab has the full capability for low temperature co-fired ceramic (LTCC) processing from tape cutting, via drilling, screen printing, laminating, to co-firing. The components and module-level test and evaluation of electrical, thermal, and reliability performance for the assembled IPEMs are also available in the IP lab. Low and high power curve tracers, impedance analyzers, and precision multimeters can be used for electrical property measurements. Thermal performance evaluation can be made by the setup of thermocouples, optic-fiber sensors, IR imaging, and the thermal diffusivity test system. Reliability analysis is performed using multi-purpose bond tester on as-made modules and ones after certain numbers of temperature/humidity cycling. An array of cross-sectioning and grinding/polishing equipment has been used to better understand the microstructure of electronic packaging materials.

High Power Lab

High power, high voltage power conversion technologies are attracting increasing attention in academia as well as industry in response to a need for more emerging power electronics applications, including alternative energy and power conversion such as wind power generations, fuel cells, hybrid electric vehicles and all-electric ships. Enabled by a 2002 award of $839,337 from the Defense University Research Instrumentation Program (DURIP) paired with CPES cost sharing of more than $250,000 for renovations, the electrical research lab area at Virginia Tech has been renovated and upfitted to accommodate medium voltage, megawatts power capability. The facility has two medium voltage 1 MVA reconfigurable transformers, corresponding reactors, capacitors, switchgears, and controllers. A 1 MW Innovation Series medium voltage IGBT drive donated by GE is installed as a programmable load. The complete set-up is capable of testing power converters in various active and reactive operation modes continuously at 1 MVA, 4160 V level. The unique installation distinguishes Virginia Tech as one of a few select universities in the nation with this capability and enhances its position as a leader in power electronics research well beyond the NSF ERC life expectancy.

Library and Computer Lab

The computer lab supports all major software used in power electronics design including: SPICE, Saber, Simplis, Code Composer, Math products – Matlab and Mathcad, Ansys Products – Workbench and Mechanical, Ansys Electromagnetics – Maxwell, Electronics Desktop (Q3D, HFSS), Simplorer, SIWave, Mentor Graphics Flowtherm, PLECS, and Altium Designer.

Spotlight on Alumni

Francisco Canales Abarca

Affiliation:
ABB Switzerland Ltd., Corporate Research

Position title:
Corporate Research Fellow

Last degree from Virginia Tech:
PhD, EE

Year Graduated:
2002

CAREER HIGHLIGHTS

2002-2005	Associate Professor with the Department of electronic Engineering, CENIDET, México. Advisor of 4 Ph.D. dissertation and 10 M.S. in the area of power electronics and control
2005-2016	Several scientific positions at ABB Corporate Research. Named Corporate Research Fellow in 2011 for the search, evaluation and identification of key technologies and trends in the area of Power Electronics which allows ABB to be in the forefront of technological development.

QUOTE

During my studies, I learned the concept of thorough research which I have been able to apply throughout my professional career in academia and industry.

Bo H. Cho

Affiliation:
Seoul National University, Seoul Korea

Position title:
Professor

Last degree from Virginia Tech:
Ph.D

Year Graduated:
1985

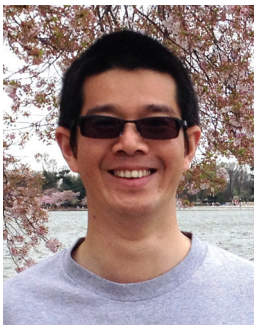
CAREER HIGHLIGHTS

1985-1995	Assistant, Associate Professor, Electrical Engineering Dept., Virginia Tech
1989	Presidential Young Investigator Award
1995-present	Professor, Seoul National University, Seoul Korea
1997-2005	Director, Power Electronics Center, Korea electrical Engineering and Science research Institute
1997-1998	Chairman, Korea Multi-purpose Satellite Development Program Advisory Committee, Korea Science and Technology Policy Institute
2000-present	Full Member, National Academy of Engineering Korea
2002-2003	Vice President, Samsung SDI PDP Division
2003-2007	Editor-in-Chief, Journal of Power Electronics, Korea Institute of Power Electronics
2004-2008	Chairman, International Relation Committee, National Academy of Engineering Korea
2005-2007	President, Korea Institute of Power Electronics
2006	General Chairman, PESC06
2007-2010	Distinguished Lecturer, IEEE PELS
2009-2011	Director, Institute of Engineering Research, Seoul National University
2009-2012	Outside Director, Iljin Electric
2010-2017	POSCO Chair Professor
2014-2017	Director, Electric Power Research Institute Seoul National University

QUOTE

I first met Dr. Lee in 1981 when I was working for TRW Space Power Group in Redondo Beach, CA after my MS degree at CalTech. Dr. Lee recruited me offering a tenure track faculty (instructor) position and I decided to join his group. My VPEC/CPES experiences have been a tremendous asset for my career growth.

Weiyi Feng



Affiliation:
Ningbo Weie Electronics Technology Co., Ltd.
Position title:
Cofounder & CTO
Last degree from Virginia Tech:
PhD
Year Graduated:
2013

CAREER HIGHLIGHTS

2013-2015 Senior Research Engineer in Delta Electronics in Shanghai
2015-present Cofounder & CTO in Weie Technology

QUOTE

Even now, after several years graduated from CPES, Dr. Lee's research methodology regulates my work in my daily life. CPES alumni around the world give me a lot of help in my work. It's my honor to study in CPES with so many talents.

Alex Q. Huang

Affiliation:
NC State University
Position title:
Progress Energy Distinguished Professor
Last degree from Virginia Tech:
Ph.D.
Affiliation at VPEC/CPES:
Assistant/Associate/Full Professor (1994-2004)

CAREER HIGHLIGHTS

1986 M.S. Thesis on IGBT, the first IGBT device ever made in China.
1992 Ph.D. from Cambridge University UK. One of the first in developing CMOS compatible high voltage integrated circuit
1994 Joined VPEC/CPES as an assistant professor
1997 Invention of the emitter turn-off (ETO) thyristor as a major innovation to improve the dynamic performance of the GTO thyristor. The work received the 2003 R&D 100 award. Received US patents US 6,933,541, 6,710,639
1999 Graduated the 1st Ph.D. student at CPES
2004 Became Alcoa Professor at NC State University, established the Semiconductor Power Electronics Center (SPEC) at NC State
2005 Became an IEEE Fellow for contribution in the developing the ETO thyristor
2007 Name the Progress Energy Distinguished Professor of Electrical Engineering.
2008 Established the FREEDM Systems Center, the second NSF ERC ever established in the US related to power electronics technology. Today the center has become one of the largest centers in power electronics systems.
2008 Established the Advanced Transportation Energy Center (ATEC) at NC State
2011 MIT Technology Magazine names Dr. Huang's work on Solid State Transformer (SST) one of the ten technologies of the year
2014 Lead PI of the Next Generation Power Electronics Manufacturing Innovation Institute (now called PowerAmerica). President Obama made the announcement at NCSU in 2014. This is a historical moment for power electronics community.
2015 Graduated the 50th Ph.D. student at FREEDM/NCSU

QUOTE

VPEC/CPES is where I developed and expanded my research interest beyond my original training in solid state power devices. I have been able to model after the well organized industry program at CPES, contributing to the success in establishing FREEDM and PowerAmerica. My friendship and interactions with CPES faculty have been a lasting source of inspiration.

Spotlight on Alumni

Kwang-Hwa Liu

Affiliation:
Gemi Semiconductor
Position title:
CEO
Last degree
from Virginia Tech:
Ph.D.
Year Graduated:
1986

CAREER HIGHLIGHTS

1986-1989	ITT Power Systems, Tucson, Arizona
1989-1991	Delta Power Electronics Lab., Blacksburg, Virginia
1991-1993	Momenta Computer, Mountain View, California
1994-1996	Siliconix, Santa Clara, California
1996-1998	O2Micron, Santa Clara, California
1999-2001	Semtech, Thousand Oaks, California
2001-2004	Arques Tech, Santa Clara, California
2004-2005	Amazion Tech., Taipei, Taiwan, RoC
2006-2014	GreenMark Inc., Taipei, Taiwan, RoC
2015-present	Gemi Semiconductor, Taipei, Taiwan, RoC

QUOTE

After working in the power electronics and power IC industry for 30 years, I can more appreciate my years of research in VPES under Dr. Lee.

In my opinion, power electronics is the ideal sub-field in electronics of new generation of electronics engineers. As of now, digital electronics and digital IC design have pretty much matured and become stagnant in new technology. Most of other analog circuit and design technology also have matured, there are only small improvement and evolution here and there.

In comparison, the power electronics technology, due to the demand of higher performance, higher power, higher efficiency applications, such as in electric vehicles and robotics, remains vivid, challenging, and fun to work on.

Also, an M.S. or a Ph. D. degree in power electronics means you have sufficient knowledge and training in a wide range of fields, such as: analog circuits, magnetics, control theories, feedback amplifier and compensation design, high voltage devices and circuits. Hence, it is easier to start as a power electronics engineer and enter other fields such as power IC design, analog IC design, control system design, or robotics design, in case your interest shifts, or your work assignment changes.

Anyway, keep a learning spirit and curious mind. Be flexible and remember the Chinese saying, “review the old, discover the new”.

Hengchun Mao

Affiliation:
NuVolta Technologies, Inc.
Position title:
CTO
Last degree
from Virginia Tech:
Ph.D.
Year Graduated:
1996

CAREER HIGHLIGHTS

1996	Join Bell Labs, Lucent Technologies. Conduct high frequency and high efficiency power conversion research.
2000	Cofounded NetPower Technologies. As its CTO and General Manager, grew NetPower into a technology leader in dc-dc power converter industry.
2010	Joined Huawei as its Principal Architect in embedded power business, responsible for technology and platform development. Invented and developed BEMRD power architecture and key blocks adopted in high performance and high density telecom/ network equipment.
2013	Joined BCD Semi/Diodes Inc as General Manager of ACDC BU. Manage the low power acdc controllers and smart phone charger solutions.
2015	Cofounded NuVolta Technologies Inc. Invented Controlled Resonance power architecture for flexible wireless power transfer, and developed industry's first integrated transmitter power IC for 6.78MHz MR solutions, which results in >50% reduction in both power loss and system cost.

QUOTE

Dr. Lee and VPEC taught me to maintain intellectual curiosity and positive altitude and to focus on solving real problems when facing tough challenges, which has helped in my personal growth as well.

Yuancheng Ren

Affiliation:
Joulwatt Technology Inc.

Position title:
VP of Marketing, System and Sales

Last degree from Virginia Tech:
Ph.D.

Year Graduated:
2005

CAREER HIGHLIGHTS

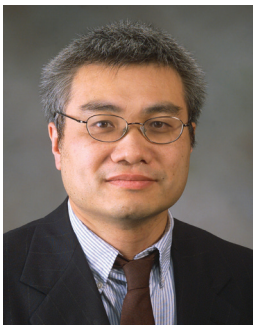
2005-2013 Work in MPS as Senior Director and General Manager of Asia R&D Center, setup a system and application team of 150 engineers. 80% new product definition is from this center. Helped MPS grow the revenue from $48 million to $220 million.

2013-now Work in Joulwatt as VP of Marketing, System and Sales, co-founder of Joulwatt

QUOTE

At CPES, I learned to work hard, work smart, and think outside the box. I learned to be thorough and rigorous when addressing engineering challenges. I am happy for the opportunity to work with the network of talented alumni in the field.

Fei (Fred) Wang



Affiliation:
University of Tennessee, Knoxville and Oak Ridge National Lab

Position title:
Professor and Condra Chair of Excellence in Power Electronics, CURENT Technical Director

Affiliation at VPEC/CPES:
Associate Professor and Technical Director

CAREER HIGHLIGHTS

1982 B.S. in Electrical Engineering, Xi'an Jiaotong University, Xi'an, China

1990 Ph.D. in Electrical Engineering, University of Southern California, Los Angeles, CA

1991 Research Scientist, Electric Power Lab, University of Southern California, Los Angeles, CA

1992 Application Engineer, GE Power Systems Engineering, Schenectady, NY

1994 Senior Design Engineer, GE Drive Systems, Salem, VA

1998 Received GE Dushman Award for contribution to GE Innovation Series Drives, including the world's first medium voltage IGBT and IGCT based three-level drives

2000 Program and Lab Manager, GE Global Research, Niskayuna, NY & Shanghai, China. Founded the GE power electronics research in China

2001 Research Associate Professor, CPES, Virginia Tech, Blacksburg, VA

2003 Started to serve concurrently as Technical Director, CPES, Virginia Tech, Blacksburg, VA

2004 Associate Professor, Virginia Tech, Blacksburg, VA

2009 Professor and Condra Chair of Excellence in Power Electronics, University of Tennessee, Knoxville with joint appointment at Oak Ridge National Lab, Knoxville, TN

2010 Elevated to IEEE fellow for contribution to high performance high density ac converters

2011 Started to serve concurrently as Technical Director, CURENT, University of Tennessee, Knoxville, TN, CURENT

QUOTE

CPES is about first class: first class people, first class facility, and first class work. My CPES experience was critical in helping establish CURENT at the University of Tennessee

Spotlight on Alumni

Pit-Leong Wong

Affiliation:
Joulwatt Technology
Position title:
CTO
Last degree
from Virginia Tech:
Ph.D.
Year Graduated:
2001

CAREER HIGHLIGHTS

2001~2013 Linear Technology, Design Engineer, Team Leader, Design Center GM
2013 Xieneng Technology, Technology VP
2014~present Joulwatt Technology, CTO

QUOTE

VPEC/CPES experiences have given me a solid background in power electronics. More importantly, the research attitude trained in VPEC/CPES has made a great impact in my career.

Eric X. Yang

Affiliation:
MPS Inc.
Position title:
VP System Engineering
Last degree
from Virginia Tech:
Ph.D.
Year Graduated:
1994

CAREER HIGHLIGHTS

1994~1998 Staff engineer of Harris Semiconductor. Lead the application team on developing MCT/IGBT devices, drivers, modules, and inverter systems.
1998~2006 Director of Semtech Corp. lead the application efforts on defining, developing, and promoting various dc-dc regulators for computer platforms.
2006~now VP System Engineering in charge of technical marketing, applications engineering, and critical system IP development.

QUOTE

The time at CPES was some of the best years of my life. I really appreciate Dr. Lee for providing the opportunity that led me into the field of power electronics. The academic environment, vigorous training, friendship with the fellow students and faculty were such valuable treasures for me. I have especially benefited by the solid methodology of doing engineering research I learned from Dr. Lee.

Feng Yu

Affiliation:
Ningbo Weie Electronics Technology Co. Ltd
Position title:
Founder & CEO
Last degree from Virginia Tech:
Master's
Year Graduated:
2011

CAREER HIGHLIGHTS

2011-2015 Senior Researcher and Manager in Silergy
2015-present Founder & CEO in Weie Technology

QUOTE

Dr. Lee's attention to details, wisdom, and foresight deeply impressed me. His methodology to the correct approach to research and work has helped me tremendously. Studying at CPES has been a very valuable experience in my life.

Xunwei Zhou

Affiliation:
Joulwatt Technology
Position title:
CEO
Last degree from Virginia Tech:
Ph.D.
Year Graduated:
1999

CAREER HIGHLIGHTS

1999~2001 Volterra Technology, Engineer
2001~2008 Linear Technology, Senior Design Engineer
2008~2010 Helix Technology, VP of Engineering
2013~present Joulwatt Technology, Founder

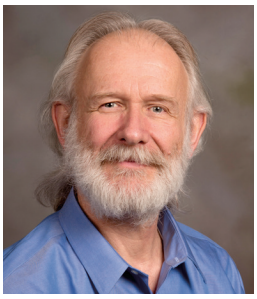
People

Faculty

Fred C. Lee

CPES Director
University Distinguished Professor (ECE)

Fred C. Lee received his B.S. degree in electrical engineering from the National Cheng Kung University in Taiwan in 1968, and his M.S. and Ph.D. degrees in electrical engineering from Duke University in 1972 and 1974, respectively. As CPES Director, Dr. Lee leads a program that encompasses research, technology development, educational outreach, industry collaboration, and technology transfer.



Dushan Boroyevich

CPES Co-Director
American Electric Power Professor (ECE)

Dushan Boroyevich was born in 1952 in Zagreb, Croatia, in what then used to be Yugoslavia. In the same country, he earned a Dipl. Ing. degree from the University of Belgrade in 1976 and an M.S. degree from the University of Novi Sad in 1982, both in electrical engineering. He obtained a Ph.D. degree in power electronics in 1986 from Virginia Polytechnic Institute and State University.

Rolando Burgos

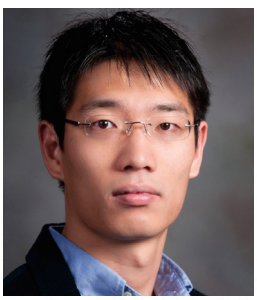
Associate Professor (ECE)

Rolando Burgos (S'96–M'03) was born in Concepcion, Chile, where he attended the University of Concepcion, earning his B.S. in electronics engineering in 1995 and a professional engineering certificate in electronics engineering in 1997, graduating with honors. At the same institution he later earned his M.S. and Ph.D. degrees in electrical engineering in 1999 and 2002, respectively.

Khai Ngo

Professor (ECE)

Khai Ngo received his B.S. degree from California State Polytechnic University, Pomona, in 1979, and his M.S. and Ph.D. degrees from the California Institute of Technology, Pasadena, in 1980 and 1984, respectively, all in electrical and electronics engineering. At Virginia Tech, he pursues technologies for integration and packaging of power passive and active components to realize building blocks for power electronic systems.



Qiang Li

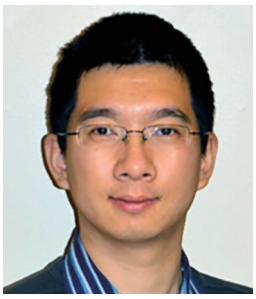
Assistant Professor (ECE)

Qiang Li received his B.S. degree in 2003 and M.S. degree in 2006 from Zhejiang University. Then in 2011 he received his Ph.D. from Virginia Tech. He started at Virginia Tech as a Research Assistant Professor in 2011 and was promoted to Assistant Professor in 2012. His research interests include high-density electronics packaging and integration, high-frequency magnetic components, high-frequency power conversion, distributed power systems, and renewable energy.

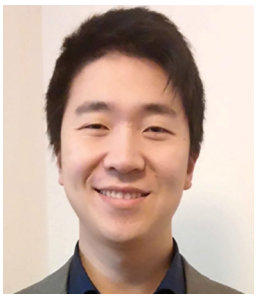
Affiliate faculty

Guo-Quan Lu

Research scientists



Zhiyu Shen



Xuning Zhang

Technical staff

Igor Cvetkovic

David Gilham

Support staff

Marianne Hawthorne

Linda Long

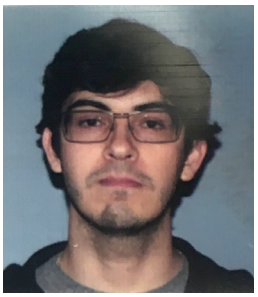
Trish Rose

Teresa Shaw

Lauren Shutt

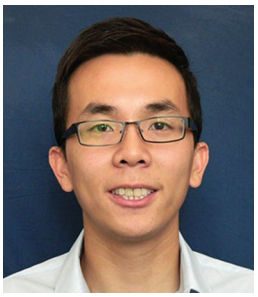
Visiting scholars

Tanbir Ahmed
STUDENT INTERN
University of Nottingham, UK



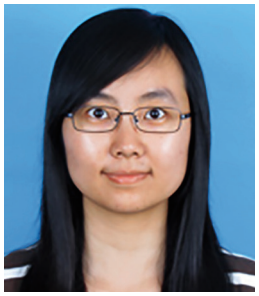
Pedro Campos
STUDENT INTERN
University of Brasilia, Brazil

Francesco Cavazzana
PH.D. STUDENT
University of Padova, Italy



Benjamin Cheong
PH.D. STUDENT
University of Nottingham, UK

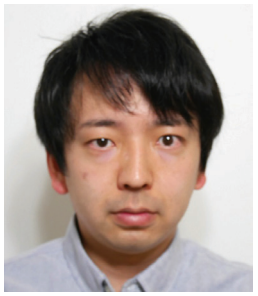
Wulong Cong
VISITING ENGINEER
Delta Electronics, Inc., China



Weijing Du
POSTDOC
Zhejiang University, China

Kenta Emori
VISITING ENGINEER
Nissan Motor Co., Ltd., Japan

Minfan Fu
PH.D. STUDENT
Univ. of Michigan/ Shanghai Jiaotong Univ. Joint Inst., China



Takayuki Ikari
VISITING ENGINEER
Nissan Motor Co., Ltd., Japan

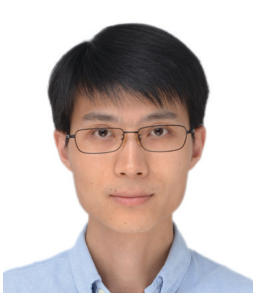
Zhihao Jiang
STUDENT INTERN
Tsinghua University, China

Akihiro Jonishi
VISITING ENGINEER
Fuji Electric Co., Ltd., Japan

Rae-Young Kim
PROFESSOR
Hanyang University, Korea

Yan-Cun (Daniel) Li
POSTDOC
National Taiwan University, Taiwan

Zeng Liu
PROFESSOR/ RESEARCHER
Xi'an Jiaotong University, China



Cheng Lu
VISITING ENGINEER
Delta Electronics, Inc., China

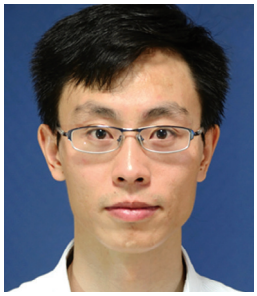
Remi Perrin
PH.D. STUDENT
Laboratoire AMPERE (SAFRAN), France

David Reusch
VISITING ENGINEER
Efficient Power Conversion, USA

Bo Sun
PH.D. STUDENT
Aalborg University, Denmark

Kenichiro Tanaka
VISITING ENGINEER
Panasonic Corporation, Japan

Meiyu (Marianne) Wang
PH.D. STUDENT
Tianjin University, China



Yifeng Wang
LECTURER
Tianjin University, China

Furong Xiao
PH.D. STUDENT
Beijing Institute of Technology, China

Guo Xu
PH.D. STUDENT
Beijing Institute of Technology, China

Rong Xu
POSTDOC
Harbin Institute of Technology, China

Xiaolong Yue
PH.D. STUDENT
Xi'an Jiaotong University, China

Seiya Yuki
VISITING ENGINEER
Dowa Metaltech Co., Ltd., Japan

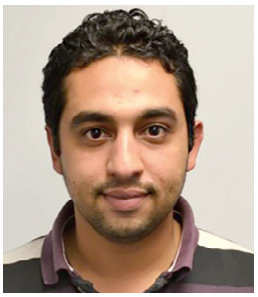
Jianhong Zeng
VISITING ENGINEER
Delta Electronics, Inc., China

Li Zeng
VISITING ENGINEER
CRRC Zhuzhou Institute Co., Ltd., China

Biao Zhao
POSTDOC
Tsinghua University, China

Students

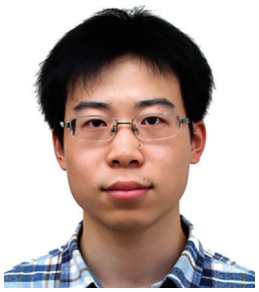

Robert Acken


Mohamed Ahmed


Syed Bari


Gitesh Bhagwat


Chien-An Chen

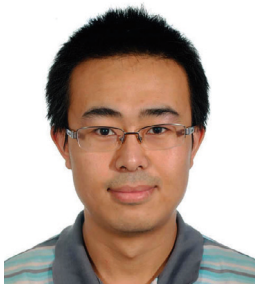

Fang Chen

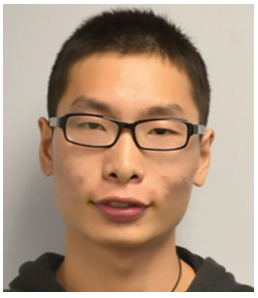

Alex Chu


Han Cui


Igor Cvetkovic


Christina DiMarino


Chao Fei


Junjie Fei

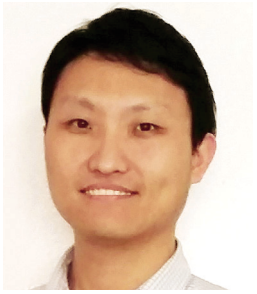

Rimon Gadelrab


Shan Gao

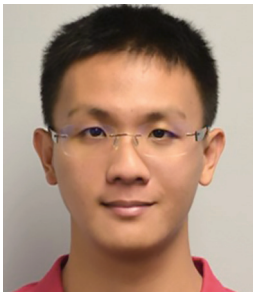

Ting Ge


Yingying Gui


Nidhi Haryani


Dongbin Hou


Xueyu Hou


Yi-Hsun Hsieh

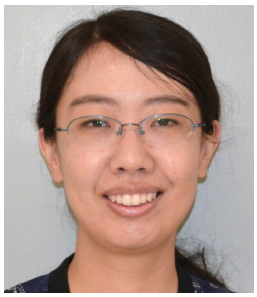

Zhengrong Huang


Mudit Khanna


Joseph Kozak

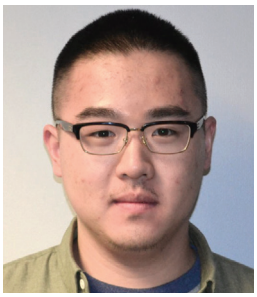

Bin Li


Chi Li


Qian Li


Virginia Li

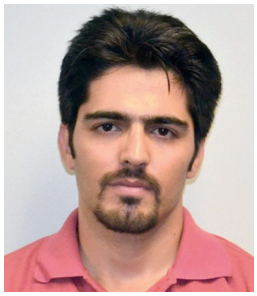

Lanbing Liu


Xingye Liu


Zhengyang Liu


Ming Lu


Yincan Mao


Alinaghi Marzoughi


Zichen Miao

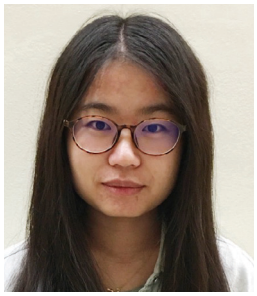

Slavko Mocevic

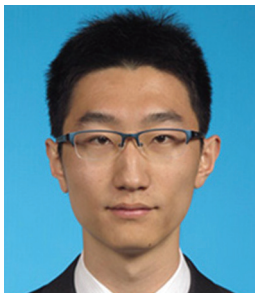

Sungjae Ohn


Paul Rankin

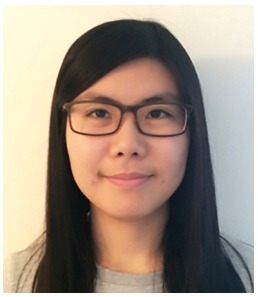

Niloofar Rashidi Mehrabadi


Amy Romero

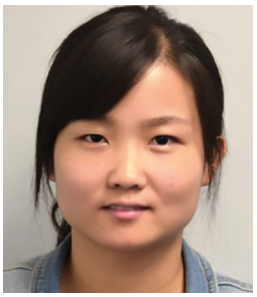

Bingyao Sun



Keyao Sun



Weizhen Sun

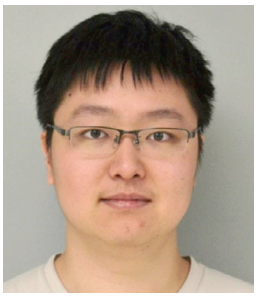


Ye Tang

Victor Turriate

Jun Wang

Qiong Wang



Kuangzhe Xu

Yue Xu

Yi Yan

Yuchen Yang

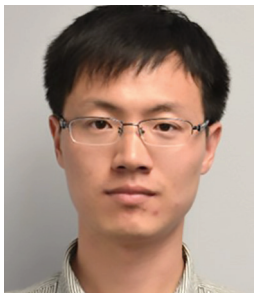
Jianghui Yu

Lujie Zhang

Graduates

Xiucheng Huang
Navitas Semiconductor

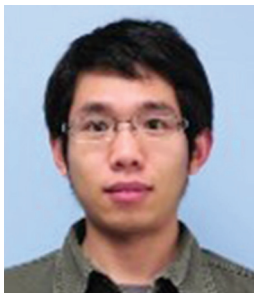
Chen Li
Zhong De Securities



Yadong Lyu
Monolithic Power Systems

Ruiyang Qin
Delta Electronics, Inc.

Zijian Wang
Linear Technology

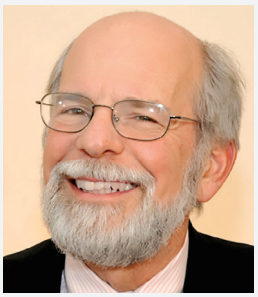


Zhemin Zhang
Texas Instruments

Shishuo Zhao
Texas Instruments

Scientific Advisory Board (SAB)

Ralph Cavin
Semiconductor Research Corporation (retired)



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Massachusetts Institute of Technology

Tom Lipo
University of Wisconsin-Madison (retired)

Bob Steigerwald
GE Global Research (retired)

Al Tucker
Office of Naval Research (retired)

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Luis Arnedo	United Technologies Research Center
Jianping Zhou	ZTE Corporation

Honors & Achievements

National and International Honors

Dushan Boroyevich – **2016 Outstanding Achievement Award**, European Power Electronics Association (EPE)

Dushan Boroyevich – **2016 IEEE Power Electronics Society Harry A. Owen Distinguished Service Award**

Dushan Boroyevich – **Kwoh-Ting Li Chair Professor** of National Cheng Kung University, Tainan, Taiwan

Qiang Li – **College of Engineering Dean's Award for Outstanding New Assistant Professor**, Virginia Tech

Fred C. Lee – **Chair Professor**, National Jiao Tong University, Taiwan

Fred C. Lee – **General Chair**, IEEE 8th International Power Electronics and Motion Control Conference (IPEMC 2016 ECCE-Asia), Hefei, China, May 22-25, 2016

Rolando Burgos – **VT Scholar of the Week**; to recognize his leading efforts in high power research in CPES and exploration of dc distributed systems for both low and medium voltage, September 2016

Fred C. Lee – **International Chair**, Subforum on "GaN Power Electronic Devices," International Forum on Wide Bandgap Semiconductors (IFWS 2016), Beijing, China, November 15-17, 2016

Rolando Burgos – **Technical Program Chair**, 2017 IEEE Electric Ship Technologies Symposium (ESTS) focused on emerging electric ship technologies

Keynote Addresses

Dushan Boroyevich, Keynote Speaker: "**Designing High-Power-Density Power Electronics for Transportation Applications, with Emphasis on the Use of WBG Semiconductor Devices**," 2016 International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles (ESARS) & International Transportation Electrification Conference (ITEC), Toulouse, France, November 2-4, 2016

Fred C. Lee, Keynote Speaker: "**Is GaN a Game Changing Device?**" International Forum on Wide Bandgap Semiconductors (IFWS 2016), Beijing, China, November 15, 2016

Invited Talks

Fred C. Lee, Invited Tutorial, "**Design for Manufacturability – Is it Time for a Paradigm Shift?**" 2017 CPES Annual Conference, Blacksburg, VA, April 3, 2016

Christina DiMarino (Ph.D. student), Invited Talk, "**Design and Integration of a 10 kV Silicon Carbide (SiC) MOSFET Power Module**," invited paper by Christina DiMarino, Mark Johnson, Dushan Boroyevich, Rolando Burgos, Guo-Quan Lu, 2016 International Conference on Electronics Packaging (ICEP), Sapporo, Japan, April 22, 2016

Qiang Li, Invited Talk, "**GaN based MHz power converters for data center application**," 2016 International Workshop on Wide Bandgap Semiconductor Power Electronics (IWWSPE-2016), Xi'an, China, May 21-22, 2016.

Qiang Li, Invited Talk: "**High Efficiency, High Density Power Converter with WBG Devices for Data Center, Battery Charger Applications**," The 3rd NPERC-J Workshop, Tokyo, Japan, May 27, 2016

Fred C. Lee, Invited Talk, "**Energy and Power Electronics: Challenges in the 21st Century**," Shanghai Jiaotong University, Shanghai, China, June 7, 2016

Fred C. Lee, Invited Talk, "**Energy and Power Electronics: Challenges in the 21st Century**," Tsinghua University, Beijing, China, June 8, 2016

Fred C. Lee, Invited Talk, "**Modular Multilevel Converter State Space Analysis**," State Grid Electric Power Research Institute, NARI Group Corporation, Beijing, China, June 9, 2016

Rolando Burgos, Invited Tutorial, "**Impedance-based Stability of AC Power Systems**," 2016 IEEE COMPEL, Trondheim, Norway, June 27, 2016

Fred C. Lee, Invited Talk, "**Evolution of Power Electronics**," Shangdong University, Jinan, Shangdong, China, November 12, 2016

Fred C. Lee, Invited Talk: "**Impact of GaN to Power Electronics and Sustainable Energy**," International Forum on Wide Bandgap Semiconductors (IFWS 2016), Beijing, China, November 16, 2016

Dushan Boroyevich, Invited Tutorial, "**Is SiC a Game Changer?**" IEEE Southern Power Electronics Conference (SPEC), Auckland, New Zealand, December 5, 2016

Fred C. Lee, Invited Talk: "**Power Delivery for Future Data Centers – Challenges and Opportunities**," IBM Watson Lab, Yorktown Heights, NY, December 8, 2016

Qiang Li, Invited talk, "**High Density Integrated Voltage Regulator Solution for Data Center**," Tutorial session, "High Speed and High Power Technologies for Modern Data Centers," 2016 IEEE MTT-S Latin America Microwave Conference (LAMC-2016), Puerto Vallarta, Mexico, December 12-14, 2016

Outstanding Presentation Awards

30th Annual IEEE Applied Power Electronics Conference & Exposition (APEC), Long Beach, CA, March 20-24, 2016

"**Equivalent Circuit Modeling of LLC Resonant Converter**," **Shuilin Tian**

"**Magnetic Characterization Technique and Materials Comparison for Very High Frequency IVR**," **Dongbin Hou**

"**Conducted EMI Analysis and Filter Design for MHz Active Clamp Flyback Front-End Converter**," **Xiucheng Huang**

"**Digital-Based Interleaving Control for GaN-Based MHz CRM Totem-Pole PFC**," **Zhengyang Liu**

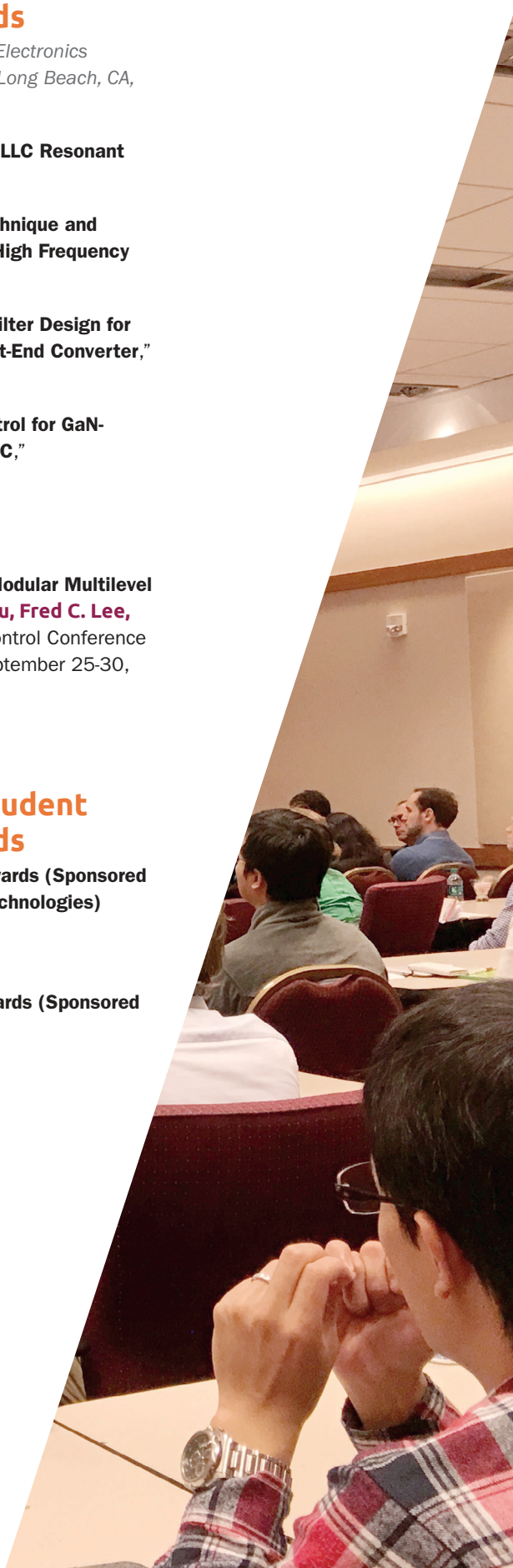
Best Paper Award

"State Trajectory Analysis for Modular Multilevel Converter," Chen Li, Yadong Lyu, Fred C. Lee, Power Electronics and Motion Control Conference (IEEE-PEMC) Varna, Bulgaria, September 25-30, 2016

2016 CPES Annual Conference Best Student Presentation Awards

Best Technical Presentation Awards (Sponsored by Delta Electronics, Huawei Technologies)
Xiucheng Huang
Syed Bari

Best Dialogue Presentation Awards (Sponsored by CPES):
Christina DiMarino
Dongbin Hou
Bingyao Sun



Publications

Transactions Papers

A New Package of High-Voltage Cascode Gallium Nitride Device for Megahertz Operation
Wenli Zhang, Xiucheng Huang, Zhengyang Liu, Fred C. Lee, Shuojie She, Weijing Du, Qiang Li
IEEE Transactions on Power Electronics, Vol. 31, No. 2, February 2016, pp. 1344-1353

Unified Equivalent Circuit Model and Optimal Design of V2 Controlled Buck Converters
Shuilin Tian, Fred C. Lee, Qiang Li, Yingyi Yan
IEEE Transactions on Power Electronics, Vol. 31, No. 2, February 2016, pp. 1734 - 1744

DBC Switch Module for Management of Temperature and Noise in 200-W/in3 Power Assembly
Jongwon Shin, Woochan Kim, Khai D.T. Ngo
IEEE Transactions on Power Electronics, Vol. 31, No. 3, March 2016, pp. 2387-2394

A Simplified Equivalent Circuit Model of Series Resonant Converter
Shuilin Tian, Fred C. Lee, Qiang Li
IEEE Transactions on Power Electronics, Vol. 31, No. 5, May 2016, pp. 3922-3931

Voltage-Level Selection of Future Two-Level LVdc Distribution Grids: A Compromise Between Grid Compatibiliy, Safety, and Efficiency
Enrique Rodriguez-Diaz, Fang Chen, Juan C. Vasquez, Josep M. Guerrero, Rolando Burgos, Dushan Boroyevich
IEEE Electrification Magazine, Vol. 4, No. 2, June 2016, pp. 20-28

High-Frequency High-Efficiency GaN-Based Interleaved CRM Bidriectional Buck/Boost Converter with Inverse Coupled Inductor
Xiucheng Huang, Fred C. Lee, Qiang Li, Weijing Du
IEEE Transactions on Power Electronics, Vol. 31, No. 6, June 2016, pp. 4343-4352

A New Circuit Performance of Modular Multilevel Inverter Suitable for Photovoltaic Conversion Plants
Hamed Nademi, Anandarup Das, Rolando Burgos, Lars E. Norum
IEEE Journal on Emerging and Selected Topics in Power Electronics, Vol. 4, No. 2, June 2016, pp. 393-404

Small Signal Analysis of V2 Control Using Equivalent Circuit Model of Current Mode Controls
Yingyi Yan, Fred C. Lee, Paolo Mattavelli, Shuilin Tian
IEEE Transactions on Power Electronics, Vol. 31, No. 7, July 2016, pp. 5344-5353

Design of GaN-based MHz Totem-pole PFC Rectifier
Zhengyang Liu, Fred C. Lee, Qiang Li, Yuchen Yang
IEEE Journal of Emerging and Selected Topics in Power Electronics, September 2016, Vol. 4, No. 3, pp. 799-807

Digital-Based Interleaving Control for GaN-based MHz CRM Totem-pole PFC
Zhengyang Liu, Zhengrong Huang, Fred C. Lee, Qiang Li
IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 4, No. 3, September 2016, pp. 808-814

Design and Optimization of a 380V-12V High-Frequency, High-Current LLC Converter with GaN Devices and Planar Matrix Transformers
Mingkai Mu, Fred C. Lee
IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 4, No. 3, September 2016, pp. 854-862

Structural Resemblance Between Droop Controllers and Phase-Locked Loops
Qing-Chang Zhong, Dushan Boroyevich
IEEE Access, Vol. 4, September 2016, pp. 5733 - 5741

A Three-Terminal Switch Model of Constant On-Time Current Mode with External Ramp Compensation
Shuilin Tian, Fred C. Lee, Jian Li, Qiang Li, Pei-Hsin Liu
IEEE Transactions on Power Electronics, Vol. 31, No. 10, October 2016, pp. 7311-7319

Analysis of Existence-Judging Criteria for Optimal Power Regions in DMPPT PV Systems
Feng Wang, Fang Zhuo, Fred C. Lee, Tianhua Zhu, Hao Yi
IEEE Transactions on Energy Conversion, Vol. 31, No. 4, December 2016, pp. 1433 - 1441

"**Multimega VAR Passive Filters for Mining Applications: Practical Limitations and Technical Considerations**"
Luis Moran, Cristobal A. Albistur, Rolando Burgos
IEEE Transactions on Industry Applications, Vol. 52, No. 6, November/December 2016, pp. 5310-5317

Application of GaN Devices for 1 kW Server Power Supply with Integrated Magnetics (Invited Paper)
Fred C. Lee, Qiang Li, Zhengyang Liu, Yuchen Yang, Chao Fei, Mingkai Mu
Chinese Power Supply Society (CPSS) Transactions on Power Electronics and Applications, Founding Issue: Vol. 1, No. 1, December 2016, pp. 3-12

Avoiding Divergent Oscillation of Cascode GaN Device under High-Current Turn-off Condition
Xiucheng Huang, Weijing Du, Fred C. Lee, Qiang Li, Wenli Zhang
IEEE Transactions on Power Electronics, Vol. 32, No. 1, January 2017, pp. 593-601

Design of Inductors With Significant AC Flux
Zhemin Zhang, Khai D. T. Ngo, Jeff L. Nilles
IEEE Transactions on Power Electronics, Vol. 32, No. 1, January 2017, pp. 529-539

Two-Dimensional Gapping to Reduce Light-Load Loss of Point-of-Load Inductor
Ting Ge, Khai D. T. Ngo, Jim Moss
IEEE Transactions on Power Electronics, Vol. 32, No. 1, January 2017, pp. 540-550

Low-Frequency Common-Mode Voltage Control for Systems Interconnected With Power Converters
Fang Chen, Rolando Burgos, Dushan Boroyevich, Xuning Zhang
IEEE Transactions on Industrial Electronics, Vol. 64, No. 1, January 2017, pp. 873-882

Conference Papers

Equivalent Circuit Modeling of LLC Resonant Converter
Shuilin Tian, Fred C. Lee, Qiang Li
2016 APEC (30th Annual IEEE Applied Power Electronics Conference & Exposition), Long Beach, CA, March 20-24, 2016

Digital Implementation of Adaptive Synchronous Rectifier (SR) Driving Scheme for LLC Resonant Converters
Chao Fei, Fred C. Lee, Qiang Li,
2016 APEC (30th Annual IEEE Applied Power Electronics Conference & Exposition), Long Beach, CA, March 20-24, 2016

Magnetic Characterization Technique and Materials Comparison for Very High Frequency IVR
Dongbin Hou, Fred C. Lee, Qiang Li
2016 APEC (30th Annual IEEE Applied Power Electronics Conference & Exposition), Long Beach, CA, March 20-24, 2016

Design Consideration of MHz Active Clamp Flyback Converter with GaN Devices for Low Power Adapter Application
Xiucheng Huang, Junjie Feng, Weijing Du, Fred C. Lee, and Qiang Li
2016 APEC (30th Annual IEEE Applied Power Electronics Conference & Exposition), Long Beach, CA, March 20-24, 2016

Conducted EMI Analysis and Filter Design for MHz Active Clamp Flyback Front-End Converter
Xiucheng Huang, Junjie Feng, Fred C. Lee, Qiang Li, and Yuchen Yang
2016 APEC (30th Annual IEEE Applied Power Electronics Conference & Exposition), Long Beach, CA, March 20-24, 2016

A New Current Mode Constant On Time Control with Ultrafast Load Transient Response
Syed Bari, Qiang Li, Fred C. Lee
2016 APEC (30th Annual IEEE Applied Power Electronics Conference & Exposition), Long Beach, CA, March 20-24, 2016

Digital-Based Interleaving Control for GaN-Based MHz CRM Totem-Pole PFC
Zhengyang Liu, Zhengrong Huang, Fred C. Lee, Qiang Li
2016 APEC (30th Annual IEEE Applied Power Electronics Conference & Exposition), Long Beach, CA, March 20-24, 2016

Avoiding Divergent Oscillation of Cascode GaN Device Under High Current Turn-Off Condition
Weijing Du, Xiucheng Huang, Fred C. Lee, Qiang Li, and Wenli Zhang
2016 APEC (30th Annual IEEE Applied Power Electronics Conference & Exposition), Long Beach, CA, March 20-24, 2016

A Novel AC-to-DC Adaptor with Ultra-High Power Density and Efficiency
Yan-Cun Li, Fred C. Lee, Qiang Li, Xiucheng Huang, Zhengyang Liu
2016 APEC (30th Annual IEEE Applied Power Electronics Conference & Exposition), Long Beach, CA, March 20-24, 2016

Improved Current-Mode Control with Single-Cycle Load Transient
Virginia Li, Peihsin Liu, Qiang Li, Fred C. Lee
2016 APEC (30th Annual IEEE Applied Power Electronics Conference & Exposition), Long Beach, CA, March 20-24, 2016

Point-of-Load Inductor with High Swinging and Low Loss at Light Load
Ting Ge, Khai Ngo, and Jim Moss
2016 APEC (30th Annual IEEE Applied Power Electronics Conference & Exposition), Long Beach, CA, March 20-24, 2016

Active Control of Low Frequency Common Mode Voltage to Connect AC Utility and 380 V DC Grid
Fang Chen, Rolando Burgos, Dushan Boroyevich, Xuning Zhang
2016 APEC (30th Annual IEEE Applied Power Electronics Conference & Exposition), Long Beach, CA, March 20-24, 2016

Ultra-Low Inductance Vertical Phase Leg Design with EMI Noise Propagation Control for Enhancement Mode GaN Transistors
Xuning Zhang, Zhiyu Shen, Nidhi Haryani, Dushan Boroyevich and Rolando Burgos
2016 APEC (30th Annual IEEE Applied Power Electronics Conference & Exposition), Long Beach, CA, March 20-24, 2016

Gate Driver Design for 1.7kV SiC MOSFET Module with Rogowski Current Sensor for Shortcircuit Protection
Jun Wang, Zhiyu Shen, Christina DiMarino, Rolando Burgos, Dushan Boroyevich
2016 APEC (30th Annual IEEE Applied Power Electronics Conference & Exposition), Long Beach, CA, March 20-24, 2016

Switching Condition and Loss Modeling of GaN-Based Dual Active Bridge Converter for PHEV Charger
Lingxiao Xue, Dushan Boroyevich, Paolo Mattavelli
2016 APEC (30th Annual IEEE Applied Power Electronics Conference & Exposition), Long Beach, CA, March 20-24, 2016

Static and Dynamic Characterization of GaN HEMT with Low Inductance Vertical Phase Leg Design for High Frequency High Power Applications
Nidhi Haryani, Xuning Zhang, Rolando Burgos, Dushan Boroyevich
2016 APEC (30th Annual IEEE Applied Power Electronics Conference & Exposition), Long Beach, CA, March 20-24, 2016

Small-Signal Terminal Characteristics Modeling of Three-Phase Boost Rectifier with Variable Fundamental Frequency
Zeng Liu, Jinjun Liu, Dushan Boroyevich
2016 APEC (30th Annual IEEE Applied Power Electronics Conference & Exposition), Long Beach, CA, March 20-24, 2016

2 MHz High-Density Integrated Power Supply for Gate Driver in High-Temperature Applications
Remi Perrin, Bruno Allard, Cyril Buttay, Nicolas Quentin, Wenli Zhang, Rolando Burgos, Dushan Boroyevich, Philipe Preciat, Donatien Martineau
2016 APEC (30th Annual IEEE Applied Power Electronics Conference & Exposition), Long Beach, CA, March 20-24, 2016, pp. 524-528

Additive Manufacturing of Magnetic Components for Power Electronics Integration
Yi Yan, Khai D. T. Ngo, Yuhui Mei, Guo-Quan Lu
2016 International Conference on Electronics Packaging (ICEP 2016), Sapporo, Japan, April 20-22, 2016, pp. 368 - 371

Thermo-mechanical Reliability of High-temperature Power Modules with Metal-ceramic Substrates and Sintered Silver Joints
Shan Gao, Seiyu Yuki, Hideyo Osanai, Weizhen Sun, Khai D. T. Ngo, Guo-Quan Lu
2016 International Conference on Electronics Packaging (ICEP 2016), Sapporo, Japan, April 20-22, 2016, pp. 395 - 399

A Large Input Voltage Range 1 MHz Full Converter with 95% Peak Efficiency for Aircraft Applications
Nicolas Quentin, Remi Perrin Christian Martin, Charles Joubert, Louis Grimaud, Rolando Burgos, Dushan Boroyevich
PCIM Europe 2016, Nuremberg, Germany, May 10 - 12, 2016, pp. 1286-1293

Stability Criterion of Droop-Controlled Parallel Inverters Based on Terminal-Characteristics of Individual Inverters
Zeng Liu, Jinjun Liu, Dushan Boroyevich, Rolando Burgos
2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC 2016-ECCE Asia), Hefei, China, May 22-25, 2016, pp. 2958 - 2963

Passive Component Loss Minimization for Interleaved dc-dc Boost Converters in Electric Vehicle Applications
Xuning Zhang, Rolando Burgos, Dushan Boroyevich
2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), Hefei, China, May 22-25, 2016, pp. 1412 - 1418

A Wirebond-less Package for High-Voltage Cascode Gallium Nitride Devices
Wenli Zhang, Zhengyang Liu, Shuojie She, Fred C. Lee
IEEE Electronic Components and Technology Conference (ECTC), Las Vegas, NV, May 31-June 3, 2016

Impact of PV Inverter Generation on Voltage Profile and Power Loss in Medium Voltage Distribution Systems
Ye Tang, Rolando Burgos, Chi Li, Dushan Boroyevich
2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC), Portland, OR, June 5-10, 2016

Additive Manufacturing of Magnetic Components for Power Electronics Integration
Yi Yan, Khai Ngo, Yunhui Mei, Guo-Quan Lu
International Symposium on 3D Power Electronics Integration and Manufacturing (PEIM), Raleigh, NC, June 13-15, 2016

Impact of PV Inverter Penetration on Voltage Profile and Power Loss in Medium Voltage Distribution Systems
Ye Tang, Rolando Burgos, Chi Li, Dushan Boroyevich
2016 IEEE COMPEL, Trondheim, Norway, June 27-30, 2016

Experimental Verification of a Virtual Synchronous Generator Control Concept
Igor Cvetkovic, Dushan Boroyevich, Rolando Burgos, Paolo Mattavelli, Yi-Hsun Hsieh, Fred C. Lee, Chi Li
2016 IEEE COMPEL, Trondheim, Norway, June 27-30, 2016

Impedance-Based Stability Analysis of Multiple STATCOMs in Proximity
Chi Li, Rolando Burgos, Ye Tang, Dushan Boroyevich
2016 IEEE COMPEL, Trondheim, Norway, June 27-30, 2016

Predicting the Behavior of a High Switching Frequency SiC-Based Modular Power Converter Based on Low-Power Validation Experiments
Niloofar Rashidi Mehrabadi, Rolando Burgos, Christopher Roy, Dushan Boroyevich, Jianghui Yu
2016 IEEE COMPEL, Trondheim, Norway, June 27-30, 2016

Output Impedance Comparison of Different Droop Control Realizations in DC Systems
Fang Chen, Rolando Burgos, Dushan Boroyevich
2016 IEEE COMPEL, Trondheim, Norway, June 27-30, 2016

Optimal Control of Three-Phase Embedded Power Grids
Andrea Formentini, David Dewar, Pericle Zanchetta, Pat Wheeler, Dushan Boroyevich, Jean-Luc Schanen
2016 IEEE COMPEL, Trondheim, Norway, June 27-30, 2016

A Frequency Domain Model for Beat Frequency Oscillation Analysis in Microgrid
Xiaolong Yue, Dushan Boroyevich, Rolando Burgos, Fang Zhuo
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Analysis and Distributed Control of Power Flow in DC Microgrids to Improve System Efficiency
Fang Chen, Rolando Burgos, Dushan Boroyevich, Enrique Rodriguez-Diaz, Lexuan Meng, Juan C. Vasquez, Josep M. Guerrero
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High Efficiency 2-Stage 48v VRM with PCB Winding Matrix Transformer
Mohamed Ahmed, Chao Fei, Fred C. Lee, Qiang Li
2016 IEEE Energy Conversion Congress & Expo (ECCE 2016), Milwaukee, WI, September 18-22, 2016

Very High Frequency Integrated Voltage Regulator for Small Portable Device
Dongbin Hou, Fred C. Lee, Qiang Li
2016 IEEE Energy Conversion Congress & Expo (ECCE 2016), Milwaukee, WI, September 18-22, 2016

Design of CRM AC/DC Converter for Very High-Frequency High-Density WBG-Based 6.6kW Bidirectional On-Board Battery Charger
Zhengyang Liu, Bin Li, Fred C. Lee, Qiang Li
2016 IEEE Energy Conversion Congress & Expo (ECCE 2016), Milwaukee, WI, September 18-22, 2016

Dynamic Bus Voltage Control for Light Load Efficiency Improvement of Two-stage Voltage Regulator
Chao Fei, Mohamed H. Ahmed, Fred C. Lee, Qiang Li
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Microcontroller-based MHz Totem-pole PFC with Critical Mode Control
Zhengrong Huang, Zhengyang Liu, Qiang Li, Fred C. Lee
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Variable Slope External Ramp to Improve the Transient Performance in Constant On-Time Current Mode Control
Syed Bari, Brian Cheng, Qiang Li, Fred C. Lee
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Additive Manufacturing of Toroid Inductor for Power Electronics Application
Yi Yan, Jim Moss, Khai Ngo, Yunhui Mei, Guo-Quan Lu
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NiCuZn Ferrite Cores by Gelcasting: Processing and Properties
Lanbing Liu, Yi Yan, Khai Ngo, Guo-Quan Lu
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Characterization and Comparison of Latest Generation 900-V and 1.2-kV SiC MOSFETs
Alinaghi Marzoughi, Rolando Burgos, Dushan Boroyevich
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Design and Optimization of a High Performance Isolated Three Phase AC/DC Converter
Qiong Wang, Xuning Zhang, Rolando Burgos, Dushan Boroyevich, Adam White, Mustansir Kheraluwala
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Small-signal Terminal-Characteristics Modeling of Three-Phase Droop-Controlled Inverters
Zeng Liu, Jinjun Liu, Dushan Boroyevich, Rolando Burgos, Teng Liu
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Busbar Design for SiC-Based H-Bridge PEBB using 1.7 kV, 400 A SiC MOSFETs Operating at 100 kHz
Niloofar Rashidi Mehrabadi, Igor Cvetkovic, Jun Wang, Rolando Burgos, Dushan Boroyevich
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Modeling and Analysis for Input Characteristics of Line-Frequency Rectifiers
Xiaolong Yue, Dushan Boroyevich, Rolando Burgos, Fang Zhuo
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Two Comparison-Alternative High Temperature PCB-Embedded Transformer Designs for a 2 W Gate Driver Power Supply
Bingyao Sun, Remi Perrin, Cyril Buttay, Bruno Allard, Nicolas Quentin, Rolando Burgos, Dushan Boroyevich, Marwan Ali
2016 IEEE Energy Conversion Congress & Expo (ECCE 2016), Milwaukee, WI, September 18-22, 2016

Active dv/dt Control of 600V GaN Transistors
Bingyao Sun, Rolando Burgos, Xuning Zhang, Dushan Boroyevich
2016 IEEE Energy Conversion Congress & Expo (ECCE 2016), Milwaukee, WI, September 18-22, 2016

Taking Into Account Interactions between Converters in the Design of Aircraft Power Networks
Qian Li, Andrea Formentini, Arnaud Baraston, Xuning Zhang, Pericle Zanchetta, Jean-Luc Schanen, Dushan Boroyevich
2016 IEEE Energy Conversion Congress & Expo (ECCE 2016), Milwaukee, WI, September 18-22, 2016

Integrated Switch Current Sensor for Shortcircuit Protection and Current Control of 1.7-kV SiC MOSFET Modules
Jun Wang, Zhiyu Shen, Rolando Burgos, Dushan Boroyevich
2016 IEEE Energy Conversion Congress & Expo (ECCE 2016), Milwaukee, WI, September 18-22, 2016

Design of a Two-Switch Flyback Power Supply Using 1.7 kV SiC Devices for Ultra-Wide Input-Voltage Range Applications
Gabriele Rizzoli, Jun Wang, Zhiyu Shen, Rolando Burgos, Dushan Boroyevich, Luca Zarri
2016 IEEE Energy Conversion Congress & Expo (ECCE 2016), Milwaukee, WI, September 18-22, 2016

State Trajectory Analysis for Modular Multilevel Converter (Best Paper Award)
Chen Li, Yalong Lyu, Fred C. Lee
Power Electronics and Motion Control (IEEE PEMC) Conference, Varna, Bulgaria, September 25-30, 2016

Optimized Design Procedure for Active Power Converters in Aircraft Electrical Power Systems
Qiong Wang, Rolando Burgos, Xuning Zhang, Dushan Boroyevich, Adam White, Mustansir Kheraluwala
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Conceptual Design and Weight Optimization of Aircraft Power Systems with High-Peak Pulsed Power Loads
Qian Li, Balakrishnan Devarajan, Xuning Zhang, Rolando Burgos, Dushan Boroyevich, Pradeep Raj
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Sequential Design for Coils in Series-Series Inductive Power Transfer Using Normalized Parameters
Ming Lu, Khai Ngo
IEEE PELS Workshop on Emerging Technologies: Wireless Power (WoW 2016), Knoxville, Tennessee, USA, October 4–6, 2016, pp. 21-26

Pareto Fronts for Coils' Efficiency Versus Stray Magnetic Field in Inductive Power Transfer
Ming Lu, Khai Ngo
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Theses and Dissertations

Spurious Turn-On inside a Power Module of Paralleled SiC MOSFETs
Zichen Miao, Khai Ngo
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A High-Density, High-Efficiency 1.2 kV SiC MOSFET Module and Gate Drive Circuit
Christina DiMarino, Wenli Zhang, Nidhi Haryani, Qiong Wang, Rolando Burgos, Dushan Boroyevich
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Conducted EMI Noise Prediction and Filter Design Optimization
Zijian Wang
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Chen Li
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High Frequency GaN Characterization and Design Considerations
Xiucheng Huang
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Study on Three-level DC/DC Converter with Coupled Inductors
Ruiyang Qin
Thesis, September 6, 2016

DC Fault Current Analysis and Control for Modular Multilevel Converters
Jianghui Yu
Thesis, November 28, 2016

High-Frequency Quasi-Square-Wave Flyback Regulator
Zhemin Zhang
Dissertation, November 28, 2016

High Frequency Isolated Power Conversion from Medium Voltage AC to Low Voltage DC
Shishuo Zhao
Thesis, December 15, 2016

Modeling and Control Strategy for Capacitor Minimization of Modular Multilevel Converters
Yadong Lyu
Thesis, January 26, 2017

CPES Research Volumes

Each volume below is a collection of papers generated by CPES researchers through a number of years, organized by technology topic.

Volume I: High-Frequency Resonant, Quasi-Resonant, and Multi-Resonant Converters
1989

Volume II: Modeling, Analysis, and Design of PWM Converters
1990

Volume III: Power Devices and their Applications
1991

Volume IV: High-Frequency Resonant and Soft-Switching PWM Converters
1992

Volume V: Switching Rectifiers for Power Factor Correction
1994

Volume VI: Power Electronics Components and Circuit Modeling and Analysis
1995

Volume VII: Advanced Power Conversion Techniques
1995

Volume VIII: Converters and Distributed Power Systems
1995

Volume IX: Low Voltage Power Conversion and Distributed Power Systems
2000

Volume X: Integrated Power Electronics Module -- a Building Block Concept for System Integration
2000

Volume XI: Advanced Soft-Switching Techniques, Device and Circuit Applications
2000

Volume XII: Conducted EMI and Power Electronics: Characterization and Mitigation
2008

Volume XIII-Book 1: Systems-Based Power Electronics Integration Technology
2008

Volume XIII-Book 2: Systems-Based Power Electronics Integration Technology
2008

Volume XIV: Distributed Power Systems Front-End Converters: Power Factor Correction and Isolated Converters
2008

Volume XV: Distributed Power Systems: Point-of-Load Converters
2008

Volume XVI: Distributed Power Systems: Front-End Converters (Part II)
2016

Volume XVII: Distributed Power Systems: Point-of-Load Converters (Part II)
2016

Volume XVIII: Wide-Bandgap Power Devices and Applications
2016


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2015 Charter

Short-term/long-term goals

Over the past four decades, CPES has developed promising new power electronics technologies, including new types of power semiconductor devices, high-frequency magnetics, soft-switching technologies that significantly reduce switching losses and EMI, advanced materials and packaging technologies with planar inter-connect processes, integrated sensors, and thermo-mechanical integration. These technologies collectively serve as the mainstay for the successful integration of modular building blocks into power electronics.

Industry adoption of the IPEM approach began in earnest in the early 2000s for applications such as power management solutions for the new generation of microprocessor, power supplies for the IT industry, electric/hybrid vehicles, and PV inverters, as well as variable-speed motor drives for applications ranging from industry automation and process control to home appliances. These core technologies offer the promise of higher performance at a lower cost with improved reliability. CPES is poised to extend these core competencies to a wide range of new and emerging applications, elaborated in the following paragraphs.

We expect the emergence of wide bandgap semiconductors to make it possible to operate converters at significantly higher switching frequencies, efficiency, and power density, and to operate at elevated temperatures. This new generation of wide bandgap devices is poised to make a significant impact on the marketplace currently dominated by silicon power devices. These high-frequency and higher-temperature devices require advanced packaging technologies, together with high-temperature interface materials, passive components and improved thermal management. CPES has unique strength in these areas and is a member of the "PowerAmerica" Institute led by North Carolina State University. This institute has been established as an alliance of 18 corporations, 5 universities and 2 government labs. This program was initiated in early 2015 with a total budget of $140M over five years aimed at developing wide bandgap power devices and associated system applications.

As the new generation of devices operate at significantly higher switching frequencies, power quality and electromagnetic interference and compatibility (EMI/EMC) have become increasingly important. The Center has pioneered a number of innovative technologies leading to significant improvements in power quality and EMI/EMC performance, and we plan to integrate these features directly into the next generation of power conversion systems. CPES researchers are well positioned to play a leading role in helping industry and

government agencies find high-performance, cost-effective solutions.

With ever-increasing current consumption and clock frequencies, today's microprocessors are operating at very low voltages (1 volt or less) and continuously switching between "sleep mode" and "wake-up mode" to conserve energy. This imposes a significant challenge to power delivery and management. Over the past 15 years, with the steady support of over 20 corporations, CPES has developed a multi-phase voltage regulator (VR) module to power new generations of Intel microprocessors. This research project has generated more than 30 US patents, covering such areas as power delivery architecture; modularity and scalability; control and sensing; current sharing; integrated magnetics; and advanced packaging and integration. Today, every PC and server microprocessor in the world is powered with this multi-phase VR.

These technologies have been further extended to high-performance graphical processors, server chipsets and memory devices, networks, telecommunications, and all forms of mobile electronics, including smartphones. This project is structured as the Power Management Consortium (PMC) within the Center's Industry Consortium Program, which has over 80 participating members. The research scope of this mini-consortium has expanded in recent years to include power architecture and the management of data centers, telecommunications equipment, LED lighting, and PV converter/inverters.

Due to the successful undertakings of the PMC, two new mini-consortiums were initiated in 2012. One is named High Density Integration (HDI) and the other is Renewable Energy and Nanogrids (REN). While the HDI is an extension of the early work supported under NSF's ERC to further develop IPEMs and system integration based on the new generation of wide bandgap devices, the REN mini-consortium is focused on high-power, high-voltage power conversion technologies to facilitate the integration of various forms of renewable energy sources, such as offshore wind farms, PV farms and energy storage systems, into the existing electrical grids. This integration will be in a distributed form via power electronics devices; from power generation, transmission, and distribution all the way to the end users. This requires significant changes of the existing power grid structure, and power electronics will play a critical role in integrating the unpredictable nature of the renewable energy sources. Future grids with distributed power electronics devices will enable the formation of a smart electronic energy network, with the ability to connect high-voltage dc grids that connect renewable energy sources to the existing ac grids through medium-voltage cascade power conversion stages, solid-state transformers, and new control technologies.

CPES has established one of the largest university/industry partnership programs in the US and has developed an innovative process for moving technology and intellectual property out of academic laboratories and into the marketplace. The process enables critical technologies developed by the Center to permeate all forms of power electronics equipment and systems, and has profoundly impacted the design and manufacturing process of the industry. With an increasing level of industry participation, more than 30 industry-funded graduate fellowships are made available to CPES students annually, with industry members serving as mentors to the students' research. This rather unique industry/university collaboration was cited by the NSF as a model ERC for its education/outreach program, industry collaboration, and technology transfer program. This program has continued to flourish since CPES graduated from the NSF ERC in 2008.

Participation and Governance

CPES is made up of the highest level of faculty in the area of power electronics and power electronics systems. Top-caliber students from electrical engineering programs worldwide pursue their masters and doctorate degrees at CPES-Virginia Tech, and in turn are heavily recruited after graduation, many by our industry partners.

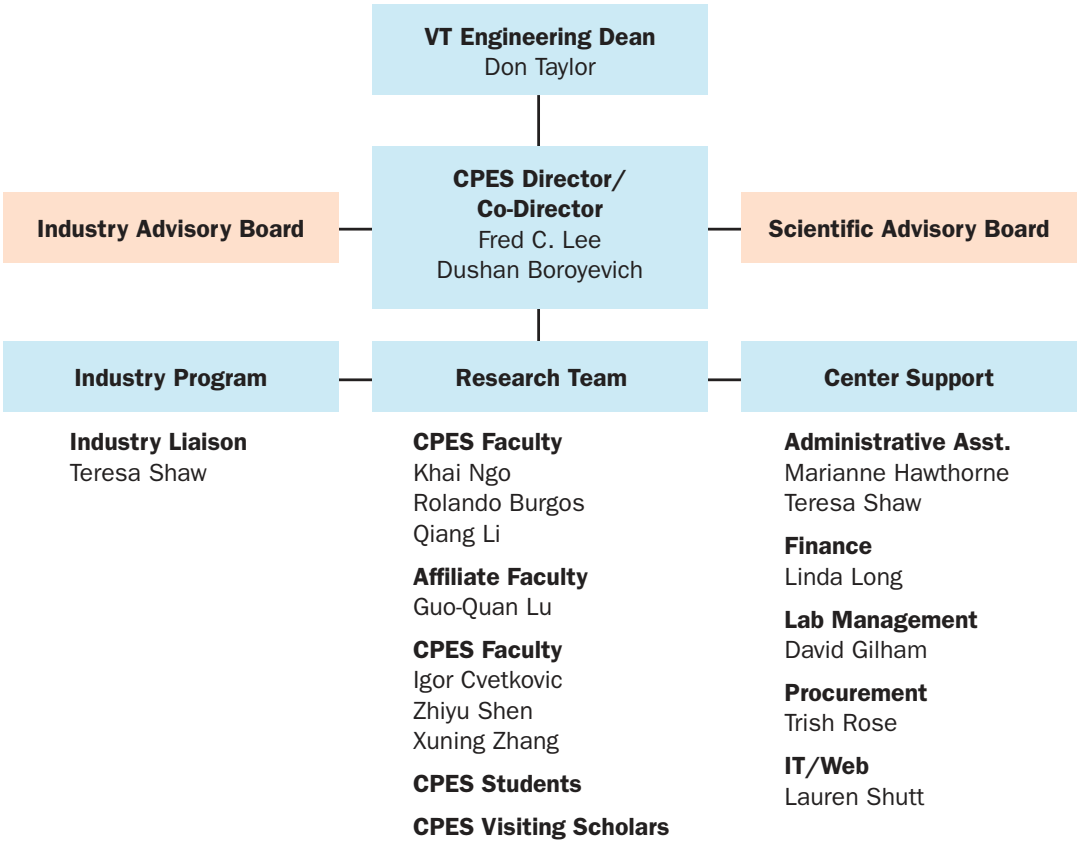
CPES is administratively established as a sub-organization under the College of Engineering. The Center Director, Fred C. Lee, reports to the Dean, and together they identify initiatives to enhance the position and contributions of the Center within the university, the industry, and the world. Dr. Lee is assisted in his role of Director by Co-Director Dushan Boroyevich.

In addition, Dr. Lee and Dr. Boroyevich receive counsel from the CPES Industry Advisory Board (IAB) and the CPES Scientific Advisory Board (SAB).

The Industry Advisory Board represents industry interests and advises the CPES Director on programmatic matters. The board is made up of an elected Chairperson, representatives from all Principal Plus and Principal Members, and Associate Member representation equal to 20% of the total number of Associate Members, or one less than the total number of Principal-level Members. Associate members are elected and serve for two years.

The Scientific Advisory Board reviews the Center's vision and strategic research plan, and offers critiques and guidance regarding the Center's research vision and its programmatic approach to ensure that the Center's research program maintains a focus on its long-term goals.

CPES Organization Management



Resource Needs and Funding

CPES has been a long-standing center, originally established in 1983 as VPEC (Virginia Power Electronics Center). Its continued support is expected to be consistent with the present sources of funding. The Center is supported by both sponsored research, presently making up about $2.4M/year, and industry member support, presently equal to an additional $2.4M/year. Returned overhead also supports the Center.

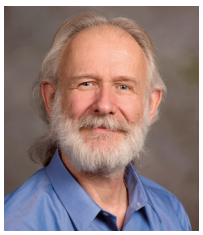
CPES has a Memorandum of Agreement (MOU) for the distribution of overhead. This agreement is reviewed periodically as new opportunities arise. The last MOU was signed by all parties in 2014.

Leadership

Dr. Fred C. Lee is a University Distinguished Professor and Founder and Director of the Center for Power Electronics Systems (CPES), a former NSF ERC. As CPES Director, Dr. Lee leads a program encompassing research, technology development, educational outreach, industry collaboration, and technology transfer. CPES focuses its research on meeting industry needs and allows industry to profit from the Center's research and output. The CPES program enables its principal industry members to sponsor graduate fellowships and provides the opportunity to direct research in areas of mutual interest, as well as the ability to access intellectual properties generated collectively by all industry-funded fellowships on a royalty-free and non-exclusive basis. To date, more than 215 companies worldwide have benefited from the industry partnership program.

Dr. Lee's research interests include high-frequency power conversion, magnetics and EMI, distributed power systems, renewable energy, power quality, high-density electronics packaging and integration, and modeling and control.

Dr. Lee holds 82 U.S. patents, and has published 296 journal articles and 722 refereed technical papers. During his tenure at Virginia Tech, Dr. Lee has supervised to completion 82 Ph.D. and 92 Master's students. In 2012, he became an inaugural member of the Virginia Tech Entrepreneur Hall of Fame, while in 2015 he received the IEEE Medal in Power Engineering. Dr. Lee is a Member of the U.S. National Academy of Engineering, an Academician of Academia Sinica, and a Foreign Member of the Chinese Academy of Engineering.



Dr. Dushan Boroyevich is the American Electric Power Professor at Virginia Tech and CPES Co-Director. He has led numerous research projects in the areas of multi-phase power conversion, electronic power distribution systems, modeling and control, and multi-disciplinary design optimization. He developed a comprehensive geometric approach to the modeling and control of high-frequency switching power converters that is widely used in the analysis, design, and control of multi-phase ac power conversion systems. He has advised 96 successful Ph.D. and Master's students, and has co-authored with them over 816 technical publications and 13 patents.

Dr. Boroyevich is an IEEE Fellow, a recipient of the IEEE William E. Newell Power Electronics Technical Field Award, a recipient of the IEEE Harry Owen Power Electronics Distinguished Service Award, and a past President of the IEEE Power Electronics Society (PELS). He is also the recipient of the Outstanding Achievement Award by the European in Power Electronics Association. He has received six prize paper awards, several awards for excellence in research and teaching at Virginia Tech, and in 2004, the award for Outstanding Achievements and Service to Profession by the European Power Electronics and Motion Control Council.

Dr. Boroyevich was elected to the U.S. National Academy of Engineering in 2014 because of his advancements in the control, modeling, and design of electronic power conversion for electric energy and transportation. In 2016 he received the Kwoh-Ting Li Chair Professor Award at the National Cheng-Kung University, Taiwan.

Power Management Consortium Nuggets

Resonant Converter with Coupling Independent Resonance for Wireless Power Transfer Application

High-Frequency High-Efficiency GaN-Based Interleaved CRM Bidirectional Buck/Boost Converter with Inverse Coupled Inductor

Omnidirectional Wireless Power Transfer for Portable Devices

A Three-Terminal Switch Model of Constant On-Time Current Mode with External Ramp Compensation

An Enhanced Adaptive Frequency-Locked Loop for Variable-Frequency Control

Small-Signal Analysis of the Sigma Converter

Small Signal Analysis of V^2 Control Using Equivalent Circuit Model of Current Mode Controls

A Novel WBG-Based Bi-Directional On-Board Charger

High-Frequency Active-Clamp Flyback Converter with GaN Devices for Low-Power AC-DC Adapter

Design of GaN-based MHz Totem-pole PFC Rectifier

Digital-Based Interleaving Control for GaN-based MHz CRM Totem-pole PFC

High-Frequency Transformer Design for Modular Power Conversion from Medium Voltage AC to 400 V DC

A Novel PCB Winding Transformer with Controllable Leakage Integration for a 6.6 kW 500 kHz High Efficiency High Density Bi-Directional On-Board Charger

High-efficiency High-power-density 380 V/12 V DC/DC Converter with a Novel Matrix Transformer

Modeling Resonant Converter in a Rotating Coordinate

A High-Frequency Small-Signal Model for Inverse-Charge Constant On-time (IQCOT) Current-Mode Control

High-Efficiency High-Density CRM Rectifier/Inverter for WBG-Based On-Board Charger

Resonant Converter with Coupling Independent Resonance for Wireless Power Transfer Application

One crucial challenge of resonant converter design in wireless power transfer (WPT) applications is the variable coupling between transmitter coil and receiver coil. The most efficient operating point of the resonant converter is normally at the system resonant frequency. If the resonant frequency is dependent on coupling, it is difficult to stay at optimal point when the coupling between transmitter and receiver is variable. Therefore, the resonant converter with coupling independent resonance is highly attractive in the WPT application. Another challenge of the resonant converter design is a zero voltage switching (ZVS) operation of the switching device. The switching frequency recommended by Rezence, a wireless power transfer standard, is 6.78 MHz. In such high switching frequency, it is detrimental for a switching device to operate without ZVS operation.

The LCCL-LC resonant converter, as shown in Fig. 1, is formed by adding two capacitors (C_p and C_s) in LCL resonant converter. C_s is added first to form a coupling independent resonant frequency f_o. The formula of resonant frequency is shown in Eq. 1, in which L_s is the self inductance of the receiver coil. Self inductance is independent of coupling, therefore, the resonant frequency is independent of coupling between the transmitter and receiver coils. C_p is added to make sure that input impedance at f_o is inductive, which is necessary for the ZVS operation of the primary switching device. From a gain characteristics point of view, C_p creates a parallel resonant frequency (f_1) lower than f_o. Then, f_1 improves the ZVS region of this converter so it is similar to the LLC resonant converter.

The gain characteristics of the LCCL-LC resonant converter in different coupling conditions are shown in Fig. 2. In this figure, it is easy to see that f_o is independent of the coupling condition, which means that this converter can always operate at an optimal point in variable coupling cases. Besides, ZVS operation in the blue region can be guaranteed due to existence of f_1. Therefore, the LCCL-LC resonant converter is very suitable for WPT applications and more topologies with similar characteristics will be provided in the full paper.

Eq. 1. $$f_o = \frac{1}{2\pi\sqrt{L_r C_r}} = \frac{1}{2\pi\sqrt{L_s C_s}}$$

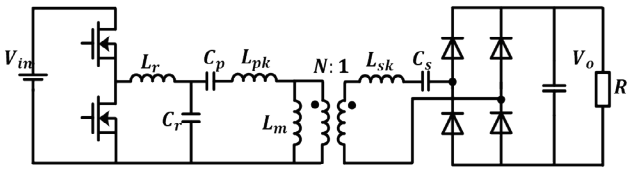


Fig. 1. LCCL-LC resonant converter.

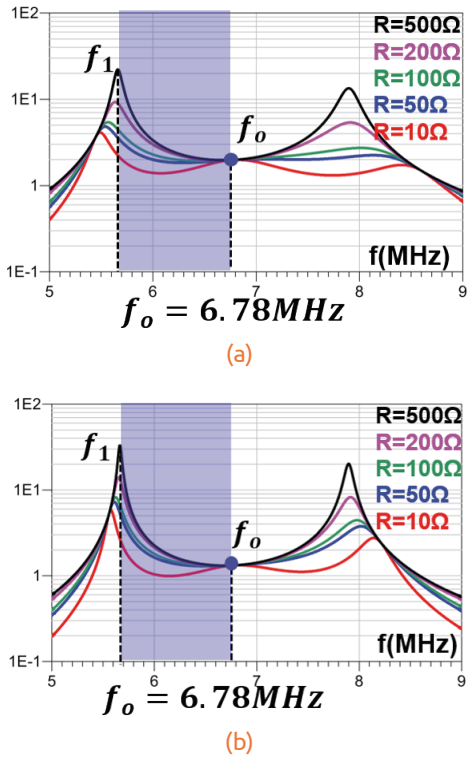


Fig. 2. Voltage gain characteristics in different coupling coefficient (k). (a) k=0.4 (b) k=0.2

High-Frequency High-Efficiency GaN-Based Interleaved CRM Bidirectional Buck/Boost Converter with Inverse Coupled Inductor

The bidirectional buck/boost converter is widely used in the power electronics system due to its simplicity and high efficiency. Examples include an on-board charger/discharger for plug-in hybrid electric vehicles and an interfaced converter for the energy storage in dc-based nano grids. A conventional silicon device-based bidirectional buck/boost converter is usually intended to be operated in discontinuous current mode (DCM) in order to alleviate the reverse recovery issue and use a small inductor size. However, the DCM operation largely increases turn-off loss because the main switch is turned off at least twice during the load current. As a result, it is hard to push the switching frequency to hundreds of kHz due to the power loss consideration.

In recent years, the GaN HEMT has emerged as a promising device for high frequency, high efficiency, and high density power conversion due to a better figure of merit than comparable Si and SiC transistors. The switching frequency has been continuously pushed up several MHz to both reduce passive components size and increase power density. Previous research concludes that the turn-on switching loss is dominant due to reverse recovery charge or junction capacitor charge of the free-wheeling device at hard-switching condition. On the other hand, the turn-off loss is negligible because of the intrinsic current source driving mechanism that existed in the cascode structure. These important switching characteristics imply that zero-voltage-switching (ZVS) is still desired for GaN devices in the high frequency application while the turn off current is no longer a big concern for cascode GaN devices.

The critical current mode (CRM) operation is the most simple and effective way to achieve ZVS and is widely used in medium-low power applications. The conventional CRM operation has some limitations in high frequency and requires further improvement. The concept of the coupled inductor has been applied successfully in the interleaved voltage regulator modules for the improvement of the efficiency and transient response. Two-phase buck/boost converters with a coupled inductor prototype are shown in Fig. 1(a). A comparison between the coupled and non-coupled inductor is shown in Fig. 1(b) demonstrating the significant reduction of the inductor size with coupling. The key waveforms are shown in Fig. 2. The resonant period in the CRM reduces with the coupled inductor when compared to the non-coupled condition, which is beneficial for high frequency operation. The soft-switching range and the circulating energy are both improved with the coupled inductor in CRM. The coupled inductor prototype efficiency is 98.5% at 1 MHz, which is 0.5% higher than the non-coupled one.

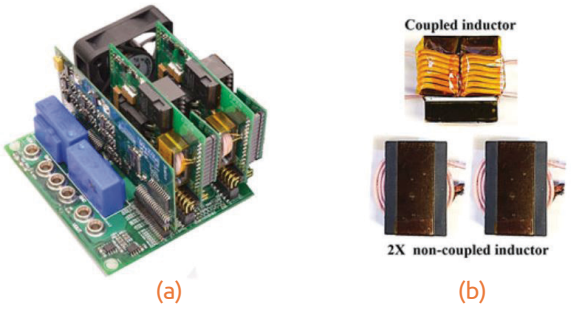


Fig. 1. Prototype and inductor comparison.
(a) Two-phase interleaved buck/boost converter prototype.
(b) Comparison of coupled and non-coupled inductors.

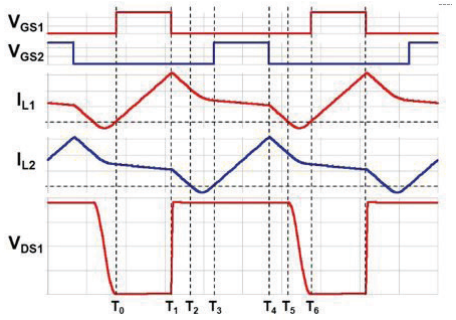


Fig. 2. Key waveforms.

Omnidirectional Wireless Power Transfer for Portable Devices

The wireless power transfer (WPT) product market is currently increasing rapidly due to its convenience. In the large growing market, low power devices, such as consumer electronics and mobile devices, share a large portion. However, the majority of wireless power transfer platforms currently on the market are directional, which means devices can only be charged efficiently in one orientation. For example, a smart phone cannot be charged quickly in a planar charging surface when it is vertical to the surface. Therefore, an omnidirectional wireless power transfer platform is highly attractive.

The field direction preference for a portable device is first analyzed. Due to mechanical reasons, a small portable device will drop into the bottom of a charging platform. Since the orientation is very flexible for the small portable device, the omnidirectional field prefers to be in the bottom of the charging platform. On the other hand, only planar devices can lay on their side face. Therefore, a field perpendicular to the surface is preferred for planar devices in side face. Then omnidirectional wireless power transfer platform proposed by Intel and the City University of Hong Kong is analyzed with FEA simulation and a numerical model. Unfortunately, there is no omnidirectional field in the bottom of the two charging platforms.

A new transmitter coil structure to achieve an omnidirectional field in the bottom and perpendicular field at side face is proposed, as shown in Fig 1. With this new coil structure, it is easy to understand that the field is perpendicular to the surface in side face. On the other hand, the omnidirectional field distribution in the bottom of proposed transmitter coil structure can be induced with modulation excitation current. The transmitter coil structure is implemented, as seen in Fig. 2. They are driven by three sets of 6.78 MHz LCL resonant converters. The excitation current of these three sets of coils is modulated excitation current. With this system, field distribution in the bottom at different time instants is shown in Fig. 3 by FEA simulation. Also, the omnidirectional field can be measured with a near-field probe in the experiment.

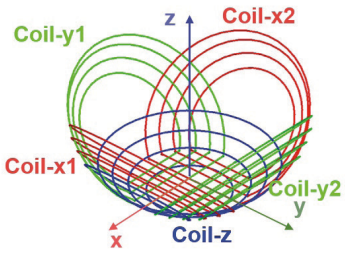


Fig. 1. Transmitter Coil Structure.

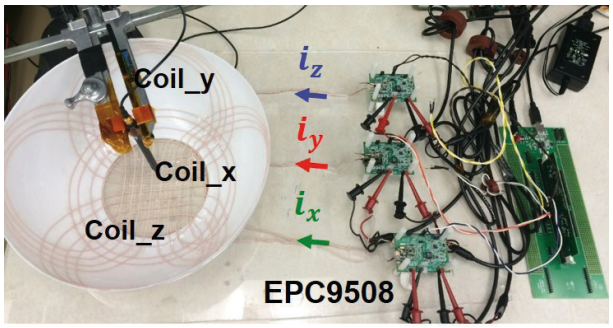


Fig. 2. Experiment Setup.

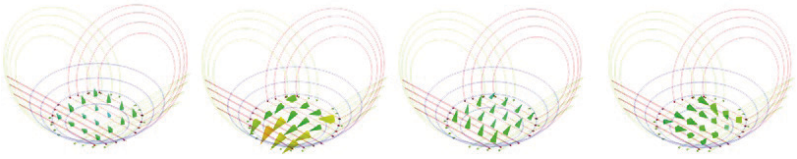
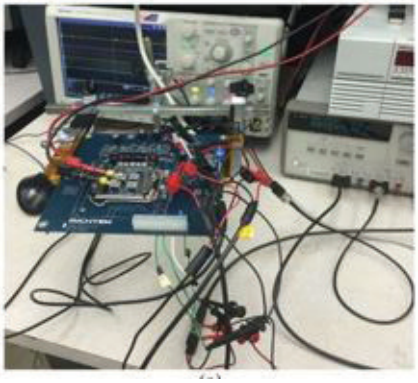


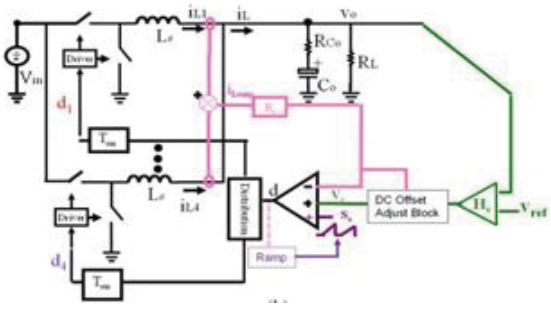
Fig. 3. Field distribution in bottom of charging platform at different time instants.

A Three-Terminal Switch Model of Constant On-Time Current Mode with External Ramp Compensation

Multiphase constant on-time current-mode control based on a pulse distribution structure is widely used in voltage regulator applications for microprocessors. To minimize the ripple cancellation effect, external ramp compensation is used in commercial products. However, using an external ramp will introduce dynamics to the system, and if this is not taken into consideration, the stability margin will suffer. We propose a simple equivalent circuit model based on a three-terminal switch concept, which considers the effect of the external ramp by adding an additional R–L branch. The equivalent circuit model can be reduced to a previous unified three-terminal switch model when the external ramp is zero, and can be reduced to a model of constant on-time voltage mode control when the external ramp is much larger than the inductor current ramp. The proposed three-terminal switch model is a complete model, which can be used to examine all transfer functions, and is accurate up to half of the switching frequency. The model is verified by SIMPLIS simulation and experimental measurement.

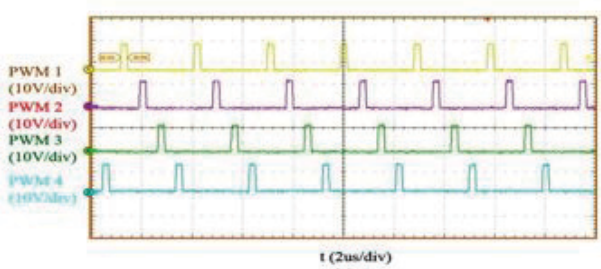


(a)

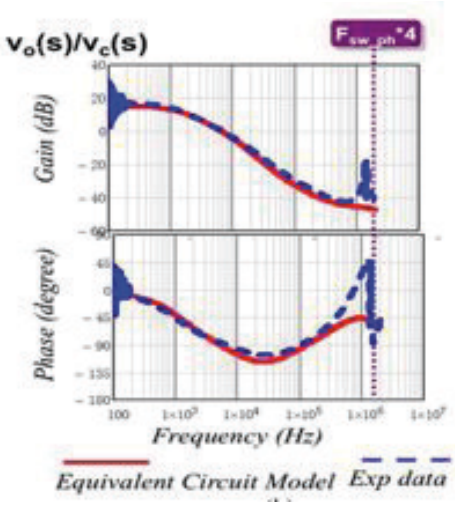


(b)

Fig. 1. (a) Experimental setup and (b) Simplified diagram for RT8859M Demo Board.



(a)



(b)

Fig. 2. Experimental verification for case II: D =0.1 (V_{in} =12V, V_o = 1V): (a) Steady-state waveform and (b) Verification of control-to-output voltage transfer function.

An Enhanced Adaptive Frequency-Locked Loop for Variable-Frequency Control

Currently, variable-frequency current-mode controls are widely used in voltage regulators (VRs) for their higher light-load efficiency, better small-signal properties and better transient response than fixed-frequency current mode controls. One major challenge for variable-frequency control is that the switching frequency (f_{sw}) varies significantly according to the duty cycle. This variable, f_{sw}, creates unpredictable noise in the system that is difficult to filter out, and hence variable-frequency current-mode control is not preferred for many frequency-sensitive applications. While using a form of variable-frequency control, such as constant on-time control (COT), for frequency-sensitive applications, people use 'adaptive COT' control, which slowly changes the T_{ON} with the duty cycle during steady-state operation to keep the steady-state frequency constant. The V_{IN}/V_{REF} feed-forward method and the phase-locked loop (PLL) method are very widely used to realize adaptive COT control. Normally, the V_{IN}/V_{REF} feed-forward method is very simple and fast, but naturally suffers from inaccuracy for its feed-forward approach. Meanwhile, the PLL method is very accurate but suffers from complicated additional loop adjustments. Therefore, this work proposes a new accurate but simple frequency control loop for variable frequency control. We also propose two additional techniques for performance improvements using the proposed method; namely, a faster loop settling time by using feed-forward signal and better loop stability with duty cycle variation by adding adaptive loop gain control.

A simple new frequency-locked loop (FLL) is proposed to work with the previously proposed IQCOT control; the conventional FLLs are more complex and not optimized for converter applications. This simplified and optimized FLL is shown inside the box marked "Frequency Variation Control" in Fig. 1, and its details of operation are described in the full conference paper. As the feedback loop bandwidth is low, it does not interact with converter loop, and the settling time for the frequency change is large. To improve this case, in addition to the simplified FLL feedback loop, V_{IN} and V_{REF} feed-forward paths are also added to the FLL (shown by the red line in Fig. 1). This way the frequency change settling time can be reduced significantly, as shown in Fig. 2. The bandwidth of the FLL also changes with the duty cycle, as shown in Fig. 3, and by adopting proposed adaptive gain control, the bandwidth has been kept fixed with the duty cycle change, as shown in Fig. 4.

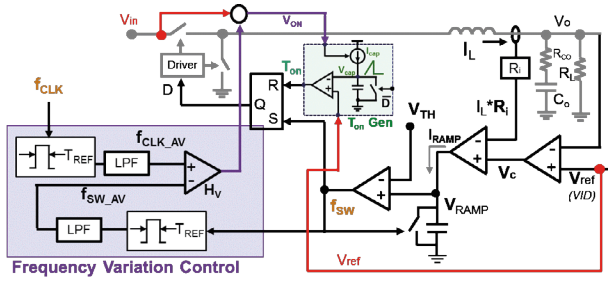


Fig. 1. Proposed FLL with 'feed-forward+feedback' control.

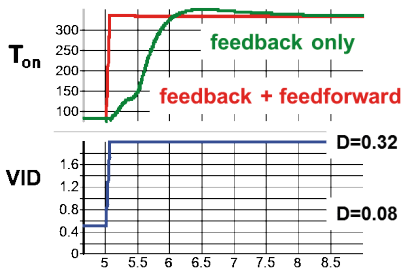


Fig. 2. Faster settling time by proposed 'feed-forward + feedback' control loop in FLL.

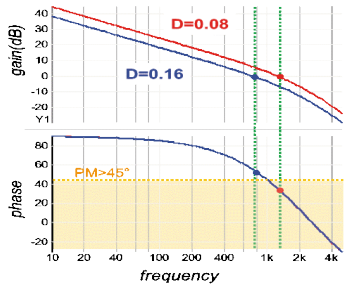


Fig. 3. FLL bandwidth variation with D.

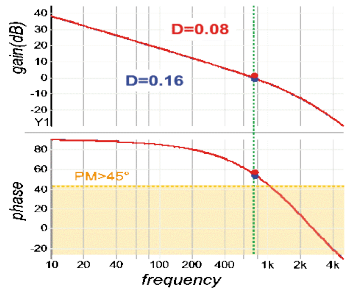


Fig. 4. Proposed adaptive gain for constant bandwidth with D.

Small-Signal Analysis of the Sigma Converter

For the new generation of server voltage regulators (VRs), Intel is employing the use of 48V to 1V boards to improve efficiency. Conventionally, a two-stage solution is used for higher efficiency than a single-stage solution. For 48V to 1V VRs, a quasi-parallel topology, the sigma converter, is shown to have high efficiency and high power density. In order to design the sigma converter for VR applications, the large-signal performance as well as the small-signal behavior of the sigma converter must be studied. In this paper, the small-signal model of the sigma converter is derived and examined for voltage regulator (VR) applications.

The sigma converter is composed of a fixed-frequency LLC running at the resonant frequency and a buck converter, with the inputs of the converters connected in series and the outputs of the converters connected in parallel, as shown in Fig. 1. The small-signal model of the sigma converter can be obtained by connecting the models of its components in the quasi-parallel configuration shown in Fig. 2. For the fixed-frequency LLC running at resonant frequency, a transformer with turns ratio n:1 and an equivalent inductance is used. For the buck converter, the three-terminal switch model is used.

The output of the VR is required by Intel to follow a specific load-line during steady-state for server applications. In order to achieve an accurate load-line, a constant output impedance is needed. Fig. 3 shows the ideal output impedance of a design with parameters of V_{in1}=40V, V_{in2}=8V, V_o=1V, f_o=f_{s_LLC}=1MHz, f_{Buck}=2MHz, n=40, C_r=110nF, L_r=192nH, L_m=22µH, C_{in1}=400nF, C_{in2}=2.1µF, C_o=862µF, and R_L= 12.5 mΩ. From the Bode plot, two double-poles and a double-zero are observed. To achieve a constant output impedance with the sigma converter, the converter components must be carefully designed before control designs are considered.

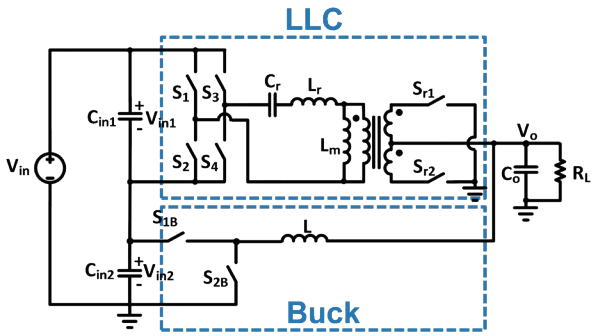


Fig. 1. Circuit representation of the sigma converter.

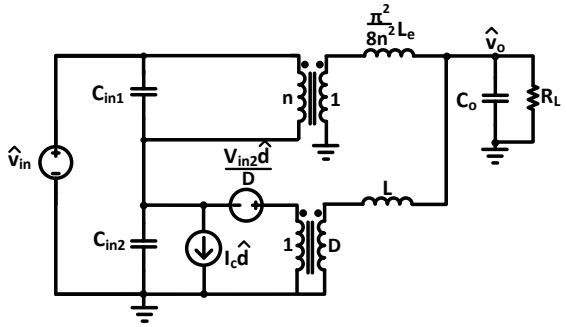


Fig. 2. Small-signal model of the sigma converter.

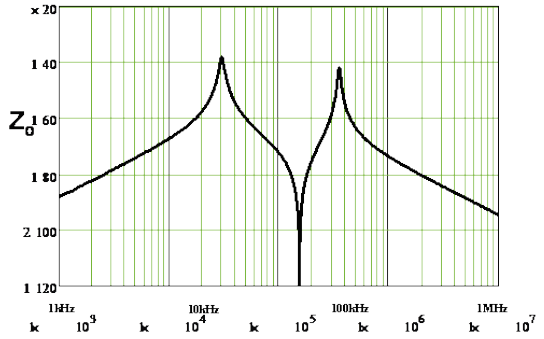


Fig. 3. Output impedance of the ideal sigma converter.

Small-Signal Analysis of V² Control Using Equivalent Circuit Model of Current Mode Controls

In V² control, the direct feedback contains the information of both state variables. In this paper, by separating current feedback and capacitor voltage feedback, an equivalent circuit of V² control based on the equivalent circuit of current mode control is proposed. The proposed equivalent circuit provides a clear physical insight of V² control and can be interpreted as an advanced implementation of current mode control with a proportional voltage feedback, as well as an additional load current feedback. The load current feed-forward dramatically reduces the output impedance. The model is extended to enhanced V² control. The proposed equivalent circuit model is applicable to both variable frequency modulation and constant frequency modulation.

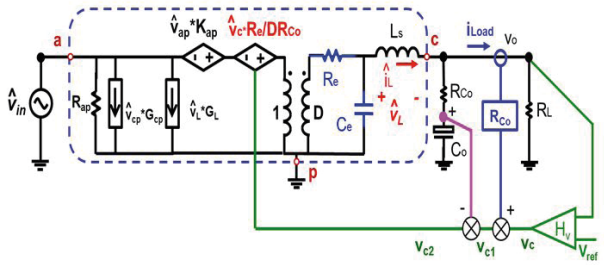


Fig. 1. Small-signal equivalent circuit of V² Control.

The direct output voltage V_o feedback consists of inductor current, capacitor voltage and load current feedback. The inductor current feedback loop does not have a low pass filter, so all the sideband frequencies (f_{sw}-f_m, f_{sw}+f_m, etc.) are fed back to the modulator. Other feedbacks are simpler: for a voltage regulator, the impedance of the capacitor branch is much smaller than that of the load resistor at $f > f_{sw}/10$. Assuming the capacitor ESR zero is well below half switching frequency, the impedance of ESR is much larger than that of intrinsic capacitance, so the sideband components at v_{cap} are overwhelmed by the ESR voltage.

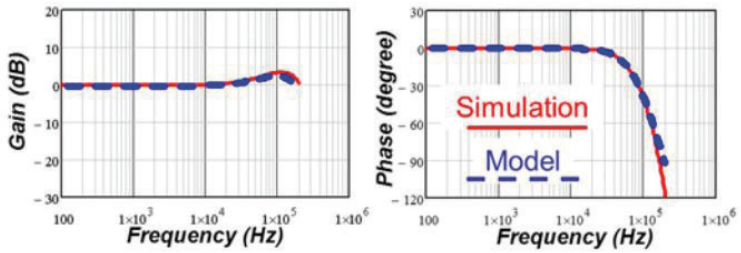


Fig. 2. Control-To-Output transfer function verification.

According to the analysis above, it is reasonable to consider all the sideband frequency feedback effect in the inductor current loop, but only consider fundamental frequency in the capacitor voltage and load current feedback. Inductor current loop is a highly nonlinear entity. It potentially has sub-harmonic instability. A three-terminal switch equivalent circuit model based on the result of a describing function derivation accurately predicts the small signal properties of this nonlinear entity. Substitute the closed current loop and the PWM switch by the equivalent circuit mode. The proposed equivalent circuit model of V² control is shown in Fig. 1 and the simulation verification of the proposed model is shown in Fig. 2.

A Novel WBG-Based Bi-Directional On-Board Charger

Today's on-board charger for hybrid electrical vehicles usually consists of two stages, an ac/dc stage, which converts the ac line input to a 400 V dc bus, and an isolated dc/dc stage, which regulates the 400 V dc bus to 250 V~450 V battery voltage. With the maturity of wide-band-gap devices, there is an opportunity to push the switching frequency of the on-board charger to several hundred kHz, bringing the efficiency and power density to a new level.

However, the large battery voltage range posts a great challenge to the design of the second stage, which is a CLLC bidirectional resonant converter. In order to guarantee the second stage working at its optimized point, four different candidate structures are evaluated and compared in terms of efficiency. Finally, a variable 500 V-840 V dc-link voltage with mixed wide-band-gap devices, as shown in Fig. 1 is proposed. It is shown that the proposed structure has the smallest gain range, resulting in the smallest frequency range and lowest loss. In order to handle the high dc-link voltage, 1.2 kV SiC devices are used in the PFC stage and the primary side of the dc/dc stage. Since the battery voltage is still low, 650 V GaN devices can be used as secondary side synchronized rectifiers.

The benefit of the proposed variable dc-link structure is to keep the switching frequency of the dc/dc stage at resonant frequency so that high efficiency can be maintained over the entire battery voltage range. This dc transformer (DCX) concept has been proved to be very efficient. However, in applications like battery chargers, this concept has the problem of a very large output current ripple.

In order to solve this problem, a two-stage combined control strategy is proposed, as shown in Fig. 2. The outer loop of the PFC stage senses the battery voltage as well as the dc-link voltage, and by using a regulator, the output power is controlled so that the dc-link voltage always tracks the battery voltage, making sure the gain range of the CLLC resonant converter is close to unity. In addition, this control strategy can be extended to discharging mode, including both grid-tied mode and stand-alone load mode.

A 6.6 kW 500 kHz prototype is built to verify the proposed two stage system structure and control strategy as shown in Fig. 3. Over 96% total efficiency can be achieved over the entire battery voltage range with power density over 37 W/in^3, which is far beyond current practice.

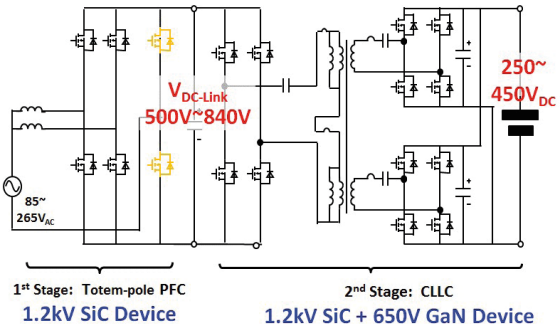


Fig. 1. Proposed two-stage system structure with variable dc-link voltage.

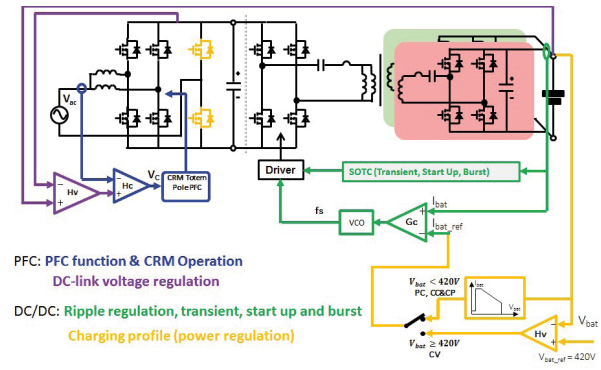


Fig. 2. Proposed two-stage control strategy.

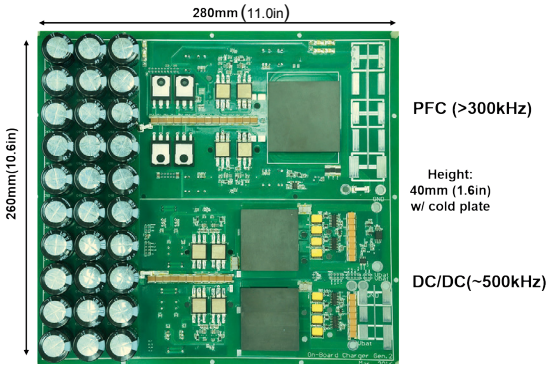


Fig. 3. Generation 2 prototype of the two-stage on-board charger.

High-Frequency Active-Clamp Flyback Converter with GaN Devices for Low-Power AC-DC Adapter

Universal ac-dc adapters for consumer electronics represent one of the biggest market sectors for power supplies, in terms of both volume and revenue. While progress on all forms of mobile devices is moving at an amazing rate, with ever-increasing performance and shrinking size and weight, their adapter counterparts continue to be relatively bulky and are capable of only meager power density. Most of the adapters in mass production today operate at relatively low frequencies (<200 kHz) and with an efficiency below 92% and power density below 12W/in^3. A few industry pioneers, such as Finsix, have tried to develop high-density universal adapters with different topologies operating at higher frequencies, and have achieved encouraging results in terms of power density, reaching 21W/in^3, which is the best in the market. However, the efficiency over a wide input line range can't be optimized due to topology limitations.

The emerging wide-band-gap devices, such as Gallium Nitride (GaN) devices, have a much lower gate charge and lower output capacitance than traditional devices. Therefore, these devices are capable of operating at a considerably higher switching frequency while maintaining high efficiency, and make it possible to shrink the size of the adapter significantly.

Using active-clamp flyback topology, CPES has developed a 65W adapter, which is shown in Fig. 1, that operates in the 1MHz frequency range with GaN devices, and can achieve 93.5% peak efficiency and 25W/in^3 in power density (including the case). For power levels higher than 75W in offline applications, CPES also developed a two-stage 150W adapter by using a MHz totem-pole PFC as the first stage, and a MHz LLC dcX as the second stage. The LLC transformer is PCB wound and integrated with a shielding layer to reduce the CM noise. An EMI filter with only one stage is good enough to attenuate the EMI noise and meet the standard. This prototype can achieve 95.1% peak efficiency and 35W/in^3 in power density, including the case, which is three times that of the state-of-the-art product.

In 2013, Intel's fourth-generation microprocessor, Haswell, integrated a voltage regulator module into the internal CPU. These fully integrated voltage regulators (iVR) can achieve more precise power control and decrease power consumption by 40-60%. The second-generation iVR has been successfully used in Broadwell microprocessors developed by Intel in 2015, which can save more power than the first generation microprocessors. As a result, a wall adapter with 45W or below will power most laptop and notebook computers, and the 45W adapter has become the mainstream for laptop power supplies. By following the design procedure of the 65W adapter, a MHz prototype of a 45W adapter with 20V/2.25A output was built and can achieve 93% peak efficiency. Its power density is 25W/in^3 including the case. A picture of the prototype is shown in Fig. 2. Meanwhile, based on the same prototype, different output conditions (15V/3A) with closed-loop control were tested under a lower frequency range, and the prototype can also achieve very high efficiency under these conditions. Fig. 3 shows the efficiency curves of the prototype compared with those of the state-of-the-art product, and a roadmap for adapters is shown in Fig. 4.

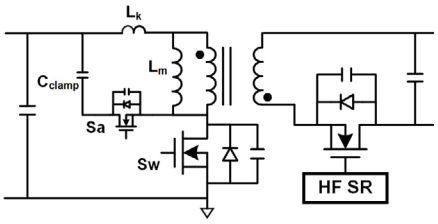


Fig. 1. Active clamp flyback converter.

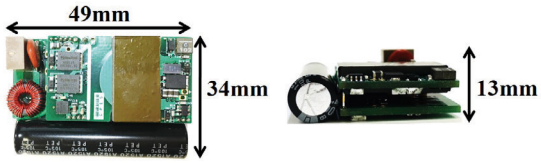


Fig. 2. MHz 45W adapter prototype.

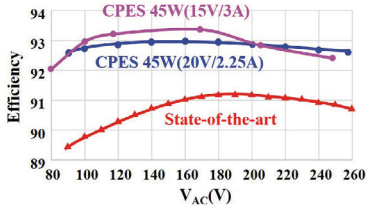


Fig. 3. Efficiency of CPES 45W adapter compared with the state-of-the-art product.

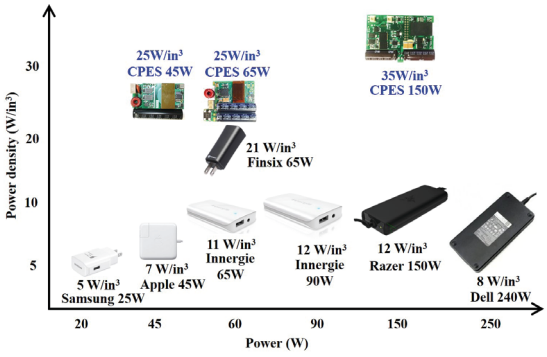


Fig. 4. Adapter roadmap.

Design of GaN-based MHz Totem-pole PFC Rectifier

With the advent of 600V gallium-nitride (GaN) power semiconductor devices, the totem-pole bridgeless power factor correction (PFC) rectifier, which was nearly abandoned topology, has suddenly become a popular solution for applications like front-end converters in server and telecommunication power supplies. This is mostly attributed to the significant performance improvement of the GaN high-electron-mobility transistor (HEMT). When compared to the silicon (Si) metal–oxide–semiconductor field-effect transistor (MOSFET), it has better figure-of-merit and a significantly smaller body diode reverse-recovery effect.

The cascode GaN HEMT is applied in the totem-pole PFC rectifier while pushing the operating frequency to above 1 MHz. Several important issues, which are less significant at low frequencies, are emphasized at high frequencies, and corresponding solutions are proposed and experimentally verified.

In this research, the advantages of the totem-pole PFC rectifier are summarized at first, while the differences between hard-switching and soft-switching and between the Si MOSFET, and the GaN HEMT are illustrated in second. After that, detailed design considerations are presented, including the ZVS extension to solve the problem of switching loss caused by non-ZVS valley switching; variable on-time control to improve the power factor, particularly the zero-crossing distortion caused by traditional constant on-time control; and interleaving control to cancel the input current ripple. The volume of the DM filter is reduced significantly by pushing the operating frequency to several MHz and the use of multi-phase interleaving.

A 1.2 kW two phase interleaved totem-pole PFC prototype is demonstrated with 220W/in^3 power density and 99% efficiency. All proposed functions with closed-loop control are implemented by a 120 MHz MCU.

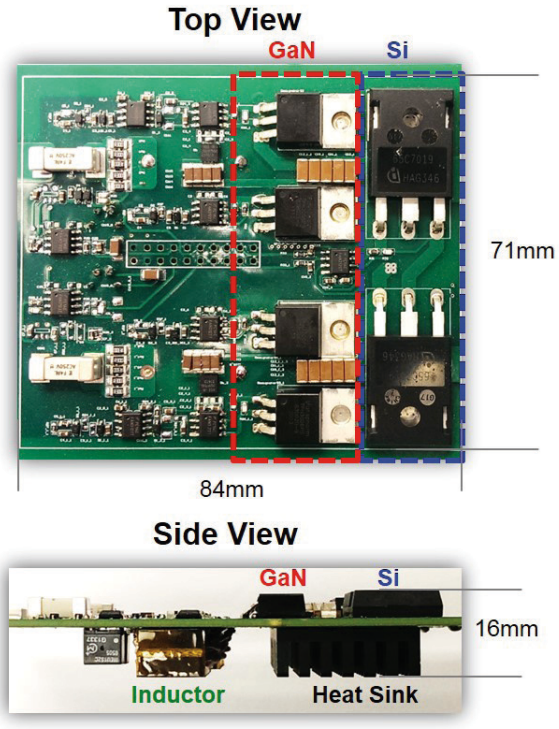


Fig. 1. Prototype of interleaved 1.2 kW MHz totem-pole PFC.

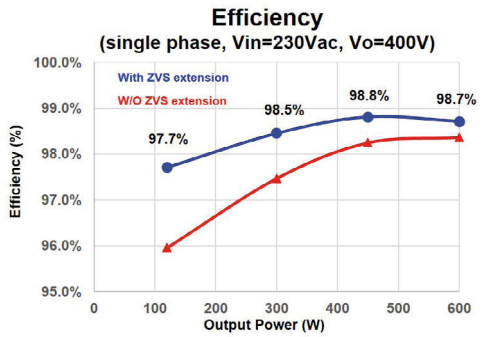


Fig. 2. Tested efficiency.

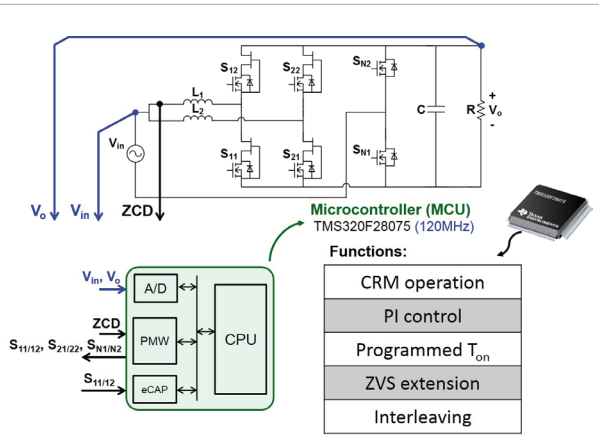


Fig. 3. MCU-based digital control implementation.

Digital-Based Interleaving Control for GaN-based MHz CRM Totem-pole PFC

The totem-pole bridgeless power-factor-correction (PFC) circuit is becoming popular. This is attributed to the emerging high voltage gallium-nitride (GaN) devices. According to the paper, the soft switching operation is important in order to achieve a very high MHz frequency operation for 600 V GaN devices. Critical conduction mode (CRM) is the simplest way to achieve soft switching; and when applied to a boost-type PFC circuit, it is easy to achieve a good power factor with a CRM operation.

A 1.2 kW 1-3 MHz GaN-based CRM totem-pole PFC was built with close to 99% peak efficiency and more than 200 W/in^3 power density. In addition, the MHz impact of the PFC is not limiting but has an even more significant impact on the input filter design. According to a previously published paper, when the switching frequency is higher, (e.g. above 400 kHz), the filter size becomes smaller. We demonstrated that from 100 kHz to 1 MHz, the DM filter is simplified from 2 stages to 1 stage and the volume is reduced by 50%. It also claims that if a two-phase PFC is interleaved with a 180 degree phase shift then another 50% volume reduction is expected.

The challenge of interleaving control for a CRM PFC is that the nature of the circuit is variable frequency operation. For a given input and load condition, the frequency varies 3-5 times in a half line cycle. For different input or load conditions, the frequency range varies as well. According to literature, there are generally two categories of interleaving control methods proposed for the variable frequency CRM PFC: closed-loop interleaving and open-loop interleaving. For low frequency, both methods work well in maintaining a minimal value in the phase error. However, when the frequency is pushed 10 times higher to multi-MHz, the interleaving control becomes a new challenge.

In this research, the impact of interleaving control on a MHz CRM totem-pole PFC and DM filter is introduced at first. The performance comparison between closed-loop interleaving and open-loop interleaving for MHz totem-pole PFC is then discussed. The optimization and experimental results of open-loop interleaving is also presented. The conclusion is a less than 3 degree phase error is accomplished with open-loop interleaving and a 60 MHz MCU. Finally, the stability analysis of open-loop interleaving is elaborated.

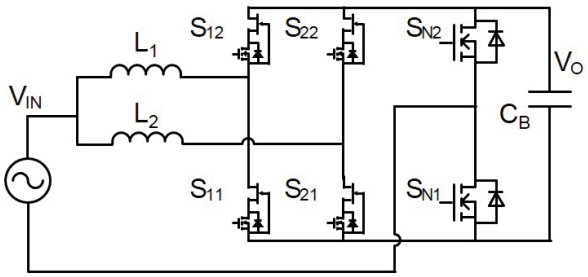


Fig. 1. Circuit diagram of two-phase interleaved totem-pole PFC with cascode GaN devices.

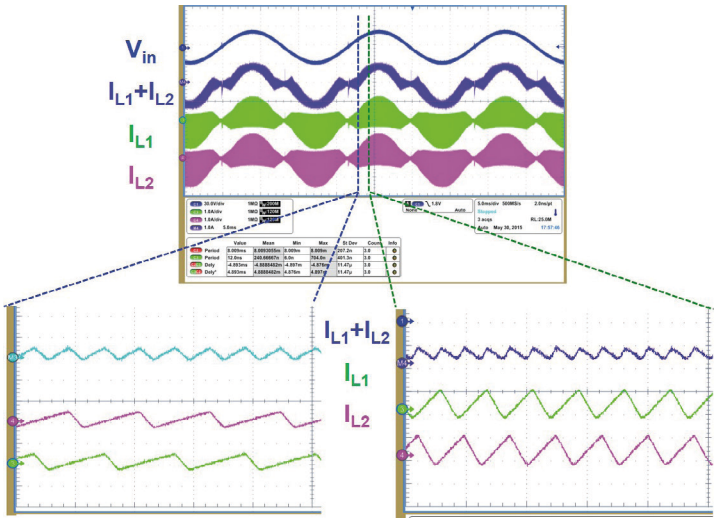


Fig. 2. Experimental waveform of open-loop interleaving.

High-Frequency Transformer Design for Modular Power Conversion from Medium Voltage AC to 400 V DC

Due to the increasing use of cloud computing and big data, the power consumption of data centers alone will reach 10% of the total electrical power consumption in the world by 2020. Considering the booming data center load development and the high cost of copper, conduction loss due to low voltage (480VAC) power distribution outside the server hall needs to be reduced. We propose to utilize a medium voltage 4.16 kV ac line as the distribution bus within the data center facilities, as shown in Fig. 1. A medium voltage of 4.16 kV is sent into each server hall. Inside each server hall, a solid-state transformer (SST) in a cascade configuration is employed to convert the medium voltage directly to 380V dc. The structure of the proposed SST is shown in Fig. 2. Five cascaded full bridges handle the high input voltage and achieve power factor correction with low switching frequency, while a high-frequency isolated dc/dc converter follows to convert 800V dc to 380V dc

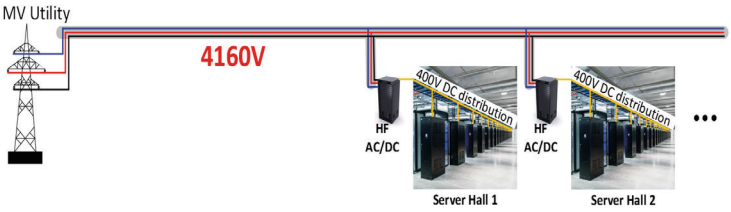


Fig. 1. Proposed Power architecture for future data centers.

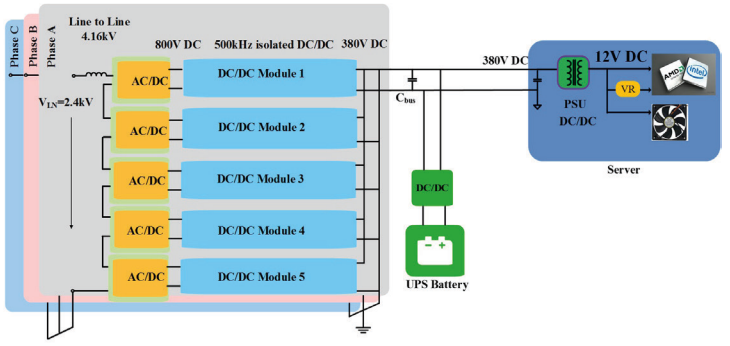


Fig. 2. Three Phase Solid State Transformer (SST) System.

With the advent of SiC and GaN devices, we propose to operate the dc/dc stage at an unprecedented high frequency: 500 kHz, which is 25 times higher than industry state-of-the-art SSTs. At 500 kHz, the selection of WBG devices and converter topologies are critical. A novel bidirectional CLLC resonant converter with a power rating of 15 kW, instead of the popular back-to-back connected dual active bridge, is used to reduce switching loss and guarantee soft switching under all conditions.

For such a 4160 V ac to 380 V dc system, insulation is critical for the entire system. We propose to use a sectionalized coil with a UU core structure to guarantee enough clearance and creepage distance between the primary and secondary windings. Fig. 3 shows a prototype of the high-frequency transformer with medium voltage isolation. The tests show that it can pass a lightning impulse test of 30 kV, applied voltage testing of 12 kV, and partial discharge test of 5.4 kV, which are the standard testing requirements of the IEEE and IEC for a 4.16 kV isolation application.

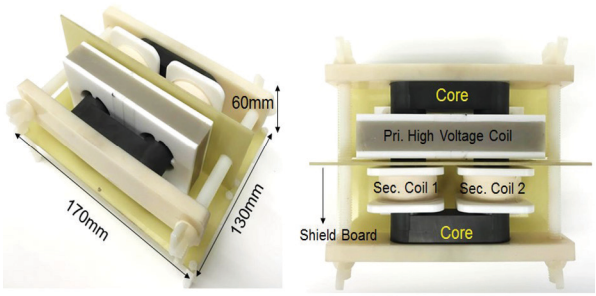


Fig. 3. High frequency transformer with medium voltage isolation.

A Novel PCB Winding Transformer with Controllable Leakage Integration for a 6.6 kW 500 kHz High Efficiency High Density Bi-Directional On-Board Charger

Plug-in electrical vehicles (PEV) or plug-in hybrid electrical vehicles (PHEV) draw more and more attention due to the increasing concerns regarding the fuel cost and air pollution. Each PEV or PHEV has a rechargeable battery that can be restored to full charge by plugging into an external electrical source. One crucial challenge of PEV's commercialization is the demand for a lightweight, compact, and efficient on-board charger system. The state-of-the-art level-2 on-board charger products are majorly Si-based design. They operate at less than 100 kHz switching frequency, have only 3~12 W/in^3 power density and at most 92~94% efficiency. The emerging wide-band-gap devices provide the enabling technology to realize bidirectional operation and dramatically increase the switching frequency as well as the efficiency of power electronics converters. The improvement becomes more significant if soft switching techniques are adopted.

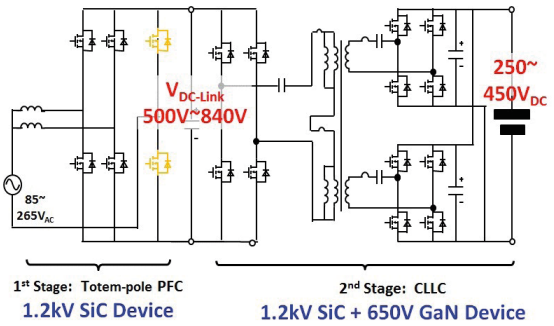


Fig.1. System structure of the proposed two stage on-board battery charger.

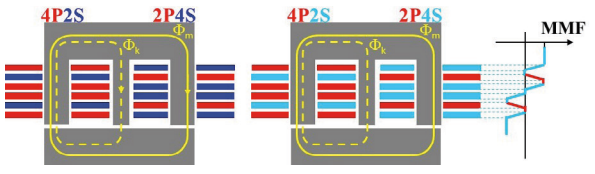


Fig. 2. Proposed PCB winding based transformer with leakage integration.

A two stage on-board charger structure with variable dc-link voltage is proposed as shown in Fig. 1, using bridgeless totem-pole PFC as the first stage and the CLLC resonant converter as the second stage. Due to the variable dc-link operation, the gain range requirement of the CLLC resonant converter is greatly reduced. For the output side, two sets of full bridge rectifiers are used to handle the high charging current. A PCB winding based transformer based on a split core is proposed so that only a 6-layer PCB is needed to realize a 12:6:6 turns ratio. Also, a novel EI core structure is used to help achieve the desired magnetizing inductance and leakage inductance, as shown in Fig. 2. By using the center post as the leakage path, leakage inductance and magnetizing inductance can be controlled by changing the gap of the center and outer posts. With leakage integration, both the primary and secondary side resonant inductance are realized by the leakage inductance of the transformer. A transformer reluctance model is built to help achieve the target inductance. Also, a loss model based on 2D FEA simulation and rectangular extension of Steinmetz's equation is built to get the winding loss and core loss of the proposed transformer. Based on this loss model, a design procedure is provided to optimize the transformer loss.

A 6.6 kW 500 kHz prototype of the proposed CLLC resonant converter with PCB integrated transformer is built. The testing results show that the proposed transformer structure can achieve the required leakage inductance and magnetizing inductance. The prototype can achieve 97.8% efficiency at 350 V battery voltage with 130 W/in^3 power density.

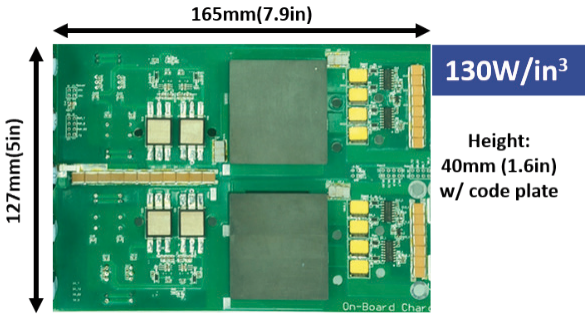


Fig. 3. 6.6kW 500kHz on-board charger second stage prototype.

High-efficiency High-power-density 380 V/12 V DC/DC Converter with a Novel Matrix Transformer

Isolated high output current dc/dc converters are critical for future data center power architecture, however, the design is very challenging due to high conduction loss. Recently, the International Electronics Manufacturing Initiative (iNEMI), at the behest of IBM and other server manufacturers, undertook a project to develop an industry standard for dc/dc converters. This converter is used to step down 380 V directly to 12 V with 800 W output and is placed directly on the motherboard. The matrix transformers for the LLC converter in this application are investigated and a novel matrix transformer structure is proposed in this paper.

To improve the current design practice, a high-frequency transformer loss model is developed and a detailed design methodology is proposed. To overcome the challenge of multiple cores, a novel matrix transformer structure is proposed to integrate four elemental transformers into one magnetic core and utilize a simple four-layer PCB as the windings. The proposed design can utilize flux cancellation and reduce flux density in the magnetic plates to reduce core loss and to integrate SRs and output capacitors into the secondary winding, which minimizes leakage and termination loss. The core loss with the proposed matrix transformer is reduced by more than half when compared to the state-of-the-art matrix transformer technique. The proposed matrix transformer is superior to the state-of-the-art due to the much reduced core loss, simple four-layer PCB windings and integrated magnetic structure.

By pushing switching frequency up to MHz with GaN devices, the proposed matrix transformer can demonstrate the impact of a GaN in such important issues as efficiency, power density and manufacturability. With the academic contribution provided in this paper, we can design a converter with 10 or even 20 times the switching frequency, as compared to the current practice that uses silicon devices. Finally, a 1MHz 380V/12V 800W LLC converter with a GaN device using the proposed matrix transformer structure is demonstrated, as shown in Fig. 1. The prototype fits in a quarter-brick footprint and achieves a peak efficiency of 97.6% and a power density of 900W/in^3. With over 3 generations of LLC converter designs for this application, the efficiency has been improved continuously and our latest design can satisfy iNEMI's requirement with enough margin as shown in Fig. 2.

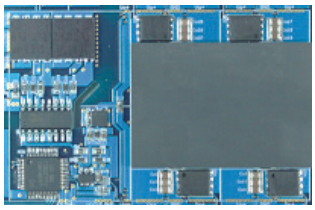


Fig. 1. Hardware prototype.

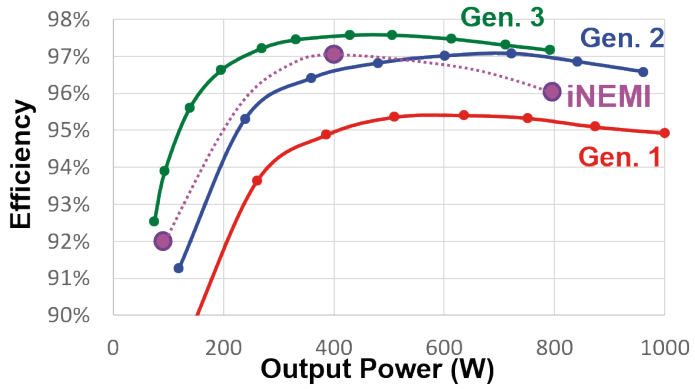


Fig. 2. Efficiency improvement.

Modeling Resonant Converter in a Rotating Coordinate

Part of the difficulty of modeling a resonant converter is the fact that, unlike a pulse-width-modulation (PWM) converter, an average concept doesn't work. The only successful equivalent circuit model, proposed by E. Yang, is based on fundamental approximation and harmonic balance theory. Although his model is accurate, it is conceptually difficult to understand because there is no clear "equilibrium state," as illustrated in Fig. 1.

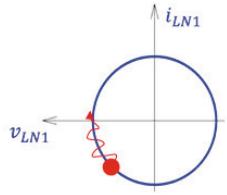


Fig. 1. Inductor phase plane of E. Yang's small-signal model.

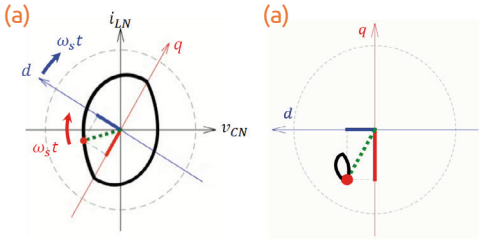


Fig. 2. State plane of an SRC
(a) Stationary coordinate
(b) Rotating coordinate.

On the other hand, ac machine theory has dealt with sinusoidal waveforms for decades. By rotating the coordinate transformation, or dq-transformation, ac signals become dc signals. As a result, the average concept works again. If we look at the trajectory in the state plane of an SRC, as shown in Fig. 2(a), the state is rotating with the switching frequency ω_s. Therefore, if the two axes, d and q, also rotate with ω_s, the state becomes stationary with respect to the new coordinate, as shown in Fig. 2(b). In this case, the equilibrium state of SRC is clearly defined.

Since the average concept applies to an SRC on a rotating coordinate, the modeling process is as simple as that for a PWM converter. The average model of an SRC on a rotating coordinate is shown in Fig. 3. Compared with a simplified version of E. Yang's model, which was derived by S. Tian, the two models are almost identical. However, the latter went through complicated mathematical derivation and lengthy simplification. Using a standard perturbation process, the small-signal model of the SRC can be derived, and the simulation results are shown in Fig. 4. The two models match well with the simulation result. Nevertheless, the rotating coordinate method is both conceptually and mathematically easier to use to model a resonant converter.

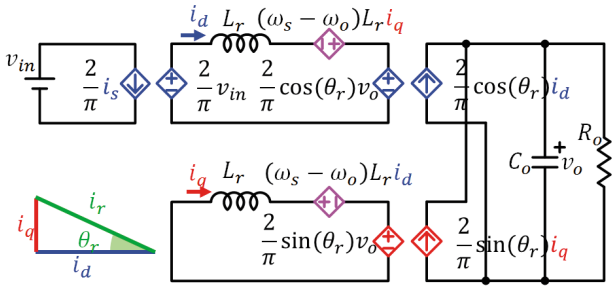


Fig. 3. Average model of SRC in rotating coordinate.

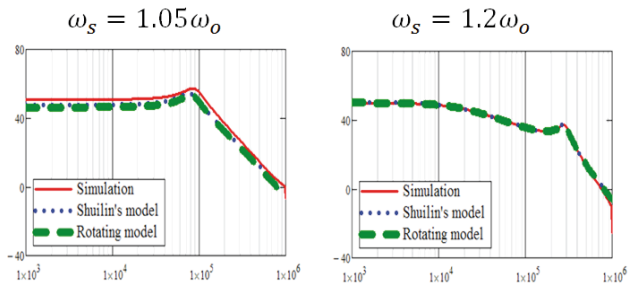


Fig. 4. Frequency-to-output transfer function.

A High-Frequency Small-Signal Model for Inverse-Charge Constant On-time (IQCOT) Current-Mode Control

Constant on-time current-mode (COTCM) control schemes are widely used in VR controllers for their light-load efficiency and higher bandwidth design with simple compensation requirements. The problem with this ripple-based current-mode control is that when the inductor current ripple becomes small because of the ripple cancellation effect for multiphase operation, the control becomes very noise-sensitive and creates jittering at the output. CPES has proposed a new non-ripple-based inverse-charge constant on-time (IQCOT) control which can operate seamlessly at the ripple cancellation point in multiphase operation. This new control also dramatically improves the transient response of constant on-time control. A high-frequency model for IQCOT control has been derived in this nugget using the describing function. An auto-tuning method for Q-value control is also proposed to maintain a constant Q value.

The control-to-output transfer function can be calculated as:

$$\frac{v_o(s)}{v_c(s)} \approx K_c \frac{R_{Co}C_o s+1}{s/\omega_a+1} \frac{1}{1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2}} \frac{1}{1+\frac{s}{Q_2''\omega_2}+\frac{s^2}{\omega_2^2}}$$

where

$$K_c=\frac{R_L}{R_i(1-k_2/R_i\cdot R_L)}, \quad k_2=\frac{1}{L_s s}\{R_i-R_i(1+\frac{s}{Q_2\omega_2}+\frac{s^2}{\omega_2^2}).(1+\frac{s}{Q_2''\omega_1}+\frac{s^2}{\omega^2})\}$$

$$\omega_a=\frac{1-R_L k_2/R_i}{(R_L+R_{Co})C_o-R_L R_{Co}C_o k_2/R_i},$$

$$\omega_1=\frac{\pi}{T_{on}} \quad Q_1=\frac{2}{\pi} \quad \omega_2=\frac{\pi}{T_{sw}} \quad Q_2''=\frac{2s_f T_{sw}}{\pi(\frac{2CV_{TH}}{g_m T_{sw}}-s_f T_{on})}$$

For low duty cycle (D), the T_{on}-related double pole will be at a very high frequency and expression:

$$\frac{v_o(s)}{v_c(s)} \approx K_c \frac{R_{Co}C_o s+1}{s/\omega_a+1} \frac{1}{1+\frac{s}{Q_2''\omega_2}+\frac{s^2}{\omega_2^2}}$$

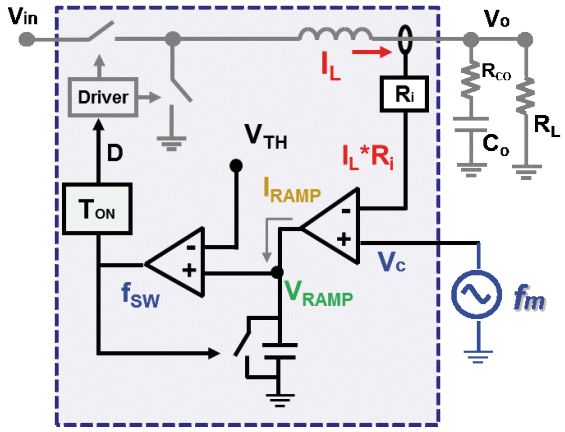


Fig. 1. Considering current feedback as a single entity to model the proposed non-ripple-based IQCOT Control with V_c perturbation.

As the expression of the quality factor of the double pole is a function of duty cycle (D), the Q value will change as the duty cycle changes, which may make the control loop more challenging to design for small-signal stability. To solve this issue, an auto-tuning method is proposed to achieve a constant Q value. For example, to keep $Q''_2 = 1$ for operation with a low duty cycle, the quality factor (Q) expression can be rewritten as:

$$\frac{V_{TH}}{V_{in}^2}\frac{V_o}{g_m}=\frac{T_{on}^2 R_i}{CL_s}$$

Therefore, to keep $Q''_2 = 1$, the control needs to maintain:

$$V_{TH} \propto V_{in}^2 \qquad \& \qquad g_m \propto V_o$$

Details are presented in the conference paper.

High-Efficiency High-Density CRM Rectifier/Inverter for WBG-Based On-Board Charger

Plug-in electric vehicles (PEVs), which include plug-in hybrid electric vehicles (PHEVs) and battery electric vehicles (BEVs), are becoming more and more popular due to their more efficient energy utilization and reduced combustion emissions. One crucial challenge of PEV commercialization is the demand for lightweight, compact, and efficient on-board chargers (OBCs). The state-of-the-art level-2 OBC products are primarily Si-based designs, which operate with a switching frequency of less than 100 kHz, and have only 3-12 W/in^3 power density and at most 92-94% efficiency.

In addition, market research conducted by automobile companies shows that consumers strongly desire a bidirectional power flow of the OBC system. However, Si-based OBC products cannot provide this flexibility without significant sacrifice of power density and/or efficiency.

Emerging wide-band-gap (WBG) power semiconductor devices provide the technology that enables a dramatic increase in the efficiency and power density of switch-mode power supplies with the potential for lower cost and better manufacturability. A high-efficiency, high-density on-board charger using E-mode GaN HEMTs has recently been demonstrated. However, the system is relatively complicated because of the added active filter and the fact that there are too many devices in parallel.

In this work, a wide-band-gap based bidirectional on-board charger (OBC) is proposed that uses a variable dc-link voltage, which tracks the battery voltage fluctuation. Although this approach is deemed most efficient for the resonant dc/dc stage, it poses significant challenges for the rectifier/inverter stage, which operates in critical mode to realize ZVS, while being subject to the large variations of input and output voltages. This paper presents design considerations of the ac/dc stage, including the evaluation of 1.2 kV SiC MOSFETs; the zero-voltage-switching (ZVS) extension techniques to realize ZVS under all input/output variations; and a novel universal control strategy for both the rectifier mode and the inverter mode. A prototype is built which achieves 98.5% efficiency at a switching frequency higher than 300 kHz. Furthermore, a 6.6 kW OBC system is demonstrated, using both SiC and GaN devices with 43 W/in^3 power density and above 96% efficiency.

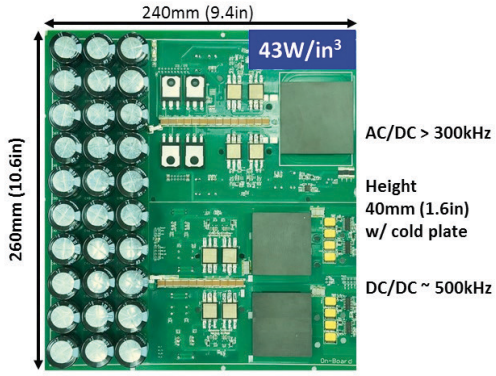


Fig. 1. Prototype of the 6.6 kW on-board charger.

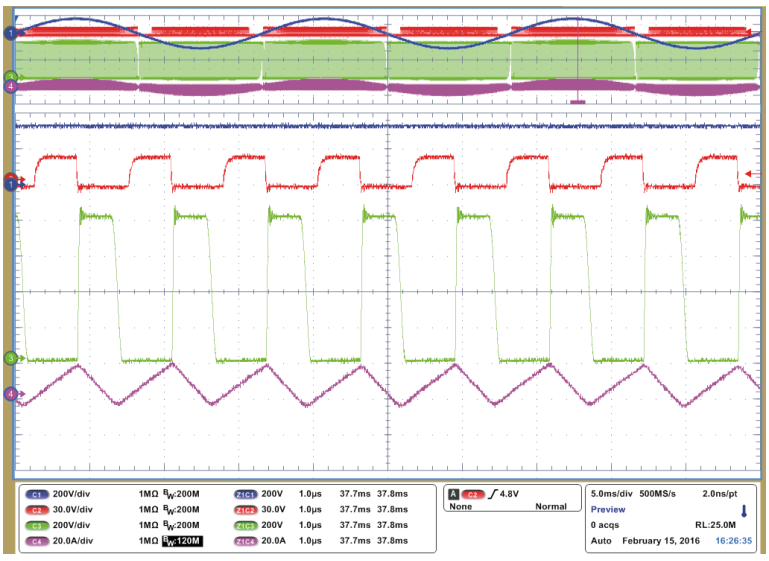


Fig. 2. Experimental waveform of the ac/dc stage at 800V/3.3kW in charging mode (CH1 is input ac voltage; CH2 is the V_{GS} of the bottom switch of Phase 1; CH3 is the V_{DS} of the bottom switch of Phase 1; CH4 is the inductor current of Phase 1).

High Density Integration Nuggets

Very High Frequency IVR for Small Portable Electronics with High-Current Multi-phase 3D Integrated Magnetics

Two Core Implementations of Coupled Inductors for Paralleled Three-phase Power Converters

Synergetic Optimization of Efficiency and Stray Magnetic Field for Planar Coils in Inductive Power Transfer Using Matrix Calculation

Additive Manufacturing of Toroid Inductors for Power Electronics Applications

Design of Inductors with Significant AC Flux

Very High Frequency Integrated Voltage Regulator for Small Portable Devices

Equivalent Electric Circuit for a Wave Energy Converter

On the Measurement of Switching Energy

Design and Development of a 10 kV, 60 A SiC MOSFET Module

Conceptual Design and Weight Optimization of Aircraft Power Systems with High-Peak Pulsed Power Loads

Large Substrates Bonded by Silver Sintering and Their Thermal Performance

Insulation Design and Evaluation via Partial Discharge (PD) Test for Power Electronics Applications

DBC Switch Module for Management of Temperature and Noise in 220-W/in^3 Power

NiCuZn Ferrite Cores by Gelcasting: Processing and Properties

Design and Development of a Novel, High-Density, High-Speed 10 kV SiC MOSFET Module

Very High Frequency IVR for Small Portable Electronics with High-Current Multi-phase 3D Integrated Magnetics

As today's small portable electronics (smartphones, tablets, e-readers, etc.) becomes lighter, thinner, quicker, and smarter, the voltage regulator for the processor is expected to be efficient, miniaturized, integrated, and placed closer to the processor. Power consumption would be reduced dramatically if the supply voltage could be modulated rapidly based on the power demand of each core. However, traditional discrete voltage regulators (VRs) are not able to realize the full potential of DVFS since they are not able to modulate the supply voltage fast enough due to their relatively low switching frequency and the high parasitic interconnect impedance between the VRs and the processors.

Integrated voltage regulators (IVR) with high granularity, small size, near-load integration, and very high switching frequency have been successful in improving the efficiency of power delivery to multi-core processors, such as those implemented in Intel's Haswell and Broadwell processor. This work extends this concept to create the 3D integrated architecture, as shown in Fig. 1 for small portable electronics. The converter is running at tens of MHz to track the core voltage. The multi-phase one-turn inductors are integrated into one magnetic core featuring a simple winding structure, small size, ultra-low profile, ultra-low DCR, high current-handling ability, and air-gap-free magnetics (to effectively confine very high-frequency stray flux). As shown in Fig. 2, the five-phase integrated inductor is designed with 0.5 mm in thickness and 16 mm^2 in footprint to fit the stringent space requirement of smartphones. The inductor is designed to be stacked with power management IC (PMIC) to save valuable motherboard footprint, and to be placed directly under the processor die to facilitate a short power delivery path. Both single-phase and five-phase integrated inductors are designed, fabricated and experimentally tested at 20 MHz in this work.

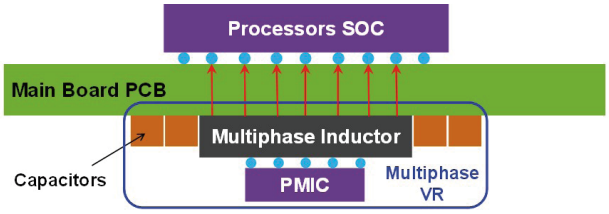


Fig. 1. 3D integrated very high frequency voltage regulator for small portable electronics.

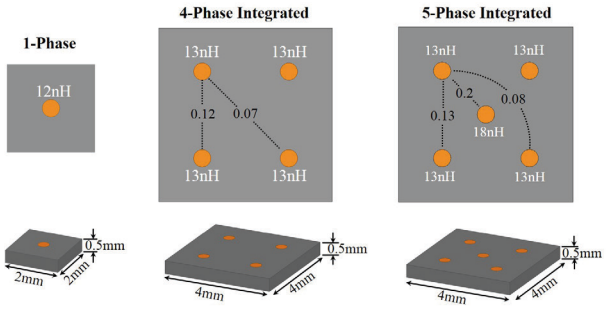


Fig. 2. Single-phase and multi-phase integrated low profile inductor. The figure shows the self-inductance of each phase and magnetic coupling coefficient between phases at 20 MHz and 3A per phase load condition.

Two Core Implementations of Coupled Inductors for Paralleled Three-phase Power Converters

Interleaving is a widely used technique in power electronics, but if the interleaved converters share a common ac output and dc link, circulating current flows between the converters. The circulating current contributes to additional loss at the power devices and the filters, deteriorating the efficiency of the system. Common-mode chokes or coupled inductors (CIs), as shown in Fig. 1, are used to suppress the circulating current. These additional magnetic components increase the total size and weight of the system and mitigate the benefits of interleaving on size and weight reduction.

This paper presents a new structure for coupled inductors in three-phase converters that minimizes the weight of the magnetics in paralleled converters. In the steady state, every current harmonic at each frequency can be classified into one of four groups according to DM and CM, and phase-shifted by 180°, as shown in Table 1. Coupled inductors provide large impedance only for circulating currents, which are in Groups 3 and 4.

The proposed coupled inductors are comprised of two cores. One core is for use in DM coupled inductors (DMCIs) to suppress the DM circulating harmonics of Group 3. The other core is a CM coupled inductor (CMCI) to suppress the CM circulating harmonics of Group 4. By combining the structure of a conventional three-phase inductor with the coupled inductors, a single E-core with six windings, as shown in the left of Fig. 2, can be implemented to suppress DM circulating current. By combining the structure of the CM choke with the coupled inductors, a U-core pair with six windings, as shown in the right of Fig. 2, can effectively couple the flux of the CM circulating current.

Between 3ϕ / Between Converter	*Differential mode* $i_{as} + i_{bs} + i_{cs} = 0$	*Common mode* $i_{as} = i_{bs} = i_{cs}$
Non-phase-shifted $i_{xs1} = i_{xs2}$	Group 1 Fundamental current at f_0, DM harmonics at $2mf_{sw}$	Group 2 CM harmonics at $2mf_{sw}$
Phase-shifted $i_{xs1} + i_{xs2} = 0$	Group 3 DM harmonics at $(2m-1)f_{sw}$	Group 4 CM harmonics at $(2m-1)f_{sw}$

Table 1. Classification of current harmonics on frequency spectrum.

Prototypes have been built to examine possible size reduction. Conventional coupled inductors and the proposed DMCI and CMCI are designed to have similar maximum magnetic-flux density, while the turns number for each coupled inductor is set to have a mutual inductance value. Using the proposed integration can reduce the weight of the coupled inductor by 30%, from 510g to 361.5g, with the same attenuation for circulating current.

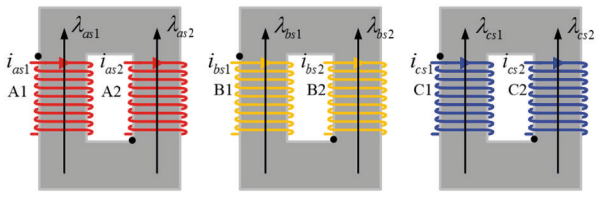


Fig. 1. Structure of Conventional Coupled Inductor.

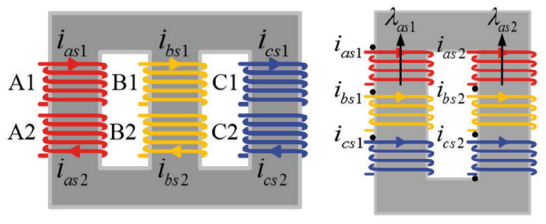


Fig. 2. Structure of DM & CM Coupled Inductor.

Fig. 3. Size Comparison for Prototype.

Synergetic Optimization of Efficiency and Stray Magnetic Field for Planar Coils in Inductive Power Transfer Using Matrix Calculation

When charging the battery of electric vehicles (EVs), inductive power transfer (IPT) uses loosely coupled coils with gaps that are tens of centimeters as a replacement for cables and plugs. Power is transferred from a transmitter to a receiver based on magnetic resonance and near-field magnetic coupling. A planar coil with a spiral winding and magnetic plate, as shown in Fig. 1, is the most popular because of higher coupling across a large air gap and more stable coupling in the presence of misalignment. The coils' efficiency and stray magnetic fields are two important properties for IPT coils. The coils' efficiency is defined as the ratio of active power from the output terminal to the input terminal of the coils. It directly influences the system's efficiency. A significant stray magnetic field around the coils is caused by a large gap between the transmitter and receiver.

Efficiency and stray magnetic fields are influenced simultaneously by design of coils' parameters, such as inner radii, outer radii, and distribution of turns. Their synergetic optimization is important. Pareto front of coils' efficiency versus a stray magnetic field is suitable for this kind of multi-objective optimization. Physical parameters are swept in finite-element simulation (FES) to derive the Pareto front. However, the problem of a parametric sweep is that it asks for thousands of simulations that are time-consuming especially for 3D simulation.

A faster method using matrix calculations is demonstrated in this paper. Efficiency and magnetic field are calculated with winding vectors, permeance matrices, and current-to-field (I-B) matrices instead of being simulated. Physical parameters of coils including inner radii, outer radii, and distribution of turns are represented with winding vectors. The parametric sweep in simulation is replaced by sweeping winding vectors in matrix calculation to derive Pareto fronts for optimization. Only tens of simulations are required in the optimization procedure using the matrix calculation. Fig. 2 shows the optimization procedure.

Accuracy of the matrix calculation is verified by comparing with experimental measurement for a set of exemplary coils. The maximum difference of the exemplary coils between calculation and measurement is 4% for inductances, 9% for ESRs, and 12.5% for stray magnetic field.

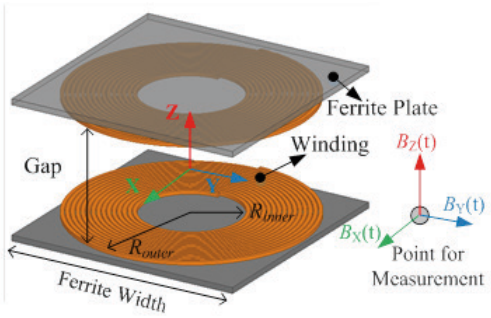


Fig. 1. Planar coil with ferrite plate in IPT.

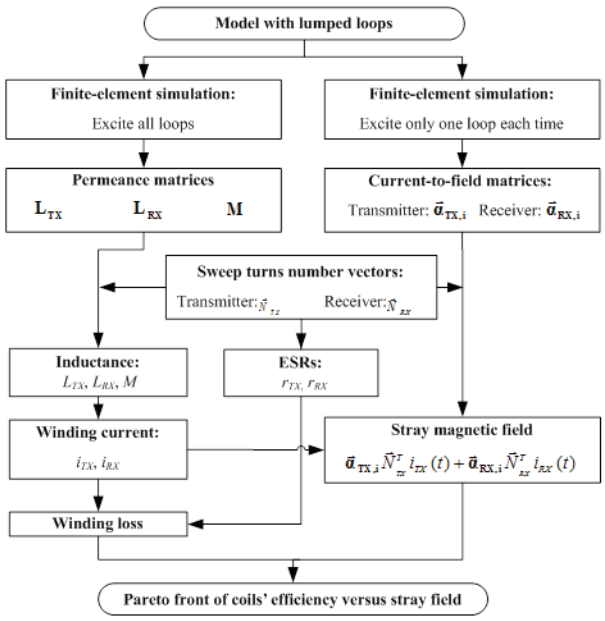


Fig. 2. Flowchart of synergetic optimization of coils' efficiency and stray magnetic field for IPT coils.

Additive Manufacturing of Toroid Inductors for Power Electronics Applications

The integration of power inductors and transformers, as illustrated in Fig. 1(a), is challenging due to the large core volume or unconventional geometries used to distribute flux or control coupling. Commercial magnetic components consisting of cores and windings are fabricated separately and then assembled, as shown in Fig. 1(b). This manufacturing approach gives rise to bulky discrete components and precludes the implementation of high-density, high-performance integrated geometries. For example, the uniform-flux magnetic component structures shown in Fig. 1(c) cannot be fabricated by the current manufacturing processes. Thus, to improve the power conversion efficiency, power density, and reliability of a power electronics system, there is a need for manufacturing technologies that ease integration of the magnetic components.

Additive manufacturing (AM) or three-dimensional (3D) printing is a layer-by-layer process of making products and components from a digital model. Some key benefits of AM are shorter lead times, mass customization, reduced part count, ability to manufacture more complex shapes, less material waste, and lower life-cycle energy use. Recently, some research groups have explored the application of AM in power electronics. The purpose of this work is to explore the feasibility of using a 3D-printing process for fabricating magnetic components that consist of both magnetic cores and conductive windings. We chose to work with a multi-material extrusion-based 3D printer because it offers the ease and flexibility of co-processing multiple materials, and for feedstock we can leverage our research expertise in the formulation of pastes of metal and magnetic + polymer composites. Use of paste as the feedstock also reduces material waste, lowers the equipment cost, and simplifies the part construction process. The paste-based additive process can be readily scaled up to manufacture a multi-material and multi-functional system. Thus, this process platform offers the potential for further integration of a power electronics circuit by concurrent manufacturing of capacitive, magnetic, and resistive components.

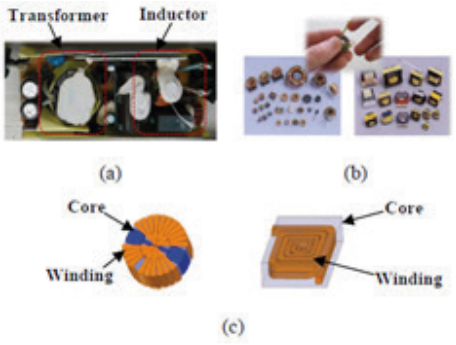


Fig. 1. (a) Typical power supply consisting of a number of discrete magnetic components; (b) Basic process for making the windings of inductors and transformers; and (c) Integrated uniform-flux inductor design.

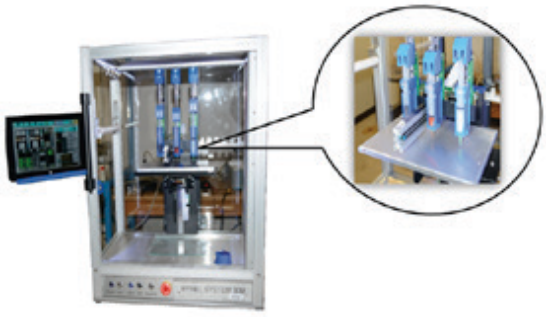


Fig. 2. Multi-extruder paste-extrusion 3D printer.

Design of Inductors with Significant AC Flux

The design methodology shown in Fig. 1 is introduced to select a minimum core volume for an inductor or coupled inductors experiencing appreciable core loss. The geometric constant (K_{gac}) has been found to be a power function of the core volume for commercial toroidal, ER, and PQ cores, permitting the total loss to be expressed as a direct function of the core volume. The inductor is designed to meet specific loss or thermal constraints. An iterative design procedure is used, in which 2D or 3D proximity effects are neglected at the beginning, and then subsequently incorporated via finite element simulation. The methodology is demonstrated in Fig. 2 for coupled inductors in a 5 MHz converter operating in critical conduction mode. The core loss is verified using rectangular excitation, and the winding loss is inferred from the noise robustness of thermal measurements and low thermal resistance. Negative couplings between conductors as well as a compact layout with 2.89-nH common-source inductance in the module eliminates self-turn-on from 420-A/μs di/dt.

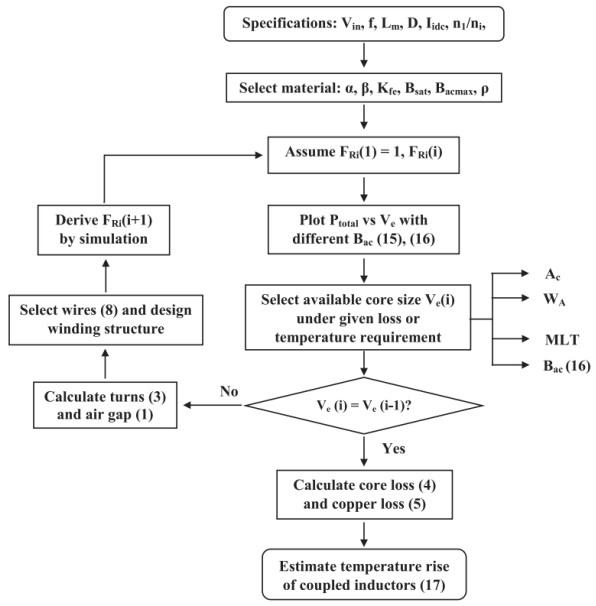


Fig. 1. Flowchart of design procedure for K_{gac} method.

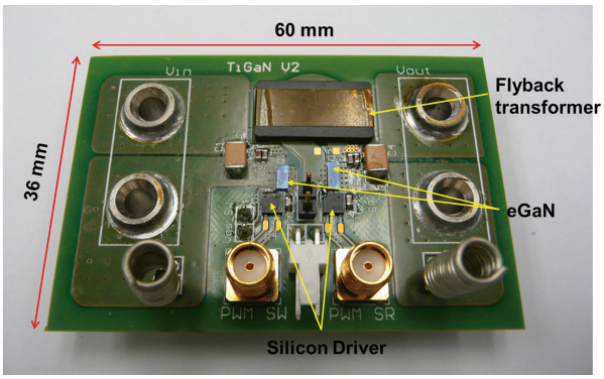


Fig. 2. Test board of 5MHz, 30W flyback power converter to verify the methodology of the designed couple inductors.

Very High Frequency Integrated Voltage Regulator for Small Portable Devices

Voltage regulators are widely used to power multi-core processors in small portable electronics such as smartphones and tablets. A four-phase buck converter and a two-phase buck converter, for instance, drive the two-core CPU and the GPU in an iPhone 6 motherboard as illustrated in Fig. 1. The power inductor is placed at the front side of the motherboard close to the processor, whereas the power management IC and capacitors are placed at the back side. A majority of the motherboard footprint is occupied by the voltage regulator.

Power consumption would be reduced dramatically if the supply voltage could be modulated rapidly based on the power demand of each core. However, the voltage regulator in Fig. 1 is unable to offer this feature because of their low switching frequency and the high interconnect impedance between the voltage regulator and the processor.

Integrated voltage regulators with high granularity, small size, near-load integration, and very high switching frequency have been successful in improving the efficiency of power delivery to multi-core processors, such as those implemented in Intel's Haswell and Broadwell processor. This work extends this concept to create the 3D integrated architecture in Fig. 2 for small portable devices. The converter is running at tens of MHz to track the core voltage. The multi-phase one-turn inductors are integrated into one magnetic core featuring a simple structure, ultra-low profile, small size, lateral non-uniform flux distribution, and air-gap free structure (to effectively confine very high-frequency stray flux). The inductor is designed with 0.5 mm thickness to fit the stringent space requirement of smartphones, and placed directly under the processor die to facilitate a short power delivery path. The inductor will be stacked with the power-management IC to save the footprint traditionally occupied by the passive components. In the case of Fig. 1 for example, a total footprint of about 100 mm^2 can be saved.

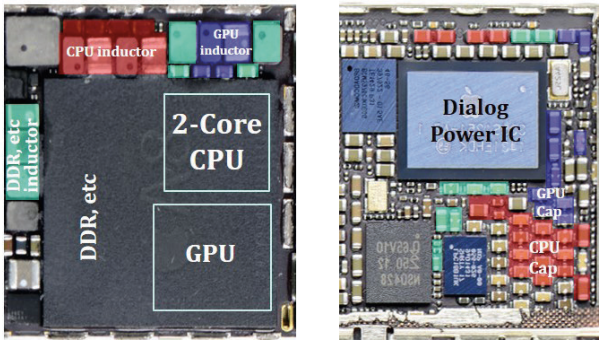


Fig. 1. Front (left) and back (right) views of existing voltage regulator for iPhone 6 using multiple cores.

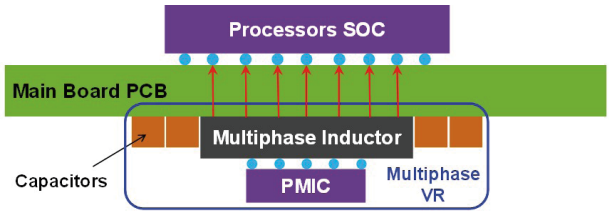


Fig. 2. 3D integrated very high frequency voltage regulator for small portable devices.

Equivalent Electric Circuit for a Wave Energy Converter

An equivalent circuit provides a faster and reliable way to analyze and design the wave energy converters (WECs). A WEC as a mechanical – electrical composite system which converts ocean wave energy to electrical power is shown in Fig. 1. The WEC system starts from buoy-wave interaction coupling with a rotational mechanical system, and then a mechanical motion rectifier (MMR) drives the permanent magnet synchronous generator (PMSG) which delivers energy to a power electronics converter.

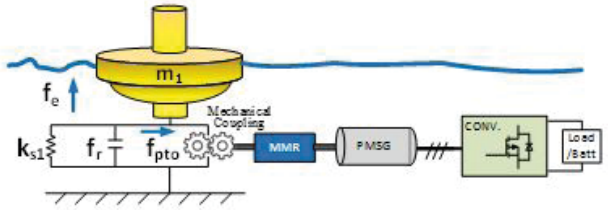


Fig. 1. Mechanical Diagram of WEC system including: Buoy, MMR, Mechanical Coupling, Generator, and Power Converter.

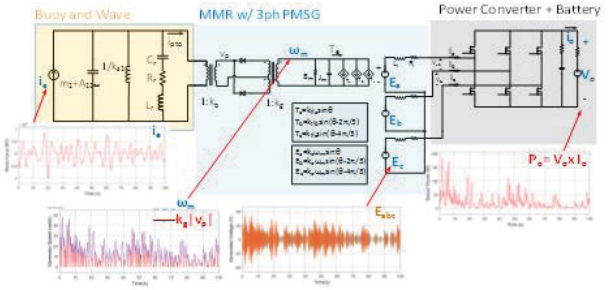


Fig. 2. Equivalent circuit of the WEC and its output waveforms under irregular wave condition.

Through approximation and circuit synthesis methods, wave-buoy behavior can be linearized as a RLC circuit network in Fig. 2. The nonlinearity of MMR sets can be modeled as transformers and diodes. Along with a generator circuit model and power converter, a general methodology is shown to convert a multidisciplinary system into electrical components, which can be an aid to the electrical designers in the wave energy area.

Two applications will be introduced in this work. One is to apply a reliability analysis of each component. Under irregular wave conditions, a wave force is modeled as a current source that defines the input of the system in Fig. 2. Each rotational speed and torque values can be monitored real-time as voltage and current waveforms, so the maximum stress of each component can be recorded. Another is applied to optimize the systems output power. Based on an equivalent circuit, the system's output power capability can, thus be analyzed under different wave periods and gear ratio in Fig. 3.

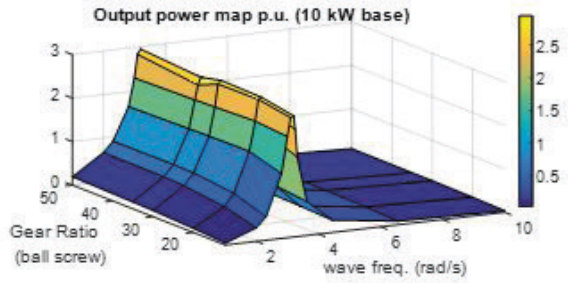


Fig. 3. Application of Equivalent Circuit for maximum output power under different wave frequency and gear ratio.

On the Measurement of Switching Energy

The way to identify the transient starting and ending points varies between manufacturers and researchers. Some manufacturers define the starting point of the turn-on transient as when gate-to-source voltage v_{gs} increases to 10% of its steady-state value V_{DR}, and the ending point to be when the drain-to-source voltage v_{ds} decreases to 2% of its steady-state value V_{CC}. The turn-off transient is defined to begin when v_{gs} decreases to 90% of V_{DR} and ends when the drain current i_d decreases to 2% of the steady-state value I_D.

Other manufacturers consider the starting point of the turn-on transient to be when v_{gs} increases to 10% of V_{DR} and ends when v_{ds} decreases to 10% of V_{CC}. The starting point of the turn-off transient is defined to be when v_{gs} decreases to 90% of V_{DR} and ends when v_{ds} increases to 90% of V_{CC}.

Both of these methods ignore the losses caused by the switching ringing, which are considered by some researchers. The turn-on transient is defined as starting when the i_d is non-zero and ending when the peak-to-peak current of the ringing is 10% of I_D. The turn-off transient is defined as beginning when i_d begins to decrease and ends when the peak-to-peak current of the ringing is 10% of I_D. This method includes the ringing loss but also contains part of the conduction loss. The proportions of the conduction losses that are included are different for different devices under various test conditions. This would make a comparison of the devices unfair.

This work describes a method to calculate the switching energy independent of transient timing. The total loss energy E is calculated from switching energy E_{switch}, conduction energy E_{cond}, steady-state current I, resistance $R_{ds(on)}$ when the MOSFET is fully on, and on-time T_{on} by $E = E_{switch} + E_{cond} = E_{switch} + I^2 R_{ds(on)} T_{on}$. Constant I is realized by a current source in simulation or large inductor in practice. "Constant $R_{ds(on)}$" is approximated by "negligible variation in $R_{ds(on)}$" by limiting the temperature rise induced by the power pulses in one period. By assigning T_{on} to be a chosen on-time T_{on1}, the associated total energy in one cycle E_1 could be obtained by simulation or experiment. By assigning T_{on} to be value T_{on2}, the associated E_2 becomes known. The switching energy is then calculated by $E_{switch} = (E_1 T_{on2} - E_2 T_{on1})/(T_{on2} - T_{on1})$. The switching energy calculated by the previous three existing methods based on the simulated power waveform differs from the simulated channel energy by more than 9%. The difference is reduced to 0.3% by using the proposed method.

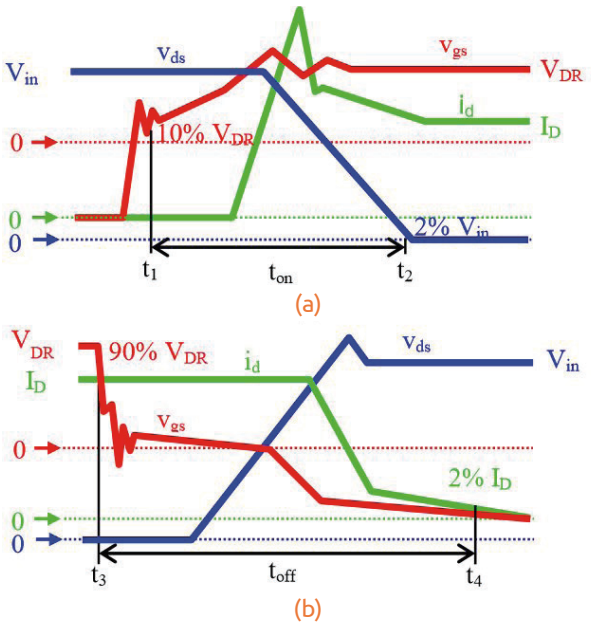


Fig. 1. (a) Turn-on transient and (b) Turn-off transient.

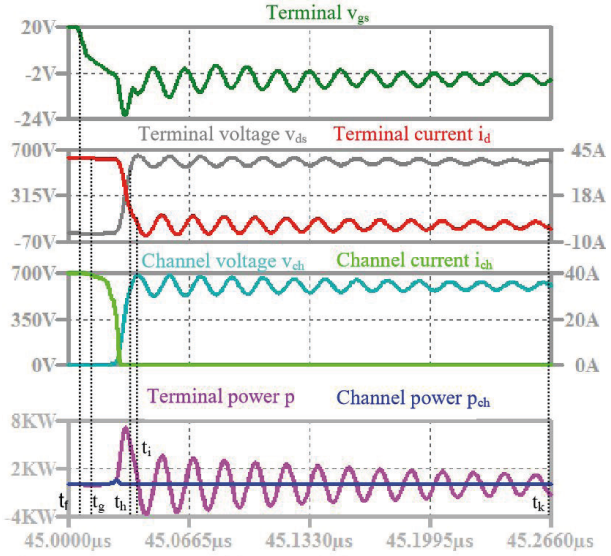


Fig. 2. Power waveform with severe ringing.

Design and Development of a 10 kV, 60 A SiC MOSFET Module

High-voltage Silicon Carbide (SiC) transistors have been demonstrated in recent years, and now Cree's 3rd-generation 10 kV, 350 mΩ SiC MOSFET is becoming available. This device is capable of switching higher voltages faster, and with lower losses, than Si IGBTs. These features reduce the complexity of medium-voltage systems, since simpler topologies with fewer levels can be used, and allow for the realization of new applications.

At present the performance of these unique devices is limited by standard module packages that were originally developed for slower, lower density Si devices. The aim of this work is to develop a high-density, high-speed, half-bridge module for these 10 kV SiC MOSFETs without antiparallel diodes; instead, the reverse current will flow through the MOSFET channel, and the body diode will only conduct during the deadtime. There are several challenges associated with this objective. In particular, the desire for high density will increase the electric field concentration within the module. This is a new challenge that has not been explicitly addressed before, and it arises from the development of this high-density, high-voltage SiC device.

The designed power module is shown in Fig. 1. The module consists of AlN direct bonded aluminum (DBA) substrates, and uses 96.5Sn/3.5Ag solder preform for the die attach, and 10-mil Al wirebonds for the interconnections. Embedded decoupling capacitors are also included in the module for improved transient performance. According to ANSYS Q3D Extractor, the gate- and power-loop inductances are 6 nH and 10 nH, respectively.

To minimize the peak electric field that occurs at the triple point of the DBA substrates, two DBAs are stacked together. Partial discharge (PD) tests were performed for both the single- and stacked-substrate cases. When stacking two DBAs together, the partial discharge inception voltage (PDIV) increased by 15%. This can be attributed to the reduction in the electric field at the triple point. Fig. 2 shows the PD signals for both cases.

Another challenge associated with the high-density design is the module termination. Specifically, how to interface the module with the rest of the high-voltage system. Commercial high-voltage connectors are significantly larger than the module itself, and are thus not viable options for this work. Consequently, alternative solutions need to be explored, and evaluated based on the tradeoffs between peak electric field, current carrying capability, parasitic inductance, ease of assembly, and reliability.

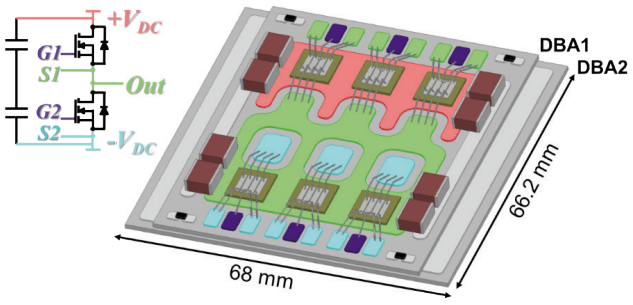


Fig. 1. Design of a 10 kV power module.

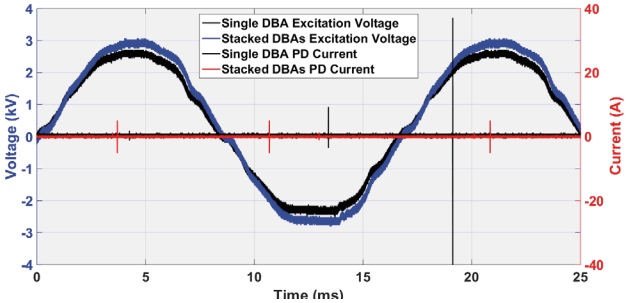


Fig. 2. PD waveforms of single and stacked DBA substrates in air.

Conceptual Design and Weight Optimization of Aircraft Power Systems with High-Peak Pulsed Power Loads

The More Electric Aircraft (MEA) concept has continued to evolve even with the development of new electrical power conversion technology. As such, one of the main building blocks in advanced aircraft power systems are multi-converter power electronics systems that have demonstrated significant advantages in terms of reliability, efficiency and weight reduction.

These power conversion units must provide energy under challenging mission profiles, which includes feeding pulsed power loads. The latter have been increasingly adopted—especially in military applications—demanding high peak power from these systems. Due to the nonlinear characteristic of a pulsed power load, when the load is on it, consumes large amounts of power in a short period of time. This is subsequently followed by periods of low power consumption. The extent of these power transients is significant, affecting the mechanical system to the point where it could impact its physical integrity if the generator-shaft mechanism is not designed to sustain such loading profile. As a consequence, in order to maintain the weight advantage of the MEA, as well as to keep the normal functionalities of aircraft power systems, it is highly desirable to apply multidisciplinary design optimization techniques on this electromechanical system under the presence of high-peak pulsed power loads.

Along these lines, this paper will introduce a novel multidisciplinary weight optimization method for the aircraft power system with high-peak pulsed power loads. The focus of this proposed optimization method will be on evaluating different power-electronics-system topologies as well as alleviating the impacts of the pulsed load. For our targeted power system, a combination of various mechanical structures and electrical subsystems including engine, gear box, shafts, synchronous generator, power electronic converters and energy storage devices, are considered. After developing weight models for each of these subsystems, it becomes possible to calculate, compare, and evaluate the weights of these power systems with different architectures. Here, two power system topologies are considered and are shown in Fig. 1. Finally, through a case study of interest, it is shown that system weight reductions in the order of 12% can be attained when applying the proposed optimization method to down select alternative system configurations. The weight comparison between the two topologies and different subsystems is presented in Fig. 2.

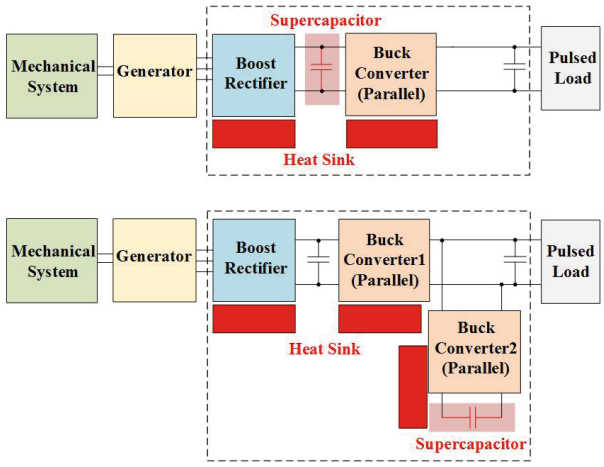


Fig.1. Topologies of the power system under study.

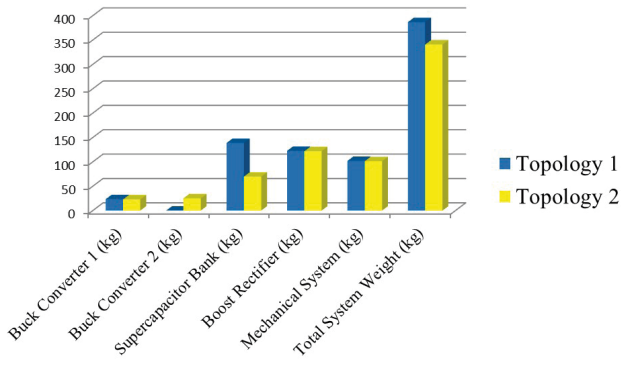


Fig. 2. Weight optimization result for Topology 1 and 2.

Large Substrates Bonded by Silver Sintering and Their Thermal Performance

Heat dissipation is a critical function of packaging power devices or modules. In a power package, heat generated by the device has to be conducted away through multiple layers of materials and bonded interfaces. One of the most important bonded interfaces is the thermal interface between the substrate and the heat spreader or heat-sink plate. The emerging sintered silver technology has been shown to offer significantly higher thermal and electrical conduction and higher reliability than the conventional soldering technologies for die-attachment, which is a promising alternative for large area bonding. The purpose of this study is to develop the large area bonding technique with silver sintering and then characterize the thermal properties. The DBA substrates were bonded together by silver paste under the heating profile shown in Fig. 1. To characterize bonding quality, thermal resistance was measured. A typical value for silver sintering is about 5 mm^2k/W.

Silicon IGBT chips are mounted on the substrate. The IGBTs are used as a heat source as well as a temperature sensor. Transient thermal impedance or Zth measurement is performed by taking the ratio of junction temperature raise over the heating power. The package is modeled by a Foster network of capacitors and resistors, which corresponds to heat capacities and resistances of the materials or interfaces, respectively. Then, using electrical network theories and mathematical algorithms, the measured junction temperature response is transformed into a cumulative structure function of the package. The function represents a relationship between the cumulative thermal capacitance and cumulative thermal resistance from the device junction through the package. Finally the thermal resistance of the substrate attach layer is derived. By mounting multiple chips at different locations, the 2-dimension map of thermal resistance is plotted as shown in Fig. 2. The average value is 5.20, which is nearly the lowest amongst the thermal interface materials. The variation is 6%, which illustrates the bonding quality is uniform across the whole area.

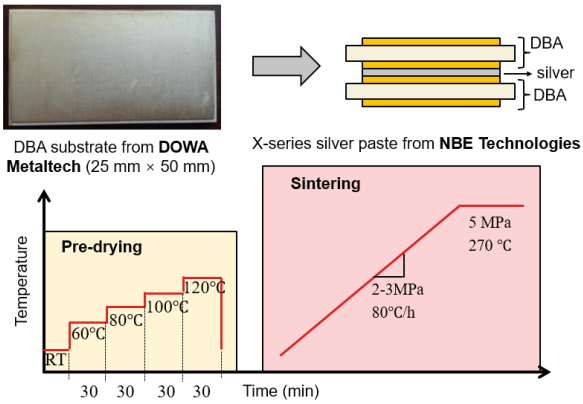


Fig. 1. Large area bonding by silver sintering at low temperature.

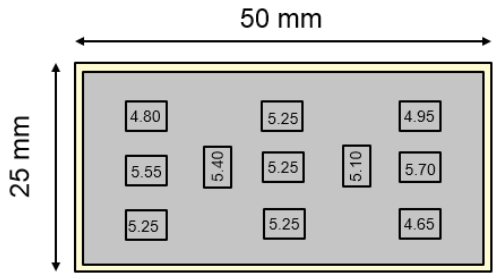


Fig. 2. 2-dimension map of thermal resistance for bonding layer.

Insulation Design and Evaluation via Partial Discharge (PD) Test for Power Electronics Applications

Due to the development of wide band-gap devices, new power electronics equipment will be able to sustain higher voltage levels with a reduced number of switches and still achieve major reduction in switching losses. This will lead to a very high power density for future power electronics equipment. The high power density will cause significantly increased electric field strengths inside the equipment. A non-uniform and concentrated electric field distribution, caused by fringing effects, may double or even triple the electric field strength in some places. High electric field strength, together with high-frequency, non-sinusoidal excitations, will become a major challenge for insulation design, which may become a limitation that will prevent future equipment from achieving the expected high power density.

Insulation evaluations and tests are usually performed for high-voltage line frequency applications, but there has not been much research on insulation evaluation and design for power electronic applications, or under repetitive short rising time impulse excitation. A great deal of work is still worthy of being done for the insulation design and evaluation for the field of power electronics.

Some ways to reduce the fringing effect are summarized and shown in Fig. 1. These methods can help reduce the dielectric stress in the system and thus improve the insulation. The effectiveness of the methods will be proved via Maxwell simulation. The PD measurement setup used in the lab is illustrated in Fig. 2, with a single-void test specimen to verify the effectiveness of the setup. The sensitivity of this setup is around 20 pC and is sufficient to evaluate the insulation for most of the existing parts in power electronics equipment. Finally, a real lab-made laminated bus is depicted in Fig. 3, and its PD behaviour under line frequency excitation is evaluated in Fig. 4. More tests for the PD behaviour under PWM excitation will be done in the future, and ways to improve the insulation for existing parts will be discussed.

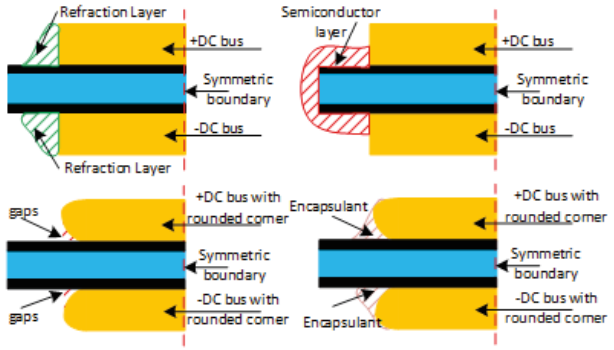


Fig. 1. Practical methods to reduce fringe effect.

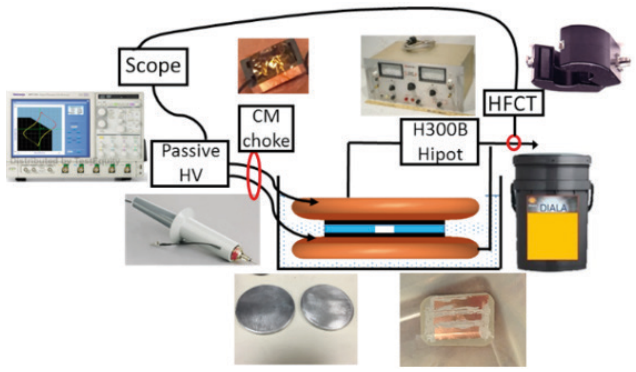


Fig. 2. Block and wire diagram for the PD test setup.

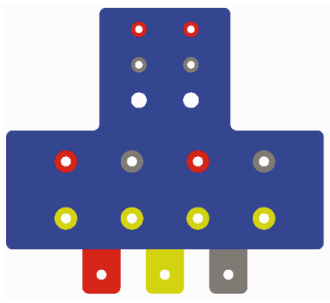


Fig. 3. 3D drawing of the laminated bus under test.

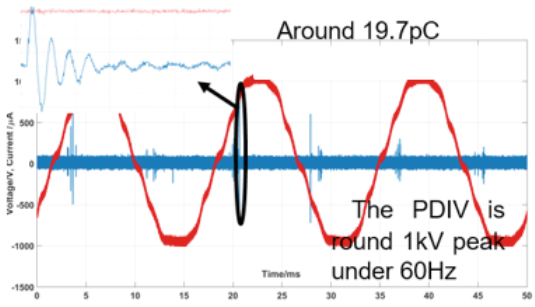


Fig. 4. PD behavior of the laminated bus.

DBC Switch Module for Management of Temperature and Noise in 220-W/in³ Power

A switch module integrates semiconductor dies on a direct-bond-copper (DBC) substrate to achieve both noise robustness and low thermal resistance. Negative couplings between conductors as well as compact layout with 2.89-nH common-source inductance in the module eliminate self-turn-on from 420-A/μs di/dt. The low thermal resistance of the DBC substrate provides 2.35° C/W thermal resistance from junction to heat sink and limits the temperature rise of semiconductors switches to 50° C. The maximum rated power and system density of the DBC and PCB modules are provided for 400-V application. A 2-kW dc–dc boost converter switched between 400 kHz and 1 MHz achieved a power density of 220 W/in³ and an efficiency of 98.4% by employing the switch module.

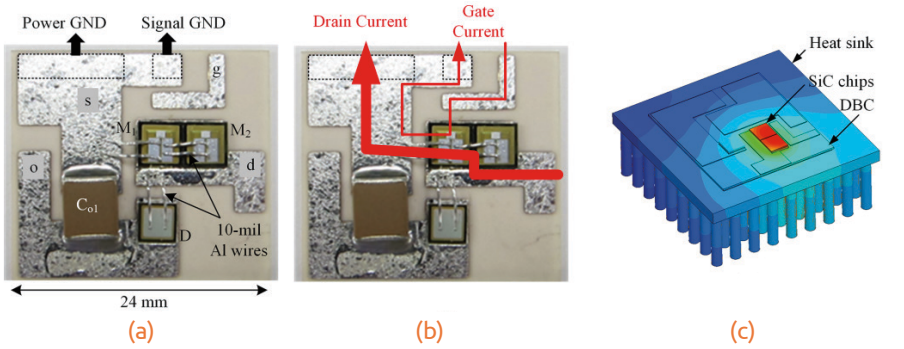


Fig. 1. (a) Photograph of DBC module. The MOSFET's and diode are SiC (M_1 and M_2 : CPM2–1200–0080B from Cree, Inc., 1.2 kV–31.6 A, 80 mΩ on resistance, die; D: CPW5–0650-Z050B, 650 V–50 A, die). Source conductor has two different joints to motherboard PCB to reduce common-source inductance. (b) Separate drain and currents. (c) Thermal simulation result from ePhysics.

Comparing a PCB module with a GaN MOSFET, the SiC DBC module in Fig. 1 shows a higher thermal conductivity. The thermal behavior of the DBC module was simulated by Ansys ePhysics to inspect the maximum junction temperature of semiconductor chips and junction-to-case thermal conductivity. Fig. 1 (c) shows that the junction temperature is 65.1° C and the heat sink temperature is 55.7° C when each MOSFET die has a 3.75-W power loss. Junction-to-case and case to-heat sink thermal resistances are calculated as 0.89 and 1.46° C/W, respectively. The total thermal resistance from junction to heat sink is 2.35° C/W, 63% of the 3.71° C/W for PCB module.

The ZVS boost converter using a DBC module is shown in Fig. 2. Capacitors and a gate driver were placed on the top side of the motherboard. Area of 57 mm × 61 mm or 3477 mm² was utilized. A fan, power supply for gate driver, and the magnetic components were assembled to the bottom side of the motherboard fixing the height of the converter as 43 mm. The volumetric power density PD with 2-kW output power is calculated a s P_D = 2000 W/ (3477 mm² × 43 mm) = 220 W/in³.

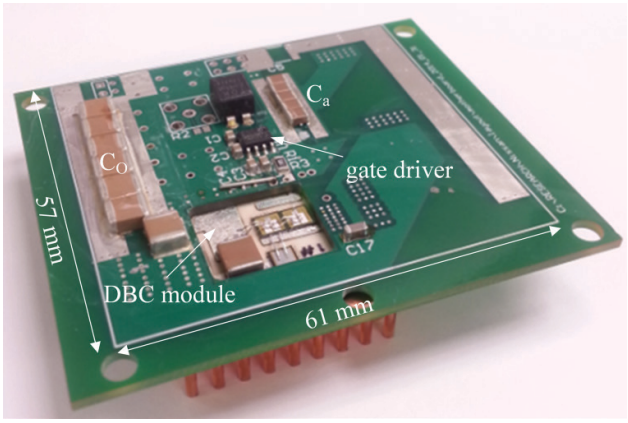


Fig. 2. Top side of 220 W/in³ dc-dc ZVS boost converter with DBC module.

NiCuZn Ferrite Cores by Gelcasting: Processing and Properties

The integration of magnetic components in a high-frequency power electronics converter poses tough challenges because of the limited options of magnetic materials and manufacturing processes that make cores that have low core losses, high flux densities, and large permeability in and beyond the megahertz range. NiZn ferrite (including NiCuZn ferrite) is widely adopted in the megahertz frequency range because of its high electrical resistivity as well as high permeability. However, the traditional process for making ferrite components requires a high sintering temperature (> 900° C) and high pressure. For example, a popular NiZn ferrite, 4F1, needs to be fabricated at a high pressure in the megapascal range to form the core shape and then sintered over 1400° C to get desired properties. The process complexity prevents fabrication of magnetic cores having novel designs for shaping magnetic flux and thus impedes their integration in a power converter.

In this study, we used the pressure-less gelcasting process to fabricate a NiCuZn ferrite aimed at simplifying the integration of magnetic components for power electronics converters. A commercial NiCuZn powder was gelcast into toroid-shaped magnetic cores and then sintered at different peak temperatures. Both the complex permeabilities and core-loss densities at high magnetic flux density and high frequency were measured.

By varying the sintering temperature from 900° C to 1000° C, the real part of the permeability of the gelcast NiCuZn core could be improved from 44 to 77. For the gelcast core sintered at 950° C, its core-loss density at 5 MHz was found to be 50% lower than that of a commercial NiZn (4F1) ferrite core. Because of its ease, flexibility, and scalability, gelcasting has the potential to enable the integration of novel designs of magnetics for shaping and coupling magnetic fluxes aimed at achieving higher efficiency and power density of high-frequency power electronics converters.

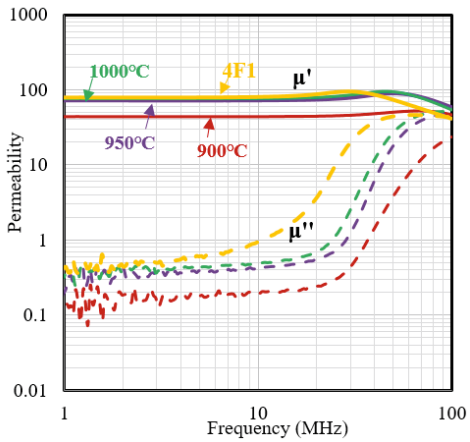


Fig. 1. Complex permeability of gelcast cores sintered at different peak temperatures and that of 4F1 core.

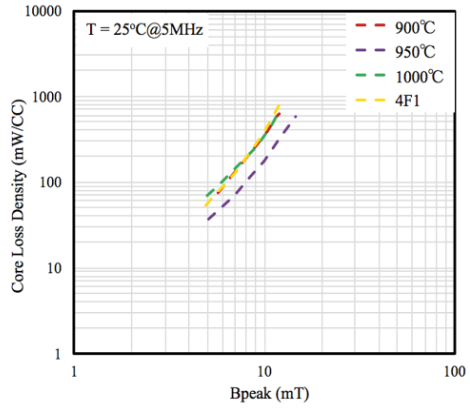


Fig. 2. Core-loss densities of sintered cores by gelcasting and NiZn ferrite (4F1) core at 5 MHz.

Design and Development of a Novel, High-Density, High-Speed 10 kV SiC MOSFET Module

It has been shown that Silicon Carbide (SiC) semiconductors can increase the efficiency, decrease the size, and reduce the cost of power electronic systems. One notable feature of SiC is its high breakdown electric field, which is ten times greater than that of silicon (Si). This characteristic allows for the fabrication of high-voltage power devices. Wolfspeed, a Cree company that has been at the forefront of the development of high-voltage SiC devices, has recently released its third-generation 10 kV, 350 mΩ SiC MOSFETs.

At present the performance of these unique devices is limited by standard module packages that were originally developed for slower, lower density Si devices. This work aims to fabricate an optimal package for 10 kV SiC MOSFETs that would have minimal parasitic elements to allow for good transient performance, low thermal impedance to effectively remove the heat from the devices, and a small footprint to achieve high power density. The 10 kV rating of these MOSFETs means that high electric fields will be present within the module. Accordingly, care must also be taken to design a layout that will reduce the concentration of these electric fields.

To achieve higher density, and reduce parasitics, the antiparallel diode is eliminated. Instead, the superior reverse conduction characteristics of the SiC MOSFETs are utilized. To minimize the parasitics, molybdenum posts and direct bonded aluminum (DBA) substrates are used for the module connections (forming a planar structure), in place of wirebonds. Embedded capacitors further improve the transient performance of the devices. Finally, to minimize the peak electric field that occurs at the triple point of the DBA substrates, two DBAs are stacked together. The designed power module, which has gate- and power-loop inductances of just 3 nH, is shown in Fig. 1.

A proper package will also consider the system integration. For instance, when designing the power module, the interface to the gate driver and dc bus bar must be considered. Fig. 2 shows a 2D electrostatic simulation of two different types of power terminations. Due to the high density of the power module, when using pins with small diameters, the electric field concentration exceeds the dielectric strength of air (3 MV/m). By placing conductive elliptical shields around the pins, the electric field can be more uniformly distributed. In this example, the electric field is reduced by nearly half. This results in a higher partial discharge inception voltage.

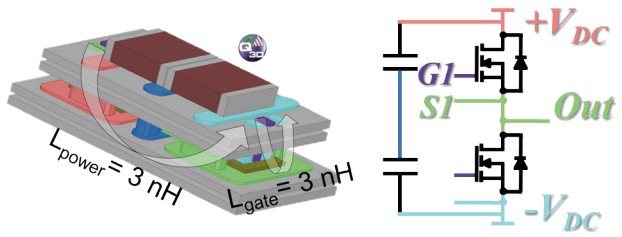


Fig. 1. Design of a planar, 10 kV power module.

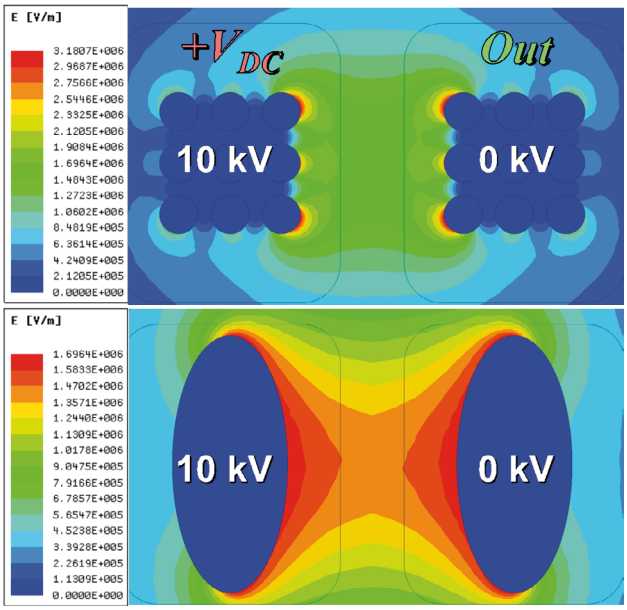


Fig. 2. 2D electrostatic simulation of pin power terminals without (top) and with (bottom) elliptical shields.

Wide Bandgap High-Power Converters and Systems Nuggets

Impedance-Based Analysis of Active Frequency Drift Islanding Detection for Grid-Tied Inverter System

Study of the Predictive Capability of Modular Multilevel Converter Simulation Models under Parametric and Model Form Uncertainty

Low-Frequency Terminal-Behavioral Modeling of Three-Phase Converters

Small-Signal Terminal-Characteristic Modeling of Three-Phase Droop-Controlled Inverters

Stability Criterion of Droop-Controlled Parallel Inverters Based on Terminal Characteristics of Individual Inverters

Decoupled αβ Model of Modular Multilevel Converters (MMCs)

Modeling and Analysis for Input Characteristics of Line-Frequency Rectifiers

Design of a Two-Switch Flyback Power Supply Using 1.7 kV SiC Devices for Ultra-Wide Input-Voltage Range Applications

Investigation of Medium-Voltage High-Power Industrial Drives in Presence of Medium-Voltage SiC MOSFETs

Integrated Switch Current Sensor for Shortcircuit Protection and Current Control of 1.7-kV SiC MOSFET Modules

Design of a SiC-Based Modular Multilevel Converter for Medium Voltage DC Distribution System

Analysis of D-Q Small-Signal Impedance of Grid-Tied Inverters

A Transformer-less Single-Phase Bidirectional Interface Converter to Connect AC and DC Power Distribution Systems

A Frequency Domain Model for Beat Frequency Oscillation Analysis in Microgrid

The Impact of PV Inverter Penetration on Voltage Profile and Power Loss in Medium-Voltage Distribution Systems

Capacitor Voltage Ripple Reduction with State Trajectory Analysis for Modular Multilevel Converter

Predicting the Behavior of a High Switching Frequency SiC-Based Modular Power Converter Based on Low-Power Validation Experiments

On-line Measurement of Inward - Outward Impedances for Stability Assessment

Application of Impedance-Based Stability Criterion in Power Systems with Multiple STATCOMs in Proximity

Critical-Mode-Based Soft-Switching Modulation for Three-Phase Inverters

Impedance-Based Analysis of Active Frequency Drift Islanding Detection for Grid-Tied Inverter System

Islanding detection is an important function of distributed generation units because of the requirements of grid code compliance. On the other hand, the islanding detection function gives a distributed generation unit the ability to adjust its operation mode according to grid conditions. For example, a three-phase inverter can work as a current source when it is connected to the grid via some grid impedance Z_g. It can also work as a voltage source to feed the local load (Z_L) when it is disconnected from the grid due to grid faults. This paper focuses on the current source operation and presents an impedance-based analysis of the active frequency drift (AFD) islanding detection method.

An impedance-based analysis for the AFD islanding detection method has been proposed in this paper. The output impedance of a grid-tied inverter was modeled in the d–q frame. The model shows that the Z_{qq} of the inverter output impedance is a negative incremental resistor at dc. The magnitude of this resistor is inversely proportional to the real power injected by the inverter with a scale factor of the square of the terminal voltage value. Coincidentally, the most difficult islanding detection scenario occurs when the real power consumed by the local load matches with the real power generated by the inverter. Under such conditions, the magnitude of Z_{qq} is equal to the dc impedance magnitude of the local load, and an impedance interaction occurs during an islanding event. The AFD method utilizes this impedance interaction. It further decreases the phase of Z_{qq} with a big value of feedforward gain N. Under islanding conditions, due to a lack of phase margin, the inverter system becomes unstable with a frequency drift away from its steady state. Based on the impedance of the inverter, it can be concluded that the grid-tied inverter with the AFD islanding method has the potential to destabilize the grid-connected inverter system when the grid is weak. Experimental results verify this analysis.

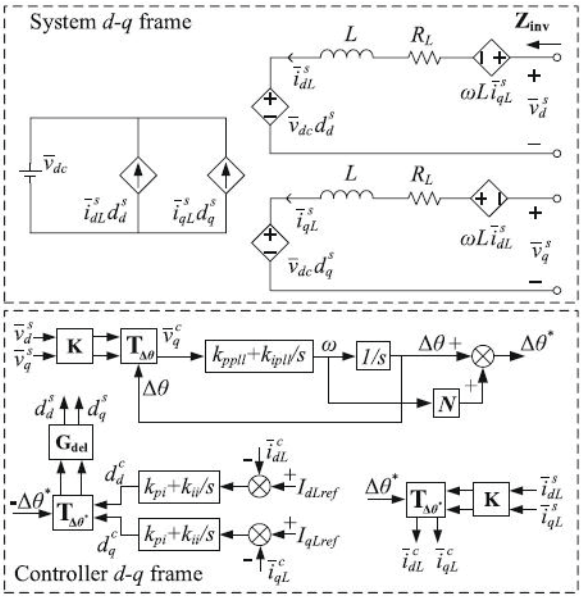


Fig. 1. Average model of an inverter with the PLL-based AFD method.

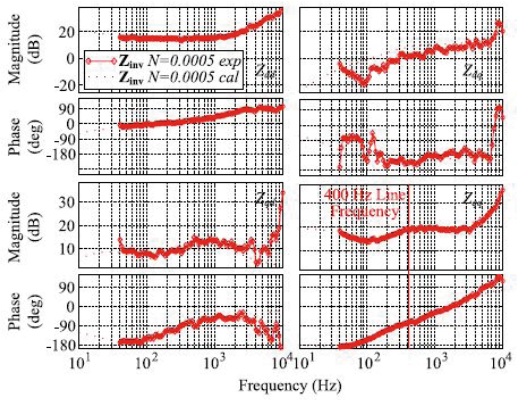


Fig. 2. Measurement results of Z_{inv} for the PLL-based AFD method with feedforward gain N = 0.0005, showing very good matching between the model and the measurement results.

Study of the Predictive Capability of Modular Multilevel Converter Simulation Models under Parametric and Model Form Uncertainty

The modular multilevel converter (MMC) has become a preferred choice for medium-voltage applications as it has several advantages when compared with two-level voltage source converters. Advantages such as ease of assembly, excellent harmonic performance, distributed energy storage, and a near ideal current and voltage scalability, make this converter the most promising converter technology for high-voltage direct current (HVDC) transmission systems.

Modeling and simulation techniques are broadly used to fine-tune the design of the power stage and control system of MMCs. Nonetheless, due to the potential sources of uncertainty in modeling and simulation, simulations are not entirely relied on, and experiments are oftentimes carried out using scaled-down laboratory prototypes. The actual predictive capability of simulation models remains unknown until the complete system is available for conducting validation experiments. Overestimating the required design margins is a common solution to deal with the unknown credibility proficiency of simulation models and ensures the safe operation of power converters.

The primary purpose of this paper is to eliminate the use of heuristic safety factors in the design of MMCs by understanding the relationship between the total uncertainty in simulation results and the number of power electronics building blocks (PEBBs) in each arm. This uncertainty is considered as the expected variation of the actual system performance from the predictions made from modeling and simulation. The scaled-down laboratory prototype and simulation model of an MMC with up to two PEBBs per arm is used to predict the expected range for different system responses of the MMC with a high number of PEBBs in each arm.

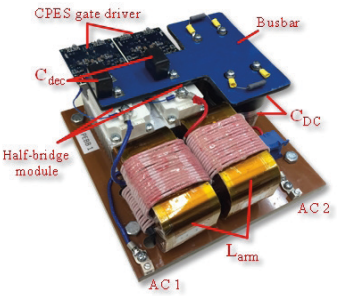


Fig. 2. Hardware prototype of PEBB.

Based on the analysis given in this paper, MMCs that are designed with more PEBBs in each arm do not necessarily require a greater margin for the design variables of interest. Accordingly, the heuristic safety factors in the design of MMC can be replaced by the estimated total uncertainty for the selected design variables. This may result in further minimizing the design margins and design improvements, while the safe operation of the converter is ensured via the gained confidence in the predictive proficiency of MMC simulation models.

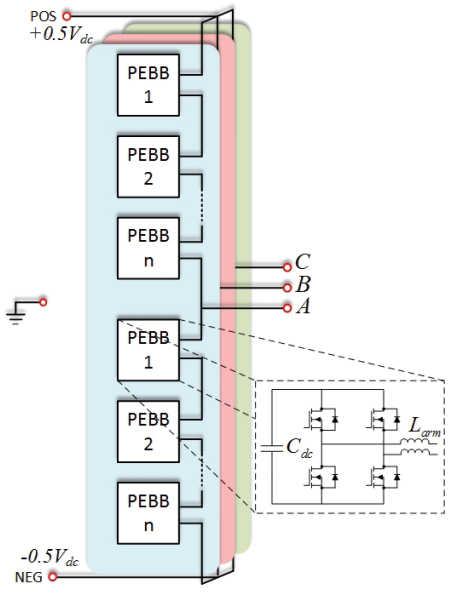


Fig. 1. Circuit configuration of MMC.

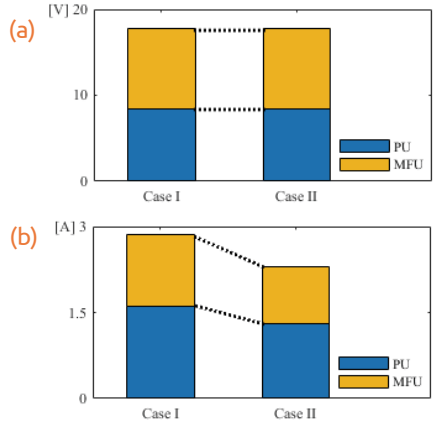


Fig. 3. Total uncertainty associated with the final prediction of: (a) Maximum dc capacitor voltage of the PEBB, and (b) peak arm current for Case I: 1PEBB/arm and Case II: 2PEBB/arm.

Low-Frequency Terminal-Behavioral Modeling of Three-Phase Converters

The Frequency-domain terminal-behavioral modeling of ac systems is unquestionably attracting more and more interest in engineering practices. New electronic power distribution systems built for airplanes, ships, electric vehicles, data-centers, and even homes, dominantly comprise a variety of power electronics converters with very different dynamic characteristics. If their behavior is not examined carefully before the system is integrated, instability can become one of the major concerns. This work addresses low-frequency terminal-behavioral modeling of three-phase converters, The dynamics can be captured on-line, in a non-intrusive way, and later decoupled from the source and load in order to get an unterminated model of a converter, or even a larger system.

The three-port network can be directly used to build the small-signal linear model of the dc-ac converter around the particular operating point (Fig. 1). The four matrices of the transfer functions can be defined: G_o - audio susceptibility, Z_o - output impedance, Y_i - input admittance, and H_i - back current gain. Nine un-terminated transfer functions describe the dynamics of the converter, however, they have to be decoupled, or "unterminated", in order to fully characterize the dynamics of the particular converter. Eq. 1 presents a generalized linear transformation that gives the un-terminated transfer functions from the measured, terminated ones (denoted with the letter *m* in the index) for any ac-ac, ac-dc, dc-ac and dc-dc converter.

The experimental results obtained using the inverter are shown in Fig. 2, demonstrating a very good match between the model and the experimental waveforms.

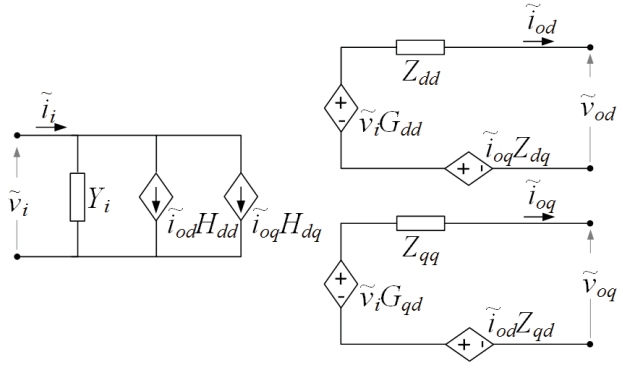


Fig. 1. Three-port network terminal behavioral model.

$$\begin{bmatrix} \mathbf{G}_o^x & -\mathbf{Z}_o^x \\ \mathbf{Y}_i^x & \mathbf{H}_i^x \end{bmatrix} = \begin{bmatrix} \mathbf{G}_{om}^x & -\mathbf{Z}_{om}^x \\ \mathbf{Y}_{im}^x & \mathbf{H}_{im}^x \end{bmatrix} \cdot \left[\mathbf{T}^x\right]^{-1}$$

$$\text{where } x = \{ac-ac,\ ac-dc,\ dc-ac,\ dc-dc\}$$

Eq. 1.

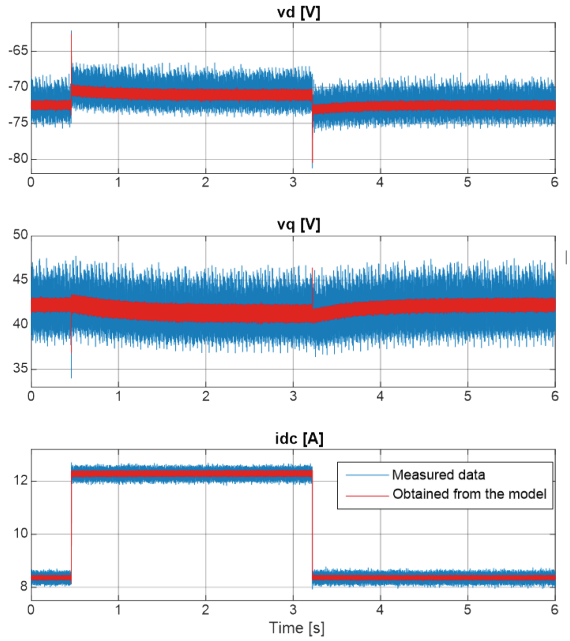


Fig. 2. dc-ac converter time domain responses in d and q axes for the given load step, and comparison with the terminal-behavioral model output.

Small-Signal Terminal-Characteristic Modeling of Three-Phase Droop-Controlled Inverters

Droop-controlled inverters are widely employed as power sources in three-phase ac power electronics systems, such as distributed power generation systems, but the interaction between the source and the load may lead the overall system to be unstable. Terminal-characteristic-based stability criteria are very attractive for analyzing the stability of three-phase ac power electronics systems. However, the systems, composed of droop-controlled inverters, exhibit the dynamical variation of fundamental angular frequencies, and the existing stability analysis approaches are suitable only for systems with constant fundamental angular frequencies.

This paper proposes a small-signal terminal-characteristic model of the three-phase droop-controlled inverter in the synchronous reference frame (SRF), covering the behavior of fundamental angular frequency. Firstly, the droop-controlled inverter can operate in both voltage mode and current mode, where its terminal characteristics are totally different. Since the inverters have different excitations and responses, they are modeled respectively in this paper. Secondly, in each operation mode, the small-signal model of the power stage and the control system are modeled in the system SRF aligned to the terminal ac voltage, considering the dynamic of fundamental frequency. Finally, we created full small-signal models of the three-phase droop-controlled inverter that covers the behavior of the fundamental frequency in both the power stage and control system in both operation modes, and the analytical expressions of the terminal-characteristics are derived. The proposed model is very beneficial for stability analysis of the distributed generation, covering the droop-controlled inverter in both grid-tied mode and islanded mode, which will be investigated in future publications.

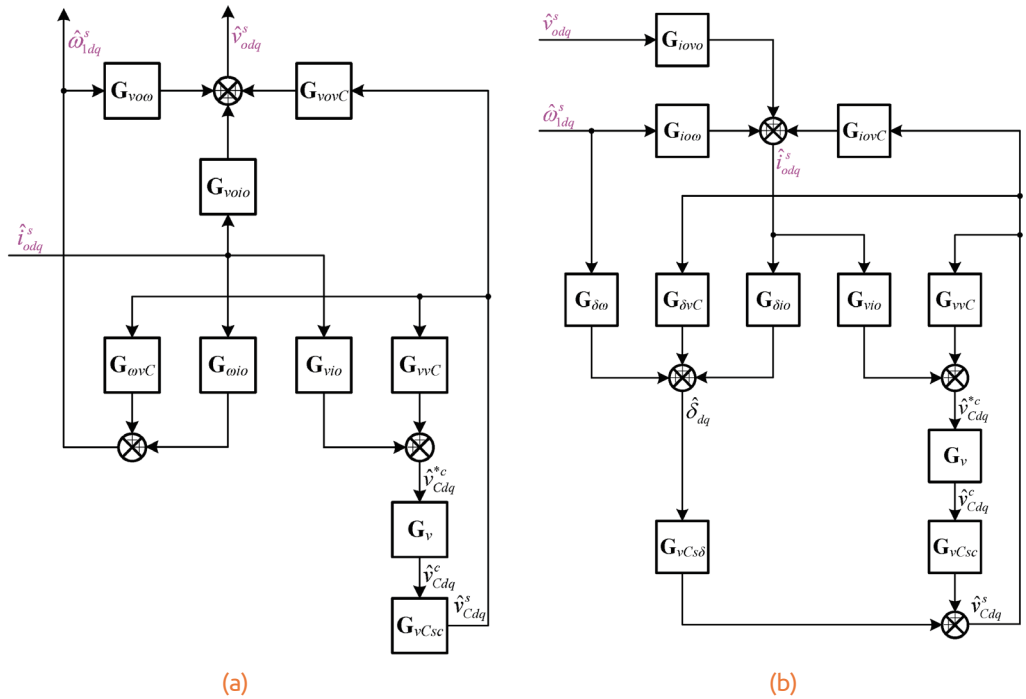


Fig. 1. Block diagram of the small-signal model of the three-phase droop-controlled inverter in (a) Voltage-mode operation and (b) Current-mode operation.

Stability Criterion of Droop-Controlled Parallel Inverters Based on Terminal Characteristics of Individual Inverters

Droop-controlled parallel inverters are widely adopted in micro-grids due to their high reliability and low cost. However, the interaction among the inverters can cause the whole system to be unstable, even though each individual inverter can operate stably in stand-alone mode. A lot of work has been done to analyze the stability of parallel inverters with droop control through the state-space approach originally used in conventional electrical power systems. For this existing approach, it is necessary to have the knowledge of the inside parameters of each individual inverter in advance, while in practical applications it is inconvenient to obtain the internal structure and parameters.

To overcome this problem, this paper proposes a stability analysis approach for the droop-controlled parallel inverters based on the terminal characteristics of individual inverters. At the beginning, the terminal characteristics of individual inverters with droop control are defined in the system synchronous reference frame (SRF), which can be represented by the transfer function between the output current and output voltage, and the transfer function between the output current and fundamental angular frequency. Then, the terminal characteristics of the whole parallel system are derived, including the characteristics of each individual inverter. Furthermore, a stability criterion is proposed for the parallel inverters based on the terminal characteristics of each individual inverter according to the Generalized Nyquist Criterion. Finally, the proposed terminal characteristics and stability criterion for droop-controlled parallel inverters are verified in the frequency domain.

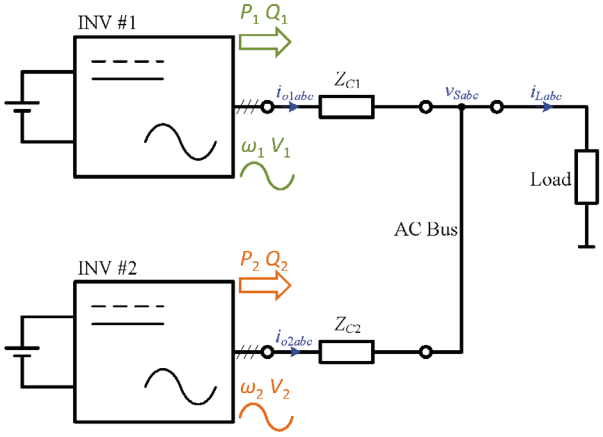


Fig. 1. Typical configuration of droop-controlled parallel inverters.

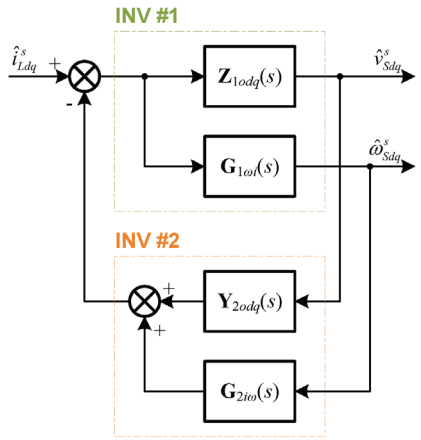


Fig. 2. Small-signal block diagram of the parallel inverters based on terminal characteristics of individual inverters.

Decoupled αβ Model of Modular Multilevel Converters (MMCs)

The modular multilevel converter (MMC), illustrated in Fig. 1, is widely adopted in high-voltage applications because of its simplicity and modularity. However, the current and power flows are very complicated. As a result, methods proposed for capacitor reduction, which is required to store line-frequency related circulating energy, have all gone through complicated mathematical derivation.

A state-plane analysis was proposed to visually illustrate the convoluted current and power flows. This analysis was able to explain for the first time the circulating energy related to source and load as well as the circulating energy swapping between capacitors. In addition, he showed that the two different kinds of circulating energy can be decoupled into two orthogonal axes, v_α and v_β.

Based on the state-plane analysis, this paper proposes a decoupled αβ model of MMC, as shown in Fig. 2. In this model, the input and output are clearly identified, and v_α and v_β represent the total capacitors in one phase. Since $v_\beta \gg v_\alpha$ because of the strong dc component, the proposed model clearly shows the major power flow is from V_{in} through v_β to R_o. Therefore, when input power p_{in} and output power p_o are not balanced, v_β needs to compensate the difference.

The model also shows that d_{in} regulates the average capacitor voltage v_β and controls i_{in}. However, d_{in} also generates circulating current on v_α. Similarly, d_o regulates i_o and generates circulating current on v_α at the same time. As a result, when the two controlled current sources in the v_α loop are not balanced, the difference becomes the circulating power that swaps between the two capacitors.

The proposed model accurately explains the power flow and the causes for each component of the circulating energy. Therefore, it paves the way for advanced control and a systematic understanding of MMC.

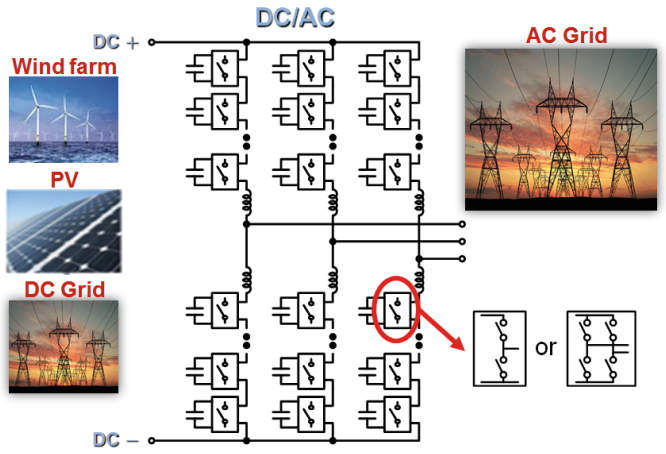


Fig. 1. Schematic of a modular multilevel converter.

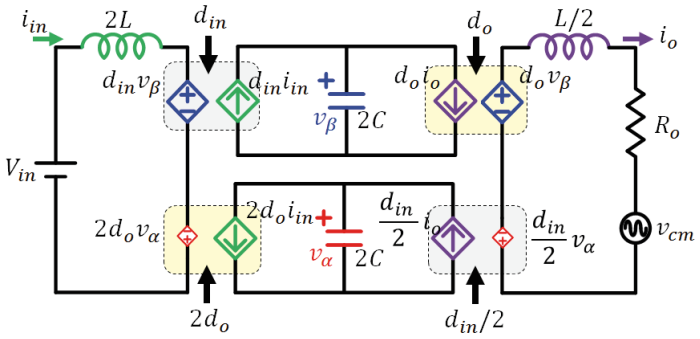


Fig. 2. Proposed decoupled αβ model.

Modeling and Analysis for Input Characteristics of Line-Frequency Rectifiers

Impedance is very important for power electronic systems because of the close relationship between impedance and system stability. The line-frequency rectifiers are commonly used ac-dc interfaces in electrical power systems. For the line-frequency rectifier with a sinusoidal voltage perturbation excitation at the input terminal, input current contains not only perturbation frequency, but also multiple additional frequency components. Therefore, input characteristics of line-frequency rectifiers are actually single input multiple output (SIMO) in frequency domain. However, input current perturbation is traditionally simplified into a sinusoidal signal at perturbation frequency by ignoring other additional frequency components. The obtained impedance models mainly focus on frequency regions below line frequency in order to describe the SIMO input characteristics of line-frequency rectifiers and to develop an impedance model that could be applied beyond switching frequency.

This paper proposes a new model by using the harmonic balance method. Detailed analysis indicates that input admittance of the line frequency rectifier in high frequency regions acts like a resistor rather than an inductor. The simulations validate the accuracy and effectiveness of the proposed model.

For nonlinear power electronic converters, the definition of impedance makes classical control theory easy to use. This solves many problems and brings lots of convenience, but the simplification of real input characteristics also has some limitations. It has been reported that the output impedance model fails to analyze the multi-phase voltage regulator's characteristics when there is a load transient whose frequency is beyond switching frequency and power electronic based systems' interactions in switching frequency range.

Fig. 1 shows the simulated input current and voltage waveforms with perturbations. Simulation results coincide with theoretical values, which validates the accuracy of the proposed model.

In regards to the input current, if only taking into consideration the component at perturbation frequency, the describing function (input admittance) $i_{in}(f_x)/v_{in}(f_x)$ can be obtained, as shown in Fig. 2. The figure shows that the highest gains appear around line frequency and the distance between peak points and line frequency is resonant frequency of output low pass filter.

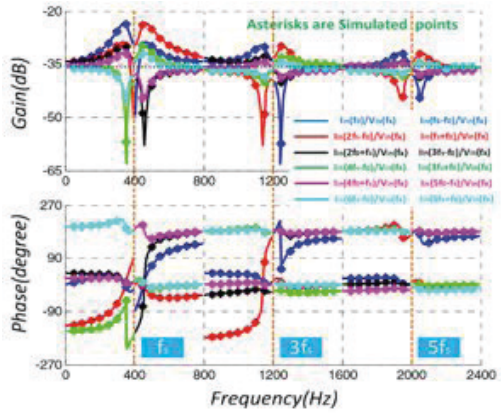


Fig. 1. Simulation for the proposed model.

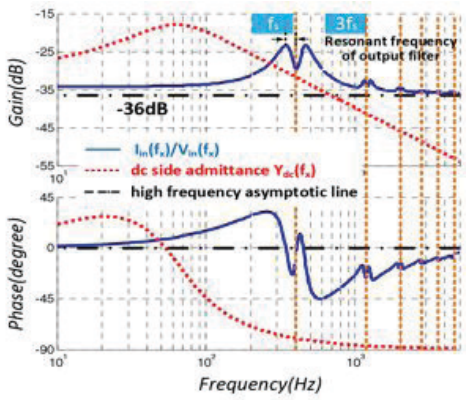


Fig. 2. Input admittance of line-frequency rectifier.

Design of a Two-Switch Flyback Power Supply Using 1.7 kV SiC Devices for Ultra-Wide Input-Voltage Range Applications

This paper presents the design and evaluation of a two-switch flyback power supply with an ultra-wide input voltage range (230–1300 V), fed from the floating dc bus of power electronics building blocks (PEBB) in medium voltage (MV) modular multilevel converter (MMC) applications. Rated at 80 W, 48 V output, and operating at 50 kHz, the proposed converter uses 1.7 kV SiC devices and a planar PCB winding transformer to achieve a low-profile form factor. Further, a pre-charge circuit and start-up sequence are developed as well, enabling the two switch flyback converter to wake up at 230 V, as shown in Fig 2. Experimental results are presented for verification and evaluation purposes.

The two-switch flyback topology provides the best trade-off in terms of performance and complexity among other topologies like LLC or full-bridge. With reference to Fig. 1, the benefit of this topology is that the over-voltages on the power switches are clamped to the dc bus by diodes D1 and D2, thus allowing the use of power switches with a breakdown voltage of 1.5 kV. Since this circuit topology is basically hard-switching, SiC MOSFETs (CREE C2M-1000170D 1.7 kV/5 A) have been chosen to reduce the losses of Q_1 and Q_2. Another feature of the two-switch flyback converter is that during the clamping period the leakage energy of the transformer is returned back to the source, effectively eliminating the need for dissipative snubber circuits.

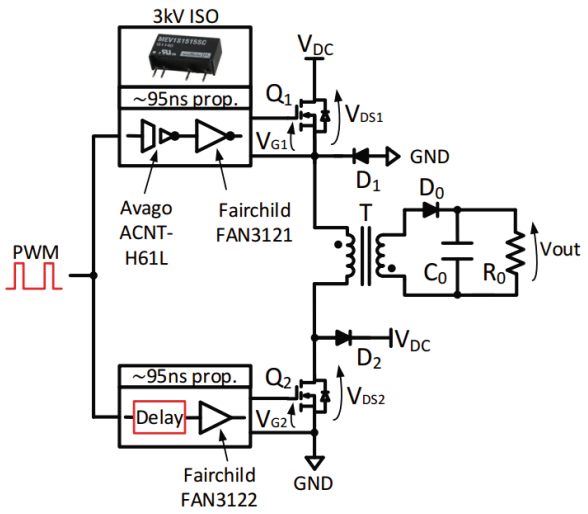


Fig. 1. Two-switch flyback schematic and gate drivers implementation.

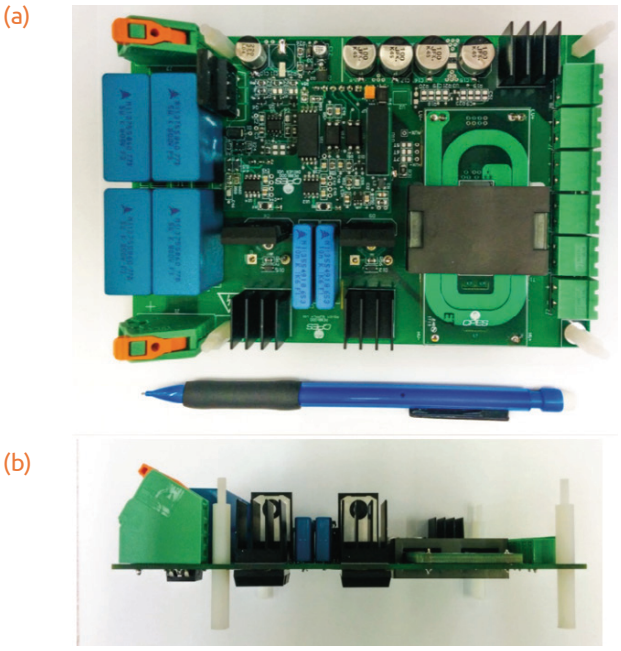


Fig. 2. Picture of PEBB prototype (a) top view (b) side view.

Investigation of Medium-Voltage High-power Industrial Drives in Presence of Medium-Voltage SiC MOSFETs

Wide-bandgap semiconductors such as Silicon Carbide (SiC) appear to be game-changing devices in medium- and high-power applications where they enable operations at higher switching frequencies by switching faster, having lower conduction losses and maintaing higher junction temperatures. In addition to this, Si semiconductors, in comparison to SiC devices have a high thermal conductivity and a high breakdown field thus creating a better performance. The aforementioned advantages have led to the commercialization of several generations of low voltage SiC power semiconductor devices in past years. However, at medium voltage the SiC switches are not fully commercialized and are still under development by a number of companies around the world.

The main application areas of SiC MOSFETs that are expected to replace existing Si IGBTs are industrial motor drives, downhole drilling and grid-tied inverters. Due to higher operating temperatures that enable higher switching frequencies, the motor drives featured by SiC MOSFETs are expected to be more efficient and have a higher power density. In downhole drilling applications where cooling systems have restrictions, SiC MOSFETs can feature better performance because of higher maximum operating temperatures. Last but not least, with higher switching frequencies enabled by the SiC MOSFETs, the size of the passive filters can be significantly reduced and power quality can be increased on grid-tied converters such as PV inverters.

This paper tries to investigate the impact of emerging medium-voltage SiC MOSFETs on converters used for an industrial drive at medium-voltage and high-power. For this purpose, non-commercialized SiC MOSFETs are characterized, and three different topologies are designed for a motor drive using tested SiC MOSFETs and existing commercial Si IGBTs. The following topologies are designed for industrial drives at 4.16-, 6.9- and 13.8 kV voltage rating and 3- and 5 MVA power rating: the cascaded H-bridge (CHB) topology, which currently is the most popular topology for medium-voltage drives; the modular multilevel converter (MMC), which is the state-of-the-art topology in multilevel converters; and the five-level active neutral point clamped (5-L ANPC) topology, which is introduced by ABB and is being used in ACS2000 drives. By selecting different voltage and power ratings for converters, the purpose of this study is to find the effective trend of the SiC on motor drives versus voltage and power rating, and also to have a comparison between the different topologies themselves under different conditions.

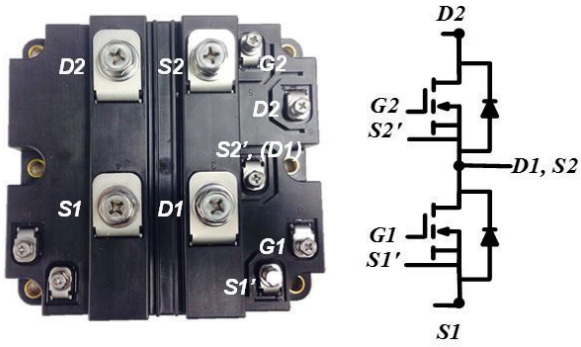


Fig. 1. 3.3 kV 400 A SiC MOSFET tested for evaluation of different topologies using SiC MOSFET. Static and dynamic performance characterization is done on the module, and results are used as input for topology evaluation.

The evaluation mainly tries to investigate the impact of the SiC technology on the efficiency and power density of industrial drives. For the converters designed at a given voltage and power rating, efficiency, power density (composed of size of capacitors, heat sinks, etc.), Joule per kVA (for installed capacitors) and total installed semiconductor die size (for a measure of semiconductor utilization) are compared to each other.

Integrated Switch Current Sensor for Shortcircuit Protection and Current Control of 1.7-kV SiC MOSFET Modules

The SiC MOSFET, as a wide-bandgap device, has superior performance for its high breakdown electric field, low on-state resistance, fast switching speed and high working temperature. High switching speed enables high switching frequency, which improves the power density of high power converters. The gradual cost reduction and packaging advancement brings a promising trend of replacing the conventional Si IGBTs with SiC MOSFET modules in high power applications.

As previous research shows, DeSat protection is not suitable for the SiC MOSFET modules. Direct measurement of the device current can be a better solution as long as the switch current sensor can provide a large enough bandwidth (BW), low response delay and fair accuracy. Rogowski's coil-based switch current sensor is able to meet the requirement for shortcircuit protection of the SiC MOSFET modules. This paper also designs the sensor for high accuracy targeting at current control, which request another set of specifications (Fig. 1). The switch current provides more than enough information for current control. The excessive information can be used as sensor redundancy where higher reliability is brought. In medium voltage applications where Power Electronics Building Block (PEBB) based converters or multilevel converter are widely used, a switch current sensor can ease the diagnostics of a damaged device, or help monitoring abnormal devices. However, challenges do exist mainly due to the high dv/dt and the non-ideal performance of the integrator.

As shown in Fig. 2, the final sensor prototype was integrated together with the gate driver on the same board, and validated with excellent performance.

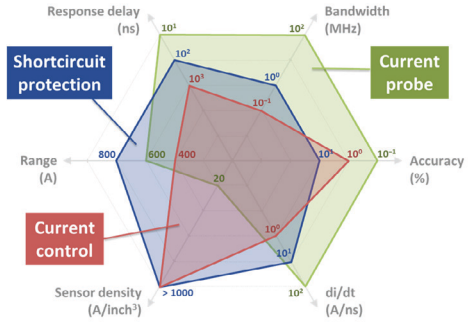


Fig. 1. Design architecture.

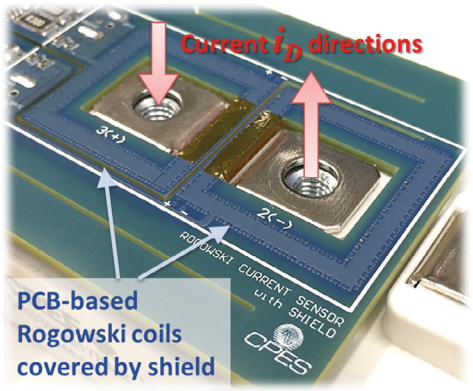


Fig. 2. Current sensor prototype.

Design of a SiC-Based Modular Multilevel Converter for Medium Voltage DC Distribution System

MVDC distribution systems have become increasingly attractive in applications such as offshore wind farm connections, shipboard power systems, railway electrification systems, and grid applications. The MMC on the other hand provides an attractive solution for these systems due to its inherent voltage scalability, excellent power quality, transformer-less operation, distributed energy storage, and its modular design among other advantages.

Currently, Si IGBTs are largely used in this type of converter, in accordance with its low switching frequency requirements and relatively low power density. The latter is perhaps its main shortcoming. This, however has been recently overcome by developing new high frequency and switching-cycle PWM and control schemes that allow the MMC circuit to profit from a high switching frequency operation and achieve high power density. Wide- bandgap (WBG) devices, such as SiC, have consequently become a viable option enabling engineers to fully exploit the benefits of this power conversion solution for MVDC systems.

The converter prototype is shown in Fig. 1. It is able to operate as an inverter or a rectifier with minor control system modifications. Unlike the traditional MMC, there is only one PEBB per arm in the converter shown in Fig. 1 thanks to the use of fast SiC devices. This configuration retains the main properties featured by the MMC, such as distributed energy storage. Despite the reduced number of PEBBs, the converter's passive components do not suffer from harsher requirements due to the fast switching speed of the SiC devices employed, specifically 1.7 kV SiC MOSFETs. In effect, by increasing the switching frequency, the converter still has a high equivalent switching frequency without requiring multiple series-connected modules. With it, a 1 kV dc bus can be generated, which is under consideration for use in commercial and military marine applications.. Higher voltages can easily be achieved by increasing the number of PEBBs per arm.

The PEBB design, control methods and hardware, pre-charge and discharge, protection will be included in the final paper.

Different functional tests need to be conducted throughout the design and construction process. First, each busbar undergoes a High Potential (HIPOT) test to verify the insulation. They can withstand at least 6 kV from positive to neutral or negative to neutral. Then the Double Pulse Test is performed on every top or bottom switch of the SiC module and every channel of the gate driver to verify the switching performance and protection action. It is tested under a 1 kV drain-source voltage and a 50 A drain current, which is close to normal operation. Then each PEBB is operated as an inverter with an open-loop control to verify the modulation and thermal behavior. Fig. 2 shows the primary test results of the whole converter prototype, including capacitor voltages, arm currents and circulating current from the same phase and three-phase ac current. It was operated as an inverter with a 300 V dc source.

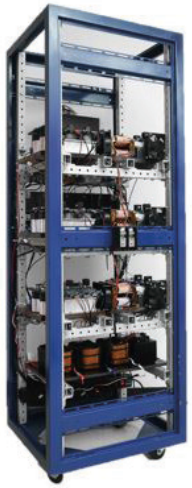


Fig. 1. Hardware prototype of a MMC.

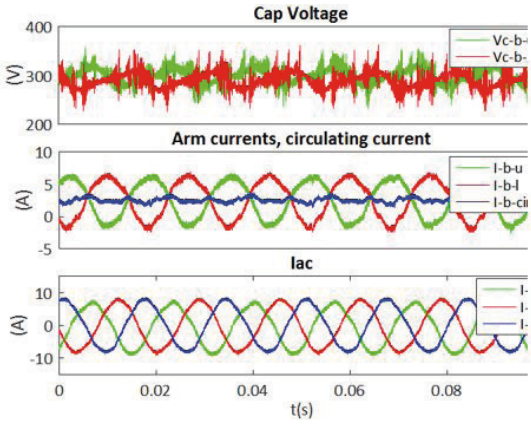


Fig. 2. Inverter test results.

Analysis of D-Q Small-Signal Impedance of Grid-Tied Inverters

Grid-tied inverters are the key components that deliver renewable energy to the grid. They are typically controlled as current sources injecting current to the grid. With the increasing prevalence of renewable energy resources, power quality and stability issues induced by grid-tied inverters become more and more important. Harmonic pollution can happen due to the interaction between inverter and grid impedance. Large grid impedance can destabilize the inverter system. In order to deliver power to the grid, the frequency and phase angle of the inverter output current should synchronize with the grid voltage, which is usually served by a phase-locked loop (PLL). Some recent literature discovered that PLL has a negative impact on the system stability.

This paper presents an analysis of the grid-tied inverter small signal impedance in a d-q frame under different control strategies. Influences of PLL, and current and power feedback control to the inverter impedance are discussed. Some important features of inverter impedance are discussed. These features indicate that a grid-tied inverter working as a current source could destabilize the system due to the negative incremental resistor of Z_{qq}. This negative incremental resistor behavior is a result of PLL and current injection. Increasing the PLL bandwidth extends the frequency range of this behavior, and increases in the inverter power level decreases the absolute value of the resistor. A brief simulation example shows that under weak grid conditions, a small increase of the PLL bandwidth can lead the system to unstable conditions. The example also shows how the proposed model can be used to predict such instability. Hardware measurements verify the proposed model. The model gives insight into the grid-tied inverter's behavior in the grid. Harmonic resonance and instability issues reported in the literature can be analyzed using the characterized impedance model.

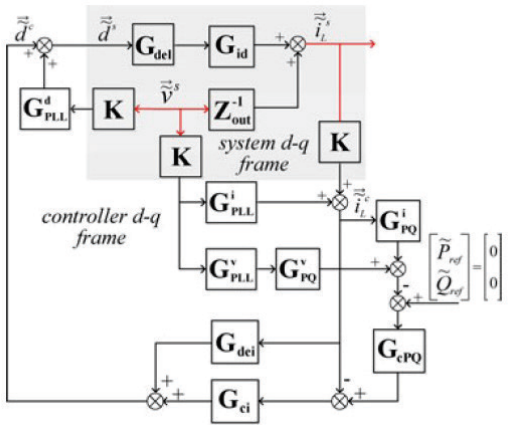


Fig. 1. Inverter small-signal model with PLL, current and power control.

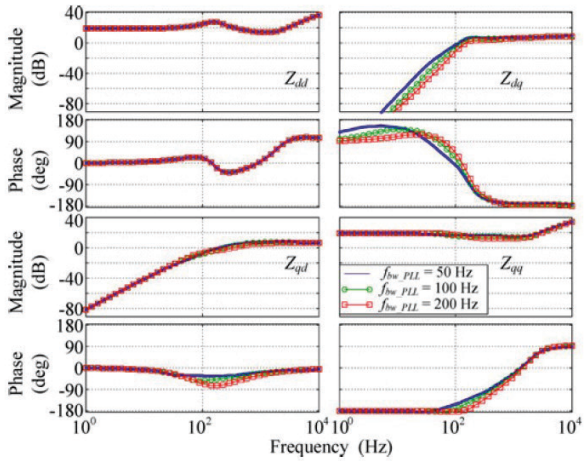


Fig. 2. Impedances of inverter with PLL and power feedback control.

Transformer-less Single-Phase Bidirectional Interface Converter to Connect AC and DC Power Distribution Systems

The dc power distribution system is gaining popularity in future residential, renewable energy, transportation and data center applications because it can be connected to an ac system through a bidirectional interface converter. Besides an ac-dc power conversion, this interface converter fulfills functions like differential-mode and common-mode decoupling, short-circuit current limiting, and both sides of EMI compliance etc.

In this paper, a 5 kW two-stage cascaded single-phase ac-dc converter that connects a 380 V dc system and a 240 V split-phase ac system is used as an example to discuss the converter design for such applications. The cascaded converter uses a full-bridge as the ac-dc stage and a full-bridge as the dc-dc stage to fully decouple the common-mode voltages between the connected ac and dc systems. A floating common-mode noise filter is directly connected between the ac and dc ports to contain the EMI noise emission within the interface converter and suppress the impact from external grounding impedance. The two-stage topology also decreases the capacitance requirement for double-line frequency ripple power in a single-phase power conversion. An experiment prototype is built using the state-of-the-art SiC MOSFETs and tested under full load range to validate the design considerations.

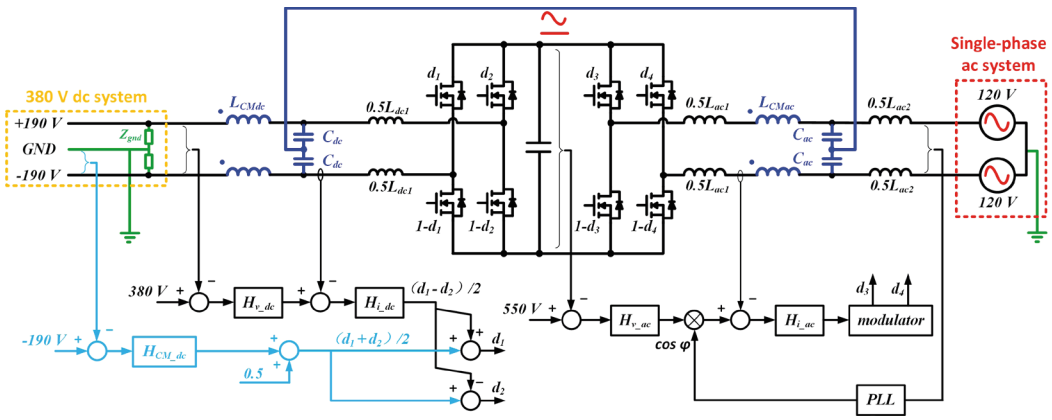


Fig. 1. Two-stage bidirectional single-phase ac-dc converter with complete common-mode decoupling.

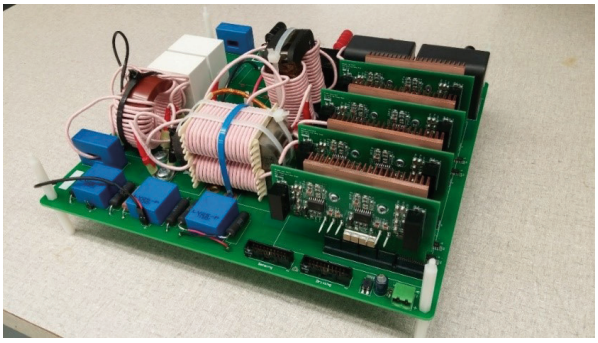


Fig. 2. Picture of 5 kW converter prototype.

A Frequency Domain Model for Beat Frequency Oscillation Analysis in Microgrid

Power electronic converters are typical nonlinear systems in frequency domain. With a perturbation frequency excitation, the current and voltage of power converters in steady state contain not only perturbation but also many sidebands. In a microgrid containing a large amount of power converters, one converter's switching frequency ripples are the other converters' perturbations and beat frequency components will be generated if the switching frequencies of those power converters are different. Since the control loops always take high gains in low frequency regions and the low pass filters almost have no effect on low-frequency disturbances, the beat frequency component has certain values that may be magnified and presented as oscillations. This paper develops a frequency domain model to describe the characteristics of the power converter around a switching frequency range and to analyze the high frequency interactions of power converters in microgrid. The voltage mode controlled boost converters are illustrated as a demonstration. The proposed model indicates that the switching frequency affects the output characteristics of power converters significantly. In a system consisting of two boost converters in parallel, the beat frequency oscillation that traditional output impedance models fail to explain could be accurately predicted by the proposed model. In addition, based on this model, a design guideline is proposed to avoid the potential beat frequency oscillation in parallel system. Simulation results validate the accuracy and effectiveness of the proposed method.

In Fig. 1, the control to output characteristics have periodicity and symmetry; in addition, the component below half switching frequency (represented by f_0) always takes the largest magnitude. It can be seen from Fig. 2 that when perturbation frequency is switching frequency, output voltage only contains dc and switching frequency harmonics. When perturbation frequency is far away from switching frequency, such as 18 kHz and 22 kHz, although there are 2 kHz low frequency component in output voltage waveforms, their magnitude is very small compared with switching frequency ripple.

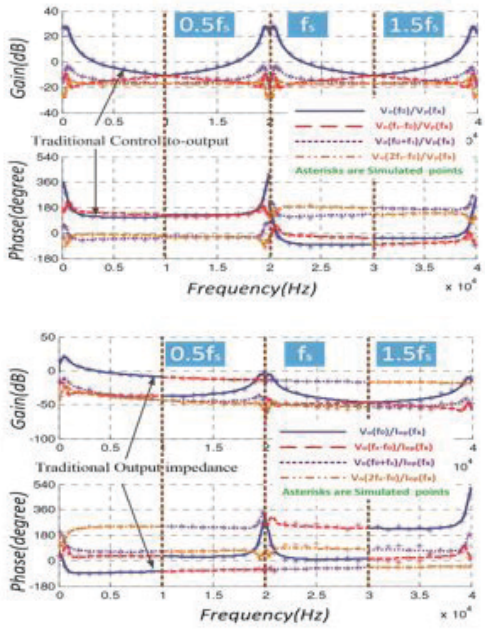


Fig. 1. Output to control characteristics.

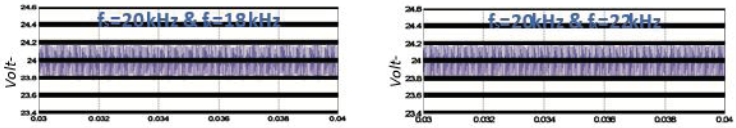


Figure 2 Output voltage waveforms under different output current perturbations

Fig. 2. Output voltage waveforms under different output current perturbations.

The Impact of PV Inverter Penetration on Voltage Profile and Power Loss in Medium-Voltage Distribution Systems

Due to environmental problems caused by fossil fuels, the installation of photovoltaic (PV) systems is increasing rapidly worldwide. The impact on the voltage profile of power distribution systems is the most commonly recognized problem caused by high PV inverter use. Accordingly, significant effort has been devoted to assess the static problems produced in distribution systems.

This paper analyzes the impact of PV generators on the voltage profile and power loss in distribution systems, taking into consideration PV inverters of different capacities installed at different locations and with different local reactive power control strategies. To measure voltage impact, sensitivity matrices are used to compare PV generators connected at different locations. After some approximations, it is shown these matrices are only related to the system topology and impedances, results that are also valid for meshed systems. Guidelines are formulated for PV inverters in terms of geographical location and reactive power control scheme.

Compared to centralized PVs, randomly distributed PVs do not necessarily relieve the voltage profile problem. Performance depends on how PV generators are distributed; integration closer to a substation will definitely reduce the possibility of under voltage and overvoltage. Distributed PVs may cause more or less system power loss compared to centralized PVs, depending on the capacity and PV distribution locations. However, if optimally located, distributed PVs yield less system power loss and are less likely to have conflict problems between minimizing power loss and controlling the voltage profile.

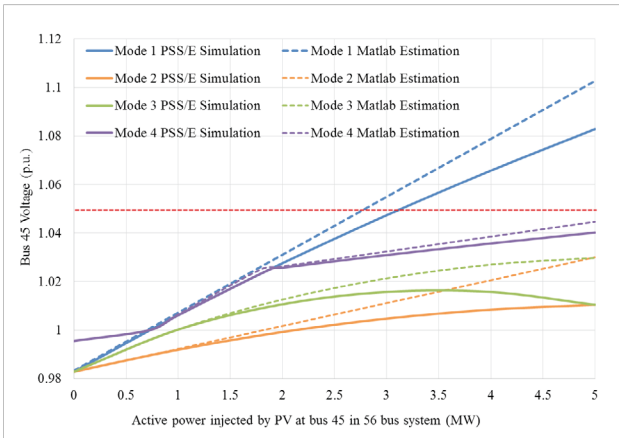


Fig. 1. 56 bus system voltage profile with PV at bus 45.

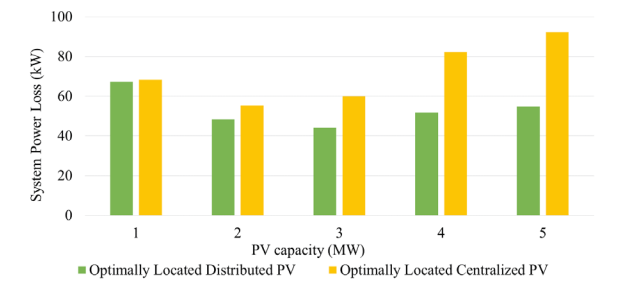


Fig. 2. IEEE 33 bus system power loss comparison for distributed PV and centralized PV.

Capacitor Voltage Ripple Reduction with State Trajectory Analysis for Modular Multilevel Converter

The modular multi-level converter (MMC) is the most prominent interface converter used between the HVDC grid and the HVAC grid. One of the important design challenges in MMC is to reduce the capacitor size. In the current practice, a rather large capacitor bank is required to store line-frequency related circulating energy, even though a number of control strategies have been introduced to reduce the capacitor voltage ripples. In the present paper, a novel control strategy is proposed by using harmonic injections in conjunction with gain control to completely eliminate both the line frequency and the second-order harmonic of the capacitor voltage ripple. Ideally, the proposed method works with the full bridge topology. However, the concept also works with half bridge topology with a significant reduction of line frequency related ripple.

To gain a better understanding of the nature of circulating energy and the means of reducing it, the method of state plane analysis is employed to offer visual support. In addition, the design trade-off between full bridge MMC and half bridge MMC is presented and a novel control strategy for hybrid MMC is proposed. Finally, the work is supported with a scaled down hardware demonstration shown in Fig. 3.

Fig. 1 and 2 show the benefit of the proposed method versus the state-of-the-art to reduce the capacitors ripples.

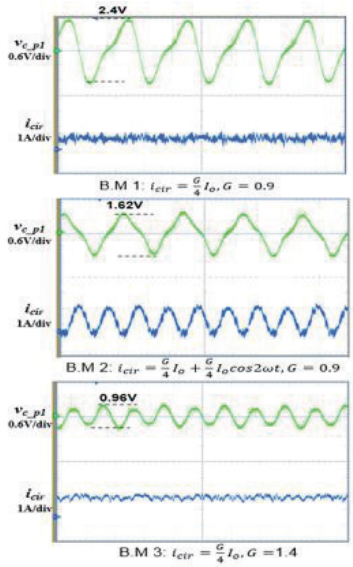


Fig. 1. State-of-the-art waveforms.

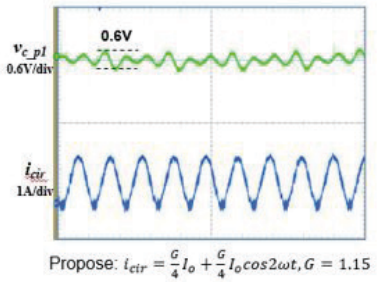


Fig. 2. Proposed control method.

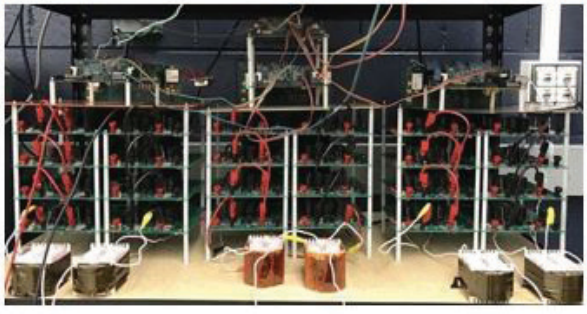


Fig. 3. Experimental setup.

Predicting the Behavior of a High Switching Frequency SiC-Based Modular Power Converter Based on Low-Power Validation Experiments

The development of high- power medium-voltage wide band-gap semiconductor devices (WBG) has facilitated the development of high power density power electronics converters operating at higher voltages and higher switching frequencies, especially when compared to conventional Silicon technology. Therefore, the SiC-based power cells for medium-voltage applications require a faster controller scheme, which is verified by modeling and simulation. In general, modeling and simulation as a set of design and development tools, play a key role in developing different power converter topologies and controller schemes; they represent the fastest and safest way to study a circuit or system, aiding in the research, design, diagnosis and debugging development phases of a power converter.

Power converter simulation models are used jointly with laboratory prototypes, as the simulation itself has not been looked upon as a true substitute for experimental results. However, testing the full-power converter can be prohibitively expensive, or sometimes impossible at the early design stage due to safety considerations or physical constraints. In this paper, low-power validation experiments jointly with modeling and simulation are used to predict the actual behavior of the converter at its full-rated power. Therefore, any possible failures in the converter can be predicted ahead of time without any physical damages and the design can be improved in later iterations

This paper presents a behavior prediction framework in which modeling and simulation together with low-power validation experiments are used as a substitute for a full-power validation experiment of a high-switching frequency SiC-based modular power converter. Different sources of uncertainty in modeling and simulation are identified, characterized, and quantified at full-rated power. A regression-based model is presented which is required to extrapolate the estimated model from uncertainties to the full-power condition and estimate the total uncertainty in modeling and simulation. As a result, the full-power modeling and simulation result can be trusted with a predefined level of confidence. Therefore, it can be looked upon as a substitute for full-power experimental results, especially at early design stages. This predicted interval for a design variable may lead to design improvements. As based on the predicted range, the design margins can be further minimized to better utilize converter components or may need to be increased to ensure safe operation of the converter.

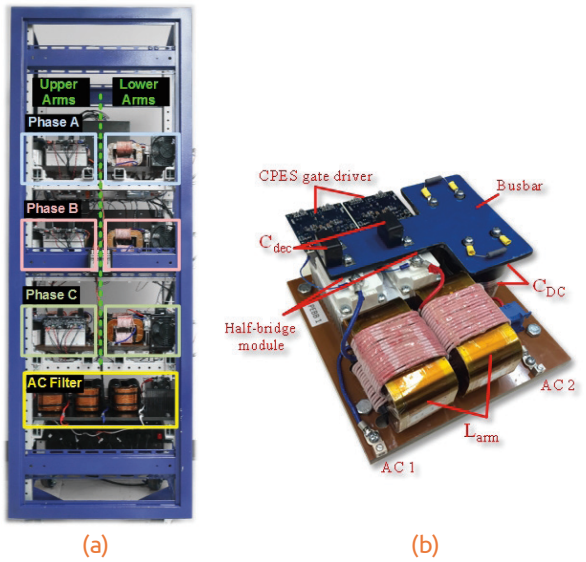


Fig. 1. Hardware prototype: (a) Modular power converter, and (b) PEBB.

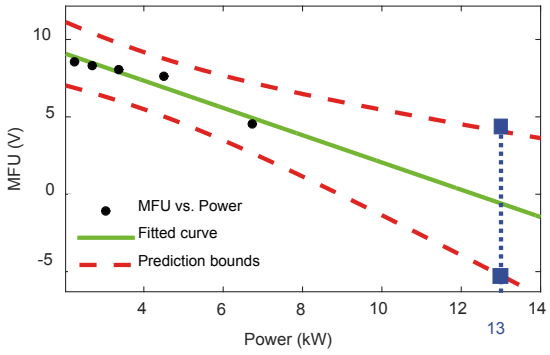


Fig. 2. Extrapolation of the model form uncertainty to the prediction condition.

On-line Measurement of Inward - Outward Impedances for Stability Assessment

The tremendous increase in the employment of power electronics in the production, transfer, and consumption of energy not only enables a sustainable future, it undoubtedly brings major energy savings and stimulating improvements to people's quality of life. However, these gains are not for "free". This trend is considerably changing the nature of the sources and the loads in the electrical grid, altering their mild properties, and inflicting low-frequency dynamic interactions that did not exist in the conventional power system before. To be able to understand, analyze, design, and dynamically control the existing and future power systems, it is unarguably required to develop concepts and tools that offer better insights into the system-level behavior and stability of the grid.

This paper presents an alternative on-line stability monitoring method, where by perturbing the converter's duty-cycle, source output impedance and load input admittance can be simultaneously measured (Eq. 1). Using these measurements, and combining them with the un-terminated transfer functions of the dc-dc converter, equivalent system output impedance (and admittance) can be calculated out (Eq. 2), offering a great insight into system stability (observed at both, input and output side of the converter) – Fig. 1. Additionally, using all terminal impedances, Nyquist plots for both sides can also be plotted offering better insight into system stability margins.

Eq. 1.

$$\frac{\hat{v}_i / \hat{d}}{\hat{i}_i / \hat{d}} = Z_o \quad \text{and} \quad \frac{\hat{i}_o / \hat{d}}{\hat{v}_o / \hat{d}} = Y_i$$

Eq. 2.

$$Z_o^{EQ(CALC)} = Z + \frac{GHZ_o}{1 + Z_o Y} \quad \text{and} \quad Y_i^{EQ(CALC)} = Y + \frac{GHY_i}{1 + ZY_i}$$

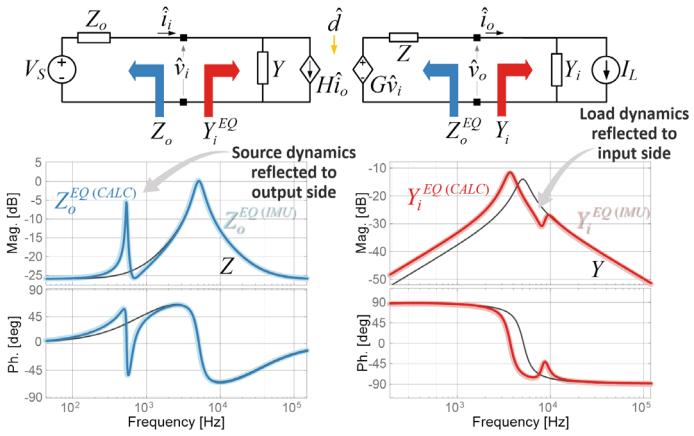


Fig. 1. Calculated Inward - Outward impedances (Eq.2) compared with those obtained using linearization (conventional approach – superscript IMU).

Application of Impedance-Based Stability Criterion in Power Systems with Multiple STATCOMs in Proximity

Ever since it was derived from Nyquist stability criterion and first developed in dc-dc power electronics converter systems, impedance-based stability criterion has been proven to be a powerful tool for small-signal stability analysis and design. It requires less knowledge than state-space modeling and is design-oriented. Recently it has been extended to ac systems to address the issues and challenges that come with more and more power electronics based converters that connect to existing ac power grids, either in at a transmission or distribution level. With that, only terminal information is necessary to judge small-signal stability and thus online detection and tuning is feasible. A case study with multiple STATCOMs in an IEEE 14-bus system is shown as an example. It is the first time that the impedance-based method has been used to demonstrate the interactions between STATCOMs at the transmission system level.

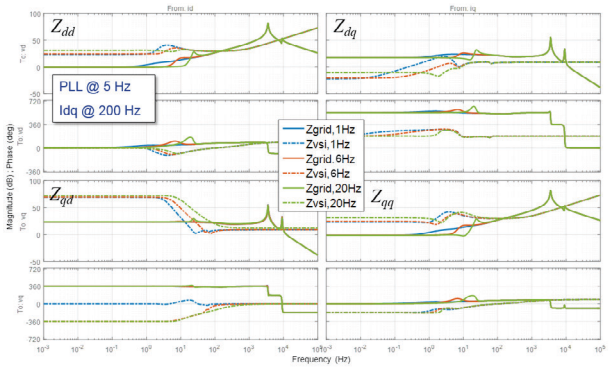


Fig. 2. Impedance measurements at PCC of STATCOM 1 with different bandwidths of ac voltage loop.

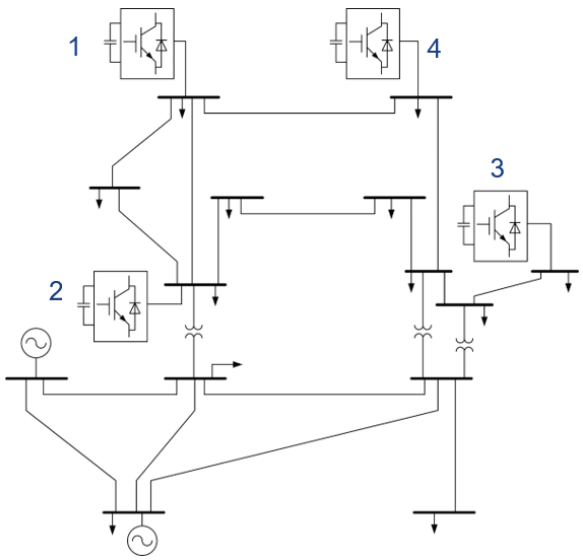


Fig. 1. IEEE 14-bus system with four STATCOMs.

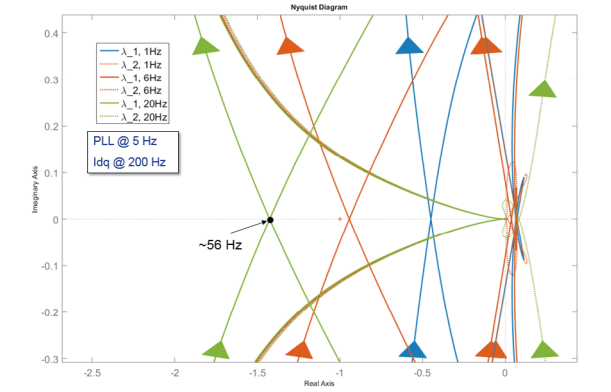


Fig. 3. Characteristic loci of the return ration L(s) with different bandwidths of ac voltage loop.

Critical-Mode-Based Soft-Switching Modulation for Three-Phase Inverters

In order to achieve high efficiency during high-frequency operation at several hundreds of kHz for three-phase inverters with a SiC MOSFET, we propose a new critical-conduction-mode (CRM)-based type of modulation. Soft switching is achieved with this modulation, and the switching frequency variation range is much narrower than prior-arts modulations. Therefore, switching-related loss is significantly reduced and high efficiency is achieved.

Soft switching is the key factor to achieving high efficiency during high-frequency operation, and CRM operation is the simplest way to achieve soft switching. In prior-art modulations, split capacitors are used on the dc side, and the middle point is connected to the ac side neutral point to electrically decouple three phases. Therefore, each phase is able to run in CRM independently. However, an extremely wide switching frequency variation range is observed when applying prior-arts modulations to high-frequency design. With a minimum switching frequency of 300 kHz, the peak switching frequency reaches 6 MHz or above, resulting in large switching-related loss.

Thus, instead a dc-side middle point and ac-side neutral point are left unconnected to avoid wide switching frequency variation. By combining discontinuous pulse width modulation (DPWM) with CRM, and synchronizing switching frequency through discontinuous conduction mode (DCM) operation, the switching frequency variation range becomes much narrower. With a minimum switching frequency of 300 kHz, the peak switching frequency is around 500 kHz, which reduces switching-related loss significantly.

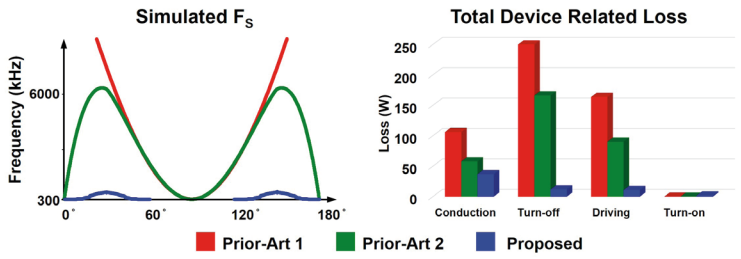


Fig. 1. Comparison of switching frequency distribution and device loss breakdown.

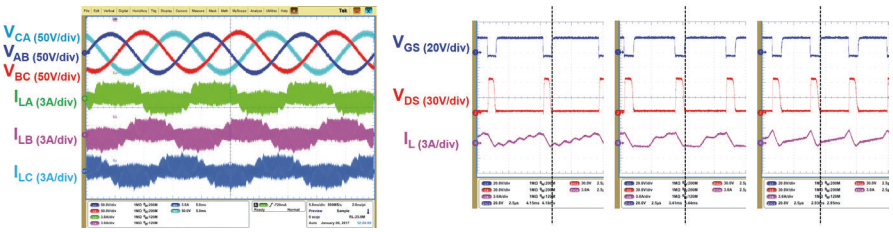


Fig. 2. Experiment waveforms over line cycle and switching cycles.

Fig. 1 shows the advantages shown by a simulation of the proposed modulation over two prior-arts modulations, in terms of switching frequency variation and device loss breakdown.

Fig. 2 shows the experiment waveforms over the course of a line cycle and at three arbitrarily selected instants during CRM operation. It can be clearly seen that ZVS soft-switching is achieved.

Sponsored Research Nuggets

2 W Gate Drive Power Supply Design with PCB-Embedded Transformer Substrate

Active dv/dt Control of 600 V GaN Transistors

Over-Molded Inductor (OMI) – Feasibility Demonstration in a DC-DC Converter

Physics-Based Equivalent Circuit for Coupled Windings with Significant Fringing

Improved Coupled Inductor Design for 6.6kW On-Board Battery Charger

New Tunable Piezoelectric Transformers and Their Application in DC-DC Converters

Modeling of Voltage-Controlled Capacitor (VCC) in DC-DC Converters

Testing the Switching Capability of a Normally-off 800 V - 2 A Vertical GaN Power Transistor

Wide-Input-Voltage-Range Dual-Output GaN-based Isolated DC-DC Converter for Aerospace Applications

Evaluation of the Reverse Behaviors of the Latest Generations of SiC MOSFET and SiC Schottky Barrier Diode

Passive Balancing of Peak Currents between Paralleled MOSFETs with Unequal Threshold Voltages

Phase Leg Design and Dynamic Characterization with two 650 V/ 60 A GaN HEMTs in parallel

Busbar Design for SiC-Based H-Bridge PEBB using 1.7 kV, 400 A SiC MOSFETs Operating at 100 kHz

10 KW Transformer and DC Stage Design for Electrical Vehicle Charging System

Two Comparison-Alternative High Temperature PCB-Embedded Transformer Designs for a 2 W Gate Driver Power Supply

High-Efficiency High-Power-Density 48/1 V Sigma Converter Voltage Regulator Module

Towards a High Performance Motor Drive System for Aerospace Applications: Topology Evaluation, Converter Optimization and Hardware Verification

2 W Gate Drive Power Supply Design with PCB-Embedded Transformer Substrate

As Silicon Carbide (SiC) and Gallium Nitride (GaN) devices become more commercially available, high switching frequency operations become a popular way to increase the power converter efficiency and power density. A key trade-off of these gains is the increasing electromagnetic inference (EMI) noise. In order to attenuate the EMI noise from the power loop into the auxiliary sources, the isolation capacitance in the isolated gate drive power supply is expected to be as small as possible. To this end, a gate drive power supply dedicated to driving two 650 V GaN devices in a phase leg is presented with a PCB-embedded transformer as substrate, thus achieving an ultra-low inter-capacitance of 1.6 pF, a high efficiency of 83% and a high power density of 72 W/in^3. The input of the power supply is 15 V and there are two isolated outputs, whose output voltage is 7 V and output power is 1 W each.

To pursue a small inter-capacitance (isolation capacitance) from the primary to the secondary side in the transformer, the primary and secondary windings should be located as far apart as possible. Accordingly, as the transformer volume increases, it exacerbates the difficulty in achieving high power density. The challenge of this work is to find an appropriate design approach, aimed at small converter volume, small inter-capacitance and high efficiency.

To design the targeted gate driver power supply, the paper first presents the circuit design, including the topology selection, operation mode analysis, and active and passive component selections. The PCB-embedded transformer structure is then illustrated in Fig. 1, and the core and PCB material selections are addressed. To find a compromise among a low inter-capacitance, low transformer loss, and a small volume, an optimization of the transformer dimensions is performed based on the transformer models. With the optimized dimensions, the transformer is built and shown in Fig. 2, and the fabrication procedures, including the standard lamination process, are introduced. The transformer and the converter hardware are shown in the end and characterized with experimental waveforms, efficiency, isolation voltage, inter-capacitance, and total volume.

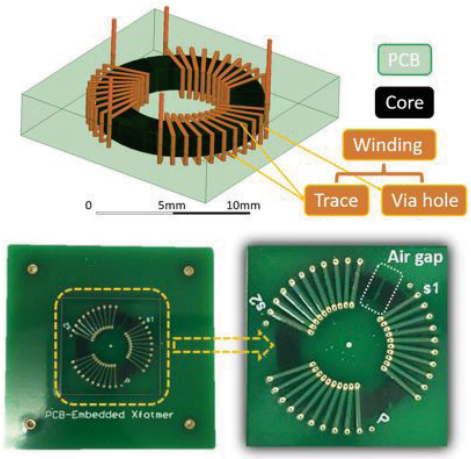


Fig. 1. PCB-embedded transformer structure illustration.

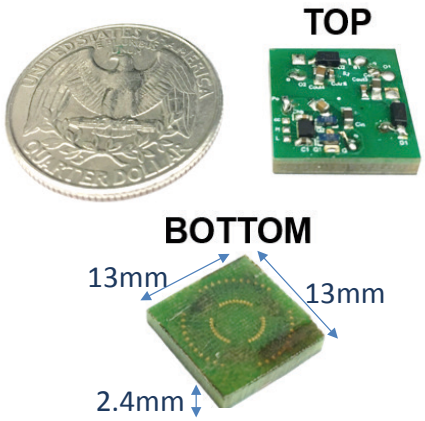


Fig. 2. Active-clamp flyback with the PCB-embedded transformer substrate.

Active dv/dt Control of 600 V GaN Transistors

The application of fast-switching devices like the GaN HEMT in power converters allows converters to achieve a higher switching frequency, a higher efficiency and a higher power density. As a result of the fast switching edge and high commutation speed, issues like electromagnetic interference (EMI), overvoltage, and gate protection become daunting tasks. The active gate control technique on the Si device has been verified to be an effective tool to relieve the challenges above, especially to reduce EMI noise by slowing down dv/dt with less penalty of switching loss.

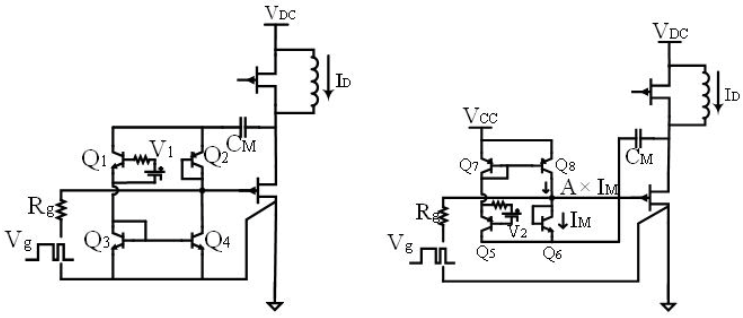


Fig. 1. Proposed turn-off (left) and turn-on (right) dv/dt control circuit.

The paper proposes a new active dv/dt control circuit with a fast response to change the 600 V GaN HEMT turn-off and turn-on dv/dt slew rate freely and independently while the converter is running. The proposed circuits are shown in Fig. 1. Simulations are first performed to verify the circuit function while considering all the possible parasitics distributed on the experimental setup, and a detailed circuit design is followed. The hardware is illustrated in Fig. 2. Experimental results, shown in Fig. 2, obtained on the 300 V dc 15 A load current double pulse tester, composed by a GaN HEMT phase leg, validates the proposed method by varying turn-on dv/dt slew rate from 27.1 V/ns to 8.8 V/ns and turn-off dv/dt from 34.6 V/ns to 7.6 V/ns. Finally, a comparison with different gate resistors is provided, showing the proposed method has a smaller switching loss under the same dv/dt condition rather than using a large gate resistor.

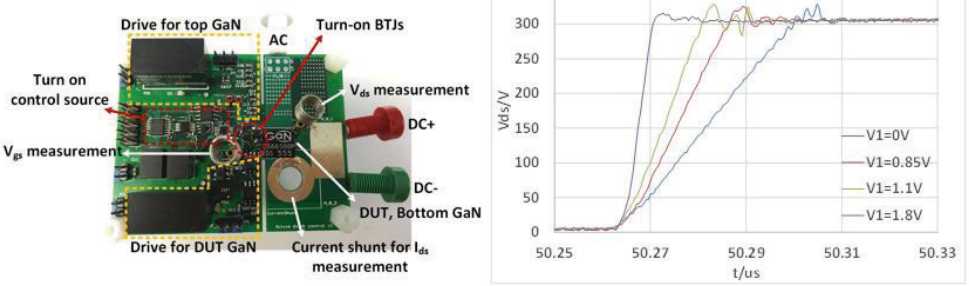


Fig. 2. Left: hardware for Double pulse test with active dv/dt control circuit;
Right: DPT turn-off Vds waveforms at 300 V dc 15 A load current with active gate driver.

Over-Molded Inductor (OMI) – Feasibility Demonstration in a DC-DC Converter

Switched-mode dc-dc converters serve a variety of products, such as point-of-load power modules, gate drivers, and mobile devices. An inductor is usually needed to attenuate the switching noise for the load. The inductor can be implemented as a discrete component, a substrate, or a package enclosure. A discrete inductor is shown soldered to a printed circuit board (or substrate) carrying the remainder of the converter in Fig. 1(a). Non-magnetic encapsulant may be added to protect the assembly against environmental stresses. Any additional shielding or isolation for protecting the magnetic device from encapsulant may increase the volume.

This paper presents an alternative to inductor fabrication called "over-molding." As depicted in Fig. 1(b), the winding is first attached to the substrate. Magnetic paste is then injected into the unused space that is normally occupied by encapsulant and is cured under atmospheric pressure below 250° C to realize the core. The prototype of the OMI is shown in Fig. 2(a).

The impact of the OMI on the converter's efficiency (Fig. 2(b)), operating temperature, and switching noise was demonstrated to be similar to that of the commercial inductor. Also demonstrated was the feasibility of storing magnetic energy in the volume normally filled by encapsulant. The next goal would be to improve the power density, which is tied directly to permeability. The materials and fabrication process will be examined to improve the homogeneity of over-molded magnetic mixtures using a low curing temperature under atmospheric pressure.

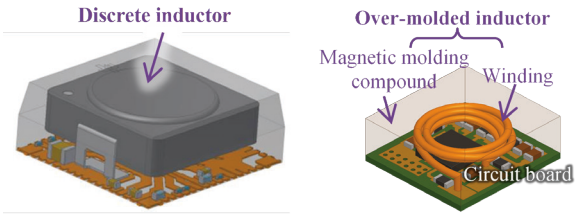


Fig. 1. Realizations of the inductor in a dc-dc converter: (a) Discrete inductor; (b) Over-molded inductor.

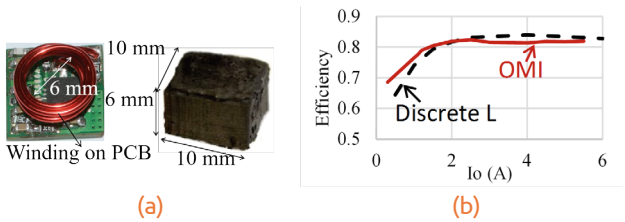


Fig. 2. (a) Winding on PCB and prototype of converter with OMI. (b) Comparison of efficiencies for dc-dc converter with discrete inductor and OMI.

Physics-Based Equivalent Circuit for Coupled Windings with Significant Fringing

An equivalent circuit for coupled windings is developed for inductors with significant fringing effect. The equivalent circuit is derived from a physical model that captures the flux paths through a leakage inductor and two mutual inductors on the primary and secondary sides. Each side has a winding resistor in parallel with one mutual inductor to model winding loss with open circuit and phase-shift impact. Two time-varying resistors are employed to represent the core loss dynamically. The equivalent circuit is verified by both finite-element simulation (FES) and prototypes fabricated with a flexible circuit.

The equivalent circuit is shown in Fig. 1 with two winding resistors and two core loss resistors on each side. R_{wp} and R_{ws} model the winding loss from coupling even if no net current is going through the winding. The core loss resistors are determined by core-loss calculation sub-circuit that dynamically predicts the core loss in the time domain.

Compared to the conventional equivalent circuit for coupled windings, the model herein is capable of predicting the winding loss when the phase shift between the primary and secondary currents is swept from 0 to 360 degrees.

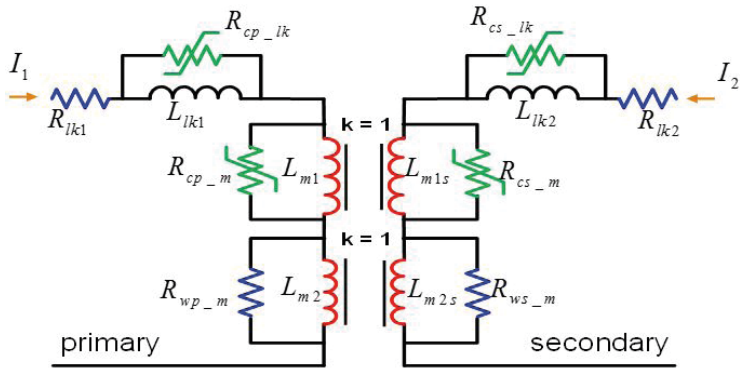


Fig. 1. Physics-based equivalent circuit for coupled windings.

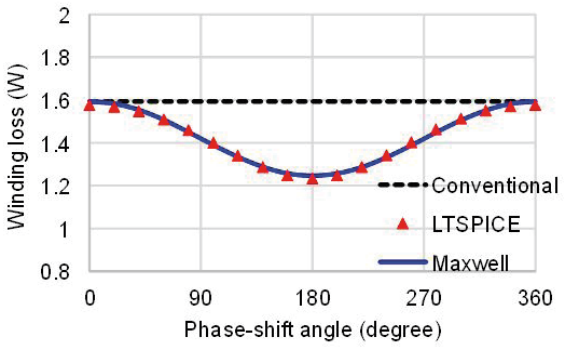


Fig. 2. Comparison of winding loss versus phase shift.

Improved Coupled Inductor Design for 6.6 kW On-Board Battery Charger

The coupled inductor has been widely adopted in VR applications for many years because of its benefits such as the ability to reduce current ripple or improve transient performance. In this paper, the positive coupled inductor concept is applied to an interleaved totem-pole CRM PFC converter for a 6.6 kW on-board battery charger. The difference between negative coupling and positive coupling will be discussed. The benefit of positive coupling for a battery charger will be presented, reducing switching frequency range and input DM noise. Hence the positive coupled inductor can improve the performance of the PFC converter. In addition, a balance technique is applied to help minimize CM noise. Furthermore, the inductor is integrated into the PCB winding. With the inductor integration, the converter can avoid labor intensive production and achieve a fully automatic manufacture. However, the PCB winding inductor has a larger parasitic capacitance and this parasitic capacitance will introduce spikes, ringing, and extra loss. In this paper, an improved PCB winding inductor design is provided to minimize parasitic capacitors and reduce loss.

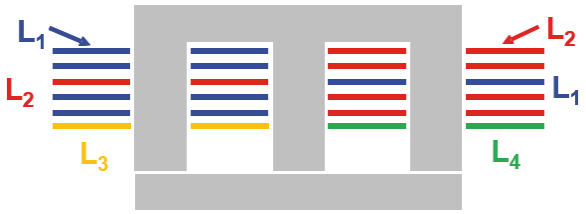


Fig. 1. Coupled inductor in PCB winding.

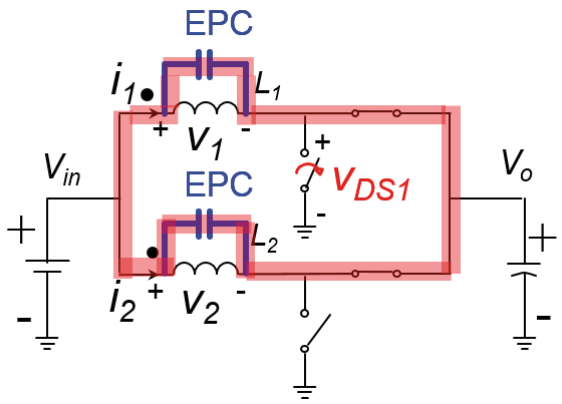


Fig. 2. EPC impact on circuit.

New Tunable Piezoelectric Transformers and Their Application in DC-DC Converters

Recently, radial Piezoelectric Transformer (PT) structures, such as the so-called Transoner® PT, have been developed and are used for ac-dc and dc-dc converter applications. Just like resonant converters, most of the converters using PTs regulate the output voltage by changing the switching frequency of the inverter bridge (variable frequency modulation control). This requires isolation in the feedback circuit between the primary and secondary, which adds to the weight and complexity of the converter. This paper discusses the basic operation of a new Tunable Piezoelectric Transformer (TPT) unit. It proposes a TPT-based dc-dc converter rated at 30 W, 120:55 V dc, and a fixed frequency control scheme to regulate the output voltage under load and input voltage variations.

The proposed Tunable PT uses the same structure as the radial PT, however, an additional piezoelectric section (control layer) is sandwiched between the existing primary and secondary layers, as shown in Fig. 1. A change in the control capacitance modifies the primary series capacitance of the control layer, thus changing the resonant frequency of the piezoelectric transformer structure. To implement this, a control scheme has been proposed, as shown in Fig. 2. with an external cap whose value can be regulated from 2 nF – 100 nF using duty cycle control.

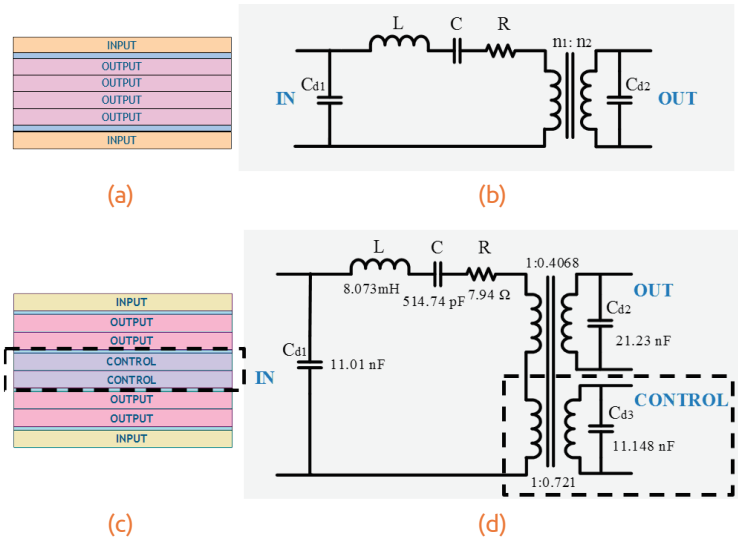


Fig. 1. (a) Structure of layers in a standard Transoner® radial PT and (b) its electrical equivalent circuit. (c) and (d) show the structure of a Tunable PT with control section sandwiched in between the input and output layers.

The proposed design is implemented on hardware using a 30 W TPT developed by Micromechatronics, Inc., PA and is shown in Fig. 3. With the nominal voltage of 220 V dc, an operating frequency of 82.5 kHz and a nominal load of 105 Ω, the output voltage is regulated at 55 V using the constant frequency control.

This paper introduces the concept behind new tunable piezoelectric transformers and demonstrates their implementation in the design of dc-dc converters. The proposed control scheme provides a way to regulate the output voltage using a fixed frequency control and without isolation in the control circuit.

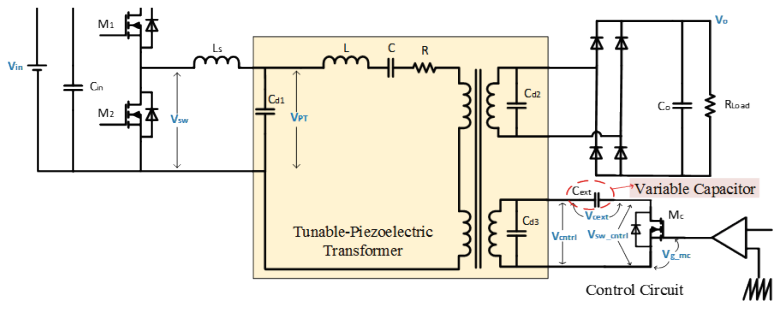


Fig. 2. Electrical schematic for dc-dc converter design using tunable PT.

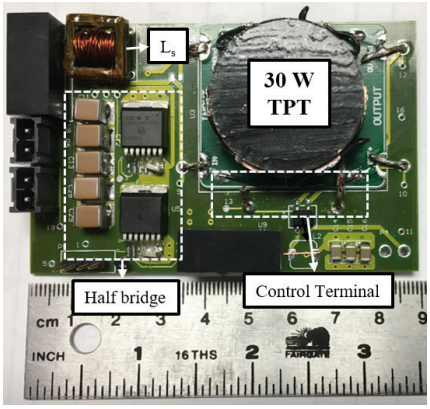


Fig. 3. A dc-dc converter board developed using a 30 W Tunable PT.

Modeling of Voltage-Controlled Capacitor (VCC) in DC-DC Converters

Capacitors transfer power, store energy, and filter harmonics in power electronics applications. Steady-state performance (e.g., efficiency and voltage ripple) and dynamic performance (e.g., overshoot and settling time) of dc-dc converters are determined by capacitor properties such as capacitance, ESR, voltage coefficient, and temperature coefficient. Capacitance usually drifts with the bias voltage because the permittivity of dielectric materials in a capacitor depends on the value of the applied electric field. Either a capacitor with stable permittivity (e.g., NP0) should be used, or the voltage across that capacitor should be well controlled to compensate for such undesired capacitance change, which both limits component selection and increases design complexity.

This paper presents a four-terminal VCC that varies from 20% to 100% of the rated capacitance (1 μF) with a control voltage from half of the voltage rating to 0 V. The prototype is shown in Fig. 1.

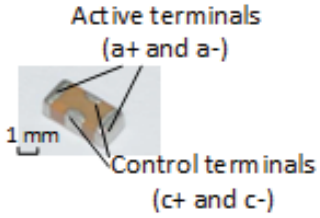


Fig. 1. Prototype of the VCC.

Models of nonlinear capacitors vary from the application. The C-V model is commonly used in dc-dc converters where the ac component is quite small compared with the dc component in capacitor voltages. In the C-V model, a capacitor current is generated only by a voltage change, such as a fixed capacitor even though a capacitance change is not considered another current source. Only the C-V curve, which can be measured by an impedance analyzer, is required in this method.

The VCC was employed as an output filter of a buck converter with input of 12 V, output of 5 V, and switching frequency of 500 kHz to demonstrate its impact of controllability on the voltage ripple. The experiment hardware is shown in Fig. 2. Simulation based on the C-V model showed an 8% error with an experimental waveform, which verified the effectiveness of the model in dc-dc converters. The comparison of simulation and experiment results are shown in Fig. 3. Future work will be focused on the design of the driver and closed-loop control of the VCC in other applications and circuit topologies.

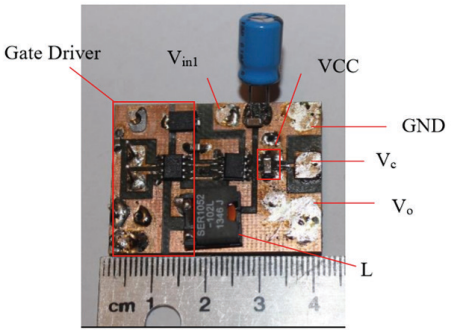
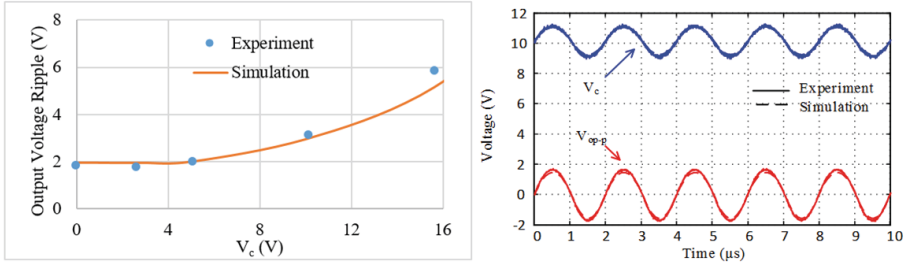


Fig. 2. Experiment hardware of buck converter with VCC in Fig. 1 as output capacitor.



(a) (b)

Fig. 3. Comparison of simulation and experiment results in Fig. 2 with (a) output voltage ripple with V_c changing from 0 V to 12 V and (b) time-domain waveform with V_c = 10 V.

Testing the Switching Capability of a Normally-off 800 V - 2 A Vertical GaN Power Transistor

The development of a normally-off vertical GaN transistor could bypass Si and SiC in both conduction and switching performance. Therefore, the goal of the development of the device presented in this paper was to create a normally-off vertical GaN transistor competitive with Si and SiC devices not only in performance but also in price. To evaluate the functionality of the 800 V - 2 A vertical GaN transistors, the bare die will be subjected to static characteristic tests. The device is also switched by using a clamped inductive load test with a double pulse input.

The bare die of the device is subjected to these tests after being mounted onto a PCB and then wire bonded to it and encapsulated. The final encapsulated stage of the transistor can be seen in Fig. 1.

To initially characterize the device, a basic static characterization is performed using Agilent's B1505A Curve Tracer. These tests consist of transfer characteristics, output characteristics and on-state resistance over current. For the double pulse test used to assess the switching of the device, the gate to source voltage is driven from 0 V to 10 V and a 10 Ω external gate resistor is used. The switching waveforms of the device at a drain to source voltage of 400 V and a load current of 2 A are shown in Fig. 2 and Fig. 3. These waveforms are used to calculate the switching losses and switching on times.

These results show the potential that a vertical GaN device has in the push to find a replacement for silicon that has better performance with a lower price. Further testing objectives are to decrease the external gate resistor used for the switching test and to test the device at higher voltages.

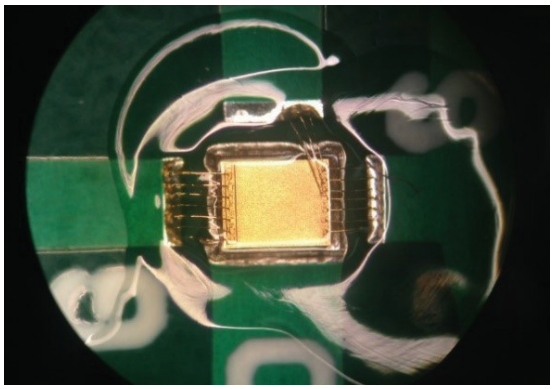


Fig. 1. Vertical GaN device after being encapsulated on PCB.

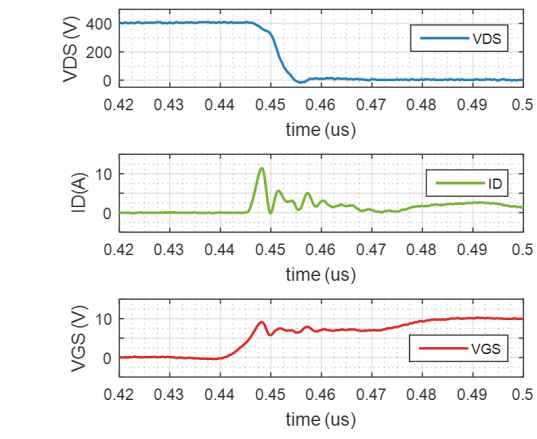


Fig. 2. Turn-on waveforms with a load current of 2 A at a VDS of 400 V.

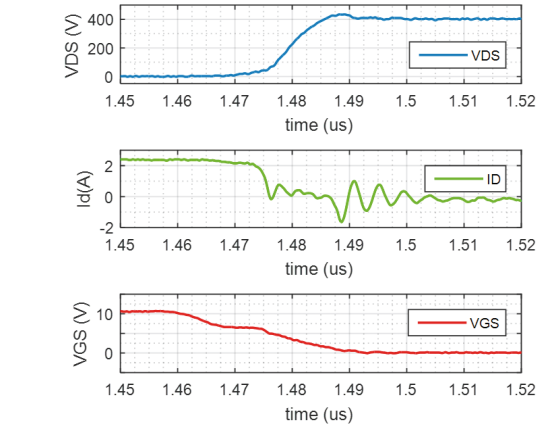


Fig. 3. Turn-off waveforms with a load current of 2 A at a VDS of 400 V.

Wide-Input-Voltage-Range Dual-Output GaN-based Isolated DC-DC Converter for Aerospace Applications

In aerospace applications, a power converter may have to deal with harsh working conditions. These can include a wide input or output voltage range and a wide range of operation temperatures. This dc-dc converter is designed to accommodate a wide input voltage range and provide two fixed output voltages. The new topology is designed with EPC GaN devices to divide the input voltages using an additional switch. The total volume is controlled and the efficiency is taken into account, and the converter shows peaks efficiency higher than 92% when working at full power. The converter works just like a traditional active-clamp flyback circuit. The additional high-side switch needs additional design for its driving loop, but the operation mode does not change much. A few steps have been taken to design a planar transformer which fits the volume requirement and maintains good performance. Thanks to the new material ML91S from Hitachi, the transformer loss can be reduced, and a high-frequency converter with high efficiency and small volume can be realized.

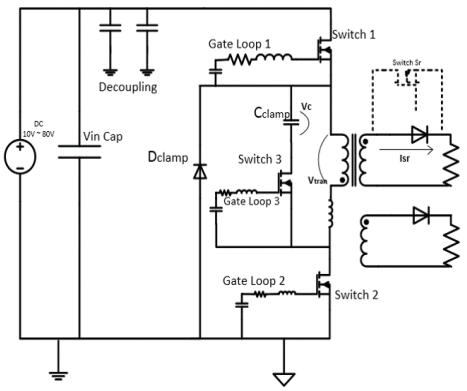


Fig. 1. Converter Topology.

With the current topology and operation level, the main challenge is efficiency over a wide range of input voltage. Even though the lowest and highest input occur at start-up and transient response, maintaining efficiency for input voltages from 18 V to 70 V still requires a significant tradeoff in design. In addition, the potential ability for control should be checked in order to limit the duty cycle to a reasonable range. In terms of efficiency, switches (or diodes) and transformers are the two main components responsible for most of the power loss. By selecting proper devices and designing a customized transformer, the whole range loss is controlled, but there is still some sacrifice at specific operation points.

In terms of manufacturing, the layout is critical, and gate driving loops for such devices on the primary side are more sensitive to noise than other converters. The final version of the converter has optimized the gate driving loop inductance and the layout is optimized for a smaller size and better power loop design.

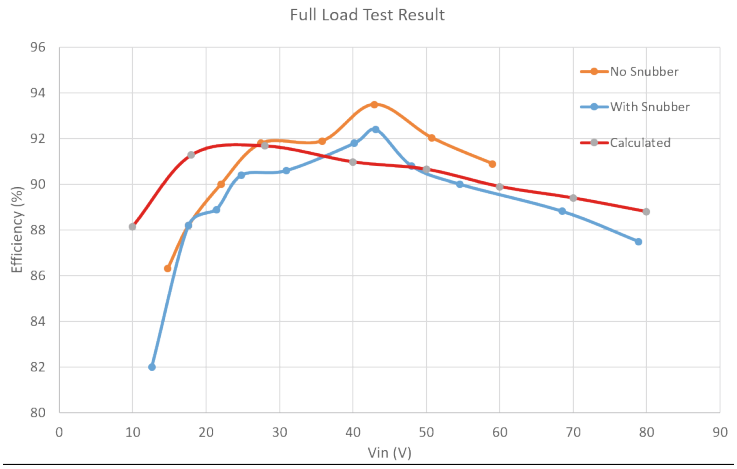
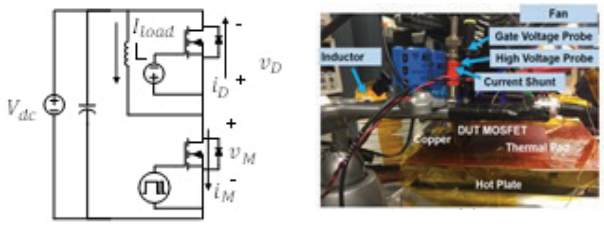


Fig. 2. Converter efficiency.

Evaluation of the Reverse Behaviors of the Latest Generations of SiC MOSFET and SiC Schottky Barrier Diode

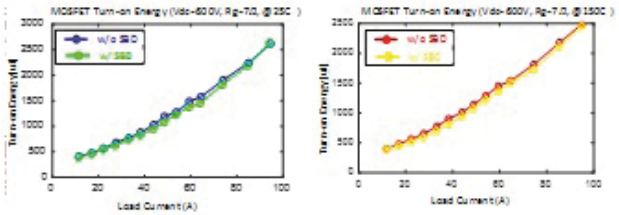
The performance of the SiC power MOSFET exceeds the Si IGBT with similar voltage ratings and bidirectional conducting capability. Unlike the Schottky Barrier Diode (SBD), the body diode of the MOSFET has a reverse recovery problem due to its P-i-N nature. The MOSFET's body diode reverse recovery issues have been widely studied since the Si MOSFET era. Though the reverse recovery of the SiC MOSFET is better than the Si MOSFET, with 10 times lower reverse-recovery current, SiC MOSFET products packaged with SBDs are still being widely developed because a design has not yet been developed that satisfies the reverse recovery problem and high conduction loss of the body diode. CREE's second-generation SiC MOSFET's reverse behaviors have been widely studied, and the necessity of paralleling the SBD to achieve small turn-on switching energy is proven.

In this paper, the record high current-rating of CREE's third-generation discrete SiC MOSFET is evaluated. CREE's 1.2 kV SiC SBDs are compared according to its current sharing capabilities in parallel with SiC MOSFETs through conducting and switching characteristics, with load currents ranging from 10 A to 95 A under both room temperature and high temperatures. Fig. 1 shows the double-pulse test setup for the reverse behavior. The diode in Fig. 1(a) represents a body diode when testing without a SBD in parallel, while that in Fig. 1(b) represents the body diode and the SBD when testing with a SBD in parallel. The high-temperature setup of the reverse behavior characterization is shown in Fig. 1(b), where a bent piece of copper is used to transfer heat to the devices being tested from the hot plate. Fans are used to cool down the top-side circuits. Fig. 2. shows the comparison between using the freewheeling diode as a body diode and using the freewheeling diode as a body diode in parallel with the SBD under both room temperature and high temperature. As the reverse-recovery behavior of the third-generation SiC MOSFET's body diode is trivial compared to its reverse behavior caused by the output capacitance, the extra reverse energy introduced by the junction capacitance of the SBD actually compensates the elimination of the reverse recovery energy by the SBD. Also, the reverse-recovery behavior of the third-generation SiC MOSFET shows very little increase under high temperatures, and paralleling the SBD does not show much improvement under high temperatures, either. In conclusion, for the third-generation SiC MOSFET, the SBD is not necessary to improve reverse-recovery behavior.



(a) (b)

Fig. 1. (a) Double Pulse Test Scheme for Reverse Behavior Characterization; (b) Hardware Setup for High Temperature Reverse Behavior Characterization.



(a) (b)

Fig. 2. Comparison of Active MOSFET Turn-on Energies without SBD in Parallel and with SBD in Parallel under Test Condition V_{dc}=600 V, R_g=7Ω: (a) Room Temperature; (b) High Temperature.

Passive Balancing of Peak Currents between Paralleled MOSFETs with Unequal Threshold Voltages

The peak switching currents of two paralleled MOSFETs turned on and off by one gate driver could differ significantly because of the mismatch in threshold voltages (V_{th}). The passive balancing method described herein employs one inductor and one resistor per MOSFET to force the currents to track with negligible penalty in loss. Sensors, feedback, and knowledge of gate-related parameters (like gate charge, polarity of V_{th} difference, gate impedances, etc.) are not required. The passive components are designed using an inequality involving V_{th}, rise time, and unbalance percentage. The mismatch in peak currents is reduced from 15% to 1% between the SiC MOSFETs tested at 20 A and 300 V, with 19% V_{th} variation.

The influence of power-source inductance (L_s) and drive-loop resistance connected to the source (R_k) on dynamic sharing with mismatched threshold voltage and balanced layout is shown in Fig. 1. The scheme with two switches for every branch represents different structures (with symmetry maintained); the influences of L_s and R_k on dynamic sharing can be tested. The parasitics of the package are not included in the analysis for simplicity. However, the theory holds up well when parasitics are considered, as shown in the experimental verification (Fig. 2), which includes parasitics from the device package and copper traces. The DPT (double-pulse tester) is used for the testing of switching transients.

Fig. 2 shows the experimental results with designed L_s and R_k. The desired current sharing is obtained within one switching cycle by utilizing a single gate driver. Better sharing is also achieved for the turn-off transient as compared to the baseline, shown in Fig 2(a).

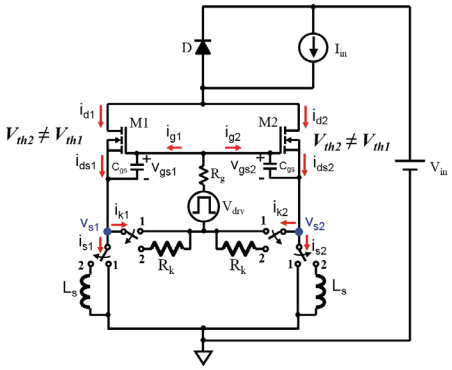


Fig. 1. Influence of power-source inductance (L_s) and drive-loop resistance connected to the source (R_k) on dynamic sharing, where the lower side is paralleled SiC MOSFETs with mismatched V_{th} and upper side is a SiC Schottky barrier diode.

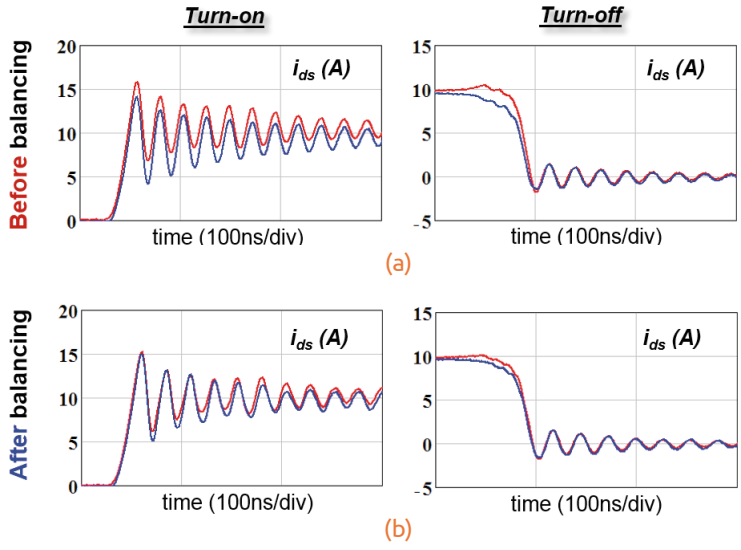


Fig. 2. Experimental results tested at V_{in} = 300 V, I_{in} = 20 A, $R_g + 0.5R_k$ = 20 Ω, V_{th1} = 2.34 V, V_{th2} = 2.78 V for verification of current balancing solution in Fig. 1. Drain-source currents for turn-on and turn-off transients (a) Without L_s and R_k design, and (b) With L_s and R_k design.

Phase Leg Design and Dynamic Characterization with two 650 V/ 60 A GaN HEMTs in parallel

Wide band-gap GaN-based devices are emerging as an attractive candidate for high-efficiency power driving systems because of their high breakdown voltage, low on-resistance, fast switching, and high temperature operation. The theoretical limit of a GaN breakdown voltage is very high with very low specific on-resistance. The 600 V cascode GaN-on-Si structure has been dominant in medium power applications for a long time but the cascode structure has issues of charge imbalance between the low voltage Si and high voltage normally-on GaN, lower reliability and high common source inductance.

However, the rated current for commercially available GaN devices is limited to 60 A. The on-resistance also increases a lot with current and temperature thus resulting in very low efficiency for high current applications. Hence, paralleling multiple GaN devices is required for high efficiency high power applications.

The schematic and layout design for two GaN devices in parallel for both phase leg and DPTer are shown in Fig. 1. The 650 V/ 60 A GaN device discussed in this paper has a very small package inductance but to fully extract the benefits of this small package, it is important to design the gate-source loop and power loop layouts to have minimum parasitic inductances. Also when paralleling multiple GaN devices, it is important to design identical gate loop and power loop for both the devices. Furthermore, the layout should be designed so that there's minimal parasitic inductance in between the two devices.

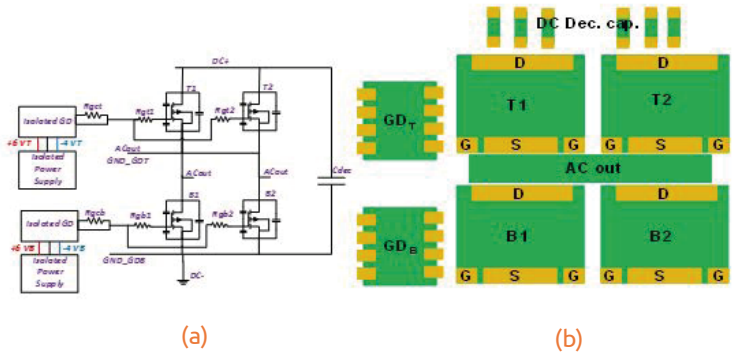


Fig. 1. (a) Phase leg schematic and (b) Phase leg block diagram.

The recommended design from GaN Systems is shown in Fig. 1, which is based on the schematic. However, the layout design guidelines presented in this paper are not discussed in any previous work in detail. A detailed dynamic characterization of the above mentioned design and the problem of circulating current during turn-on transient is observed. The issue of circulating current has not been discussed in any previous work. The limit of this DPTer design is tested and findings show that due to the parasitics added by the current shunts, the design's current limit is much lower than the case when the shunts are shorted. The methods to control the circulating current are also discussed.

Busbar Design for SiC-Based H-Bridge PEBB using 1.7 kV, 400 A SiC MOSFETs Operating at 100 kHz

The concept of a power electronics building block (PEBB) is the integration of fundamental components, such as power devices, gate drives, and control schemes. This allow for numerous power conversion topologies to be implemented by a series/parallel connection of these building blocks to achieve practically any desired current/voltage/power level, and is therefore able to be used in a variety of applications. Although SiC-based PEBBs are capable of operating at high switching frequencies and high power levels, the high-speed switching transients within the PEBB are strongly affected by the resistance and inductance of the connections between components. The large stray inductance in the PEBB may cause excessive transient voltage overshoots across the MOSFETs. The voltage overshoots can result in increasing power loss, high voltage stress, and exceed the MOSFET safe operating range. Stray inductance is hence an important concern in the design of high-power and high-frequency power converters. The busbar technology is an effective way to reduce interconnection inductance. It consists of stacking several copper sheets, each separated from the other by a dielectric material. The role of the dc link busbar of the PEBB is to achieve a series or parallel configuration of the capacitors and to link the dc capacitor bank and power modules. In addition to its low impedance (both inductance and resistance), using a busbar improves the thermal performance, since the surfaces of exchange are increased, and heat transfer is facilitated. Furthermore, adding thick external layers to the busbar improves the mechanical strength of the busbar without affecting its impedance. Lastly, busbar connections contribute to a compact size, which is a critical aspect of the PEBB design.

This paper presents a study of busbar optimization for a high-power and high-switiching-frequency SiC-based H-bridge PEBB. A new double-sided busbar with symmetric minimized commutation loops is presented, which eliminates the use of the decoupling capacitors and also results in improved thermal and switching performance of the PEBB. Step-by-step busbar design guidelines are provided with all the necessary equations and analysis to select the materials and calculate the dimensions of the different layers. Furthermore, the stray inductance of the current commutation loops is estimated by simulation and verified experimentally. The power stage model of the PEBB is also developed including busbar parasitics. Finally, the switching performance of the PEBB is presented to show the effects of the minimized loop inductance on the switching transients.

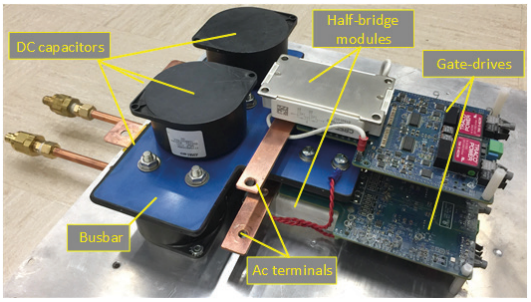


Fig. 1. Final assembled PEBB with double-sided busbar.

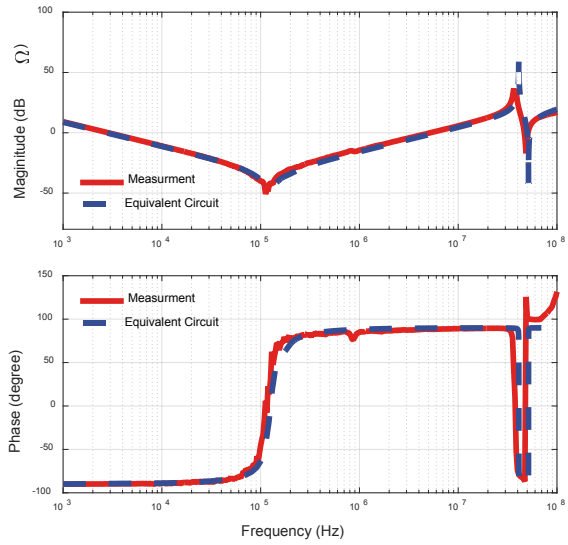


Fig. 2. Power stage impedance result from measurement and equivalent circuit of the PEBB.

10 KW Transformer and DC Stage Design for Electrical Vehicle Charging System

The vehicle charging system used in this design includes an ac/dc PFC stage and a dc/dc stage to accommodate the wide range of output voltage. The output voltage ranges from 200 V to 500 V and the thermal design is considered at full power level. Paralleling GaN devices is used at both stages to increase the power level and efficiency at the same time. This paper focuses on the design of the dc stage, including LLC converter operation, efficiency estimation and high-power, high-frequency transformer design. The dc input for the dc stage will be fixed at 400 V, so the operation frequency should be tuned to fit different output voltages. A full comparison and selection has been made to compare different operation frequency ranges based on peak current and RMS current. The transformer is designed after the operation frequency is determined. In the first prototype, the transformer loss can be controlled to be below 50 W for the entire range, and the peak efficiency of the LLC stage can reach 98.3% using diodes and 98.7% is using switches as the secondary side.

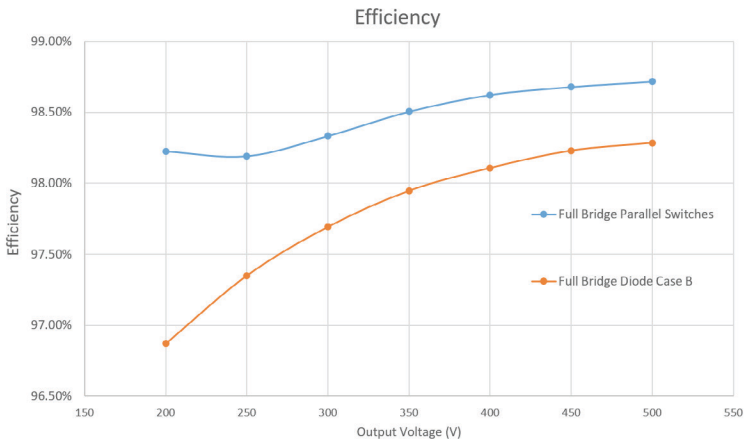


Fig. 1. Efficiency comparison.

When designing the converter operation mode, in order to regulate the output voltage, the operation frequency range should be below the resonant frequency so a high gain can be achieved without any additional loss. In this range there is no secondary side switching loss, and the primary switches' turn-off loss can be minimized as well. Peak current and RMS current are compared for different resonant frequencies, and the final operation range is selected to be 200 KHz to 400 KHz.

The transformer design is based on this frequency range. Because the switches (or diodes) can create a great deal of power loss, the transformer should have a better performance as it will determine the whole converter's power density. Ferrite 3C97 is selected as the material for this operation range, and the first prototype is designed by first limiting the loss. The volume is still large, and further efforts will be made to design a better high-power-density transformer.

The first LLC converter with open-loop control will be tested, and more work will be done on transformer design. Either a matrix transformer or a planar structure will be studied as well.

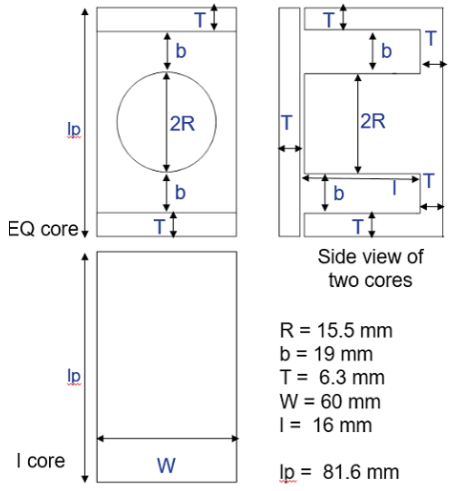


Fig. 2. Core design overview.

Two Comparison-Alternative High Temperature PCB-Embedded Transformer Designs for a 2 W Gate Driver Power Supply

Fast power semiconductor devices based on GaN and SiC are becoming more common increasing the need for improved driving circuits. Transformers with smaller inter-winding capacitance in the isolated gate drive power supply help to reduce the conducted EMI emission from the power converter to auxiliary sources. This paper presents a transformer with a small volume, a low power loss and a small inter-capacitance in a gate drive power supply for fast switching devices, such as GaN HEMT and SiC MOSFET. The transformer core is embedded into the PCB to increase the integration density.

Two different transformer designs, the coplanar-winding PCB embedded transformer and the toroidal PCB embedded transformer, are presented and compared, as shown in Fig. 1 and Fig. 2 respectively. Both designs are dedicated to a 2 W gate drive power supply for wide-band-gap device, which can operate at 200° C ambient temperature. The former uses a 'C I' core and PCB winding within the core, which enables a far distance between the primary and secondary windings. Thanks to this structure, the co-planar transformer achieves 0.8 pF inter-capacitance. With the switching device located on the transformer surface, the final converter with 1 MHz switching frequency has a 74% overall efficiency at 2 W output power and its volume is 23 mm x 18 mm x 2.8 mm. The secondary transformer is called the toroidal PCB-embedded transformer, where the core is toroidal and its windings are twisted around the core. With an optimization on the core size and winding size parameters, a targeted small inter-capacitance, a small transformer loss, and a small total volume, the transformer has a 1.6 pF inter-capacitance allowing the corresponding converter to achieve an 85% efficiency with a 1 MHz switching frequency and a total converter volume of 13 mm x 13 mm x 2.4 mm. The corresponding power density is 72.6 W/in^3.

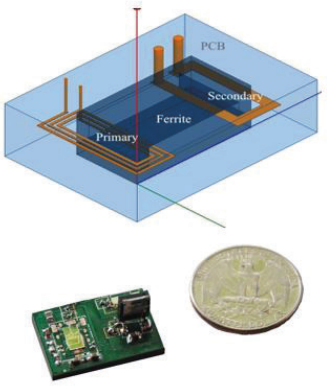


Fig. 1. Coplanar-windings transformer design and the prototype with top components of the coplanar windings transformer.

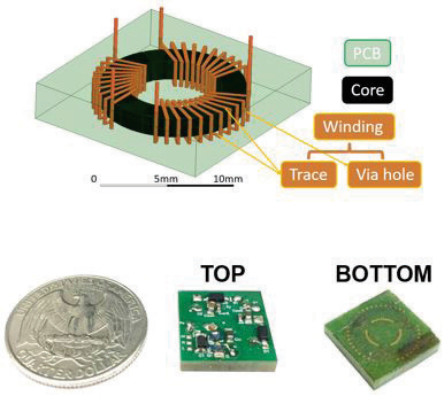


Fig. 2. Toroidal PCB-embedded transformer design and the converter design with device on the top of the transformer.

High-Efficiency High-Power-Density 48/1 V Sigma Converter Voltage Regulator Module

Efficient power delivery architecture is gaining more attention in the design of future generations of Data Centers and Telecom power supplies in order to minimize the ever increasing trend of power consumption. 48 V voltage regulator modules (VRMs) have been used in telecom applications for many years. A recent study indicated that 48 V VRMs, instead of 12 V VRMs, are deemed a more efficient and cost effective architecture for data center applications.

In this work, a one stage sigma converter is proposed for a high efficiency solution in such applications. The sigma converter consists of two series connected converters from the input side and parallel connected from the output side as shown in Fig. 1.

Comparing the two stage solutions, the power flow in the sigma converter is shared between two converters. A ratio is determined with the input voltage across each of them. For a higher efficiency solution, an unregulated LLC converter (DCX) was designed to have a 40 V input while the remaining 8 V is applied to the buck converter responsible for the output voltage regulation. This allows the majority of the power to slowly flow through a higher efficiency path. A small portion of the power flows through the less efficient buck converter resulting in a higher total efficiency.

A PCB winding Matrix transformer structure integrating four transformers in one core was adopted for the LLC-DCX. A one turn PCB winding inductor was used for the buck converter resulting in a very high density solution reaching 420 W/in^3 as shown in Fig. 2.

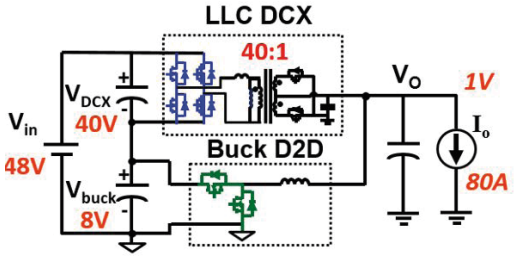


Fig. 1. One Stage 48/1 V Sigma Converter Power architecture.

The prototype was experimentally tested achieving a maximum efficiency of 93.4% with a heavy load efficiency of 91.6%. The converter efficiency was measured at different input voltages and achieved a higher efficiency than the state-of-the-art solution from VICOR as shown in Fig. 3.

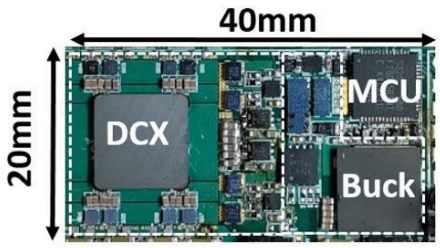


Fig. 2. Sigma Converter prototype.

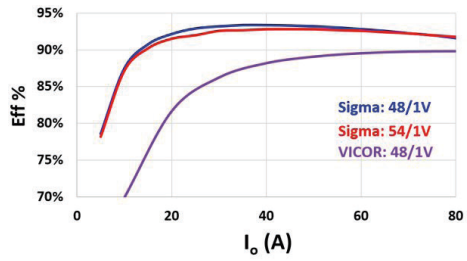


Fig. 3. Sigma Converter efficiency comparison with state-of-the-art product.

Towards a High Performance Motor Drive System for Aerospace Applications: Topology Evaluation, Converter Optimization and Hardware Verification

For recent aerospace applications, the trend towards higher fuel efficiency and lighter take-off weight calls for more efficient, more compact and lighter power electronics converters. The multi-objective optimization of power electronics converters is one of the key techniques to achieving better design. This paper develops a framework for designing a high-performance on-board motor drive system utilizing a multi-objective optimization concept. The design framework aims to maximize the tenable power rating within specific loss (30 W) and volume (8.3" x 7.3" x 1.0") constraints while addressing EMI on both the dc and ac sides, power quality, and thermal (free convection cooled) requirements. Specifically, the converter is designed for 540 V dc input, 200 Vrms ac three-phase output, and 50 - 2000 Hz output frequency under the requirements of the DO-160E standard.

Converter topology is one of the key design variables; hence the two-level voltage source converter, three-level neutral-point-clamped voltage source converter, T-type converter and three-phase triangular conduction mode converter are evaluated. Each topology has gone through converter optimization procedures under different power ratings in order to explore their loss-size trade-offs, demonstrated as Pareto fronts. This study shows that the T-type converter achieves the highest power rating of 5 kVA. Fig. 1 demonstrates the possible design points and loss-size Pareto front of a 5 kVA T-type converter. Similar studies were conducted for other topology candidates and power ratings.

Finally, a 5 kVA free convection cooled prototype is constructed (shown in Fig. 2), which achieves a power density of 80 W/inch^3. Under a nominal load, it achieved an efficiency of 99.3% (32.4 W from power stage, 4.0 W from auxiliary), in close agreement with the predicted loss (26.1 W from power stage, 4.0 W from auxiliary). The compliance with EMI and power quality standard was experimentally verified, which validated the EMI filter design.

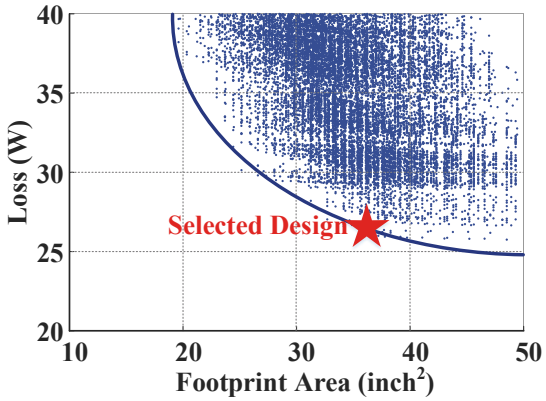


Fig. 1. Loss-Size Pareto Front of 5 kVA T-Type Converter.

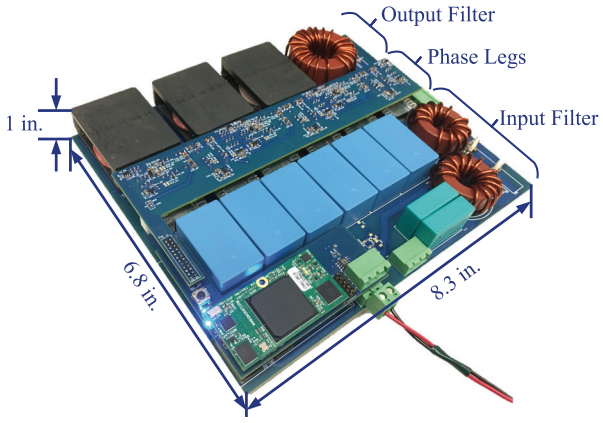


Fig. 2. Converter Prototype.

Center for Power Electronics Systems *– Virginia Tech*

1185 Perry Street
655 Whittemore Hall
Blacksburg, VA 24061

www.cpes.vt.edu