Appendix C. Miscellaneous Information about the Three-Phase VSC

C.01 PWM Signal Generation

The PWM signals for the three-phase VSI test are also generated by the EPLD and the DSP. The circuit configuration of the EPLD and the program for the DSP are based on that for the PEBB leg test. The EPLD and the DSP are modified to generate twelve sets of gate signals for the main and the auxiliary switches.

(a) The Logic Design

Two PWM signals are needed for the three-phase VSI test, according to Figure 5-12. Therefore, the EPLD needs to be designed to get the two main switch PWM signals and two auxiliary switch signals. The EPLD design for the three-phase VSI is based on the PWM pulse generating circuit. Figure C-2 is the basic functional block diagram of the design. Each block corresponds to a sub-design. The decoder receives control and address signals from the DSP and stores the corresponding data on designated latches. The timer makes an interrupt signal to the DSP and resets the state machine every switching period, which is every 256^{th} of the EPLD clock.

Since the duty ratio of a leg can be one for a 60^{o} period, the leg needs to be able to switch on or off continuously. With this function, the space vector modulation can be divided into six regions, as shown in Figure C-1. For example, at the boundary of the 30^{o}, when the phasor rotates from mode 1 to mode 3, the phase *C* can be kept turned on. The polarity of the phase *B* can be changed and increased from zero. The phase *A*, which is connected to *p* input continuously, can starts to be PWMed from the continuously turned on state. While the phasor travels from the mode 3 region to the mode 5 region, the phase

C becomes connected to *n* continuously. The duty ratio of the phase *A* can be changed from one to zero, and that of the phase *B* can be changed from zero to one while connected to *p* input.

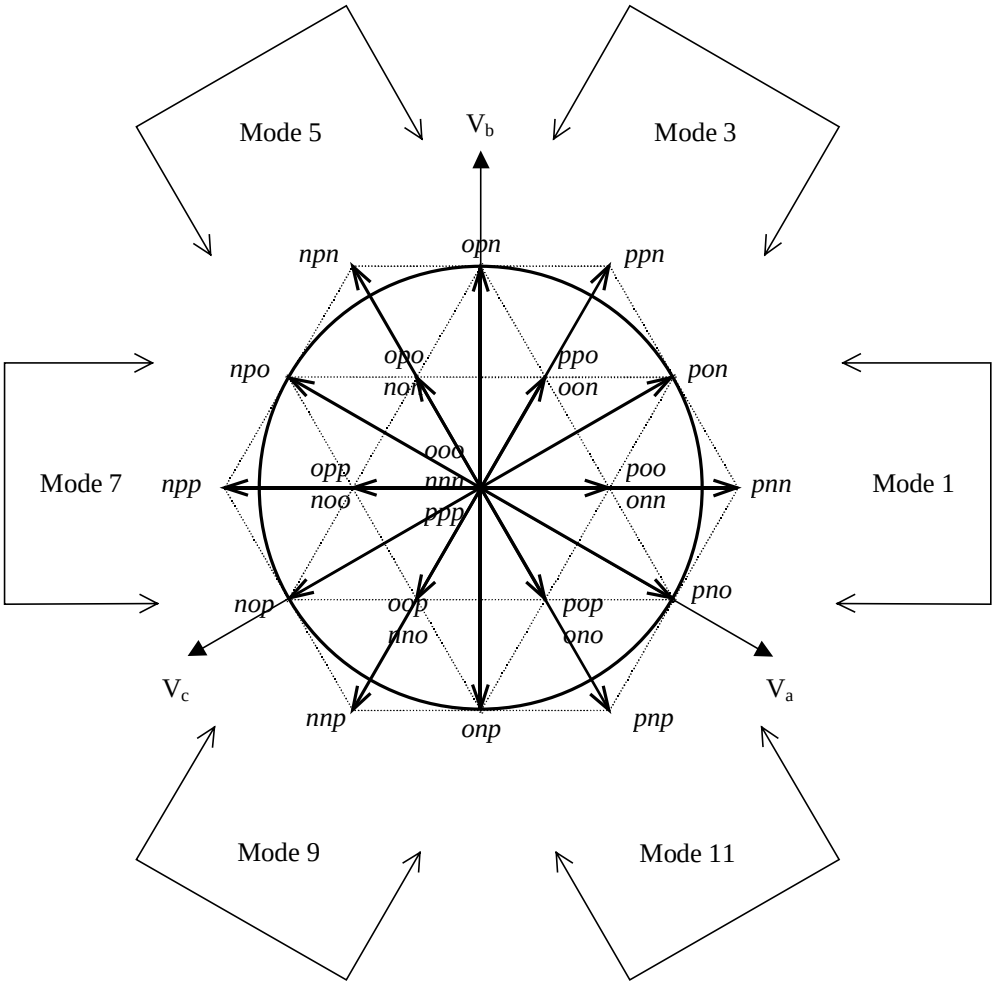


Figure C-1. Space-vector representation and its mode assignment of the three-level VSI

The PWM strategy described above can be implemented easily with the EPLD. The design of the EPLD includes four functional blocks: the decoder, timer, PWM signal generator, and switch combination circuit, as shown in Figure C-2. The decoder determines a latch to load the data from the DSP. The timer is used to give a periodic

interrupt signal to the DSP to get the next data. The PWM generation circuit developed for the PEBB leg test can be utilized as a subcircuit to generate two PWM signals for the three-phase SVM. These two signals can be connected to the switches of each leg through the switch combination circuit according to the mode information from the DSP.

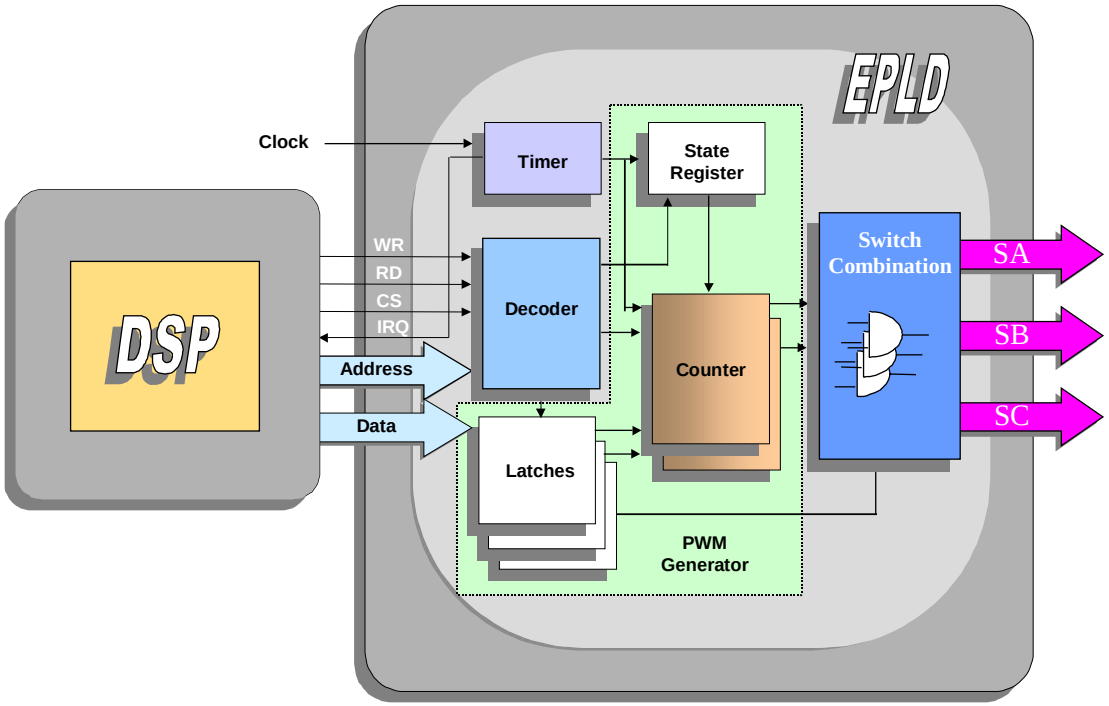


Figure C-2. EPLD functional block diagram for the three-phase VSI

Two EPLD chips, EPF8820ARC208-2 from Altera Corp., are used to generate the SVM signal to test the three-level VSI. There are a couple of problems that arouses during programming of the EPLD. The EPLD chip can operate up to a 80-Mhz clock, and a small delay between transitions can make a small, narrow glitch which can cause some undesired transition. One of the glitches is in the decoder, which is supposed to generate a latch signal for the each of the counters. The glitches are generated during the transition of WR signal, and cause an undesirable latching of data. Most of the decoder outputs include the glitches. Those glitches are eliminated when all of the output pins of the

decoder are given their default values, which are VCC. After the decoder has generated correct signals, all of the latches can get the correct values.

The next problem is in the state machine. This problem is related to the method of loading data into the counters and the state registers. At the beginning of the state, which is St_1, the state registers are reset by zero of the *Timer*. The reset command is of an asynchronous type, so is not synchronized with the value loaded into the counters, which are synchronized with the clock. To solve these problems, a couple of different combinations of asynchronization and synchronization methods are tried. The problem is eventually solved with a combination of asynchronous and synchronous methods. At the beginning of the state, all of the counter and state registers are loaded asynchronously. After the start of the state machine, all of the state transitions and loads of the counter are synchronized with the clock.

(b) DSP Programming

The DSP programming is also based on that for the PEBB leg test. However, for the three-phase SVM operation, the DSP is supposed to inform the EPLD which legs are switched. This information is the *mode* value shown in Figure C-1. Another difference from the PEBB leg test is the content of the circular table. In this case, the table contains the values for the 60° instead of 180°. The length of the table is 56 for the 60° of the 60-Hz output with a 20-kHz switching frequency. Figure C-3 shows the flow diagram of the DSP program.

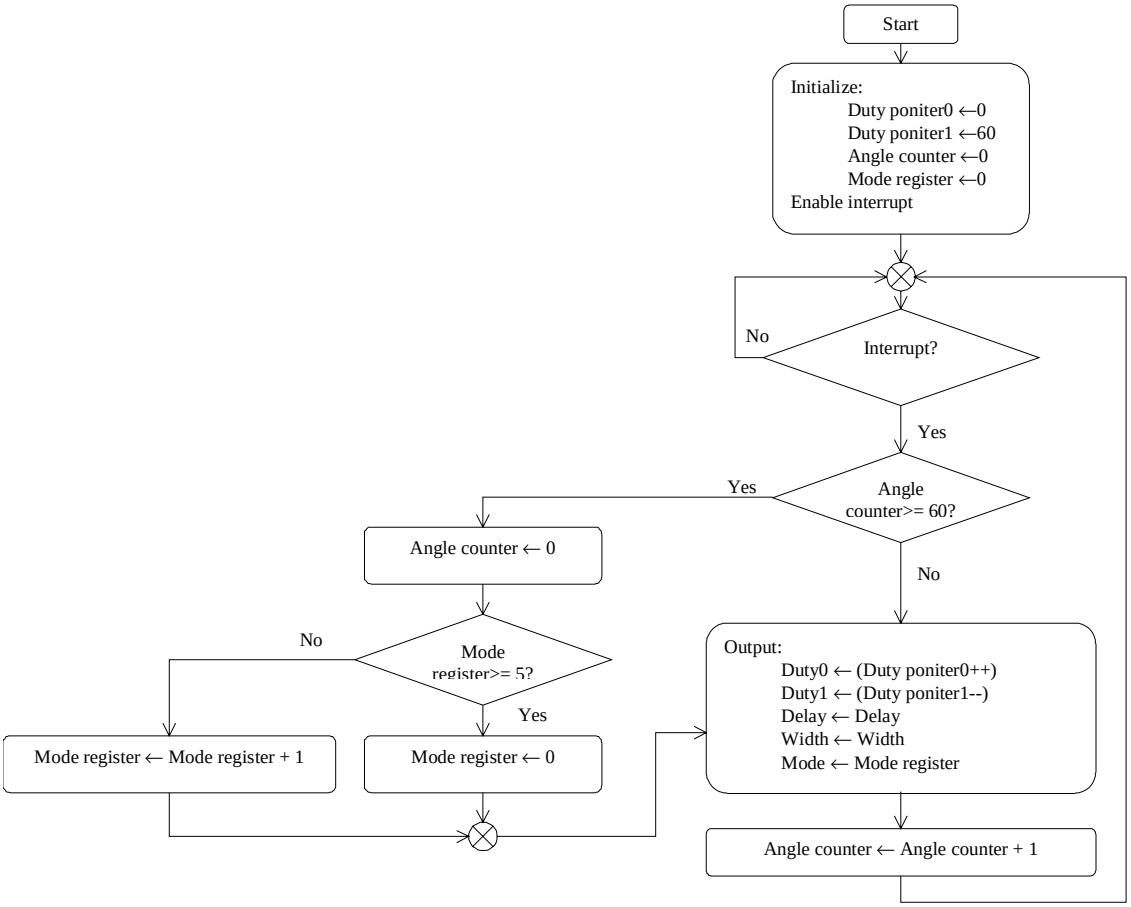


Figure C-3. Flow diagram of the DSP program

C.02 Noise at the Sensed Signal

Even though the sensors provide the galvanic isolation with the power stage, a great deal of EMI can be expected despite that. When the VSI power stage is excited, the voltage sensor experiences a great deal of noise. Many methods have been tried to reduce the noise through the sensor.

At first, a common mode choke is placed between the sensors and the ADC board, as shown in Figure C-4(a). Due to the location of the sensor, the CM choke does not work properly. Solutions to the problem of this noise can be explained as follows.

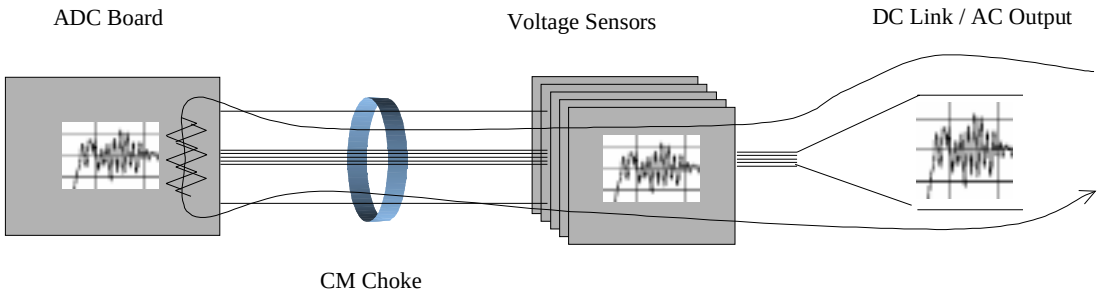
First, the sensors should be placed after the CM choke except the current sensor, which is difficult to isolate from the power stage due to its primary line.

Then, the series resistors need to be placed before the CM choke.

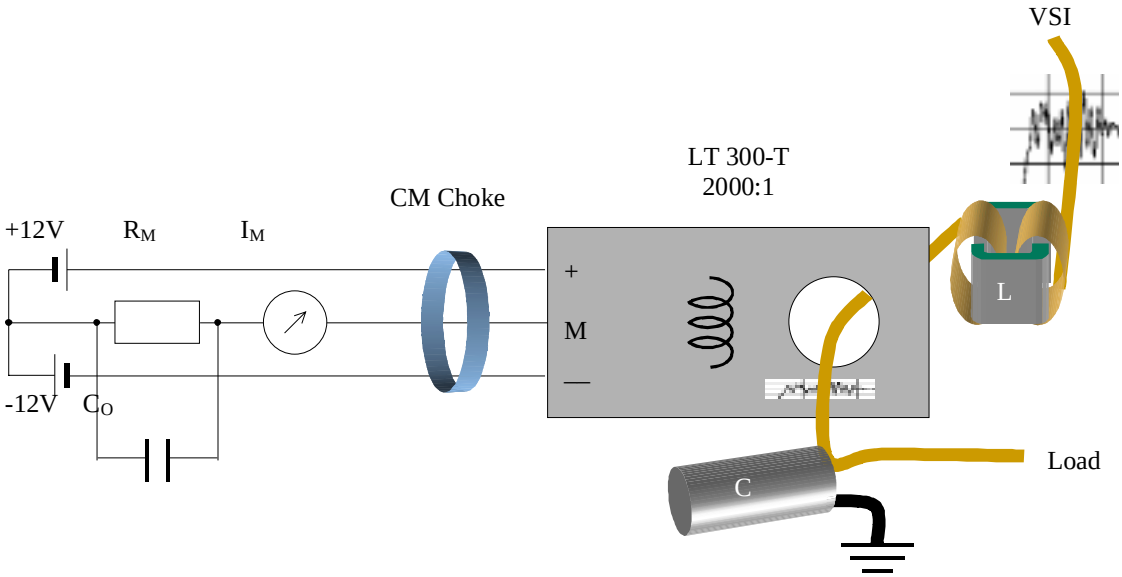
Third, the value of the series resistors have to be reduced to have a maximum current of 10-mA at 1000-V, which is 100-kΩ. This can increase the S/N ratio, due to the higher output for the same amount of noise.

After placing the CM choke before the sensor, the noise level is reduced. However, it is not enough, and the sensed signals oscillate. Another method tried involved using capacitors at various points. These capacitors can reduce the noise, but they also reduce the bandwidth of the sensors. Therefore, a compromise has to be made between the two solutions. The best choice in the capacitors are 0.1-μF at the output resistor and 820-pF at the input terminal. These capacitors not only reduce the noise but also are helpful in reducing the oscillation.

The current sensors, as mentioned before, cannot be placed after the CM choke. Instead of the CM choke, the main inductor can play similar role, and the sensor can then be placed after the main inductor, as shown in Figure C-4(b). By doing this, *dv/dt* at the sensor line is reduced from the direct output of the VSI to the capacitor voltage. Figure C-5 is a picture of the current sensor placed after the main inductors. Figure C-6 shows the voltage sensors placed after the CM choke.



(a) Voltage sensor



(b) Current sensor

Figure C-4. Location of sensors and noise path through the sensing line

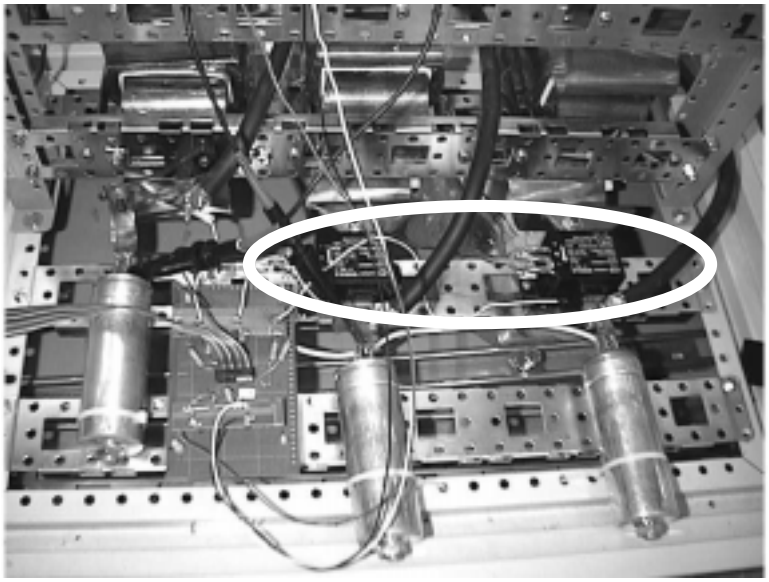


Figure C-5. Current sensors placed after main inductors

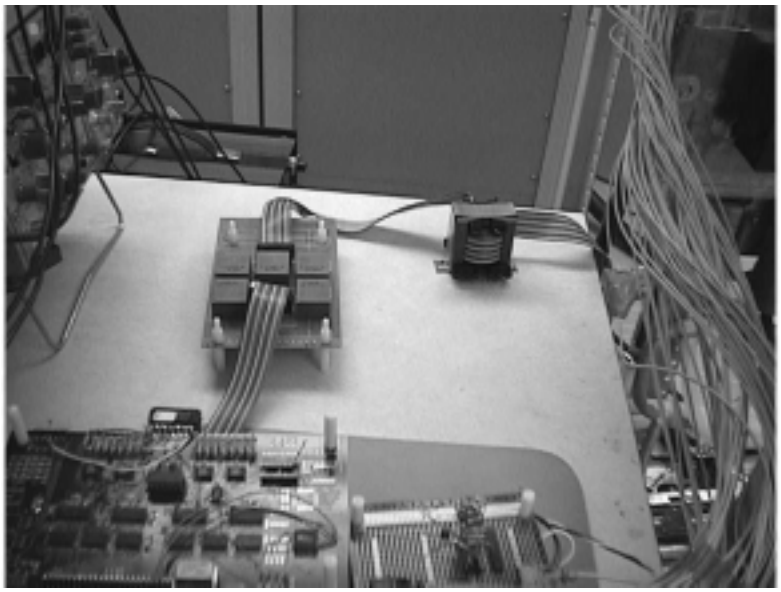


Figure C-6. Voltage sensors and CM choke for three AC outputs and two DC inputs