Performance Improvement of Power Conversion by Utilizing Coupled Inductors

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PERFROMANCE IMPROVEMENT OF POWER CONVERSION BY UTILIZING COUPLED INDUCTORS

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(ABSTRACT)

This dissertation presents the derivation, analysis and application issues of advanced topologies with coupled inductors. The proposed innovative solutions can achieve significant performance improvement compared to the state-of-the-art technology.

New applications call for high-efficiency high step-up DC-DC converters. The basic topologies suffer from extreme duty ratios and severe rectifier reverse recovery. Utilizing coupled inductor is a simple solution to avoid extreme duty ratios, but the leakage inductance associated with the coupled inductor induces severe voltage stress and loss. An innovative solution is proposed featuring with efficient leakage energy recovery and alleviated rectifier reverse recovery. Impressive efficiency improvement is achieved with a simple topology structure. The coupled inductor switching cell is identified. Topology variations and evaluations are also addressed.

The concept that utilizes coupled inductors to alleviate rectifier reverse recovery is then extended, and new topologies suitable for other applications are generated. The proposed concept is demonstrated to solve the severe rectifier reverse recovery that occurs in continuous current mode (CCM) boost converters. Significant profile reduction and power density improvement can be achieved in front-end CCM power factor correction (PFC) boost converters, which are the overwhelmingly choice for use in telecommunications and server applications.

This dissertation also proposes topologies to realize the single-stage parallel PFC by utilizing coupled inductors. Compared to the state-of-the-art single-stage PFC converters, the proposed topologies introduce a new power flow pattern that minimizes the bulk-capacitor voltage stress and the switch current stress.

TO MY WIFE MIAO, SON ETHAN XING-YI

AND

MY PARENTS

YUNSHENG ZHAO
YING WANG

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Chapter 1.

Introduction

1.1. Research Background

Instead of conventional lamps, high intensity discharge (HID) lamps are preferable for use as the headlamps for high-end automobiles because of their significant advantages, such as longer life, better color-rendering properties, and higher efficacy in converting the electrical power to visible light. Fig. 1.1 compares road conditions with a 36W HID lamp and a 55W conventional lamp [B2]. As can be seen, although the HID lamp consumes one-third less power, it provides a much better road condition than that achieved with a conventional lamp. Another advantage of the HID lamp is the good focusing capability of the light beam, as shown in Fig. 1.2(a). The focused far-reaching light beam provides drivers with more safety and comfort. The HID lamp also has a much longer lifetime than that of the traditional lamp, as shown in Fig. 1.2(b). A HID lamp can last about ten thousand hours, while the conventional reaches only about three thousand. Although the HID lamp has so many advantages, it is the same as all other discharge lamps that require a ballast to control the lamp power during steady state. The voltage drop of the 36W HID lamp is from -60 to -100V. During the ignition period of the lamp, a -400V open circuit voltage is also necessary. Since the power source of the HID headlamps are the automobile 12V battery, which provides a voltage much lower than the lamp operation voltage, a

high step-up DC-DC converter is necessary in the ballast to supply the low battery voltage with a voltage gain of about tenfold for steady-state operation.

(a) (b)

Fig. 1.1. Comparison of road conditions with different headlamps [B2]:
(a) 35W HID lamp and (b) 55W conventional lamp.

(a) (b)

Fig. 1.2. High performance of HID lamps:
(a) good focusing capability [B2] and (b) longer lamp life.

The requirements for the high step-up in the HID ballast converter are as follows:

- ***High step-up voltage gain.*** The voltage of the automobile battery is 9 to 16V, and the steady-state voltage of the lamp is -60 to -100V. About ten times the step-up gain is

required to boost the battery to the required operation voltage of the lamp. During the startup period, a -400V open circuit voltage must be provided.

- ***High efficiency.*** The encapsulated environment of the car provides a bad thermal condition for the converter. High-efficiency DC-DC converters can dramatically reduce the thermal management cost. The target efficiency of the high step-up DC-DC converter is 90% [B1].
- ***No isolation is required.***

Fig. 1.3 is a block diagram of a HID ballast for automobiles. The ballast calls for high efficiency high step-up DC-DC converters that do not require isolation. The high-frequency DC-DC converter is used to boost the nominal 9-16V battery voltage to -60 V to -100V with a constant 36W of output power. To extend the life of the lamp, one terminal of the output voltage must be negative referring to the input ground in order to avoid the migration of the material in the lamp. During the startup process, the DC-DC converter should be capable of generating a -400V open-circuit voltage to ignite the lamp. An unregulated low-frequency DC-AC full-bridge converter that contains no magnetic component follows the DC-DC converter. This DC-AC converter is used to chop the DC output voltage to a 50% duty cycle at 400Hz of low frequency to avoid the acoustic resonance of the lamp. The performance of the front-end DC-DC converter dominates the performance of the whole ballast system because the second DC-AC stage is an unregulated low-frequency full-bridge converter without magnetic components. A high-performance, high step-up DC-DC converter is a crucial part for the ballast.

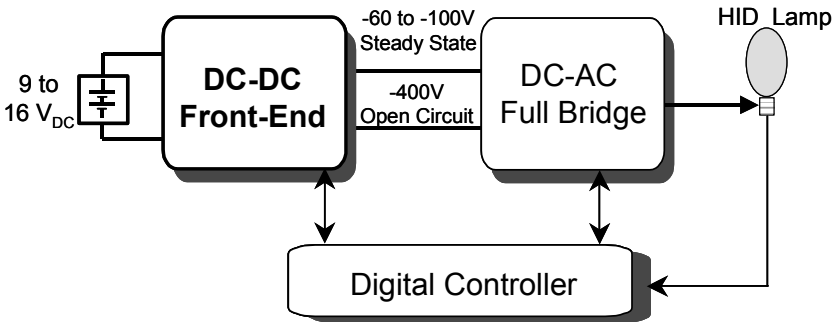


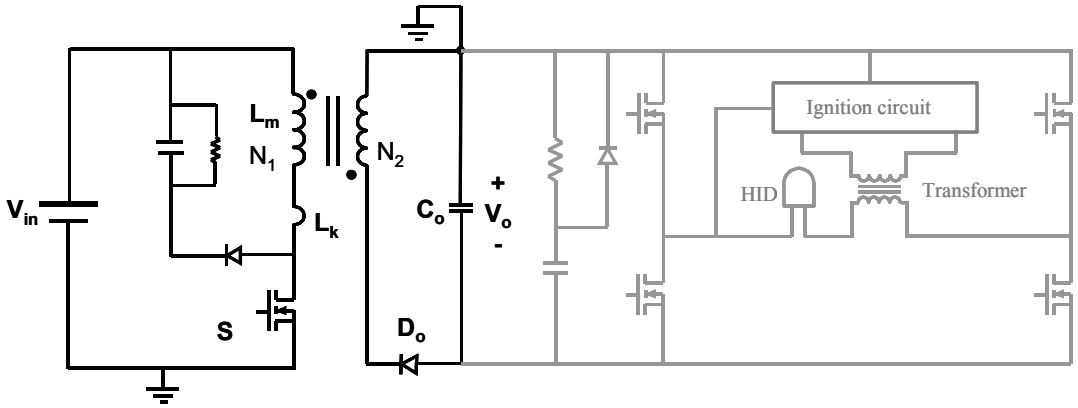
Fig. 1.3. Block diagram of HID ballast for automobiles.

The buck-boost converter is the simplest non-isolation topology for this application. However, a buck-boost converter encounters extreme duty ratios to provide the tenfold step-up voltage gain during steady-state operation. In particular, the requirement of –400 startup voltage severely penalizes the efficiency since the device rating is about 500V. This high voltage rating device is not a good choice for the steady-state operation because of the high input current. The converter has high conduction and switching losses under extreme duty ratio operation. The challenge for this high-efficiency, high step-up DC-DC converter is to avoid extreme duty ratios so that conduction loss and switching loss can be dramatically reduced. The cascade structure can be used to avoid the extreme duty ratios; however, the –400V startup voltage remains problematic in terms of efficiency.

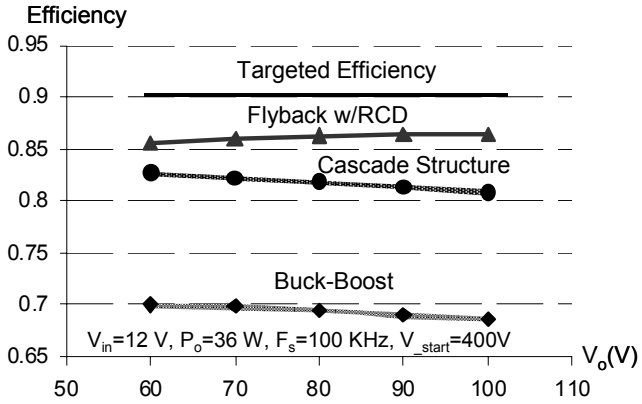
Utilizing a coupled inductor is a solution. Fig. 1.4(a) shows the circuit diagram of the state-of-the-art HID ballast for automobile headlamps. The front-end step-up DC-DC converter is a Flyback converter with a resistor-capacitor-diode (RCD) snubber. The downstream full-bridge converter does not have much impact on the performance. Fig. 1.4(b) shows the efficiency

comparison between the buck-boost converter, the cascade structure, and the Flyback converter for this HID front-end DC-DC application [Appendix A]. The efficiency of the Flyback converter for this application is about 85% to 86%, which is much lower than the targeted 90%. Although the Flyback converter can provide high step-up voltage gain, the leakage inductance of the coupled inductor not only increases the voltage stress of the switch but also induces significant loss. The RCD snubber can alleviate the voltage stress of the switch, but all of the leakage energy is dissipated. The input ground and the positive terminal of the output are connected in the Flyback converter so that one of the output terminals is negative referring to the ground. This solution does not take advantage of the fact that isolation is not required in this application.

An advanced solution to handle the leakage energy must be identified, because the loss analysis shows that the leakage inductance induces significant loss. If the loss related to the leakage inductance can be recovered, the efficiency can be higher than 90%. Finding a way to improve the performance of the high step-up converters is one of the motivations of this dissertation.



(a)



(b)

Fig. 1.4. State-of-the-art HID ballast:
(a) ballast circuit diagram and (b) efficiency comparison of the front-end step-up converter.

In the application of HID lamps for high-end automobiles, the steady-state power is 36W and the output voltage is –60 to –100V. At this power and output voltage, the output rectifier reverse-recovery problem is not a major concern. For some other high step-up applications with higher levels of output power and output voltage, the rectifier reverse-recovery problem is another possible concern. Fig. 1.5(a) shows a distributed power system (DPS) with an uninterruptible power supply (UPS). The AC-DC front-end converter provides power factor correction (PFC)

and a roughly regulated 380 to 400V DC bus. The downstream DC-DC converter provides tightly regulated output voltage and isolation. During a blackout period, the UPS generates AC voltage from the battery. However, the UPS typically provides 30 minutes of reserve time. The convergence of computer and telecommunications industries makes the well-defined -48V DC battery plant the natural choice for providing hours of reserve time during outages in the AC mains [B7]-[B9]. The emerging DC-backup converter is a simple and efficient solution compared with the UPS solution, since it contains only a DC-DC converter instead of an inverter. Fig. 1.5(b) shows a dual-input front-end boost converter. A non-isolation DC-DC converter instead of a UPS inverter (AC UPS), both of which would be powered by the 48V DC power plant, is more efficient and much less complex [B8]-[B11]. A high-efficiency DC-DC converter that can generate 380V DC bus from a 48V DC plant is the most important part of the DC-backup system. It should be pointed out that isolation is not necessary for the AC-DC or DC-DC front-end converter, since the isolation is provided by the consequent DC-DC stages. The DC-input front-end converter must provide approximately ten times the voltage gain.

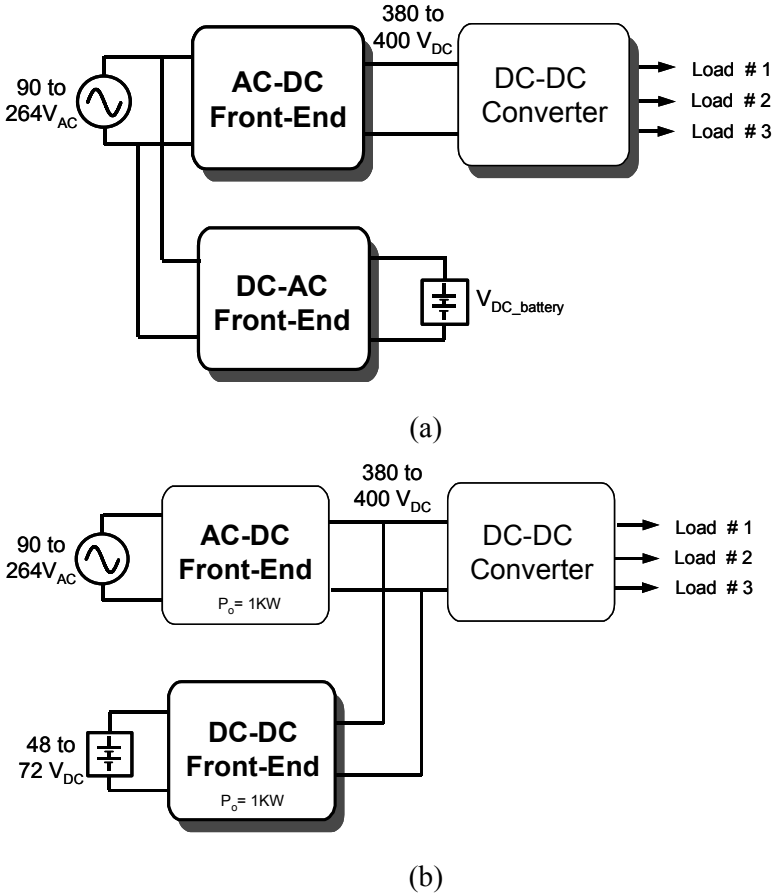
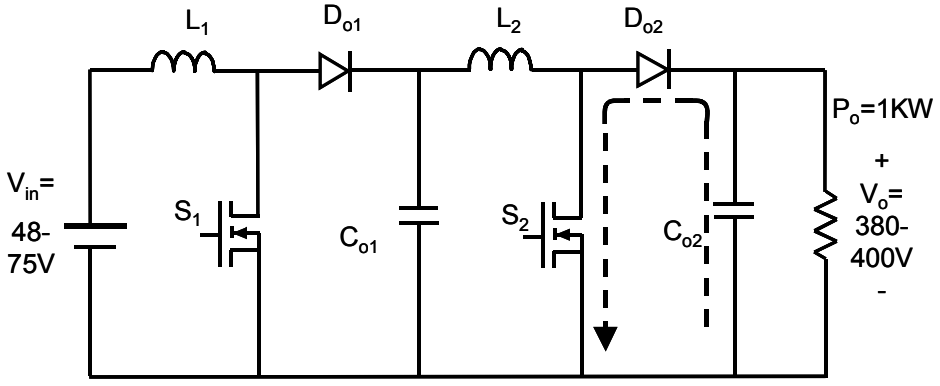


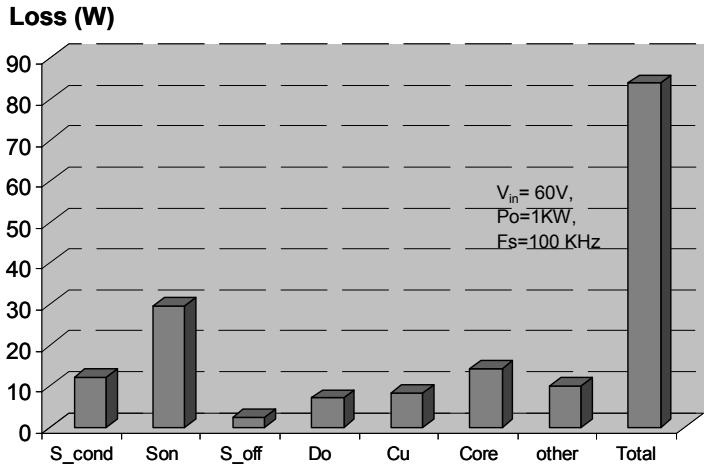
Fig. 1.5. Different backup schemes:
(a) AC-UPS and (b) dual-input front-end converters [B9].

In a HID ballast, the –400V startup voltage severely penalizes the efficiency of both the buck-boost and the cascade converters. For the DC-backup application, different specifications make the cascade boost converter the state-of-the-art solution, as shown in Fig. 1.6(a). However, the cascade structure is only used to avoid the extreme duty ratios for high step-up voltage gain. CCM operation of a power converter is preferred because of the low current stress to the switch. The output rectifier reverse-recovery problem of rectifier D_{o2} can result in high levels of turn-on loss for the switch. Fig. 1.6(a) shows the loss breakdown of the cascade converter with 1kW of

output power. The loss due to the rectifier reverse recovery is the most salient portion of total losses. This high switching loss dramatically deteriorates the thermal condition of the switch.



(a)

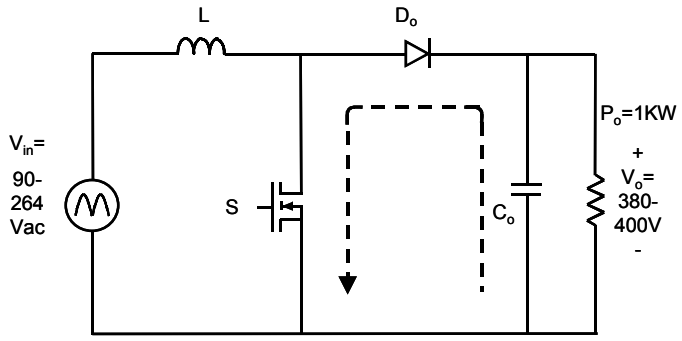


(b)

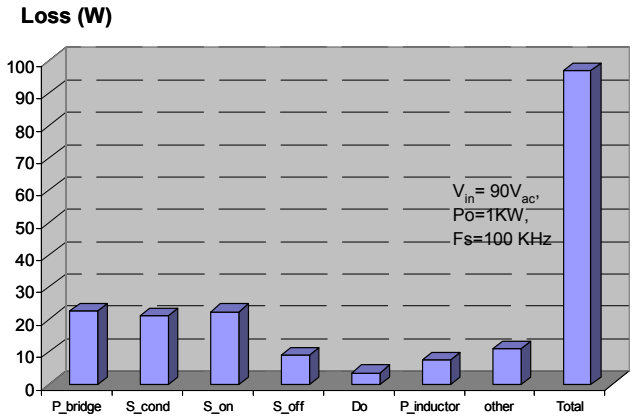
Fig. 1.6. The cascade boost is used for the DC-input converter:
(a) circuit diagram and (b) loss breakdown.

The second challenge for the high-efficiency, high step-up DC-DC converters is to alleviate the rectifier reverse recovery so that the switching loss can be dramatically reduced. Elimination of extreme duty ratios and alleviation of the rectifier reverse-recovery problem can significantly improve the efficiency of the power conversion.

It is also well known that the front-end PFC AC-DC converters shown in Fig. 1.7(a) have the same rectifier reverse-recovery problem when they are operated in CCM because of the 380 to 400V DC output voltage. The difference is that the duty ratio must change within a very large range in order to achieve unity power factor. In other words, the extreme duty ratio is not a concern but the rectifier reverse-recovery problem is. Fig. 1.7(b) shows the loss breakdown of a 1KW boost converter with 90V AC input voltage. The switch turn-on loss could be dramatically reduced if an approach to alleviate the rectifier reverse recovery would be adopted. The rectifier reverse-recovery problem deteriorates the thermal condition of the boost switch. The extreme thermal condition limits the power of a front-end boost converter. The performance of both AC-input and DC-input front-end converters is dramatically degraded. The solution of alleviating rectifier reverse-recovery problem benefits both the AC-input and the DC-input front-end converters. Finding a simple and effective solution to alleviate the rectifier reverse recovery in the DC-backup power supply and the AC-DC front-end converter is another motivation of this dissertation.



(a)



(b)

Fig. 1.7. CCM boost converter as the front-end boost converter:
(a) a front-end boost converter and (b) loss breakdown.

As can be seen from the proceeding analysis, the extreme duty ratio and severe rectifier reverse-recovery problem are the two major challenges for the relevant applications. Table 1.1 summarizes the major problems in these applications. Advanced topologies with coupled inductors developed in this dissertation demonstrate that the proposed solutions can achieve a significant performance improvement.

Table 1.1. Problems to be solved.

Applications	Specifications	Identified Problems	
		Duty Ratios	Reverse-Recovery Problem
High Step-Up for HID Ballast	V_{in}=9 to16V, V_o=-60 to –100 (Ignition 400V) P_o=36W	**Extreme**	Not Severe
DC-Input Backup Converter	V_{in}=48 to 72V_{dc}, V_o=380 to 400V_{dc} P_o=1KW	**Extreme**	**Severe**
AC-Input Front-End Converter	V_{in}=90 to 264V_{ac}, V_o=380 to 400V P_o=1KW	Variable (Not a Problem)	**Severe**

1.2. Dissertation Outline and Major Results

This dissertation addresses solutions to improve the performance of power conversion by utilizing coupled inductors for different applications. When a converter is operated under extreme duty ratios to provide large conversion ratios, it suffers from high voltage and current stresses. When a buck-boost converter is used for this HID application, the efficiency is around 70% because of the penalty that results from the extreme duty ratios and the –400 startup voltage. For the high step-up DC-DC converter in a HID ballast, the output power and output voltage are relative low. The major concern is to avoid the extreme duty ratio so that the conduction and switching losses can be reduced. To avoid extreme duty ratio and complexity of the topology, a coupled-inductor converter, such as a Flyback converter or a coupled-inductor Sepic converter, is a good option for low-power applications. By utilizing a coupled inductor, various voltage gains can be achieved by properly designing the turns ratio. The problem is that

the leakage inductance of a coupled inductor has detrimental effects on the performance of the converters. The state-of-the-art solution is a Flyback converter with RCD snubber. The efficiency is about 85% to 86%, which is far below the targeted 90% [B1]. The active-clamp scheme minimizes the switch voltage stress and offers an efficiency improvement of about 3%.. The drawbacks of the active-clamp scheme are its complex topology and control circuit. For applications that do not require isolation, methods available to handle leakage energy do not take advantage of the lack of an isolation requirement. In Chapter 2, a non-isolation coupled-inductor buck-boost converter is first derived from the Flyback converter. The active-clamp scheme is then applied to this converter. The active switch in the active-clamp scheme provides a discharge path for the clamp capacitor; However, analysis shows that this discharge path exists through the secondary coupled winding and the output rectifier. Therefore, the active switch in the active-clamp circuit can be eliminated. A novel leakage recycling scheme with a simple topology is proposed, as shown in Fig. 1.8.

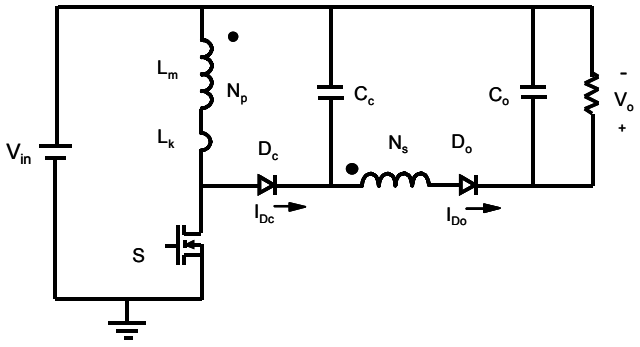


Fig. 1.8. Clamp-mode coupled-inductor buck-boost converter.

The proposed clamp scheme only needs an extra rectifier D_c and a clamp capacitor C_c, and it can realize a function similar to that of the active-clamp scheme. Furthermore, the proposed

scheme has much less current circulating in the clamp circuit as compared to the active-clamp scheme. Significant efficiency improvement can be achieved for the proposed converters. The proposed topology can achieve more than 90% efficiency with the input voltage variation range from 9 to 16V for the front-end converter of the HID ballast. Topology derivation, operation analysis, design issues and experimental verification are addressed in the first part of Chapter 1. The coupled-inductor switching cell is then identified. In practical applications, leakage energy must be handled properly for the family of converters that use the coupled-inductor switching cell. The proposed concept for recycling the leakage energy is then generalized and applied to other non-isolation coupled-inductor step-up converters. New clamp-mode coupled-inductor topologies are generated.

The clamp-mode coupled-inductor boost converter as shown in Fig. 1.9 is a member of the new circuits. This converter can be used as the DC-backup power supply. For the DC-backup power supply, the output voltage is 380 to 400V, and the output power is 1KW. It has been shown that the rectifier reverse recovery becomes another concern in this high step-up application. The current solution for alleviating the rectifier reverse-recovery problem is to control the di/dt of the rectifier during its turn-off time period. To accomplish this purpose, an auxiliary circuit is necessary. But for the proposed solution, alleviating the rectifier reverse-recovery problem can be achieved without any extra circuit because the clamp scheme can inherently realize the current steering. During the switch turn-off time period, the magnetizing current will shift from loop 1 (dashed-line loop) to loop 2 (solid-line loop). Before switch S turns on again, the complete current shifting is guaranteed so that rectifier D_c is naturally recovered. When S turns on again, rectifier D_o turns off. Since rectifier D_o is in series with a coupled

winding, the leakage inductance of the coupled winding controls the di/dt of the output rectifier Do. The rectifier reverse-recovery problem is thus alleviated. The operation of the current steering process, design details that guarantee the current shifting, and experimental verification are also provided in Chapter 2.

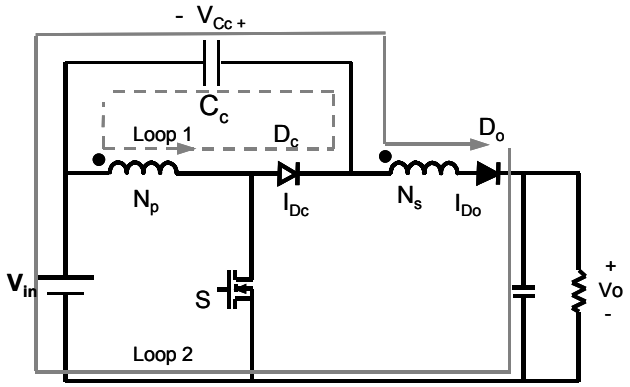


Fig. 1.9. Clamp-mode coupled-inductor boost converter.

The rectifier reverse-recovery problem is also a concern for the PFC front-end converter, and can dramatically degrade its performance. A method for alleviating the rectifier reverse-recovery problem by utilizing the current steering of the coupled inductor is discussed in Chapter 3. Starting from the coupled-inductor switching cell covered in Chapter 2, an equivalent coupled inductor switching cell is derived. A simple discharge path for the leakage energy is through the output voltage source. A family of new topologies with alleviated rectifier reverse-recovery problem is proposed. Fig. 1.10 shows the boost version. The current steering process is similar to that of the high step-up DC-DC converter. After switch S turns off, the magnetizing current will shift form the loop with a dashed line (loop 1) to the current loop with a solid line (loop 2). Under proper design, the complete current shift from loop 1 to loop 2 can be achieved during the

switch turn-off time period. Therefore, rectifier D_c can be naturally recovered. When switch S turns on, rectifier D_o turns off. Since rectifier D_o is in series with a coupled winding, the leakage inductance of the coupled winding controls the di/dt of the output rectifier. The rectifier reverse-recovery problem is alleviated. In Chapter 3, topology development, operation principle design issues, and parasitic resonance handling for practical applications are addressed. Experimental results show that an efficiency improvement of more than 2% can be achieved for a 1KW front-end CCM PFC boost converter with universal line input. By adopting the proposed solution, the thermal condition of the MOSFET is dramatically improved. Improved power density and reduced profile are achieved. In Chapter 3, the proposed solution is also demonstrated with a low-profile (1U), high power-density (11W/inch^3) front-end converter.

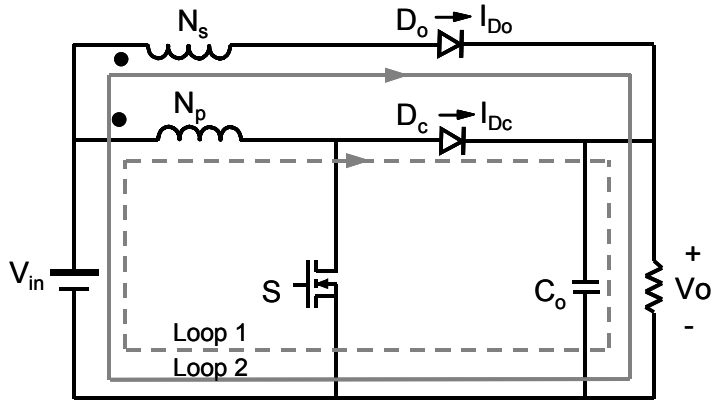


Fig. 1.10. Coupled-inductor boost converter with alleviated rectifier reverse-recovery problem.

In Chapter 4, a new coupled-inductor switching cell is derived from the ideal coupled-inductor switching cell. The equivalent circuit is shown in Fig. 1.11(a). When the input voltage source is separated into two voltage sources, a new feature emerges: The current path to charge

the magnetizing inductor can be changed as the voltage sources are varied. The converter then has two possible charge paths, as shown in Fig. 1.11(b). This converter can be utilized to realize single-stage parallel PFC (PPFC). The goal of PPFC is to not process all the power twice in an AC-DC converter with PFC; only 32% of the output power must be processed twice. This scheme reveals the benefit of efficiency improvement. In order to realize unity power factor with PPFC, the converter consists of two stages. Because stage one and stage two are two different converters, the complexity of the circuit makes the solution less cost-effective in low-power applications. The proposed converter can realize PPFC in low-power applications in which the input current harmonic requirement is not stringent. Compared to the conventional single-stage approach, in which the bulk capacitor voltage and the switch current stress are the major concerns, the proposed converters have much lower voltage stress and the switch current stress is minimized.

The proposed single-stage coupled-inductor PPFC converters realize a new power flow pattern, which is different from the current single-stage approach. This new pattern allows for a direct load current feedback, which automatically reduces the input power when the output power decreases. The concerns of bulk capacitor voltage stress and switch current stress in the current single-stage approach are eliminated. Theoretical analysis and the experimental results verify the proposed solution.

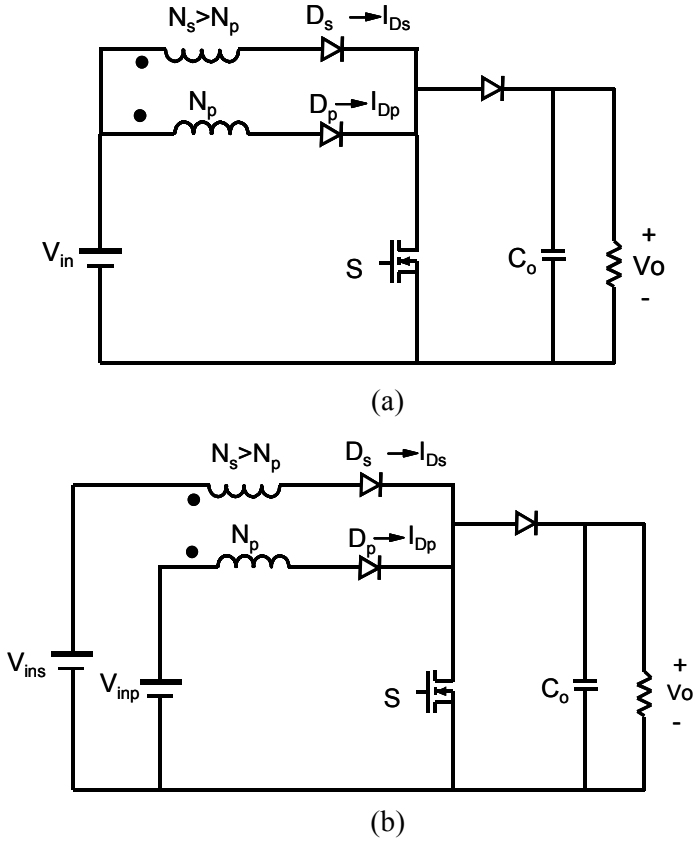


Fig. 1.11. Derivation of PPFC topologies:
(a) an equivalent circuit of the converter shown in Fig. 1.10 and
(b) topology with two separated voltage sources.

In Chapter 5, the functions of the coupled inductor studied in this dissertation are summarized, and the possible future work is discussed.

Chapter 2.

High-Efficiency, High Step-up Coupled-Inductor DC-DC Converters

2.1. Introduction

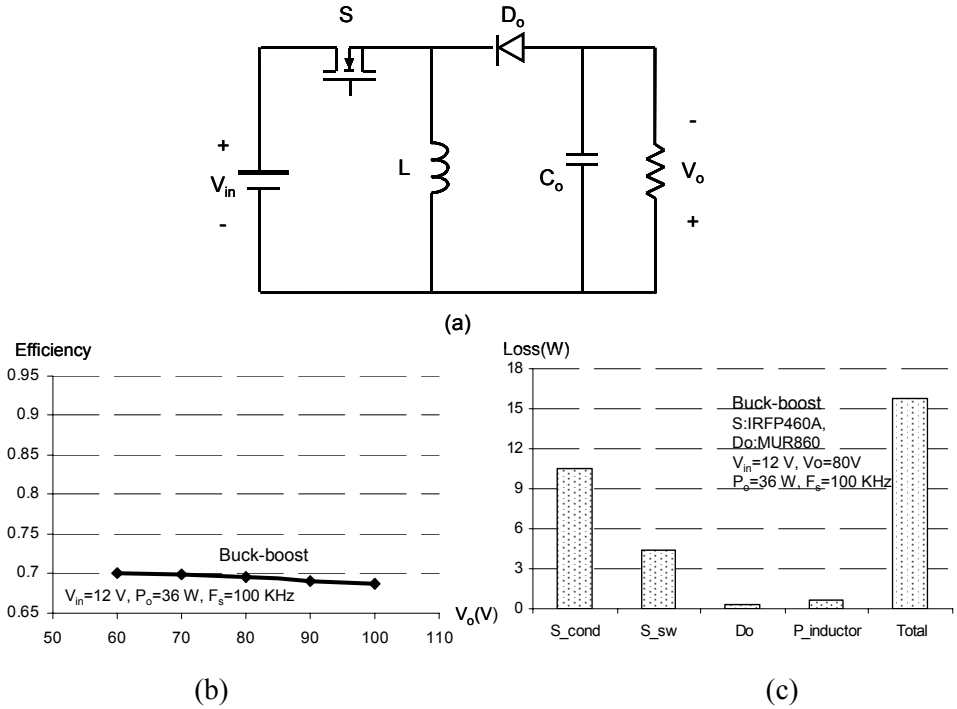
The major concern related to the efficiency of the high step-up converters for the HID lamp ballast is the extreme duty ratio that exists if basic topologies, such as buck-boost and boost, are used. Because of the high input current that results from the low input voltage, low-voltage-rated devices with low $R_{DS\text{-}on}$ are necessary to reduce the conduction loss. The buck-boost converter is the simplest non-isolation topology that can achieve the step-up function and negative output for the HID ballast. Unfortunately, 500V-rated devices are necessary to generate the 400V DC voltage for the ignition. Furthermore, the high output voltage and the short pulse current with high amplitude through the output rectifier (due to the extreme duty ratio) induce high switching loss. Instead of non-isolation converters, the Flyback converter could be used [B4][B5][B16]. The coupled inductors are used not for isolation but for high step-up voltage gain in this application, because there is no isolation requirement. Converters with coupled inductors can easily achieve high step-up voltage gain, utilizing low $R_{DS\text{-}on}$ switches for this low-power application. Unfortunately, the leakage energy induces high voltage stress, large switching losses, and severe EMI problems. Either a snubber circuit or an active-clamp scheme is necessary to handle the leakage energy. The use of a RCD snubber is a simple solution, but all of the leakage energy is dissipated in the snubber circuit. An active-clamp circuit can recycle the leakage energy, but at the cost of topology complexity and some losses related to the clamp

circuit [B16]. Although the active-clamp Flyback converter can achieve the highest efficiency, as compared to other solutions, this approach does not take advantage of the fact that isolation is not required.

This chapter presents a family of high-efficiency, high step-up clamp-mode converters derived from the non-isolation coupled-inductor converters by taking advantage of the lack of an isolation requirement. The non-isolation coupled-inductor buck-boost converter is first derived from the Flyback converter. Then, a novel and simple clamp scheme for recycling the leakage energy is proposed. The operation of the proposed converter is similar to that of its active-clamp counterparts, but with better performance. In the proposed converter, only one diode and a small clamp capacitor are added to the coupled inductor converter. The additional diode serves as the body diode of the active-clamp switch, and the coupled winding and output rectifier serve the same function as the active-clamp switch [B16]. Topologies with one active switch have significantly reduced cost and circuit complexity, as compared to those using the active-clamp scheme. Therefore, the reliability of the converter could be dramatically increased. The proposed clamp-mode coupled-inductor converter can use a low-voltage-rated active switch for the conduction loss reduction. The clamp circuit recovers the leakage energy with a lower circulating current. High efficiency is achieved because of the low $R_{DS\text{-}on}$ of the switch and the efficient leakage energy recycling. The concept is the then generalized and extended to other topologies.

2.2. Topology Evaluations for HID Ballast Converter

The operation of a power converter under extreme duty ratios can result in high voltage and current stresses incurred to achieve high step-up voltage gain. For the 36W HID front-end converter, the buck-boost converter (negative output is required), as shown in Fig. 2.1, is the simplest non-isolation topology. Unfortunately, 500V-rated devices are necessary to generate the 400V open-circuit voltage. Furthermore, the high output voltage and short pulse current, with high amplitude through the output rectifier due to the extreme duty ratio, induce high levels of switching loss. The high conduction loss that occurs due to the high $R_{DS\text{-}on}$ of the switch, and the high switching loss resulting from the short pulse current with high amplitude, dramatically degrade the efficiency. The results of loss analysis are shown in Fig. 2.1(b)(c).



(b) (c)

Fig. 2.1. Buck-boost converter under extreme duty ratio:
(a) buck-boost converter; (b) calculated efficiency; and (c) loss breakdown.

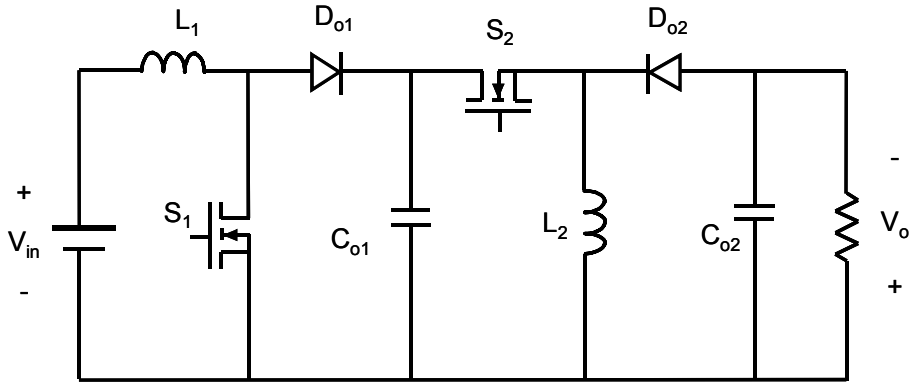
The non-isolation converters [B13] can provide high step-up voltage gain without incurring an extreme duty ratio. For example, the voltage gain of the third-order two-switch converter is given by Eq. 2-1:

$$\frac{V_o}{V_i} = \frac{d}{1-2\cdot d}, \qquad \text{Eq. 2-1}$$

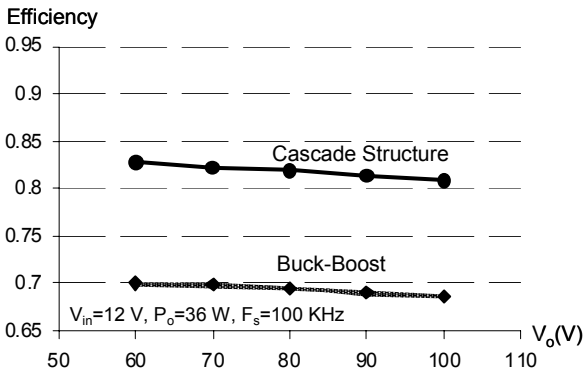
where the d is the duty ratio. The voltage gain is infinite when the duty is equal to 0.5 for the third-order two-switch converter. The basic idea for this group of circuits is to store sufficient energy in the inductors by putting the input and output voltage sources in series during the switch-on time. However, having the output voltage source charge the inductor introduces high circulating current. Another problem with this idea is the high voltage stress of the active switch, which is 2Vo+Vi. For HID applications, the voltage rating of the switch needs to be higher than 900V. The high $R_{DS\text{-}on}$ of the switch and the huge circulating current make it extremely difficult to achieve decent efficiency with these converters. Although this converter can avoid extreme duty ratio for high step-up voltage gain, it is neither a cost-effective nor an efficient solution. The conduction loss will degrade the efficiency to lower than 70%.

The cascade step-up DC-DC converter is another solution for avoiding extreme duty ratios. Fig. 2.2(a) shows a cascade structure with boost converter and a buck-boost converter (for negative output). By utilizing the cascade structure, both stages can realize step-up functions without extreme duty ratio, and thus the conduction loss and switching loss are significantly reduced. The intermediate DC bus is designed as 36 to 40V so that the extreme duty ratio can be avoided for both stages. Fig. 2.2(b)(c) shows the calculated efficiency and the loss breakdown

(S_1:IRF24N, S_2:IRFP460A, D_{o2}:MUR860). For the first stage, the voltage rating of the device could be 55V in order for the conduction loss of the switch to be very low even though the input current is high. For the second stage, the input current is low due to the boosted voltage, and thus the conduction loss is reduced. As can be seen, both conduction loss and switching loss are dramatically reduced. However, form an efficiency standpoint, it is preferable that the energy not have to be processed twice.



(a)



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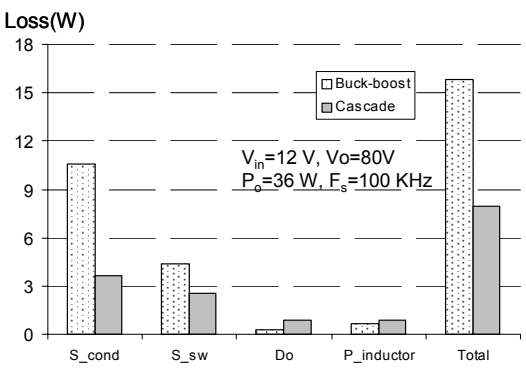


(c)

Fig. 2.2. Analysis the feasibility of the cascade structure:
(a) topology structure; (b) calculated efficiency; and (c) loss comparision.

Instead of non-isolation converters or cascade non-isolation DC-DC converters, converters with coupled inductors, such as the Flyback or isolation SEPIC converters, could be used

[B4][B5][B14][B15]. State-of-the-art solutions are the Flyback or coupled inductor SEPIC converters for this low-power high step-up applications [B4][B5]. Converters with coupled inductors can easily achieve high step-up voltage gain utilizing the transformer function of a coupled inductor. Therefore, extreme duty is avoided and low $R_{DS\text{-}on}$ switches could be used. The conduction and switching losses are dramatically reduced.

However, the leakage energy of a coupled inductor induces not only high voltage stress but also high losses. A leakage recycling circuit must be used. Due to its simplicity, the RCD snubber is adopted in the HID ballast. Unfortunately, the RCD snubber dissipates all the leakage energy in the resistor after the switch turns off. The equivalent circuit of the Flyback converter after the switch turns off is shown in Fig. 2.3(a). Fig. 2.3(b) shows the current waveforms of the leakage and the reflected output current. After the switch turns off, the leakage inductor current decreases and the magnetizing current increases. There is an overlapping time period t_c for the current transfer.

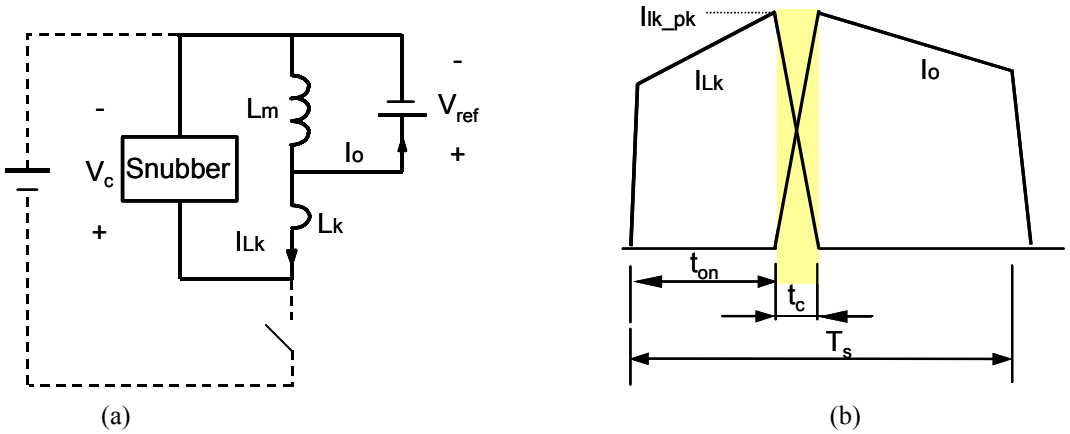


Fig. 2.3. Equivalent circuit of the Flyback converter and the current waveforms: (a) the equivalent circuit and (b) waveforms for loss calculation.

The overlap time of t_c can be calculated as follows:

$$t_c = \frac{I_{Lk\_pk} \cdot L_k}{V_c - V_{ref}}. \qquad \text{Eq. 2-2}$$

The loss related to the leakage inductance is then given by:

$$P_{Loss\_Lk} = \frac{1}{2}(I_{Lk\_pk}^2 \cdot L_k + I_{Lk\_pk} \cdot V_{ref} \cdot t_c) \cdot F_s \ . \qquad \text{Eq. 2-3}$$

Fig. 2.4 shows only the loss that occurs due to the leakage inductance in a Flyback converter with an RCD snubber. Not only all of the leakage energy but also some of the output energy is dissipated in the snubber circuit. There are two ways to reduce the loss related to the leakage inductance. First, a good coupling inductor with less leakage inductance is an effective solution. Second, increasing the clamp capacitor voltage can shorten the overlapping time period t_c. Therefore, the loss can be reduced. However, the leakage inductance is always present, and increasing the clamp capacitor voltage increases the switch voltage stress.

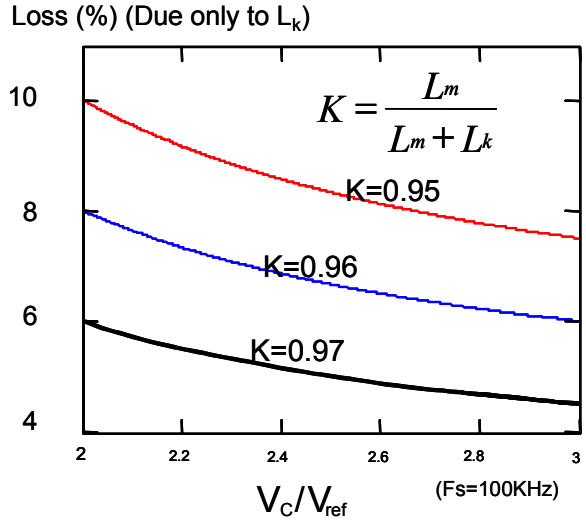


Fig. 2.4. Loss related to the leakage inductance.

The calculated efficiency of a Flyback converter with an RCD snubber for the HID ballast application is about 86%, which is far away from the targeted 90%, as shown in Fig. 2.5(b)(c).

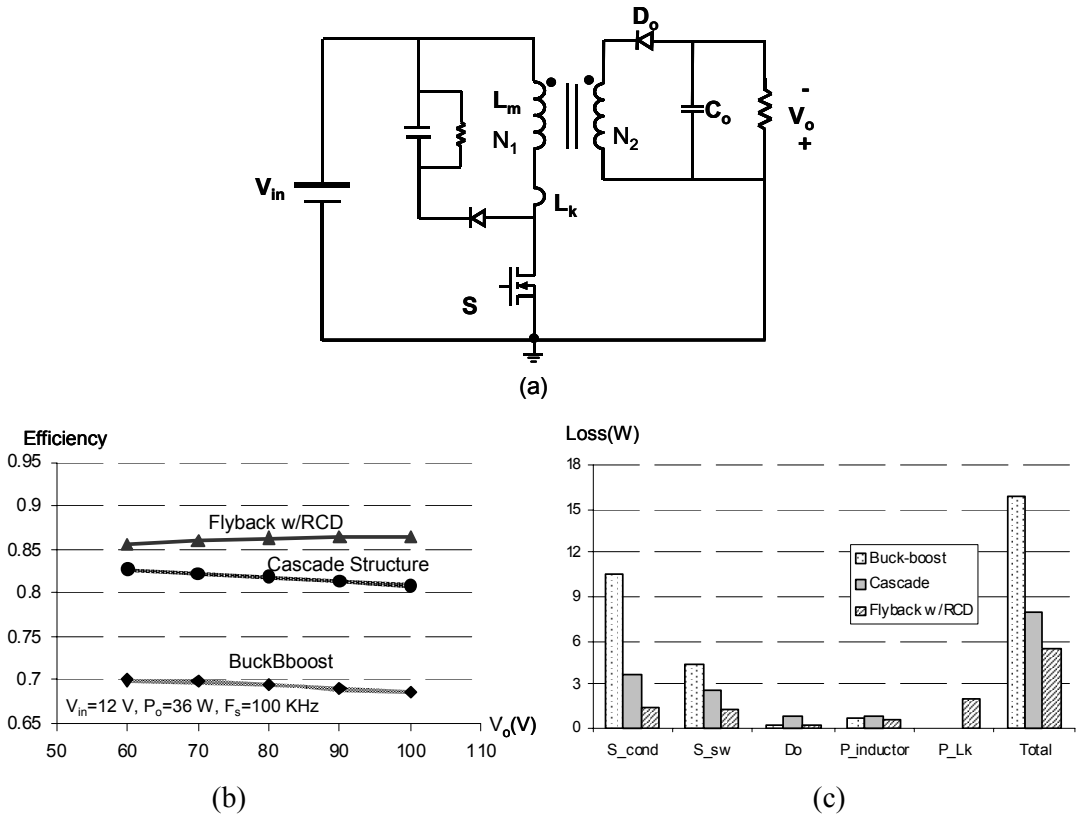


Fig. 2.5. Flyback converter with RCD snubber:
(a) circuit diagram; (b) predicted efficiency; and (c) loss breakdown.

An active-clamp circuit is an effective and efficient method for recycling leakage energy. The active-clamp Flyback converter, as shown in Fig. 2.6(a), can recycle leakage energy with minimal voltage stress to the main switch because the active-clamp scheme resets the leakage inductor during the whole turn-off time period. The drawbacks are that adding the active-clamp switch and its associated floating gate drivers increase the cost, complexity and the losses related to the clamp circuit [B16]. Any accidental overlap of the main and active-clamp switch gate-drive signals could lead to a fatal failure of the circuit. The efficiency improvement is limited

because the high current through the active-clamp switch can induce a high level of conduction loss.

Fig. 2.6(b)(c) shows that a 3% efficiency improvement can be achieved by using the active-clamp scheme instead of the dissipative RCD snubber.

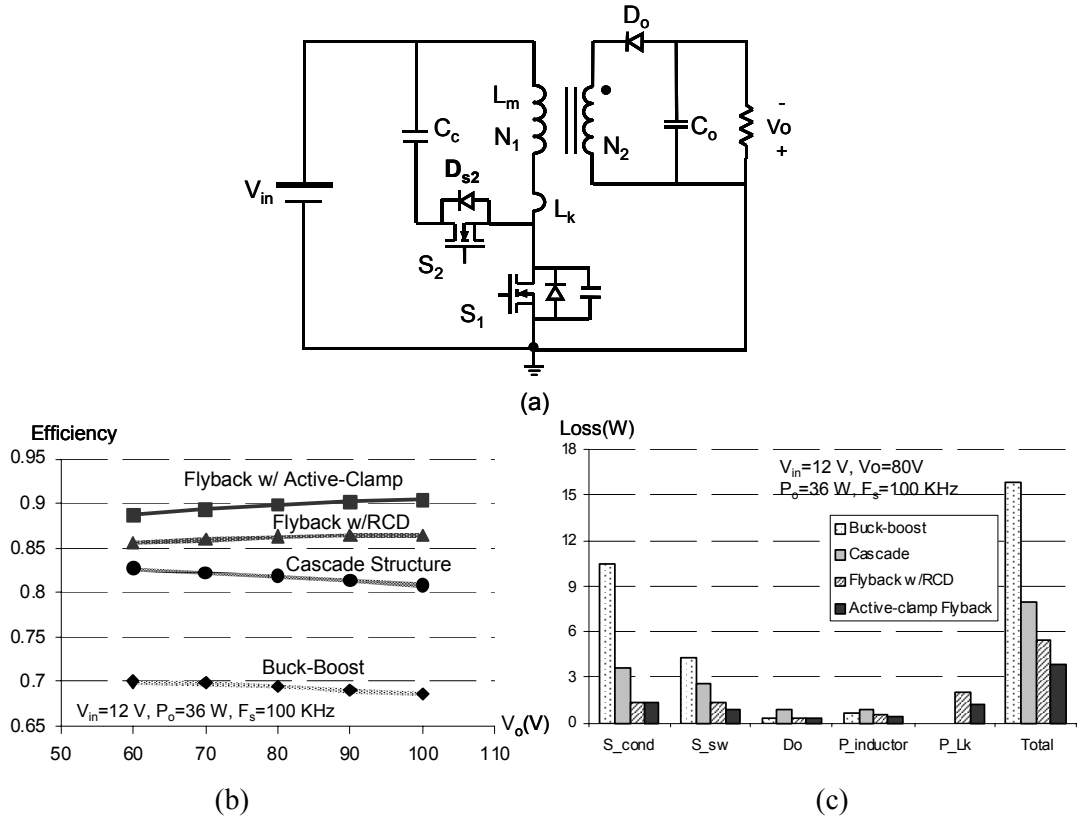


Fig. 2.6. Active-clamp flyback converter:
(a) circuit diagram; (b) predicted efficiency; and (c) loss breakdown.

However, the Flyback converter with either an RCD snubber or an active clamp is adopted in many applications that require isolation. However, the HID step-up converters do not have this requirement. A simple way needs to be found to effectively recycle the leakage energy in a coupled inductor without the isolation requirement.

As discussed above, leakage inductance can cause severe voltage stress and extra loss. An effective leakage-recycling scheme should be used to make coupled-inductor converters simple and efficient. In applications with large step-up conversion ratios, the important question pertaining to the use of coupled-inductor converters is how to effectively recycle the leakage energy with a novel leakage-recycling scheme.

2.3. Advantages and Disadvantages of the Active-Clamp Flyback Converter

The buck-boost converter is not a good candidate for the HID ballast application because of its extreme duty ratios as well as its high conduction and switching losses. Coupled-inductor converters, such as the Flyback and the isolation SEPIC converter, have been used for this application. The voltage gain of a Flyback converter is given by Eq. 2-4:

$$\frac{V_o}{V_{in}} = \frac{d}{1-d} \cdot \frac{N_s}{N_p}, \qquad \text{Eq. 2-4}$$

where V_o is the average value of the output voltage;

V_{in} is the average value of the input voltage;

d is the duty ratio of the converter;

N_p is the number of primary turns for the coupled inductor; and

N_s is the number of secondary turns for the coupled inductor.

Utilizing a coupled inductor can easily achieve high step-up voltage gain without incurring extreme duty ratios. However, the leakage inductor of the coupled inductor not only induces high voltage spikes but also dramatically degrades efficiency. In practical applications, an auxiliary circuit must be used to handle the leakage energy. This auxiliary circuit can either dissipate the leakage energy or recover the leakage energy to the input or output.

An RCD snubber circuit dissipates the leakage energy to reduce the voltage stress of the switch, but the loss related to the leakage inductance is dramatic, as analyzed in Chapter 1. The coupled-inductor converter with RCD clamp cannot achieve decent efficiency as compared to the scheme involving lossless leakage energy recovery.

The active-clamp flyback converter, as shown in Fig. 2.7, recovers the leakage energy and minimizes the voltage stress of the switch. The active-clamp scheme utilizes the entire turn-off time to reset the leakage inductance. Therefore, the voltage stress is minimized. Compared to the Flyback with RCD snubber, the active-clamp Flyback converter can achieve a 3% higher efficiency. The drawbacks of the active-clamp solution are the topology complexity and the high loss related to the clamp circuit. The active-clamp approach requires two switches and two isolated gate drivers. The current through the active-clamp switch is the primary current with large magnitude, which can induce high conduction losses in the active-clamp circuit. The average current of the positive part of current I_{Cc} induces conduction loss in diode D_{s2}. The root-mean-squire (RMS) value of the negative portion of current I_{Cc} induces conduction loss in switch S_2. Although the leakage energy is recycled, the loss in the active-clamp circuit is not small. From this standpoint, a clamp scheme with simple topology and less circulating energy is a better choice than the active-clamp Flyback converter.

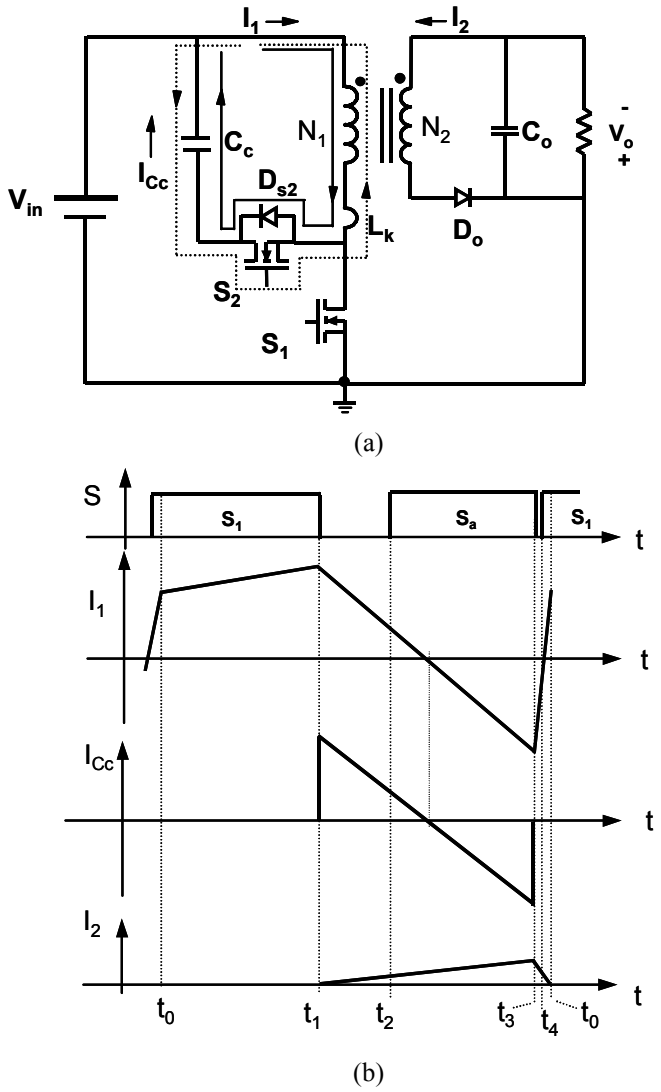


Fig. 2.7. Active-clamp Flyback converter:
(a) topology and (b) key waveforms.

2.4. Clamp-Mode Coupled-Inductor High Step-Up DC-DC Converters

In this section, the transformation of the isolation coupled-inductor converters to the non-isolation version was introduced. The transformation allows the two windings to share the common part of the transformer, while the electrical characteristics of the terminals remain

unchanged. Then, the active-clamp scheme is applied to the non-isolation coupled-inductor converters. The analysis shows that the secondary winding and the output rectifier provide an existing discharge path for the clamp capacitor. Therefore, the switch providing the discharge path of the clamp capacitor could be eliminated. A simple and efficient high step-up DC-DC converter is then proposed for the HID ballast application.

2.4.1. Non-Isolation Coupled-Inductor DC-DC Converters

The coupled inductor is used not to provide isolation but to achieve high voltage gain. The state-of-the-art solution is the Flyback converter, but it does not take advantage of the lack of an isolation requirement. By utilizing non-isolation coupled-inductor converters, the magnetic structure is simplified by using less copper. It will be further demonstrated that the leakage energy recovery can be more efficient with a simple auxiliary circuit.

Fig. 2.8(a) shows a transformer with turns ratio N_1:N_2 (N_1<N_2). It is equivalent to the auto-transformer version, as shown in Fig. 2.8(b).

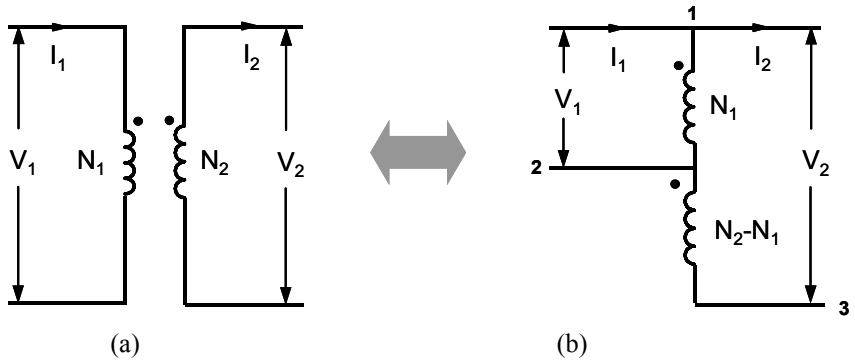


Fig. 2.8. Equivalence of isolation transformer and auto transformer:
(a) isolation transformer and (b) auto transformer.

For a Flyback converter with $N_1<N_2$ for the step-up function, the coupled inductor can be modeled as the combination of a magnetizing inductor and an ideal transformer, as shown in Fig. 2.9(a). Changing the isolation transformer into the non-isolation version by using the rule shown in Fig. 2.8, we can obtain the non-isolation coupled-inductor buck-boost converter, as shown in Fig. 2.9(b).

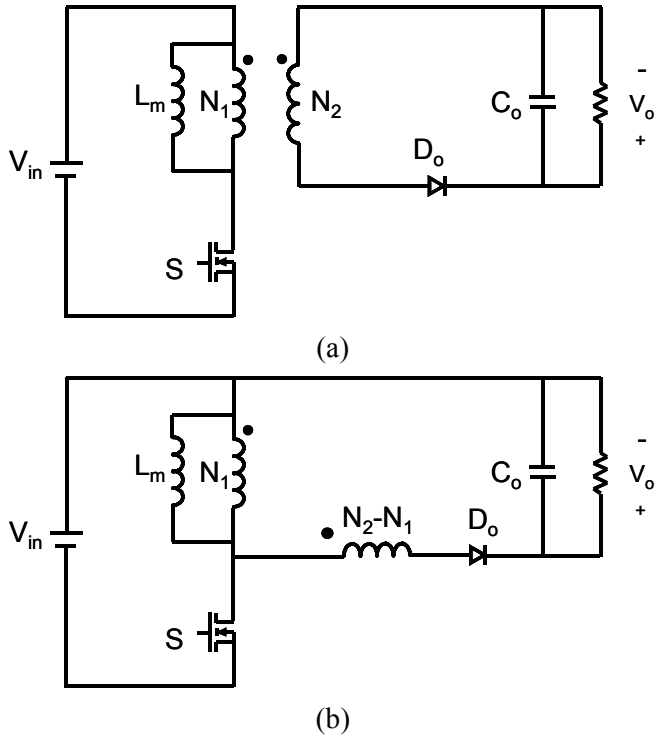


Fig. 2.9. Transformation of Flyback converter to the coupled-inductor converter without isolation : (a) Flyback converter and (b) non-isolation coupled-inductor converter.

The non-isolation version has a turns number that is lower than that of the isolation version. The advantage of this non-isolation version over the Flyback converter could not be justified if both converters had an ideal coupled inductor. However, for practical applications, there must be an auxiliary snubber or clamp circuit. The advantage of the non-isolation version is that the

simple and effective leakage energy recovery scheme can be adopted. Therefore, a cost-effective and high-performance DC-DC converter for the HID ballast can be found.

2.4.2. Proposed Coupled-Inductor High Step-up DC-DC Converters

Similar to the Flyback converter, the leakage energy must be handled properly to reduce the voltage stress of the switch and to improve the efficiency. The active-clamp scheme is used from the performance standpoint. The resulting coupled-inductor buck-boost converter with active-clamp scheme is shown in Fig. 2.10. Compared to the active-clamp Flyback converter, this converter works in a similar way, except that the primary winding current is different when the turns ratio of the two converter has the following relationship:

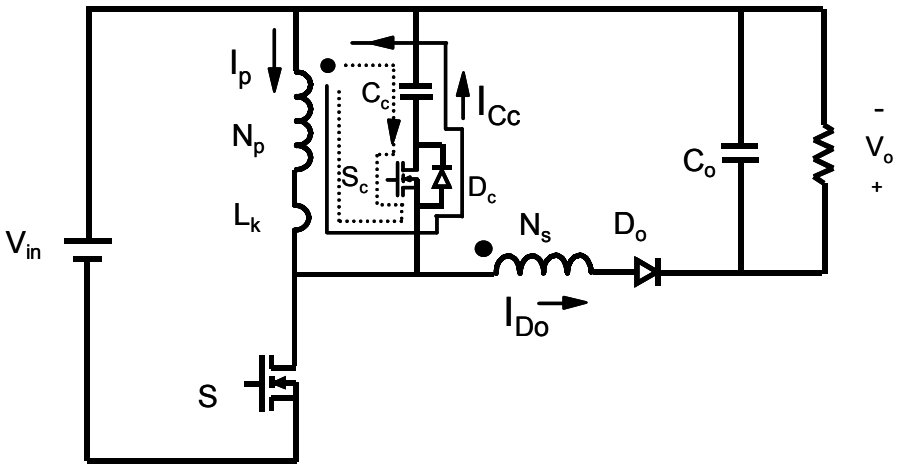
$$N_p = N_1, \quad \text{and} \qquad \text{Eq. 2-5}$$

$$N_s = N_2 - N_1. \qquad \text{Eq. 2-6}$$

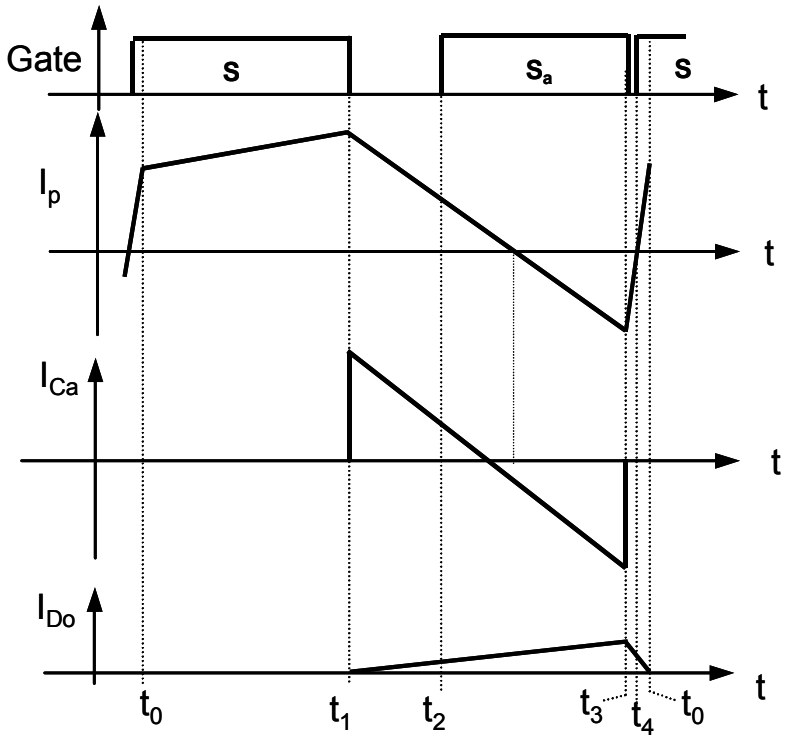
The difference is that the secondary winding current now goes through the primary winding in the reverse direction, which helps to reduce the RMS current of the primary winding. In the non-isolation coupled-inductor buck-boost converter with active-clamp scheme, diode D_a is used to provide a charge path to absorb the leakage energy, while switch S_a is used to provide a discharge path for the clamp capacitor C_a. As can be seen from Fig. 2.10, the switch S_a can be turned on any time after the main switch turns off and before the current through the clamp capacitor reverses its direction.

When N_s is equal to N_p, then the current decrease slope of the primary current is equal to the current increase slope of the secondary current when a ripple-free magnetizing current is assumed. As can be seen from Fig. 2.11(a), the primary current is always positive if the active-clamp switch turns on immediately after the main switch turns off. This means that the discharge current of the clamp capacitor comes from the secondary current, which hints that there is an existing discharge path for the clamp capacitor. The active-clamp diode and switch can be shifted to the charge and discharge branch, as shown in Fig. 2.11(b). This switch shift does not change the circuit operation. Since diode D_o and switch S_a have the same turn-on and turn-off times, switch S_a is redundant and is therefore removed. The resulting proposed circuit is shown in Fig. 2.12.

Fig. 2.12 shows the proposed solution to achieve the function of the active clamp by adding only diode D_c and clamp capacitor C_c, when N_s is equal to N_p. The primary leakage energy charges the clamp capacitor, while the secondary coupled inductor serves as the switch to provide a discharge path for the clamp capacitor. It works the same as the active-clamp version when N_s is equal to N_p. The new solution proposed here is based on a simple principle: The current of winding N_s is used to discharge the clamp capacitor. In other words, the discharge path already exists in the non-isolation coupled-inductor buck-boost converter. In high step-up applications, N_s is much larger than N_p. Further analysis shows that the proposed solution can achieve a function similar to that of the active-clamp scheme, but with much less current circulating in the clamp circuit.



(a)



(b)

Fig. 2.10. Coupled-inductor converter with active-clamp scheme:
(a) topology and (b) key waveforms.

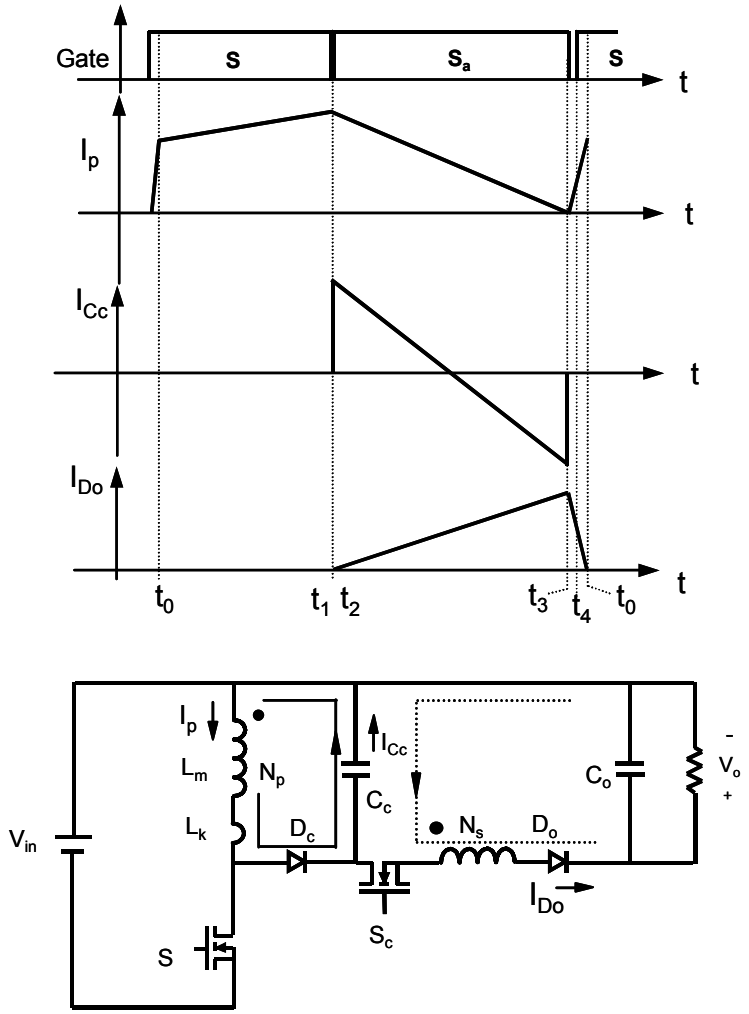


Fig. 2.11. Derivation of the clamp-mode coupled-inductor converters with N_s=N_p.

The new converter requires only one additional clamp capacitor C_c and one diode D_c. The converter can achieve a level of operation comparable to that of the active-clamp scheme. The basic idea for this topology is that the clamp capacitor C_c and the added diode Dc function as the active-clamp charging path, while the induced current in the secondary winding N_s of the coupled inductor is used to discharge the clamp capacitor C_c. Therefore, the secondary winding of the coupled inductor serves the same function as the active-clamp switch, and is different from

the so-called magnetic switch [D13]. The leakage energy is recovered and the switch voltage stress is reduced. Therefore, the performance of the converter is significantly improved.

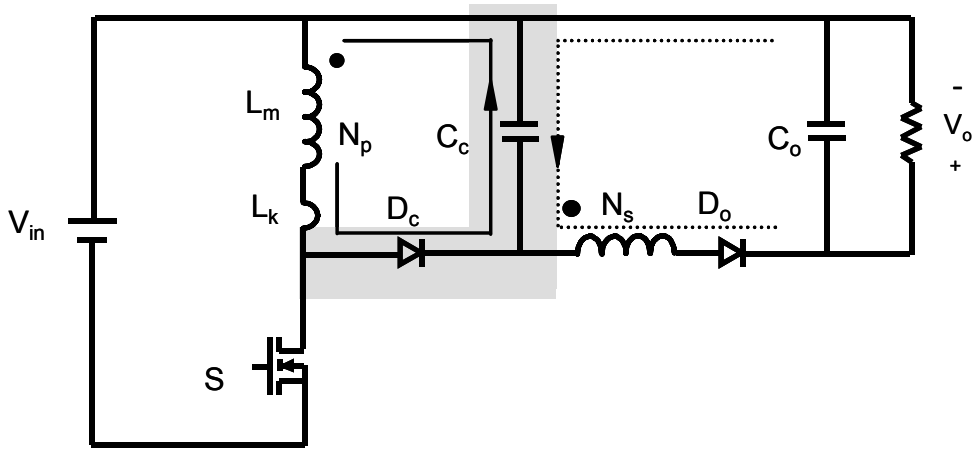


Fig. 2.12. Proposed clamp-mode coupled-inductor buck-boost converter.

2.4.3. Operation Analysis

Fig. 2.13 illustrates the six topological stages in one switching cycle for the proposed clamp-mode coupled-inductor buck-boost converter. The coupled inductor is modeled as a magnetizing inductor Lm, an ideal transformer with a turns ratio of N_p:N_s, and a leakage inductor L_k. The converter is redrawn to facilitate the comparison with the active-clamp Flyback converter. Fig. 2.14 shows the key waveforms of the operation modes corresponding to the different topological stages shown in Fig. 2.13. The six operation modes are briefly described as follows.

[t_0, t_1]: Switch S is on, and the output rectifier D_o is reverse-biased. Both the magnetizing inductor and the leakage inductor are linearly charged by the input voltage source V_{in}.

[t_1, t_2]: Switch S turns off at t_1. The parasitic capacitor of the switch is charged by the magnetizing current in an approximately linear way.

[t_2, t_3]: At t_2, the parasitic capacitor of switch S is charged to the voltage of $V_{in}+V_{Cc}$. Clamp diode D_c conducts. Almost all of the magnetizing current begins to charge clamp capacitor C_c.

[t_3, t_4]: At t_3, V_{Cc} is charged to the point that output diode D_o is forward-biased. The reflected voltage from the secondary winding N_s of the coupled inductor clamps the primary winding N_p. Leakage inductor L_k and clamp capacitor C_c begin to resonate.

[t_4, t_5]: At t_4, the resonant current reaches zero. All of the magnetizing current is reflected to the secondary winding N_s from the primary winding N_p. The clamp capacitor is then discharged by the output rectifier current I_{Do} (I_{Lm}/N).

[t_5, t_0]: Switch S turns on at t_5. The leakage inductor L_k is quickly charged by the sum of input voltage V_{in} and the reflected voltage $(V_o-V_c)/N$ until the leakage inductor current I_{Lk} is equal to the magnetizing current I_{Lm}. The output rectifier D_o is reverse-biased. Then, the next switching cycle begins.

It is should be pointed out that the time periods [t_1, t_2] and [t_2, t_3] are much shorter than those shown in Fig. 2.14, which were enlarged in order to clearly show the waveform variations.

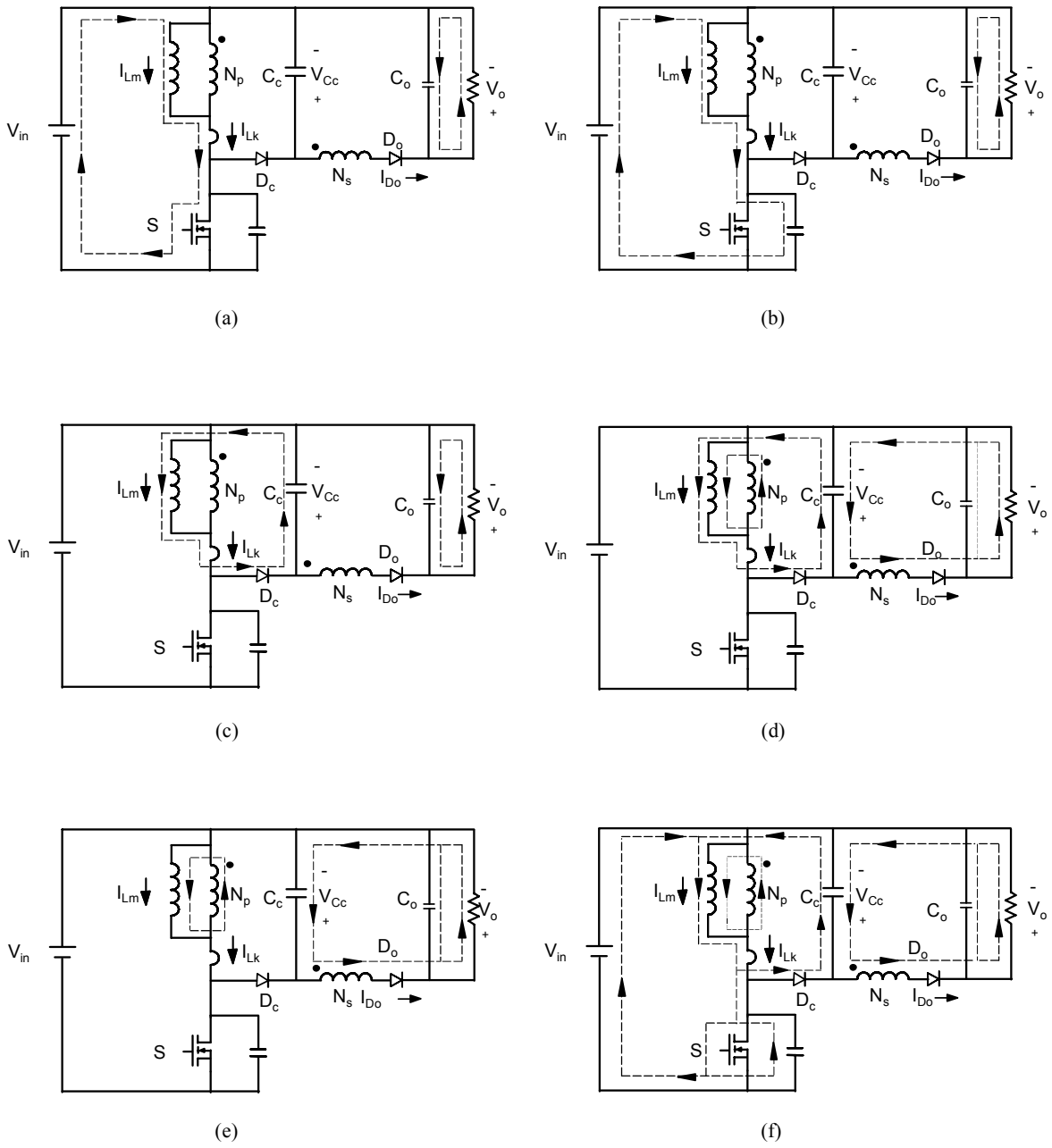


Fig. 2.13. Operation modes of the clamp-mode coupled-inductor buck-boost converter: (a) [t_0, t_1], (b) [t_1, t_2], (c) [t_2, t_3], (d) [t_3, t_4], (e) [t_4, t_5] and (f) [t_5, t_0].

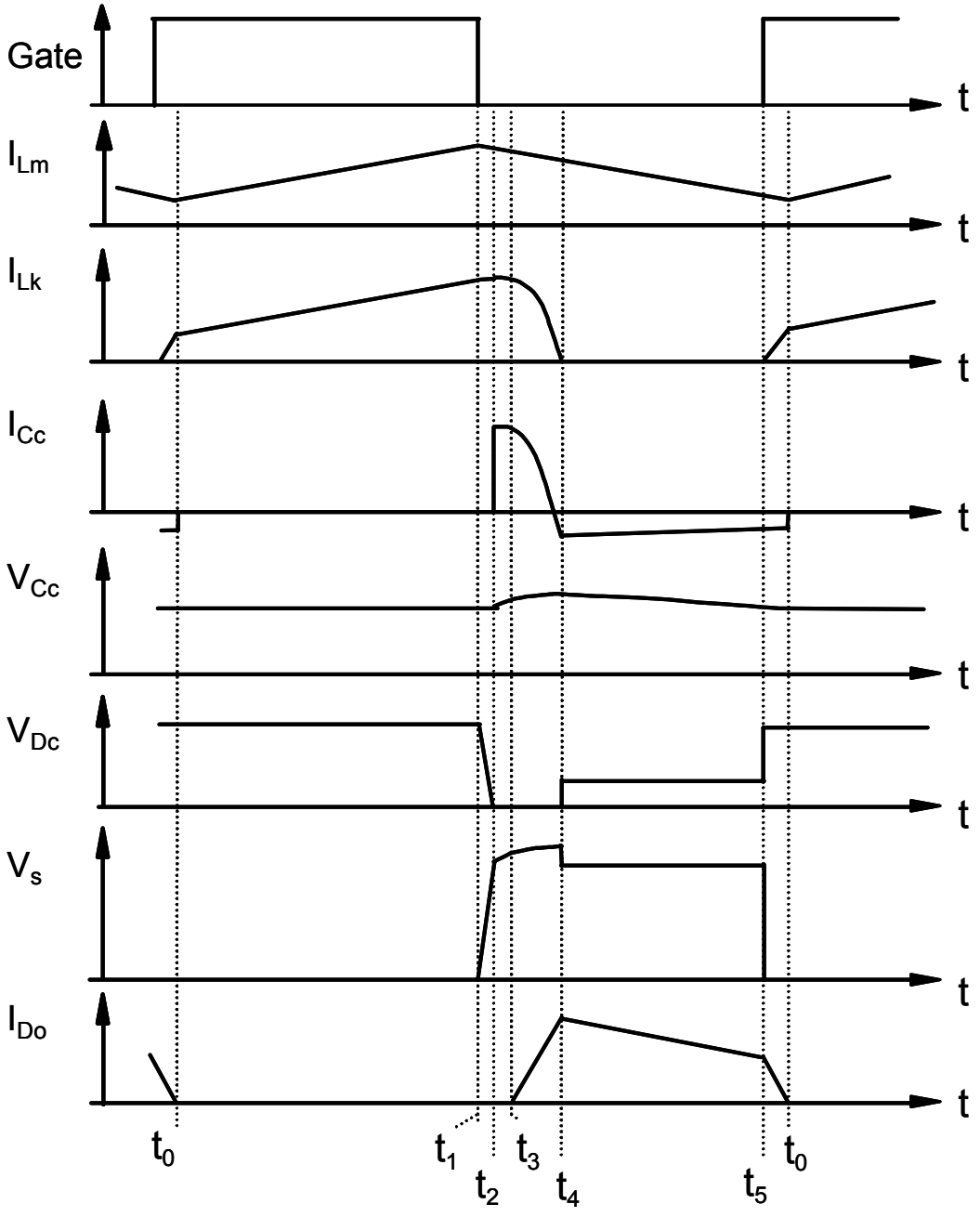


Fig. 2.14. Key waveforms of the clamp-mode coupled-inductor buck-boost converter.

As can be seen from the analysis, the leakage energy stored in L_k is recovered by the clamp capacitor such that the voltage of the switch is clamped. The clamp capacitor is discharged by the output rectifier current I_{Do}, which is equal to the reflected secondary current from the primary transformer winding. The primary transformer current equals the difference between the magnetizing current and the leakage inductor current. Fig. 2.15 shows the relationship between the clamp capacitor charge and discharge currents by assuming that the magnetizing current is ripple-free. The clamp capacitor needs to maintain a balance between charge and discharge.

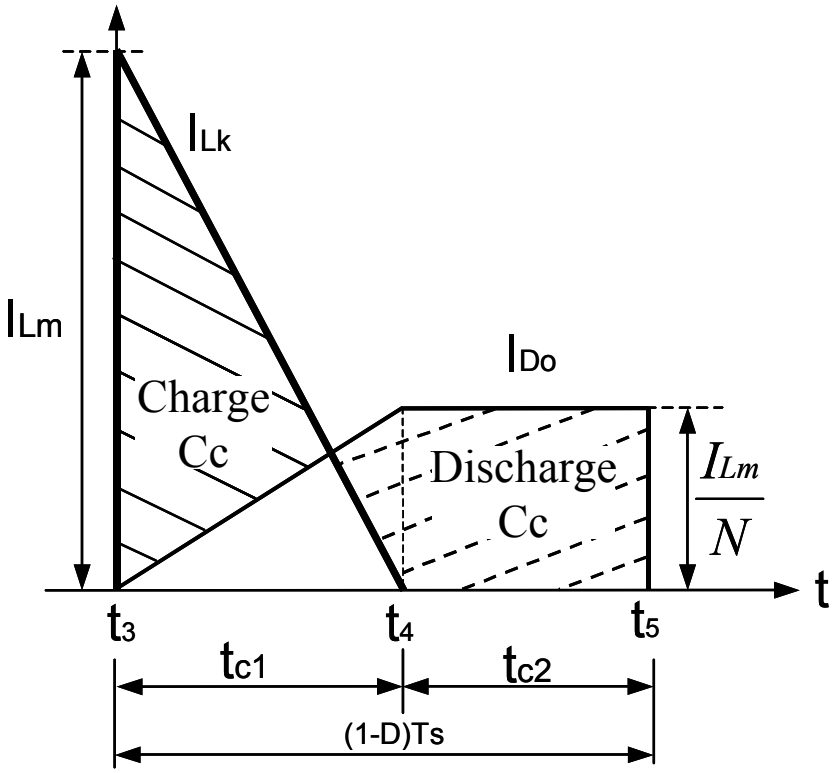


Fig. 2.15. Current relationship.

By making the charge area equal to the discharge area in Fig. 2.15, the following relationship is found:

$$t_{c1} = \frac{2}{N+1} \cdot (1-D) \cdot T_s \,, \qquad \text{Eq. 2-7}$$

where N is the turns ratio N_s / N_p.

To make the following derivation simple, define K as:

$$K = \frac{L_m}{L_m + L_k} \,. \qquad \text{Eq. 2-8}$$

By applying the volt-second balance of the magnetizing inductor and the leakage inductor, the voltage gain and the clamp capacitor voltage of the converter are given by Eq. 2-9 and Eq. 2-10, respectively. The time needed for the leakage inductor to reset is represented by t_{c1}.

$$\frac{V_o}{V_i} = \frac{d}{1-d} \cdot (N+1) \cdot \frac{(1+K)}{2} \qquad \text{Eq. 2-9}$$

$$V_c = \frac{d}{1-d} \cdot V_i \cdot \frac{(1+K)+(1-K) \cdot N}{2} \qquad \text{Eq. 2-10}$$

The voltage of the output rectifier is given by Eq. 2-11:

$$V_{Do} = (\frac{d}{1-d} \cdot N \cdot K + N - 1) \cdot V_i \,. \qquad \text{Eq. 2-11}$$

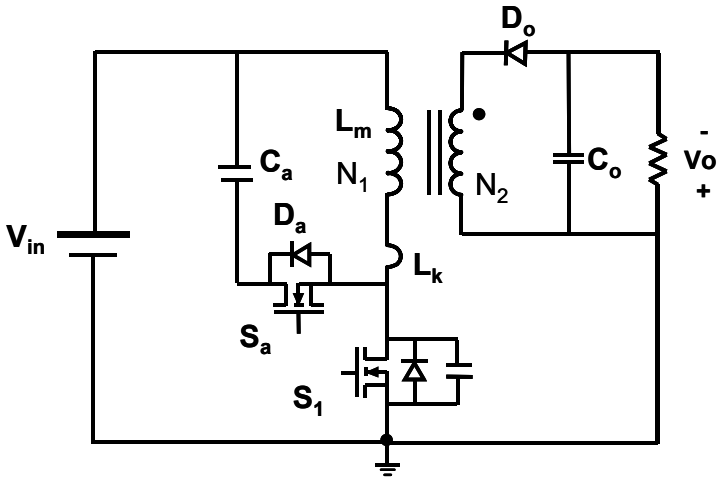
The proposed converter is able to provide a wide range of step-up voltage gains using various turns ratios for the coupled inductor. High step-up voltage gain is achieved without requiring an extreme duty ratio.

2.4.4. Current Stress Comparison with the Active-Clamp Counterpart

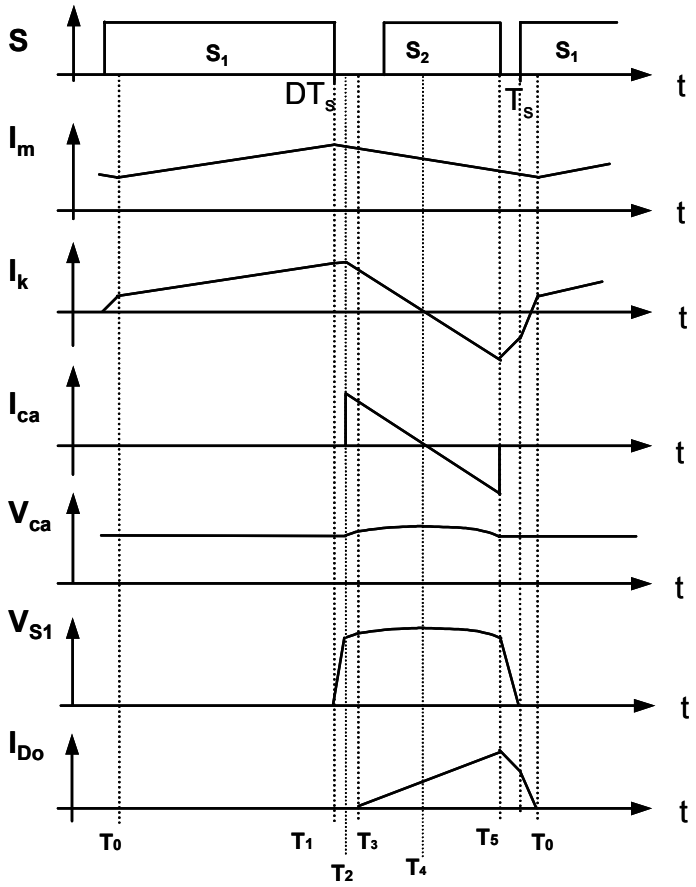
On one hand, the active-clamp scheme utilizes the entire off-time of the main switch to reset the leakage inductor, as shown in Fig. 2.16. Therefore, the average voltage of the clamp capacitor is minimized. The average voltage V_a of the clamp capacitor C_a is given as follows.

$$V_{Ca} = \frac{d}{1-d} \cdot V_i . \qquad \text{Eq. 2-12}$$

On the other hand, there is a large circulating current going through either the active-clamp switch body diode or the active-clamp switch. The reason is that N_p acts as a voltage source reflected from N_s after D_o conducts. The leakage inductor L_k resonates with the clamp capacitor C_a. The difference between the proposed converter and its active-clamp counterpart is that the clamp capacitor is linearly discharged by the secondary reflected magnetizing current (I_{Lm}/N) during [t_4, t_5], as shown in Fig. 2.15. The secondary reflected magnetizing current is much smaller than the primary magnetizing current because N>>1. The discharge period [t_4, t_5] in the proposed converter is longer than half of the [t_3, t_5] period in the active-clamp converter. A longer [t_4, t_5] period makes the charge period [t_3, t_4] shorter in the proposed converter than it is in the active-clamp scheme. Therefore, the proposed converter has less energy circulating in the additional clamp circuit.



(a)



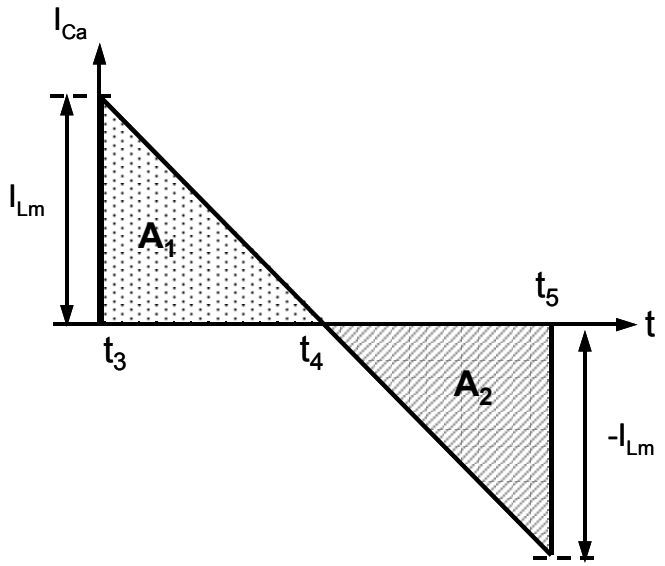
(b)

Fig. 2.16. Active-clamp flyback converter:
(a) circuit diagram and (b) key waveforms.

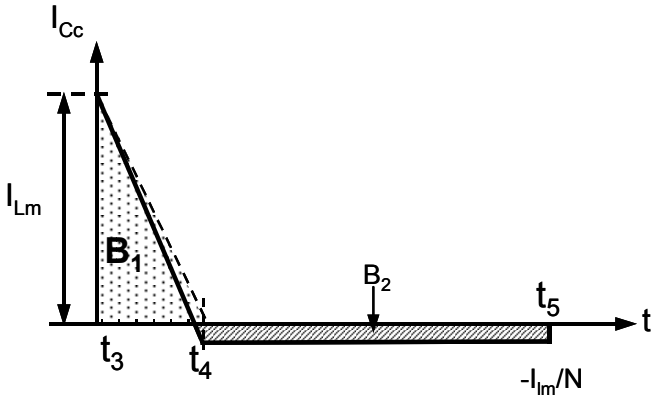
Fig. 2.17 compares the proposed clamp-mode coupled-inductor buck-boost converter shown in Fig. 2.12 with the corresponding active-clamp scheme shown in Fig. 2.16 after the main switch turns off. The leakage inductor begins to charge the clamp capacitor in both the proposed converter and in its active-clamp counterpart, with the initial current acting as the magnetizing current. For the active-clamp converter, the charge current, represented by the dotted area A1 in Fig. 2.17(a), goes through the clamp switch D_a. This current is independent of the turns ratio. But for the proposed circuit, the current going through the clamp diode D_c, represented by the dotted area B1 in Fig. 2.17(b), is much smaller than it is in the active-clamp converter. Unlike the active-clamp circuit, the current going through the clamp capacitor in the proposed circuit depends on the turns ratio: The larger the turns ratio, the smaller the current. Another advantage of the proposed circuit can be observed after the charge current decreases to zero. In the active-clamp converter, the reversed discharge current goes through the active-clamp switch Sa, which is a high primary-side current when the input voltage is low, as shown in Fig. 2.17(a). This part of the circulating energy results in a high conduction loss in the active-clamp switch. In the proposed circuit shown in Fig. 2.17(b), the current goes directly to the output filter through the output rectifier D_o. The loss related to the clamp switch is zero. Table 2.1 summarizes these comparisons.

Table 2.1. Loss comparison.

	Reason for Loss in D_a or D_c	Reason for Loss in S_a
Active-Clamp Converter	Average of A_1	RMS of A_2
Proposed Converter	Average of B_1	N/A (=0)
Comparison	$A_1 > B_1$	$A_2 >> 0$



(a)



(b)

Fig. 2.17. Comparison of circulating energy:
(a) active-clamp counterpart and (b) clamp-mode buck-boost converter.

The benefit of this clamp scheme is quantified. Fig. 2.18 illustrates the loss breakdown [A4] comparison of the proposed converter and the active-clamp converter. The operation conditions are: V_{in}=12V, V_o=90V, P_o=36W, and F_s= 100KHz. As can be seen, the active-clamp Flyback

converter has less switching loss due to its zero-voltage-switching (ZVS) turn-on. But the high primary current can result in large conduction losses if the active-clamp switch is used. Although the clamp-mode coupled-inductor converters have higher switching losses, the loss in the clamp switch is much less. Therefore, the efficiency is higher in the clamp-mode coupled-inductor converters than in the active-clamp Flyback converters.

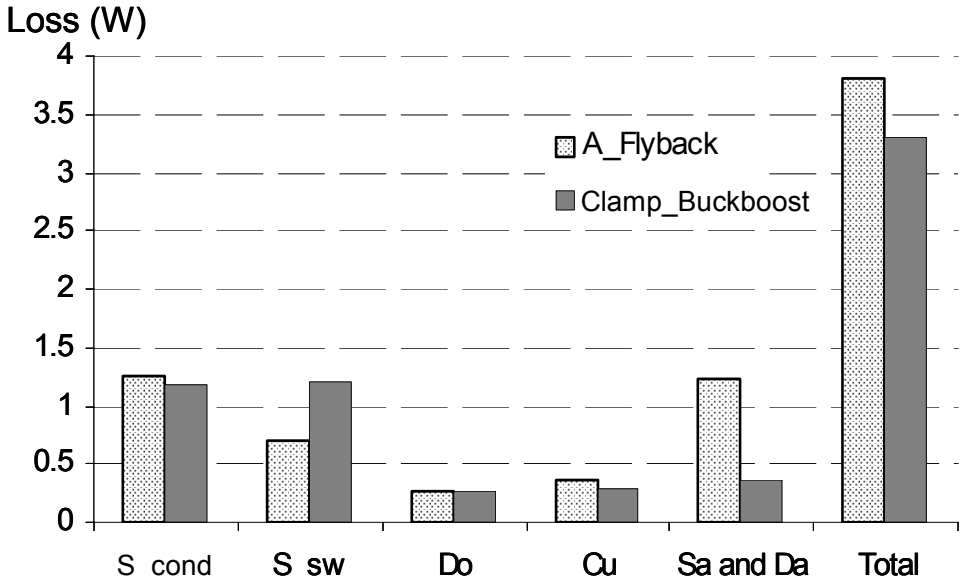


Fig. 2.18. Loss breakdown.

2.4.5. Voltage Stress Comparison with the Active-Clamp Counterpart

The proposed converter has much less clamp circuit-related loss. The reason is that the clamp capacitor voltage is higher than it is in the active-clamp solution. The vertical axis in Fig. 2.19 shows the clamp capacitor voltage of the proposed converter, normalized to the clamp capacitor voltage of its active-clamp counterpart. The difference between the clamp capacitor voltage and

the primary winding voltage resets the leakage inductor. The proposed solution utilizes part of the turn-off time given by Eq. 2-7 to reset the leakage inductance. Therefore, the clamp capacitor voltage is higher than in the active-clamp scheme. Fortunately, the leakage inductor is a small inductor, so the extra voltage needed to reset this small inductor does not need to be high. As can be seen from Fig. 2.19, the voltage stress increase is less than 5% when the coefficient of coupled effect is around 0.98. In fact, the extra voltage stress in the proposed converter does not have to change the device voltage rating as it does in the active-clamp converter.

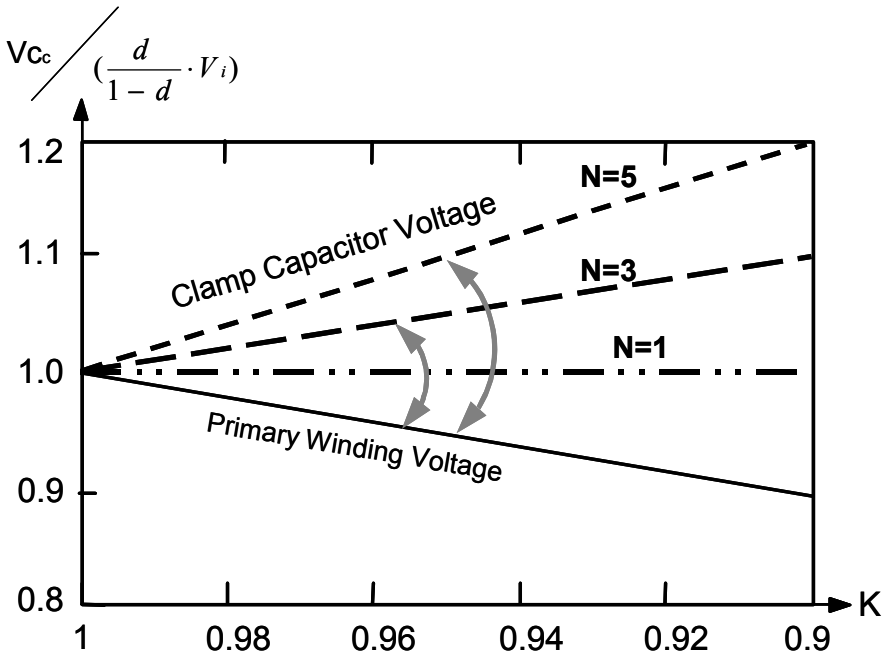


Fig. 2.19. Normalized clamp capacitor voltage.

2.5. Design Guidelines

The key design step is to determine the turns ratio that allows a low-voltage-rated device to have a sufficient safety margin, and that enables the converter to operate without an extreme duty ratio. The key design equation to calculate the turns ratio is as follows:

$$N = \frac{V_{o\_\max}}{V_{DS} - V_{i\_\min}} - 1. \qquad \text{Eq. 2-13}$$

Fig. 2.20 is the design graph targeted at DC-DC front-end converters for HID ballasts with 9-16V input voltage and 60-100V output voltage (start-up voltage 400V). The horizontal axis and the left vertical axis of Fig. 2.20 show the relationship between switch voltage stress and input voltage using different turns ratios. In the same graph, the relationship between duty ratio and input voltage under different turns ratios is shown on the horizontal axis and the right vertical axis. After the turns ratio is defined, the corresponding duty ratio can be found from Fig. 2.20. The voltage rating of the output rectifier and the clamp capacitor can be easily calculated. The design must make a tradeoff between the switch and rectifier voltage stresses. The optimal design can be achieved by carrying out the process shown in Fig. 2.21. The loss analysis mechanism is based on the switching-cycle performance [A4].

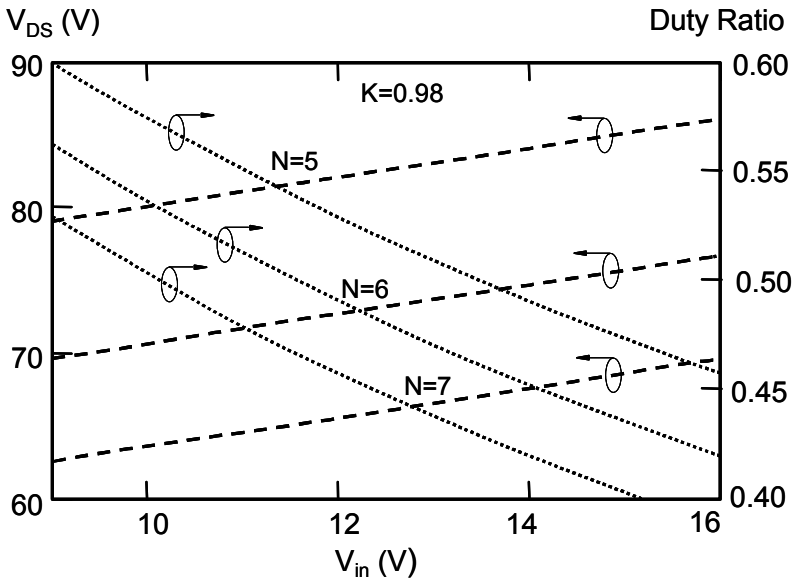


Fig. 2.20. Design curves.

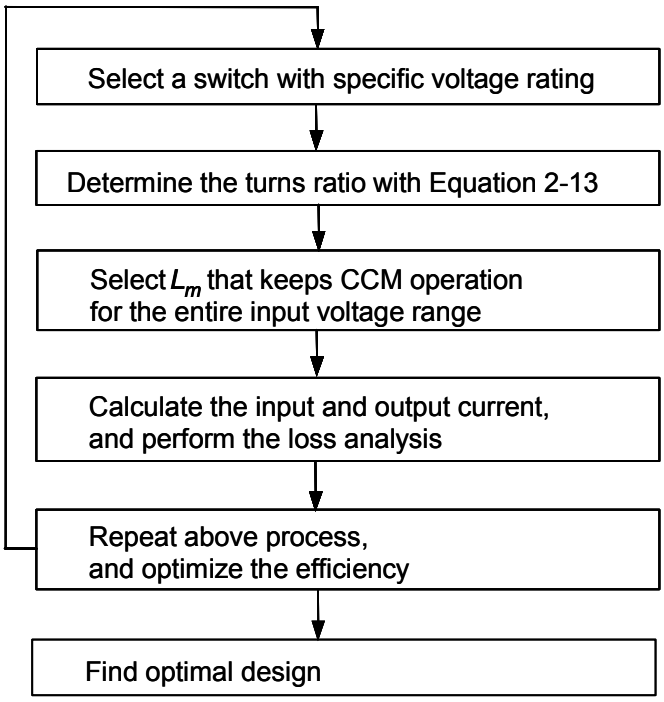


Fig. 2.21. Optimization procedure.

2.6. Experimental Verification

As shown in Fig. 2.22, a prototype converter targeted at the HID lamp ballast application is built. Because the converter needs to generate 400V open-circuit voltage to ignite the HID lamp, the voltage rating of the selected active switch is 100V. The maximum voltage stress is designed to be 70V when the 400V open-circuit voltage is generated. The prototype has the following parameters:

N_1=14 T, N_2=82 T, and C_c=1.36 μF;

S is IRF1310, D_o is MUR860, and D_c is 3A, 100V Schottky diode.

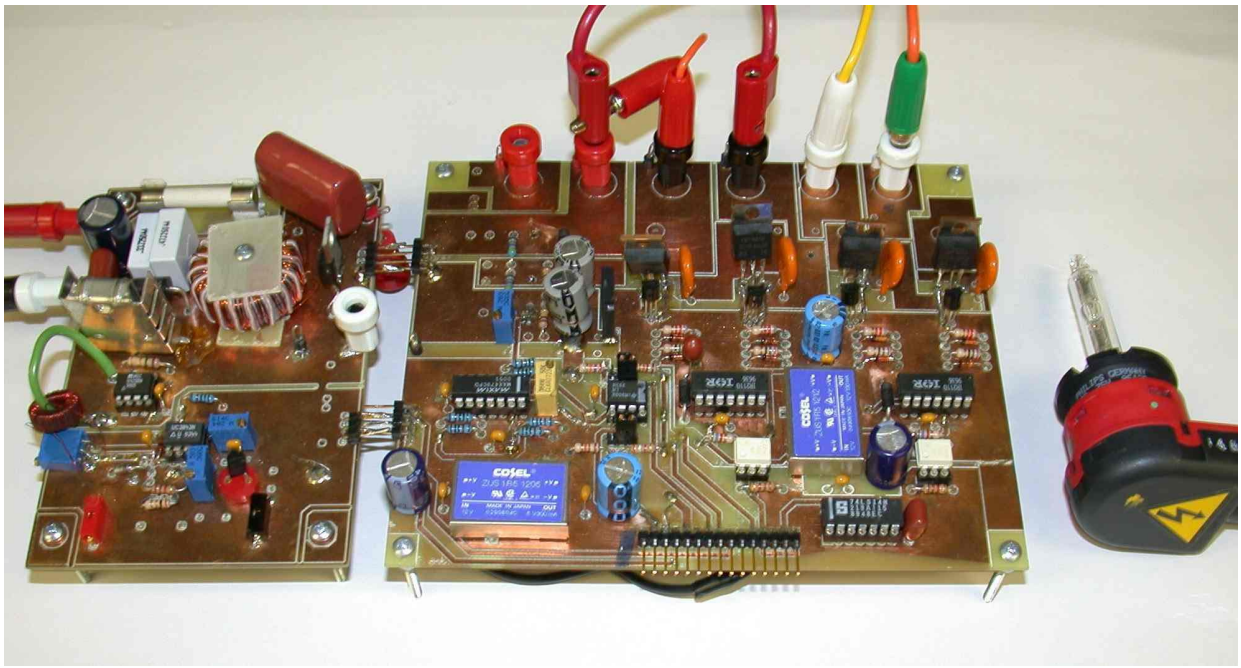


Fig. 2.22. Prototype of the HID ballast.

Fig. 2.23 shows the experimental waveforms of the proposed circuit. The waveforms agree with the analysis, and the voltage of the switch is effectively clamped.

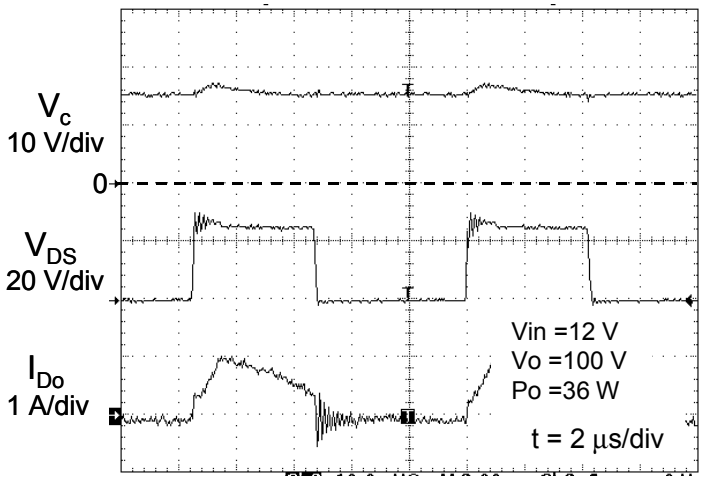


Fig. 2.23. Experimental waveforms of the DC-DC converter for use in HID ballasts.

Fig. 2.24 shows that the voltage stress is about 70 V when the 400V startup output voltage is generated. The 100V MOSFET has sufficient safety margins. A 100V-voltage-rating MOSFET has much lower $R_{DS\text{-}on}$ than does a 500V MOSFET.

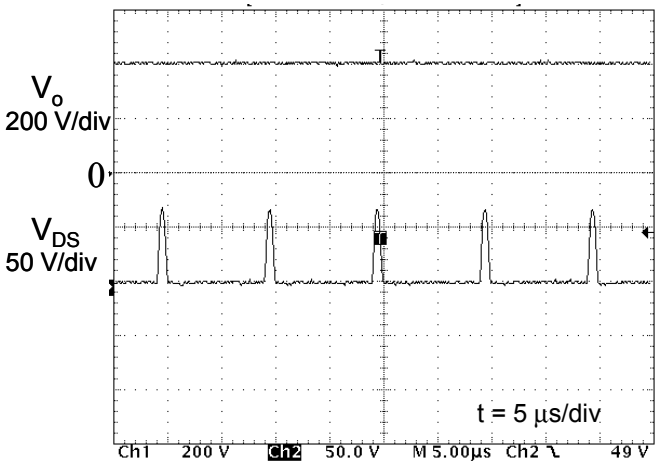


Fig. 2.24. Experimental waveforms when generating 400V open-circuit output voltage.

By adopting the analysis approach based on the detailed dynamic switching performance [A4], the loss analysis is conducted for three different step-up converters; these results are given in Fig. 2.25. For the 36W DC-DC front-end converter of the HID ballast, the proposed clamp-mode coupled-inductor buck-boost converter has higher efficiency than does the active-clamp Flyback converter. The primary magnetizing current of the DC-DC converters for HID lamp ballasts in automobiles is fairly high because of the low-input battery voltage. When the clamp capacitor and the leakage inductor resonate, the high primary current through the active-clamp switch will result in high losses in that switch. Therefore, the proposed converter has an even greater efficiency improvement than is achieved by the active-clamp Flyback. Furthermore, the proposed converter is more cost-effective and more reliable than the active-clamp Flyback converter for those applications not requiring isolation. The experimental results are also shown by the solid line in Fig. 2.25. The theoretical and measured efficiency are closely matched.

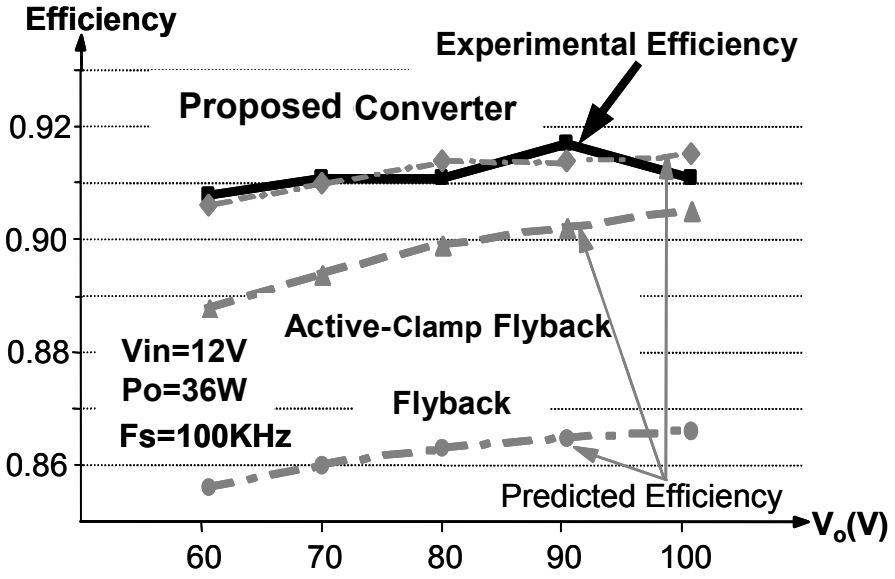


Fig. 2.25. Predicted and measured efficiency.

2.7. Generalized Concept

The buck-boost is not a good candidate for high step-up applications. The non-isolation coupled-inductor buck-boost converter can achieve high step-up voltage gain without extreme duty ratio. A three-terminal coupled-inductor switching cell can be identified. Since the buck and boost converters have the same three-terminal cell as is used in the buck-boost converter, the switching cell in the coupled-inductor buck-boost converter can also extend to buck and boost converters. Step-up and step-down converters without extreme duty ratios are unified. In practical applications, the leakage energy must be properly handled. The proposed clamp scheme can be extended to other high step-up applications.

2.7.1 Three-Terminal Cell of Coupled-Inductor Converters

Buck, boost and buck-boost converters have a three-terminal switching cell [B13] as shown in Fig. 2.26(a). These topologies encounter an extreme duty ratio for high step-up or -down power conversions. The non-isolation coupled-inductor converter can achieve a high conversion ratio without incurring an extreme duty cycle. In that converter, a three-terminal cell in the step-up coupled-inductor step-up power conversion can be identified, as shown in Fig. 2.26(b).

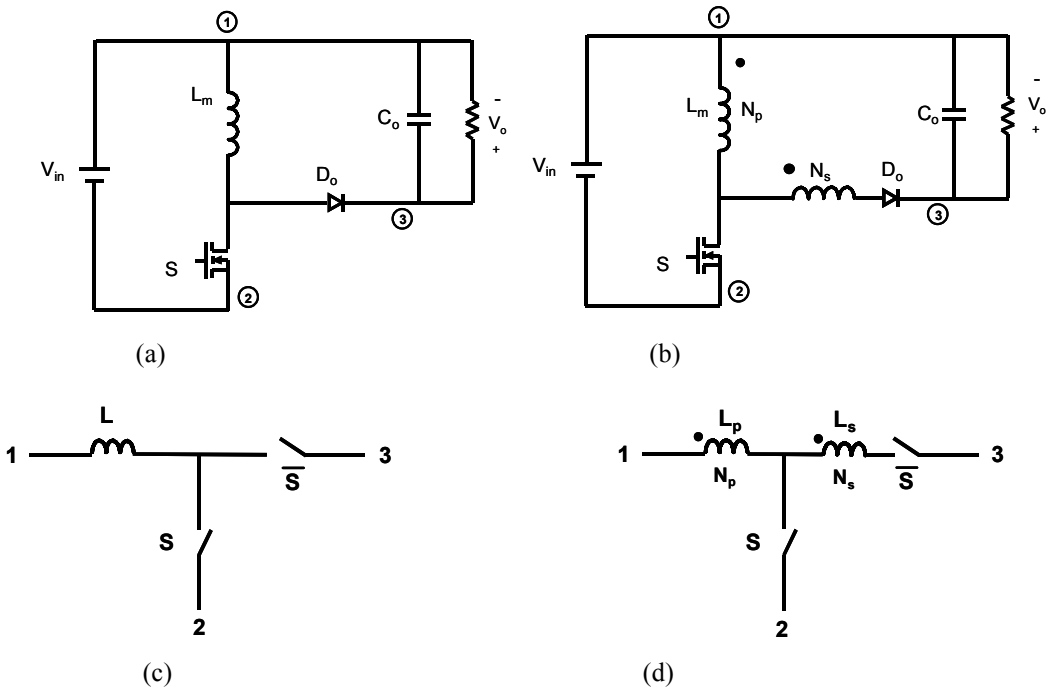


Fig. 2.26. Three-terminal cell and coupled-inductor switching cell.

As discussed in other work [B13], the cell has different connections to the input voltage source and output sink, as shown in Fig. 2.27. There are six possible connections, as listed in Table 2.2.

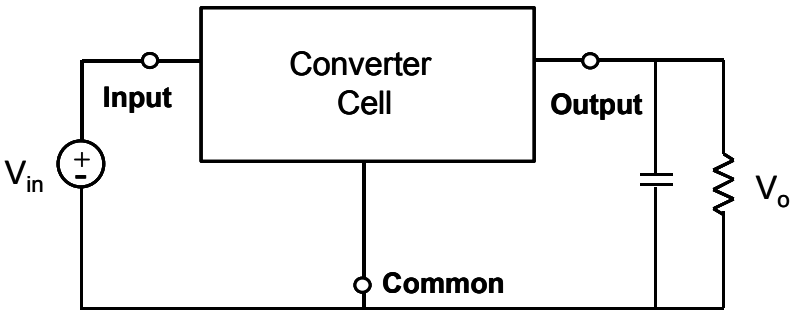
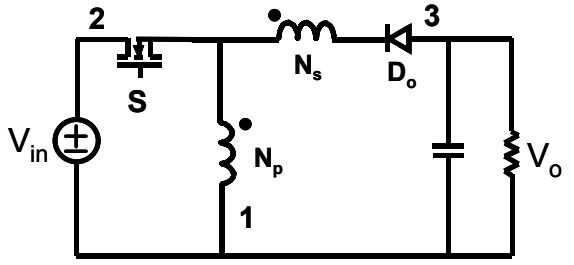


Fig. 2.27. Converter cell.

Table 2.2. Connection of the converter cell to the input and output.

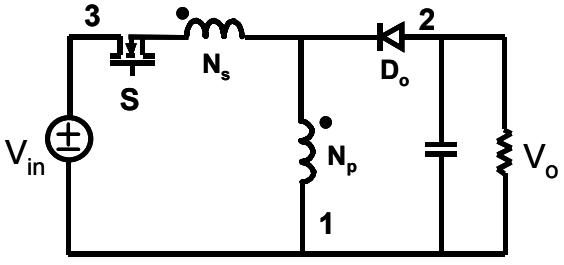
	A	B	C	D	E	F
Common	1	1	2	2	3	3
Input	2	3	1	3	1	2
Output	3	2	3	1	2	1

The six converters are shown in Fig. 2.28. The voltage gains of the converters are also given. The converters shown in Fig. 2.28(a) and (b) are the buck-boost and the boost versions of coupled-inductor converters, which can achieve high step-up voltage gain with a proper turns ratio.



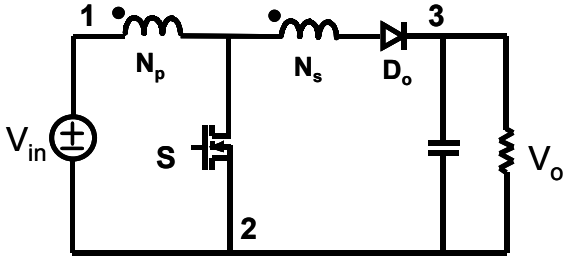
$$M = \frac{N_s + N_p}{N_p} \cdot \frac{d}{1-d}$$

(a) High step-up buck-boost converter



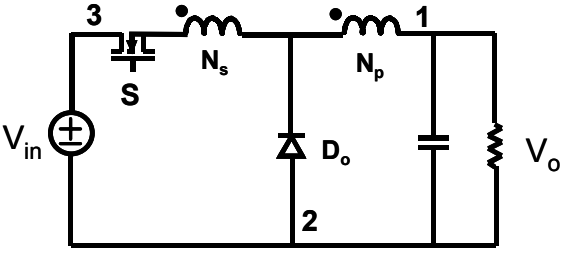
$$M = \frac{N_p}{N_p + N_s} \cdot \frac{d}{1-d}$$

(b) High step-down buck-boost converter



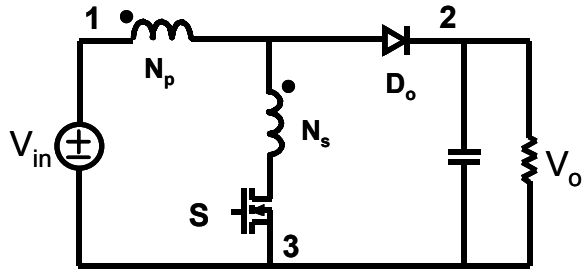
$$M = \frac{N_s}{N_p} \cdot \frac{d}{1-d} + \frac{1}{1-d}$$

(c) High step-up boost converter



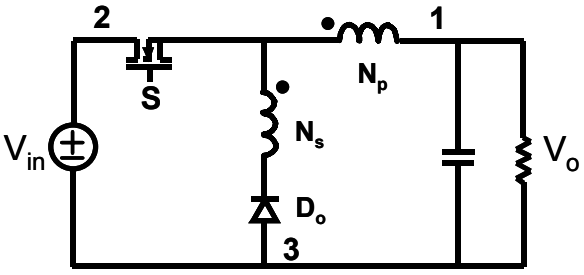
$$M = \frac{N_p}{N_p + N_s - d \cdot N_s} \cdot d$$

(d) High step-down buck converter



$$M = \frac{1}{1-d} - \frac{N_s}{N_s + N_p} \cdot \frac{d}{1-d}$$

(e) Coupled-inductor boost-type converter



$$M = \frac{N_s + N_p}{d \cdot N_s + N_p} \cdot d$$

(f) Coupled-inductor buck-type converter

Fig. 2.28. Six topologies with coupled-inductor switching cell.

2.7.2 Schemes for Leakage Energy Recovery

The leakage inductance not only degrades the efficiency but also increases the switch voltage stress. To handle the leakage energy, either a dissipative snubber or a lossless clamp circuit could be used. The dissipative snubber results in loower efficiency. The active-clamp scheme can minimize the switch voltage stress and improve the efficiency, but with the drawbacks of increased circuit complexity and the loss in the clamp circuit. A novel clamp scheme is proposed for the high step-up DC-DC converters, as shown in Fig. 2.29. This clamp scheme operates much the same way as the active-clamp scheme, but the topology is far simpler and the loss in the clamp circuits is significantly reduced.

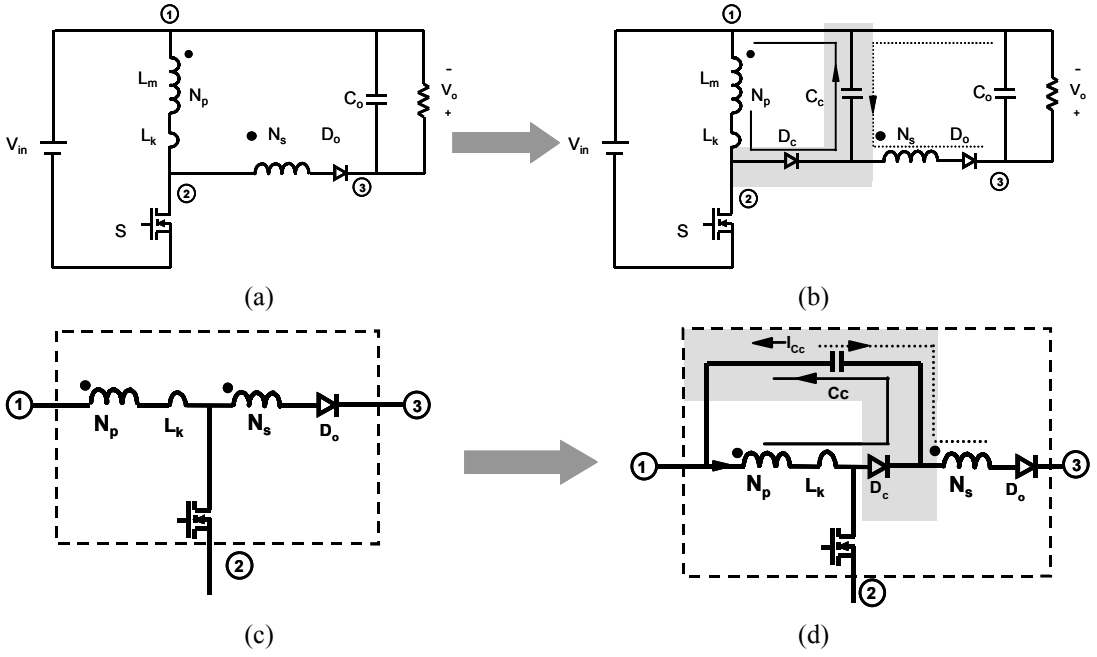


Fig. 2.29. Leakage handling for the step-up converters:
(a) non-ideal coupled-inductor converter; (b) clamp-mode coupled-inductor converter;
(c) switching cell of the converter in (a) and (d) switching cell of the converter in (b).

Both the coupled-inductor buck-boost and the boost versions shown in Fig. 2.29 (a) and (c) can achieve high step-up voltage gains. Applying the proposed leakage energy-recycling scheme

and the capacitor-shifting rule leads to other new topologies, as shown in Fig. 2.31. The leakage energy is efficiently recycled by the added diode and capacitor, and is then discharged directly to the output by the secondary coupled winding. Compared to the active-clamp schemes, the proposed solutions use only one active switch to achieve the same clamp function, while dramatically reducing losses related to the clamp circuit.

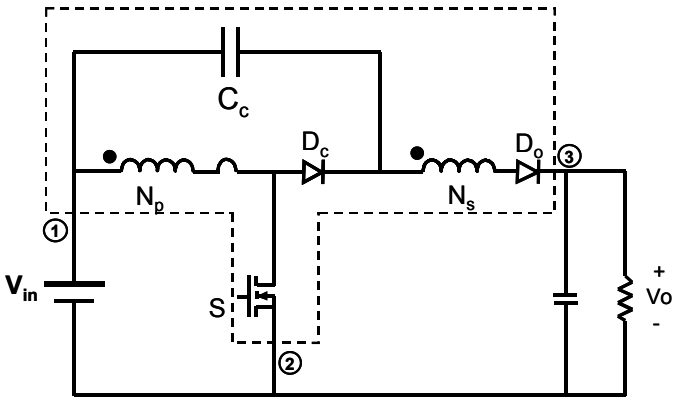


Fig. 2.30. The cell can be applied to the high step-up boost converter.

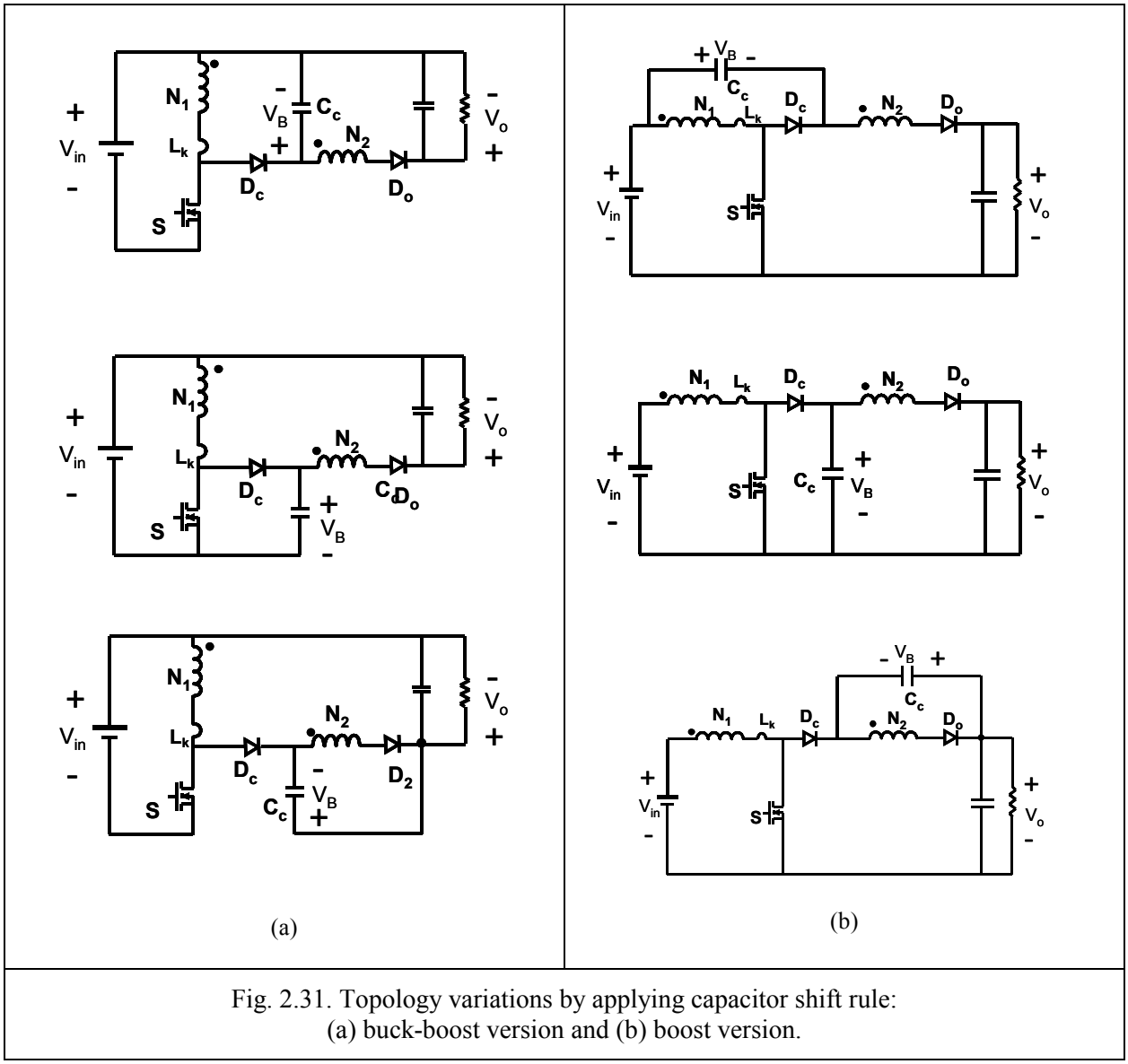


Fig. 2.31. Topology variations by applying capacitor shift rule:
(a) buck-boost version and (b) boost version.

Fig. 2.32 and Fig.2.33 compare the buck-boost and boost versions of high step-up DC-DC converters. As stated in the capacitor-shifting rule, only the clamp capacitor voltage and the current through the input or the output voltage source will change. Thus, a topology with the minimum stress can be identified. In the next section, the application of the derived converters will be demonstrated

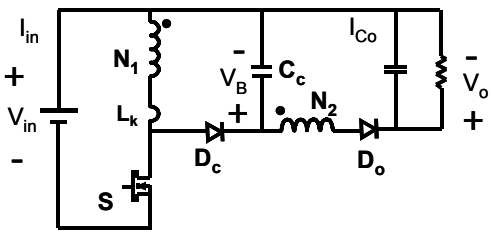
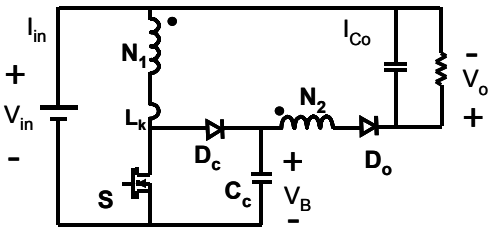
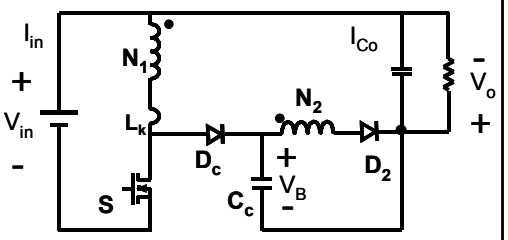
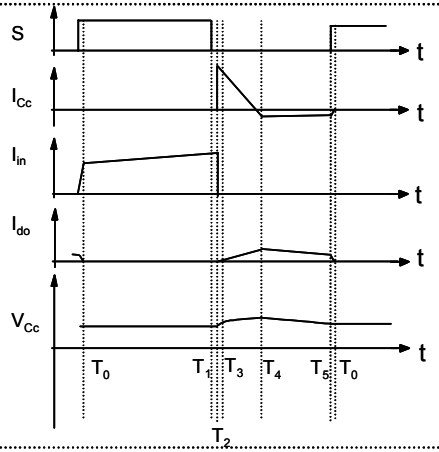
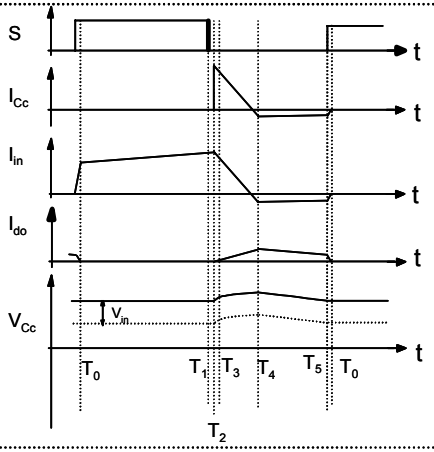
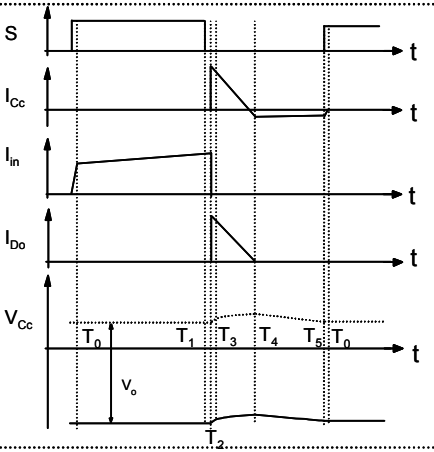
	Buck-boost version		
			
			
Gain		$\frac{V_o}{V_i}=\frac{d}{1-d}\cdot(N+1)\cdot\frac{(1+K)}{2}$	
V_{cc}	$V_c=\frac{d}{1-d}\cdot V_i\cdot\frac{(1+K)+(1-K)\cdot N}{2}$	$V_c=\frac{d}{1-d}\cdot V_i\cdot\frac{(1+K)+(1-K)\cdot N}{2}$	$V_c=-\frac{d}{1-d}\cdot V_i\cdot\frac{(1+N)-(1-K)\cdot N}{2}$
Remark	Minimum stress		

Fig. 2.32. Topology variations and comparison of the buck-boost version.

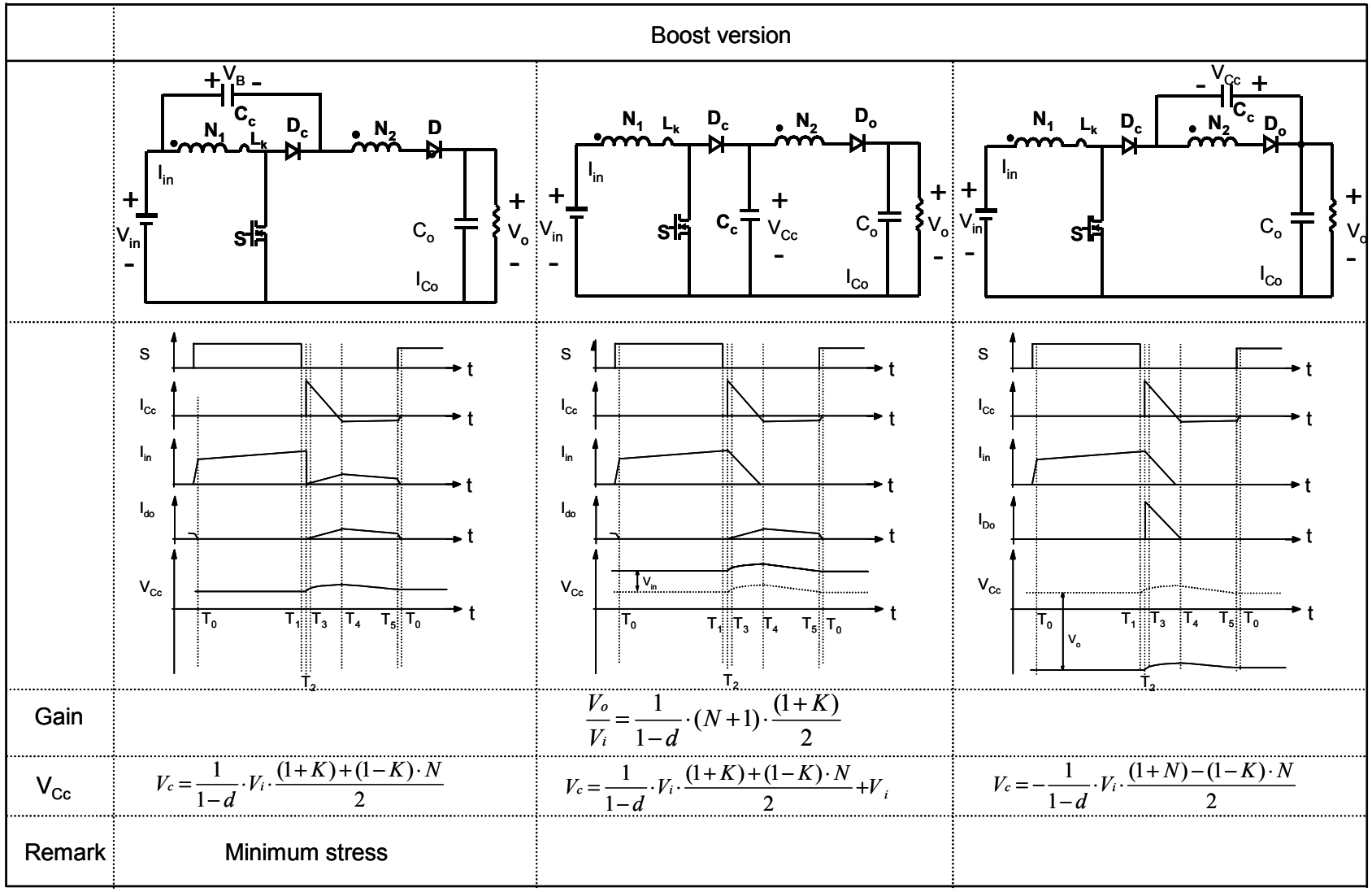


Fig. 2.33. Topology variations and comparison of the boost version.

For the step-down converter, the leakage energy-recycling scheme is proposed by authors at CPES [B18]. Fig. 2.34 shows the details for applying the concept to the step-down applications.

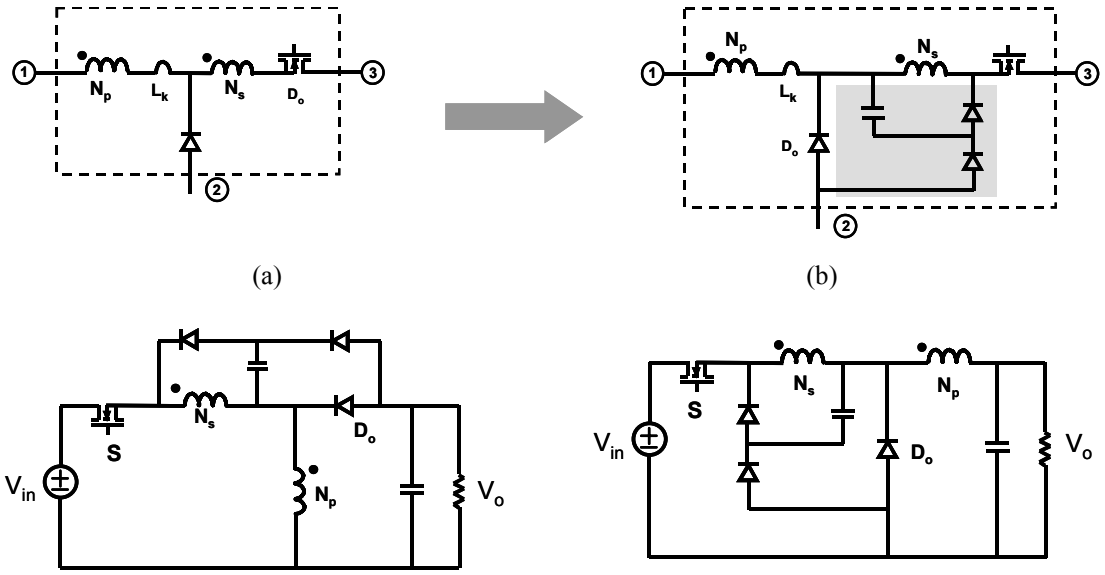


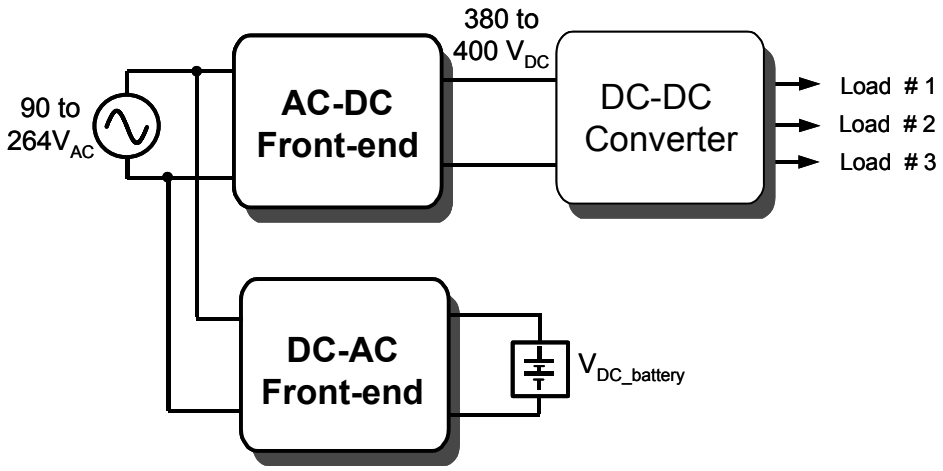
Fig. 2.34. Leakage handling for the step-up converters.

It has been demonstrated that this clamp circuit can achieve the switch voltage stress clamping and leakage energy recovery. The detailed analysis and verification are carried out for a 12V VRM with 1.5V and 50A output [B18].

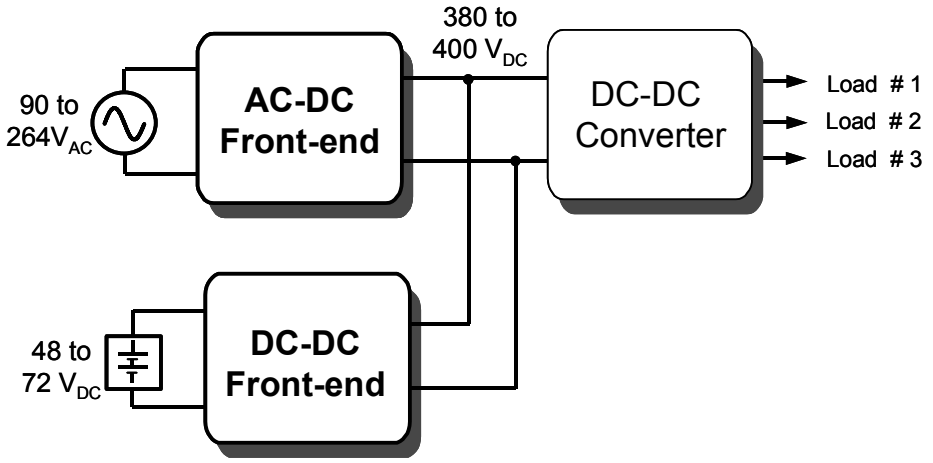
2.8. Application Example of the New Family of Topologies---DC-Backup Power Supply

New topologies with the proposed clamp concept can be derived. These circuits have a wide application range for achieving high step-up voltage gain. The new boost coupled-inductor converter is a good candidate for replacing the cascade DC-DC converters in DC-backup for

networking applications. The emerging DC-backup converter is a simple and efficient solution compared with the UPS solution, since it uses only a DC-DC converter instead of an inverter. Fig. 2.35(b) shows a dual-input front-end boost converter. The convergence of the computer and telecommunications industries makes the well-defined -48V DC battery plant a natural choice to offer hours of reserve time during outages of the AC mains [B7]-[B9]. A non-isolation DC-DC converter instead of a UPS inverter (AC UPS), both of which would be powered by the 48V DC power plant, is more efficient and much less complex [B8]-[B11]. A high-efficiency DC-DC converter that can generate 380V of DC bus from a 48V DC plant is the most important part of the DC-backup system. It should be pointed out that isolation is not necessary for the AC-DC or DC-DC front-ends, since the isolation is provided by the subsequent DC-DC stages. The DC-input front-end converter must provide approximately ten times the voltage gain. The state-of-the-art solution is the cascade boost converter. CCM operation of a power converter is preferred because of the low current stress to the switch. However, the output rectifier reverse recovery can result in high turn-on loss for the switch. Another major concern of high step-up DC-DC converters for this application is the extreme duty ratio and the rectifier reverse-recovery problem. Elimination of extreme duty ratios and alleviation rectifier reverse-recovery problem can significantly improve the performance of the power conversion.



(a)



(b)

Fig. 2.35. Different backup schemes:
(a) AC-UPS and (b) dual-input front-end converters [B9].

Both active and passive approaches adopt an auxiliary circuit to divert the rectifier current to a desired path. Utilizing coupled inductor to realize ripple current steering [A7]-[A12] and switching loss reduction [C20]-[C23]. Current steering using coupled inductors is a passive approach, which needs only a coupled winding of the existing magnetic component and few

passive components. Utilizing the current steering characteristic of coupled inductors to realize soft switching can simplify the topology.

Each family of circuits has a circuit with minimal voltage and current stress. In this section, the utilization of the converters is demonstrated. For the DC-input front-end converter, the boost-type coupled-inductor converter can be used because the output and the input have the same ground. The proposed solution, shown in Fig. 2.36, has minimum clamp capacitor voltage stress. It can be used for the step-up backup power supply. This converter has an inherent current steering characteristic. During the switch turn-off time period, the current is steered from the loop with the solid line to the loop with the dashed line. Before switch S turns on again, the current through D_c is already zero and D_c is naturally recovered. All output current goes through D_o and when switch S turns on, the leakage inductance of the coupled inductor controls the current decrease rate of the rectifier. The rectifier reverse-recovery problem is thus alleviated.

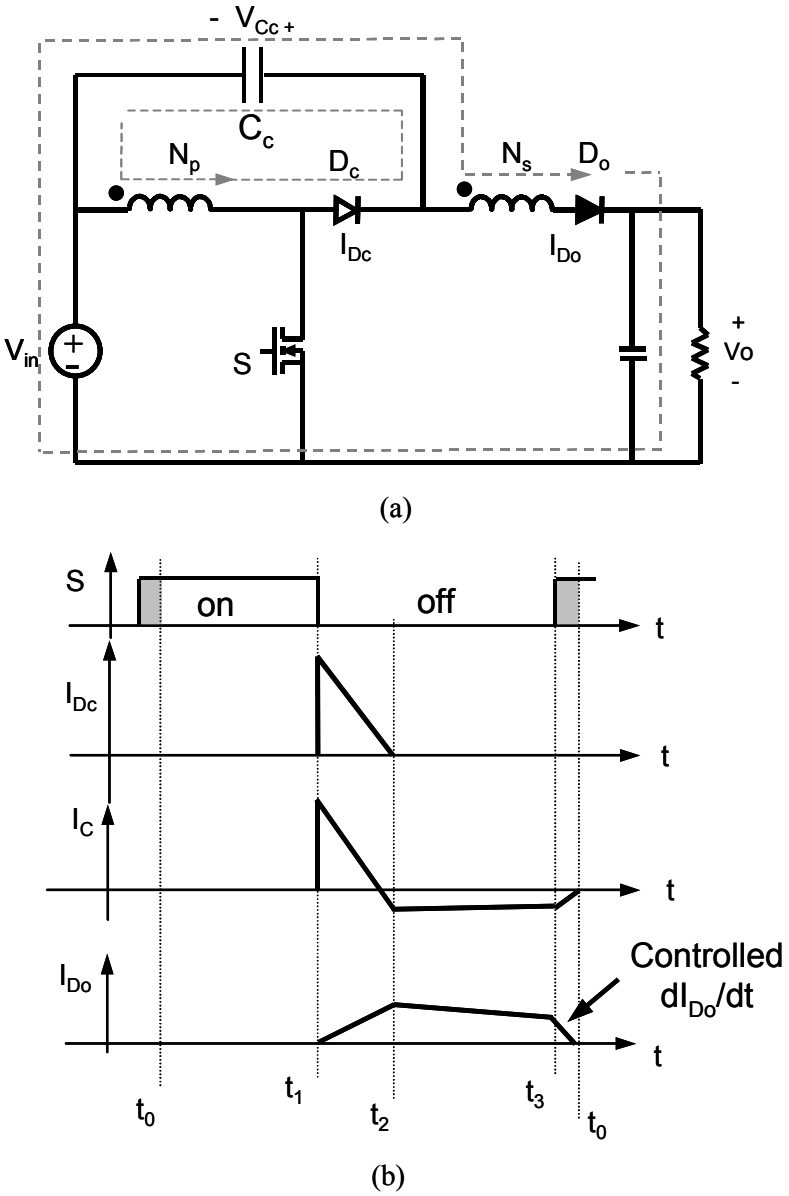


Fig. 2.36. Current steering of the proposed solution:
(a) circuit diagram and (b) key waveforms.

Fig. 2.37 shows the design graph for the DC-backup power supply. The other design steps are similar to those for the high step-up converter for use in the HID ballast.

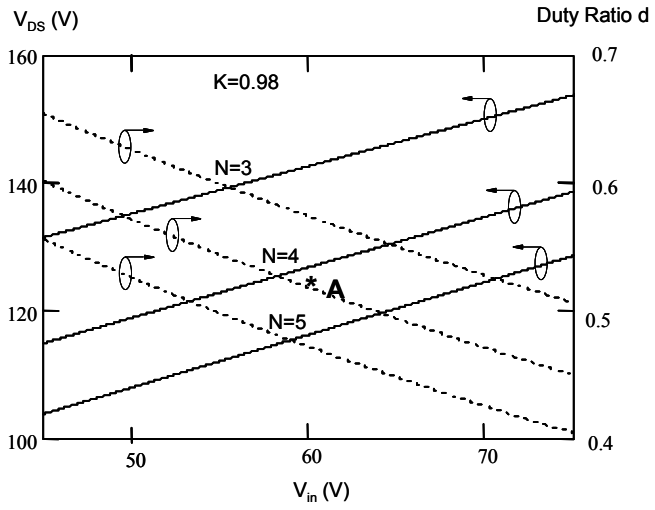


Fig. 2.37. Design graph for DC-backup power supply.

A 1kW DC-input front-end converter targeting 750W power supplies for high-end server systems [C1] was also built. The circuit topology is a clamp-mode coupled-inductor boost converter. Fig. 2.38 shows the topology and circuit parameters. Because the leakage inductor of the coupled inductor and the parasitic capacitor of the output diode resonate after boost switch S turns on, a proper snubber circuit is necessary in order to reduce the output rectifier peak voltage. The input voltage is 48-75V and the output voltage is 380V. Switch S is implemented with three paralleled IRFP254s (250V, 23A, 0.14Ω, To-247) from IR© (International Rectifier). The coupled inductor is implemented with one Kool Mμ toroidal core 77110-A7 from Magnetics©.

The primary winding is 40 turns with four strands of 175/40 litz wire in parallel. The secondary winding is 165 turns with 100/40 litz wire.

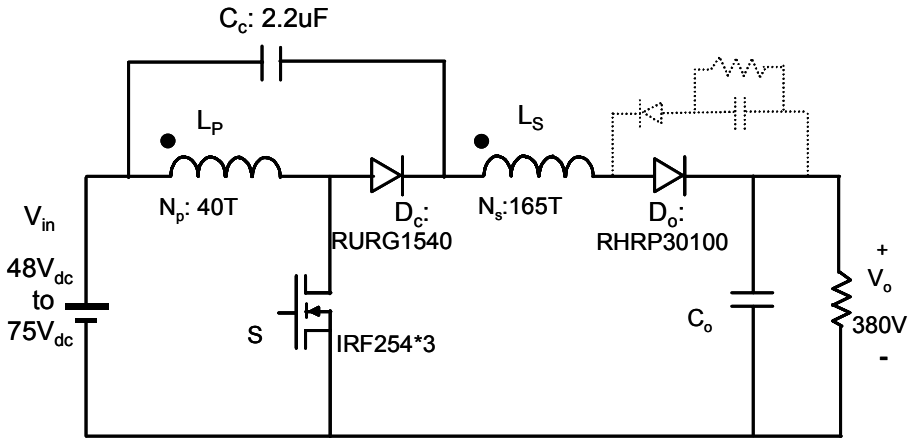


Fig. 2.38. Experimental test set up.

Fig. 2.39 shows the current waveform through primary inductor I_{Lp}, the voltage of clamp diode V_{DC}, and the voltage of active switch V_{DS}. Because the output diode is in series with the secondary winding of the coupled inductor, the leakage inductor limits the diode current decrease rate di/dt. The reverse-recovery problem of the output diode is significantly lessened, although the converter has high output power and high output voltage. As can be seen from Fig. 2.40, not only is the reverse-recovery current reduced, it is also delayed. There is no overlap between the switch voltage and the reverse-recovery current.

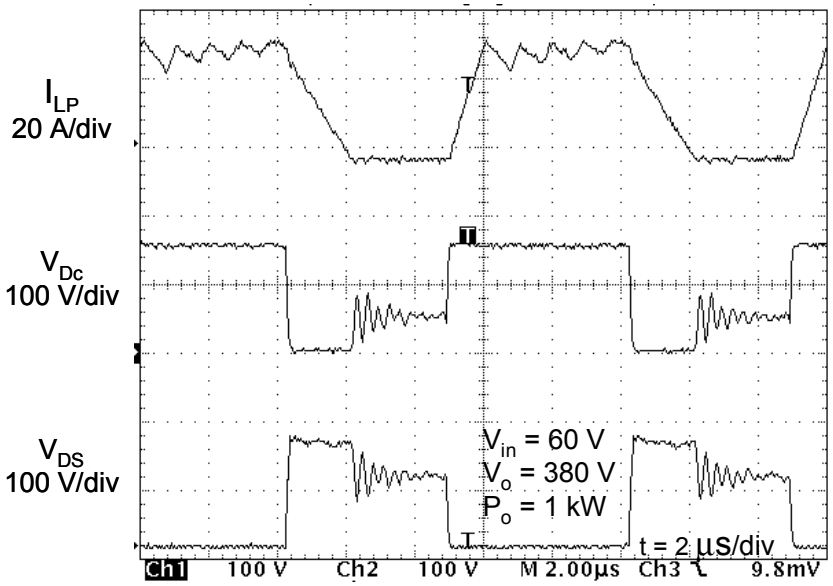


Fig. 2.39. Experimental waveforms of input inductor current and switch voltage.

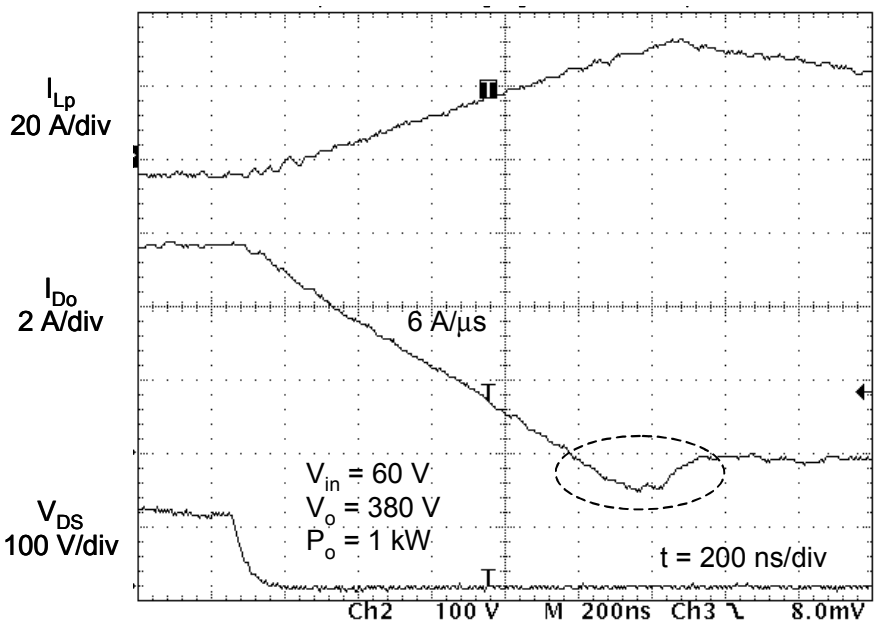


Fig. 2.40. Experimental waveforms of input inductor current, output diode current, and switch voltage.

Table 2.3 shows the measured efficiency of the prototype converter. As can be seen, the converter achieves more than 90% conversion efficiency under nominal operation conditions.

Table 2.3. Measured efficiency of the prototype converter.

Vin	48V	60V	75V
Duty Ratio	0.60	0.52	0.45
Efficiency	90.8%	91.9%	92.4%

The loss breakdown shown in Fig. 2.41 compares the proposed solution with the cascade boost converter. The proposed converter has lower loss than that of the cascade boost converter. The reason is that the output rectifier reverse-recovery problem is alleviated in the proposed converter. In reality, the efficiency of the cascade boost converter could also be improved if the output rectifier reverse-recovery problem could be alleviated. However, alleviating the rectifier reverse recovery in the second boost converter requires an extra circuit. The active approach will make the circuit more complex.

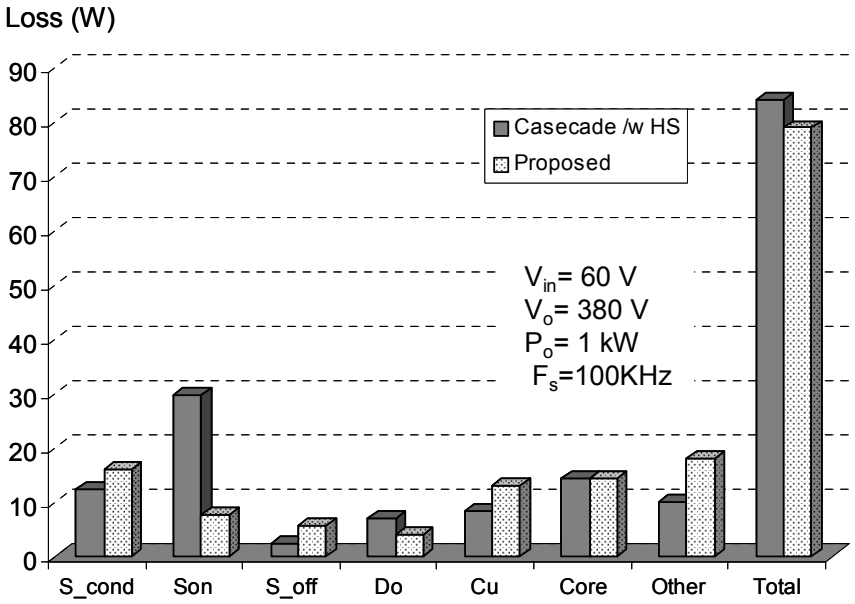


Fig. 2.41. Loss breakdown.

Not only does the proposed converter have an efficiency that is about 1% higher than that of the hard-switching cascade boost converter, but it is also much simpler than the cascade topologies. Table 2.4 compares the device components of the two solutions. In the proposed converter, three IRFP254s (250V, 23A, 0.14Ω, To-247) are used. In the cascade converter, three IRFP3415 (150V, 43A, 0.042Ω, To-220) and two IRFP22N50A (500V, 22A, 0.23Ω, To-247) are used. In the proposed converter, only one set of controller and magnetic components are necessary, while the cascade solution needs two sets.

Table 2.4. Component list.

	Mosfet	Diode	Magnetics	Controller
Proposed	3	2	1	1
Cascade	5	2	2	2

The proposed solution can steer the current by utilizing the coupled inductor, and has a simple structure. The leakage inductance of the coupled inductor can be used to control the di/dt of a rectifier. Compared to either the active or other passive approaches, this solution is easy to realize without introducing voltage and current stresses.

One observation is that the cascade boost converter can also achieve significantly performance improvement if the rectifier reverse-recovery loss could be eliminated, as shown in Fig. 2.42. Although the extreme duty ratio is not a concern for the cascade boost converter, the rectifier reverse-recovery problem still can cause extreme losses. There are also many similar applications, such as the front-end PFC converters. Adding an extra circuit to alleviate the rectifier reverse recovery will make the circuit more complex. Utilizing the coupled inductor to alleviate the rectifier reverse-recovery problem is a simple and effective solution, as demonstrated in this chapter. How to alleviate the rectifier reverse-recovery problem by using the coupled inductor for CCM boost converters motivates the study of the next chapter.

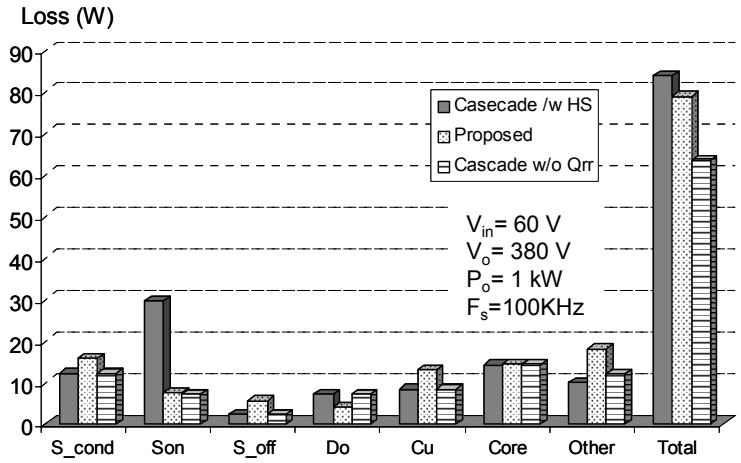


Fig. 2.42. Significant reverse-recovery loss in the cascade converter.

2.9. Summary

Emerging applications call for high-efficiency, high step-up DC-DC converters. Basic topologies suffer from extreme duty ratios and severe rectifier reverse-recovery problems. This chapter presents the derivation, theoretical analysis, practical design and experimental results for a family of high-efficiency, high step-up, clamp-mode coupled-inductor converters. The operation of the proposed converters is similar to that of their active-clamp counterparts, but the new converters utilize one additional diode and one coupled winding instead of an active switch in order to realize the clamp function. By adding a small capacitor, the leakage energy is recovered in such a way as to generate only a low level of circulating energy, and the switch voltage stress is significantly reduced. When the output voltage and power reach a certain level, the rectifier reverse-recovery problem can cause severe loss. The state-of-the-art solution is to control the di/dt of the rectifier during its turn-off. The circuit realization involves an auxiliary circuit and makes the solution complex. The proposed topology has an inherent current steering capability so that no extra circuit is necessary to alleviate the rectifier reverse-recovery problem. The proposed concept is generalized as a coupled-inductor switching cell and is applied to other DC-DC converters. The experimental results, demonstrated in a 36W converter for HID ballast and a 1KW converter for DC-backup power supply, closely match both the theoretical analysis and the efficiency prediction.

The rectifier reverse-recovery problem causes severe loss for some applications such as front-end CCM boost converters for telecommunications and server application. How to alleviate the rectifier reverse recovery with coupled inductors will be addressed in the next chapter.

Chapter 3.
Utilizing Coupled Inductors to Alleviate Rectifier Reverse Recovery

3.1. Introduction

The output rectifier reverse-recovery problem becomes a severe concern when the output voltage reaches a certain level and no Schottky diode is available. The reverse-recovery current of the output rectifier has detrimental effects on the performance of converters. High switching loss resulting from the reverse-recovery current dramatically deteriorates the thermal condition of the switches. The state-of-the-art solution is to control the current decrease rate *di/dt* of the rectifier during its turn-off. To accomplish this function, either a simple auxiliary circuit with an active switch or a complex network consisting only of passive components is needed. The solution with the active switch increases the circuit complexity. The problem with the method that uses only passive components is high voltage stress and/or current stress. The high step-up converters proposed in Chapter 2 have an inherent current-steering characteristic to alleviate the rectifier reverse-recovery problem. Utilizing coupled inductors instead of an active switch or a complex circuit to steer the current can result in a simple topology. In this chapter, such use of a coupled inductor is studied. Extension of the current-steering approach into the CCM boost converter is demonstrated. A simple and effective solution for alleviating the rectifier reverse-recovery problem is proposed, analyzed, and experimentally verified. Then the concept is also extended to other basic topologies.

3.2. A Brief Review of State-of-The Art Solutions

When a boost converter is operated in CCM, the reverse-recovery current of the output rectifier D_o has a detrimental effect on the performance of the converter. The adverse effects related to the rectifier reverse-recovery problem are illustrated in Fig. 3.1.

1) During the turn-on transition of switch S, the reverse-recovery current I_{rr} induces extra turn on loss due to the overlapping of the high current and voltage.

2) The reverse-recovery current increases the current stress of switch S.

3) The parasitic inductance L_k in loop O can increase the voltage stress of the output rectifier D_o. The maximum voltage stress of the output rectifier is given by:

$$V_{Do} = V_o + L_k \cdot di(rec)M / dt , \qquad \text{Eq. 3-1}$$

where *di(rec)M/dt* is a parameter to quantify the softness of a rectifier during its turn-off.

4) The high level of reverse-recovery current may increase the electromagnetic interference (EMI) noise.

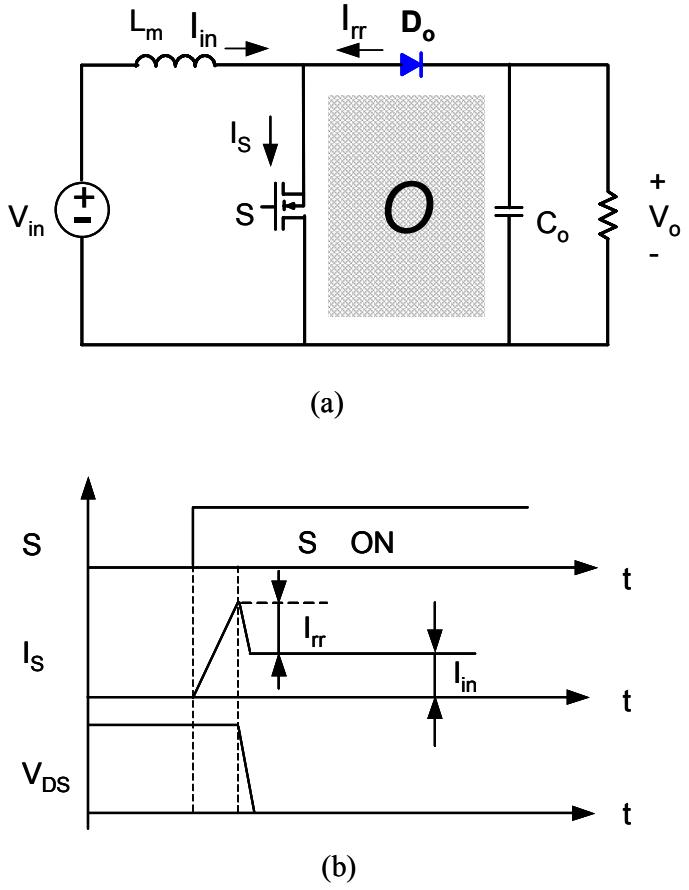


Fig. 3.1. Detrimental effects of rectifier reverse-recovery on CCM boost converters: (a) a CCM boost converter and (b) waveforms showing reverse-recovery effect.

To avoid these adverse effects, the use of a discontinuous current mode (DCM) boost converter is an alternative. By paralleling two or more DCM boost converters with a phase-shift control strategy, the input current ripple is dramatically reduced. Although this approach can be extended to high-power applications [C4], the complicated power stage and control circuits are not desirable. CCM boost converters are the best front-end converters for active input current shaping. Reducing the operation frequency of CCM boost converters is an option for improving

the efficiency. However, reducing the operating frequency is not a good solution in terms of power density and cost. The GaAs rectifiers can significantly improve the efficiency and reduce both device stress and EMI noise. Unfortunately, the GaAs rectifiers are expensive, and the thermal problems still exist although the GaAS rectifiers' performance is almost independent of the junction temperature [C5]. The SiC diode is similar [C6].

The efficiency of a CCM boost converter would be significantly improved if the output rectifier could be softly turned off to reduce the adverse effects of reverse-recovery current. State-of-the-art technology to alleviate the silicon rectifier reverse-recovery problems involves softly turning off the rectifier by controlling the current decrease rates *di/dt* of the rectifier during its turn-off. A snubber inductor L_s can be inserted into parallel branch A of the boost switch S, or into the loop (B or C) that passes the rectifier reverse-recovery current, as shown in Fig. 3.2. This snubber inductor L_s is used to control the current decrease rates of the rectifier as roughly V_o/L_s during its turn-off. An auxiliary circuit is necessary to provide reset to the snubber inductor. The reset circuit can use either all passive lossless components or the combination of passive components and an active switch. When the reset circuit includes an active switch, it is called an active approach; otherwise it is a passive approach.

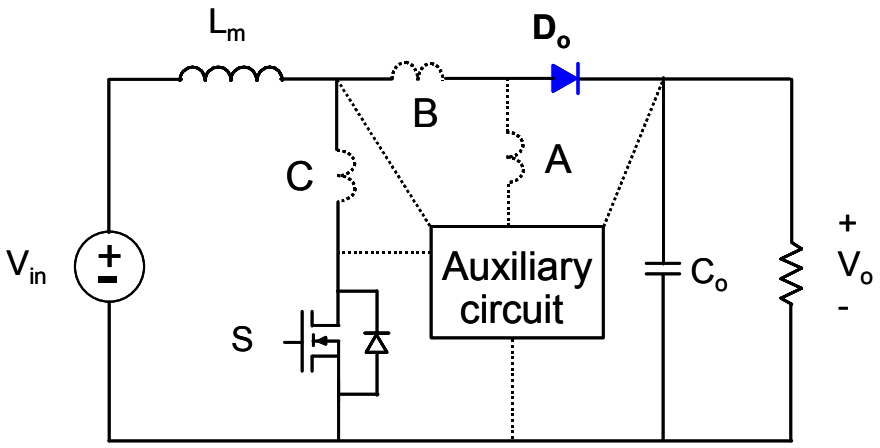


Fig. 3.2. General structure for alleviating rectifier reverse-recovery problem.

The active approach has two advantages. Not only can the rectifier reverse-recovery problem be alleviated, but also zero-voltage-switching (ZVS) operation of the main switch can be achieved. The well-known circuits in the active approach category [C7]-[C14] are the baby boost and the active-clamp scheme. The baby boost circuit involves shifting the output rectifier current to a new parallel branch with an extra active switch. The boost switch turns on under a ZVS condition. The new branch utilizes a small inductor Ls to control the rectifier current decrease rates during its turn-off. Because the added small inductor is essentially in parallel with the branch of the boost switch, the boost switch suffers no extra voltage or current stress. The conversion efficiency can be dramatically improved, because the power dissipation in the added branch can be much smaller than the extra power loss incurred when the new auxiliary circuit is not used. However, adding an auxiliary circuit with an active switch increases the complexity of both the circuit topology and control. The output capacitor of the auxiliary switch and the small inductor can induce severe undesired resonance. Although adding a rectifier and a saturable inductor can reduce the resonance, the topology becomes complex and the cost increases. The

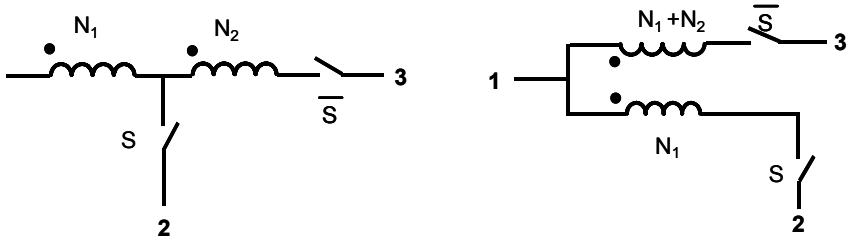
active-clamp approach [C10]-[C14] inserts a snubber inductor L_s into the loop that passes the rectifier reverse-recovery current. The rectifier current decrease rate *di/dt* during turn-off can be controlled as roughly V_o / L_s. Meanwhile, an active switch and a small capacitor are also necessary in order to reset the snubber inductor. Despite the advantages of this approach, its disadvantage is that there is a large amount of circulating energy in the auxiliary circuit, which may induce high conduction loss. Almost all of these circuits require an isolation gate driver [C10]-[C13]. Overlapping the driver signals of the main switch and auxiliary switch will lead to a fatal circuit failure. The circuit proposed by Jovanović, et al [C14] does not require an isolation gate driver, and the converter provides better performance, but the leakage inductor is a possible concern at high power levels. The extra active-clamp switch and its associated controller are not desirable from both cost and reliability standpoints.

It has been demonstrated in Chapter 2 that the step-up DC-DC converter can realize inherent current steering. The current in the original output rectifier is steered to a new branch consisting of an added diode and an inductive impedance so that the rectifier current of the added diode is controlled. The rectifier reverse-recovery problem can be alleviated by using the current-steering function of a coupled inductor.

3.3. Alleviated Reverse-Recovery Problem with Coupled Inductors

3.3.1. Topology Derivation

The coupled-inductor switching cell in Fig. 3.3(b) is derived form the switching cell shown in Fig. 3.3(a). These two cells are equivalent. The new switching cell is symmetrical. Therefore, there are three converters derived from this cell, as shown in Fig. 3.4.



(a) (b)

Fig. 3.3. Derivation of equivalent switching cell:
(a) the cell discussed in the previous chapter and (b) a new equivalent cell.

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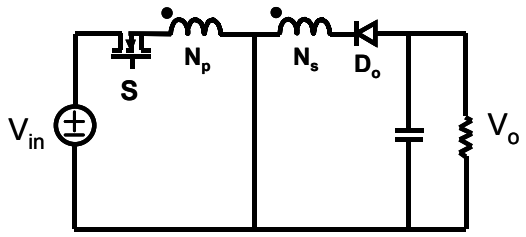
<td> 

$$M = \frac{N_s}{N_p} \cdot \frac{d}{1-d}$$
(a) coupled-inductor buck-boost converter</td>
<td>Same as (a)
(b)</td>
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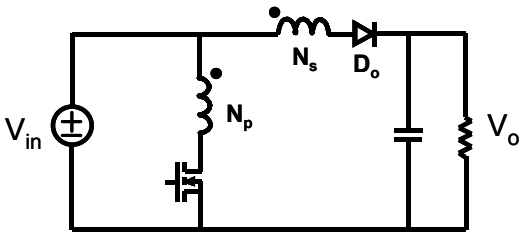
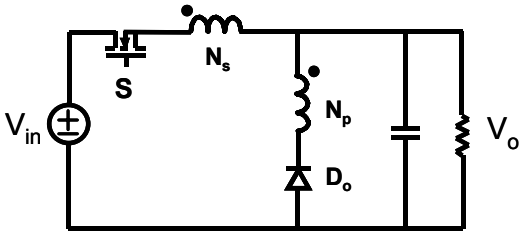
<td> 

$$M = \frac{N_s - N_p}{N_p} \cdot \frac{d}{1-d} + \frac{1}{1-d}$$
(c) coupled-inductor boost</td>
<td> 

$$M = \frac{N_p}{N_s + (N_p - N_s) \cdot d} \cdot d$$
(d) coupled-inductor buck converter</td>
</tr>
<tr>
<td>Same as (c)
(e)</td>
<td>Same as (d)
(f)</td>
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Fig. 3.4. Current steering of a coupled inductor.

These converters all operate in the same way as the conventional buck, boost or buck-boost converter when N_s is equal to N_p.

In order to alleviate the rectifier reverse-recovery problem, it is necessary for the leakage inductance of the coupled inductor to control the current-steering rate. However, the leakage energy must be handled properly. The way that the leakage energy is discharged to the output can also be extended to other topologies.

Fig. 3.5(a) shows the new coupled-inductor switching cell. In practical applications, the leakage inductance can be used to control the current-steering process and then to control the di/dt of the diode during the turn-on of switch S. However, the leakage energy can induce switch stress and loss for switch S when it is turned off. A solution that discharges the leakage energy to the output has been verified. Therefore, the practical cell can be shown in Fig. 3.5(b). Applying this cell to the converter shown in Fig. 3.4 generates the new converters shown in Fig. 3.5(c)(d)(e). The two converters have basically the same topology. The leakage inductor is utilized on one hand to control the di/dt of the output rectifier; on the other hand, the leakage energy must be handled properly to make the circuit work. As discussed in Chapter 2, either a dissipative snubber or an active-clamp scheme can be used. The previously proposed clamp scheme does not apply to this case since the discharge path has been shifted. But the active-clamp scheme can still be applied. The clamp voltage is slightly higher than the output voltage; this voltage difference drives the current steering. This active-clamp scheme results in a complex topology. A simple solution to handle the leakage energy in this converter is to discharge the leakage energy directly to the output.

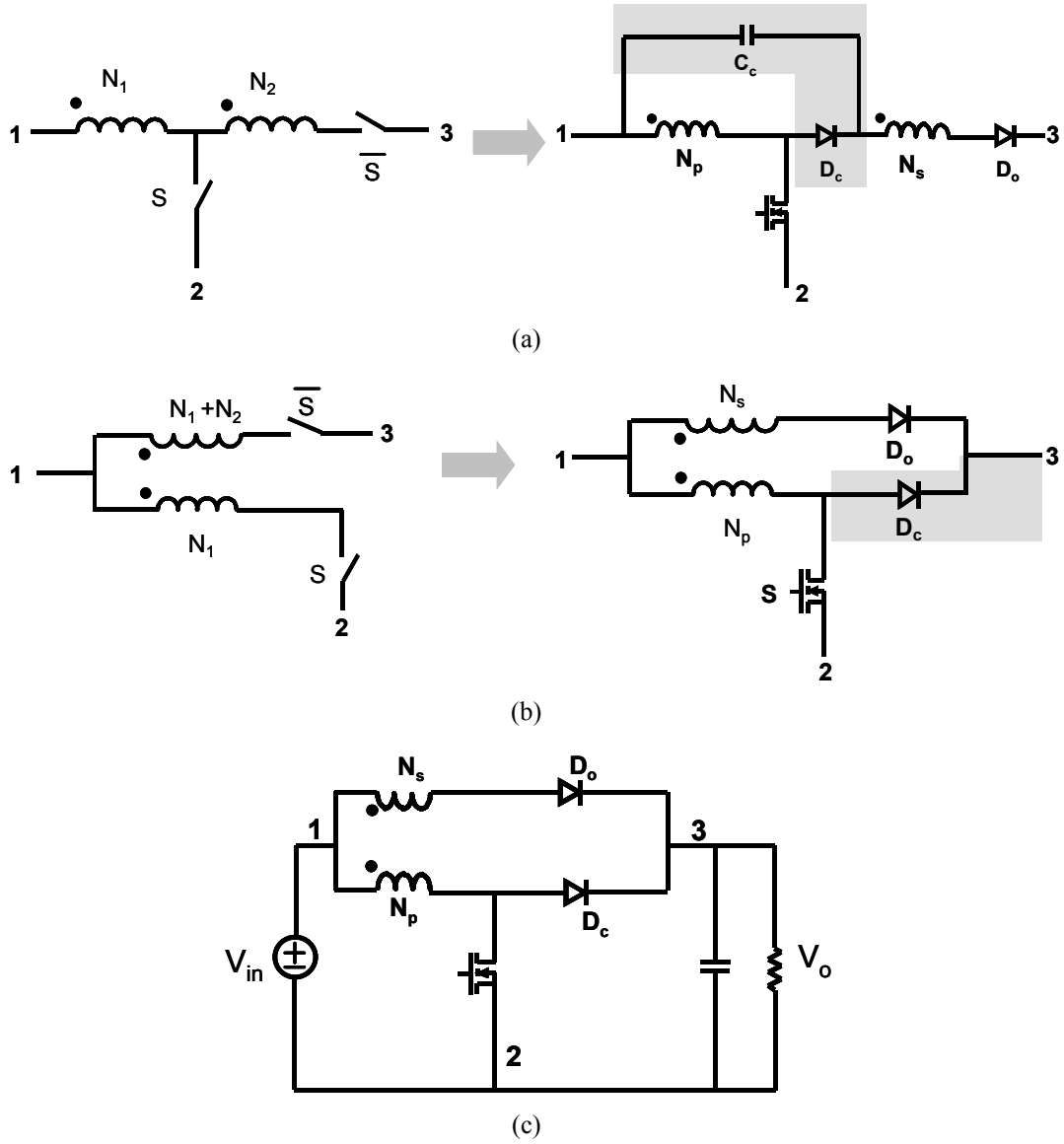
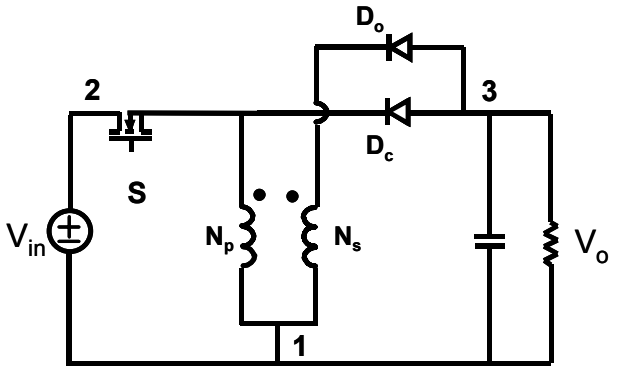


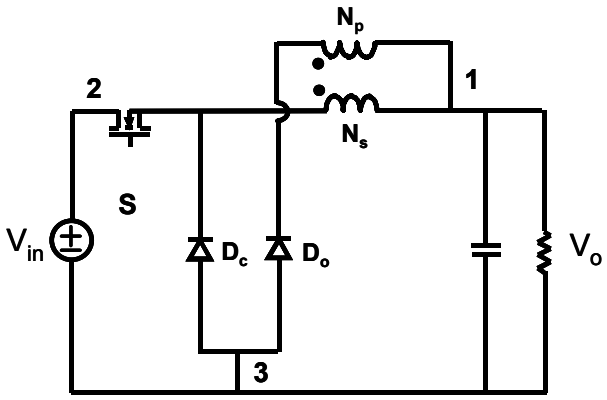
Fig. 3.5 Derivation of boost converter with alleviated rectifier reverse recovery: (a) previous leakage energy-recovery scheme; (b) new leakage-recovery scheme; and (c) coupled-inductor boost converter.

The converter shown in Fig. 3.5 can achieve current steering. If both windings are connected to the same voltage source, then the current-shifting condition can be met by changing the turns

ratio. We have found that the condition is that the secondary winding must be larger than *1/K*, which means that the secondary winding turns number must be higher than that of the primary. Because the turns ratio is larger than one, the input current is different from that in a CCM boost converter. There is a small slope change, which will be discussed in the operation analysis.



(a)



(b)

Fig. 3.6. The concept as applied to other coupled-inductor converters:
(a) buck converter and (b) buck-boost converter.

3.3.2. Operation Analysis

The proposed boost converter employing a coupled inductor reduces the reverse-recovery-related loss. Compared to the conventional boost converter, the proposed converter has a new branch that consists of a rectifier D_o and a new coupled winding for the original boost inductor. The added winding has a number of turns that is slightly larger than that of the original boost inductor. The basic idea of the circuit is simply to control the current decrease rate through the output rectifier D_o using the leakage inductor of the coupled inductor when switch S turns on. During the switch turn-off time period, the coupled inductor will steer the current of the rectifier D_c to the rectifier D_o. The current through the clamp boost rectifier D_c can be reduced to zero before switch S turns on.

To analyze the circuit operation, the coupled boost inductor is modeled as a combination of the magnetizing inductor L_m, an ideal transformer with turns ration N_s:N_p, and a leakage inductor L_k, as shown in Fig. 3.7. The reference directions for currents and voltage are also given in the same graph.

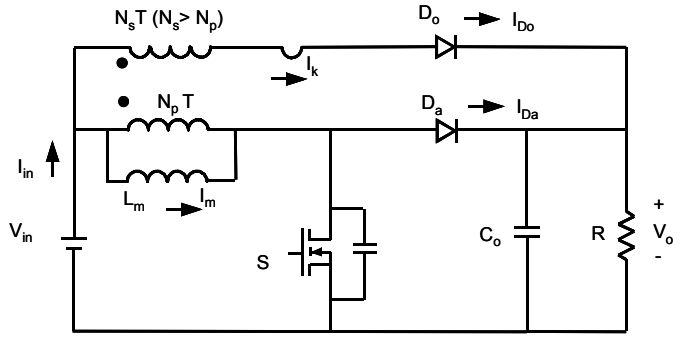


Fig. 3.7. Analysis model.

Fig. 3.8 shows the seven topological stages of the converter in one switching cycle. Fig. 3.9 shows the corresponding key waveforms of the operation.

[T_0, T_1]: Switch S is already on, and the output rectifier D_o and clamp rectifier D_a are reverse-biased. The magnetizing inductor is linearly charged by the input voltage source. During this time period, the voltage stress of D_a is the same as that of the conventional boost, while the voltage stress of D_o is given by Eq. 3-2:

$$V_{Do} = V_o + V_{in} \cdot (N-1) . \qquad \text{Eq. 3-2}$$

[T_1, T_2]: Switch S turns off at T_1. The parasitic capacitor of the switch is charged by the magnetizing current in an approximately linear way.

[T_2, T_3]: The output rectifier D_o is forward-biased at T_2 when V_{DS} (voltage on parasitic capacitor of switch S) is charged to the value meeting condition Eq. 3-3:

$$V_{in} + (V_{DS} - V_{in}) \cdot N > V_o . \qquad \text{Eq. 3-3}$$

[T_3, T_4]: At T_3, the parasitic capacitor is charged to the level of the output voltage. Output rectifier D_o conducts. The reflected voltage from the winding with $1T$ to the winding with NT is $N(V_o - V_{in})$. The total voltage applied to the winding with NT is $V_o - V_{in}$. Therefore, a positive voltage $(V_o - V_{in})(N-1)$ is applied to the leakage inductor L_k. The current through L_k increases linearly. The current-shifting process, from the clamp rectifier to the output rectifier, begins.

[T_4, T_5]: If the leakage inductor L_k is provided with sufficient charge voltage and time, the output current is completely shifted to the new branch at T_4. All boost current goes to the output

filter through D_o. The clamp rectifier D_a will be naturally recovered. The reflected magnetizing current through D_a decreases linearly.

[T_5, T_6]: At T_5, switch S turns on again. The voltage $V_o+V_{in}(N-1)$ is applied to the leakage inductor L_k. The di/dt of the rectifier D_o is controlled by the leakage inductor L_k. The reverse-recovery problem of the rectifier D_o is alleviated due to the controlled di/dt.

[T_6, T_0]: The switch current increases linearly until it reaches the level of the input current, and the rectifier current i_{Da} falls to zero. However, the rectifier current continues flowing in the opposite direction due to the residual stored charge, even though this charge has been dramatically reduced.

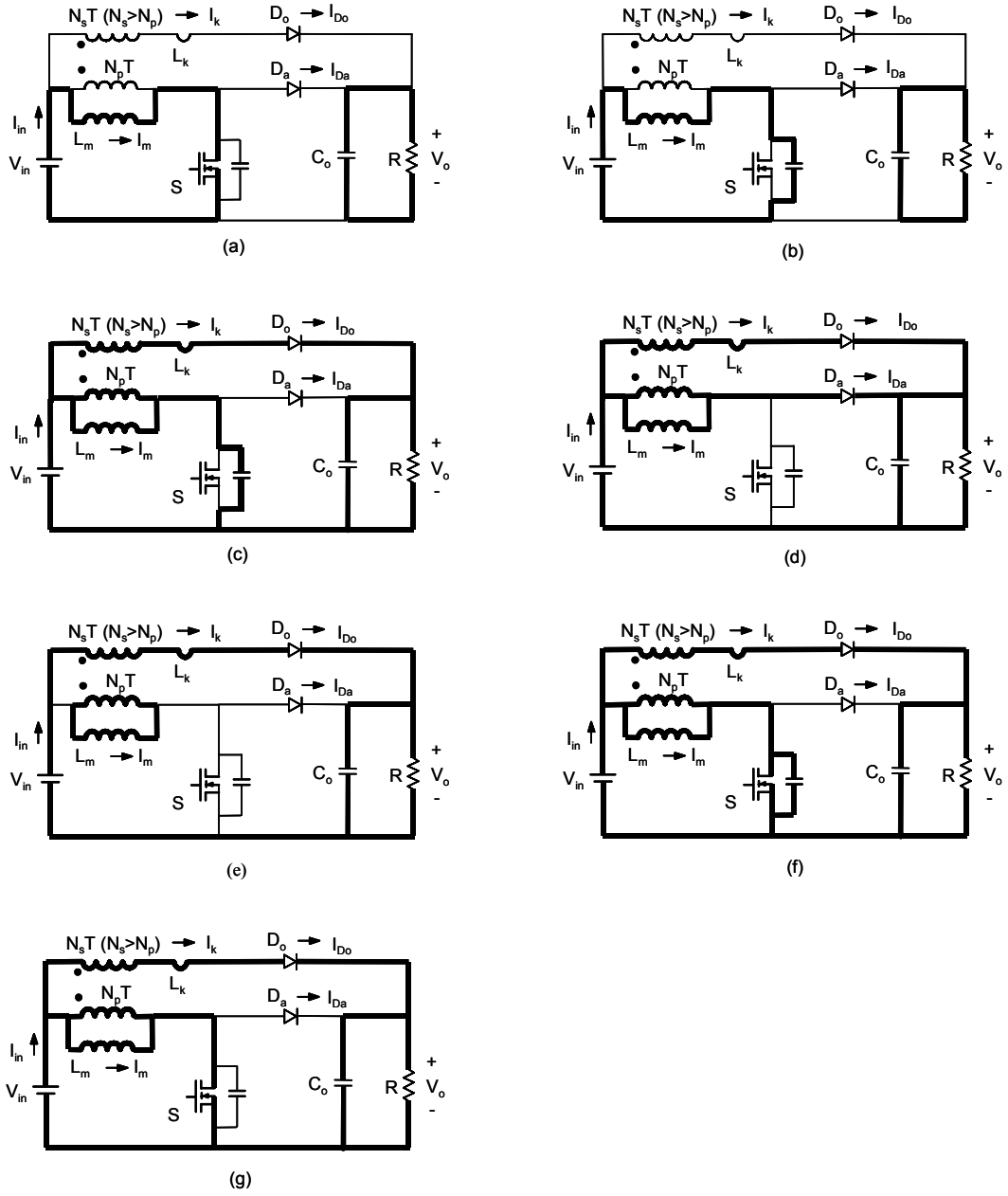


Fig. 3.8. Operation modes of the proposed converter:
(a) [T_0, T_1]; (b) [T_1, T_2]; (c) [T_2, T_3]; (d) [T_3, T_4]; (e) [T_4, T_5]; (f) [T_5, T_6]; and (g) [T_6, T_0].

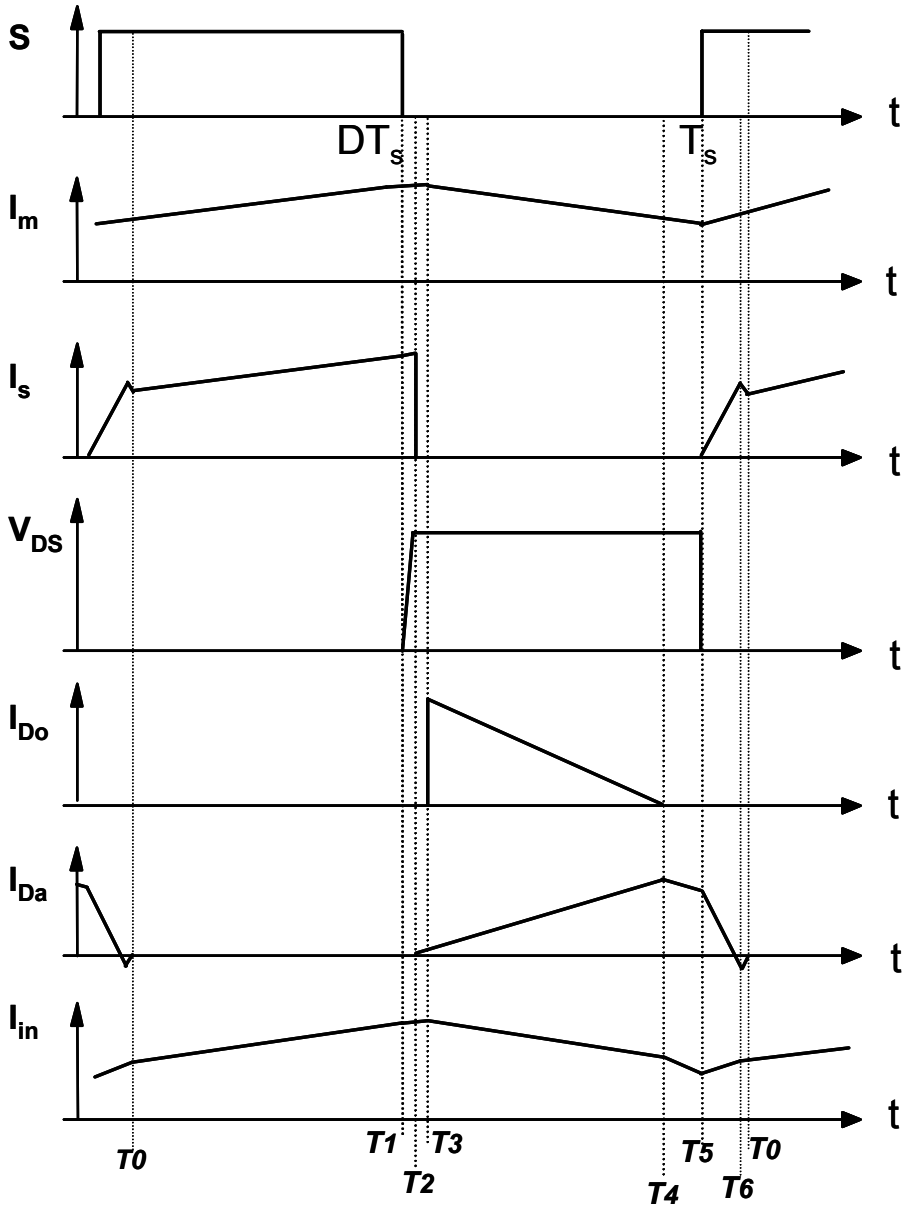


Fig. 3.9. Key waveforms corresponding to the operation modes.

Rectifier D_o has a junction capacitor. This parasitic capacitor and the leakage inductor form a resonant tank. Due to the undesirable resonance that occurs between the leakage inductor and the

parasitic capacitor of D_o after switch S turns on, a small snubber circuit for D_o is generally necessary to avoid extra voltage stress on D_o. It also should be mentioned that the so-called *di(rec)M/dt* of a fast-recovery rectifier has a significant effect on the voltage stress of D_a [C3], since the maximum voltage stress of the rectifier D_o is given by Eq. 3-4:

$$V_{Do} = V_o + L_k \cdot di(rec)M / dt \,. \qquad \text{Eq. 3-4}$$

To effectively alleviate the rectifier reverse-recovery problem in the proposed circuit, two conditions must be satisfied.

First, the current through rectifier D_a must be reduced to zero before switch S turns on so that D_a can be naturally recovered. The decrease rate of I_{Da} is given by Eq. 3-5:

$$\frac{dI_{Da}}{dt} = \frac{(V_o - V_{in}) \cdot (N-1)}{L_k} \cdot N \,. \qquad \text{Eq. 3-5}$$

At this decrease rate, the forward current through clamp rectifier D_a can be reduced to zero during the turn-off time period if the following condition is satisfied:

$$\frac{dI_{Da}}{dt} \cdot (1-d) \cdot T_s > I_{Da\_T2} \,, \qquad \text{Eq. 3-6}$$

where T_s is the switching time, d is the duty ratio, and I_{Da_T2} is the current of D_a at time instance T_2.

The duty ratios of CCM boost converters for PFC vary with the line variations. Fortunately, the current is small when the duty ratio is large at the input voltage near the zero-crossing point. Although switch S has a shorter turn-off time period during which the current must be shifted to the new branch, the current is also small. When the input voltage is close to the peak area, the CCM boost converter has a large level of rectifier forward current and small duty ratios.

Therefore, more time is available for the current through D_a to be shifted. In other words, no large N is needed to shift the current. Section IV will address the design issues in detail.

The second condition that must be met is that, in order to alleviate the rectifier reverse-recovery problem of the output rectifier D_o, the current decrease rate of rectifier D_o must be controlled when switch S turns on. The controlled rate is given by Eq. 3-7:

$$\frac{dI_{Do}}{dt} = \frac{V_o + V_{in} \cdot (N-1)}{L_k}. \qquad \text{Eq. 3-7}$$

Generally, it is preferable for this decrease rate to be controlled within 100 A/μS in order to effectively alleviate the rectifier reverse-recovery problem.

A larger L_k could offer better control of the di_{Do}/dt. However, a larger L_k requires a higher reset voltage in order to reduce its current to zero during a given period, which means a larger N is needed. There are two disadvantages to having a larger N.

First, the voltage stress of D_o given by Eq. 3-2 increases when N increases. It is preferred to be able to use a rectifier with the same voltage rating as the original rectifier. To minimize the voltage stress of rectifier D_o, the N should be designed to be close to one.

Second, there is a small slope change in the input current during the current-steering process. After switch S turns on, the current is quickly steered back from the added branch to the original one; the input current has a larger increase slope during [T_5, T_6] than during [T_0, T_1]. From both input filter and EMI standpoints, the less the slope changes, the better, which means a small N is preferred.

3.3.3. Design Issues and Experimental Results for DC-DC Applications

Although silicon rectifiers have problems with reverse recovery, which has a significant impact on the performance of a power converter, there is insufficient information in the data sheets provided by rectifier manufacturers. Table 3.1 shows a comparison of different hyper-fast recovery rectifiers from different manufacturers. As can be seen, the data sheets only provide one point of test data under room temperature, which is far from sufficient to know how to effectively control the reverse-recovery current. A circuit to test rectifier reverse-recovery performance as shown in Fig. 3.10, was built in order to obtain an understanding of how to alleviate the rectifier reverse-recovery problem. *Loop O* is minimized to reduce the parasitic parameters. Two probes with the same properties are used to measure the voltage and current to avoid delay. From the survey and previous experiences, the RHRP860 from Intersil (Fairchild now) is selected as the output rectifier because of its low reverse-recovery charge and soft recovery characteristic. Fig. 3.11 shows the test waveforms with different levels of di/dt at room temperature (25^{o}). Fig. 3.12 shows the test waveforms with different levels of di/dt under an ambient temperature of 55^{o}.

Table 3.1. Comparison of different fast-recovery diodes.

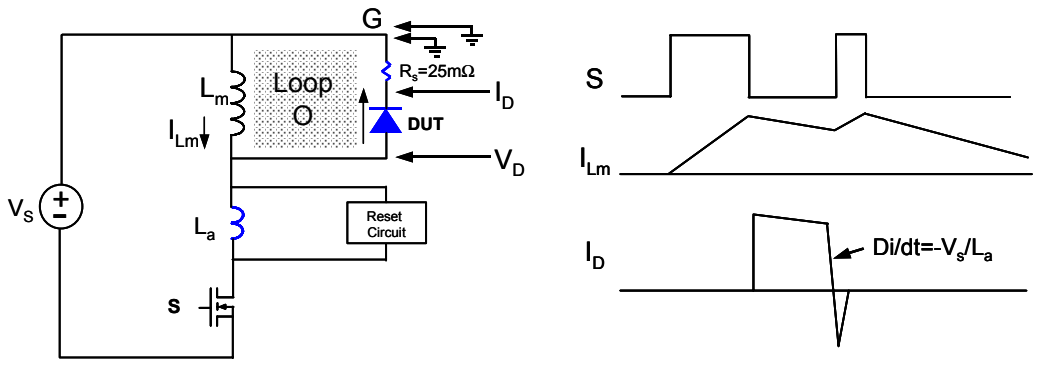
Manufacture	Device	V_{Res}(V)	I_F(A)	V_F(V)	T_{rr}(nS)	Q_{rr}(nC)	Package
ON	MUR860	600	8	1.2-1.5 @ 8A	60 @ 1A	NA	To-220
IXYS	DSEI8-06A	600	8	1.3-1.5 @ 8A	100ns @ 8A	400 @ 200A/us 8A	To-220AC
IXYS	DESP8-06B	600	8	1.6-2.5 @ 8A	NA	NA	To-220AC
IR	HFA08TB06	600	8	1.7-2.1 @ 8A	37 @ 8A	65 @ 200V	To-220AC
Intersil	RURD860	600	8	1.3-1.5 @ 8A	60 @ 8A	195	To-251
Intersil	RHRP860	600	8	1.7-2.1 @ 8A	35	56	To-220AC

Fig. 3.13 shows the measured reverse-recovery charge Qrr of the RHRP860 under different temperatures. From Fig. 3.13, we can draw the following conclusions:

- The temperature of the rectifier can strongly affect the reverse-recovery charge. Therefore, the output rectifier that can result in the reverse-recovery problem should be as cool as possible.
- The current decrease rate di/dt of the rectifier can dramatically affect the reverse-recovery charge Qrr. An effective solution for alleviating the rectifier reverse-recovery problem is to control the current decrease rate di/dt so that it remains under 100 A/μs; this is also

verified in other work [C12]. No further significant benefits can be achieved if the di/dt is controlled lower than 40 A/μs.

- The current decrease rate di/dt of the rectifier does not change the snap factor. Low levels of rectifier reverse-recovery current also reduce the rectifier voltage stress.



(a) (b)

Fig. 3.10. Test bed for measuring reverse-recovery charge:
(a) diagram of test circuit and (b) waveforms of the two-pulse test method.

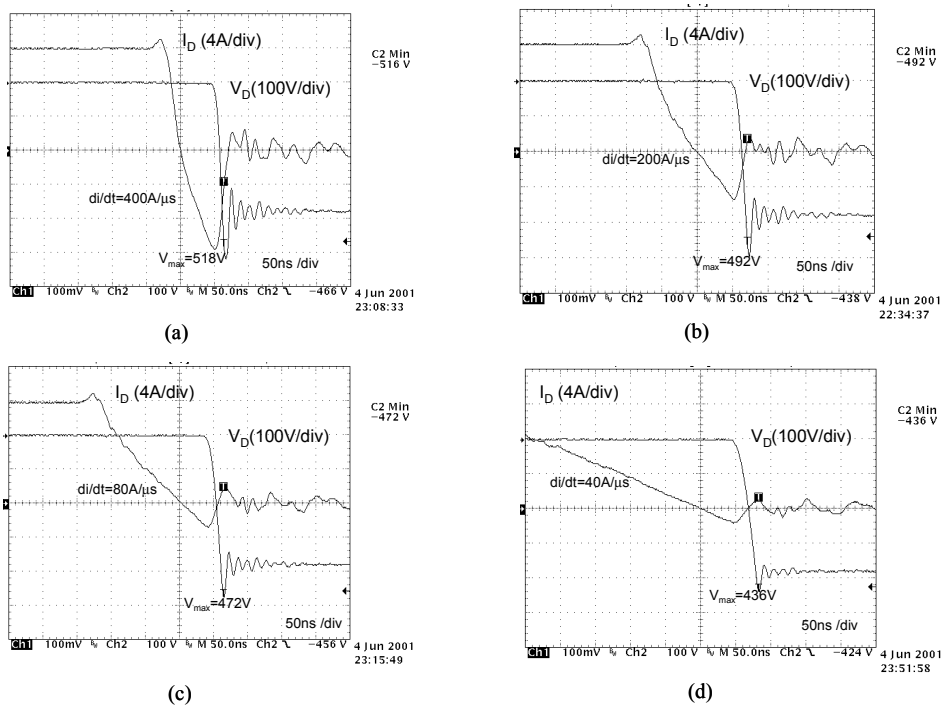


Fig. 3.11. Measured waveforms showing the reverse-recovery of PHRP860 (at 25°C).

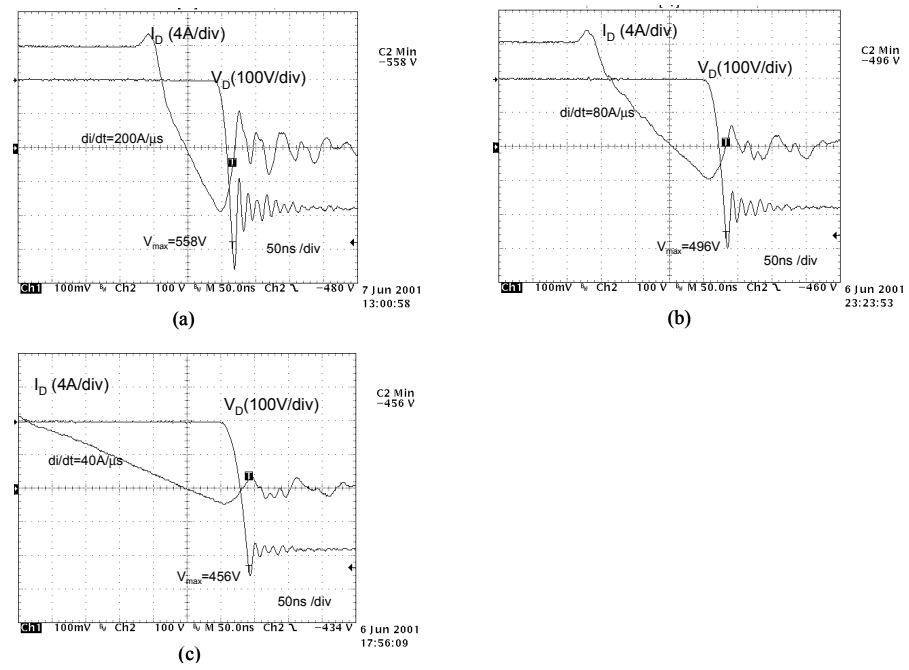


Fig. 3.12. Measured waveforms showing the reverse-recovery of PHRP860 (at 55°C).

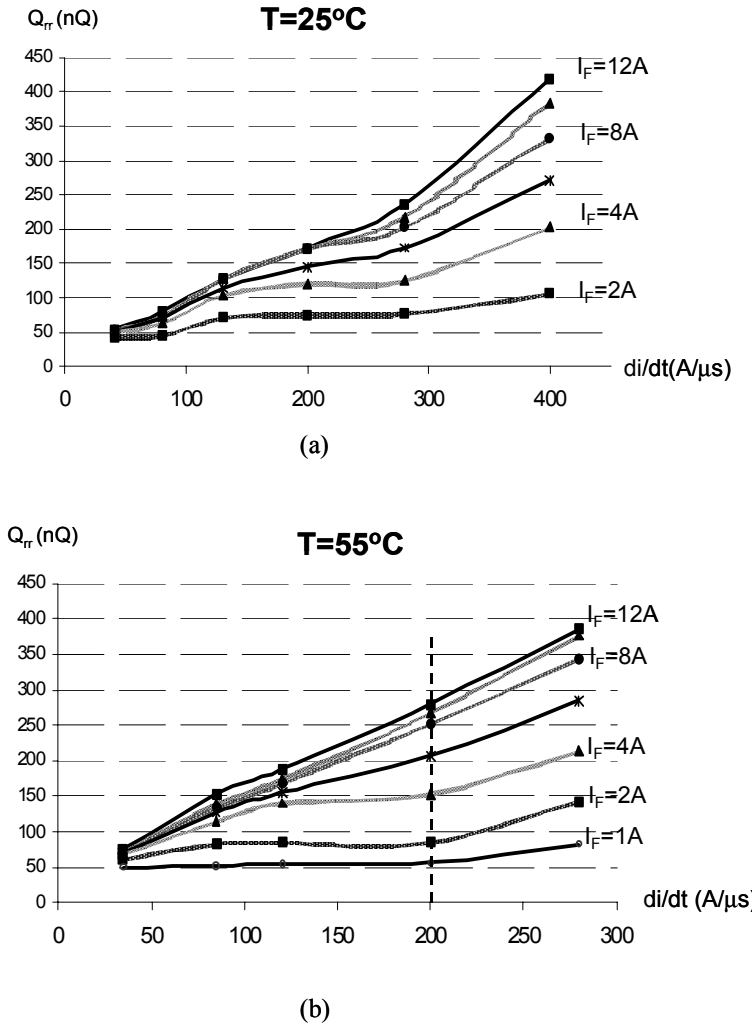


Fig. 3.13. Measured reverse-recovery charge:
(a) at room temperature (25°C) and (b) under an ambient temperature of 55°C.

For the silicon rectifiers, the preferred *di/dt* of the rectifier turn-off rate is less than 100 A/µS. Eq. 3-7 shows that the *di/dt* of rectifier D_o during its turn-off is roughly determined by V_o / L_k when N is close to one. The output voltage is generally 400 V for a boost converter with

universal-line input. A leakage inductance of about 5 μH to 10 μH is sufficient to achieve the desired improvement.

Rectifier D_o has a junction capacitor. This parasitic capacitor and the leakage inductor form a resonant tank. Due to the undesirable resonance between the leakage inductor and the parasitic capacitor of D_o after switch S turns on, a small snubber circuit for D_o is generally necessary to avoid extra voltage stress on D_o. It also should be mentioned that the so-called di(rec)M/dt of a fast-recovery rectifier has a significant effect on the voltage stress of D_o [C3], since the maximum voltage stress of the rectifier D_o is given by Eq. 3-8:

$$V_{Do} = V_o + L_k \cdot di(rec)M / dt \,. \qquad \text{Eq. 3-8}$$

A 500W CCM DC-DC boost converter operating at 100KHz was built to verify the proposed concept. The experimental set-up is given in Fig. 3.14. Fig. 3.15 shows the current waveforms through the two rectifiers with the maximum current, which is the worst case. As can be seen, the current begins to shift from rectifier D_a to the output rectifier D_o. The current through D_a is reduced to zero before switch S turns on, and D_a is naturally recovered before S turns on.

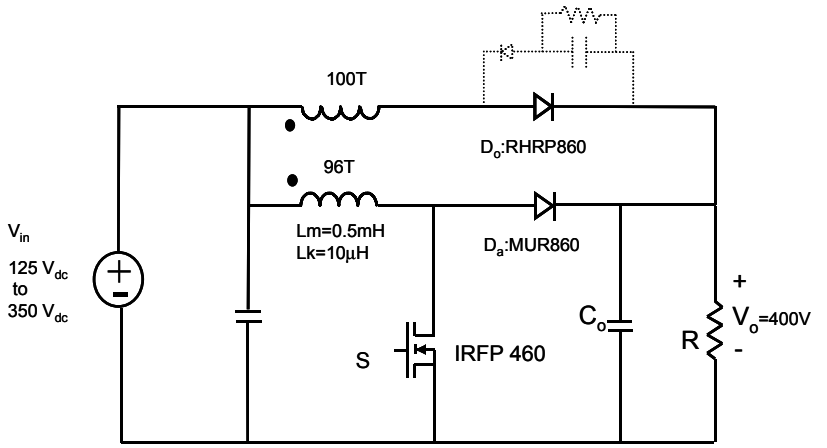


Fig. 3.14. Experimental set-up for DC-DC boost converter.

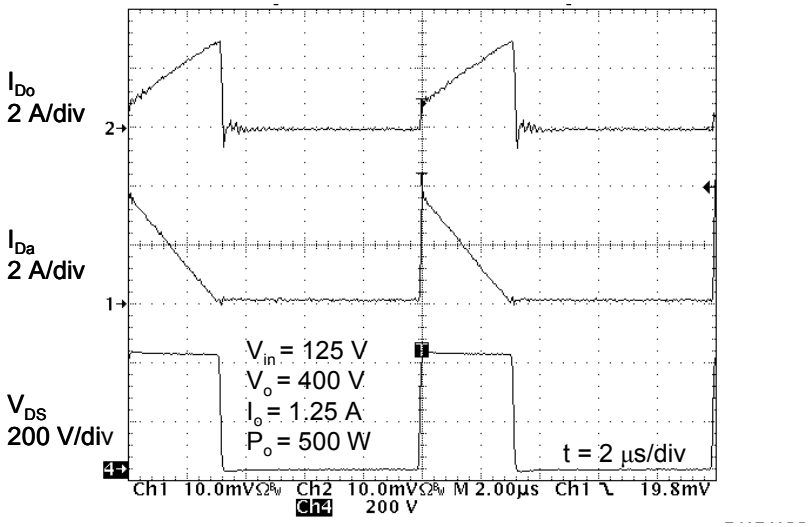


Fig. 3.15. Completed current shift before switch S turns on when V_{in} = 125 V_{dc}

Fig. 3.16 shows the significant performance improvement attained by controlling the rectifier di/dt during its turn-off. As illustrated, not only is the reverse-recovery peak current reduced, but also the time at which the reverse-recovery current appears is delayed. The voltage of switch V_{DS} is already zero when the reduced reverse-recovery current appears. Therefore, switching loss related to this reverse-recovery current is dramatically reduced.

Fig. 3.17 shows that the maximum voltage stress for the rectifier D_o is 505 V when D_o is RHRP860. Therefore, this 600V rectifier could safely be used. However, when D_o is MUR860, the maximum voltage stress is about 600V because the RHRP860 has smaller *di(rec)M/dt*.

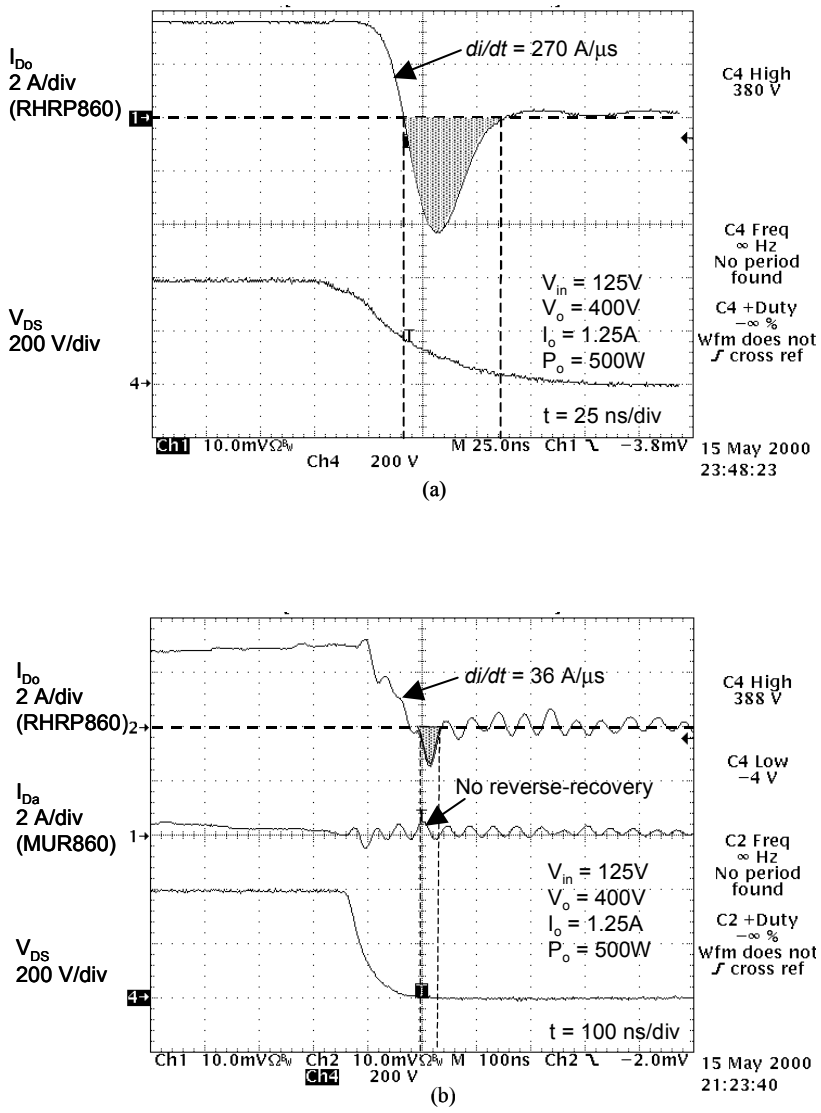


Fig. 3.16. Effect comparisons:
(a) severe reverse-recovery problem for hyper-fast rectifier RHRP860 (trr< 30 ns) without controlled di/dt; and
(b) not only is the reverse-recovery current reduced, but the current appearance is also delayed.

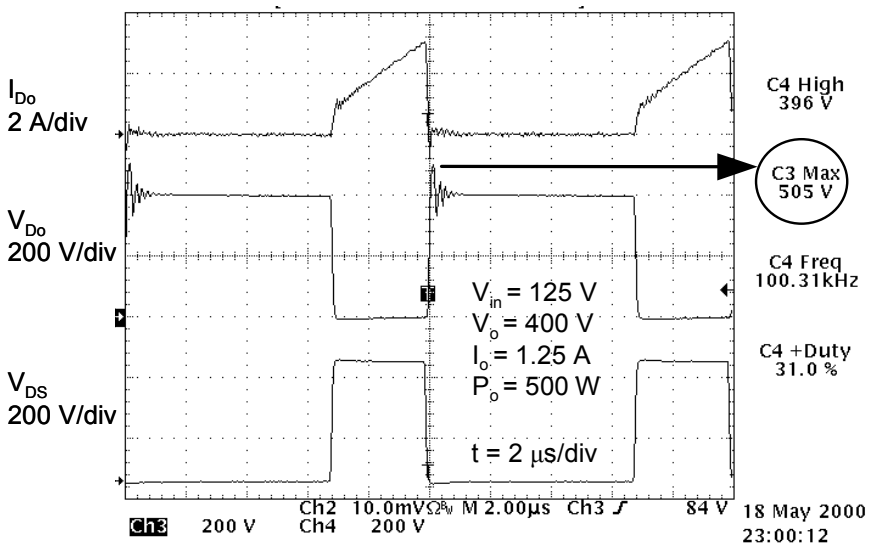


Fig. 3.17. The voltage stress of rectifier D_o.

The maximum 2% efficiency improvement is obtained at the minimum input voltage, where the reverse-recovery losses are the most significant. The efficiency improvement continues, but the improvement amplitude decreases to 0.5% at the maximum input voltage, as shown in Fig. 3.18.

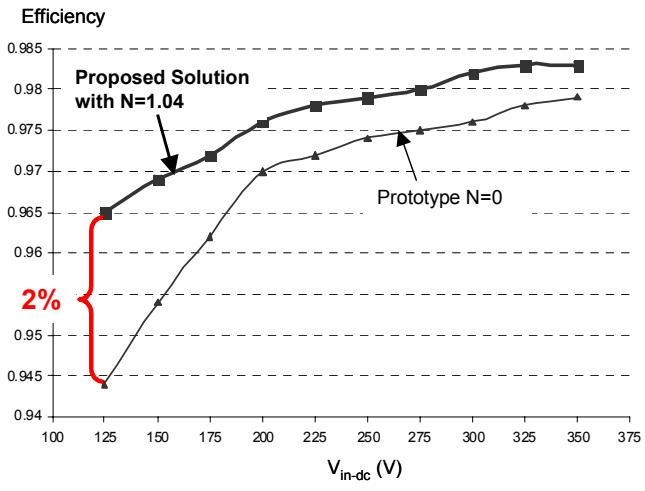


Fig. 3.18. Efficiency measurements of the DC-DC converter

3.4. Improved Topologies for the Front-End PFC Applications

The CCM boost converter has been widely used as the front-end PFC converter for telecom and server applications. Table 3.2 shows the specifications of the state-of-the-art front-end converters.

Table 3.2. State-of-the-art front-end converters.

Product	**Profile** (Inch)	**Cooling Method**	**Po (W)**	**Power Density** ($W/inch^3$)	**Input Voltage** (V_{ac})	**Eff** (%)	**Power Factor**
A	2.6*7.9*13.8	Fan	1200	4.30	90-264	?	>0.99
B	3.35*6.75*11.5	Fan	1200	4.62	90-264	>86	>0.99
C	2.5*7*10	Fan	1000	5.72	90-264	?	>0.99
D	2.74*4.9*12.5	Fan	1000	5.96	90-264	>89	>0.98
E	1U*6*12	Fan	1200	9.50	90-264	?	0.99@115V 0.95@230V
F	2.6*8.7*10.4	Natural	1000 (500W @ $90V_{ac}$)	4.30	150-300	>91	>0.99

As can be seen from the table, some applications require constant output power with universal input voltage, and some applications degrade the output power at low-line input voltage. The major challenge for improving the CCM boost performance is thee rectifier reverse recovery. In this section, the proposed converter will be demonstrated to achieve a significant performance improvement for front-end PFC applications.

The output power in such applications is generally around 1KW to 1.2KW. On one hand, the leakage inductance of the coupled inductor controls the di/dt of the output rectifier to alleviate the reverse-recovery problem; on the other hand, the leakage inductance and the parasitic capacitance constitute a resonant tank. The resonance induces severe voltage stress in the output rectifier. Although utilizing an RCD snubber can reduce the voltage stress of the output rectifier, the loss and thermal handling in the sunbber circuit becomes another problem. The solutions of this parasitic resonance will be addressed.

3.4.1. Coupled-Inductor Converter with a Lossless Snubber

In this section, the proposed converter with a lossless snubber in the output rectifier is analyzed and experimentally verified.

3.4.1.1. Topology and Operation Analysis

Rectifier D_o has a junction capacitor. This parasitic capacitor and the leakage inductor form a resonant tank. Due to the undesirable resonance between the leakage inductor and the parasitic capacitor of D_o after switch S turns on, a snubber circuit for D_o is generally necessary to avoid extra voltage stress on D_o. An RCD snubber can be used for applications with relatively low power. For a front-end converter with about a kilowatt of output power, the excessive loss in the RCD snubber deteriorates the thermal handling of the snubber circuit. A lossless snubber can be added by using the flying capacitor concept [C7]. The lossless snubber has two diodes and a small capacitor, as shown in Fig. 3.19.

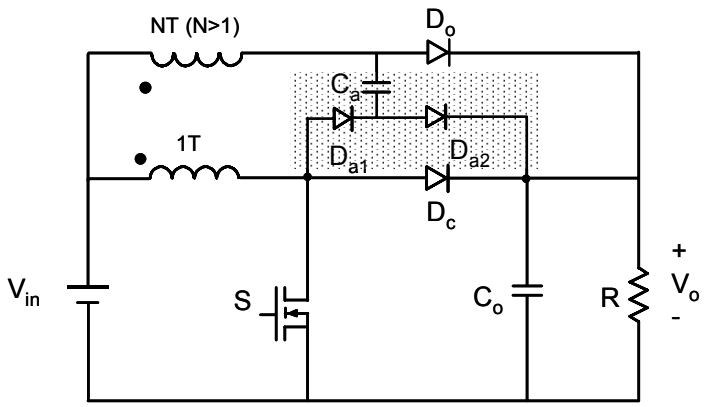


Fig. 3.19. The proposed converter with a lossless snubber for the stress reduction of D_o.

Fig. 3.20 andFig. 3.21 illustrate the topological stages and the key waveforms of the proposed converter with a lossless snubber.

Compared to the original proposed converter, three new stages (c, d and h) appear. The voltage stress of output rectifier D_o is dramatically reduced because of this clamp circuit.

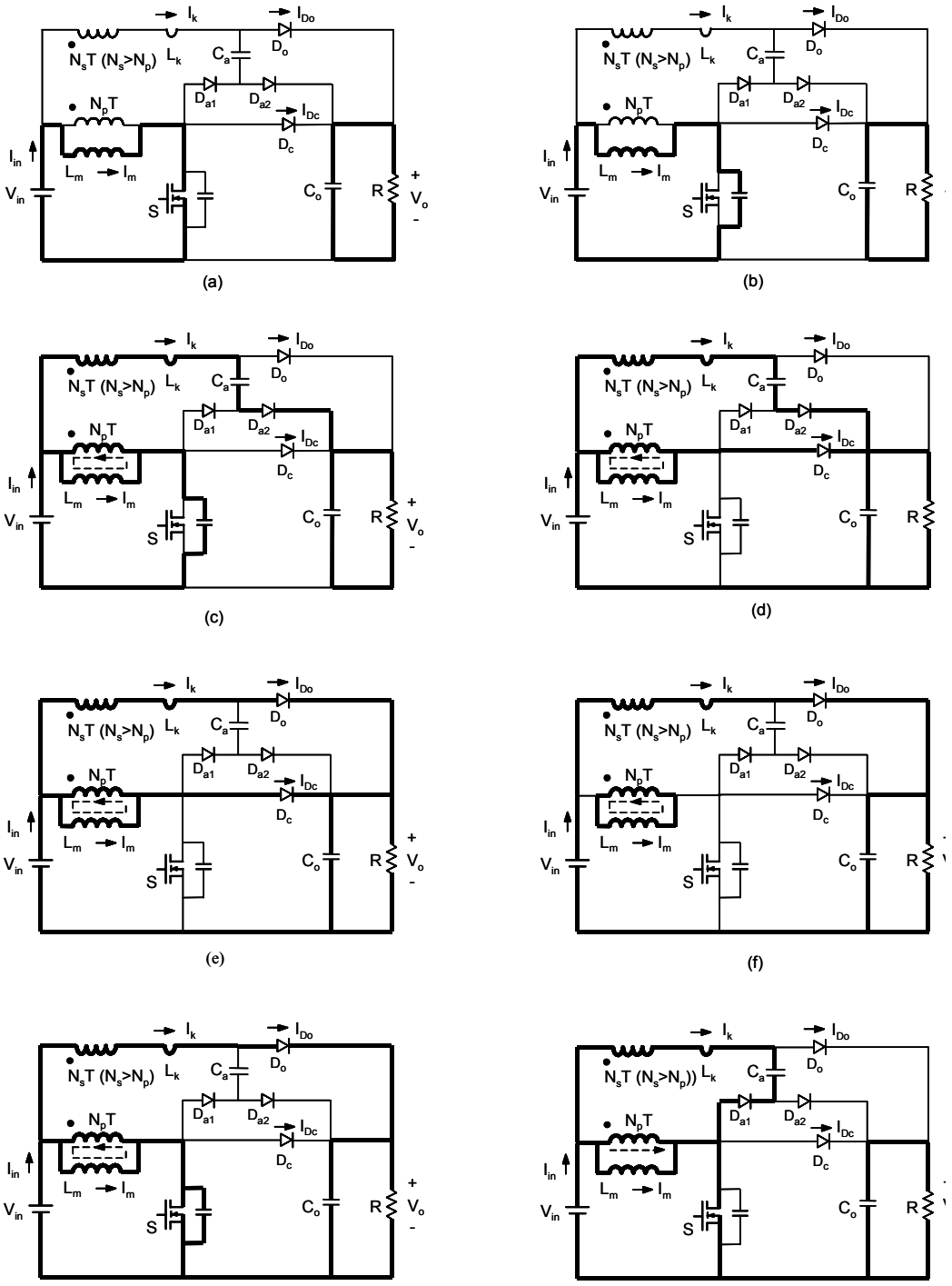


Fig. 3.20. Eight operation modes of the proposed converter with a lossless snubber.
(a) [T_0, T_1]; (b) [T_1, T_2]; (c) [T_2, T_3]; (d) [T_3, T_4]; (e) [T_4, T_5]; (f) [T_5, T_6]; and (g) [T_6, T_0].

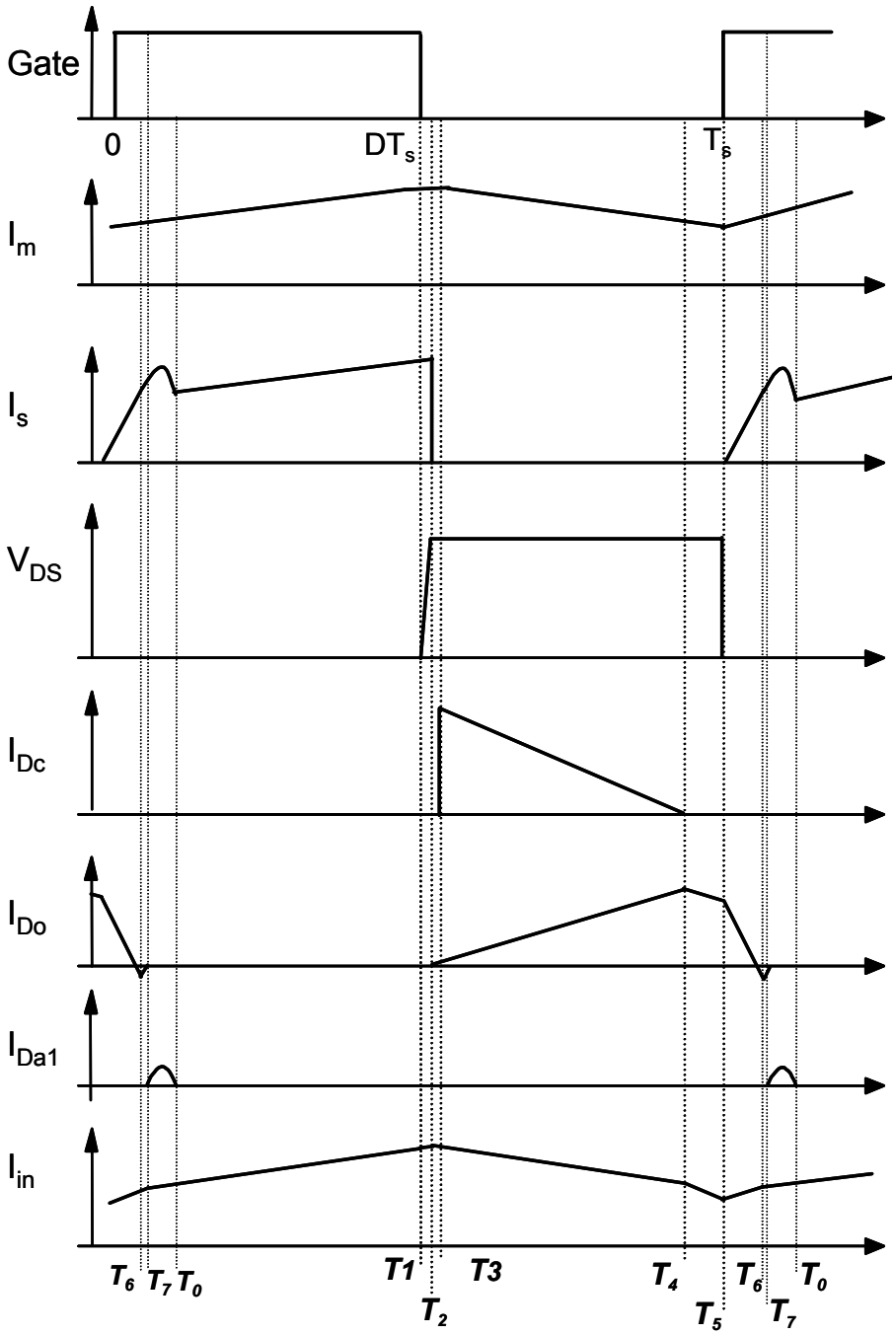


Fig. 3.21. Key waveforms of of the proposed converter with a lossless snubber.

The design procedure for the PFC applications is different from that of the DC-DC applications because the line voltage and the input current are variable. The design details will be discussed here.

3.4.1.2. Design of the Turns Ratio for PFC Applications

Compared to the DC-DC application, the input current changes with the input line voltage. Therefore, the design for the PFC applications is more complicated than that for the DC-DC applications. The duty ratios of CCM boost converters for PFC vary with the line variations. Fortunately, the current is small when the duty ratio is large at the input voltage near the zero-crossing point. Although switch *S* has a shorter turn-off time period during which the current must be shifted to the new branch, the current is also small. When the input voltage is close to the peak area, the CCM boost converter has large rectifier forward current and small duty ratios. Therefore, more time is available for the current through D_a to be shifted. In other words, no large *N* is needed to shift the current. Section IV will address the design issues in detail.

As in the previous discussion, the value of *N* is close to one. To simplify the practical design, the slight increase of the voltage gain of the proposed converter is ignored. Therefore, the current through output rectifier D_a must be reduced to zero during the turn-off period of switch *S*, which is given by Eq. 3-9:

$$T_{off} = (1-d)\cdot T_s = \frac{V_{in\_pk}\cdot \sin(\omega t)}{V_o}\cdot T_s, \qquad \text{Eq. 3-9}$$

where T_s is the time period of a switching cycle, V_{in_pk} is the input peak voltage, and V_o is the output voltage.

At time T_2, the current I_{Do_T2} of the output rectifier D_a is defined by Eq. 3-10:

$$I_{Do\_T2} = \frac{2P_o}{V_{in\_pk}} \cdot \sin(\omega t), \qquad \text{Eq. 3-10}$$

where P_o is the output power.

Substituting Eq. 3-5, Eq. 3-9 and Eq. 3-10 into Eq. 3-6 gives the minimum turns ratio N, which can be expressed by Eq. 3-11:

$$N \approx \frac{V_o - V_{in\_pk} \cdot \sin(\omega t) + 2P_o \cdot \dfrac{V_o}{{V_{in\_pk}}^2} \cdot L_k \cdot F_s}{V_o - V_{in\_pk} \cdot \sin(\omega t)}, \qquad \text{Eq. 3-11}$$

where ω is the angular frequency of the input line voltage, and F_s is the switching frequency.

For a given output power, the turns ratio is a function of leakage inductance L_k. The physical meaning of this key design equation is quite simple: The L_k determines the preferred rectifier current rate *di/dt* during its turn-off, while the minimum N guarantees complete current shifting so that the original rectifier D_a can be naturally recovered. The worst case occurs at the line peak. Fig. 3.22 shows the relationship between the N and the line variations for a 1KW CCM boost converter at low line input. This converter requires that N be at least 1.07 in order to control the *di/dt*, which is about 100 A/μS.

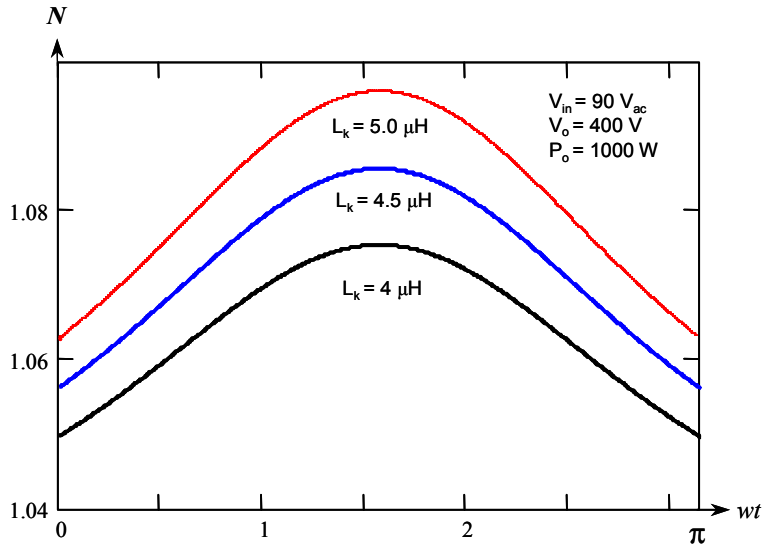


Fig. 3.22. Turns ratio for complete current steering.

3.4.1.3. Control of the Leakage Inductance

For the proposed topology, the rectifier di/dt is controlled by the leakage inductor. The leakage inductance plays a crucial function in alleviating the rectifier reverse recovery. Therefore, finding a method to control the leakage inductance and determining how the topology is sensitive to the variations of the leakage inductance are important. Fig. 3.23(a) shows a toroidal core with a path length of l_m. Fig. 3.23(b) shows the cross-section of the core with two coupled windings. Fig. 3.23(c) shows the structure if the core is cut and then stretched. Assume the area between the two coupled windings is A, as shown in Fig. 3.23(b). The leakage inductance of this structure can be given by:

$$L_k = \frac{\mu_0 \cdot N^2 \cdot A}{l_m}. \qquad \text{Eq. 3-12}$$

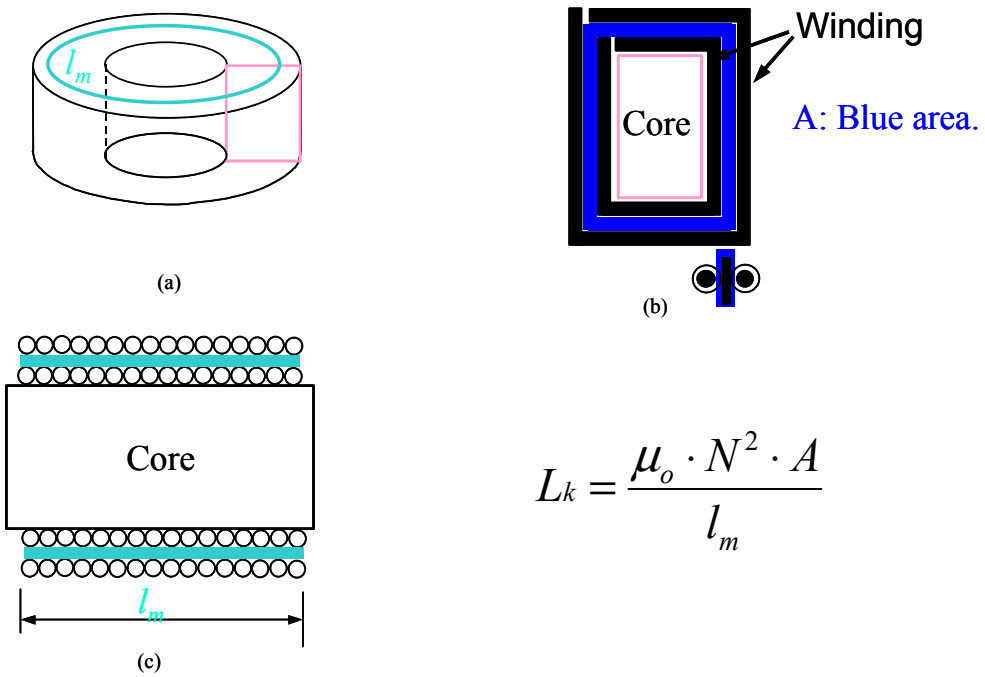
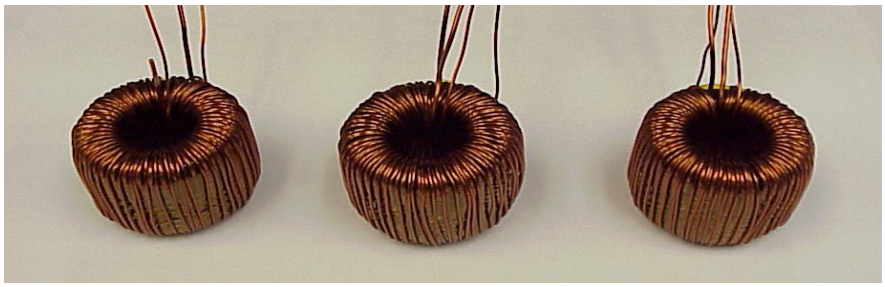


Fig. 3.23. Factors affecting the leakage inductance of the coupled inductor.

It can be found that A is the only controllable factor that can change the leakage inductor of this coupled inductor. Adding isolation tape is an effective way to change the leakage inductance. Three coupled inductors are made by hand to check the variation of the leakage inductance. We try to get 4 μH of leakage inductance in all three inductors, as shown in Fig. 3.24. The primary winding is one-layer with 48 turns and the secondary winding is 50 turns. As can be seen, the leakage inductance can be varied from 3.65 μH to 4.08 μH.



L = 372.2 μH *L = 371.3 μH* *L = 366 μH*
Lk = 3.9 μH *Lk = 4.08 μH* *Lk = 3.65 μH*

Fig. 3.24. Three coupled inductors.

3.4.1.4. Sensitivity of the Complete Current Steering to the Leakage Inductance

The leakage inductance will have some variation during the manufacture process, so the next step is to determine how sensitive the complete current steering is to the variation. Fortunately, the proposed topology has a high tolerance to the leakage inductance variation in order to guarantee the complete current steering. For the given 48 turns of the primary winding, the secondary nominal turns can be changed from 1.065 to 1.085. The secondary winding is 52 turns if the leakage inductance varies from 4 μH to 4.5 μH. The number of secondary turns is not sensitive to the variation of leakage inductance.

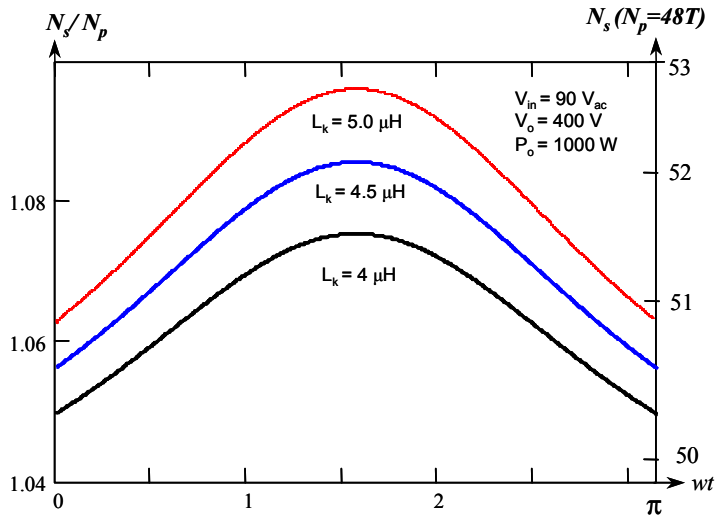
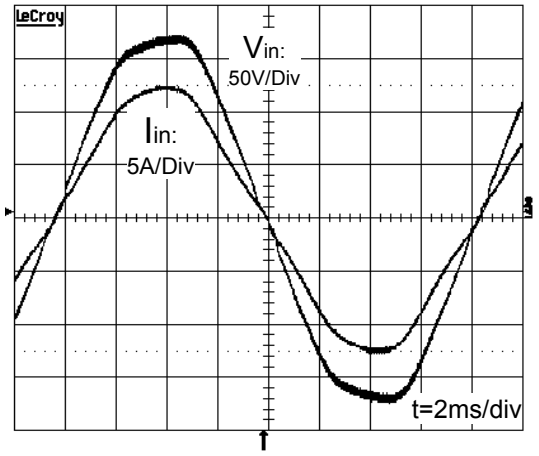


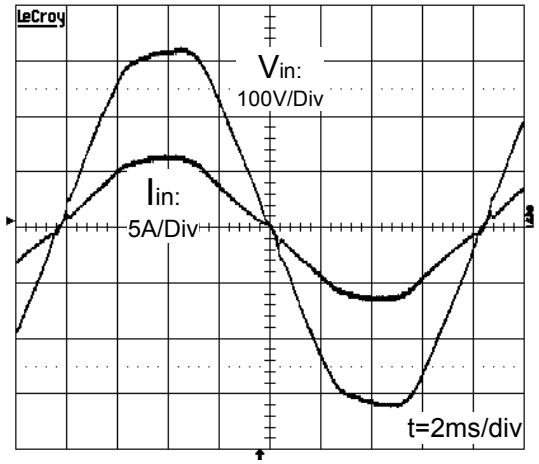
Fig. 3.25. Sensitivity to the leakage inductance.

3.4.1.5. Experimental Results

Based on the design procedure, a 1KW prototype has been built and tested to verify the performance improvement of the proposed converter in the front-end PFC applications. Fig. 3.26(a) and (b) show the input voltage and current waveform at low line and high line input voltage, respectively. As can be seen from the waveforms, the input current has no distortion.



(a)



(b)

Fig. 3.26. Input voltage and current waveforms at low line and high line input.
(a) V_{in}=120V and (b) V_{in}=230V.

Fig. 3.27(a) shows the current of the two coupled windings. The current-steering process during the switching turn-off time period can be observed. The current is steered from the branch with N_p to the branch with N_s just before the switch turns on. Rectifier D_a is recovered naturally. The reverse-recovery problem is alleviated because the current decrease rate of D_o is controlled at bout 100A/μs, shown in Fig. 3.27(b).

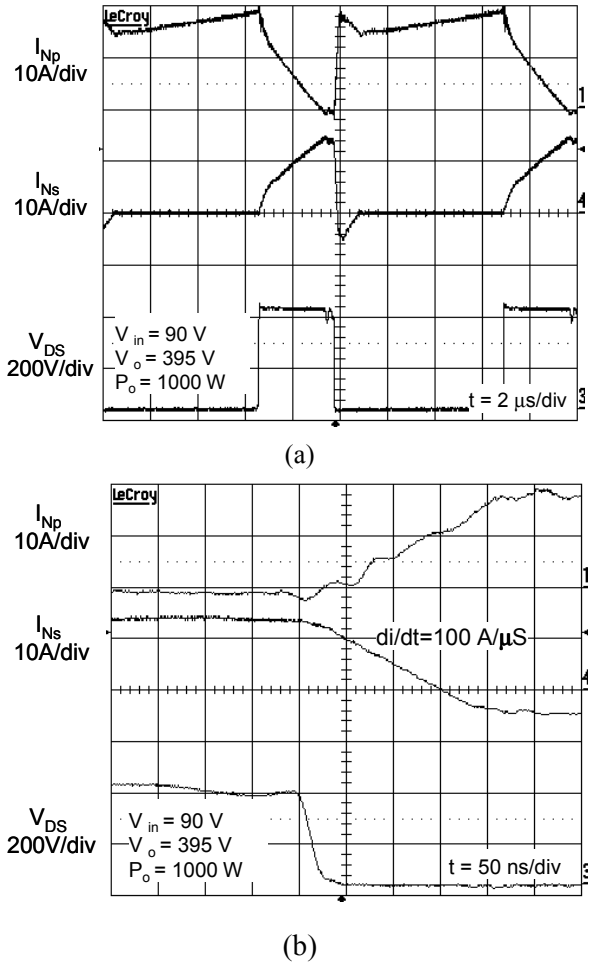


Fig. 3.27. Current steering of the coupled inductor:
(a) waveforms with the time scale 2µs/div and (b) enlarged waveforms with time scale 50ns/div.

Due to the effectiveness of the snubber, the voltage stress has been dramatically reduced to about 450V, as shown in Fig. 3.28.

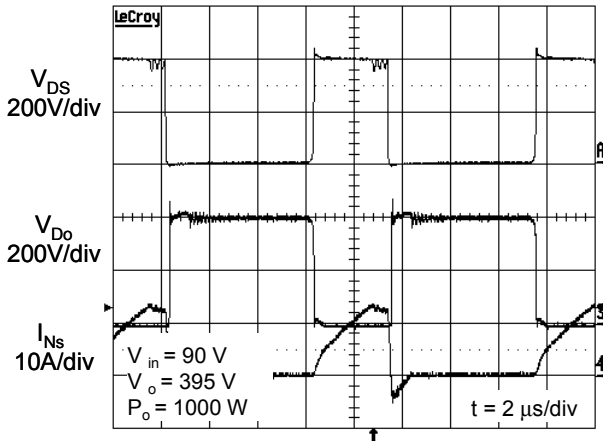


Fig. 3.28. Reduced voltage stress of the output rectifier.

The measured efficiency of the proposed converter is shown in Fig. 3.29. The hard-switching version has a thermal runaway problem when the input voltage is decreased to 110V. The proposed converter with an RCD snubber can work at voltage as low as 100V with a significant performance improvement. The proposed converter can achieve universal-line operation with the best efficiency.

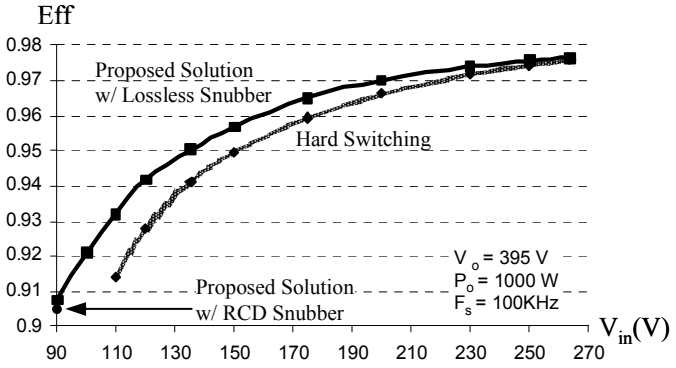


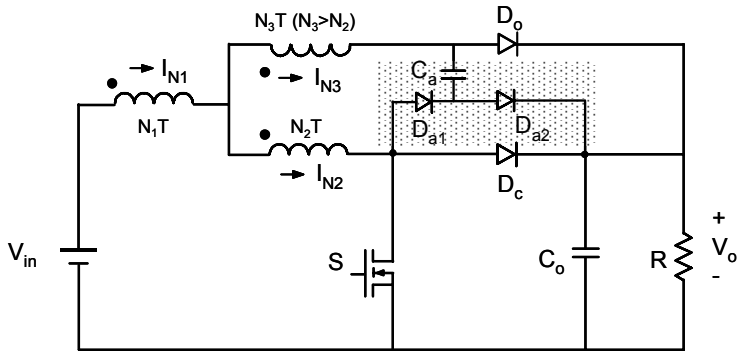
Fig. 3.29. Measured efficiency.

3.4.2. Coupled-Inductor Boost Converter with Reduced Winding Loss

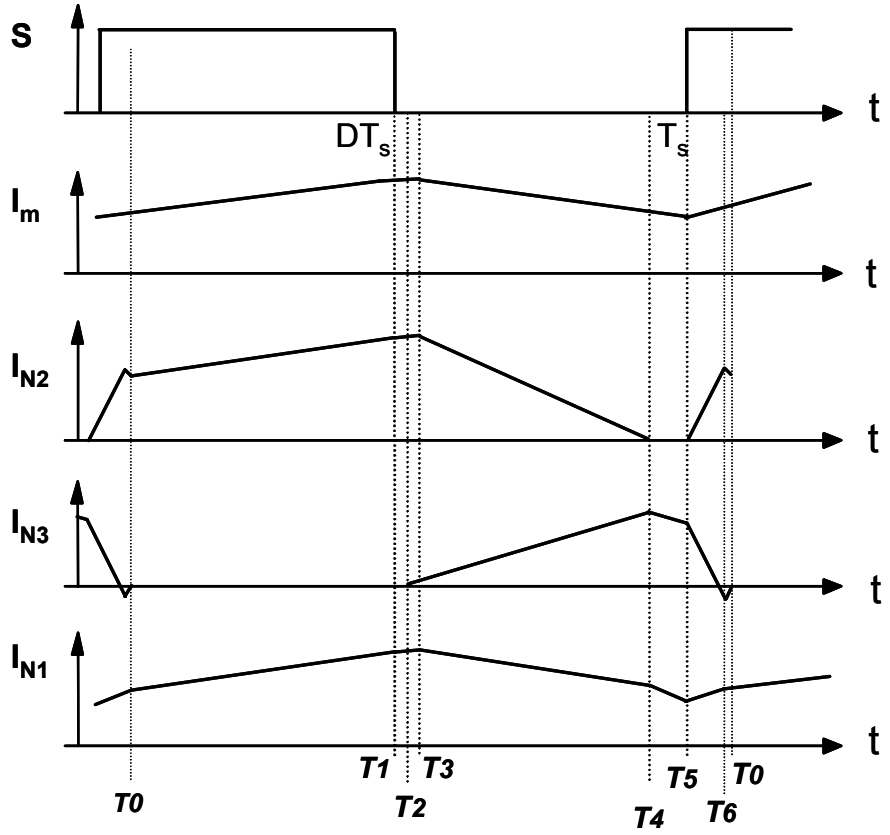
As can been see from Fig. 3.27(a), the magnetizing current alternates between the two coupled windings. The AC components of the coupled winding can result in large loss in the coupled inductor at high-frequency operation. To overcome this drawback, an improved topology structure with the same concept is developed, and is shown in Fig. 3.30(a). The major idea is that the CCM input current can flow through the most turns of winding N_1, while windings N_2 and N_3 (with much fewer turns of the coupled inductor) are used to alleviate the rectifier reverse recovery. Fig. 3.30(b) shows the key waveforms of the operation of the improved version. It is obvious that the CCM input current I_{in} flows through winding N_1, and only N_2 and N_3 are used for the current-shifting purpose. By utilizing this structure, the inductor loss can be reduced.

As to the design of the boost inductor with three windings, the windings on the first layer are used for winding N_1. Two coupled windings with much fewer turns on the second layer should be located far away from each other in order to achieve sufficient leakage inductance. The turns ratio N in Eq. 3-11 is defined as Eq. 3-13 for the improved version:

$$N = \frac{N_1 + N_3}{N_1 + N_2}. \qquad \text{Eq. 3-13}$$



(a)



(b)

Fig. 3.30. Improved version with the reduced inductor winding loss:
(a) circuit diagram and (b) key waveforms.

The inductor has the following number of turns: N_1=45T, N_2=3T, and N_3=6T. Fig. 3.31 shows that a CCM current flows through the winding N1. The loss in the coupled winding is reduced.

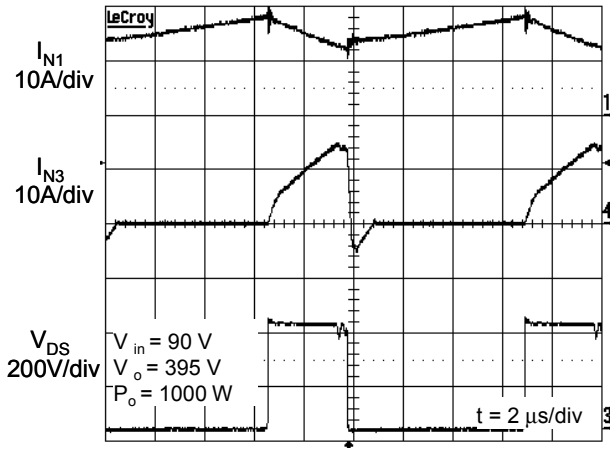


Fig. 3.31. CCM current in winding N_1.

Fig. 3.32 shows the measured efficiency. There is an improvement of about 0.6% at 90V input voltage.

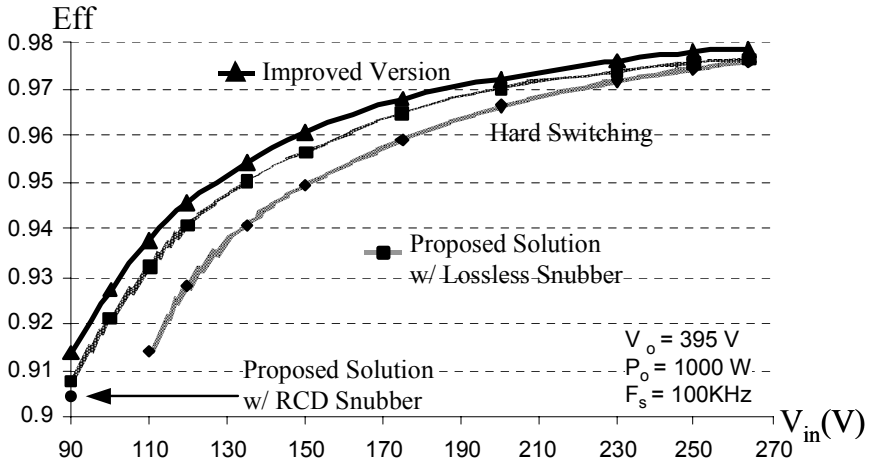


Fig. 3.32. Measure efficiency.

3.4.3. Coupled-Inductor Converter with Minimal Voltage Stress

The proposed snubber only achieves the turn-on snubber function by suppressing the diode reverse-recovery current. The turn-off of the device is still under the hard-switching condition. Besides that, there is still an undesirable resonance between the output capacitance of either the active switch or the diode and the equivalent resonant inductor. The ringing causes the excessive voltage stress over the semiconductor devices and affects the circuit operation. A new lossless snubber configuration for the boost converter is proposed by Wei Dong [C22]. It further enhances the concept of the turn-on and turn-off snubber function. One coupled inductor is used to help reduce both turn-on and turn-off losses. During the switch's off period, the coupled inductor shifts the current from the original output diode to the auxiliary output diode. Therefore, the diode reverse-recovery loss is much reduced in a way that is similar to the proposed converter. After the switch is on, the coupled inductor can charge the snubber capacitor voltage to the output voltage level. Consequently, the snubber capacitor can effectively slow the voltage rising time at the switch's turn-off and reduces the turn-off loss accordingly. The reduced dv/dt is also expected to alleviate the EMI noise. The proposed snubber circuit has two interesting features: First, all devices block the voltage not exceeding V_o and no additional clamping circuit is required in the actual implementation; Second, it requires small number of added components. It adds one coupled inductor, three auxiliary diodes and one snubber capacitor. Although there is one more diode voltage drop during the switch's off period, as compared with the conventional hard-switching boost converter, the resultant extra conduction loss is not significant when compared with the switching loss reduction. Fig. 3.33 andFig. 3.34 show the operation modes and key waveforms.

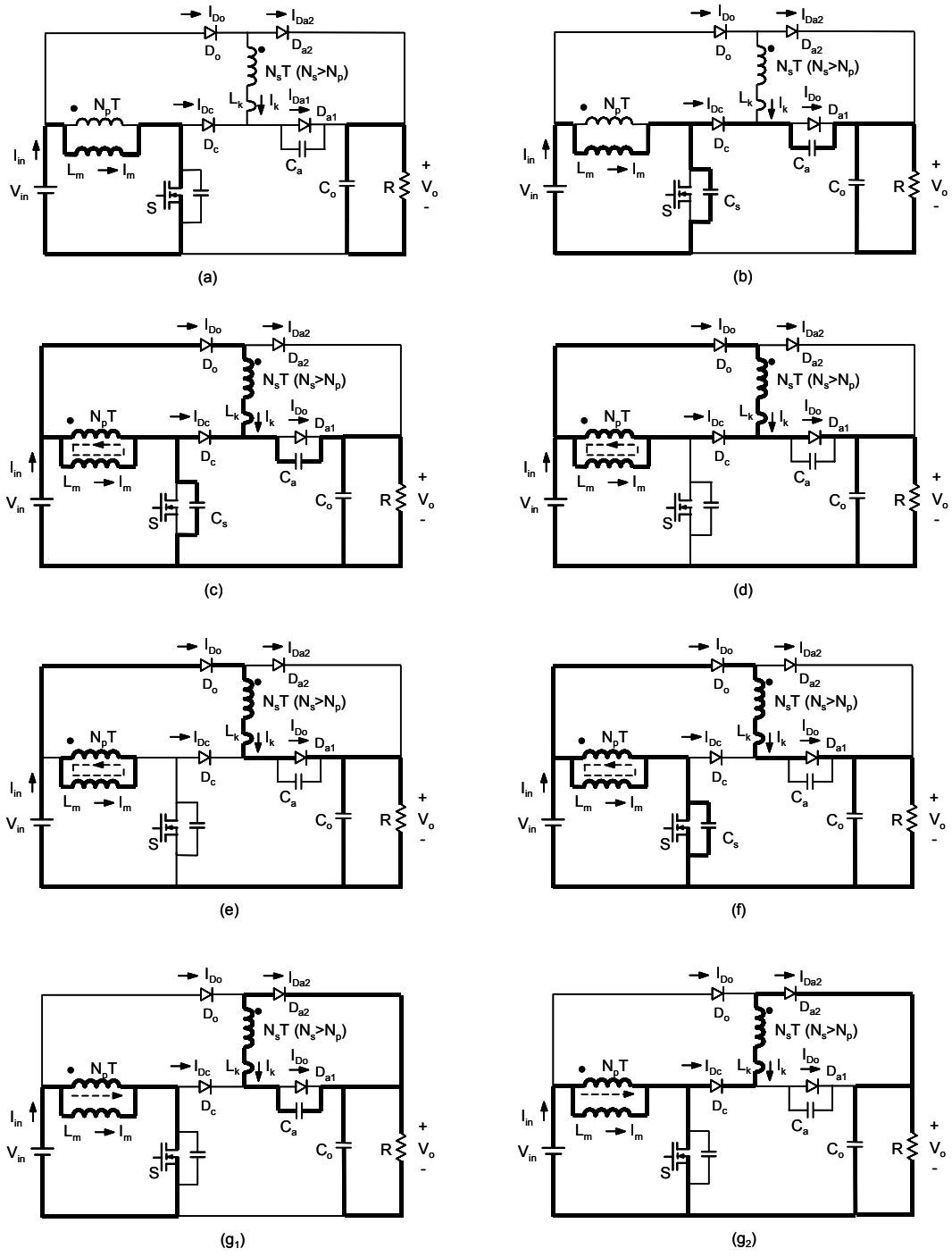


Fig. 3.33. Operation modes of the converter with minimum voltage stress: (a) [T_0, T_1]; (b) [T_1, T_2]; (c) [T_2, T_3]; (d) [T_3, T_4]; (e) [T_4, T_5]; (f) [T_5, T_6]; (g_1) mode I during [T_6, T_0] and (g_2) mode II during [T_6, T_0].

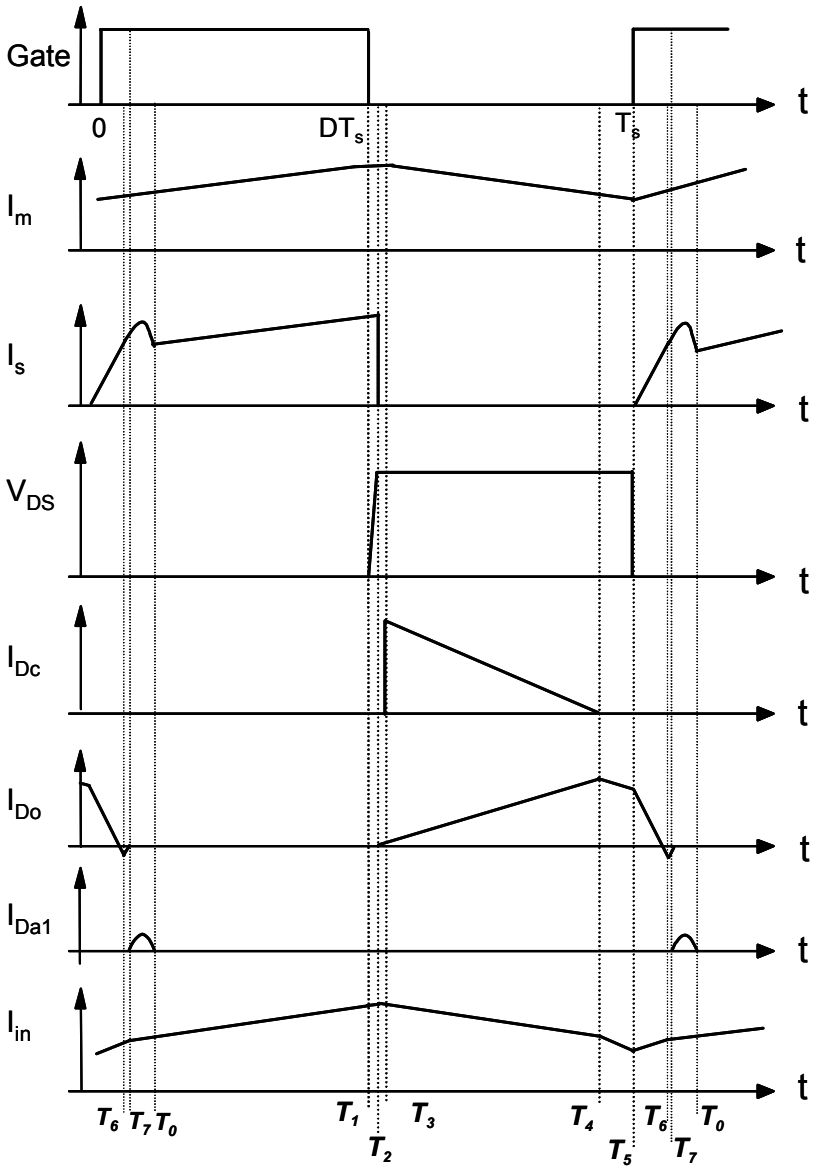
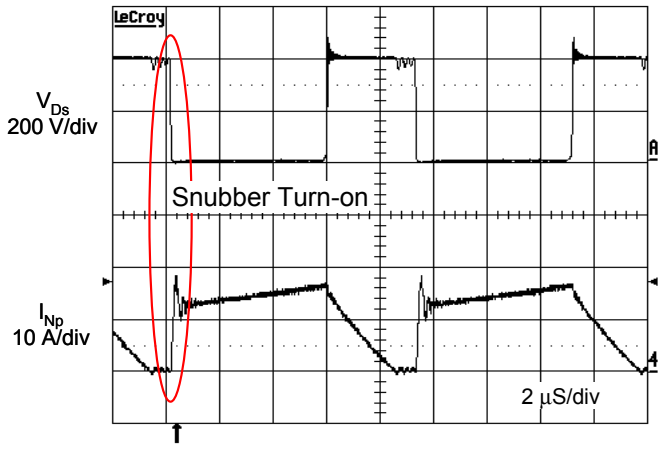
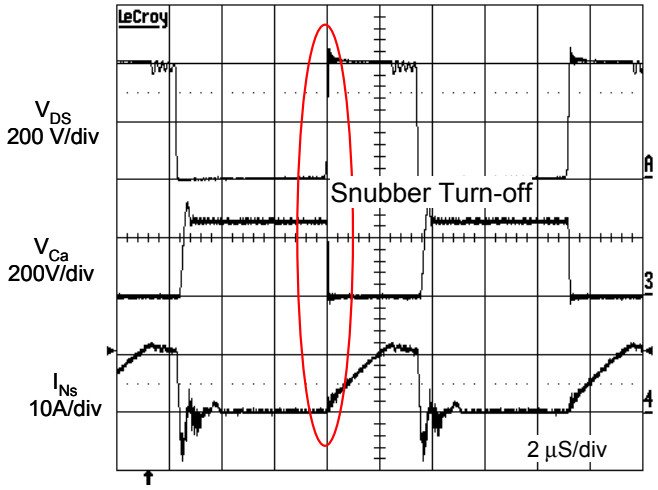


Fig. 3.34. Key waveforms.

Fig. 3.35 shows the experimental results during the switch turn-on and turn-off time periods. As can be seen, the rectifier reverse-recovery problem is alleviated when switch turns on, and the voltage increase slope is reduced when S turns off.



(a)



(b)

Fig. 3.35. Experimental results.
(a) snubber turn-on and (b) snubber turn off.

The fast recovery diode D_o in the alternative branch only needs to block V_o-V_{in}. Shown in Fig. 3.36(a), including the effect of the parasitics in the circuit, D_o blocks no more than 300 V after turning off at high current levels. D_c, with no current flowing before turning the switch on, blocks the output voltage V_o when the switch turns on, as can been from Fig. 3.36 (b). After D_o has recovered, the D_c voltage starts to slowly decrease. This implies that D_{a1} began to block the

voltage. Therefore, the D_c's series diode, D_{a1}, does not need to be a hyper-fast diode, which helps to further alleviate the effect of the extra conduction loss.

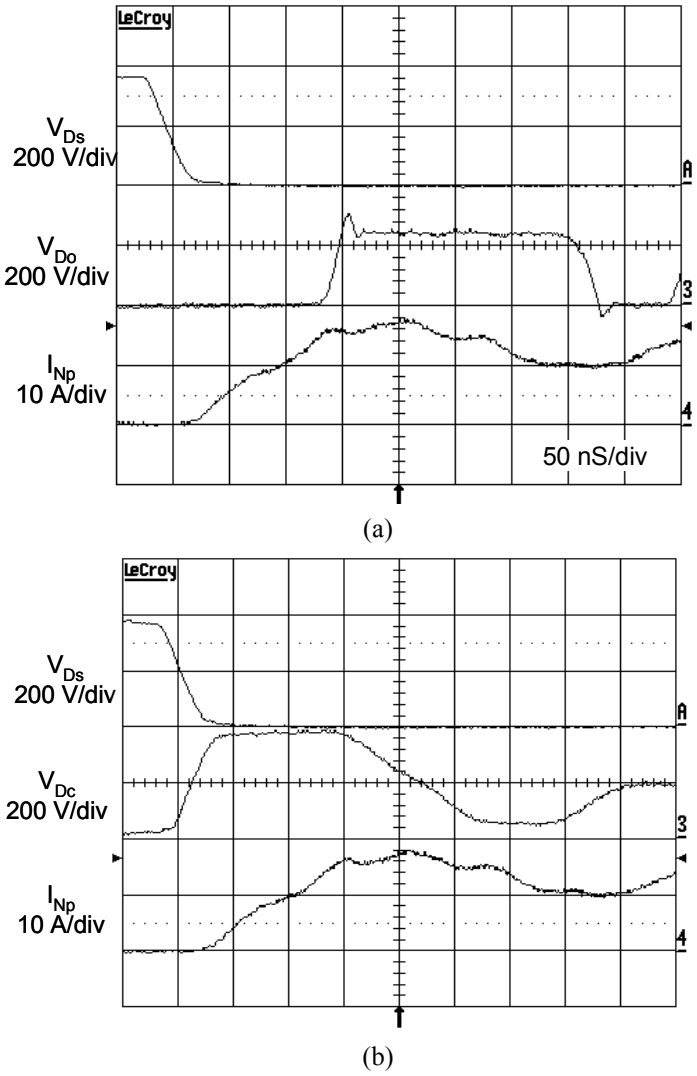


Fig. 3.36. Detailed waveforms of the rectifier voltage stress:
(a) D_o blocks the voltage V_o-V_{in} and (b) D_c blocks the voltage V_o.

Fig. 3.37 shows the measured efficiency. The efficiency improvement of the converter with minimal voltage stress is similar to that of the converter with reduced inductor winding loss. The

major reasons are that there are two diodes in series in the current path and the turn-off loss is not significant.

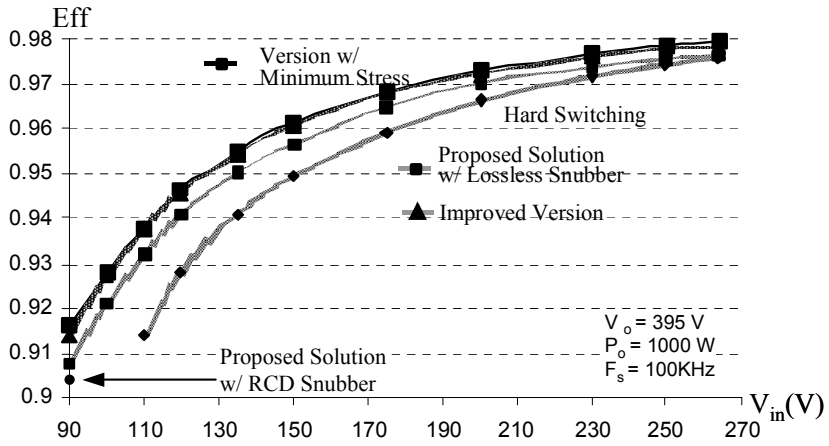


Fig. 3.37. Measured efficiency.

3.5. Development of the 1U High Power-Density Front-End Converter

CCM boost converters are used in front-end converters to achieve unity power factor for both telecommunications and computer servers. It is quite clear that the low-profile (1U) and high power-density front-end converter is emerging as a standard package. To achieve this target, the rectifier reverse-recovery problem is the major obstacle for the PFC front-end. In this section, the development of the 1U low-profile, high power-density front-end converter by utilizing the proposed solution is demonstrated.

The original operation frequency of the benchmark boost front-end is 60KHz. The downstream DC-DC converter is a half-bridge of a full-bridge converter with an input-voltage range of 350V to 400V. The reason is that the front-end converter needs to provide 10ms holdup

time during an AC outage. The normal operation condition for the DC-DC converter will be 400V of DC input. A pulse width modulation (PWM) converter, such as a half-bridge converter or a full-bridge converter, is unable to achieve optimized efficiency under a wide input-voltage range. The design tradeoff of the wide input-voltage range sacrifices the efficiency. Therefore, high power density of the front-end converter is impossible. The power density of the benchmark converter is about 4.3 W/inch^3.

Fig. 3.38 shows the targeted dimensions of the front-end converter. The profile of the converter is 1U, and the nominal output power is 1.2KW at V_{in}=150V. The power density is about 11 W/inch^3. The converter uses fan cooling instead of natural cooling.

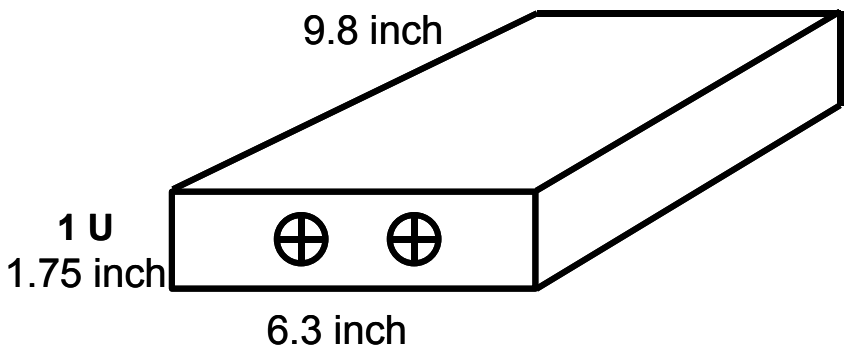


Fig. 3.38. Targeted dimensions of the front-end converter.

To meet these new challenges, new topologies and design techniques must be employed. For the boost front-end converter, increasing the operating frequency of the CCM boost converter with alleviated rectifier reverse-recovery problem is a viable option for reducing the volume and increasing the power density. For the downstream DC-DC converter, the holdup time requirement imposes a tradeoff of the efficiency of PWM converters, because a PWM converter

cannot achieve optimized efficiency under nominal operation conditions with a wide input voltage variation. To overcome this drawback, the LLC resonant converter has been comprehensively investigated [C26]. The LLC resonant converter can achieve the highest efficiency at high input voltage. Therefore, it is easy for the converter to be optimized under nominal operation conditions. However, the LLC resonant converter is beyond the scope of this research.

3.5.1. Design Guideline

Fig. 3.39 shows the relationship between the *N* and the line variations for a 1200W CCM boost converter at low line input. This converter requires that *N* be at least 1.05 in order to control the *di/dt*, which is about 100 A/μS.

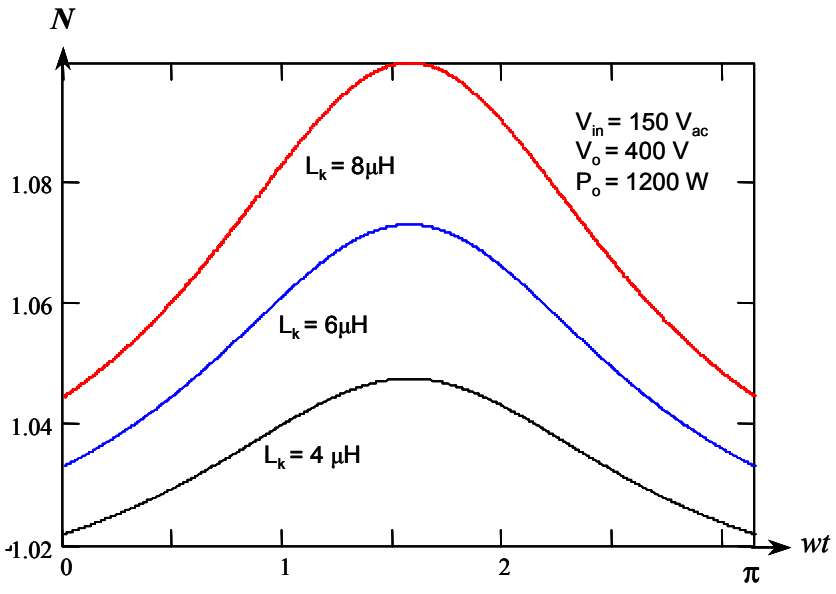
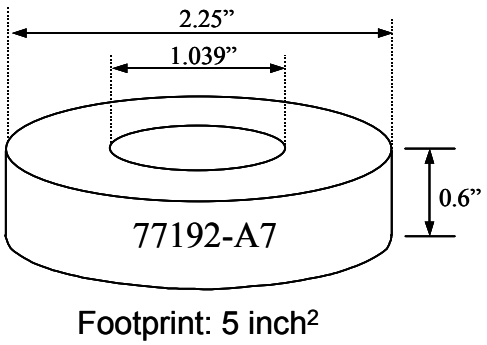


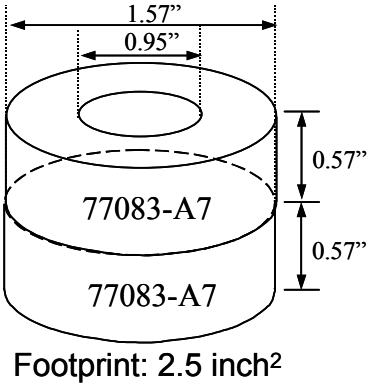
Fig. 3.39. Design graph to determine the turns ratio N.

Kool Mμ power cores are a product made by Magnetics Inc. The high flux saturation level and low core losses make Kool Mμ cores excellent for use in PFC circuits. Kool Mμ cores provide a higher energy-storage capability than can be obtained with gapped ferrites of the same size and effective permeability.

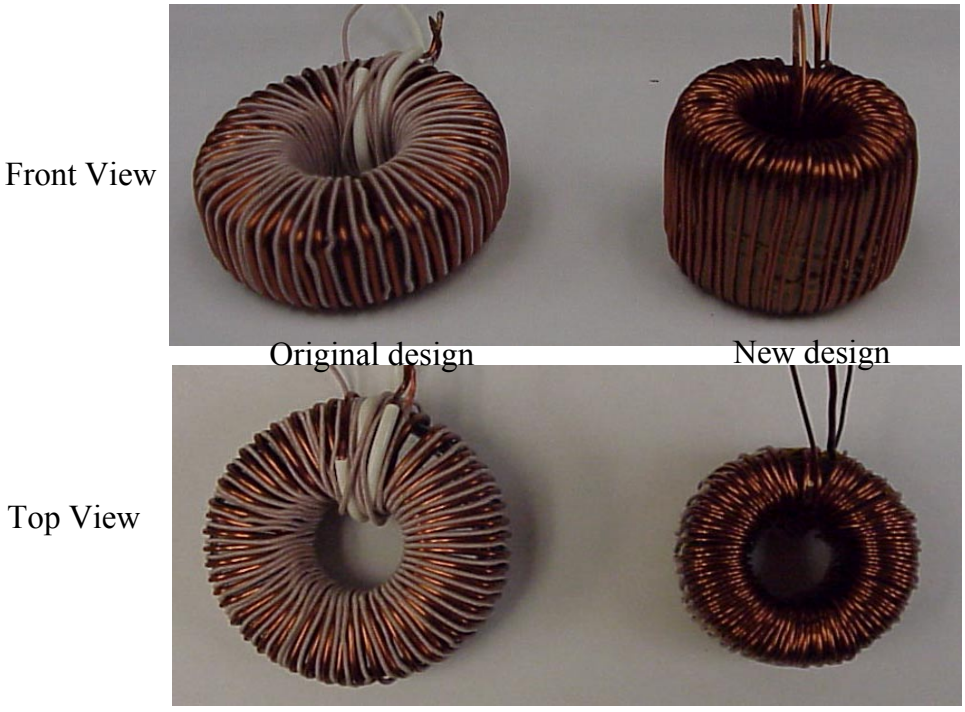
Following the design procedure, we can find that the 77192-A7 from Magnetics is appropriate for the application. For the front-end converter under study, high power density is a major concern. Not only the profile but also the footprint needs to be minimized. Although the 77192-A7 can meet application specifications, the large footprint and small profile are problematic. The component profile and the footprint should reach a tradeoff in order to achieve optimal result. Two 77083-A7 Kool Mμ cores are used for this application. Fig. 3.40(a)(b) compares the two designs from the standpoints of profile and footprint. Fig. 3.40(c) shows pictures of the two designs.



(a)



(b)



(c)

Fig. 3.40. Comparisons of the two designs:
(a) footprint by use of 77192; (b) footprint by use of 77083 and (c) comparison of two inductors.

3.5.2. High Power-Density Front-End Boost Converter with 1U Low Profile

Based on the design guidelines, a high power-density, low profile front-end converter is built. The circuit diagram parameters are shown in Fig. 3.41. The switching frequency is 100 KHz, the boost inductor is 0.3 mH under DC bias, and the measured leakage inductance is about 4 μH. The output power is 1200 W under the nominal operation condition in which V_{in}=230V_{ac}. The output power degrades to 600 W when the input voltage is between 90 V_{ac} and 150 V_{ac}.

Fig. 3.42 compares the measured efficiency of the proposed converter to the hard-switching boost converter. For the worst case, which is full power with 150V input, the efficiency improvement is about 0.5%, which is equivalent to a loss reduction of 7W.

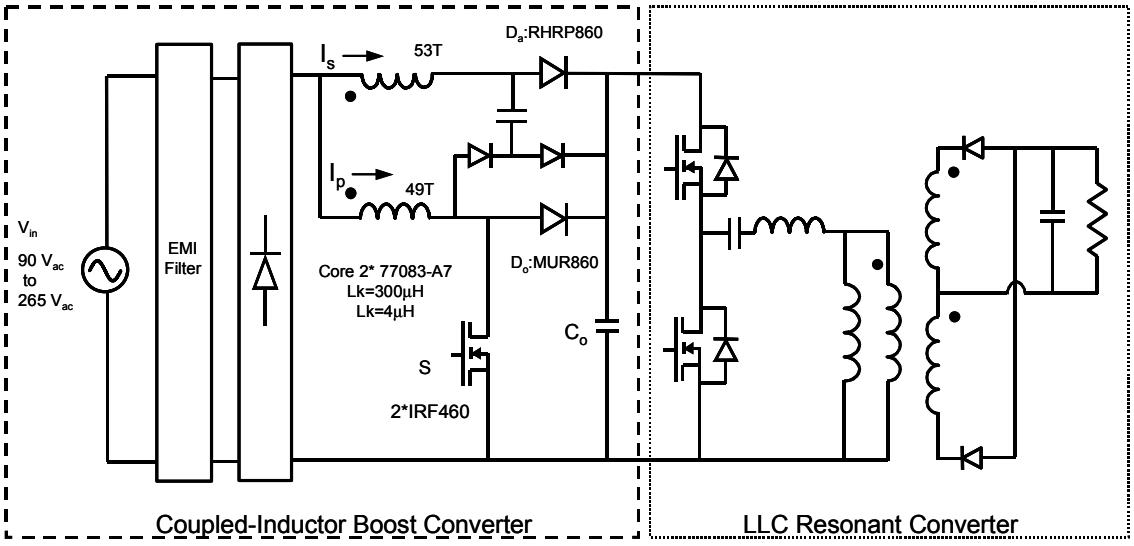


Fig. 3.41. High power-density 1U front-end converter.

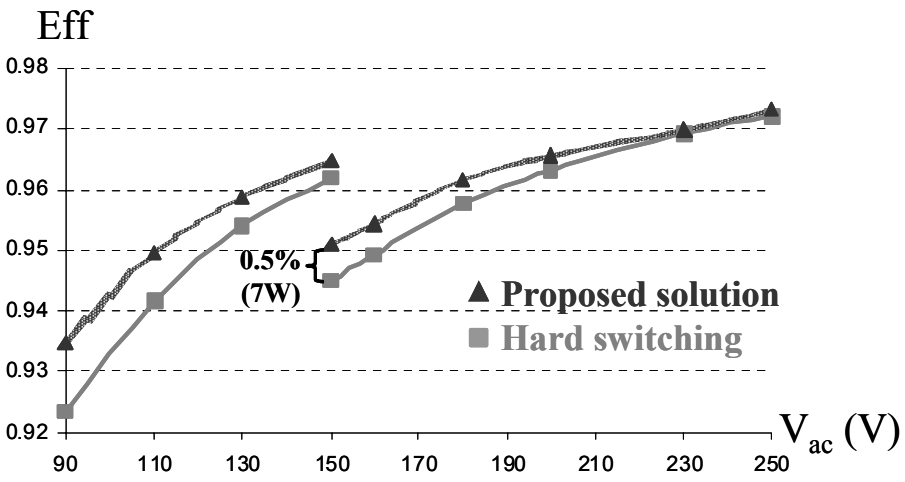


Fig. 3.42. Compariosn of the proposed solution and the hard-switching converter.

Fig. 3.43 shows the coupled inductor with three windings for the improved topology. There are two 77083-A7 cores in stack. The wire is AWG#16.

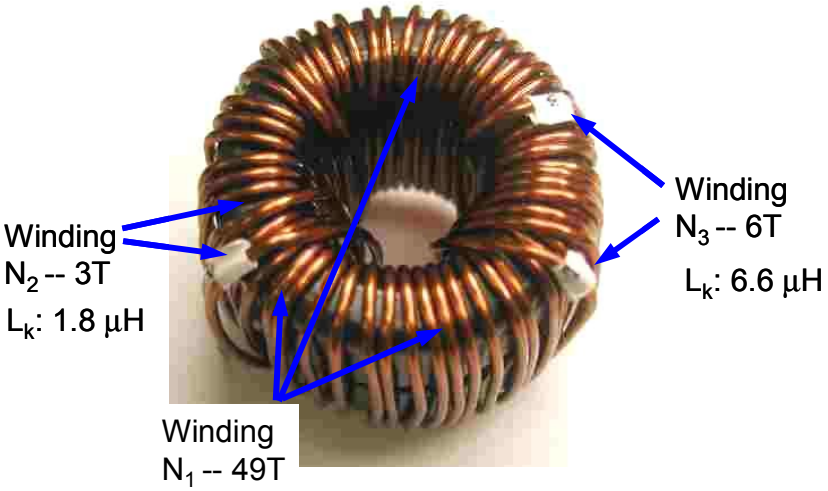


Fig. 3.43. The coupled inductor for the improved topology.

Fig. 3.44 shows the circuit parameters of the 1U front-end boost converter.

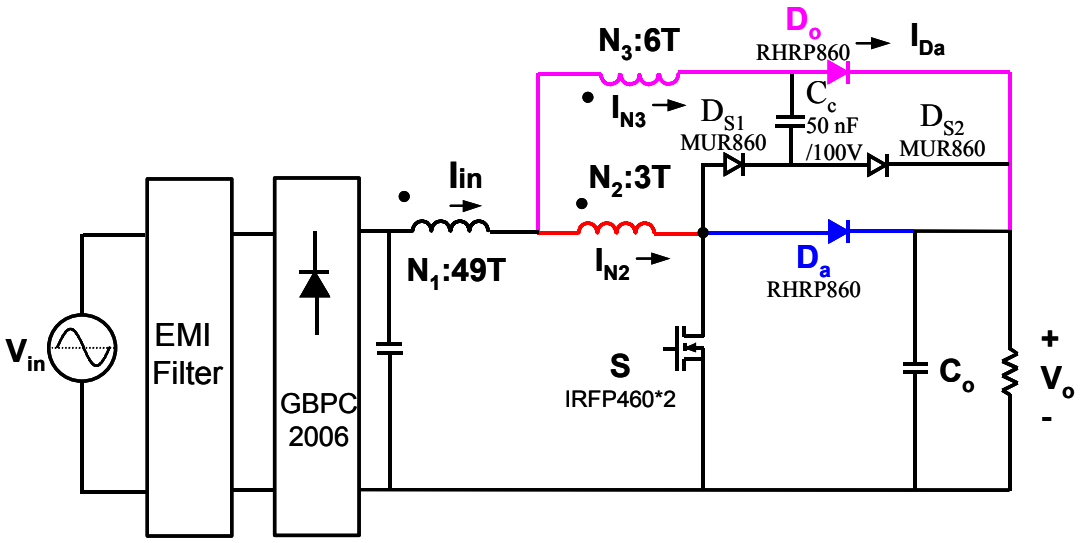
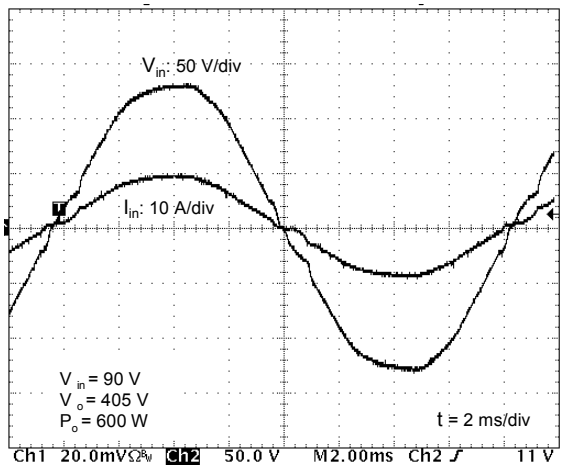
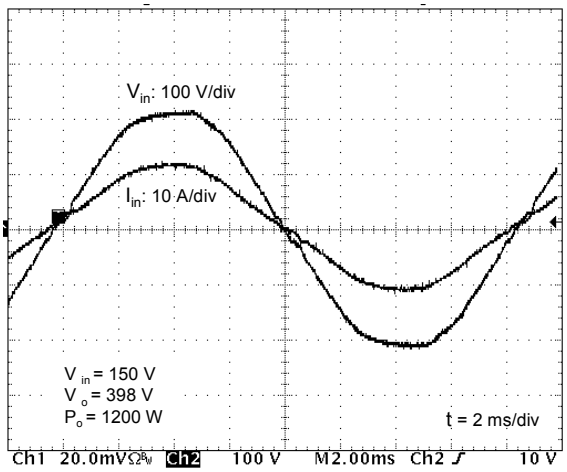


Fig. 3.44. Circuit realization of the improved version.

Fig. 3.45(a) and (b) show the input voltage and current waveforms in a line cycle at low line input with 600W of output power, and high line input with 1200W of output power. As can be seen from the waveforms, the input current has no distortion. The input current harmonic can meet IEC requirements.



(a)



(b)

Fig. 3.45. Input voltage and current waveforms at low and high line input: (a) V_{in} = 90V and (b) V_{in} = 150V.

As can be seen from Fig. 3.46, most of the winding flows a continuous current containing a large DC component, which can reduce the loss in the core.

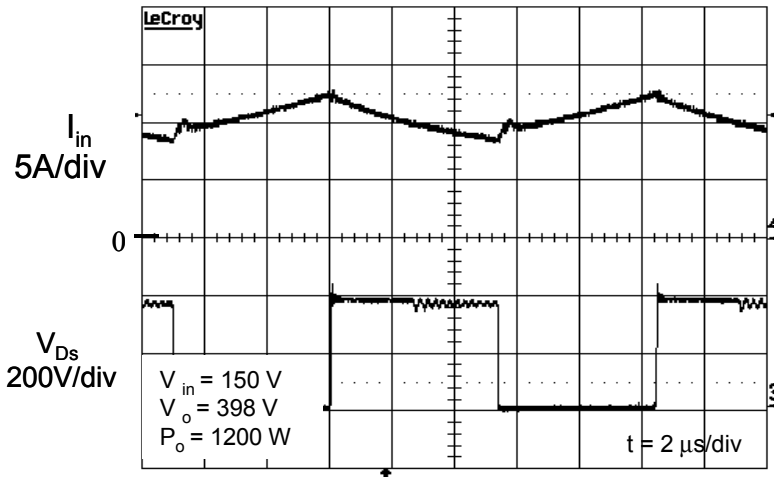


Fig. 3.46. Experimental waveforms of input current, switch current and voltage at 90Vac input..

Fig. 3.47 shows the current steering of the coupled inductor boost converter. During the switch turn-off time period, the current shifts from the original winding to the added coupled winding. Before switch turns on again, the winding current I_p is reduced to zero, the clamp rectifier D_a recovers naturally. The current is completely shifted to the added coupled winding when I_p reaches zero. When the switch turns on again, the current shifts back from the added coupled winding to the original winding. The output rectifier is turned off with controlled di/dt.

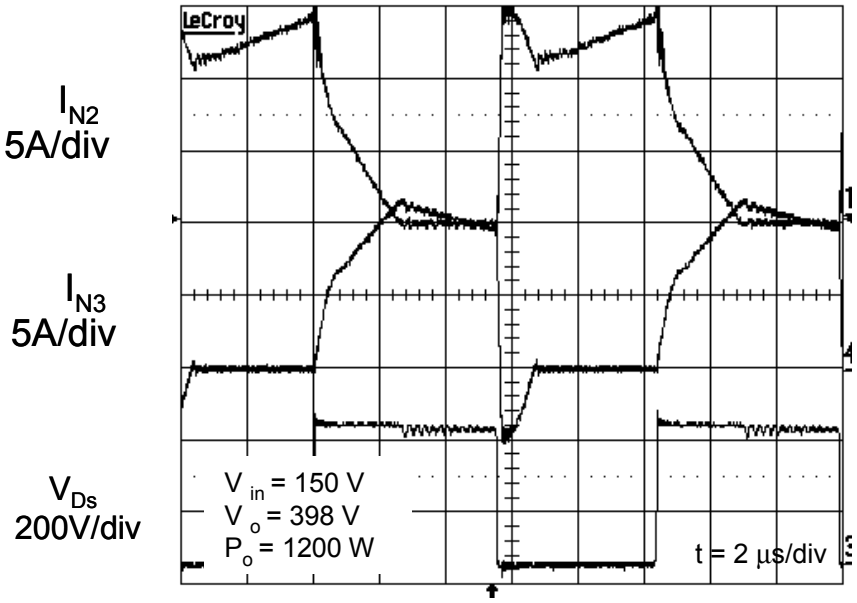


Fig. 3.47. Experimental waveforms of current steering.

Fig. 3.48(a) shows the rectifier current waveforms measured at the line peak with V_{in} =150V and P_o = 1200W. The current decrease rate through the added rectifier D_o is controlled, so the reverse-recovery problem is alleviated. Fig. 3.48 (b) shows the details with an enlarged time base of the encircled area in Fig. 3.48 (a). The current decrease rate is about 90 A/µs.

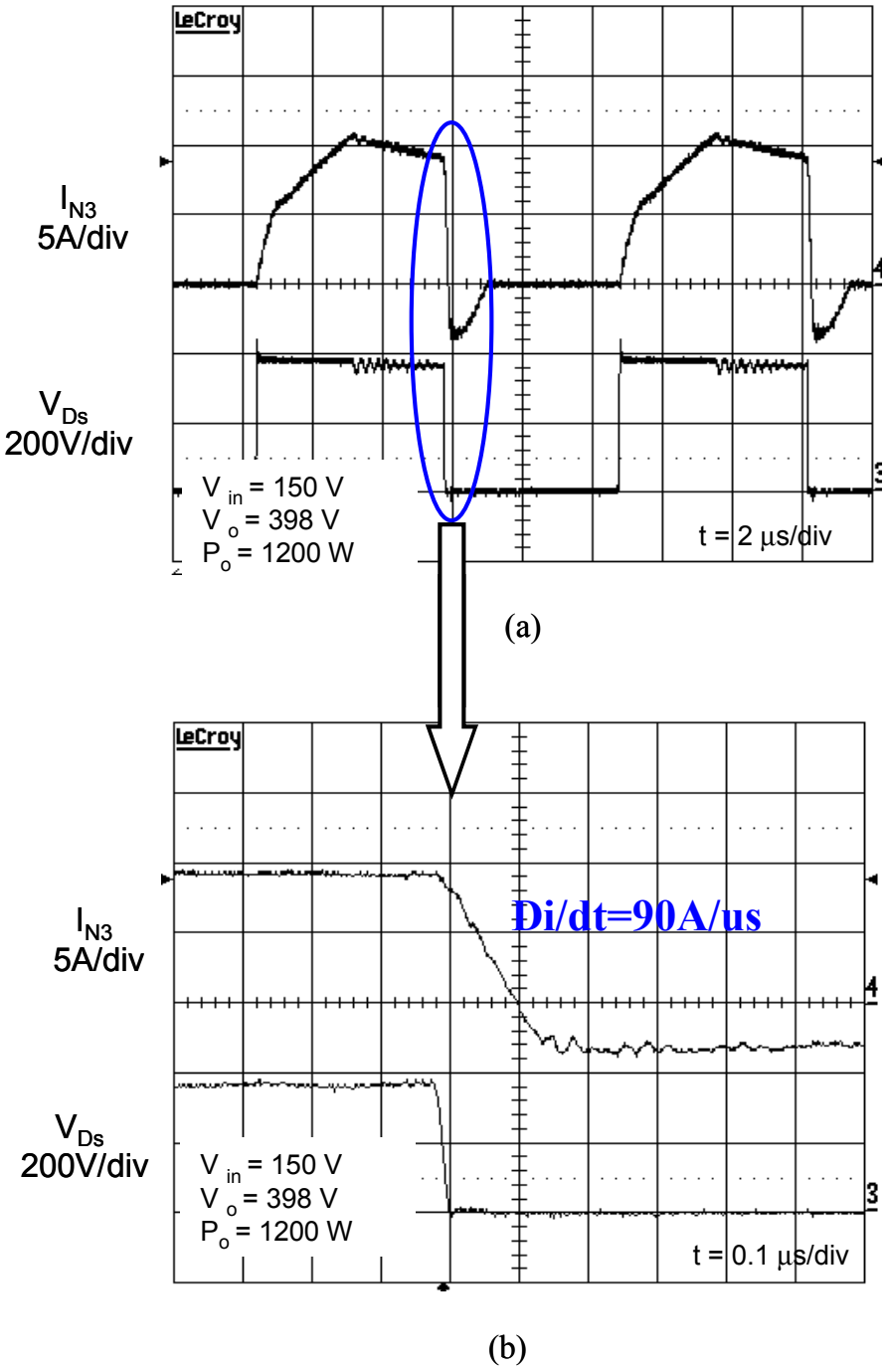


Fig. 3.48. The worst case of the rectifier reverse recovery has been alleviated: (a) complete current shift and (b) details of the circled waveforms in (a).

Fig. 3.49 shows the clamp capacitor voltage, which is about 70V. This capacitor helps to reduce the voltage stress of rectifier D_o.

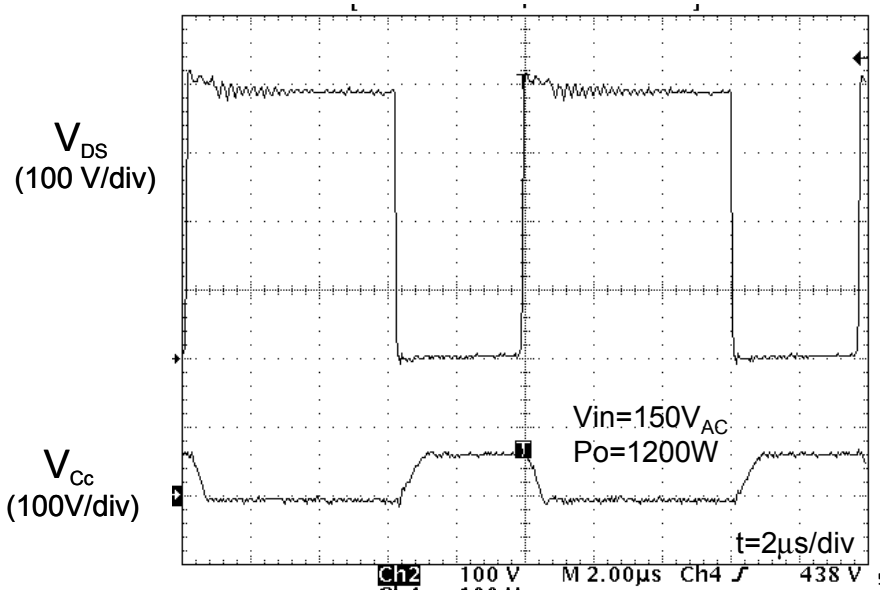


Fig. 3.49. Voltage waveform of the capacitor in the lossless snubber.

Fig. 3.50 compares the efficiency under hard switching (N_s=0) and soft switching (N_s=1.08). Due to the alleviated rectifier reverse-recovery problem, the switching losses of the converter can be dramatically reduced. The efficiency of the improved version is increased by a maximum of 1% when the input voltage is 150 V because the reverse-recovery-related losses are dramatically reduced. The efficiency improvement dramatically reduces the cost of the thermal management of the boost switch and the output rectifiers.

Fig. 3.51 shows the pictures of the baseline converter and the high power density, low profile front-end converter.

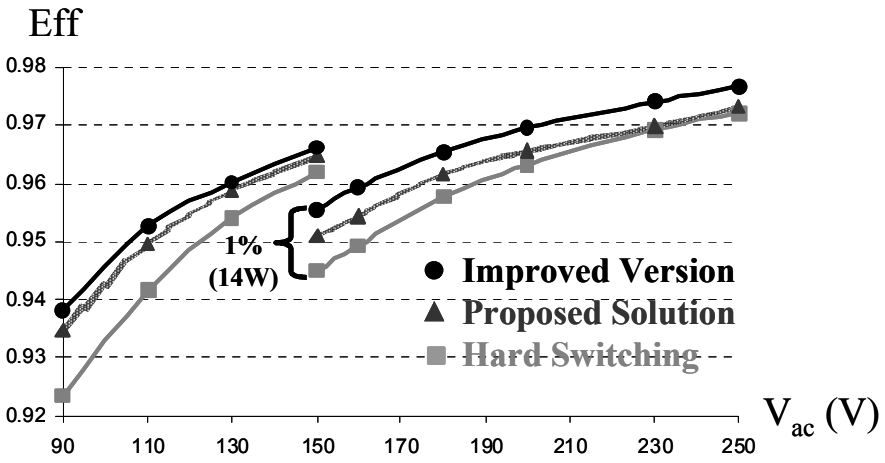


Fig. 3.50. Efficiency comparison for the PFC converter.

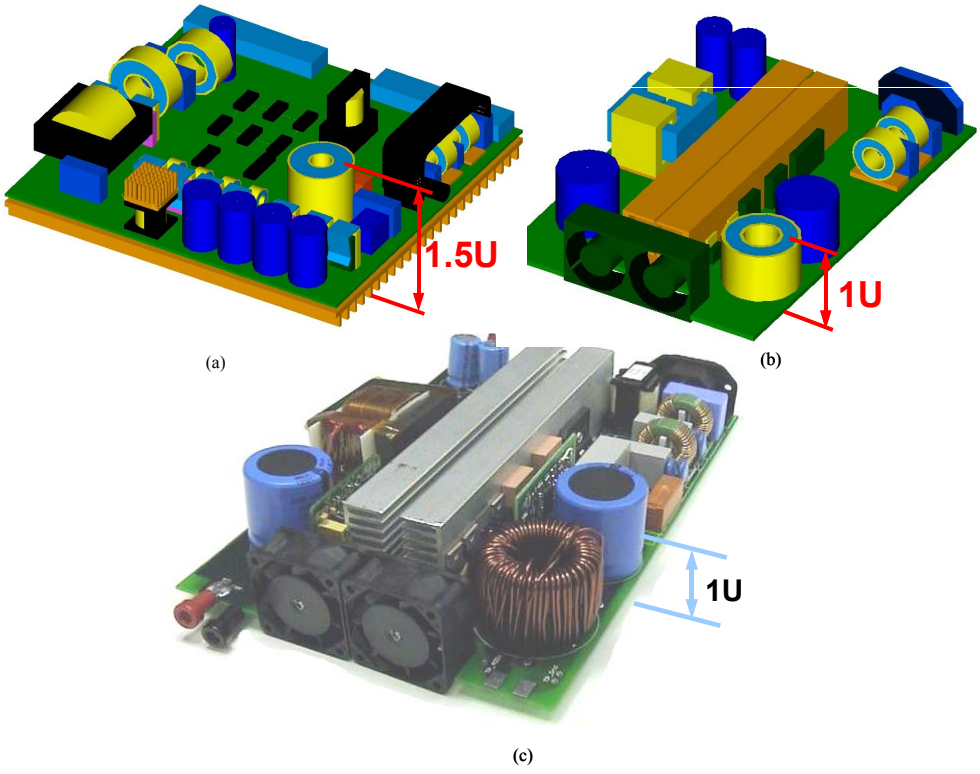


Fig. 3.51 Comparisons between the baseline and the developed converter:
(a) existing front-end converter; (b) low-profile, high power-density front-end converter and (c) picture of the low-profile, high power-density front-end converter.

Fig. 3.52 shows the reduction of profile and footprint, as well as the increase of power density for the developed converter.

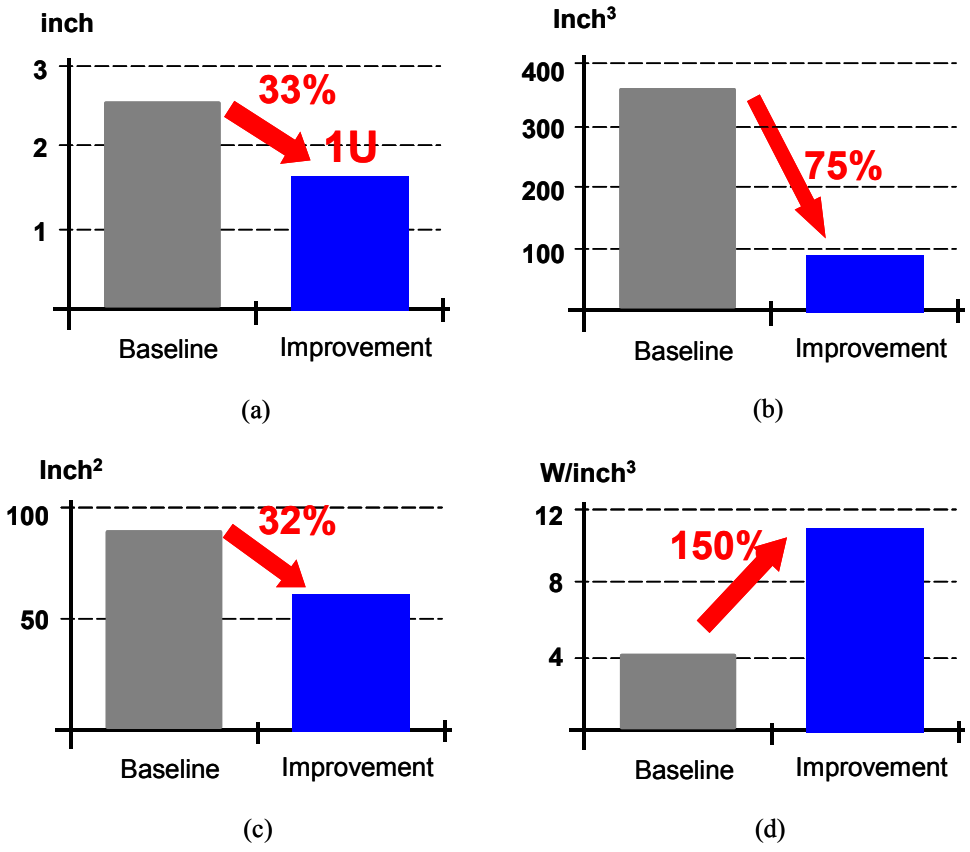


Fig. 3.52. Comparisons between the baseline and the developed converter: (a) profile; (b) volume; (c) footprint and (d) power density.

3.6. Concept Extension and Unified Current-Steering Condition

The boost converter with a totem-pole structure is capable of achieving higher efficiency because there are fewer switches in series in the current loop at low line input compared with the number in the conventional boost converter [C24] [C25]. These boost converters are actually a combination of two boost converters that share a common inductor. Each boost converter utilizes the body diode of another switch as the output rectifier. However, it is difficult to push the converter to CCM while maintaining decent efficiency if the two switches are hard-switched. Applying the proposed concept to the boost converter with a totem-pole structure requires only one additional winding coupled with the inductor and two additional rectifiers. Fig. 3.53 shows how to apply the proposed concept to the boost converter with totem-pole switches in order to alleviate the rectifier reverse-recovery problem. Under CCM, the performance of the boost converter shown in Fig. 3.53 can be dramatically improved because its rectifier reverse recovery can be alleviated. Less conduction loss will be induced because part of the input current will be steered to D_{o1} or D_{o2} after the main switch turns off. Only one rectifier voltage drop exists in the current loop with D_{o1} or D_{o2}. Another significant benefit of this converter is that the maximum voltage stress of D_{o1} and D_{o2} is clamped as the output voltage V_o. D_{o1} and D_{o2} serve as reciprocal clamp diodes. Therefore, no extra snubber circuits are needed to damp the undesired resonance between the leakage inductor and the parasitic capacitor of D_{o1} and D_{o2}.

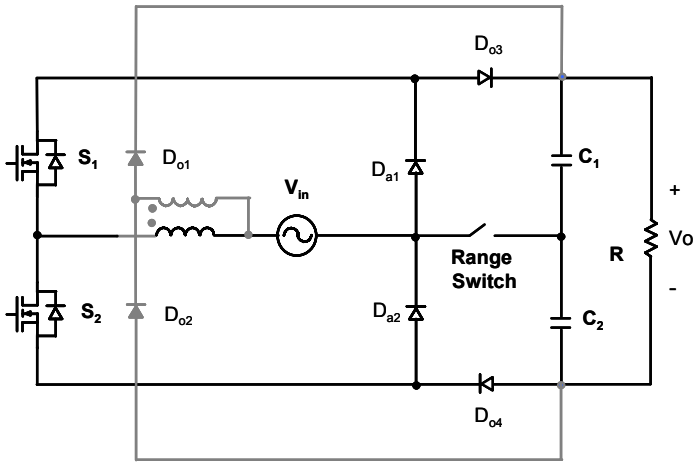


Fig. 3.53 Extension of the proposed concept to other boost PFC circuits for universal-line-input applications.

The switching cell, as shown in Fig. 3.54, can be identified. The unified condition for complete current steering can be derived.

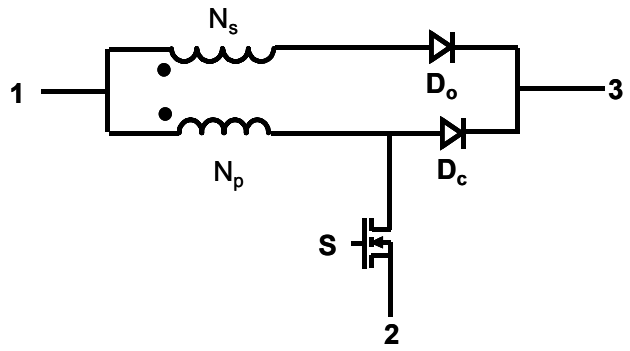


Fig. 3.54 Switching cell for alleviating the rectifier reverse recovery.

For this structure, Eq. 3-14 must be satisfied to guarantee the complete current transfer from the rectifier D_c to D_o, as follows:

$$\frac{dI_{Do}}{dt} = \frac{V_{31} \cdot (N-1)}{L_k} \cdot N \cdot (1-d) \cdot T_s > I_{Dc} \cdot \quad \text{Eq. 3-14}$$

Eq. 3-15 calculates the current decrease rate of the output rectifier. This rate should be less than 100A/μs.

$$\frac{dI_{Do}}{dt} = \frac{V_{12} + V_{13} / N}{L_k} \cdot \frac{1}{N} \cdot \quad \text{Eq. 3-15}$$

3.7. Summary

Utilizing a coupled inductor to realize current steering in order to alleviate rectifier reverse recovery is proposed, analyzed and experimentally verified in this chapter. From the ideal coupled-inductor switching cell introduced in Chapter 2, another equivalent coupled inductor switching cell can be derived. On one hand, the leakage inductance in the switching cell can control the rectifier reverse-recovery problem in practical applications; on the other hand, an effective way to recycle the leakage energy must be applied. Adding a diode so that the leakage energy can be discharged to the output is a simple solution. Based on the practical switching cell, new coupled-inductor converters with alleviated rectifier reverse-recovery problems are proposed. The proposed solution requires only one additional winding of the boost inductor and one additional rectifier. During the switch turn-off periods, the current through the clamp rectifier is completely shifted to the branch with the output rectifier. The clamp rectifier is

naturally recovered. When the switch turns on, the current decrease rate *di/dt* through the output rectifier is controlled. Therefore, the rectifier reverse-recovery problem is alleviated.

When the output power reaches the kilowatts, the parasitic resonance becomes a concern. Solutions for reducing the voltage stress of the output rectifier that occurs due to the parasitic resonance are proposed and compared. The proposed solutions are verified on a low-profile high power-density 1200W PFC AC-DC boost converter. The concept can easily be applied to other topologies, as it requires only a few simple modifications.

Chapter 4.
Utilizing Coupled Inductors to Realize Parallel Power Factor Correction

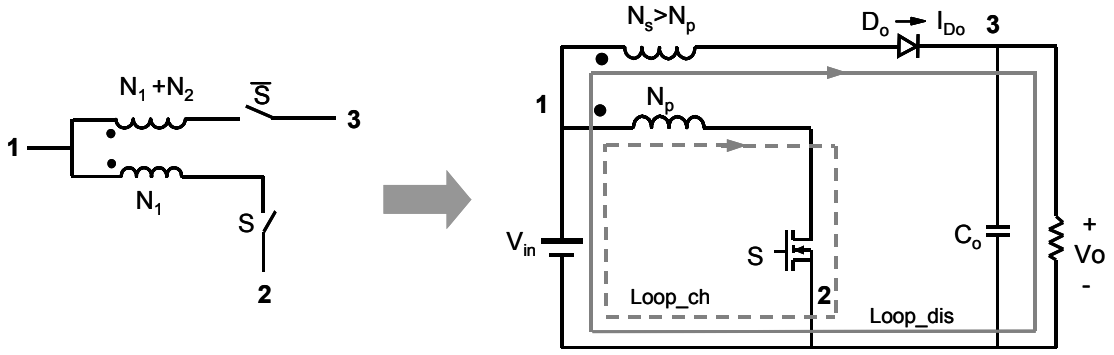
4.1. Introduction

In order to realize unity power factor and precise output regulation, the two-stage approach, which consists of a boost converter and a subsequent DC-DC converter, is a common choice for front-end telecom and server power supplies. The major disadvantages of this conventional two-stage conversion approach are the added cost and the complexity of the two-control-loop, two-power-stage nature. Another disadvantage of the two-stage approach is that the output power is processed twice. From the PFC standpoint, the converter does not need to process all of the power. Only 32% of the output power must be processed twice, which can be realized by the parallel power factor correction (PPFC) [D1]. This PPFC scheme reveals the benefit of efficiency improvement. The realization of unity power factor with PPFC involves a very complex topology and control. However, for many low-power applications, the single-stage approach has been developed to reduce the cost. The power factor does not need to be very high for the single-stage PFC AC-DC converters as long as the input current harmonics can meet the IEC requirements. This chapter proposes the use of a coupled inductor to realize the PPFC scheme. In the proposed scheme, the DC-DC converter takes the power directly from the rectified input voltage source and stores some energy in a bulk capacitor during the line peak area. The bulk capacitor will provide the power to the DC-DC converter when the line voltage

decreases below a certain value. The converter selects one of two voltages with the line variation. From the coupled-inductor switching cell, an equivalent circuit is derived. By separating the input voltage source into two voltage sources connected to the two coupled windings, a topology for PPFC can be found. As determined by the turns ratio and the external voltage, the current selects different discharge paths. This characteristic can be used to select the current path for PPFC applications. The single-stage coupled-inductor PPFC converters are proposed and verified. Compared to the conventional single-stage approach, in which the bulk capacitor voltage and the switch current stress are the major concerns, the proposed converters have much lower voltage stress and the switch current stress is minimized.

4.2. Coupled-Inductor Converters with Two Input Voltage Sources

Fig. 4.1(b) shows the coupled-inductor boost converter derived from the coupled-inductor switching cell shown in Fig. 4.1(a). The dashed line shows the magnetizing current charge path and the loop with the solid line shows the magnetizing current discharge path.



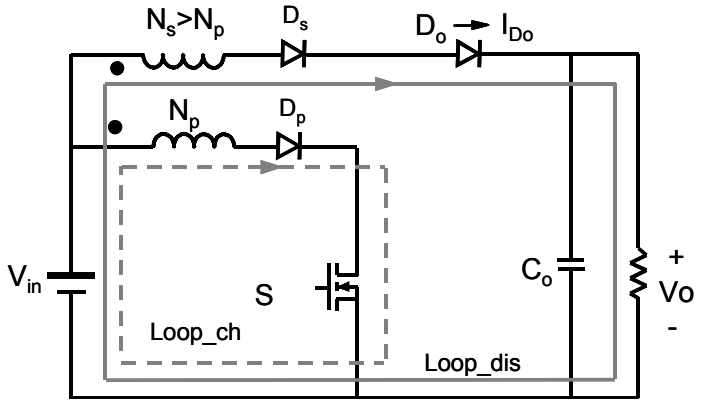
(a) (b)

Fig. 4.1. Coupled inductor converter derived in Chapter 3:
(a) the switching cell and (b) the coupled-inductor boost converter containing the switching cell.

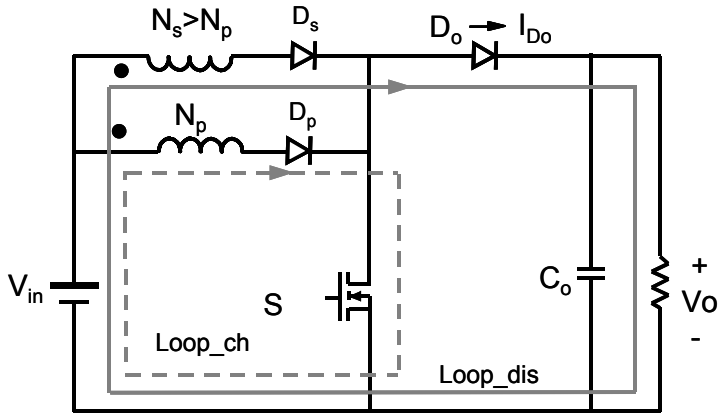
The coupled-inductor boost converter shown in Fig. 4.2(a) is the same as the converter shown in Fig. 4.1(b) except that two extra diodes are added in series with the two coupled windings. By adding the two diodes, the two coupled-inductor windings can be in a parallel structure, as shown in Fig. 4.2(b). This converter still has the same charge and discharge current paths. The converter also still operates the same way except that the voltage stress of the switch and diode are changed. In Fig. 4.2(c), the input voltage source is split into two input voltages, V_{inp} and V_{ins}. If the two voltage sources have different magnitudes, then the converter has two possible charge paths. When the following condition is met, the current charge source is V_{inp}:

$$\frac{V_{inp}}{N_p} > \frac{V_{ins}}{N_s}. \qquad \text{Eq. 4-1}$$

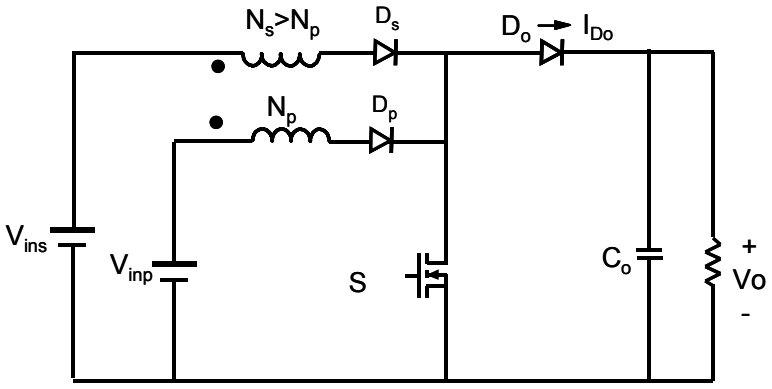
If the left-side term of the above equation is smaller than the right-side term, then the magnetizing current will be discharged through diode D_s. This converter can be used to realize the PPFC.



(a)



(b)



(c)

Fig. 4.2. Derivation of PPFC topologies:
(a) the boost version derived in Chapter 2; (b) a converter with same operation modes as the converter shown in (a) and (c) separate the input voltage source into two sources.

4.3. Parallel Power Factor Correction with PF=1

In order to realize unity power factor and precise output regulation, the two-stage approach, which consists of a boost converter followed by a DC-DC converter, is a common choice. The output capacitor of the boost stage must be sufficient to handle the power imbalance between the pulsating input power and the constant output power in one half-line cycle. For the conventional two-stage approach, if unity power factor is achieved, the input power pulsates. The PFC stage handles this pulsating power to generate a roughly constant DC bus. The downstream DC-DC converter regulates the output with constant power. In the two-stage approach, the output power is processed twice. For the single-stage approach, one switch does the work of the two switches. These two approaches have similar power flow pattern, as shown in Fig. 4.3.

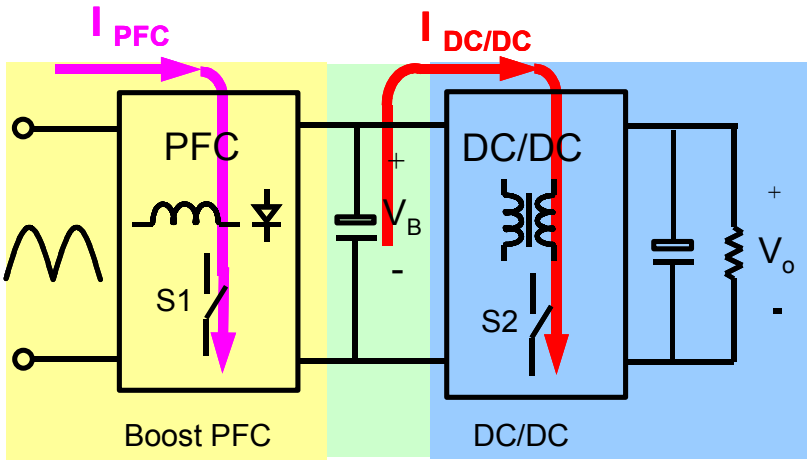


Fig. 4.3. Output power is processed twice in the two-stage approach.

Only a small part of the output power is processed twice in converters with PPFC [D1]. The input power variation with unity power factor is shown in Fig. 4.4(a). From the PFC standpoint, the converter does not need to process all of the power. As shown in Fig. 4.4(b), P_1 can be directly transferred to the output. Only P_2 must be processed twice, and it is only 32% of the output power. This scheme reveals the benefit of this efficiency improvement. However, in order to realize unity power factor with PPFC, the converter consists of two stages, and because stage one and stage two are two different converters, the complexity of the circuit makes the solution less cost-effective in low-power applications.

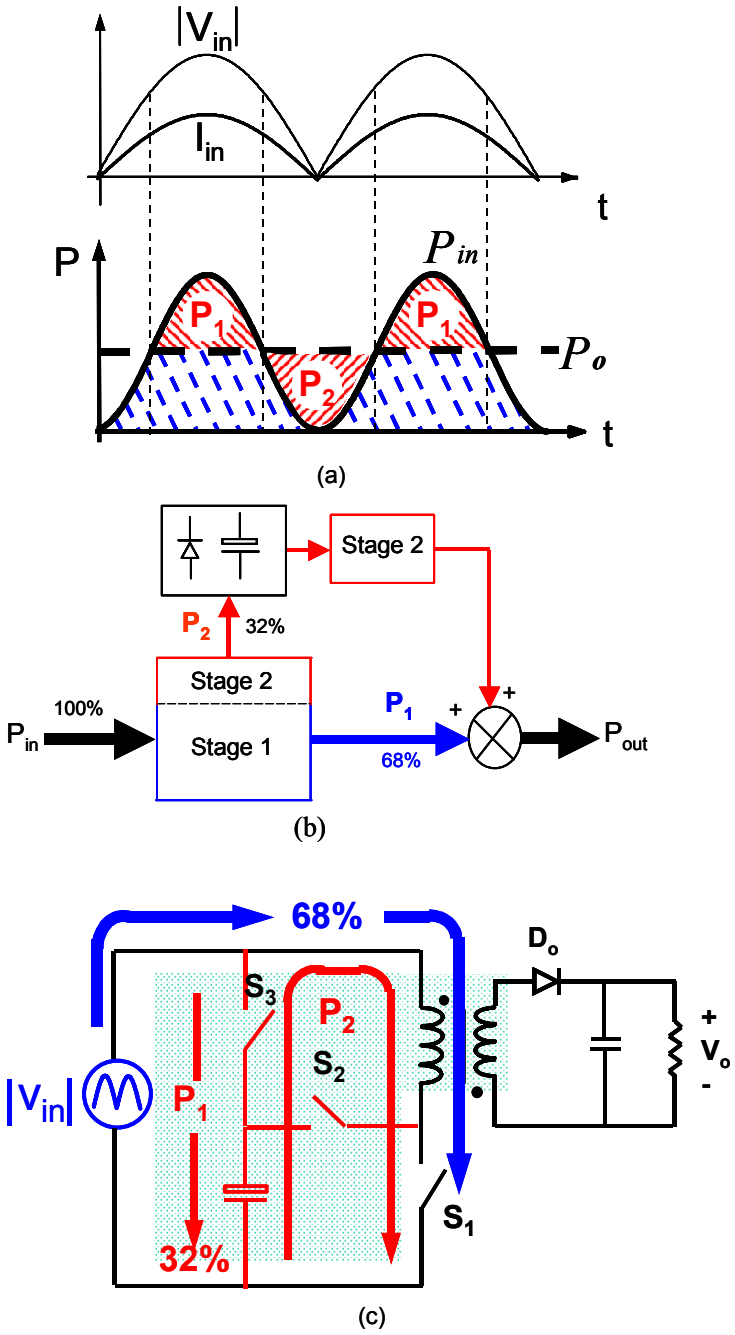
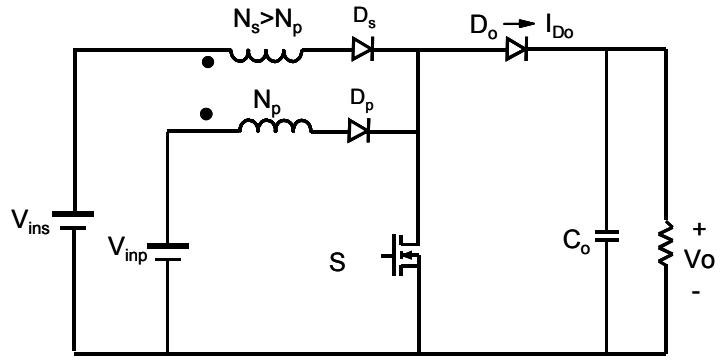


Fig. 4.4. Parallel PFC scheme with unity power factor:
(a) the input and output power for PF=1; (b) the concept of PPFC and (c) circuit realization.

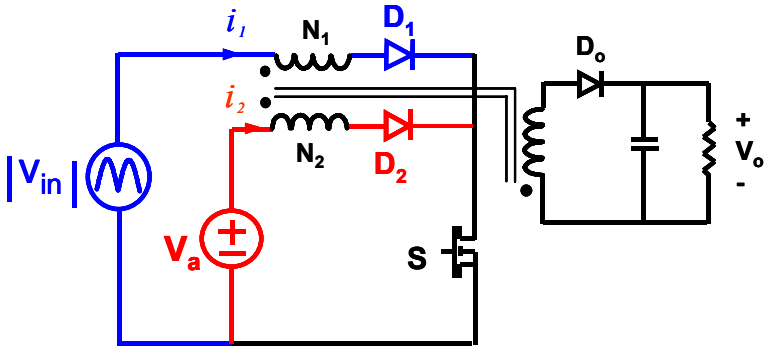
If the power factor is not required to be ideal, the single-stage single-switch topologies with PPFC [20][21] demonstrate two benefits compared to other single-stage approaches: The clamped bulk capacitor voltage and that there is no extra current stress associated with input current shaper (ICS). The problems with these PPFC configurations are the topology complexity and the input current harmonics. These schemes require both an additional magnetic component and an additional output rectifier. The additional magnetic component must handle the same maximum instantaneous power as that processed by the magnetic component in the DC-DC converter. The two magnetic components are not significantly different in terms of size. It is also difficult for the input current harmonics to meet the IEC1000-3-2 Class D regulations. The input current must be purposely shaped to go out of the Class D envelope in order to avoid Class D regulations. Therefore, the input current harmonics can only comply with Class A instead of Class D requirements. To overcome these drawbacks, single-switch PPFC converters with only a very small additional magnetic component are proposed in this chapter. Although the power factor is not ideal, the input current harmonics can meet IEC1000-3-2 Class D requirements. The simple topology structure has significant advantages, such as low bulk capacitor voltage at any load and no current stress associated with the ICS.

4.3.1. Parallel Power Factor Correction with PF<1

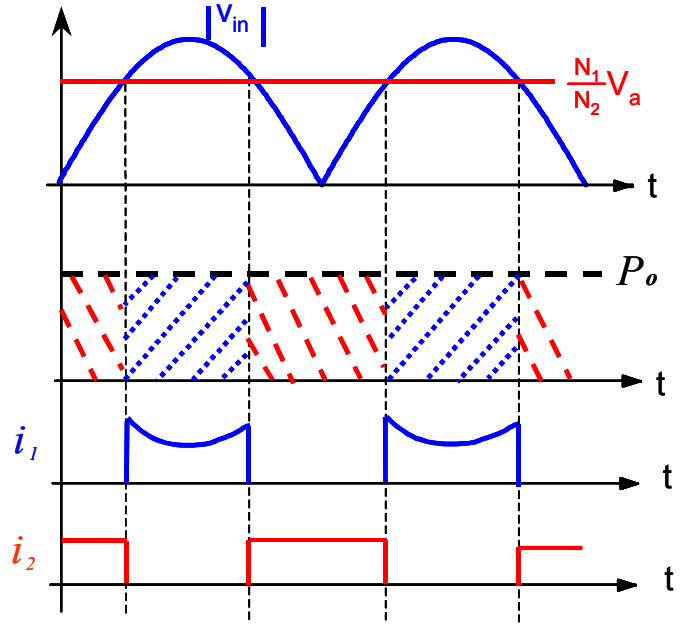
The original proposed concept and the key waveforms for realizing the single-stage single-switch PPFC are shown in Fig. 4.5(a).



(a)



(b)

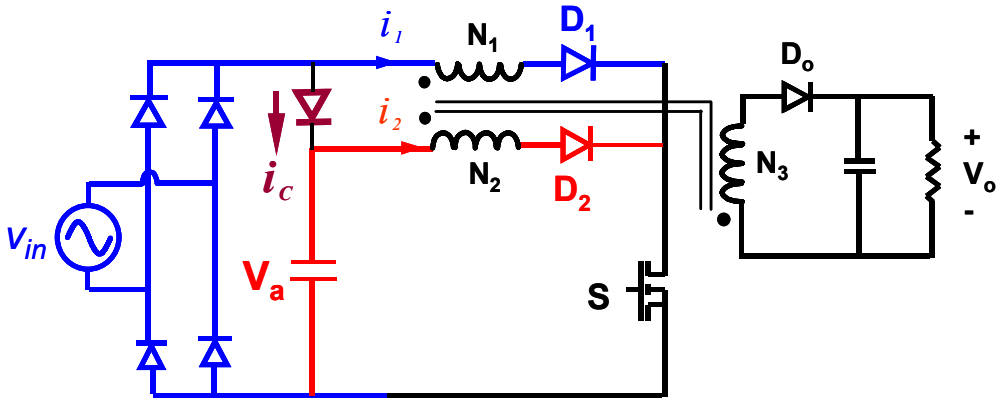


(c)

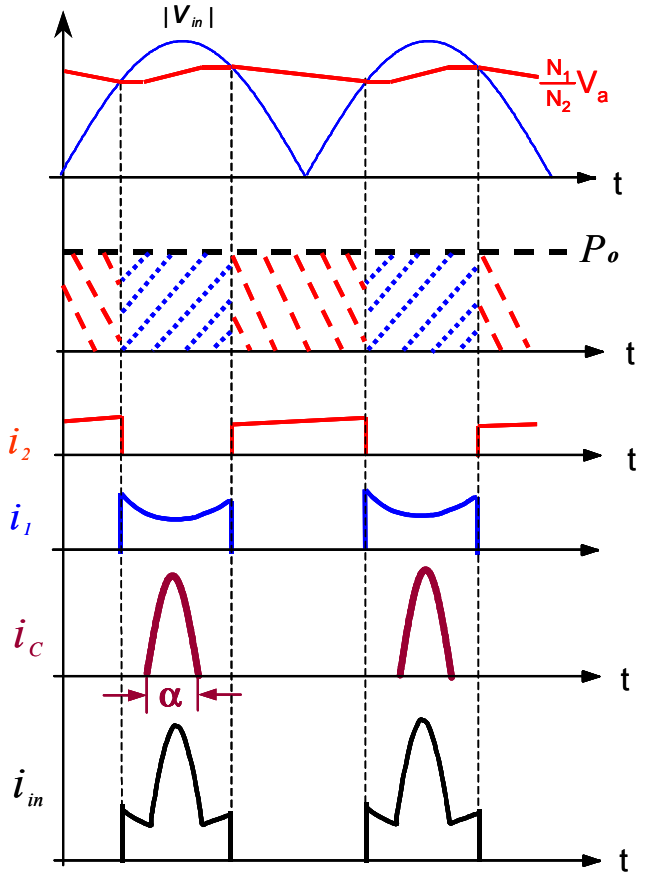
Fig. 4.5. Concept of parallel PFC for PF<1.
(a) boost version; (b) concept circuit and (c) simplified PPFC waveforms.

The DC-DC converter can select one of the two difference voltage sources depending on the magnitude of the rectified line voltage compared to KV_a ($K < 1$). The DC-DC converter draws the power from whichever has a higher instantaneous voltage. Therefore, the variation of the rectified input voltage source determines which voltage source provides power to the DC-DC converter. When the rectified input voltage is lower than KV_a, the power is provided by the voltage controlled-voltage source KV_a. When the input voltage is higher than KV_a, the power is provided by the rectified input voltage source. The PPFC concept for PF<1 can be realized using the Flyback version of the converter as shown Fig. 4.5(b).

Fig. 4.6 shows how to create the new voltage source by simply placing a diode after the rectifier bridge. As can be seen from Fig. 4.5, the maximum bulk capacitor voltage is the input peak voltage. The switch handles only the current for the DC-DC stage; no extra current for PFC goes through the active switch S.



(a)



(b)

Fig. 4.6. PPFC topology and the key waveforms:
(a) the topology and (b) key waveforms.

Fig. 4.6 also shows the three operation modes of the converters from the line cycle standpoint. During operation mode I, the input voltage is near a zero-crossing area. The rectified input voltage source is decoupled from the DC-DC converter because the rectified input voltage is lower than KV_{in_pk}. The output power is provided solely by the bulk capacitor. During operation mode II, the rectified input voltage source is larger than KV_{in_pk} but less than the instantaneous bulk capacitor voltage. The bulk capacitor is then decoupled from the DC-DC converter. The DC-DC converter takes the output power directly from the rectified input voltage source. During operation mode III, the rectified input voltage is larger than the instantaneous bulk capacitor voltage due to the ripple effect. The input current includes that provided to the DC-DC converter and that which charges the bulk capacitor. The conduction angle α corresponds to the time period for the rectified input voltage source to charge the bulk capacitor.

The operation of the converter is very simple. During the line valley area, the DC-DC converter takes the power from the paralleled voltage source. The current is roughly constant. When the line voltage is high, the DC-DC converter draws the power directly from the rectified input voltage. Because of the line voltage's variation, the input current should also vary in order to achieve constant output power. During the line peak area, there is a pulse current charging the bulk capacitor to compensate for the power loss that occurred during the line valley area. It is easy to understand that the input current looks the way shown in Fig. 4.6(b). We can find from the analysis that the I_c is not controlled and thus the input current has a large harmonic distortion.

4.3.2. Experimental Results

The proposed concept is verified on a 5V, 60W output, universal-line input voltage AC-DC converter. The turns of the coupled inductor are: $N_1 = 34T$, $N_2 = 28T$, and $N_3 = 3T$. Fig. 4.7 shows the input voltage and current waveforms and the current harmonic distributions at different input lines without boost inductor L_i. The input current harmonics can only meet the corresponding IEC-1000-3-2 Class D requirements at low line. The reason is that a relatively smaller percentage of the bulk capacitor energy is withdrawn during mode I in the high-line operation than that in the low-line situation. The bulk capacitor voltage has a small ripple at high line. The time period in which the bulk capacitor is charged is short, and the input current has a higher peak current. This could result in high third to thirteenth current harmonics.

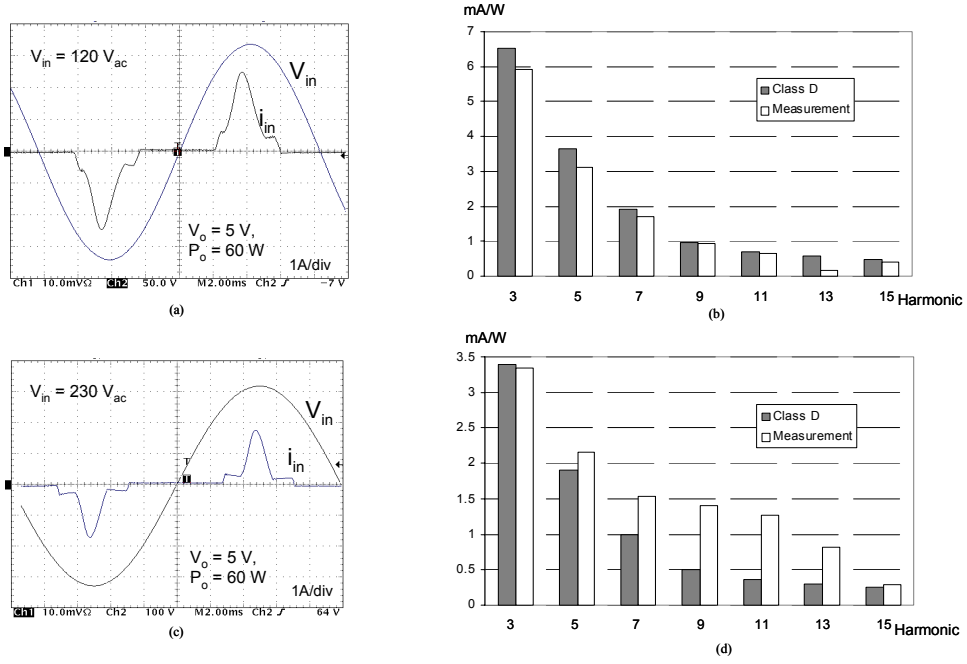


Fig. 4.7. Experimental results without:
(a) low-line voltage and current; (b) harmonic current distribution at low line;
(c) high-line voltage and current; and (d) harmonic current distribution at high line.

4.4. Improved Parallel Power Factor Correction with PF<1

4.4.1. Topology Derivation

In order to further improve the input current waveform, we need go back to re-analyze the waveform. It is obvious that all these waveforms are from the line cycle standpoint. Let's take a look what happens in the dotted area shown in Fig. 4.8(a) from the switching cycle perspective. In this area, the input current follows the Flyback magnetizing current. When the switch turns on, the input current jumps immediately to the magnetizing current. When the switch turns off, the input current drops immediately to zero. There is no current charge in the capacitor. The thinking is that if a small inductor is added as shown in Fig. 4.8(d) and the turn off current is assumed to remain the same, then the current has to be discharged somewhere after the switch turns off. This part will be discharged to the bulk capacitor. So the charge angle of the bulk capacitor is increased, the peak current will decrease, and then the input current can be shaped better.

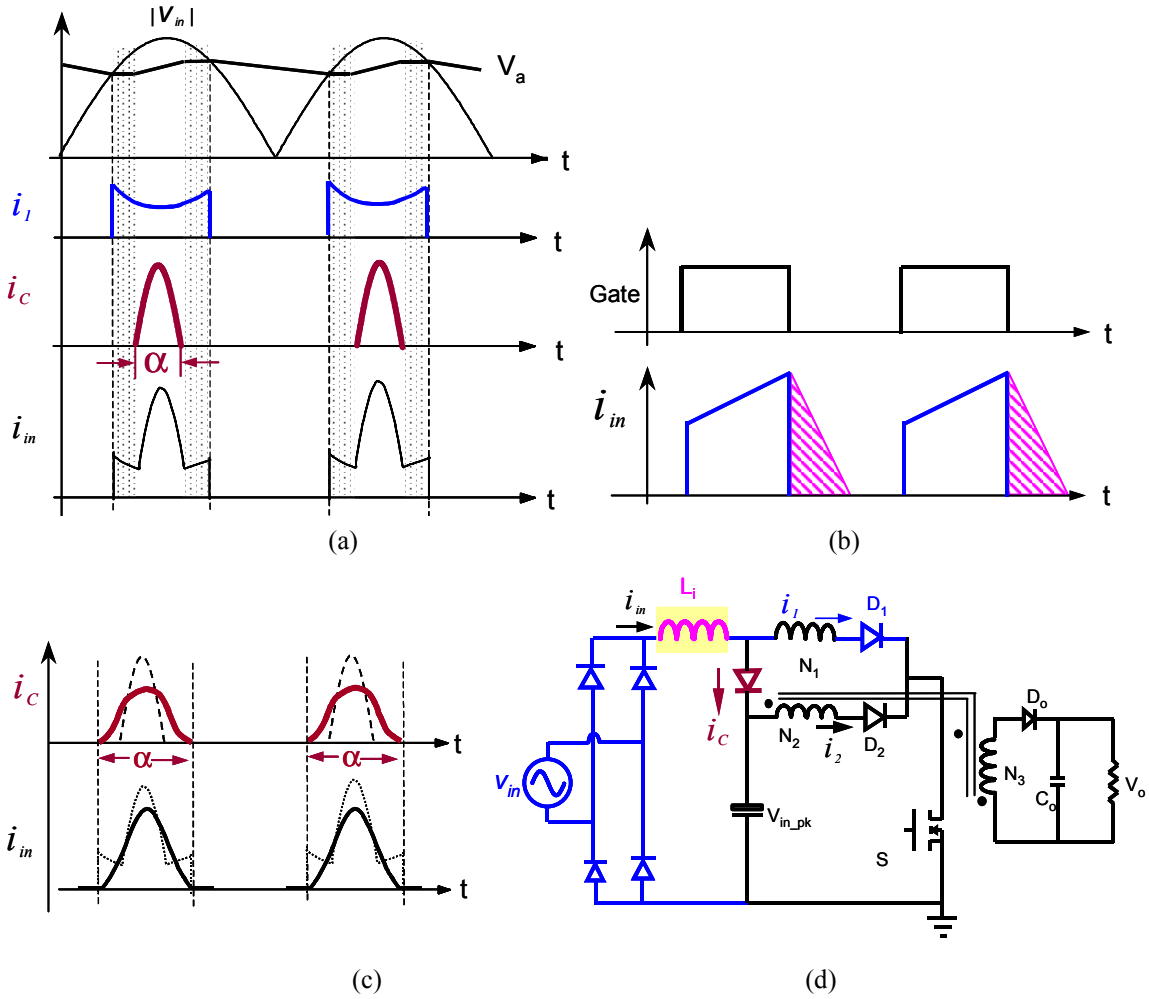


Fig. 4.8. Improving the input current waveform:
(a) waveform in a line cycle; (b) waveform in a switching cycle corresponding the dotted area of (a); (c) extension of the input current conduction angle; and (d) when a small inductor is added.

4.4.2. Operation Analysis

In terms of the switching-cycle, the down-slope of the input current I_{in} is vertical during operation mode II. No current is charged to the bulk capacitor during this operation mode. If a small input L_i is added, as shown in Fig. 4.8, the energy stored in L_i is then discharged to the bulk

capacitor after switch *S* turns off. To maintain the energy balance, the input peak current can be reduced if L_i is added because the bulk capacitor is charged in both operation modes II and III. The added small inductor L_i is essentially a boost inductor, but the bulk capacitor voltage is well controlled under different load conditions because of the inherent load current feedback mechanism, which differs from the bulk voltage feedback [D12]-[D14]. The operation of the converter becomes much more complicated after the small inductor L_i is added.

Operation mode I: during the intervals [0, t_1] and [t_6, t_7], the converter operates in mode I when the rectified input voltage is between zero and KV_B. The converter operates as a conventional Flyback converter with turns ratio N_2:N_3 by drawing the energy only from the bulk capacitor. The key waveforms for mode I in one switching cycle are shown in Fig. 4.9(a). No input current is drawn from the input voltage source. Therefore, the input current waveform has dead time periods near the zero-crossing area. The corresponding angle θ is given by Eq. 4-2:

$$\theta = \arcsin\frac{K \cdot V_B}{V_{in\_pk}}. \qquad \text{Eq. 4-2}$$

where V_B is the bulk capacitor voltage, and V_{in_pk} is the input peak voltage.

The up-slope and the down-slope of the magnetizing inductor current I_{Lm} are given in Eq. 4-3 and Eq. 4-4, respectively:

$$K\_{I_{Lm\_up}} = \frac{K \cdot V_B}{L_m}. \qquad \text{Eq. 4-3}$$

$$K\_{I_{Lm}\_dw} = -\frac{(N_1/N_3)\cdot V_o}{L_m}. \quad \text{Eq. 4-4}$$

The converter's duty ratio is essentially constant, as given in Eq. 4-5:

$$D = \frac{[(N_1+N_2)/N_3]\cdot V_o}{V_B + [(N_1+N_2)/N_3]\cdot V_o}. \quad \text{Eq. 4-5}$$

Operation mode II: the rectified input voltage $|V_{in}|$ increases to KV_B at time t_1. The converter then begins to operate in mode II. The magnetizing current includes two components. One is associated with the boost inductor current, and is represented by the vertically dashed part in Fig. 4.9(b). The ramp-up slope of the boost inductor current is given as follows:

$$K\_{I_{Li}\_up}(t) = \frac{|V_{in}(t)| - K\cdot V_B}{L_i}. \quad \text{Eq. 4-6}$$

The other component of I_{Lm} is taken from the bulk capacitor and is represented by the horizontally dashed part in Fig. 4.9(b). The up-slope and the duty ratio remain the same as those of operation mode I.

After switch S turns off, the boost inductor current is discharged to the bulk capacitor. The ramp-down slope of the current is given by Eq. 4-7. The down-slope of I_{Lm} remains the same as that of operation mode I.

$$K\_{I_{Li}\_dw}(t) = -\frac{V_B - |V_{in}(t)|}{L_i}. \quad \text{Eq. 4-7}$$

Compared to Fig. 4.6, the conduction angle α for the rectified input voltage source to charge the bulk capacitor is enlarged after the small inductor L_i is added, as shown in Fig. 4.8.

For the input boost inductor current, the discharge duty ratio d_2 could be given as Eq. 4-8:

$$d_{2(t)} = \frac{|V_{in(t)}| - K \cdot V_B}{V_B - |V_{in(t)}|} \cdot D \cdot \qquad \text{Eq. 4-8}$$

The average current of the boost inductor in a switch cycle can be given as Eq. 4-9:

$$I_{av\_sw(t)} = \frac{|V_{in(t)}| - K \cdot V_B}{2 \cdot L_i} \cdot D^2 \cdot T_s \cdot \frac{(1-K) \cdot V_B}{V_B - |V_{in(t)}|} \cdot \qquad \text{Eq. 4-9}$$

Operation mode III: when $|V_{in}|$ increases further, the converter enters mode III at time t_2. The boost inductor L_i is still under DCM operation. The magnetizing current has two different slopes. Correspondingly, the boost inductor current has two different slopes, as shown in Fig. 4.9 (c). The first slope is defined by Eq. 4-6 before the boost inductor current reaches the magnitude of magnetizing current I_{Lm}. Both the rectified input voltage source and the bulk capacitor provide the magnetizing energy. Once the boost inductor current is charged to the level of the magnetizing current, the input inductor current charge slope is changed to that given in Eq. 4-10. The rectified input voltage is then the only source providing the magnetizing energy.

$$K_{\_I_{Lm}\_up2(t)} = \frac{|V_{in}|}{L_i + L_m} \cdot \qquad \text{Eq. 4-10}$$

The duty ratio is reduced compared with that of modes I and II. The higher the input voltage, the lower the duty ratio.

Operation mode IV: when $|V_{in}|$ is around the line peak area, the converter operates in mode IV, as shown in Fig. 4.9(d). The input boost inductor is operated in CCM. Almost all magnetizing current is drawn from the rectified input voltage $|V_{in}|$. The up-slope and the down-slope of the input inductor current are the same as those in mode III, and are given in Eq. 4-6, Eq. 4-10 and Eq. 4-7.

The duty ratio is further reduced, and its approximate value can be given in Eq. 4-11:

$$d_{(t)} = \frac{(N_1/N_3)\cdot V_o}{V_{in(t)} + (N_1/N_3)\cdot V_o}. \qquad \text{Eq. 4-11}$$

To simplify the analysis and clarify the physical meaning, the average current of the boost inductor in a switch cycle during modes III and IV can be given in Eq. 4-12:

$$I_{av\_sw(t)} = I_o^{'}\cdot D(t) + \frac{1}{2}\cdot I_{o\_pk(t)}^{'2}\cdot\frac{L_i}{V_B - V_{in(t)}}\cdot F_s. \qquad \text{Eq. 4-12}$$

where $I_o^{'}$ is the average load current reflected to the primary side, and $I_{o\_PK}^{'}(t)$ is the peak load current reflected to the primary side

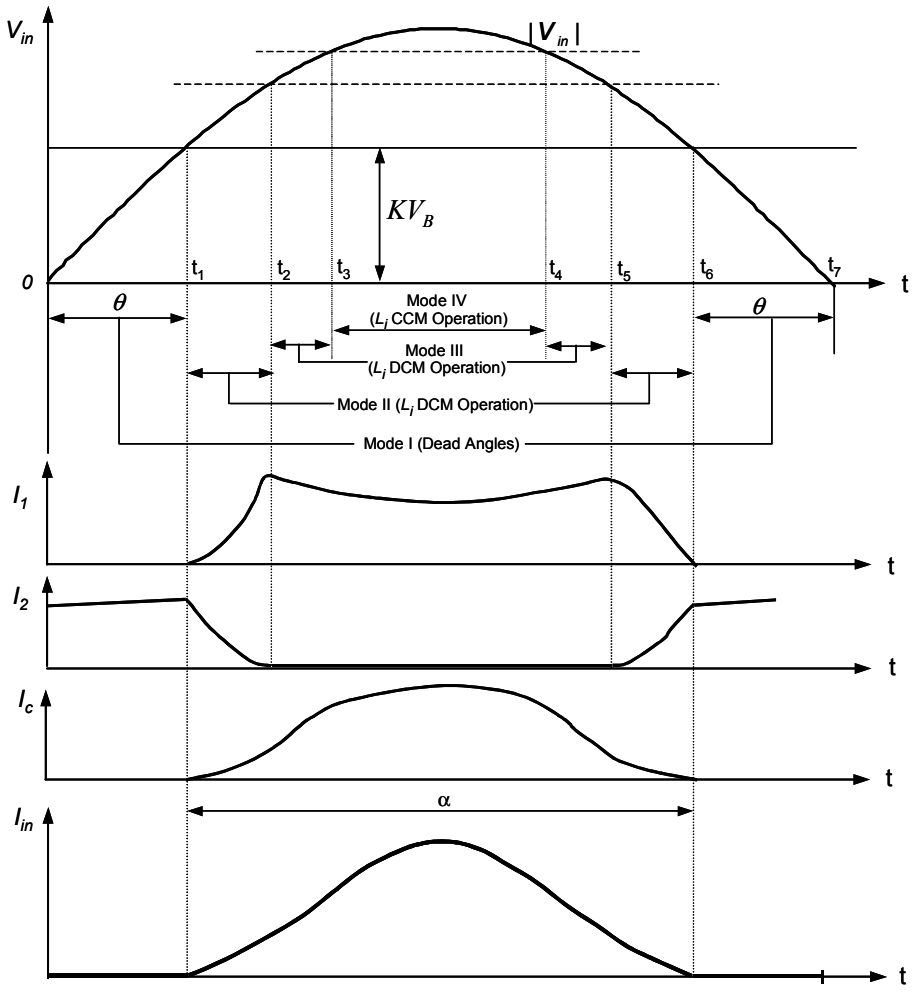


Fig. 4.9. Four operation modes of the converter with a boost inductor.

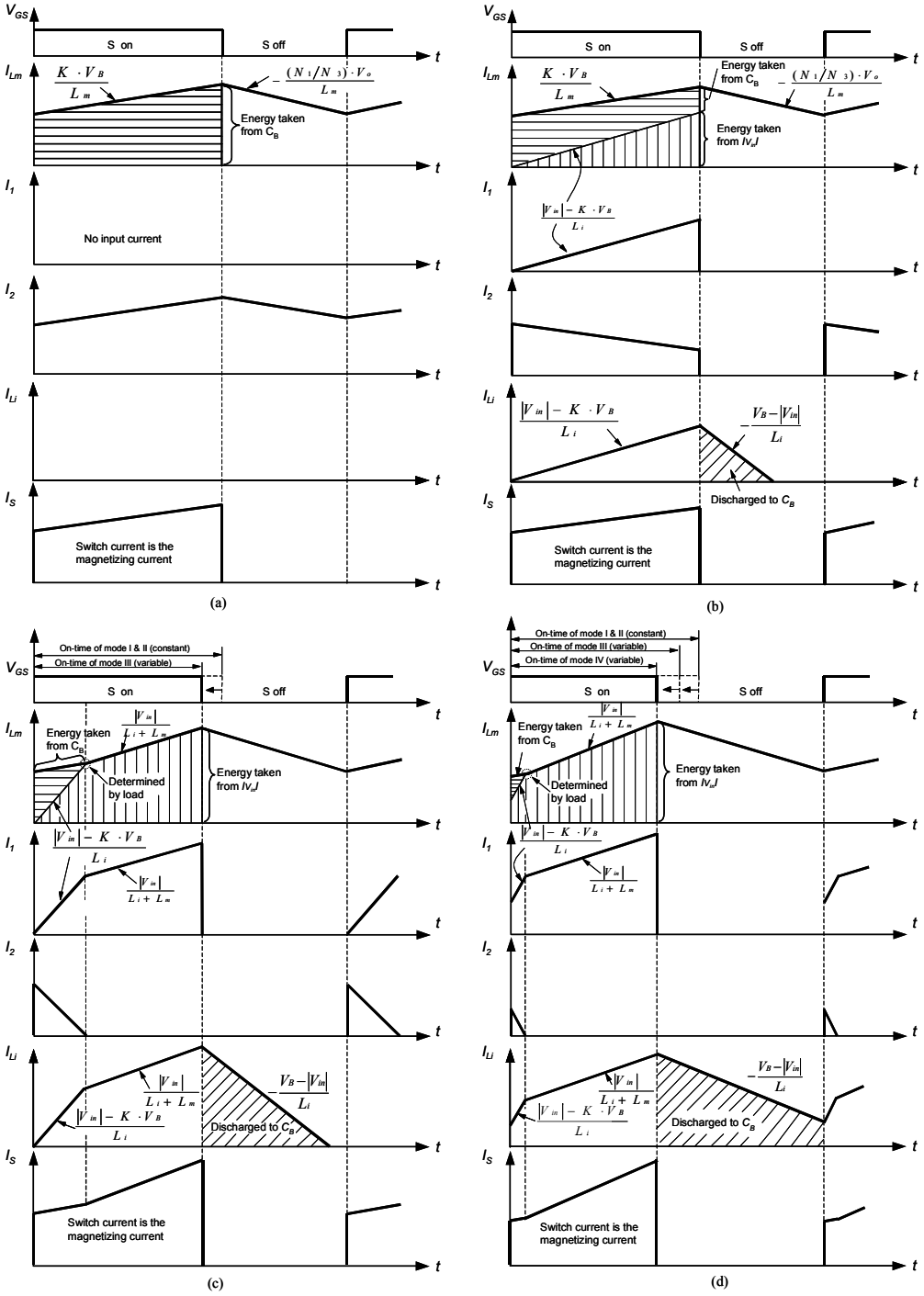


Fig. 4.10. Key waveforms in one switching cycle for four different operation modes: (a) mode I; (b) mode II; (c) mode III; and (d) mode IV..

The average input current in modes III and IV is strongly dependent on the reflected load current. This inherent load current feedback mechanism can reduce the input power at light load without reducing the duty ratio. During the switch-on time, the boost inductor current is the current of the DC-DC inductor, as shown in Fig. 4.10. If the output power decreases, the input inductor current decreases accordingly. At light load, it is not necessary for the duty ratio $D_{\_Light}$ to shrink in order to reduce the input power. As can be seen from Fig. 4.10, the $D_{\_Light}$ is almost the same as the duty ratio $D_{\_full}$ at full load. The input power has been reduced even if the DC-DC converter is operated in CCM. Unlike this feedback mechanism, the bulk capacitor voltage feedback utilizes an additional winding to control the input inductor current [D12]-[D14][D19], which works only after the bulk capacitor voltage has been increased. The load current feedback directly feeds back the output power information instead of indirectly feeding back the bulk capacitor voltage. It is also obvious that the switch has no extra current stress. The load current feedback can effectively reduce both the voltage stress of the bulk capacitor and the current stress of the active switch.

4.5. Comparison of the Proposed Approach with Other Single-Stage PFC AC-DC Converters

4.5.1. A Brief Review of Single-Stage PFC Technology

In low-power applications, for which cost is the dominant issue, the single-stage PFC AC-DC converters that integrate the two power stages into one, thus reducing significantly the component count and cost, have gained much attention in many low-power applications during the past ten years. Integration of a boost-derived ICS and a DC-DC converter with a bulk capacitor between them is the dominant configuration [D4]. The major drawbacks of the single-stage approach are the voltage stress of the bulk capacitor voltage stress and the switch current stress problem. Since the controller is used to tightly regulate the output with a roughly constant duty ratio, the bulk capacitor voltage is not controlled. The bulk capacitor could be as high as 1,000V at light load, which makes the solution impossible. The switch stress results from handling the current from both the PFC stage and the DC-DC stage. High current stress of the switch reduces the efficiency of the converter. It has been proved that the single-stage approach is a cost-effective solution for applications with power levels lower than 200 W [D5][D6], when the bulk capacitor voltage is well controlled below 450 V for the universal-line input. Many approaches have been proposed to alleviate the bulk capacitor voltage stress and to reduce the switch current stress. Basically, the practical solution is to modify the topology so that automatic feedback of the bulk capacitor voltage and the reduction of switch current stress can be achieved. The bulk capacitor voltage feedback using a coupled winding structure [D7] can reduce the bulk capacitor voltage to within this practical range. Due to simplicity and effectiveness, the coupled feedback windings are widely used to reduce bulk capacitor voltage stress and switch current

stress in state-of-the-art single-stage PFC AC/DC converters [D7]-[D10], although this feedback winding increases the input current distortion by inducing a dead angle for the input current. The first part of this chapter presents a detailed analysis of bulk capacitor voltage feedback. The relationship between bulk capacitor voltage, input current harmonics, feedback-winding ratio, and load condition is numerically quantified and experimentally verified. To further reduce the bulk capacitor voltage stress and switch current stress, new topologies with inherent load current feedback are proposed, analyzed and experimentally verified. The research on single-stage PFC AC-DC converters can be traced back to the early 1990s, and includes such concepts as the dither [D11] and the well-known boost integrated with Flyback rectifier / energy storage / DC-DC converter (BIFRED) [D12]. A new family of single-stage PFC AC-DC converters [D13] utilizes the same concept as the BIFRED. Only one control is used to tightly regulate the DC-DC output voltage with a roughly constant duty ratio. Therefore, the boost converter operating in DCM with constant duty ratio can achieve automatic input current shaping. The difference is that the bulk capacitor of the BIFRED converter is in the series path of the energy flow, while the bulk capacitor of the other converter [D9] is in the parallel path of the energy flow. In contrast to this ICS [D13], which is a three-terminal cell because the charge path and the discharge path of the boost inductor are different, the ICS using the magnetic-switch (MS) concept [D14] is a two-terminal cell because the charge path and the discharge path before the bulk capacitor are the same. Actually, the three-terminal and the two-terminal ICS cells are functionally equivalent [D4][D15][D16]. Fig. 4.11 illustrates the general structure of a single-stage PFC AC-DC converter.

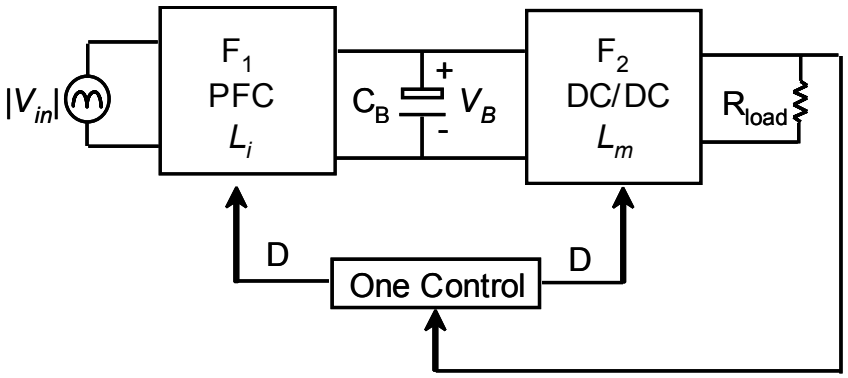


Fig. 4.11. Block diagram of single-stage PFC AC/DC converter.

Although two blocks are shown in the figure, the converter has only one switch and one control loop. The F_1 acts as the ICS, and the F_2 is an isolated DC-DC step-down converter. L_i and L_m are the input boost inductor and the inductor of the DC-DC converter, respectively. Between F_1 and F_2, there is a bulk capacitor C_B, which handles the instantaneous imbalance between the input power and the output power. Excessively high $V_{B\text{-}max}$ is generated at high line, light load operation when the DC-DC converter is operated in CCM. The reason is simple: The duty ratio of a DC-DC converter in CCM operation is determined only by the voltage gain; it does not change immediately when the output power decreases. Therefore, the input power remains constant, and is larger than the output power; the difference between the input and output power must be stored in the bulk capacitor. As a result, the bulk capacitor voltage increases. To tightly regulate the output voltage, the duty ratio must decrease. Consequently, the input power decreases. This dynamic process will not stop until the input and output power reach a new balance. The new power balance at light load is reached at the penalty of high bulk capacitor voltage, which results in a small duty ratio for reducing the input power. Variable frequency control (VFC) alleviates the bulk capacitor voltage stress [D17], but VFC is unable to

effectively limit the bulk capacitor voltage to less than 450 V, even with ten times the frequency variation range. For VFC, the magnetic components must be over-designed to meet the requirements of the worst operation condition. The alternative solution is to design F_2 in DCM operation. If F_2 is operated in DCM, both the duty ratio and the input power decrease automatically when the output power decreases. If both L_i and L_m are operated in DCM, the bulk capacitor voltage V_B is independent of load; it is only determined by the ratio of L_m/L_i and the input line voltage [D18]-[D21]. However, the high root-mean-square (RMS) current of the switch (due to the DCM operation of the DC-DC converter) requires a high-current-rated switch and reduces the efficiency, as compared to CCM operation. The current through the switch is actually the sum of the ICS and DC-DC currents, because the ICS inductor and the DC-DC inductor are in parallel during the switch's on-time. The RMS current through the active switch in the single-stage approach is higher than the sum of the RMS current of the two switches in the two-stage approach [D6]. A switch with a high current rating is required, which reduces the efficiency as compared to that achieved in CCM operation. The third scheme is to operate L_i in CCM; if both L_i and L_m are operated in CCM, the bulk capacitor has limited stress [D22][D23]. All these phenomena are qualitatively explained in other work [D10]. The single-stage PFC converters have the following categories:

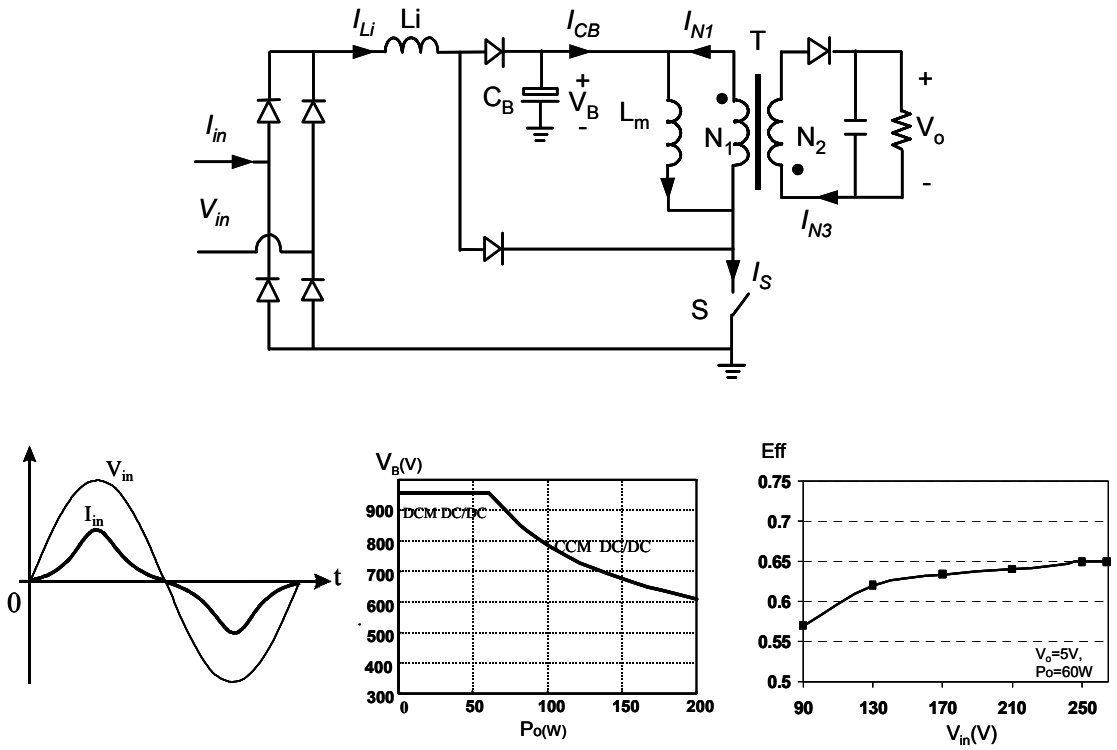


Fig. 4.12. An example of DCM S^2PFC AC-DC converters:
(a) without feedback winding and (b) with feedback winding.

a) DCM S^2PFC Converter

Other converters [D8]-[D10] [D15] employ extra coupled windings of the transformer in order to suppress the bulk capacitor voltage. The major objective here is not to achieve a high power factor; the performance and the cost are the primary concern once the input current harmonic is able to meet the IEC 1000-3-2 requirements. Converters with feedback windings can be effectively designed to have a bulk capacitor voltage of less than 450 V, which is a limitation for commercial capacitors. The multi-winding arrangement adds an additional dimension to the design of the converter. Converters [D13]-[D15] employ extra coupled windings of the coupled inductor to reduce the bulk capacitor voltage stress and the switch current stress. Although the

extra coupled windings induce input current distortion, the input current harmonics can meet the European IEC 1000-3-2 Class D requirements [D2]. The coupled-winding structure can also effectively be extended to single-stage PFC AC-DC converters with both inductors operating in CCM, as discussed in other research and analyses [D21][D23]. The multi-winding arrangement adds an additional dimension to the design of the converter. Introducing the feedback ratio as a new control dimension dramatically alleviates the bulk capacitor voltage stress, but the bulk capacitor voltage stress is still higher than 400 V for universal-line input [D25]. Although the switch current stress has been dramatically reduced with bulk capacitor voltage feedback, there is still an extra ICS current through the switch.

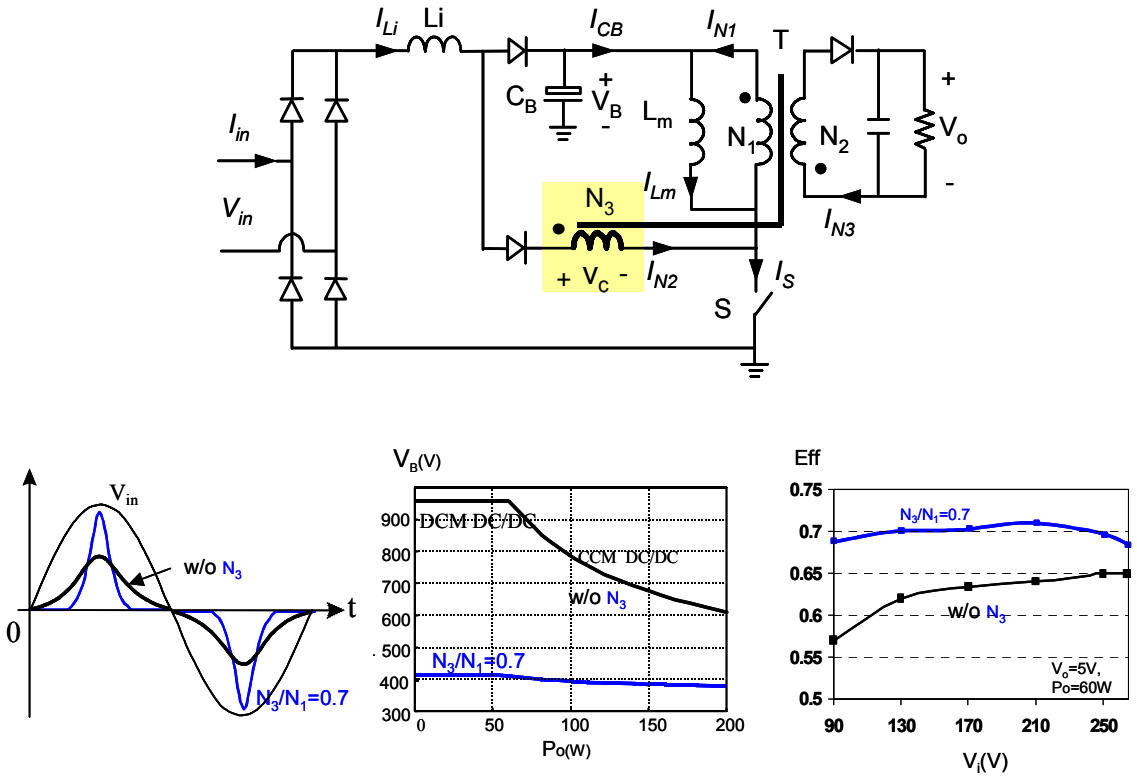
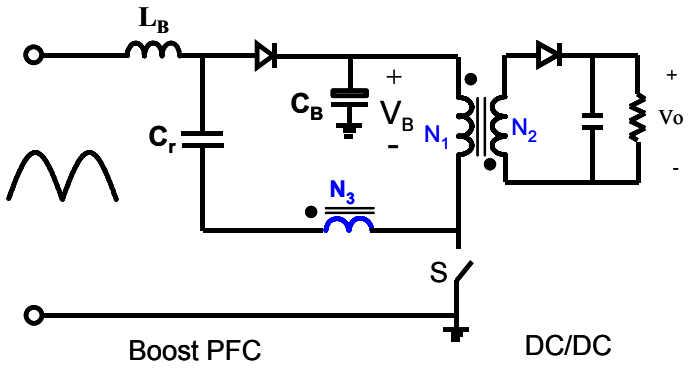
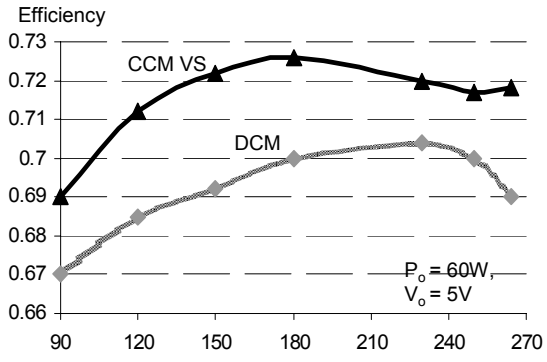


Fig. 4.13. Reducing the voltage and current stresses using a coupled winding: (a) without feedback winding and (b) with feedback winding.

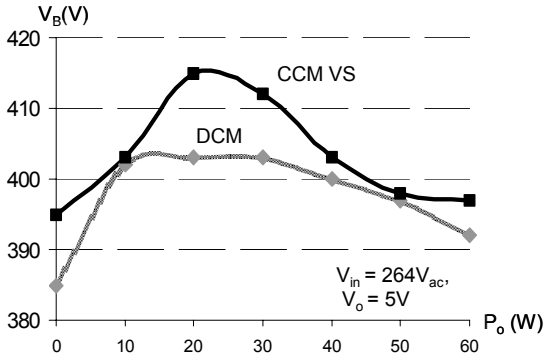
b) CCM Voltage-Source (VS) Single-Stage PFC Converter

The DCM operation of the PFC inductor of the single-stage PFC increases the current stress of the switch. Therefore, the efficiency of the DCM is low. In order to reduce the switch current stress, the voltage-source (VS) single-stage PFC converter is proposed, as shown in Fig. 4.14(a). Adding a modulation capacitor C_r changes the effective boost duty cycle on the input inductor L_B [D28]. As a result, the bulk-capacitor voltage V_B is also changed. Fig. 4.14(b)(c) illustrates the efficiency improvement and offers a comparison of the bulk capacitor voltage stress [D28].





(b)

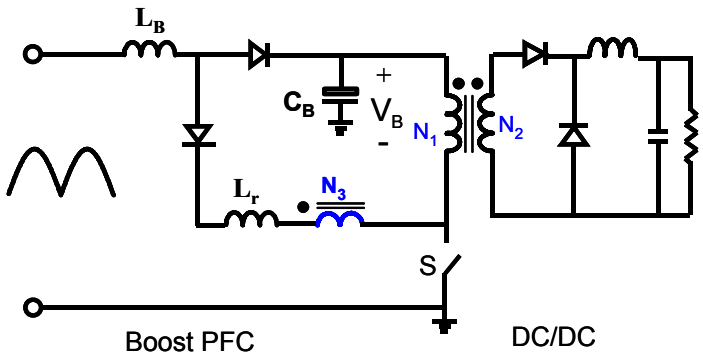


(c)

Fig. 4.14. CCM VS S^2PFC converter:
(a) the topology; (b) the comparison of the efficiency and (c) the comparison of voltage stress.

c) CCM Current-Source (CS) Single-Stage PFC Converter

Similar to the VS S^2PFC converter, adding a modulation inductor L_r changes the effective boost duty cycle of the input inductor L_B [D28]. The current-source (CS) single-stage PFC converter is shown in Fig. 4.15(a). In order to reduce the switch current stress, the bulk-capacitor voltage V_B is also changed. Fig. 4.15 (b)(c) illustrate the efficiency improvement and gives the comparison of the bulk capacitor voltage stress [D28].



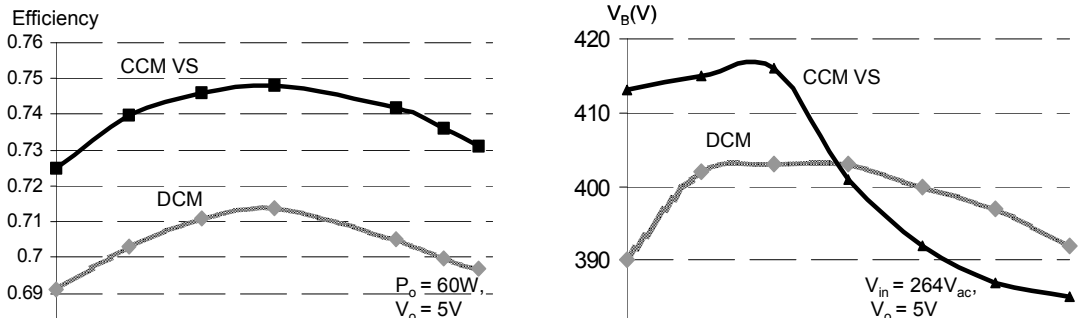
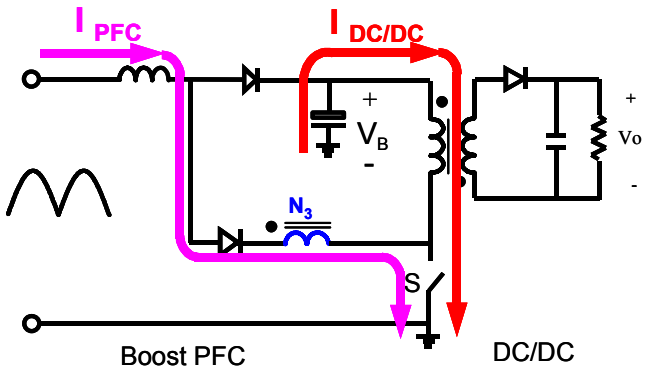


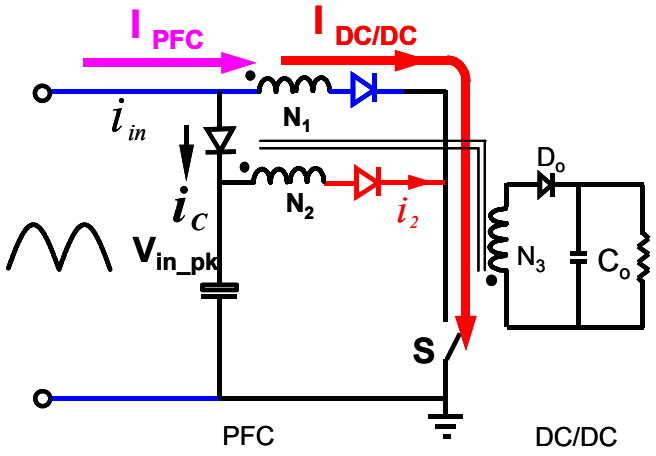
Fig. 4.15. CCM CS S^2PFC converter:
(a) the topology; (b) the comparison of the efficiency and (c) the comparison of voltage stress.

4.5.2. A New Power Flow Pattern

All current single-stage PFC converters have the same power flow pattern, which is similar to the two-stage approach, as shown in Fig. 4.16(a). But for the proposed topology, this topology structure has a different power flow pattern than the previous case, as shown in Fig. 4.16. Now the PFC current can go directly to the output. The minimized current and voltage stress are achieved because of this new power flow pattern.



(a)



(b)

Fig. 4.16. Different power flow pattern of the proposed converter:
(a) current flow pattern of existing approach and
(b) new proposed new power flow pattern for the proposed approach.

4.6. Experimental Verification

The proposed concept is verified on a 5V, 60W output, universal-line input voltage AC-DC converter. The turns of the coupled inductor are: $N_1 = 6T$, $N_2 = 28T$, and $N_3 = 3T$. After a 20μH inductor L_i is added, as shown in Fig. 4.8, the input current waveform is shaped much more effectively at high line. The experimental results are given in Fig. 4.17. As can be seen, the input current harmonics meet the IEC-1000-3-2 Class D requirements with universal-line input.

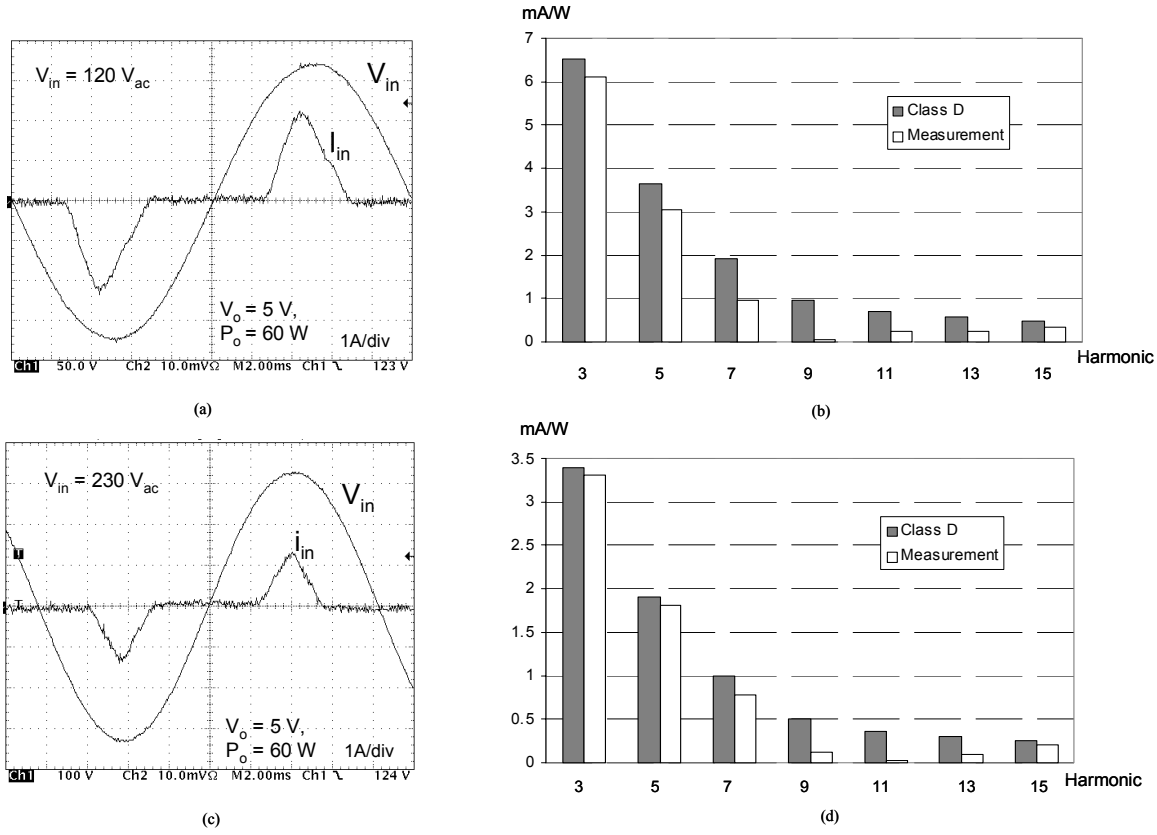
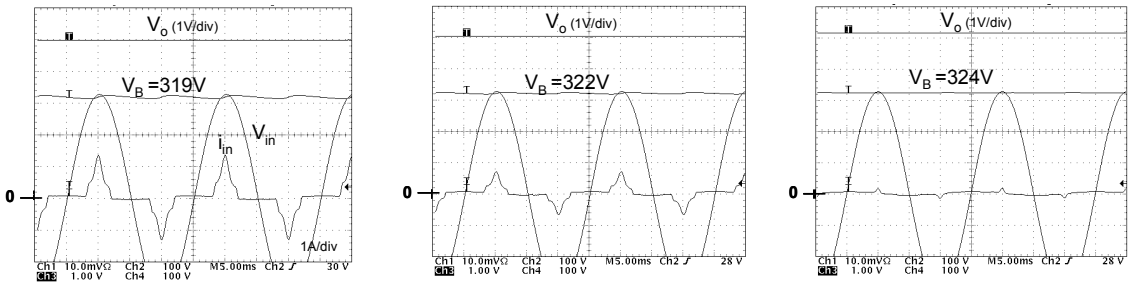


Fig. 4.17. Experimental results with L_i (20 μH):
(a) low-line voltage and current; (b) harmonic current distribution at low line;
(c) high-line voltage and current; and (d) harmonic current distribution at high line.

Fig. 4.18 shows the maximum bulk capacitor voltage stress is almost independent of the load variations. The reduced bulk capacitor voltage stress is achieved because of the new power flow pattern.

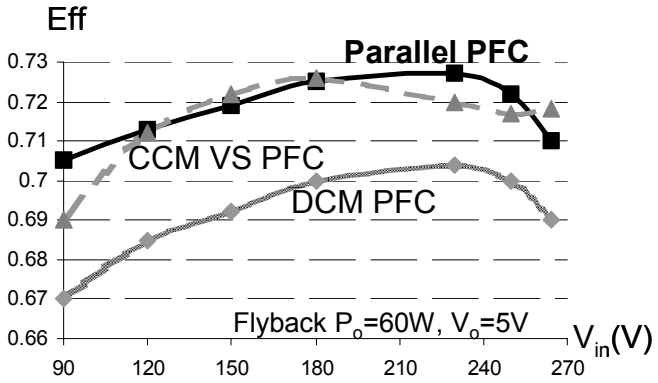


(a) (b) (c)

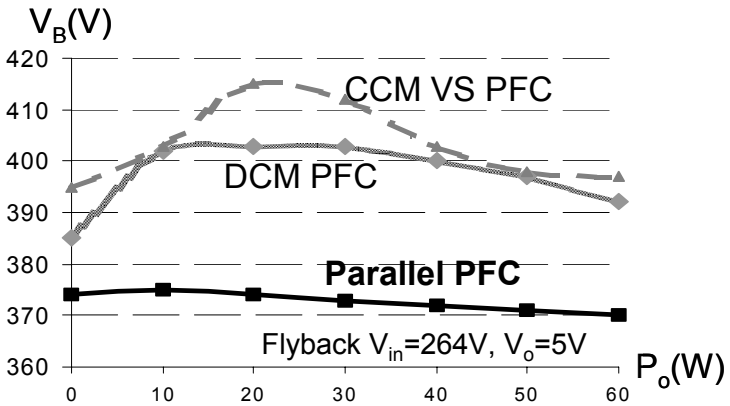
Fig. 4.18. Clamped bulk capacitor at different load conditions (Vin = 230 Vac): (a) Po = 60 W; (b) Po = 30 W; and (c) Po = 0 W.

As shown in Fig. 4.19(a), the conversion efficiency is 71.3% at low-line operation and 72.8% at high-line operation. This efficiency measurement includes consideration of the control power. Since the switch current stress is minimized, the efficiency has 2-3% improvement. Fig. 4.19(b) compares the maximum bulk capacitor voltage stress with bulk capacitor voltage feedback and load current feedback with V_{in} = 264V_{ac}. The maximum bulk capacitor voltage for the converter with bulk capacitor voltage feedback is higher than 400V, while the maximum bulk capacitor voltage for the converter with load current feedback is 375V. It is apparent that the load current feedback can control the bulk capacitor voltage more effectively.

A Forward version as shown in Fig. 4.20(a) is also built to verify the concept for comparison with the CS PFC AC-DC converter.



(a)



(b)

Fig. 4.19. Comparison of bulk capacitor with voltage source single-stage PFC converters: (a) efficiency comparison and (b) bulk capacitor voltage comparison.

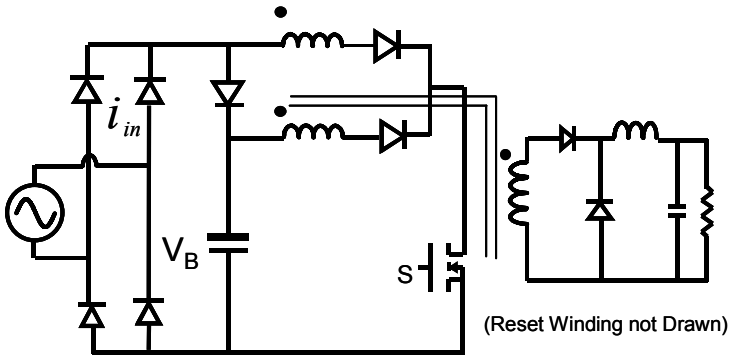
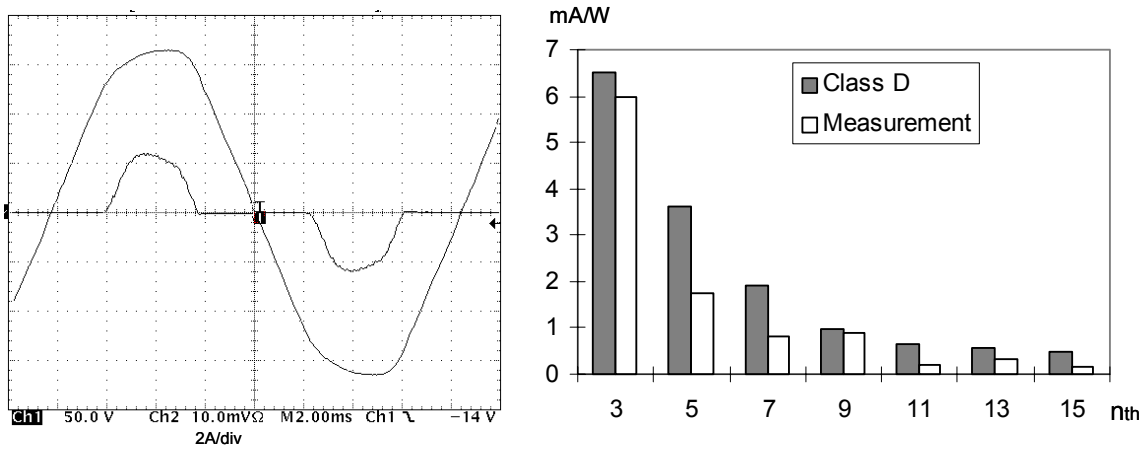
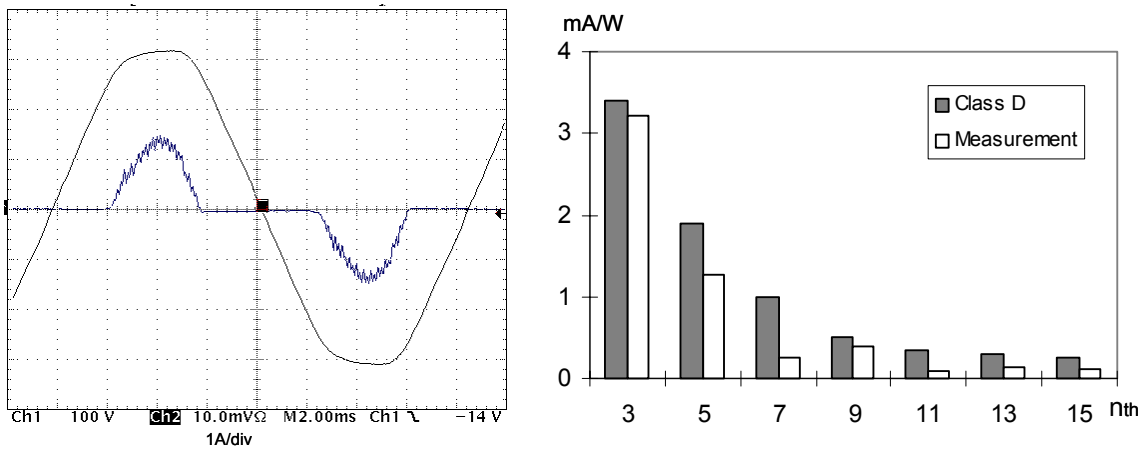


Fig. 4.20. The proposed converter using a Forward converter.

The experimental results are given in Fig. 4.21. As can be seen, the input current harmonics meet the IEC-1000-3-2 Class D requirements with universal-line input.



(a)

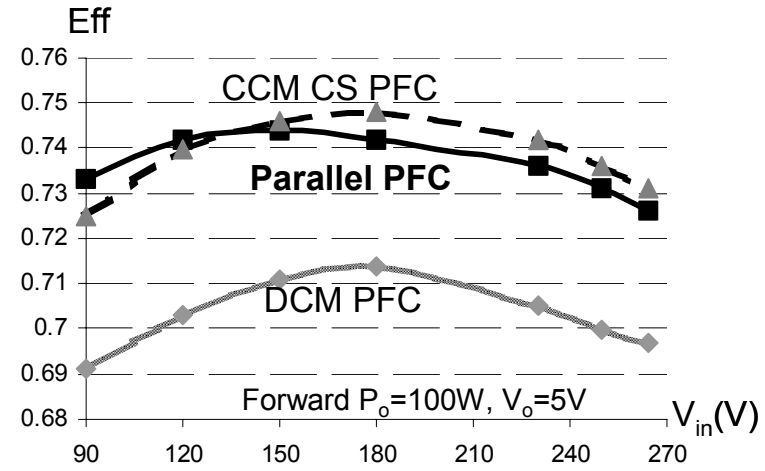


(b)

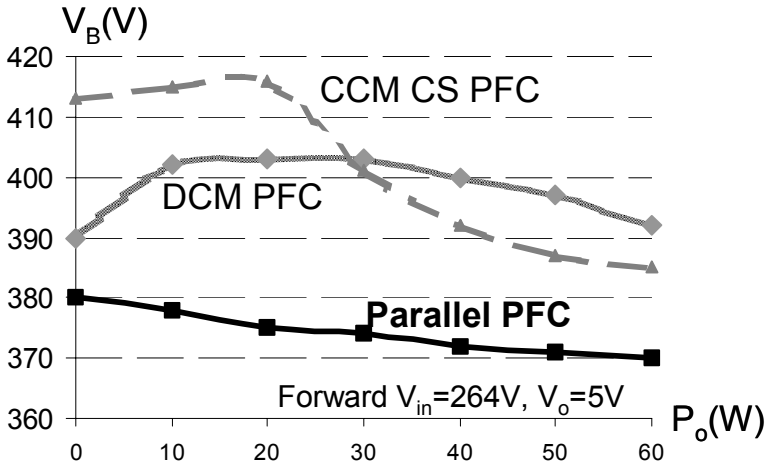
Fig. 4.21. Experimental results with P_o=100W and V_o=5V:
(a) V_{in}=120V and (b) V_{in}=230V.

The conversion efficiency is shown in Fig. 4.22 when the output voltage is 5V and the output power is 100W. Because the switch current stress is minimized, the efficiency is higher than

74%. Because of the inherent load current feedback, the bulk capacitor voltage is almost independent of the load variation, with the maximum voltage 380V.



(a)



(b)

Fig. 4.22. Comparison with the single-stage current source PFC converter: (a) efficiency comparison and (b) bulk capacitor voltage comparison.

4.7. Generalized Structure

Fig. 4.23 generalizes the topology realization of the proposed concept using different converters, in which the virtual voltage-controlled voltage sources are created by a coupled winding. The proposed concept that utilizes a coupled inductor to realize PPFC also has different realizations. We can generalize this concept as a three-terminal cell and extend it to other topologies. For non-isolation converters, the boost version as shown in Fig. 4.23(a) is an example. This converter can realize precise regulation by compromising the power factor. For isolation converters, the Flyback converter can be substituted with other isolation converters.

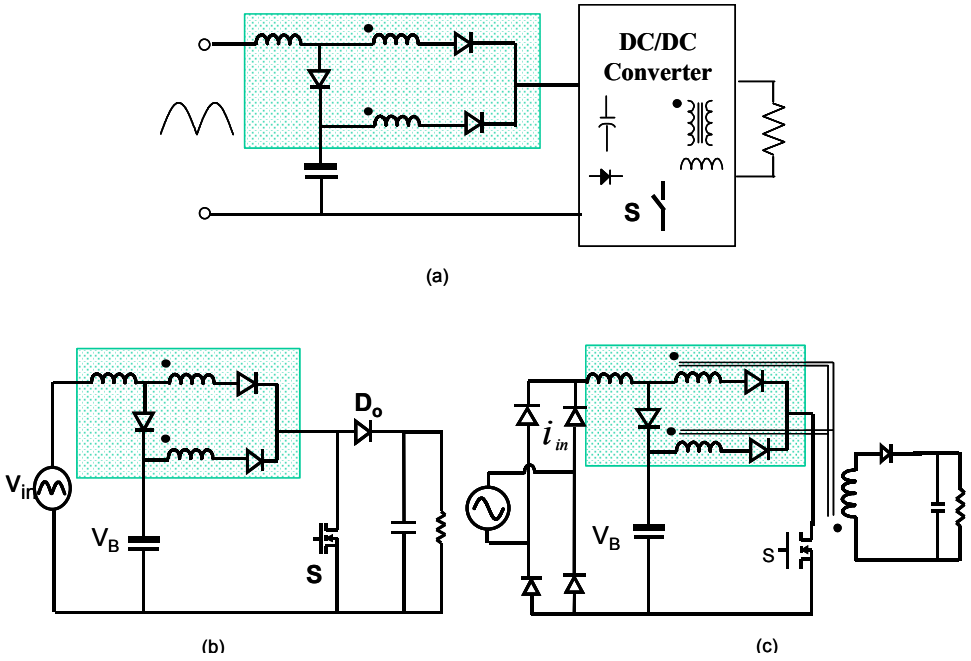


Fig. 4.23. Topology variations:
(a) general structure; (b) boost version; and (c) voltage-doubler version.

4.8. Summary

In this chapter, current path control in topologies with two input voltage sources are studied. The current path control adjusts with the line variation. The concept is demonstrated in single-switch PPFC AC-DC converters. The proposed converters have an inherent load current feedback mechanism. The concept is to create a new parallel voltage source with the rectified input voltage using the bulk capacitor voltage. The two paralleled voltage sources alternately provide power to the DC-DC converter depending on the line variations. The input power is processed once, and the bulk capacitor voltage is slightly higher than the input peak voltage regardless of load variations. Adding a boost inductor does not increase the voltage stress of the bulk capacitor at light load because the converter has the inherent load current feedback. Unlike the voltage feedback, which reduces the input power by shrinking the duty ratio at light load, the proposed load current feedback can automatically reduce the input power. Both voltage stress of the bulk capacitor and the current stress of the switch are minimized.

The input current harmonics of an AC-DC converter with universal-line input and 5V, 60W output meet the IEC-1000-3-2 Class D requirements. The conversion efficiency is higher than 71.5%. A Forward converter with universal-line input and 5V, 100W of output meet the IEC-1000-3-2 Class D requirements. The conversion efficiency is higher than 74%. The proposed concept can be easily extended to other AC-DC converters with different DC-DC topologies.

Chapter 5.

Conclusion and Future Work

5.1. Conclusion

This dissertation presents the derivation, analysis and application issues of advanced topologies with coupled inductors. The proposed innovative solutions can achieve significant performance improvements over the state-of-the-art technology.

In power conversion with large conversion ratios, the basic topologies suffer from extreme duty ratios and severe rectifier reverse recovery. Utilizing coupled inductors is a simple solution to avoid extreme duty ratios. Unfortunately, the leakage inductance of the coupled inductor induces severe voltage stress and losses. The use of a dissipative snubber or the active-clamp schemes can reduce the voltage stress, but with the penalty of either high loss or complex topology. None of the solutions take advantage of the fact that the applications do not require isolation. In this dissertation, the non-isolation coupled-inductor converters are first derived from the isolation ones. Then the active-clamp scheme is applied to the non-isolation coupled-inductor converters. The analysis shows that the active-clamp switch can be eliminated because there is an existing discharge path for the clamp capacitor, consisting of the secondary winding and the output rectifier. A novel and simple leakage-recovery scheme is proposed that achieves a level of operation similar to that of the active-clamp scheme, but with a better performance. The new schemes utilize one additional diode and one coupled winding instead of an active switch in

order to realize the clamp function. By adding a small capacitor, the leakage energy is recovered in such a way as to generate only a low level of circulating energy, and the switch voltage stress is significantly reduced. Meanwhile, the rectifier current decrease rate is controlled by the leakage inductance of the coupled inductor. The rectifier reverse-recovery problem is alleviated. Due to the effective leakage-energy recycling and the alleviated rectifier reverse-recovery problem, a significant performance improvement can be achieved. Experimental results closely match both the theoretical analysis and the efficiency prediction. The proposed concept is then generalized as a coupled-inductor switching cell. Manipulation of the switching cell for equivalent versions generates new topologies suitable for other applications.

The concept that utilizes coupled inductors to alleviate rectifier reverse recovery is then extended and new topologies suitable for other applications are generated. The rectifier reverse-recovery problem dramatically degrades the efficiency of CCM PFC boost converter and the extreme duty ratio is not a concern. The new topologies with the equivalent coupled-inductor switching cell but using a different leakage recovery scheme, as presented in Chapter 2, are good candidates. These topologies can utilize the coupled inductor to alleviate the rectifier reverse recovery, while the input current remains in CCM. Utilizing coupled inductors instead of an active switch or a complex circuit can result in a simple topology structure. The proposed solution requires only one additional winding of the boost inductor and one additional rectifier. During the switch turn-off periods, the current through the original boost rectifier is completely shifted to a new branch. The original boost rectifier is naturally recovered. When a switch turns on, the current decrease rate *di/dt* through the rectifier in the new branch is controlled. Therefore, the rectifier reverse-recovery problem is alleviated. On one hand, the leakage inductance controls

the di/dt of the output rectifier to alleviate the rectifier reverse-recovery problem; on the other hand, the leakage inductance can induce severe parasitic resonance with the diode capacitance. Two ways to handle this resonance are analyzed and verified. The CCM PFC front-end converters are overwhelmingly used for telecommunications and server applications. The current trend is to develop a low-profile, high power-density front-end converter. The proposed method was verified on a 1U 1200W PFC AC-DC front-end converter with a high power density of 11W/inch^3. By adopting the proposed concept, a power density improvement of 150% and a profile reduction of 30% can be achieved. Compared with active and other passive solutions, the proposed approach is cost-effective, and incurs no extra voltage or current stress. The concept can be easily applied to other topologies.

Further study of the coupled inductor switching cell can lead to new topologies. The new topologies can realize single-stage PPFC. PPFC only processes a small portion of the output power twice, which brings the potential benefit of efficiency improvement. The state-of-the-art single-stage PFC converters suffer from switching current and bulk capacitor voltage stress problems. The proposed converters have an inherent load current feedback mechanism that can overcome these drawbacks. The concept is to create a new parallel voltage source with the rectified input voltage using the bulk capacitor voltage. The two paralleled voltage sources alternately provide power to the DC-DC converter, depending on the line variations. The input power is processed once and the bulk capacitor voltage is slightly higher than the input peak voltage regardless of load variations. Adding a boost inductor does not increase the voltage stress of the bulk capacitor at light load because the converter has the inherent load current feedback. Unlike the voltage feedback, which reduces the input power by shrinking the duty ratio at light

load, the proposed load current feedback can automatically reduce the input power. Both the voltage stress of the bulk capacitor and the current stress of the switch are minimized. Experimental results and comparisons with the CCM, VS and CS single-stage PFC converters verify the advantages of the proposed concepts.

5.2. Future Work

In this dissertation, advanced topologies have been proposed for different applications. Significant performance improvement can be achieved. Due to the efficiency improvement, the thermal condition of the semiconductor devices is improved.

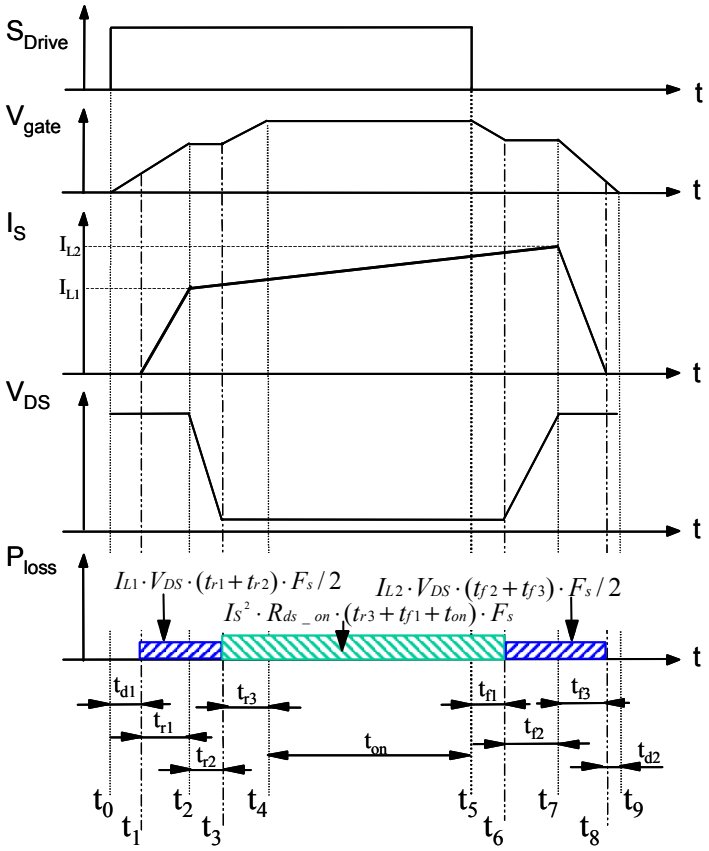
The future trend is for low profile, high power density in front-end PFC converters. The improvement of thermal conditions provides the possibility that the operation frequency could be pushed further to increase the power density for front-end PFC converters. Increasing the switching frequency makes the magnetic component smaller, but the extent of the benefit needs further investigation. This research should incorporate the study of the impact of increasing switching frequency on the EMI filter. Another thought is that the proposed converters need an extra rectifier and passive components, integration of the passive component would also help to reduce the footprint of the converter.

The design of the single-stage PPFC is mainly based on the simulation because no analytical expression of the input current and the bulk capacitor voltage can be obtained. Further study of the parallel power converters and the design optimization, as well as the comparison of the state-of-the-art single-stage converters, would be an interesting research topic.

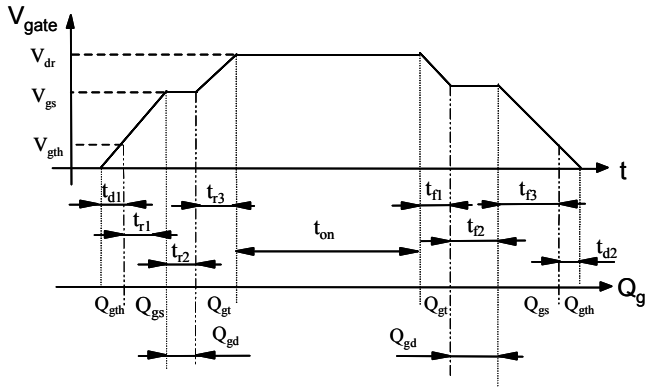
Appendix A.

Topology Evaluations for the Front-End Converter of a HID Ballast

It is important to evaluate different topologies based on the loss breakdown. The loss analysis is based on the switching performance of a MOSFET [A4]. Fig. A1 shows the switching performance of a MOSFET and the charge during the turn-on and turn-off.



(a)



(b)

Fig. A1.Typical waveforms of a MOSFET in a switching cycle:
(a) the timing of switching action and (b) the charge and discharge related to the switching action.

As can be seen, the switching loss during turn-on and turn-off can be given by Eq. A1 and Eq. A2:

$$P_{\_on} = I_{L1} \cdot V_{DS} \cdot (t_{r1} + t_{r2}) \cdot F_s / 2 \text{ , and} \qquad \text{Eq. A1}$$

$$P_{\_off} = I_{L2} \cdot V_{DS} \cdot (t_{f2} + t_{f3}) \cdot F_s / 2 . \qquad \text{Eq. A2}$$

The conduction loss of the switch is given by Eq. A3:

$$P_{\_Ron} = I_S{}^2 \cdot R_{ds\_on} \cdot (t_{r3} + t_{f1} + t_{on}) \cdot F_s . \qquad \text{Eq. A3}$$

The timing during the switch turn-on could be calculated as follows:

$$t_{r1} = \frac{Q_{gs} - Q_{gth}}{V_{gs} - V_{th}} \cdot R_g \cdot \ln(\frac{V_{dr} - V_{gth}}{V_{dr} - V_{gs}}) \text{ , and} \qquad \text{Eq. A4}$$

$$t_{r2} = \frac{Q_{gd} \cdot R_g}{V_{dr} - V_{gs}} . \qquad \text{Eq. A5}$$

After the gate drive signal is removed, the turn-off timing is as follows in Eq. A6, Eq. A7, and Eq. A8:

$$t_{f1} = \frac{Q_{gt} - Q_{gs} - Q_{gd}}{V_{dr} - V_{gs}} \cdot R_g \cdot \ln(\frac{V_{dr}}{V_{gs}}), \quad \text{Eq. A6}$$

$$t_{f2} = \frac{Q_{gd} \cdot R_g}{V_{gs}}, \text{ and} \quad \text{Eq. A7}$$

$$t_{f3} = \frac{Q_{gs} - Q_{gth}}{V_{gs} - V_{th}} \cdot R_g \cdot \ln(\frac{V_{gs}}{V_{gth}}). \quad \text{Eq. A8}$$

The gate charge information can be found from the data sheet of the devices, and thus the loss analysis can be conducted by a Mathcad program.

Appendix B.
Capacitor Shift Rule

Fig. B1(a) shows a circuit that consists of sub-circuits A and B. In sub-circuit B, there is no circuit element whose value is dependent on the capacitor voltage or the current through the DC voltage source. Then the capacitor can be transformed by shifting the capacitor through the voltage source, as shown in Fig. B1(b). This shift will not affect circuit operation. The changes associated with the circuit variables are the capacitor voltage and the current through the DC voltage source.

Assume the voltage of the capacitor voltage and the current through the voltage source V_E in Fig. B1(a) are as the follows:

$V_{C1}\big|_{t=0} = V_{Co}$, and

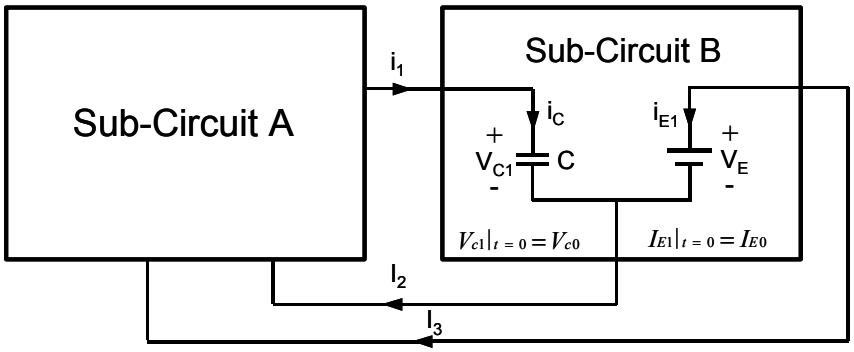
$I_{E1}\big|_{t=0} = I_{Eo}$.

Shifting the capacitor as shown in Fig. B1(b) does not affect the circuit operation, but the capacitor voltage and the current through the DC voltage source are changed. The capacitor voltage is changed by the magnitude of the DC voltage source V_E and the current through the DC voltage source is altered by that of the current through the capacitor, such that:

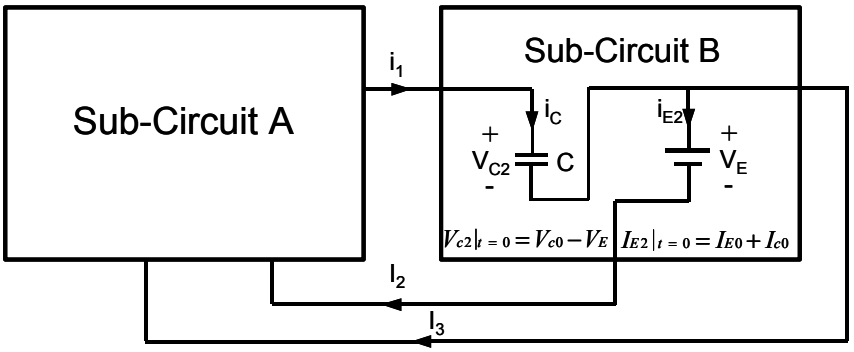
$V_{C2}\big|_{t=0} = V_{Co} - V_E$, and

$I_{E2}\big|_{t=0} = I_{Eo} + I_{C0}$.

Utilizing the capacitor-shifting rule can generate different topology variations. By applying the capacitor shift rule, many topologies can be found equivalent.



(a)



(b)

Fig. B1. Capacitor-shifting rule.

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